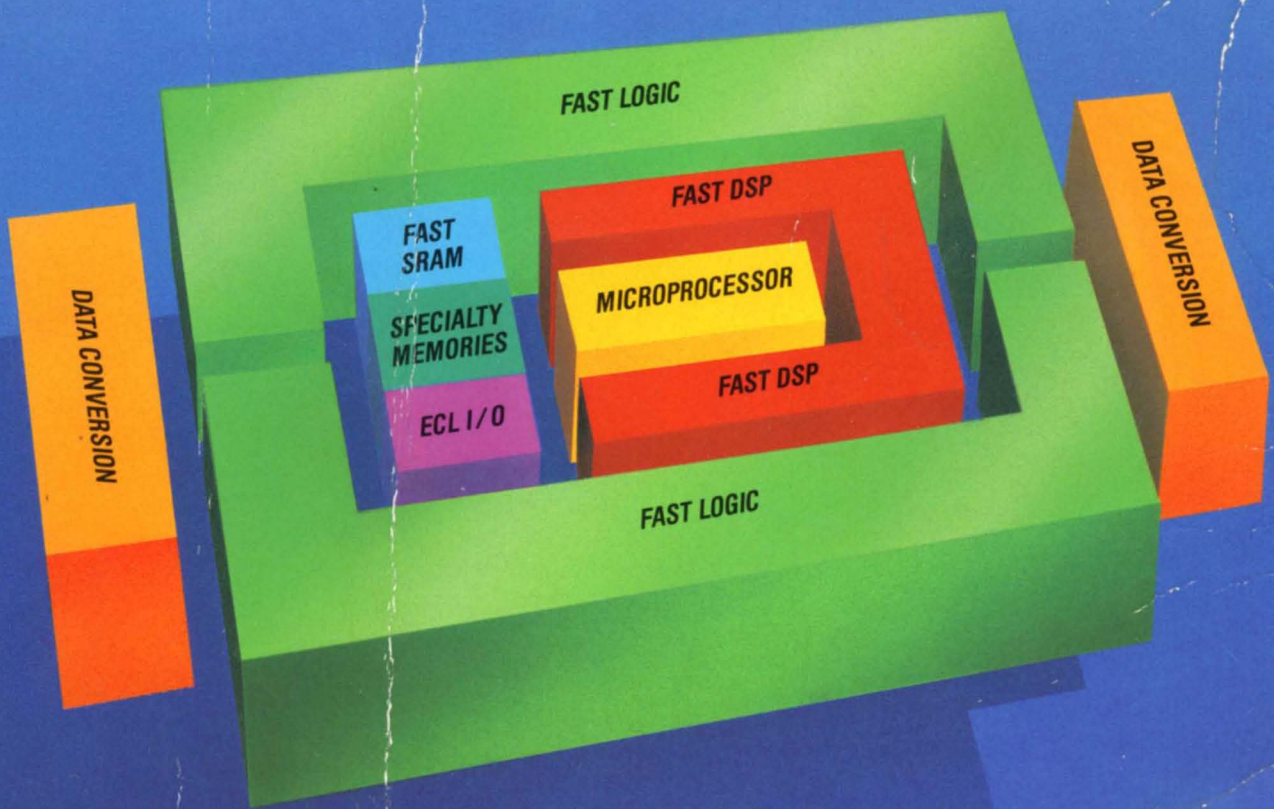
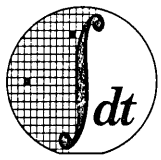
Integrated
Device Technology

High Performance CMOS
DATA BOOK SUPPLEMENT
1989





Integrated Device Technology, Inc.

HIGH-SPEED CMOS DATA BOOK

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CONTENTS OVERVIEW

Integrated Device Technology's Data Book Supplement is comprised of new/revised data sheets, application notes and package drawings to its 1988 Data Book. Only new or revised data sheets are contained in the supplement. The data sheets for those products whose specification have not changed are in the 1988 Data Book. Customers, with **both** the Data Book Supplement and 1988 Data Book, now have a complete specification set of IDT's advanced CMOS products.

The supplement's table of contents contains a listing of all of IDT's products. Products which are in the supplement will have their page number listed as "Sx-yy", where:

S = data sheet is in supplement
x = section where data sheet resides
yy = page number within the section

Products which are **boldfaced,** and have their page numbers listed as "x-yy", can be found in the 1988 Data Book.

The block diagram on the cover of this book pictorially illustrates the multiple product lines offered by Integrated Device Technology, a recognized leader in high-speed CMOS technology. IDT's broad line of products enables us to provide a complete CMOS solution to designers of high-performance digital systems. Our products include industry standard devices as well as products with speed, lower power, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information: Start with the Ordering Information chart at the back of each data sheet, or Cross Reference Guides (p S1-23) along with Package Diagram Outline Index (p S15-3), to compose the complete IDT part number. Reference data on our Technology Capabilities and Quality Commitments are included in separate sections (S2, S3, respectively).

Use this book to find product data: Start with the Table of Contents, organized by product line (p Sii), or with the Numeric Table of Contents across all product lines (p Sxiv); for a more complete summary of product line offerings, use the Product Selector Guide (p S1-2). These indexes will direct you to the page on which the complete technical data sheet can be found, and may in some cases refer you to related Application or Technical Notes (p S14-1). Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY—contain descriptions for products soon to be or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Product Selector and Cross Reference Guides

IDT PACKAGE MARKING DESCRIPTION

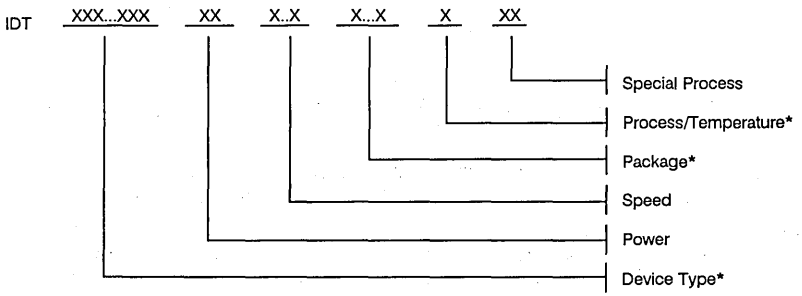
1

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, on ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two alpha characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or tolerance (RT).

Example:



* Field Identifier Applicable To All Products

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly and are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

IDT High-Speed CMOS Products Common Features

- Fabricated with IDT's advanced CEMOS™ dual-well, oxide-isolated, ion-implanted technology with feature sizes down to submicron.
- Proprietary ESD protection circuitry is designed into all inputs and outputs to ensure that they will withstand repeated applications of ESD stress and do not exhibit the degradation found in many other MOS or bipolar products.
- IDT products are designed, manufactured and tested to the highest standards of quality and reliability
  — they begin with stringent design rules derived for use in high-reliability programs
  — they are manufactured with a dedicated commitment to reliable workmanship
  — rigid controls are employed throughout wafer fab, device assembly and test
- All military grade products are manufactured in compliance with the latest revision of MIL-STD-883, Class B.
- Military module assemblies are constructed using screened IDT monolithic products and receive additional burn-in and electrical test screening to assure package integrity and mechanical reliability.
- Monolithic products are available in ceramic and plastic packages. The various packages available are DIPs, Pin Grid Arrays, LCCs, SOICs and Flatpacks
- All products operate from a single 5V power supply.
- Inputs and outputs, depending on the product, are directly TTL, CMOS or ECL-compatible.
- Alpha-particle induced soft error protection for static RAMs.
- Latch-up protection circuitry.

High-Speed CMOS Radiation Hardened Products

- Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products available. Parameters/Speed options of IDT's military product data sheets are applicable for most 'RT & 'RE devices (consult factory).
- IDT has purchased/installed equipment for Total Dose testing. The IDT Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level. Only wafers with sampled die that pass Total Dose level test are assembled and used for order (consult factory for more details on Total Dose sample testing).
- Radiation Enhanced devices processed on Epi wafers are qualified by IDT's Total Dose test plan sample die testing of 10K Rads Total Dose [RADs(Si)] or greater (consult factory for higher Total Dose levels).
- Radiation Tolerant devices are qualified by IDT's Total Dose plan sample die testing of 10K Rads Total Dose [RADs(Si)].
- Manufactured in compliance with the latest revision of MIL-STD-883, Class B or Class S.

Key

Boldface indicates an improved IDT feature.

The availability column shows the above date when limited production quantities will be available.

CALL in the data book page column means that the data sheet has not been included in the data book; a copy, when available, may be obtained from IDT or from its sales offices.

High-Speed CMOS RISC Microprocessor Family

- Highest performance CMOS RISC processors available
- Flexible architecture can be tailored to wide set of price/performance needs
- Applications range from embedded control to multi-processing systems
- Efficient pipelining assists in obtaining an execution rate of one instruction per cycle
- Optimizing compilers for C, Pascal, FORTRAN, Ada, PL/1, and Cobol
- R2000A and R3000 are code compatible
- Floating Point Accelerator conforms with IEEE 754-1985 standard
- Write-Buffer enhances CPU performance by allowing memory "write-through" during run cycles
- R2000A available in 12.5 and 16.7MHz clock rates
- R3000 available in 16.7, 20, and 25MHz clock rates

Part Number	Description	Typical Power (mW)	Avail.
IDT79R3000	RISC CPU Processor, 20 mips @ 25MHz, On-chip Cache Control, Memory Management Unit, 64-Entry Translation Lookaside Buffer, Thirty-two 32-bit General Purpose Registers	1500	NOW
IDT79R3010	RISC Floating-Point Accelerator, 7 MFLOPS single precision LINPACK, 4 MFLOPS double precision LINPACK	2000	NOW
IDT79R3020	RISC CPU Write Buffer	100	NOW
IDT79R2000A	RISC CPU Processor, 10 mips @ 16.7MHz, On-chip Cache Control, Memory Management Unit, 64-entry Translation Lookaside Buffer, Thirty-two 32-bit General Purpose Registers	1500	NOW
IDT79R2010A	RISC Floating-Point Accelerator, 4 MFLOPS single precision LINPACK, 2 MFLOPS double precision LINPACK	2000	NOW
IDT79R2020A	RISC CPU Write Buffer	100	NOW

R3000/2000A Development Systems

Model Number	Description	Avail.
7RS201*	R3000 NuBus Card for Macintosh, Code development and debugging environment for single-user	Q2'89
8104**	M/120-3 Mid-range multiple user development system. Rated at 9 mips processing power with 12.5MHz CPU	NOW
8102	M/120-5 Same as 8104 except rated at 12 mips with 16.7MHz CPU	NOW
8305	M/2000-6 High-end multi-user development system with 20MHz R3000 CPU	NOW
8302	M/2000-8 Same as 8305 except rated at 20 mips with 25MHz CPU	

* Note: All development systems (NuBus Card and M/Series) come standard with RISC/os (UNIX) and C compiler software.
** Note: Additional memory, disk peripherals, tape peripherals and interface options are available from IDT.

R3000/2000A Software

Model Number	Description	Avail.
3103C-E	FORTRAN RISCompiler and runtimes	NOW
3104C-E	Pascal RISCompiler and runtimes	NOW
3105C-E	COBOL RISCompiler and runtimes	NOW
3106C-E	Ada RISCompiler and runtimes	NOW
3107C-E	PL/1 RISCompiler and runtimes	NOW
3120C-SCR	System Programmer's Package (SPP) Source license and software	NOW

Integrated RISC Solutions

IDT is committed to provide a complete Integrated RISC Solution by combining expertise in silicon process technology with leadership products in development systems and software. Long an industry leader in producing the fastest Static RAMs for cache memory application and high speed logic for memory interface, IDT also offers a low-cost development system for R3000 designs. An R3000 CPU board that is hosted in the Macintosh II (P/N IDT7RS201) comes complete with RISC/os (Mips UNIX operating system), the C language compiler, and debugging software tools.

IDT Components for Cache and Memory Interface

IDT offers a broad range of cache RAMs and high-speed logic to complement the R2000/R3000 RISC components and provide a fully integrated approach to RISC design. SRAMs available include densities from 16K to 1 Megabit and feature access times as low as 20 nanoseconds (ns) for standard CMOS and 10ns for BiCEMOS/ECL SRAMs.

Devices specifically developed for RISC systems include IDT's new 71586 4K by 16 latched SRAM. This combination device helps eliminate propagation delay in the cache-logic interface and thereby boost system speed. These standard and proprietary devices can be configured by cache size and speed to match a wide variety of applications from embedded control to high-performance workstations. IDT components typically used for cache and memory interface in the R3000 system include:

Cache Memory	• IDT6116	2K x 8 SRAM	20ns Access Time
	• IDT71586	4K x 16 Latch/SRAM	35ns Access Time
	• IDT7198	16K x 4 SRAM	20ns Access Time
	• IDT7164	8K x 8 SRAM	25ns Access Time
	• IDT71258	64K x 4 SRAM	25ns Access Time

Bus Interface Logic	• IDT74FCT373A	Octal Latch
	• IDT74FCT374A	Octal Register
	• IDT74FCT240A	Octal Buffer
	• IDT74FCT244A	Octal Buffer
	• IDT74FCT646A	Bi-directional Latch
	• IDT74FCT823A	9-bit Register

RISC Subsystem Modules and Peripheral Support

IDT is introducing a number of R3000 CPU subsystem modules as well as high-speed SRAM cache-modules targeted for RISC-based systems. These surface mount modules decrease motherboard complexity and thereby decrease overall system cost. Because IDT modules and their components are fully tested, the need for component testing is eliminated. All individual components are selected and tested for their sub-system speed-timing compatibility. Modules also expedite system development and therefore decrease time-to-market.

RISC Modules and Peripheral Components

Peripheral Support	• IDT49C460	32-bit EDC
	• IDT49C465	32-bit FLOWTHRU — EDC™
	• IDT7252	Bi-directional FIFO Peripheral Interface Card (32-bit bus to 8-bit bus)
Cache Memory Modules	Standard Versions:	
	• IDT7MB6039	Dual 16K x 60
	• IDT7MB6042	Dual 8K x 60
	• IDT7MB6044	Dual 4K x 60
	Multi processing:	
	• IDT7MB6049	Dual 16K x 60
	• IDT7MB6051	Dual 8K x 60
CPU Communication Devices	• IDT7202	1K x 9 FIFO
	• IDT7203	2K x 9 FIFO
	• IDT7204	4K x 9 FIFO
	• IDT7205	8K x 9 FIFO (in development)
	• IDT7130	1K x 8 Dual-Port DRAM with interrupts
	• IDT7132	2K x 8 Dual-Port SRAM
	• IDT7133	2K x 16 Dual-Port SRAM
	• IDT7134	4K x 8 Dual-Port SRAM
	• IDT71342	4K x 8 Dual-Port with Semaphores

DESC SMD Products

- DESC SMD (Standard Military Drawing) program eliminates the need for multiple source control drawings. IC manufacturers, primes, and DOD share the same specification format. The benefits are improved availability to a military drawing, stable data sheet parameters, and a listed DESC SMD product
- DESC SMD numbers, pending or listed, for 64 IDT products
  - — SRAM
  - — DSP
  - — MICROSLICE
  - — DATA CONVERSION
  - — HIGH SPEED FCT/FCTA LOGIC
- SMD numbers for the following packages
  - — Cerpacks
  - — CERDIPS
  - — LCC
  - — Sidebraze DIPs
  - — Flatpacks
- IDT has a direct modem link to DESC to minimize turnaround time for pending SMDs

DESC SMD No.	IDT Part No.	Status
SRAM		
84036	6116	LISTED
84132	6167	LISTED
5962–86015	7187	LISTED
5962–86859	6198/7198/7188	LISTED
5962–86705	6168	LISTED
5962–85525	7164	LISTED
5962–88552	71256	LISTED
5962–88611	71682L	LISTED
5962–88662	71256S	LISTED
5962–88681	71258S	LISTED
5962–88545	71258L	LISTED
5962–88544	71257L	LISTED
5962–88725	71257S	LISTED
5962–89524	61298L	PENDING
5962–88740	6116	PENDING
SMP		
5962–86875	7130/7140	LISTED
5962–87002	7132/7142	LISTED
5962–88610	7133S/7143S	LISTED
5962–88665	7133L/7143L	LISTED
DSP		
5962–87531	7201LA	LISTED
5962–86873	7216L	LISTED
5962–86846	72404	LISTED
5962–87686	7217L	LISTED
5962–88669	7203S	PENDING
5962–89536	7202L	PENDING
5962–88733	7210	PENDING
5962–89523	72403L	PENDING
MICROSLICE		
5962–87708	39C10B/C	LISTED
5962–88535	39C01C/D	LISTED
5962–88533	49C460A/B	LISTED
5962–88613	39C60/A	LISTED

DESC SMD No.	IDT Part No.	Status
MICROSLICE (continued)		
5962–88643	49C410/A	LISTED
5962–89517	49C402/A	PENDING
DCP		
5962–88743	75C48	LISTED
LOGIC		
5962–87630	54FCT244/A	LIST/PEND
5962–87629	54FCT245/A	LIST/PEND
5962–86862	54FCT299	LISTED
5962–87644	54FCT373/A	LISTED
5962–87628	54FCT374/A	PENDING
5962–87627	54FCT377/A	LIST/PEND
5962–87654	54FCT138/A	LIST/PEND
5962–87655	54FCT240/A	LIST/PEND
5962–87656	54FCT273/A	LIST/PEND
5962–87704	54FCT861	PENDING
5962–87667	54FCT827A/B	PENDING
5962–88575	54FCT841	PENDING
	54FCT533	PENDING
	54FCT182/A	PENDING
5962–88608	54FCT821/A	LISTED
	54FCT645	PENDING
	54FCT640	PENDING
	54FCT534	PENDING
5962–88543	54FCT521/A	PENDING
5962–88675	54FCT845A/B	LISTED
5962–88640	54FCT161/A	LIST/PEND
5962–88639	54FCT573	LISTED
5962–88656	54FCT823A/B	LISTED
5962–88657	54FCT163/A	LISTED
5962–88674	54FCT825A/B	LISTED
5962–88661	54FCT863A/B	PENDING
5962–88736	29FCT520A	PENDING
	54FCT646	PENDING
	54FCT139/A	PENDING
	54FCT824	PENDING

High-Speed CMOS Static RAMs

- Extremely fast access times
- Low power consumption
- 2V data retention battery backup on all low-power devices
- Three-state outputs
- Available in military and commercial temperature ranges

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
MONOLITHIC					
IDT6167	16K (16K x 1)	20	15	225	NOW
		15	**12**	225	Q2'89
IDT6168	16K (4K x 4)	25	20	225	NOW
		20	**15**	275	Q2'89
		15	**12**	300	Q2'89
IDT71681	16K (4K x 4) with separate data inputs and outputs; outputs track inputs during write mode	25	20	225	NOW
		20	**15**	300	Q2'89
		15	**12**	300	Q2'89
IDT71682	16K (4K x 4) with separate data inputs and outputs; outputs in high-impedence state during write mode	25	20	225	NOW
		20	**15**	300	Q2'89
		15	**12**	300	Q2'89
IDT6116	16K (2K x 8)	25	20	225	NOW
		25	15	275	NOW
IDT7187	64K (64K x 1)	**25**	**20**	250	Q3'89
		20	**15**	300	Q4'89
IDT7188	64K (16K x 4)	**25**	**20**	300	Q3'89
		20	**15**	350	Q4'89
IDT6198	64K (16K x 4) with output enable ($\overline{OE}$) for added system flexibility	**25**	**20**	300	Q3'89
		20	**15**	350	Q4'89
IDT7198	64K (16K x 4) output enable ($\overline{OE}$) and second chip select ($\overline{CS_2}$) for added system flexibility and memory control	**25**	**20**	300	Q3'89
		20	**15**	350	Q4'89
IDT71981	64K (16K x 4) with separate data inputs and outputs; outputs track inputs during write mode	**25**	**20**	300	Q3'89
		20	**15**	350	Q4'89
IDT71982	64K (16K x 4) with separate data inputs and outputs; outputs in high-impedence state during write mode	**25**	**20**	300	Q3'89
		20	**15**	350	Q4'89
IDT7164	64K (8K x 8)	30	25	250	NOW
		25	**20**	250	Q3'89
IDT7165	64K (8K x 8) with asynchronous clear and high-speed chip select	35	30	250	NOW
		30	**25**	250	Q3'89
IDT71C65	64K (8K x 8) with CMOS compatible I/O	35	30	250	NOW
		30	**25**	250	Q3'89
IDT7186	64K (4K x 16)	45	35	300	NOW
		35	**25**	300	Q2'89
IDT71586	64K (4K x 16) with address latches	45	35	300	NOW
		35	**25**	300	Q2'89
IDT71257	256K (256K x 1)	—	35	350	NOW
		35	**30**	350	Q2'89
		35	**25**	350	Q4'89
IDT71258	256K (64K x 4)	—	35	350	NOW
		35	**30**	350	Q2'89
		35	**25**	350	Q4'89
IDT61298	256K (64K x 4) with output enable ($\overline{OE}$) for added system flexibility	**35**	**30**	350	Q3'89
		35	**25**	350	Q4'89

High-Speed CMOS Static RAMs (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT71281	256K (64K x 4) with separate data inputs and outputs; outputs track inputs during write mode	**35**	**30**	350	Q3'89
		35	**25**	350	Q4'89
IDT71282	256K (64K x 4) with separate data inputs and outputs; outputs in high-impedence state during write mode	**35**	**30**	350	Q3'89
		35	**25**	350	Q4'89
IDT71256	256K (32K x 8)	35	30	250	NOW
		35	**25**	250	Q4'89
IDT71027	1 Megabit (1024K x 1)	**45**	**35**	500	1990
IDT71028	1 Megabit (256K x 4)	**45**	**35**	500	1990
IDT71024	1 Megabit (128K x 8)	**45**	**35**	500	1990
IDT6178	16K (4K x 4) cache-tag with cache address comparator and asynchronous clear	**15**	**12**	300	Q2'89
		12	**10**	300	Q4'89
IDT61970	16K (4K x 4) with output enable ($\overline{OE}$)	**20**	**15**	300	Q2'89
		15	**12**	300	Q2'89
IDT7174	64K (8K x 8) with cache address comparator, asynchronous clear and high-speed chip select	45	35	250	NOW
		35	**25**	250	Q4'89
IDT71502	64K (4K x 16) registered RAM for writable control store use; has on-board serial load, parity, breakpoint and trace logic	**35**	**25**	350	NOW

STANDARD RAM MODULES

For additional RAM sizes and configurations from 80K to 4 Megabit, see page 9, High-Speed CMOS Module Products

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT10490	64K (64K x 1) with ECL 10K compatible I/O	15	8	420	NOW
IDT100490	64K (64K x 1) with ECL 100K compatible I/O	—	8	320	NOW
IDT10494	64K (16K x 4) with ECL 10K compatible I/O	15	8	600	Q2'89
IDT100494	64K (16K x 4) with ECL 100K compatible I/O	—	8	500	Q2'89
IDT10496RL	64K (16K x 4) with ECL 10K compatible I/O and self-timed mode (STRAM), reg. input	—	10	800	Q2'89
IDT100496RL	64K (16K x 4) with ECL 100K compatible I/O and self-timed mode (STRAM), reg. input	—	10	700	Q2'89
IDT10496LL	64K (16K x 4) with ECL 10K compatible I/O and self-timed mode (STRAM), latch input	—	10	800	2H'89
IDT100496LL	64K (16K x 4) with ECL 100K compatible I/O and self-timed mode (STRAM), latch input	—	10	700	2H'89
IDT10497	64K (16K x 4) with ECL 10K compatible I/O and synchronous-write mode	—	12	800	2H'89
IDT100497	64K (16K x 4) with ECL 100K compatible I/O and synchronous-write mode	—	12	700	2H'89
IDT10498	64K (16K x 4) with ECL 10K compatible I/O and conditional-write mode	—	12	800	2H'89
IDT100498	64K (16K x 4) with ECL 100K compatible I/O and conditional-write mode	—	12	700	2H'89

High-Speed CMOS Module Products

- High density solutions
- 'M' type ceramic RAM modules are built with monolithic RAMs in LCC packages surface mounted onto multilayered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process.
- 'MP' and 'MB' type commercial plastic modules are built using monolithic RAMs in SMD plastic packages, surface mounted onto epoxy laminate (FR4) substrates.
- 'MC' type ceramic SIP modules are constructed using monolithic RAMs in LCC packages on a vertically mounted substrate. This packaging configuration allows for very low profile modules with high packing density.
- Custom solutions are available to achieve the optimum system integration and performance.

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
STANDARD RAM MODULES					
IDT8MP628	128K (8K x 16) plastic SIP RAM module	—	**35**	825	NOW
IDT8M628	128K (8K x 16) RAM module with monolithic pinout	**45**	**35**	825	NOW
IDT7MP156	256K (256K x 1) plastic SIP RAM module	—	25	600	NOW
IDT7MC156	256K (256K x 1) static RAM module (ceramic SIP)	**35**	25	600	NOW
IDT7MP456	256K (64K x 4) plastic SIP RAM module	—	25	1200	NOW
IDT7M856	256K (32K x 8) RAM module with monolithic pinout	**40**	**30**	950	NOW
IDT8M856	256K (32K x 8) RAM module with monolithic pinout (low-power)	**45**	**35**	350	NOW
IDT7MC4005	256K (16K x 16) static RAM module (ceramic SIP)	**35**	25	2235	NOW
IDT8MP656	256K (16K x 16) plastic SIP RAM module	—	**35**	825	NOW
IDT8M656	256K (16K x 16) RAM module with monolithic pinout	**45**	**35**	825	NOW
IDT7M656	256K (16K x 16, 32K x 8, 64K x 4) RAM module customer configurable organization	**25**	**20**	3200	Q2'89
IDT7M812	512K (64K x 8) RAM module offering maximum addressable memory required by 8-bit MPs	35	25	2400	NOW
IDT7M912	512K (64K x 8) RAM module offering maximum addressable memory required by 8-bit MPs with parity	35	25	2700	NOW
IDT8MP612	512K (32K x 16) plastic SIP RAM module	—	40	875	NOW
IDT8M612	512K 932K x 16) RAM module with monolithic pinout	**50**	40	750	NOW
IDT7MC4032	512K (16K x 32) RAM module with separate I/O (ceramic dual SIP)	**35**	25	1400	NOW
IDT7MC4001	1 Megabit (1024K x 1) static RAM module (ceramic SIP)	TBD	45	675	NOW
IDT8MP824	1 Megabit (128K x 8) plastic SIP RAM module	—	40	500	NOW
IDT8M824	1 Megabit (128K x 8) RAM module with monolithic pinout	50	40	550	NOW
IDT8MP624	1 Megabit (64K x 16) plastic SIP RAM module	—	40	875	NOW
IDT8M624	1 Megabit (64K x 16) RAM module with monolithic pinout	50	40	875	NOW
IDT7M624	1 Megabit (64K x 16, 128K x 8, 256K x 4) RAM module — customer configurable organization	35	25	4800	NOW

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT7MB4009	512K (2 x 16K x 16) dual banked plastic RAM QIP module	—	25	3100	NOW
IDT7M4017	2 Megabit (64K x 32) RAM module	50	40	6200	NOW
IDT7MP4008	4 Megabit (512K x 8) RAM module (plastic SIP)	—	40	1950	NOW
IDT7M4016	4 Megabit (256K x 16) RAM module	TBD	45	6200	NOW
APPLICATION SPECIFIC MODULES — Synchronous RAM Modules					
IDT7MP6025	512K (64K x 8) registered static RAM module	—	35	3500	NOW
IDT7M824	1 Megabit (128K x 8) RAM module with registered buffered-latched address and I/O's	60	45	1500	NOW
IDT7M6001	32K x 20 double buffered RAM module with registered, multiplexed address	55	45	3750	NOW
APPLICATION SPECIFIC MODULES — Writable Control Store Modules					
IDT7M6032	16K x 32 high-speed writable control store with SPC™	30	25	4500	NOW
IDT7MB6042	8k x 112 high-speed writable control store with SPC™	—	35	8000	NOW
IDT7M6052	4K x 80 high-speed writable control store with onboard sequencer	45	35	4125	NOW
APPLICATION SPECIFIC MODULES — Dual-Port Modules					
IDT7M134	64K (8K x 8) dual-port RAM module	60	45	950	NOW
IDT7M144	64K (8K x 8) functions as slave with IDT7M134 to provide 16-bit words or wider; pin compatible with IDT7M134	60	45	950	NOW
IDT7M135	128K (16K x 8) dual-port RAM module	60	45	1600	NOW
IDT7M145	128K (16K x 8) functions as slave with IDT7M135 to provide 16-bit words or wider; pin compatible with IDT7M135	60	45	1600	NOW
IDT7M137	256K (32K x 8) dual-port RAM module where on-chip arbitration is not needed	60	55	1375	NOW
IDT7MB6036	128K x 16 shared port RAM module	—	70	2100	Q2'89
APPLICATION SPECIFIC MODULES — Cache Modules					
IDT7MB6039	Dual (16K x 60) data and instruction cache for MIPS R2000/R3000	—	25MHz	10W	NOW
IDT7MB6040	Dual (16K x 64) general purpose cache	—	25MHz	10W	NOW
IDT7MB6043	Dual (8K x 60) data and instruction cache for MIPS R2000/R3000	—	20MHz	TBD	CALL
IDT7MB6044	Dual (4K x 60) data and instruction cache for MIPS R2000/R3000	—	20MHz	TBD	CALL
IDT7MB6049	Dual (16K x 60) data and instruction cache for multiprocessor MIPS R2000/R3000 systems	—	25MHz	10W	Q2'89
IDT7MB6051	Dual (8K x 64) data and instruction cache for multiprocessor MIPS R2000/R3000 systems	—	20MHz	TBD	CALL

High-Speed CMOS Module Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
APPLICATION SPECIFIC MODULES — FIFO Modules					
IDT7M203	2K x 9 FIFO module using four IDT7201s	50	40	550	NOW
IDT7M204	4K x 9 FIFO module using four IDT7202s	50	40	550	NOW
IDT7M205	8K x 9 FIFO module using four IDT7203s	**50**	**40**	840	NOW
IDT7M206	16K x 9 FIFO module using four IDT7204s	**50**	**40**	840	NOW
IDT7MB2001	8K x 18 BiFIFO module or 8K x 36/16K x 18 unindirectional FIFO module	—	40	3000	NOW
IDT7MB2002	4K x 36 to 16K x 9 BiFIFO module w/transceiver	—	45	3400	NOW
IDT7MB2012	4K x 36 to 16K x 9 FIFO	—	45	1700	NOW
IDT7MB2022	16K x 9 to 4K x 36 FIFO	—	45	1700	NOW

High-Speed CMOS Multi-Port RAMs

- High speed, low power
- Independent read or write access to any memory locations from any port
- Each port has separate controls, address and I/O
- On-chip arbitration logic (except for IDT7134 and IDT7M137)
- Fully asynchronous operation from any port
- Several handshaking options (busy, interrupt, semaphores and combinations)
- Automatic power-down feature controller by $\overline{CE}$
- 2V data retention battery back-up on all low-power devices

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
DUAL-PORT RAMs					
IDT7130	8K (1K x 8) industry's most popular dual-port SRAM	45	35	325	NOW
IDT7140	8K (1K x 8) functions as slave with IDT7130 to provide 16-bit words or wider; pin compatible with IDT7130	45	35	325	NOW
IDT7132	16K (2K x 8) fastest available speeds in this industry standard product; now multiple sourced	45	35	325	NOW
IDT7142	16K (2K x 8) functions as slave with IDT7132 to provide 16-bit words or wider; pin compatible with IDT7132	45	35	325	NOW
IDT71321	16K (2K x 8) high-speed dual-port with interrupt output	45	35	325	NOW
IDT71421	16K (2K x 8) functions as slave with IDT71321 to provide 16-bit words or wider; pin compatible with IDT71321	45	35	325	NOW
IDT71322	16K (2K x 8) with Semaphores	45	35	500	NOW
IDT7133	32K (2K x 16)	55	45	375	NOW
IDT7143	32K (2K x 16) functions as slave with IDT7133 to provide 32-bit words or wider	55	45	375	NOW
IDT7134	32K (4K x 8) high speed operation in systems where on-chip arbitration is not needed	45	35	500	NOW
IDT71342	32K (4K x 8) with Semaphores	45	35	500	NOW
IDT7024	64K (4K x 16) with busy, interrupt, semaphore and master/slave select, all on one device	45	30	750	JUL'89
IDT7005	64K (8K x 8) with busy, interrupt, semaphore and master/slave select, all on one device	45	35	750	JUL'89
IDT7025	128K (8K x 16) industry's largest monolithic dual-port RAM with all the handshaking operations (busy, interrupt, semaphores and master/slave) on one device	45	30	750	JUN'89
IDT7006	128K (16K x 8) with busy, interrupt, semaphore and master/slave select, all on one device	45	35	750	JUL'89
FOUR-PORT RAMs					
IDT7050	8K (1K x 8) four-port SRAM offers increased-system performance in multiprocessor systems that have a need to communicate in real time	35	25	750	MAY'89
IDT7052	16K (2K x 8) four-port SRAM offers added benefits for high-speed systems in which multiple access is required in the same cycle	35	25	750	APR'89

High-Speed CMOS FIFOs

- High speed, low power FIFO products
- TTL compatible
- All products MIL-STD-883 compliant

INDUSTRY STANDARD FIFOS

- Seven x9 pin-compatible versions
- Asynchronous, simultaneous read and write
- Simple width and depth expandibility
- Space efficient packaging
- Full, empty and half-full flags

STANDARD X18 FIFOS

- x18 word widths
- Asynchronous, simultaneous read and write
- Multiple flags — Full, empty, half-full, almost-empty, almost-full

FLAGGED FIFOS

- Multiple flags — Full, empty, half-full, almost-empty, almost-full
- Incorporate output enable

SYNCHRONOUS FIFOS

- Ultra high performance — 20ns
- Separate READ/WRITE enable clock inputs
- Programmable almost-empty, almost-full flags

BIDIRECTIONAL FIFOS

- Matches different bus widths: 16-bit to 8-bit buses and 32-bit to 8-bit buses
- REQ/ACK interface built on-chip
- 8 programmable status flags (offset and polarity)

PARALLEL/SERIAL FIFOS

- Dedicated configurations in space efficient packages
- User configurable — P/S, S/P, P/P or S/S
- FLEXISHIFT™ allows for easy programmable serial word widths
- Multiple flags — Full, almost-full, full – 1, empty, almost-empty, empty + 1 and half-full

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
INDUSTRY STANDARD FIFOS					
IDT72401	64 x 4 (replaces 67401)	35MHz	45MHz	175	NOW
IDT72402	64 x 5 (replaces 67402)	35MHz	45MHz	175	NOW
IDT72403	64 x 4 with $\overline{OE}$ (replaces 67403)	35MHz	45MHz	175	NOW
IDT72404	64 x 5 with $\overline{OE}$ (replaces 67404)	35MHz	45MHz	175	NOW
IDT72413	64 x 5 with $\overline{OE}$, Half-Full, Almost-Empty, Almost-Full flags (replaces 67413)	35MHz	45MHz	300	NOW
IDT7200	256 x 9, 28-pin 300 mil DIP	30	25	312	NOW
IDT7201A	512 x 9 with Half-Full Flag	30	25	312	NOW
IDT7202A	1K x 9 with Half-Full Flag	30	25	312	NOW
IDT7203	2K x 9 with Half-Full Flag	40	35	375	NOW
IDT7204	4K x 9 with Half-Full Flag	40	35	375	NOW
IDT72B04	4K x 9 BiCEMOS with Half-Full Flag	20	15	TBD	Q3'89
IDT7205	8K x 9 Half-Full Flag	50	50	TBD	Q4'89
IDT7206	16K x 9 with Half-Full Flag	50	50	TBD	Q4'89
STANDARD x18 FIFOS					
IDT72045	4K x 18 with Flags	50	50	TBD	Q4'89
IDT72055	8K x 18 with Flags	50	50	TBD	Q4'89

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
FLAGGED FIFOs					
IDT72021	1K x9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	30	25	312	NOW
IDT72031	2K x 9 with Half-Full, Almost-Empty Almost-Full flags and $\overline{OE}$	40	35	375	NOW
IDT72041	4K x 9 with Half-full, Almost-Empty, Almost-Full flags and $\overline{OE}$	40	35	375	NOW
IDT72052	8K x 9 with Flags	50	50	TBD	Q4'89
IDT72062	16K x 9 with Flags	50	50	TBD	Q4'89
SYNCHRONOUS FIFOS					
IDT72215	512 x 18 Synchronous FIFO	25	20	TBD	Q3'89
IDT72225	1K x 18 Synchronous FIFO	25	20	TBD	Q3'89
BIDIRECTIONAL FIFOs					
IDT7251	512 x 18 – 1K x 9 Bidirectional FIFO	40	35	450	Q3'89
IDT72510	512 x 18 – 1K x 9 Bidirectional FIFO	40	35	450	Q3'89
IDT72511	512 x 18 – 512 x 18 Bidirectional FIFO	40	35	450	Q3'89
IDT7252	1K x 18 – 2K x 9 Bidirectional FIFO	40	35	350	Q3'89
IDT72520	1K x 18 – 2K x 9 Bidirectional FIFO	40	35	350	Q3'89
IDT72521	1K x 18 – 1K x 18 Bidirectional FIFO	40	35	350	Q3'89
IDT7MB2001	8K x 36 FIFO/8K x 18 BIFIFO	—	40	—	NOW
IDT7MB2002	4K x 36 to 9 BIFIFO	—	TBD	—	NOW
PARALLEL/SERIAL FIFOS					
IDT72103	2K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FLEXISHIFT™	40	35	450	NOW
IDT72104	4K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FLEXISHIFT™	40	35	450	NOW
IDT72105	256 x 16 Dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	TBD	25	450	Q3'89
IDT72115	512 x 16 Dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	TBD	25	450	Q3'89
IDT72125	1K x 16 Dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	TBD	25	450	Q3'89
IDT72131	2K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	APR'89
IDT72132	2K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	APR'89
IDT72141	4K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	NOW
IDT72142	4K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT™	40	35	450	APR'89

High-Speed CMOS DSP Building Blocks

- High-speed, low power DSP building blocks
- TTL-compatible
- All products MIL-STD-883 compliant

ADVANCED DSP BUILDING BLOCKS

- Very fast 50MHz components
- Supports both 16- and 32-bit integer formats
- Advanced ALU features for DSP performance

PARALLEL MULTIPLIERS

- Configures for easy array expansion
- User-controlled option for transparent output register mode
- Round Control for the MSP

PARALLEL MACs

- Selectable accumulation, rounding, and pre-loading
- Extended product output for multiple accumulations
- Pre-load function allows output register to be present
- All devices perform subtraction and double-precision addition and multiplication

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
ADVANCED DSP BUILDING BLOCKS					
IDT7320	16-bit eight-level Pipeline Register	15	12	150	Q3'89
IDT7321	16-bit seven-level Pipeline Register	15	12	150	Q3'89
IDT7317	16 x 16-bit Parallel Multiplier with 32-bit output	25	20	250	Q2'89
IDT7381	16-bit Cascadable ALU	**25**	**20**	150	NOW
IDT7383	16-bit Cascadable ALU	25	20	150	NOW
MACs					
IDT7209	12 x 12-bit, replaces TDC1009J	55	45	200	NOW
IDT7210	16 x 16-bit with 35-bit output, replaces TDC1010J	**30**	**25**	225	NOW
IDT7243	16 x 16-bit with 19-bit output, replaces TDC1043	55	45	225	NOW
MULTIPLIERS					
IDT7212	12 x 12-bit, replaces MPY012H	40	35	150	NOW
IDT7213	12 x 12-bit with single clock architecture	40	35	150	NOW
IDT7216	16 x 16-bit, replaces Am29516	**25**	**20**	200	NOW
IDT7217	16 x 16-bit with single clock architecture, replaces Am29517	**25**	**20**	200	NOW

High-Speed CMOS MICROSLICE™ Products

CMOS MICROPROGRAMMABLE MICROPROCESSOR FAMILY

- IDT49C400 products offer dramatically improved system performance through innovative architectures
- IDT3900 products are pin-compatible, microcode-compatible, performance-enhanced AM2900 family replacements
- Faster than bipolar equivalent circuits: 20-40% faster
- Lower power than bipolar equivalent circuits: 70-80% less power
- Higher output drive than bipolar equivalent circuits

CMOS ERROR DETECTION AND CORRECTION FAMILY

- Provides soft and hard error checking and correcting scheme for high-density, high-reliability memory systems
- Corrects all single bit errors; detects all double bit errors

Part Number	Description	Max. Speed (Com'l.)	Typical Power (mW)	Avail.
MICROPROCESSORS				
IDT39C01C	4-bit µP Slice —	A,B addr to Y = 40ns	125	NOW
IDT39C01D	replaces Am2901B/C, Am29C01,	A,B addr to Y = 30ns		NOW
IDT39C01E	CY7C901	A,B addr to Y = **22ns**		NOW
IDT39C03A	4-bit µP Slice —	A,B addr to Y = 67ns	150	NOW
IDT39C03B	replaces Am2903/A	A,B addr to Y = 54ns		NOW
IDT49C402	16-bit µP Slice, quad 2901 with 8	A,B, addr to Y = 47ns	350	NOW
IDT49C402A	additional destination functions and	A,B, addr to Y = 37ns		NOW
IDT49C402B	64 x 16 register file capacity —	A,B, addr to Y = **28ns**		**Q3'89**
	superset of Am29C101, CY7C9101, WSI59016			
IDT49C403	16-bit µP Slice, quad 2903/29203 with	A,B, addr to Y = 49ns	450	NOW
IDT49C403A	64 x 16 register file, 4 Q registers, word/	A,B, addr to Y = 41ns		NOW
	byte control, byte swap and SPC™			
SEQUENCERS				
IDT39C10B	12-bit Sequencer with 33-deep stack —	D to Y = 20ns	150	NOW
IDT39C10C	replaces Am 2910/A, CY7C910	D to Y = 12ns		NOW
IDT49C410	16-bit Sequencer with 33-deep stack	D to Y = 20ns	150	NOW
IDT49C410A	address up to 64K microcode	D to Y = 12ns		NOW
ERROR DETECTION AND CORRECTION				
IDT39C60	16-bit Cascadable EDC —	Detect Time = 32ns	265	NOW
IDT39C60–1	replaces Am2960,-1,A; N2960	Detect Time = 25ns		NOW
IDT39C60A	MC74F2960, -1,A	Detect Time = 20ns		NOW
IDT39C60B		**Detect Time = 18ns**		**Q3'89**
IDT49C460	32-bit Cascadable EDC —	Detect Time = 40ns	300	NOW
IDT49C460A	functional equivalent to DP8402;	Detect Time = 30ns		NOW
IDT49C460B	AS/ALS632	Detect Time = 25ns		NOW
IDT49C460C		**Detect Time = 16ns**		**NOW**
IDT49C465	32-bit Flowthru EDC™ —	Detect Time = 20ns	100	Q3'89
	two separate bidirectional 32-bit buses;			
	expandable to 64-bit			
SUPPORT CIRCUITS				
IDT39C02A	Carry Look Ahead Generator			
IDT49C25	Microcycle Length Controller			
IDT71502	4K x 16 Registered RAM for Writable Control Store			

High-Speed CMOS Data Conversion Products

- High speed — low power
- Available in military and commercial temperature ranges
- Produced with advanced CEMOS™ high-performance technology

VIDEO DACs

- IDT75C18 is pin and function compatible with TRW 1018 with half the power consumption
- IDT75C19 is world's first CMOS 9-bit video DAC
- IDT75C451/7/8 PalletteDAC™ is pin and function compatible with Brooktree BT451/7/8 with reduced power consumption and faster speed grades. MIL-STD-883 compliant devices are available
- IDT75MB38 is a triple 8-bit, 125MHz module with on-board voltage reference

FLASH A/D CONVERTERS

- IDT75C48 is pin and function compatible with TRW 1048 with half the power consumption, on-chip Error Detection and Correction, extended analog input range and improved output characteristics
- IDT75C58 has enhanced features such as overflow output and three state control which allows stacking two devices for 9-bit resolution
- IDT75MB58 is a complete Flash ADC module product with input buffer amplifier, reference voltage generator and optimized layout and decoupling

Part Number	Description	Replaces	Typical Power (mW)	Avail.
DAC				
IDT75C18	8-bit, 125MHz Video DAC with ECL inputs	TDC1018	400	NOW
IDT75C19	World's first 9-bit, 125MHz Video DAC		400	NOW
IDT75MB38	Triple 8-bit, 125MHz Video DAC Module	TDC1318, BT109	1500	NOW
IDT75C451	Triple 4-bit, 165MHz PaletteDAC™	BT451	1000	NOW
IDT75C457	Single 8-bit, 165MHz PaletteDAC™	BT457	1000	Q3'89
IDT75C458	Triple 8-bit, 165MHz PaletteDAC™	BT458	1000	NOW
ADC				
IDT75C48	8-bit, 20MHz Flash ADC	TDC1048	500	NOW
IDT75C58	8-bit, 20MHz Flash ADC with overflow output		500	NOW
IDT75MB58	Complete Flash Module using IDT75C58		800	NOW

- FCTXXXA devices 35%-50% faster then FAST™ with equivalent output drive but at dramatically lower CMOS power over full temperature and voltage supply extremes
- FCT devices same speed and output drive as FAST™ but at dramatically lower CMOS power
- 54/74FCT8XXA devices same speed and output drive as 29800, but dramatically lower CMOS power
- 54/74FCT8XXB devices 30%–40% faster than 29800 with equivalent output drive, but at dramatically lower CMOS power
- Meet JEDEC Standard No. 18
- Both CMOS and TTL output compatible (eliminates need for pull-up resistors when driving CMOS static RAMs)
- Substantially lower input current levels than FAST™, ALS or 298000 (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Pin-compatible with industry standard MSI logic
- Devices formerly designated 39CXXX are now designated 54/74FCT8XXXA or 29FCTXXXA

FCTB Family of Devices

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT29FCT52B	Non-inverting Octal Registered Transceiver	8.0	7.5	10.0	NOW
IDT29FCT53B	Inverting Octal Registered Transceiver	8.0	7.5	10.0	NOW
IDT29FCT520B	Multilevel Pipeline Register	8.0	7.5	10.0	NOW
IDT54/74FCT521B	8-Bit Comparator	7.3	5.5	10.0	NOW
IDT54/74FCT821B	10-Bit Non-inverting Register	8.5	7.5	10.0	NOW
IDT54/74FCT823B	9-Bit Non-inverting Register	8.5	7.5	10.0	NOW
IDT54/74FCT824B	9-Bit Non-inverting Register	8.5	7.5	10.0	NOW
IDT54/74FCT825B	8-Bit Non-Inverting Register	8.5	7.5	10.0	NOW
IDT54/74FCT827B	10-Bit Non-inverting Buffer	6.5	5.0	10.0	NOW
IDT54/74FCT833B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	NOW
IDT54/74FCT841B	10-Bit Non-inverting Latch	7.5	6.5	10.0	NOW
IDT54/74FCT843B	9-Bit Non-inverting Latch	7.5	6.5	10.0	NOW
IDT54/74FCT844B	9-Bit Inverting Latch	9.0	—	10.0	NOW
IDT54/74FCT845B	8-Bit Non-inverting Latch	7.5	6.5	10.0	NOW
IDT54/74FCT853B	8-Bit Transceiver w/Parity	10.0	7.0	10.0	Q3'89
IDT54/74FCT861B	10-Bit Non-inverting Transceiver	6.5	6.0	10.0	NOW
IDT54/74FCT863B	9-Bit Non-inverting Transceiver	6.5	6.0	10.0	NOW
IDT54/74FCT864B	9-Bit Inverting Transceiver	6.5	5.5	10.0	NOW

FCTA Family of Devices

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT29FCT52A	Non-inverting Octal Registered Transceiver	11.0	10.0	10.0	NOW
IDT29FCT53A	Inverting Octal Registered Transceiver	11.0	10.0	10.0	NOW
IDT29FCT520A	Multilevel Pipeline Register	16.0	14.0	10.0	NOW
IDT49FCT818A	Octal Register with SPC™	10.0	9.0	10.0	NOW
IDT54/74FCT138A	1-of-8 Decoder	7.8	5.8	10.0	NOW
IDT54/74FCT139A	Dual 1-of-4 Decoder	7.8	5.9	10.0	NOW

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT54/74FCT161A	Synchronous Binary Counter	7.5	7.2	10.0	NOW
IDT54/74FCT163A	Synchronous Binary Counter	7.5	7.2	10.0	NOW
IDT54/74FCT182A	Carry Lookahead Generator	10.7	7.0	10.0	NOW
IDT54/74FCT191A	Up/Down Binary Counter	10.5	7.8	10.0	Q3'89
IDT54/74FCT193A	Up/Down Binary Counter	6.9	6.5	10.0	Q3'89
IDT54/74FCT240A	Inverting Octal Buffer/Line Driver	5.1	4.8	10.0	NOW
IDT54/74FCT241A	Non-inverting Octal Buffer/Line Driver	5.1	4.8	10.0	NOW
IDT54/74FCT244A	Non-inverting Octal Buffer/Line Driver	5.1	4.8	10.0	NOW
IDT54/74FCT245A	Non-inverting Buffer Transceiver	4.9	4.6	10.0	NOW
IDT54/74FCT273A	Octal D Flip-Flop	8.3	7.2	10.0	NOW
IDT54/74FCT299A	Octal Universal Shift Register	9.5	7.2	10.0	NOW
IDT54/74FCT373A	Octal Transparent Latch	5.6	5.2	10.0	NOW
IDT54/74FCT374A	Octal D Register	7.2	6.5	10.0	NOW
IDT54/74FCT377A	Octal D Flip-Flop	8.3	7.2	10.0	NOW
IDT54/74FCT399A	Quad Dual-Port Register	7.5	7.0	10.0	NOW
IDT54/74FCT521A	8-Bit Identity Comparator	9.5	7.2	10.0	NOW
IDT54/74FCT533A	Octal Transparent Latch	5.6	5.2	10.0	NOW
IDT54/74FCT534A	Octal D Flip-Flop	7.2	6.5	10.0	NOW
IDT54/74FCT540A	Octal Inverting Buffer/Line Driver	5.1	4.8	10.0	NOW
IDT54/74FCT541A	Octal Non-inverting Buffer/Line Driver	5.1	4.8	10.0	NOW
IDT54/74FCT543A	Non-inverting Octal Registered Transceiver	7.5	6.5	10.0	NOW
IDT54/74FCT573A	Octal Transparent Latch	5.6	5.2	10.0	NOW
IDT54/74FCT574A	Octal D Register	7.2	6.5	10.0	NOW
IDT54/74FCT640A	Octal Inverting Buffer Transceiver	5.3	5.0	10.0	NOW
IDT54/74FCT645A	Octal Non-inverting Buffer Transceiver	4.9	4.6	10.0	NOW
IDT54/74FCT646A	Octal Non-inverting Transceiver/Register	7.7	6.3	10.0	Q2'89
IDT54/74FCT648A	Octal Inverting Transceiver/Register	6.3	5.6	10.0	Q2'89
IDT54/74FCT651A	Octal Non-inverting Transceiver/Register	—	—	10.0	Q2'89
IDT54/74FCT652A	Octal Inverting Transceiver/Register	—	—	10.0	Q2'89
IDT54/74FCT821A	10-Bit Non-inverting Register	12.0	12.0	10.0	NOW
IDT54/74FCT824A	9-Bit Non-inverting Register	12.0	12.0	10.0	NOW
IDT54/74FCT843A	9-Bit Inverting Register	12.0	12.0	10.0	NOW
IDT54/74FCT825A	8-Bit Non-inverting Register	12.0	12.0	10.0	NOW
IDT54/74FCT827A	10-Bit Non-inverting Buffer	10.0	8.0	10.0	NOW
IDT54/74FCT833A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	NOW
IDT54/74FCT841A	10-Bit Non-inverting Latch	11.0	9.5	10.0	NOW
IDT54/74FCT843A	9-Bit Non-inverting Latch	11.0	9.5	10.0	NOW
IDT54/74FCT844A	9-Bit Inverting Latch	12.0	10.0	10.0	NOW
IDT54/74FCT845A	8-Bit Non-inverting Latch	11.0	9.5	10.0	NOW
IDT54/74FCT853A	8-Bit Transceiver w/Parity	14.0	10.0	10.0	Q3'89
IDT54/74FCT861A	10-Bit Non-inverting Transceiver	10.0	8.0	10.0	NOW
IDT54/74FCT863A	9-Bit Non-inverting Transceiver	10.0	8.0	10.0	NOW
IDT54/74FCT864A	9-Bit Inverting Transceiver	9.5	7.5	10.0	NOW

FCT Family of Devices

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Typical Power (mW)	Avail.
IDT49FCT601	16-Bit Bidirectional Latch w/Byte-Swap	—	—	20.0	Q2'89
IDT49FCT618	16-Bit Register with SPC™	14.0	12.5	20.0	Q2'89
IDT49FCT661	16-Bit Synchronous Binary Counter	—	—	20.0	Q2'89
IDT49FCT818	Octal Register with SPC™	14.0	12.5	10.0	NOW
IDT54/74FCT138	1-of-8 Decoder	12.0	9.0	10.0	NOW
IDT54/74FCT139	Dual 1-of-4 Decoder	12.0	9.0	10.0	NOW
IDT54/74FCT161	Synchronous Binary Counter	11.5	11.0	10.0	NOW
IDT54/74FCT163	Synchronous Binary Counter	11.5	11.0	10.0	NOW
IDT54/74FCT182	Carry Lookahead Generator	16.5	10.0	10.0	NOW
IDT54/74FCT191	Up/Down Binary Counter	16.0	12.0	10.0	Q1'89
IDT54/74FCT193	Up/Down Binary Counter	10.5	10.0	10.0	Q1'89
IDT54/74FCT240	Inverting Octal Buffer/Line Driver	9.0	8.0	10.0	NOW
IDT54/74FCT241	Non-inverting Octal Buffer/Line Driver	7.0	6.5	10.0	NOW
IDT54/75FCT244	Non-inverting Octal Buffer/Line Driver	7.0	6.5	10.0	NOW
IDT54/74FCT245	Non-inverting Buffer Transceiver	7.5	7.0	10.0	NOW
IDT54/74FCT273	Octal D Flip-Flop	15.0	13.0	10.0	NOW
IDT54/74FCT299	Octal Universal Shift Transceiver	14.0	10.0	10.0	NOW
IDT54/74FCT373	Octal Transparent Latch	8.5	8.0	10.0	NOW
IDT54/74FCT374	Octal D Register	11.0	10.0	10.0	NOW
IDT54/74FCT377	Octal D Flip-Flop	15.0	13.0	10.0	NOW
IDT54/74FCT399	Quad Dual-Port Register	11.5	10.0	10.0	NOW
IDT54/74FCT521	8-Bit Identity Comparator	15.0	11.0	10.0	NOW
IDT54/74FCT533	Octal Transparent Latch	12.0	10.0	10.0	NOW
IDT54/74FCT534	Octal D Flip-Flop	11.0	10.0	10.0	NOW
IDT54/74FCT540	Octal Inverting Buffer/Line Driver	9.5	8.5	10.0	NOW
IDT54/74FCT541	Octal Non-inverting Buffer/Line Driver	9.0	8.0	10.0	NOW
IDT54/74FCT543	Octal Non-inverting Octal RegisteredTransceiver	10.0	8.5	10.0	NOW
IDT54/74FCT573	Octal Transparent Latch	8.5	8.0	10.0	NOW
IDT54/74FCT574	Octal D Register	11.0	10.0	10.0	NOW
IDT54/74FCT640	Octal Inverting Buffer Transceiver	8.0	7.0	10.0	NOW
IDT54/74FCT645	Octal Non-inverting Buffer Transceiver	11.0	9.5	10.0	NOW
IDT54/74FCT646	Octal Non-inverting Transceiver/Register	11.0	9.0	10.0	NOW
IDT54/74FCT648	Octal Inverting Transceiver/Register	9.0	8.0	10.0	Q2'89
IDT54/74FCT651	Octal Non-inverting Transceiver/Register	10.0	9.0	10.0	Q2'89
IDT54/74FCT652	Octal Inverting Transceiver/Register	10.0	9.0	10.0	Q2'89

AHCT Family of Devices

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.
IDT54AHCT138	1-of-8 Decoder	27.0	—	3.5	NOW
IDT54AHCT139	Dual 1-of-4 Decoder	25.0	—	3.5	NOW
IDT54AHCT161	Synchronous Binary Counter	20.0	—	3.5	NOW
IDT54AHCT163	Synchronous Binary Counter	20.0	—	5.0	NOW
IDT54AHCT182	Carry Lookahead Generator	20.5	—	3.5	NOW
IDT54AHCT191	Up/Down Binary Counter	22.0	—	5.0	NOW
IDT54AHCT193	Up/Down Binary Counter	19.0	—	3.5	NOW
IDT54AHCT240	Inverting Octal Buffer/Line Driver	12.0	—	3.5	NOW
IDT54AHCT244	Non-inverting Octal Buffer/Line Driver	13.0	—	3.5	NOW
IDT54AHCT245	Non-inverting Buffer Transceiver	15.0	—	3.5	NOW
IDT54AHCT273	Octal D Flip-Flop	17.0	—	3.5	NOW
IDT54AHCT299	Universal Shift Register	17.0	—	3.5	NOW
IDT54AHCT373	Octal Transparent Latch	19.0	—	3.5	NOW
IDT54AHCT374	Octal D Register	18.0	—	3.5	NOW
IDT54AHCT377	Octal D Flip-Flop	20.0	—	3.5	NOW
IDT54AHCT521	8-Bit Identity Comparator	17.0	—	3.5	NOW
IDT54AHCT533	Octal Transparent Latch	24.0	—	3.5	NOW
IDT54AHCT534	Octal D Flip-Flop	18.0	—	3.5	NOW
IDT54AHCT573	Octal Transparent Latch	15.0	—	3.5	NOW
IDT54AHCT574	Octal D Register	15.0	—	3.5	NOW
IDT54AHCT640	Octal Inverting Buffer Transceiver	14.0	—	3.5	NOW
IDT54AHCT645	Octal Non-inverting Buffer Transceiver	15.0	—	3.5	NOW

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STATIC RAM CROSS REFERENCE GUIDE

AMD	IDT
AM2167-35DC	IDT6167SA35D
AM2167-35LC	IDT6167SA35L
AM2167-35PC	IDT6167SA35P
AM2167-45/BRA	IDT6167SA45DB
AM2167-45/BUC	IDT6167SA45LB
AM2167-45DE	IDT6167SA45DM
AM2167-55/BRA	IDT6167SA55DB
AM2167-55/BUC	IDT6167SA55LB
AM2167-55DE	IDT6167SA55DM
AM2167-70/BRA	IDT6167SA70DB
AM2167-70/BUC	IDT6167SA70LB
AM2167-70DE	IDT6167SA70DM
AM2168-35DC	IDT6168SA35D
AM2168-35LC	IDT6168SA35L
AM2168-35PC	IDT6168SA35P
AM2168-45/BRA	IDT6168SA45DB
AM2168-45/BUC	IDT6168SA45LB
AM2168-45DE	IDT6168SA45DM
AM2168-45LE	IDT6168SA45LM
AM2168-55/BRA	IDT6168SA55DB
AM2168-55/BUC	IDT6168SA55LB
AM2168-55DE	IDT6168SA55DM
AM2168-55LE	IDT6168SA55LM
AM2168-70/BRA	IDT6168SA70DB
AM2168-70/BUC	IDT6168SA70LB
AM2168-70DE	IDT6168SA70DM
AM2168-70LE	IDT6168SA70LM
AM2169-40DC	IDT6168SA20D
AM2169-40LC	IDT6168SA20L
AM2169-40PC	IDT6168SA20P
AM2169-50/BRA	IDT6168SA25DB
AM2169-50DC	IDT6168SA25D
AM2169-50DE	IDT6168SA25DM
AM2169-50LE	IDT6168SA25LM
AM2169-50PC	IDT6168SA25P
AM2169-70/BRA	IDT6168SA30DB
AM2169-70DE	IDT6168SA30DM
AM2169-70LE	IDT6168SA30LM
AM2130-10/BUC	IDT7130S100L52B*
AM2130-10/BXC	IDT7130S100CB
AM2130-10DC	IDT7130S100C
AM2130-10DCB	IDT7130S100C
AM2130-10JC	IDT7130S100J*
AM2130-10LC	IDT7130S100L52*
AM2130-10LCB	IDT7130S100L52*
AM2130-10PC	IDT7130S100P
AM2130-10PCB	IDT7130S100P
AM2130-12/BUC	IDT7130S120L52B*
AM2130-12/BXC	IDT7130S120CB
AM2130-70/BXC	IDT7130S70CB
AM2130-70DC	IDT7130S70C
AM2130-70DCB	IDT7130S70C
AM2130-70JC	IDT7130S70J*
AM2130-70LC	IDT7130S70L52*
AM2130-70LCB	IDT7130S70L52*
AM2130-70PC	IDT7130S70P
AM2130-70PCB	IDT7130S70P
AM9128-12/BJA	IDT6116SA120DB

NOTES:
A lower case ""x"" indicates the packages of the AMD part are unknown."
All AM99 series parts have 2 Volt data retention capability.

AMD CONT.	IDT
AM9128-12/BUC	IDT6116SA120L32B
AM9128-15/BJA	IDT6116SA150DB
AM9128-15/BUC	IDT6116SA150L32B
AM9128-70DE	IDT6116SA70D
AM9128-90/BJA	IDT6116SA90DB
AM9128-90/BUC	IDT6116SA90L32B
AM99C164-35x	IDT7188L35x
AM99C164-45x	IDT7188L45x
AM99C165-35x	IDT6198L35x
AM99C165-45x	IDT6198L45x
AM99C328-45x	IDT71256L45x
AM99C328-55x	IDT71256L55x
AM99C641-25DC	IDT7187L25C
AM99C641-25LC	IDT7187L25L22
AM99C641-25PC	IDT7187L25P
AM99C641-35DC	IDT7187L35C
AM99C641-35LC	IDT7187L35L22
AM99C641-35PC	IDT7187L35P
AM99C641-45/BWA	IDT7187L45CB
AM99C641-45/LMC	IDT7187L45L22B
AM99C641-45DC	IDT7187L45C
AM99C641-45DE	IDT7187L45CM
AM99C641-45LC	IDT7187L45L22
AM99C641-45LE	IDT7187L45L22M
AM99C641-45PC	IDT7187L45P
AM99C641-55/BWA	IDT7187L55CB
AM99C641-55/LMC	IDT7187L55L22B
AM99C641-55DE	IDT7187L55CM
AM99C641-55LE	IDT7187L55L22M
AM99C641-70/BWA	IDT7187L70CB
AM99C641-70/LMC	IDT7187L70L22B
AM99C641-70DE	IDT7187L70CM
AM99C641-70LE	IDT7187L70L22M
AM99C68-45/BRA	IDT6168LA45DB
AM99C68-55/BRA	IDT6168LA55DB
AM99C68-55DMB	IDT6168LA55DB
AM99C68-70/BRA	IDT6168LA70DB
AM99C68-70DMB	IDT6168LA70DB
AM99CL68-45/BRA	IDT6168LA45DB
AM99CL68-55/BRA	IDT6168LA55DB
AM99CL68-70/BRA	IDT6168LA70DB
AM99C88-10/BUC	IDT7164L100L32B
AM99C88-10/BXC	IDT7164L100DB
AM99C88-12/BUC	IDT7164L120L32B
AM99C88-12/BXC	IDT7164L120DB
AM99C88-15/BUC	IDT7164L150L32B
AM99C88-15/BXC	IDT7164L150DB
AM99C88-20/BUC	IDT7164L200DB
AM99C88-20/BXC	IDT7164L200L32B
AM99C88-70/BUC	IDT7164L70L32B
AM99C88-70/BXC	IDT7164L70DB
AM99C88-70DE	IDT7164L70DM
AM99C88-70LC	IDT7164L45L32
AM99C88-70LE	IDT7164L70L32M
AM99C88H-35x	IDT7164L35x
AM99C88H-45/x	IDT7164L45xB
AM99CL88-10/BUC	IDT7164L100L32B
AM99CL88-10/BXC	IDT7164L100DB
AM99CL88-12/BUC	IDT7164L120L32B
AM99CL88-12/BXC	IDT7164L120DB
AM99CL88-15/BUC	IDT7164L150L32B
AM99CL88-15/BXC	IDT7164L150DB
AM99CL88-70/BUC	IDT7164L70L32B

AMD CONT.	IDT
AM99CL88-70/BXC	IDT7164L70DB
AM99CS88-10/BUC	IDT7164L100L32B
AM99CS88-10/BXC	IDT7164L100DB
AM99CS88-12/BUC	IDT7164L120L32B
AM99CS88-12/BXC	IDT7164L120DB
AM99CS88-15/BUC	IDT7164L150L32B
AM99CS88-15/BXC	IDT7164L150DB
AM99CS88-20/BUC	IDT7164L200L32B
AM99CS88-20/BXC	IDT7164L200DB
AM99CS88-70/BUC	IDT7164L70L32B
AM99CS88-70/BXC	IDT7164L70DB

CYPRESS	IDT
CY6116-35PC	IDT6116SA35P
CY6116-35DC	IDT6116SA35D
CY6116-35LC	IDT6116SA35L28
CY6116-35DMB	IDT6116SA35DB
CY6116-35LMB	IDT6116SA35L28B
CY6116-45PC	IDT6116SA45P
CY6116-45DC	IDT6116SA45D
CY6116-45LC	IDT6116SA45L28
CY6116-45DMB	IDT6116SA45DB
CY6116-45LMB	IDT6116SA45L28B
CY6116-55DMB	IDT6116SA55DB
CY6116-55LMB	IDT6116SA55L28B
CY7C128-25DC	IDT6116SA25TD
CY7C128-25LC	IDT6116SA25L24
CY7C128-25PC	IDT6116SA25TP
CY7C128-25SC	IDT6116SA25SO
CY7C128-35DC	IDT6116SA35TD
CY7C128-35DMB	IDT6116SA35TDB
CY7C128-35LC	IDT6116SA35L24
CY7C128-35LMB	IDT6116SA35L24B
CY7C128-35PC	IDT6116SA35TP
CY7C128-35SC	IDT6116SA35SO
CY7C128-45DC	IDT6116SA45TD
CY7C128-45DMB	IDT6116SA45TDB
CY7C128-45LC	IDT6116SA45L24
CY7C128-45LMB	IDT6116SA45L24B
CY7C128-45PC	IDT6116SA45TP
CY7C128-45SC	IDT6116SA45SO
CY7C128-55DMB	IDT6116SA55TDB
CY7C128-55LMB	IDT6116SA55L24B
CY7C130-45LC	IDT7130S45L52
CY7C130-45PC	IDT7130S45P
CY7C130-55DC	IDT7130S55C
CY7C130-55LC	IDT7130S55L52
CY7C130-55PC	IDT7130S55P
CY7C132-35DC	IDT7132S35C
CY7C132-35LC	IDT7132S35L52
CY7C132-35PC	IDT7132S35P
CY7C132-45DC	IDT7132S45C
CY7C132-45LC	IDT7132S45L52
CY7C132-45PC	IDT7132S45P
CY7C132-55DC	IDT7132S55C
CY7C132-55LC	IDT7132S55L52
CY7C132-55PC	IDT7132S55P
CY7C140-45DC	IDT7140S45C
CY7C140-45LC	IDT7140S45L52
CY7C140-45PC	IDT7140S45P
CY7C140-55DC	IDT7140S55C
CY7C140-55LC	IDT7140S55L52

CYPRESS CONT.	IDT
CY7C140-55PC	IDT7140S55P
CY7C142-35DC	IDT7142S35C
CY7C142-35LC	IDT7142S35L52
CY7C142-35PC	IDT7142S35P
CY7C142-45DC	IDT7142S45C
CY7C142-45LC	IDT7142S45L52
CY7C142-45PC	IDT7142S45P
CY7C142-55DC	IDT7142S55C
CY7C142-55LC	IDT7142S55L52
CY7C142-55PC	IDT7142S55P
CY7C161-25DC*	IDT71981S25C
CY7C161-35DC*	IDT71981S35C
CY7C161-35DMB*	IDT71981S35CB
CY7C161-35LC*	IDT71981S35L
CY7C161-45DC*	IDT71981S45C
CY7C161-45DMB*	IDT71981S45CB
CY7C161-45LC*	IDT71981S45L
CY7C161-45LMB*	IDT71981S45LB
CY7C161L-25DC*	IDT71981L25C
CY7C161L-35DC*	IDT71981L35C
CY7C161L-35DMB*	IDT71981L35CB
CY7C161L-35LC*	IDT71981L35L24
CY7C161L-35LMB*	IDT71981L35L24B
CY7C161L-45DC*	IDT7198LS45C
CY7C161L-45DMB*	IDT71981L45CB
CY7C161L-45LC*	IDT71981L45L24
CY7C161L-45LMB*	IDT71981L45L24B
CY7C162-25DC*	IDT71982S25C
CY7C162-35DC*	IDT71982S35C
CY7C162-35LC*	IDT71982S35L
CY7C162-35LMB*	IDT71982S35LB
CY7C162-45DC*	IDT71982S45C
CY7C162-45DMB*	IDT71982S45CB
CY7C162-45LC*	IDT71982S45L
CY7C162-45LMB*	IDT71982S45LB
CY7C162L-25DC*	IDT71982L25C
CY7C162L-35DC*	IDT71982L35C
CY7C162L-35DMB*	IDT71982L35CB
CY7C162L-35LC*	IDT71982L35L
CY7C162L-35LMB*	IDT71982L35LB
CY7C162L-45DC*	IDT71982L45C
CY7C162L-45DMB*	IDT71982L45CB
CY7C162L-45LC*	IDT71982L45L
CY7C162L-45LMB*	IDT71982L45LB
CY7C164-25DC	IDT7188S25C
CY7C164-25PC	IDT7188S25P
CY7C164-35DC	IDT7188S35C
CY7C164-35DMB	IDT7188S35CB
CY7C164-35LC	IDT7188S35L
CY7C164-35LMB	IDT7188S35LB
CY7C164-35PC	IDT7188S35P
CY7C164-45DC	IDT7188S45C
CY7C164-45DMB	IDT7188S45CB
CY7C164-45LC	IDT7188S35L
CY7C164-45LMB	IDT7188S45LB
CY7C164-45PC	IDT7188S45P
CY7C164L-25DC	IDT7188L25C
CY7C164L-25PC	IDT7188L25P
CY7C164L-35DC	IDT7188L35C
CY7C164L-35DMB	IDT7188L35CB
CY7C164L-35LC	IDT7188L35L
CY7C164L-35LMB	IDT7188L35LB
CY7C164L-35PC	IDT7188L35P
CY7C164L-45DC	IDT7188L45C
CY7C164L-45DMB	IDT7188L45CB
CY7C164L-45LC	IDT7188L35L
CY7C164L-45LMB	IDT7188L45LB
CY7C164L-45PC	IDT7188L45P
CY7C166-25DC	IDT6198S25C
CY7C166-25PC	IDT6198S25P
CY7C166-35DC	IDT6198S35C
CY7C166-35DMB	IDT6198S35CB
CY7C166-35LC	IDT6198S35L
CY7C166-35LMB	IDT6198S35LB
CY7C166-35PC	IDT6198S35P
CY7C166-45DC	IDT6198S45C
CY7C166-45DMB	IDT6198S45CB
CY7C166-45LC	IDT6198S45L
CY7C166-45LMB	IDT6198S45LB
CY7C166-45PC	IDT6198S45P
CY7C166L-25DC	IDT6198L25C
CY7C166L-25PC	IDT6198L25P
CY7C166L-35DC	IDT6198L35C
CY7C166L-35DMB	IDT6198L35CB
CY7C166L-35LC	IDT6198L35L
CY7C166L-35LMB	IDT6198L35LB
CY7C166L-35PC	IDT6198L35P
CY7C166L-45DC	IDT6198L45C
CY7C166L-45DMB	IDT6198L45CB
CY7C166L-45LC	IDT6198L45L
CY7C166L-45LMB	IDT6198L45LB
CY7C166L-45PC	IDT6198L45P
CY7C167-25PC	IDT6167SA25P
CY7C167-25DC	IDT6167SA25D
CY7C167-25LC	IDT6167SA25L
CY7C167-35PC	IDT6167SA35P
CY7C167-35DC	IDT6167SA35D
CY7C167-35LC	IDT6167SA35L
CY7C167-35DMB	IDT6167SA35DB
CY7C167-35LMB	IDT6167SA35LB
CY7C167-45LC	IDT6167SA35L
CY7C167-45DMB	IDT6167SA45DB
CY7C167-45LMB	IDT6167SA45LB
CY7C167L-25DC	IDT6167LA25D
CY7C167L-25LC	IDT6167LA25L
CY7C167L-25PC	IDT6167LA25P
CY7C167L-35DC	IDT6167LA35D
CY7C167L-35LC	IDT6167LA35L
CY7C167L-35PC	IDT6167LA35P
CY7C168-25DC	IDT6168SA25D
CY7C168-25LC	IDT6168SA25L
CY7C168-25PC	IDT6168SA25P
CY7C168-25SC	IDT6168SA25SO
CY7C168-35DC	IDT6168SA35D
CY7C168-35DMB	IDT6168SA35DB
CY7C168-35LC	IDT6168SA35L
CY7C168-35LMB	IDT6168SA35LB
CY7C168-35PC	IDT6168SA35P
CY7C168-35SC	IDT6168SA35SO
CY7C168-45DMB	IDT6168SA45DB
CY7C168-45LMB	IDT6168SA45LB
CY7C168L-25DC	IDT6168LA25D
CY7C168L-25LC	IDT6168LA25L
CY7C168L-25PC	IDT6168LA25P
CY7C168L-25SC	IDT6168LA25SO
CY7C168L-35DC	IDT6168LA35D
CY7C168L-35LC	IDT6168LA35L
CY7C168L-35PC	IDT6168LA35P
CY7C168L-35SC	IDT6168LA35SO
CY7C169-25DC	IDT6168SA15D
CY7C169-25LC	IDT6168SA15L
CY7C169-25PC	IDT6168SA15P
CY7C169-35DC	IDT6168SA20D
CY7C169-35DMB	IDT6168SA20DB
CY7C169-35LC	IDT6168SA20L
CY7C169-35LMB	IDT6168SA20LB
CY7C169-35PC	IDT6168SA20P
CY7C169-40DC	IDT6168SA20D
CY7C169-40DMB	IDT6168SA20DB
CY7C169-40LC	IDT6168SA20L
CY7C169-40LMB	IDT6168SA20LB
CY7C169-40PC	IDT6168SA20P
CY7C169L-25DC	IDT6168LA15D
CY7C169L-25LC	IDT6168LA15L
CY7C169L-25PC	IDT6168LA15P
CY7C169L-35DC	IDT6168LA20D
CY7C169L-35LC	IDT6168LA20L
CY7C169L-35PC	IDT6168LA20P
CY7C170-25PC	IDT61970S25P
CY7C170-25DC	IDT61970S25D
CY7C170-35PC	IDT61970S35P
CY7C170-35DC	IDT61970S35D
CY7C170-35DMB	IDT61970S35DB
CY7C170-45PC	IDT61970S45P
CY7C170-45DC	IDT61970S45D
CY7C170-45DMB	IDT61970S45DB
CY7C171-25DC	IDT71681SA25D
CY7C171-25LC	IDT71681SA25L
CY7C171-25PC	IDT71681SA25P
CY7C171-35DC	IDT71681SA35D
CY7C171-35DMB	IDT71681SA35DB
CY7C171-35LC	IDT71681SA35L
CY7C171-35LMB	IDT71681SA35LB
CY7C171-35PC	IDT71681SA35P
CY7C171-45DC	IDT71681SA45D
CY7C171-45DMB	IDT71681SA45DB
CY7C171-45LC	IDT71681SA45L
CY7C171-45LMB	IDT71681SA45LB
CY7C171-45PC	IDT71681SA45P
CY7C171L-25DC	IDT71681LA25D
CY7C171L-25LC	IDT71681LA25L
CY7C171L-25PC	IDT71681LA25P
CY7C171L-35DC	IDT71681LA35D
CY7C171L-35LC	IDT71681LA35L
CY7C171L-35PC	IDT71681LA35P
CY7C172-25DC	IDT71682SA25D
CY7C172-25LC	IDT71682SA25L
CY7C172-25PC	IDT71682SA25P
CY7C172-35DC	IDT71682SA35D
CY7C172-35DMB	IDT71682SA35DB
CY7C172-35LC	IDT71682SA35L
CY7C172-35LMB	IDT71682SA35LB
CY7C172-35PC	IDT71682SA35P
CY7C172-45DC	IDT71682SA45D
CY7C172-45DMB	IDT71682SA45DB
CY7C172-45LC	IDT71682SA45L
CY7C172-45LMB	IDT71682SA45LB
CY7C172-45PC	IDT71682SA45P
CY7C172L-25DC	IDT71682LA25D
CY7C172L-25LC	IDT71682LA25L
CY7C172L-25PC	IDT71682LA25P
CY7C172L-35DC	IDT71682LA35D
CY7C172L-35LC	IDT71682LA35L
CY7C172L-35PC	IDT71682LA35P
CY7C185-35DC	IDT7164S35TD
CY7C185-35PC	IDT7164S35TP
CY7C185-45DC	IDT7164S45TD
CY7C185-45DMB	IDT7164S45TDB
CY7C185-45PC	IDT7164S45TP
CY7C185L-35DC	IDT7164L35TD
CY7C185L-35PC	IDT7164L35TP
CY7C185L-45DC	IDT7164L45TD
CY7C185L-45DMB	IDT7164L45TDB
CY7C185L-45PC	IDT7164L45TP
CY7C185L-55DMB	IDT7164L55TDB
CY7C186-35DC	IDT7164S35D
CY7C186-35PC	IDT7164S35P
CY7C186-45DC	IDT7164S45D
CY7C186-45DMB	IDT7164S45DB
CY7C186-45PC	IDT7164S45P
CY7C186-55DMB	IDT7164S55DB
CY7C186L-35DC	IDT7164L35D
CY7C186L-35PC	IDT7164L35P
CY7C186L-45DC	IDT7164L45D

NOTES:
An asterisk "*" indicates the IDT part is NOT pin for pin compatible.
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

CYPRESS CONT.	IDT
CY7C186L-45DMB	IDT7164L45DB
CY7C186L-45PC	IDT7164L45P
CY7C186L-55DMB	IDT7164L55DB
CY7C187-25DC	IDT7187S25D
CY7C187-25PC	IDT7187S25P
CY7C187-35DC	IDT7187S35D
CY7C187-35DMB	IDT7187S35DB
CY7C187-35LC	IDT7187S35L22
CY7C187-35LMB	IDT7187S35L22B
CY7C187-35PC	IDT7187S35P
CY7C187-45DC	IDT7187S45D
CY7C187-45DMB	IDT7187S45DB
CY7C187-45LC	IDT7187S45L22
CY7C187-45LMB	IDT7187S45L22B
CY7C187-45PC	IDT7187S45P
CY7C187L-25DC	IDT7187L25D
CY7C187L-25PC	IDT7187L25P
CY7C187L-35DC	IDT7187L35D
CY7C187L-35DMB	IDT7187L35DB
CY7C187L-35LC	IDT7187L35L22
CY7C187L-35LMB	IDT7187L35L22B
CY7C187L-35PC	IDT7187L35P
CY7C187L-45DC	IDT7187L45D
CY7C187L-45DMB	IDT7187L45DB
CY7C187L-45LC	IDT7187L45L22
CY7C187L-45LMB	IDT7187L45L22B
CY7C187L-45PC	IDT7187L45P
CY7C191-25PC	IDT71281S25P
CY7C191-25DC	IDT71281S25D
CY7C191-25LC	IDT71281S25L
CY7C191-35PC	IDT71281S35P
CY7C191-35DC	IDT71281S35D
CY7C191-35LC	IDT71281S35L
CY7C191-35DMB	IDT71281S35DB
CY7C191-35LMB	IDT71281S35LB
CY7C191-45PC	IDT71281S45P
CY7C191-45DC	IDT71281S45D
CY7C191-45LC	IDT71281S45L
CY7C191-45DMB	IDT71281S45DB
CY7C191-45LMB	IDT71281S45LB
CY7C192-25PC	IDT71282S25P
CY7C192-25DC	IDT71282S25D
CY7C192-25LC	IDT71282S25L
CY7C192-35PC	IDT71282S35P
CY7C192-35DC	IDT71282S35D
CY7C192-35LC	IDT71282S35L
CY7C192-35DMB	IDT71282S35DB
CY7C192-35LMB	IDT71282S35LB
CY7C192-45PC	IDT71282S45P
CY7C192-45DC	IDT71282S45D
CY7C192-45LC	IDT71282S45L
CY7C192-45DMB	IDT71282S45DB
CY7C192-45LMB	IDT71282S45LB
CY7C194-25PC	IDT71258S25P
CY7C194-25VC	IDT71258S25Y
CY7C194-25DC	IDT71258S25D
CY7C194-25LC	IDT71258S25L
CY7C194-35PC	IDT71258S35P
CY7C194-35VC	IDT71258S35Y
CY7C194-35DC	IDT71258S35D
CY7C194-35LC	IDT71258S35L
CY7C194-35DMB	IDT71258S35DB
CY7C194-35LMB	IDT71258S35LB
CY7C194-45PC	IDT71258S45P

NOTES:
An asterisk "*" indicates the IDT part is NOT pin for pin compatible.
*The CY7C161/162 come in a 300 mil package vs. 400 mil IDT71981/982.

CYPRESS CONT.	IDT
CY7C194-45VC	IDT71258S45Y
CY7C194-45DC	IDT71258S45D
CY7C194-45LC	IDT71258S45L
CY7C194-45DMB	IDT71258S45DB
CY7C194-45LMB	IDT71258S45LB
CY7C196-25PC	IDT61298S25P
CY7C196-25VC	IDT61298S25Y
CY7C196-25DC	IDT61298S25D
CY7C196-25LC	IDT61298S25L
CY7C196-35PC	IDT61298S35P
CY7C196-35VC	IDT61298S35Y
CY7C196-35DC	IDT61298S35D
CY7C196-35LC	IDT61298S35L
CY7C196-35DMB	IDT61298S35DB
CY7C196-35LMB	IDT61298S35LB
CY7C196-45PC	IDT61298S45P
CY7C196-45VC	IDT61298S45Y
CY7C196-45DC	IDT61298S45D
CY7C196-45LC	IDT61298S45L
CY7C196-45DMB	IDT61298S45DB
CY7C196-45LMB	IDT61298S45LB
CY7C197-25PC	IDT71257S25P
CY7C197-25VC	IDT71257S25Y
CY7C197-25DC	IDT71257S25D
CY7C197-25LC	IDT71257S25L
CY7C197-35PC	IDT71257S35P
CY7C197-35VC	IDT71257S35Y
CY7C197-35DC	IDT71257S35D
CY7C197-35LC	IDT71257S35L
CY7C197-35DMB	IDT71257S35DB
CY7C197-35LMB	IDT71257S35LB
CY7C197-45PC	IDT71257S45P
CY7C197-45VC	IDT71257S45Y
CY7C197-45DC	IDT71257S45D
CY7C197-45LC	IDT71257S45L
CY7C197-45DMB	IDT71257S45DB
CY7C197-45LMB	IDT71257S45LB
CY7C198-35PC	IDT71256S35P
CY7C198-45DMB	IDT71256S45DB
CY7C198-45DC	IDT71256S45D
CY7C198-45PC	IDT71256S45P
CY7C198-55DC	IDT71256S55D
CY7C198-55DMB	IDT71256S55DB
CY7C198-55PC	IDT71256S55P

EDI	IDT
EDI8164C25QB	IDT7187S25DB
EDI8164C35QB	IDT7187S35DB
EDI8164C45QB	IDT7187S45DB
EDI8164C55QB	IDT7187S55DB
EDI8164P45QB	IDT7187L45DB
EDI8164P55QB	IDT7187L55DB
EDI8164C25LB	IDT7187S25LB
EDI8164C35LB	IDT7187S35LB
EDI8164C45LB	IDT7187S45LB
EDI8164C55LB	IDT7187S55LB
EDI8164P45LB	IDT7187L45LB
EDI8164P55LB	IDT7187L55LB
EDI8416C25QB	IDT7188S25CB
EDI8416C35QB	IDT7188S35CB
EDI8416C45QB	IDT7188S45CB
EDI8416C55QB	IDT7188S55CB
EDI8416P25QB	IDT7188L25CB
EDI8416P35QB	IDT7188L35CB
EDI8416P45QB	IDT7188L45CB
EDI8416P55QB	IDT7188L55CB
EDI8417C35QB	IDT7198S35CB
EDI8417C45QB	IDT7198S45CB
EDI8417C55QB	IDT7198S55CB
EDI8417C35LB	IDT7198S35LB
EDI8417C45LB	IDT7198S45LB
EDI8417C55LB	IDT7198S55LB
EDI8464C45QB	IDT71258S45CB
EDI8464C55QB	IDT71258S55CB

EDI CONT.	IDT
EDI8464C45LB	IDT71258S45LB
EDI8464C55LB	IDT71258S55LB
EDI8802L55QB	IDT6116LA55TDB
EDI8802L70QB	IDT6116LA70TDB
EDI8802L85QB	IDT6116LA85TDB
EDI8802L100QB	IDT6116LA90TDB
EDI8802L120QB	IDT6116LA120TDB
EDI8802L150QB	IDT6116LA150TDB
EDI8802L55LB	IDT6116LA55L32B
EDI8802L70LB	IDT6116LA70L32B
EDI8802L85LB	IDT6116LA85L32B
EDI8802L100LB	IDT6116LA90L32B
EDI8802L120LB	IDT6116LA120L32B
EDI8802L150LB	IDT6116LA150L32B
EDI8802H55QB	IDT6116SA55TDB
EDI8802H70QB	IDT6116SA70TDB
EDI8802H85QB	IDT6116SA85TDB
EDI8802H100QB	IDT6116SA90TDB
EDI8802H120QB	IDT6116SA120TDB
EDI8802H150QB	IDT6116SA150TDB
EDI8802H55LB	IDT6116SA55L32B
EDI8802H70LB	IDT6116SA70L32B
EDI8802H85LB	IDT6116SA85L32B
EDI8802H100LB	IDT6116SA90L32B
EDI8802H120LB	IDT6116SA120L32B
EDI8802H150LB	IDT6116SA150L32B
EDI8808C35CB	IDT7164S35DB
EDI8808C45CB	IDT7164S45DB
EDI8808C55CB	IDT7164S55DB
EDI8808C35QB	IDT7164S35TCB
EDI8808C45QB	IDT7164S45TCB
EDI8808C55QB	IDT7164S55TCB
EDI8808C35LB	IDT7164S35L32B
EDI8808C45LB	IDT7164S45L32B
EDI8808C55LB	IDT7164S55L32B
EDI8808C-70LPKMHR	IDT7164L70DB
EDI8808C-10LPKMHR	IDT7164L100DB
EDI8808C-12LPKMHR	IDT7164L120DB
EDI8808C-15LPKMHR	IDT7164L150DB
EDI8832C55CB	IDT71256S55DB
EDI8832C-70KMHR	IDT71256S70DB
EDI8832C-85KMHR	IDT71256S85DB
EDI8832C-10KMHR	IDT71256S100DB
EDI8832C-12KMHR	IDT71256S120DB
EDI8832C-15KMHR	IDT71256S150DB
EDI8832C55LB	IDT71256S55L32B
EDI8832C-70JMHR	IDT71256S70L32B
EDI8832C-85JMHR	IDT71256S85L32B
EDI8832C-10JMHR	IDT71256S100L32B
EDI8832C-12JMHR	IDT71256S120L32B
EDI8832C-15JMHR	IDT71256S150L32B

FUJITSU	IDT
MB81C67-35	IDT6167SA35P
MB81C67-45	IDT6167SA35P
MB81C67-45-W	IDT6167SA45xM
MB81C67-55	IDT6167SA35P
MB81C67-55-W	IDT6167SA55xM
MB81C68-35C	IDT6168SA35L
MB81C68-35P	IDT6168SA35P
MB81C68-35Z	IDT6168SA35D
MB81C68-45-W	IDT6168SA45xM
MB81C68-45C	IDT6168SA35L
MB81C68-45P	IDT6168SA35P
MB81C68-45Z	IDT6168SA35D
MB81C68-55-W	IDT6168SA55xM
MB81C68A-25C	IDT6168SA25L
MB81C68A-25P	IDT6168SA25P
MB81C68A-25Z	IDT6168SA25D
MB81C68A-30C	IDT6168SA25L
MB81C68A-30P	IDT6168SA25P
MB81C68A-30Z	IDT6168SA25D
MB81C68A-35C	IDT6168SA35L
MB81C68A-35P	IDT6168SA35P

FUJITSU CONT.	IDT
MB81C68A-35Z	IDT6168SA35D
MB81C69A-25C	IDT6168SA15L
MB81C69A-25P	IDT6168SA15P
MB81C69A-25Z	IDT6168SA15D
MB81C69A-30C	IDT6168SA15L
MB81C69A-30P	IDT6168SA15P
MB81C69A-30Z	IDT6168SA15D
MB81C69A-35C	IDT6168SA20L
MB81C69A-35P	IDT6168SA20P
MB81C69A-35Z	IDT6168SA20D
MB81C71-35	IDT7187S35P
MB81C71-45C	IDT7187S45L22
MB81C71-45Z	IDT7187S45D
MB81C71-55C	IDT7187S45L22
MB81C71-55Z	IDT7187S45D
MB81C74-25x	IDT7188S25x
MB81C74-35x	IDT7188S35x
MB81C75-35	IDT7198S35P
MB81C75-45	IDT7198S45P
MB81C75-55	IDT7198S45P
MB81C78-45	IDT7164S45P
MB81C78-55	IDT7164S45P
MB81C78-70	IDT7164S45P
MB81C78A-35CV	IDT7164S35L22
MB81C78A-35P	IDT7164S35P
MB81C78A-35PF	IDT7164S35SO
MB81C81-35	IDT71257S35P
MB81C81-45	IDT71257S45P
MB81C81-55	IDT71257S55P
MB81C84-45	IDT71258S45P
MB81C84-55	IDT71258S55P
MB8416A-12x	IDT6116LA45P
MB8416A-12x	IDT6116LA45D
MB8416A-12x	IDT6116LA45TP
MB8464-15-W	IDT7164S150DM
MB8464-15-W	IDT7164S150L32M
MB8464-20-W	IDT7164S200DM
MB8464-20-W	IDT7164S200L32M
MB8464A-10-W	IDT7164L100DM
MB8464A-10-W	IDT7164L100L32M
MB8464A-15-W	IDT7164L150DM
MB8464A-15-W	IDT7164L150L32M
MB8464A-70x	IDT7164L45L32
MB8464A-70x	IDT7164L45P
MB8464A-70x	IDT7164L45SO
MB84256-10	IDT71256L70L
MB84256-10	IDT71256L70P
MB84256-10	IDT71256L70SO

HARRIS	IDT
HM1-6516B-8	IDT6116SA120DB
HM1-65162-8	IDT6116LA90DB
HM1-65162B-8	IDT6116LA70DB
HM1-65162C-8	IDT6116SA90DB
HM1-65162S-5	IDT6116LA45D
HM4-65162-8	IDT6116LA90DB
HM4-65162C-8	IDT6116SA90LB
HM4-65162S-5	IDT6116LA45L
HM1-65262-8	IDT6167SA70DB
HM1-65262B-8	IDT6167SA70DB
HM4-65262-8	IDT6167SA70LB
HM4-65262B-8	IDT6167SA70LB
HM1-65642-8	IDT7164L150DB
HM4-65642-8	IDT7164L150L32B

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

HITACHI	IDT
HM6116-2	IDT6116SA45D
HM6116FP-2	IDT6116SA45F
HM6116LFP-2	IDT6116LA45SO
HM6116LP-2	IDT6116LA45P
HM6116P-2	IDT6116SA45P
HM6116ALP-12	IDT6116LA45P
HM6116ALSP-12	IDT6116LA45TP
HM6116AP-12	IDT6116LA45P
HM6116ASP-12	IDT6116LA45TP
HM6167H-45	IDT6167SA35D
HM6167H-55	IDT6167SA35D
HM6167HCG-45	IDT6167SA35L
HM6167HCG-55	IDT6167SA35L
HM6167HLP-45	IDT6167LA35P
HM6167HLP-55	IDT6167LA35P
HM6167HP-45	IDT6167SA35P
HM6167HP-55	IDT6167SA35P
HM6168H-45	IDT6168SA35D
HM6168H-55	IDT6168SA35D
HM6168HLP-45	IDT6168LA35P
HM6168HLP-55	IDT6168LA35P
HM6168HP-45	IDT6168SA35P
HM6168HP-55	IDT6168SA35P
HM62256LFP-10SL	IDT71256L70P
HM62256LFP-8	IDT71256L70SO
HM62256LP-10SL	IDT71256L70P
HM62256LP-8	IDT71256L70P
HM62256P-8	IDT71256S70P
HM6264FP-10	IDT7164S45SO
HM6264LFP-10	IDT7164L45SO
HM6264LFP-10L	IDT7164L45SO
HM6264LP-10	IDT7164L45P
HM6264LP-10L	IDT7164L45P
HM6264LP-10SL	IDT7164L45P
HM6264P-10	IDT7164S45P
HM6264AFP-12	IDT7164S45SO
HM6264ALFP-12	IDT7164L45SO
HM6264ALSP-12	IDT7164L45TC
HM6264ASP-12	IDT7164S45TC
HM6267CG-35	IDT6167SA35L
HM6267CG-45	IDT6167SA35L
HM6267LP-35	IDT6167LA35P
HM6267LP-45	IDT6167LA35P
HM6267P-35	IDT6167SA35P
HM6267P-45	IDT6167SA35P
HM6268LP-25	IDT6168LA25P
HM6268LP-35	IDT6168LA35P
HM6268P-25	IDT6168SA25P
HM6268P-35	IDT6168SA35P
HM6287CG-45	IDT7187S45L
HM6287CG-55	IDT7187S45L
HM6287CG-70	IDT7187S45L
HM6287LP-45	IDT7187L45P
HM6287LP-55	IDT7187L45P
HM6287LP-70	IDT7187L45P
HM6287P-45	IDT7187S45P
HM6287P-55	IDT7187S45P
HM6287P-70	IDT7187S45P
HM6288P-35	IDT7188S35P
HM6288P-45	IDT7188S45P
HM6288P-55	IDT7188S55P
HM65256AP-12	IDT71256S70P
HM6716	IDT6116SA25TD
HM6716-30	IDT6116SA30TD
HM6787	IDT7187S25C
HM6787-30	IDT7187S30C
HM6787CG	IDT7187S25L22
HM6787CG-30	IDT7187S30L22
HM6788	IDT7188S25C
HM6789	IDT6198S25C
HM6789-30	IDT6198S30C

INMOS	IDT
IMS1400P-35	IDT6167SA35P
IMS1400S-45M	IDT6167SA45DB
IMS1400S-55M	IDT6167SA55DB
IMS1400S-70M	IDT6167SA70DB
IMS1400W-35	IDT6167SA35L
IMS1400W-45M	IDT6167SA45LB
IMS1400W-55M	IDT6167SA55LB
IMS1400W-70M	IDT6167SA70LB
IMS1403P-25	IDT6167SA25P
IMS1403P-35	IDT6167SA35P
IMS1403S-25	IDT6167SA25D
IMS1403S-35	IDT6167SA35D
IMS1403W-25	IDT6167SA25L
IMS1403W-35	IDT6167SA35L
IMS1420S-55M	IDT6168SA55DB
IMS1420S-70M	IDT6168SA70DB
IMS1420W-55M	IDT6168SA55LB
IMS1420W-70M	IDT6168SA70LB
IMS1423P-25	IDT6168SA25P
IMS1423P-35	IDT6168SA35P
IMS1423S-25	IDT6168SA25D
IMS1423S-35	IDT6168SA35D
IMS1423S-35M	IDT6168SA35DB
IMS1423S-45M	IDT6168SA45DB
IMS1423S-55M	IDT6168SA55DB
IMS1423W-25	IDT6168SA25L
IMS1423W-35	IDT6168SA35L
IMS1423W-35M	IDT6168SA35LB
IMS1423W-45M	IDT6168SA45LB
IMS1423W-55M	IDT6168SA55LB
IMS1433x-35	IDT6116SA35
IMS1600S-45	IDT7187S45C
IMS1600S-55M	IDT7187S55CB
IMS1600S-70M	IDT7187S70CB
IMS1600W-45	IDT7187S45L
IMS1600W-55M	IDT7187S55LB
IMS1600W-70M	IDT7187S70LB
IMS1620S-45	IDT7188S45C
IMS1620S-55M	IDT7188S55CB
IMS1620S-70M	IDT7188S70CB
IMS1624S-45	IDT6198S45C
IMS1624S-55M	IDT6198S55CB
IMS1624S-70M	IDT6198S70CB
IMS1624W-45	IDT6198S45L
IMS1624W-55M	IDT6198S55LB
IMS1624W-70M	IDT6198S70LB
IMS1630S-45	IDT7164S45D
IMS1800x-35	IDT71257S35x
IMS1820P-35	IDT71258S35P
IMS1820P-45	IDT71258S45P
IMS1820P-55	IDT71258S55P
IMS1830x-45	IDT71256S45x

MATRA-HARRIS	IDT
HM1-2064-2	IDT7164L150DM
HM1-2064-5	IDT7164L45D
HM1-2064-8	IDT7164L150DB
HM3-2064-5	IDT7164L45P
HM3-2064U-5	IDT7164L45P
HM4-2064-2	IDT7164L150L32M
HM4-2064-5	IDT7164L45L32
HM4-2064-8	IDT7164L150L32B
HMT-2064-5	IDT7164L45SO
HMT-2064U-5	IDT7164L45SO
HM1-6116-2	IDT6116SA90DM
HM1-6116-5	IDT6116SA45D
HM1-6116-8	IDT6116SA120DB
HM1-6116L-2	IDT6116LA90DM
HM1-6116L-5	IDT6116LA45D
HM1-6116L-8	IDT6116LA120DB

MATRA-HARRIS CONT.	IDT
HM3-6116-5	IDT6116SA45P
HM3-6116L-5	IDT6116LA45P
HM4-6116-2	IDT6116SA90L32M
HM4-6116-5	IDT6116SA45L32
HM4-6116-8	IDT6116SA120L32B
HM4-6116L-2	IDT6116LA90L32M
HM4-6116L-5	IDT6116LA45L32
HM1-65161-2	IDT6116LA90DM
HM1-65161-5	IDT6116LA45D
HM1-65161-8	IDT6116LA90DB
HM3-65161-5	IDT6116LA45P
HM4-65161-2	IDT6116LA90L32M
HM4-65161-5	IDT6116LA45L32
HM4-65161-8	IDT6116LA90L32B
HM1-65163-2	IDT6116LA85DM
HM1-65163-5	IDT6116LA45D
HM1-65163-8	IDT6116LA85DB
HM3-65163-5	IDT6116LA45P
HM4-65163-2	IDT6116LA55LM
HM4-65163-5	IDT6116LA45L
HM4-65163-8	IDT6116LA45LB
HM1-65261-2	IDT6167LA85DM
HM1-65261-5	IDT6167LA35D
HM1-65261-8	IDT6167LA85DB
HM1-65261B-2	IDT6167LA70DM
HM1-65261B-5	IDT6167LA35D
HM1-65261B-8	IDT6167LA70DB
HM1-65261C-2	IDT6167SA100DM
HM1-65261C-5	IDT6167SA35D
HM1-65261C-8	IDT6167SA100DB
HM1-65261S-2	IDT6167SA70DM
HM1-65261S-5	IDT6167SA35D
HM1-65261S-8	IDT6167SA70DB
HM3-65261-5	IDT6167LA35P
HM3-65261B-5	IDT6167LA35P
HM3-65261C-5	IDT6167SA35P
HM3-65261S-5	IDT6167SA35P
HM4-65261-2	IDT6167LA85LM
HM4-65261-5	IDT6167LA35L
HM4-65261-8	IDT6167LA85LB
HM4-65261B-2	IDT6167LA70LM
HM4-65261B-5	IDT6167LA35L
HM4-65261B-8	IDT6167LA70LB
HM4-65261C-2	IDT6167SA100LM
HM4-65261C-5	IDT6167SA35L
HM4-65261C-8	IDT6167SA100LB
HM4-65261S-2	IDT6167SA70LM
HM4-65261S-5	IDT6167SA35L
HM4-65261S-8	IDT6167SA70LB
HM1-65263-2	IDT6167LA55DM
HM1-65263-5	IDT6167LA35D
HM3-65263-5	IDT6167LA35P
HM4-65263-2	IDT6167LA55LM
HM4-65263-5	IDT6167LA35L
HM1-65641-2	IDT7164L85DM
HM1-65641-5	IDT7164L45D
HM1-65641-8	IDT7164L85DB
HM1-65641S-2	IDT7164L55DM
HM1-65641S-5	IDT7164L45D
HM1-65641S-8	IDT7164L55DB
HM3-65641-5	IDT7164L45P
HM4-65641-2	IDT7164L85L32M
HM4-65641-5	IDT7164L45L32
HM4-65641-8	IDT7164L85L32B
HM1-65681-2	IDT6168LA85DM
HM1-65681-5	IDT6168LA35D
HM1-65681-8	IDT6168LA85DB

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

MATRA-HARRIS CONT.	IDT
HM1-65681B-2	IDT6168LA70DM
HM1-65681B-5	IDT6168LA35D
HM1-65681C-2	IDT6168SA85DM
HM1-65681C-5	IDT6168SA35D
HM1-65681C-8	IDT6168SA85DB
HM1-65681S-2	IDT6168SA70DM
HM1-65681S-5	IDT6168SA35D
HM1-65681S-8	IDT6168SA70DB
HM3-65681-5	IDT6168LA35P
HM3-65681B-5	IDT6168LA35P
HM3-65681C-5	IDT6168SA35P
HM3-65681S-5	IDT6168SA35P
HM4-65681-2	IDT6168LA85LM
HM4-65681-5	IDT6168LA35L
HM4-65681-8	IDT6168LA85LB
HM4-65681B-2	IDT6168LA70LM
HM4-65681B-5	IDT6168LA35L
HM4-65681C-2	IDT6168SA85LM
HM4-65681C-5	IDT6168SA35L
HM4-65681C-8	IDT6168SA85LB
HM4-65681S-2	IDT6168SA70LM
HM4-65681S-5	IDT6168SA35L
HM4-65681S-8	IDT6168SA70LB
HM1-65682-2	IDT6168LA55DM
HM1-65682-5	IDT6168LA35D
HM1-65682-8	IDT6168LA45DB
HM3-65682-5	IDT6168LA35P
HM4-65682-2	IDT6168LA55LM
HM4-65682-5	IDT6168LA35L
HM4-65682-8	IDT6168LA55LB
HM1-65728K-5	IDT6116SA35D
HM1-65728M-2	IDT6116SA45DM
HM1-65728M-5	IDT6116SA45D
HM1-65728M-5	IDT6116SA45L24
HM1-65728N-2	IDT6116SA55DM
HM1-65728N-2	IDT6116SA55L24M
HM1-65728N-5	IDT6116SA45D
HM1-65728N-5	IDT6116SA45L24
HM3-65728K-5	IDT6116SA35TP
HM3-65728M-5	IDT6116SA45TP
HM3-65728N-5	IDT6116SA45TP
HM4-65728K-5	IDT6116SA35L24
HM4-65728M-2	IDT6116SA45L24M
HM1-65767H-5	IDT6167SA25D
HM1-65767K-2	IDT6167SA35DM
HM1-65767K-5	IDT6167SA35D
HM1-65767K-8	IDT6167SA35DB
HM1-65767M-2	IDT6167SA45DM
HM1-65767M-5	IDT6167SA35D
HM1-65767M-8	IDT6167SA45DB
HM3-65767H-5	IDT6167SA25P
HM3-65767K-5	IDT6167SA35P
HM3-65767M-5	IDT6167SA35P
HM4-65767H-5	IDT6167SA25L
HM4-65767K-2	IDT6167SA35LM
HM4-65767K-5	IDT6167SA35L
HM4-65767K-8	IDT6167SA35LB
HM4-65767M-2	IDT6167SA45LM
HM4-65767M-5	IDT6167SA35L
HM4-65767M-8	IDT6167SA45LB
HM1-65768H-5	IDT6168SA25D
HM1-65768K-2	IDT6168SA35DM
HM1-65768K-5	IDT6168SA35D
HM1-65768K-8	IDT6168SA35DB
HM1-65768M-2	IDT6168SA45DM
HM1-65768M-5	IDT6168SA35D
HM1-65768M-8	IDT6168SA45DB
HM3-65768H-5	IDT6168SA25P
HM3-65768K-5	IDT6168SA35P
HM3-65768M-5	IDT6168SA35P
HM4-65768H-5	IDT6168SA25L
HM4-65768K-2	IDT6168SA35LM
HM4-65768K-5	IDT6168SA35L
HM4-65768K-8	IDT6168SA35LB
HM4-65768M-2	IDT6168SA45LM

MATRA-HARRIS CONT.	IDT
HM4-65768M-5	IDT6168SA35L
HM4-65768M-8	IDT6168SA45LB
HM1-65769H-5	IDT6168SA15D
HM1-65769K-2	IDT6168SA20DM
HM1-65769K-5	IDT6168SA20D
HM1-65769K-8	IDT6168SA20DB
HM1-65769M-2	IDT6168SA25DM
HM1-65769M-5	IDT6168SA25D
HM1-65769M-8	IDT6168SA25DB
HM3-65769H-5	IDT6168SA15P
HM3-65769K-5	IDT6168SA20P
HM3-65769M-5	IDT6168SA25P
HM4-65769H-5	IDT6168SA15L
HM4-65769K-2	IDT6168SA20LM
HM4-65769K-5	IDT6168SA20L
HM4-65769K-8	IDT6168SA20LB
HM4-65769M-2	IDT6168SA25LM
HM4-65769M-5	IDT6168SA25L
HM4-65769M-8	IDT6168SA25LB

MICRON	IDT
MT5C1601-15	IDT6167SA15P
MT5C1601-20	IDT6167SA20P
MT5C1601-25	IDT6167SA25P
MT5C1601-30	IDT6167SA30P
MT5C1601-35	IDT6167SA35P
MT5C1601DJ-15	IDT6167SA15Y
MT5C1601DJ-20	IDT6167SA20Y
MT5C1601DJ-25	IDT6167SA25Y
MT5C1601DJ-30	IDT6167SA30Y
MT5C1601DJ-35	IDT6167SA35Y
MT5C1601EC-15	IDT6167SA15L
MT5C1601EC-20	IDT6167SA20L
MT5C1601EC-25	IDT6167SA25L
MT5C1601EC-30	IDT6167SA30L
MT5C1601EC-35	IDT6167SA35L
MT5C1601-15L	IDT6167LA15P
MT5C1601-20L	IDT6167LA20P
MT5C1601-25L	IDT6167LA25P
MT5C1601-30L	IDT6167LA30P
MT5C1601-35L	IDT6167LA35P
MT5C1601DJ-15L	IDT6167LA15Y
MT5C1601DJ-20L	IDT6167LA20Y
MT5C1601DJ-25L	IDT6167LA25Y
MT5C1601DJ-30L	IDT6167LA30Y
MT5C1601DJ-35L	IDT6167LA35Y
MT5C1601EC-15L	IDT6167LA15L
MT5C1601EC-20L	IDT6167LA20L
MT5C1601EC-25L	IDT6167LA25L
MT5C1601EC-30L	IDT6167LA30L
MT5C1601EC-35L	IDT6167LA35L
MT5C1604-15	IDT6168SA15P
MT5C1604-20	IDT6168SA20P
MT5C1604-25	IDT6168SA25P
MT5C1604-35	IDT6168SA35P
MT5C1604DJ-15	IDT6168SA15Y
MT5C1604DJ-20	IDT6168SA20Y
MT5C1604DJ-25	IDT6168SA25Y
MT5C1604DJ-35	IDT6168SA35Y
MT5C1604EC-15	IDT6168SA15L
MT5C1604EC-20	IDT6168SA20L
MT5C1604EC-25	IDT6168SA25L
MT5C1604EC-35	IDT6168SA35L
MT5C1604-15L	IDT6168LA15P
MT5C1604-20L	IDT6168LA20P
MT5C1604-25L	IDT6168LA25P
MT5C1604-35L	IDT6168LA35P
MT5C1604DJ-15L	IDT6168LA15Y
MT5C1604DJ-20L	IDT6168LA20Y
MT5C1604DJ-25L	IDT6168LA25Y
MT5C1604DJ-35L	IDT6168LA35Y
MT5C1604EC-15L	IDT6168LA15L
MT5C1604EC-20L	IDT6168LA20L
MT5C1604EC-25L	IDT6168LA25L

MICRON CONT.	IDT
MT5C1604EC-35L	IDT6168LA35L
MT5C1605-15	IDT6198SA15P
MT5C1605-20	IDT6198SA20P
MT5C1605-25	IDT6198SA25P
MT5C1605-30	IDT6198SA30P
MT5C1605-35	IDT6198SA35P
MT5C1605DJ-15	IDT6198SA15Y
MT5C1605DJ-20	IDT6198SA20Y
MT5C1605DJ-25	IDT6198SA25Y
MT5C1605DJ-30	IDT6198SA30Y
MT5C1605DJ-35	IDT6198SA35Y
MT5C1605EC-15	IDT6198SA15L
MT5C1605EC-20	IDT6198SA20L
MT5C1605EC-25	IDT6198SA25L
MT5C1605EC-30	IDT6198SA30L
MT5C1605EC-35	IDT6198SA35L
MT5C1605-15L	IDT6198LA15P
MT5C1605-20L	IDT6198LA20P
MT5C1605-25L	IDT6198LA25P
MT5C1605-30L	IDT6198LA30P
MT5C1605-35L	IDT6198LA35P
MT5C1605DJ-15L	IDT6198LA15Y
MT5C1605DJ-20L	IDT6198LA20Y
MT5C1605DJ-25L	IDT6198LA25Y
MT5C1605DJ-30L	IDT6198LA30Y
MT5C1605DJ-35L	IDT6198LA35Y
MT5C1605EC-15L	IDT6198LA15L
MT5C1605EC-20L	IDT6198LA20L
MT5C1605EC-25L	IDT6198LA25L
MT5C1605EC-30L	IDT6198LA30L
MT5C1605EC-35L	IDT6198LA35L
MT5C1608-15	IDT6116SA15TP
MT5C1608-20	IDT6116SA20TP
MT5C1608-25	IDT6116SA25TP
MT5C1608-30	IDT6116SA30TP
MT5C1608-35	IDT6116SA35TP
MT5C1608DJ-15	IDT6116SA15Y
MT5C1608DJ-20	IDT6116SA20Y
MT5C1608DJ-25	IDT6116SA25Y
MT5C1608DJ-30	IDT6116SA30Y
MT5C1608DJ-35	IDT6116SA35Y
MT5C1608EC-15	IDT6116SA15L28
MT5C1608EC-20	IDT6116SA20L28
MT5C1608EC-25	IDT6116SA25L28
MT5C1608EC-30	IDT6116SA30L28
MT5C1608EC-35	IDT6116SA35L28
MT5C1608-15L	IDT6116LA15TP
MT5C1608-20L	IDT6116LA20TP
MT5C1608-25L	IDT6116LA25TP
MT5C1608-30L	IDT6116LA30TP
MT5C1608-35L	IDT6116LA35TP
MT5C1608DJ-15L	IDT6116LA15Y
MT5C1608DJ-20L	IDT6116LA20Y
MT5C1608DJ-25L	IDT6116LA25Y
MT5C1608DJ-30L	IDT6116LA30Y
MT5C1608DJ-35L	IDT6116LA35Y
MT5C1608EC-15L	IDT6116LA15L28
MT5C1608EC-20L	IDT6116LA20L28
MT5C1608EC-25L	IDT6116LA25L28
MT5C1608EC-30L	IDT6116LA30L28
MT5C1608EC-35L	IDT6116LA35L28
MT5C6401-15	IDT7187S15P
MT5C6401-20	IDT7187S20P
MT5C6401-25	IDT7187S25P

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

MICRON CONT.	IDT
MT5C6401-30	IDT7187S30P
MT5C6401-35	IDT7187S35P
MT5C6401C-15	IDT7187S15C
MT5C6401C-20	IDT7187S20C
MT5C6401C-25	IDT7187S25C
MT5C6401C-30	IDT7187S30C
MT5C6401C-35	IDT7187S35C
MT5C6401DJ-15	IDT7187S15Y
MT5C6401DJ-20	IDT7187S20Y
MT5C6401DJ-25	IDT7187S25Y
MT5C6401DJ-30	IDT7187S30Y
MT5C6401DJ-35	IDT7187S35Y
MT5C6401EC-15	IDT7187S15L22
MT5C6401EC-20	IDT7187S20L22
MT5C6401EC-25	IDT7187S25L22
MT5C6401EC-30	IDT7187S30L22
MT5C6401EC-35	IDT7187S35L22
MT5C6401-15L	IDT7187L15P
MT5C6401-20L	IDT7187L20P
MT5C6401-25L	IDT7187L25P
MT5C6401-30L	IDT7187L30P
MT5C6401-35L	IDT7187L35P
MT5C6401C-15L	IDT7187L15C
MT5C6401C-20L	IDT7187L20C
MT5C6401C-25L	IDT7187L25C
MT5C6401C-30L	IDT7187L30C
MT5C6401C-35L	IDT7187L35C
MT5C6401DJ-15L	IDT7187L15Y
MT5C6401DJ-20L	IDT7187L20Y
MT5C6401DJ-25L	IDT7187SL25Y
MT5C6401DJ-30L	IDT7187L30Y
MT5C6401DJ-35L	IDT7187L35Y
MT5C6401EC-15L	IDT7187L15L22
MT5C6401EC-20L	IDT7187L20L22
MT5C6401EC-25L	IDT7187L25L22
MT5C6401EC-30L	IDT7187L30L22
MT5C6401EC-35L	IDT7187L35L22
MT5C6404-15	IDT7188S15P
MT5C6404-20	IDT7188S20P
MT5C6404-25	IDT7188S25P
MT5C6404-30	IDT7188S30P
MT5C6404-35	IDT7188S35P
MT5C6404C-15	IDT7188S15C
MT5C6404C-20	IDT7188S20C
MT5C6404C-25	IDT7188S25C
MT5C6404C-30	IDT7188S30C
MT5C6404C-35	IDT7188S35C
MT5C6404DJ-15	IDT7188S15Y
MT5C6404DJ-20	IDT7188S20Y
MT5C6404DJ-25	IDT7188S25Y
MT5C6404DJ-30	IDT7188S30Y
MT5C6404DJ-35	IDT7188S35Y
MT5C6404-15L	IDT7188L15P
MT5C6404-20L	IDT7188L20P
MT5C6404-25L	IDT7188L25P
MT5C6404-30L	IDT7188L30P
MT5C6404-35L	IDT7188L35P
MT5C6404C-15L	IDT7188L15C
MT5C6404C-20L	IDT7188L20C
MT5C6404C-25L	IDT7188L25C
MT5C6404C-30L	IDT7188L30C
MT5C6404C-35L	IDT7188L35C
MT5C6404DJ-15L	IDT7188L15Y
MT5C6404DJ-20L	IDT7188L20Y
MT5C6404DJ-25L	IDT7188L25Y
MT5C6404DJ-30L	IDT7188L30Y
MT5C6404DJ-35L	IDT7188L35Y
MT5C6405-15	IDT7198S15P
MT5C6405-20	IDT7198S20P
MT5C6405-25	IDT7198S25P
MT5C6405-30	IDT7198S30P
MT5C6405-35	IDT7198S35P
MT5C6405C-15	IDT7198S15C
MT5C6405C-20	IDT7198S20C
MT5C6405C-25	IDT7198S25C

MICRON CONT.	IDT
MT5C6405C-30	IDT7198S30C
MT5C6405C-35	IDT7198S35C
MT5C6405DJ-15	IDT7198S15Y
MT5C6405DJ-20	IDT7198S20Y
MT5C6405DJ-25	IDT7198S25Y
MT5C6405DJ-30	IDT7198S30Y
MT5C6405DJ-35	IDT7198S35Y
MT5C6405-15L	IDT7198L15P
MT5C6405-20L	IDT7198L20P
MT5C6405-25L	IDT7198L25P
MT5C6405-30L	IDT7198L30P
MT5C6405-35L	IDT7198L35P
MT5C6405C-15L	IDT7198L15C
MT5C6405C-20L	IDT7198L20C
MT5C6405C-25L	IDT7198L25C
MT5C6405C-30L	IDT7198L30C
MT5C6405C-35L	IDT7198L35C
MT5C6405DJ-15L	IDT7198L15Y
MT5C6405DJ-20L	IDT7198L20Y
MT5C6405DJ-25L	IDT7198L25Y
MT5C6405DJ-30L	IDT7198L30Y
MT5C6405DJ-35L	IDT7198L35Y
MT5C6408-20	IDT7164S20TP
MT5C6408-25	IDT7164S25TP
MT5C6408-30	IDT7164S30TP
MT5C6408-35	IDT7164S35TP
MT5C6408C-20	IDT7164S20TC
MT5C6408C-25	IDT7164S25TC
MT5C6408C-30	IDT7164S30TC
MT5C6408C-35	IDT7164S35TC
MT5C6408DJ-20	IDT7164S20Y
MT5C6408DJ-25	IDT7164S25Y
MT5C6408DJ-30	IDT7164S30Y
MT5C6408DJ-35	IDT7164S35Y
MT5C6408EC-20	IDT7164S20L32
MT5C6408EC-25	IDT7164S25L32
MT5C6408EC-30	IDT7164S30L32
MT5C6408EC-35	IDT7164S35L32
MT5C6408-20L	IDT7164L20TP
MT5C6408-25L	IDT7164L25TP
MT5C6408-30L	IDT7164L30TP
MT5C6408-35L	IDT7164L35TP
MT5C6408C-20L	IDT7164L20TC
MT5C6408C-25L	IDT7164L25TC
MT5C6408C-30L	IDT7164L30TC
MT5C6408C-35L	IDT7164L35TC
MT5C6408DJ-20L	IDT7164L20Y
MT5C6408DJ-25L	IDT7164L25Y
MT5C6408DJ-30L	IDT7164L30Y
MT5C6408DJ-35L	IDT7164L35Y
MT5C6408EC-20L	IDT7164S20L32
MT5C6408EC-25L	IDT7164S25L32
MT5C6408EC-30L	IDT7164S30L32
MT5C6408EC-35L	IDT7164S35L32
MT5C2561-25	IDT71257S25P
MT5C2561-30	IDT71257S30P
MT5C2561-35	IDT71257S35P
MT5C2561-45	IDT71257S45P
MT5C2561-55	IDT71257S55P
MT5C2561C-25	IDT71257S25C
MT5C2561C-30	IDT71257S30C
MT5C2561C-35	IDT71257S35C
MT5C2561C-45	IDT71257S45C
MT5C2561C-55	IDT71257S55C
MT5C2561DJ-25	IDT71257S25Y
MT5C2561DJ-30	IDT71257S30Y
MT5C2561DJ-35	IDT71257S35Y
MT5C2561DJ-45	IDT71257S45Y
MT5C2561DJ-55	IDT71257S55Y
MT5C2561EC-25	IDT71257S25L
MT5C2561EC-30	IDT71257S30L
MT5C2561EC-35	IDT71257S35L
MT5C2561EC-45	IDT71257S45L
MT5C2561EC-55	IDT71257S55L
MT5C2561-25L	IDT71257L25P

MICRON CONT.	IDT
MT5C2561-30L	IDT71257L30P
MT5C2561-35L	IDT71257L35P
MT5C2561-45L	IDT71257L45P
MT5C2561-55L	IDT71257L55P
MT5C2561C-25L	IDT71257L25C
MT5C2561C-30L	IDT71257L30C
MT5C2561C-35L	IDT71257L35C
MT5C2561C-45L	IDT71257L45C
MT5C2561C-55L	IDT71257L55C
MT5C2561DJ-25L	IDT71257L25Y
MT5C2561DJ-30L	IDT71257L30Y
MT5C2561DJ-35L	IDT71257L35Y
MT5C2561DJ-45L	IDT71257L45Y
MT5C2561DJ-55L	IDT71257L55Y
MT5C2561EC-25L	IDT71257L25L
MT5C2561EC-30L	IDT71257L30L
MT5C2561EC-35L	IDT71257L35L
MT5C2561EC-45L	IDT71257L45L
MT5C2561EC-55L	IDT71257L55L
MT5C2564-25	IDT71258S25P
MT5C2564-30	IDT71258S30P
MT5C2564-35	IDT71258S35P
MT5C2564-45	IDT71258S45P
MT5C2564-55	IDT71258S55P
MT5C2564C-25	IDT71258S25C
MT5C2564C-30	IDT71258S30C
MT5C2564C-35	IDT71258S35C
MT5C2564C-45	IDT71258S45C
MT5C2564C-55	IDT71258S55C
MT5C2564DJ-25	IDT71258S25Y
MT5C2564DJ-30	IDT71258S30Y
MT5C2564DJ-35	IDT71258S35Y
MT5C2564DJ-45	IDT71258S45Y
MT5C2564DJ-55	IDT71258S55Y
MT5C2564EC-25	IDT71258S25L
MT5C2564EC-30	IDT71258S30L
MT5C2564EC-35	IDT71258S35L
MT5C2564EC-45	IDT71258S45L
MT5C2564EC-55	IDT71258S55L
MT5C2564-25L	IDT71258L25P
MT5C2564-30L	IDT71258L30P
MT5C2564-35L	IDT71258L35P
MT5C2564-45L	IDT71258L45P
MT5C2564-55L	IDT71258L55P
MT5C2564C-25L	IDT71258L25C
MT5C2564C-30L	IDT71258L30C
MT5C2564C-35L	IDT71258L35C
MT5C2564C-45L	IDT71258L45C
MT5C2564C-55L	IDT71258L55C
MT5C2564DJ-25L	IDT71258L25Y
MT5C2564DJ-30L	IDT71258L30Y
MT5C2564DJ-35L	IDT71258L35Y
MT5C2564DJ-45L	IDT71258L45Y
MT5C2564DJ-55L	IDT71258L55Y
MT5C2564EC-25L	IDT71258L25L
MT5C2564EC-30L	IDT71258L30L
MT5C2564EC-35L	IDT71258L35L
MT5C2564EC-45L	IDT71258L45L
MT5C2564EC-55L	IDT71258L55L
MT5C2565-25	IDT61298S25P
MT5C2565-30	IDT61298S30P
MT5C2565-35	IDT61298S35P
MT5C2565-45	IDT61298S45P
MT5C2565-55	IDT61298S55P
MT5C2565C-25	IDT61298S25C
MT5C2565C-30	IDT61298S30C
MT5C2565C-35	IDT61298S35C

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

MICRON CONT.	IDT
MT5C2565C-45	IDT61298S45C
MT5C2565C-55	IDT61298S55C
MT5C2565DJ-25	IDT61298S25Y
MT5C2565DJ-30	IDT61298S30Y
MT5C2565DJ-35	IDT61298S35Y
MT5C2565DJ-45	IDT61298S45Y
MT5C2565DJ-55	IDT61298S55Y
MT5C2565EC-25	IDT61298S25L
MT5C2565EC-30	IDT61298S30L
MT5C2565EC-35	IDT61298S35L
MT5C2565EC-45	IDT61298S45L
MT5C2565EC-55	IDT61298S55L
MT5C2565-25L	IDT61298L25P
MT5C2565-30L	IDT61298L30P
MT5C2565-35L	IDT61298L35P
MT5C2565-45L	IDT61298L45P
MT5C2565-55L	IDT61298L55P
MT5C2565C-25L	IDT61298L25C
MT5C2565C-30L	IDT61298L30C
MT5C2565C-35L	IDT61298L35C
MT5C2565C-45L	IDT61298L45C
MT5C2565C-55L	IDT61298L55C
MT5C2565DJ-25L	IDT61298L25Y
MT5C2565DJ-30L	IDT61298L30Y
MT5C2565DJ-35L	IDT61298L35Y
MT5C2565DJ-45L	IDT61298L45Y
MT5C2565DJ-55L	IDT61298L55Y
MT5C2565EC-25L	IDT61298L25L
MT5C2565EC-30L	IDT61298L30L
MT5C2565EC-35L	IDT61298L35L
MT5C2565EC-45L	IDT61298L45L
MT5C2565EC-55L	IDT61298L55L
MT5C2568-25	IDT71256S25TP
MT5C2568-30	IDT71256S30TP
MT5C2568-35	IDT71256S35TP
MT5C2568-45	IDT71256S45TP
MT5C2568-55	IDT71256S55TP
MT5C2568C-25	IDT71256S25D
MT5C2568C-30	IDT71256S30D
MT5C2568C-35	IDT71256S35D
MT5C2568C-45	IDT71256S45D
MT5C2568C-55	IDT71256S55D
MT5C2568DJ-25	IDT71256S25Y
MT5C2568DJ-30	IDT71256S30Y
MT5C2568DJ-35	IDT71256S35Y
MT5C2568DJ-45	IDT71256S45Y
MT5C2568DJ-55	IDT71256S55Y
MT5C2568EC-25	IDT71256S25L32
MT5C2568EC-30	IDT71256S30L32
MT5C2568EC-35	IDT71256S35L32
MT5C2568EC-45	IDT71256S45L32
MT5C2568EC-55	IDT71256S55L32
MT5C2568-25L	IDT71256L25TP
MT5C2568-30L	IDT71256L30TP
MT5C2568-35L	IDT71256L35TP
MT5C2568-45L	IDT71256L45TP
MT5C2568-55L	IDT71256L55TP
MT5C2568C-25L	IDT71256L25D
MT5C2568C-30L	IDT71256L30D
MT5C2568C-35L	IDT71256L35D
MT5C2568C-45L	IDT71256L45D
MT5C2568C-55L	IDT71256L55D
MT5C2568DJ-25L	IDT71256L25Y
MT5C2568DJ-30L	IDT71256L30Y
MT5C2568DJ-35L	IDT71256L35Y
MT5C2568DJ-45L	IDT71256L45Y
MT5C2568DJ-55L	IDT71256L55Y
MT5C2568EC-25L	IDT71256L25L32
MT5C2568EC-30L	IDT71256L30L32
MT5C2568EC-35L	IDT71256L35L32
MT5C2568EC-45L	IDT71256L45L32
MT5C2568EC-55L	IDT71256L55L32

MITSUBISHI	IDT
M5M21C67P-35	IDT6167LA35P
M5M21C67P-45	IDT6167LA35P
M5M21C67P-55	IDT6167LA35P
M5M21C68P-35	IDT6168LA35P
M5M21C68P-45	IDT6168LA35P
M5M21C68P-55	IDT6168LA35P
M5M5165FP-70	IDT7164S45SO
M5M5165FP-70L	IDT7164L45SO
M5M5178P-45	IDT7164L45P
M5M5178P-55	IDT7164L45P
M5M5187AD-25	IDT7187L25L22
M5M5187AD-35	IDT7187L35L22
M5M5187AP-25	IDT7187L25P
M5M5187AP-35	IDT7187L35P
M5M5187P-45	IDT7187L45P
M5M5187P-55	IDT7187L55P
M5M5188AD-25	IDT7188L25L22
M5M5188AD-35	IDT7188L35L22
M5M5188AP-25	IDT7188L25P
M5M5188AP-35	IDT7188L35P
M5M5188P-45	IDT7188L45P
M5M5188P-55	IDT7188L45P
M5M5257P-35	IDT71257S35P
M5M5257P-45	IDT71257S45P
M5M5257P-55	IDT71257S55P
M5M5258P-35	IDT71258S35P
M5M5258P-45	IDT71258S45P
M5M5258P-55	IDT71258S55P

MOTOROLA	IDT
MCM2016HN45	IDT6116SA45TP
MCM2167P45	IDT6167SA45P
MCM4180P25	IDT6178S20P
MCM6164P45	IDT7164S45P
MCM6168P35	IDT6168SA35P
MCM6206P45	IDT71256S45P
MCM6206P55	IDT71256S55P
MCM6207P25	IDT71257S25P
MCM6207P35	IDT71257S35P
MCM6207L25	IDT71257S25C
MCM6207L35	IDT71257S35C
MCM6208P25	IDT71258S25P
MCM6208P35	IDT71258S35P
MCM6208L25	IDT71258S25C
MCM6208L35	IDT71258S35C
MCM6268P25	IDT6168SA25P
MCM6268P35	IDT6168SA35P
MCM6287P35	IDT7187S35P
MCM6287P45	IDT7187S45P
MCM6287P25	IDT7187S25P
MCM6288P25	IDT7188S25P
MCM6288P35	IDT7188S35P
MCM6288P45	IDT7188S45P
MCM6290P25	IDT6198S25P
MCM6290P35	IDT6198S35P
MCM6292C25	IDT61592S25D
MCM6292C35	IDT61592S35D
MCM6293P25	IDT61593S25P
MCM6293P35	IDT61593S35P
MCM6294P25	IDT61594S25P
MCM6294P35	IDT61594S35P
MCM6295C25	IDT61595S25D
MCM6295C35	IDT61595S35D

NEC	IDT
5PD4311C-35	IDT6167SA35P
5PD4311C-45	IDT6167SA35P
5PD4311C-55	IDT6167SA35P
5PD4311D-35	IDT6167SA35D
5PD4311D-45	IDT6167SA35D
5PD4311D-55	IDT6167SA35D
5PD4314C-35	IDT6168SA35P

NEC CONT.	IDT
5PD4314C-45	IDT6168SA35P
5PD4314C-55	IDT6168SA35P
5PD43256C-10	IDT71256S70P
5PD43256C-10L	IDT71256L70P
5PD43256G-10	IDT71256S70SO
5PD43256G-10L	IDT71256L70SO
5PD4361C-45	IDT7187S45P
5PD4361C-45L	IDT7187L45P
5PD4361C-55	IDT7187S45P
5PD4361C-55L	IDT7187L45P
5PD4361C-70	IDT7187S45P
5PD4361C-70L	IDT7187L45P
5PD4361K-40	IDT7187S35L22
5PD4361K-45	IDT7187S45L22
5PD4361K-55	IDT7187S45L22
5PD4362C-45	IDT7188SA45P
5PD4362C-55	IDT7188SA45P
5PD4362C-70	IDT7188SA45P
5PD4364C-12	IDT7164S45P
5PD4364C-12L	IDT7164L45P
5PD4364G-12	IDT7164S45SO
5PD4364G-12L	IDT7164L45SO
5PD446C	IDT6116LA45P
5PD4464C-x	IDT7164L45P
5PD4464G-x	IDT7164L45SO

PERFORMANCE	IDT
P4C116-25DC	IDT6116SA25TD
P4C116-25JC	IDT6116SA25Y
P4C116-25PC	IDT6116SA25TP
P4C116-30DC	IDT6116SA30TD
P4C116-30JC	IDT6116SA30Y
P4C116-30PC	IDT6116SA30TP
P4C116-35DC	IDT6116SA35TD
P4C116-35DM	IDT6116SA35TDM
P4C116-35DMB	IDT6116SA35TDB
P4C116-35JC	IDT6116SA35Y
P4C116-35PC	IDT6116SA35TP
P4C116L-25DC	IDT6116LA25TD
P4C116L-25JC	IDT6116LA25Y
P4C116L-25PC	IDT6116LA25TP
P4C116L-30DC	IDT6116LA30TD
P4C116L-30LC	IDT6116LA30Y
P4C116L-30PC	IDT6116LA30TP
P4C116L-35CC	IDT6116LA35TD
P4C116L-35CM	IDT6116LA35TDM
P4C116L-35CMB	IDT6116LA35TDB
P4C116L-35LC	IDT6116LA35L24
P4C116L-35LM	IDT6116LA35L24M
P4C116L-35LMB	IDT6116LA35L24B
P4C116L-35PC	IDT6116LA35TP
P4C164-25CC	IDT7164S25TC
P4C164-25LC	IDT7164S25L28
P4C164-25PC	IDT7164S25TP
P4C164-25JC	IDT7164S25Y
P4C164-30CC	IDT7164S30TC
P4C164-30LC	IDT7164S30L28
P4C164-30PC	IDT7164S30TP
P4C164-30JC	IDT7164S30Y
P4C164-35CC	IDT7164S35TC
P4C164-35CM	IDT7164S35TCM
P4C164-35CMB	IDT7164S35TCB
P4C164-35LC	IDT7164S30L28
P4C164-35LM	IDT7164S35L28M

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

PERFORMANCE CONT.	IDT
P4C164-35LMB	IDT7164S35L28B
P4C164-35PC	IDT7164S35TP
P4C164-35JC	IDT7164S35Y
P4C164-45CM	IDT7164S45TCM
P4C164-45CMB	IDT7164S45TCB
P4C164-45LM	IDT7164S45L28M
P4C164-45LMB	IDT7164S45L28B
P4C164L-30CC	IDT7164L30TC
P4C164L-30LC	IDT7164L30L28
P4C164L-30PC	IDT7164L30TP
P4C164L-30JC	IDT7164L30Y
P4C164L-35CC	IDT7164L35TC
P4C164L-35CM	IDT7164L35TCM
P4C164L-35CMB	IDT7164L35TCB
P4C164L-35LC	IDT7164L30L28
P4C164L-35LM	IDT7164L35L28M
P4C164L-35LMB	IDT7164L35L28B
P4C164L-35PC	IDT7164L35TP
P4C164L-35JC	IDT7164L35Y
P4C164L-45CM	IDT7164L45TCM
P4C164L-45CMB	IDT7164L45TCB
P4C164L-45LM	IDT7164L45L28M
P4C164L-45LMB	IDT7164L45L28B
P4C168-20DC	IDT6168SA20D
P4C168-20PC	IDT6168SA20P
P4C168-20JC	IDT6168SA20Y
P4C168-25DC	IDT6168SA25D
P4C168-25DM	IDT6168SA25DM
P4C168-25DMB	IDT6168SA25DB
P4C168-25JC	IDT6168SA25Y
P4C168-25PC	IDT6168SA25P
P4C168-35DC	IDT6168SA35D
P4C168-35DM	IDT6168SA35DM
P4C168-35DMB	IDT6168SA35DB
P4C168-35JC	IDT6168SA35Y
P4C168-35PC	IDT6168SA35P
P4C168-45DM	IDT6168SA45DM
P4C168-45DMB	IDT6168SA45DB
P4C168L-20DC	IDT6168LA20D
P4C168L-20JC	IDT6168LA20Y
P4C168L-20PC	IDT6168LA20P
P4C168L-25DC	IDT6168LA25D
P4C168L-25DM	IDT6168LA25DM
P4C168L-25DMB	IDT6168LA25DB
P4C168L-25JC	IDT6168LA25Y
P4C168L-25PC	IDT6168LA25P
P4C168L-35DC	IDT6168LA35D
P4C168L-35DM	IDT6168LA35DM
P4C168L-35DMB	IDT6168LA35DB
P4C168L-35JC	IDT6168LA35Y
P4C168L-35PC	IDT6168LA35P
P4C168L-45DM	IDT6168LA45DM
P4C168L-45DMB	IDT6168LA45DB
P4C1681-20DC	IDT71681SA20D
P4C1681-20LC	IDT71681SA20L
P4C1681-20PC	IDT71681SA20P
P4C1681-25DC	IDT71681SA25D
P4C1681-25CM	IDT71681SA25DM
P4C1681-25CMB	IDT71681SA25DB
P4C1681-25LC	IDT71681SA25L
P4C1681-25LM	IDT71681SA25LM
P4C1681-25LMB	IDT71681SA25LB
P4C1681-25PC	IDT71681SA25P
P4C1681-35DC	IDT71681SA35D
P4C1681-35CM	IDT71681SA35DM
P4C1681-35CMB	IDT71681SA35DB
P4C1681-35LC	IDT71681SA35L
P4C1681-35LM	IDT71681SA35LM
P4C1681-35LMB	IDT71681SA35LB
P4C1681-35PC	IDT71681SA35P
P4C1681-45DC	IDT71681SA45D
P4C1681-45CM	IDT71681SA45DM
P4C1681-45CMB	IDT71681SA45CB
P4C1681-45LC	IDT71681SA45L
P4C1681-45LM	IDT71681SA45LM

PERFORMANCE CONT.	IDT
P4C1681-45LMB	IDT71681SA45LB
P4C1681-45PC	IDT71681SA45P
P4C1681L-20DC	IDT71681LA20D
P4C1681L-20LC	IDT71681LA20L
P4C1681L-20PC	IDT71681LA20P
P4C1681L-25DC	IDT71681LA25D
P4C1681L-25CM	IDT71681LA25DM
P4C1681L-25CMB	IDT71681LA25DB
P4C1681L-25LC	IDT71681LA25L
P4C1681L-25LM	IDT71681LA25LM
P4C1681L-25LMB	IDT71681LA25LB
P4C1681L-25PC	IDT71681LA25P
P4C1681L-35DC	IDT71681LA35D
P4C1681L-35CM	IDT71681LA35DM
P4C1681L-35CMB	IDT71681LA35DB
P4C1681L-35LC	IDT71681LA35L
P4C1681L-35LM	IDT71681LA35LM
P4C1681L-35LMB	IDT71681LA35LB
P4C1681L-35PC	IDT71681LA35P
P4C1681L-45DC	IDT71681LA45D
P4C1681L-45CM	IDT71681LA45DM
P4C1681L-45CMB	IDT71681LA45CB
P4C1681L-45LC	IDT71681LA45L
P4C1681L-45LM	IDT71681LA45LM
P4C1681L-45LMB	IDT71681LA45LB
P4C1681L-45PC	IDT71681LA45P
P4C1682-20CC	IDT71682SA20D
P4C1682-20LC	IDT71682SA20L
P4C1682-20PC	IDT71682SA20P
P4C1682-25CC	IDT71682SA25D
P4C1682-25CM	IDT71682SA25DM
P4C1682-25CMB	IDT71682SA25DB
P4C1682-25LC	IDT71682SA25L
P4C1682-25LM	IDT71682SA25LM
P4C1682-25LMB	IDT71682SA25LB
P4C1682-25PC	IDT71682SA25P
P4C1682-35CC	IDT71682SA35D
P4C1682-35CM	IDT71682SA35DM
P4C1682-35CMB	IDT71682SA35DB
P4C1682-35LC	IDT71682SA35L
P4C1682-35LM	IDT71682SA35LM
P4C1682-35LMB	IDT71682SA35LB
P4C1682-35PC	IDT71682SA35P
P4C1682-45CC	IDT71682SA45D
P4C1682-45CM	IDT71682SA45DM
P4C1682-45CMB	IDT71682SA45CB
P4C1682-45LC	IDT71682SA45L
P4C1682-45LM	IDT71682SA45LM
P4C1682-45LMB	IDT71682SA45LB
P4C1682-45PC	IDT71682SA45P
P4C187-20CC	IDT7187S20C

PERFORMANCE CONT.	IDT
P4C187-20PC	IDT7187S20P
P4C187-20LC	IDT7187S20L22
P4C187-20JC	IDT7187S20Y
P4C187-25CC	IDT7187S25C
P4C187-25CM	IDT7187S25CM
P4C187-25CMB	IDT7187S25CB
P4C187-25PC	IDT7187S25P
P4C187-25LC	IDT7187S25L22
P4C187-25CM	IDT7187S25CM
P4C187-25CMB	IDT7187S25CB
P4C187-25JC	IDT7187S25Y
P4C187-30CM	IDT7187S30CM
P4C187-30CMB	IDT7187S30CB
P4C187-30LM	IDT7187S30L22M
P4C187-30LMB	IDT7187S35L22B
P4C187-35CM	IDT7187S35CM
P4C187-35CMB	IDT7187S35CB
P4C187-35LM	IDT7187S35L22M
P4C187-35LMB	IDT7187S35L22B
P4C187L-20CC	IDT7187L20C
P4C187L-20PC	IDT7187L20P
P4C187L-20LC	IDT7187L20L22
P4C187L-20JC	IDT7187L20Y
P4C187L-25CC	IDT7187L25C
P4C187L-25CM	IDT7187L25CM
P4C187L-25CMB	IDT7187L25CB
P4C187L-25PC	IDT7187L25P
P4C187L-25LC	IDT7187L25L22
P4C187L-25CM	IDT7187L25CM
P4C187L-25CMB	IDT7187L25CB
P4C187L-25JC	IDT7187L25Y
P4C187L-30CM	IDT7187L30CM
P4C187L-30CMB	IDT7187L30CB
P4C187L-30LM	IDT7187L30L22M
P4C187L-30LMB	IDT7187L35L22B
P4C187L-35CM	IDT7187L35CM
P4C187L-35CMB	IDT7187L35CB
P4C187L-35LM	IDT7187L35L22M
P4C187L-35LMB	IDT7187L35L22B
P4C188-20CC	IDT7188S20C
P4C188-20PC	IDT7188S20P
P4C188-20LC	IDT7188S20L
P4C188-20JC	IDT7188S20Y
P4C188-25CC	IDT7188S25C
P4C188-25CM	IDT7188S25CM
P4C188-25CMB	IDT7188S25CB
P4C188-25LC	IDT7188S25L
P4C188-25LM	IDT7188S25LM
P4C188-25LMB	IDT7188S25LB
P4C188-25PC	IDT7188S25P
P4C188-25JC	IDT7188S25Y
P4C188-30CC	IDT7188S30C
P4C188-30CM	IDT7188S30CM
P4C188-30CMB	IDT7188S30CB
P4C188-30LC	IDT7188S30L
P4C188-30LM	IDT7188S30LM
P4C188-30LMB	IDT7188S30LB
P4C188-30PC	IDT7188S30P
P4C188-30JC	IDT7188S30Y
P4C188-35CC	IDT7188S35C
P4C188-35CM	IDT7188S35CM
P4C188-35CMB	IDT7188S35CB
P4C188-35LC	IDT7188S35L
P4C188-35LM	IDT7188S35LM
P4C188-35LMB	IDT7188S35LB
P4C188-35PC	IDT7188S35P
P4C188-35JC	IDT7188S35Y
P4C188-45CM	IDT7188S45CM
P4C188-45CMB	IDT7188S45CB
P4C188-45LM	IDT7188S45LM
P4C188-45LMB	IDT7188S45LB
P4C188-55CM	IDT7188S55CM
P4C188-55CMB	IDT7188S55CB
P4C188-55LM	IDT7188S55LM
P4C188-55LMB	IDT7188S55LB
P4C188L-20CC	IDT7188L20C
P4C188L-20PC	IDT7188L20P
P4C188L-20LC	IDT7188L20L
P4C188L-20JC	IDT7188L20Y
P4C188L-25CC	IDT7188L25C
P4C188L-25CM	IDT7188L25CM
P4C188L-25CMB	IDT7188L25CB
P4C188L-25LC	IDT7188L25L
P4C188L-25LM	IDT7188L25LM
P4C188L-25LMB	IDT7188L25LB
P4C188L-25PC	IDT7188L25P
P4C188L-25JC	IDT7188L25Y
P4C188L-30CC	IDT7188L30C
P4C188L-30CM	IDT7188L30CM
P4C188L-30CMB	IDT7188L30CB
P4C188L-30LC	IDT7188L30L
P4C188L-30LM	IDT7188L30LM
P4C188L-30LMB	IDT7188L30LB
P4C188L-30PC	IDT7188L30P
P4C188L-30JC	IDT7188L30Y
P4C188L-35CC	IDT7188L35C
P4C188L-35CM	IDT7188L35CM
P4C188L-35CMB	IDT7188L35CB
P4C188L-35LC	IDT7188L35L
P4C188L-35LM	IDT7188L35LM
P4C188L-35LMB	IDT7188L35LB
P4C188L-35PC	IDT7188L35P
P4C188L-35JC	IDT7188L35Y
P4C188L-45CM	IDT7188L45CM
P4C188L-45CMB	IDT7188L45CB
P4C188L-45LM	IDT7188L45LM
P4C188L-45LMB	IDT7188L45LB
P4C188L-55CM	IDT7188L55CM
P4C188L-55CMB	IDT7188L55CB
P4C188L-55LM	IDT7188L55LM
P4C188L-55LMB	IDT7188L55LB
P4C198-20CC	IDT6198S20C
P4C198-20LC	IDT6198S20L
P4C198-20PC	IDT6198S20P
P4C198-20JC	IDT6198S20Y
P4C198-25CC	IDT6198S25C
P4C198-25CM	IDT6198S25CM
P4C198-25CMB	IDT6198S25CB
P4C198-25LC	IDT6198S25L
P4C198-25LM	IDT6198S25LM
P4C198-25LMB	IDT6198S25LB
P4C198-25PC	IDT6198S25P
P4C198-25JC	IDT6198S25Y
P4C198-30CC	IDT6198S30C
P4C198-30CM	IDT6198S30CM
P4C198-30CMB	IDT6198S30CB
P4C198-30LC	IDT6198S30L
P4C198-30LM	IDT6198S30LM
P4C198-30LMB	IDT6198S30LB
P4C198-30PC	IDT6198S30P
P4C198-30JC	IDT6198S30Y
P4C198-35CC	IDT6198S35C
P4C198-35CM	IDT6198S35CM
P4C198-35CMB	IDT6198S35CB
P4C198-35LC	IDT6198S35L
P4C198-35LM	IDT6198S35LM
P4C198-35LMB	IDT6198S35LB
P4C198-35PC	IDT6198S35P
P4C198-35JC	IDT6198S35Y
P4C198-45CM	IDT6198S45CM
P4C198-45CMB	IDT6198S45CB
P4C198-45LM	IDT6198S45LM
P4C198-45LMB	IDT6198S45LB
P4C198-55CM	IDT6198S55CM
P4C198-55CMB	IDT6198S55CB
P4C198-55LM	IDT6198S55LM
P4C198-55LMB	IDT6198S55LB
P4C198L-20CC	IDT6198L20C
P4C198L-20LC	IDT6198L20L
P4C198L-20PC	IDT6198L20P
P4C198L-20JC	IDT6198L20Y
P4C198L-25CC	IDT6198L25C
P4C198L-25CM	IDT6198L25CM
P4C198L-25CMB	IDT6198L25CB
P4C198L-25LC	IDT6198L25L
P4C198L-25LM	IDT6198L25LM
P4C198L-25LMB	IDT6198L25LB
P4C198L-25PC	IDT6198L25P
P4C198L-25JC	IDT6198L25Y
P4C198L-30CC	IDT6198L30C
P4C198L-30CM	IDT6198L30CM
P4C198L-30CMB	IDT6198L30CB
P4C198L-30LC	IDT6198L30L
P4C198L-30LM	IDT6198L30LM
P4C198L-30LMB	IDT6198L30LB
P4C198L-30PC	IDT6198L30P
P4C198L-30JC	IDT6198L30Y
P4C198L-35CC	IDT6198L35C
P4C198L-35CM	IDT6198L35CM
P4C198L-35CMB	IDT6198L35CB
P4C198L-35LC	IDT6198L35L
P4C198L-35LM	IDT6198L35LM
P4C198L-35LMB	IDT6198L35LB
P4C198L-35PC	IDT6198L35P
P4C198L-35JC	IDT6198L35Y
P4C198L-45CM	IDT6198L45CM
P4C198L-45CMB	IDT6198L45CB
P4C198L-45LM	IDT6198L45LM
P4C198L-45LMB	IDT6198L45LB
P4C198L-55CM	IDT6198L55CM
P4C198L-55CMB	IDT6198L55CB
P4C198L-55LM	IDT6198L55LM
P4C198L-55LMB	IDT6198L55LB
P4C1981-20CC	IDT71981S20C
P4C1981-20LC	IDT71981S20L
P4C1981-20PC	IDT71981S20P
P4C1981-20JC	IDT71981S20Y
P4C1981-25CC	IDT71981S25C
P4C1981-25CM	IDT71981S25CM
P4C1981-25CMB	IDT71981S25CB
P4C1981-25LC	IDT71981S25L
P4C1981-25LM	IDT71981S25LM
P4C1981-25LMB	IDT71981S25LB
P4C1981-25PC	IDT71981S25P
P4C1981-25JC	IDT71981S25Y
P4C1981-30CC	IDT71981S30C
P4C1981-30CM	IDT71981S30CM
P4C1981-30CMB	IDT71981S30CB
P4C1981-30LC	IDT71981S30L
P4C1981-30LM	IDT71981S30LM
P4C1981-30LMB	IDT71981S30LB
P4C1981-30PC	IDT71981S30P
P4C1981-30JC	IDT71981S30Y
P4C1981-35CC	IDT71981S35C
P4C1981-35CM	IDT71981S35CM
P4C1981-35CMB	IDT71981S35CB
P4C1981-35LC	IDT71981S35L
P4C1981-35LM	IDT71981S35LM
P4C1981-35LMB	IDT71981S35LB
P4C1981-35PC	IDT71981S35P
P4C1981-35JC	IDT71981S35Y
P4C1981-45CM	IDT71981S45CM
P4C1981-45CMB	IDT71981S45CB
P4C1981-45LM	IDT71981S45LM
P4C1981-45LMB	IDT71981S45LB
P4C1981-55CM	IDT71981S55CM
P4C1981-55CMB	IDT71981S55CB
P4C1981-55LM	IDT71981S55LM
P4C1981-55LMB	IDT71981S55LB
P4C1981L-20CC	IDT71981L20C

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

PERFORMANCE CONT.	IDT
P4C1981L-20LC	IDT71981L20L
P4C1981L-20PC	IDT71981L20P
P4C1981L-20JC	IDT71981L20Y
P4C1981L-25CC	IDT71981L25C
P4C1981L-25CM	IDT71981L25CM
P4C1981L-25CMB	IDT71981L25CB
P4C1981L-25LC	IDT71981L25L
P4C1981L-25LM	IDT71981L25LM
P4C1981L-25LMB	IDT71981L25LB
P4C1981L-25PC	IDT71981L25P
P4C1981L-25JC	IDT71981L25Y
P4C1981L-30CC	IDT71981L30C
P4C1981L-30CM	IDT71981L30CM
P4C1981L-30CMB	IDT71981L30CB
P4C1981L-30LC	IDT71981L30L
P4C1981L-30LM	IDT71981L30LM
P4C1981L-30LMB	IDT71981L30LB
P4C1981L-30PC	IDT71981L30P
P4C1981L-30JC	IDT71981L30Y
P4C1981L-35CC	IDT71981L35C
P4C1981L-35CM	IDT71981L35CM
P4C1981L-35CMB	IDT71981L35CB
P4C1981L-35LC	IDT71981L35L
P4C1981L-35LM	IDT71981L35LM
P4C1981L-35LMB	IDT71981L35LB
P4C1981L-35PC	IDT71981L35P
P4C1981L-35JC	IDT71981L35Y
P4C1981L-45CM	IDT71981L45CM
P4C1981L-45CMB	IDT71981L45CB
P4C1981L-45LM	IDT71981L45LM
P4C1981L-45LMB	IDT71981L45LB
P4C1981L-55CM	IDT71981L55CM
P4C1981L-55CMB	IDT71981L55CB
P4C1981L-55LM	IDT71981L55LM
P4C1981L-55LMB	IDT71981L55LB
P4C1982-20CC	IDT71982S20C
P4C1982-20LC	IDT71982S20L
P4C1982-20PC	IDT71982S20P
P4C1982-20JC	IDT71982S20Y
P4C1982-25CC	IDT71982S25C
P4C1982-25CM	IDT71982S25CM
P4C1982-25CMB	IDT71982S25CB
P4C1982-25LC	IDT71982S25L
P4C1982-25LM	IDT71982S25LM
P4C1982-25LMB	IDT71982S25LB
P4C1982-25PC	IDT71982S25P
P4C1982-25JC	IDT71982S25Y
P4C1982-30CC	IDT71982S30C
P4C1982-30CM	IDT71982S30CM
P4C1982-30CMB	IDT71982S30CB
P4C1982-30LC	IDT71982S30L
P4C1982-30LM	IDT71982S30LM
P4C1982-30LMB	IDT71982S30LB
P4C1982-30PC	IDT71982S30P
P4C1982-30JC	IDT71982S30Y
P4C1982-35CC	IDT71982S35C
P4C1982-35CM	IDT71982S35CM
P4C1982-35CMB	IDT71982S35CB
P4C1982-35LC	IDT71982S35L
P4C1982-35LM	IDT71982S35LM
P4C1982-35LMB	IDT71982S35LB
P4C1982-35PC	IDT71982S35P
P4C1982-35JC	IDT71982S35Y
P4C1982-45CM	IDT71982S45CM
P4C1982-45CMB	IDT71982S45CB
P4C1982-45LM	IDT71982S45LM
P4C1982-45LMB	IDT71982S45LB
P4C1982-55CM	IDT71982S55CM
P4C1982-55CMB	IDT71982S55CB
P4C1982-55LM	IDT71982S55LM

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

PERFORMANCE CONT.	IDT
P4C1982-55LMB	IDT71982S55LB
P4C1982L-20CC	IDT71982L20C
P4C1982L-20LC	IDT71982L20L
P4C1982L-20PC	IDT71982L20P
P4C1982L-20JC	IDT71982L20Y
P4C1982L-25CC	IDT71982L25C
P4C1982L-25CM	IDT71982L25CM
P4C1982L-25CMB	IDT71982L25CB
P4C1982L-25LC	IDT71982L25L
P4C1982L-25LM	IDT71982L25LM
P4C1982L-25LMB	IDT71982L25LB
P4C1982L-25PC	IDT71982L25P
P4C1982L-25JC	IDT71982L25Y
P4C1982L-30CC	IDT71982L30C
P4C1982L-30CM	IDT71982L30CM
P4C1982L-30CMB	IDT71982L30CB
P4C1982L-30LC	IDT71982L30L
P4C1982L-30LM	IDT71982L30LM
P4C1982L-30LMB	IDT71982L30LB
P4C1982L-30PC	IDT71982L30P
P4C1982L-30JC	IDT71982L30Y
P4C1982L-35CC	IDT71982L35C
P4C1982L-35CM	IDT71982L35CM
P4C1982L-35CMB	IDT71982L35CB
P4C1982L-35LC	IDT71982L35L
P4C1982L-35LM	IDT71982L35LM
P4C1982L-35LMB	IDT71982L35LB
P4C1982L-35PC	IDT71982L35P
P4C1982L-35JC	IDT71982L35Y
P4C1982L-45CM	IDT71982L45CM
P4C1982L-45CMB	IDT71982L45CB
P4C1982L-45LM	IDT71982L45LM
P4C1982L-45LMB	IDT71982L45LB
P4C1982L-55CM	IDT71982L55CM
P4C1982L-55CMB	IDT71982L55CB
P4C1982L-55LM	IDT71982L55LM
P4C1982L-55LMB	IDT71982L55LB
P4C198A-20CC	IDT7198S20C
P4C198A-20PC	IDT7198S20P
P4C198A-20LC	IDT7198S20L
P4C198A-20JC	IDT7198S20Y
P4C198A-25CC	IDT7198S25C
P4C198A-25CM	IDT7198S25CM
P4C198A-25CMB	IDT7198S25CB
P4C198A-25LC	IDT7198S25L
P4C198A-25LM	IDT7198S25LM
P4C198A-25LMB	IDT7198S25LB
P4C198A-25PC	IDT7198S25P
P4C198A-25JC	IDT7198S25Y
P4C198A-30CC	IDT7198S30C
P4C198A-30CM	IDT7198S30CM
P4C198A-30CMB	IDT7198S30CB
P4C198A-30LC	IDT7198S30L
P4C198A-30LM	IDT7198S30LM
P4C198A-30LMB	IDT7198S30LB
P4C198A-30PC	IDT7198S30P
P4C198A-30JC	IDT7198S30Y
P4C198A-35CC	IDT7198S35C
P4C198A-35CM	IDT7198S35CM
P4C198A-35CMB	IDT7198S35CB
P4C198A-35LC	IDT7198S35L
P4C198A-35LM	IDT7198S35LM
P4C198A-35LMB	IDT7198S35LB
P4C198A-35PC	IDT7198S35P
P4C198A-35JC	IDT7198S35Y
P4C198A-45CM	IDT7198S45CM
P4C198A-45CMB	IDT7198S45CB
P4C198A-45LM	IDT7198S45LM
P4C198A-45LMB	IDT7198S45LB
P4C198A-55CM	IDT7198S55CM
P4C198A-55CMB	IDT7198S55CB
P4C198A-55LM	IDT7198S55LM
P4C198A-55LMB	IDT7198S55LB

PERFORMANCE CONT.	IDT
P4C198AL-20CC	IDT7198L20C
P4C198AL-20PC	IDT7198L20P
P4C198AL-20LC	IDT7198L20L
P4C198AL-20JC	IDT7198L20Y
P4C198AL-25CC	IDT7198L25C
P4C198AL-25CM	IDT7198L25CM
P4C198AL-25CMB	IDT7198L25CB
P4C198AL-25LC	IDT7198L25L
P4C198AL-25LM	IDT7198L25LM
P4C198AL-25LMB	IDT7198L25LB
P4C198AL-25PC	IDT7198L25P
P4C198AL-25JC	IDT7198L25Y
P4C198AL-30CC	IDT7198L30C
P4C198AL-30CM	IDT7198L30CM
P4C198AL-30CMB	IDT7198L30CB
P4C198AL-30LC	IDT7198L30L
P4C198AL-30LM	IDT7198L30LM
P4C198AL-30LMB	IDT7198L30LB
P4C198AL-30PC	IDT7198L30P
P4C198AL-30JC	IDT7198L30Y
P4C198AL-35CC	IDT7198L35C
P4C198AL-35CM	IDT7198L35CM
P4C198AL-35CMB	IDT7198L35CB
P4C198AL-35LC	IDT7198L35L
P4C198AL-35LM	IDT7198L35LM
P4C198AL-35LMB	IDT7198L35LB
P4C198AL-35PC	IDT7198L35P
P4C198AL-35JC	IDT7198L35Y
P4C198AL-45CM	IDT7198L45CM
P4C198AL-45CMB	IDT7198L45CB
P4C198AL-45LM	IDT7198L45LM
P4C198AL-45LMB	IDT7198L45LB
P4C198AL-55CM	IDT7198L55CM
P4C198AL-55CMB	IDT7198L55CB
P4C198AL-55LM	IDT7198L55LM
P4C198AL-55LMB	IDT7198L55LB

SARATOGA	IDT
SSM6116-20SC	IDT6116SA20D
SSM6116-20EC	IDT6116SA20Y
SSM6116-20PC	IDT6116SA20P
SSM6116-20DC	IDT6116SA20SO
SSM6116-25SC	IDT6116SA25D
SSM6116-25SB	IDT6116SA25DB
SSM6116-25EC	IDT6116SA25Y
SSM6116-25PC	IDT6116SA25P
SSM6116-25DC	IDT6116SA25SO
SSM6116-35SC	IDT6116SA35D
SSM6116-35SB	IDT6116SA35DB
SSM6116-35EC	IDT6116SA35Y
SSM6116-35PC	IDT6116SA35P
SSM6116-35DC	IDT6116SA35SO
SSM6116-45SB	IDT6116SA45DB
SSM6167-20CC	IDT6167SA20D
SSM6167-25CC	IDT6167SA25D
SSM6167-25CB	IDT6167SA25DB
SSM6167-35CC	IDT6167SA35D
SSM6167-35CB	IDT6167SA35DB
SSM6167-45CB	IDT6167SA45DB
SSM6168-20SC	IDT6168SA20D
SSM6168-20EC	IDT6168SA20Y
SSM6168-20PC	IDT6168SA20P
SSM6168-25SC	IDT6168SA25D
SSM6168-25SB	IDT6168SA25DB
SSM6168-25EC	IDT6168SA25Y
SSM6168-25PC	IDT6168SA25P
SSM6168-35SC	IDT6168SA35D
SSM6168-35SB	IDT6168SA35DB
SSM6168-35EC	IDT6168SA35Y
SSM6168-35PC	IDT6168SA35P
SSM6168-45SB	IDT6168SA45DB
SSM6171-20SC	IDT71681SA20D

SARATOGA CONT.	IDT
SSM6171-20EC	IDT71681SA20Y
SSM6171-20PC	IDT71681SA20P
SSM6171-20DC	IDT71681SA20SO
SSM6171-25SC	IDT71681SA25D
SSM6171-25SB	IDT71681SA25DB
SSM6171-25EC	IDT71681SA25Y
SSM6171-25PC	IDT71681SA25P
SSM6171-25DC	IDT71681SA25SO
SSM6171-35SC	IDT71681SA35D
SSM6171-35SB	IDT71681SA35DB
SSM6171-35EC	IDT71681SA35Y
SSM6171-35PC	IDT71681SA35P
SSM6171-35DC	IDT71681SA35SO
SSM6171-45SB	IDT71681SA45DB
SSM6172-20SC	IDT71682SA20D
SSM6172-20EC	IDT71682SA20Y
SSM6172-20PC	IDT71682SA20P
SSM6172-20DC	IDT71682SA20SO
SSM6172-25SC	IDT71682SA25D
SSM6172-25SB	IDT71682SA25DB
SSM6172-25EC	IDT71682SA25Y
SSM6172-25PC	IDT71682SA25P
SSM6172-25DC	IDT71682SA25SO
SSM6172-35SC	IDT71682SA35D
SSM6172-35SB	IDT71682SA35DB
SSM6172-35EC	IDT71682SA35Y
SSM6172-35PC	IDT71682SA35P
SSM6172-35DC	IDT71682SA35SO
SSM6172-45SB	IDT71682SA45DB
SSM7161-20SC	IDT71981SA20D
SSM7161-20PC	IDT71981SA20P
SSM7161-25SC	IDT71981SA25D
SSM7161-25SB	IDT71981SA25DB
SSM7161-25PC	IDT71981SA25P
SSM7161-35SC	IDT71981SA35D
SSM7161-35SB	IDT71981SA35DB
SSM7161-35PC	IDT71981SA35P
SSM7161-45SB	IDT71981SA45DB
SSM7162-20SC	IDT71982SA20D
SSM7162-20PC	IDT71982SA20P
SSM7162-25	IDT71982S25C
SSM7162-25SC	IDT71982SA25D
SSM7162-25SB	IDT71982SA25DB
SSM7162-25PC	IDT71982SA25P
SSM7162-35SC	IDT71982SA35D
SSM7162-35SB	IDT71982SA35DB
SSM7162-35PC	IDT71982SA35P
SSM7162-45SB	IDT71982SA45DB
SSM7162L-25	IDT71982L25C
SSM7164-20SC	IDT7164SA20TC
SSM7164-20PC	IDT7164SA20TP
SSM7164-25	IDT7164S25TC
SSM7164-25SC	IDT7164SA25TC
SSM7164-25SB	IDT7164SA25TCB
SSM7164-25PC	IDT7164SA25TP
SSM7164-35SC	IDT7164SA35TC
SSM7164-35SB	IDT7164SA35TCB
SSM7164-35PC	IDT7164SA35TP
SSM7164-45SB	IDT7164SA45TCB
SSM7164L-25	IDT7164L25TC
SSM7166-20SC	IDT6198SA20D
SSM7166-20PC	IDT6198SA20P
SSM7166-25SC	IDT6198SA25D
SSM7166-25SB	IDT6198SA25DB
SSM7166-25PC	IDT6198SA25P
SSM7166-35SC	IDT6198SA35D
SSM7166-35SB	IDT6198SA35DB
SSM7166-35PC	IDT6198SA35P
SSM7166-45SB	IDT6198SA45DB
SSM7187-25	IDT7187S25C

SARATOGA CONT.	IDT
SSM7187L-25	IDT7187L25C
SSM7188-20SC	IDT7188SA20D
SSM7188-20PC	IDT7188SA20P
SSM7188-25	IDT7188S25C
SSM7188-25SC	IDT7188SA25D
SSM7188-25SB	IDT7188SA25DB
SSM7188-25PC	IDT7188SA25P
SSM7188-35SC	IDT7188SA35D
SSM7188-35SB	IDT7188SA35DB
SSM7188-35PC	IDT7188SA35P
SSM7188-45SB	IDT7188SA45DB
SSM7188L-25	IDT7188L25C
SSM7198-20SC	IDT7198SA20D
SSM7198-20PC	IDT7198SA20P
SSM7198-25	IDT7198S25C
SSM7198-25SC	IDT7198SA25D
SSM7198-25SB	IDT7198SA25DB
SSM7198-25PC	IDT7198SA25P
SSM7198-35SC	IDT7198SA35D
SSM7198-35SB	IDT7198SA35DB
SSM7198-35PC	IDT7198SA35P
SSM7198-45SB	IDT7198SA45DB
SSM7198L-25	IDT7198L25C
SSL4180-15SC	IDT6178SA15D
SSL4180-15PC	IDT6178SA15P
SSL4180-20SC	IDT6178SA20D
SSL4180-20SM	IDT6178SA20DB
SSL4180-20PC	IDT6178SA20P
SSL4180-25SC	IDT6178SA25D
SSL4180-25SM	IDT6178SA25DB
SSL4180-25PC	IDT6178SA25P
SSL4180-35SM	IDT6178SA35DB
SSL4181-15SC	IDT7178SA15D
SSL4181-15PC	IDT7178SA15P
SSL4181-20SC	IDT7178SA20D
SSL4181-20SM	IDT7178SA20DB
SSL4181-20PC	IDT7178SA20P
SSL4181-25SC	IDT7178SA25D
SSL4181-25SM	IDT7178SA25DB
SSL4181-25PC	IDT7178SA25P
SSL4181-35SM	IDT7178SA35DB

SGS-THOMSON	IDT
MK41H67N-20	IDT6167S20P
MK41H67N-25	IDT6167S25P
MK41H67N-35	IDT6167S35P
MK41H68N-20	IDT6168L20P
MK41H68N-25	IDT6168L25P
MK41H68N-35	IDT6168L35P
MK41H78N-20	IDT61970S20P
MK41H78N-25	IDT61970S25P
MK41H78N-35	IDT61970S35P
MK41H80N-20	IDT6178S20P
MK41H80P-20	IDT6178S20D
MK41H87N-25	IDT7187S25P
MK41H87N-35	IDT7187S35P
MK41H87N-45	IDT7187S45P

SONY	IDT
CXK5416P-35	IDT6168LA35P
CXK5416P-45	IDT6168LA35P
CXK5416P-55	IDT6168LA35P
CXK5464P-45	IDT7188L45P
CXK5464P-55	IDT7188L45P
CXK5464P-70	IDT7188L45P
CXK5814P-35	IDT6116LA35TP
CXK5814P-45	IDT6116LA45TP
CXK5814P-55	IDT6116LA45TP
CXK5818PN-10	IDT6116L45P
CXK5818M-10	IDT6116L45SO
CXK58256P-10	IDT71256L70P
CXK58256M-10	IDT71256L70SO
CXK5864AP-70L	IDT7164L45P
CXK5864AM-70L	IDT7164L45SO
CXK5865P-45L	IDT7164L45P
CXK5865P-55L	IDT7164L55P

TI	IDT
SMJ61CD16-25M	IDT6167-25B
SMJ61CD16-35M	IDT6167-35B
SMJ61CD16-45M	IDT6167-45B
SMJ64C16-25M	IDT6168-25B
SMJ64C16-35M	IDT6168-35B
SMJ64C16-45M	IDT6168-45B
SMJ68CE16-25M	IDT6116-25B
SMJ68CE16-35M	IDT6116-35B
SMJ68CE16-45M	IDT6116-45B
SMJ61CD64-25M	IDT7187-25B
SMJ61CD64-35M	IDT7187-35B
SMJ61CD64-45M	IDT7187-45B
SMJ64C64-25M	IDT7188-25B
SMJ64C64-35M	IDT7188-35B
SMJ64C64-45M	IDT7188-45B
SMJ68CE64-25M	IDT7164-25B
SMJ68CE64-35M	IDT7164-35B
SMJ68CE64-45M	IDT7164-45B
SMJ61CD256-35M	IDT71257-35B
SMJ61CD256-45M	IDT71257-45B
SMJ61CD256-55M	IDT71257-55B
SMJ64C256-35M	IDT71258-35B
SMJ64C256-45M	IDT71258-45B
SMJ64C256-55M	IDT71258-55B
SMJ68CE256-45M	IDT71256-45B
SMJ68CE256-55M	IDT71256-55B
SMJ68CE256-70M	IDT71256-70B
SMJ69CE72-25M	IDT7169-25B
SMJ69CE72-35M	IDT7169-35B
SMJ69CE72-45M	IDT7169-45B
SMJ69CE288-35M	IDT71259-35B
SMJ69CE288-45M	IDT71259-45B
SMJ69CE288-55M	IDT71259-55B

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

TOSHIBA	IDT
TMM2018AD-25	IDT6116SA25TD
TMM2018AP-25	IDT6116SA25TP
TMM2018AD-35	IDT6116SA35TD
TMM2018AP-35	IDT6116SA35TP
TMM2068AP-25	IDT6168SA25P
TMM2068AP-35	IDT6168SA35P
TC55417P-35	IDT6198S35P
TC55417P-45	IDT6198S45P
TC5562P-45	IDT7187S45P

VITELIC	IDT
V61C16P35	IDT6116SA35P
V61C16P35L	IDT6116LA35P
V61C16P45	IDT6116SA45P
V61C16P45L	IDT6116LA45P
V61C16P55	IDT6116SA45P
V61C16P55L	IDT6116LA45P
V61C16S35	IDT6116SA35TP
V61C16S35L	IDT6116LA35TP
V61C16S45	IDT6116SA45TP
V61C16S45L	IDT6116LA45TP
V61C16S55	IDT6116SA45TP
V61C16S55L	IDT6116LA45TP
V61C32P70	IDT7132SA70P
V61C32P70L	IDT7132LA70P
V61C32P90	IDT7132SA90P
V61C32P90L	IDT7132LA90P
V61C34P90	IDT71322S90P
V61C62P45	IDT7188S45P
V61C62P45L	IDT7188L45P
V61C62P55	IDT7188S45P
V61C62P55L	IDT7188L45P
V61C62P70	IDT7188S45P
V61C62P70L	IDT7188L45P
V61C64P45	IDT7164S45P
V61C64P45L	IDT7164L45P
V61C64P55	IDT7164S45P
V61C64P55L	IDT7164L45P
V61C64P70	IDT7164S45P
V61C64P70L	IDT7164L45P
V61C67P35	IDT6167SA35P
V61C67P35L	IDT6167LA35P
V61C67P45	IDT6167SA35P
V61C67P45L	IDT6167LA35P
V61C67P55	IDT6167SA35P
V61C67P55L	IDT6167LA35P
V61C68P35	IDT6168SA35P
V61C68P35L	IDT6168LA35P
V61C68P45	IDT6168SA35P
V61C68P45L	IDT6168LA35P
V61C68P55	IDT6168SA35P
V61C68P55L	IDT6168LA35P

VTI	IDT
VT16H4-35	IDT71981-35
VT16H4-45	IDT71981-45
VT16H4-55	IDT71981-45
VT20C18-20	ITD6116SA20TP
VT20C18-25	ITD6116SA25TP
VT20C18-35	ITD6116SA35TP
VT20C19-25	IDT6116SA15TP
VT20C19-35	IDT6116SA20TP
VT20C68-20	IDT6168SA20P
VT20C68-25	IDT6168SA25P
VT20C68-35	IDT6168SA35P
VT20C68-45	IDT6168SA35P
VT20C69-20	IDT6168SA12P
VT20C69-25	IDT6168SA15P
VT20C69-35	IDT6168SA20P
VT20C69-45	IDT6168SA25P
VT2130	IDT7130SA100P
VT65KS4-25	IDT7188S25P
VT65KS4-35CC	IDT7188S35C
VT65KS4-45CC	IDT7188S45C
VT65KS4-55CC	IDT7188S45C
VT7132-55	IDT7132SA55D
VT7132-70	IDT7132SA70D
VT7132-90	IDT7132SA90D
VT7132A-35	IDT7132SA35D
VT7132A-45	IDT7132SA45D
VT7142-55	IDT7142SA55D
VT7142-70	IDT7142SA70D
VT7142-90	IDT7142SA90D
VT7142A-35	IDT7142SA35D
VT7142A-45	IDT7142SA45D

NOTE:
A lower case "x" indicates the speed and/or package of the part are unknown."

Integrated Device Technology, Inc.

MULTI-PORT PRODUCTS CROSS REFERENCE GUIDE

CYPRESS	IDT
CY7C130-35PC	IDT7130SA35P
CY7C130-35DC	IDT7130SA35C
CY7C130-35LC	IDT7130SA35L48
CY7C130-35JC	IDT7130SA35J
CY7C130-45PC	IDT7130SA45P
CY7C130-45DC	IDT7130SA45C
CY7C130-45LC	IDT7130SA45L48
CY7C130-45JC	IDT7130SA45J
CY7C130-45DMB	IDT7130SA45CB
CY7C130-45LMB	IDT7130SA45L48B
CY7C130-55PC	IDT7130SA55P
CY7C130-55DC	IDT7130SA55C
CY7C130-55LC	IDT7130SA55L48
CY7C130-55JC	IDT7130SA55J
CY7C130-55DMB	IDT7130SA55CB
CY7C130-55LMB	IDT7130SA55L48B
CY7C132-35PC	IDT7132SA35P
CY7C132-35DC	IDT7132SA35C
CY7C132-35LC	IDT7132SA35L48
CY7C132-35JC	IDT7132SA35J
CY7C132-45PC	IDT7132SA45P
CY7C132-45DC	IDT7132SA45C
CY7C132-45LC	IDT7132SA45L48
CY7C132-45JC	IDT7132SA45J
CY7C132-45DMB	IDT7132SA45CB
CY7C132-45LMB	IDT7132SA45L48B
CY7C132-55PC	IDT7132SA55P.
CY7C132-55DC	IDT7132SA55C
CY7C132-55LC	IDT7132SA55L48
CY7C132-55JC	IDT7132SA55J
CY7C132-55DMB	IDT7132SA55CB
CY7C132-55LMB	IDT7132SA55L48B
CY7C140-35PC	IDT7140SA35P
CY7C140-35DC	IDT7140SA35C
CY7C140-35LC	IDT7140SA35L48
CY7C140-35JC	IDT7140SA35J
CY7C140-45PC	IDT7140SA45P
CY7C140-45DC	IDT7140SA45C
CY7C140-45LC	IDT7140SA45L48
CY7C140-45JC	IDT7140SA45J
CY7C140-45DMB	IDT7140SA45CB
CY7C140-45LMB	IDT7140SA45L48B
CY7C140-55PC	IDT7140SA55P
CY7C140-55DC	IDT7140SA55C
CY7C140-55LC	IDT7140SA55L48
CY7C140-55JC	IDT7140SA55J
CY7C140-55DMB	IDT7140SA55CB
CY7C140-55LMB	IDT7140SA55L48B
CY7C142-35PC	IDT7142SA35P
CY7C142-35DC	IDT7142SA35C
CY7C142-35LC	IDT7142SA35L48
CY7C142-35JC	IDT7142SA35J
CY7C142-45PC	IDT7142SA45P
CY7C142-45DC	IDT7142SA45C
CY7C142-45LC	IDT7142SA45L48
CY7C142-45JC	IDT7142SA45J
CY7C142-45DMB	IDT7142SA45CB
CY7C142-45LMB	IDT7142SA45L48B
CY7C142-55PC	IDT7142SA55P
CY7C142-55DC	IDT7142SA55C
CY7C142-55LC	IDT7142SA55L48
CY7C142-55JC	IDT7142SA55J
CY7C142-55DMB	IDT7142SA55CB
CY7C142-55LMB	IDT7142SA55L48B

AMD	IDT
AM2130-55PC	IDT7130SA55P
AM2130-55DC	IDT7130SA55C
AM2130-55LC	IDT7130SA55L52
AM2130-55JC	IDT7130SA55J
AM2130-70PC	IDT7130SA70P
AM2130-70DC	IDT7130SA70C
AM2130-70LC	IDT7130SA70L52
AM2130-70JC	IDT7130SA70J
AM2130-70/BXC	IDT7130SA70CB
AM2130-10PC	IDT7130SA100P
AM2130-10DC	IDT7130SA100C
AM2130-10LC	IDT7130SA100L52
AM2130-10JC	IDT7130SA100J
AM2130-10/BXC	IDT7130SA100CB
AM2130-12/BXC	IDT7130SA120CB
AM2140-55PC	IDT7140SA55P
AM2140-55DC	IDT7140SA55C
AM2140-55LC	IDT7140SA55L52
AM2140-55JC	IDT7140SA55J
AM2140-70PC	IDT7140SA70P
AM2140-70DC	IDT7140SA70C
AM2140-70LC	IDT7140SA70L52
AM2140-70JC	IDT7140SA70J
AM2140-70/BXC	IDT7140SA70CB
AM2140-10PC	IDT7140SA100P
AM2140-10DC	IDT7140SA100C
AM2140-10LC	IDT7140SA100L52
AM2140-10JC	IDT7140SA100J
AM2140-10/BXC	IDT7140SA100CB
AM2140-12/BXC	IDT7140SA120CB

VLSI	IDT
VT7132A-35PC	IDT7132SA35P
VT7132A-45PC	IDT7132SA45P
VT7132-55PC	IDT7132SA55P
VT7132-55QC	IDT7132SA55J
VT7132-70PC	IDT7132SA70P
VT7132-70QC	IDT7132SA70J
VT7132-90PC	IDT7132SA90P
VT7132-90QC	IDT7132SA90J
VT7142A-35PC	IDT7142SA35P
VT7142A-45PC	IDT7142SA45P
VT7142-55PC	IDT7142SA55P
VT7142-55QC	IDT7142SA55J
VT7142-70PC	IDT7142SA70P
VT7142-70QC	IDT7142SA70J
VT7142-90PC	IDT7142SA90P
VT7142-90QC	IDT7142SA90J

Integrated Device Technology, Inc.

FIFO CROSS REFERENCE GUIDE

SMALL FIFOs	
AMD	**IDT**
67401	**72401**
57401AJB	72401L15DB
57401BJB	72401L25DB
57401JB	72401L10DB
67401AJ	72401L15D
67401AN	72401L15P
67401BJ	72401L25D
67401J	72401L10D
67401N	72401L10P
C57401AJB	72401L15DB
C57401BJB	72401L25DB
C57401JB	72401L10DB
C57L401DJB	72401L15DB
C67401AJ	72401L15D
C67401AN	72401L15P
C67401BJ	72401L25D
C67401J	72401L10D
C67401N	72401L10P
C67L401DJ	72401L15D
C67L401DN	72401L15P
67402	**72402**
57402AJB	72402L15DB
57402BJB	72402L25DB
57402JB	72402L10DB
67402AJ	72402L15D
67402AN	72402L15P
67402BJ	72402L25D
67402J	72402L10D
67402N	72402L10P
C57402AJB	72402L15DB
C57402BJB	72402L25DB
C57402JB	72402L10DB
C57L402DJB	72402L15DB
C67402AJ	72402L15D
C67402AN	72402L15P
C67402BJ	72402L25D
C67402J	72402L10D
C67402N	72402L10P
C67L402DJ	72402L25D
C67L402DN	72402L15P
67C4013	**72403**
67C4013-10N	72403L10P
67C4013-10J	72403L10D
67C4013-15N	72403L15P
67C4013-15J	72403L15D
67C4023	**72404**
67C4023-10N	72404L10P
67C4023-10J	72404L10D
67C4023-15N	72404L15P
67C4023-15J	72404L15D
67411	**72401**
57411JB	72401L25DB
67411AJ	72401L35D
67411J	72401L25D
67412	**72402**
57412JB	72402L25DB
67412AJ	72402L35D
67412J	72402L25D
67413	**72413**
57413JB	72413L25DB
67413AJ	72413L35D
67413J	72413L25D

LARGE FIFOs	
AMD	**IDT**
67C4501	**7201**
67C4501-35J	7201SA35D
67C4501-35N	7201SA35P
67C4501-35NL	7201SA35J
67C4501-50J	7201SA50D
67C4501-50N	7201SA50P
67C4501-50NL	7201SA50J
67C4501-65J	7201SA65D
67C4501-65N	7201SA65P
67C4501-65NL	7201SA65J
67C4501-80J	7201SA80D
67C4501-80N	7201SA80P
67C4501-80NL	7201SA80J
67C4502	**7202**
67C4502-35J	7202SA35D
67C4502-35N	7202SA35P
67C4502-35NL	7202SA35J
67C4502-50J	7202SA50D
67C4502-50N	7202SA50P
67C4502-50NL	7202SA50J
67C4502-65J	7202SA64D
67C4502-65N	7202SA65P
67C4502-65NL	7202SA65J
67C4502-80J	7202SA80D
67C4502-80N	7202SA80P
67C4502-80NL	7202SA80J
67C4503	**7203**
67C4503-35N	7203S35P
67C4503-50N	7203S50P
67C4503-65N	7203S65P
67C4503-80N	7203S80P

CYPRESS	IDT
7C401	**72401**
7C401-10DC	72401L10D
7C401-10DMB	72401L10DB
7C401-10LC	72401L10L
7C401-10LMB	72401L10LB
7C401-10PC	72401L10P
7C401-15DC	72401L15D
7C401-15DMB	72401L15DB
7C401-15LC	72401L15L
7C401-15LMB	72401L15LB
7C401-15PC	72401L15P
7C402	**72402**
7C402-10DC	72402L10D
7C402-10DMB	72402L10DB
7C402-10LC	72402L10L
7C402-10LMB	72402L10LB
7C402-10PC	72402L10P
7C402-15DC	72402L15D
7C402-15DMB	72402L15DB
7C402-15LC	72402L15L
7C402-15LMB	72402L15LB
7C402-15PC	72402L15P
7C403	**72403**
7C403-10DC	72403L10D
7C403-10DMB	72403L10DB
7C403-10LC	72403L10L
7C403-10LMB	72403L10LB
7C403-10PC	72403L10P

CYPRESS CONT.	IDT
7C403-15DC	72403L15D
7C403-15DMB	72403L15DB
7C403-15LC	72403L15L
7C403-15LMB	72403L15LB
7C403-15PC	72403L15P
7C403-25DC	72403L25D
7C403-25DMB	72403L25DB
7C403-25LC	72403L25L
7C403-25LMB	72403L25LB
7C403-25PC	72403L25P
7C404	**72404**
7C404-10DC	72404L10D
7C404-10DMB	72404L10DB
7C404-10LC	72404L10L
7C404-10LMB	72404L10LB
7C404-10PC	72404L10P
7C404-15DC	72404L15D
7C404-15DMB	72404L15DB
7C404-15LC	72404L15L
7C404-15LMB	72404L15LB
7C404-15PC	72404L15P
7C404-25DC	72404L25D
7C404-25DMB	72404L25DB
7C404-25LC	72404L25L
7C404-25LMB	72404L25LB
7C404-25PC	72404L25P

DALLAS	IDT
DS2009	**7201**
DS2009-35	7201SA35P
DS2009-50	7201SA50P
DS2009-65	7201SA65P
DS2009-80	7201SA80P
DS2010	**7202**
DS2010-35	7202SA35P
DS2010-50	7202SA50P
DS2010-65	7202SA65P
DS2010-80	7202SA80P
DS2011	**7203**
DS2011-35	7203SA35P
DS2011-50	7203SA50P
DS2011-65	7203SA65P
DS2011-80	7203SA80P

MOSTEK	IDT
MK4501	**7201**
MK4501-10N	7201S80P
MK4501-12N	7201S120P
MK4501-65N	7201S65P
MK4501-80N	7201S80P

TI	IDT
SN74ACT7201	**7201**
SN74ACT7201A-35N	7201LA35P
SN74ACT7201A-50N	7201LA50P
SN74ACT7202	**7202**
SN74ACT7202-35N	7202L35P
SN74ACT7202-50N	7202L50P

Integrated Device Technology, Inc.

DIGITAL SIGNAL PROCESSING CROSS REFERENCE GUIDE

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DSP DIVISION	
ANALOG DEVICES	**IDT**
ADSP-1009	**7209**
ADSP-1009JD	7209L135C
ADSP-1009KD	7209L135C
ADSP-1009SD	7209L170CB
ADSP-1009TD	7209L170CB
ADSP-1012	**7212**
ADSP-1012JD	7212L115C
ADSP-1012KD	7212LL115C
ADSP-1012SD	7212L140CB
ADSP-1012TD	7212L140CB
ADSP-1010	**7210**
ADSP-1010AKD	7210L75C
ADSP-1010AKG	7210L75G
ADSP-1010JD	7210L165C
ADSP-1010JG	7210L165G
ADSP-1010KD	7210L165C
ADSP-1010KG	7210L165G
ADSP-1010SD	7210L200CB
ADSP-1010SG	7210L200GB
ADSP-1010TD	7210L200CB
ADSP-1010TG	7210L200GB
ADSP-1016	**7216**
ADSP-1016AKD	7216L75C
ADSP-1016AKG	7216L75G
ADSP-1016JD	7216L140C
ADSP-1016JG	7216L140G
ADSP-1016KD	7216L140C
ADSP-1016KG	7216L140G
ADSP-1016SD	7216L185CB
ADSP-1016SG	7216L185GB
ADSP-1016TD	7216L120CB
ADSP-1016TG	7216L120GB
CYPRESS	**IDT**
7C510	7210
7C510-45DC	7210L45D
7C510-45GC	7210L45G
7C510-45LC	7210L45L
7C510-45PC	7210L45P
7C510-55DC	7210L55D
7C510-55DMB	7210L55DB
7C510-55GC	7210L55G
7C510-55GMB	7210L55GB
7C510-55LC	7210L55L
7C510-55LMB	7210L55LB
7C510-55PC	7210L55P
7C510-65DC	7210L65D
7C510-65DMB	7210L65DB
7C510-65GC	7210L65G
7C510-65GMB	7210L65GB
7C510-65LC	7210L65L
7C510-65LMB	7210L65LB
7C510-65PC	7210L65P
7C510-75DC	7210L75D
7C510-75DMB	7210L75DB
7C510-75GC	7210L75G
7C510-75GMB	7210L75GB
7C510-75LC	7210L75L
7C510-75LMB	7210L75LB
7C510-75PC	7210L75P
7C516	7216
7C516-38DC	7216L35D

CYPRESS CONT.	IDT
7C516-38GC	7216L35G
7C516-38LC	7216L35L
7C516-38PC	7216L35P
7C516-42DMB	7216L40DB
7C516-42GMB	7216L40GB
7C516-42LMB	7216L40LB
7C516-45DC	7216L45D
7C516-45GC	7216L45G
7C516-45LC	7216L45L
7C516-45PC	7216L45P
7C516-55DC	7216L55D
7C516-55DMB	7216L55DB
7C516-55GC	7216L55G
7C516-55GMB	7216L55GB
7C516-55LC	7216L55L
7C516-55LMB	7216L55LB
7C516-55PC	7216L55P
7C516-65DC	7216L65D
7C516-65DMB	7216L65DB
7C516-65GC	7216L65G
7C516-65GMB	7216L65GB
7C516-65LC	7216L65L
7C516-65LMB	7216L65LB
7C516-65PC	7216L65P
7C516-75DC	7216L75D
7C516-75DMB	7216L75DB
7C516-75GC	7216L75G
7C516-75GMB	7216L75GB
7C516-75LC	7216L75L
7C516-75LMB	7216L75LB
7C516-75PC	7216L75P
7C517	7217
7C517-45DC	7217L45D
7C517-45GC	7217L45G
7C517-45LC	7217L45L
7C517-45PC	7217L45P
7C517-55DC	7217L55D
7C517-55DMB	7217L55DB
7C517-55GC	7217L55G
7C517-55GMB	7217L55GB
7C517-55LC	7217L55L
7C517-55LMB	7217L55LB
7C517-55PC	7217L55P
7C517-65DC	7217L65D
7C517-65DMB	7217L65DB
7C517-65GC	7217L65G
7C517-65GMB	7217L65GB
7C517-65LC	7217L65L
7C517-65LMB	7217L65LB
7C517-65PC	7217L65P
7C517-75DC	7217L75D
7C517-75DMB	7217L75DB
7C517-75GC	7217L75G
7C517-75GMB	7217L75GB
7C517-75LC	7217L75L
7C517-75LMB	7217L75LB
7C517-75PC	7217L75P
LOGIC DEVICES	**IDT**
LMA1009	**7209**
LMA1009DC-45	7209L45C
LMA1009GC-45	7209L45G
LMA1009DMB-55	7209L55CB
LMA1009GMB-55	7209L55GB
LMA1009DC-75	7209L65C

LOGIC DEVICES CONT.	IDT
LMA1009GC-75	7209L65G
LMA1009DC-90	7209L65C
LMA1009GC-90	7209L65G
LMA1009DMB-95	7209L75CB
LMA1009GMB-95	7209L75GB
LMA1009DMB-115	7209L75CB
LMA1009GMB-115	7209L75GB
LMA2009	**7209**
LMA2009KC-45	7209L45L
LMA2009KMB-55	7209L55LB
LMA2009KC-55	7209L45L
LMA2009KMB-65	7209L55LB
LMA2009KC-75	7209L65L
LMA2009KC-90	7209L65L
LMA2009KMB-95	7209L75LB
LMA2009KMB-115	7209L75LB
LMA1010	**7210**
LMA1010PC-45	7210L45P
LMA1010DC-45	7210L45C
LMA1010GC-45	7210L45G
LMA1010PC-55	7210L55P
LMA1010DC-55	7210L55C
LMA1010GC-55	7210L55G
LMA1010DBM-55	7210L55CB
LMA1010GMB-55	7210L55GB
LMA1010PC-65	7210L65P
LMA1010DC-65	7210L65C
LMA1010GC-65	7210L65G
LMA1010DMB-65	7210L65CB
LMA1010GMB-65	7210L65GB
LMA1010DMB-75	7210L75CB
LMA1010GMB-75	7210L75GB
LMA1010PC	7210L100P
LMA1010DC	7210L100C
LMA1010GC	7210L100G
LMA1010DMB	7210L120CB
LMA1010GMB	7210L120GB
LMA2010	**7210**
LMA2010JC-45	7210L45J
LMA2010KC-45	7210L45L
LMA2010JC-55	7210L55J
LMA2010KC-55	7210L55L
LMA2010KMB-55	7210L55LB
LMA2010JC-65	7210L65J
LMA2010KC-65	7210L65L
LMA2010KMB-65	7210L65LB
LMA2010KMB-75	7210L75LB
LMA2010JC	7210L100J
LMA2010KC	7210L100L
LMA2010KMB	7210L120LB
LMA1043	**7243**
LMA1043PC-45	7243L45P
LMA1043DC-45	7243L45D
LMA1043GC-45	7343L45G
LMA1043PC-55	7243L55P
LMA1043DC-55	7243L55D
LMA1043GC-55	7243L55G
LMA1043DMB-55	7243L55DB
LMA1043GMB-55	7243L55GB
LMA1043PC-65	7243L65P
LMA1043DC-65	7243L65D
LMA1043GC-65	7243L65G
LMA1043DMB-65	7243L65DB
LMA1043GMB-65	7243L65GB
LMA1043DMB-75	7243L75DB
LMA1043GMB-75	7243L75GB

DSP DIVISION CONT.	
LOGIC DEVICES CONT.	**IDT**
LMA1043PC	7243L100P
LMA1043DC	7243L100D
LMA1043GC	7243L100G
LMA1043DMB	7243L120DB
LMA1043GMB	7243L120GB
LMA2043	**7243**
LMA2043JC-45	7243L45J
LMA2043KC-45	7243L45L
LMA2043JC-55	7243L55J
LMA2043KC-55	7243L55L
LMA2043KMB-55	7243L55LB
LMA2043JC-65	7243L65J
LMA2043KC-65	7243L65L
LMA2043KMB-65	7243L65LB
LMA2043KMB-75	7243L75LB
LMA2043JC	7243L100J
LMA2043KC	7243L100L
LMA2043KMB	7243L120LB
LMU12	**7212**
LMU12DC-35	7212L35C
LMU12DC-45	7212L45C
LMU12DMB-45	7212L40CB
LMU12DMB-55	7212L55CB
LMU12DC-65	7212L45C
LMU12DMB-75	7212L55CB
LMU12DC	7212L70C
LMU12DMB	7212L90CB
LMU16	**7216**
LMU16PC-45	7216L45P
LMU16DC-45	7216L45C
LMU16GC-45	7216L45G
LMU16PC-55	7216L55P
LMU16DC-55	7216L55C
LMU16GC-55	7216L55G
LMU16DMB-55	7216L55CB
LMU16GMB-55	7216L55GB
LMU16PC-65	7216L65P
LMU16DC-65	7216L65C
LMU16GC-65	7216L65G
LMU16DMB-65	7216L55CB
LMU16GMB-65	7216L55GB
LMU16DMB-75	7216L75CB
LMU16GMB-75	7216L75GB
LMU16PC	7216L65P
LMU16DC	7216L65C
LMU16GC	7216L65G
LMU16DMB	7216L90CB
LMU16GMB	7216L90GB
LMU216	**7216**
LMU216JC-45	7216L45J
LMU216KC-45	7216L45L
LMU216JC-55	7216L55J
LMU216KC-55	7216L55L
LMU216KMB-55	7216L55LB
LMU216JC-65	7216L65J
LMU216KC-65	7216L65L
LMU216KMB-65	7216L65LB
LMU216KMB-75	7216L75LB
LMU216JC	7216L75J
LMU216KC	7216L75L
LMU216KMB	7216L90LB
LMU17	**7217**
LMU17PC-45	7217L45P
LMU17DC-45	7217L45C
LMU17GC-45	7217L45G
LMU17PC-55	7217L55P
LMU17DC-55	7217L55C
LMU17GC-55	7217L55G
LMU17DMB-55	7217L55CB
LMU17GMB-55	7217L55GB
LMU17PC-65	7217L65P
LMU17DC-65	7217L65C

LOGIC DEVICES CONT.	IDT
LMU17GC-65	7217L65G
LMU17DMB-65	7217L55CB
LMU17GMB-65	7217L55GB
LMU17DMB-75	7217L75CB
LMU17GMB-75	7217L75GB
LMU17PC	7217L65P
LMU17DC	7217L65C
LMU17GC	7217L65G
LMU17DMB	7217L90CB
LMU17GMB	7217L90GB
LMU217	**7217**
LMU217JC-45	7217L45J
LMU217KC-45	7217L45L
LMU217JC-55	7217L55J
LMU217KC-55	7217L55L
LMU217KMB-55	7217L55LB
LMU217JC-65	7217L65J
LMU217KC-65	7217L65L
LMU217KMB-65	7217L65LB
LMU217KMB-75	7217L75LB
LMU217JC	7217L75J
LMU217KC	7217L75L
LMU217KMB	7217L90LB

TRW	IDT
MPY012	**7212**
MPY012HJ1A	7212L140CB
MPY012HJ1C	7212L115C
MPY012HJ1G	7212L115C
MPY016	**7216**
MPY016HJ1A	7216L185CB
MPY016HJ1C	7216L140C
MPY016HJ1G	7216L140C
MPY016KJ1A	7216L45CB
MPY016KJ1A1	7216L45CB
MPY016KJ1C	7216L45C
MPY016KJ1C1	7216L35C
MPY016KJ1G	7216L45C
MPY016KJ1G1	7216L35C
TMC216H	**7216**
TMC216HC1A	7216L185LB
TMC216HC1C	7216L140L
TMC216HC1G	7216L140L
TMC216HJ3A	7216L185CB
TMC216HJ3C	7216L140C
TMC216HJ3G	7216L140C
TDC1009	**7209**
TDC1009C1A	7209L170LB
TDC1009C1F	7209L170LB
TDC1009J1A	7209L170CB
TDC1009J1C	7209L135C
TDC1009J1F	7209L170CB
TDC1009J1G	7209L135C
TDC1010	**7210**
TDC1010C1A	7210L200LB
TDC1010C1F	7210L200LB
TDC1010J1A	7210L200CB
TDC1010J1C	7210L165C
TDC1010J1F	7210L200CB
TDC1010J1G	7210L165C
TDC1043	**7243**
TDC1043C1C	7243L100L
TDC1043C1G	7243L100L
TDC1043J3C	7243L100C
TDC1043J3G	7243L100C
TMC2009	**7209**
TMC2009C1A	7209L170LB
TMC2009C1C	7209L135L
TMC2009C1F	7209L120LB
TMC2009C1G	7209L135L
TMC2009J3A	7209L170CB
TMC2009J3C	7209L135C
TMC2009J3F	7209L120CB
TMC2009J3G	7209L135C

TRW CONT.	IDT
TMC2010	**7210**
TMC2010C1C	7210L165L
TMC2010C1C	7210L200LB
TMC2010C1F	7210L200LB
TMC2010C1G	7210L165L
TMC2010J3A	7210L200CB
TMC2010J3C	7210L165C
TMC2010J3F	7210L200CB
TMC2010J3G	7210L165C
TMC2110	**7210**
TMC2110C1C	7210L100L
TMC2110C1C	7210L120LB
TMC2110C1F	7210L120LB
TMC2110C1G	7210L100L
TMC2110J3C	7210L100C
TMC2110J3C	7210L120CB
TMC2110J3F	7210L120CB
TMC2110J3G	7210L100C

Integrated Device Technology, Inc.

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AMD	IDT
2901B	**39C01C**
2901C	**39C01C**
2901CDC	39C01CD
2901CDCB	39C01CD
2901CLC	39C01CL
2901CPC	39C01CP
2901CPCB	39C01CP
2901C/BQA	39C01CDB
2901C/BUA	39C01CLB
2901C/BUC	39C01CLB
29C01	**39C01C**
29C01DC	39C01CD
29C01DCB	39C01CD
29C01PC	39C01CP
29C01PCB	39C01CP
29C01/BQA	39C01CDB
29C01/BUA	39C01CLB
29C01-1	**39C01C**
29C01-1DC	39C01CD
29C01-1DCB	39C01CD
29C01-1PC	39C01CP
29C01-1PCB	39C01CP
2903	**39C03A**
2903A	**39C03A**
2903ADC	39C03AC
2903ADCB	39C03AC
2903ALC	39C03AL
2903ADMB	39C03ACB
2903A/BXC	39C03ACB
2903ALMB	39C03ALB
2910 or -1	**39C10B**
2910A	**39C10B**
2910ADC	39C10BD
2910ADCB	39C10BD
2910ALC	39C10BL
2910APC	39C10BP
2910APCB	39C10BP
2910A/BQA	39C10BDB
2910A/BUC	39C10BLB
29C10A	**39C10B**
29C10ADC	39C10BD
29C10AJC	39C10BJ
29C10AJCB	39C10BJ
29C10ALC	39C10BL
29C10APC	39C10BP
29C10APCB	39C10BP
29C10A/BQA	39C10BDB
29C10A/BUA	39C10BLB
29C10A-1	**39C10C**
29C10A-1DC	39C10CD
29C10A-1DCB	39C10CD
29C10A-1JC	39C10CJ
29C10A-1JCB	39C10CJ
29C10A-1PC	39C10CP
29C10A-1PCB	39C10CP
29C101	**49C402**
29C111	**49C410**

AMD (CONT.)	IDT
29C660	**49C460**
29C660A	**49C460A**
29C660B	**49C460B**
29C660C	**49C460C**
2960	**39C60**
2960DC	39C60C
2960DCB	39C60C
2960JC	**39C60J**
2960JCB	**39C60J**
2960LC	39C60L
2960PC	39C60P
2960PCB	39C60P
2960/BXC	39C60CB
2960/BUC	39C60LB
29C60	**39C60**
29C60DC	39C60C
29C60DCB	39C60C
29C60JC	**39C60J**
29C60LC	39C60 L
29C60LCB	39C60 L
2960-1	**39C60-1**
2960-1DC	39C60-1C
2960-1DCB	39C60-1C
2960-1JC	**39C60-1J**
2960-1JCB	**39C60-1J**
2960-1LC	39C60-1L
2960-1PC	39C60-1P
2960-1PCB	39C60-1P
2960-1/BXC	39C60-1CB
2960-1/BUC	39C60-1LB
29C60-1	**39C60-1**
29C60-1DC	39C60-1C
29C60-1DCB	39C60-1C
29C60-1JC	**39C60-1J**
29C60-1LC	39C60-1L
29C60-1LCB	39C60-1L
29C60-1PC	39C60-1P
29C60-1PCB	39C60-1P
29C60-1/BXC	39C60-1CB
2960A	**39C60A**
2960ADC	39C60AC
2960ADCB	39C60AC
2960AJC	**39C60AJ**
2960ALC	39C60AL
2960APC	39C60AP
2960APCB	39C60AP
29C60A	**39C60A**
29C60ADC	39C60AC
29C60ADCB	39C60AC
29C60AJC	**39C60AJ**
29C60ALC	39C60AL
29C60ALCB	39C60AL
29C60APC	39C60AP
29C60APCB	39C60AP
29C60A/BXC	39C60ACB
29C60A/BUA	39C60ALB

CYPRESS	IDT
2901C	**39C01C**
2901CDC	39C01CD
2901CPC	39C01CP
2901CDMB	39C01CDB
7C901-31	**39C01C**
7C901-31DC	39C01CD
7C901-31LC	39C01CL
7C901-31PC	39C01CP
7C901-32DMB	39C01CDB
7C901-32LMB	39C01CLB
7C901-23	**39C01D**
7C901-23DC	39C01DD
7C901-23LC	39C01DL
7C901-23PC	39C01DP
7C901-27DMB	39C01DDB
7C901-27LMB	39C01DLB
7C910	**39C10B**
7C910-90	**39C10B**
7C910-99	**39C10B**
2910A	**39C10B**
2910ADC	39C10BD
2910AJC	39C10BJ
2910ALC	39C10BL
2910APC	39C10BP
2910ADMB	39C10BDB
2910ALMB	39C10BLB
7C910-50	**39C10B**
7C910-50DC	39C10BD
7C910-50JC	39C10BJ
7C910-50LC	39C10BL
7C910-50PC	39C10BP
7C910-51DMB	39C10BDB
7C910-51LMB	39C10BLB
7C910-40	**39C10C**
7C910-40DC	39C10CD
7C910-40JC	39C10CJ
7C910-40LC	39C10CL
7C910-40PC	39C10CP
7C910-46DMB	39C10CDB
7C910-46LMB	39C10CLB
7C9101	**49C402**

NOTES:
1. Bold text indicates a functional equivalent.
2. Plain text indicates a plug-in replacement.

Integrated Device Technology, Inc.

DATA CONVERSION CROSS REFERENCE GUIDE

TRW	IDT	PARAMETERS
TDC1018B7C	IDT75C18S125D	VDAC, Single 8-bit, CERDIP, Comm'l Temp Range
TDC1018B7G	IDT75C18S125D	VDAC, Single 8-bit, CERDIP, Comm'l w/ Burn-in
TDC1018C3C	IDT75C18S125L	VDAC, Single 8-bit, LCC, Comm'l Temp Range
TDC1018C3G	IDT75C18S125L	VDAC, Single 8-bit, LCC, Comm'l w/ Burn-in
TDC1018J7C	IDT75C18S125D	VDAC, Single 8-bit, Sidebraze, Comm'l Temp Range
TDC1018J7G	IDT75C18S125D	VDAC, Single 8-bit, Sidebraze, Comm'l w/ Burn-in
TDC1048J6C	IDT75C48S20D	Flash ADC, 1/2 LSB, Sidebraze, Comm'l Temp Range
TDC1048J6G	IDT75C48S20D	Flash ADC, 1/2 LSB, Sidebraze, Comm'l w/ Burn-in
TDC1048J6F	IDT75C48S20M	Flash ADC, 1/2 LSB, Sidebraze, Extended Temp Range
TDC1048J6A	IDT75C48S20M	Flash ADC, 1/2 LSB, Sidebraze, Extended, High-Rel
TDC1048J6V	IDT75C48S20DB	Flash ADC, 1/2 LSB, Sidebraze, MIL-883
TDC1048C3C	IDT75C48S20L	Flash ADC, 1/2 LSB, LCC, Comm'l Temp Range
TDC1048C3G	IDT75C48S20L	Flash ADC, 1/2 LSB, LCC, Comm'l w/ Burn-in
TDC1048C3F	IDT75C48S20LM	Flash ADC, 1/2 LSB, LCC, Extended Temp Range
TDC1048C3A	IDT75C48S20LM	Flash ADC, 1/2 LSB, LCC, Extended, High-Rel
TDC1048C3V	IDT75C48S20LB	Flash ADC, 1/2 LSB, LCC, MIL-883
TDC1048B6C	IDT75C48S20D	Flash ADC, 1/2 LSB, CERDIP, Comm'l Temp Range
TDC1048B6G	IDT75C48S20D	Flash ADC, 1/2 LSB, CERDIP, Comm'l w/ Burn-in
TDC1048N6C	IDT75C48S20P	Flash ADC, 1/2 LSB, Plastic, Comm'l Temp Range
TDC1318B5C	IDT75MB38P	VDAC, Triple 8-bit, CERDIP, Comm'l Temp Range
TDC1318B5G	IDT75MB38P	VDAC, Triple 8-bit, CERDIP, Comm'l w/ Burn-in
TDC1318J5C	IDT75MB38P	VDAC, Triple 8-bit, Sidebraze, Comm'l Temp Range
TDC1318J5G	IDT75MB38P	VDAC, Triple 8-bit, Sidebraze, Comm'l w/ Burn-in

ANALOG DEVICES	IDT	PARAMETERS
AD9048JN	IDT75C48SB20P	Flash ADC, 3/4 LSB, Plastic, Comm'l Temp Range
AD9048KN	IDT75C48S20P	Flash ADC, 1/2 LSB, Plastic, Comm'l Temp Range
AD9048SE	IDT75C48SB20LM	Flash ADC, 3/4 LSB, LCC, Extended Temp Range
AD9048SQ	IDT75C48SB20DM	Flash ADC, 3/4 LSB, Sidebraze, Extended Temp Range
AD9048TE	IDT75C48S20LM	Flash ADC, 1/2 LSB, LCC, Extended Temp Range
AD9048TQ	IDT75C48S20DM	Flash ADC, 1/2 LSB, Sidebraze, Extended Temp Range

DATEL	IDT	PARAMETERS
ADC304	IDT75C48S20P	Flash ADC, 1/2 LSB, Plastic, Comm'l Temp Range

SONY	IDT	PARAMETERS
CXA1096P	IDT75C48S20P	Flash ADC, 1/2 LSB, Plastic, Comm'l Temp Range

BROOKTREE	IDT	PARAMETERS
BT108BC	IDT75C18S125D	VDAC, Single 8-bit, CERDIP, Comm'l Temp Range
BT109KC	IDT75MB38P	VDAC, Triple 8-bit, CERDIP, Comm'l Temp Range
BT451KG125	IDT75C451S125G	PaletteDAC™, Triple 4-bit, PGA
BT451KG110	IDT75C451S110G	PaletteDAC™, Triple 4-bit, PGA
BT451KG80	IDT75C451S80G	PaletteDAC™, Triple 4-bit, PGA
BT457KG125	IDT75C457S125G	PaletteDAC™, Single 8-bit, PGA
BT457KG110	IDT75C457S110G	PaletteDAC™, Single 8-bit, PGA
BT457KG80	IDT75C457S80G	PaletteDAC™, Single 8-bit, PGA
BT458KG125	IDT75C458S125G	PaletteDAC™, Triple 8-bit, PGA
BT458KG110	IDT75C458S110G	PaletteDAC™, Triple 8-bit, PGA
BT458KG80	IDT75C458S80G	PaletteDAC™, Triple 8-bit, PGA
BT458SG/883	IDT75C458S110G	PaletteDAC™, Triple 8-bit, PGA, 883 Compliant

AMD	IDT	PARAMETERS
AM81C458	IDT75C458S110G	PaletteDAC™, Triple 8-bit, PGA

HONEYWELL	IDT	PARAMETERS
HDAC10180	IDT75C18S125D	VDAC, Single 8-bit, CERDIP, Comm'l Temp Range

FUJITSU	IDT
MBM10490-15C	IDT10490S15D
MBM10490-25C	IDT10490S20D
MBM10494-12C	IDT10494S10D
MBM100490-15C	IDT100490S15D
MBM100490-25C	IDT100490S20D
MBM100494-12C	IDT100494S10D
HITACHI	**IDT**
HM10490-12	IDT10490S12D
HM10490-15	IDT10490S15D
HM10490-20	IDT10490S20D
HM10494-10	IDT10494S10D
HM100490-15	IDT100490S15D
HM100490-20	IDT100490S20D
HM100494-10	IDT100494S10D
SARATOGA	**IDT**
SSM10494-15	IDT10494S15D
SSM10494-20	IDT10494S15D
SSM100494-15	IDT100494S15D
SSM100494-20	IDT100494S15D

Integrated Device Technology, Inc.

SUBSYSTEMS CROSS REFERENCE GUIDE

CYPRESS/MULTICHIP	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	ORG/PACKAGE
CYM1420HD-45C	8M824S45C		1024K(128KX8)
CYM1420HD-45C	8M824S45N		32 PIN DIP
CYM1420HD-55C	8M824S55C		
CYM1420HD-55C	8M824S45N		
CYM1420HD-70C	8M824S60C		
CYM1420HD-70C	8M824S60N		
CYM1421HD-70C	8M824S70C		
CYM1421HD-70C	8M824S70N		
CYM1421HD-85C	8M824S85C		
CYM1421HD-85C	8M824S85N		
CYM1421HD-100C	8M824L100C		
CYM1421HD-100C	8M824L100N		
CYM1460PS-45C	7MP4008S45S		512K X 8
CYM1460PS-55C	7MP4008S55S		36 PIN SIP
CYM1461PS-70C	7MP4008S70S		
CYM1461PS-85C	7MP4008L85S		
CYM1461PS-100C	7MP4008L100S		
CYM1610HD-XXX	8M656S40C		16K X 16
CYM1610HD-XXX	8M656S50C		40 PIN DIP
CYM1610HD-XXX	8M656S70C		
CYM1611HV-25C	7MC4005S25CV		16K X 16
CYM1611HV-35C	7MC4005S35CV		36 PIN DSIP
CYM1611HV-45C	7MC4005S45CV		
CYM1611HV-55C	7MC4005S55CV		
CYM1620HD-45C	8M624S45C		64K X 16
CYM1620HD-55C	8M624S50C		28 PIN DIP
CYM1620HD-70C	8M624S60C		
CYM1620HD-70C	8M624S70C		
CYM1621HD-25C		8M624,8MP624	1024K (64K X 16)
CYM1621HD-30C	7M624S30C		(128K X 8)
CYM1621HD-35C	7M624S35C		(256K X 4)
CYM1621HD-45C	7M624S45C		40 PIN DIP
CYM1621HD-55C	7M624S55C		
CYM1621HD-65C	7M624S65C		
CYM1641HD-35C	7M4016S35C		256K X 16
CYM1641HD-45C	7M4016L45C		48 PIN DIP
CYM1641HD-55C	7M4016L55C		
CYM1821PZ-25C		7MC4032S25CV	16K X 32
CYM1821PZ-30C		7MC4032S30CV	88 PIN DSIP
CYM1821PZ-35C		7MC4032S30CV	
CYM1821PZ-45C		7MC4032S40CV	
CYM1822HV-25C	7MC4032S25CV		16K X 32
CYM1822HV-30C	7MC4032S30CV		88 PIN DSIP
CYM1822HV-35C	7MC4032S35CV		
CYM1822HV-45C	7MC4032S45CV		
CYM1830HD-45C	7M4017S45C		64K X 32
CYM1830HD-55C	7M4017S55C		60 PIN DIP
CYM1830HD-70C	7M4017S70C		

DENSE PAC	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	ORG/PACKAGE
DPS1024-XXX		7M624	1024K(256KX4) (128KX8) (64KX16) 42 PIN DIP
DPS1026-XXX		7M624	1024K(256KX4) (128KX8) (64KX16) 40 PIN DIP
DPS1027-35C	7M624S35C		1024K(256KX4) (128KX8) (64KX16) 40 PIN DIP
DPS16X5-XXX	7MP564		64K(16KX5) 28 PIN SIP
DPS16X17-25 -35 -45 -55	7MC4005S25CV 7MC4005S35CV 7MC4005S45CV 7MC4005S55CV		16KX16 36 PIN DSIP
DPS257-XXX	7M656		256K(16KX16) (32KX8) (64KX4) 40 PIN DIP
DPS32H8-XXX DPS40256-XXX DPS41257-XXX	7M856 8M856	8M856	256K(32KX8) 28 PIN DIP
DPS41288-70 -85 -100	8M824S70C 8M824L85C, N 8M824L100C, N		1024K(128KX8) 32 PIN DIP
DPS6432-55 DPS6432-70	7M4017S55C 7M4017S70C		2048K(64K X 32) 60 PIN DIP
DPS8645-XXX	7MP456		256K(64KX4) 28 PIN SIP
DPS8808-XXX	7M864		64K(8KX8) 28 PIN DIP
EDI	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**ORG/PACKAGE**
EDH816H64C-35CC EDH816H64C-45CC EDH816H64C-55CC EDH816H64C-70CC EDH816H64C-35CMHR EDH816H64C-45CMHR EDH816H64C-55CMHR EDH816H64C-70CMHR	7M624S35C 7M624S45C 7M624S55C 7M624S65C 7M624S35CB 7M624S45CB 7M624S55CB 7M624S65CB	7MB624, 8MP624	64K X 16 40 PIN DIP
EDI8M1664C60CC EDI8M1664C70CC EDI8M1664C85CC EDI8M1664C100CC EDI8M1664C70CB EDI8M1664C85CB EDI8M1664C100CB	8M624S60C 8M624S70C 8M624S70C 8M624S70C 8M624S70CB 8M624S85CB 8M624S100CB		64K X 16 40 PIN DIP JEDEC PIN-OUT
EDI8M8128C60CC EDI8M8128C70CC EDI8M8128C80CC EDI8M8128C90CC EDI8M8128C100CC EDI8M8128C120CC	8M824S50C 8M824S50C 8M824S50C 8M824S50C 8M824S50C 8M824S50C	8M824SXXN, 8MP824S	1024K(128KX8) 32 PIN DIP

EDI	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	ORG/PACKAGE
EDI8M8128C150CC	8M824S50C		
EDI8M8128C70CB	8M824S70CB		
EDI8M8128C80CB	8M824S70CB		
EDI8M8128C90CB	8M824S85CB		
EDI8M8128C100CB	8M824S100CB		
EDI8M8128C120CB	8M824S100CB		
EDI8M8128C150CB	8M824S100CB		
EDI8M8128P90CC	8M824L70C	8M824LXXN,8MP824LXXS	1024K(128KX8)
EDI8M8128P100CC	8M824L70C		32 PIN DIP
EDI8M8128P120CC	8M824L70C		LOW POWER
EDI8M8128P150CC	8M824L70C		
EDI8M8128P90CB		8M824, 8MP824	
EDI8M8128P100CB			
EDI8M8128P120CB			
EDI8M8128P150CB			
EDH816H64C-55	7M624S55CB		1024K(128KX8)
EDH816H64C-70	7M624S65CB		40 PIN DIP
EDH816H16C-25CC-Z		7M656L, 8M656	16K X 16
EDH816H16C-35CC-Z			36 PIN ZIP
EDH816H16C-45CC-Z			
EDH816H16C-25	7MC4005S25CV		16K X 16
EDH816H16C-35	7MC4005S35CV		36 PIN DSIP
EDH816H16C-45	7MC4005S45CV		
EDH816H16C-55	7MC4005S55C		
EDI8M864C60CC	7M812S55C		64K X 8
EDI8M864C70CC	7M812S55C		32 PIN DIP
EDI8M864C80CC	7M812S55C		
EDI8M864C90CC	7M812S55C		
EDI8M864C100CC	7M812S55		
EDI8M864C120CC	7M812S55C		
EDI8M864C150CC	7M812S55C		
EDI8M864C70CB	7M812S65CB		
EDI8M864C80CB	7M812S65CB		
EDI8M864C90CB	7M812S85CB		
EDI8M864C100CB	7M812S100CB		
EDI8M864C120CB	7M812S100CB		
EDI8M864C150CB	7M812S100CB		
EDH8832HC-45CMHR	7M856S45CB	8M856L	32K X 8
EDH8832HC-45CMHR	7M856S55CB		28 PIN DIP
EDH84H64C-35CC-D3		7MP456	64K X 4
EDH84H64C-45CC-D3			24 PIN DIP
EDH84H64C-55CC-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CC-S	7MP456S35S		64K X 4
EDH84H64C-45CC-S	7MP456S45S		28 PIN SIP
EDH84H64C-55CC-S	7MP456S55S		
EDH81H256C-55	7MC156S55CS	7MP156	256K(256KX1)
EDH81H256C-70	7MC156S70CS		28 PIN SIP
EDH8808HC-55		8M864L55CB	64K(8KX8)
EDH8808HC-70		8M864L75CB	28 PIN DIP
EDH8808A-10	7M864L85CB		
EDH8808A-12	7M864L120CB		
EDH8088A-15	7M864L150CB		
EDH8808C-10	8M864L85CB		
EDH8808C-12	8M864L120CB		
EDH8808C-15	8M864L150CB		
EDH8808CL-20	8M864L150CB		

EDI	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	ORG/PACKAGE
EDH8808CL-25 EDH8808AL-20 EDH8808AL-25	8M864L150CB 7M864L150CB 7M864L150CB		
EDH8832C-12 EDH8832C-15 EDH8832C-20 EDH8832C-12 EDH8832C-15 EDH8832C-20 EDH8832HC-70 EDH8832HC-85 (see part number guide)	8M856L85C 8M856L85C 8M856L85C 8M856L100CB 8M856L100CB 8M856L100CB 7M856S65CB 7M856S75CB		256K(32KX8) 28 PIN DIP
MISC VENDORS	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**ORG/PACKAGE**
AEP AEPSS512K8-85 AEPSS512K8-10 AEPSS512K8-12 AEPSS512K8-10SL AEPSS512K8-12SL	 7MP4008S70S 7MP4008S70S 7MP4008L100S 7MP4008L100S	 7MP4008S70S	512K x 8 36 PIN SIP
HARRIS HM-8808, A		 7M134, 7M144	8K X 8 28 PIN DIP JEDEC
HM-8816HB, H		7M135, 7M145	16K X 8 28 PIN DIP JEDEC
HM-92560		7M856, 8M656	256K (32K X 8) (16K X 16) SYNCHRONOUS 48 PIN DIP
HITACHI HM66204-120ns HM66204-150ns	 8M824S50C 8M824S50C	 8M824SXXN, 8MP824	128K X 8 32 PIN DIP JEDEC
HM62256P-8 HM62256P-10 HM62256P-12	7M856S85C 7M856S85C 7M856S85C		32K X 8 28 PIN DIP
HM62256LP-8 HM62256LP-10 HM62256LP-12	8M856L85C 8M856L85C 8M856L85C		32K X 8 28 PIN DIP LOW POWER
INOVA S128K8-70C S128K8-85C S128K8-85M S128K8-100M S128K8-120M	 8M824S50C 8M824S50C 8M824S85CB 8M824S100CB 8M824S100CB	 8M824SXXN, 8MP824	128K X 8 32 PIN DIP JEDEC
S32K8-55C S32K8-70C S32K8-85C S32K8-70M S32K8-85M S32K8-100M	7M856S50C 7M856S70C 7M856S85C 7M856S65CB 7M856S75CB 7M856S90CB	8M856L 8M856LXXCB	32K X 8 28 PIN DIP JEDEC
MARCONI SF63000	 7M4016	 7MP4008	1 MEG (256K X 16) (512K X 8) 48 PIN DIP
MICROELECTRONICS MS12808 (100ns) MS12808 (120ns) MS12808 (150ns)	 8M824S50C 8M824S50C 8M824S50C	 8M824SXXN, 8MP824	128 K X 8 32 PIN DIP JEDEC

MISC VENDORS	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	ORG/PACKAGE
MITSUBISHI			128K X 8
MH12808TNA (100ns)	8M824S50C	8M824SXXN, 8MP824	32 PIN DIP
MH12808TNA (120ns)	8M824S50C		
MH51208S1N (70ns)	7MP4008S70C		512K X 8
MH51208S1N (85ns)	7MP4008S70C		64 PIN SIP
MH51208S1N (100ns)	7MP4008S70C		
MH51208S1N (120ns)	7MP4008S70C		
MOSAIC			256K X 1
MS1256CS (25ns)		7MP156, 7MC156	25 PIN SIP
MS1256CS (35ns)			
MS8128SC	8M824		128K X 8
			32 PIN DIP
MOSEL			128K X 8
MS88128 (100ns)	8M824S50C	8M824SXXN, 8MP824	32 PIN DIP
MS88128 (120ns)	8M824S50C		
MS88128 (150ns)	8M824S50C		
NEC			128K X 8
MC-120	8M824S50C	8M824SXXN, 8MP824	32 PIN DIP
SARATOGA			256K (32K X 8)
SSMM91256 (20ns)		7M856	38 PIN ZIP
SSMM91256 (25ns)			
SSMM91256 (30ns)			
SSMM91256 (35ns)			
SSMM91257, 258, 259		7M656, 8M656, 8MP656	256K (16K X 16)
		7MC4005	38 PIN ZIP
SSMM91512, 513, 514		7MC4032	512K (16K X 32)
			60 PIN ZIP
VALTRONIC			32K X 8
XXX (120ns)	7M85685C		28 PIN DIP
VITAREL			(64K X 16)
VMS10A24 (100ns)	8M824S50C	8M824SXXN, 8MP824	(128K X 8)
VMS10A24 (150ns)	8M824S50C	7M624, 7MB624,	(64K X 8)
VMS10A24 (200ns)	8M824S50C	8M624, 8MP624	40 PIN DIP
VMS32K8 (45ns)	7M856S45C	8M856L	32K X 8
VMS32K8 (55ns)	7M856S50C		28 PIN DIP
VMS32K8 (70ns)	7M856S70C		
VMS128K8M (55ns)	8M824S50C	8M824SXXN, 8MP824	128K X 8
VMS128K8M (60ns)	8M824S50C		32 PIN DIP
ZYREL			1 MEG (128K X 8)
Z108-10	8M824S50C	8M824SXXN, 8MP824	32 PIN DIP
Z108-15	8M824S50C		
Z108L-10	8M824L60C	8M824LXXN, 8MP824L	(LOW POWER)
Z108L-15	8M824L60C		

Product Selector and Cross Reference Guides

Technology/Capabilities

Quality and Reliability

Static RAMs

Multi-Port RAMs

FIFO Memories

Digital Signal Processing (DSP)

Bit-Slice Microprocessor Devices (MICROSLICE™) and EDC

Reduced Instruction Set Computer (RISC) Processors

Logic Devices

Data Conversion

ECL Products

Subsystems Modules

Application and Technical Notes

Package Diagram Outlines

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, our product strategy has been to apply the advantages of our extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of our innovative product designs offer higher levels of integration, advanced architectures, higher density packaging, and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance static RAMs, Specialty memories, ECL I/O RAMs, logic, DSP, Microprocessors (RISC and MICROSLICE™ bit-slice products), data conversion devices, and modular subsystem assemblies complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufactuer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing to determine the latest product offerings. If you're building state-of-the-art equipment, IDT may be able to solve some of your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance static RAMs, Logic, DSP, Microprocessor, Data Conversion and Modular Subsystem product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Each product line offers products which are fully compliant to the latest revision of MIL-STD-883. In addition, IDT offers radiation tolerant, as well as enhanced, products.

IDT has an active program to have a Defense Electronic Supply Center (DESC) listing for Standard Military Drawings (SMD) of its products. The SMD program allows standardization of militarized products and reduction of the proliferation of nonstandard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 64 devices which are listed or pending listing. The devices are from IDT's SRAM, Logic, DSP, Microprocessor and Data Conversion Product Lines. IDT expects to add another 75 devices to the SMD program. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681	71258S
5962-88545	71258L
5962-88544	71257L
5962-88725	71257S
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133S/7143S
5962-88665	7133L/7143L
SMP	**IDT**
5962-87531	7201LA
5962-86873	7216L
5962-86846	72404
5962-87686	7217L
5962-88669	7203S/7204S
	7203L/7204L
5962-89536	7202L

SMD	
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-87704	54FCT861A/B
5962-87667	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646A/B
	54FCT139/A
	54FCT824A/B
	54FCT533/A
	54FCT182/A
	54FCT645A/B
	54FCT640A/B
	54FCT534/A
	54FCT540/A
	54FCT541/A
MPR	**IDT**
5962-87708	39C10B & C
5962-88535	39C01
5962-88533	49C460A
5962-88613	39C60A
5962-88643	49C410
DCP	**IDT**
5962-88743	75C48S
	75C58
	75C458

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices are able to survive in hostile radiation environments. In total dose, dose rate and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all of its products on these processes.

Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an ongoing research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

CEMOS™ (the "E" stands for enhanced) is a state-of-the-art proprietary CMOS technology initially developed and continually refined by IDT to be at the leading-edge of new high-speed CMOS processes. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL.

The company has been producing CEMOS products in large volume for over seven years. During this time, CEMOS technology has been re-engineered and refined from the original 2.5 micron CEMOS I to the present CEMOS V direct step-on-wafer, dry etch process providing gate lengths as small as submicron (Figure 1). Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits.

CEMOS is a technology designed to optimize high-speed, low-power and dense integration of advanced architecture VLSI and memory products.

	CEMOS I	CEMOS II			CEMOS III		CEMOS V
		A	B	C	A	B	
Year	1981	1983	1984	1985	1986	1987	1988
Drawn Feature Size	2.5μ	1.7μ	1.5μ	1.5μ/1.2μ	1.3μ	1.2μ	1.0μ
Leff	1.3μ	1.1μ	0.9μ	0.9μ	0.9μ	0.8μ	0.6μ
Basic Process	Dual Well Oxide Isolated Ion Implanted Wet Etch Projection Aligned	Dry Etch Stepper Aligned					
Enhancements			Shrink	Spacer	Silicide LDD BPSG	Shrink BiCEMOS™ Multi-Layer Metal	Process Tolerance ±0.1μ

CEMOS IV = CEMOS III - scaled process optimized for high-speed logic.

Figure 1.

DUAL-WELL STRUCTURES

CEMOS is constructed using an advanced dual-well, or twin-well, process architecture (Figure 2) to optimize the overall characteristics of a high-performance CMOS process. CMOS processes using only "P-Wells" result in inferior P (or N) channel transistors or compromised P/N channels. This compromise is largely eliminated by utilizing both a deep underlying main "well" (in this case a "P-Well" in "N-substrate") and by altering the doping profile nearer the surface of the P-channel transistor regions. The latter region becomes the "N-Well" of the dual-well process. This technique allows the fabrication of high-performance transistors in both polarities.

The industry now recognizes that the best combination of balanced capabilities is achieved using this dual-well approach. This construction technique supresses punch-through, minimizes junction capacitance and transistor body effects and allows extremely fast speeds. In addition, it significantly reduces soft errors induced by high-energy alpha particles in fine line geometry memory products.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Another traditional limitation associated with many MOS and bipolar products is electrostatic discharge induced failures. This problem has also been solved by a combination of IDT's CEMOS process and proper circuit design. All IDT products incorporate proprietary ESD protection circuitry on all inputs and outputs to ensure that they are insensitive to repeated application of ESD stress and do not exhibit the degradation found in other MOS or bipolar products which can eventually result in product failure.

IDT CEMOS
Device Cross Section

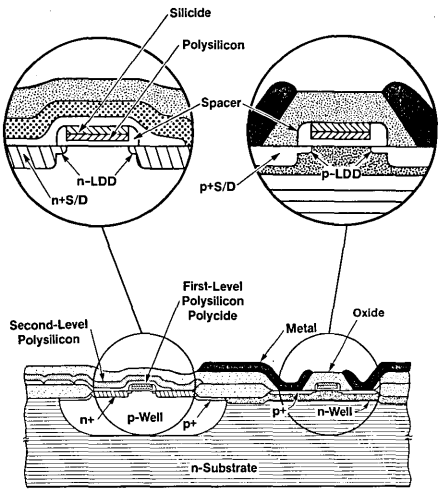


Figure 2.

IDT CEMOS
Built-In High Alpha Particle Immunity

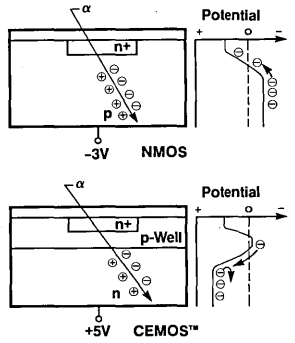


Figure 3.

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles in well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 2 & 3) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific technique used may vary and change from device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 4). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than 700mA.

IDT CEMOS
Latchup Suppression

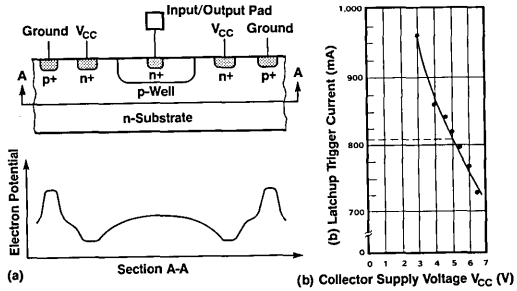


Figure 4.

SURFACE MOUNT TECHNOLOGY

To take full advantage of the low-power aspect of CMOS, and obtain two to three times the space savings, CMOS products should be used as SMDs (surface mount devices). However, most integrated circuits sold today are still packaged in the traditional DIP (dual in-line package) configuration and there is a tremendous support industry to handle thru-board assembly.

Determined to utilize CMOS advantages, IDT re-invented the DIP. This was accomplished by developing multilayered substrates (either co-fired ceramic or glass filled epoxy FR-4) with dual in-line (DIP) or single in-line (SIP) pins. An advanced IR (InfraRed) reflow and vapor phase reflow surface mount technology was also developed to produce the most reliable solder connections available.

Products that are to be interconnected to form larger electronic elements are electrically tested, environmentally screened, performance selected and then thermally matched to the appropriate ceramic or glass filled epoxy substrates. After modular assembly, the finished product is 100% re-tested to ensure that it completely performs to the specifications required.

As a result, IDT produces extraordinarily dense, high-speed combinations of monolithic ICs as complex subsystem modular assemblies. These modules convert SMDs to user-friendly DIPs/SIPs providing customers with the density advantages of surface mount in a format compatible with their extensive, thru-board, assembly expertise.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California — the heart of the "Silicon Valley." The company's operations are housed in five facilities totaling close to 400,000 square feet. These facilities incorporate all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. In-house capabilities incorporate scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic packaging, military and commercial testing, burn-in, life test and a full complement of environmental screening equipment.

IDT's 54,000 square foot Corporate Headquarters houses technology and product research and development. Teams equipped with state-of-the-art computerized design and analytical tools conduct the continuous research and development required to push CEMOS technology forward and to create future product lines. This facility contains a 10,000 square foot Class 10 (no more than 10 particles larger than 0.2 micron per cubic foot) wafer fabrication clean room used to produce the Microprocessor, DSP and Logic product families, as well as support R&D.

Located adjacent to the headquarter facility, forming an IDT corporate campus, is a 100,000 square foot two-building complex that houses the DSP Division and Microprocessor product line. Design and product teams, along with administrative functions, are situated in these buildings.

A second small wafer fabrication area, used for research and development, is also located at this site. This facility houses its own design tools, laboratories, test and burn-in facilities and in-house plastic assembly.

IDT's Subsystem Division is housed in a third Santa Clara location, only a few blocks away from the other sites. This 37,000 square foot facility contains the development and product teams that produce IDT's FCT, AHCT, IDT39C800 logic families and modular assemblies. Included at this facility are a quick turnaround hermetic package assembly line and an advanced vapor phase reflow surface mounting module assembly area.

IDT's largest facility is located in Salinas, California, about an hour away from Santa Clara. This is the Static RAM Division's headquarters, a 100,000 square foot facility located on a 14 acre site. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume wafer fabrication area measured at Class 2-to-3 clean room conditions (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger). Careful design and construction created a clean room environment far beyond the average of U.S. fab areas (Class 100), capable of producing large volumes of very high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site has future expansion capabilities to accomodate a 250,000 square foot complex.

IDT's Packaging and Assembly Process Development teams are located at the Corporate Headquarters in Santa Clara. To keep pace with the development of new products and to enhance the IDT philosophy of "Innovation," these teams have ultra modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 Laminar Flow Hoods.

Development of assembly materials, processes and equipment is accomplished in these two facilities under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA manufactured product while developing state-of-the-art surface mount technology, patterned after MIL-STD-883.

To extend these philosophies while maintaining strict control of our processes, IDT has acquired an operational Assembly and Test facility located in Penang, Malaysia. This facility has been upgraded to USA standards and is fully operational. As in the USA facility, all assemblies will be accomplished under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility will be manufactured to the quality control requirements of MIL-STD-883.

IDT's facilities total nearly 400,000 square feet of floor space and house three wafer fabrication clean rooms, four assembly lines, five test areas and four burn-in areas. All of these facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing—as opposed to being "tested-in" later—in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials and chemicals are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For module assemblies, additional screening of the fully assembled substrates is performed to assure package integrity and mechanical reliability. One-hundred percent electrical tests are performed on the finished module to ensure compliance with the defined "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-M-38510 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *modular* hermetic products are fully compliant with the MIL-STD-883 test procedures for electronic module assemblies on ceramic substrates.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

MONOLITHIC HERMETIC PACKAGE PROCESSING FLOW[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

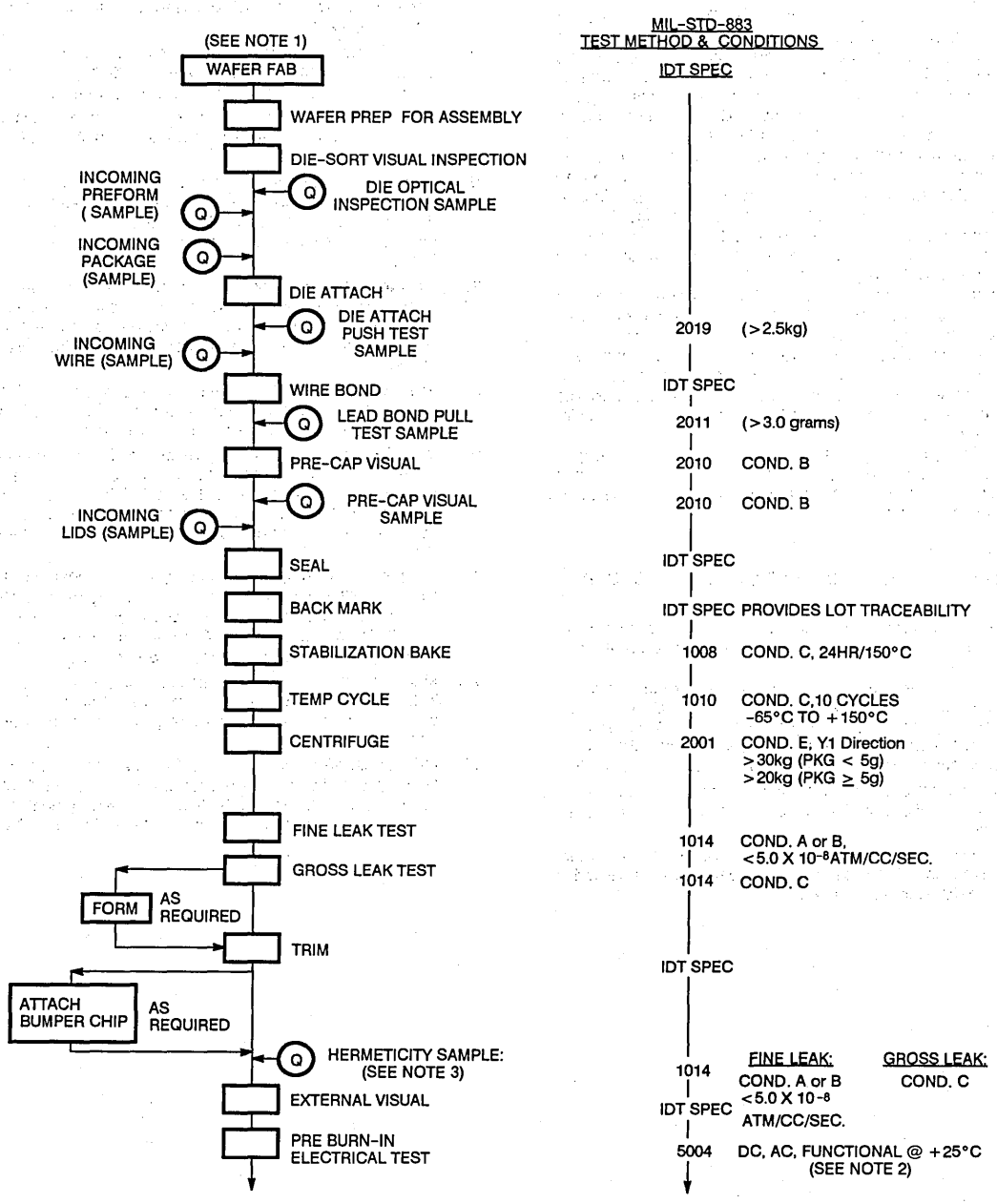
1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.
2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT defined internal criteria.
3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.
4. **Wire Bond Monitor:** Products samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.
5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.
6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical stress tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.
7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.
8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in to the same conditions as Military Grade devices.
10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the -55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.
11. **Mark:** All product is marked with product type and lot code indentifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.
12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Monolithic Hermetic Package Processing Flow



SEE FINAL PROCESSING FLOW ON PAGE 3-3 FOR REMAINDER OF OPERATIONS AND NOTES

Monolithic Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 160 Hours	100% 16 Hours	100% 16 Hours
Post Burn-in Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	100% +25, -55 & +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)[4]	5004 or IDT Spec.	5%	10%	10%
Group A Electrical: Static (DC), Functional and Switching (AC)[2]	5005 & IDT Spec.	Sample -55 & +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical[2]	IDT Spec.	100%[5]	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	5005 (Group B, C, D)	Yes	–	–
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

NOTES:

1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. This hermeticity sample is performed after all lead finish operations.
4. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
5. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
6. (Q) Quality sample inspection

SUMMARY

MONOLITHIC PLASTIC PACKAGE PROCESSING FLOW

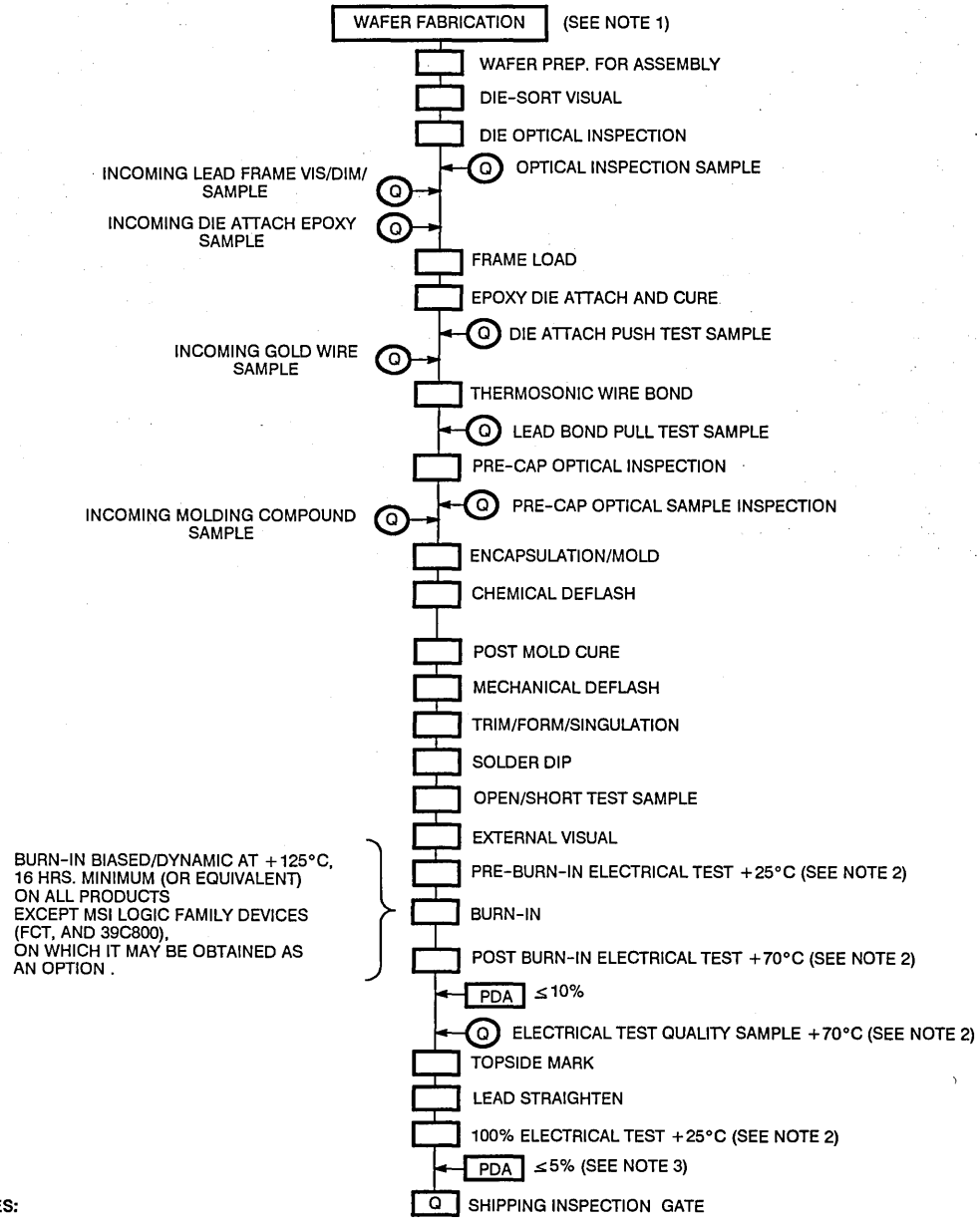
Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to scanning electron microscope analysis on a periodic basis.
2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict internal criteria.
3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests.
4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.
5. **Pre-cap Visual:** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.
6. **Post Mold Cure:** Plastic encapsulated devices are baked to insure an optimum plastic seal so as to enhance moisture barrier characteristics.
7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in 16 hours at +125°C (or equivalent), utilizing the same burn-in circuit conditions as the Military Grade product.
9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.
10. **Mark:** All product is marked with product type and lot code identifiers.
11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated the test methods are patterned after MIL-STD-883 criteria.

Monolithic Plastic Package Processing Flow



NOTES:

1) All screens are 100% unless otherwise noted.
2) All electrical test programs are per the applicable IDT test specification.
3) IDT performs a 100% electrical test at +25°C with a 5% PDA limit at this point.
4) (Q) = Quality sample inspection

SUMMARY

MODULE ASSEMBLY HERMETIC PACKAGE PROCESSING FLOW[1]

Refer to the Module Assembly Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

Components

1. ***Military Grade Class B monolithic microcircuit products*** utilized in Module Assembly products are manufactured and screened in compliance with the applicable demanding criteria of MIL-STD-883. (See the Monolithic Hermetic Package Processing Flow diagram.)
2. ***Commercial Grade monolithic microcircuit products*** utilized in Module Assembly products differ from Military Grade only in the burn-in time and electrical test temperatures.
3. ***Passive components*** such as chip capacitors are obtained from qualified vendors to the applicable military and IDT specifications.

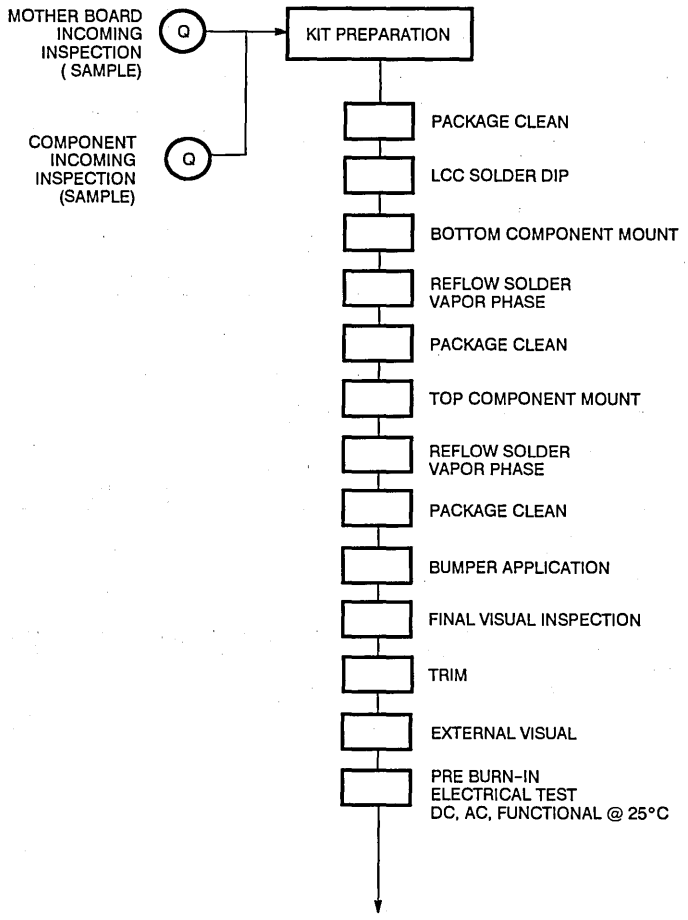
Modules

1. **Module Assembly:** The active and passive components and substrates used in the assembly of modules must pass incoming inspection requirements. The components are then mounted onto the substrate using the reflow solder vapor phase technique.
2. **Pre-Burn-In Electrical Test:** Each module is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
3. **Burn-In:** 100% of Military Grade module product is burned-in under the dynamic electrical conditions of Method 1015, Condition D, for 44 ± 4 hours at a T_A of +125°C. Commercial Grade module products do not require burn-in.
4. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the -55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.
5. **PDA Calculation:** A PDA (Percent Defective Allowed) of 5% is imposed on all Military module products for the 25°C parameters after completion of burn-in.
6. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliancy code letter.
7. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to 100% screening tests are routinely subjected to the Quality Conformance Inspection requirements of MIL-STD-883 applicable to Module Assembly products.
8. **External Visual:** Product is 100% visually inspected prior to shipment to the applicable criteria for modules as required by MIL-STD-883.

NOTE:

1. For quality requirements beyond Class B levels, such as SEM analysis, X-ray inspection, Particle Impact Noise Detection (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Module Assembly Hermetic Package Processing Flow



SEE FINAL PROCESSING FLOW ON PAGE 3-8 FOR REMAINDER OF OPERATIONS AND NOTES

Module Assembly Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 44 ± 4 Hours	–	–
Post Burn-in Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	100% +25, -55 & +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)[3]	5004	5%	–	–
Group A Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	Sample -55 & +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical[2]	IDT Spec.	100%[4]	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	(Note 5)	Yes	–	–
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

NOTES:

1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
4. IDT performs a 100% electrical test at +25° C with a 5% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 5, with an accept number of 1. If a lot fails the 5% PDA limit, it may be rescreened one time only to a tightened PDA limit of 3%.
5. IDT presently utilizes QCI tests patterned after method 5005. A new method for module products is under development by the military.
6. (Q) Quality sample inspection

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The lower power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS(SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by devices in the system due to a pulse event, and is measured in RADS(SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is created either through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

RADIATION CATEGORY	PRIMARY PARTICLE	SOURCE	EFFECT
Total Dose	Gamma	Space or Nuclear Event	Permanent
DoseRate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-Up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as error checking and correction (ECC) circuitry, since the occurrance of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU data has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing).

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance, or radiation "hardness", as shown in Figure 2.

- Radiation Enhanced process uses Epi wafers and is able to provide memory devices that are qualified by IDT's Total Dose test plan for levels of 10K RADs Total Dose [RADs/Si]. 'RE non-memory devices are qualified by IDT's Total Dose test plan for levels of 30K RADs Total Dose [RADs (Si)]. Higher Total Dose levels are possible for more information contact IDT's Radiation Hardened Product Group.
- Radiation Tolerant process uses standard wafer material and is able to provide devices (memory and non-memory) that are qualified by IDTs Total Dose test plan to 10K RADs Total Dose [RADs (Si)].

TYPE OF RADIATION	UNITS	PRODUCT TYPES MEMORY	MEMORY+ LOGIC	LOGIC	IDT PROCESS
Total Dose	RADs (Si) [Rate: 10K RADs (Si)/min.]	≤6K	≤6K	≤15K	Standard
		≥10K	≥10K	≥10K	Tolerant
		≥10K*	≥10K*	≥30K*	Enhanced
Dose Rate (Latchup)	RADs(Si)/sec. [pulse width = 50ns]	1.0E8			Standard
		1.0E8			Tolerant
		>2.4E10	>2.4E10	>2.4E10	Enhanced
		----------No Latchup----------			

*Note: consult IDT's Radiation Hardened Product Group for higher Total Dose level considerations.

Figure 2.

Integrated Device Technology can provide radiation tolerant/enhanced versions of any of its products. Consult IDT's Radiation Hardened Product Group for product availability/ordering information.

Please contact your local IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications. Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

SRAM INTRODUCTION

Integrated Device Technology is the major U.S. supplier of high-performance Static Random Access Memories. Leading edge CEMOS and BiCEMOS process technology, coupled with advanced design techniques, enables IDT to supply our military and commercial customers with production volumes of the industry's fastest SRAMs. IDT is committed to providing our customers with early access to innovative circuit designs, taking full advantage of this advanced process technology. This results in the broadest range of SRAM speeds, densities and organizations available in today's market.

Integrated with performance leadership at IDT is a commitment to provide our customers with a wide selection of SRAM organizations. 16K, 64K and 256K devices are offered in x1, x4 and x8 organizations. This year, these offerings will be expanded to include x16 and x9 devices, as well as 1 Megabit densities. To further match IDT SRAMs with system architectural needs, several devices are available with separate inputs and outputs, additional control features and functions.

Leadership products offered by IDT include BiCEMOS devices, incorporating both TTL and ECL compatible inputs and outputs, as well as CEMOS devices offering true CMOS I/O levels. These products confirm our charter to offer technology to system designers in its most friendly and usable form.

Cache is an area of strong emphasis for IDT. It is critical for RISC-based systems, and most microprocessors require caches since DRAM speeds have not kept up with microprocessor speeds.

IDT offers the largest Cache-Tag RAM in the industry, the 7174 (8K x 8); and the fastest Cache-Tag RAM in the industry, the 6178 (4K x 4). IDT also has the most complete line of Data RAMs available anywhere. The 71586 with latched addresses is the industry's first specialty RAM intended for cache data storage.

Our fast standard RAMs with Output Enable are also used as Data RAMs, with specifications optimized for the fastest IDT79R3000 applications.

Our intensive and innovative process technology development effort has resulted in truly outstanding advances in device performance. Over the past 7 years, as an example, our 2K x 8 SRAM has been redesigned in successively advanced CEMOS processes, progressing from 2μ geometries to less than 1μ. This resulted in access time being improved by about a factor of 10, to the currently available 15 nanosecond devices. This continuing dedication to advancement will result in 1 Megabit CEMOS devices and 256K bit BiCEMOS devices this year.

IDT's advanced SRAMs are available in a wide variety of packages, ranging from commercial surface mount through DIPs and LCCs to military flatpacks. This continually expanding package offering is in direct response to critical second-level interconnect issues confronting today's system designer. Our commitment to technology extends to advanced, cost-effective packaging techniques.

Both commercial and military versions of all IDT SRAMs are available. Our military devices are manufactured and processed strictly in conformance with all the administrative, processing and performance requirements of MIL-STD-883. Having anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As a leading supplier of military SRAMs, IDT provides performance and quality levels second to none. Our commercial products, in fact, share most processing steps with military devices.

IDT's continuing commitment to cutting edge technology and performance will assure the availability of SRAMs most compatible with the exacting needs of today's systems. Look to IDT SRAMs for performance, technology, quality and imaginative solutions to memory system problems.

TABLE OF CONTENTS

TABLE OF CONTENTS (CON'T.)

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT 6167SA
IDT 6167LA

4

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - IDT6167SA
    Active: 200mW (typ.)
    Standby:100µW (typ.)
  - IDT6167LA
    Active: 150mW (typ.)
    Standby:10µW (typ.)
- Battery backup operation—2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and plastic DIP, 20-pin Flatpack or CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-84132 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

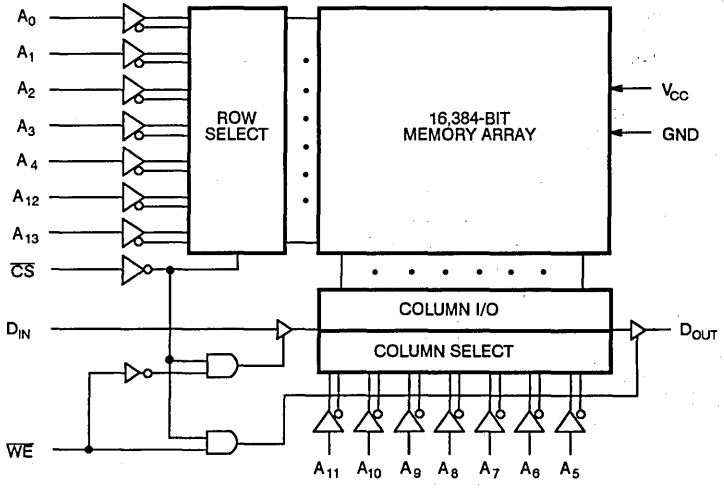
Access times as fast as 12ns are available with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, plastic 20-pin SOIC, 20-pin flatpack or CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

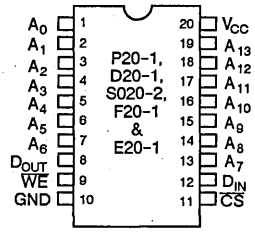
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

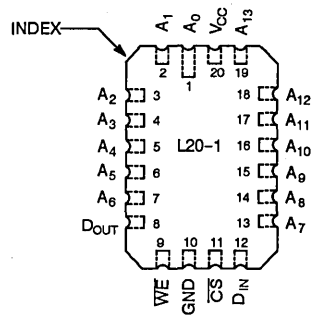


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

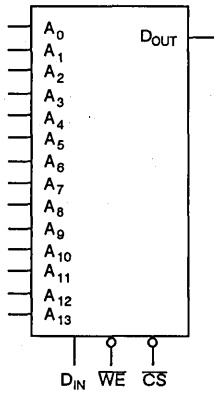


DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	Address Inputs	D_{IN}	$DATA_{IN}$
$\overline{CS}$	Chip Select	D_{OUT}	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT6167SA MIN.	IDT6167SA TYP.(1)	IDT6167SA MAX.	IDT6167LA MIN.	IDT6167LA TYP.(1)	IDT6167LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1) V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6167SA12(4) COM'L.	6167SA12(4) MIL.	6167SA15 6167LA15 COM'L.	6167SA15 6167LA15 MIL.	6167SA20/25 6167LA20/25 COM'L.	6167SA20/25 6167LA20/25 MIL.	6167SA35 6167LA35 COM'L.	6167SA35 6167LA35 MIL.	6167SA45(5) 6167LA45(5) COM'L.	6167SA45(5) 6167LA45(5) MIL.	6167SA55(5) 6167LA55(5) COM'L.	6167SA55(5) 6167LA55(5) MIL.	6167SA70(5) 6167LA70(5) COM'L.	6167SA70(5) 6167LA70(5) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	–	90	90	90	90	90	90	–	90	–	90	–	90	mA
		LA	–	–	55	60	55	60	55	60	–	60	–	60	–	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL} Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	140	–	120	130	100	110/100	100	100	–	100	–	100	–	100	mA
		LA	–	–	100	110	80/70	85/75	65	70	–	65	–	60	–	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	SA	50	–	50	50	35	35	35	35	–	35	–	35	–	35	mA
		LA	–	–	35	35	30/25	30/25	20	20	–	20	–	20	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(3)	SA	10	–	5	10	5	10	5	10	–	10	–	10	–	10	mA
		LA	–	–	0.9	2	0.05	2/0.9	0.05	0.9	–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices
3. f = f_{MAX} (All Inputs cycling at f = $1/t_{RC}$). f = 0 means no address control lines change.
4. 0°C to +70°C temperature range only.
5. -55°C to +125°C temperature range only.

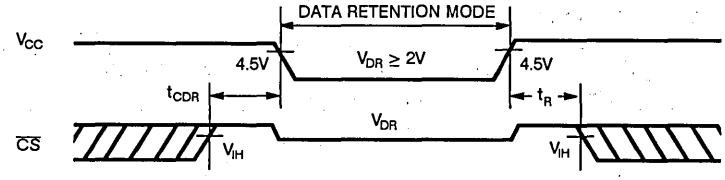
DATA RETENTION CHARACTERISTICS

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC}@ 2.0V	TYP.(1) V_{CC}@ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.0	200	300	µA
			COM'L.	–	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

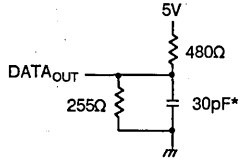


Figure 1. Output Load

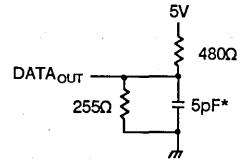


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

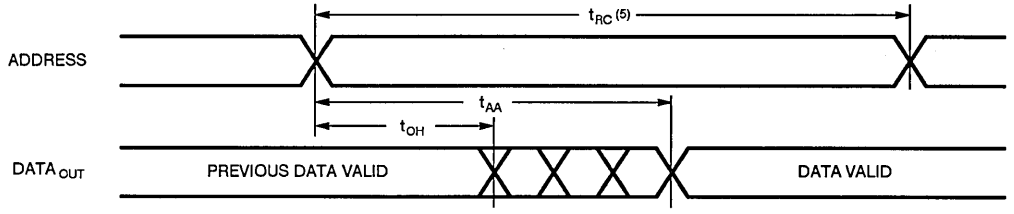
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6167SA12[1] MIN.	6167SA12[1] MAX.	6167SA15 6167LA15 MIN.	6167SA15 6167LA15 MAX.	6167SA20/25 6167LA20/25 MIN.	6167SA20/25 6167LA20/25 MAX.	6167SA35/45[2] 6167LA35/45[2] MIN.	6167SA35/45[2] 6167LA35/45[2] MAX.	6167SA55[2]/70[2] 6167LA55[2]/70[2] MIN.	6167SA55[2]/70[2] 6167LA55[2]/70[2] MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	12	–	15	–	20/25	–	35/45	–	55/70	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{ACS}	Chip Select Access Time	–	12	–	15	–	20/25	–	35/45	–	55/70	ns
t_{OH}	Output Hold from Address Change	3	–	3	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Deselect to Output in Low Z[3]	3	–	3	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Select to Output in High Z[3]	–	8	–	10	–	10	–	15/30	–	40	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	12	–	15	–	20/25	–	35	–	55/70	ns

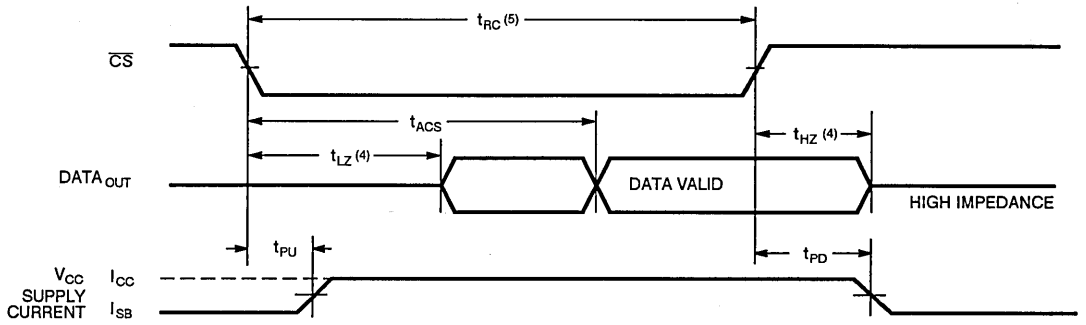
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

4

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

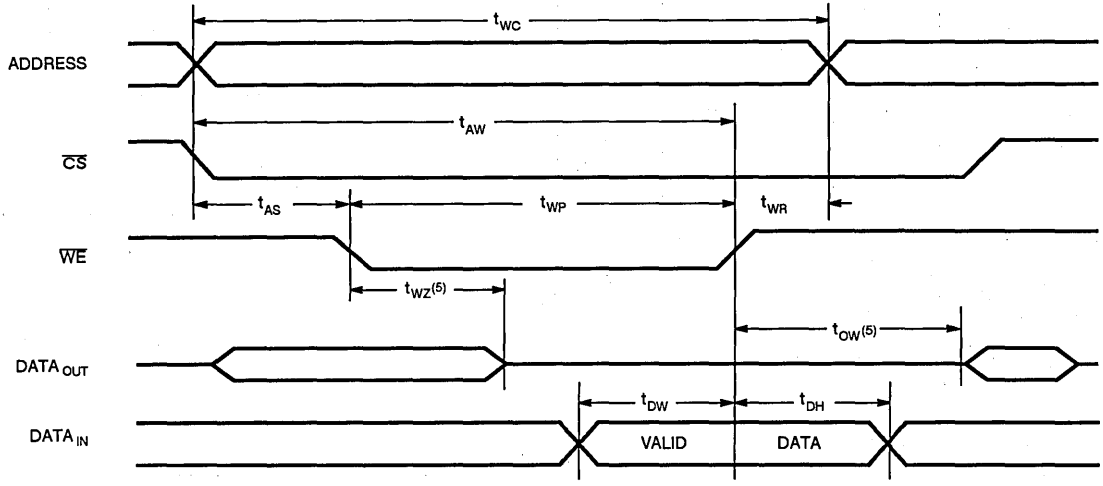
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6167SA12[1]		6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45[2] 6167LA35/45[2]		6167SA55[2]/70[2] 6167LA55[2]/70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	12	–	15	–	20/20	–	30/45	–	55/70	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AW}	Address Valid to End of Write	12	–	15	–	15/20	–	30/40	–	45/55	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	15/20	–	30	–	35/40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	10	–	10	–	12/15	–	17/20	–	25/30	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	6	–	7	–	8	–	15/30	–	40	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	ns

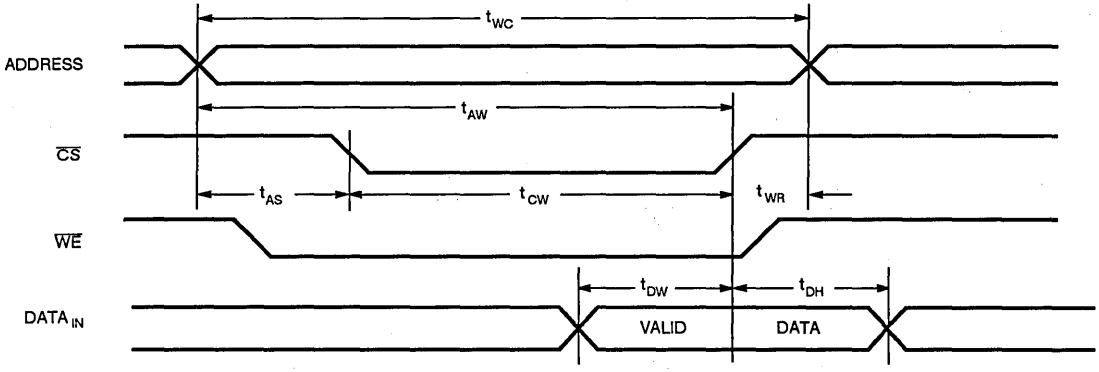
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)

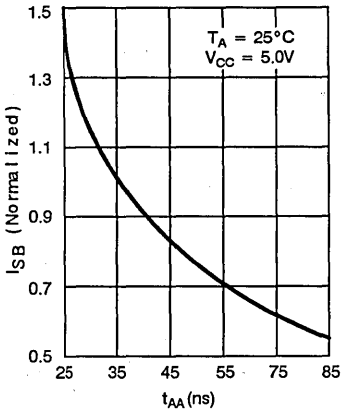


NOTES:

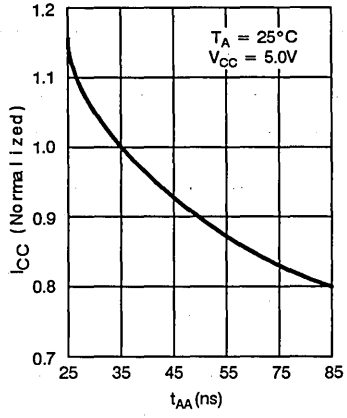
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

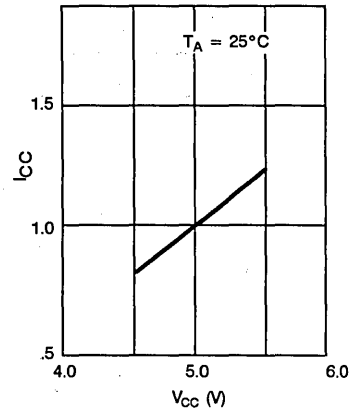
I_{SB} vs. t_{AA} (35ns Device)



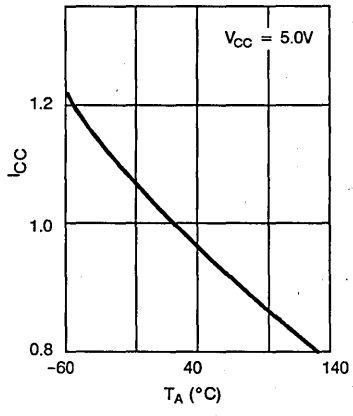
I_{CC} vs. t_{AA} (35ns Device)



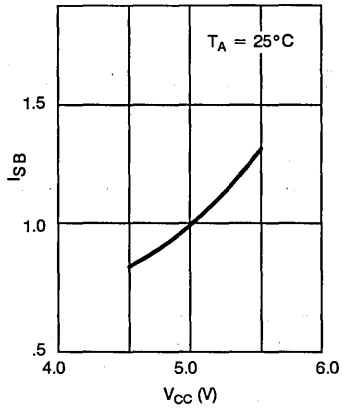
I_{CC} vs. Supply Voltage



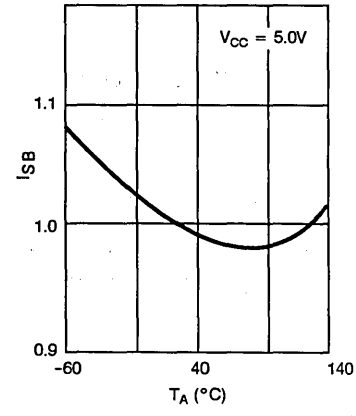
I_{CC} vs. Temperature



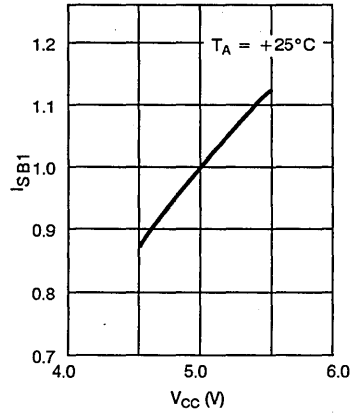
I_{SB} vs. Supply Voltage



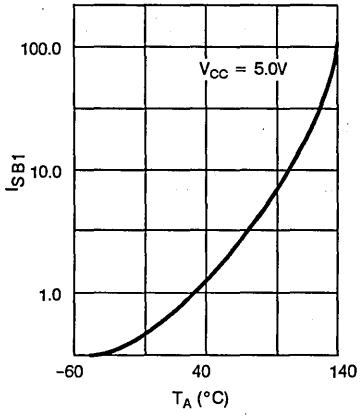
I_{SB} vs. Temperature



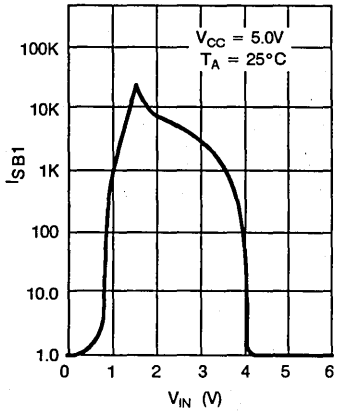
I_{SB1} vs. Supply Voltage



I_{SB1} vs. Temperature

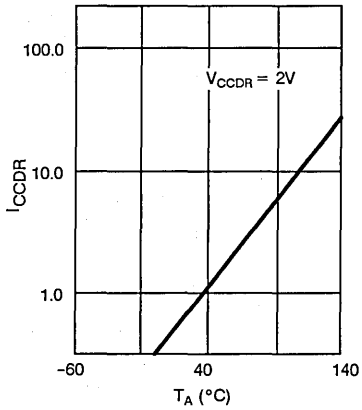


I_{SB1} vs. V_{IN}

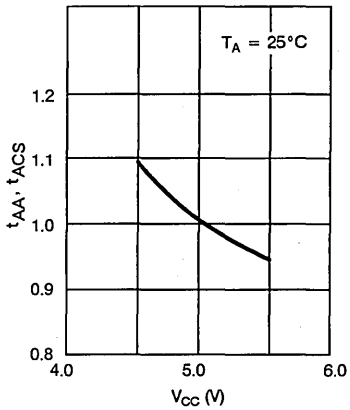


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

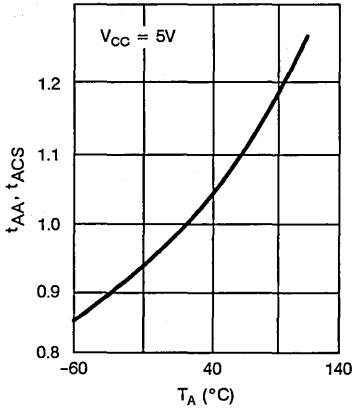
I_{CCDR} vs. Temperature



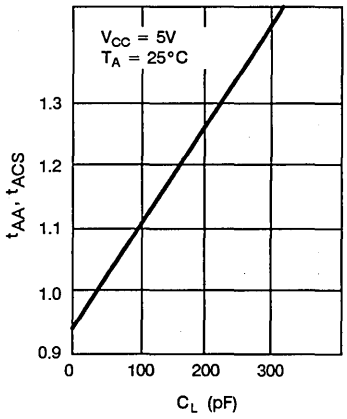
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

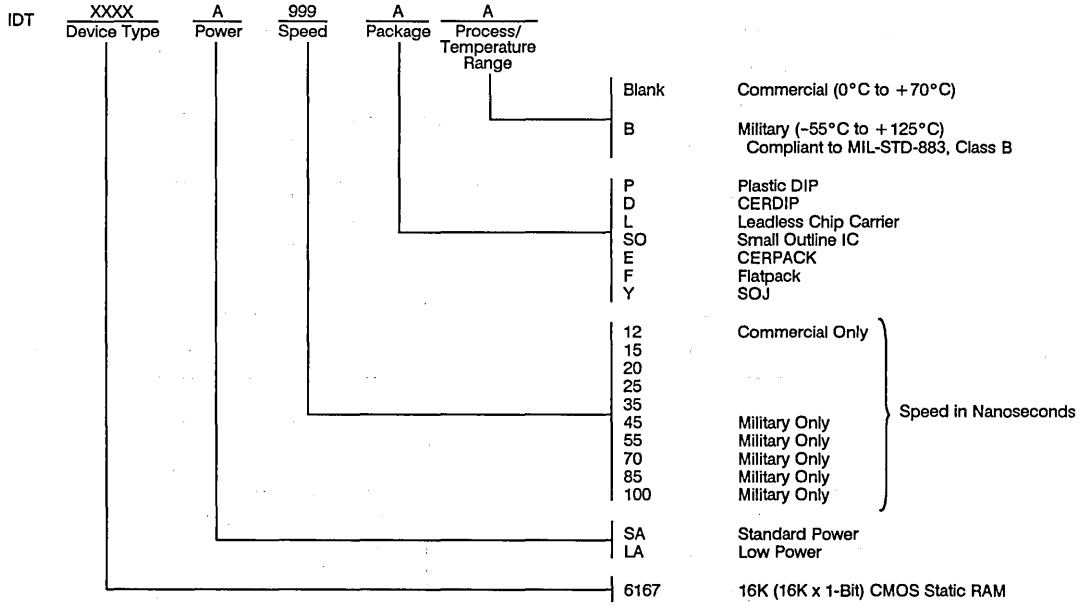
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization and is not production tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT 7187S
IDT 7187L

4

FEATURES:

- High speed (equal access and cycle time)
  - Military: 25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7187S
    Active: 300mW (typ.)
    Standby: 100µw (typ.)
  - IDT7187L
    Active: 250mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and hermetic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin flatpack and CERPACK
- Produced with advanced CEMOS™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86015 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

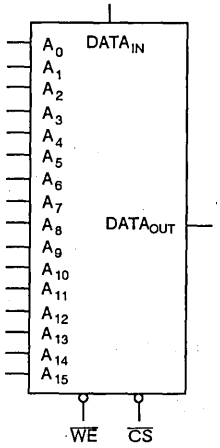
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 15ns are available with maximum power consumption of 880mW.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation (358mW max.); I_{SB1} provides ultra-low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

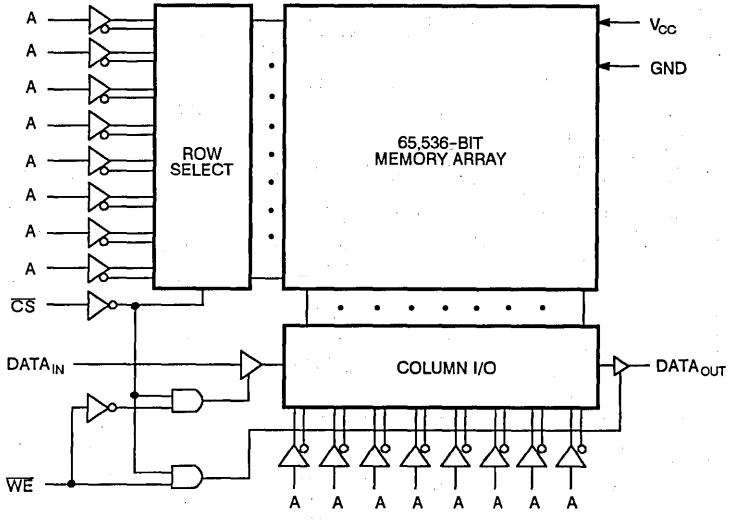
Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or hermetic DIP, 24-pin plastic SOIC, 22- and 28-pin leadless chip carriers, or 24-pin flatpack or CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



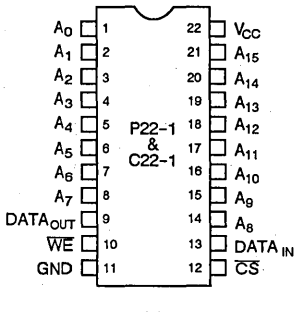
FUNCTIONAL BLOCK DIAGRAM



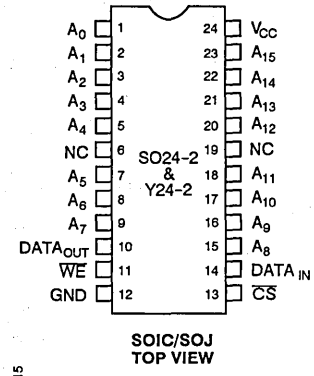
CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-1025/1

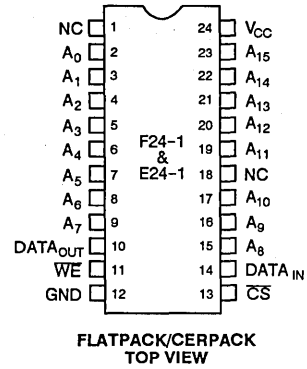
PIN CONFIGURATIONS



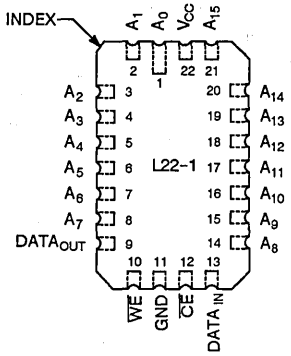
DIP
TOP VIEW



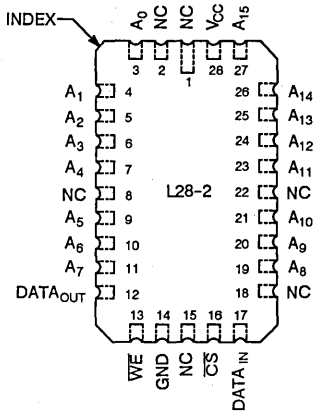
SOIC/SOJ
TOP VIEW



FLATPACK/CERPACK
TOP VIEW



22-PIN LCC
TOP VIEW



28-PIN LCC
TOP VIEW

PIN NAMES

A_0–A_{15}	Address Inputs	$DATA_{IN}$	Data Input
$\overline{CS}$	Chip Select	$DATA_{OUT}$	Data Output
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7187S MIN.	IDT7187S TYP.(1)	IDT7187S MAX.	IDT7187L MIN.	IDT7187L TYP.(1)	IDT7187L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7187S15 COM'L.	7187S15 MIL.	7187S20 COM'L.	7187S20 MIL.	7187S25 7187L25 COM'L.	7187S25 7187L25 MIL.	7187S30/35 7187L30/35 COM'L.	7187S30/35 7187L30/35 MIL.	7187S45/55(3) 7187L45/55(3) COM'L.	7187S45/55(3) 7187L45/55(3) MIL.	7187S70 7187L70 COM'L.	7187S70 7187L70 MIL.	7187S85 7187L85 COM'L.	7187S85 7187L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	90	105	90	105	90	105	–	105	–	105	mA
		L	–	–	–	–	70	85	70	85	70	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	120	130	110	120	110	120	–	120	–	120	mA
		L	–	–	–	–	100	110	95/90	110/100	85	95	–	90	–	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	65	–	60	65	55	55	45	50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30/25	35/30	–	28	–	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.3	1.5	0.3	1.5	0.3	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
3. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS

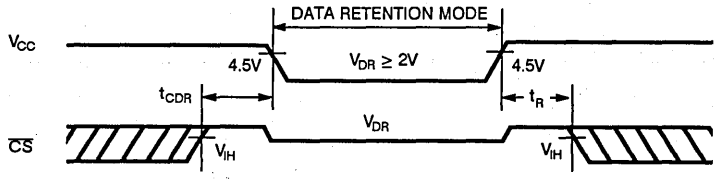
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

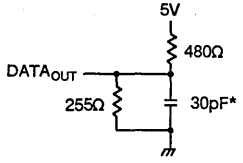


Figure 1. Output Load

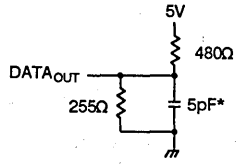


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

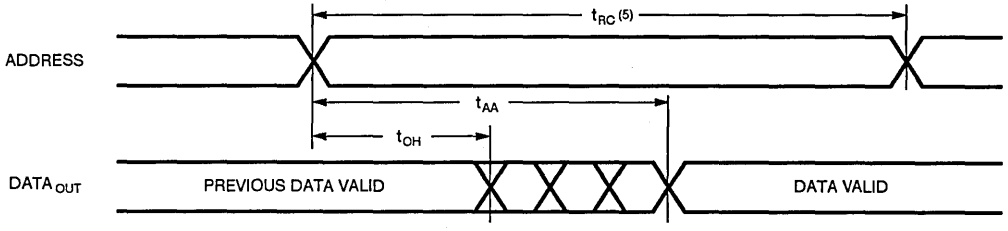
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

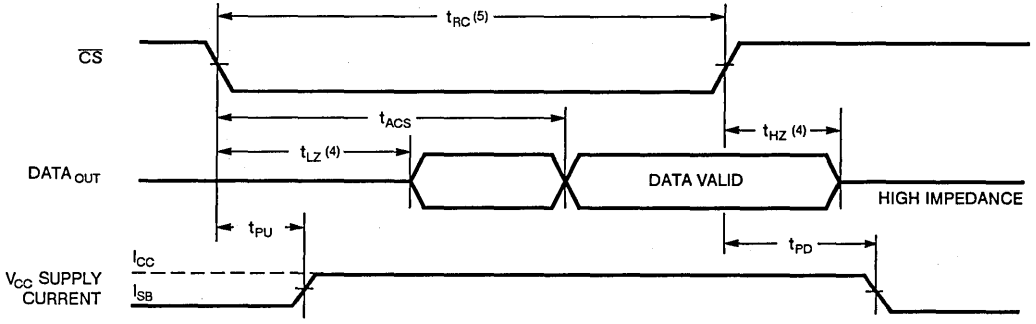
SYMBOL	PARAMETER	7187S15[1]/20 MIN.	7187S15[1]/20 MAX.	7187S25/30 7187L25/30 MIN.	7187S25/30 7187L25/30 MAX.	7187S35/45 7187L35/45 MIN.	7187S35/45 7187L35/45 MAX.	7187S55[2] 7187L55[2] MIN.	7187S55[2] 7187L55[2] MAX.	7187S70[2] 7187L70[2] MIN.	7187S70[2] 7187L70[2] MAX.	7187S85[2] 7187L85[2] MIN.	7187S85[2] 7187L85[2] MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	6	–	12/15	–	17/20	–	30	–	30	–	40	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15/20	–	20/30	–	30/35	–	35	–	35	–	40	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



NOTES:
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

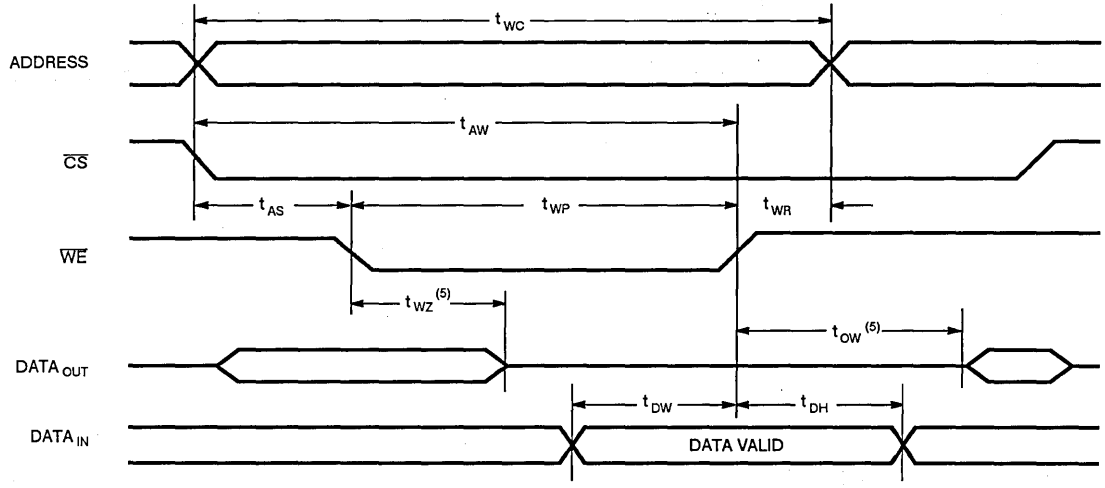
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7187S15[1]/20		7187S25/30 7187L25/30		7187S35/45 7187L35/45		7187S55[2] 7187L55[2]		7187S70[2] 7187L70[2]		7187S85[2] 7187L85[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	12/15	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{CW}	Chip Select to End of Write	12/15	–	20/22	–	25/40	–	50	–	55	–	65	–	ns
t_{AW}	Address Valid to End of Write	12/15	–	20/22	–	25/40	–	50	–	55	–	65	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12/15	–	20	–	20/25	–	35	–	40	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8/10	–	15/20	–	15/25	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	6/8	–	12/15	–	15/30	–	30	–	30	–	40	ns
t_{OW}	Output Active from End of Write[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns

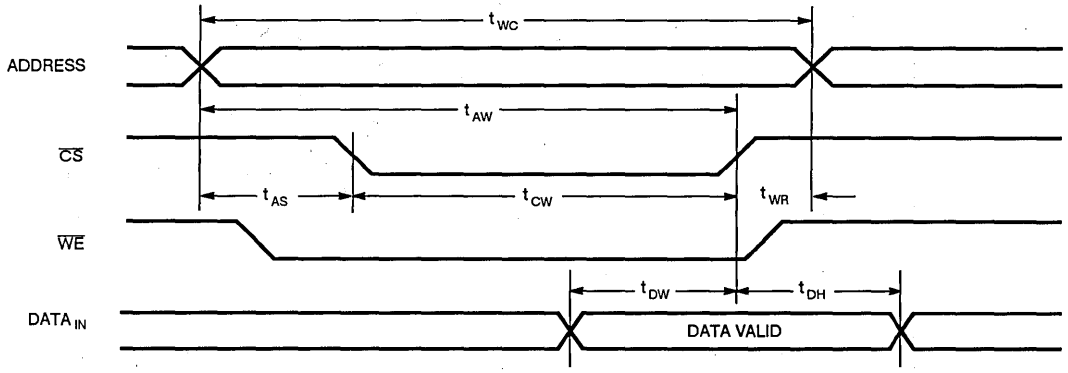
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 4)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

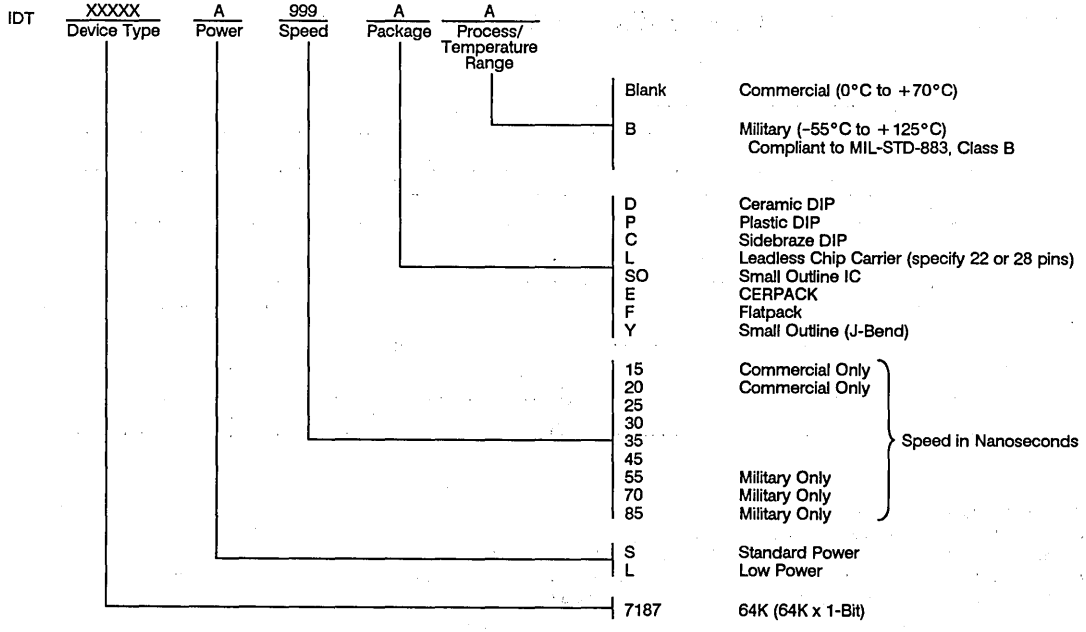
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (256K x 1-BIT)

PRELIMINARY
IDT 71257S
IDT 71257L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55ns (max.)
- Low-power operation
  - IDT71257S
    Active: 400mW (typ.)
    Standby: 400µW (typ.)
  - IDT71257L
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP, 24-pin SOIC, and LCC.
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71257 is a 262,144-bit high-speed static RAM organized as 256K x 1. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

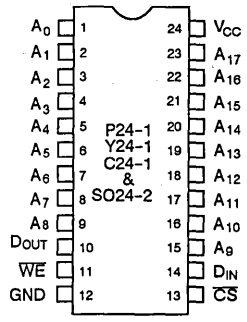
Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT71257 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation off a 2V battery.

All inputs and outputs of the IDT71257 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71257 is packaged in a 24-pin 300 mil DIP, a 24-pin SOIC, and a 28-pin Leadless chip carrier, providing high board-level packing densities.

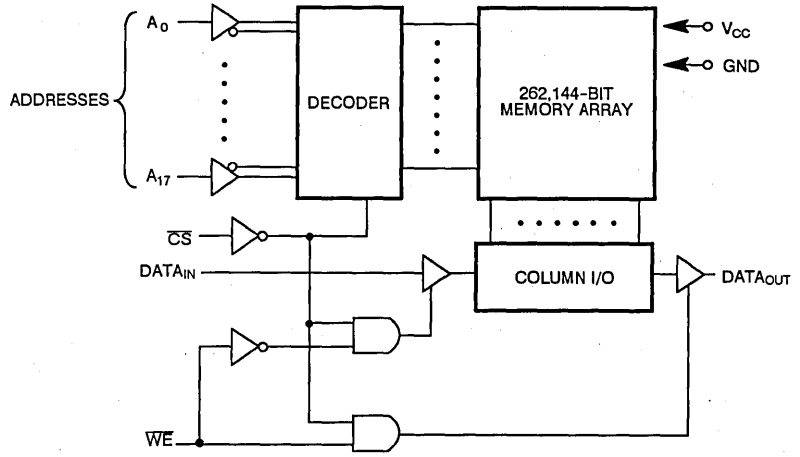
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOIC
TOP VIEW

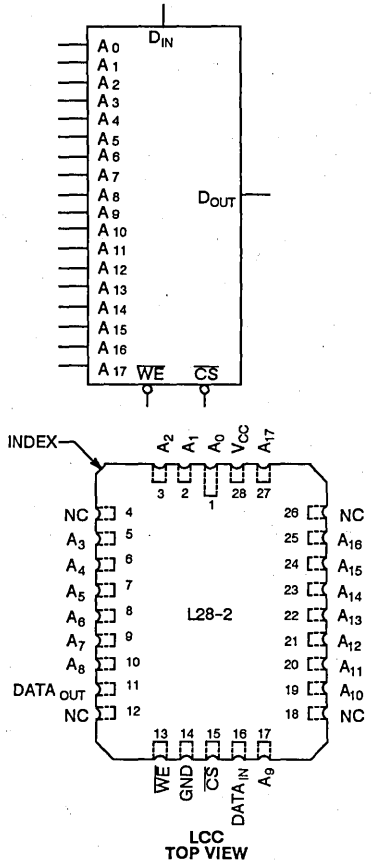
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-1016/1

LOGIC SYMBOL



LCC
TOP VIEW

PIN NAMES

$A_0 - A_{17}$	Addresses
D_{IN}	Data Input
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D_{OUT}	Data Output
GND	Ground
V_{CC}	Power

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71257S MIN.	IDT71257S MAX.	IDT71257L MIN.	IDT71257L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

SYMBOL	PARAMETER	POWER	FUNCTION	71257S20 71257L20		71257S25[4] 71257L25[4]		71257S35 71257L35		71257S45 71257L45		71257S55 71257L55		71257S70 71257L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COML.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	S	READ	70	–	60	70	50	60	50	60	50	60	–	60	mA
			WRITE[2]	120	–	110	120	100	110	100	110	100	110	–	110	
		L	READ	50	–	40	50	30	40	30	40	30	40	–	40	
			WRITE[2]	110	–	100	110	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	S	READ	170	–	160	170	150	160	150	160	150	160	–	160	mA
			WRITE[2]	170	–	160	170	150	160	150	160	150	160	–	160	
		L	READ	150	–	140	150	130	140	130	140	130	140	–	140	
			WRITE[2]	150	–	140	150	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S		35	–	35	35	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[3]	S		30	–	30	35	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Preliminary data for military devices only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS}$	OUTPUT	MODE
X	H	Hi-Z	Standby (I_{SB})
X	V_{HC}	Hi-Z	Standby (I_{SB1})
H	L	D_{OUT}	Read
L	L	Hi-Z	Write

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care

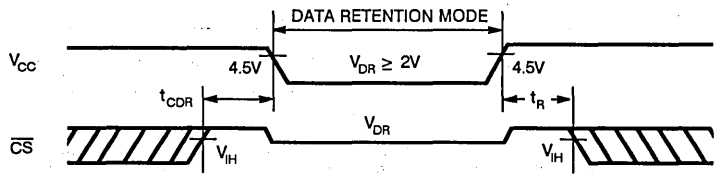
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

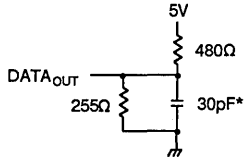


Figure 1. Output Load

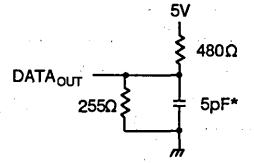


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

*Including scope and jig.

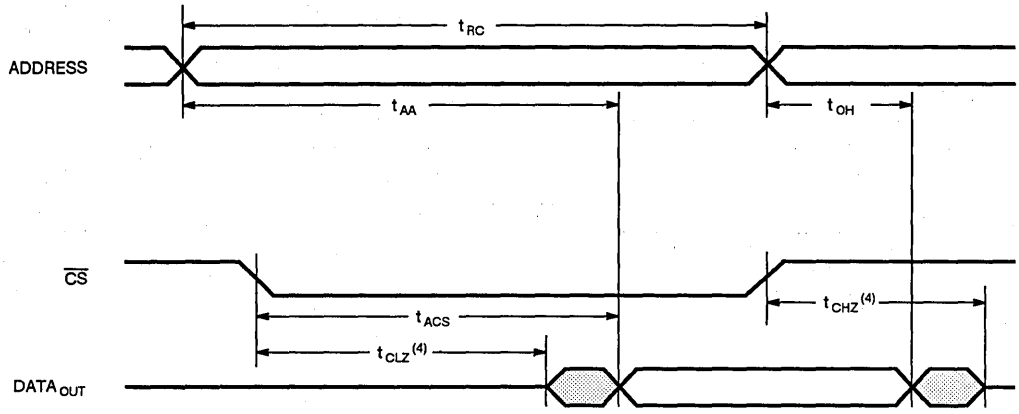
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71257S20[1] 71257L20[1] MIN.	MAX.	71257S25 71257L25 MIN.	MAX.	71257S35 71257L35 MIN.	MAX.	71257S45 71257L45 MIN.	MAX.	71257S55 71257L55 MIN.	MAX.	71257S70[2] 71257L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

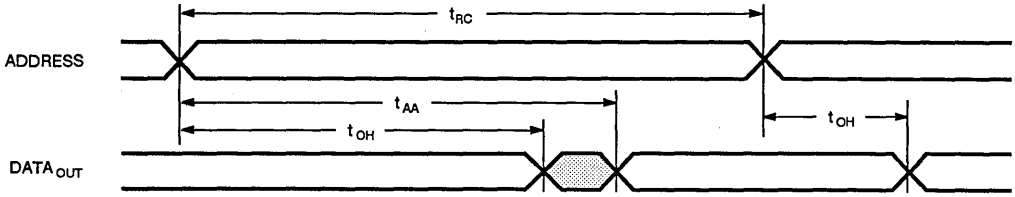
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

4

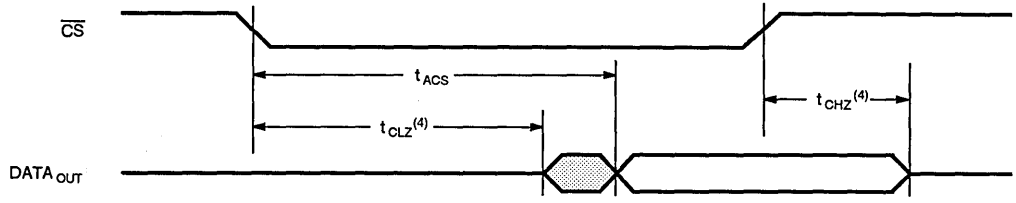
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3]



NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

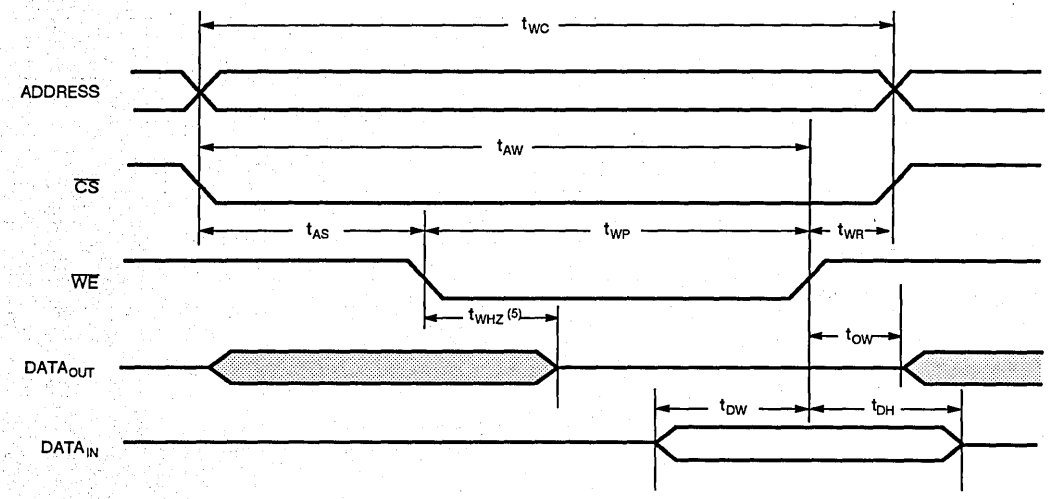
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71257S20[1] 71257L20[1] MIN.	MAX.	71257S25 71257L25 MIN.	MAX.	71257S35 71257L35 MIN.	MAX.	71257S45 71257L45 MIN.	MAX.	71257S55 71257L55 MIN.	MAX.	71257S70[2] 71257L70[2] MIN.	MAX	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z[3]	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

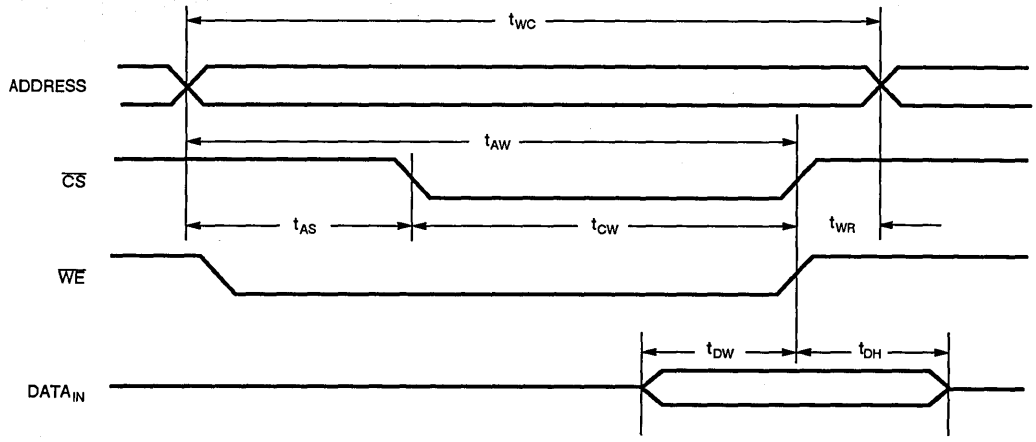
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1 [1, 2, 3] ($\overline{WE}$ CONTROLLED TIMING)



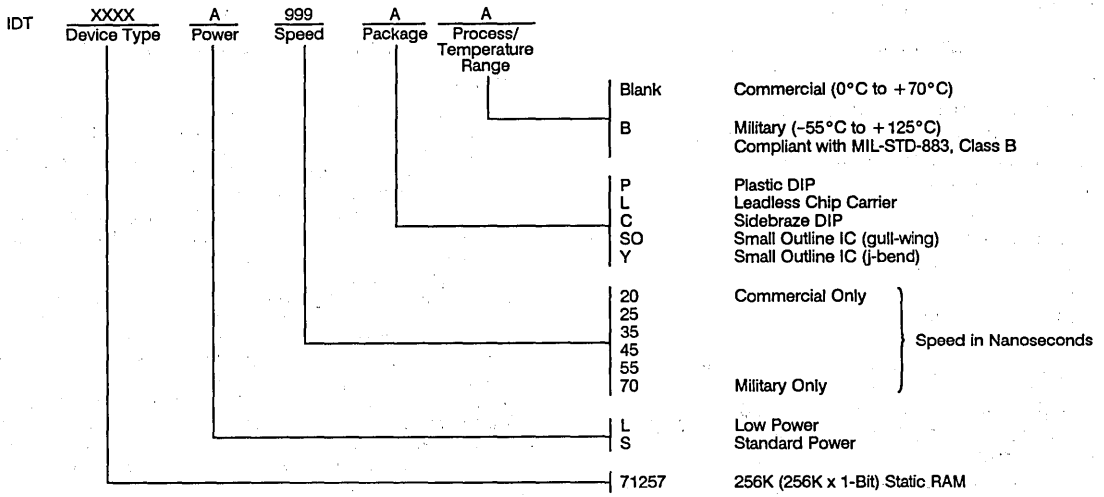
TIMING WAVEFORM OF WRITE CYCLE NO. 2 [1, 2, 3, 4] ($\overline{CS}$ CONTROLLED TIMING)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION



4

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT 6168SA
IDT 6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - IDT6168SA
    Active: 225mW (typ.)
    Standby: 100µW (typ.)
  - IDT6168LA
    Active: 225mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin CERDIP and plastic DIP, 20-pin SOIC, 20-pin Flatpack and CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86705 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

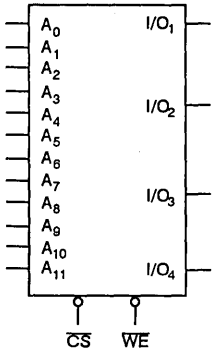
Access times as fast as 12ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

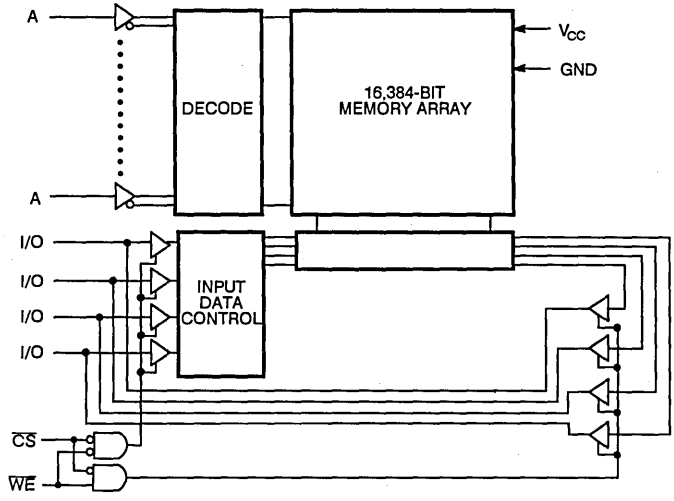
The IDT6168 is packaged in either a space saving 20-pin, 300 mil CERDIP or plastic DIP, 20-pin flatpack or CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



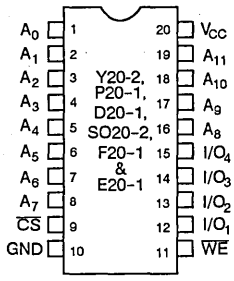
FUNCTIONAL BLOCK DIAGRAM



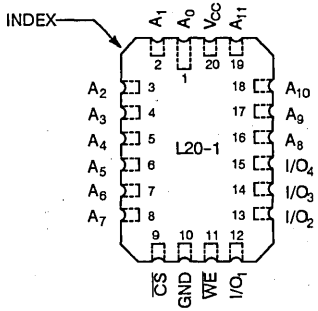
CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-1008/-

PIN CONFIGURATIONS



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A_0–A_{11}	Address Inputs	I/O_1 –I/O_4	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT6168SA MIN.	IDT6168SA TYP.(1)	IDT6168SA MAX.	IDT6168LA MIN.	IDT6168LA TYP.(1)	IDT6168LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	2	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	2	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	6168SA12 COM'L.	6168SA12 MIL.	6168SA15 COM'L.	6168SA15 MIL.	6168SA20 6168LA20 COM'L.	6168SA20 6168LA20 MIL.	6168SA25 6168LA25 COM'L.	6168SA25 6168LA25 MIL.	6168SA35/45(4) 6168LA35/45(4) COM'L.	6168SA35/45(4) 6168LA35/45(4) MIL.	6168SA55 6168LA55 COM'L.	6168SA55 6168LA55 MIL.	6168SA70(2) 6168LA70(2) COM'L.	6168SA70(2) 6168LA70(2) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(3)	SA	110	–	110	120	90	100	90	100	90	100	–	100	–	100	mA
		LA	–	–	–	–	70	80	70	80	70	80	–	80	–	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (3)	SA	165	–	145	165	120	120	110	120	100	110	–	110	–	110	mA
		LA	–	–	–	–	100	110	90	100	80	90/80	–	80	–	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	65	–	55	60	45	45	35	45	30	35	–	35	–	35	mA
		LA	–	–	–	–	30	35	25	30	20	25	–	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	20	–	20	30	20	20	2	10	2	10	–	10	–	10	mA
		LA	–	–	–	–	0.5	5	0.05	0.3	0.05	0.3	–	0.3	–	0.3	

NOTES:

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
4. -55°C to +125°C temperature range only.

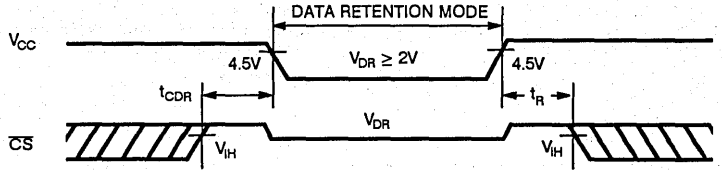
DATA RETENTION CHARACTERISTICS (LA Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT6168LA MIN.	IDT6168LA TYP (1)	IDT6168LA MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	– –	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	– –	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)			ns

NOTES:
1. T_A = +25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

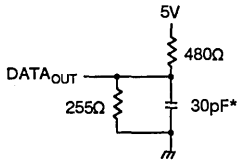


Figure 1. Output Load

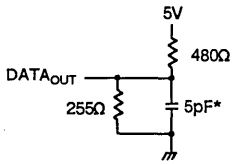


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

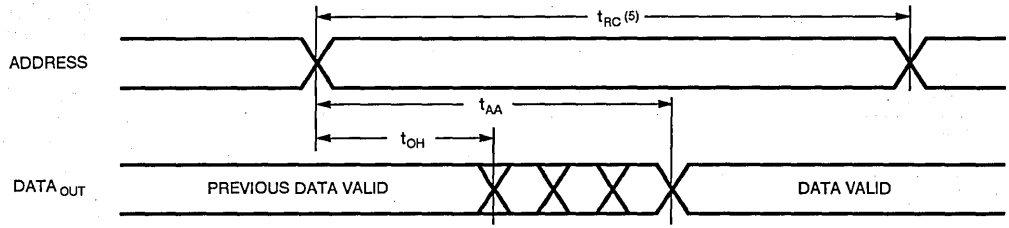
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6168SA12[3] MIN.	6168SA12[3] MAX.	6168SA15 MIN.	6168SA15 MAX.	6168SA20/25 6168LA20/25 MIN.	6168SA20/25 6168LA20/25 MAX.	6168SA35/45[1] 6168LA35/45[1] MIN.	6168SA35/45[1] 6168LA35/45[1] MAX.	6168SA55[1] 6168LA55[1] MIN.	6168SA55[1] 6168LA55[1] MAX.	6168SA70[1] 6168LA70[1] MIN.	6168SA70[1] 6168LA70[1] MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	12	–	15	–	20/25	–	35/45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20/25	–	35/45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	12	–	15	–	20/25	–	35/45	–	55	–	70	ns
t_{OH}	Output Hold from Address Change	3	–	3	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[2]	3	–	3	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[2]	–	7	–	8	–	10	–	15	–	25	–	30	ns
t_{PU}	Chip Select to Power Up Time[2]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[2]	–	12	–	15	–	20/25	–	35/40	–	50	–	60	ns

NOTES:

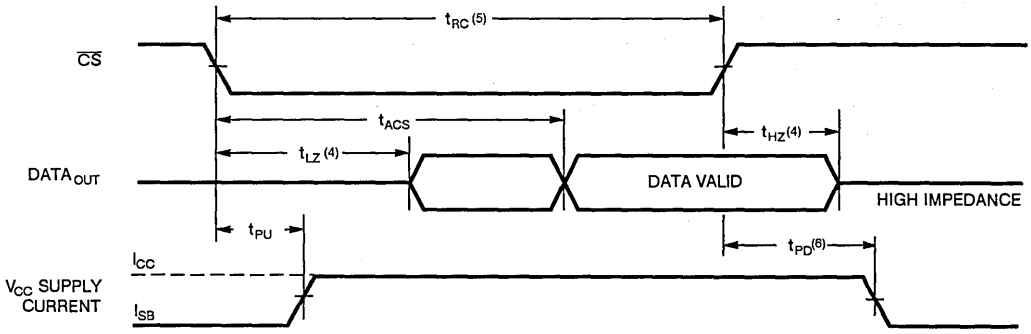
1. -55°C to +25°C temperature range only. Also available 85 and 100ns military devices.
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



4

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



NOTES:

1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is guaranteed and not 100% tested.

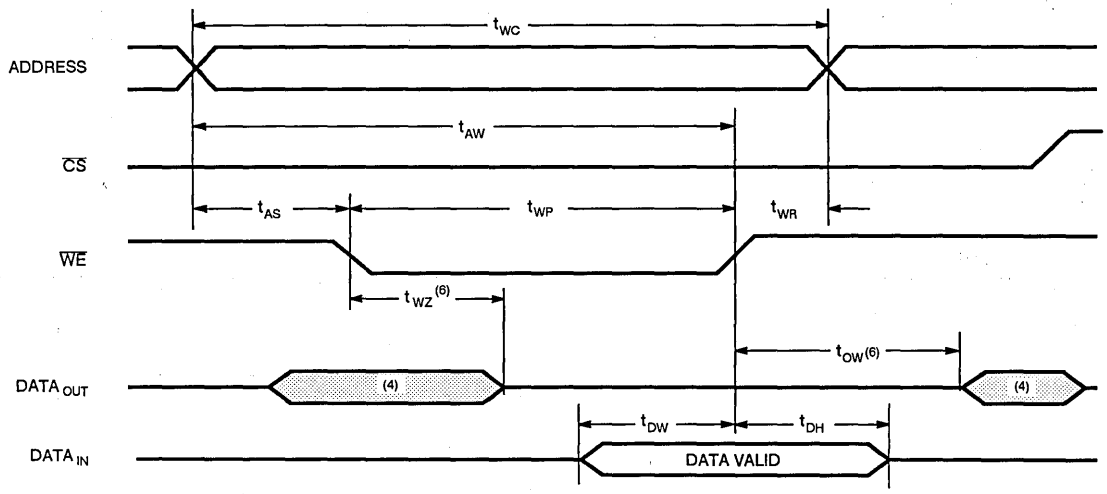
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6168SA12[4] MIN.	6168SA12[4] MAX	6168SA15 MIN.	6168SA15 MAX.	6168SA20/25 6168LA20/25 MIN.	6168SA20/25 6168LA20/25 MAX.	6168SA35/45[1] 6168LA35/45[1] MIN.	6168SA35/45[1] 6168LA35/45[1] MAX.	6168SA55[1] 6168LA55[1] MIN.	6168SA55[1] 6168LA55[1] MAX.	6168SA70[1] 6168LA70[1] MIN.	6168SA70[1] 6168LA70[1] MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	12	–	15	–	20	–	30/40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	20	–	30/40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	12	–	15	–	20	–	30/40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	12	–	15	–	20	–	30/40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	9	–	10	–	15/20	–	20	–	25	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0/3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in HighZ[2]	–	5	–	6	–	7	–	13/20	–	25	–	30	ns
t_{OW}	Output Active from End of Write[2]	0	–	0	–	0	–	0	–	0	–	0	–	ns

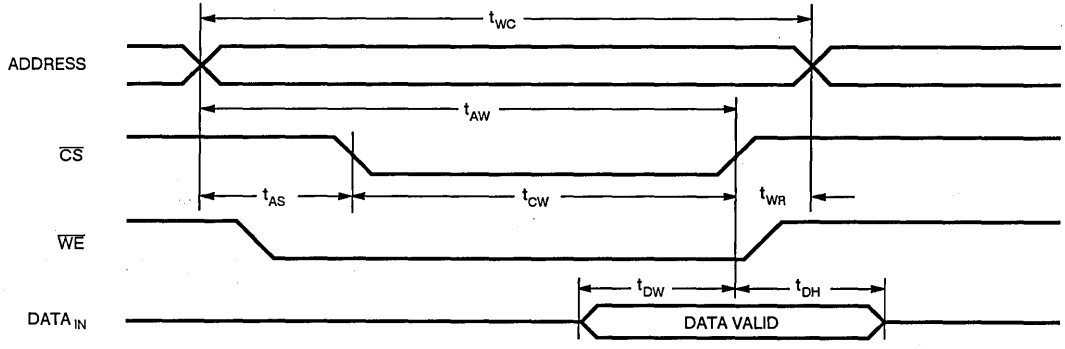
NOTES:

1. -55°C to +125°C temperature range only. Also available 85 and 100ns military devices.
2. This parameter is guaranteed but not tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP} or t_{CW}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

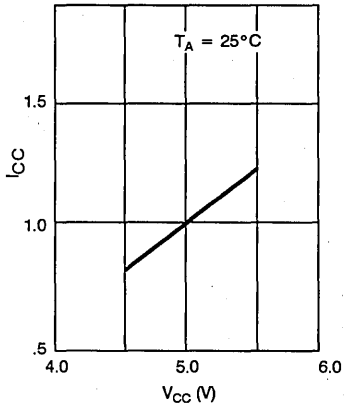
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

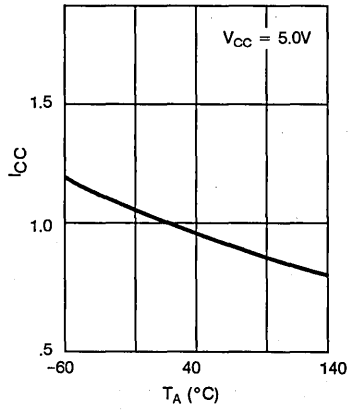
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

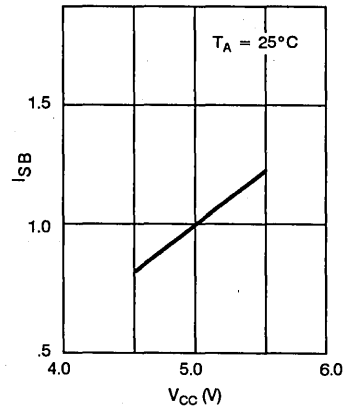
I_{CC} vs. Supply Voltage



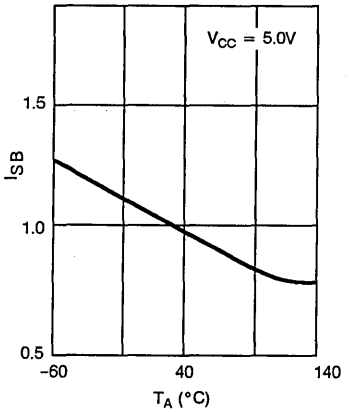
I_{CC} vs. Temperature



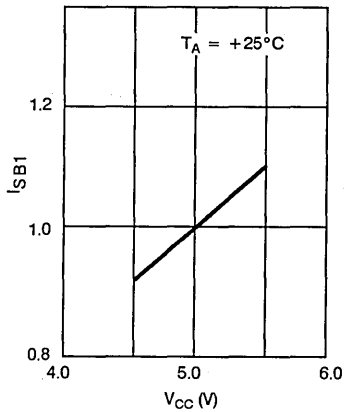
I_{SB} vs. Supply Voltage



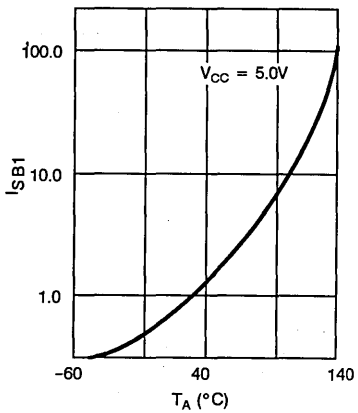
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

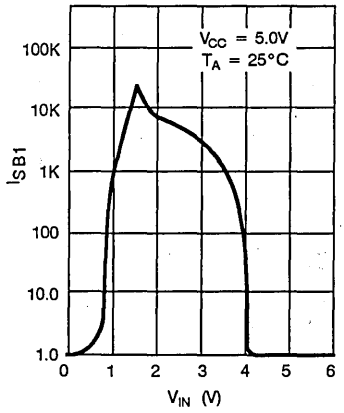


I_{SB1} vs. Temperature

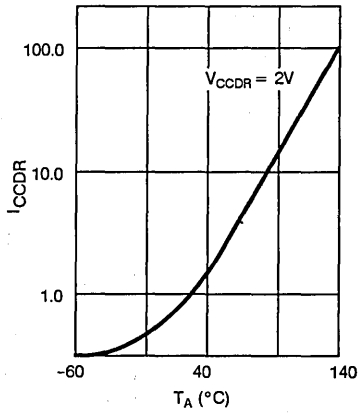


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

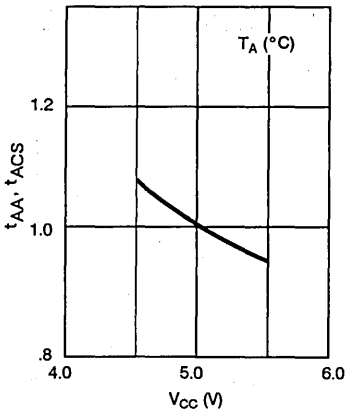
I_{SB1} vs. V_{IN}



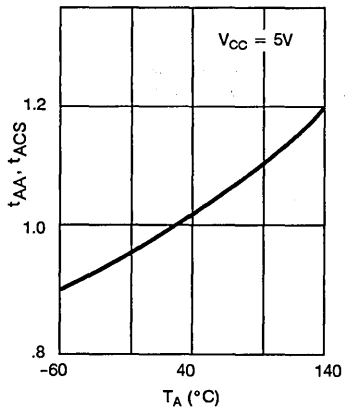
I_{CCDR} vs. Temperature



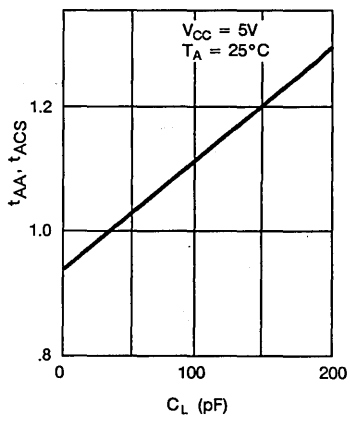
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature

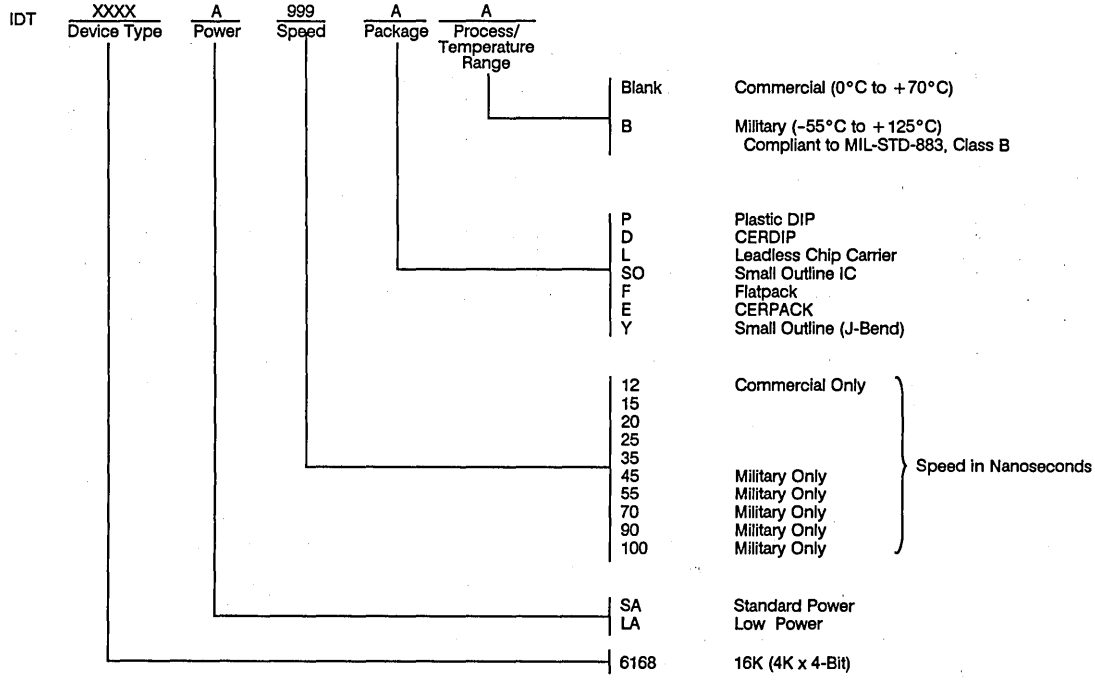


t_{AA}, t_{ACS} vs. Output Loading



4

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT)

Separate Data Inputs and Outputs

IDT 71681SA/LA
IDT 71682SA/LA

4

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682/SA/LA: high impedance outputs during write mode
- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 12/15/20/25/35/45ns (max.)
- Low power consumption
  - IDT71681/2SA
    Active: 225mW (typ.)
    Standby: 100µw (typ.)
  - IDT71681/2LA
    Active: 225mW (typ.)
    Standby: 10µw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 24-pin 300-mil CERDIP and plastic DIP, 24-pin Flatpack and CERPACK, 24-pin SOIC (gull-wing or J-bend) and 28-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

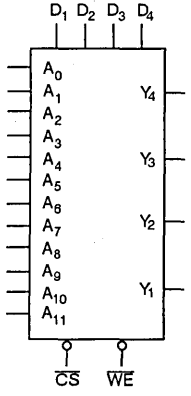
Access times as fast as 12ns are available, with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

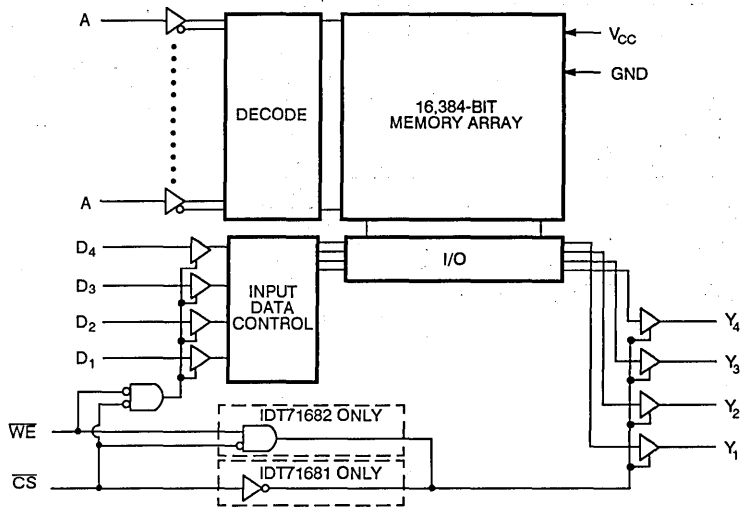
The IDT71681/IDT71682 are packaged in either space-saving 24-pin 300 mil DIPs, SOICs, Flatpacks, CERPACKS, or 28-pin leadless chip carriers, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL

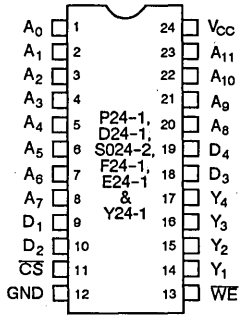


FUNCTIONAL BLOCK DIAGRAM

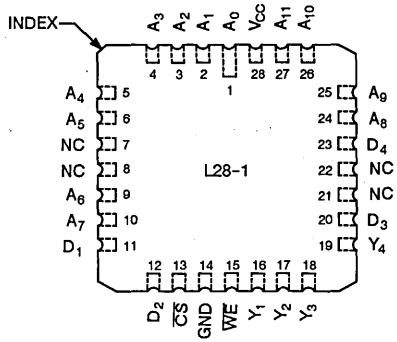


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A_0-A_{11}	Address Inputs	D_1 - D_4	$DATA_{IN}$
$\overline{CS}$	Chip Select	Y_1 - Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71681SA IDT71682SA MIN.	TYP.(1)	MAX.	IDT71681LA IDT71682LA MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

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DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	71681x12 71682x12 COM'L.	MIL.	71681x15 71682x15 COM'L.	MIL.	71681x20 71682x20 COM'L.	MIL.	71681x25 71682x25 COM'L.	MIL.	71681x35 71682x35 COM'L.	MIL.	71681x45 71682x45 COM'L.	MIL.	71681x55(6) 71682x55(6) COM'L.	MIL.	71681x70(2,6) 71682x70(2,6) COM'L.	MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	110	–	110	120	90	100	90	100	90	100	90	100	–	100	–	100	mA
		LA	–	–	–	–	70	80	70	80	70	80	70	80	–	80	–	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	165	–	145	165	120	120	110	120	100	110	100	110	–	110	–	110	mA
		LA	–	–	–	–	100	110	90	100	80	90	70	80	–	80	–	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	SA	65	–	55	65	45	55	35	45	30	35	30	35	–	35	–	35	mA
		LA	–	–	–	–	30	35	25	30	20	25	20	25	–	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	20	–	20	30	20	30	2	10	2	10	2	10	–	10	–	10	mA
		LA	–	–	–	–	0.5	5	0.05	0.3	0.05	0.3	0.05	0.3	–	0.3	–	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. "x" in part numbers indicates power rating (SA or LA).
5. 0°C to +70°C temperature range only.
6. -55°C to +125°C temperature range only.

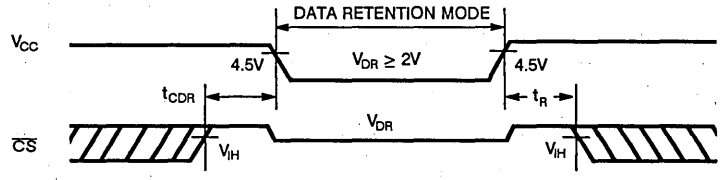
DATA RETENTION CHARACTERISTICS

(L Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT71681LA - IDT71682LA MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	– –	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	– –	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(5)	Operation Recovery Time			t_{RC}(4)	–	–	ns

NOTES:
1. T_A = +25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

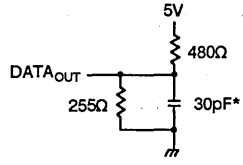


Figure 1. Output Load

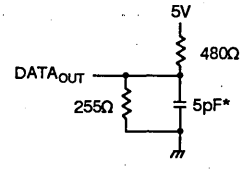


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

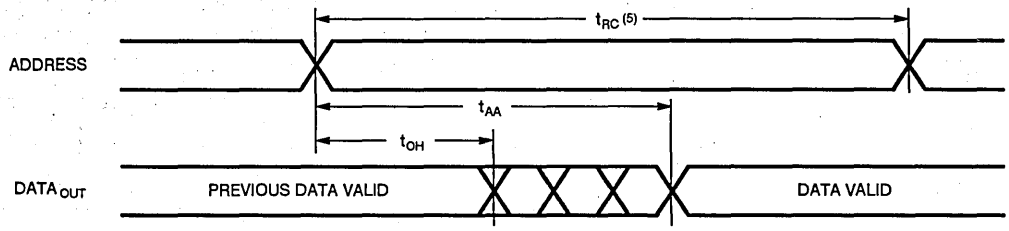
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS[4] (V_{CC} = 5V ±10%, All Temperature Ranges)

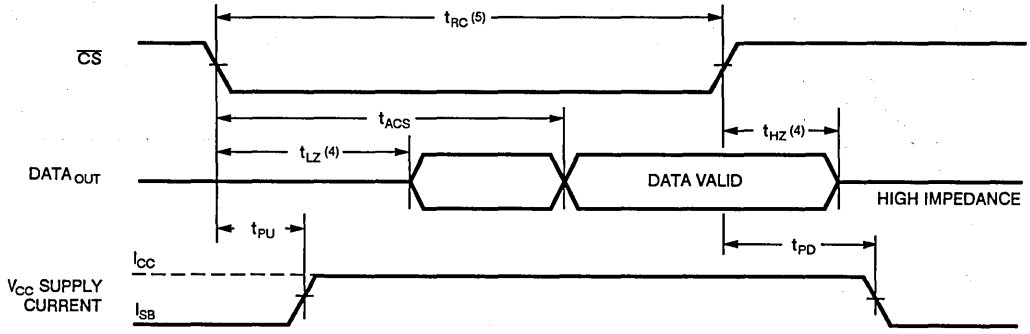
SYMBOL	PARAMETER	71681x12[1] 71682x12[1] MIN.	MAX.	71681x15 71682x15 MIN.	MAX.	71681x20 71682x20 MIN.	MAX.	71681x25 71682x25 MIN.	MAX.	71681x35 71682x35 MIN.	MAX.	71681x45 71682x45 MIN.	MAX.	71681x55[2] 71682x55[2] MIN.	MAX.	71681x70[2] 71682x70[2] MIN.	MAX.	UNIT
READ CYCLE																		
t_{RC}	Read Cycle Time	12	–	15	–	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	12	–	15	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Select to Output in Low Z[3]	3	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	7	–	7	–	9	–	10	–	15	–	20	–	25	–	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	10	–	15	–	20	–	25	–	35	–	40	–	50	–	60	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers represents SA or LA.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



NOTES:

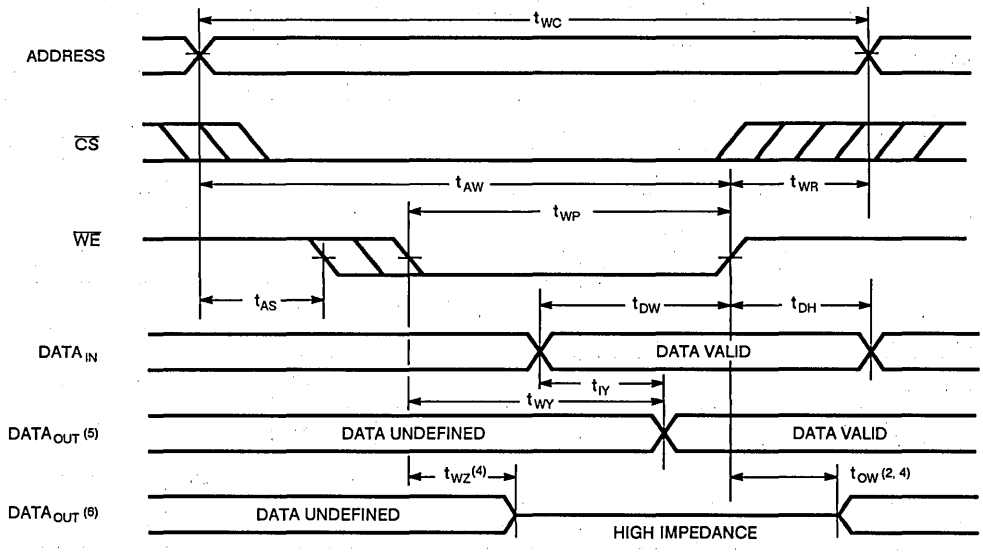
1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS[4] (V_{CC} = 5V ±10%, All Temperature Ranges)

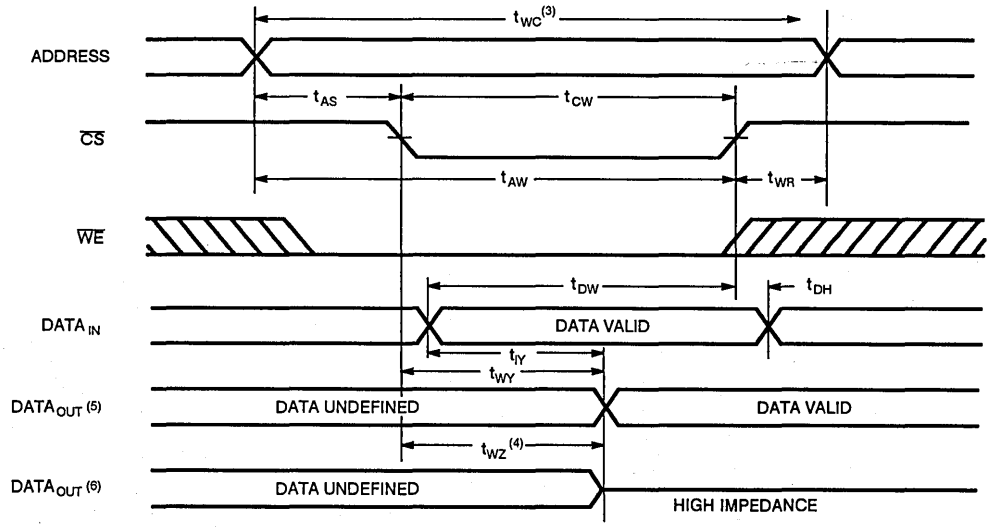
SYMBOL	PARAMETER	71681x12[1] 71682x12[1] MIN.	MAX.	71681x15 71682x15 MIN.	MAX.	71681x20 71682x20 MIN.	MAX.	71681x25 71682x25 MIN.	MAX.	71681x35 71682x35 MIN.	MAX.	71681x45 71682x45 MIN.	MAX.	71681x55[2] 71682x55[2] MIN.	MAX.	71681x70[2] 71682x70[2] MIN.	MAX.	UNIT
WRITE CYCLE																		
t_{WC}	Write Cycle Time	12	–	15	–	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	10	–	15	–	20	–	20	–	25	–	35	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	10	–	15	–	20	–	20	–	25	–	35	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	10	–	15	–	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	9	–	10	–	10	–	15	–	20	–	20	–	25	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	3	–	3	–	3	–	3	–	ns
t_{IY}	Data Valid to Output Valid (71681 only)[3]	–	12	–	15	–	20	–	25	–	30	–	35	–	35	–	40	ns
t_{WY}	Write Enable to Output Valid (71681 only)[3]	–	12	–	15	–	20	–	25	–	30	–	35	–	35	–	40	ns
t_{WZ}	Write Enable to Output in HIGH Z (71682 only)[3]	–	5	–	6	–	7	–	7	–	13	–	20	–	25	–	30	ns
t_{OW}	Output Active from End of Write (71682 only)[3]	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers represents SA or LA.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.
5. For IDT71681 only.
6. For IDT71682 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write (1)	L	L	D_{IN}	Active
Write (2)	L	L	High Z	Active

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

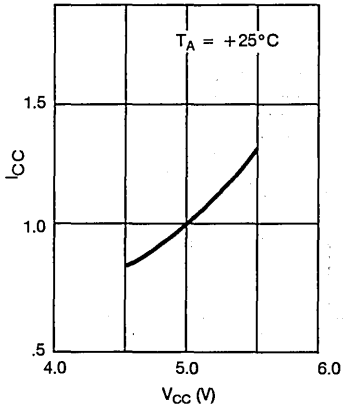
SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

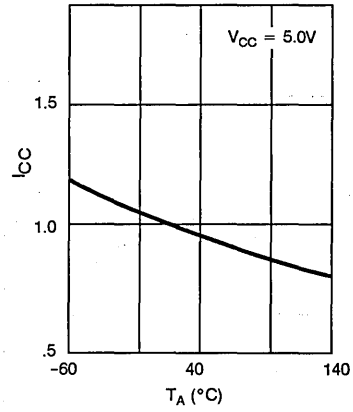
4

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

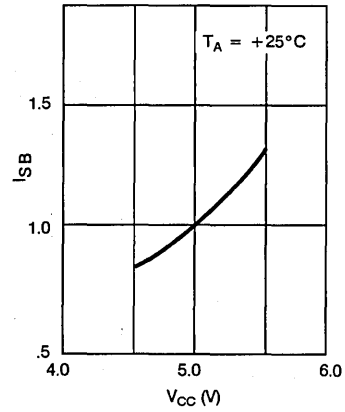
I_{CC} vs. Supply Voltage



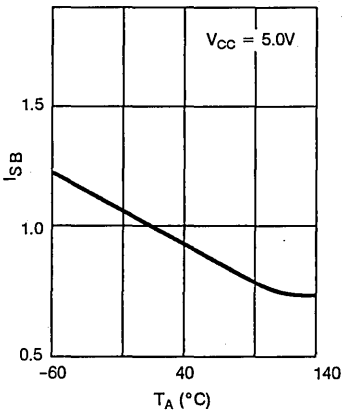
I_{CC} vs. Temperature



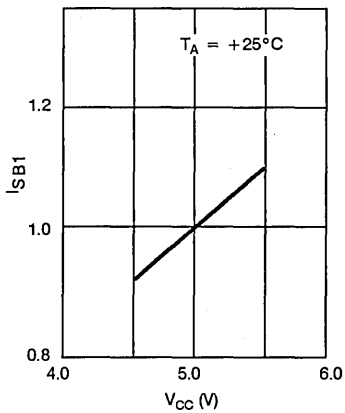
I_{SB} vs. Supply Voltage



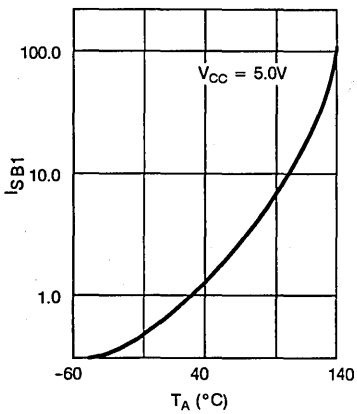
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

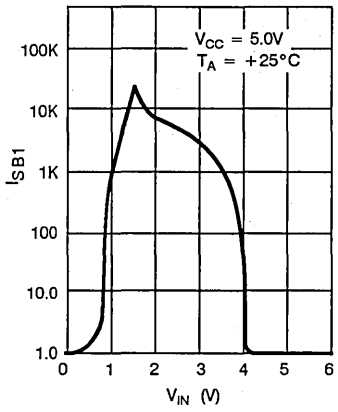


I_{SB1} vs. Temperature

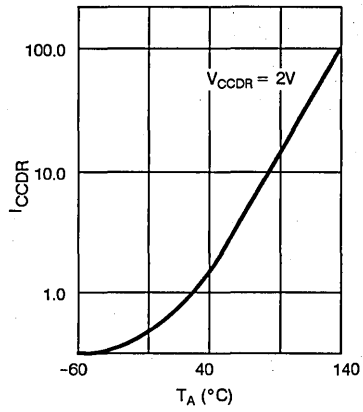


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

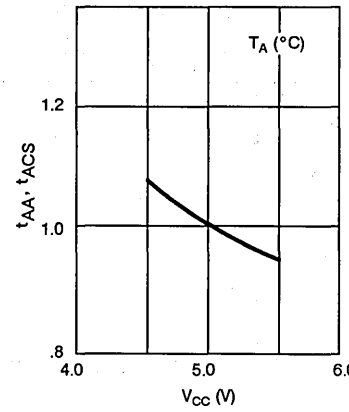
I_{SB1} vs. V_{IN}



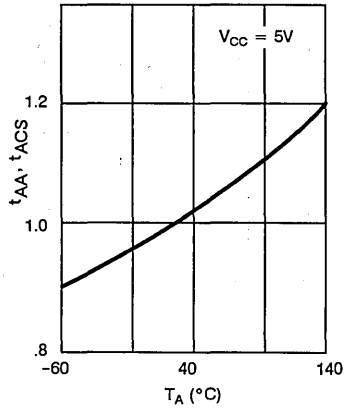
I_{CCDR} vs. Temperature



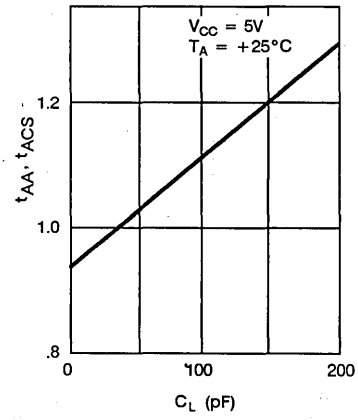
t_{AA}, t_{ACS} vs. Supply Voltage



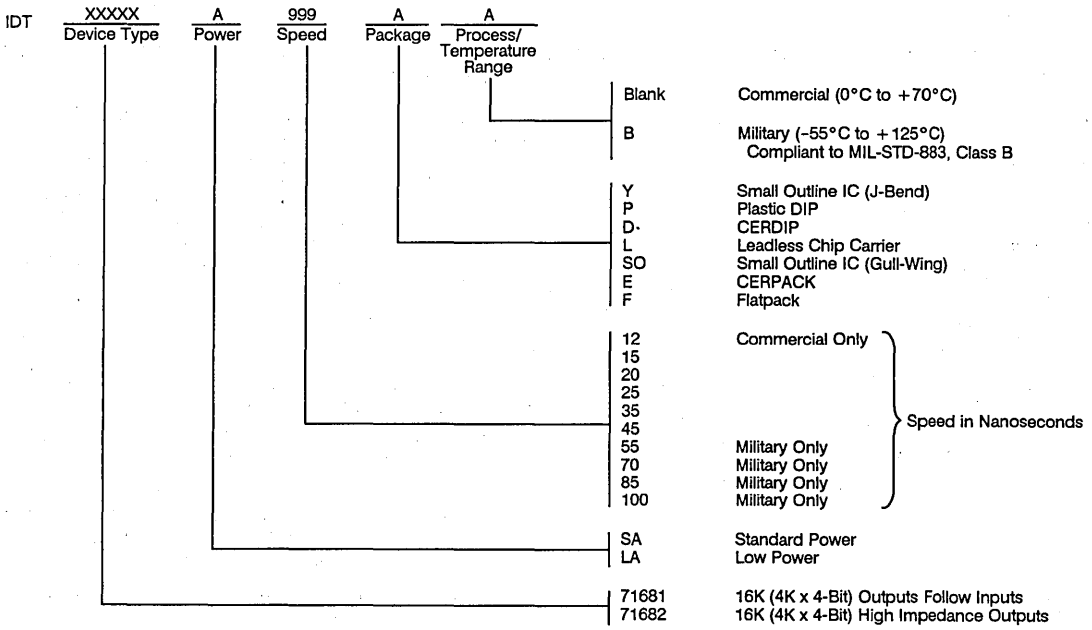
t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



ORDERING INFORMATION



4

Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM Cache TAG 16K(4K x 4-BIT)

ADVANCE INFORMATION
IDT 6177

FEATURES:

- High-speed address to Match comparison time
  - Military: 15ns
  - Commercial: 12ns
- High-speed address access time
  - Military: 15ns
  - Commercial: 12ns
- Low-power operation
  - IDT6177S
  - Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Open drain MATCH output
- Standard 22 pin plastic or ceramic DIP, 24 pin SOJ
- Static operation: no clocks or refresh required
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6177 is a high-speed cache address comparator subsystem consisting or a 16384-bit static RAM organized as 4K x 4. Cycle Time and Compare Access Time are equal. The IDT6177 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins or several IDT6177's can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor thus eliminating logic delays and increasing system throughput.

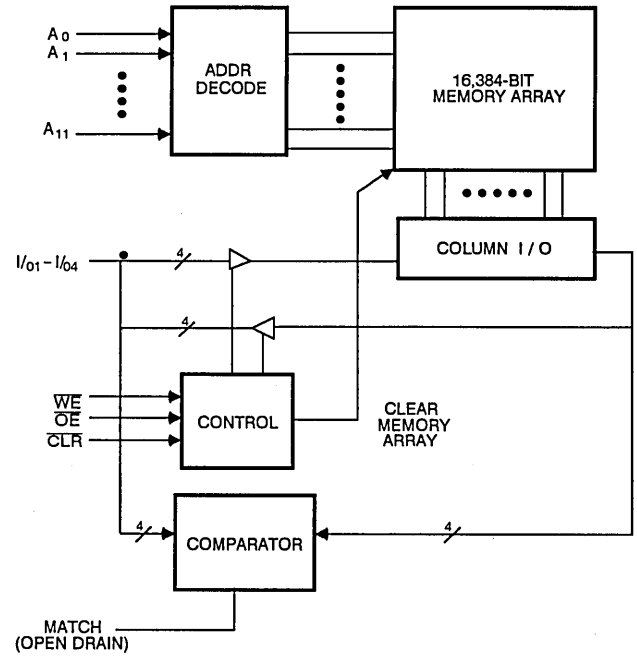
The IDT6177 is fabricated using IDT's high-performance, high reliability technology - CEMOS™ address to compare and data to compare access times as fast as 12ns.

All inputs and outputs of the IDT6177 are TTL-compatible except MATCH, which is open drain. The device operates from a single 5V supply and fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6177 is packaged in either a 22 pin, 300 mil plastic or ceramic DIP package, and 24 pin SOJ.

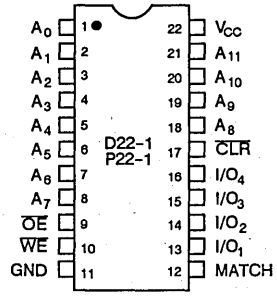
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

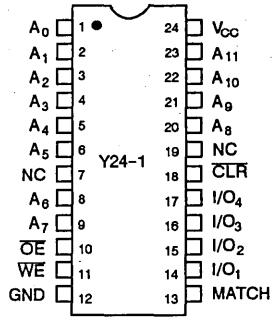


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



DIP
TOP VIEW

4

TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	FUNCTION
H	H	H	Valid	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

X = Don't Care

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT) CACHE-TAG RAM

PRELIMINARY
IDT 6178S

FEATURES:

- High-speed Address to Match comparison time
  - Military: 15ns
  - Commercial: 12ns
- High-speed address access time
  - Military: 15ns
  - Commercial: 12ns
- Low-power operation
  - IDT6178S
    Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Input and output TTL compatible
- Standard 22 pin plastic or ceramic DIP, 24 pin SOJ
- Static operation: no clocks or refresh required
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6178 is a high-speed cache address comparator subsystem consisting of a 16384-bit static RAM organized as 4K x 4. Cycle Time and Compare Access Time are equal. The IDT6178 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins of several IDT6178's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

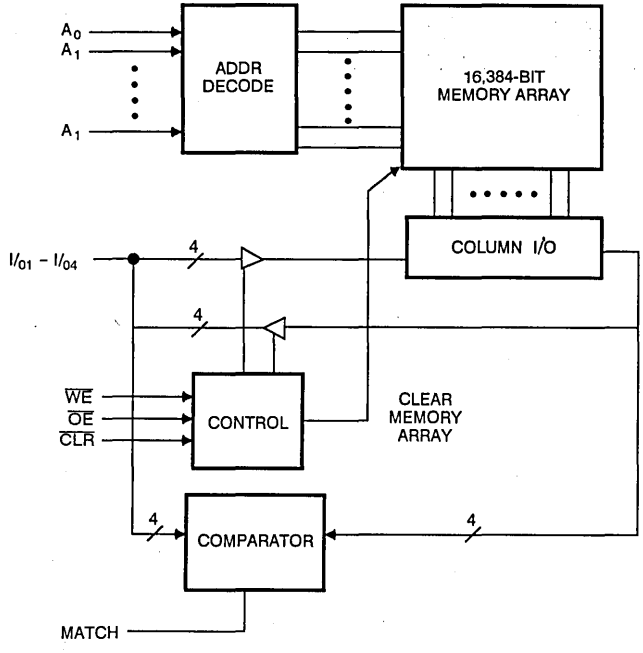
The IDT6178 is fabricated using IDT's high-performance, high-reliability technology — CEMOS™. Address to compare and Data to compare access times as fast as 12ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6178 is packaged in either a 22 pin, 300mil plastic or ceramic DIP package, and 24 pin SOJ.

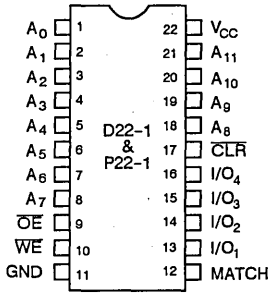
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

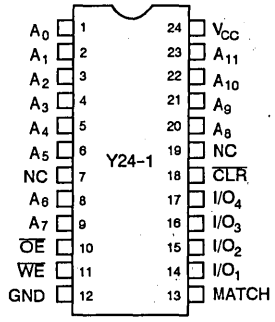


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



SOJ
TOP VIEW

4

PIN NAMES

$A_0 - A_{11}$	Address	$\overline{WE}$	Write Enable
$I/O_1 - I/O_4$	Data Input/Output	$\overline{OE}$	Output Enable
MATCH	Match	$\overline{CLR}$	Power
V_{CC}	Power	GND	Ground

TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

X = DON'T CARE

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 2 & 3
Output Load for Match Cycle	See Figure 1

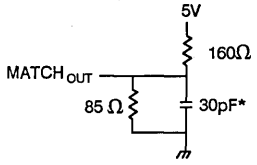


Figure 1

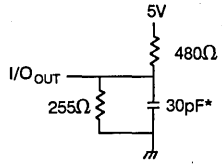


Figure 2

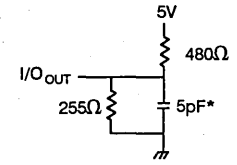


Figure 3
(for t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6178S MIN.	IDT6178S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA (I/O_1 - I/O_4)	–	0.4	V
		I_{OL} = 10mA (I/O_1 - I/O_4)	–	0.5	V
		I_{OL} = 24mA (Match)	–	0.4	V
		I_{OL} = 30mA (Match)	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA (I/O_1 - I/O_4)	2.4	–	V
		I_{OH} = -12mA (Match)	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER		IDT6178S12 MAX.	IDT6178S15 MAX.	IDT6178S20 MAX.	UNIT
I_{CC1}	Operating Power Supply Current Outputs Open V_{CC} = Max., f = 0	MIL.	110	110	110	mA
		COM'L.	90	90	90	
I_{CC2}	Dynamic Operating Current Outputs Open V_{CC} = Max., f = f_{MAX}	MIL.	180	160	160	
		COM'L.	160	140	140	

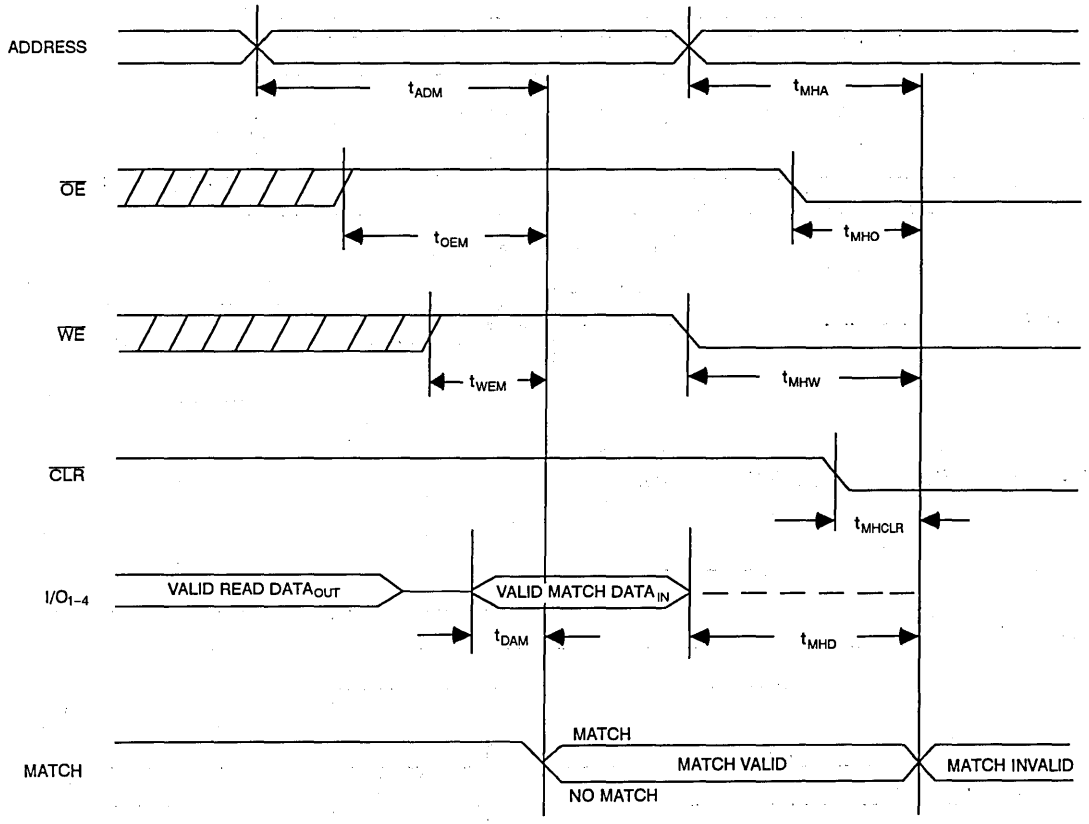
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT6178S12 [1] MIN.	IDT6178S12 [1] MAX.	IDT6178S15 MIN.	IDT6178S15 MAX.	IDT6178S20 MIN.	IDT6178S20 MAX.	UNIT
MATCH CYCLE								
t_{ADM}	Address to Match Valid	–	12	–	15	–	20	ns
t_{DAM}	Data Input to Match Valid	–	11	–	13	–	15	ns
t_{MHO}	Match Valid Hold From $\overline{OE}$	0	–	0	–	0	–	ns
t_{OEM}	$\overline{OE}$ High to Match Valid	–	12	–	15	–	20	ns
t_{MHW}	Match Valid Hold From $\overline{WE}$	0	–	0	–	0	–	ns
t_{WEM}	$\overline{WE}$ High to Match Valid	–	12	–	15	–	20	ns
t_{MHCLR}	Match Valid Hold From $\overline{CLR}$	0	–	0	–	0	–	ns
t_{MHA}	Match Valid Hold From Address	3	–	3	–	3	–	ns
t_{MHD}	Match Valid Hold From Data	3	–	3	–	3	–	ns

NOTE:
1. 0°C to +70°C temperature range only.

4

TIMING WAVEFORM OF MATCH CYCLE

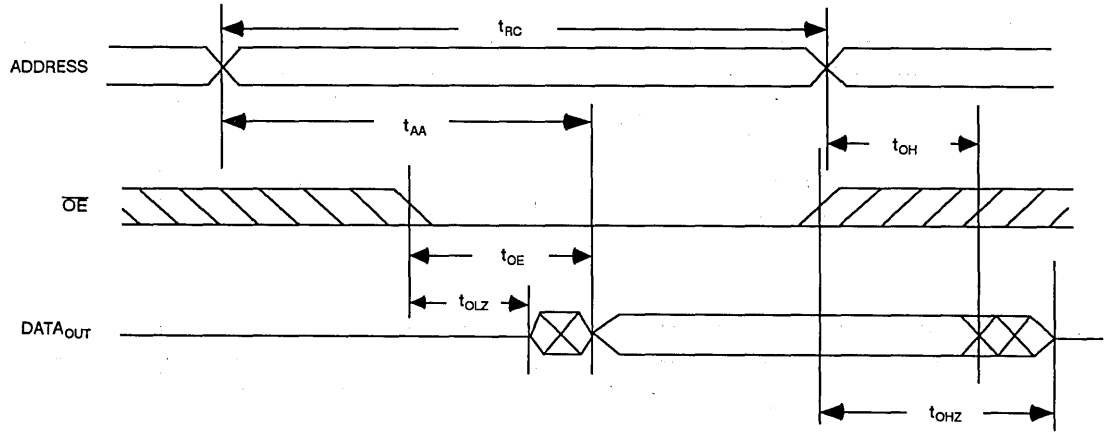


AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

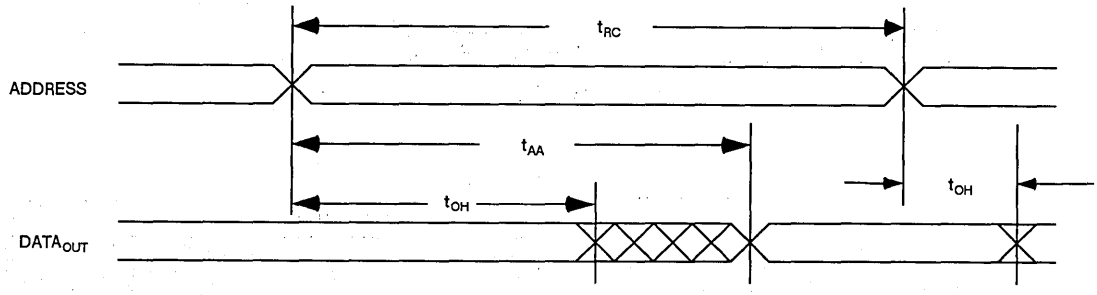
SYMBOL	PARAMETER	IDT6178S12 [3] MIN.	IDT6178S12 [3] MAX.	IDT6178S15 MIN.	IDT6178S15 MAX.	IDT6178S20 MIN.	IDT6178S20 MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	12	–	15	–	20	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20	ns
t_{OE}	Output Enable Access Time	–	8	–	10	–	15	ns
t_{OH}	Output Hold From Address Change	3	–	3	–	3	–	ns
t_{OLZ}	Output Low Z Time[1, 2]	2	–	2	–	2	–	ns
t_{OHZ}	Output High Z Time[1, 2]	–	7	–	9	–	12	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 & 2).
2. This parameter is guaranteed but not tested.
3. 0 - 70°C only.

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2

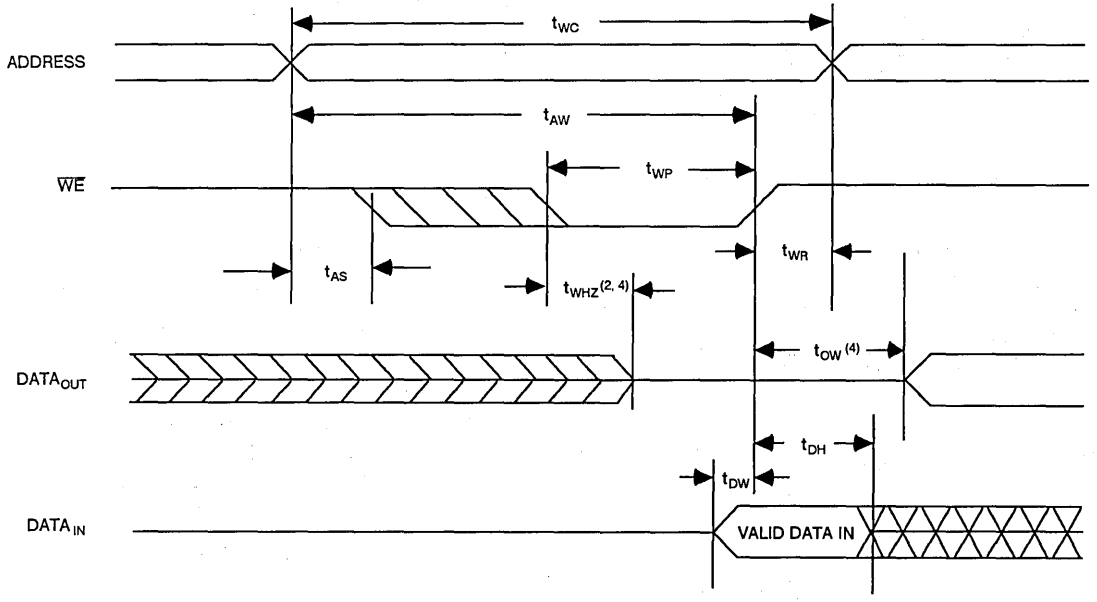


AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT6178S12 [3] MIN.	MAX.	IDT6178S15 MIN.	MAX.	IDT6178S20 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	12	–	15	–	20	–	ns
t_{AW}	Address Valid to End of Write	10	–	12	–	14	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	10	–	12	–	14	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	10	–	12	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z [1, 2]	–	6	–	7	–	9	ns
t_{OW}	Output Active From End of Write [1, 2]	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance with load (Figures 1 & 2).
2. This parameter guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE [1, 3]



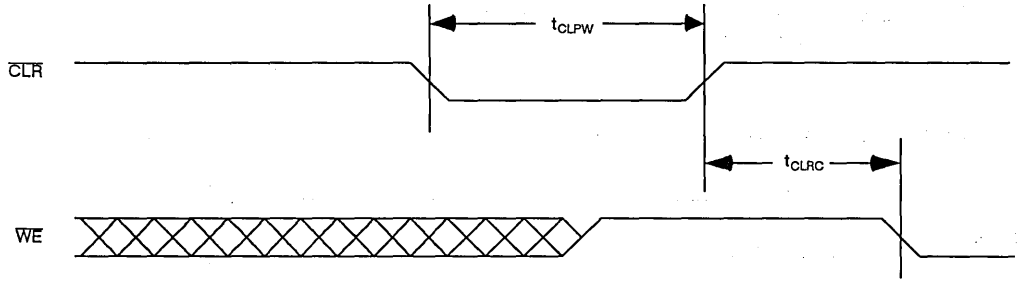
NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. $\overline{OE}$ is continuously high or low. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

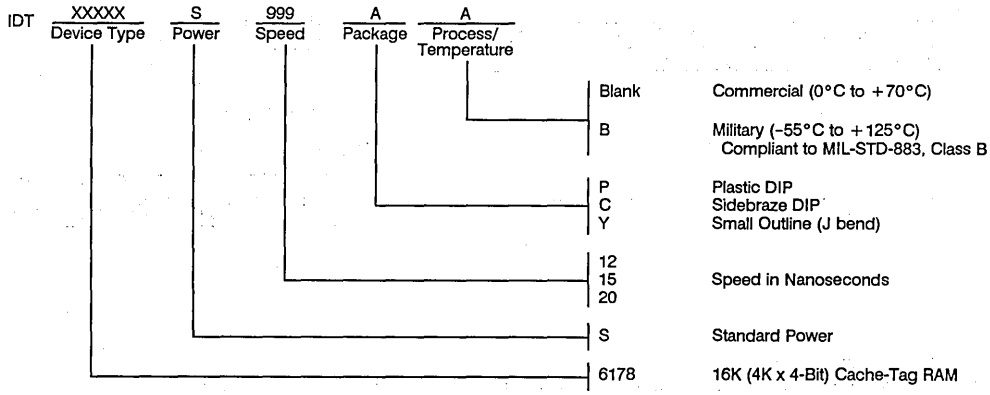
SYMBOL	PARAMETER	IDT6178S12 (1) MIN.	MAX.	IDT6178S15 MIN.	MAX.	IDT6178S20 MIN.	MAX.	UNIT
CLEAR CYCLE								
t_{CLPW}	$\overline{CLR}$ Pulse Width (2)	25	–	30	–	40	–	ns
t_{CLRC}	$\overline{CLR}$ High to $\overline{WE}$ Low	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Recommended duty cycle of 10% maximum.

TIMING WAVEFORM OF CLEAR CYCLE



ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM WITH OUTPUT ENABLE 16K (4K x 4-BIT)

PRELIMINARY
IDT61970S
IDT61970L

FEATURES:

- High Speed (equal access and cycle times)
  - Military 20/25/35/45/55
  - Commercial 12/15/20/25/35/45
- Low power consumption
  - IDT61970S
    Active: 300mW (typ)
    Standby: 100µW (typ)
  - IDT61970L
    Active: 300mW (typ)
    Standby: 10µW (typ)
- Battery backup operation - 2V data retention (IDT61970L only)
- Available in 22-pin ceramic or plastic DIP and 24-pin SOJ
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Produced with advanced CEMOS™ high-performance technology
- Separate Output Enable control
- Military product compliant to MIL-STD-883

DESCRIPTION:

The IDT61970 is a 16,384-bit high speed static RAM organized as 4096 x 4 bits. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art techology, combined with innovative circuit design techniques, provide a cost effective approach for memory intensive applications.

The IDT61970 features two memory control functions: chip select ($\overline{CS}$) and output enable ($\overline{OE}$). These two functions greatly enhance the IDT61970's overall flexibility in high-speed memory applications. This feature makes the IDT61970 ideal for use in cache memory applications.

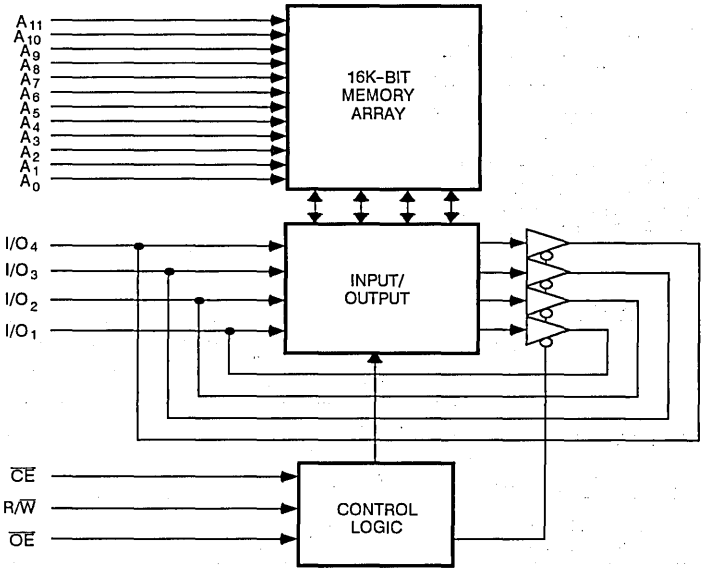
Access times as fast as 12ns are available, with typical power consumption of only 300mW. The IDT61970 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capibility significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power (L) version also offers a battery backup data retention capibility where the circuit typically consumes only 10µW when opperating from a 2 volt battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61970 is packaged in either a space saving 22-pin, 300-mil ceramic or plastic DIP, or a 24-pin SOJ, providing high board level packing densities.

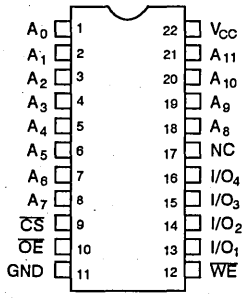
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliabilty.

FUNCTIONAL BLOCK DIAGRAM



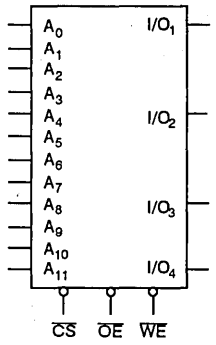
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW

LOGIC DIAGRAM



PIN NAMES

A_0– A_{11}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_4	Data Input/Output	$\overline{OE}$	Output Enable
V_{CC}	Power	$\overline{CS}$	Chip Select
GND	Ground	NC	No Connection

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		IDT61970S MIN.	IDT61970S MAX.	IDT61970L MIN.	IDT61970L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	2	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} Max. $\overline{CS}$ = V_{IH}, V_{CC} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	2	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA V_{CC} = Min.		–	0.5	–	0.5	V
		I_{OL} = 8mA V_{CC} = Min.		–	0.4	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS [1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	61970SA12		61970SA15		61970SA20 61970LA20		61970SA25 61970LA25		61970SA35/45[4] 61970LA35/45[4]		61970SA55 61970LA55		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[3]	SA	110	–	110	120	90	100	90	100	90	100	–	100	mA
		LA	–	–	–	–	70	80	70	80	70	80	–	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} [3]	SA	165	–	145	165	120	120	110	120	100	110	–	110	mA
		LA	–	–	–	–	100	110	90	100	80	90/80	–	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	65	–	55	60	45	45	35	45	30	35	–	35	mA
		LA	–	–	–	–	30	35	25	30	20	25	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[3]	SA	20	–	20	30	20	20	2	10	2	10	–	10	mA
		LA	–	–	–	–	0.5	5	0.05	0.3	0.05	0.3	–	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (All inputs except Chip Select cycling at f = $1/t_{RC}$). f = 0 means no address or control lines change.
4. -55°C to +125°C temperature range only.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

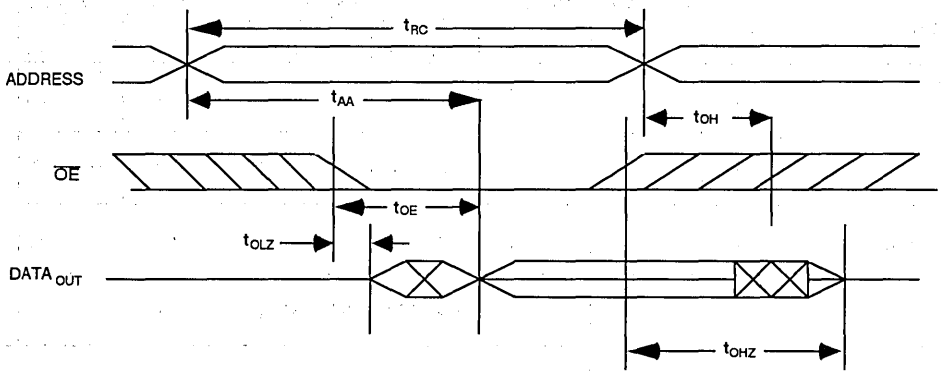
NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

AC ELECTRICAL CHARACTERISTICS

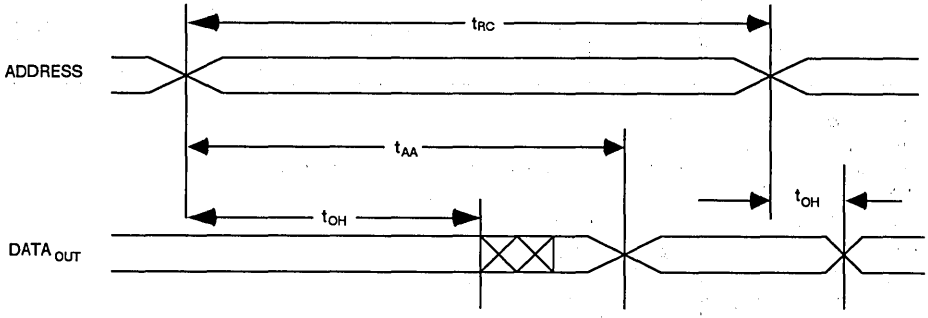
SYMBOL	PARAMETER	12ns		15ns		20/25ns		35/45ns		55ns		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	12	–	15	–	20/25	–	35/45	–	55	–	ns
t_{AA}	Address Access Time	–	12	–	15	–	20/25	–	35/45	–	55	ns
t_{OE}	Output Enable Access Time	–	8	–	10		15	–	15	–	20	ns
t_{OLZ}	Output Low Z Time[1, 2]	2	–	2	–	2	–	2	–	2	–	ns
t_{OHZ}	Output High Z Time[1, 2]	–	7	–	9	–	12	–	15	–	15	ns
t_{OH}	Output Hold from Address Change	3	–	3	–	3	–	3	–	3	–	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load.
2. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NUMBER 1



TIMING WAVEFORM OF READ CYCLE NUMBER 2



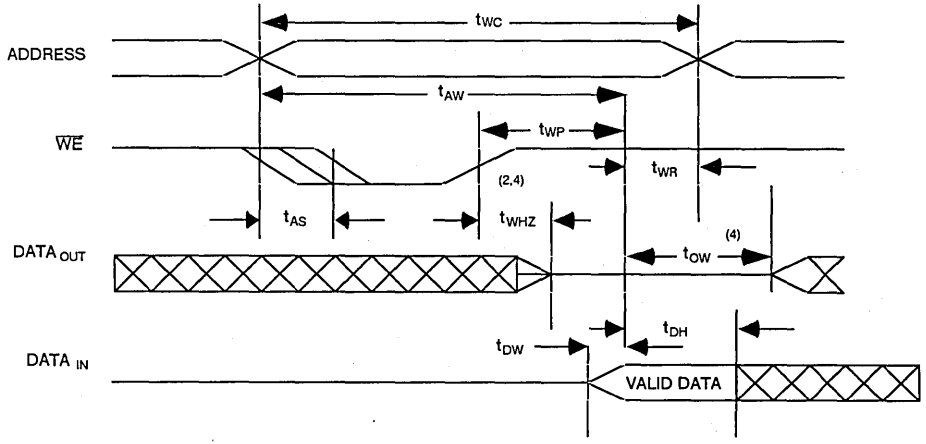
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	12ns		15ns		20/25ns		35/45ns		55ns		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	12	–	15	–	20/25	–	35/45	–	55	–	ns
t_{AW}	Address Valid to End of Write	10	–	12	–	14/20	–	30/40	–	50	–	ns
t_{AS}	Address Set-Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	10	–	12	–	14/20	–	30/40	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	9	–	10/13	–	17/20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	3	–	3	–	3	–	ns
t_{WHZ}	Write Enable to Output in High Z(1, 2)	–	6	–	7	–	9	–	13/20	–	25	ns
t_{OW}	Output Active from End of Write(1, 2)	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load.
2. This parameter is guaranteed, but not tested.

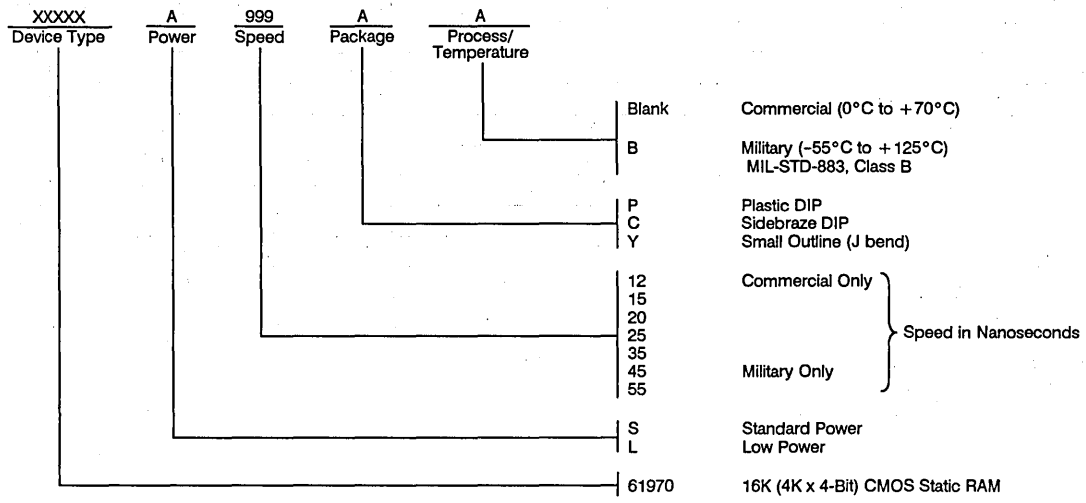
4

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the inputs must not be applied.
3. $\overline{OE}$ is continuously high or low. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
4. Transition is measured +/-200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM Cache TAG 16K(4K x 4-BIT)

ADVANCE INFORMATION IDT 7177

FEATURES:

- High-speed address to Match comparison time
  - Military: 15ns
  - Commercial: 12ns
- High-speed address access time
  - Military: 15ns
  - Commercial: 12ns
- Low-power operation
  - IDT7177S
  - Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Open drain MATCH output
- CE for depth expansion
- Two ground pins to reduce noise
- Standard 24 pin plastic or ceramic DIP, 24 pin SOJ
- Static operation: no clocks or refresh required
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7177 is a high-speed cache address comparator subsystem consisting of a 16384-bit static RAM organized as 4K x 4. Cycle Time and Compare Access Time are equal. The IDT7177 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins of several IDT7177's can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput. The 7177's $\overline{CE}$ can be used to accommodate deeper than 4K cache systems.

The IDT7177 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. Address to compare and data to compare access times as fast as 12ns.

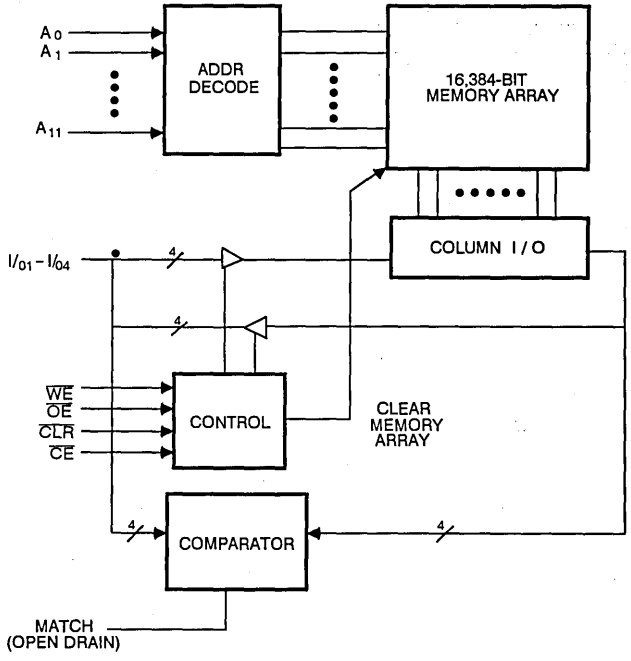
All inputs and outputs of the IDT7177 are TTL-compatible except MATCH, which is open drain. The 7177 features an extra GND. pin which significantly reduces noise. The device operates from a single 5V supply and Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7177 is packaged in either a 24 pin, 300 mil plastic or ceramic DIP package, and 24 pin SOJ.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

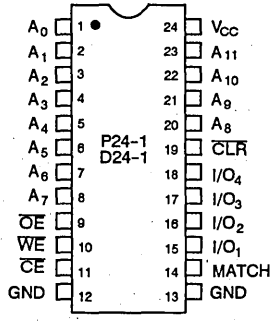
4

FUNCTIONAL BLOCK DIAGRAM

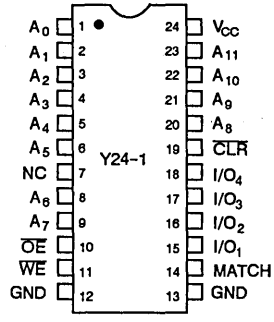


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



DIP
TOP VIEW

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	FUNCTION
L	H	H	H	Valid	Match Cycle
L	L	X	H	Invalid	Write Cycle
L	H	L	H	Invalid	Read Cycle
L	X	X	L	Invalid	Clear Cycle
H	X	X	X	Invalid	High Z

X = Don't Care

Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM Cache TAG 16K(4K x 4-BIT)

ADVANCE INFORMATION
IDT 7178

FEATURES:

- High-speed address to Match comparison time
  - Military: 15ns
  - Commercial: 12ns
- High-speed address access time
  - Military: 15ns
  - Commercial: 12ns
- Low-power operation
  - IDT7178S
  - Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Inputs/Outputs TTL compatible
- $\overline{CE}$ for depth expansion
- Two ground pins to reduce noise
- Standard 24 pin plastic or ceramic DIP, 24 pin SOJ
- Static operation: no clocks or refresh required
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7178 is a high-speed cache address comparator subsystem consisting of a 16384-bit static RAM organized as 4K x 4. Cycle Time and Compare Access Time are equal. The IDT7178 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins of several IDT7178's can be NANDed together to provide enabling or acknowledging signals to the data cache or processor. The 7178's $\overline{CE}$ can be used to accommodate deeper than 4K cache systems.

The IDT7178 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. Address to compare and data to compare access times as fast as 12ns.

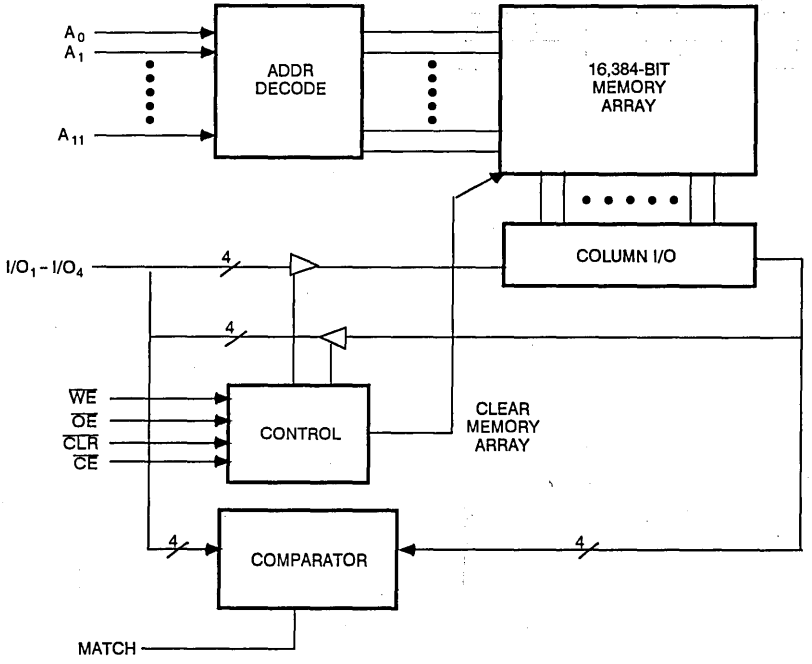
All inputs and outputs of the IDT7178 are TTL-compatible. The IDT7178 features an extra Gnd. pin which significantly reduces noise. The device operates from a single 5V supply and Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7178 is packaged in either a 24 pin, 300 mil plastic or ceramic DIP package, and 24 pin SOJ.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

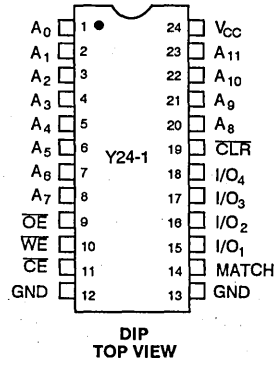
4

FUNCTIONAL BLOCK DIAGRAM

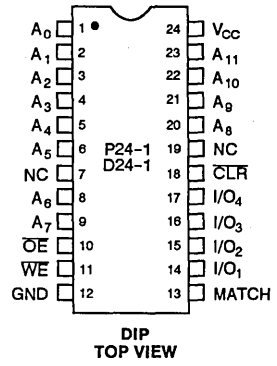


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



DIP
TOP VIEW

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	FUNCTION
L	H	H	H	Valid	Match Cycle
L	L	X	H	Invalid	Write Cycle
L	H	L	H	Invalid	Read Cycle
L	X	X	L	Invalid	Clear Cycle
H	X	X	X	Invalid	High Z

X = Don't Care

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT 6198S
IDT 6198L

4

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Output Enable ($\overline{OE}$) pin available for added system flexibility
- High-speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low-power consumption
  - IDT6198S
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
  - IDT6198L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin THINDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier and 24-pin SOIC (gull-wing and J-bend)
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

The IDT6198 features two memory control functions: chip select ($\overline{CS}$) and output enable ($\overline{OE}$). These two functions greatly enhance the IDT6198's overall flexibility in high-speed memory applications.

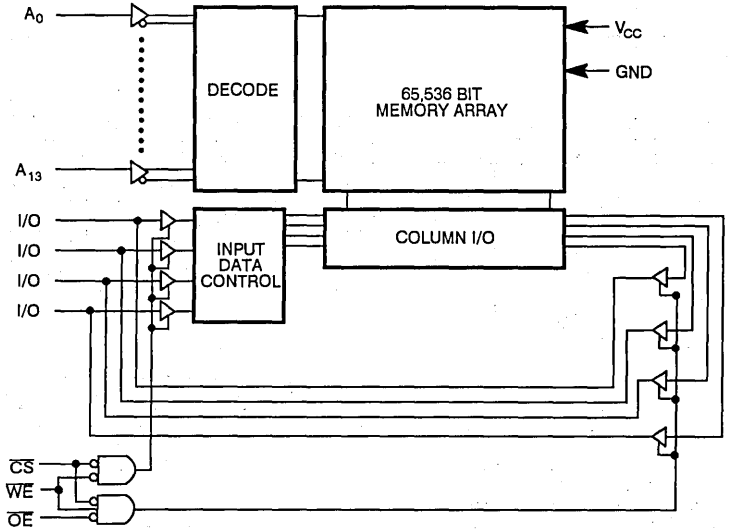
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT6198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2 volt battery.

All inputs and outputs are a TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT6198 is packaged in either a 24-pin THINDIP, 24-pin plastic DIP, 28-pin leadless chip carrier or 24-pin gull-wing or J-bend small outline IC, providing improved board-level packing densities.

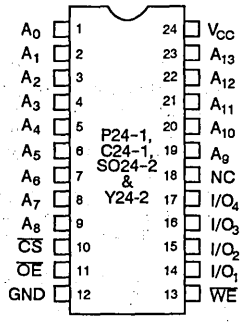
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

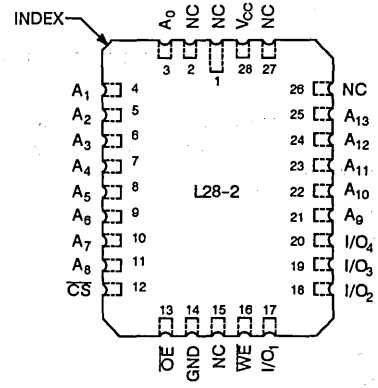


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

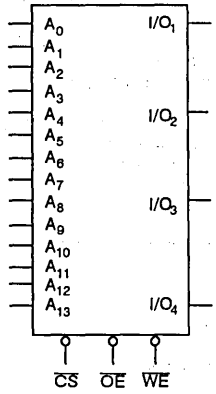


DIP/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_{1-4}	Data Input/Output
V_{CC}	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6198S MIN.	IDT6198S TYP.(1)	IDT6198S MAX.	IDT6198L MIN.	IDT6198L TYP.(1)	IDT6198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	6198S15 COM'L.	6198S15 MIL.	6198S19/20(2) COM'L.	6198S19/20(2) MIL.	6198S25 6198L25 COM'L.	6198S25 6198L25 MIL.	6198S30/35 6198L30/35 COM'L.	6198S30/35 6198L30/35 MIL.	6198S45/55(4) 6198L45/55(4) COM'L.	6198S45/55(4) 6198L45/55(4) MIL.	6198S70/85 6198L70/85 COM'L.	6198S70/85 6198L70/85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	S	135	–	120	140	100	125	100	110	100	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	180	–	155	175	135	155	125	140	125	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110/105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(3)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	S	25	–	20	25	15	20	15	20	15	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for Military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

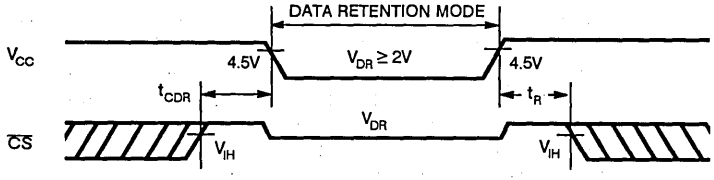
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

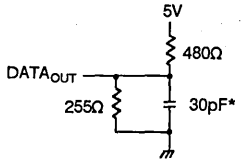


Figure 1. Output Load

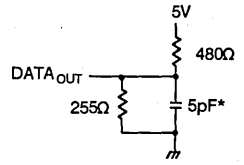


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

* Including scope and jig.

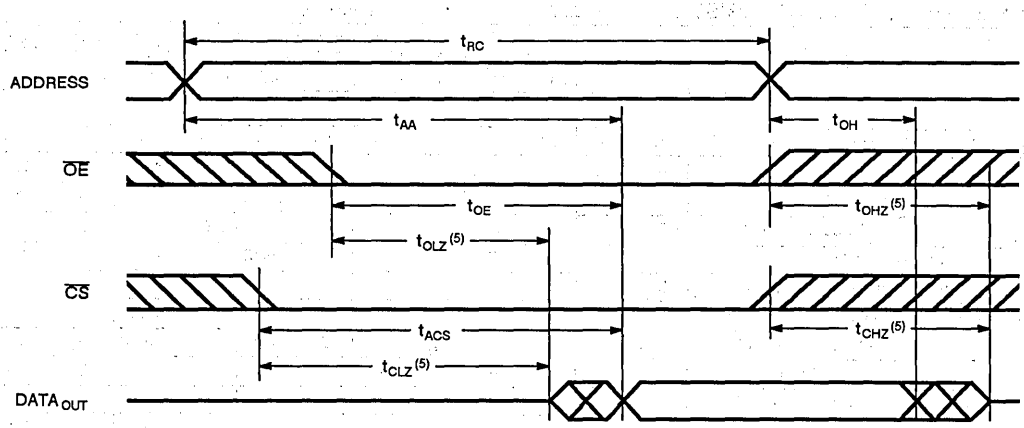
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6198S15[1] MIN.	6198S15[1] MAX.	6198S19/20 MIN.	6198S19/20 MAX.	6198S25 6198L25 MIN.	6198S25 6198L25 MAX.	6198S30/35 6198L30/35 MIN.	6198S30/35 6198L30/35 MAX.	6198S45/55[2] 6198L45/55[2] MIN.	6198S45/55[2] 6198L45/55[2] MAX.	6198S70[2]/85[2] 6198L70[2]/85[2] MIN.	6198S70[2]/85[2] 6198L70[2]/85[2] MAX.	UNIT
t_{RC}	Read Cycle Time	15	–	20	–	25	–	30/35	–	45/55	–	70/85	–	ns
t_{AA}	Address Access Time	–	15	–	19/20	–	25	–	29/35	–	45/55	–	70/85	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25	–	30/35	–	45/55	–	70/85	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	8	–	9	–	11	–	15/18	–	25/35	–	45/55	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z[3]	–	7	2	8	2	10	2	12/14	–	15/20	–	25/30	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	7	2	8	2	9	2	12/15	–	15/20	–	25/30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	2	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15	–	20	–	25	–	30/35	–	45/55	–	70/85	ns

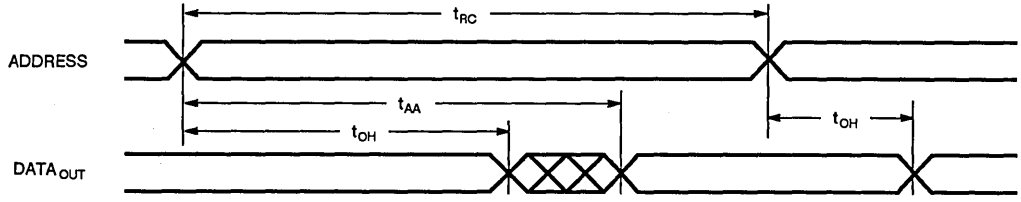
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

4

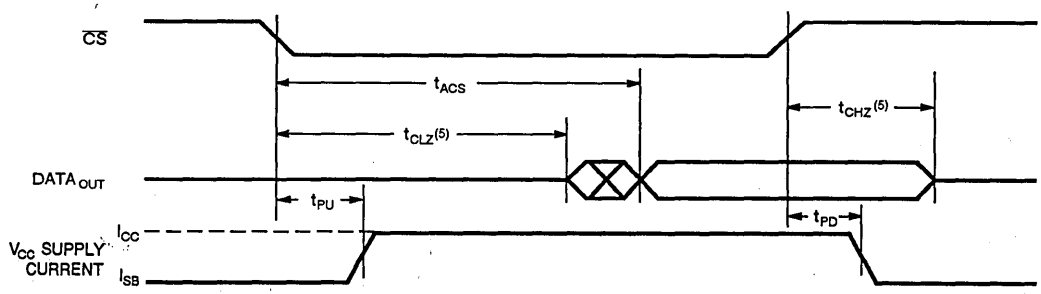
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state.

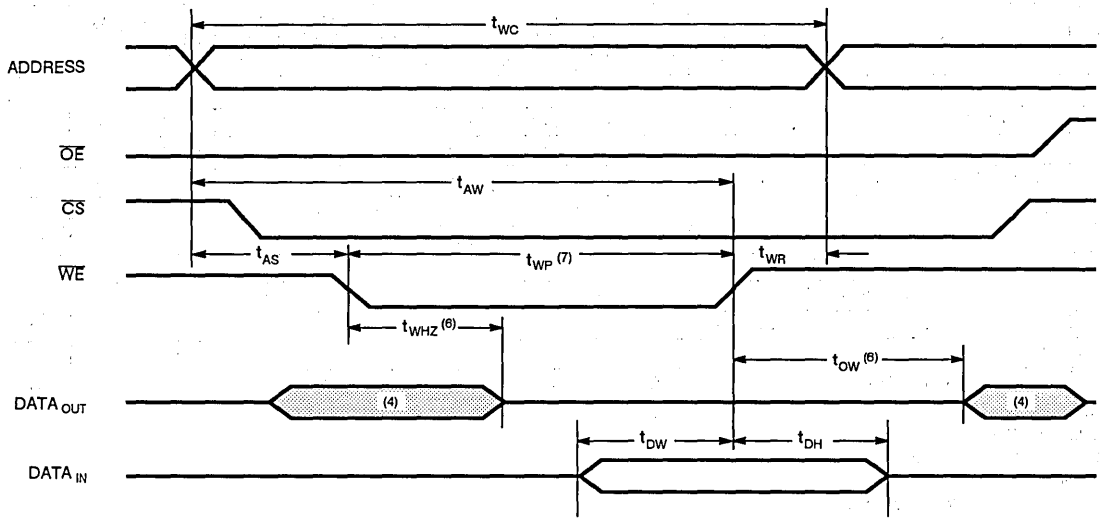
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6198S15[1] MIN.	6198S15[1] MAX.	6198S19/20[4] MIN.	6198S19/20[4] MAX.	6198S25 6198L25 MIN.	6198S25 6198L25 MAX.	6198S30/35 6198L30/35 MIN.	6198S30/35 6198L30/35 MAX.	6198S45/55[2] 6198L45/55[2] MIN.	6198S45/55[2] 6198L45/55[2] MAX.	6198S70[2]/85[2] 6198L70[2]/85[2] MIN.	6198S70[2]/85[2] 6198L70[2]/85[2] MAX.	UNIT
t_{WC}	Write Cycle Time	14	–	17	–	20	–	22/30	–	40/50	–	60/75	–	ns
t_{CW}	Chip Select to End of Write	14	–	17	–	20	–	22/25	–	35/50	–	60/75	–	ns
t_{AW}	Address Valid to End of Write	14	–	17	–	20	–	22/25	–	35/50	–	60/75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	14	–	17	–	20	–	22/25	–	35/50	–	60/75	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z[3]	–	5	–	6	–	7	–	10	–	15/25	–	30/40	ns
t_{DW}	Data Valid to End of Write	8	–	10	–	13	–	13/15	–	20/25	–	30/35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

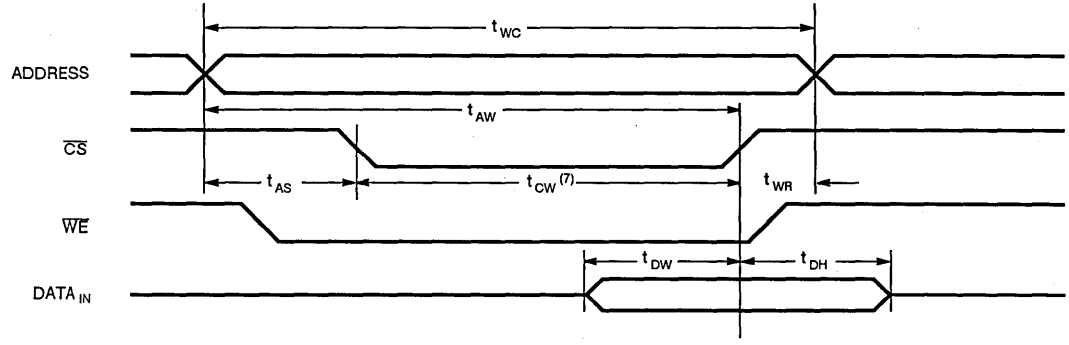
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5, 8)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IH}

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

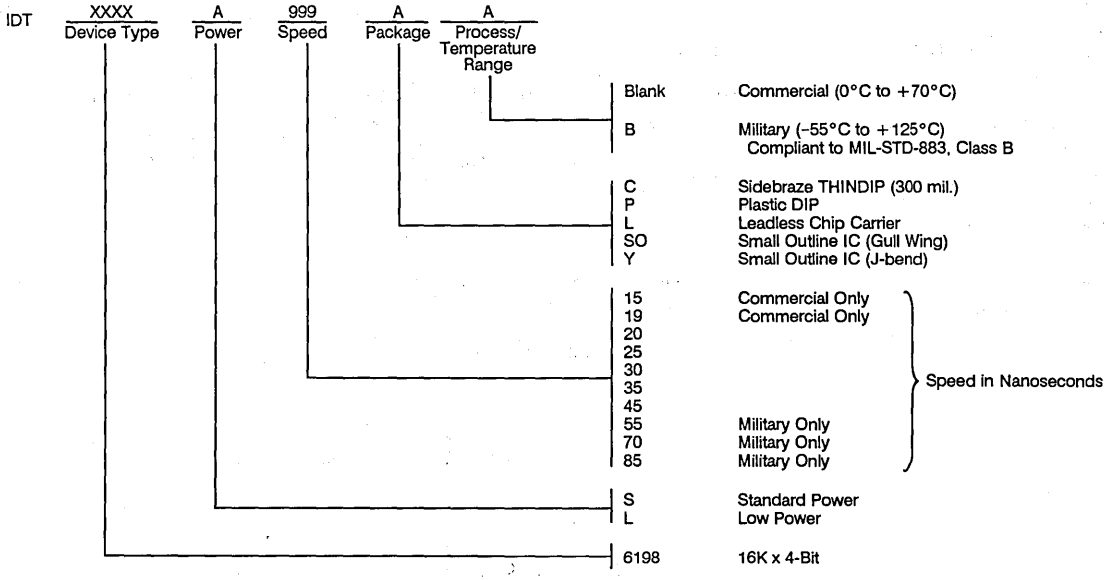
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

4

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT 7188S
IDT 7188L

FEATURES:

- High-speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7188S
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
  - IDT7188L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOIC, 24-pin Flatpack and CERPACK
- Produced with advanced CEMOS™ technology
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three-state outputs
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

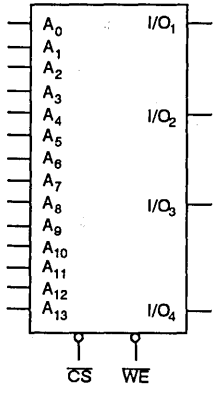
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

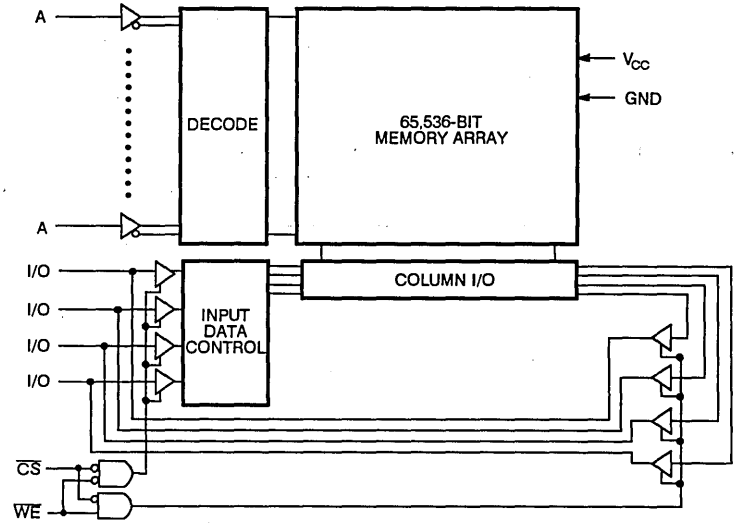
The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOICs, flatpacks and CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL

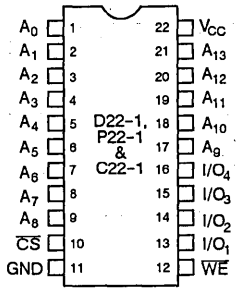


FUNCTIONAL BLOCK DIAGRAM

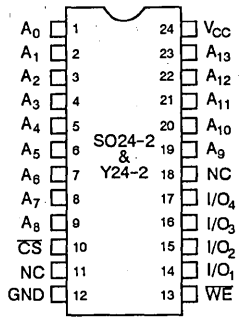


CEMOS is a trademark of Integrated Device Technology, Inc.

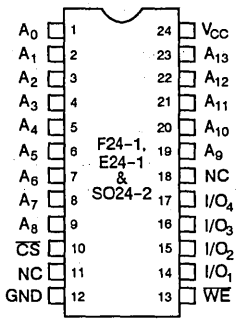
PIN CONFIGURATIONS



DIP
TOP VIEW



SOIC
TOP VIEW



FLATPACK/CERPACK/SOIC
TOP VIEW

4

PIN NAMES

A_0–A_{13}	Address Inputs	I/O_1–I/O_4	Data I/O
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7188S MIN.	IDT7188S TYP.(1)	IDT7188S MAX.	IDT7188L MIN.	IDT7188L TYP.(1)	IDT7188L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7188S15 COM'L.	7188S15 MIL.	7188S20 COM'L.	7188S20 MIL.	7188S25 7188L25 COM'L.	7188S25 7188L25 MIL.	7188S30/35 7188L30/35 COM'L.	7188S30/35 7188L30/35 MIL.	7188S45/55(3) 7188L45/55(3) COM'L.	7188S45/55(3) 7188L45/55(3) MIL.	7188S70 7188L70 COM'L.	7188S70 7188L70 MIL.	7188S85 7188L85 COM'L.	7188S85 7188L85 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	135	155	125	140	125	140	–	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC} f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

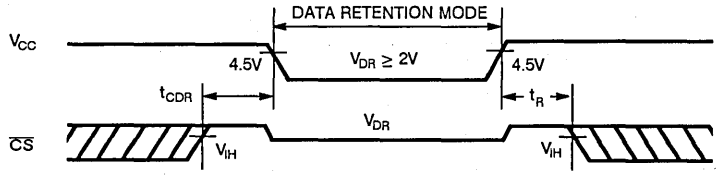
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = 25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

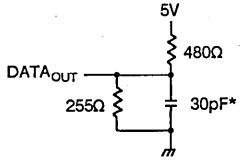


Figure 1. Output Load

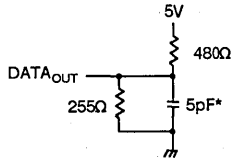


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

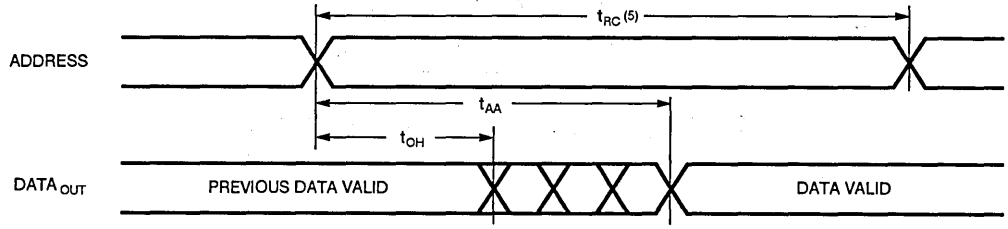
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

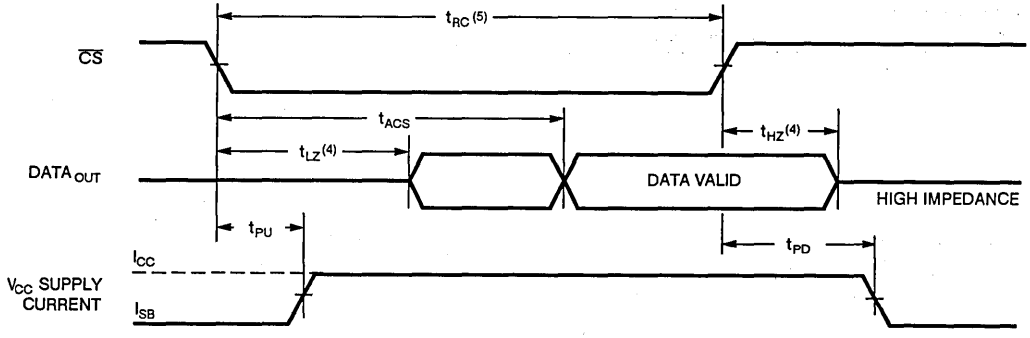
SYMBOL	PARAMETER	7188S15[1] MIN.	7188S15[1] MAX.	7188S20[4] MIN.	7188S20[4] MAX.	7188S25/30 7188L25/30 MIN.	7188S25/30 7188L25/30 MAX.	7188S35/45 7188L35/45 MIN.	7188S35/45 7188L35/45 MAX.	7188S55/70[2] 7188L55/70[2] MIN.	7188S55/70[2] 7188L55/70[2] MAX.	7188S85[2] 7188L85[2] MIN.	7188S85[2] 7188L85[2] MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25/30	–	35/45	–	55/70	–	85	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	–	7	–	8	–	10/12	–	14	–	20/25	–	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	15	–	20	–	25/30	–	35/45	–	55/70	–	85	ns

NOTES:
1. 0°C to -70°C temperature range only.
2. -55°C to -125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



NOTES:
1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

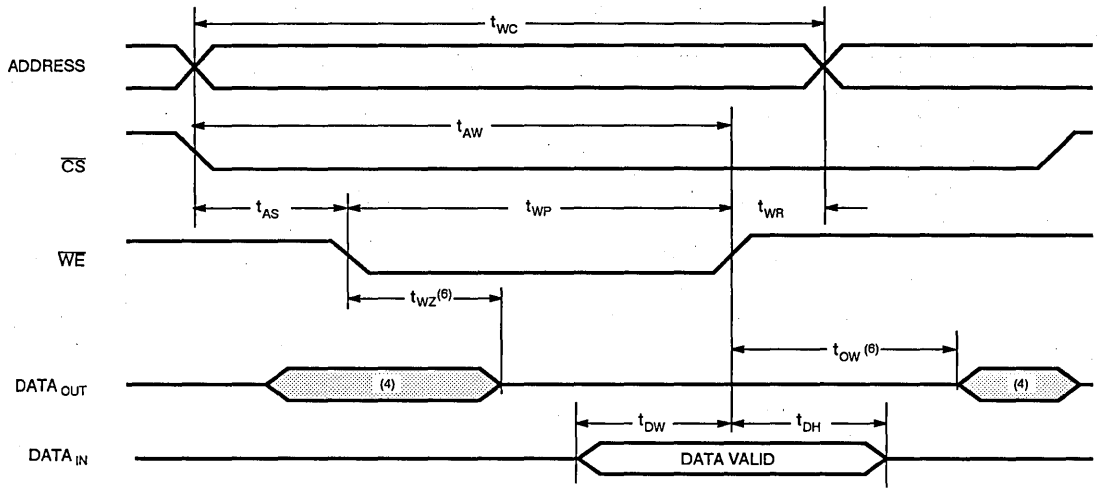
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7188S15[1]		7188S20[4]		7188S25/30 7188L25/30		7188S35/45 7188L35/45		7188S55/70[2] 7188L55/70[2]		7188S85[2] 7188L85[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	14	–	17	–	20/22	–	30/40	–	50/60	–	75	–	ns
t_{CW}	Chip Select to End of Write	14	–	17	–	20/22	–	25/35	–	50/60	–	75	–	ns
t_{AW}	Address Valid to End of Write	14	–	17	–	20/22	–	25/35	–	50/60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	14	–	17	–	20/22	–	25/35	–	50/60	–	75	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	8	–	10	–	13/15	–	15/20	–	25/30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enable to Output in High Z[3]	–	5	–	6	–	7/10	–	10/15	–	25/30	–	40	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

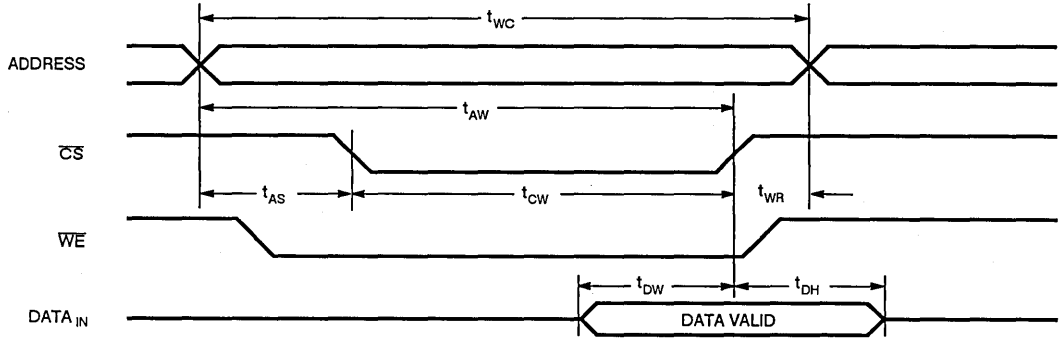
NOTES:
1. 0°C to -70°C temperature range only.
2. -55°C to -125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data only for military devices.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/O	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

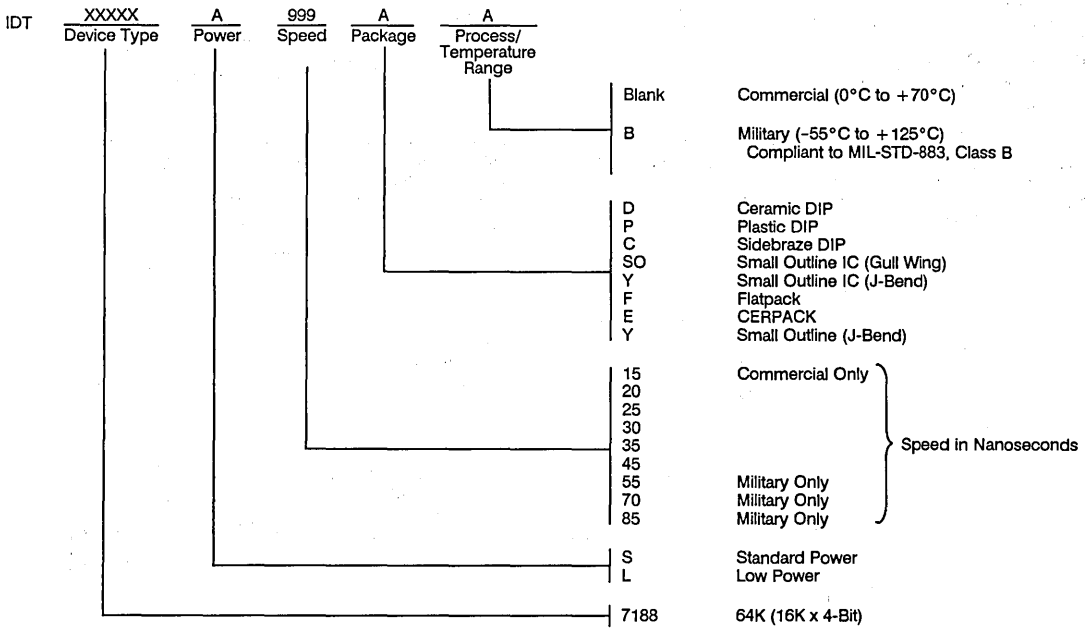
SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

4

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

Added Chip Select and Output Enable Controls

IDT 7198S
IDT 7198L

FEATURES:

- Optimized for fast RISC processors, including IDT79R3000
- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS_1}$, $\overline{CS_2}$) simplify system design and operation
- High speed (equal access and cycle times)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7198S
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
  - IDT7198L
    Active: 300mW (typ.)
    Standby: 30µw (typ.)
- Battery back-up operation—2V data retention (L version only)
- 24-pin THINDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOIC, flatpack and CERPACK
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86859 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

The IDT7198 features three memory control functions: Chip Select 1 ($\overline{CS_1}$), Chip Select 2 ($\overline{CS_2}$) and Output Enable ($\overline{OE}$). These three functions greatly enhance the IDT7198's overall flexibility in high-speed memory applications.

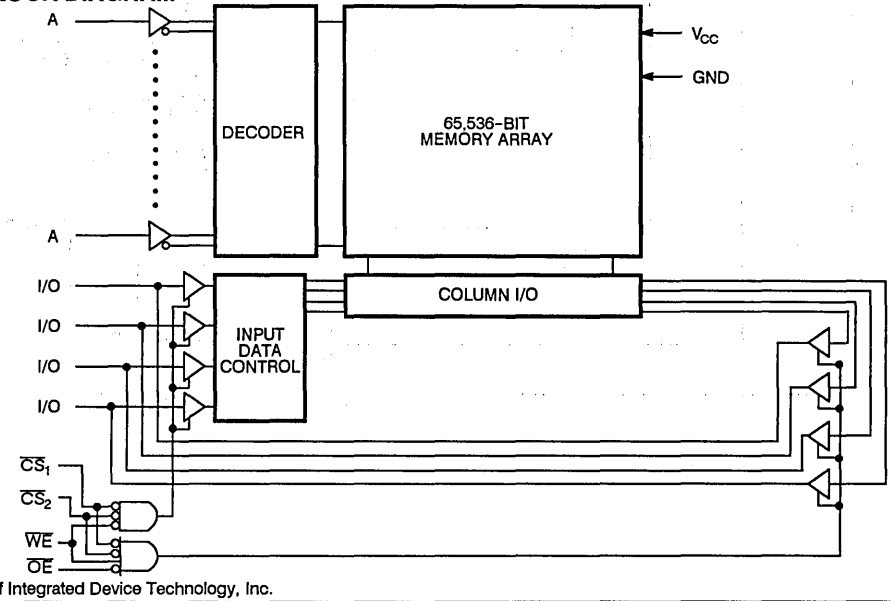
Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOIC and 24-pin flatpack or CERPACK, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

MEMORY CONTROL:

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature ($\overline{CS_1}$, $\overline{CS_2}$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding. Since external decoding logic is reduced, board space is saved, system speed is enhanced by approximately 10-20ns and system reliability improves as a result of lower parts count. (See technical note 1 "Using Two Chip Selects on the IDT7198.")

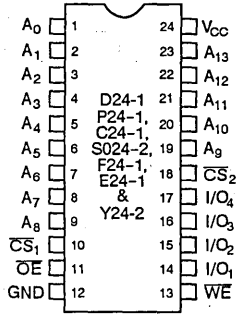
Both chip selects, Chip Select 1($\overline{CS_1}$) and Chip Select 2 ($\overline{CS_2}$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

The fast output enable function ($\overline{OE}$) is also a highly desirable feature of the IDT7198 high-speed common I/O static RAM. This function is designed to eliminate problems associated with data bus contention by allowing the data outputs to be controlled independent of either chip select. Its speed permits further decreases in overall read cycle timing.

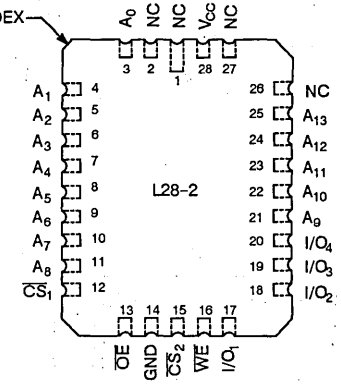
These added memory control features provide improved system design flexibility, along with overall system speed performance enhancements.

4

PIN CONFIGURATION

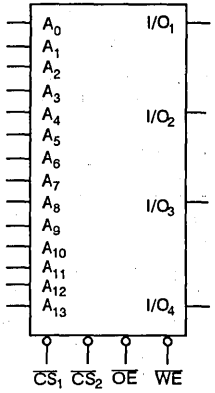


DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	Address Inputs	$\overline{OE}$	Output Enable
$\overline{CS_1}$	Chip Select 1	I/O_1 –I/O_4	Data I/O
$\overline{CS_2}$	Chip Select 2	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7198S MIN.	IDT7198S TYP.(1)	IDT7198S MAX.	IDT7198L MIN.	IDT7198L TYP.(1)	IDT7198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7198S15		7198S19/20		7198S25 7198L25		7198S30/35 7198L30/35		7198S45/55[3] 7198L45/55[3]		7198S70[3] 7198L70[3]		7198S85[3] 7198L85[3]		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	180	–	155	175	135	155	125	140	125	140	–	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}[2]	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

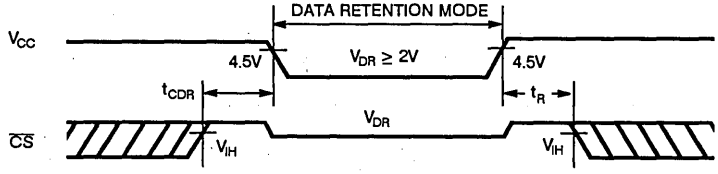
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

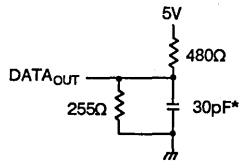


Figure 1. Output Load

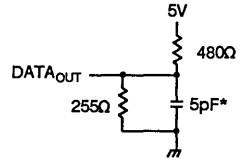


Figure 2. Output Load (for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

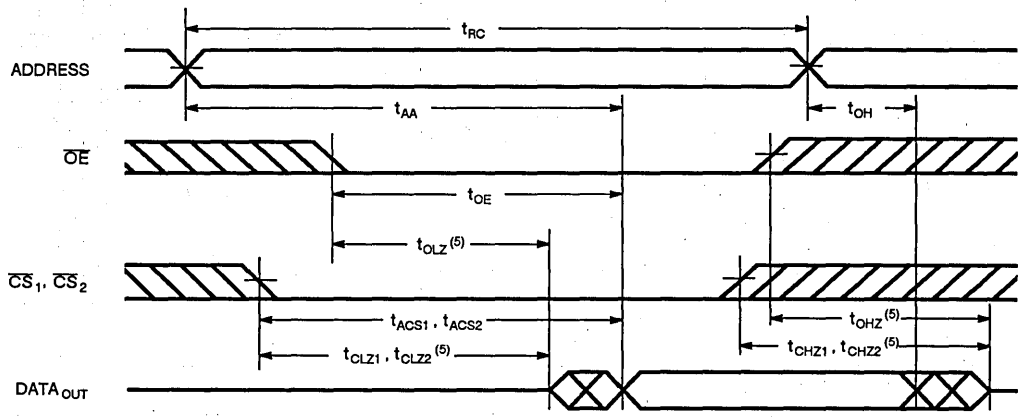
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7198S15[1]19/20[5] MIN.	MAX.	7198S25/30 7198L25/30 MIN.	MAX.	7198S35/45 7198L35/45 MIN.	MAX.	7198S55[2] 7198L55[2] MIN.	MAX.	7198S70[2] 7198L70[2] MIN.	MAX.	7198S85[2] 7198L85[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/19/20	–	25/29	–	35/45	–	55	–	70	–	85	ns
$t_{ACS1, 2}$	Chip Select-1, 2 Access Time[3]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{CLZ1, 2}$	Chip Select-1, 2 to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	8/9/9	–	11/18	–	20/25	–	35	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ1, 2}$	Chip Select-1, 2 to Output in High Z[4]	–	7/8/8	–	10/12	–	14	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z[4]	–	7/8/8	–	9/12	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[4]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns

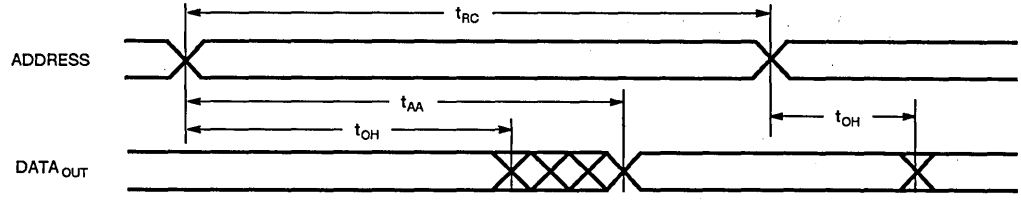
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data only for military devices.

4

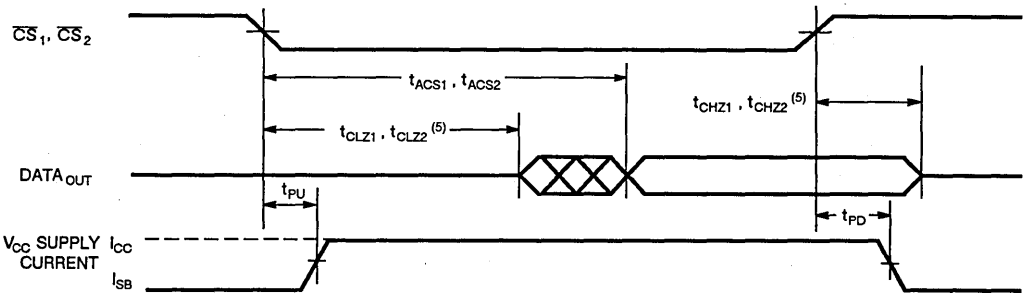
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

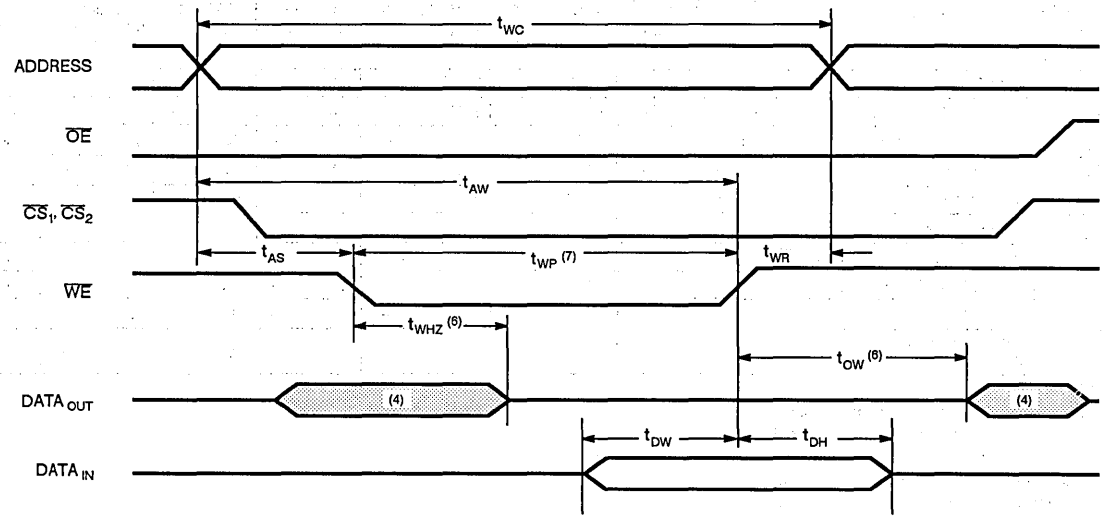
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7198S15[1]19/20[5] MIN.	MAX.	7198S25/30 7198L25/30 MIN.	MAX.	7198S35/45 7198L35/45 MIN.	MAX.	7198S55[2] 7198L55[2] MIN.	MAX.	7198S70[2] 7198L70[2] MIN.	MAX.	7198S85[2] 7198L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17/17	–	20/22	–	30/40	–	50	–	60	–	75	–	ns
$t_{CW1,2}$	Chip Select to End of Write[3]	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
$t_{WR1,2}$	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z[4]	–	5/6/6	–	7/10	–	10/15	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	8/10/10	–	13	–	15/20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns

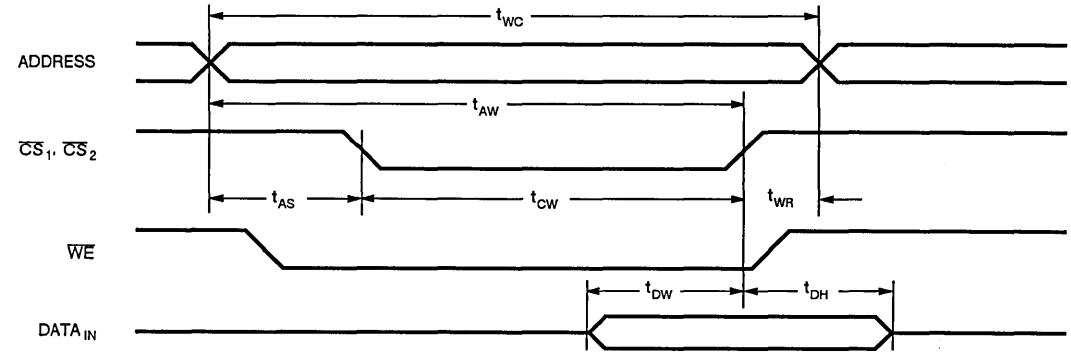
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data only for military devices.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5, 8]



NOTES:

1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a low $\overline{CS_2}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IH}

TRUTH TABLE

MODE	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write	L	L	L	X	D_{IN}	Active
Read	L	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

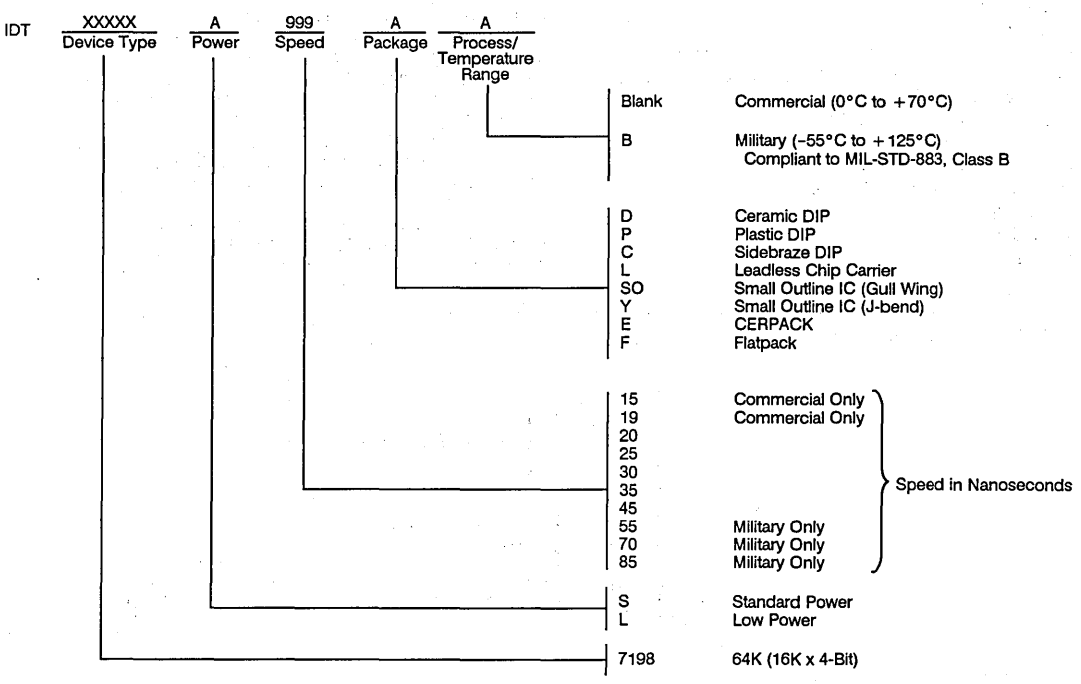
SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

4

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

Separate Data Inputs and Outputs

IDT 71981S/L
IDT 71982S/L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 20/25/30/35/45/55/70/85ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT71981/2S
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
  - IDT71981/2L
    Active: 300mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation – 2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, 28-pin SOIC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology – CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

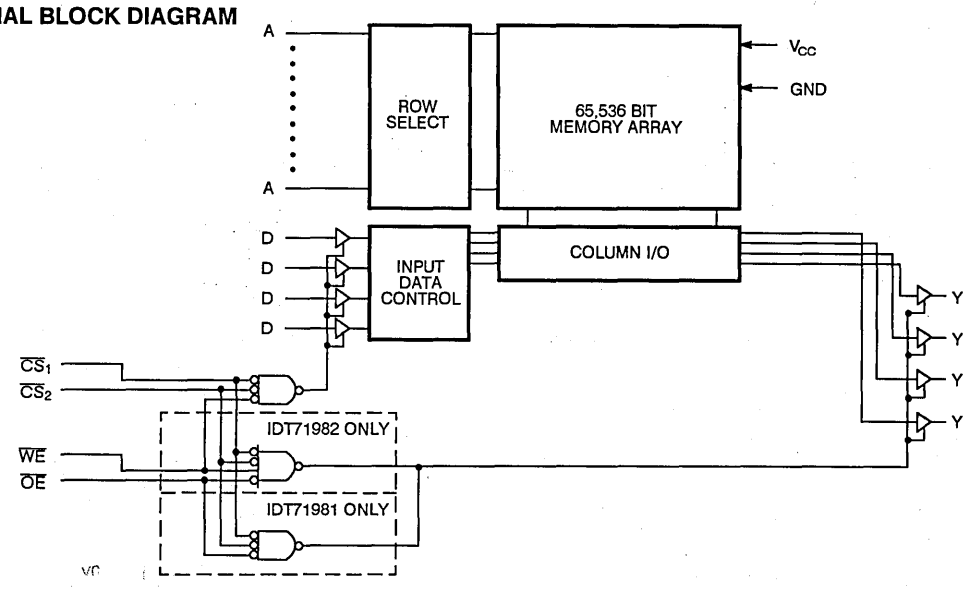
Access times as fast as 15ns are available with typical power consumption of only 300mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}_1$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30µW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71981/IDT71982 are packaged in either space-saving 28-pin, 400 mil hermetic DIPs, 28-pin 300 mil plastic DIP, 28-pin SOIC or 28-pin leadless chip carriers, providing high board-level packing densities.

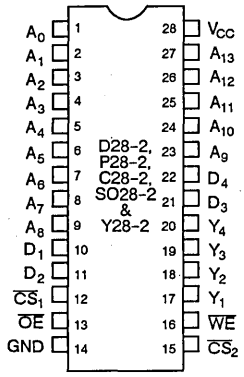
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

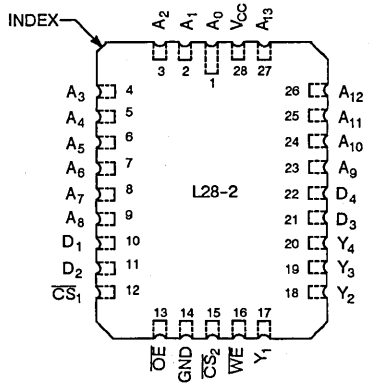


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

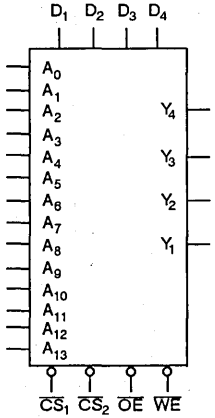


DIP/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{13}	Address Inputs	D_1–D_4	$DATA_{IN}$
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects	Y_1–Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71981/2S MIN.	IDT71981/2S TYP.(1)	IDT71981/2S MAX.	IDT71981/2L MIN.	IDT71981/2L TYP.(1)	IDT71981/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	71981/2S15		71981/2 S19/20		71981/2S25 71981/2L25		71981/2S30/35 71981/2L30/35		71981/2S45/55(3) 71981/2L45/55(3)		71981/2S70 71981/2L70		71981/2S85 71981/2L85		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	135	–	120	140	100	125	100	110	100	110	–	110	–	110	mA
		L	–	–	–	–	85	110	85	95	85	95	–	95	–	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	180	–	155	175	135	155	125	140	125	140	–	140	–	140	mA
		L	–	–	–	–	125	145	115/105	125/115	100	110	–	110	–	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IL}, V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S	75	–	60	70	55	60	50/45	55/50	45	50	–	50	–	50	mA
		L	–	–	–	–	45	50	40/35	45/40	30	35	–	35	–	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	25	–	20	25	15	20	15	20	15	20	–	20	–	20	mA
		L	–	–	–	–	0.5	1.5	0.5	1.5	0.5	1.5	–	1.5	–	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. -55°C to +125°C temperature range only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

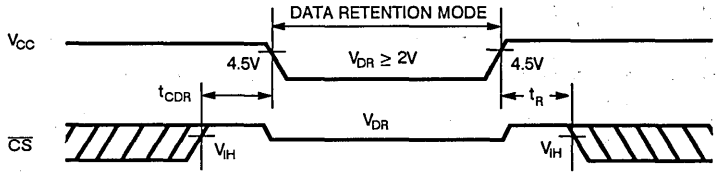
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	10	15	600	900	µA
			COM'L.	–	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

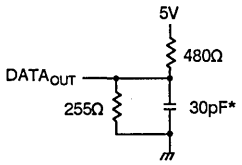


Figure 1. Output Load

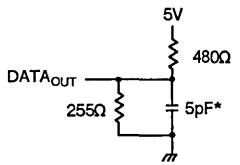


Figure 2. Output Load (for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

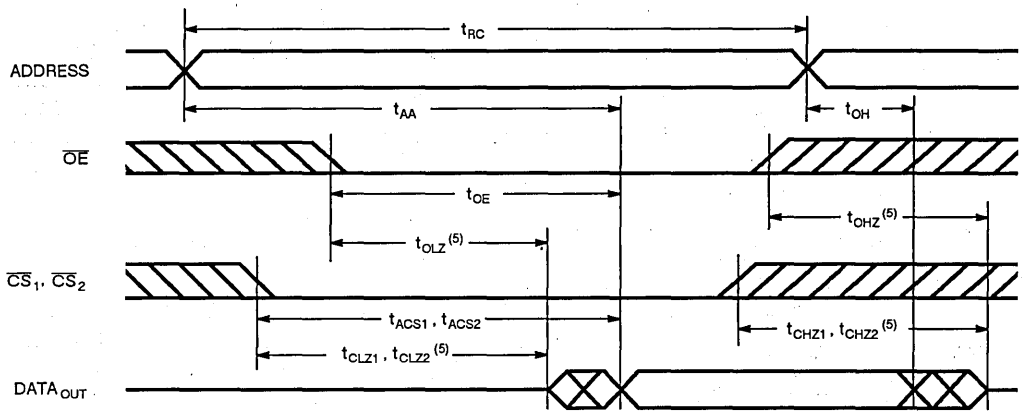
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71981/2S15[1] /19/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	15/19/20	–	25/29	–	35/45	–	55	–	70	–	85	ns
$t_{ACS1,2}$	Chip Select-1, 2 Access Time[3]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	8/9/9	–	11/18	–	20/25	–	35	–	45	–	55	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z[4]	–	7/8/8	–	10/12	–	14	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z[4]	–	7/8/8	–	9/12	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[4]	–	15/20/20	–	25/30	–	35/45	–	55	–	70	–	85	ns

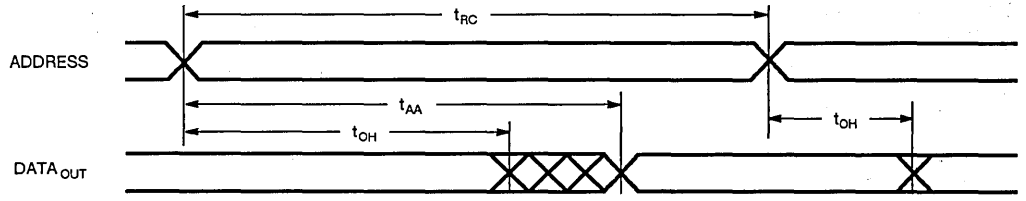
NOTES:

1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

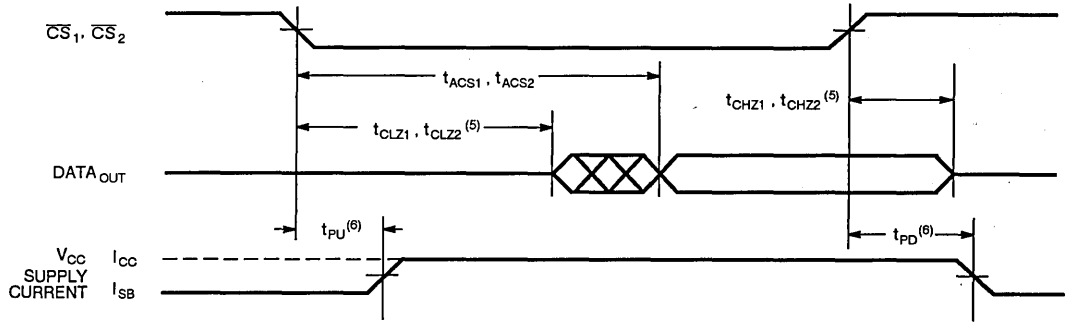
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$, and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.
6. This parameter is guaranteed but not tested.

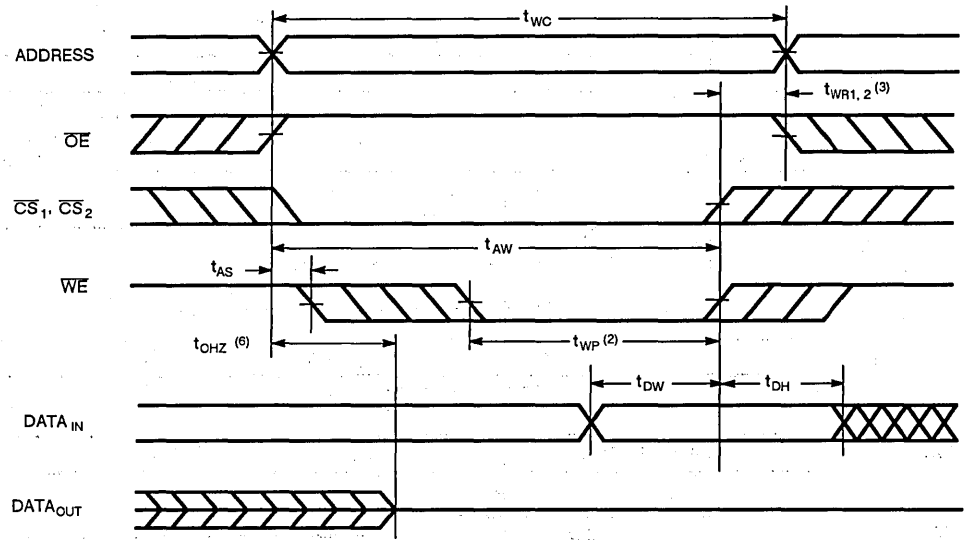
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71981/2S15[1] /19/20 MIN.	MAX.	71981/2S25/30 71981/2L25/30 MIN.	MAX.	71981/2S35/45 71981/2L35/45 MIN.	MAX.	71981/2S55[2] 71981/2L55[2] MIN.	MAX.	71981/2S70[2] 71981/2L70[2] MIN.	MAX.	71981/2S85[2] 71981/2L85[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	13/17/17	–	20/22	–	30/40	–	50	–	60	–	75	–	ns
$t_{CW1,2}$	Chip Select to End of Write	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13/17/17	–	20/22	–	25/35	–	50	–	60	–	75	–	ns
$t_{WR1,2}$	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output High Z [3,5]	–	5/6/6	–	7/10	–	10/15	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	8/10/10	–	13	–	15/20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [3,5]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid [3,4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns
t_{WY}	Write Enable to Output Valid [3,4]	–	12/15	–	20/25	–	30/35	–	40	–	45	–	50	ns

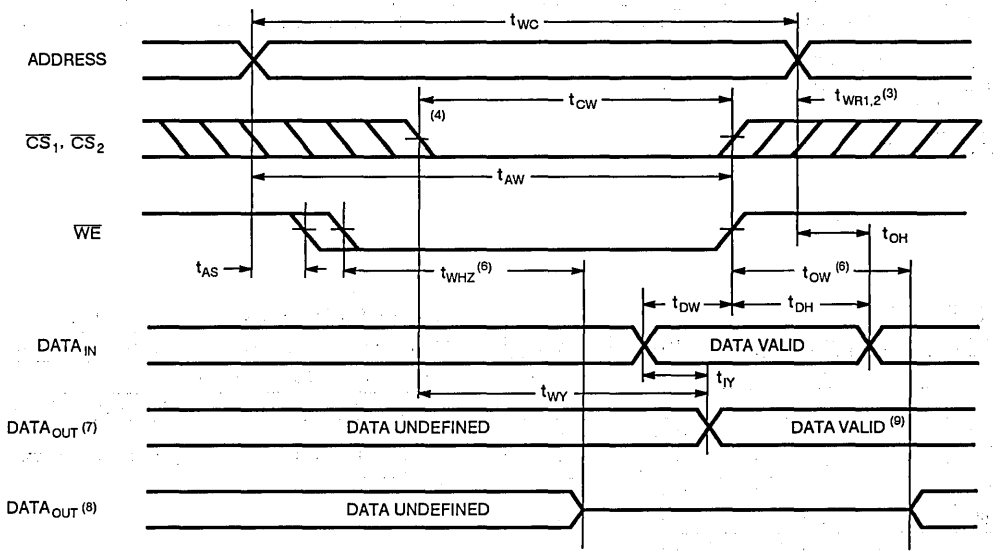
NOTES:

1. 0°C to +70°C temperature range only. Data for 20ns devices is preliminary for military temperature range.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

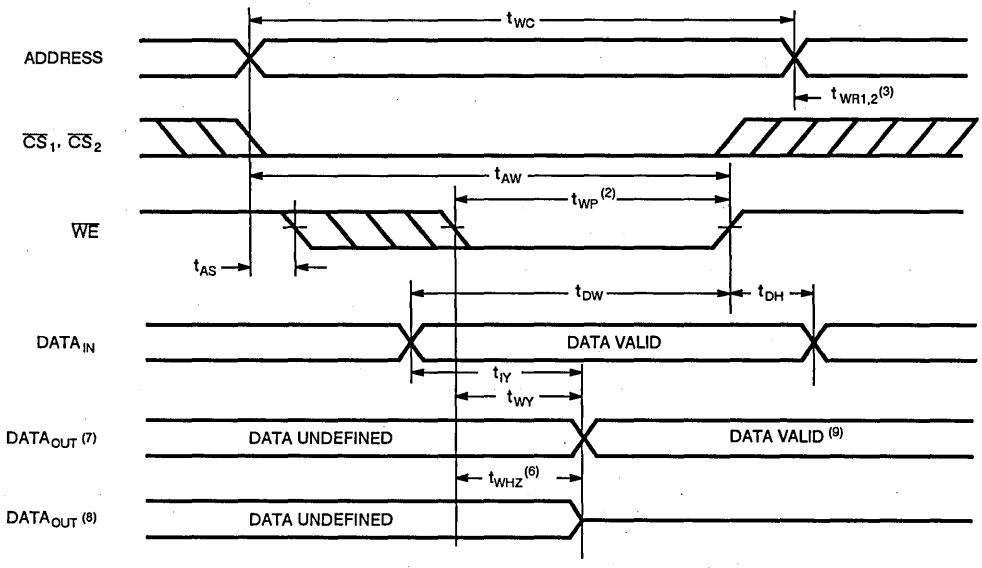
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 5)



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW) (1, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$, or $\overline{CS_2}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS_1}$ and a low $\overline{CS_2}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS_1}$ and or $\overline{CS_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT}$ = $DATA_{IN}$

TRUTH TABLE

MODE	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write (1)	L	L	L	L	D_{IN}	Active
Write (1)	L	L	L	H	High Z	Active
Write (2)	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

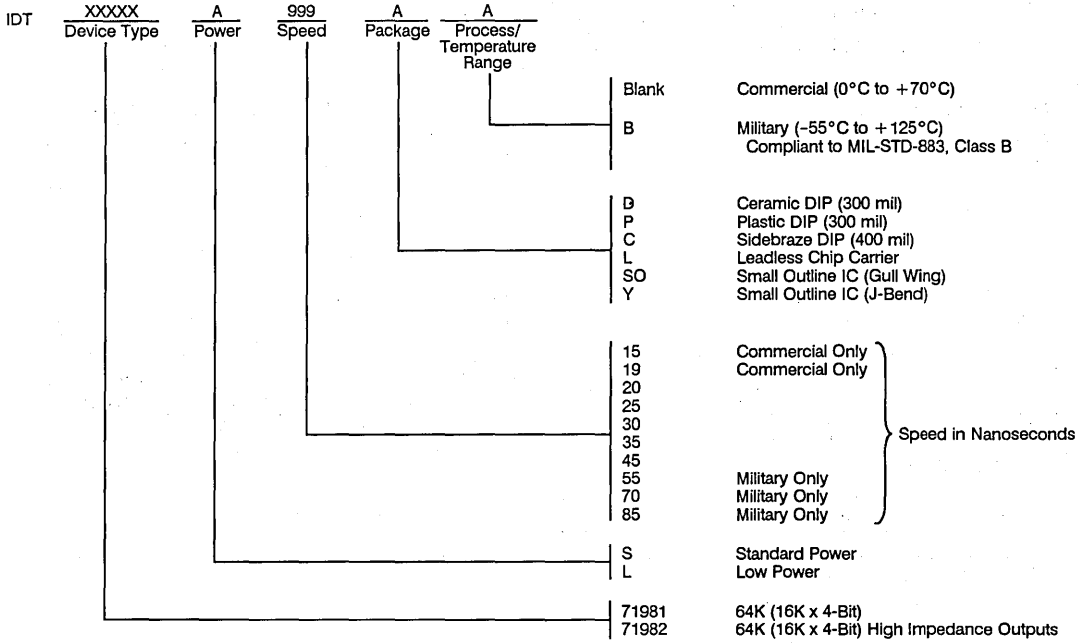
NOTES:
1. For IDT71981 only.
2. For IDT71982 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION



4

Integrated Device Technology, Inc.

CMOS SYNCHRONOUS STATIC RAM WITH TRANSPARENT OUTPUTS 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT 61592S
IDT 61592L

FEATURES:

- 16K x 4-Bit Organization
- High-speed Cycle Time
  - Commercial: 25ns
  - Military: 30ns
- Address, Data, $\overline{S}$ and $\overline{W}$ Registered Inputs
- External Clock Control
- Transparent Latched Outputs
- Internal Self-Timed Write Pulse Generation
- Separate I/O
- TTL-Compatible Input and Output
- High Output Drive Capability
- Produced with Advanced CEMOS™ High-Performance Technology
- Low Power-Consumption and High Reliability
- Single 5 Volt Power Supply
- Military Product is MIL-STD-883, Class B Compliant
- Wide Variety of Packages Available

DESCRIPTION:

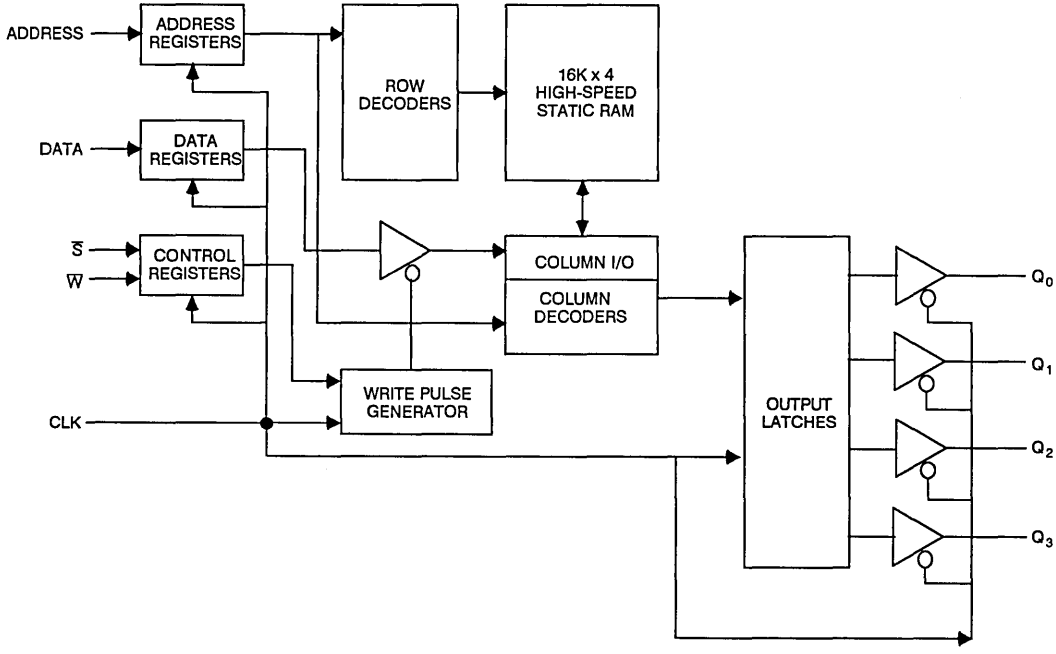
The IDT61592 is a 65,536-bit high-speed, synchronous static RAM organized as 16K x 4. It features the input registers and transparent latched outputs needed for low chip-count cache data RAM and writeable control store designs.

All inputs have positive-edge triggered, non-inverting registers controlled by the external clock input (CLK), allowing precise cycle control. When CLK is low, the device output becomes transparent, permitting access to RAM data within the same cycle. When CLK is high, the output data is latched.

The device features internally self-timed write operations, which are triggered by the rising edge of the external clock input. This eliminates the need for external write pulse generation and allows greater flexibility for incoming signals.

The IDT61592 is fabricated using IDT's high-performance CEMOS™ technology, which features extremely low power consumption and high-reliability.

FUNCTIONAL BLOCK DIAGRAM



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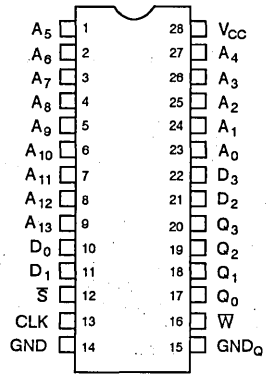
PIN CONFIGURATION



DIP
TOP VIEW

TRUTH TABLE

$\overline{S}$	$\overline{W}$	Q_0-Q_3	FUNCTION
L	L	Z	Write
L	H	Data Out	Read
H	X	Z	Deselected

NOTE:
H = High, L = Low, X = Don't care, Z = High Impedance

Integrated Device Technology, Inc.

CMOS SYNCHRONOUS STATIC RAM WITH OUTPUT REGISTERS 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT 61593S
IDT 61593L

FEATURES:

- 16K x 4-Bit Organization
- High-speed Cycle Time
  - Commercial: 25ns
  - Military: 30ns
- High-speed Clock Access Time
  - Commercial: 10ns
  - Military: 13ns
- Address, Data, $\overline{S}$ and $\overline{W}$ Registered Inputs
- Registered Outputs
- Internal Self-Timed Write Pulse Generation
- Separate I/O
- TTL-Compatible Input and Output
- High Output Drive Capability
- Produced with Advanced CEMOS™ High-Performance Technology
- Low Power-Consumption and High Reliability
- Single 5 Volt Power Supply
- Military Product is MIL-STD-883, Class B Compliant

DESCRIPTION:

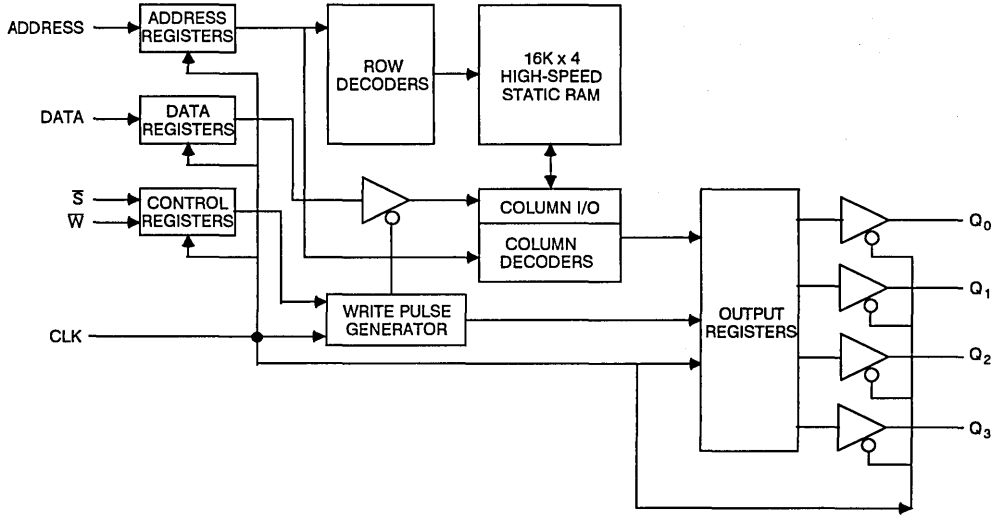
The IDT61593 is a 65,536-bit high-speed, synchronous static RAM organized as 16K x 4. It features the registered inputs and outputs needed for low chip-count cache data RAM and writeable control store designs.

All inputs have positive-edge triggered, non-inverting registers controlled by the external clock input (CLK), allowing precise cycle control. All outputs are also registered. At the rising edge of CLK, the RAM data from the previous CLK high cycle is clocked into the output registers. This feature is ideal in pipelined applications.

The device features internally self-timed write operations, which are triggered by the rising edge of the external clock input. This eliminates the need for external write pulse generation and allows greater flexibility for incoming signals.

The IDT61593 is fabricated using IDT's high-performance CEMOS™ technology, which features extremely low power consumption and high-reliability.

FUNCTIONAL BLOCK DIAGRAM



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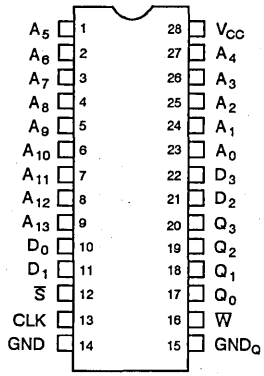
PIN CONFIGURATION



DIP
TOP VIEW

4

TRUTH TABLE [1]

$\overline{S}$	$\overline{W}$	Q_0-Q_3	FUNCTION
L	L	Z	Write
L	H	Data Out	Read
H	X	Z	Deselected

NOTE:
1. H = High, L = Low, X = Don't care, Z = High Impedance

Integrated Device Technology, Inc.

CMOS SYNCHRONOUS STATIC RAM W/ OUTPUT REGISTERS AND $\overline{OE}$ 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT 61594S
IDT 61594L

FEATURES:

- 16K x 4-Bit Organization
- High-speed Cycle Time
  - Commercial: 25ns
  - Military: 30ns
- High-speed Clock Access Time
  - Commercial: 10ns
  - Military: 13ns
- Address, Data and $\overline{W}$ Registered Inputs
- External Clock Control
- Registered Outputs
- Output Enable
- Internal Self-Timed Write Pulse Generation
- Separate I/O
- TTL-Compatible Input and Output
- High Output Drive Capability
- Produced with Advanced CEMOS™ High-Performance Technology
- Low Power-Consumption and High Reliability
- Single 5 Volt Power Supply
- Military Product is MIL-STD-883, Class B Compliant
- Wide Variety of Packages Available

DESCRIPTION:

The IDT61594 is a 65,536-bit high-speed, synchronous static RAM organized as 16K x 4. It features the registered inputs and outputs needed for low chip-count cache data RAM and writeable control store designs.

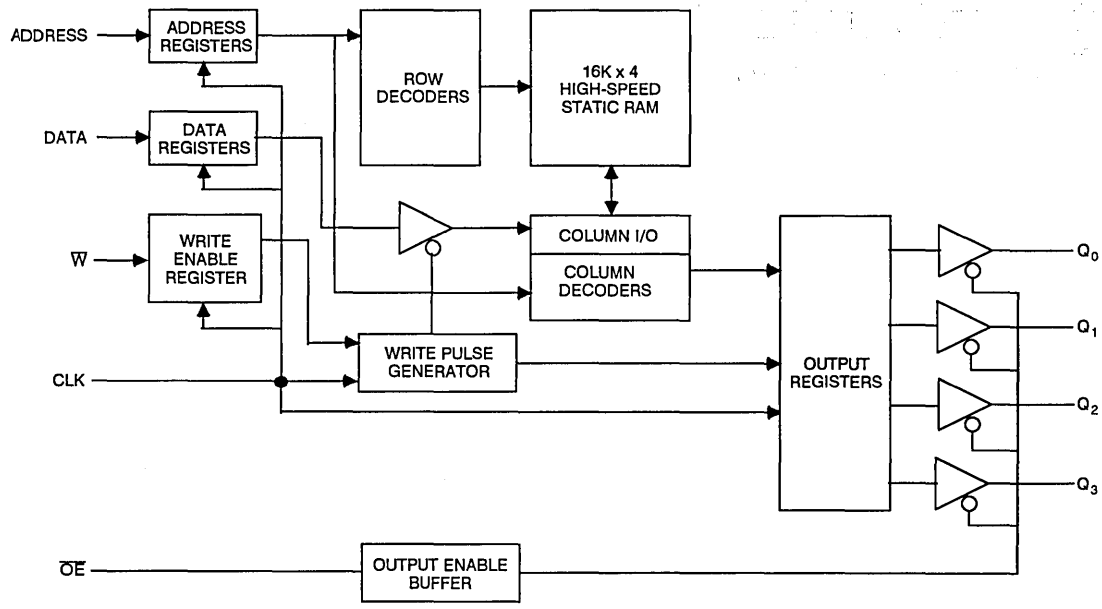
All inputs have positive-edge triggered, non-inverting registers controlled by the external clock input (CLK), allowing precise cycle control. All outputs are also registered. At the rising edge of CLK, the RAM data from the previous CLK high cycle is clocked into the output registers. This feature is ideal in pipelined applications.

The output enable ($\overline{OE}$) facilitates designs using asynchronous bus control.

The device features internally self-timed write operations, which are triggered by the rising edge of the external clock input. This eliminates the need for external write pulse generation and allows greater flexibility for incoming signals.

The IDT61594 is fabricated using IDT's high-performance CEMOS™ technology, which features extremely low power consumption and high-reliability.

FUNCTIONAL BLOCK DIAGRAM



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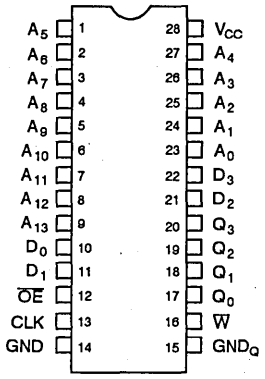
DSC-1053/-

PIN CONFIGURATION



DIP
TOP VIEW

TRUTH TABLE

$\overline{W}$	Q_0-Q_3	FUNCTION
L	High Z	Write
H	Data Out	Read

H = High, L = Low

Integrated Device Technology, Inc.

CMOS SYNCHRONOUS STATIC RAM W/ TRANSPARENT OUTPUTS AND $\overline{OE}$ 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT 61595S
IDT 61595L

FEATURES:

- 16K x 4-Bit Organization
- High-speed Cycle Time
  - Commercial: 25ns
  - Military: 30ns
- Address, Data and $\overline{W}$ Registered Inputs
- External Clock Control
- Transparent Latched Outputs
- Output Enable
- Internal Self-Timed Write Pulse Generation
- Separate I/O
- TTL-Compatible Input and Output
- High Output Drive Capability
- Produced with Advanced CEMOS™ High-Performance Technology
- Low Power-Consumption and High Reliability
- Single 5 Volt Power Supply
- Military Product is MIL-STD-883, Class B Compliant
- Wide Variety of Packages Available

DESCRIPTION:

The IDT61595 is a 65,536-bit high-speed, synchronous static RAM organized as 16K x 4. It features the registered inputs and outputs needed for low chip-count cache data RAM and writeable control store designs.

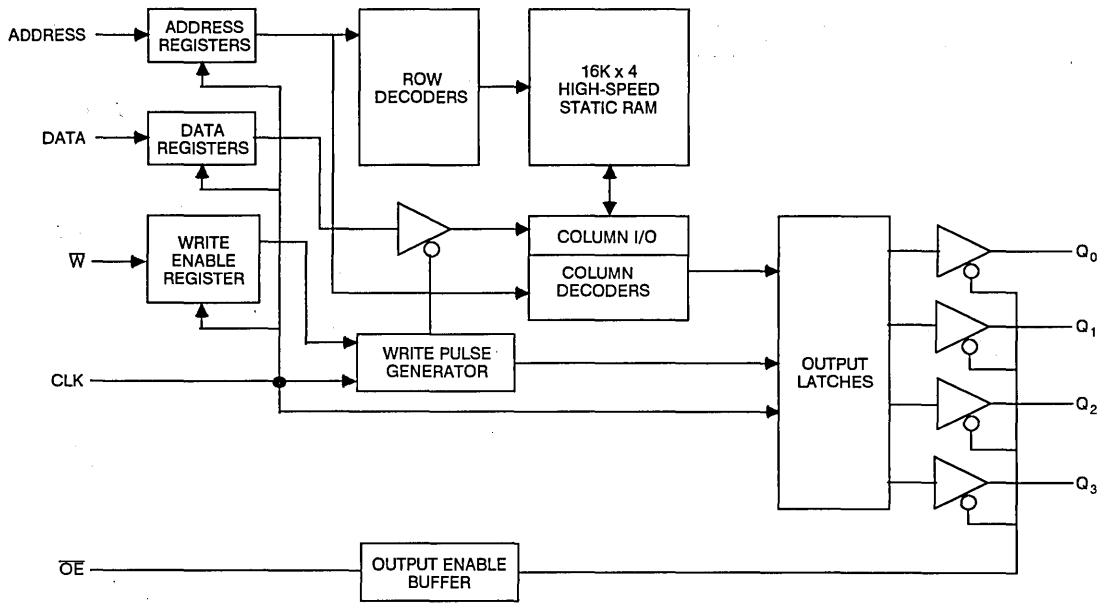
All inputs have positive-edge triggered, non-inverting registers controlled by the external clock input (CLK), allowing precise cycle control. When CLK is low, the device output becomes transparent, permitting access to RAM data within the same cycle. When CLK is high, the output data is latched.

The output enable ($\overline{OE}$) facilitates designs using asynchronous bus control.

The device features internally self-timed write operations, which are triggered by the rising edge of the external clock input. This eliminates the need for external write pulse generation and allows greater flexibility for incoming signals.

The IDT61595 is fabricated using IDT's high-performance CEMOS™ technology, which features extremely low power consumption and high-reliability.

FUNCTIONAL BLOCK DIAGRAM



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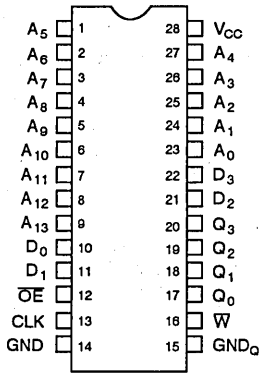
PIN CONFIGURATION



DIP
TOP VIEW

TRUTH TABLE

$\overline{W}$	$Q_0 - Q_3$	FUNCTION
L	High Z	Write
H	Data Out	Read

H = High, L = Low

Integrated Device Technology, Inc.

CMOS STATIC RAM WITH LATCHED ADDRESSES 64K (16K x 4-BIT)

ADVANCE INFORMATION
IDT 71598S
IDT 71598L

FEATURES:

- High-Speed Address Access Time
  - Military: 20/25/35ns
  - Commercial: 15/20/25ns
- On-Board Address Latches
- Low-Power Consumption and High-Reliability
- Battery Back-Up Operation: 2-Volt Data Retention (L Version Only)
- Produced with Advanced CEMOS™ High-Performance Technology
- Single 5V (±10%) Power Supply
- Input and Output Directly TTL Compatible
- Three-State Output
- Bidirectional Data Inputs and Outputs
- Static Operation No Clocks or Refresh Required
- Military Product Compliant to MIL-STD-883, Class B

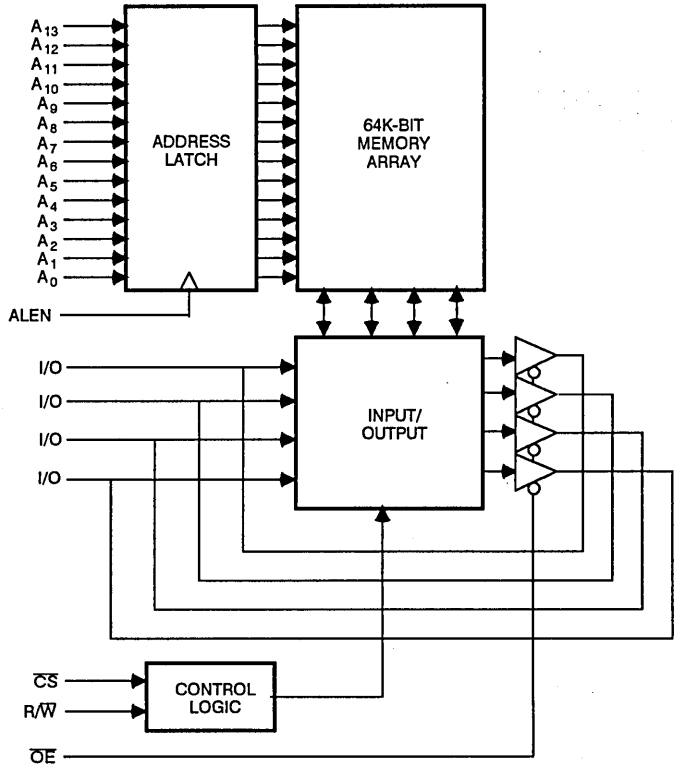
DESCRIPTION:

The 71598 is 65,536-bit high-speed static RAM organized as 16K x 4 with internal address latches. It is fabricated using IDT's high-performance, high-reliability CEMOS™ technology.

Address access times as fast as 15ns are available with typical power consumption of only 300mW. The 71598 excels in cache applications because of the on-chip address latches, which reduce system part count. This device is the preferred solution with 64K Byte Caches including the Intel 80386 and MIPS applications. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating off a 2V battery.

All inputs and outputs of the IDT71598 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT 61298S
IDT 61298L

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55ns (max.)
- Low power consumption
  - IDT61298S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - IDT61298L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery back-up operation—2V data retention (L version only)
- JEDEC standard pinout
- 28-pin DIP
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT61298 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

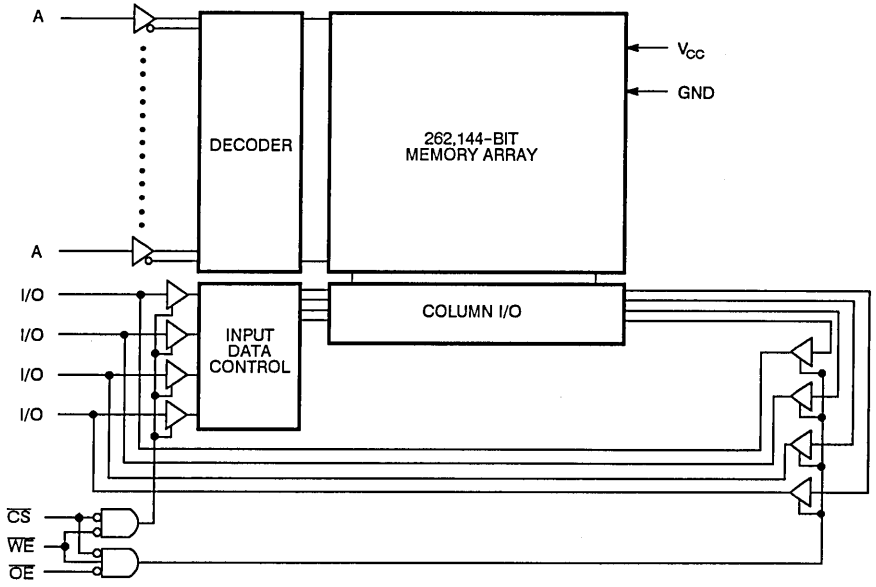
Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61298 is packaged in a 28-pin sidebraze or plastic 300mil DIP plus an SOIC, providing improved board-level packing densities.

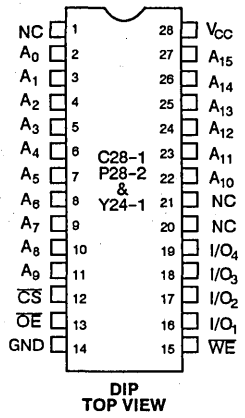
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



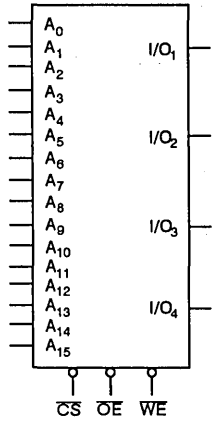
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{15}	Address Inputs	I/O_{1-4}	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

4

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT61298S MIN.	IDT61298S TYP.(1)	IDT61298S MAX.	IDT61298L MIN.	IDT61298L TYP.(1)	IDT61298L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS [1] V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	61298S20 61298L20		61298S25 [2] 61298L25 [2]		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		61298S70 61298L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0 [3]	S	READ	70	–	60	70	50	60	50	60	50	60	–	60	mA
			WRITE [4]	120	–	110	120	100	110	100	110	100	110	–	110	
		L	READ	50	–	40	50	30	40	30	40	30	40	–	40	
			WRITE [4]	110	–	100	110	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} [3]	S	READ	170	–	160	170	150	160	150	160	150	160	–	160	mA
			WRITE [4]	170	–	160	170	150	160	150	160	150	160	–	160	
		L	READ	150	–	140	150	130	140	130	140	130	140	–	140	
			WRITE [4]	150	–	140	150	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., f = f_{MAX} [3] Outputs Open.	S		35	–	35	35	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0 [3]	S		30	–	30	35	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{HC} = V_{CC} - 0.2V$

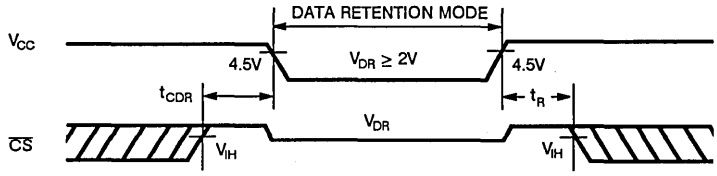
SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

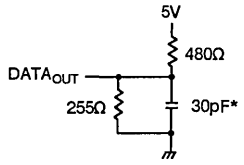


Figure 1. Output Load

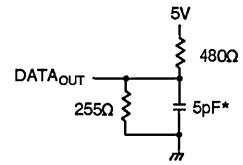


Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

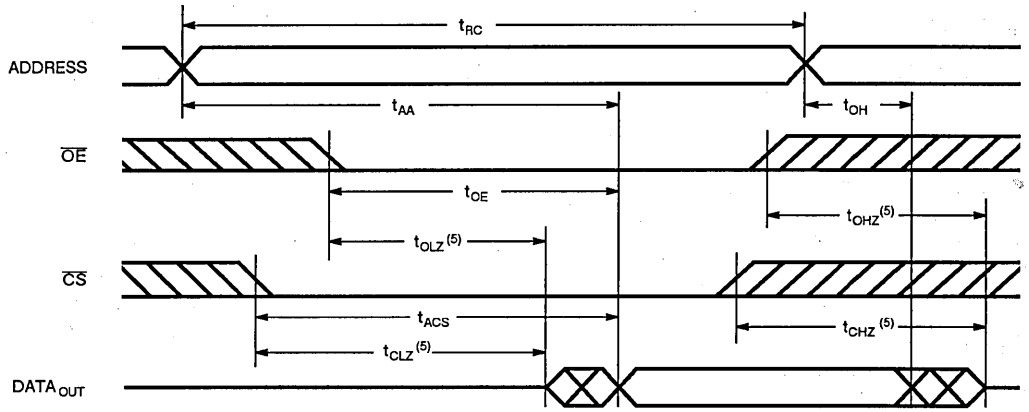
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	61298S20[1] 61298L20[1] MIN.	MAX.	61298S25[4] 61298L25[4] MIN.	MAX.	61298S35 61298L35 MIN.	MAX.	61298S45 61298L45 MIN.	MAX.	61298S55 61298L55 MIN.	MAX.	61298S70[2] 61298L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}[3]	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	12	–	15	–	25	–	30	–	35	–	45	ns
t_{OLZ}[3]	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}[3]	Chip Select to Output in High Z	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OHZ}[3]	Output Disable to Output in High Z	–	10	–	13	–	15	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}[3]	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}[3]	Chip Deselect to Power Down Time	–	20	–	25	–	35	–	45	–	55	–	70	ns

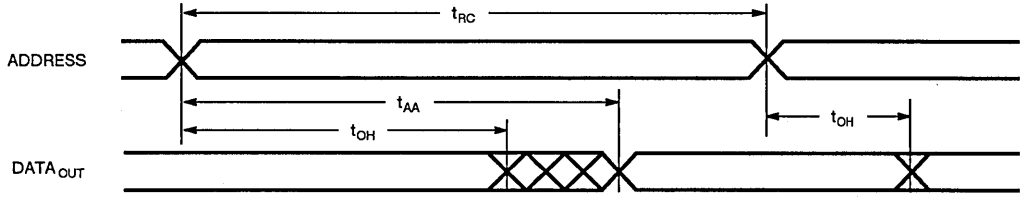
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

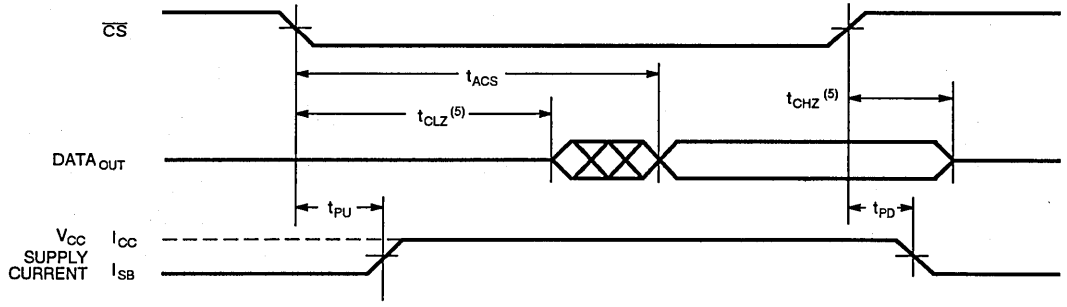
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state.

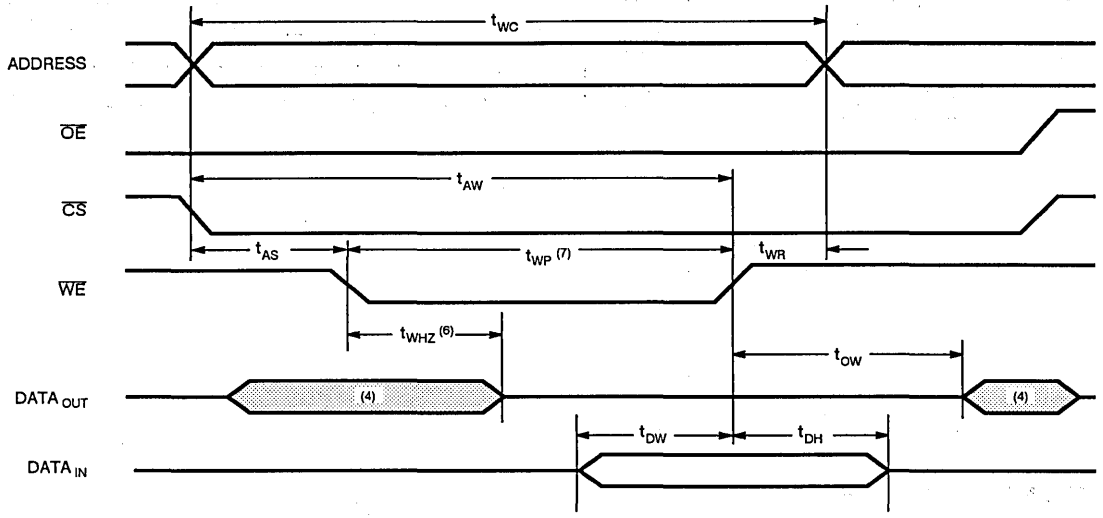
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	61298S20[1] 61298L20[1] MIN.	MAX.	61298S25[4] 61298L25[4] MIN.	MAX.	61298S35 61298L35 MIN.	MAX.	61298S45 61298L45 MIN.	MAX.	61298S55 61298L55 MIN.	MAX.	61298S70[2] 61298L70[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}[3]	Write Enable to Output in High Z	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}[3]	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

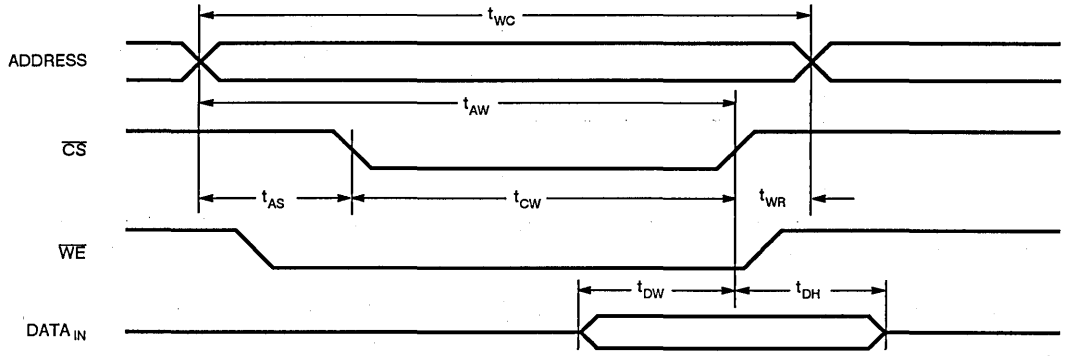
NOTES:

1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

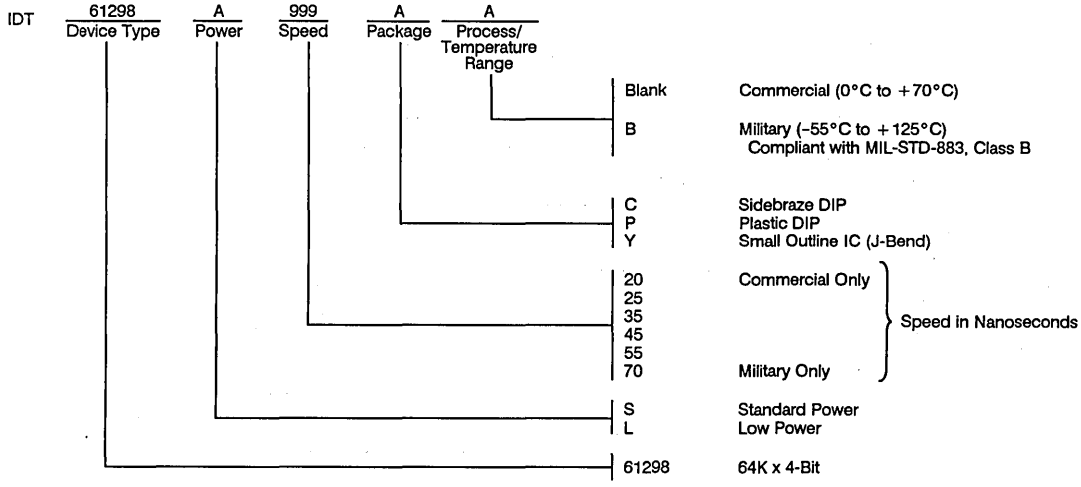
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT 71258S
IDT 71258L

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55/ns (max.)
- Low-power operation
  - IDT71258S
    Active: 400mW (typ.)
    Standby: 400µW (typ.)
  - IDT71258L
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP, 24-pin SOIC (gull-wing and J-Bend), 28-pin LCC, and a 24-pin Cerpack
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71258 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

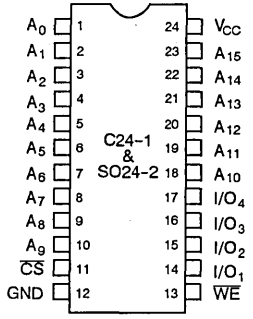
Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT71258 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation off a 2V battery.

All inputs and outputs of the IDT71258 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71258 is packaged in a 24-pin 300 mil DIP, a 24-pin SOIC (gull-wing or J-Bend), a 28-pin LCC, and a 24-pin Cerpack providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

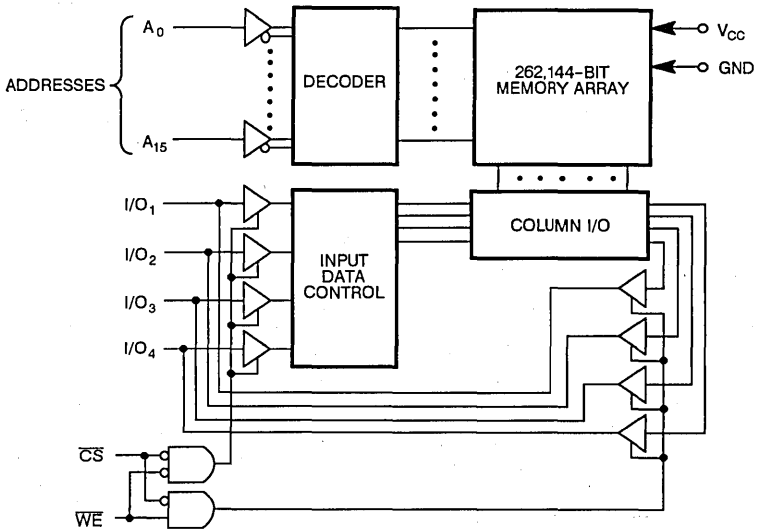


DIP/SOIC/CERPACK
TOP VIEW

PIN NAMES

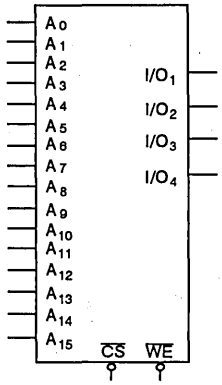
$A_0 - A_{15}$	Addresses
$I/O_1 - I/O_4$	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
GND	Ground
V_{CC}	Power

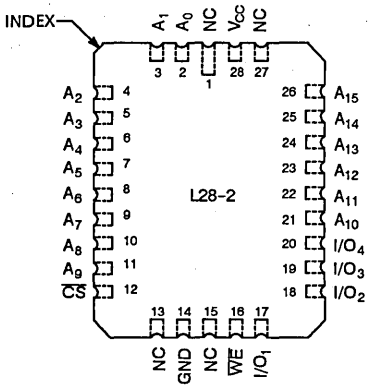
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL





RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71258S MIN.	IDT71258S MAX.	IDT71258L MIN.	IDT71258L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS[1] (V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

SYMBOL	PARAMETER	POWER	FUNCTION	71258S20 71258L20		71258S25[4] 71258L25[4]		71258S35 71258L35		71258S45 71258L45		71258S55 71258L55		71258S70 71258L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	S	READ	60	–	60	60	50	60	50	60	50	60	–	60	mA
			WRITE[2]	110	–	110	110	100	110	100	110	100	110	–	110	
		L	READ	40	–	40	40	30	40	30	40	30	40	–	40	
			WRITE[2]	100	–	100	100	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	S	READ	160	–	160	160	150	160	150	160	150	160	–	160	mA
			WRITE[2]	160	–	160	160	150	160	150	160	150	160	–	160	
		L	READ	140	–	140	140	130	140	130	140	130	140	–	140	
			WRITE[2]	140	–	140	140	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open f = f_{MAX}[3]	S	–	35	–	35	35	35	35	35	35	35	35	–	35	mA
		L	–	20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[3]	S	–	30	–	30	35	30	35	30	35	30	35	–	35	mA
		L	–	1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When comparing these figures to those on other data sheets, we recommend that the read cycle data is used (especially where "Average" current consumption figures are specified).
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $/t_{RC}$. f = 0 means no input lines change.
4. Preliminary data for military devices only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is but production tested.

TRUTH TABLE (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS}$	I/O	MODE
X	H	Hi-Z	Standby (I_{SB})
X	V_{HC}	Hi-Z	Standby (I_{SB1})
H	L	D_{OUT}	Read
L	L	D_{IN}	Write

NOTE:

1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

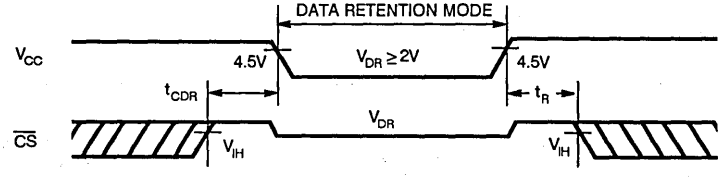
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

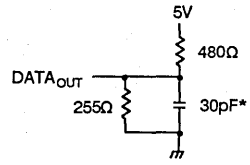


Figure 1. Output Load

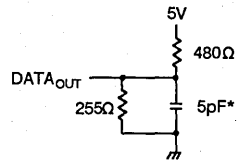


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

*Including scope and jig.

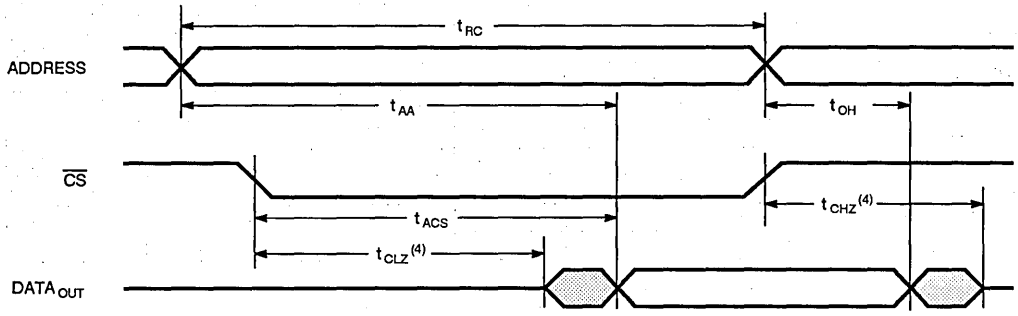
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	71258S20[1] 71258L20[1] MIN.	MAX.	71258S25 71258L25 MIN.	MAX.	71258S35 71258L35 MIN.	MAX.	71258S45 71258L45 MIN.	MAX.	71258S55 71258L55 MIN.	MAX.	71258S70[2] 71258L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

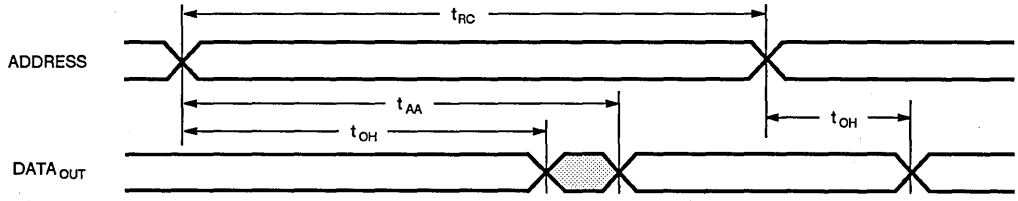
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed, but not tested.

4

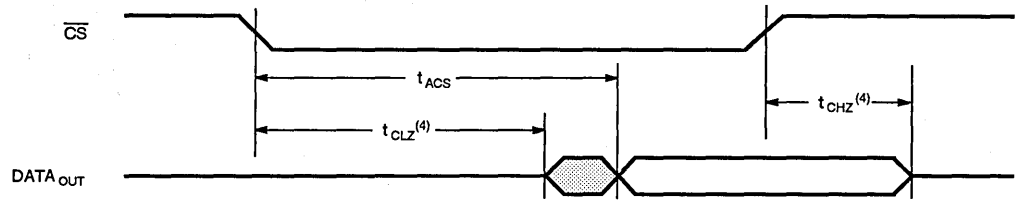
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3]



NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

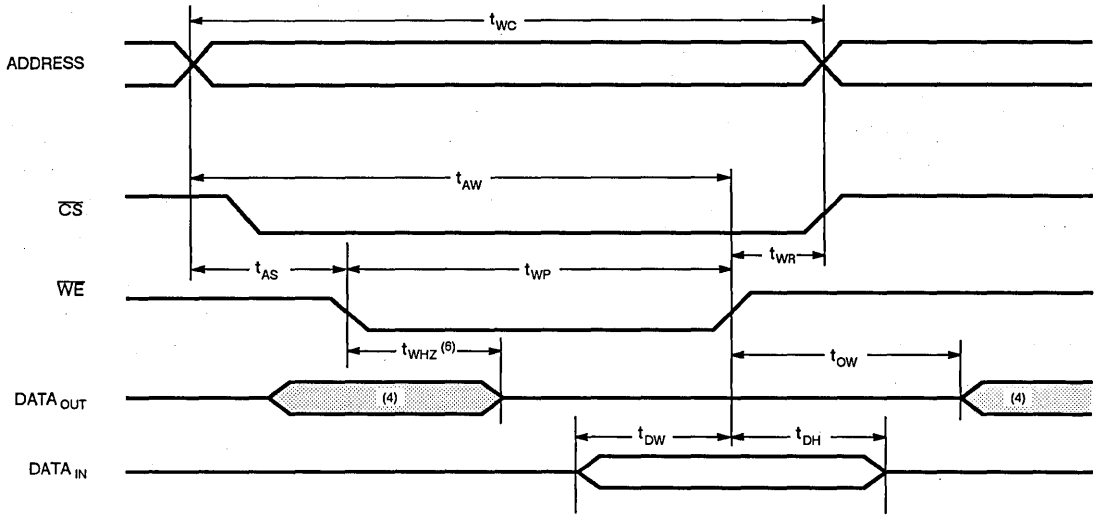
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	71258S20 (1) 71258L20 (1)		71258S25 71258L25		71258S35 71258L35		71258S45 71258L45		71258S55 71258L55		71258S70 (2) 71258L70 (2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z (3)	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write (3)	5	–	5	–	5	–	5	–	5	–	5	–	ns

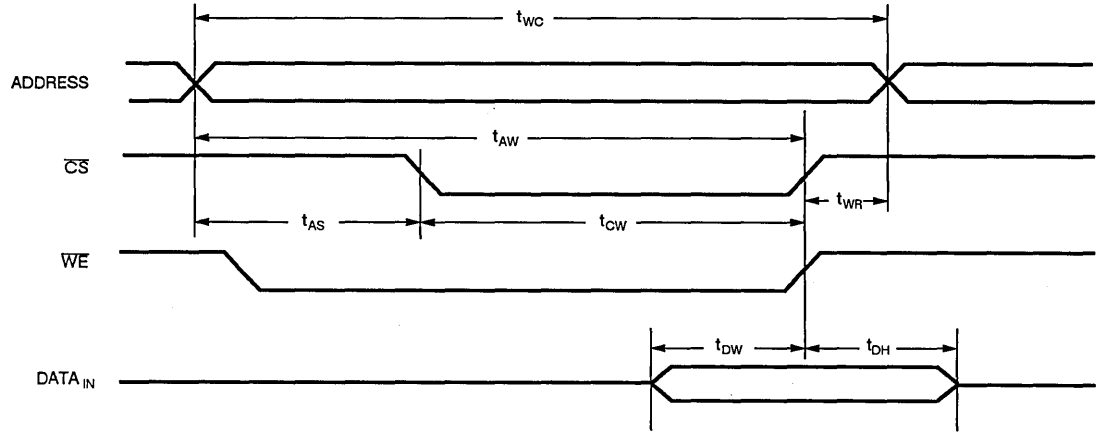
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed, but not tested.

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 6]



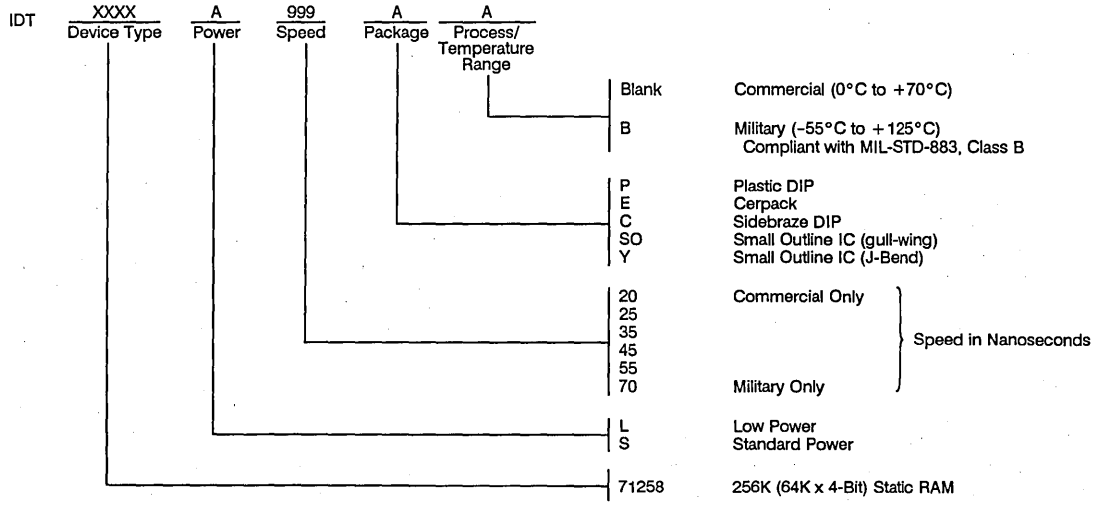
TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of t_{WP} or (t_{DW} + t_{WHZ}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}.

ORDERING INFORMATION



4

Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (64K x 4-BIT)

Separate Data Inputs and Outputs

PRELIMINARY
IDT 71281S/L
IDT 71282S/L

FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55ns (max.)
- Low power consumption
  - IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin DIP, and 28-pin SOIC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

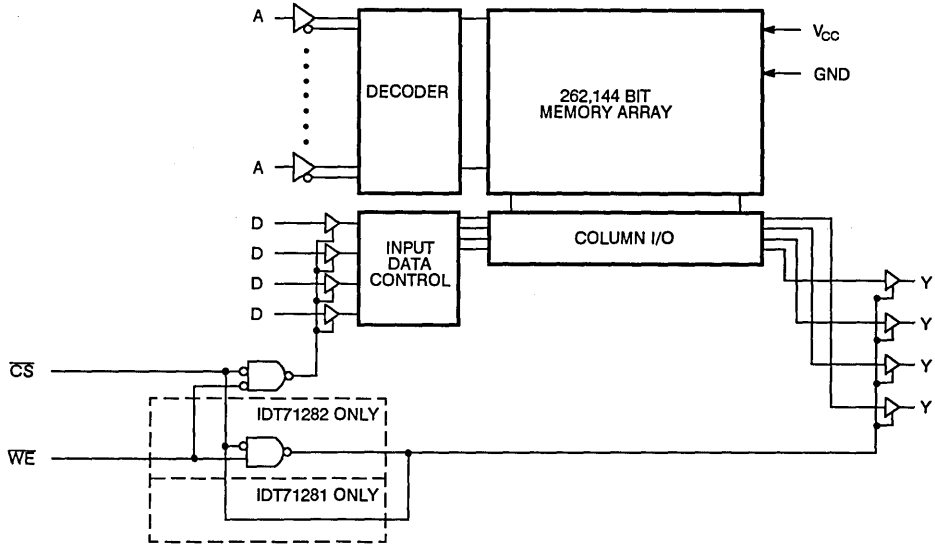
Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultra-low-power standby mode capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100µW operating off a 2V battery.

All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze and plastic DIPs, and SOICs providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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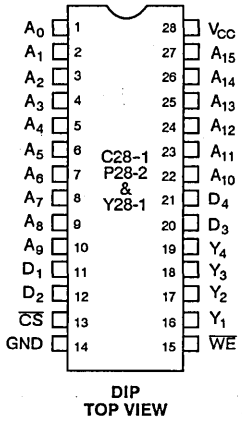
PIN CONFIGURATIONS

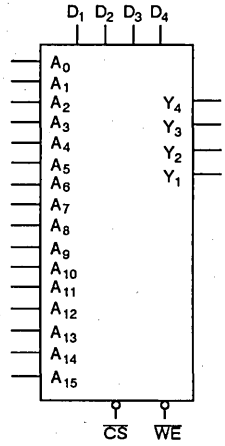


DIP
TOP VIEW

PIN NAMES

A_0-A_{15}	Address Inputs	D_1-D_4	$DATA_{IN}$
$\overline{CS}$	Chip Select	Y_1-Y_4	$DATA_{OUT}$
$\overline{WE}$	Write Enable	GND	Ground
V_{CC}	Power		

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS (for all speeds)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT71281/2S MIN.	IDT71281/2S TYP.(1)	IDT71281/2S MAX.	IDT71281/2L MIN.	IDT71281/2L TYP.(1)	IDT71281/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	71281/2S20 71281/2L20 COM'L.	71281/2S20 71281/2L20 MIL.	71281/2S25(2) 71281/2L25(2) COM'L.	71281/2S25(2) 71281/2L25(2) MIL.	71281/2S35 71281/2L35 COM'L.	71281/2S35 71281/2L35 MIL.	71281/2S45 71281/2L45 COM'L.	71281/2S45 71281/2L45 MIL.	71281/2S55 71281/2L55 COM'L.	71281/2S55 71281/2L55 MIL.	71281/2S70 71281/2L70 COM'L.	71281/2S70 71281/2L70 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	S	READ	70	–	60	70	50	60	50	60	50	60	–	60	mA
			WRITE (4)	140	–	130	140	120	130	120	130	120	130	–	130	
		L	READ	50	–	40	50	30	40	30	40	30	40	–	40	
			WRITE (4)	130	–	120	130	110	120	110	120	110	120	–	120	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	READ	170	–	160	170	150	160	150	160	150	160	–	160	mA
			WRITE (4)	180	–	170	180	160	170	160	170	160	170	–	170	
		L	READ	150	–	140	150	130	140	130	140	130	140	–	140	
			WRITE (4)	160	–	150	160	140	150	140	150	140	150	–	150	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., Outputs Open f = f_{MAX}(2)	S		35	–	35	35	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0(2)	S		30	–	30	35	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that, in most systems, the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

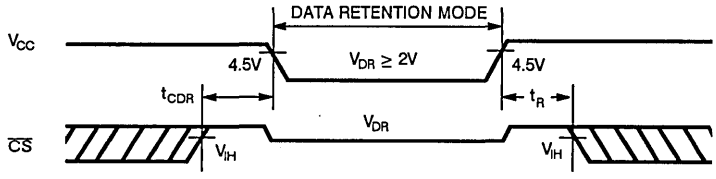
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

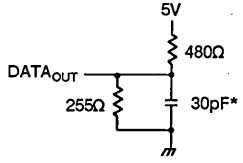


Figure 1. Output Load

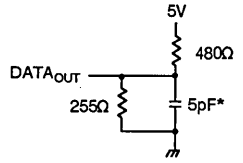


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

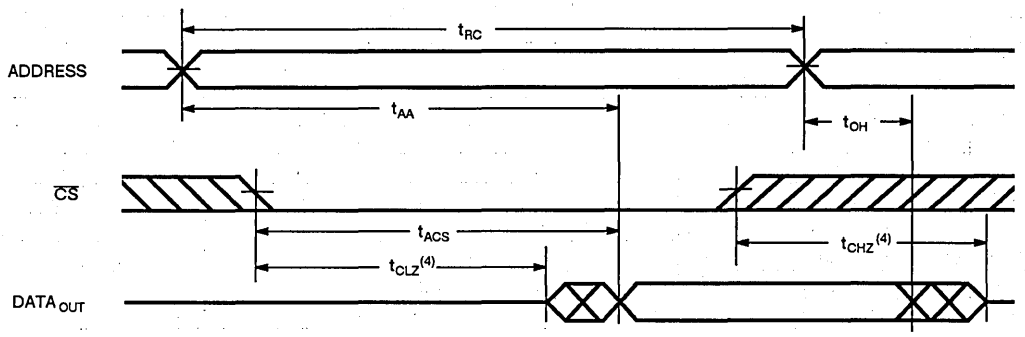
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71281/2S20[1] 71281/2L20[1] MIN.	MAX.	71281/2S25[5] 71281/2L25[5] MIN.	MAX.	71281/2S35 71281/2L35 MIN.	MAX.	71281/2S45 71281/2L45 MIN.	MAX.	71281/2S55 71281/2L55 MIN.	MAX.	71281/2S70[2] 71281/2L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time[3]	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}	Chip Select to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Select to Output in High Z[4]	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[4]	–	20	–	25	–	35	–	45	–	55	–	70	ns

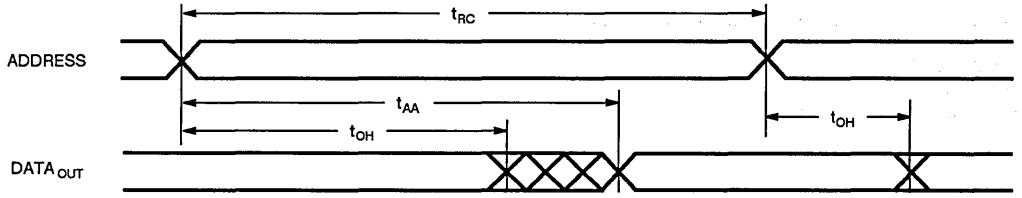
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data for military devices only.

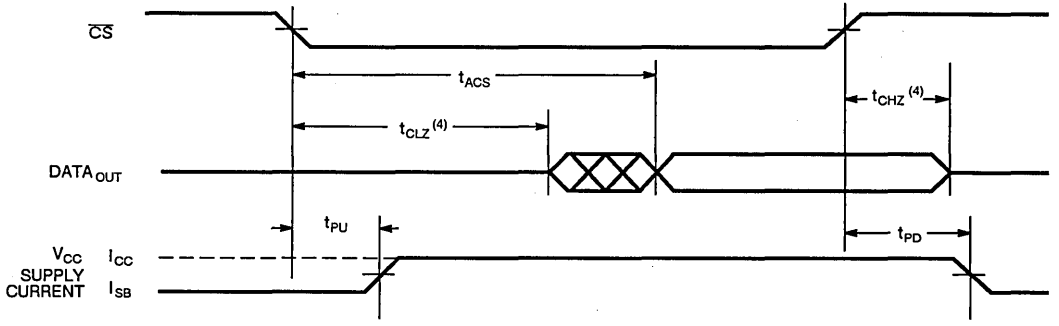
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2]



TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

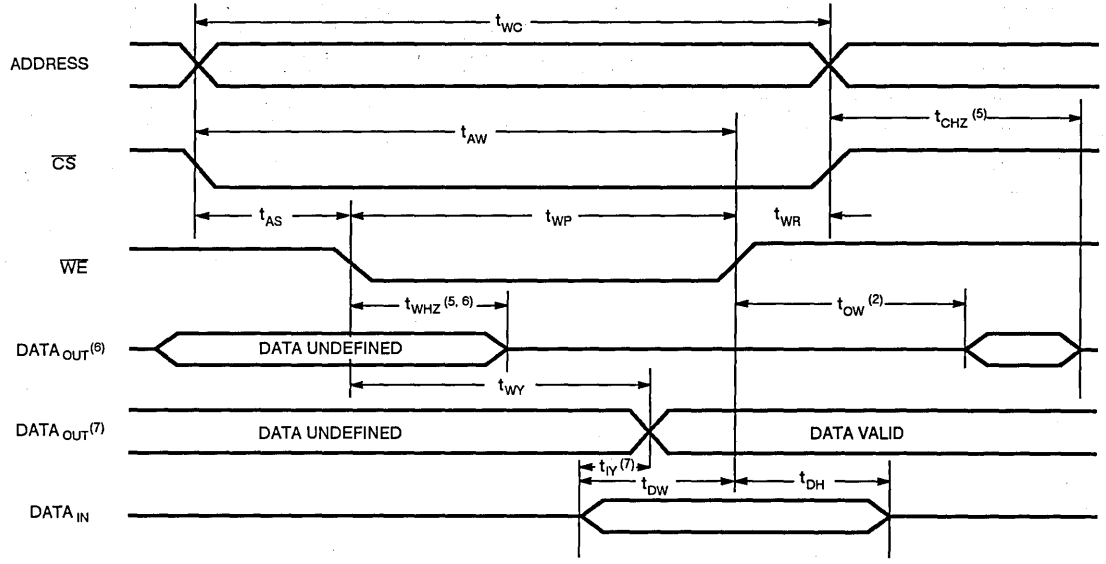
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	71281/2S20[1] 71281/2L20[1]		71281/2S25[7] 71281/2L25[7]		71281/2S35 71281/2L35		71281/2S45 71281/2L45		71281/2S55 71281/2L55		71281/2S70[2] 71281/2L70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write [3]	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z [4, 6]	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write [4, 6]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Data Valid to Output Valid [4, 5]	–	20	–	20	–	30	–	35	–	40	–	45	ns
t_{WY}	Write Enable to Output Valid [4, 5]	–	20	–	20	–	30	–	35	–	40	–	45	ns

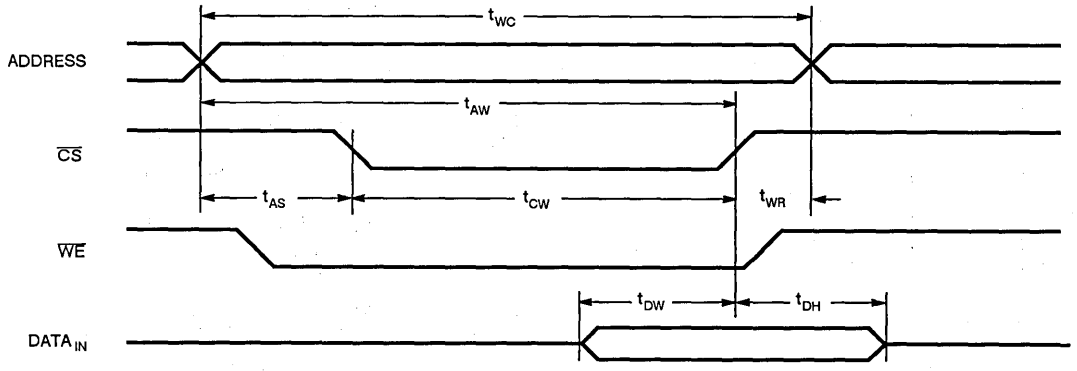
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. For IDT71281S/L only.
6. For IDT71282S/L only.
7. Preliminary data for military devices only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 4]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state (IDT71282 only).
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. IDT71282 only.
7. IDT71281 only.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write (1)	L	L	D_{IN}	Active
Write (2)	L	L	High Z	Active

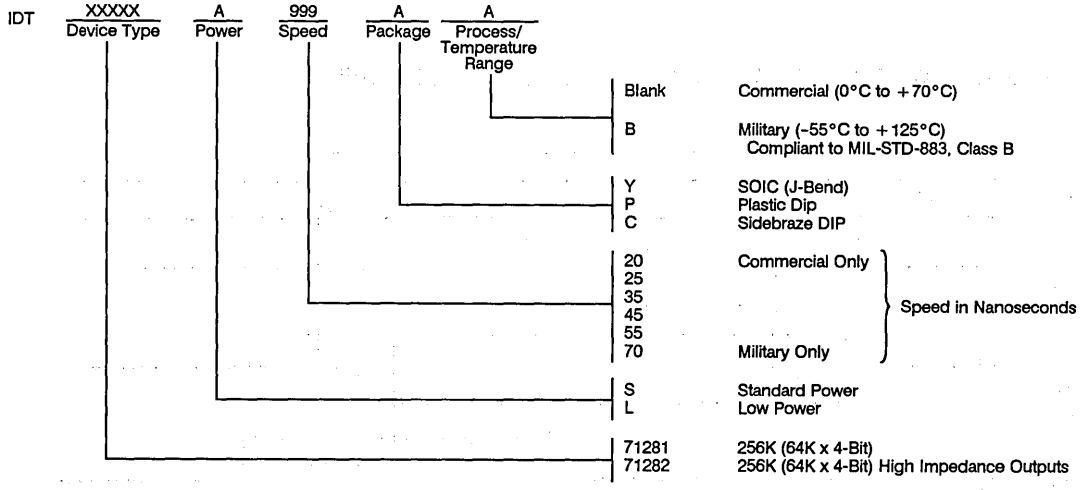
NOTES:
1. For IDT71281 only.
2. For IDT71282 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K x 8-BIT)

IDT 6116SA
IDT 6116LA

4

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed
  - Military: 25/30/35/45/55/70/90/120/150ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low-power operation
  - IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation—2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

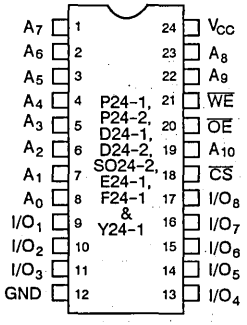
Access times as fast as 15ns are available with maximum power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK and flatpack, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

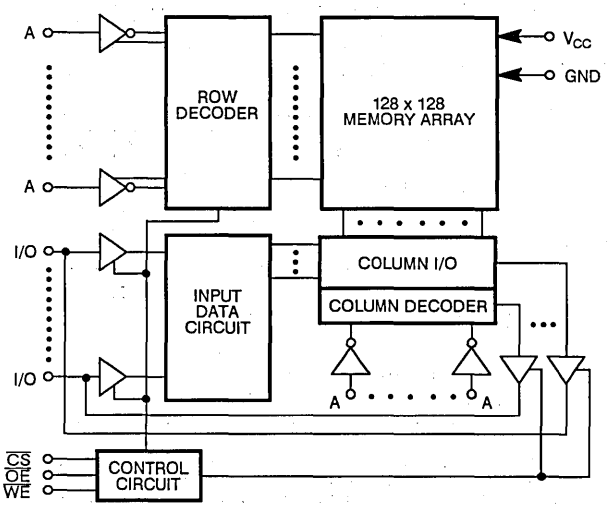
Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



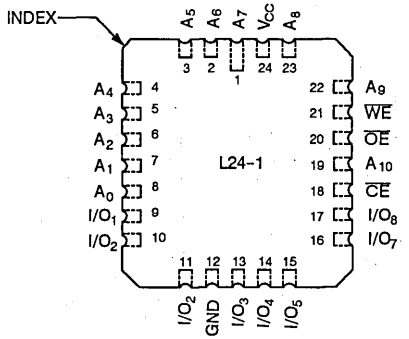
DIP/SOIC/FLATPACK/CERPACK
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM

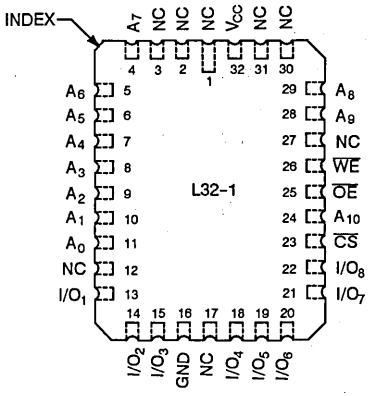


CEMOS is a trademark of Integrated Device Technology, Inc.

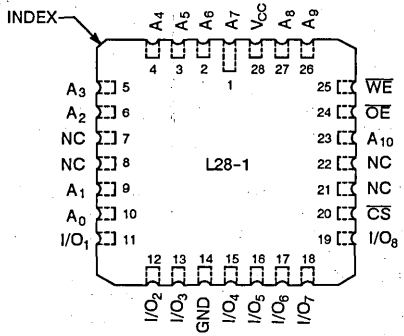
PIN CONFIGURATIONS



24-PIN LCC
TOP VIEW

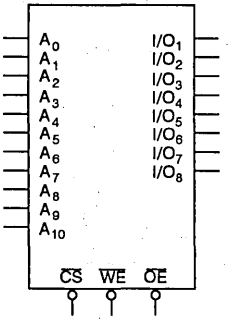


32-PIN LCC
TOP VIEW



28-PIN LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0- A_{10}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V
C_L	Output Load	–	–	30	pF

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116SA MIN.	IDT6116SA TYP.(1)	IDT6116SA MAX.	IDT6116LA MIN.	IDT6116LA TYP.(1)	IDT6116LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6116SA15(2)/19(2)/20(2) 6116LA15(2)/19(2)/20(2) COM'L.	6116SA15(2)/19(2)/20(2) 6116LA15(2)/19(2)/20(2) MIL.	6116SA25/30 6116LA25/30 COM'L.	6116SA25/30 6116LA25/30 MIL.	6116SA35 6116LA35 COM'L.	6116SA35 6116LA35 MIL.	6116SA45/55 6116LA45/55 COM'L.	6116SA45/55 6116LA45/55 MIL.	6116SA70/90 6116LA70/90 COM'L.	6116SA70/90 6116LA70/90 MIL.	6116SA120/150(3) 6116LA120/150(3) COM'L.	6116SA120/150(3) 6116LA120/150(3) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	125/110	–	100/80	110	80	90	80/–	90	–	90	–	90	mA
		LA	115/100	–	90/75	105	75	85	75/–	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (4)	SA	150/130	–	120/110	135	100	115	100/–	100	–	100	–	100/90	mA
		LA	140/120	–	110/105	125	95	105	90/–	95/90	–	90/85	–	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX} (4)	SA	40	–	40/35	45	25	35	25/–	25	–	25	–	25	mA
		LA	35	–	35/30	40	25	30	20/–	20	–	20/15	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	–	2	10	2	10	2/–	10	–	10	–	10	mA
		LA	0.1	–	0.1	0.9	0.1	0.9	0.1/–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f_{MAX} = $1/t_{RC}$

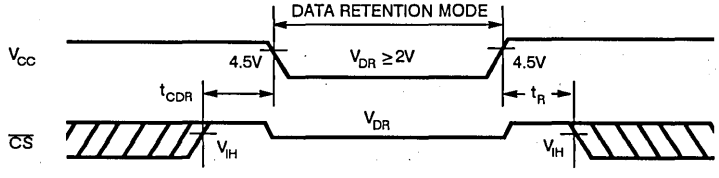
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.5	200	300	µA
			COM'L.	–	0.5	1.5	20	30	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

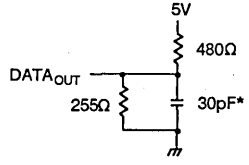


Figure 1. Output Load

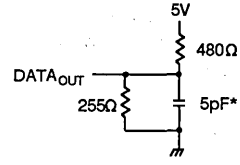


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

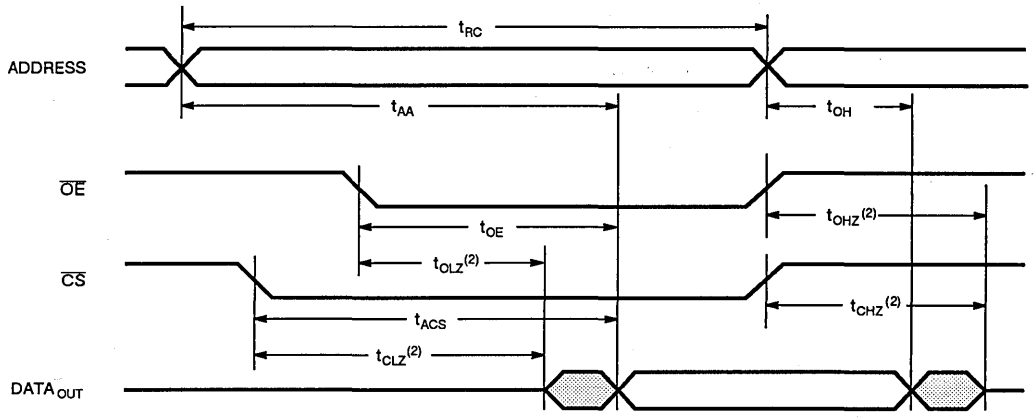
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6116SA15/19[1]/20[1] 6116LA15/19[1]/20[1] MIN.	MAX.	6116SA25/30 6116LA25/30 MIN.	MAX.	6116SA35/45 6116LA35/45 MIN.	MAX.	6116SA55[2] 6116LA55[2] MIN.	MAX.	6116SA70/90[2] 6116LA70/90[2] MIN.	MAX.	6116SA120/150[2] 6116LA120/150[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/19/20	—	25/30	—	35/45	—	55	—	70/90	—	120/150	—	ns
t_{AA}	Address Access Time	—	15/19/20	—	25/29	—	35/45	—	55	—	70/90	—	120/150	ns
t_{ACS}	Chip Select Access Time	—	15/20/20	—	25/30	—	35/45	—	50	—	65/90	—	120/150	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	13/15	—	20/25	—	40	—	50/65	—	80/100	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	0	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	—	10/11/11	—	12/13	—	15/20	—	30	—	35/40	—	40	ns
t_{OHZ}	Output Disable to Output in High Z[3]	—	8/8/9	—	10/12	—	13/15	—	30	—	35/40	—	40	ns
t_{OH}	Output Hold from Address Change	3	—	5	—	5	—	5	—	5	—	5	—	ns

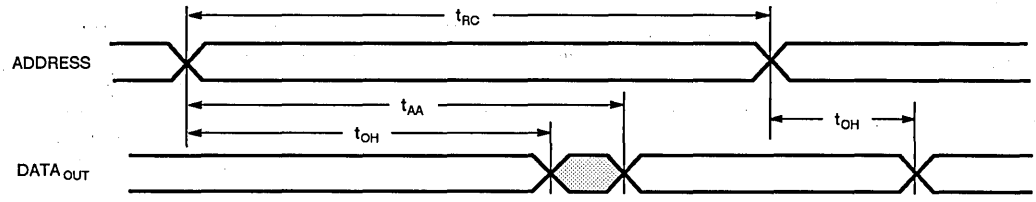
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1]

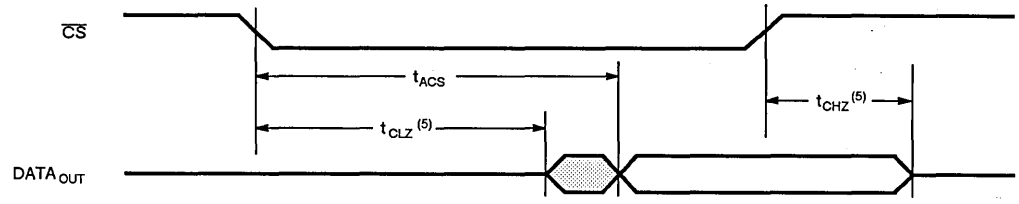


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

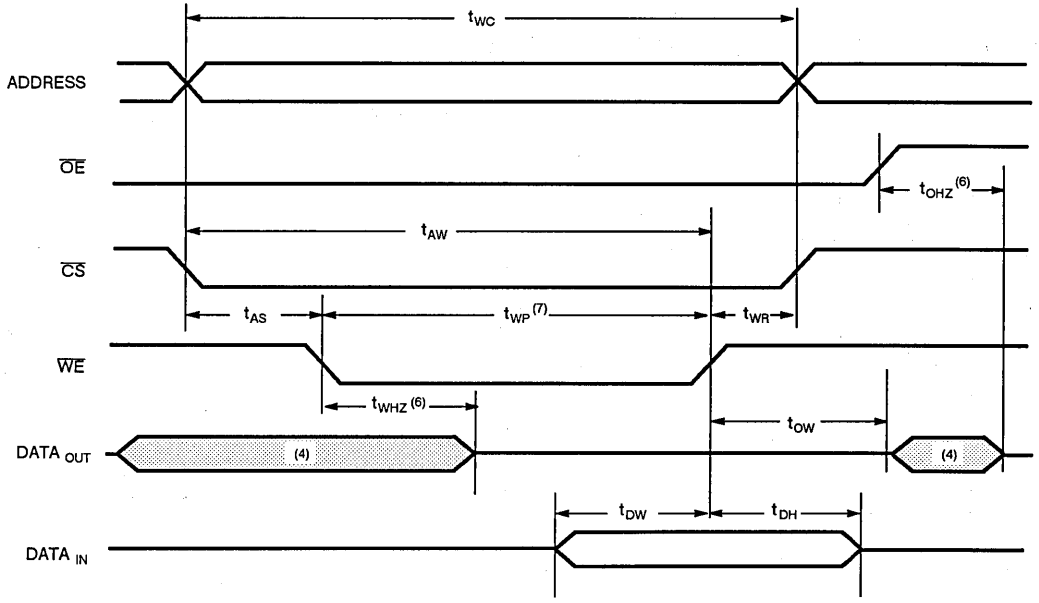
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

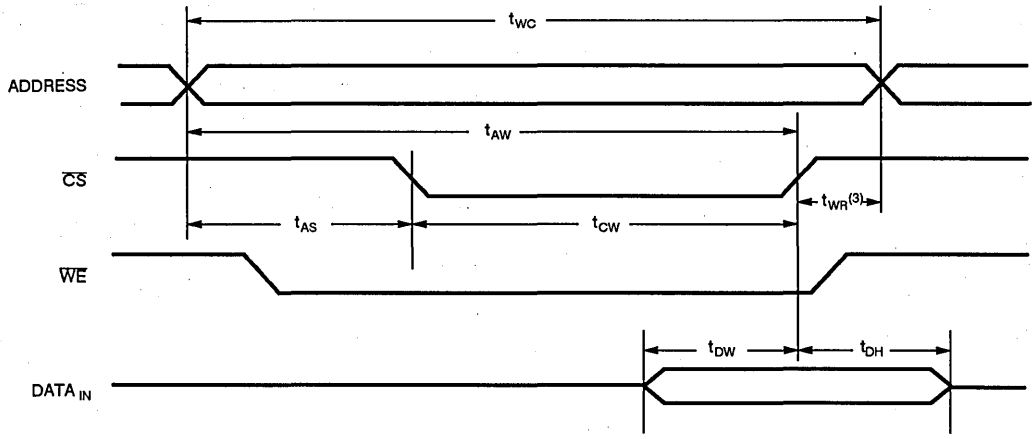
SYMBOL	PARAMETER	6116SA15/19[1]/20[1] 6116LA15/19[1]/20[1] MIN.	MAX.	6116SA25/30 6116LA25/30 MIN.	MAX.	6116SA35/45 6116LA35/45 MIN.	MAX.	6116SA55[2] 6116LA55[2] MIN.	MAX.	6116SA70/90[2] 6116LA70/90[2] MIN.	MAX.	6116SA120/150[2] 6116LA120/150[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	15/19/20	–	25/30	–	35/45	–	55	–	70/90	–	120/150	–	ns
t_{CW}	Chip Select to End of Write	13/15/15	–	17/20	–	25/30	–	40	–	40/55	–	70/90	–	ns
t_{AW}	Address Valid to End of Write	14/15/15	–	17/20	–	25/30	–	45	–	65/80	–	105/120	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	5	–	15	–	20	–	ns
t_{WP}	Write Pulse Width	12/12/15	–	15	–	20/25	–	40	–	40/55	–	70/90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8/9/9	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{WHZ}	Write to Output in High Z[3]	–	7/8/8	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{DW}	Data to Write Time Overlap	12	–	13/14	–	15/20	–	25	–	30	–	35/40	–	ns
t_{DH}	Data Hold from Write Time[4]	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OW}	Output Active from End of Write[3,4]	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]

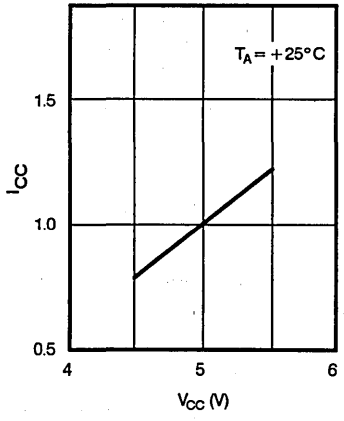


NOTES:

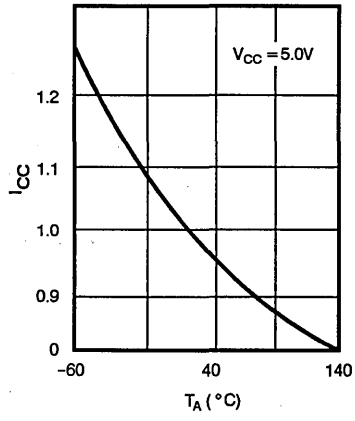
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

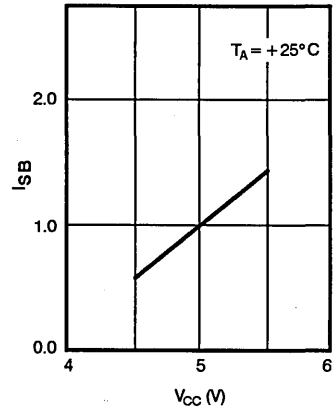
I_{CC} vs. Supply Voltage



I_{CC} vs. Temperature

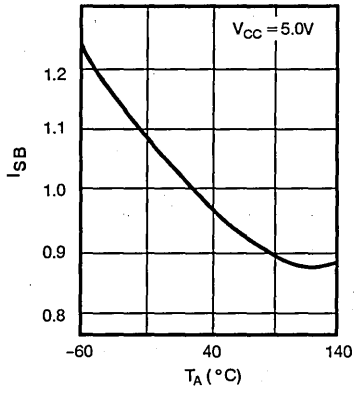


I_{SB} vs. Supply Voltage

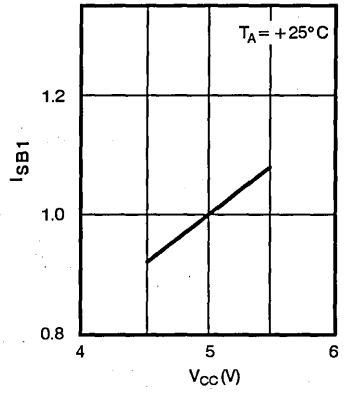


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

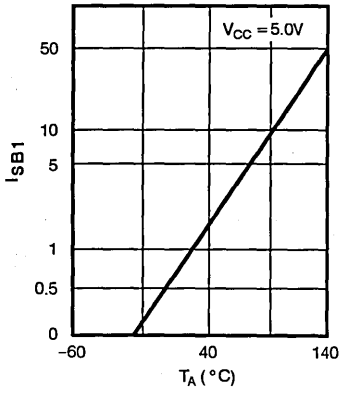
I_{SB} vs. Temperature



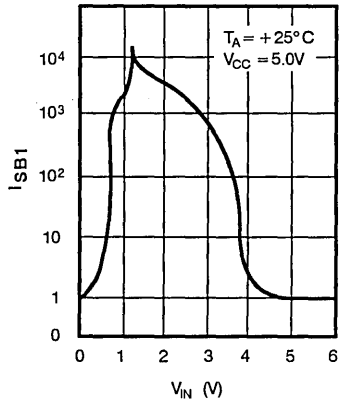
I_{SB1} vs. Supply Voltage



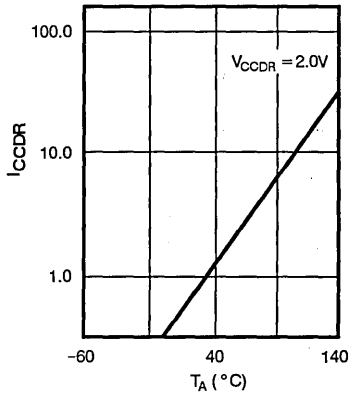
I_{SB1} vs. Temperature



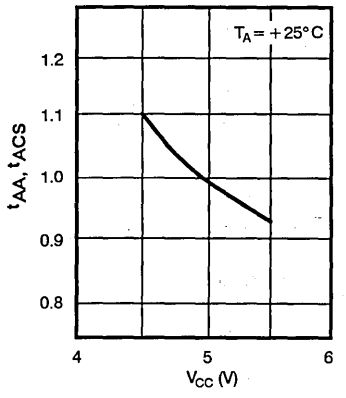
I_{SB1} vs. V_{IN}



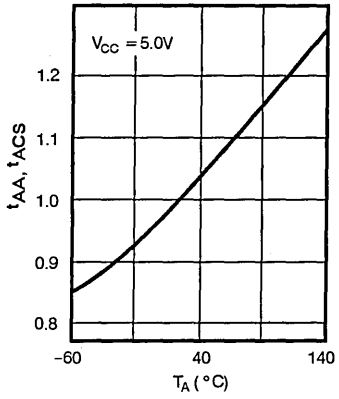
I_{CCDR} vs. Temperature



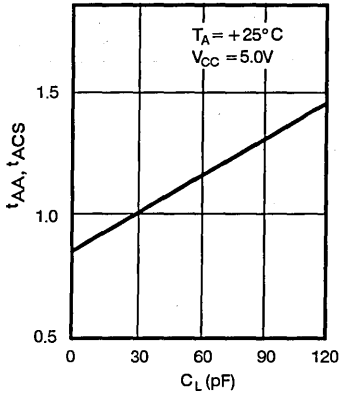
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High Z
Write	L	X	L	$DATA_{IN}$

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}= 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

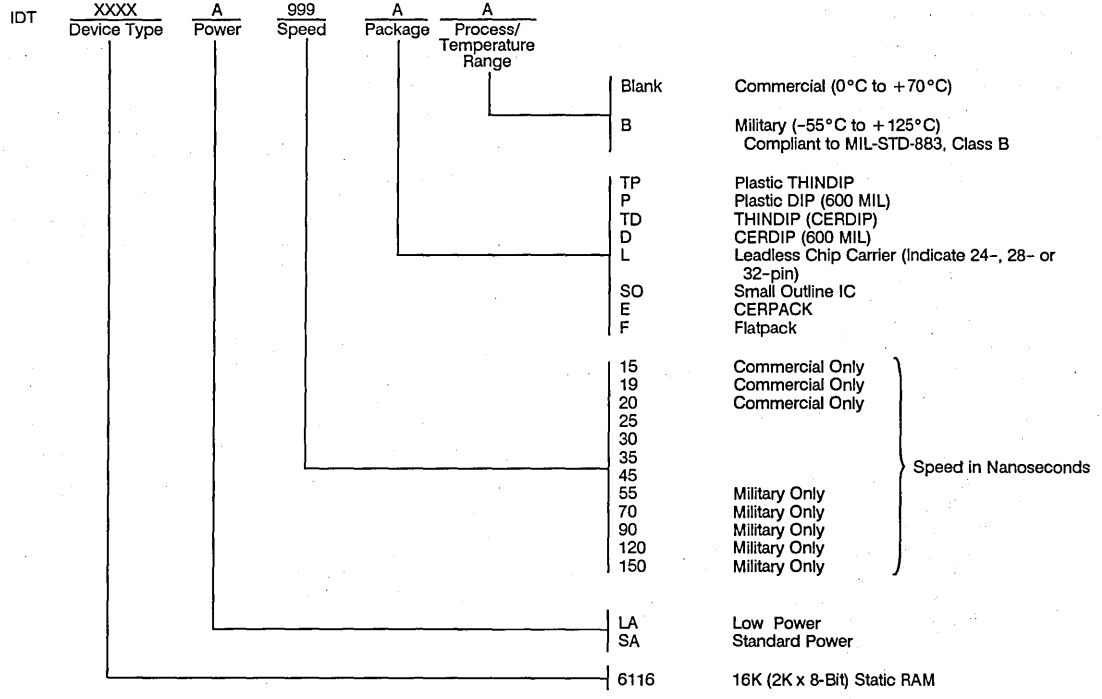
PINOUT CONFIGURATION
16K CMOS SRAM
IDT6116 (2K x 8)

FUNCTION	LOGIC SYMBOL	PIN NUMBER 24 DIP/ SOIC/ LCC/ FLATPACK	28 LCC	32 LCC
Address Line	A_7	1	1	4
Address Line	A_6	2	2	5
Address Line	A_5	3	3	6
Address Line	A_4	4	4	7
Address Line	A_3	5	5	8
Address Line	A_2	6	6	9
Address Line	A_1	7	9	10
Address Line	A_0	8	10	11
Input/Output	I/O_1	9	11	13
Input/Output	I/O_2	10	12	14
Input/Output	I/O_3	11	13	15
Power Ground	GND	12	14	16
Input/Output	I/O_4	13	15	18
Input/Output	I/O_5	14	16	19
Input/Output	I/O_6	15	17	20
Input/Output	I/O_7	16	18	21
Input/Output	I/O_8	17	19	22
Chip Select/ Data Retention	$\overline{CS}$	18	20	23
Address Line	A_{10}	19	23	24
Output Enable	$\overline{OE}$	20	24	25
Write Enable	$\overline{WE}$	21	25	26
Address Line	A_9	22	26	28
Address Line	A_8	23	27	29
Power Supply	V_{CC}	24	28	32

THERMAL RESISTANCE (Typical)

PACKAGE	PIN COUNT	θ_{JA}	θ_{JC}	UNIT
300 MIL PLASTIC DIP	24	54-58	28-32	°C/ WATT
600 MIL PLASTIC DIP	24	53-56	25-30	
300 MIL CERDIP	24	48-52	24-28	
600 MIL CERDIP	24	50-55	17-25	
FLATPACK	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC	24	45-70	25-30	

ORDERING INFORMATION



4

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT 7164S
IDT 7164L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select access time
  - Military: 25/30/35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7164S
    Active: 300mW (typ.)
    Standby: 100µw (typ.)
  - IDT7164L
    Active: 250mW (typ.)
    Standby: 30µw (typ.)
- Battery backup operation—2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Available in standard 28-pin DIP (600 mil), 28-pin THINDIP (300 mil), 28-pin LCC, 32-pin LCC and PLCC and 28-pin SOIC
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function. Refer to Section 2/page 2-2.

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. Timing parameters have been specified to meet the demands of the fastest IDT79R3000 RISC processors.

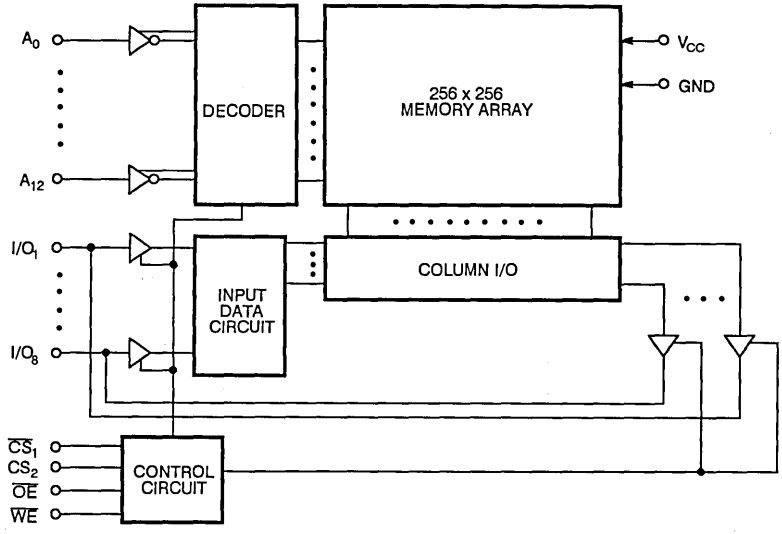
Address access times as fast as 19ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin, 300 mil THINDIP; 28-pin, 600 mil DIP; 32-pin LCC and PLCC and 28-pin LCC and SOIC (gull-wing and J-bend), providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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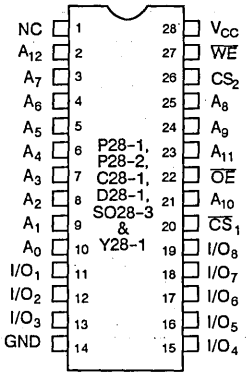
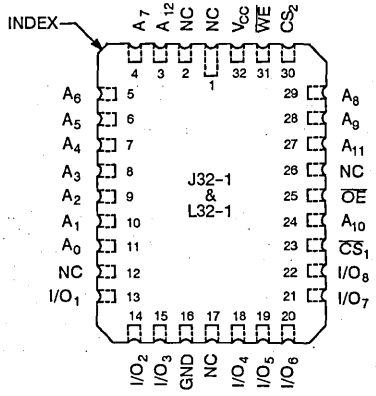
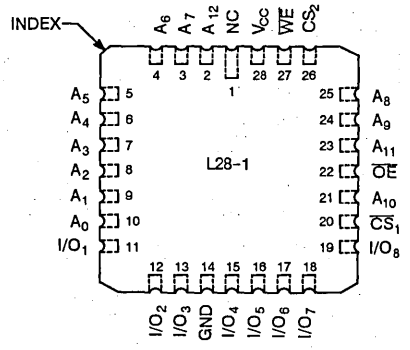
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

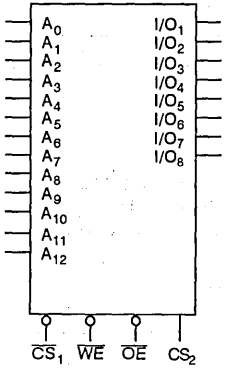


32-PIN LCC/PLCC
TOP VIEW



28-PIN LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0- A_{12}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS_1}$	Chip Select	GND	Ground
CS_2	Chip Select	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7164S MIN.	IDT7164S TYP.(1)	IDT7164S MAX.	IDT7164L MIN.	IDT7164L TYP.(1)	IDT7164L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7164S19/20 7164L20 COM'L.	7164S19/20 7164L20 MIL.	7164S25(4) 7164L25(4) COM'L.	7164S25(4) 7164L25(4) MIL.	7164S30 7164L30 COM'L.	7164S30 7164L30 MIL.	7164S35 7164L35 COM'L.	7164S35 7164L35 MIL.	7164S45 7164L45 COM'L.	7164S45 7164L45 MIL.	7164S55 7164L55 COM'L.	7164S55 7164L55 MIL.	7164S70 7164L70 COM'L.	7164S70 7164L70 MIL.	7164S85(2) 7164L85(2) COM'L.	7164S85(2) 7164L85(2) MIL.	UNIT
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = 0 (3)	S	100	–	90	110	90	100	90	100	90	100	–	100	–	100	–	100	mA
		L	90	–	80	100	80	90	80	90	80	90	–	90	–	90	–	90	
I_{CC2}	Dynamic Operating Current, $\overline{CS_1}$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = f_{MAX} (3)	S	190	–	170	190	160	170	150	160	150	160	–	160	–	160	–	160	mA
		L	170	–	150	170	140	150	130	140	120	130	–	125	–	120	–	120	
I_{SB}	Standby Power Supply Current (TTL Level), f = f_{MAX} (3), $\overline{CS_1}$ ≥ V_{IH}, or CS_2 ≥ V_{IL}, V_{CC} = Max., Outputs Open	S	20	–	20	20	20	20	20	20	20	20	–	20	–	20	–	20	mA
		L	3	–	3	5	3	5	3	5	3	5	–	5	–	5	–	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) f = 0 (3) 1. $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC} 2. CS_2 ≤ V_{LC}, V_{CC} = Max.	S	15	–	15	20	15	20	15	20	15	20	–	20	–	20	–	20	mA
		L	0.2	–	0.2	1.0	0.2	1.0	0.2	1.0	0.2	1.0	–	1.0	–	1.0	–	1.0	

NOTES:

1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Military values are preliminary only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

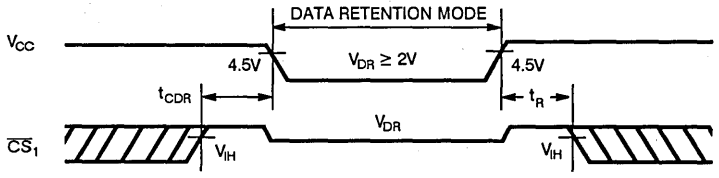
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	1. $\overline{CS}_1 \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	
t_{CDR}	Chip Deselect to Data Retention Time			0	–		–		ns
t_R	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

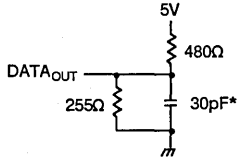


Figure 1. Output Load

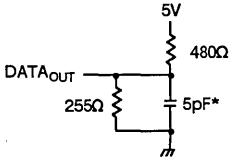


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig.

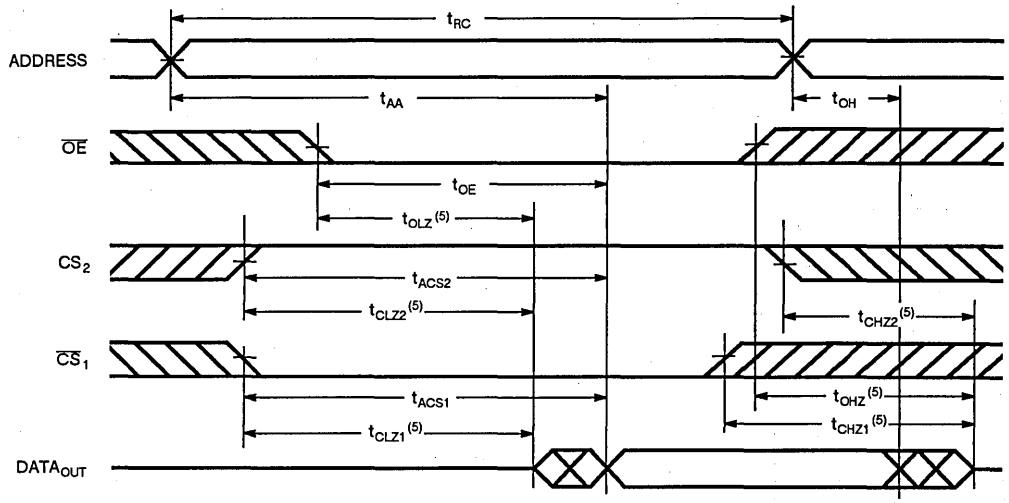
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S19/20[1] 7164L20[1] MIN.	MAX.	7164S25 7164L25 MIN.	MAX.	7164S30 7164L30 MIN.	MAX.	7164S35 7164L35 MIN.	MAX.	7164S45 7164L45 MIN.	MAX.	7164S55[2] 7164L55[2] MIN.	MAX.	7164S70[2] 7164L70[2] MIN.	MAX.	7164S85[2] 7164L85[2] MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	19/20	–	25	–	29	–	35	–	45	–	55	–	70	–	85	ns
t_{ACS1}	Chip Select-1 Access Time[3]	–	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	ns
t_{ACS2}	Chip Select-2 Access Time[3]	–	25	–	30	–	35	–	40	–	45	–	55	–	70	–	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	12	–	15	–	18	–	25	–	30	–	35	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	3	–	3	–	3	–	3	–	3	–	3	–	3	–	3	–	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z[4]	–	9	–	13	–	13	–	15	–	20	–	25	–	30	–	35	ns
t_{OHZ}	Output Disable to Output in High Z[4]	–	8	–	10	–	12	–	15	–	20	–	25	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time[4]	–	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	ns

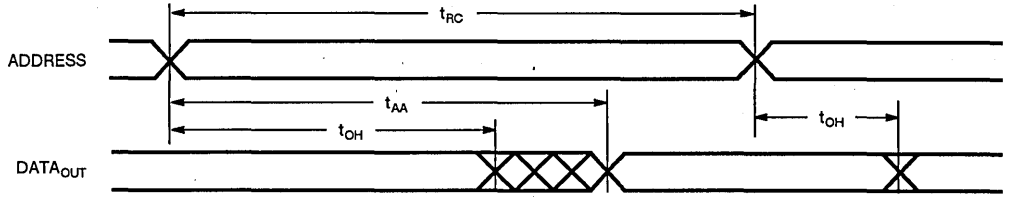
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter guaranteed but not tested.

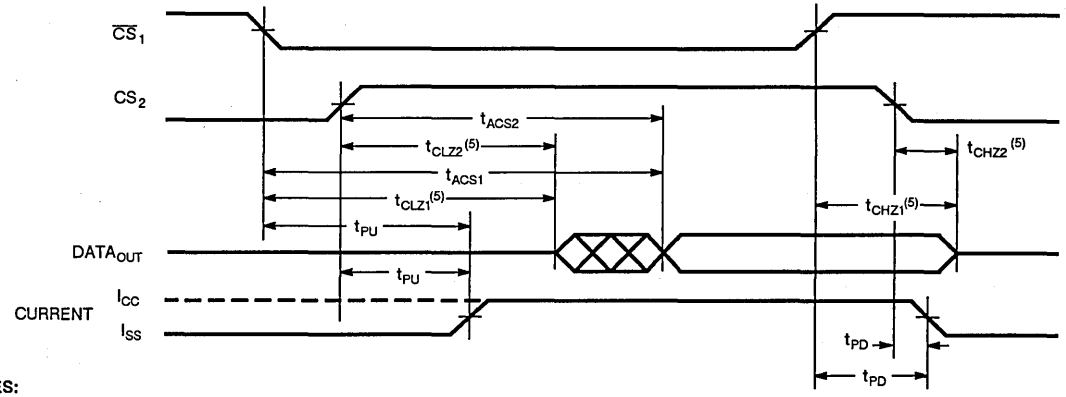
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

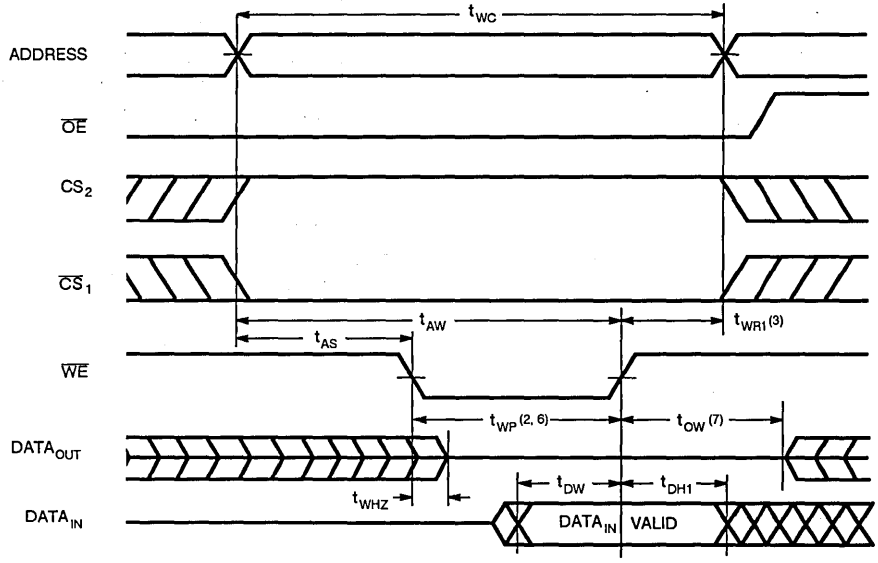
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S19/20[1] 7164L20[1] MIN.	MAX.	7164S25 7164L25 MIN.	MAX.	7164S30 7164L30 MIN.	MAX.	7164S35 7164L35 MIN.	MAX.	7164S45 7164L45 MIN.	MAX.	7164S55[2] 7164L55[2] MIN.	MAX.	7164S70[2] 7164L70[2] MIN.	MAX.	7164S85[2] 7164L85[2] MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	–	ns
$t_{CW1,2}$	Chip Select to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	21	–	23	–	25	–	25	–	50	–	60	–	75	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write Enable to Output High Z[3]	–	8	–	10	–	12	–	14	–	18	–	25	–	30	–	35	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	13	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns

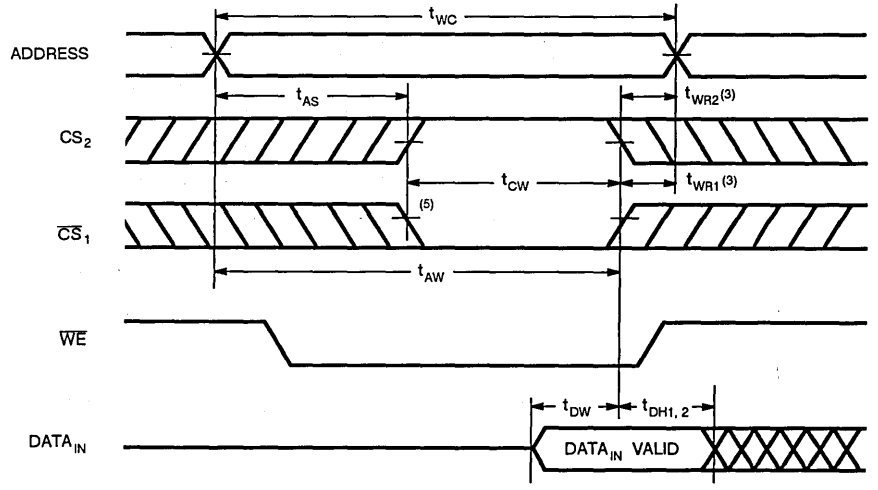
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1]



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WR}
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ±200mV from steady state.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

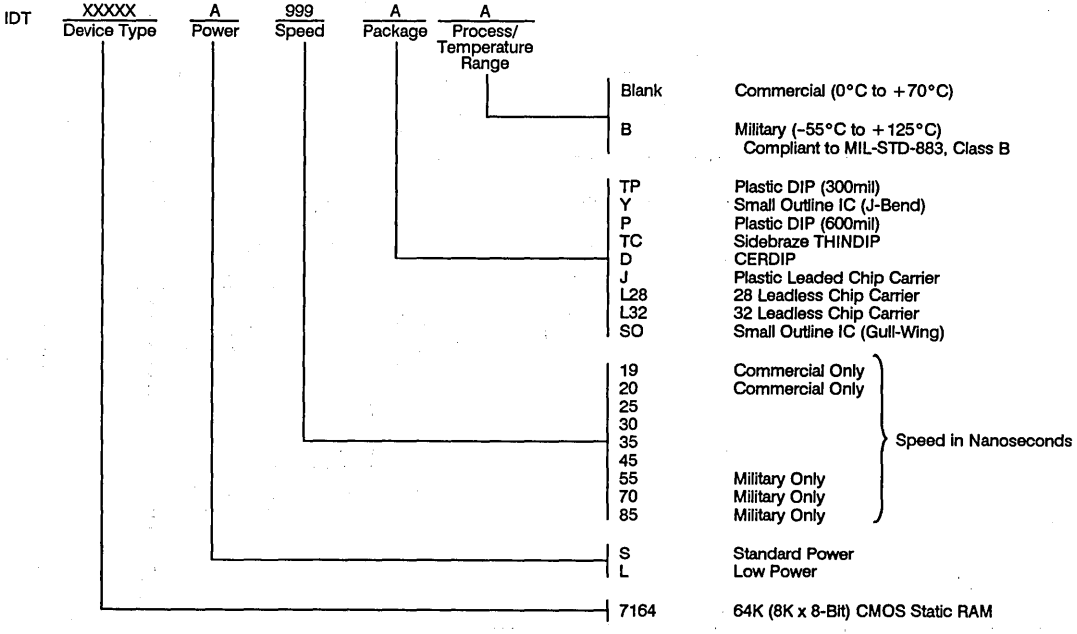
NOTE:
1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	I/O	MODE
X	H	X	X	HIGH Z	Standby (I_{SB})
X	X	L	X	HIGH Z	Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	HIGH Z	Standby (I_{SB1})
X	X	V_{LC}	X	HIGH Z	Standby (I_{SB1})
H	L	H	H	HIGH Z	Output disable
H	L	H	L	D_{OUT}	Read
L	L	H	X	D_{IN}	Write

NOTE:
1. CS_2 will power-down $\overline{CS}_1$, but $\overline{CS}_1$ will not power-down CS_2.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

IDT 7165S
IDT 7165L

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x t_{AA})
- High-speed address access time
  - Military: 25/30/35/45/55ns (max.)
  - Commercial: 20/25/30/35/45/55ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - Military: 12/15/20/25/30/35ns (max.)
  - Commercial: 10/12/15/20/25/30ns (max.)
- Low-power operation
  - IDT7165S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT7165L
    Active:250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin, 600 mil DIP, 300 mil DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{RESET}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

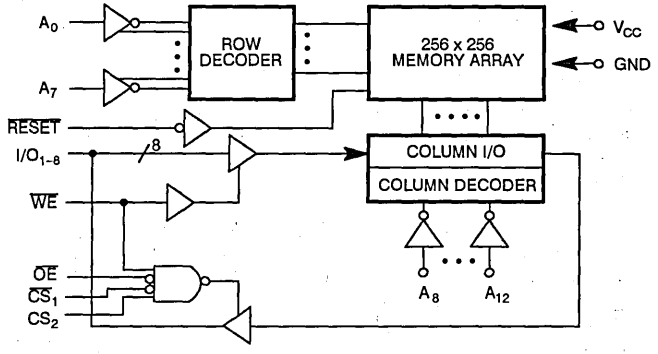
This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 20ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS_2 goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating from a 2V battery.

All inputs and outputs of the IDT7165 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, so no clocks or refreshing operation is required.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin gull-wing & J-bend SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

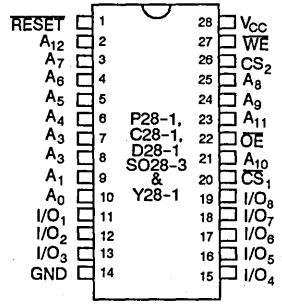
FUNCTIONAL BLOCK DIAGRAM



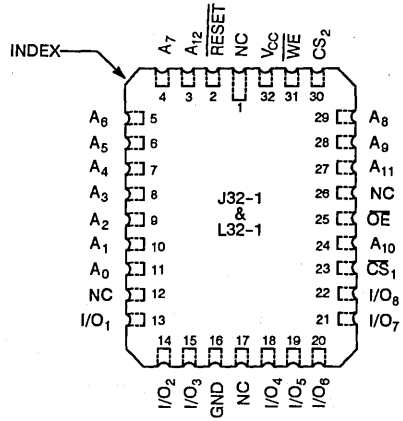
CEMOS is a trademark of Integrated Device Technology, Inc.

DSC-1021/-1

PIN CONFIGURATIONS

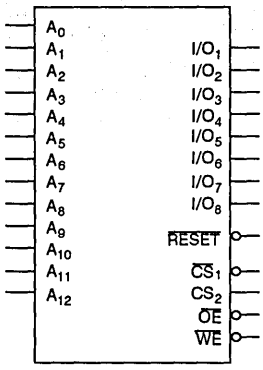


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}_1$, CS_2	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage (1)	2.2	–	6.0	V
V_{IHR}	$\overline{RESET}$ Input High Voltage	2.5(2)	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(3)	–	0.8	V

NOTES:

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7165S MIN.	IDT7165S TYP.(1)	IDT7165S MAX.	IDT7165L MIN.	IDT7165L TYP.(1)	IDT7165L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	7165S/L20 COM'L.	7165S/L20 MIL.	7165S/L25(3) COM'L.	7165S/L25(3) MIL.	7165S/L30 COM'L.	7165S/L30 MIL.	7165S/L35 COM'L.	7165S/L35 MIL.	7165S/L45 COM'L.	7165S/L45 MIL.	7165S/L55 COM'L.	7165S/L55 MIL.	UNIT
I_{CC1} (2)	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	S	100	–	90	110	90	100	90	100	90	100	90	100	mA
		L	90	–	80	100	80	90	80	90	80	90	80	90	
I_{CC2} (2)	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	S	190	–	170	190	160	170	150	160	150	160	150	160	mA
		L	170	–	150	170	140	150	130	140	120	130	115	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_1 \geq V_{IH}$, $CS_2 \leq V_{IL}$ and $\overline{RESET} \geq V_{IH}$ V_{CC} = Max., Outputs Open	S	20	–	20	20	20	20	20	20	20	20	20	20	mA
		L	3	–	3	5	3	5	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$, V_{CC} = Max.	S	15	–	15	20	15	20	15	20	15	20	15	20	mA
		L	0.2	–	0.2	1.0	0.2	1.0	0.2	1.0	0.2	1.0	0.2	1.0	

NOTES:
1. All values are maximum guaranteed values.
2. CS_2 = V_{IH}
3. Military values are preliminary only.

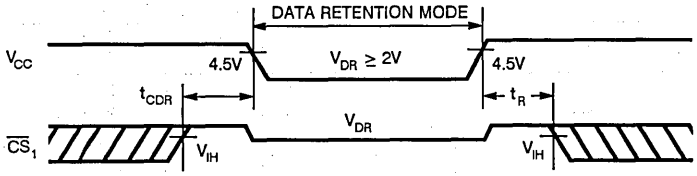
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

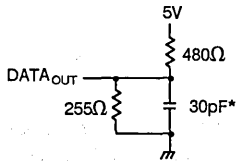


Figure 1. Output Load

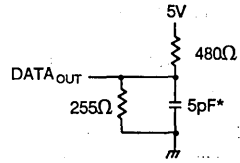


Figure 2. Output Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, t_{WHZ})

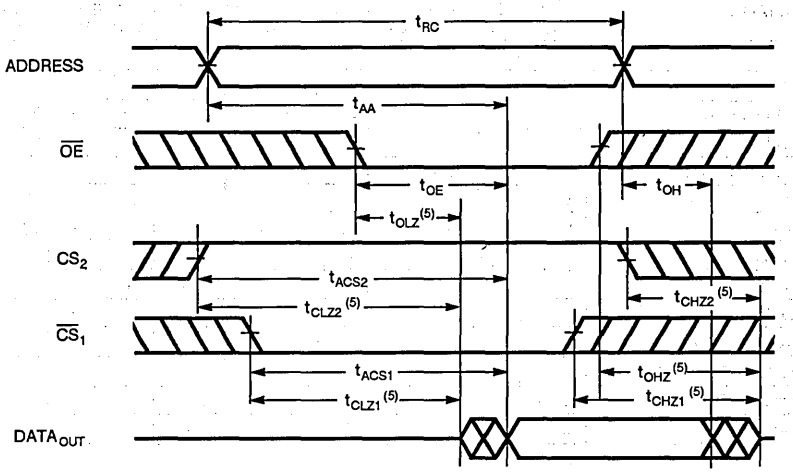
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

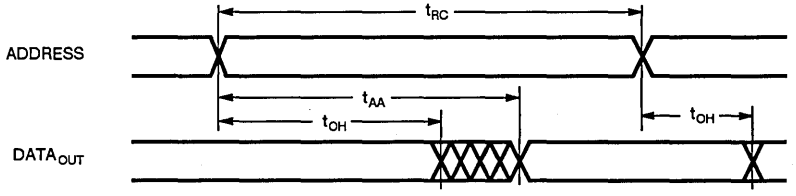
SYMBOL	PARAMETER	7165S20[1] 7165L20[1] MIN.	MAX.	7165S25 7165L25 MIN.	MAX.	7165S30 7165L30 MIN.	MAX.	7165S35 7165L35 MIN.	MAX.	7165S45 7165L45 MIN.	MAX.	7165S55 7165L55 MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS1}	Chip Select-1 Access Time[2]	–	10	–	12	–	15	–	20	–	25	–	30	ns
t_{ACS2}	Chip Select-2 Access Time[2]	–	25	–	30	–	35	–	40	–	45	–	55	ns
t_{CLZ1}	Chip Select-1 to Output in Low Z[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{CLZ2}	Chip Select-2 to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	12	–	15	–	20	–	25	–	30	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	3	–	3	–	3	–	3	–	3	–	3	–	ns
t_{CHZ1}	Chip Select-1 to Output in High Z[3]	–	9	–	13	–	13	–	15	–	20	–	25	ns
t_{CHZ2}	Chip Select-2 to Output in High Z[3]	–	9	–	13	–	13	–	15	–	20	–	25	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8	–	12	–	14	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time[3]	–	20	–	25	–	30	–	35	–	45	–	55	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. This parameter is guaranteed but not tested.

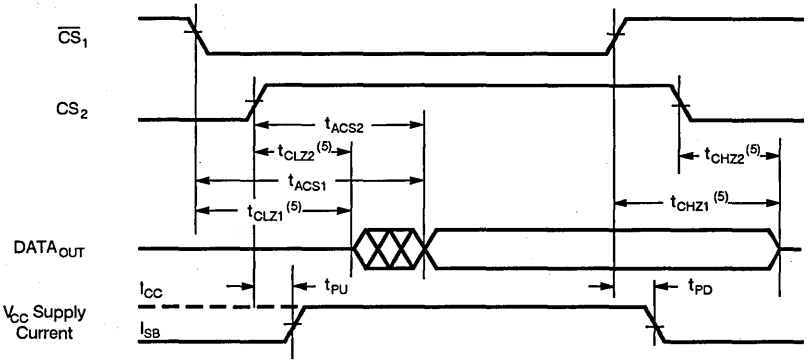
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Addresses valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

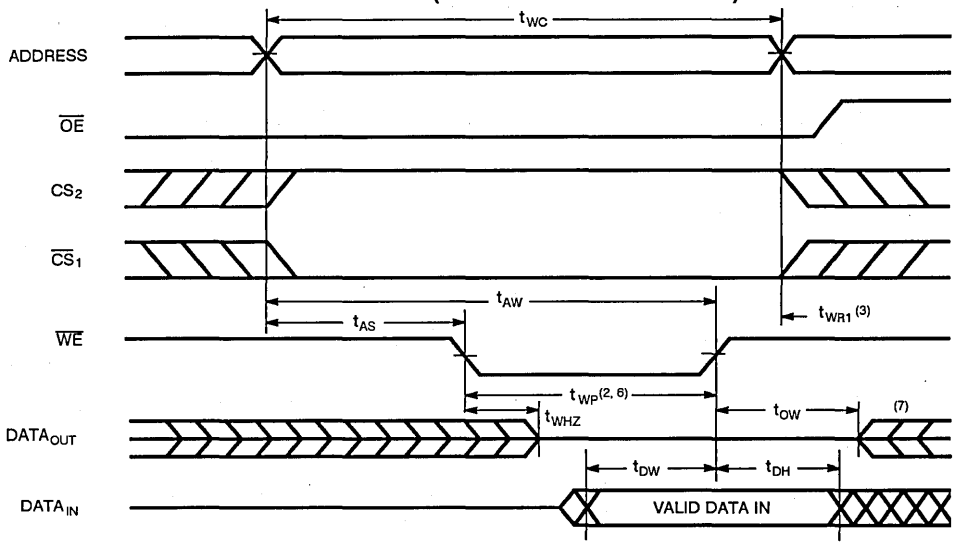
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7165S20[1] 7165L20[1] MIN.	MAX.	7165S25 7165L25 MIN.	MAX.	7165S30 7165L30 MIN.	MAX.	7165S35 7165L35 MIN.	MAX.	7165S45 7165L45 MIN.	MAX.	7165S55 7165L55 MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{CW1}	Chip Select-1 to End of Write	12	–	15	–	20	–	20	–	25	–	30	–	ns
t_{CW2}	Chip Select-2 to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	ns
t_{AW}	Address Valid to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	ns
t_{AS}	Address Setup Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	21	–	23	–	25	–	25	–	50	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write Enable to Output In High Z[2]	–	8	–	10	–	12	–	14	–	18	–	25	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	13	–	15	–	20	–	25	–	ns
t_{DH1}	Data Hold From Write Time ($\overline{CS_1}$)	3	–	3	–	3	–	3	–	3	–	3	–	ns
t_{DH2}	Data Hold From Write Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write[2]	5	–	5	–	5	–	5	–	5	–	5	–	ns

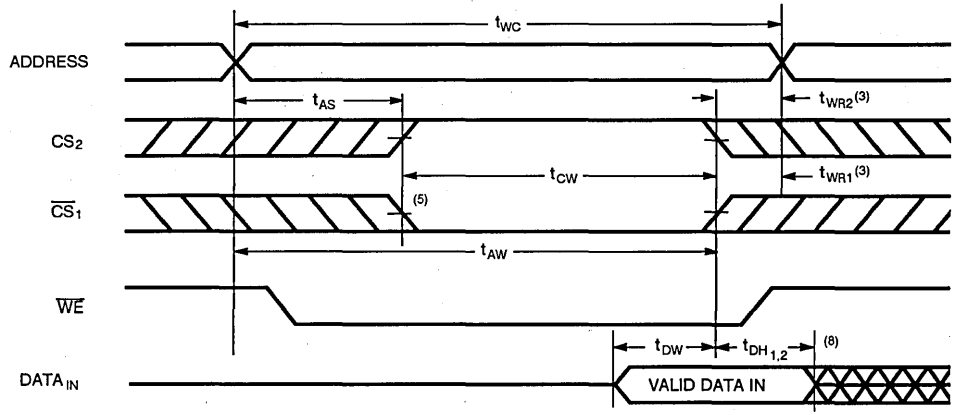
NOTES:

1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1] ($\overline{WE}$ CONTROLLED TIMING)



TIMING WAVEFORM OF WRITE CYCLE NO. 2[1] ($\overline{CS}$ CONTROLLED TIMING)



NOTES:

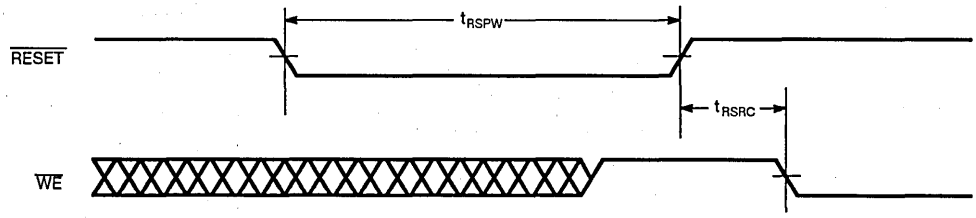
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requiremnt does not apply and the write pulse can be as short as the specified t_{WP}.
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7165S20[1] 7165L20[1] MIN.	MAX.	7165S25 7165L25 MIN.	MAX.	7165S30 7165L30 MIN.	MAX.	7165S35 7165L35 MIN.	MAX.	7165S45 7165L45 MIN.	MAX.	7165S55 7165L55 MIN.	MAX.	UNIT
RESET														
t_{RSPW}	Reset Pulse Width [2]	45	–	50	–	55	–	65	–	80	–	100	–	ns
t_{RSRC}	Reset High to $\overline{WE}$ Low	5	–	5	–	5	–	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.

RESET TIMING



CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

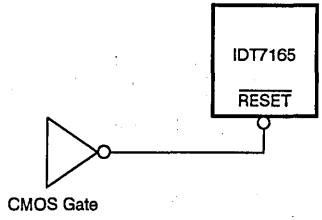
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE

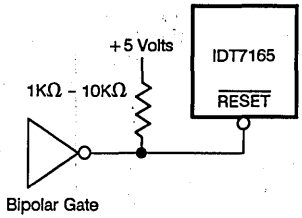
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{RESET}$	I/O	FUNCTION
X	X	X	X	L	–	Reset all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down[1]
X	V_{HC}	X	X	H	Z	Deselect chip
X	X	V_{LC}	X	V_{HC}	Z	CMOS deselect power down [1]
H	L	H	H	H	Z	Output disable
H	L	H	L	H	D_{OUT}	Read
L	L	H	X	H	D_{IN}	Write

NOTE:
1. CS_2 will power down $\overline{CS_1}$, but $\overline{CS_1}$ will not power down CS_2.



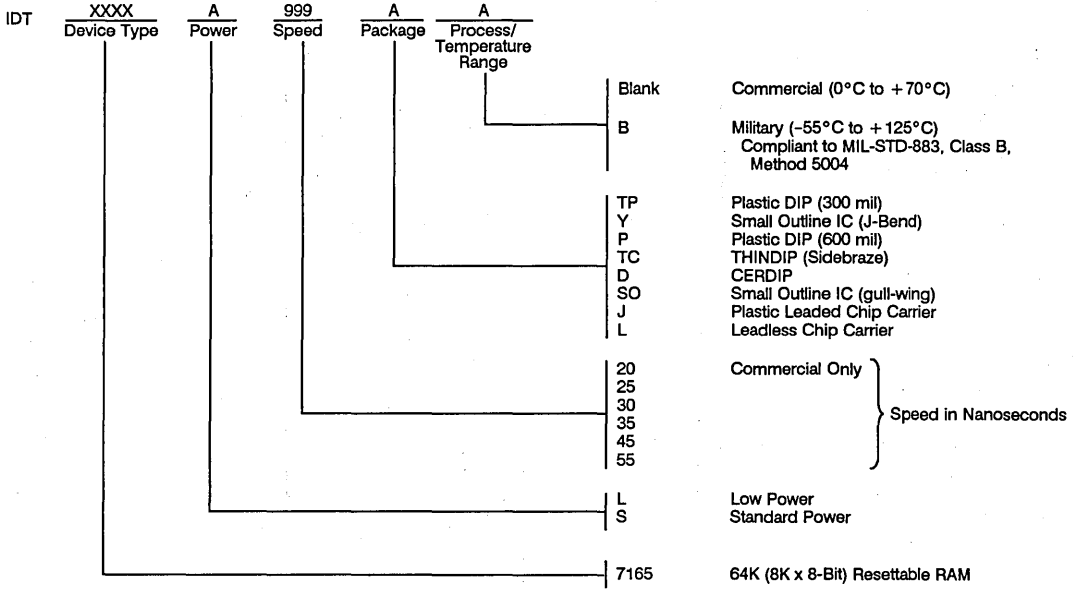
Driving the $\overline{RESET}$ pin with CMOS logic.



Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 3.

ORDERING INFORMATION



4

Integrated Device Technology, Inc.

CMOS RESETTABLE RAM WITH CMOS I/O LEVELS 64K (8K x 8-BIT)

IDT 71C65S
IDT 71C65L

FEATURES:

- Input and output directly CMOS-compatible
- High-speed (equal access and cycle time)
  - Military: 35/45/55ns (max.)
  - Commercial: 30/35/45ns (max.)
- Low-power operation
  - IDT71C65S
    Active: 300mW (typ.)
    Standby: 100μW (typ.)
  - IDT71C65L
    Active: 250mW (typ.)
    Standby: 30μW (typ.)
- Battery backup operation—2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V(±10%) power supply
- Static operation: no clocks or refresh required
- Available in standard 28-pin, 300 mil THINDIP; 28-pin, 600 mil plastic DIP; 28-pin SOIC and 32-pin LCC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71C65 is a 65,536-bit high-speed static RAM organized as 8K x 8. Inputs and outputs are compatible with industry standard CMOS input and output voltage levels.

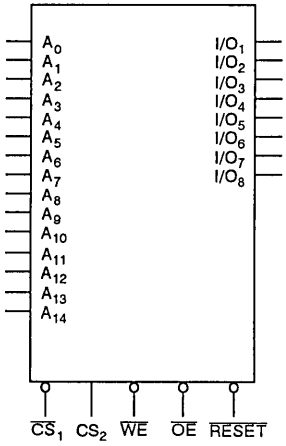
This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. An address access time of 30ns and a chip select ($\overline{CS}_1$) time of 15ns are available with typical power consumption of only 250mW. This circuit also offers a reduced power standby mode. In the full standby mode, the low-power device consumes less than 30μW typically. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 80μW operation off a 2V battery.

All inputs and outputs of the IDT71C65 are CMOS-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

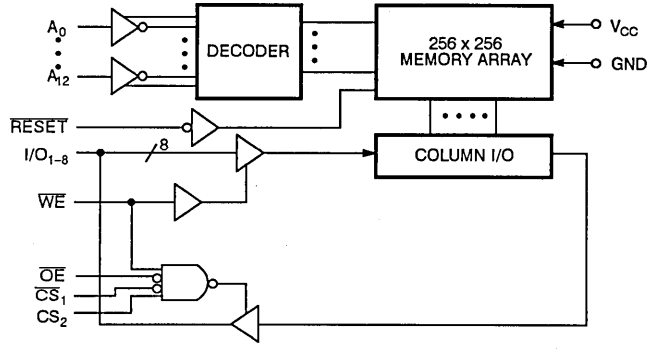
The IDT71C65 is packaged in a 28-pin, 300 mil THINDIP; 600 mil plastic DIP; a 32-pin LCC and a 28-pin SOIC, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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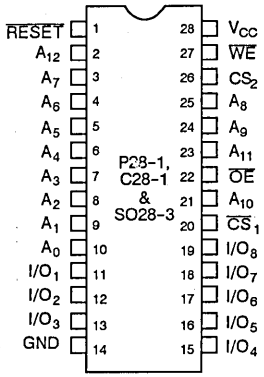
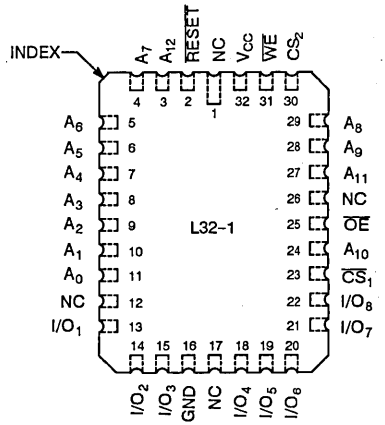
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

PIN NAMES

$A_0 - A_{12}$	Address	$\overline{OE}$	Output Enable
$I/O_1 - I/O_8$	Data Input/Output	$\overline{RESET}$ (1)	Memory Reset
$\overline{CS_1}$, CS_2	Chip Select	GND	Ground
$\overline{WE}$	Write Enable	V_{CC}	Power

NOTE:
1. A 1KΩ pull-up resistor on the $\overline{RESET}$ input is required for added noise immunity.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND(2)	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All inputs and V_{CC} pin. Data pins $I/O_1 - I/O_8$ must not be taken above V_{CC} + 1.0V.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	70% of V_{CC}	–	5.5(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	–	30% of V_{CC}	V

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. If V_{IH} = 5.5V, V_{CC} = 4.5V, there is risk of latch up.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71C65S MIN.	IDT71C65S MAX.	IDT71C65L MIN.	IDT71C65L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}_1$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	MIL.	–	0.44	–	0.44	V
		I_{OL} = 10mA, V_{CC} = Min.	COM'L.	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -50µA, V_{CC} = 4.5V		4.4	–	4.4	–	V
		I_{OH} = -6mA, V_{CC} = 4.5V	COM'L.	3.7	–	3.7	–	V
		I_{OH} = -6mA, V_{CC} = 4.5V	MIL.	3.8	–	3.8	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V, V_{IH} = V_{CC}-0.8V, V_{IL} = 0.8V

SYMBOL	PARAMETER	POWER	IDT71C65S30 IDT71C65L30 COM'L.	IDT71C65S30 IDT71C65L30 MIL.	IDT71C65S35 IDT71C65L35 COM'L.	IDT71C65S35 IDT71C65L35 MIL.	IDT71C65S45 IDT71C65L45 COM'L.	IDT71C65S45 IDT71C65L45 MIL.	IDT71C65S55 IDT71C65L55 COM'L.	IDT71C65S55 IDT71C65L55 MIL.	UNIT
I_{CC1} (2)	Operating Power Supply Current V_{CC} = Max., f = 0 (3)	S	95	–	95	105	95	105	–	105	mA
		L	85	–	85	95	85	95	–	95	
I_{CC2} (2)	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX} (3)	S	160	–	160	170	160	170	–	170	mA
		L	135	–	125	135	115	125	–	120	
I_{SB}	Standby Power Supply Current 1) $CS_2 \le V_{LC}$, and $\overline{RESET} \ge V_{IH}$, f = f_{MAX} (3) 2) $\overline{CS}_1 \ge V_{IH}$, V_{CC} = Max., Outputs Open, $CS_2 \ge V_{IH}$, f = f_{MAX} (3), $\overline{RESET} \ge V_{IH}$	S	20	–	20	20	20	20	–	20	mA
		L	3	–	3	5	3	5	–	5	
I_{SB1}	Full Standby Power Supply Current 1) $CS_2 \le V_{LC}$, $\overline{RESET} \ge V_{HC}$, f = 0 (3) 2) $\overline{CS}_1 \ge V_{HC}$, $CS_2 \ge V_{HC}$, $\overline{RESET} \ge V_{HC}$ f = 0 (3)	S	15	–	15	20	15	20	–	20	mA
		L	0.2	–	0.2	1	0.2	1	–	1	

NOTES:

1. All values are maximum guaranteed values.
2. CS_2 = V_{IH}, $\overline{CS}_1$ = V_{IL}
3. At f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

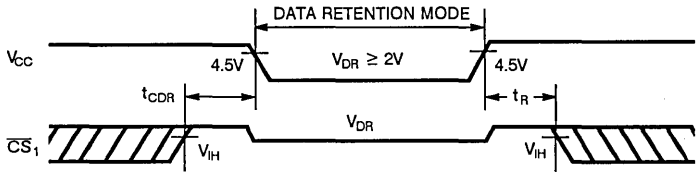
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	1) $\overline{RESET} \geq V_{HC}$, $\overline{CS_1} \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2) $CS_2 \leq V_{LC}$, $\overline{RESET} \geq V_{HC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	
t_{CDR}	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns
$\|I_{LI}\|$	Input Leakage Current(3)			–	–	–	2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.
4. During data retention all I/O pins have to be ≤ V_{LC} or ≥ V_{HC} but ≤ V_{CC}.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to V_{CC}
Input Rise/Fall Times	5ns
Input Timing Reference Levels	2.5V
Output Reference Levels	2.5V
Output Load	See Figures 1 and 2

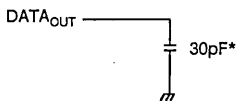


Figure 1. Output Load

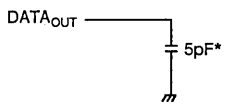


Figure 2. Output Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, t_{WHZ})

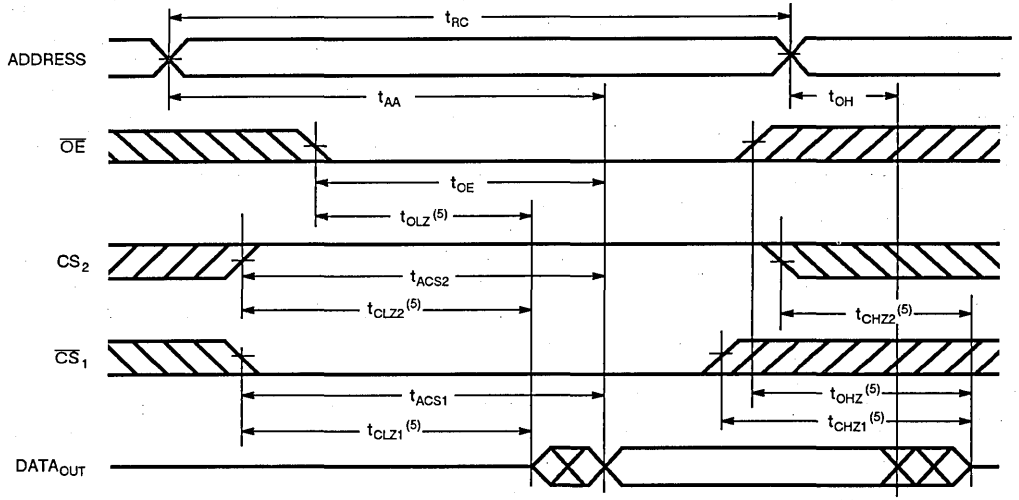
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

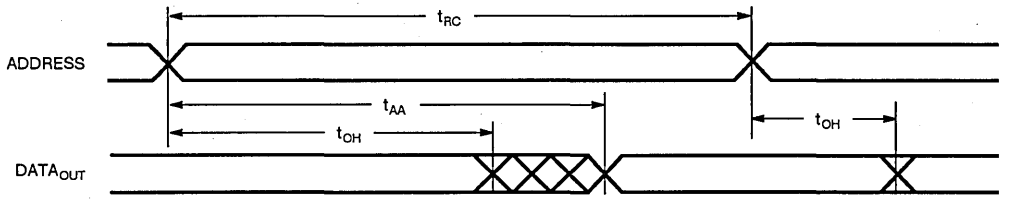
SYMBOL	PARAMETER	IDT71C65S30[1] IDT71C65L30[1] MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55[4] IDT71C65L55[4] MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	30	–	35	–	45	–	55	ns
t_{ACS1}	Chip Select 1 Access Time[2]	–	20	–	25	–	35	–	40	ns
t_{ACS2}	Chip Select 2 Access Time[2]	–	35	–	40	–	45	–	55	ns
t_{CLZ1}	Chip Select 1 to Output in Low Z[3]	0	–	0	–	0	–	0	–	ns
t_{CLZ2}	Chip Select 2 to Output in Low Z[3]	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	20	–	25	–	35	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	0	–	0	–	0	–	0	–	ns
t_{CHZ1}	Chip Select 1 to Output in High Z[3]	–	15	–	20	–	25	–	30	ns
t_{CHZ2}	Chip Select 2 to Output in High Z[3]	–	15	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[3]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselect to Power Down Time[3]	–	30	–	35	–	45	–	55	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. This parameter is guaranteed but not tested.
4. -55°C to +125°C temperature range only.

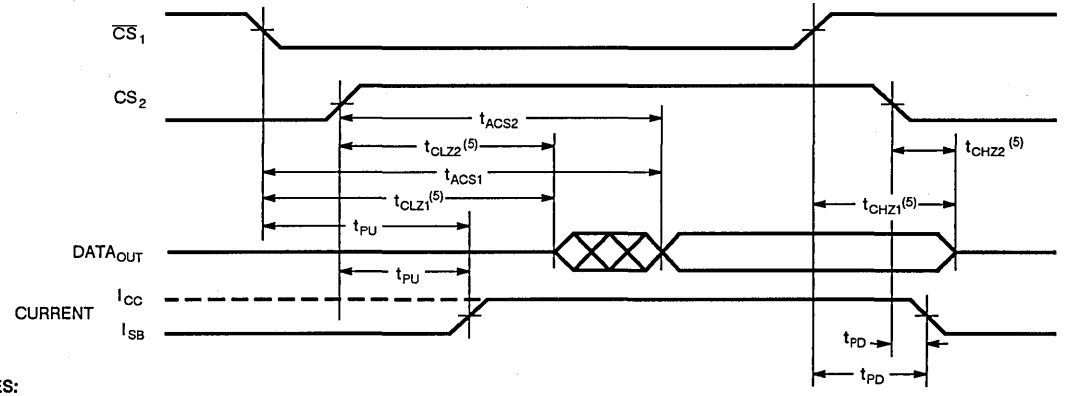
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



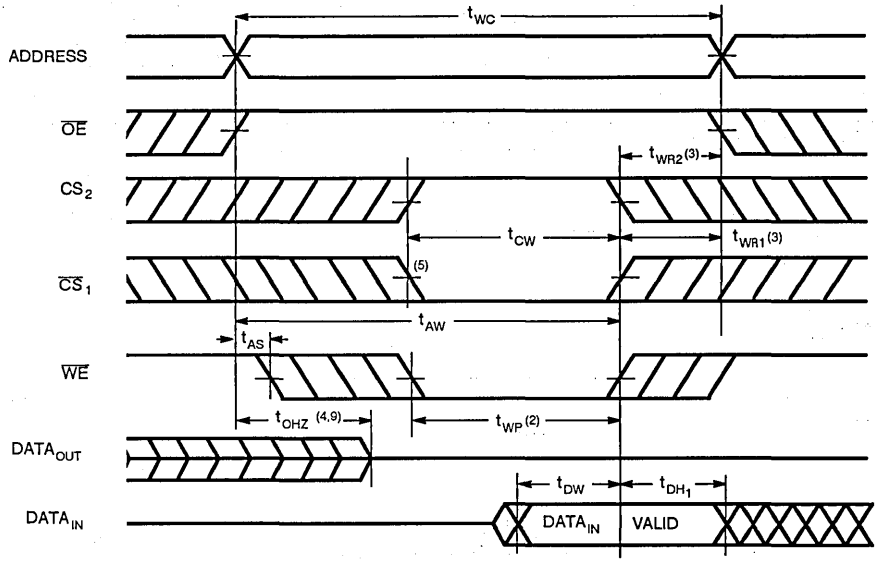
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

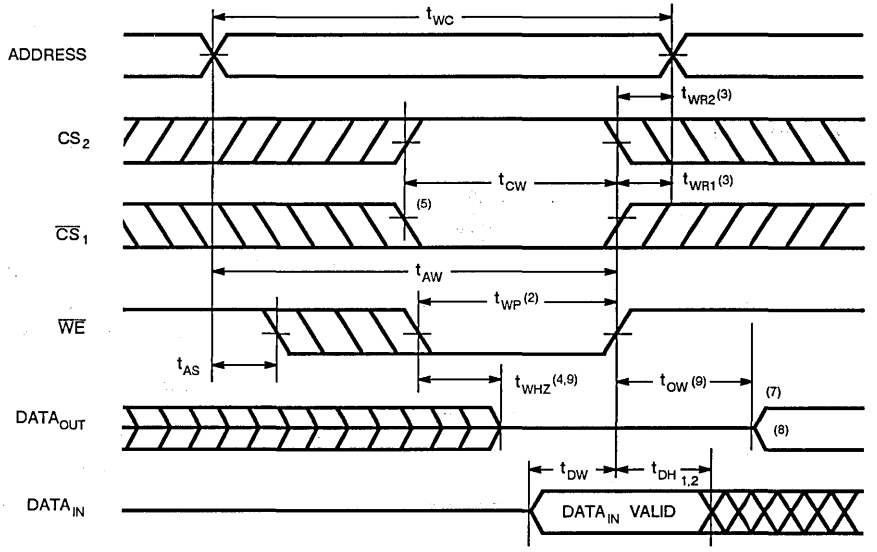
SYMBOL	PARAMETER	IDT71C65S30 [1] IDT71C65L30 [1] MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55 [2] IDT71C65L55 [2] MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	55	–	ns
t_{CW1}	Chip Select 1 to End of Write	20	–	20	–	25	–	30	–	ns
t_{CW2}	Chip Select 2 to End of Write	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	40	–	50	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output In High Z [3]	–	10	–	12	–	15	–	20	ns
t_{DW}	Data to Write Time Overlap	15	–	18	–	25	–	30	–	ns
t_{DH1}	Data Hold From Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	ns
t_{DH2}	Data Hold From Write Time (CS_2)	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write [3]	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2[1, 6]



NOTES:

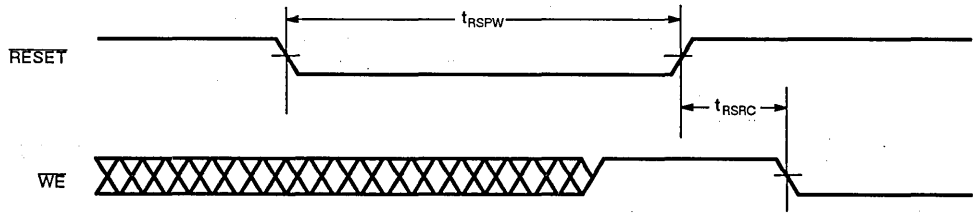
1. $\overline{WE}$ or $\overline{CS_1}$, or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS_1}$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

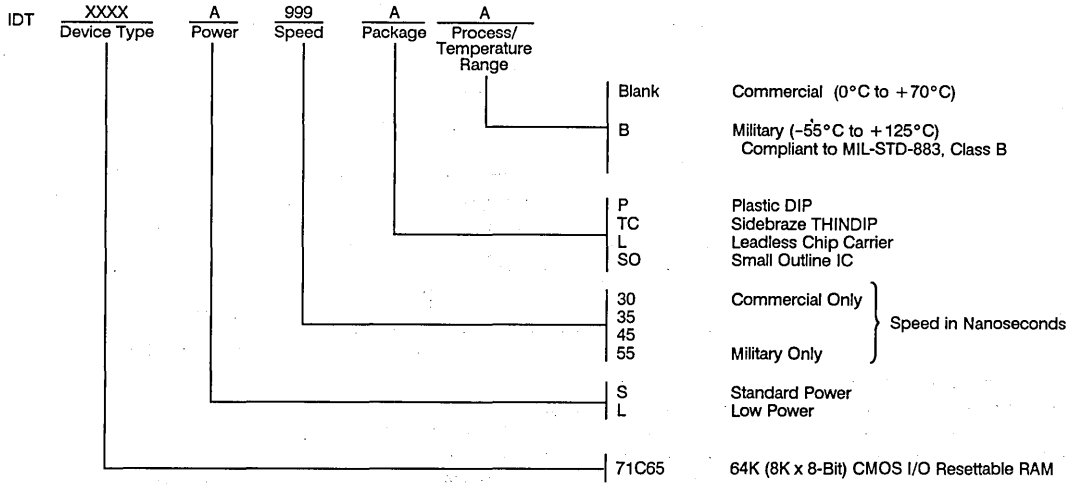
SYMBOL	PARAMETER	IDT71C65S30[1] IDT71C65L30[1] MIN.	MAX.	IDT71C65S35 IDT71C65L35 MIN.	MAX.	IDT71C65S45 IDT71C65L45 MIN.	MAX.	IDT71C65S55[2] IDT71C65L55[2] MIN.	MAX.	UNIT
$\overline{RESET}$[3]										
t_{RSPW}	$\overline{RESET}$ Pulse Width[4]	55	–	65	–	80	–	100	–	ns
t_{RSR}	$\overline{RESET}$ High to $\overline{WE}$ Low	5	–	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. A 1KΩ pull-up resistor to V_{CC} on the $\overline{RESET}$ pin is required for added noise immunity.
4. Maximum 10% duty cycle applies.

$\overline{RESET}$ TIMING



ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT 7174S

FEATURES:

- High-speed address to MATCH comparison time
  - Military: 25/35/45/55ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- High-speed address access time
  - Military: 25/35/45/55ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- High-speed chip select access time
  - Military: 15/20/25/30ns (max.)
  - Commercial: 10/15/20/25ns (max.)
- Low-power operation
  - IDT7174S
    Active: 300mW (typ.)
- High-speed asynchronous RAM Clear on Pin 1 (Reset Cycle Time = 2 x t_{AA})
- MATCH Output on Pin 26
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil and 300 mil), 28-pin SOIC (gull-wing or J-bend), 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT7174 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT7174s can be combined to provide 28 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT7174 can also be used as an 8K x 8 high-speed static RAM.

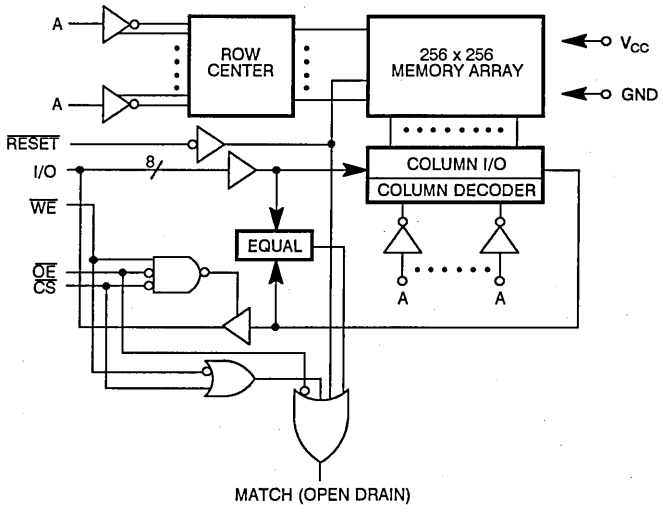
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology—CEMOS. Address access times as fast as 20ns, chip select times of 10ns and address-to-comparison times of 20ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7174 is packaged in a 28-pin DIP (600 mil and 300 mil), a 28-pin SOIC (gull-wing or J-bend) and 32-pin LCC and PLCC, providing high board level packing densities.

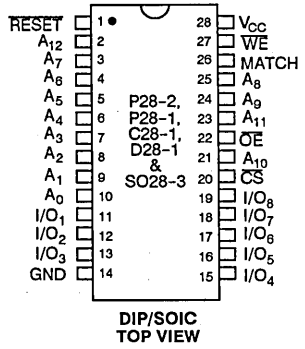
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

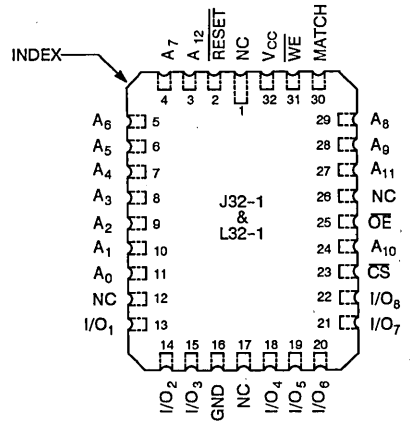


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

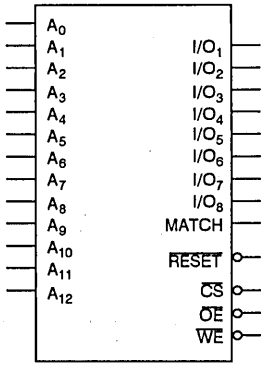


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power
MATCH	Data/Memory Match (Open Drain)		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage (1)	2.2	–	6.0	V
V_{IHR}	$\overline{RESET}$ Input High Voltage	2.5 (2)	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 (3)	–	0.8	V

NOTES:

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7174S MIN.	IDT7174S TYP.(1)	IDT7174S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	µA
$\|I_{LO}\|$	Output Leakage Current(2)	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	– –	– –	10 5	µA
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH	MIL.	–	–	0.5	V
		I_{OL} = 22mA MATCH	COM'L.	–	–	0.5	V
		I_{OL} = 10mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min. (Except MATCH)		2.4	–	–	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. Data and MATCH

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	IDT7174S20 COM'L.	IDT7174S20 MIL.	IDT7174S25(2) COM'L.	IDT7174S25(2) MIL.	IDT7174S35 COM'L.	IDT7174S35 MIL.	IDT7174S45 COM'L.	IDT7174S45 MIL.	IDT7174S55 COM'L.	IDT7174S55 MIL.	UNIT
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	110	–	110	125	110	125	110	125	–	125	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	190	–	170	190	150	170	140	150	–	145	mA

NOTES:
1. All values are maximum guaranteed values.
2. Military values are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

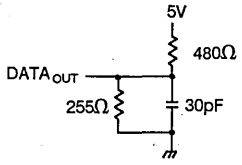


Figure 1. Output Load

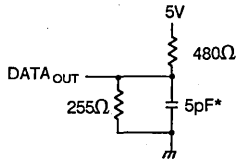


Figure 2. Output Load (for t_{CLZ} t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

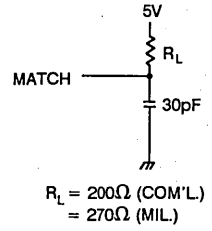


Figure 3. Output Load for MATCH

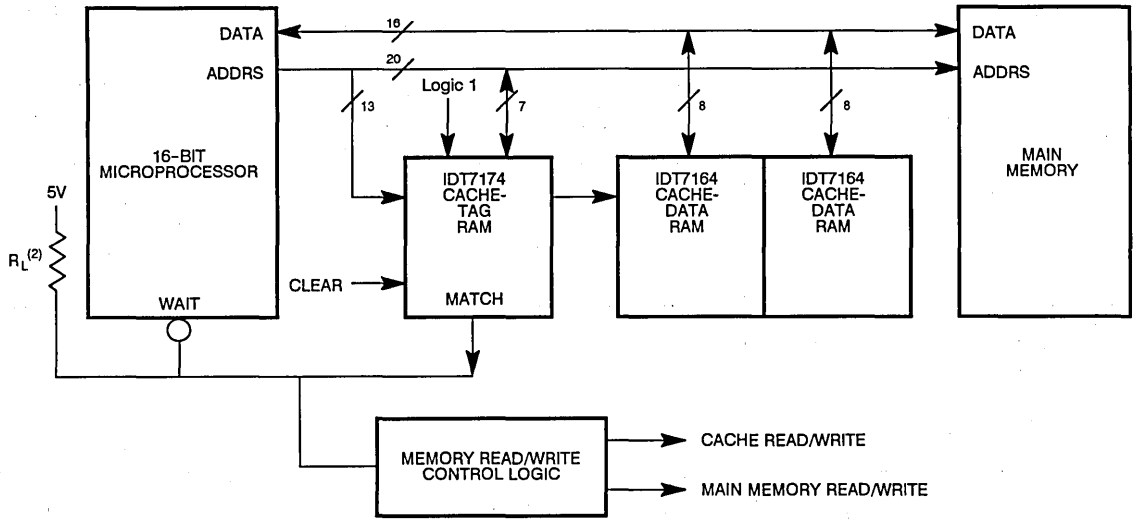


Figure 4. Example of Cache Memory System Block Diagram

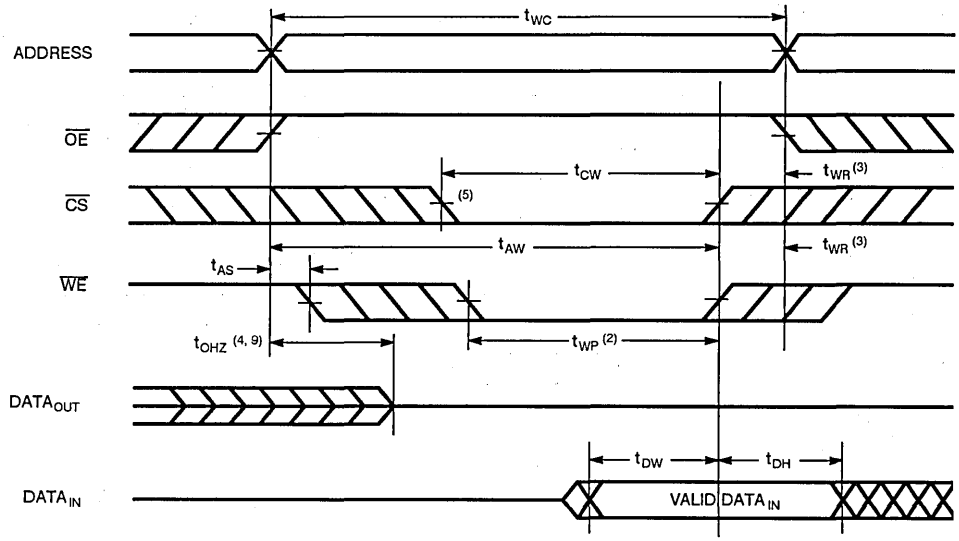
NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. R_L = 200Ω (commercial) or 270Ω (military)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

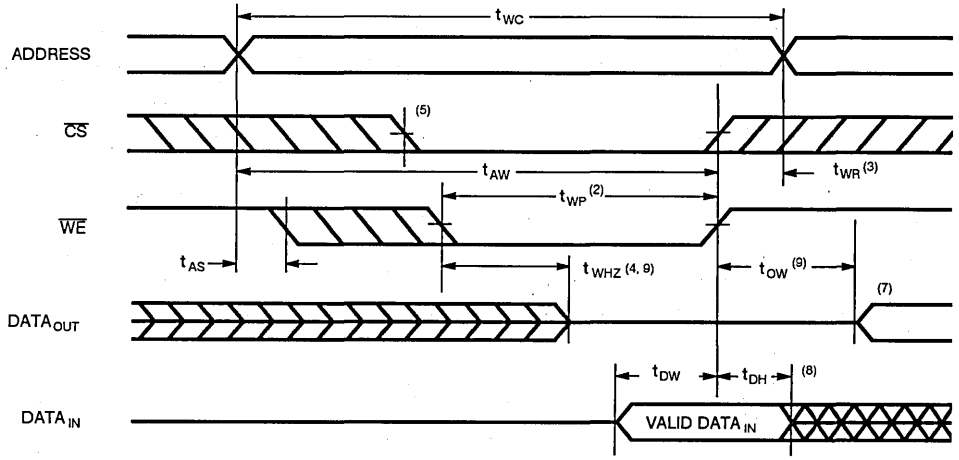
SYMBOL	PARAMETER	IDT7174S20(1)		IDT7174S25		IDT7174S35(1)		IDT7174S45		IDT7174S55(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	–	25	–	35	–	45	–	55	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	20	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	21	–	30	–	40	–	50	–	ns
t_{WR}	Write Recovery Time (CS, WE)	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z(3)	–	8	–	10	–	15	–	20	–	25	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold From Write Time	2	–	2	–	2	–	2	–	2	–	ns
t_{OW}	Output Active from End of Write(3)	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data for -55°C to +125°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:

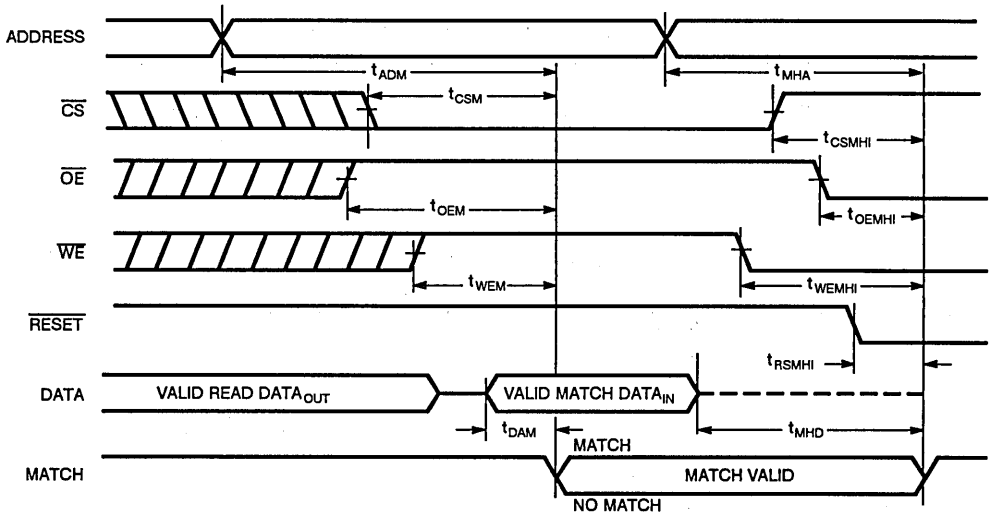
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S20[1]		IDT7174S25		IDT7174S35[3]		IDT7174S45		IDT7174S55[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
MATCH												
t_{ADM}	Address to MATCH Valid	–	20	–	25	–	35	–	45	–	55	ns
t_{CSM}	Chip Select to MATCH Valid	–	10	–	15	–	20	–	25	–	30	ns
t_{CSMHI}	Chip Deselect to MATCH High	–	10	–	15	–	20	–	25	–	30	ns
t_{DAM}	Data Input to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{OEMHI}	$\overline{OE}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{OEM}	$\overline{OE}$ High to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{WEMHI}	$\overline{WE}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{WEM}	$\overline{WE}$ High to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{RSMHI}	$\overline{RESET}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{MHA}	MATCH Valid Hold From Address	5	–	5	–	5	–	5	–	5	–	ns
t_{MHD}	MATCH Valid Hold From Data	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Preliminary data for -55°C to +125°C temperature range only.

MATCH TIMING



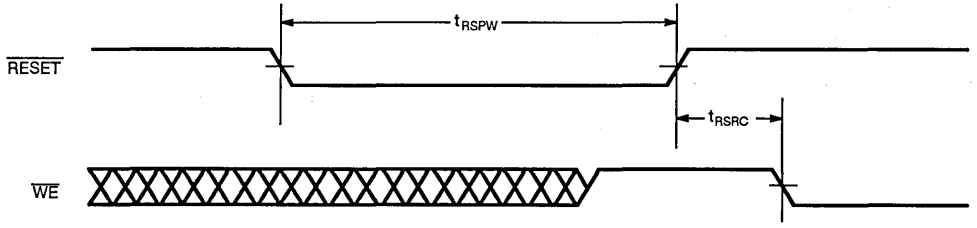
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S20[1] MIN.	IDT7174S20[1] MAX.	IDT7174S25 MIN.	IDT7174S25 MAX.	IDT7174S35[4] MIN.	IDT7174S35[4] MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55[2] MIN.	IDT7174S55[2] MAX.	UNIT
RESET												
t_{RSPW}	$\overline{RESET}$ Pulse Width [3]	45	–	55	–	65	–	80	–	100	–	ns
t_{RSRC}	$\overline{RESET}$ High to $\overline{WE}$ Low	5	–	5	–	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Recommended duty cycle 10% maximum.
4. Preliminary Information for -55°C to +125°C temperature range only.

4

RESET TIMING



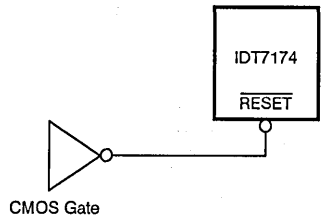
CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

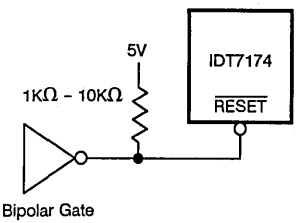
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{RESET}$	MATCH	I/O	FUNCTION
X	X	X	L	H	–	Reset all bits to low
X	H	X	H	H	High Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write



Driving the $\overline{RESET}$ pin with CMOS logic.



Driving the $\overline{RESET}$ pin with bipolar logic.

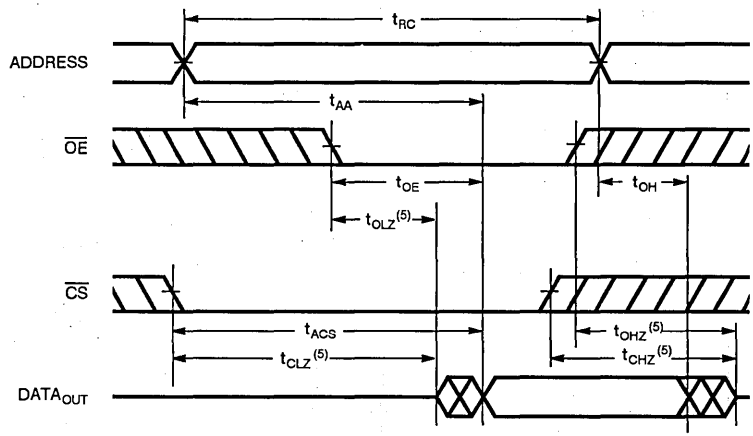
Figure 4.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

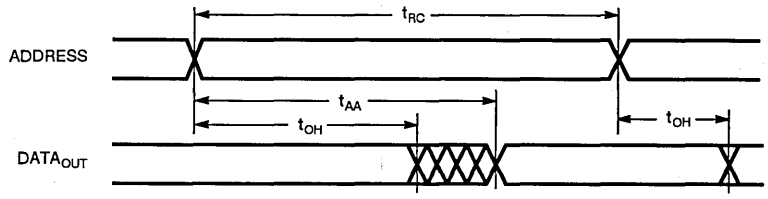
SYMBOL	PARAMETER	IDT7174S20[1]		IDT7174S25		IDT7174S35[4]		IDT7174S45		IDT7174S55[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	10	–	12	–	20	–	25	–	30	ns
t_{CLZ}	Chip Select to Output in Low Z	0	–	0	–	0	–	0	–	0	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	12	–	20	–	25	–	30	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	3	–	3	–	3	–	3	–	3	–	ns
t_{CHZ}	Chip Select to Output in High Z[3]	–	9	–	13	–	15	–	20	–	25	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8	–	12	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary information for -55°C to +125°C temperature range only.

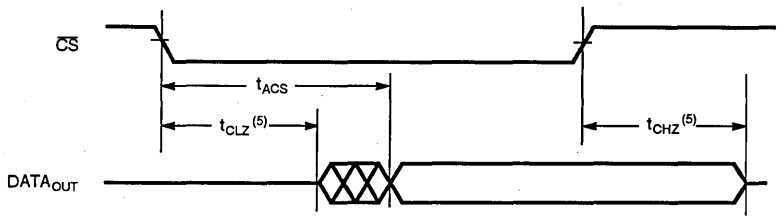
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



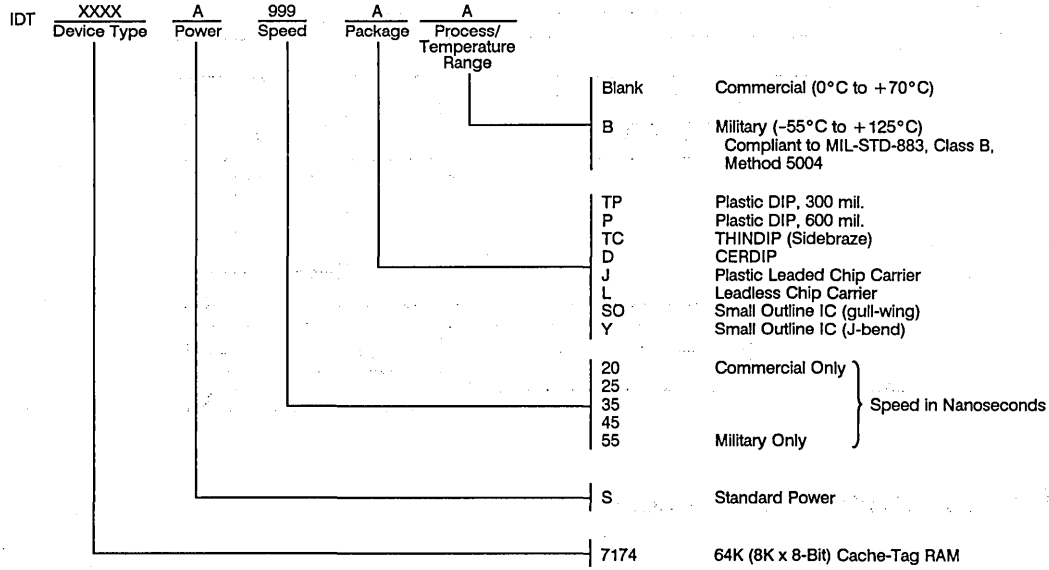
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM WITH LATCHED ADDRESSES 64K (8K x 8-BIT)

ADVANCE INFORMATION
IDT 71564S
IDT 71564L

4

FEATURES:

- High-Speed Address Access Time
  - Military: 25/35/45ns
  - Commercial: 20/25/35ns
- On-Board Address Latches
- Low-Power Consumption and High-Reliability
- Battery Back-Up Operation: 2-Volt Data Retention (L Version Only)
- Produced with Advanced CEMOS™ High-Performance Technology
- Single 5V (±10%) Power Supply
- Input and Output Directly TTL Compatible
- Three-State Output
- Static Operation No Clocks or Refresh Required
- Military Product Compliant to MIL-STD-883, Class B

DESCRIPTION:

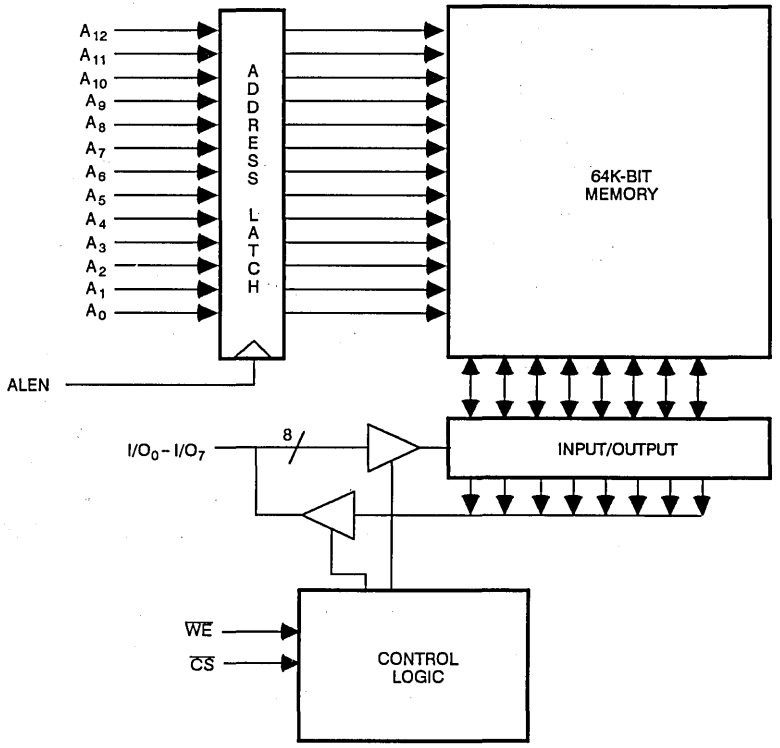
The 71564 is 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS™ technology.

Address access times as fast as 20ns are available with typical power consumption of only 250mW. The 71564 excels in cache applications because of the on-chip address latches, which reduces system part count. This device is the preferred solution with 64K Byte Caches in systems requiring address latches, ie. the IDT79R3000.

The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

All inputs and outputs of the IDT71564 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

CMOS STATIC RAM EXCLUSIVE-OR LATCHED ADDRESSES 64K (8K x 8-BIT)

ADVANCE INFORMATION
IDT 71578S
IDT 71578L

FEATURES:

- High-Speed Address Access Time
  - Military: 25/35/45ns
  - Commercial: 20/25/35ns
- On-Board Address Latches
- Exclusive-Or on the Least Significant Bit
- Low-Power Consumption and High-Reliability
- Battery Back-Up Operation: 2-Volt Data Retention (L Version Only)
- Produced with Advanced CEMOS™ High-Performance Technology
- Single 5V (±10%) Power Supply
- Input and Output Directly TTL Compatible
- Three-State Output
- Static Operation No Clocks or Refresh Required
- Military Product Compliant to MIL-STD-883, Class B

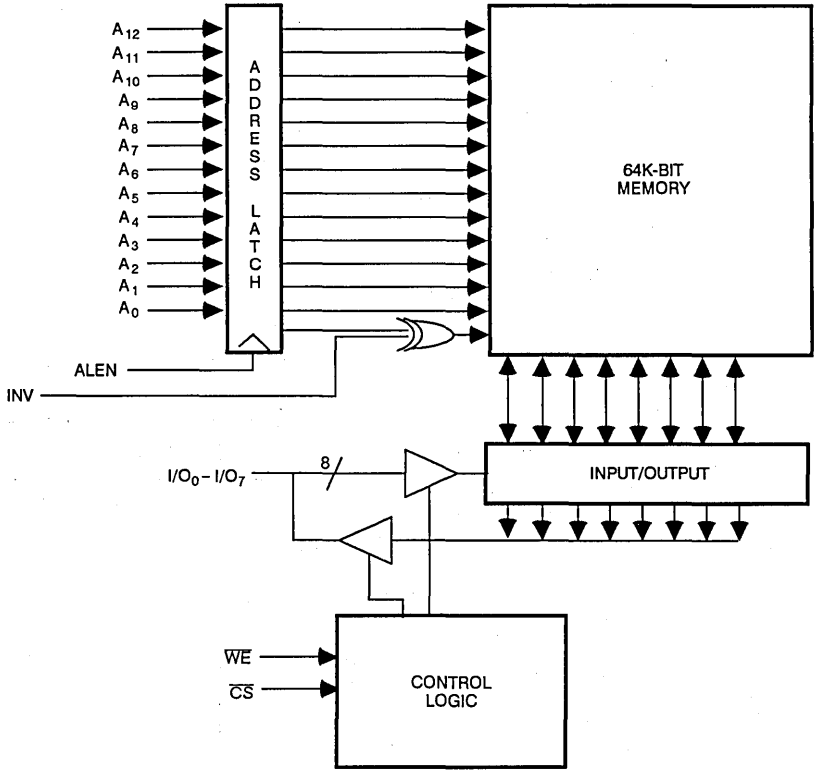
DESCRIPTION:

The 71578 is 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS™ technology.

Address access times as fast as 20ns are available with typical power consumption of only 250mW. The 71578 excels in cache applications because of the on-chip address latches, which reduce system part count. An exclusive-or function on the least significant address bit simplifies implementation of "burst-mode" cache refills. This device is the preferred solution with 64K Byte Caches for the Intel 80386. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10mW operating off a 2V battery.

All inputs and outputs of the IDT71578 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAM 256K (32K x 8-BIT)

IDT 71256S
IDT 71256L

4

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select time
  - Military: 30/35/45/55/70/85/100ns (max.)
  - Commercial: 19/20/25/30/35/45/55/70ns (max.)
- Low-power operation
  - IDT71256S
    Active: 300mW (typ.)
    Standby: 200μW (typ.)
  - IDT71256L
    Active: 250mW (typ.)
    Standby: 15μW (typ.)
- Battery Backup operation—2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin CERDIP and plastic DIP (600 mil), 28-pin SOIC, 28-pin Cerpack and 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-88552 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

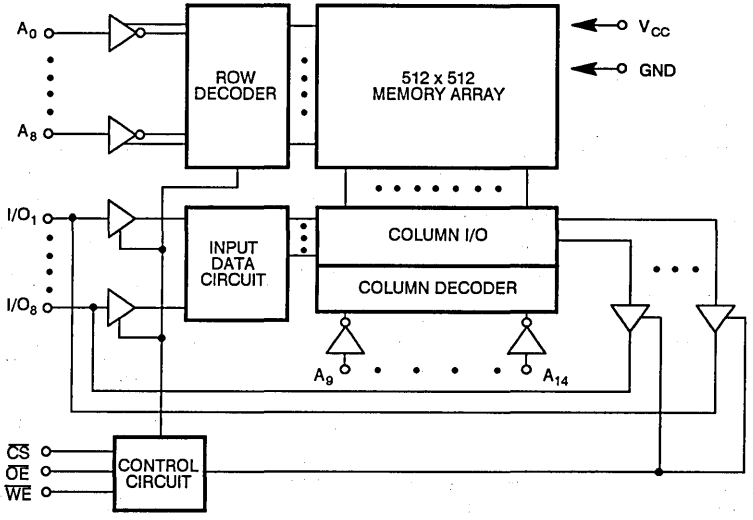
Address access times as fast as 19ns are available with power consumption of only 300mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15μW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5μW when operating off a 2V battery.

All inputs and outputs of the IDT71256 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71256 is packaged in a 28-pin gull-wing or J-bend SOIC, a 28-pin 600 mil CERDIP or plastic DIP, 28-pin Cerpack and 32-pin leadless chip carrier and PLCC, providing high board-level packing densities.

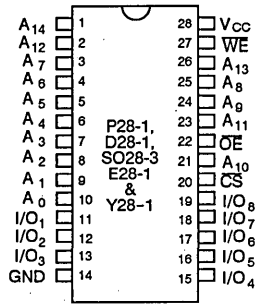
The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

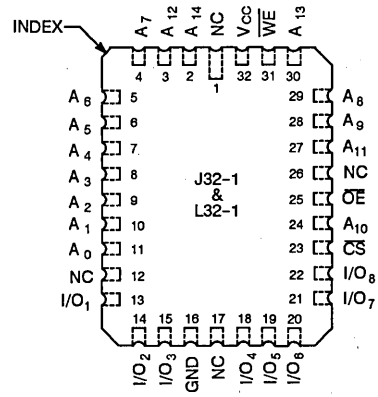


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

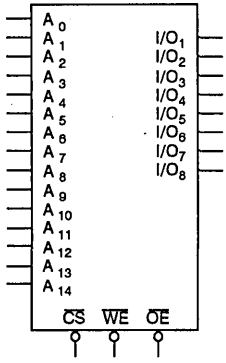


DIP/SOIC/Cerpack
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

$A_0 - A_{14}$	Addresses
$I/O_1 - I/O_8$	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71256S MIN.	IDT71256S MAX.	IDT71256L MIN.	IDT71256L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	5	–	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

4

DC ELECTRICAL CHARACTERISTICS[1, 3] V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	71256x19/20 COM'L.	71256x19/20 MIL.	71256x25 COM'L.	71256x25 MIL.	71256x30/35 COM'L.	71256x30/35 MIL.	71256x45/55 COM'L.	71256x45/55 MIL.	71256x70 COM'L.	71256x70 MIL.	71256x85/100 COM'L.	71256x85/100 MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	READ	100	–	30	–	30	40	30	40	30	40	–	40	mA
			WRITE[2]	100	–	90	–	90	100	90	100	90	100	–	100	
		L	READ	100	–	15	–	15	20	15	20	15	20	–	20	
			WRITE[2]	100	–	80	–	80	90	80	90	80	90	–	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[4]	S	READ	200	–	195	–	170/155	180/165	140	150	140	150	–	150	mA
			WRITE[2]	200	–	180	–	165/150	175/165	140	150	140	150	–	150	
		L	READ	200	–	175	–	150/135	160/145	110/90	120/100	75	85	–	70	
			WRITE[2]	200	–	160	–	145/130	155/135	115/105	125/115	95	105	–	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., f = f_{MAX}[4] Outputs Open.	S		30	–	20	–	20	20	20	20	20	20	–	20	mA
		L		5	–	3	–	3	3	3	3	3	3	–	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0	S		20	–	15	–	15	20	15	20	15	20	–	20	mA
		L		1.0	–	0.4	–	0.4	1.5	0.4	1.5	0.4	1.5	0.4	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of Read cycles to Write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of Read to Write cycles (usually greater than 90%).
3. "x" in part numbers indicates power rating (S or L).
4. f_{MAX} = $1/t_{RC}$

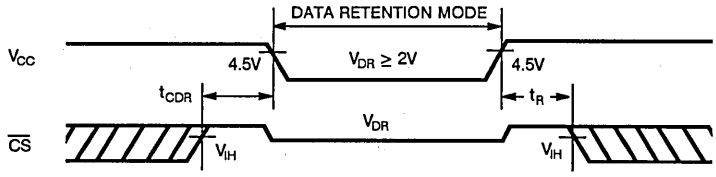
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	–	–	500	800	µA
			COM'L.	–			120	200	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

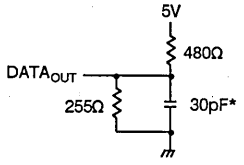


Figure 1. Output Load

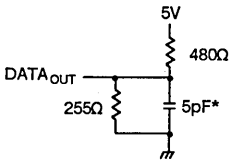


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

* Including scope and jig.

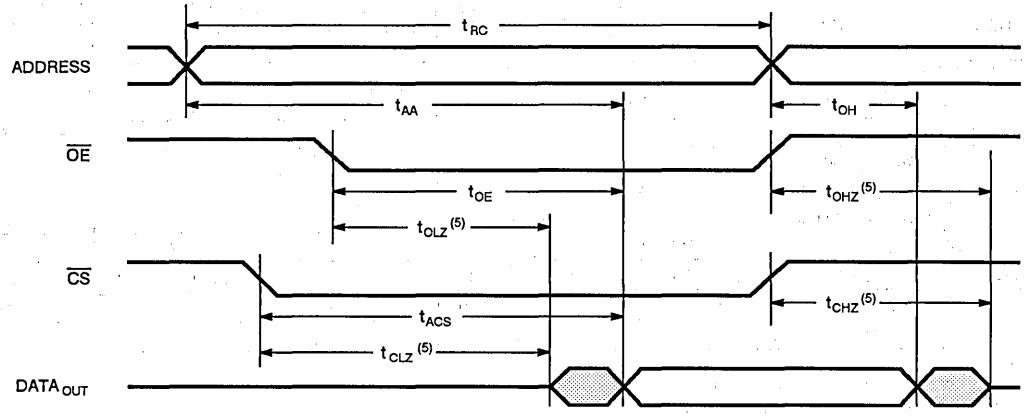
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	71256S19/20[3] 71256L20[3] MIN.	MAX.	71256S25[3] 71256L25[3] MIN.	MAX.	71256S30/35 71256L30/35 MIN.	MAX.	71256S45/55 71256L45/55 MIN.	MAX.	71256S70 71256L70 MIN.	MAX.	71256S85/100[1] 71256L85/100[1] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	30/35	–	45/55	–	70	–	85/100	–	ns
t_{AA}	Address Access Time	–	19/20	–	25	–	29/35	–	45/55	–	70	–	85/100	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30/35	–	45/55	–	70	–	85/100	ns
t_{CLZ}	Chip Select to Output in Low Z[2]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	11	–	13/15	–	20/25	–	30	–	35/40	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	2	–	2	–	2	–	0	–	0	–	0	–	ns
t_{CHZ}	Chip Deselect to Output in High Z[2]	–	10	–	11	–	15	–	20/25	–	30	–	35/40	ns
t_{OHZ}	Output Disable to Output in High Z[2]	2	8	2	10	2/2	12/15	–	20/25	–	30	–	35/40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

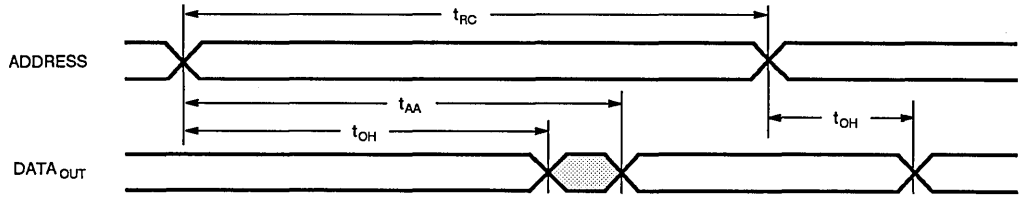
NOTES:
1. -55°C to +125°C temperature range only.
2. This parameter is guaranteed, but not tested.
3. 0°C to +70°C temperature range only.

4

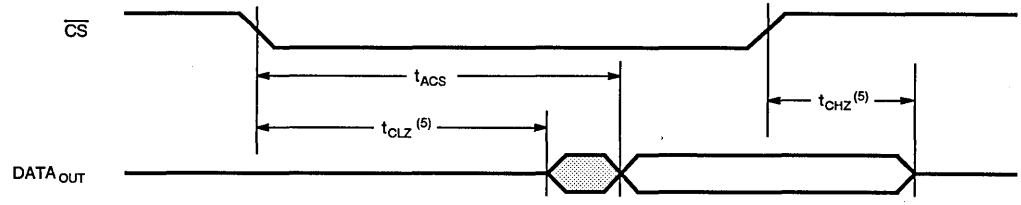
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

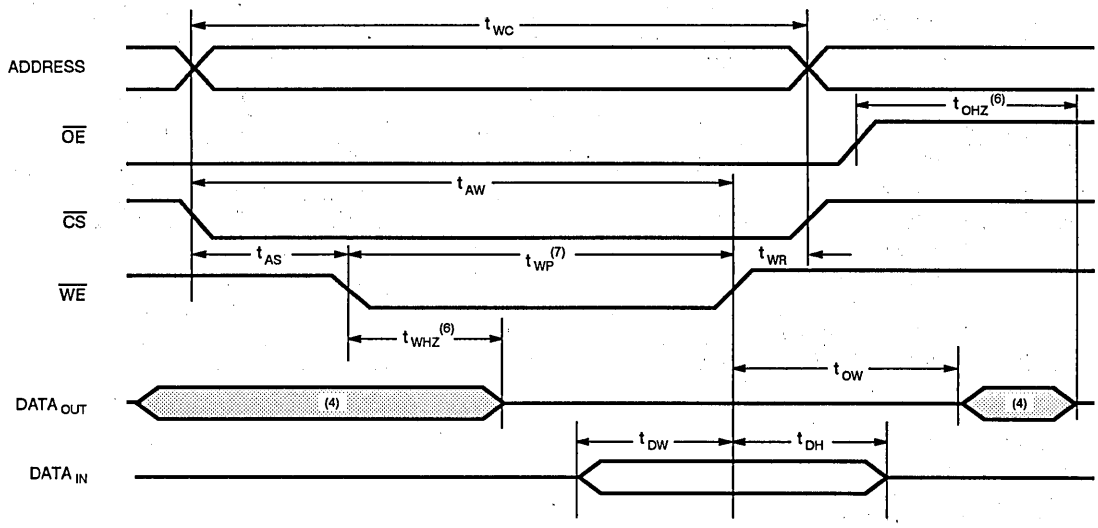
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	71256S19/20[4] 71256L20[4] MIN.	MAX.	71256S25[4] 71256L25[4] MIN.	MAX.	71256S30/35 71256L30/35 MIN.	MAX.	71256S45/55 71256L45/55 MIN.	MAX.	71256S70 71256L70 MIN.	MAX.	71256S85/100[2] 71256L85/100[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	25	–	30/35	–	45/55	–	70	–	85/100	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	25/30	–	40/50	–	60	–	70/80	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	25/30	–	40/50	–	60	–	70/80	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	20	–	23/30	–	35/40	–	45	–	50/55	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z[3]	–	10	–	11	–	15	–	20/25	–	30	–	35/40	ns
t_{DW}	Data to Write Time Overlap	11	–	13	–	14/18[1]	–	20/25	–	30	–	35/40	–	ns
t_{DH1}	Data hold from Write Time ($\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DH2}	Data hold from Write Time ($\overline{CS}$)	3	–	3	–	3	–	3	–	3	–	3	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns

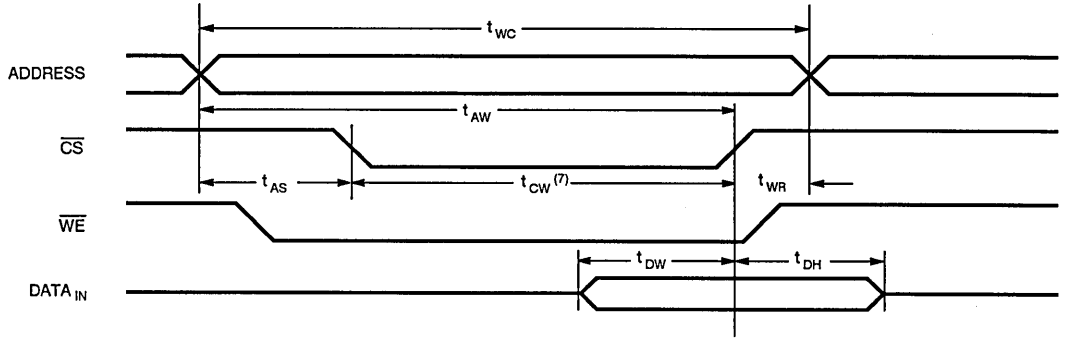
NOTES:

1. For the 0°C to 70°C temperature range,
   30ns speed grade, t_{DW} = 14ns.
   35ns speed grade, t_{DW} = 15ns.
   Over the -55°C to +125°C temperature range,
   30ns speed grade, t_{DW} = 17ns.
   35ns speed grade, t_{DW} = 18ns.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.
4. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

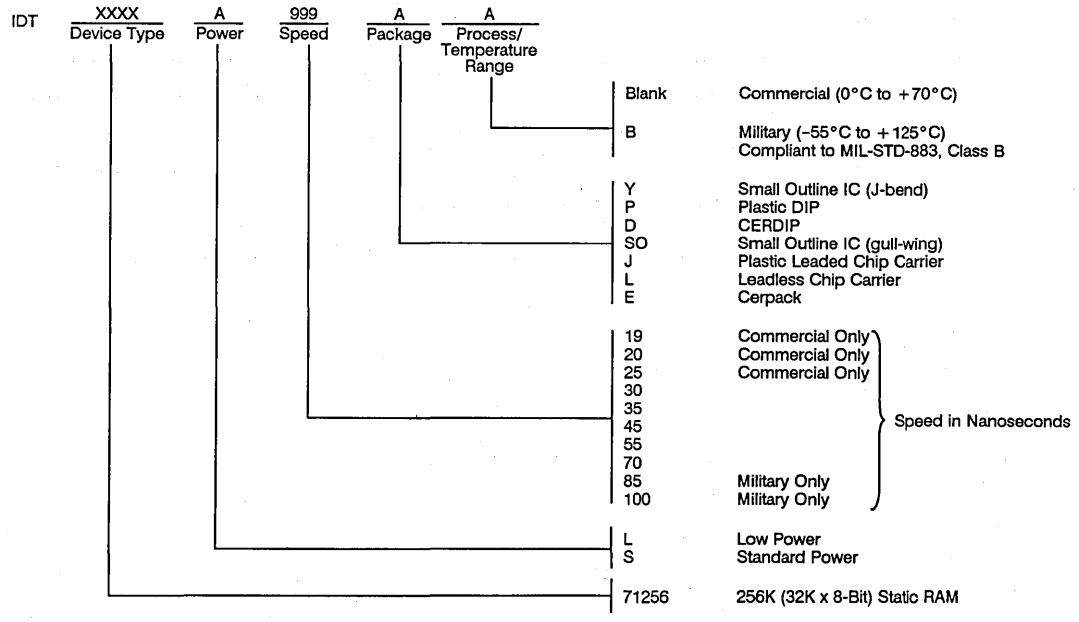
TRUTH TABLE V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	FUNCTION
X	H	X	Hi-Z	Standby (I_{SB})
X	V_{HC}	X	Hi-Z	Standby (I_{SB1})
H	L	H	Hi-Z	Output Disable
H	L	L	$DATA_{OUT}$	Read
L	L	X	$DATA_{IN}$	Write

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

4

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM ORGANIZED AS 32K x 8

ADVANCE INFORMATION
IDT 71583

FEATURES:

- 32K x 8 Parity checking Static RAM
- High-speed address/chip select time
  - Military: 35/45/55
  - Commercial: 25/35/45
- Low power operation
  - IDT71583S
    Active: 450mW (typ.)
    Standby: 300mW (typ.)
  - IDT71583L
    Active: 350mW (typ.)
    Standby: 200mW (typ.)
- Three chip selects plus one Output Enable pin
- Address latches, activated by positive-true Latch Enable
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Battery back-up operation—2V data retention
- Available in 32-pin side-brazed and plastic DIP (300mil) and 32-pin SOIC
- Military product is fully compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71583 is a 294,912-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

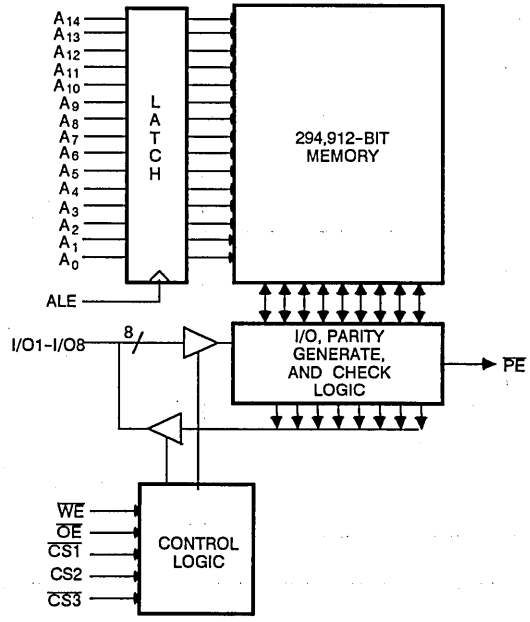
Address access times as fast as 25ns are available with power consumption of only 450mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 200mW (typ.). This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 20µW when operating off a 2V battery.

All inputs and outputs of the IDT71583 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71583 is packaged in a 32-pin 300mil side-brazed, 32-pin 300mil Plastic DIP, and 32-pin SOIC.

The IDT71583 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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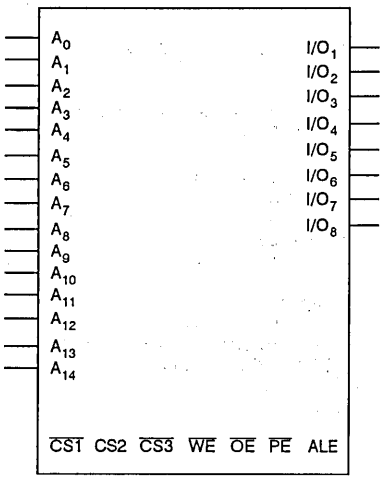
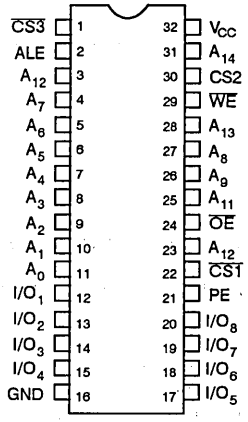
LOGIC SYMBOL



PIN CONFIGURATION



TRUTH TABLE

WE	CS1	CS2	CS3	OE	I/O	PE	MODE
X	H	X	X	X	Hi-Z	Hi-Z	Standby (ISB1)
X	X	L	X	X	Hi-Z	Hi-Z	Standby (ISB1)
X	X	X	H	X	Hi-Z	Hi-Z	Standby (ISB1)
H	L	H	L	H	Hi-Z	Hi-Z	Output Disable
H	L	H	L	L	D_{OUT}	D_{OUT}	Read
L	L	H	L	X	D_{IN}	D_{IN}	Write

NOTES:

1. CS2 and $\overline{CS3}$ are used for conditional write.
2. When ALE (Address Latch) is H (HIGH) address function in "flow through" manner (Standard RAM Function).
   When ALE is L (LOW) addresses are latched.

Integrated Device Technology, Inc.

CMOS HIGH-SPEED STATIC RAM 8K x 9-BIT

ADVANCE INFORMATION
IDT 7169S
IDT 7169L

FEATURES:

- 8192-words x 9-bits organization
- JEDEC standard 28-pin package
- Fast access time:
  - Commercial: 35/45
  - Military: 45/55
- Battery backup operation—2V data retention voltage (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V power supply
- Input and output directly TTL compatible
- Static operation: no clocks or refresh required
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7169 is a 73728-bit high-speed static RAM organized as 8K x 9. It is fabricated using IDT's high-performance, high reliability CEMOS technology.

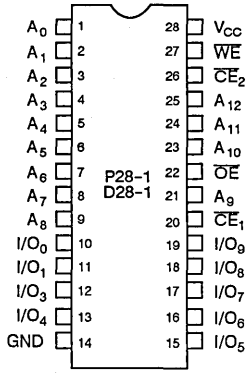
The IDT7169 offers address access times as fast as 35ns. The ninth bit is optimized for parity check.

All inputs and outputs of the IDT7169 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

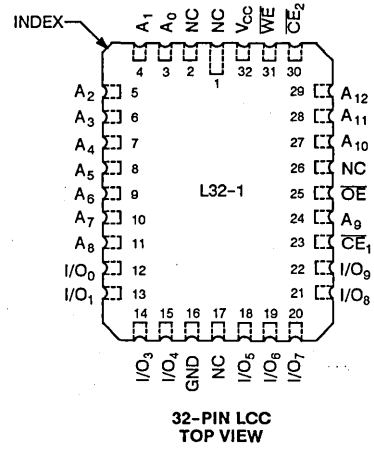
The IDT7169 is packaged in an industry standard 28-pin DIP and LCC, along with a 32-pin LCC package.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW



32-PIN LCC
TOP VIEW

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Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM ORGANIZED AS 32K x 9

ADVANCE INFORMATION
IDT 71259

FEATURES:

- High-speed address/chip select time
  - Military: 35/45/55
  - Commercial: 25/35/45
- Low power operation
  IDT71259S
  - Active: 450 mW (typ)
  - Standby: 300 mW (typ)
  IDT71259L
  - Active:350 mW (typ)
  - Standby: 200 mW (typ)
- Two chip selects plus one Output Enable pin
- Single 5V (+/-10%) power supply
- Input and output directly TTL-compatible
- Battery back-up operation-2V data retention
- Available in 32-pin side-brazed and plastic DIP (300 mil) and 32-pin SOIC.
- Military product is fully compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71259 is a 294,912-bit high-speed static RAM organized as 32K x 9. It is fabricated using IDT's high-performance high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Address access times as fast as 25ns are available with power consumption of only 450mW (typ). The circuit also offers a reduced power standby mode. When CS goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 200 mW (typ). This capability provides significant system level power and cooling savings. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 20 µW when operating off a 2V battery.

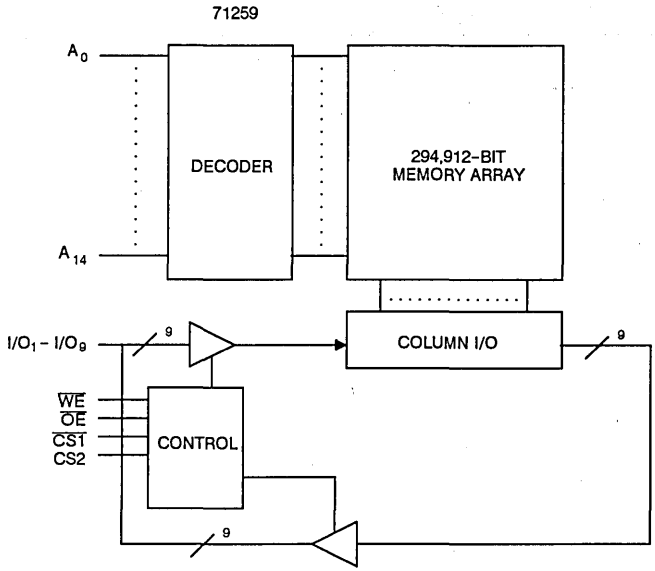
All inputs and outputs of the IDT71259 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71259 is packaged in a 32-pin 300 mil side-braze, 32-pin 300 mil Plastic DIP, and 32-pin SOIC.

The IDT71259 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

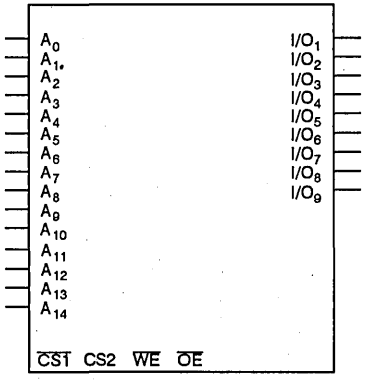
4

FUNCTIONAL BLOCK DIAGRAM

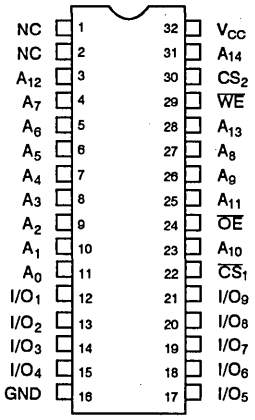


CEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL



PIN CONFIGURATION



TRUTH TABLE

WE	CS1	CS2	OE	I/O	MODE
X	H	X	X	Hi-Z	Standby (ISB1)
X	X	L	X	Hi-Z	Standby (ISB1)
H	L	H	H	Hi-Z	Output Disable
H	L	H	L	Dout	Read
L	L	H	X	Din	Write

Integrated Device Technology, Inc.

HIGH-SPEED STATIC RAM ORGANIZED AS 32K x 9

ADVANCE INFORMATION
IDT 71509

FEATURES:

- 32K x 9 Parity checking Static RAM
- High-speed address/chip select time
  - Military: 35/45/55
  - Commercial: 25/35/45
- Low power operation
  - IDT71509S
    Active: 450mW (typ.)
    Standby: 300mW (typ.)
  - IDT71509L
    Active: 350mW (typ.)
    Standby: 200mW (typ.)
- Two chip selects plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Battery back-up operation—2V data retention
- Available in 32-pin side-brazed and plastic DIP (300mil) and 32-pin SOIC
- Military product is fully compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71509 is a 294,912-bit high-speed static RAM organized as 32K x 9. It is fabricated using IDT's high-performance high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

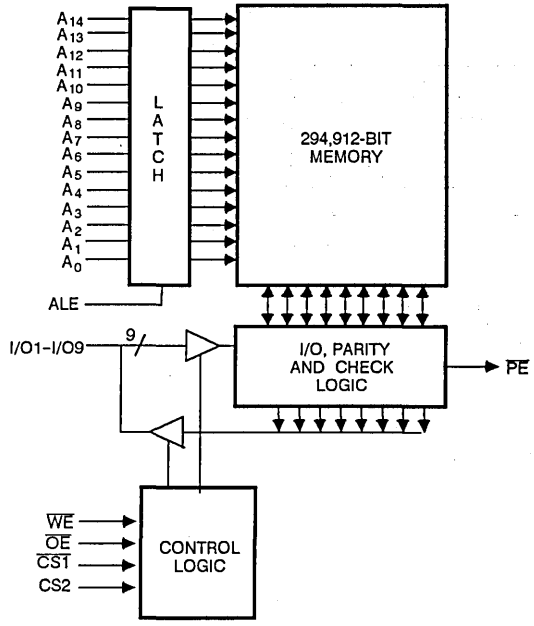
Address access times as fast as 25ns are available with power consumption of only 450mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 200mW (typ.). This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 20µW when operating off a 2V battery.

All inputs and outputs of the IDT71509 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT71509 is packaged in a 32-pin 300mil side-brazed, 32-pin 300mil Plastic DIP, and 32-pin SOIC.

The IDT71509 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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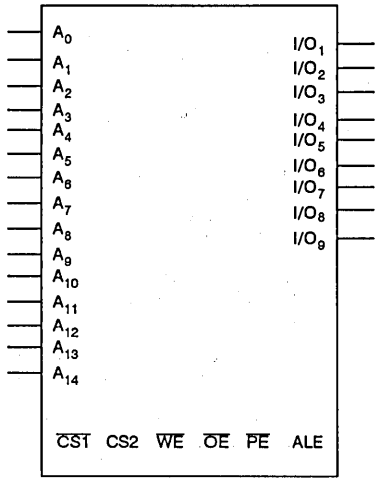
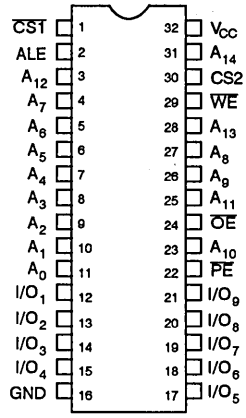
LOGIC SYMBOL



PIN CONFIGURATION



TRUTH TABLE

WE	CS1	CS2	OE	I/O	PE	MODE
X	H	X	X	Hi-Z	Hi-Z	Standby (ISB1)
X	X	L	X	Hi-Z	Hi-Z	Standby (ISB1)
H	L	H	H	Hi-Z	Hi-Z	Output Disable
H	L	H	L	D_{OUT}	D_{OUT}	Read
L	L	H	X	D_{IN}	D_{IN}	Write

NOTES:

1. CS2 is used for conditional write.
2. When ALE (Address Latch) is H (HIGH) address function in "flow through" manner (Standard RAM Function).
   When ALE is L (LOW) addresses are latched.

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16)

IDT 7186S
IDT 7186L

FEATURES:

- 16-bit word width, with separate control of upper and lower bytes
- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low power consumption
  - IDT7186S
    Active: 400mW (typ.)
    Standby: 100μW (typ.)
  - IDT7186L
    Active: 300mW (typ.)
    Standby: 30μW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- JEDEC compatible pinout
- Battery backup operation—2V data retention
- Available in 40-pin, 600 mil plastic and sidebraze DIP, and 44-pin plastic or ceramic leadless chip carrier
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7186 is an extremely high-speed 4K x 16-bit static RAM designed for use in wide-word systems where high speed, low power and board density are of the utmost importance.

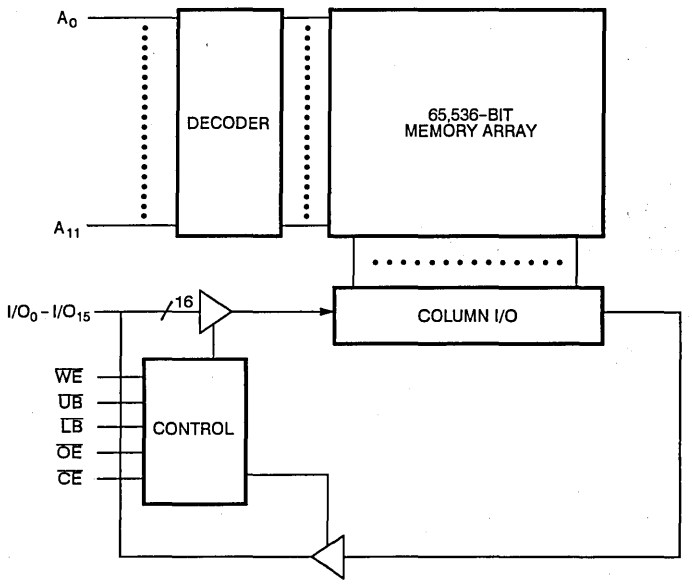
The IDT7186 uses sixteen bidirectional input/output lines to provide simultaneous access to all bits in a word and has two byte enable lines to allow the upper and lower byte of a word to be accessed either together or independently. A high-speed output enable pin allows designers to turn on the IDT7186's outputs at a speed much higher than the already fast address access time and achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry to enter a very low standby mode.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT7186 typically operates on only 300mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 30μW from a 2V battery.

The IDT7186 is packaged in either a sidebraze or plastic 40-pin DIP or a plastic or ceramic 44-pin leadless chip carrier. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

4

FUNCTIONAL BLOCK DIAGRAM



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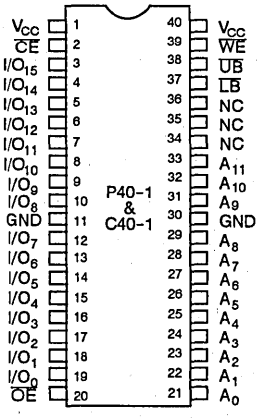
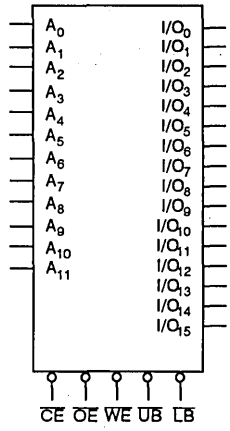
DSC-1024/1

PIN CONFIGURATIONS



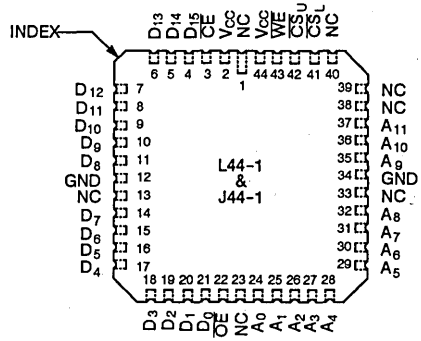
DIP
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0-A_{11}	Addresses
I/O_0-I/O_{15}	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
GND	Ground
V_{CC}	Power



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION		IDT7186S MIN.	IDT7186S MAX.	IDT7186L MIN.	IDT7186L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	10	–	5	µA
			COM'L.	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA, V_{CC} = Min.		–	0.4	–	0.4	V
		I_{OL} = 8mA, V_{CC} = Min.		–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	2.4	–	V

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	IDT7186S25 IDT7186L25		IDT7186S35 IDT7186L35		IDT7186S45 IDT7186L45		IDT7186S55 IDT7186L55		IDT7186S70 IDT7186L70		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CE}$=V_{IL}, Outputs Open, V_{CC} = Max., f = 0 (2)	S	160	–	140	160	130	150	130	150	130	150	mA
		L	135	–	125	145	115	135	115	135	115	135	mA
I_{CC2}	Dynamic Operating Current $\overline{CE}$=V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (2)	S	190	–	170	200	160	190	160	190	160	190	mA
		L	160	–	150	180	140	170	140	170	140	170	mA
I_{SB}	Standby Power Supply Current (TTL Level) CE ≥ V_{IH}, (2) V_{CC} = Max., f = f_{MAX} Outputs Open	S	50	–	40	40	40	40	40	40	40	40	mA
		L	10	–	6	6	6	6	6	6	6	6	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) CE ≥ V_{HC}, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC} V_{CC} = Max., f=0 (2)	S	20	–	15	20	15	20	15	20	15	20	mA
		L	1.0	–	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	mA

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data input are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

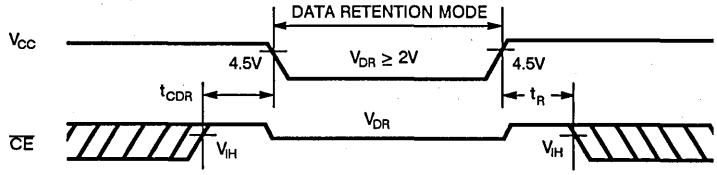
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	–	–	600	900	µA
			COM'L.	–	–	–	200	300	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	–	–	ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–	–	2	2	µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	12	pF

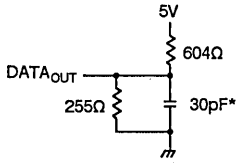


Figure 1. Output Load

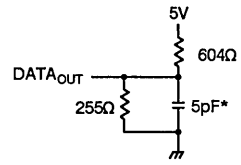


Figure 2. Output Load (for t_{OW}, t_{WHZ}, t_{CHZ}, t_{CLZ}, t_{BHZ}, t_{BLZ}, t_{OHZ}, t_{OLZ})

* Including scope and jig.

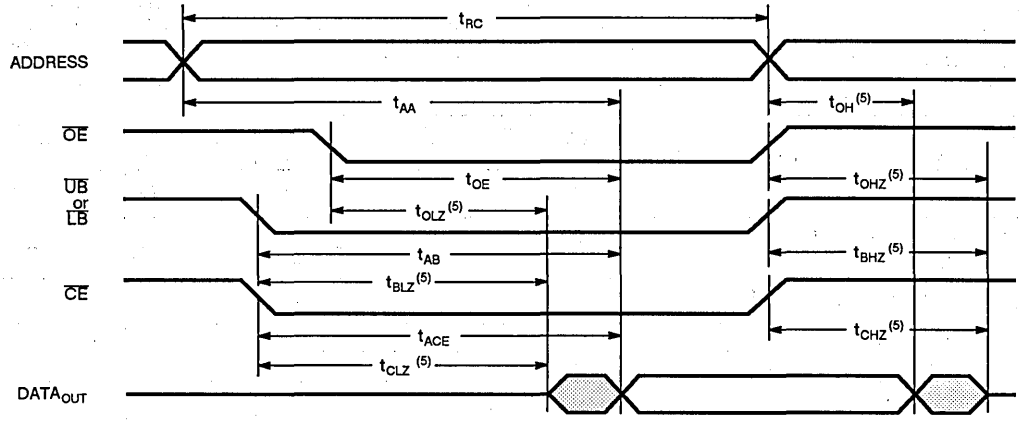
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7186S25[1] IDT7186L25[1] MIN.	MAX.	IDT7186S35 IDT7186L35 MIN.	MAX.	IDT7186S45 IDT7186L45 MIN.	MAX.	IDT7186S55 IDT7186L55 MIN.	MAX.	IDT7186S70 IDT7186L70 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{AB}	Upper/Lower Byte Enable Access Time	–	15	–	18	–	20	–	25	–	30	ns
t_{CLZ}	Chip Enable to Output in Low Z[2]	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	18	–	20	–	25	–	30	ns
t_{BLZ}	Upper/Lower Byte Enable to Output in Low Z[2]	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z[2]	–	15	–	18	–	20	–	25	–	30	ns
t_{OHZ}	Output Disable to Output in High Z[2]	–	15	–	18	–	20	–	25	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{BHZ}	Upper/Lower Byte Enable to Output in High Z[2]	–	15	–	18	–	20	–	25	–	30	ns
t_{PU}	Chip Enable to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time	–	25	–	35	–	45	–	55	–	70	ns

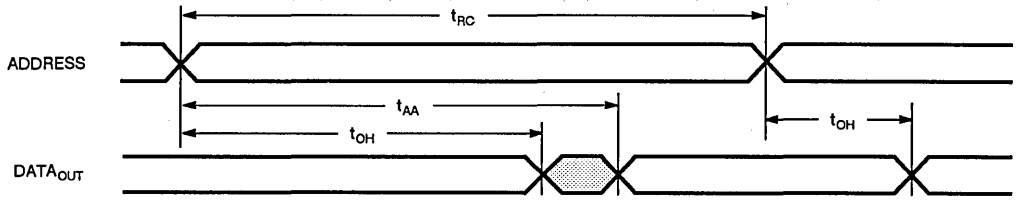
NOTES:
1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

4

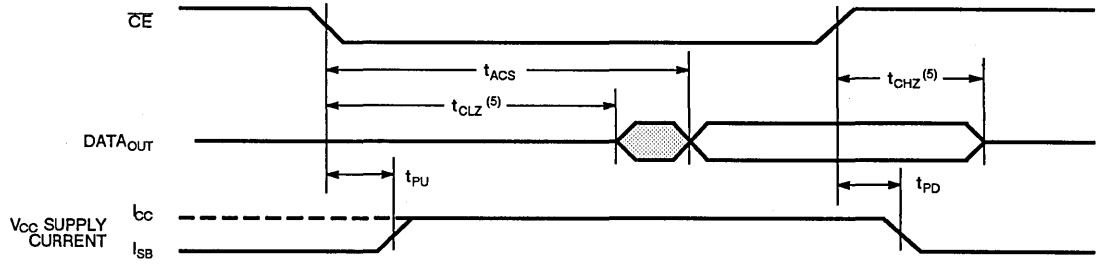
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (Continuously Enabled Read) (1, 2, 4, 6)



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}$ Controlled Read W/Power-Up/Down Timing) (1, 3, 4, 6)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state with 5pf load (including scope and jig).
6. $\overline{UB}$ or $\overline{LB}$ = V_{IL}

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

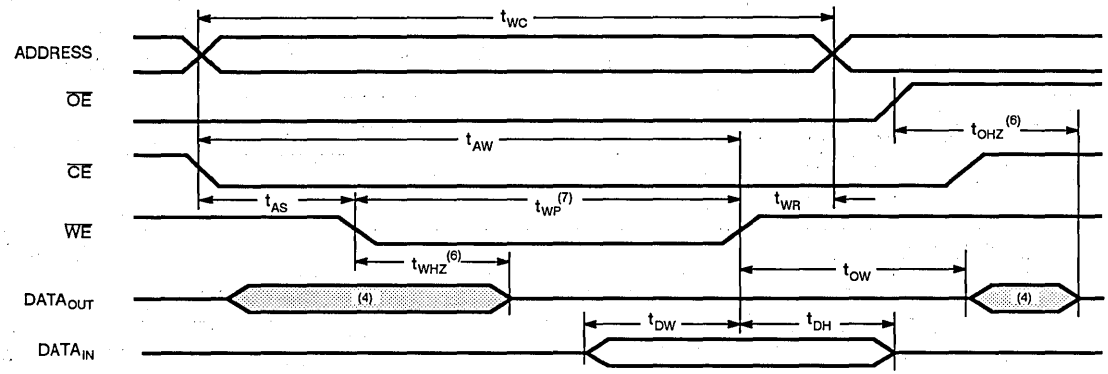
SYMBOL	PARAMETER	IDT7186S25 [1] IDT7186L25 [1] MIN.	MAX.	IDT7186S35 IDT7186L35 MIN.	MAX.	IDT7186S45 IDT7186L45 MIN.	MAX.	IDT7186S55 IDT7186L55 MIN.	MAX.	IDT7186S70 IDT7186L70 MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{CW}	Chip Enable to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{BW}	Upper/Lower Byte Enable to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	–	15	–	18	–	20	–	25	–	30	ns
t_{DW}	Data Set-up Time	15	–	18	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	3	–	3	–	3	–	3	–	3	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

NOTES:

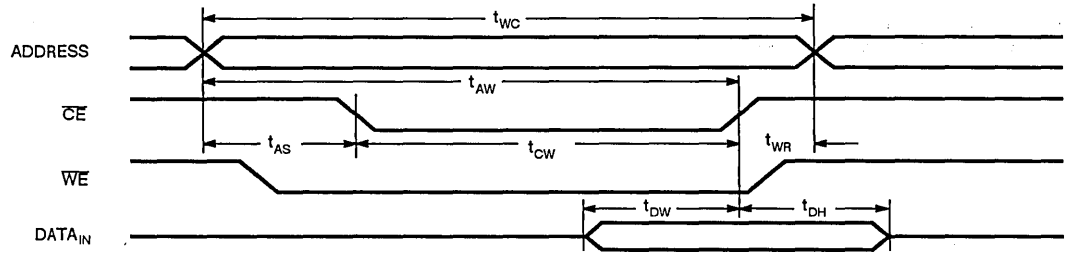
1. 0°C to +70°C temperature range only.
2. This parameter is guaranteed but not tested.

4

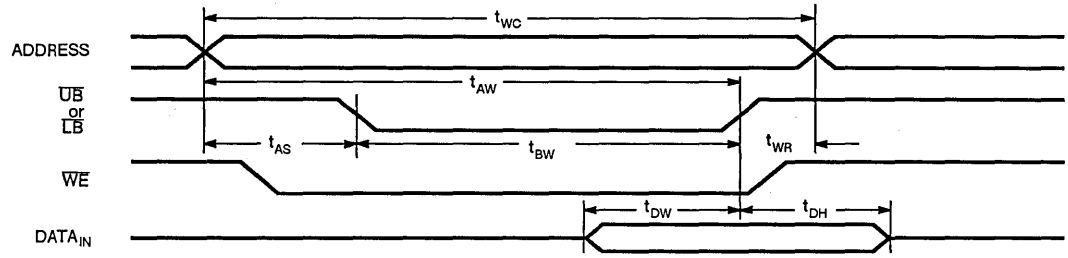
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 3, ($\overline{UB}$ or $\overline{LB}$ CONTROLLED TIMING) (1, 2, 3, 5, 9)



NOTES:

1. $\overline{WE}$, $\overline{CE}$, or both $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{BW}, t_{CW} or t_{WP}) of a low $\overline{UB}$ or $\overline{LB}$, a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{UB}$, $\overline{LB}$, $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{UB}$ or $\overline{LB}$ = V_{IL}
9. $\overline{CE}$ = V_{IL}

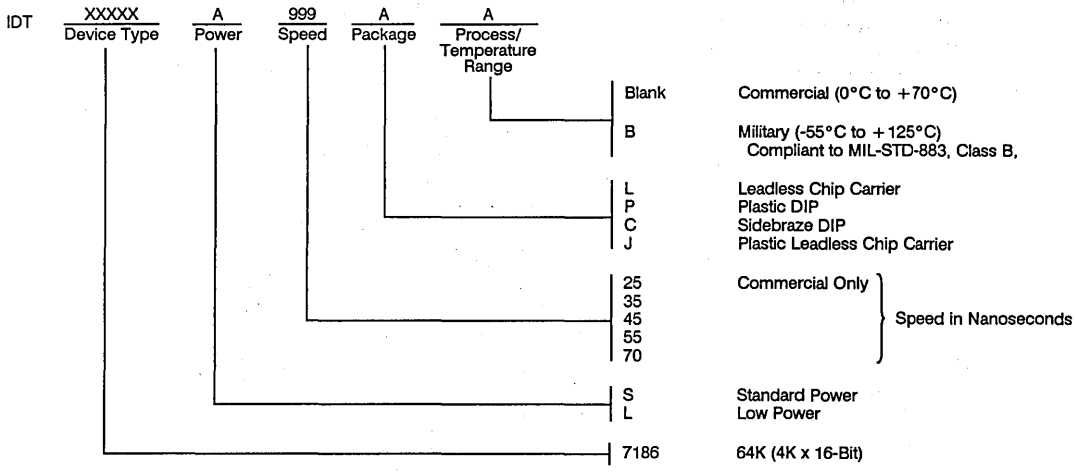
TRUTH TABLE [1]

INPUTS					OUTPUTS		MODE
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$I/O_8 - I/O_{15}$	$I/O_0 - I/O_7$	
H	X	X	X	X	Hi-Z	Hi-Z	Deselected, Powered Down
L	X	X	H	H	Hi-Z	Hi-Z	Both Bytes Deselected
L	L	X	L	H	$DATA_{IN}$	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	Hi-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes (Word Write)
L	H	L	L	H	$DATA_{OUT}$	Hi-Z	Read Upper Byte Only
L	H	L	H	L	Hi-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes (Word Read)
L	H	H	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTE:
1. H = High, L = Low, X = Don't Care, Hi-Z = High Impedance

4

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

IDT 71502S
IDT 71502L

FEATURES:

- 4K x 16 RAM with registered outputs, serial or parallel load and readback capability in only 48 pins
- Serial Protocol Channel allows serial load and readback of RAM over a 4-wire channel
- RAM address counter speeds RAM load and readback
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Programmable chip selects enable depth & width expansion without any external decode logic
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high reliability designs
- High-speed (address set-up before clock)
  - Military: 35/45/55ns (max.)
  - Commercial: 25/35/45ns (max.)
- Low-power consumption
  - IDT71502S - Active: 750mW (typ.)
  - IDT71502L - Active: 600mW (typ.)
- Input and output directly TTL-compatible
- Standard 48-pin DIP, 48-pin LCC and 52-pin PLCC.
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is a 65,536 bits high speed static RAM organized as 4K x 16, with a high speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel, SPC™.

This device is the first in a family of multifeatured RAM's with a built-in Serial Protocol Channel SPC™ letting the user set the best configuration for his system:

- SELF-ADDRESSING RAM
- WRITABLE CONTROL STORE
- LOGIC ANALYZER/RECORDER

The 71502 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This technology gives the 71502 the combination of low power, high speed, and high density that makes it a cost effective solution.

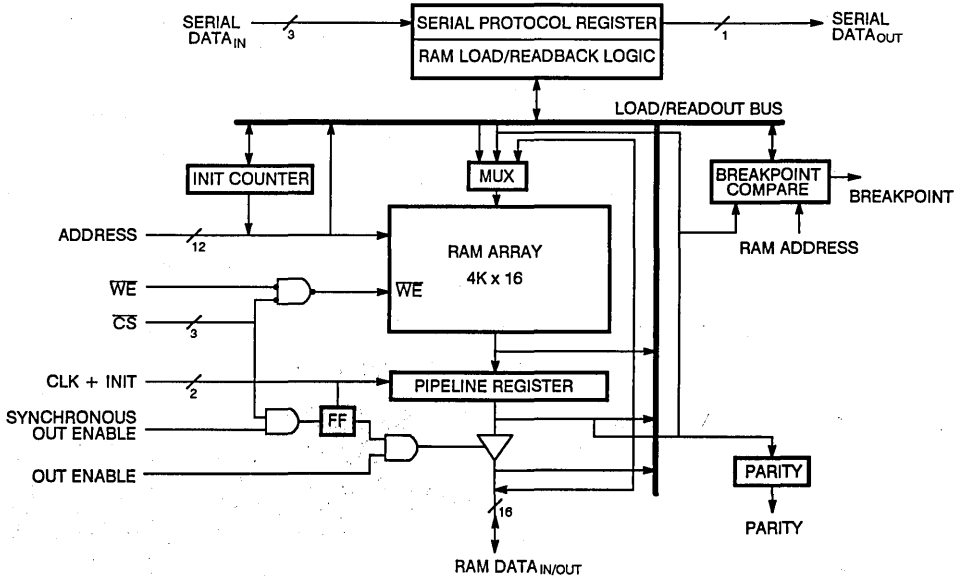
The IDT71502 is available with address set up before clock times as fast as 25ns. These times are available with a maximum power consumption of only 1.6W.

All inputs and outputs of the IDT71502 are TTL-compatible, and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is packaged in plastic and ceramic versions of either a 48-pin, 600 mil DIP; a 48-pin leadless chip carrier, or a 52-pin plastic leadless chip carrier providing high board level packing densities.

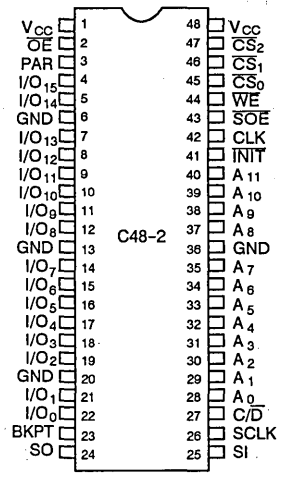
The IDT71502 is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



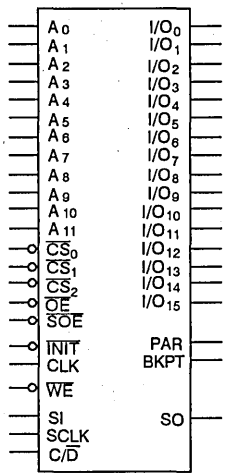
CEMOS is a trademark of Integrated Device Technology, Inc.

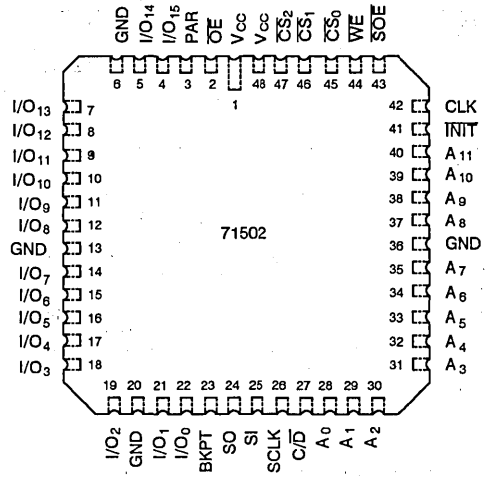
PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



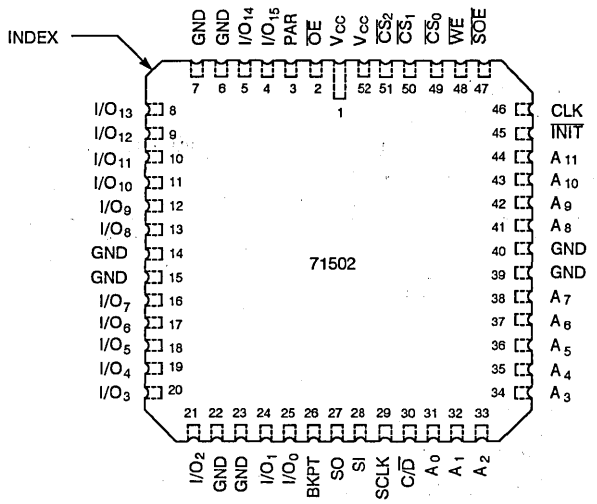


LCC PINOUT
TOP VIEW

PIN NAMES

NAME	FUNCTION
A_{0-11}	Address
I/O_{0-15}	Data Input/Output
$\overline{CS}_{0-2}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{SOE}$	Synchronous Output Enable
CLK	Clock (to register)
$\overline{INIT}$	Initialize
BKPT	Breakpoint Detect
PAR	Parity
SI	SPC Serial $DATA_{IN}$ (1)
SO	SPC Serial $DATA_{OUT}$ (1)
SCLK	SPC Clock (1)
C/$\overline{D}$	SPC Command/$\overline{Data}$ (1)
GND	Ground
V_{CC}	Power

NOTE:
1. The Serial Protocol Channel (SPC) is discussed at length in IDT Application Note 16.



PLCC PINOUT
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (1) (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE - READ/WRITE OPERATIONS STANDARD PIPELINED MODE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{SOE}$	CLK	I/O OPERATION
Deselected	H	X	L	X	↓	High Z
Read	L	H	H	X	X	High Z
Read	L	H	L	H	↓	High Z
Read	L	H	L	L	↓	$DATA_{OUT}$ @ Address
Write	L	L	X	X	X	$DATA_{IN}$ @ Address

TRUTH TABLE - SPC OPERATIONS

MODE	C/$\overline{D}$	SCLK	FUNCTION
Command	H	↓	Shift bit into command register
Data	L	↓	Shift bit into data register
Execute	↑	↓	Execute command during time between C/$\overline{D}$ and SCLK

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71502S MIN.	IDT71502S TYP.(1)	IDT71502S MAX.	IDT71502L MIN.	IDT71502L TYP.(1)	IDT71502L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage(2)	I_{OL} = 16mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
V_{OH}	Output High Voltage(2)	I_{OH} = -8mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage, BKPT	I_{OL} = 24mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. All outputs except BKPT, which is open drain.

4

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	POWER	IDT71502S25(2, 4) IDT71502L25(2, 4) COM'L.	IDT71502S35(4) IDT71502L35(4) COM'L.	IDT71502S35(4) IDT71502L35(4) MIL.	IDT71502S45(4) IDT71502L45(4) COM'L.	IDT71502S45(4) IDT71502L45(4) MIL.	IDT71502S55(3, 4) IDT71502L55(3, 4) COM'L.	IDT71502S55(3, 4) IDT71502L55(3, 4) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	155	155	170	155	170	155	170	mA
		L	135	135	150	135	150	135	150	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} = 1/TRC	S	280	255	270	230	245	220	235	mA
		L	250	225	240	200	215	190	205	

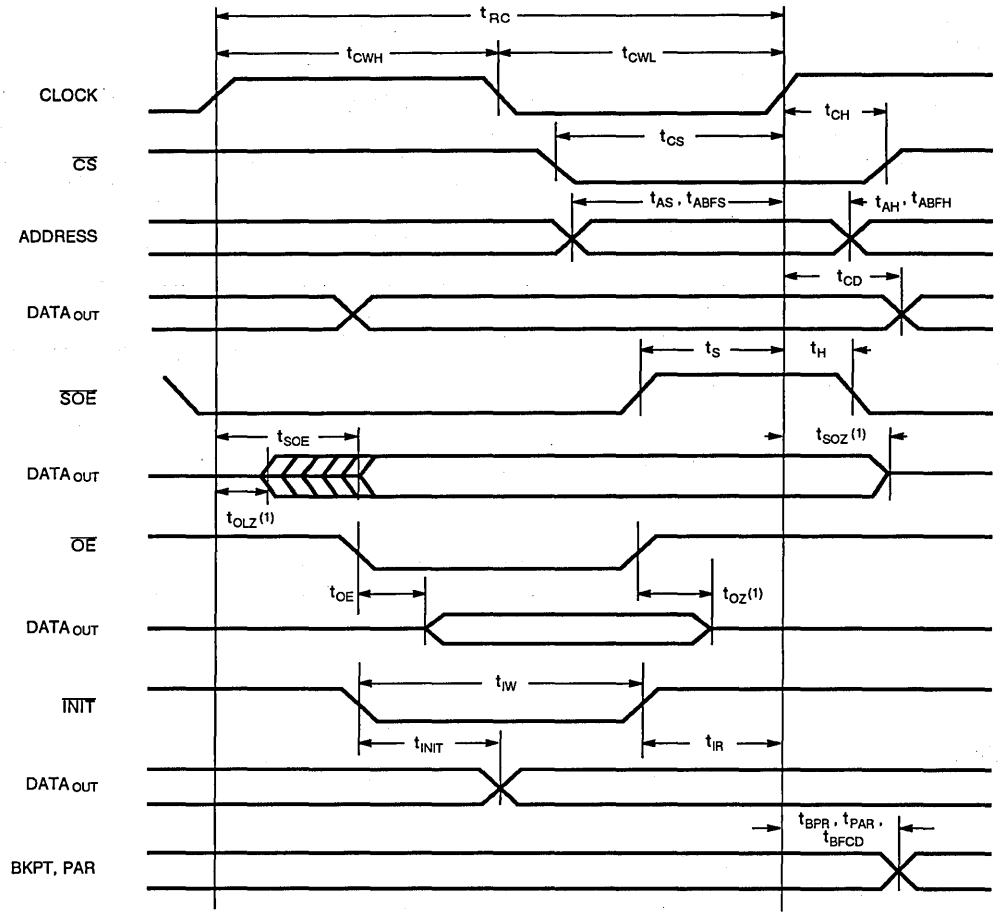
NOTES:
1. All values are guaranteed maximums.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. Pipelined address access set-up time.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
READ CYCLE – PIPELINED										
t_{RC}	Read Cycle Time	40	–	50	–	65	–	80	–	ns
t_{AS}	Address Set-up Time	25	–	35	–	45	–	55	–	ns
t_{CS}	Chip Select Set-up Time	10	–	12	–	15	–	20	–	ns
t_S	Set-up Time: $\overline{SOE}$	10	–	12	–	15	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	0	–	ns
t_{CH}	Chip Select Hold Time	2	–	2	–	2	–	2	–	ns
t_H	Hold Time: $\overline{SOE}$	2	–	2	–	2	–	2	–	ns
t_{CD}	Clock to Output Delay	–	12	–	15	–	20	–	25	ns
t_{CWH}	Clock Width, High	15	–	15	–	20	–	20	–	ns
t_{CWL}	Clock Width, Low	15	–	15	–	20	–	20	–	ns
t_{OE}	Asynchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{OZ}	Asynchronous Output Disable Time[3][5]	–	11	–	14	–	19	–	24	ns
t_{SOE}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{SOZ}	Synchronous Output Disable Time[3][5]	–	11	–	14	–	19	–	24	ns
t_{INIT}	Initialize to Output Delay	–	45	–	50	–	65	–	80	ns
t_{IR}	Initialize Recovery Time	30	–	35	–	45	–	55	–	ns
t_{IW}	Initialize Pulse Width	30	–	35	–	45	–	55	–	ns
t_{PAR}	Parity Generation Time	–	30	–	35	–	45	–	55	ns
t_{BPR}	Breakpoint Delay From Register	–	35	–	35	–	45	–	55	ns
t_{BPA}	Breakpoint Delay From Address	–	35	–	35	–	45	–	55	ns
t_{ABFS}	Address to BKPT FF Set-up	30	–	35	–	40	–	50	–	ns
t_{ABFH}	Address to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{BFCD}	BKPT FF Clock to Data	–	16	–	20	–	25	–	30	ns
READ CYCLE – NON-PIPELINED										
t_{AAN}	Address Access Time	–	30	–	35	–	65	–	80	ns
t_{OLZ}	Asynchronous Output Enable Time[3][5]	2	–	2	–	2	–	2	–	ns
t_{SOEN}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{CAN}	Chip Select Access Time	–	15	–	20	–	30	–	35	ns
t_{ASPN}	Address Set-up Parity Time	40	–	50	–	65	–	80	–	ns
t_{AABN}	Address Access to Breakpoint	–	55	–	65	–	80	–	95	ns
t_{AABFS}	Address Access to BKPT FF Set-up	40	–	50	–	65	–	80	–	ns
t_{AABFH}	Address Access to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{PFCD}	Parity Flip-Flop Clock to data	–	12	–	15	–	20	–	25	ns

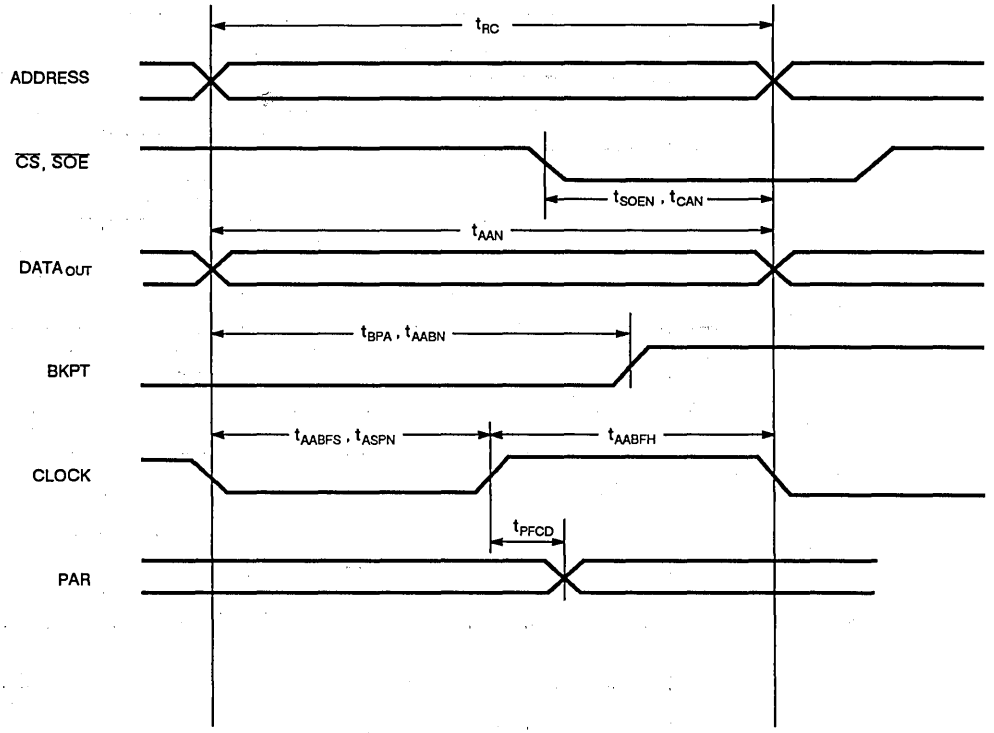
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Pipelined address access set-up time.
5. Transition is measured ±500mW from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 1



NOTE:
1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 – NON-PIPELINED



NOTE:

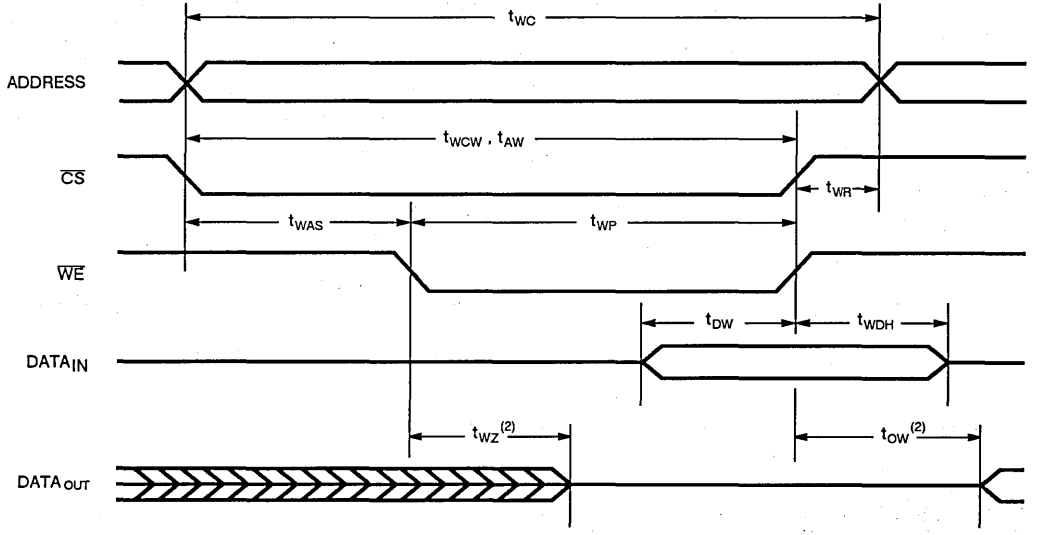
1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25 (1, 4) IDT71502L25 (1, 4) MIN.	MAX.	IDT71502S35 (4) IDT71502L35 (4) MIN.	MAX.	IDT71502S45 (4) IDT71502L45 (4) MIN.	MAX.	IDT71502S55 (2, 4) IDT71502L55 (2, 4) MIN.	MAX.	UNIT
RAM WRITE CYCLE										
t_{WC}	RAM Write Cycle Time	40	–	50	–	65	–	80	–	ns
t_{WAS}	RAM Write Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	RAM Write Pulse Width (5)	20	–	25	–	35	–	45	–	ns
t_{DW}	RAM Write Data Set-up Before End Of Write	15	–	17	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	50	–	60	–	ns
t_{WCW}	Chip Select To End Of Write	25	–	30	–	50	–	60	–	ns
t_{WDH}	RAM Write Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output Hi-Z (3, 6)	–	15	–	15	–	20	–	20	ns
t_{OW}	Output Active from End of Write (3, 6)	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.
5. $\overline{OE}$ = V_{IH}.
6. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE (1)



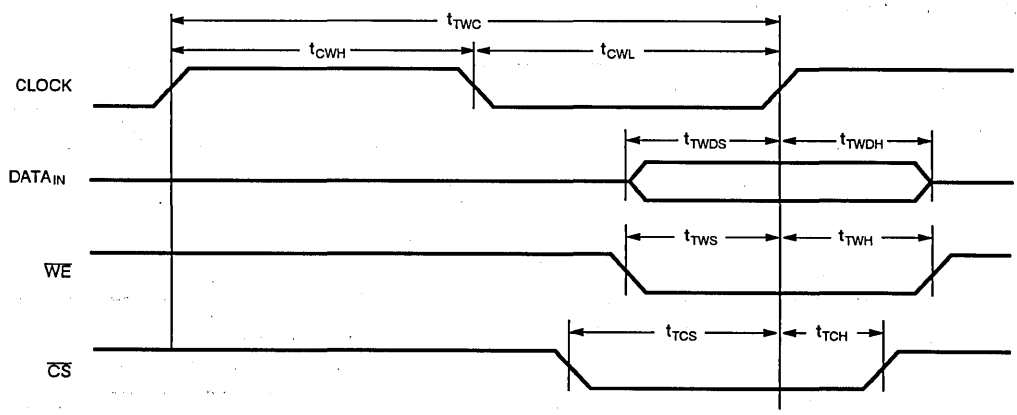
NOTE:
1. A write occurs during the overlap of both $\overline{CS}$ and $\overline{WE}$ low.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
TRACE WRITE CYCLE										
t_{TWC}	Trace Write Cycle Time	40		50	–	65	–	80	–	ns
t_{TWDS}	Trace Write Data Set-up Time	8		10	–	12	–	15	–	ns
t_{TWDH}	Trace Write Data Hold Time	2	–	2	–	2	–	2	–	ns
t_{TWS}	Trace Write Enable Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TCS}	Trace Write Chip Select Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TWH}	Trace Write Enable Hold Time	2	–	2	–	2	–	2	–	ns
t_{TCH}	Trace Write Chip Select Hold Time	2	–	2	–	2	–	2	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.

TIMING WAVEFORM OF TRACE WRITE CYCLE[1]



NOTE:
1. A write occurs if both $\overline{CS}$ and $\overline{WE}$ are low at the clock low-to-high transition

AC TEST CONDITIONS (Read and Write Cycles)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

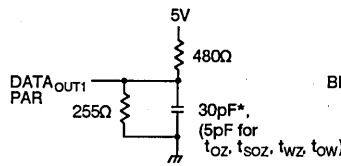


Figure 1. Output Load, Parity Output

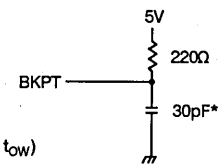


Figure 2. Output Load (for BKPT pin)

*Includes scope and jig.

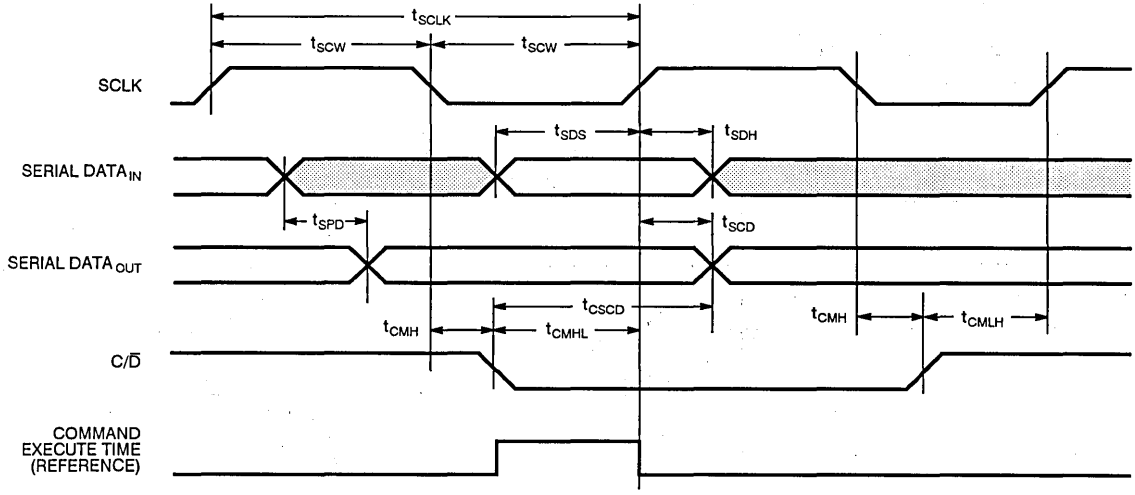
SPC AC ELECTRICAL CHARACTERISTICS [1] V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	IDT71502S/L[1] MIN.	MAX.	UNIT
t_{SCLK}	SCLK Period	100	–	ns
t_{SCW}	SCLK Pulse Width	40	–	ns
t_{SDS}	Serial Data Set-up Time	20	–	ns
t_{SDH}	Serial Data Hold Time	2	–	ns
t_{SCD}	Clock to serial Data Output Delay	–	30	ns
t_{SPD}	Serial Data-In-to-Out Delay, Stub Mode	–	20	ns
t_{CMLH}	Command/Data Set-up Time, Low-to-High[2]	20	–	ns
t_{CMHL}	Command Set-up Time, High-to-Low (Execution Time)[2]	35	–	ns
t_{CMH}	Command/Data Hold Time[2]	5	–	ns
t_{CSCD}	Command/Data to Serial Data Output Delay (1st Bit Only)	–	45	ns

4

NOTES:
1. These specifications apply to all speed grades of the product.
2. C/$\overline{D}$ cannot change while SCLK is high.

TIMING WAVEFORM OF SPC CHANNEL



AC TEST CONDITIONS (SPC)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

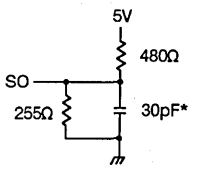
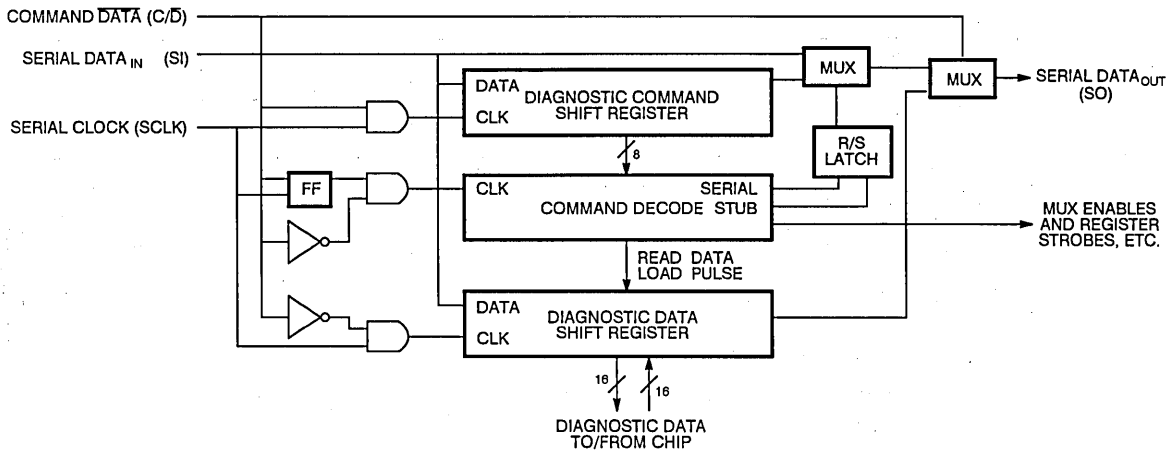


Figure 3. Output Load for Serial Output

*Includes scope and jig.

SPC FUNCTIONAL BLOCK DIAGRAM



SPC COMMAND FORMAT

7 4	3 0
SPC Command Code 4 bits	SPC Register Code 4 bits

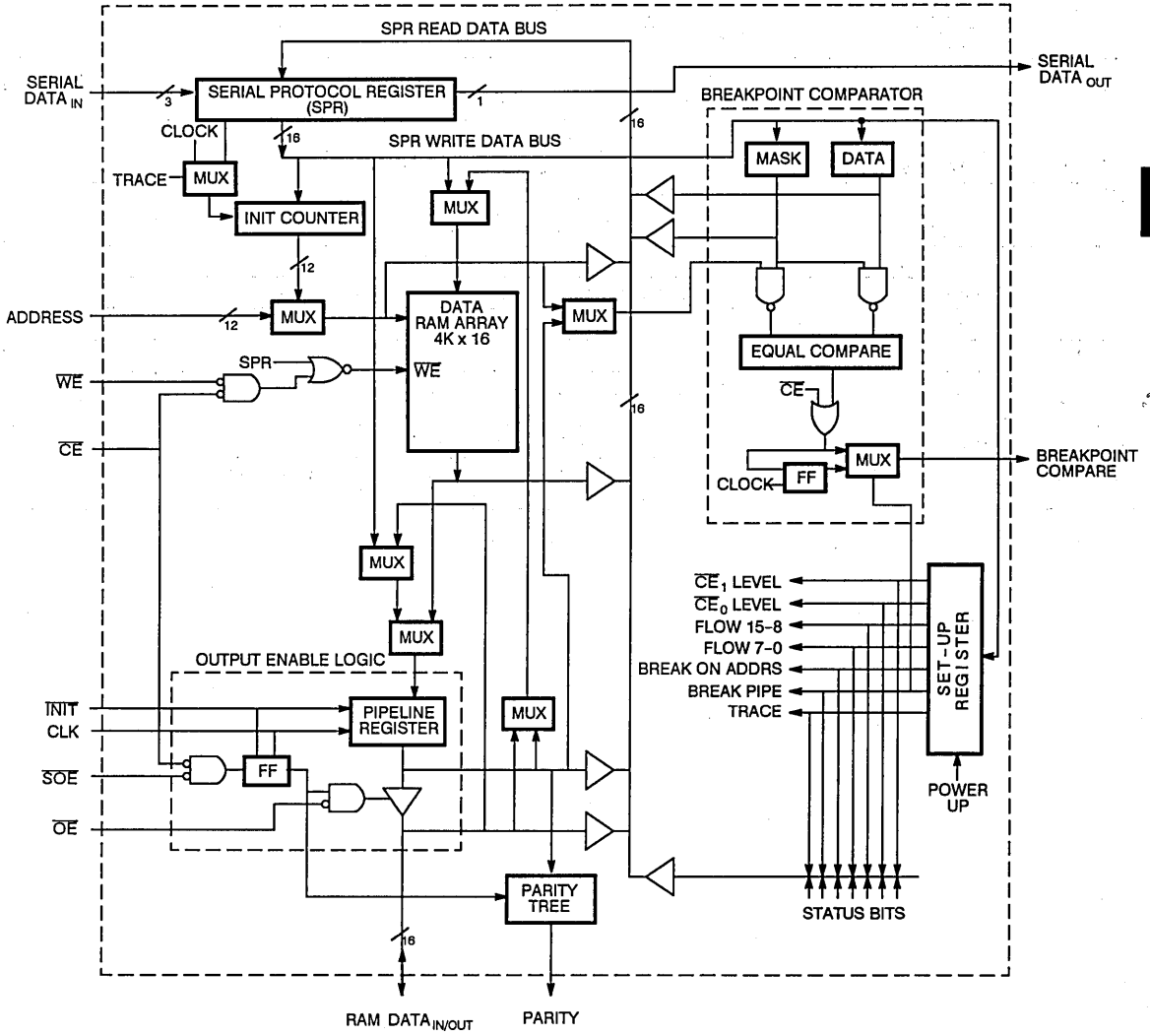
SPC COMMAND CODES

COMMAND CODE	READ/WRITE FUNCTION	ACTION	NOTES
0	Read	Read Register	Uses Register Select Field
1	Write	Write Register	Uses Register Select Field
2	Read	Read Register and Increment Initialize Counter	Serial RAM Read
3	Write	Write Register and Increment Initialize Counter	Serial RAM Write
4-C	–	Reserved (No-Op)	–
D	Write	Stub Diagnostic	Broadcast Commands
E	Write	Serial Diagnostic	Serial Commands
F	–	No-Op	Guaranteed No-Op

SPC REGISTER CODES

REGISTER CODE	READ/WRITE FUNCTION	REGISTER	NOTES
0	R/W	Initialize Counter	–
1	R/W	RAM Output (or Input if reading)	–
2	R/W	Pipeline Register	–
3	R/W	Break Mask Register	–
4	R/W	Break Data Register	–
5	R/W	Set-up + Status Register	Break Multiplexer, Trace Mode, etc.
6	Rd Only	I/O_{15} - I/O_0 (Data Pins)	Data Pins of Chip
7	Rd Only	RAM Address	Address Going into RAM
8-F	–	Reserved (unused)	–

REGISTERED RAM DATA FLOW BLOCK DIAGRAM



SET-UP REGISTER FORMAT

BIT	NAME	TYPE[1]	FUNCTION	POWER-UP VALUE
15	CE	RO	Chip Enable State: NOR of All Chip Enable Pins	0
14	$\overline{SOE}$ FF	RO	$\overline{SOE}$ FF State: 1 = Output Enabled, 0 = Output Disabled	0
13	$\overline{SOE}$ Pin	RO	$\overline{SOE}$ Pin State: 1 = High, 0 = Low	0
12	$\overline{OE}$ Pin	RO	$\overline{OE}$ Pin State: 1 = High, 0 = Low	0
11	$\overline{WE}$ Pin	RO	$\overline{WE}$ Pin State: 1 = High, 0 = Low	0
10	$\overline{INIT}$ Pin	RO	$\overline{INIT}$ Pin State: 1 = High, 0 = Low	0
9	BP Compare	RO	Breakpoint Comparator Output: 1 = Compare Valid	0
8	BP Pin	RO	BP Pin State: 1 = High, 0 = Low	0
7	$\overline{CS}_1$ Level	R/W	0 = $\overline{CS}_1$ is Low Active; 1 = CS_1 is High Active	0
6	$\overline{CS}_0$ Level	R/W	0 = $\overline{CS}_0$ is Low Active; 1 = CS_0 is High Active	0
5	Non-Reg High	R/W	Set Pipeline Register Bits 15-8 to Flow-Through Mode	0
4	Non-Reg Low	R/W	Set Pipeline Register Bits 7-0 to Flow-Through Mode	0
3	–	–	(Unused)	0
2	BC Address	R/W	0 = Breakpoint on Pipeline Register Output, 1 = Breakpoint on RAM Address Inputs	0
1	BC Pipelined	R/W	Set Breakpoint Output MUX for Pipeline FF Output	0
0	Trace Mode	R/W	Set for Trace Mode: I/O_{15-0} to Pipeline Register, Pipeline Register to RAM, Initialize Counter as Address, Write with Clock Pulse	0

NOTE:
1. RO means Read Only. R/W means Read/Write.

GENERAL DESCRIPTION

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and read-back of the RAM data. A RAM address counter is also provided to speed up RAM load and read-back. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 Registered RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize register as the address counter. The Trace mode, in combination with the breakpoint comparator, allows the IDT71502 Registered RAM to be used as a one-chip logic analyzer.

RAM Operation

After power up, and in its typical operating mode, the IDT71502 Registered RAM is set for pipelined read and direct (non-pipelined) write. Data may be directly written into the RAM by driving the address and data inputs and strobing the Write Enable input. Data is read from the RAM by driving the address lines and clocking the pipeline register.

The RAM may also be read and written by the Serial Protocol Channel (SPC). This is the typical path for loading the RAM after power up.

Serial Protocol Channel

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. A block diagram of the command decode logic is shown for reference. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (NOTE: The data to the SPC is shifted in LSB first.)

The SPC is connected to the outside world through four wires. These wires consist of serial data in and out, a shift clock and a command/$\overline{\text{data}}$ line. When the command/$\overline{\text{data}}$ line is high, commands are shifted from the serial data in to the command register by the clock. When the command/$\overline{\text{data}}$ line is low, data is shifted into the data shift register by the clock. When the command/data line transitions from high (command) to low (data), a clock pulse is generated internally to the command decode logic. This pulse lasts from the beginning of the high-to-low transition to the next serial clock pulse and is used to execute the command in the command register.

Two of the defined commands are Serial and Stub. These commands control a latch which determines the source of the serial data out in the command mode. The Serial command causes the data output to be taken from the last stage of the command shift register. This is the normal operating mode, where all the shift registers in a system are connected into one long shift register. The SPC logic in the IDT71502 is automatically set to the Serial mode by power up. The Stub command sets the latch and causes the serial output data to be taken from the serial input. In this mode, the serial data is passed directly from one chip to the next so that all command registers have the same data at their serial inputs. This allows a broadcast mode where all command registers in a system can be loaded with the same command at the same time.

RAM Load/Readback Logic

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

A detailed block diagram of the IDT71502 Registered RAM, showing the various internal registers and the load and readback paths, is shown in the Registered RAM Data Flow Block Diagram. In addition to the logic shown in the Functional Block Diagram on the first page of the data sheet, there is an Initialize Counter for loading and initializing the RAM, Break Data and Mask registers for the Breakpoint Comparator and multiplexers at the input to the Pipeline register for allowing data from the data I/O pins to be clocked into the Pipeline register in the Trace mode before being written into the RAM. The data flow block diagram also shows the various multiplexers for routing data for breakpoint and readback use.

Initialize Counter

The Initialize Counter provides the initial address to the RAM after reset of the part. A pulse applied to the Initialize pin causes the Initialize Counter to be gated to the RAM address and the RAM data to be preset into the pipeline register. This provides an initial value in the pipeline register before the first clock pulse arrives. The Initialize Counter can be reset to zero at power up of the chip and can be loaded with a value other than zero by the SPC. Once loaded with a value by the SPC, this value is used in further chip reset operations.

Set-up Register

The Set-up Register is a 16-bit register used to set the chip operating mode and to read back chip operating status conditions. A command word written into the Set-up Register sets 7 latches which control the chip operating conditions. Reading the Set-up Register provides the current status of these 7 latches and various other signals on the chip. At power up, the 7 latches are cleared to zero and the Initialize counter is cleared to zero. The format of the Set-up Register is shown in the Set-up Register Format table.

The Set-up Register has 7 latches which determine the operating mode of the chip. These are $\overline{CS}_1$, $\overline{CS}_0$, Non-Reg High, Non-Reg Low, BC RAM, Break Pipe and Trace. The $\overline{CS}_1$ and $\overline{CS}_0$ bits determine the polarity of the $\overline{CS}_1$ and $\overline{CS}_0$ chip enables. The Non-Reg High and Low bits set the upper and lower bytes of the Pipeline Register to a flow-through mode, respectively. The BC RAM bit determines the source of the data for breakpoint comparison, either the Pipeline Register or the RAM address. The Break Pipe latch switches the breakpoint pin multiplexer from the comparator to the buffer flip-flop. The trace latch sets the chip into the Trace mode.

Power Up State

Power up is defined as taking V_{CC} from below 1.0 volts to 5.0 volts nominal. This generates power up reset, an internal signal which resets several registers on the chip. After power up, the IDT71502 is in the following state:

- Set-up Register cleared to zero
- Initialize Counter cleared to zero
- Breakpoint Mask Register cleared to equal (Breakpoint output high)
- $\overline{SOE}$ Flip-Flop cleared to outputs off

Note that taking V_{CC} from 5.0 volts to 2.0 volts and back to 5.0 volts will not cause power up reset.

Set-up Register: Programmable Chip Enable

The chip enable function is programmable by bits in the Set-up Register. The logic for this is shown in Figure 1. The bits in the Set-up Register define the active state of each chip enable: high or low. This allows up to four RAMs to be cascaded in depth with no external decoders required (16K x 16 bits of RAM).

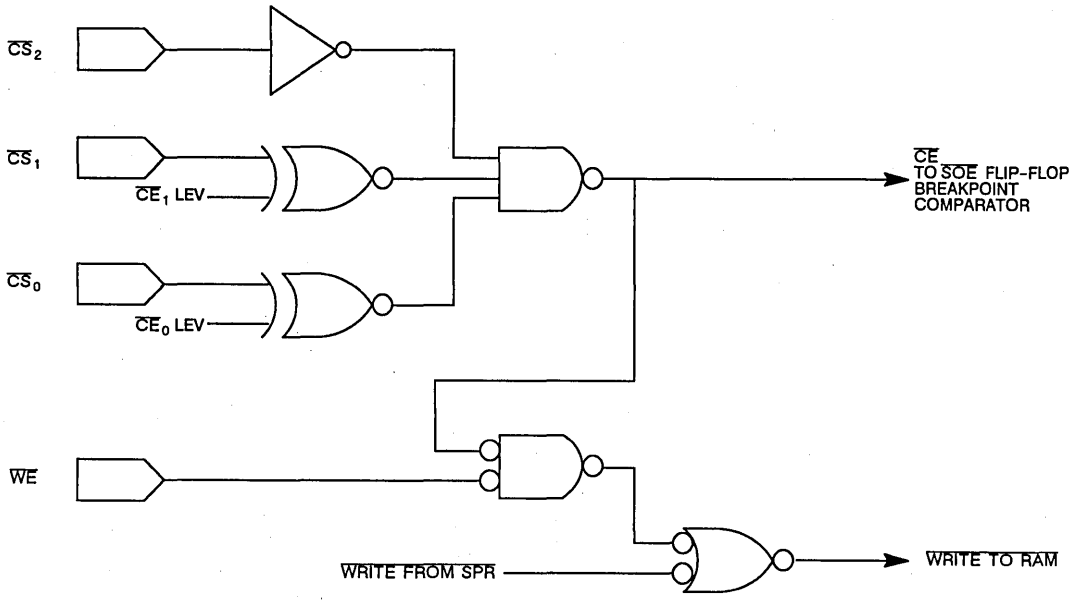


Figure 1. Chip Enable Logic Block Diagram

Set-up Register: Non-Registered Outputs

Two bits of the Set-up Register, Non-Reg Hi and Non-Reg Lo, can be set to cause the Pipeline Register bits 15-9 and 7-0, respectively, to be set to the flow-through mode. In the flow-through mode, both latches of the register are open and the register acts like a simple buffer with its output following its input. This allows the user to have some non-registered bits in microcode applications. The output circuit consisting of the Pipeline Register, the Synchronous Output Enable ($\overline{SOE}$), and the Output Enable ($\overline{OE}$), has some special logic to support this mode, as shown in Figure 2. Also, activating the Initialize pin causes the Pipeline Register to be put in the flow-through mode. Figure 2 shows the Pipeline Register as two latches operated in the MASTER/SLAVE configuration. The clock input will cause the latch pair to work as a register. If the Initialize pin is activated, both registers will be placed in the flow-through mode by the OR gates. Also, if either Non-Reg bit is set, its corresponding 8-bit portion of the register will be placed in the flow-through mode.

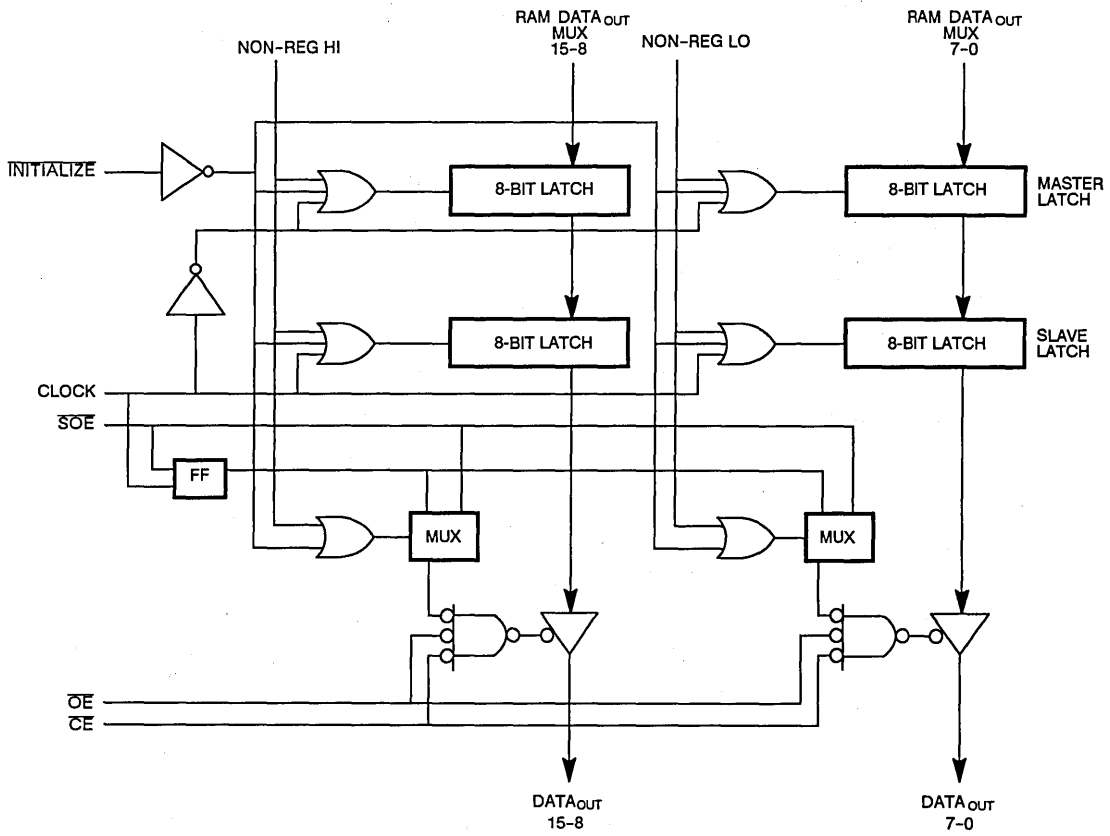


Figure 2. Output Logic Block Diagram

When in the flow-through mode, the output enable flip-flop for that half must also be in the flow-through mode for external chip expansion to work properly. A non-registered RAM bit must be enabled by a non-registered output enable, while a registered bit must be enabled by a synchronous output enable. This is done by using the non-registered bit to control a multiplexer which selects between the $\overline{SOE}$ flip-flop input and output as the source of the output enable.

Set-up Register: Breakpoint Comparator Control

The Breakpoint Comparator (BC) provides a masked 16-bit comparison of the various data paths that can be read by the SPC. It consists of an equal-comparator and the Break Data and Mask registers, as shown in Breakpoint Comparator Logic Block Diagram (Figure 3). The BC compares the data from the chip against the data In the Break Data Register and activates the Breakpoint Compare output if the two are equal. The Mask Register enables comparison: if a bit in the Mask Register is a one, comparison is enabled on the corresponding bit in the Break Data Register. If it is zero, the comparison on the that bit is disabled: i.e., forced to equal.

The Breakpoint output is an open drain type to allow width expansion of the Breakpoint Comparison. For example, if two IDT71502 chips have their breakpoint pins tied together to the same load resistor, both breakpoint comparators must be valid before the output can rise. The result is a 32-bit comparison.

A selectable flip-flop is provided for the Breakpoint Output. This allows pipeline registered bits, non-registered bits and address bits to be used in comparison with the same timing. Breakpoint comparison is commonly performed on the pipeline register outputs. These outputs are valid after the clock; i.e. for the current cycle. Address inputs and non-pipelined outputs are valid before the clock, representing address and data for the next cycle, respectively. If address or non-pipelined outputs are to be used in breakpoint comparison, a flip-flop delay must be added so that they will be valid after the clock in the same manner as pipelined bits. The selectable flip-flop provides this delay so that all breakpoint comparison outputs are valid in the current cycle.

The Breakpoint output driver is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the comparison. $\overline{SOE}$ must be low prior to clock going high whether in pipelined mode or not.

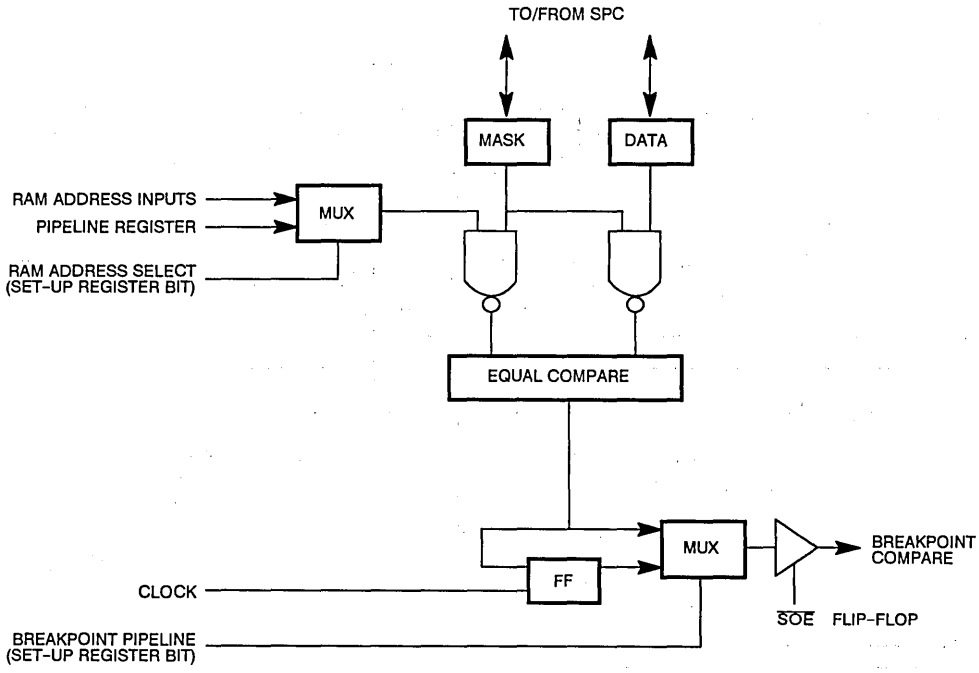


Figure 3. Breakpoint Comparator Logic Block Diagram

Set-up Register: Trace Mode Operation

When the trace bit in the Set-up Register is set, the chip is in the Trace mode. In this mode, data from the chip data pins, I/O_{15} - I/O_0, is written into sequential locations in the RAM . The address for the RAM comes from the Initialize Counter, which is incremented after each RAM write. The Trace mode is used to record external data events in the same manner as a logic analyzer. The Trace mode recording sequence is as follows:

1. Data from the I/O pins is written into the Pipeline Register by the clock.
2. Data in the Pipeline Register is written into the RAM by a one-shot driven by the trailing edge of the clock. The RAM address comes from the Initialize Counter.
3. The Initialize Counter is incremented by the trailing edge of the RAM write pulse.

Trace operation requires both $\overline{WE}$ and $\overline{CS}$ to be active. If either is inactive (high), the Initialize Register will not be incremented and data will not be written into the RAM. The Pipeline Register will be loaded, however. This allows the write enable to be used for skipping words. A timing diagram of this logic is shown in the Trace Mode Sequence Timing Diagram (Figure 4).

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

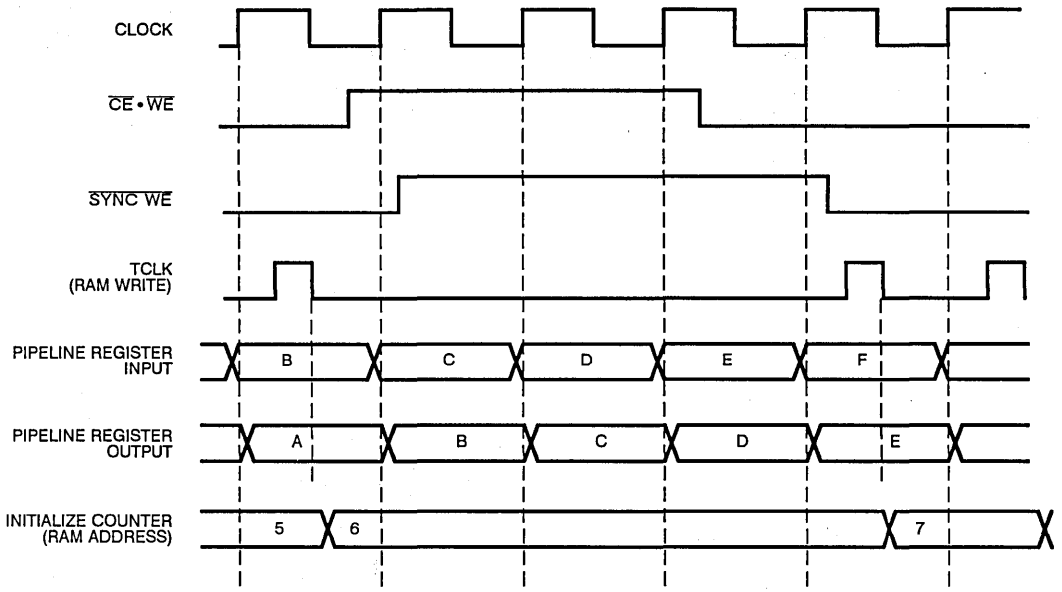


Figure 4. Trace Mode Sequence Timing Diagram

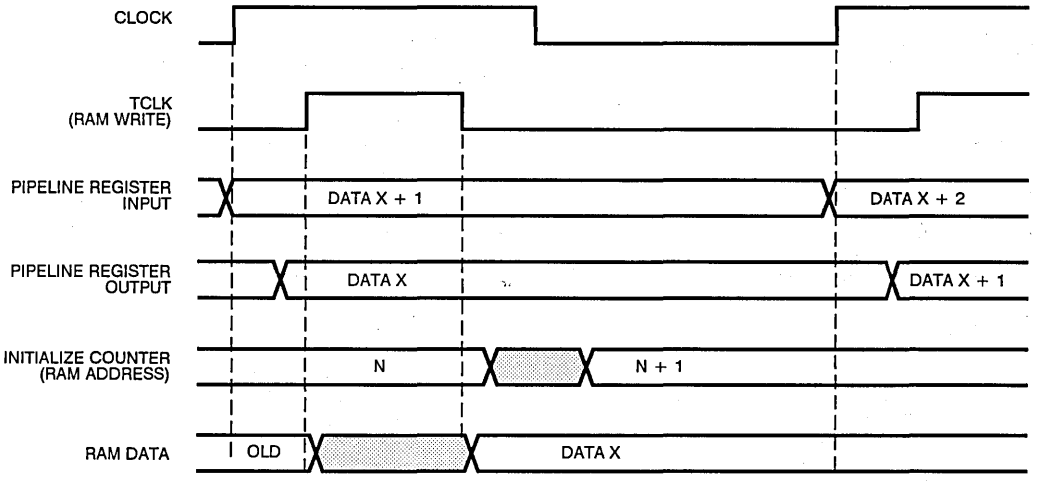


Figure 5. Trace Mode Clock Timing Diagram

Parity Output

The Parity Output pin is generated from a 16-bit parity tree, as shown in the Parity Tree Logic Block Diagram (Figure 6). Even parity is used. Parity is generated on the contents of the Pipeline Register. The parity output driver is three-state and is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the parity output.

The Parity Output always reflects the parity of the registered value. Additional flip-flops and multiplexers are included in the parity tree to cover the case of non-registered outputs. If one or both bytes of the Pipeline Register are set to the Non-Registered mode, a flip-flop pipeline delay is added to the corresponding byte parity chain to make the result of that byte parity calculation the same as if the Pipeline Register was not in the Non-Pipelined mode. $\overline{SOE}$ must be low prior to the clock going high in pipelined or non-pipelined mode.

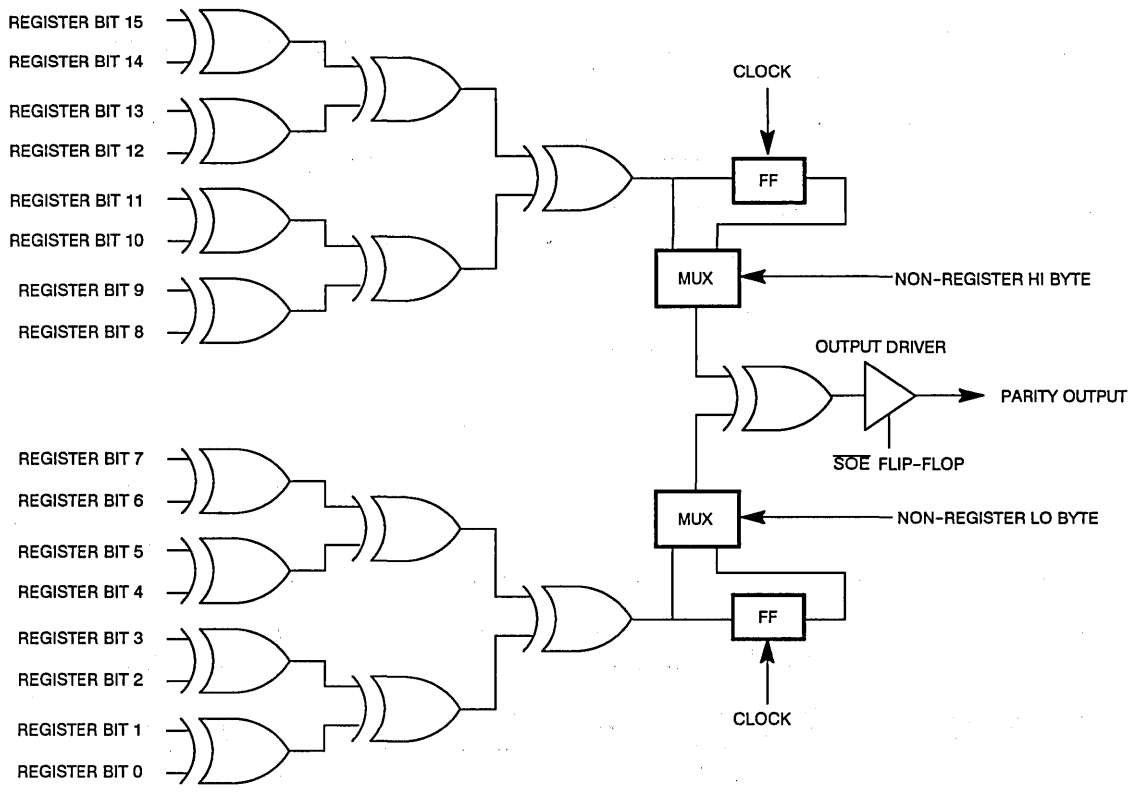


Figure 6. Parity Tree Logic Block Diagram

REGISTERED RAM APPLICATIONS

Using the Registered RAM in Writable Control Stores

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. A simplified block diagram of a 16-bit microprogram-controlled system using the IDT71502 is shown in Writable Control Store Using Registered RAM (Figure 7). The system shown uses four IDT71502 Registered RAM chips to provide 4K x 64 bits of microcode writable control store.

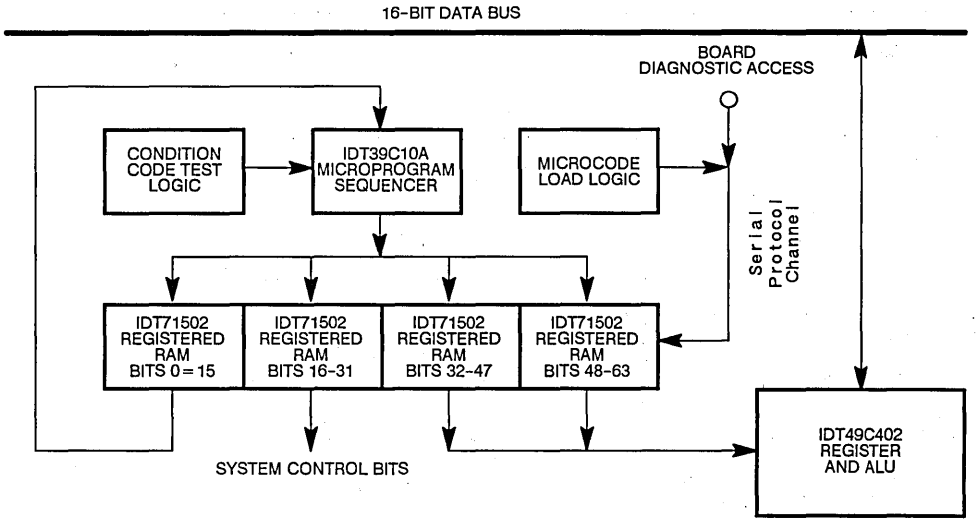


Figure 7. Writable Control Store Using Registered RAM

Using the Parity Output

The parity output can be used in conjunction with an additional IDT71502 Registered RAM to provide parity checking for control stores. This is shown in the Parity Check in a Writable Control Store System (Figure 8) block diagram. The parity output driver is gated by the $\overline{SOE}$ Flip-Flop. This allows simple depth expansion of the parity function by paralleling the parity outputs in the same manner as the data outputs, as shown in the Parity Check in a Depth Expanded Writable Control Store System (Figure 9) block diagram.

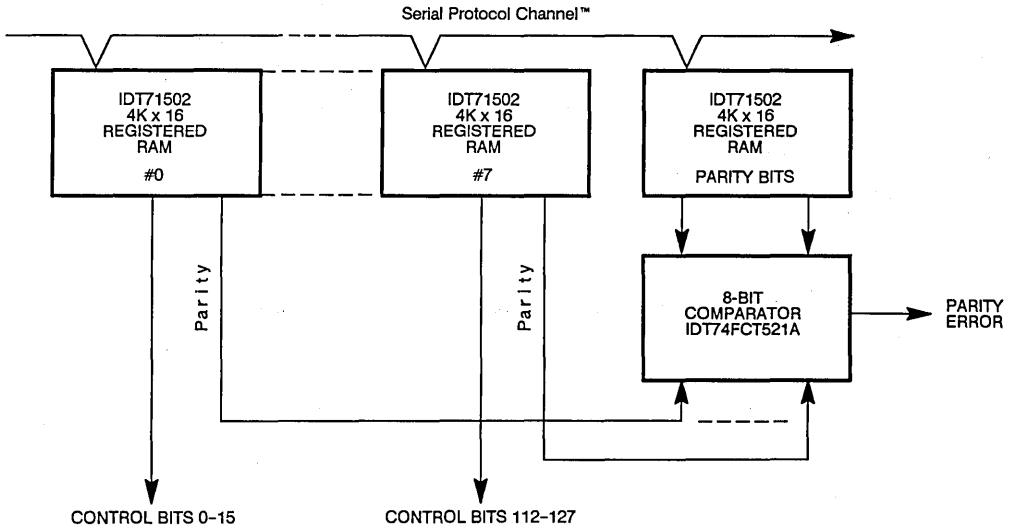


Figure 8. Parity Check In a Writable Control Store System

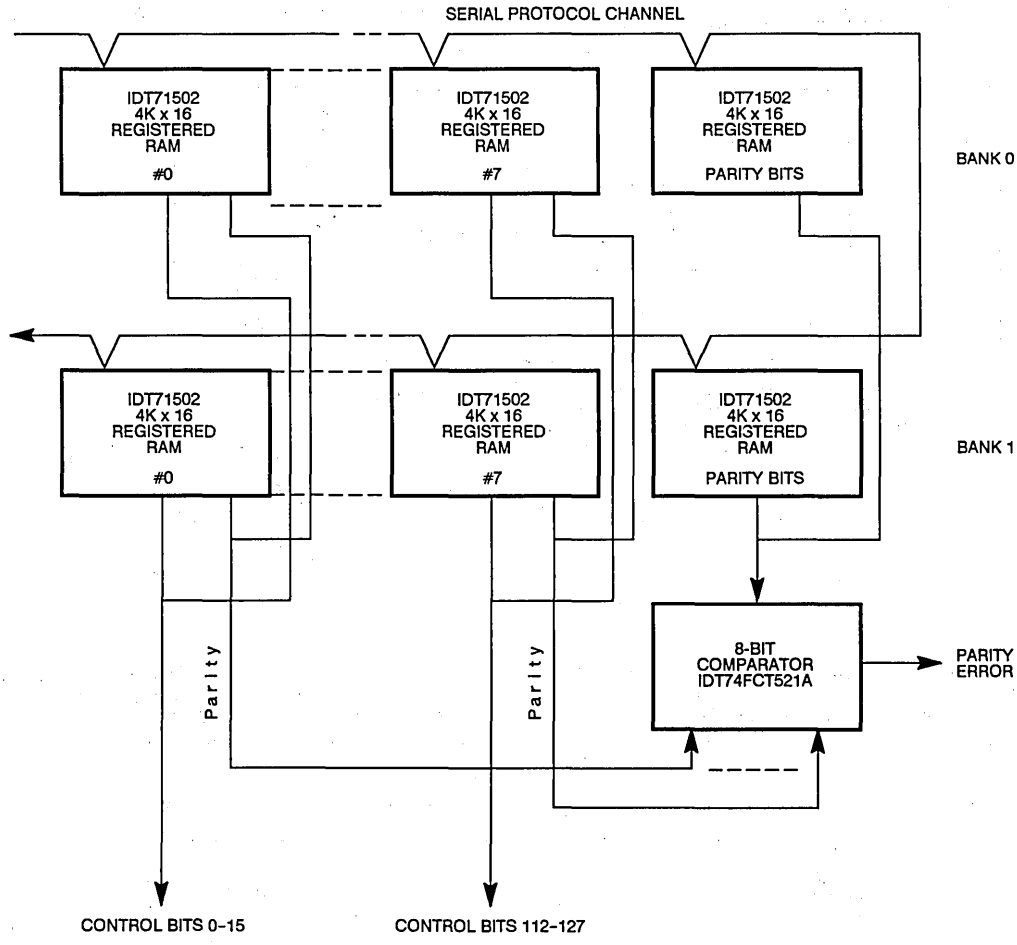


Figure 9. Parity Check in a Depth Expanded Writable Control Store System

Using Trace Mode as a Logic Analyzer

The Trace mode allows the IDT71502 to be used as an on-board logic analyzer for system diagnostics. It is particularly powerful when used in conjunction with the Breakpoint function. In the Trace mode, data is recorded in sequential locations in the RAM as controlled by the Trace Counter. Since the incoming data is clocked into the pipeline register, the set-up and hold times are short and compatible with capturing changing bus data, for example. A block diagram of a system with an IDT71502 used in the Trace mode is shown in Diagnostic Bus Monitoring Using Trace Mode (Figure 10).

The Breakpoint outputs from the IDT71502 devices in a system can be used to control the Trace mode writing. The Breakpoint outputs are open drain types which provide a wire-AND function when connected together to a single pull-up resistor. By tying the Breakpoint outputs for the writable control store RAMs and the trace RAM, a breakpoint comparison can be made over the full microcode word plus the data bus contents. This comparison can be used to enable the trace write so that only data which occurred at the Breakpoint times is recorded. This allows recording the data that was on the bus during each instance of an I/O write, for example.

4

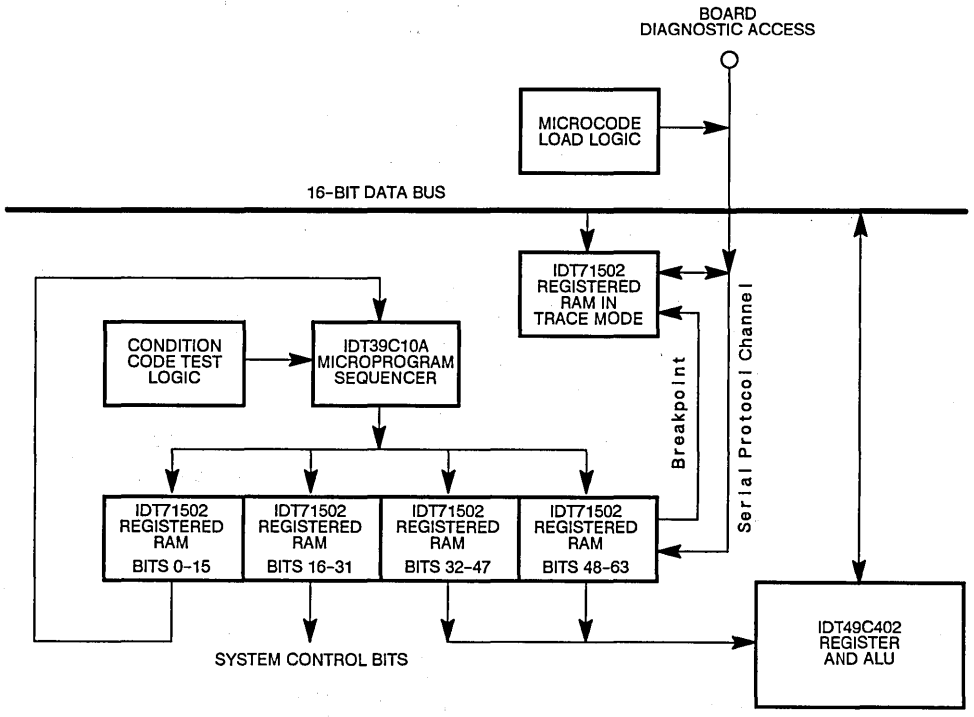


Figure 10. Diagnostic Bus Monitoring Using Trace Mode

Serial Loading of the IDT71502 Using the SPC

In order to use the IDT71502 in writable control store applications, it must be loaded with the microprogram before use. This is done using the Serial Protocol Channel (SPC). Loading the RAM over the SPC can be done in several ways. The microcode can be loaded from a central microprocessor, which can perform both microcode load and system diagnostics at power up, or it can be loaded using dedicated load logic.

An example of a design of this dedicated load logic is shown in the Microcode Load Logic Example (Figure 11). The purpose of this example is to show how one goes about designing this logic. This example shows an approach which loads the RAMs with data from a single EPROM. The load logic gets the SPC command and data information from the EPROM. It is controlled by single byte instructions from the same EPROM. The format of these instructions is shown in Microcode Load Logic Instruction Formats (Figure 12), and a map of the typical contents of the EPROM is shown in Microcode Load EPROM Memory Map (Figure 13).

The load logic consists of a 16-bit address counter, an 8-bit shift register, a 4-bit byte counter and a PAL containing a 2-bit instruction register. The logic in the PAL interprets the 2-bit load instructions to cause bytes of command or data information to be loaded into the IDT74FCT299 shift register and shifted to the SPC. The two IDT74FCT161 counters are used to count the bytes being sent and the 8 bits in each byte.

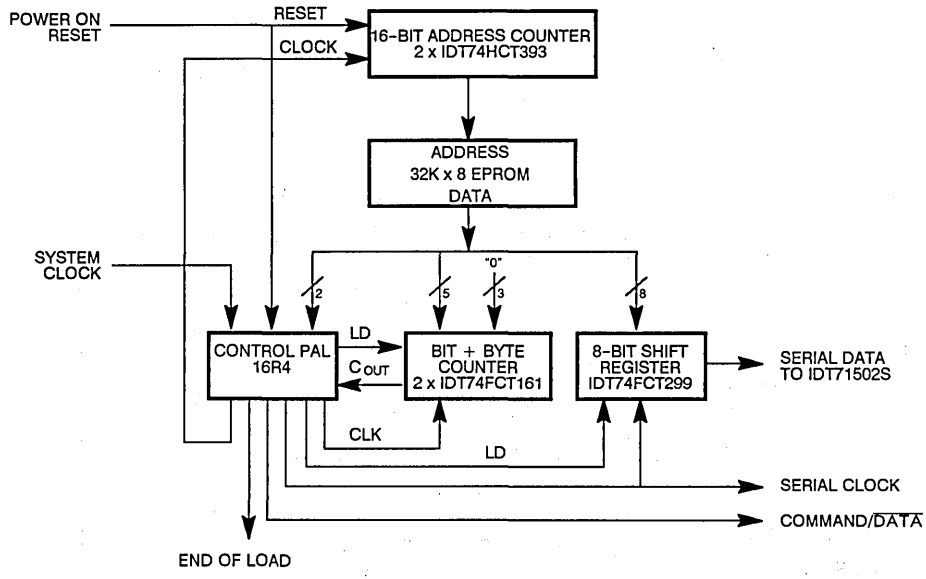


Figure 11. Microcode Load Logic Example

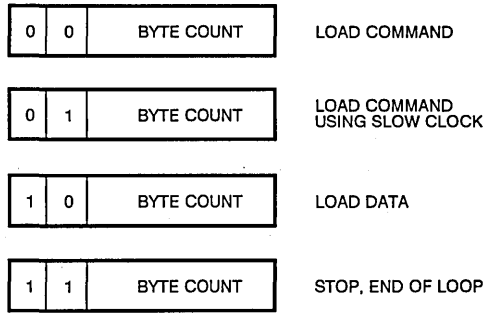


Figure 12. Microcode Load Logic Instruction Formats

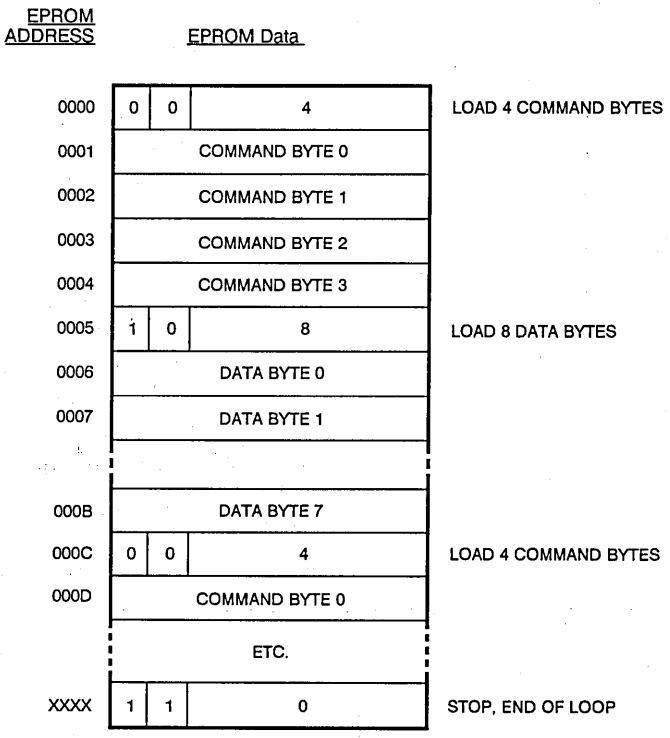
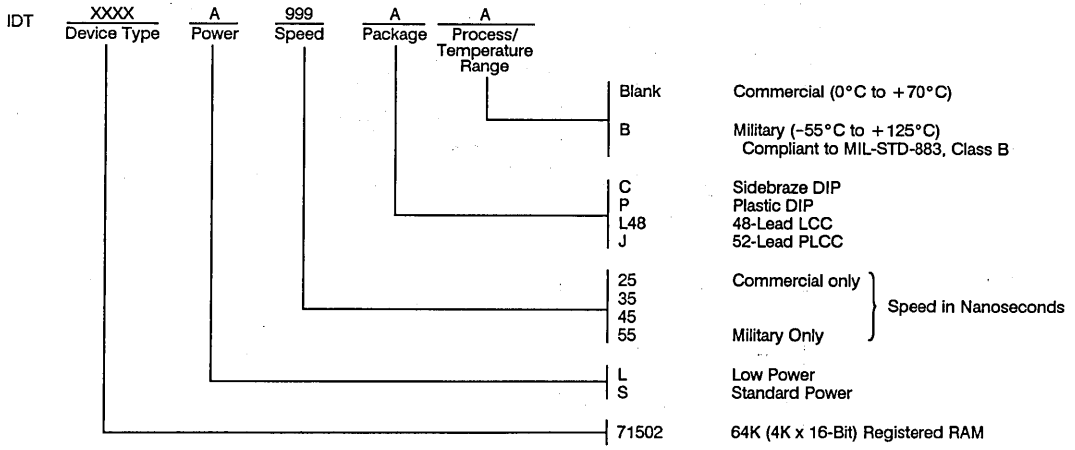


Figure 13. Microcode Load EPROM Memory Map

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) LATCHED CacheRAM™

IDT 71586

FEATURES:

- Wide 4K x 16 Organization
- High-speed access
  - Commercial: 24/35/45/55ns (max.)
  - Military: 35/45/55ns (max.)
- Internal fast 12-bit address latch (5ns set-up & hold times)
- Best fit for popular cache configurations:
  - Intel 82385 cache controller (for 80386)
  - IDT79R3000 RISC CPU instruction & data caches
  - Chips & Technologies 82C307 cache controller (for 80386)
- Fast Output Enable - 10ns (max.)
- Separate enables for upper and lower bytes
- Packaged in 40 pin, 600 mil CERDIP or plastic DIP, or 44 pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71586 is a fast 4K x 16 latched address CMOS static RAM designed to enhance cache memory designs. This device offers improved circuit board densities over designs using traditional RAM architectures in caches for the Intel 80386/82385 the Chips & Technologies 82C307, and the IDT79R3000 RISC CPU.

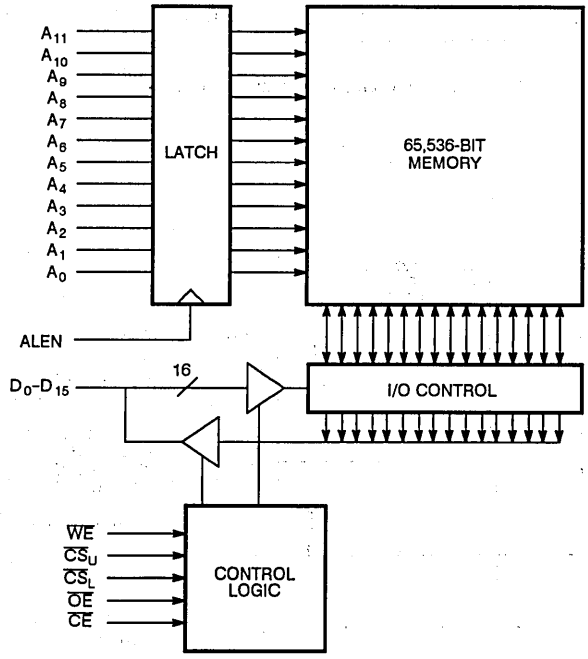
The IDT71586 boasts a fast address access time down to 24ns (max.), a very fast 10ns (max.) Output Enable pin, and short set-up and hold times (5ns max.) on the address input latch. All of these features help the IDT71586 to make the most efficient use of CPU-local buses.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71586 achieves this high throughput at a typical operating power of only 300mW.

All inputs and outputs of the IDT71586 are TTL-compatible, and the device operates from a standard 5V supply, simplifying system design. The IDT71586 is offered in a 40 pin CERDIP or plastic DIP, or a 44 pin plastic leadless chip carrier, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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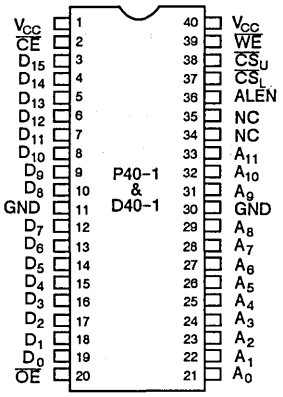
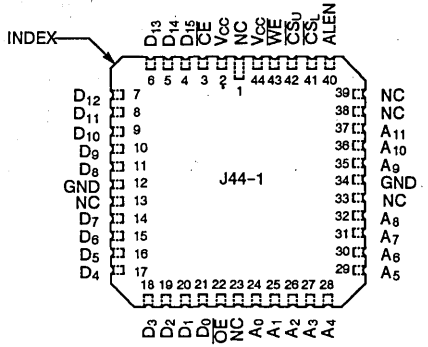
PIN CONFIGURATION



DIP
TOP VIEW



PLCC
TOP VIEW

PIN NAMES

$A_0 - A_{11}$	Address Inputs
$D_0 - D_{15}$	Data Input/Output
$\overline{CE}$	Chip Enable/Power-Down
$\overline{CS}_U$	Upper Byte Select
$\overline{CS}_L$	Lower Byte Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
ALEN	Address Latch Enable
GND	Ground
V_{CC}	Power

SPEED SELECTION

IDT79R3000 SPEED	80386 SPEED	SUGGESTED IDT71586
–	16MHz	71586S55
12MHz	20MHz	71586S45
16MHz	25MHz	71586S35
20-25MHz	33MHz	71586S25

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation Plastic Hermetic	1.5 2.0	W W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5V(1)	–	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	–	10	µA
V_{OL}	Output Low Voltage (D_0 - D_{15})	I_{OL} = 6mA, V_{CC} = Min.	–	0.4	V
		I_{OL} = 8mA, V_{CC} = Min.	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT71586S25		IDT71586S35		IDT71586S45		IDT71586S55		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	130	–	130	150	130	150	130	150	mA
I_{CC2}	Dynamic Operating Current	$\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	240	–	240	290	240	290	240	290	
I_{SB}	Standby Power Supply Current (TTL Level Inputs)	$\overline{CE}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	70	–	70	70	70	70	70	70	
I_{SB1}	Full Standby Power Supply Current (CMOS Level Inputs)	$\overline{CE}$ ≥ V_{HC}, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}, V_{CC} = Max., f = 0[2]	15	–	15	20	15	20	15	20	

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

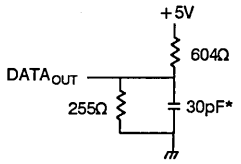


Figure 1. Output Load

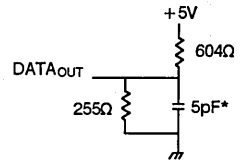


Figure 2. Output Load
(for t_{OHZ}, t_{BHZ}, t_{CHZ}, t_{OLZ} t_{BLZ}, t_{CLZ}, t_{WHZ}, and t_{OW})

*Including scope and jig

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

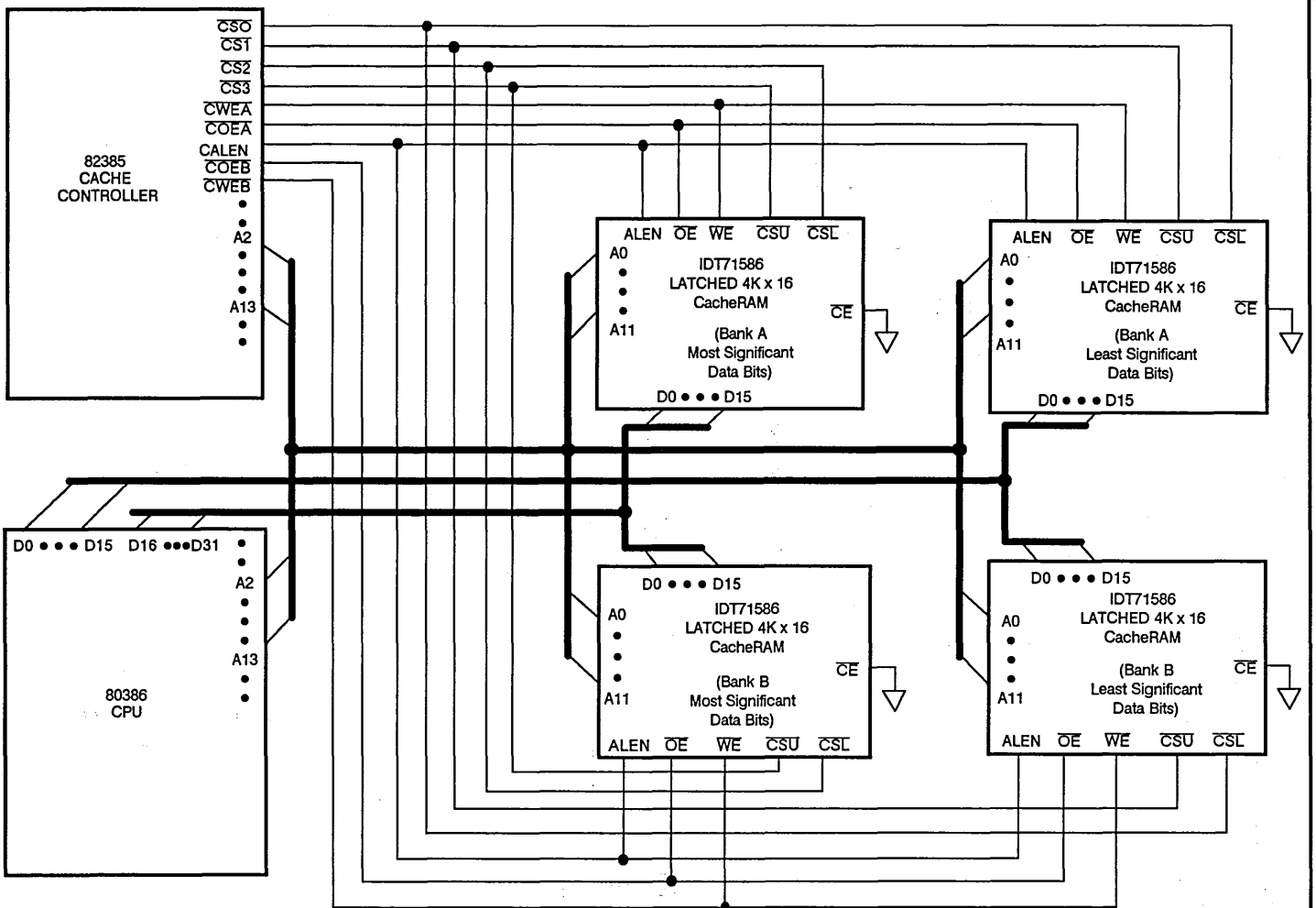


Figure 3. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Intel 82385.

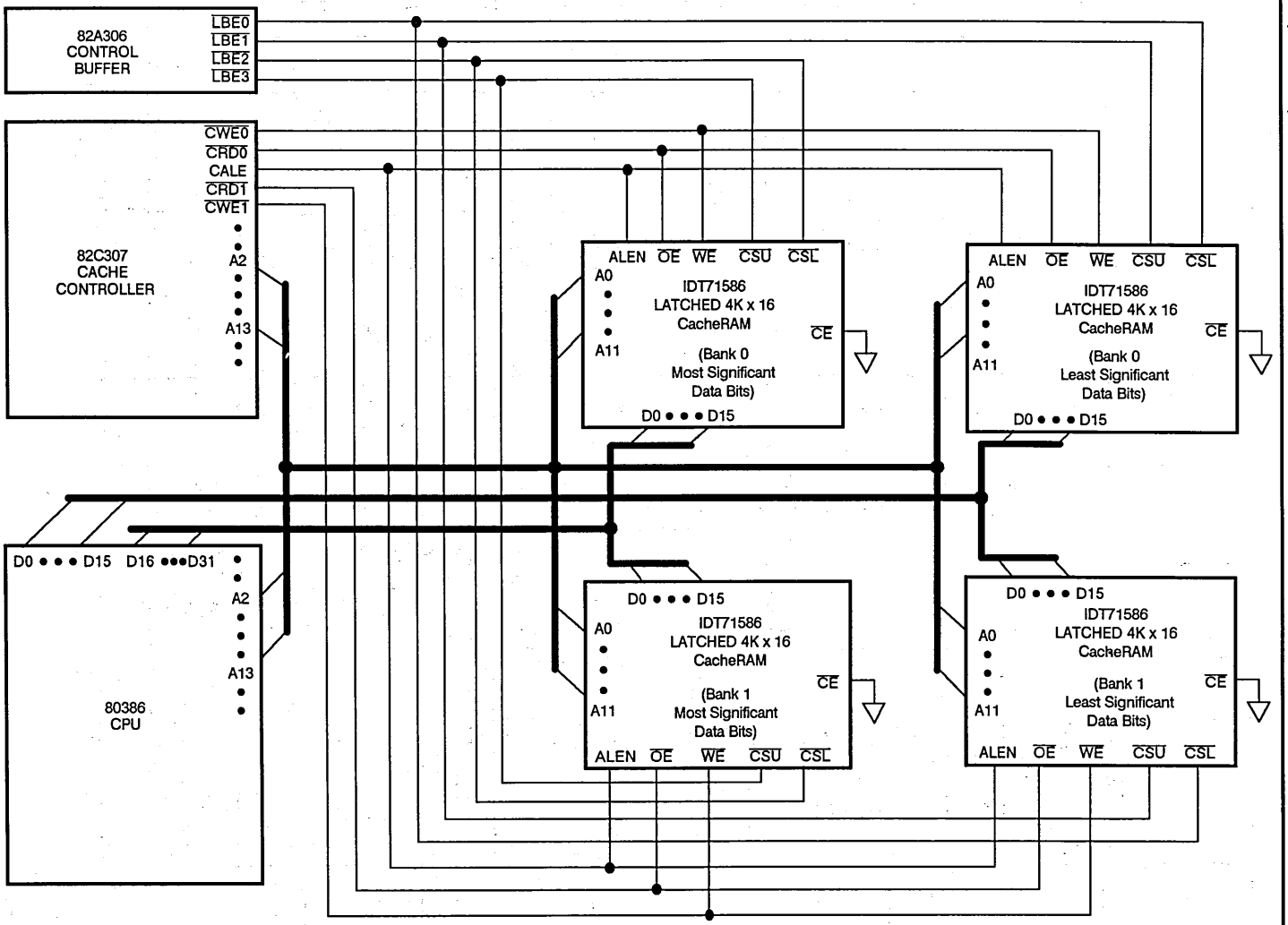


Figure 4. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Chips & Technologies 82C307.

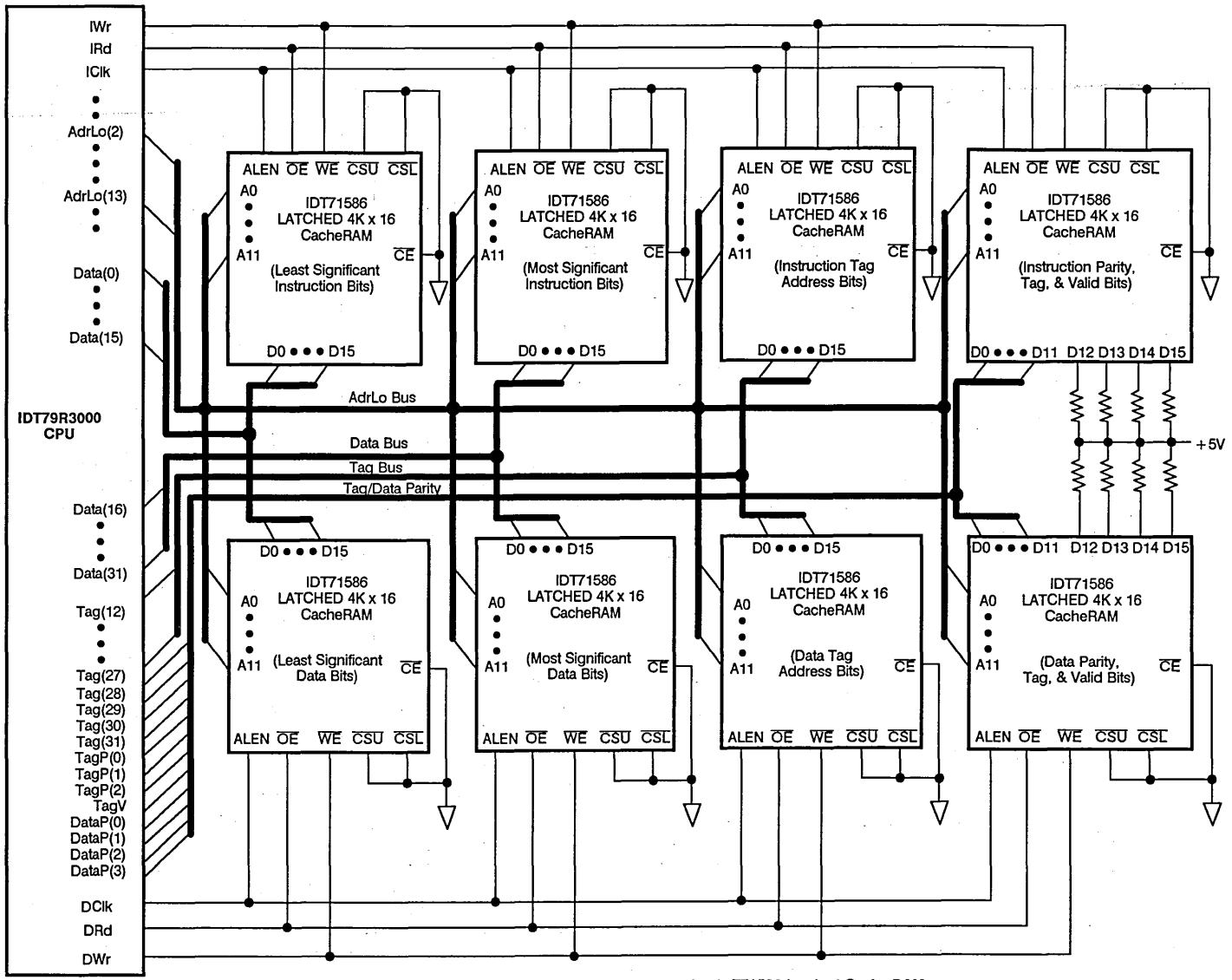


Figure 5. Example Instruction and Data Caches for IDT79R3000 using IDT71586 Latched Cache RAM.

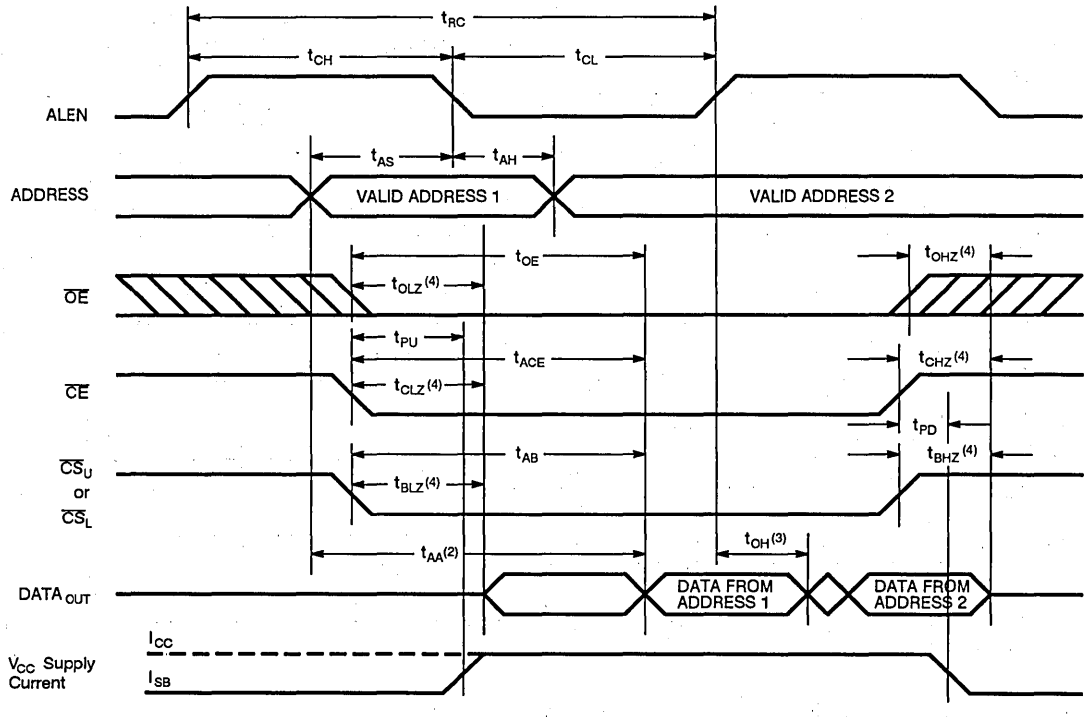
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71586S25[1] MIN.	IDT71586S25[1] MAX.	IDT71586S35[1] MIN.	IDT71586S35[1] MAX.	IDT71586S45 MIN.	IDT71586S45 MAX.	IDT71586S55 MIN.	IDT71586S55 MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	ns
t_{CH}	ALEN High Time[3]	10	–	10	–	12	–	15	–	
t_{CL}	ALEN Low Time[3]	10	–	10	–	12	–	15	–	
t_{AS}	Address Latch Set-Up Time	5	–	5	–	5	–	5	–	
t_{AH}	Address Latch Hold Time	4	–	5	–	5	–	5	–	
t_{AA}	Address Access Time[4]	–	24	–	35	–	45	–	55	
t_{ACE}	Chip Enable Access Time	–	25	–	35	–	45	–	55	
t_{AB}	Upper/Lower Byte Chip Select Access Time	–	13	–	15	–	20	–	25	
t_{OE}	Output Enable to Output Valid	–	10	–	13	–	15	–	18	
t_{CLZ}	Chip Enable to Output in Low Z[2, 3]	3	–	3	–	3	–	3	–	
t_{BLZ}	Upper/Lower Byte Chip Select to Output in Low Z[2, 3]	3	–	3	–	3	–	3	–	
t_{OLZ}	Output Enable to Output in Low Z[2, 3]	2	–	2	–	2	–	2	–	
t_{CHZ}	Chip Disable to Output in High Z[2, 3]	–	20	–	25	–	30	–	35	
t_{BHZ}	Upper/Lower Byte Chip Select to Output in High Z[2, 3]	–	20	–	25	–	30	–	35	
t_{OHZ}	Output Disable to Output in High Z[2, 3]		4	–	9	–	13	–	15	
t_{OH}	Output Hold from Address Change[4]	3	–	3	–	3	–	3	–	
t_{PU}	Chip Enable to Power Up Time[3]	0	–	0	–	0	–	0	–	
t_{PD}	Chip Disable to Power Down Time[3]	–	25	–	35	–	45	–	55	

NOTES:

1. 0°C to +70°C temperature range only.
2. Transition is measured ± 200mV from low or high impedance voltage with load (Figures 1&2).
3. This parameter is guaranteed, but not tested.
4. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.

TIMING WAVEFORM OF READ CYCLE (1)



NOTES:

1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter t_{AA} is measured either from the first low to high transition of ALEN after the read address has become valid, or from the stabilization of the read address during the period when ALEN is high, whichever occurs last.
3. The parameter t_{OH} is measured either from the first low to high transition of ALEN after the an address change, or from an address change during the period when ALEN is high, whichever occurs first.
4. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

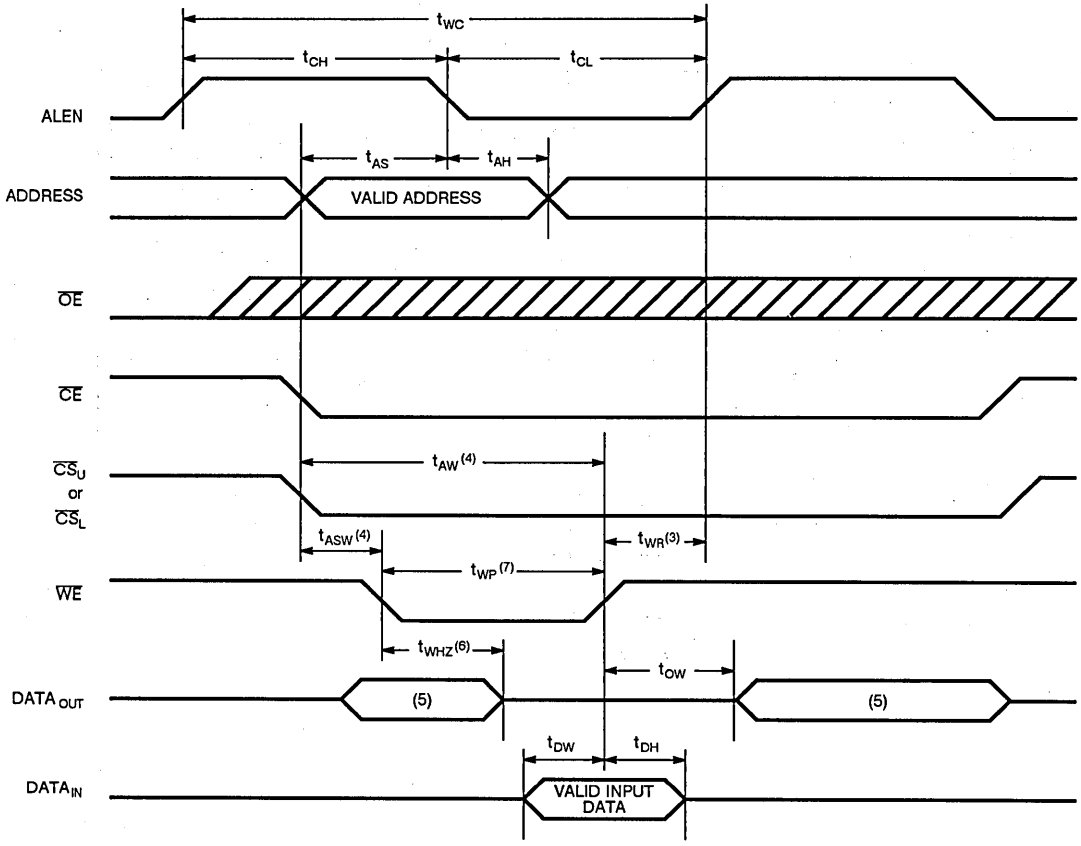
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71586S25[1] MIN.	IDT71586S25[1] MAX.	IDT71586S35[1] MIN.	IDT71586S35[1] MAX.	IDT71586S45 MIN.	IDT71586S45 MAX.	IDT71586S55 MIN.	IDT71586S55 MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	–	35	–	45	–	55	–	ns
t_{CH}	ALEN High Time	10	–	10	–	12	–	15	–	
t_{CL}	ALEN Low Time	10	–	10	–	12	–	15	–	
t_{AS}	Address Latch Set-Up Time	5	–	5	–	5	–	5	–	
t_{AH}	Address Latch Hold Time	4	–	5	–	5	–	5	–	
t_{AW}	Address Valid to End of Write[3]	25	–	35	–	45	–	55	–	
t_{ASW}	Address Set-Up Time[3]	0	–	0	–	0	–	0	–	
t_{WP}	Write Pulse Width	17	–	25	–	30	–	40	–	
t_{CW}	Chip Enable to End of Write	20	–	25	–	30	–	40	–	
t_{BW}	Upper/Lower Byte Chip Select to End of Write	20	–	25	–	30	–	40	–	
t_{WR}	Write Recovery Time[3]	0	–	0	–	0	–	0	–	
t_{WHZ}	Write to Output in High Z[2]	–	13	–	15	–	20	–	25	
t_{DW}	Data Set-Up Time	11	–	13	–	15	–	18	–	
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	
t_{OW}	Output Active from End of Write[2]	5	–	5	–	5	–	5	–	

NOTES:

1. 0°C to +70°C temperature range only.
2. Transition is measured ± 200mV from low or high impedance voltage with load (Figures 1&2). This parameter is guaranteed, but not tested.
3. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.

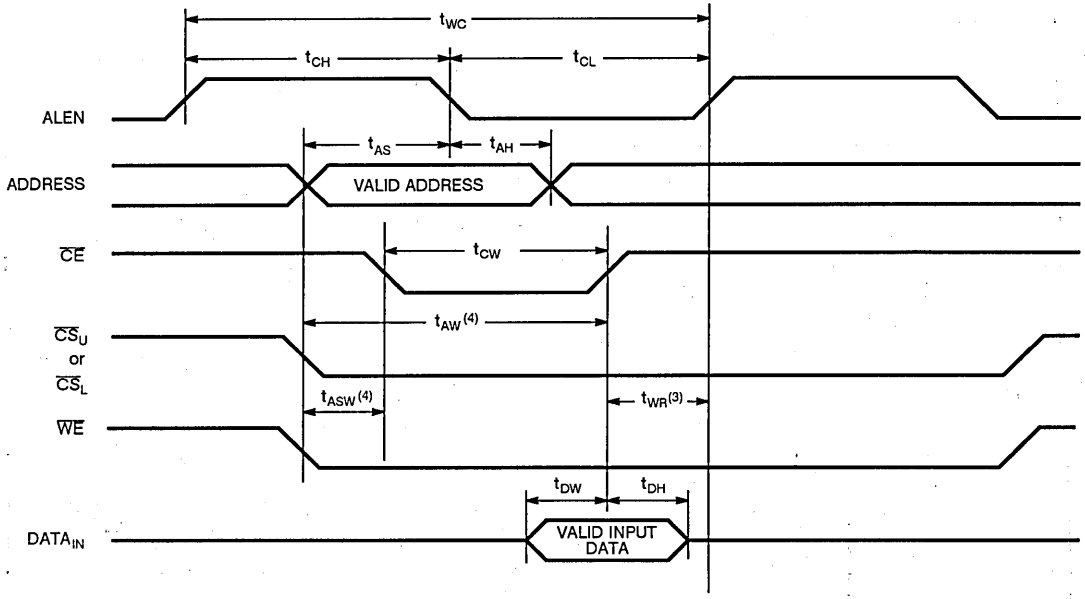
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2)



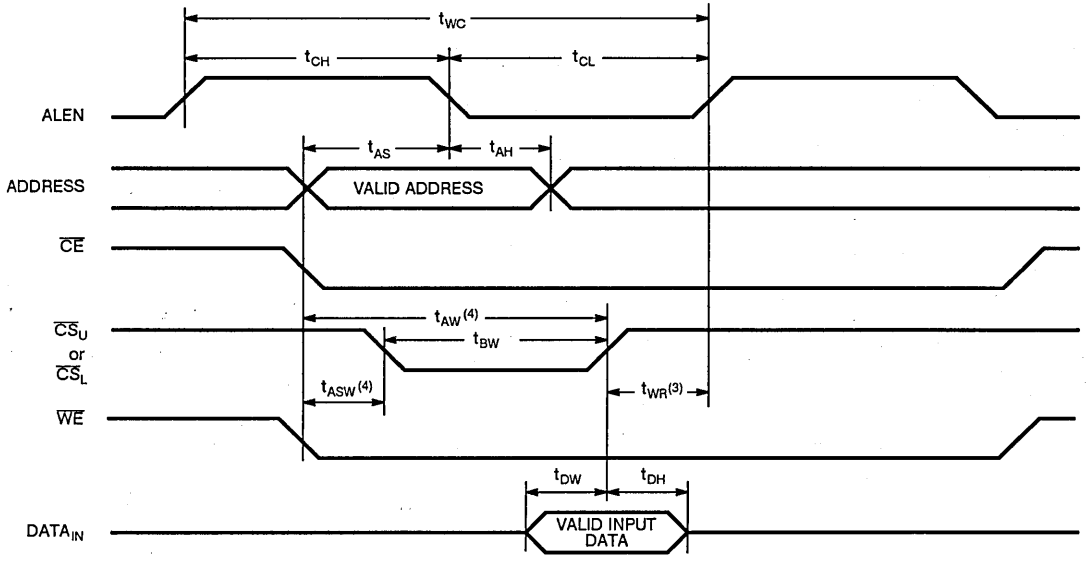
NOTES:

1. $\overline{WE}$, $\overline{CE}$, or both $\overline{CS_U}$ and $\overline{CS_L}$ must be high during address transitions.
2. A write occurs during the overlap (t_{BW}, t_{CW} or t_{WP}) of a low $\overline{CS_U}$ or $\overline{CS_L}$, a low $\overline{CE}$, and a low $\overline{WE}$.
3. The parameter t_{WR} is measured from the earlier of $\overline{CS_U}$, $\overline{CS_L}$, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters t_{ASW} and t_{AW} are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.
5. During this period the I/O pins are in the output state, and input signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2)



TIMING WAVEFORM OF WRITE CYCLE NO. 3, ($\overline{CS_U}$ or $\overline{CS_L}$ CONTROLLED TIMING)(1, 2)



NOTES:

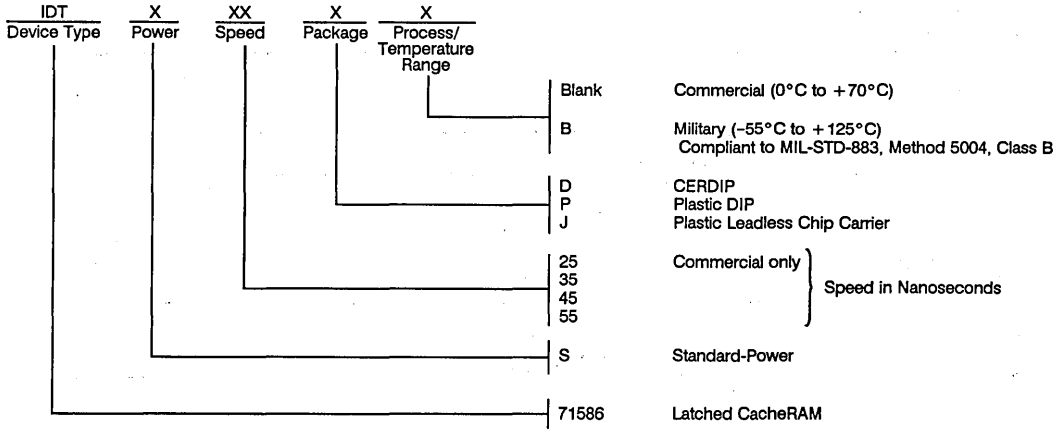
1. $\overline{WE}$, $\overline{CE}$, or both $\overline{CS_U}$ and $\overline{CS_L}$ must be high during address transitions.
2. A write occurs during the overlap (t_{BW}, t_{CW} or t_{WP}) of a low $\overline{CS_U}$ or $\overline{CS_L}$, a low $\overline{CE}$, and a low $\overline{WE}$.
3. The parameter t_{WR} is measured from the earlier of $\overline{CS_U}$, $\overline{CS_L}$, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters t_{ASW} and t_{AW} are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.

TRUTH TABLE [1]

INPUTS						OUTPUTS		
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{CS}_U$	$\overline{CS}_L$	ALEN	D_8 - D_{15}	D_0 - D_7	MODE
H	X	X	X	X	–	Hi-Z	Hi-Z	Deselected, powered-down (I_{SB}).
X	X	X	H	H	–	Hi-Z	Hi-Z	Deselected.
–	–	H	–	–	–	Hi-Z	Hi-Z	Outputs disabled.
–	–	–	–	–	H	–	–	Address latch transparent.
X	X	–	–	–	L	–	–	Address latch closed.
L	L	X	L	H	H	$DATA_{IN}$	Hi-Z	Write to upper byte of current address.
L	L	X	L	H	L	$DATA_{IN}$	Hi-Z	Write to upper byte of latched address.
L	L	X	H	L	H	Hi-Z	$DATA_{IN}$	Write to lower byte of current address.
L	L	X	H	L	L	Hi-Z	$DATA_{IN}$	Write to lower byte of latched address.
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to both bytes of current address (Word Write).
L	L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to both bytes of latched address (Word Write).
L	H	L	L	H	H	$DATA_{OUT}$	HI-Z	Read upper byte of current address.
L	H	L	L	H	L	$DATA_{OUT}$	Hi-Z	Read upper byte of latched address.
L	H	L	H	L	H	Hi-Z	$DATA_{OUT}$	Read lower byte of current address.
L	H	L	H	L	L	Hi-Z	$DATA_{OUT}$	Read lower byte of latched address.
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read both bytes of current address (Word Read).
L	H	L	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read both bytes of latched address (Word Read).

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   – = Unrelated
   Hi-Z = High Impedance

ORDERING INFORMATION



MULTI-PORT RAMS

Integrated Device Technology has emerged as the leading multi-port RAM supplier by combining advanced CEMOS technology with innovative circuit design. With system performance advantages as a goal, we have brought system design expertise together with circuit and technology expertise in defining dual-port and four-port RAM products. Our dual-port memories are now industry standards.

The synergistic relationship between advanced process technology, system expertise and unique design capability add value beyond that normally achieved. As an example, our dual-port memories provide arbitration along with a completely tested solution to the metastability problem. Various arbitration techniques are available to the designer to prevent contention and system wait states. On-chip hardware arbitration, "semaphore" token passing or software arbitration allow the most efficient memory to be selected for each application. At IDT, innovation counts only when it provides system advantages to the user.

Both commercial and military versions of all IDT memories are available. Our military devices are manufactured and processed strictly in conformance with all the administrative processing and performance requirements of MIL-STD-883. Because we anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As the leading supplier of military specialty RAMs, IDT provides performance and quality levels second to none.

Our commercial dual-port and four-port memories, in fact, share most processing steps with military devices.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 8K (1K x 8-BIT)

IDT 7130SA/LA
IDT 7140SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7130/40SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7130/40LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86875

DESCRIPTION:

The IDT7130/IDT7140 are high-speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

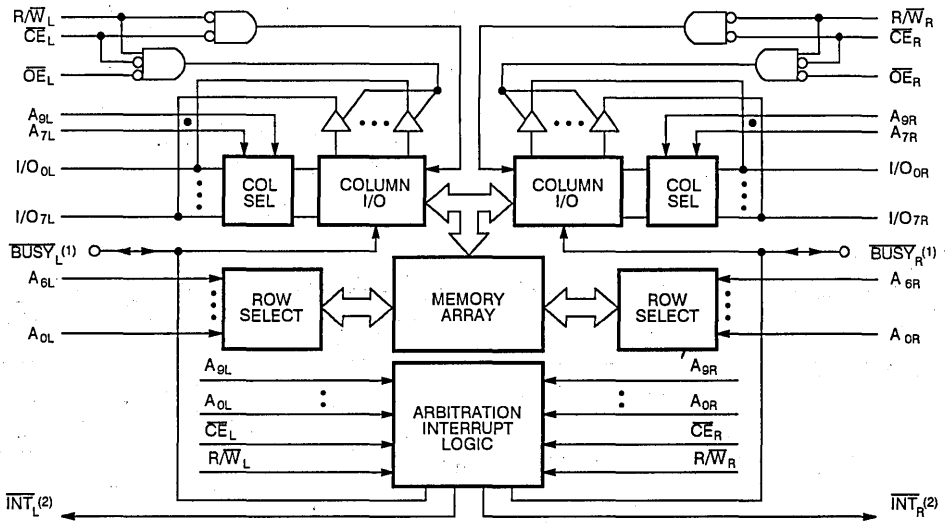
Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7130/7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM

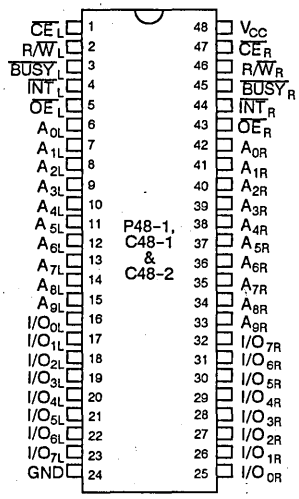


NOTES:

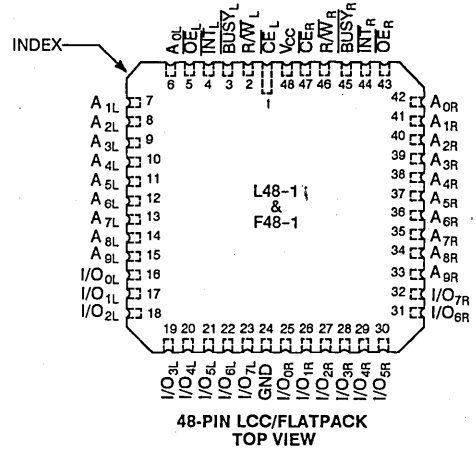
1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

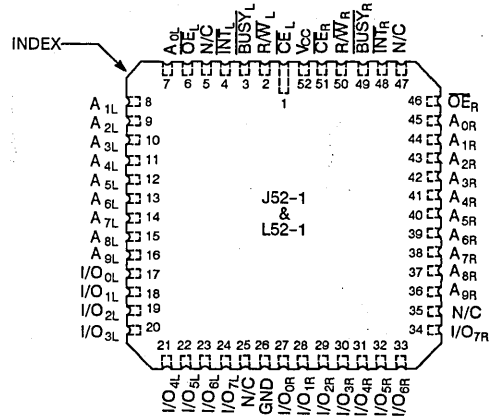
PIN CONFIGURATIONS



DIP
TOP VIEW



48-PIN LCC/FLATPACK
TOP VIEW



52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7130SA IDT7140SA MIN.	IDT7130SA IDT7140SA MAX.	IDT7130LA IDT7140LA MIN.	IDT7130LA IDT7140LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 4.0mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		7130 x 25[2] 7140 x 25[2] TYP.	7130 x 25[2] 7140 x 25[2] MAX.	7130 x 30[2] 7140 x 30[2] TYP.	7130 x 30[2] 7140 x 30[2] MAX.	7130 x 35[2] 7140 x 35[2] TYP.	7130 x 35[2] 7140 x 35[2] MAX.	7130 x 45 7140 x 45 TYP.	7130 x 45 7140 x 45 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	75	230	mA
				LA	–	–	–	–	–	–	75	185	
			COM'L.	SA	75	250	75	240	75	195	75	190	
				LA	75	180	75	170	75	155	75	145	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	25	65	mA
				LA	–	–	–	–	–	–	25	55	
			COM'L.	SA	25	65	25	65	25	65	25	65	
				LA	25	45	25	45	25	45	25	45	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	40	135	mA
				LA	–	–	–	–	–	–	40	110	
			COM'L.	SA	50	170	46	155	40	130	40	120	
				LA	50	120	46	110	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	–	–	–	–	–	–	1.0	30	mA
				LA	–	–	–	–	–	–	0.2	10	
			COM'L.	SA	1.2	15	1.2	15	1.0	15	1.0	15	
				LA	0.4	5	0.4	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	40	125	mA
				LA	–	–	–	–	–	–	35	95	
			COM'L.	SA	50	150	45	137	40	115	40	105	
				LA	46	115	42	105	35	90	35	80	

NOTES:

1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (Continued) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		7130 x 55 7140 x 55		7130 x 70 7140 x 70		7130 x 90 7140 x 90		7130 x 100 7140 x 100		7130 x 120[3] 7140 x 120[3]		UNIT
					TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
			COM'L.	SA	65	180	65	180	65	180	65	180	65	180	
				LA	65	140	65	135	65	130	65	130	65	130	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
			COM'L.	SA	25	65	25	60	25	55	25	55	25	55	
				LA	25	45	25	40	25	35	25	35	25	35	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	40	135	40	135	10	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
			COM'L.	SA	40	115	40	110	40	110	40	110	40	110	
				LA	40	85	40	85	40	75	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			COM'L.	SA	40	100	40	100	40	95	40	95	40	95	
				LA	35	75	35	75	35	70	35	70	35	70	

NOTES:

1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

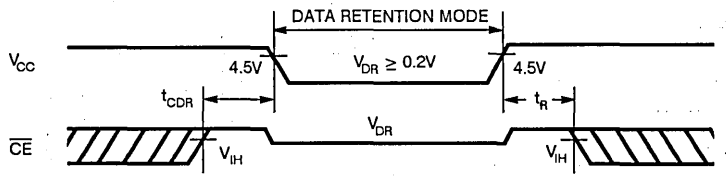
DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130LA/IDT7140LA MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

5

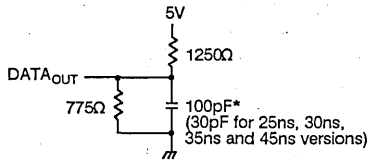


Figure 1. Output Load

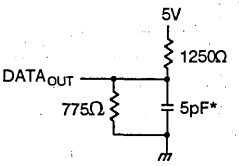


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

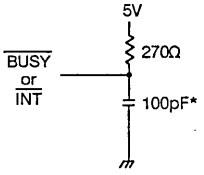


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

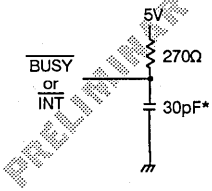


Figure 4. $\overline{BUSY}$ and $\overline{INT}$ Output Load (for 25ns and 30ns versions)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5]

SYMBOL	PARAMETER	7130 x 25[2] 7140 x 25[2] MIN.	MAX.	7130 x 30[2] 7140 x 30[2] MIN.	MAX.	7130 x 35[2] 7140 x 35[2] MIN.	MAX.	7130 x 45 7140 x 45 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	ns
t_{ACE}	Chip Enable Access Time	–	25	–	30	–	35	–	45	ns
t_{AOE}	Output Enable Access Time	–	12	–	15	–	25	–	30	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time [1, 4]	0	–	0	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 4]	–	10	–	12	–	15	–	20	ns
t_{PU}	Chip Enable to Power Up Time [4]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [4]	–	50	–	50	–	50	–	50	ns

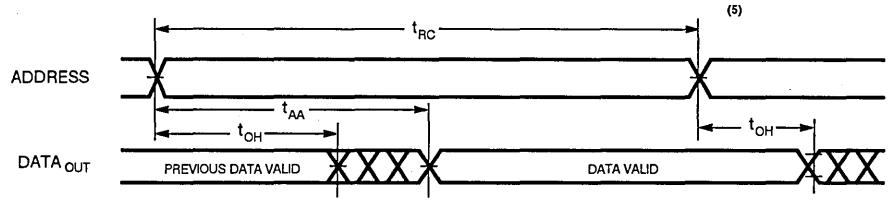
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Continued)

SYMBOL	PARAMETER	7130 x 55 7140 x 55 MIN.	MAX.	7130 x 70 7140 x 70 MIN.	MAX.	7130 x 90 7140 x 90 MIN.	MAX.	7130 x 100 7140 x 100 MIN.	MAX.	7130 x 120[3] 7140 x 120[3] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	55	–	70	–	90	–	100	–	120	–	ns
t_{AA}	Address Access Time	–	55	–	70	–	90	–	100	–	120	ns
t_{ACE}	Chip Enable Access Time	–	55	–	70	–	90	–	100	–	120	ns
t_{AOE}	Output Enable Access Time	–	35	–	40	–	40	–	40	–	60	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	10	–	10	–	10	–	ns
t_{LZ}	Output Low Z Time [1, 4]	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 4]	–	30	–	35	–	40	–	40	–	40	ns
t_{PU}	Chip Enable to Power Up Time [4]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [4]	–	50	–	50	–	50	–	50	–	50	ns

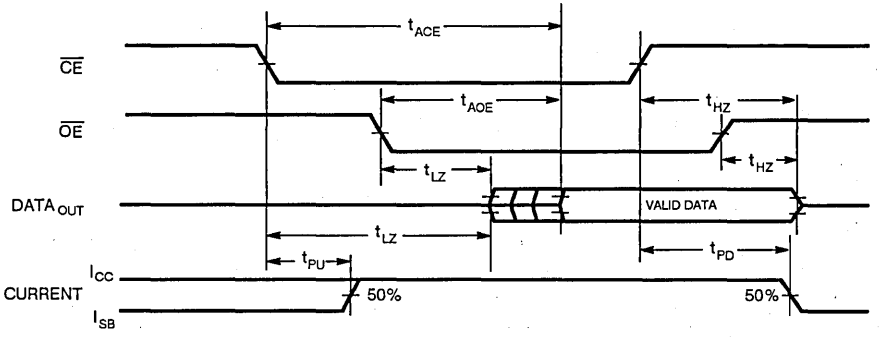
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

5

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [7]

SYMBOL	PARAMETER	7130 x 25[2] 7140 x 25[2]		7130 x 30[2] 7140 x 30[2]		7130 x 35[2] 7140 x 35[2]		7130 x 45 7140 x 45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE										
t_{WC}	Write Cycle Time[5]	25	–	30	–	35	–	45	–	ns
t_{EW}	Chip Enable to End of Write	20	–	25	–	30	–	35	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[6]	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	12	–	15	–	20	–	20	–	ns
t_{HZ}	Output High Z Time[1, 4]	–	10	–	12	–	15	–	20	ns
t_{DH}	Data Hold Tme	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1, 4]	0	10	–	12	–	15	–	20	ns
t_{OW}	Output Active From End of Write[1, 4]	0	–	0	–	0	–	0	–	ns

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [7]

SYMBOL	PARAMETER	7130 x 55 7140 x 55		7130 x 70 7140 x 70		7130 x 90 7140 x 90		7130 x 100 7140 x 100		7130 x 120[3] 7140 x 120[3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time[5]	55	–	70	–	90	–	100	–	120	–	ns
t_{EW}	Chip Enable to End of Write	40	–	50	–	85	–	90	–	100	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	85	–	90	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[6]	40	–	50	–	55	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	30	–	40	–	40	–	40	–	ns
t_{HZ}	Output High Z Time[1, 4]	–	30	–	35	–	40	–	40	–	40	ns
t_{DH}	Data Hold Tme	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1, 4]	–	30	–	35	–	40	–	40	–	50	ns
t_{OW}	Output Active From End of Write[1, 4]	0	–	0	–	0	–	0	–	0	–	ns

NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (S or L).

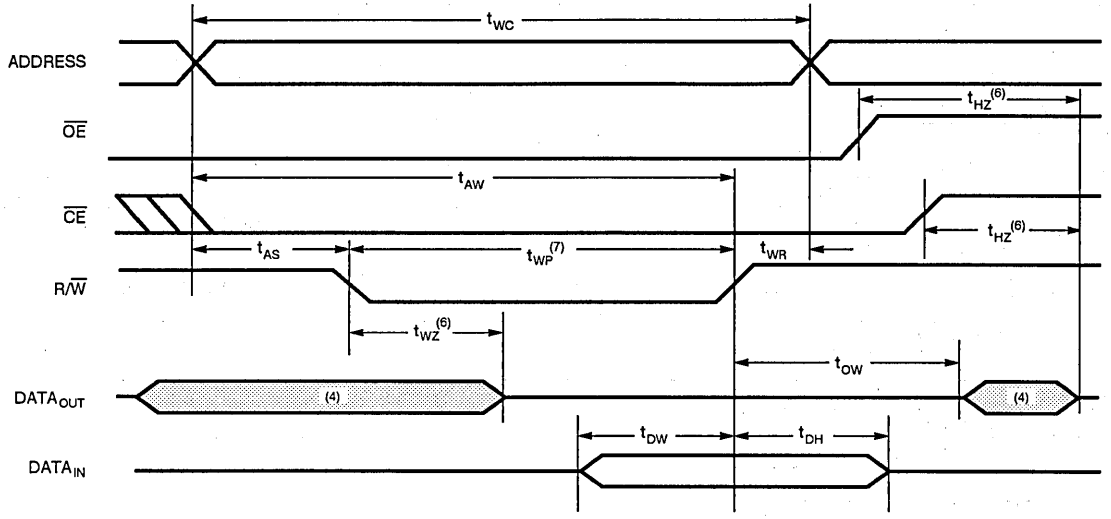
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

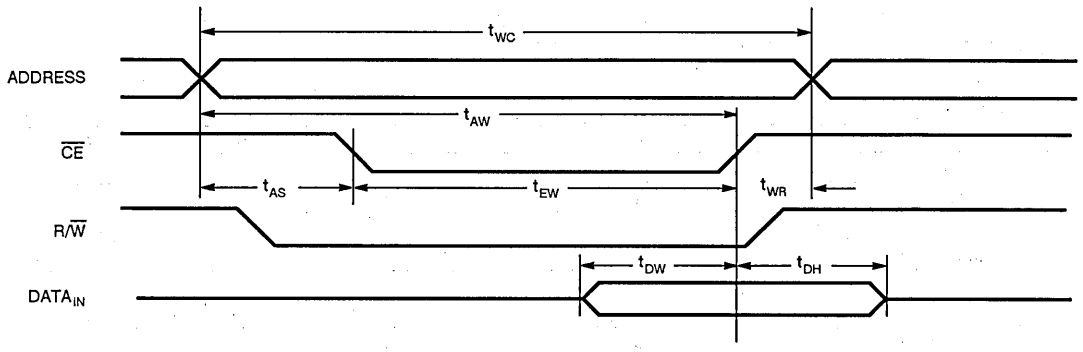
NOTE:

1. This parameter is determined by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $t_{WZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [8]

SYMBOL	PARAMETER	7130 x 25[1] 7140 x 25[1] MIN.	MAX.	7130 x 30[1] 7140 x 30[1] MIN.	MAX.	7130 x 35[1] 7140 x 35[1] MIN.	MAX.	7130 x 45 7140 x 45 MIN.	MAX.	UNIT
BUSY TIMING (FOR MASTER IDT7130 ONLY)										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	25	–	30	–	35	–	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	20	–	25	–	30	–	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	20	–	25	–	30	–	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	20	–	25	–	25	–	25	ns
t_{WDD}	Write Pulse to Data Delay[3]	–	50	–	55	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	–	30	–	30	–	35	–	45	ns
t_{APS}	Arbitration Priority Set-up Time[4]	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)										
t_{WB}	Write to $\overline{BUSY}$ Input[6]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[7]	15	–	20	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay[9]	–	50	–	55	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	–	30	–	30	–	35	–	45	ns

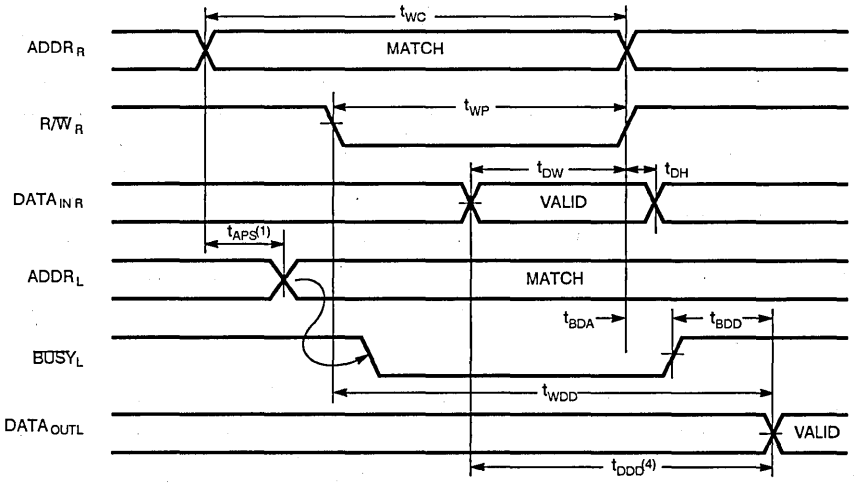
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5]

SYMBOL	PARAMETER	7130 x 55 7140 x 55 MIN.	MAX.	7130 x 70 7140 x 70 MIN.	MAX.	7130 x 90 7140 x 90 MIN.	MAX.	7130 x 100 7140 x 100 MIN.	MAX.	7130 x 120[2] 7140 x 120[2] MIN.	MAX.	UNIT
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	45	–	45	–	45	–	50	–	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	40	–	40	–	45	–	50	–	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	35	–	35	–	45	–	50	–	60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	30	–	30	–	45	–	50	–	60	ns
t_{WDD}	Write Pulse to Data Delay[3]	–	80	–	90	–	100	–	120	–	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	–	55	–	70	–	90	–	100	–	120	ns
t_{APS}	Arbitration Priority Set-up Time[4]	5	–	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
t_{WB}	Write to $\overline{BUSY}$ Input[6]	0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[7]	20	–	20	–	20	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay[9]	–	80	–	90	–	100	–	120	–	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	–	55	–	70	–	90	–	100	–	120	ns

NOTES:

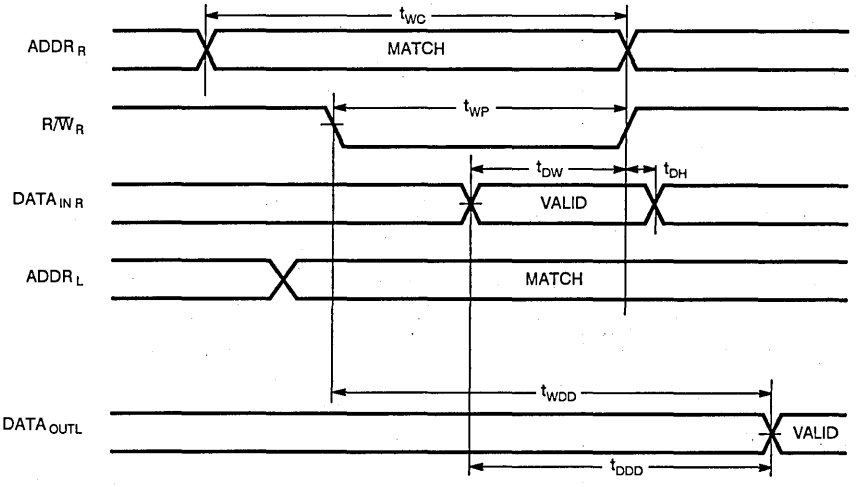
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7130 only)".
4. To ensure that the earlier of the two ports wins.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual or $t_{DDD} - t_{WP}$ (actual)).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" In part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7140 Only)".

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1, 2, 3) (FOR MASTER IDT7130 ONLY)



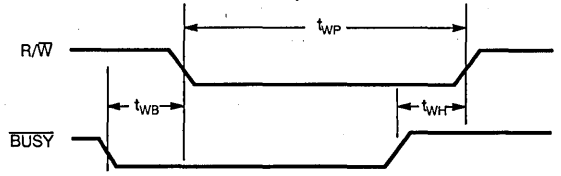
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (1, 2, 3) (FOR SLAVE IDT7140 ONLY)



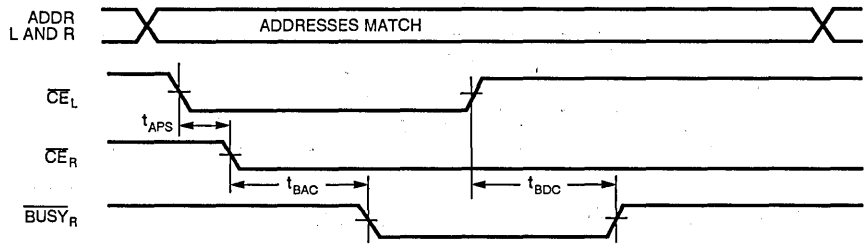
NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7140 ONLY)

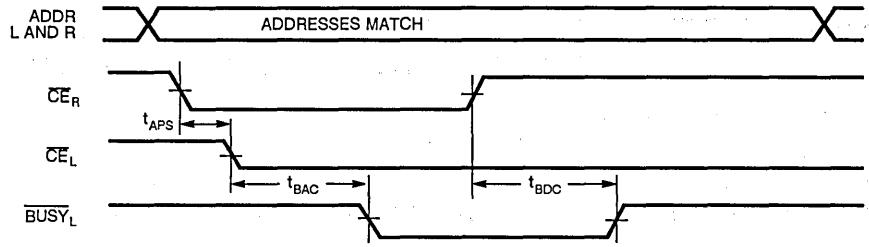


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

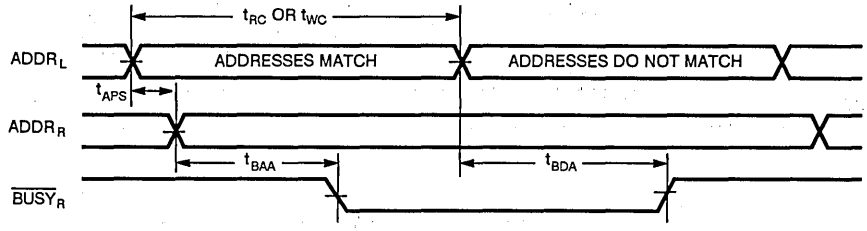


$\overline{CE}_R$ VALID FIRST:

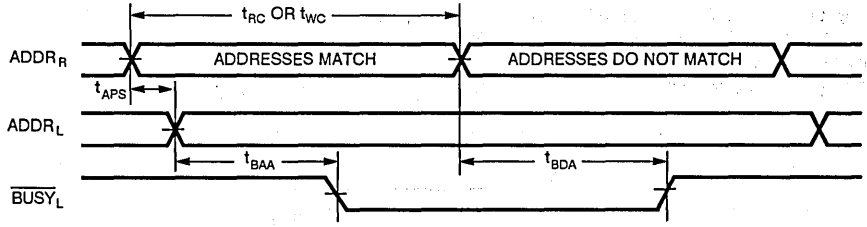


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION [1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	7130 x 25[1] 7140 x 25[1]		7130 x 30[1] 7140 x 30[1]		7130 x 35[1] 7140 x 35[1]		7130 x 45 7140 x 45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
INTERRUPT TIMING										
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{INS}	Interrupt Set Time	–	25	–	30	–	35	–	40	ns
t_{INR}	Interrupt Reset Time	–	25	–	30	–	35	–	40	ns

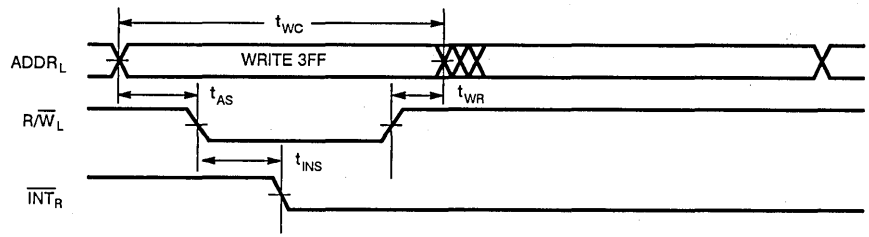
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	7130 x 55 7140 x 55		7130 x 70 7140 x 70		7130 x 90 7140 x 90		7130 x 100 7140 x 100		7130 x 120[2] 7140 x 120[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
INTERRUPT TIMING												
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{INS}	Interrupt Set Time	–	45	–	50	–	55	–	60	–	70	ns
t_{INR}	Interrupt Reset Time	–	45	–	50	–	55	–	60	–	70	ns

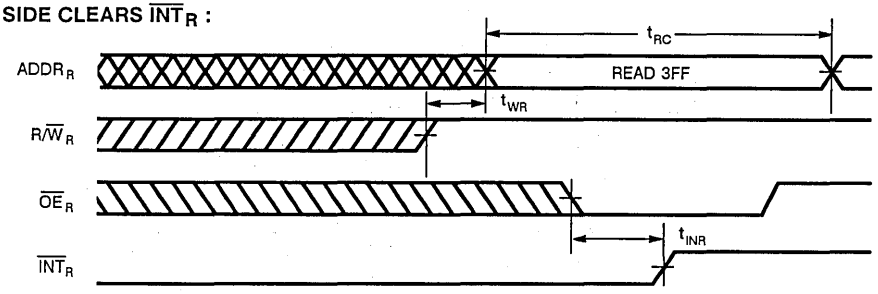
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF INTERRUPT MODE [1, 2]

LEFT SIDE SETS $\overline{INT}_R$:



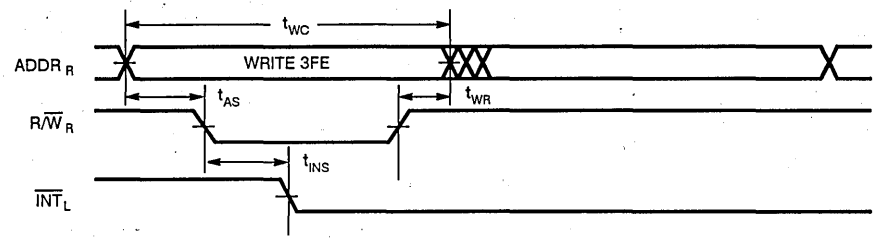
RIGHT SIDE CLEARS $\overline{INT}_R$:



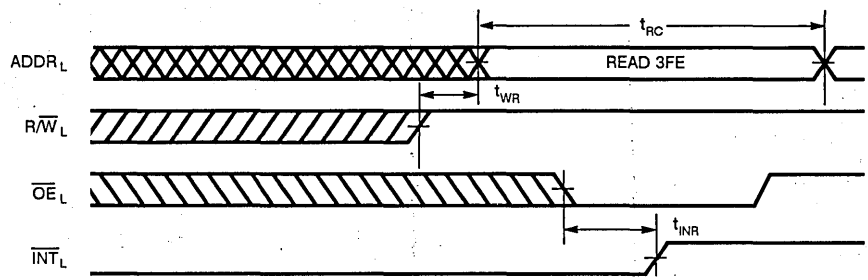
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power up.

TIMING WAVEFORM OF INTERRUPT MODE [1, 2]

RIGHT SIDE SETS $\overline{INT}_L$:

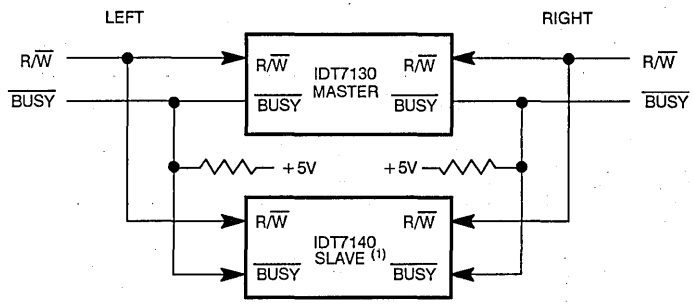


LEFT SIDE CLEARS $\overline{INT}_L$:



NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/40 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/40 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

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TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL [4]

LEFT OR RIGHT PORT [1]				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory [2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port [3]
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG [1, 4]

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{9R}$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L [2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H [3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L [3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H [2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

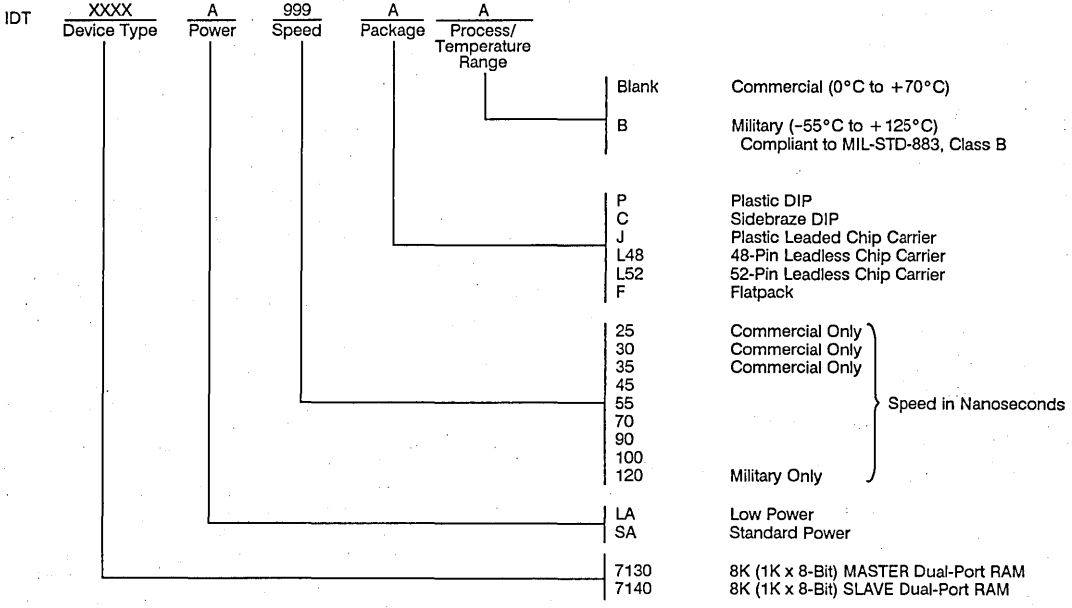
NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III – ARBITRATION [2]

LEFT PORT		RIGHT PORT		FLAGS [1]		FUNCTION
$\overline{CE}_L$	$A_{0L} - A_{9L}$	$\overline{CE}_R$	$A_{0R} - A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{9R}$	L	$\neq A_{0L} - A_{9L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{9R}$	LL5R	$= A_{0L} - A_{9L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{9R}$	RL5L	$= A_{0L} - A_{9L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	L	H	Arbitration Resolved

NOTE:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid $\geq$ 5ns before right address.
   RV5L = Right Address Valid $\geq$ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

HIGH-SPEED 1K x 9 DUAL-PORT STATIC RAM WITH BUSY

ADVANCE INFORMATION
IDT 7010
IDT 70104

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT7010/70104S
    Active: ---mW(typ.)
    Standby: --mW(typ.)
  - IDT7010/70104L
    Active: ---mW(typ.)
    Standby: ---mW(typ.)
- Fully asynchronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- MASTER IDT7010 easily expands data bus width to 18 bits or more using SLAVE IDT70104 chip
- On-chip port arbitration logic (IDT7010 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7010/IDT70104 are high-speed 1K X 9 dual port static RAMs. The IDT7010 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70104 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

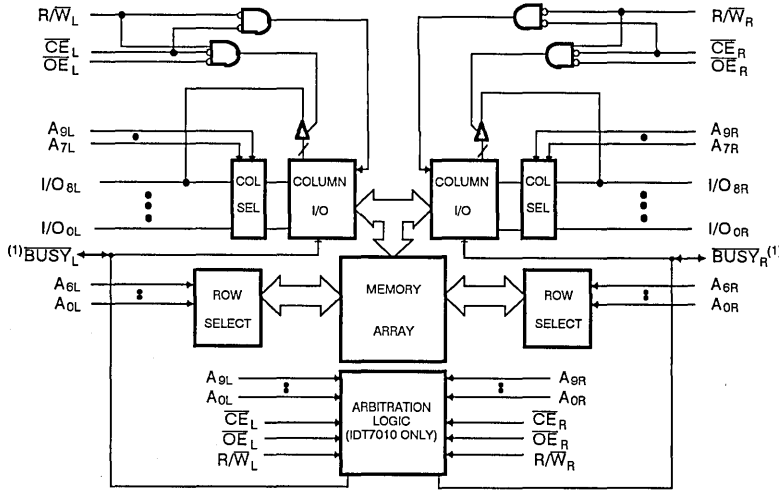
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by CE permits the on-chip circuitry of each port to enter a very low standby power mode.

The devices utilize a 9-bit wide data path to allow for control/data and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---μW from a 2V battery.

The IDT7010/70104 devices are packaged in 48-pin sidebrazed or plastic DIPs, 48- or 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

1. 7010(MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   70104(SLAVE): $\overline{BUSY}$ is input.

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Integrated Device Technology, Inc.

HIGH-SPEED 1K x 9 DUAL-PORT STATIC RAM WITH INTERRUPT AND BUSY

ADVANCE INFORMATION
IDT 70101
IDT 70105

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70101/70105S
    Active: ---mW(typ.)
    Standby: --mW(typ.)
  - IDT70101/70105L
    Active: ---mW(typ.)
    Standby: ---mW(typ.)
- Fully asychronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- MASTER IDT70101 easily expands data bus width to 18 bits or more using SLAVE IDT70105 chip
- On-chip port arbitration logic (IDT70101 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ (INTERRUPT) flag for port-to-port communication
- Battery backup operation - 2V data retention
- TTL compatible, signal 5V (± 10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT70101/IDT70105 are high-speed 1K x 9 dual-port static RAMs. The IDT70101 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70105 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

The devices utilize a 9-bit wide data path to allow for data/control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT70101/70105 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

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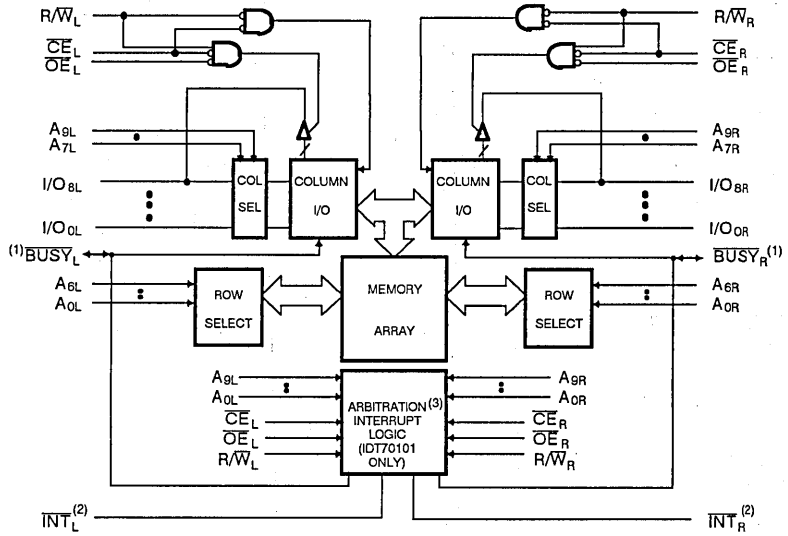
FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. 70101(MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor. 70105(SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is open drain output and requires pullup resistor.
3. Arbitration Logic is for IDT70101 (master).

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DSC-1048/-

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT 7132SA/LA
IDT 7142SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation—2V data retention
- TTL-compatible, single 5V±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87002

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

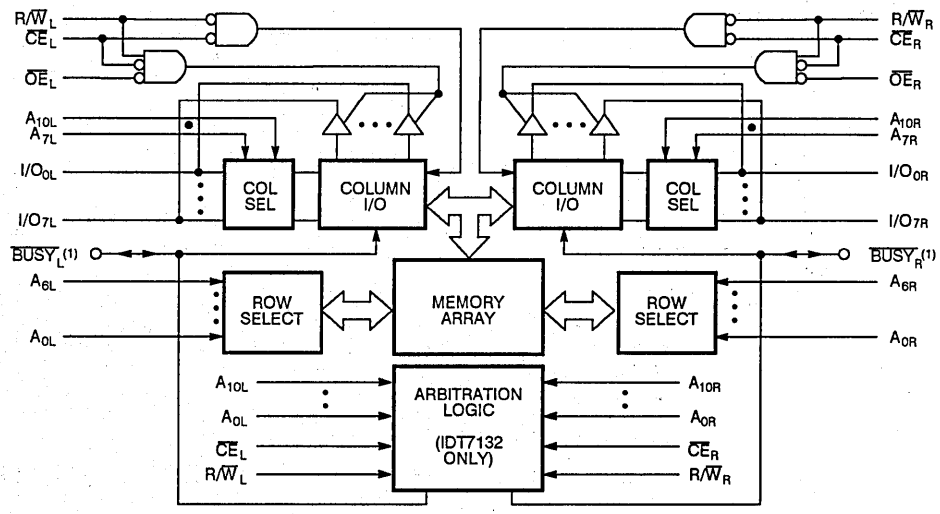
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 35ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIP, 48- or 52-pin LCC, 52-pin PLCC, and a 48-lead flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.

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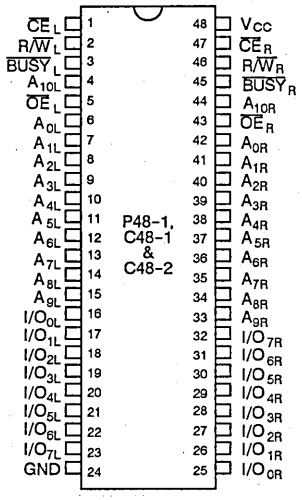
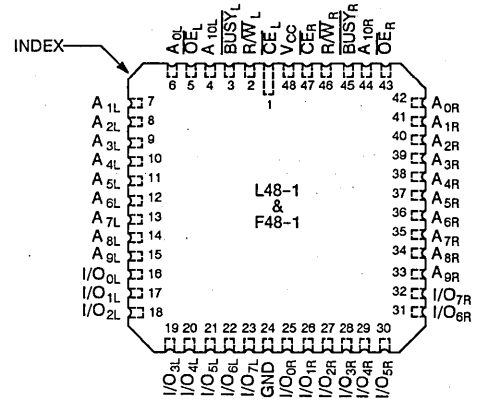
DSC-1001/1

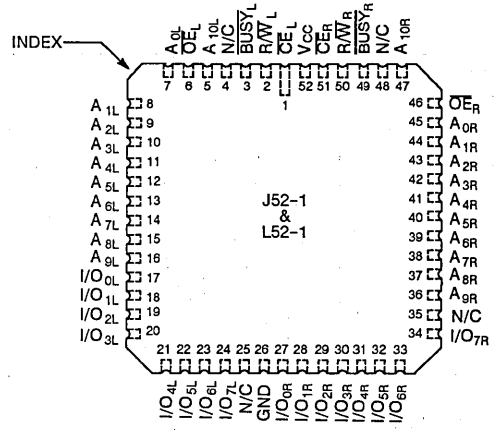
PIN CONFIGURATIONS



DIP
TOP VIEW



48-PIN LCC/FLATPACK
TOP VIEW



52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7132SA IDT7142SA		IDT7132LA IDT7142LA		UNIT
			MIN.	MAX.	MIN.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		7132 x 25[2] 7142 x 25[2]		7132 x 30[2] 7142 x 30[2]		7132 x 35[2] 7142 x 35[2]		7132 x 45 7142 x 45		UNIT
					TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	75	230	mA
				LA	–	–	–	–	–	–	75	185	
			COM'L.	SA	75	250	75	240	75	195	75	190	
				LA	75	180	75	170	75	155	75	145	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	25	65	mA
				LA	–	–	–	–	–	–	25	55	
			COM'L.	SA	25	65	25	65	25	65	25	65	
				LA	25	45	25	45	25	45	25	45	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	40	135	mA
				LA	–	–	–	–	–	–	40	110	
			COM'L.	SA	50	170	46	155	40	130	40	120	
				LA	50	120	46	110	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	MIL.	SA	–	–	–	–	–	–	1.0	30	mA
				LA	–	–	–	–	–	–	0.2	10	
			COM'L.	SA	1.2	15	1.2	15	1.0	15	1.0	15	
				LA	0.4	5	0.4	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	–	–	–	–	–	–	40	125	mA
				LA	–	–	–	–	–	–	35	95	
			COM'L.	SA	50	150	45	137	40	115	40	105	
				LA	46	115	42	105	35	90	35	80	

NOTES:

1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (Continued) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100 7142 x 100		7132 x 120[3] 7142 x 120[3]		UNIT
					TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
			COM'L.	SA	65	180	65	180	65	180	65	180	65	180	
				LA	65	140	65	135	65	130	65	130	65	130	
I_{SB1}	Standby Current (Both Ports–TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
			COM'L.	SA	25	65	25	60	25	55	25	55	25	55	
				LA	25	45	25	40	25	35	25	35	25	35	
I_{SB2}	Standby Current (One Port–TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	40	135	40	135	10	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
			COM'L.	SA	40	115	40	110	40	110	40	110	40	110	
				LA	40	85	40	85	40	75	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports–All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port–All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			COM'L.	SA	40	100	40	100	40	95	40	95	40	95	
				LA	35	75	35	75	35	70	35	70	35	70	

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

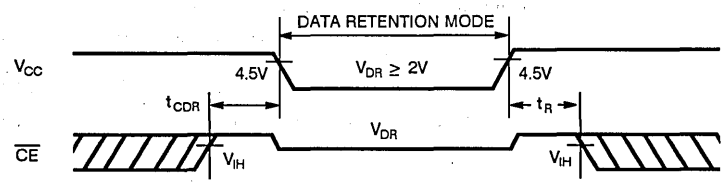
DATA RETENTION CHARACTERISTICS (LA Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7132LA/IDT7142LA MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

5

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

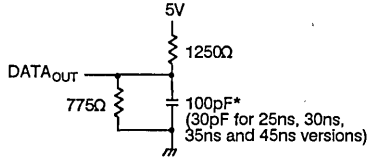


Figure 1. Output Load

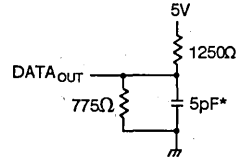


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

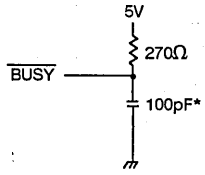


Figure 3. $\overline{BUSY}$ Output Load (IDT7132 only)

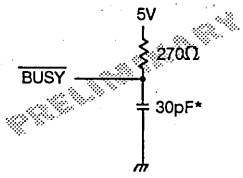


Figure 4. $\overline{BUSY}$ Output Load (for 25ns and 30ns versions)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5]

SYMBOL	PARAMETER	7132 x 25 [2] 7142 x 25 [2]		7132 x 30 [2] 7142 x 30 [2]		7132 x 35 [2] 7142 x 35 [2]		7132 x 45 7142 x 45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	ns
t_{ACE}	Chip Enable Access Time	–	25	–	30	–	35	–	45	ns
t_{AOE}	Output Enable Access Time	–	12	–	15	–	25	–	30	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time [1, 4]	0	–	0	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 4]	–	10	–	12	–	15	–	20	ns
t_{PU}	Chip Enable to Power Up Time [4]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [4]	–	50	–	50	–	50	–	50	ns

5

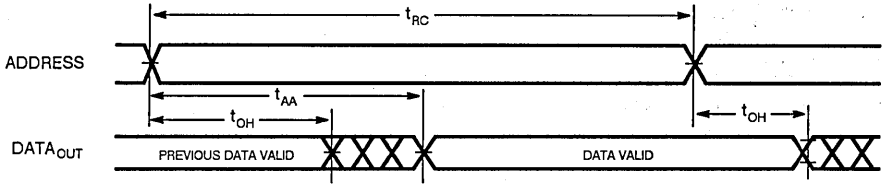
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5] (Continued)

SYMBOL	PARAMETER	7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100 7142 x 100		7132 x 120[3] 7142 x 120[3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	55	–	70	–	90	–	100	–	120	–	ns
t_{AA}	Address Access Time	–	55	–	70	–	90	–	100	–	120	ns
t_{ACE}	Chip Enable Access Time	–	55	–	70	–	90	–	100	–	120	ns
t_{AOE}	Output Enable Access Time	–	35	–	40	–	40	–	40	–	60	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	10	–	10	–	10	–	ns
t_{LZ}	Output Low Z Time [1, 4]	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 4]	–	30	–	35	–	40	–	40	–	40	ns
t_{PU}	Chip Enable to Power Up Time [4]	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [4]	–	50	–	50	–	50	–	50	–	50	ns

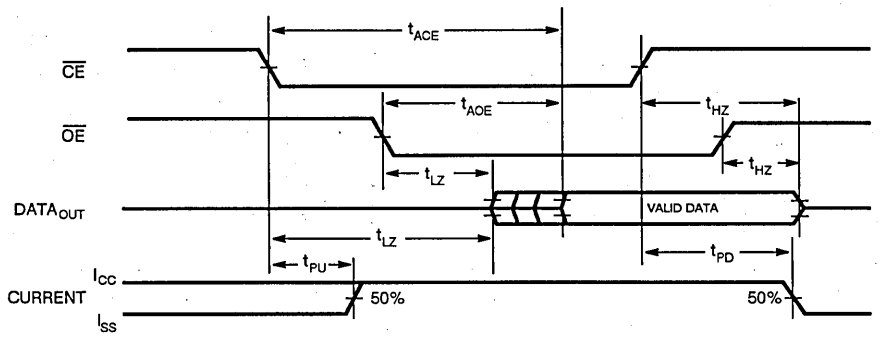
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [7]

SYMBOL	PARAMETER	7132 x 25[2] 7142 x 25[2] MIN.	MAX.	7132 x 30[2] 7142 x 30[2] MIN.	MAX.	7132 x 35[2] 7142 x 35[2] MIN.	MAX.	7132 x 45 7142 x 45 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time[5]	25	–	30	–	35	–	45	–	ns
t_{EW}	Chip Enable to End of Write	20	–	25	–	30	–	35	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[6]	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	12	–	15	–	20	–	20	–	ns
t_{HZ}	Output High Z Time[1, 4]	–	10	–	12	–	15	–	20	ns
t_{DH}	Data Hold Tme	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1, 4]	–	10	–	12	–	15	–	20	ns
t_{OW}	Output Active From End of Write[1, 4]	0	–	0	–	0	–	0	–	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, t_{WC} = t_{BAA} + t_{WP}.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (S or L).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [7]

SYMBOL	PARAMETER	7132 x 55 7142 x 55		7132 x 70 7142 x 70		7132 x 90 7142 x 90		7132 x 100 7142 x 100		7132 x 120[3] 7142 x 120[3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time[5]	55	–	70	–	90	–	100	–	120	–	ns
t_{EW}	Chip Enable to End of Write	40	–	50	–	85	–	90	–	100	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	85	–	90	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	40	–	50	–	55	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	30	–	40	–	40	–	40	–	ns
t_{HZ}	Output High Z Time[1, 4]	–	30	–	35	–	40	–	40	–	40	ns
t_{DH}	Data Hold Tme	0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1, 4]	–	30	–	35	–	40	–	40	–	50	ns
t_{OW}	Output Active From End of Write[1, 4]	0	–	0	–	0	–	0	–	0	–	ns

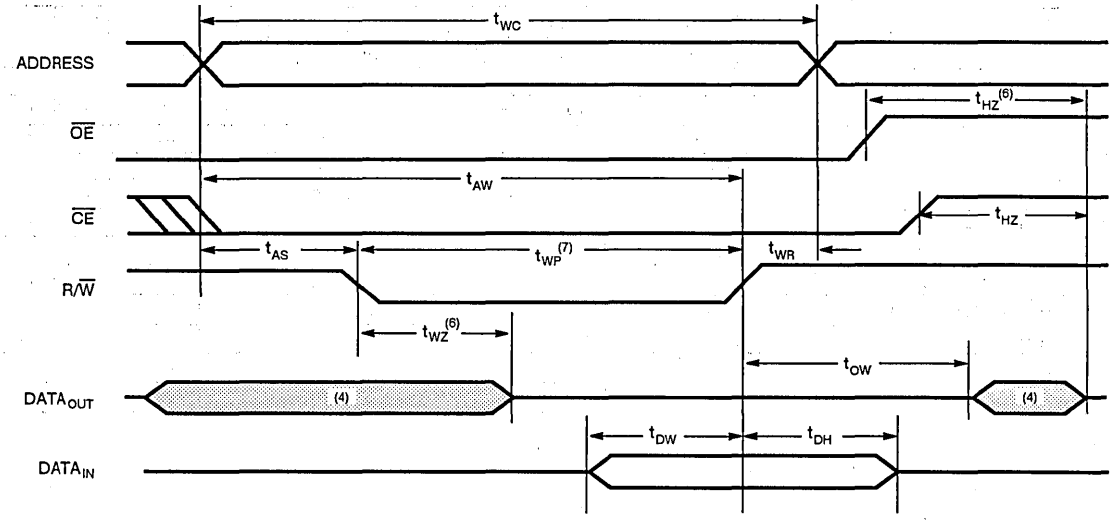
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (S or L).

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

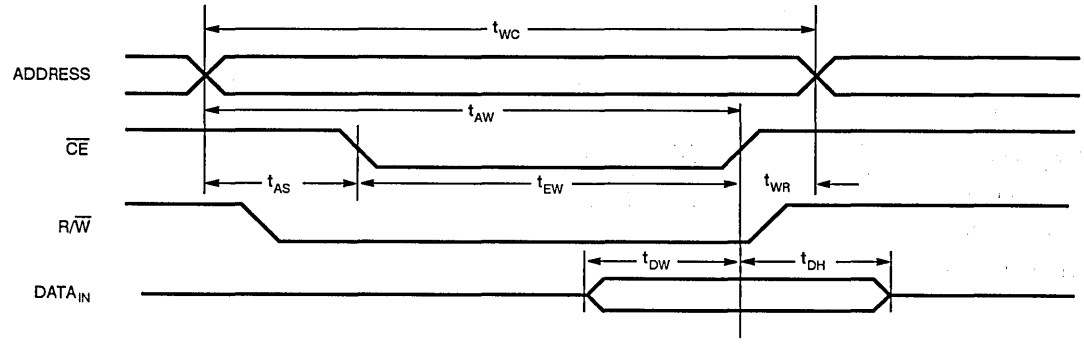
SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING) [1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) [1, 2, 3, 5]



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ}+ t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5]

SYMBOL	PARAMETER	7132 x 25[1] 7142 x 25[1] MIN.	MAX.	7132 x 30[1] 7142 x 30[1] MIN.	MAX.	7132 x 35[1] 7142 x 35[1] MIN.	MAX.	7132 x 45 7142 x 45 MIN.	MAX.	UNIT
BUSY TIMING (FOR MASTER IDT7132 ONLY)										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	25	–	30	–	35	–	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	20	–	25	–	30	–	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	20	–	25	–	30	–	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	20	–	25	–	25	–	25	ns
t_{WDD}	Write Pulse to Data Delay[3]	–	50	–	55	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	–	30	–	30	–	35	–	45	ns
t_{APS}	Arbitration Priority Set-up Time[4]	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7142 ONLY)										
t_{WB}	Write to $\overline{BUSY}$ Input[6]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[3]	15	–	20	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay[9]	–	50	–	55	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	–	30	–	30	–	35	–	45	ns

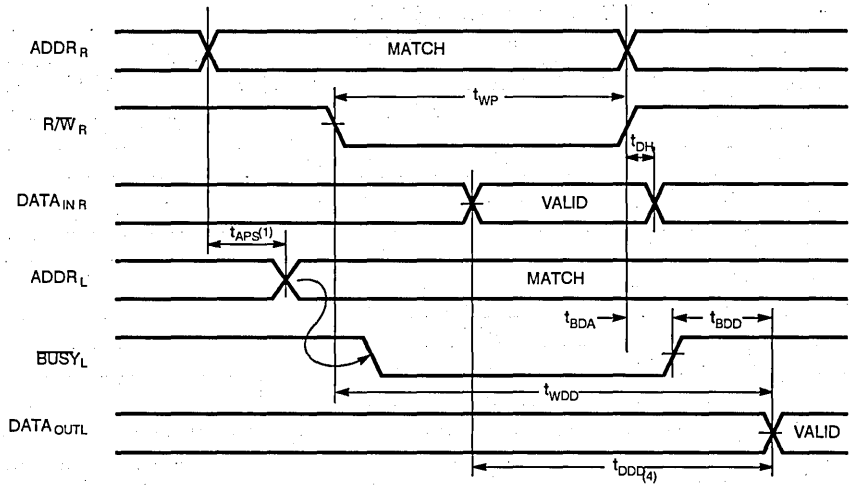
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [5]

SYMBOL	PARAMETER	7132 x 55 7142 x 55 MIN.	MAX.	7132 x 70 7142 x 70 MIN.	MAX.	7132 x 90 7142 x 90 MIN.	MAX.	7132 x 100 7142 x 100 MIN.	MAX.	7132 x 120[2] 7142 x 120[2] MIN.	MAX.	UNIT
BUSY TIMING (FOR MASTER IDT7132 ONLY)												
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	45	–	45	–	45	–	50	–	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	40	–	40	–	45	–	50	–	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	35	–	35	–	45	–	50	–	60	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	30	–	30	–	45	–	50	–	60	ns
t_{WDD}	Write Pulse to Data Delay[3]	–	80	–	90	–	100	–	120	–	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	–	55	–	70	–	90	–	100	–	120	ns
t_{APS}	Arbitration Priority Set-up Time[4]	5	–	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7142 ONLY)												
t_{WB}	Write to $\overline{BUSY}$ Input[6]	0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[7]	20	–	20	–	20	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay[9]	–	80	–	90	–	100	–	120	–	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	–	55	–	70	–	90	–	100	–	120	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7132 only)".
4. To ensure that the earlier of the two ports wins.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual or $t_{DDD} - t_{WP}$ (actual)
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7142 Only)".

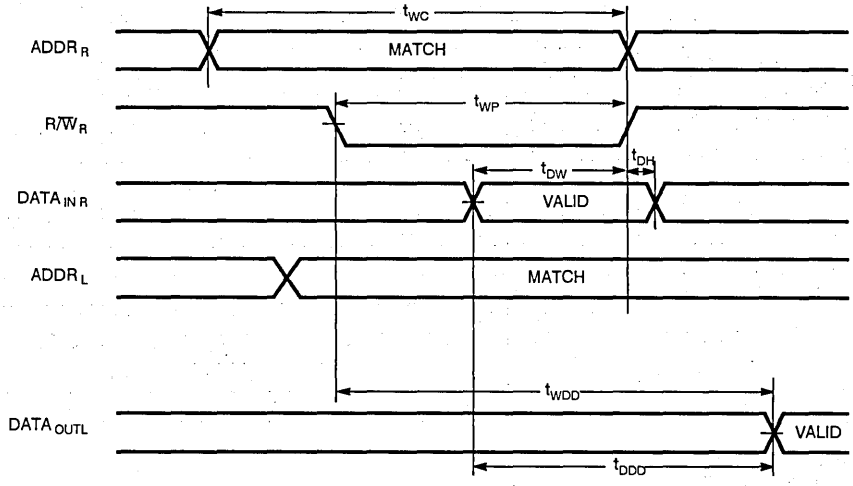
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1, 2, 3)(FOR MASTER IDT7132 ONLY)



NOTES:

1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

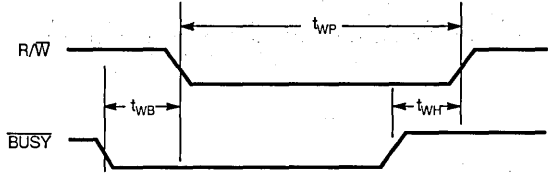
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2, 3)(FOR SLAVE IDT7142 ONLY)



NOTES:

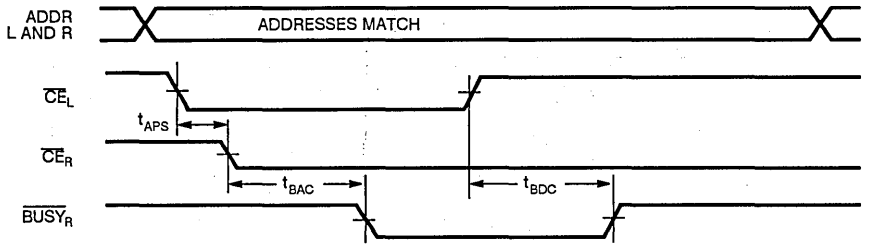
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7142 ONLY)

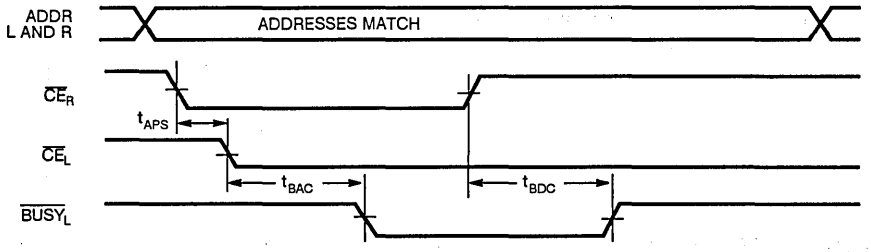


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



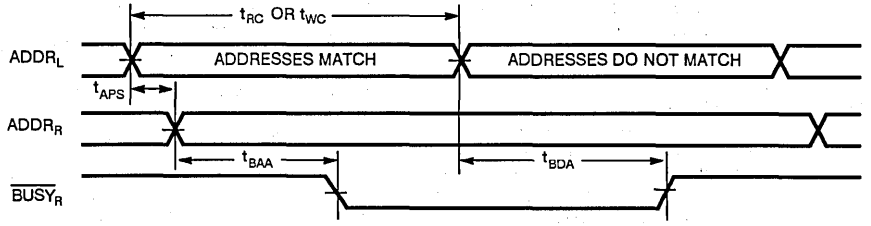
$\overline{CE}_R$ VALID FIRST:



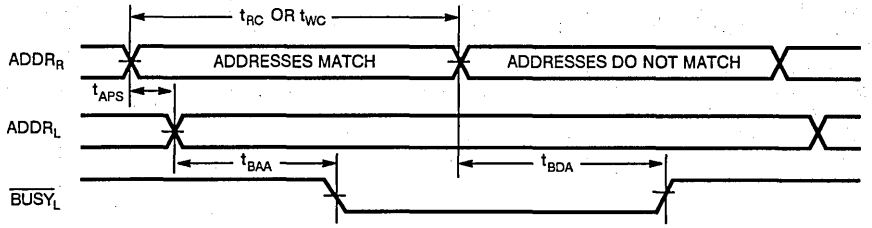
5

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION [1]

LEFT ADDRESS VALID FIRST:

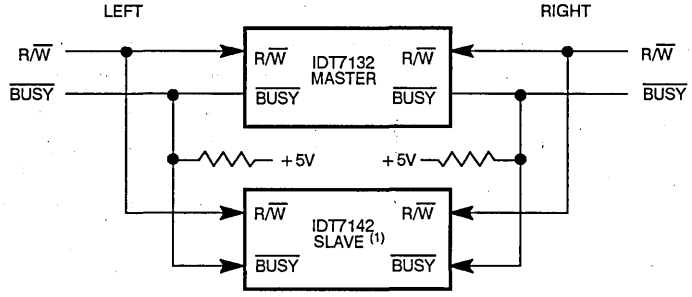


RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT7142 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)				FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port (3)
H	L	H	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{BDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

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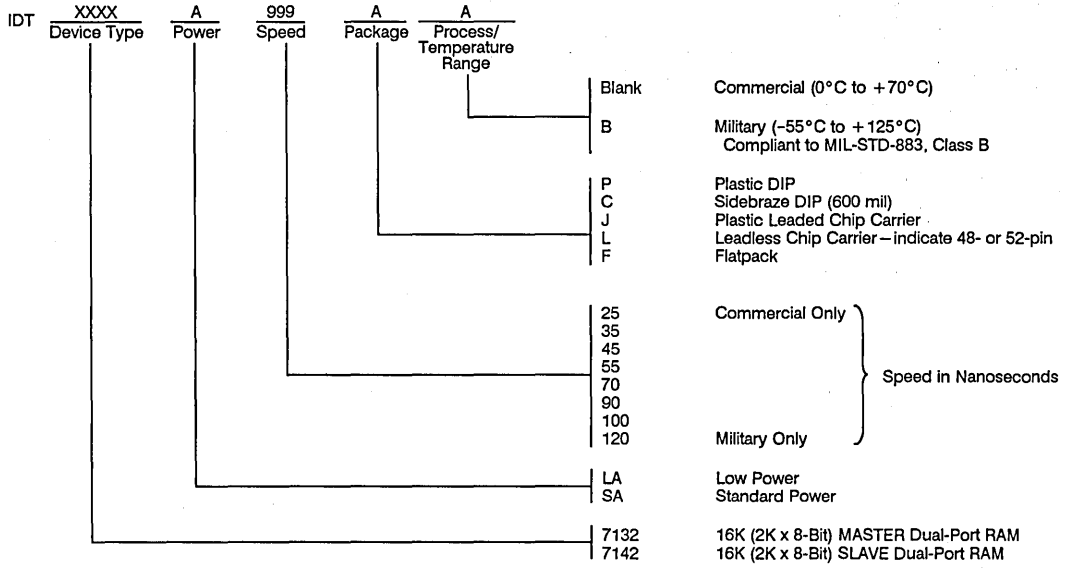
TABLE II – ARBITRATION (2)

LEFT PORT		RIGHT PORT		FLAGS (1)		FUNCTION
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}-A_{10R}$	L	$\neq A_{0L}-A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R}-A_{10R}$	LL5R	$= A_{0L}-A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R}-A_{10R}$	RL5L	$= A_{0L}-A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	L	H	Arbitration Resolved

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid $\geq$ 5ns before right address.
   RV5L = Right Address Valid $\geq$ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 16K (2K x 8-BIT) WITH INTERRUPTS

IDT 71321SA/LA
IDT 71421SA/LA

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 25/30/35/45/55ns (max.)
- Low-power operation
  - IDT71321/421SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - IDT71321/421LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM, together with the IDT71421 "SLAVE" dual-port, in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

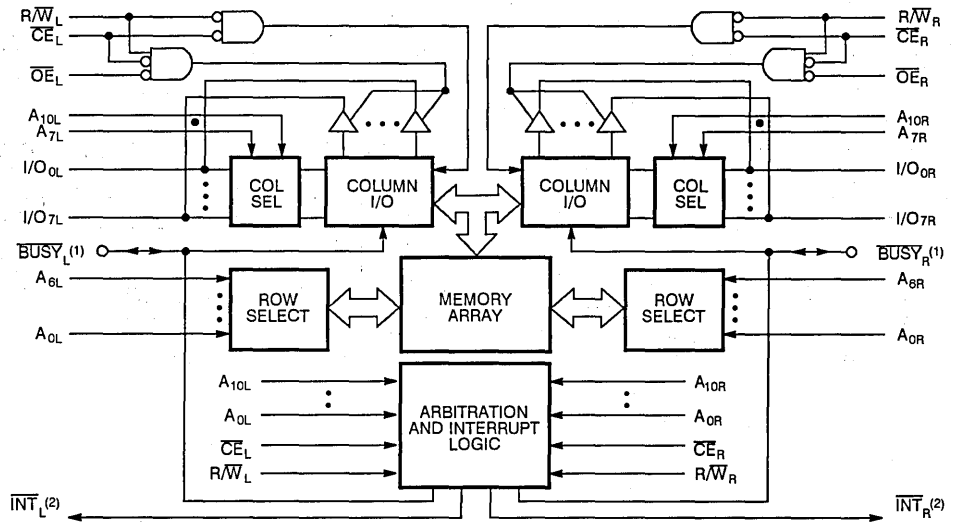
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 25ns. Low-power (LA) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT71321/71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM

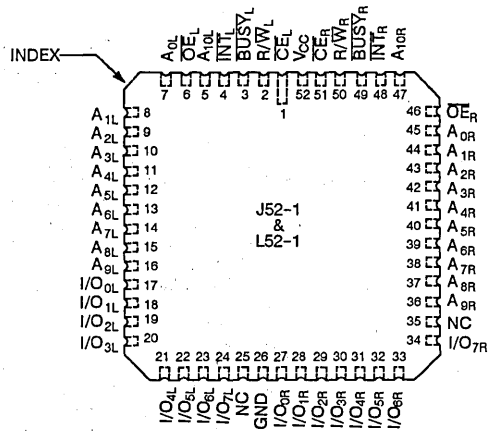


NOTES:

1. IDT71321 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	IDT71321SA IDT71421SA MIN.	IDT71321SA IDT71421SA MAX.	IDT71321LA IDT71421LA MIN.	IDT71321LA IDT71421LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0– I/O_7)	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}/\overline{INT}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	VERSION		71321x25/30 71421x25/30 TYP.	71321x25/30 71421x25/30 MAX.	71321x35[2] 71421x35[2] TYP.	71321x35[2] 71421x35[2] MAX.	71321x45 71421x45 TYP.	71321x45 71421x45 MAX.	71321x55 71421x55 TYP.	71321x55 71421x55 MAX.	71321x70[3] 71421x70[3] TYP.	71321x70[3] 71421x70[3] MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX} [4]	MIL.	SA	–	–	–	–	75	230	65	230	65	225	mA
				LA	–	–	–	–	75	185	65	185	65	180	
			COM'L.	SA	75/70	250/240	75	195	75	190	65	180	–	–	
				LA	75/70	180/170	75	155	75	145	65	140	–	–	
I_{SB1}	Standby Current (Both Ports-TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX} [4]	MIL.	SA	–	–	–	–	25	65	25	65	25	65	mA
				LA	–	–	–	–	25	55	25	55	25	55	
			COM'L.	SA	25/25	65/65	25	65	25	65	25	65	–	–	
				LA	25/25	45/45	25	45	25	45	25	45	–	–	
I_{SB2}	Standby Current (One Port-TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX} [4]	MIL.	SA	–	–	–	–	40	135	40	135	40	135	mA
				LA	–	–	–	–	40	110	40	110	40	110	
			COM'L.	SA	50/46	170/155	40	130	40	120	40	115	–	–	
				LA	50/46	120/110	40	95	40	85	40	85	–	–	
I_{SB3}	Full Standby Current (Both Ports-CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq$ V –0.2V $V_{IN} \geq V_{CC}$ –0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	–	–	–	–	1.0	30	1.0	30	1.0	30	mA
				LA	–	–	–	–	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.2/1.2	15/15	1.0	15	1.0	15	1.0	15	–	–	
				LA	0.4/0.4	5/5	0.2	4.0	0.2	4.0	0.2	4.0	–	–	
I_{SB4}	Full Standby Current (One Port-CMOS Level Inputs f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$–0.2V $V_{IN} \geq V_{CC}$ –0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX} [4]	MIL.	SA	–	–	–	–	40	125	40	120	40	110	mA
				LA	–	–	–	–	35	95	35	90	35	80	
			COM'L.	SA	50/45	150/137	40	115	40	115	40	100	–	–	
				LA	46/42	115/105	35	90	35	80	35	75	–	–	

NOTES:

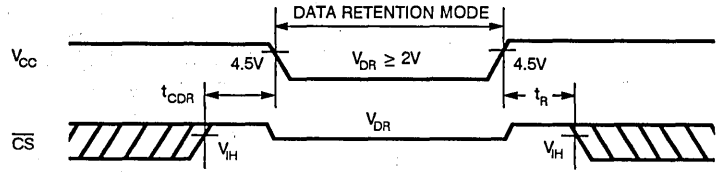
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITION		IDT71321LA/IDT71421LA MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	100	4000	µA
			COM'L.	–	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

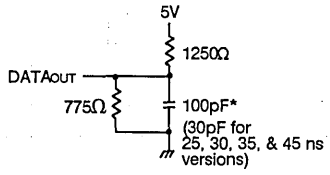


Figure 1. Output Load

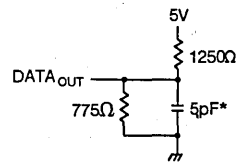


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

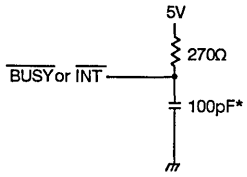


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

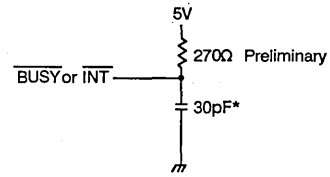


Figure 4. $\overline{BUSY}$ and $\overline{INT}$ Output Load (for 25ns and 30ns versions)

* Including scope and jig.

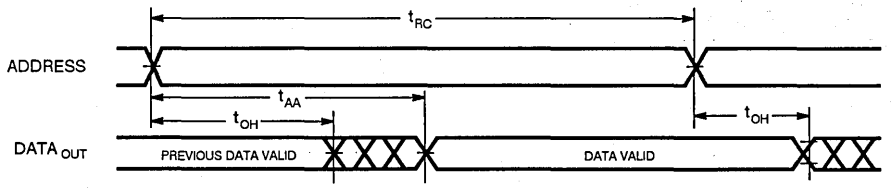
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321x25/30 [2] 71421x25/30 [2]		71321x35 [2] 71421x35 [2]		71321x45 71421x45		71321x55 71421x55		71321x70 [3] 71421x70 [3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	25/30	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25/30	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	25/30	–	35	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	12/15	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold From Address Change	0/0	–	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time [1, 4]	0/0	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 4]	–	10/12	–	15	–	20	–	30	–	35	ns
t_{PU}	Chip Enable to Power Up Time [4]	0/0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [4]	–	50/50	–	50	–	50	–	50	–	50	ns

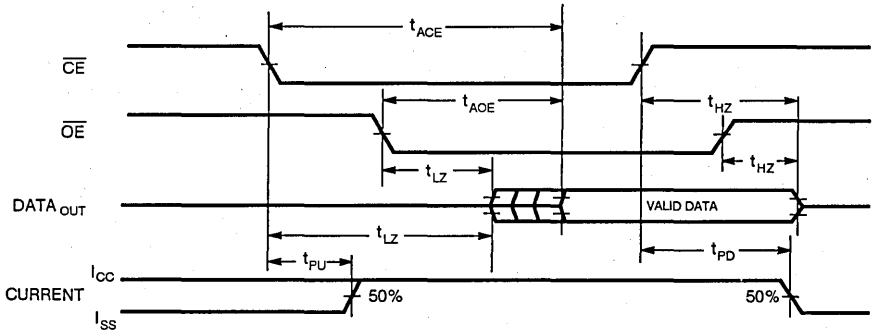
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

5

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to, or coincident with, $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

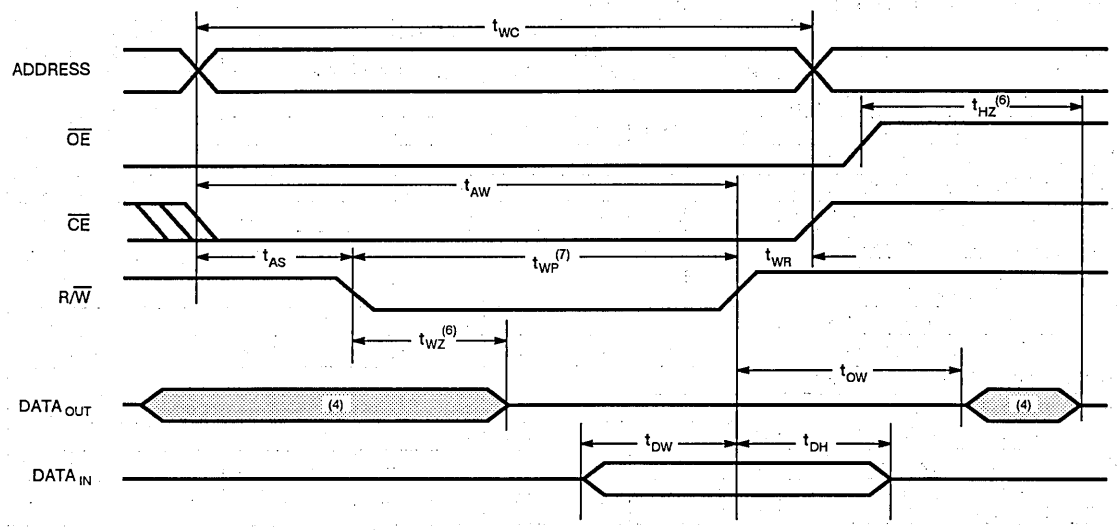
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321x 25/30[2] 71421x 25/30[2] MIN.	MAX.	71321x 35[2] 71421x 35[2] MIN.	MAX.	71321x 45 71421x 45 MIN.	MAX.	71321x 55 71421x 55 MIN.	MAX.	71321x 70[3] 71421x 70[3] MIN.	MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time[5]	25/30	–	35	–	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write	20/25	–	30	–	35	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	20/25	–	30	–	35	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0/0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20/25	–	30	–	35	–	40	–	50	–	ns
t_{WR}	Write Recovery Time	0/0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	12/15	–	20	–	20	–	20	–	30	–	ns
t_{HZ}	Output High Z Time[1,4]	–	10/12	–	15	–	20	–	30	–	35	ns
t_{DH}	Data Hold Time	0/0	–	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	–	10/12	–	15	–	20	–	30	–	35	ns
t_{OW}	Output Active From End of Write[1,4]	0/0	–	0	–	0	–	0	–	0	–	ns

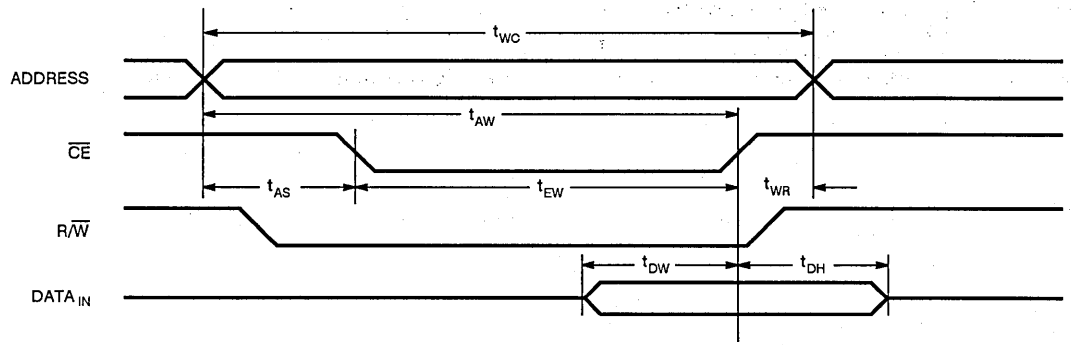
NOTES:

1. Transition is measured ±500mV from low or high voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

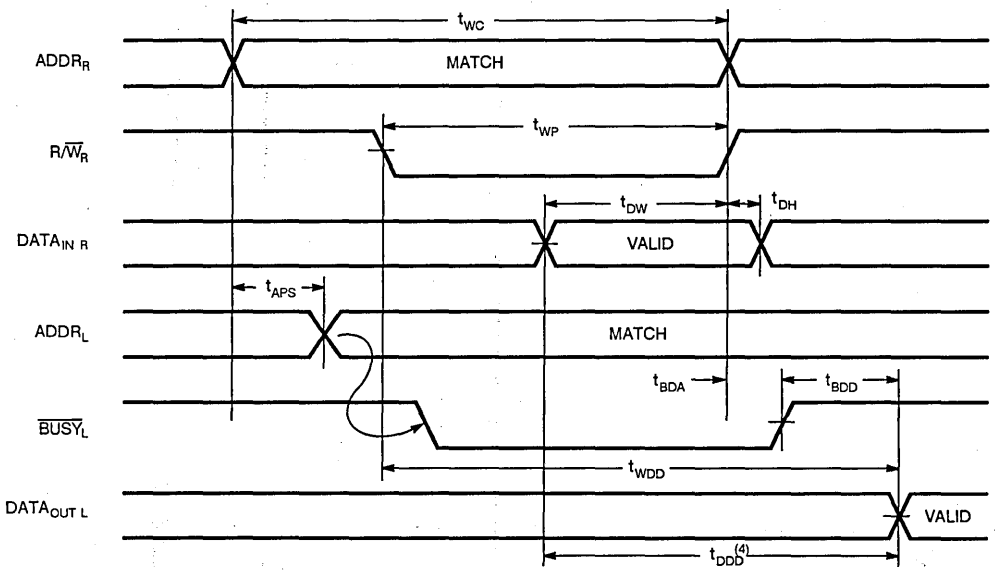
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321x25/30[1] 71421x25/30[1] MIN.	MAX.	71321x35[1] 71421x35[1] MIN.	MAX.	71321x45 71421x45 MIN.	MAX.	71321x55 71421x55 MIN.	MAX.	71321x70[2] 71421x70[2] MIN.	MAX.	UNIT
BUSY TIMING (For Master IDT71321 only)												
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	25/30	–	35	–	35	–	45	–	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	20/25	–	30	–	35	–	40	–	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	20/25	–	30	–	30	–	35	–	35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	20/25	–	25	–	25	–	30	–	30	ns
t_{WDD}	Write Pulse to Data Delay[3]	–	50/55	–	60	–	70	–	80	–	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	–	30/30	–	35	–	45	–	55	–	70	
t_{APS}	Arbitration Priority Set-up Time[4]	5/5	–	5	–	5	–	5	–	5	–	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	–	Note 5	–	Note 5	–	Note 5	–	Note 5	–	Note 5	ns
BUSY TIMING (For Slave IDT71421 only)												
t_{WS}	Write to $\overline{BUSY}$ input[6]	0/0	–	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[7]	15/20	–	20	–	20	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay[9]	–	50/55	–	60	–	70	–	80	90	–	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	–	30/30	–	35	–	45	–	55	–	70	ns

NOTES:

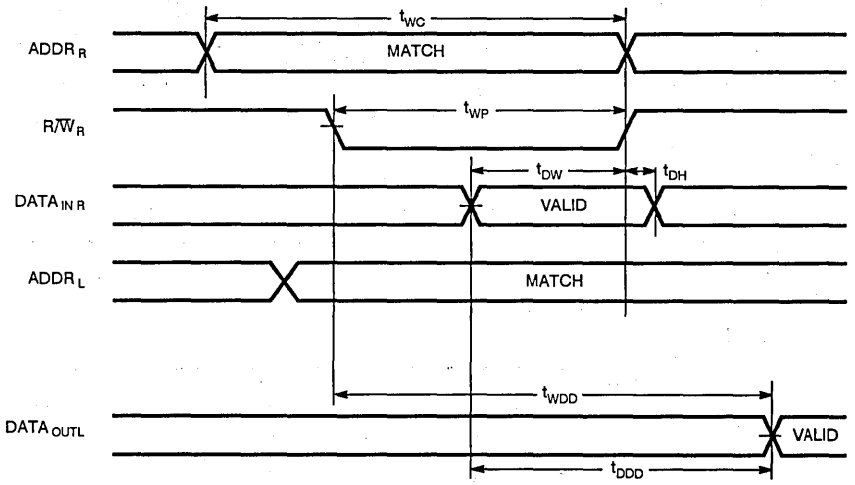
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with BUSY (For Master IDT71321 only)"
4. To ensure that the earlier of the two ports wins.
5. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveforms of Read with Port-to-port delay (For Slave IDT71421 only)"

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ [1, 2, 3] (FOR MASTER IDT71321)



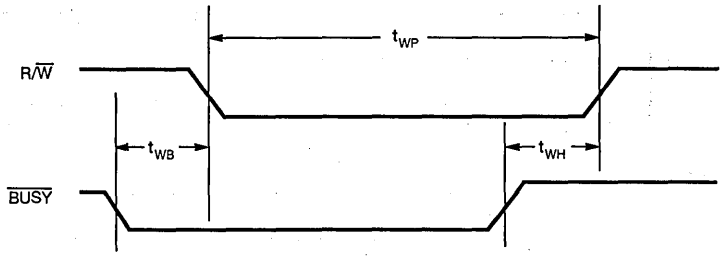
NOTES:
1. To ensure that the earlier of the two port wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at Lo for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY [1, 2, 3] (FOR SLAVE IDT71421 ONLY)



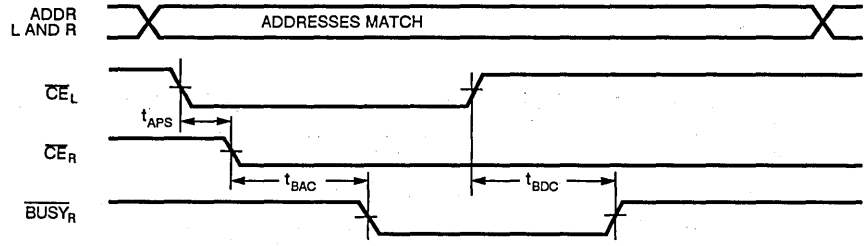
NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (FOR SLAVE IDT71421)

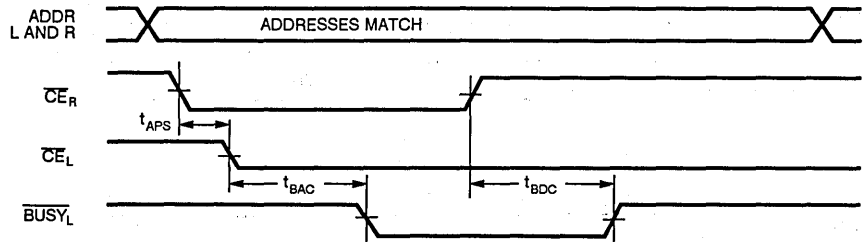


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT71321 ONLY)

$\overline{CE}_L$ VALID FIRST:

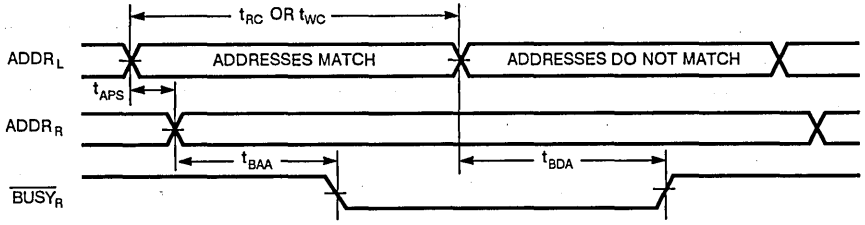


$\overline{CE}_R$ VALID FIRST:

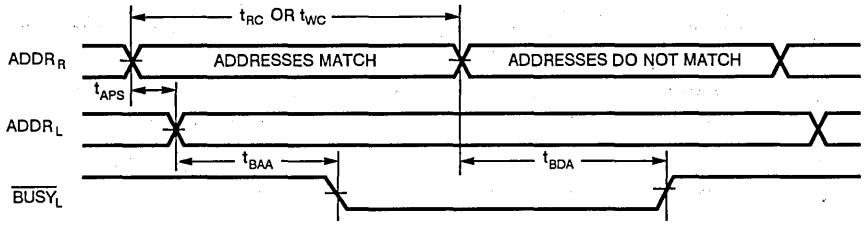


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT71321 ONLY) (1)

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

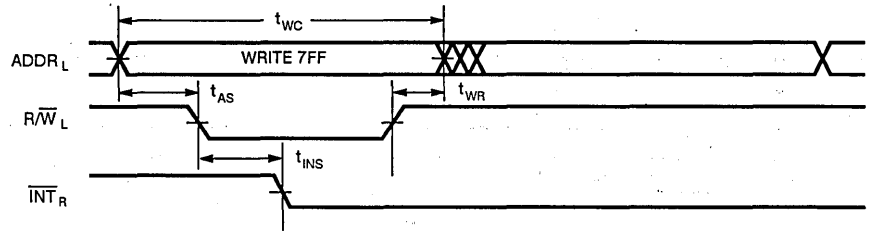
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	71321SA/LA25/30(1) 71421SA/LA25/30(1) MIN.	MAX.	71321SA/LA35(1) 71421SA/LA35(1) MIN.	MAX.	71321SA/LA45 71421SA/LA45 MIN.	MAX.	71321SA/LA55 71421SA/LA55 MIN.	MAX.	71321SA/LA70(2) 71421SA/LA70(2) MIN.	MAX.	UNIT
INTERRUPT TIMING												
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{INS}	Interrupt Set Time	–	25/30	–	35	–	40	–	45	–	50	ns
t_{INR}	Interrupt Reset Time	–	25/30	–	35	–	40	–	45	–	50	ns

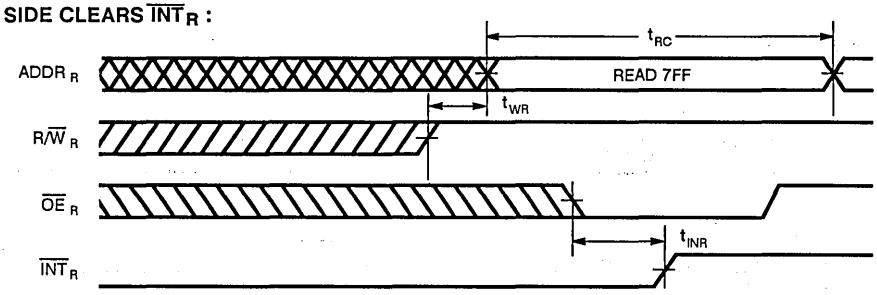
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF INTERRUPT MODE [1, 2]

LEFT SIDE SETS $\overline{INT}_R$:



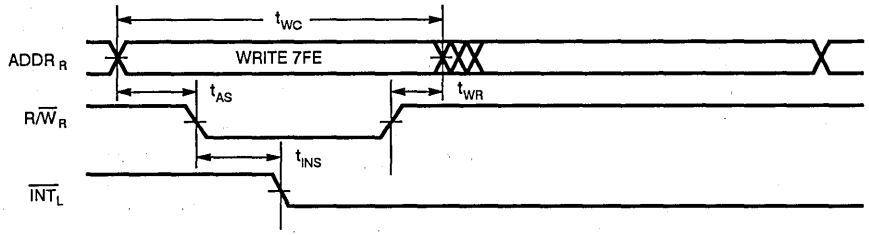
RIGHT SIDE CLEARS $\overline{INT}_R$:



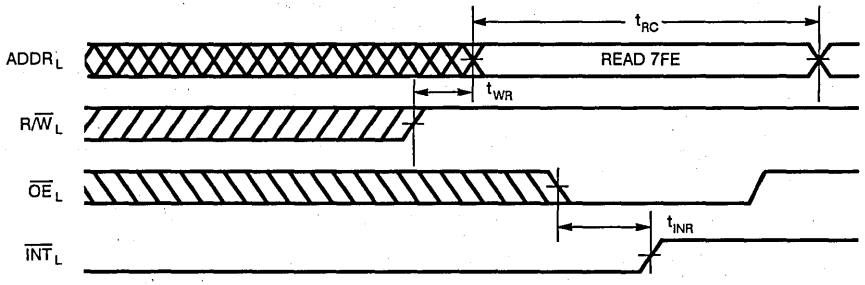
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power up.

TIMING WAVEFORM OF INTERRUPT MODE [1, 2]

RIGHT SIDE SETS $\overline{INT}_L$:



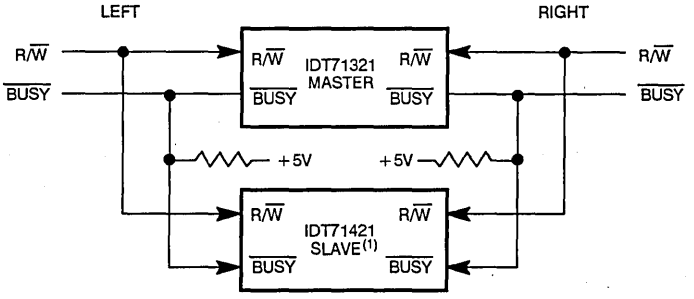
LEFT SIDE CLEARS $\overline{INT}_L$:



NOTES:

1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT71421 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT71421 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT71321/421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$) is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag ($\overline{INT_R}$) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE_L}$ and $\overline{CE_R}$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I—NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT [1]				FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE_R}$ = $\overline{CE_L}$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{BDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

TABLE II – INTERRUPT FLAG [1, 4]

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{10L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{10R}$	$\overline{INT}_R$	
L	L	X	7FF	X	X	X	X	X	L [2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H [3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L [3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H [2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

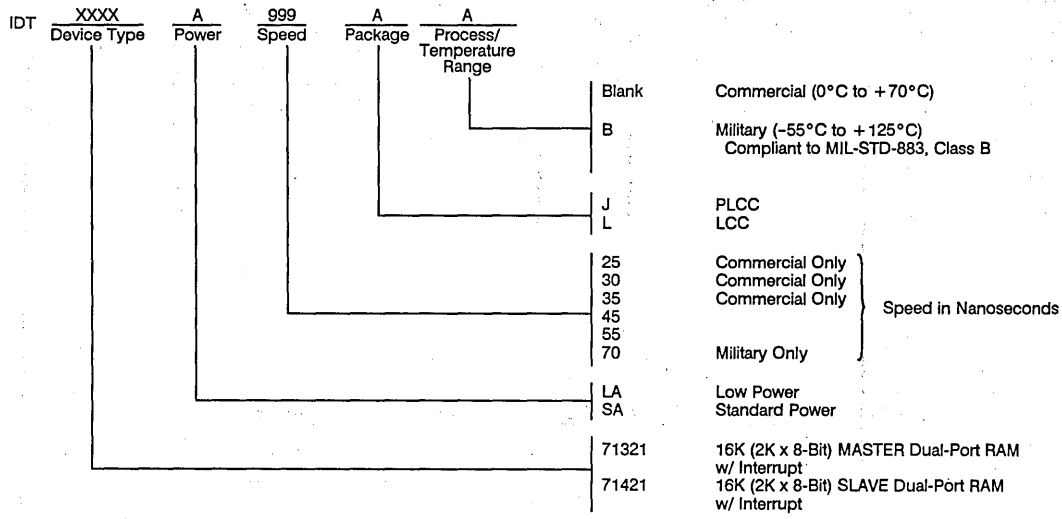
NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III – ARBITRATION [2]

LEFT PORT		RIGHT PORT		FLAGS [1]		FUNCTION
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0L} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ $A_{0R} - A_{10R}$	L	≠ $A_{0L} - A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	= $A_{0R} - A_{10R}$	LL5R	= $A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	= $A_{0R} - A_{10R}$	RL5L	= $A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	L	H	Arbitration Resolved

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7012

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT7012S
    Active: ---mW(typ.)
    Standby: --mW(typ.)
  - IDT7012L
    Active: ---mW(typ.)
    Standby: ---mW(typ.)
- Fully asychronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit.
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (± 10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7012 is an extremely high-speed 2K x 9 dual port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simunltaneously access the same dual-port location.

The IDT7012 provides two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

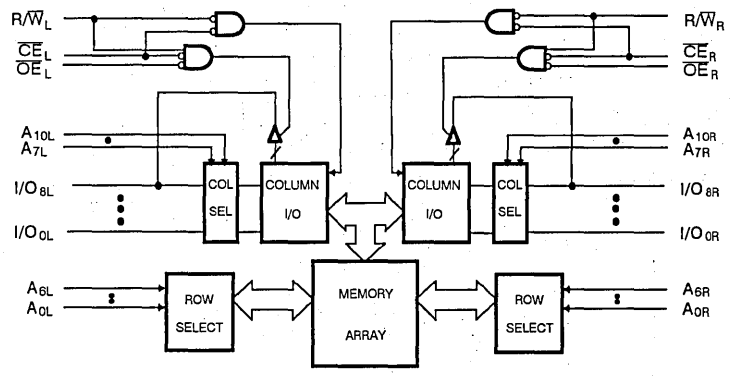
The IDT7012 utilizes a 9-bit wide data path to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7012 is packaged in 48-pin sidebrazed or plastic DIPs, 48- or 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

5

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

ADVANCE INFORMATION
IDT 70121
IDT 70125

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70121/70125S
    Active: ---mW(typ.)
    Standby: --mW(typ.)
  - IDT70121/70125L
    Active: ---mW(typ.)
    Standby: ---mW(typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (± 10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, class B

DESCRIPTION:

The IDT70121/IDT70125 are high-speed 2K x 9 dual port static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70125 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

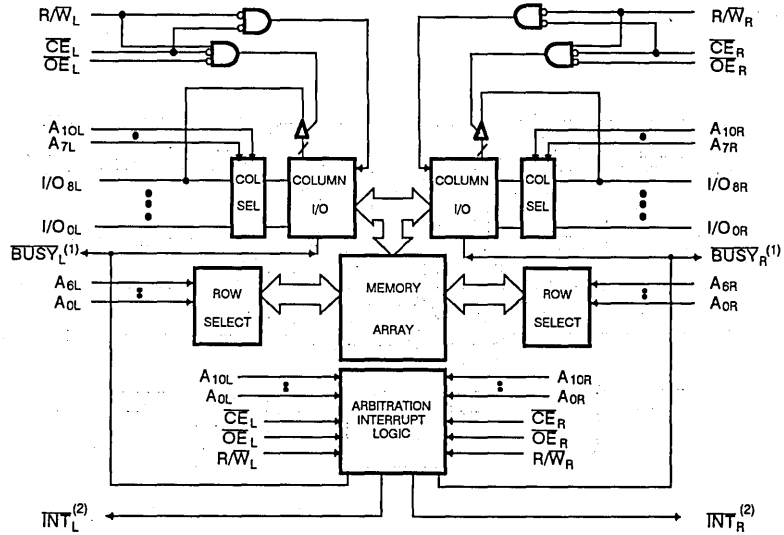
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---mW from a 2V battery.

The IDT70121/70125 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

1. 70121(MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   70125(SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is open drain output and requires pullup resistor.

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CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH SEMAPHORE

IDT 71322S
IDT 71322L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - IDT71322S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71322L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible, single 5V(±10%) power supply
- Available in a variety of plastic and hermetic packages for both through hole and surface mount applications
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71322 is an extremely high-speed 2K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71322 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery.

The IDT71322 is packaged in a 48-pin sidebraze or plastic DIP or 52-pin LCC and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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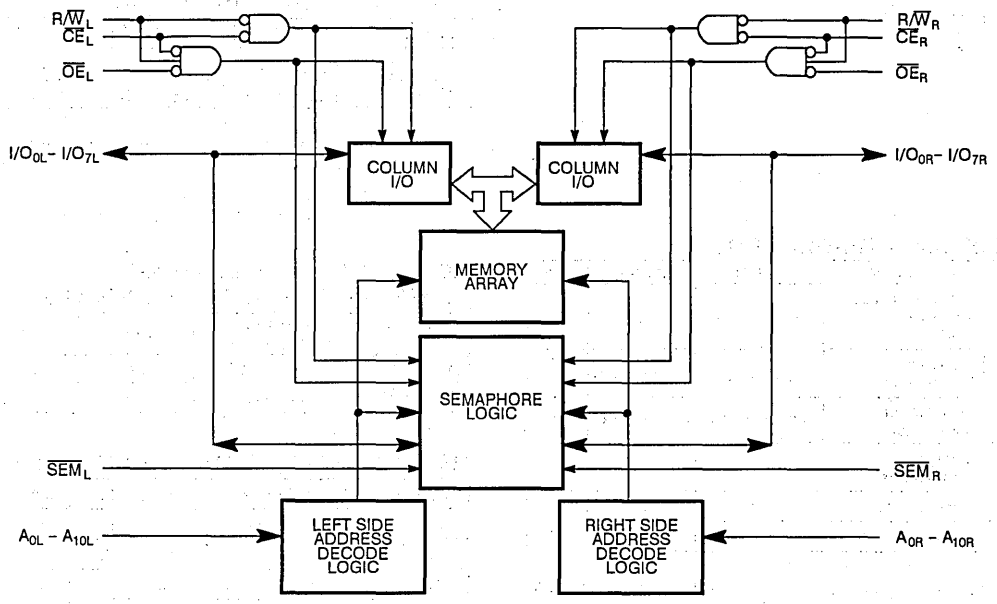
FUNCTIONAL BLOCK DIAGRAM



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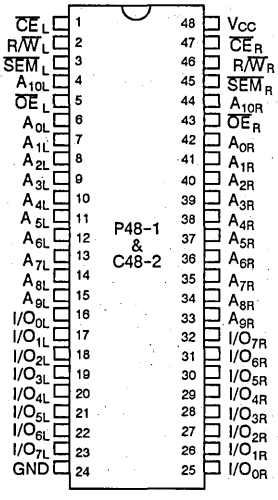
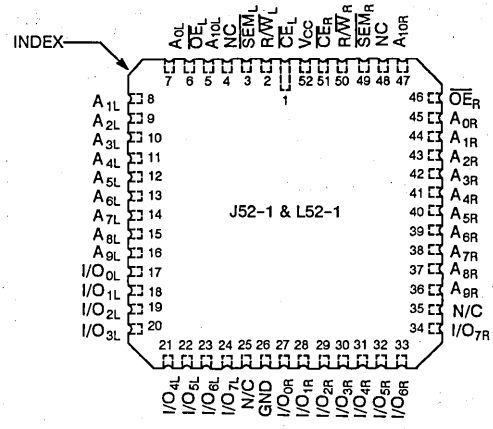
DSC-1032/-1

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characteristics, but is not production tested.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT71322S MIN.	IDT71322S MAX.	IDT71322L MIN.	IDT71322L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT71322x35 COM'L ONLY TYP.[2]	IDT71322x35 COM'L ONLY MAX.	IDT71322x45 TYP.[2]	IDT71322x45 MAX.	IDT71322x55 TYP.[2]	IDT71322x55 MAX.	IDT71322x70 TYP.[2]	IDT71322x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open $\overline{SEM}$ = Don't Care f = f_{MAX}[3]	MIL.	S	–	–	100	240	100	230	100	230	mA
				L	–	–	100	200	100	180	100	180	
			COM'L.	S	–	220	100	200	100	200	100	200	
				L	–	180	100	160	100	160	100	160	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ = V_{IH} $\overline{SEM}$ = V_{IL} Outputs Open f = f_{MAX}[3]	MIL.	S	–	–	85	130	85	130	85	130	mA
				L	–	–	85	110	85	110	85	110	
			COM'L.	S	–	145	85	130	85	130	85	130	
				L	–	115	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{IH}$ f = f_{MAX}[3]	MIL.	S	–	–	25	70	25	70	25	70	mA
				L	–	–	25	50	25	50	25	50	
			COM'L.	S	–	75	25	70	25	70	25	70	
				L	–	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$	MIL.	S	–	–	50	160	50	150	50	150	mA
				L	–	–	50	130	50	120	50	120	
			COM'L.	S	–	140	50	130	50	130	50	130	
				L	–	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, $\overline{SEM}_R = \overline{SEM}_L$ = V_{CC} -0.2V, f = 0[3]	MIL.	S	–	–	1	30	1	30	1	30	mA
				L	–	–	0.2	10	0.2	10	0.2	10	
			COM'L.	S	–	15	1	15	1	15	1	15	
				L	–	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	–	–	50	130	50	120	50	120	mA
				L	–	–	45	100	45	90	45	90	
			COM'L.	S	–	120	45	110	50	110	50	110	
				L	–	100	45	90	45	90	45	90	

NOTES:

1. x in part numbers indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby, I_{SB3}.

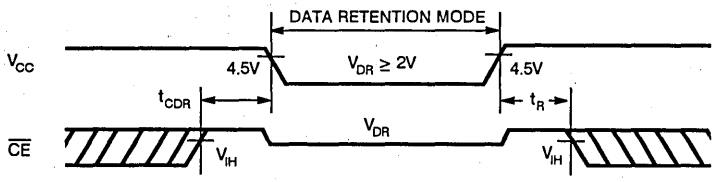
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) 2.0V	MAX. 2.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V $\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	100	4000	µA
			COM'L.	–	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–	–	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–	–	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2 V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

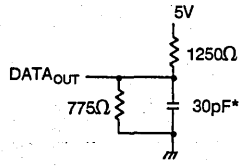


Figure 1. Output Load

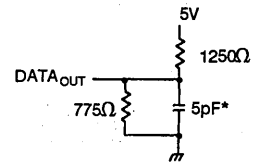


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

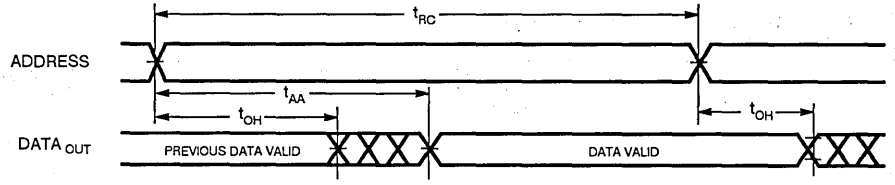
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

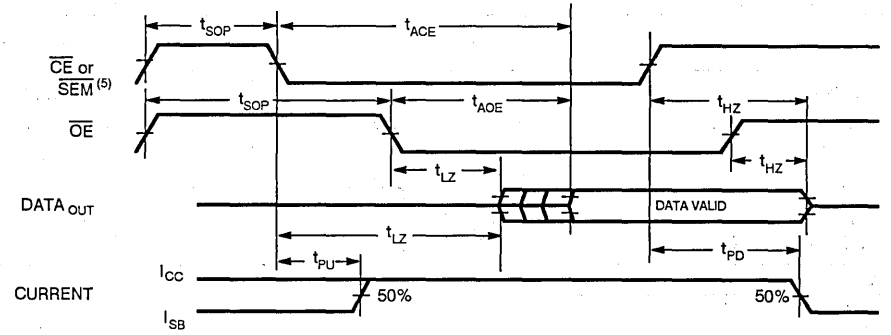
SYMBOL	PARAMETER	IDT71322S35 IDT71322L35 COM'L ONLY		IDT71322S45 IDT71322L45		IDT71322S55 IDT71322L55		IDT71322S70 IDT71322L70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time (3)	–	35	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	20	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time (1, 2)	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 2)	–	20	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time (2)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (2)	–	50	–	50	–	50	–	50	ns
t_{SOP}	Sem Flg update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	15	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay (4)	–	70	–	80	–	90	–	60	ns
t_{DDD}	Write Data Valid to Read Data Delay (4)	–	35	–	45	–	55	–	70	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.
4. Port to Port delay through RAM cells from writing port to Reading port.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)

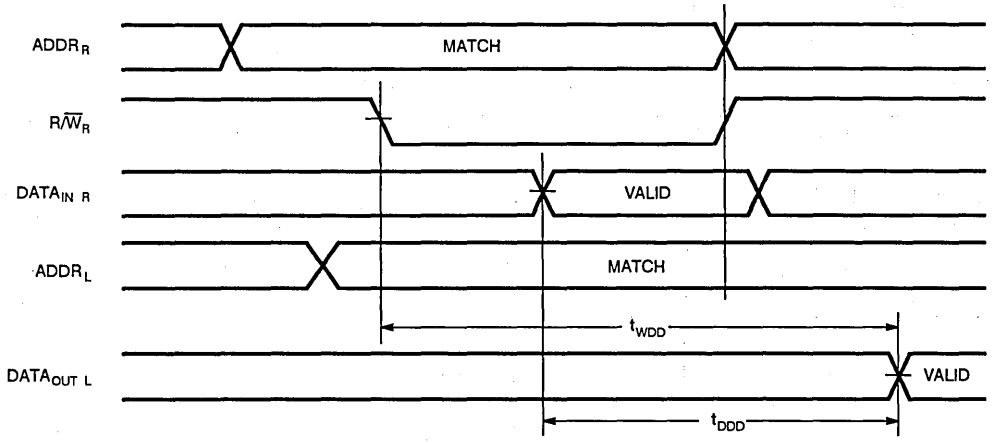


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$
5. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

TIMING WAVEFORM OF READ WITH DELAY



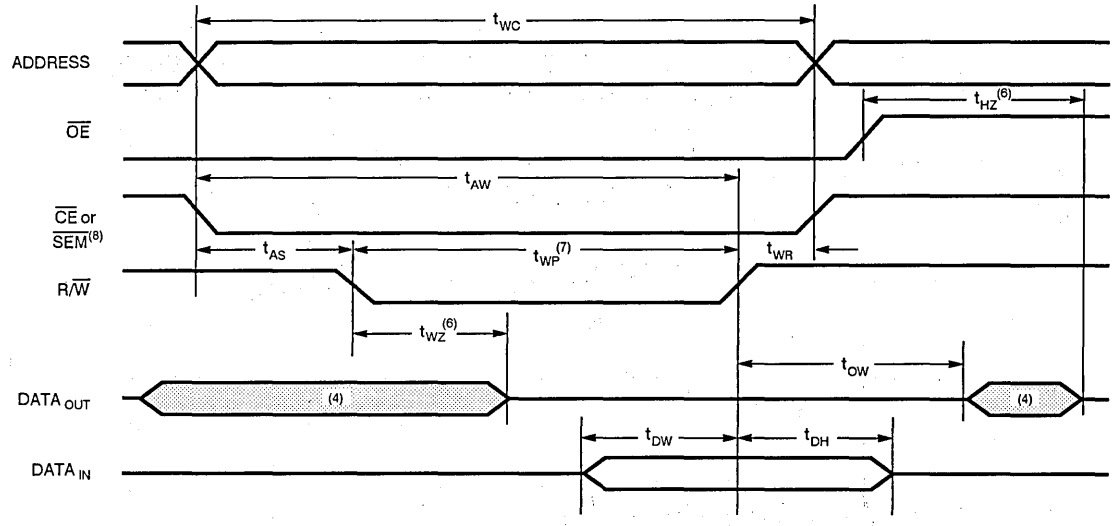
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT71322S35 IDT71322L35 COM'L ONLY		IDT71322S45 IDT71322L45		IDT71322S55 IDT71322L55		IDT71322S70 IDT71322L70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	35	–	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write (3)	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time (1,2)	–	20	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time (4)	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z (1,2)	–	20	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write (1,2,4)	3	–	3	–	3	–	3	–	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	–	10	–	10	–	10	–	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	–	10	–	10	–	10	–	ns

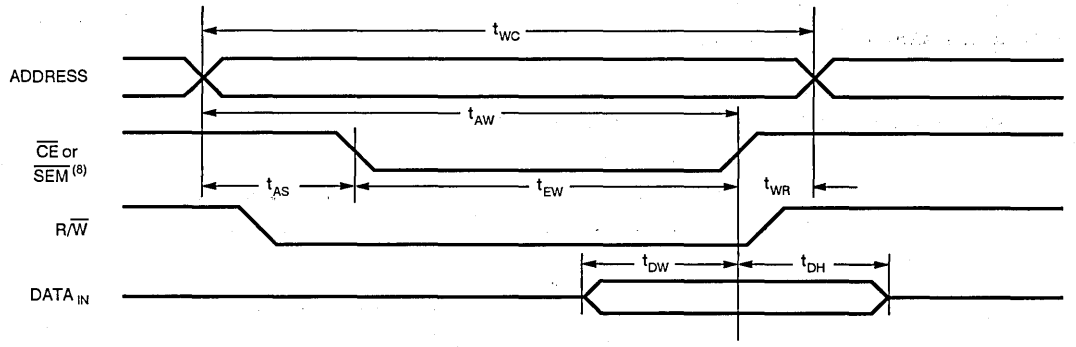
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING [1, 2, 3, 4, 6, 7, 8]



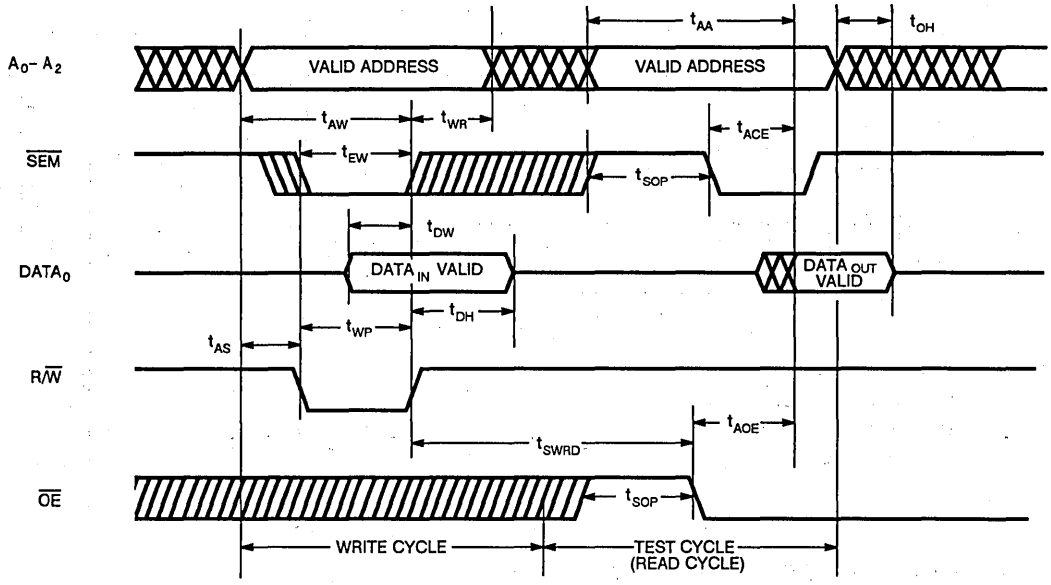
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING [1, 2, 3, 5, 8]



NOTES:

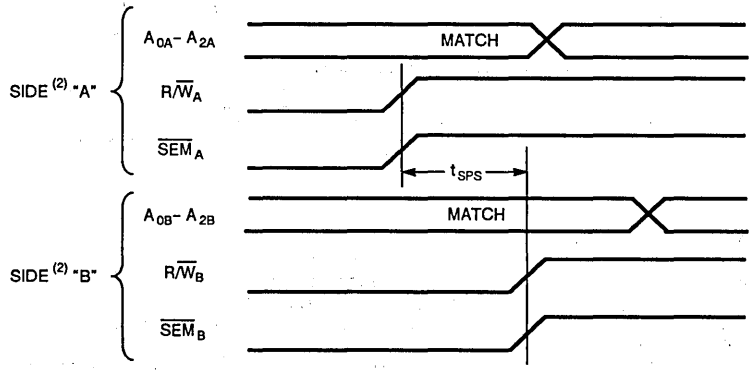
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE [1]



NOTE:
1. $\overline{CE}$ = V_{IH} for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION [1, 3, 4]



NOTES:
1. D_{0R} = D_{0L} = V_{IL}, $\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH}, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71322 is an extremely fast dual-port 2K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table I where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71322 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71322's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71322 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71322 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins $A_0 - A_2$. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT [1]					FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
⌐	H	L	X	$DATA_{IN}$	Port Data Bit D_0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data In Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data On Port Written Into Memory
X	L	L	X	–	Not Allowed

NOTE:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
   ⌐ = Low-to-High transition

TABLE II – EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE [1]

FUNCTION	$D_0 - D_7$ LEFT	$D_0 - D_7$ RIGHT	STATUS
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71322.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71322's dual-port RAM. Say the 2K x 8 RAM was to be divided into two 1K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 1K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 1K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 1K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 1K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

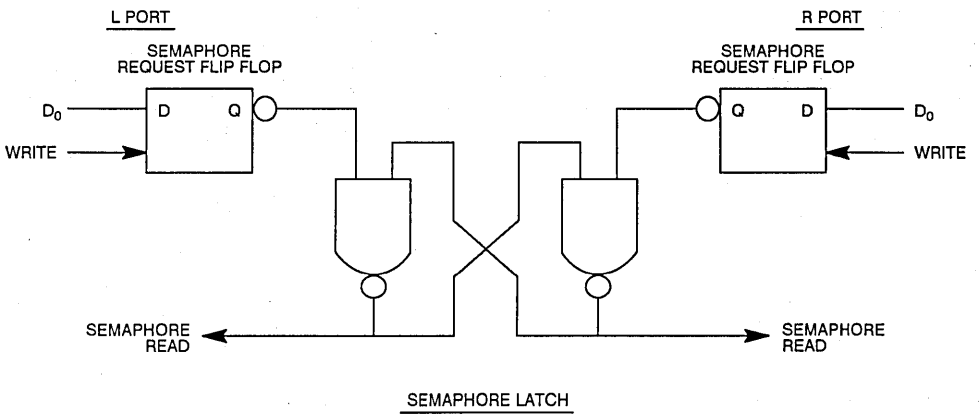
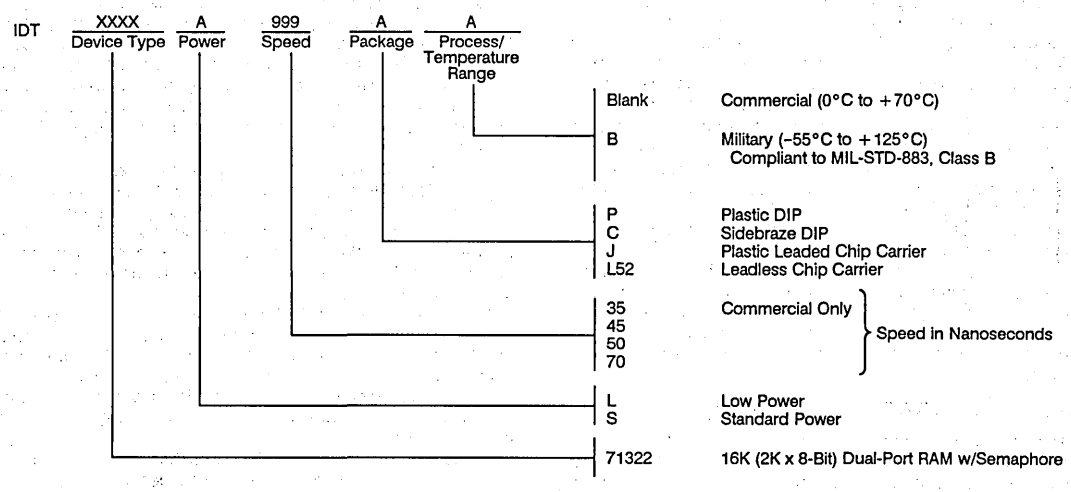


FIGURE 3. IDT71322 Semaphore Logic

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

PRELIMINARY
IDT 7133S/L
IDT 7143S/L

FEATURES:

- High-speed access
  - Military: 55/70/90ns (max.)
  - Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - IDT7133/43S
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - IDT7133/43L
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin ceramic or plastic PGA, DIP (600 mil, 70 mil centers), LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

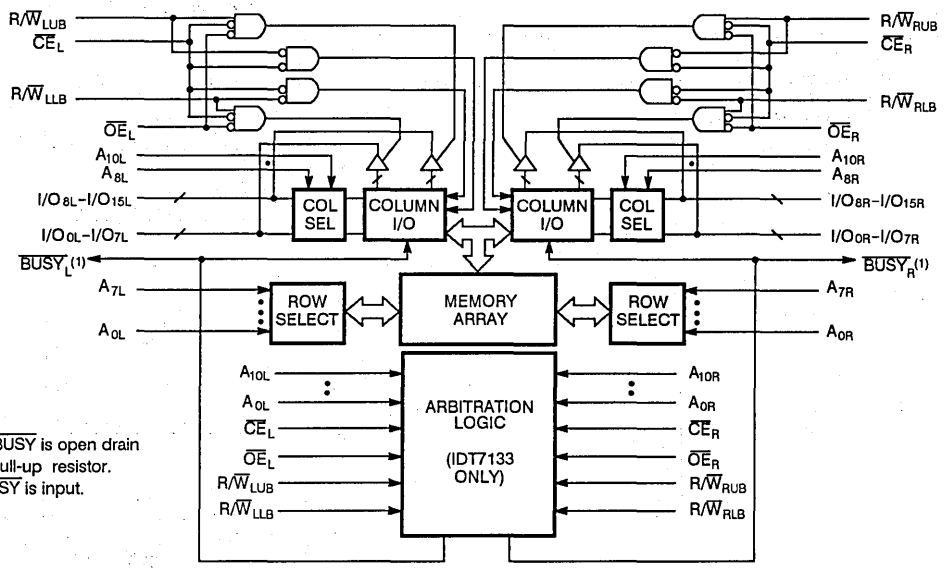
Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 375mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 1mW from a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packaged in a 68-pin ceramic or plastic PGA, 68-pin LCC, 68-pin PLCC, and 70 mil center DIPs.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

5

FUNCTIONAL BLOCK DIAGRAM

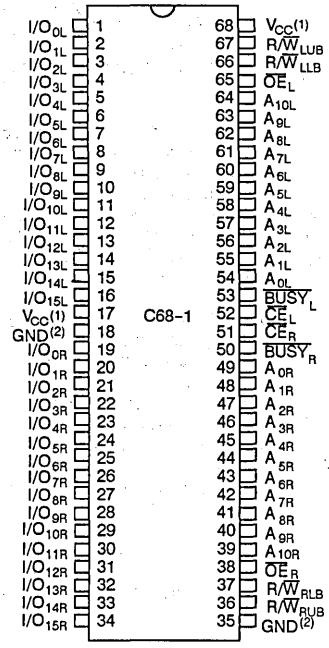


NOTES:

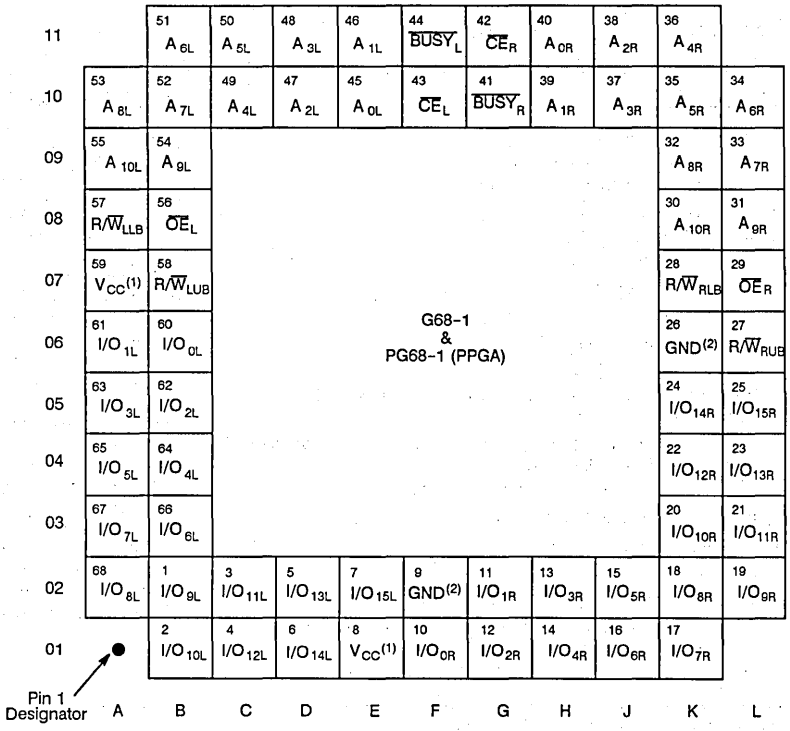
1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): $\overline{BUSY}$ is input.
2. LB = LOWER BYTE
   UB = UPPER BYTE

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



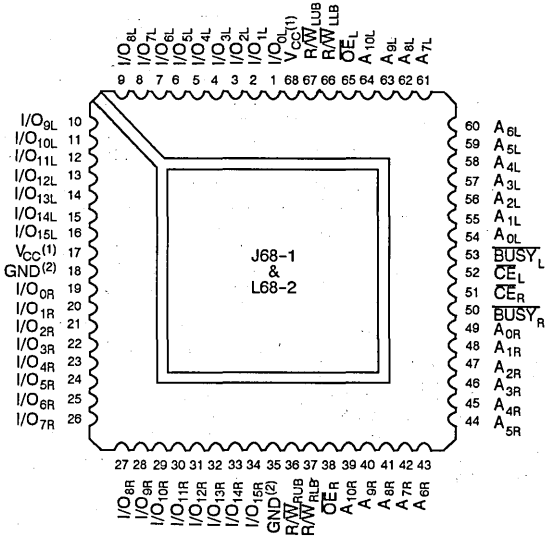
DIP
TOP VIEW



PGA TOP VIEW (Ceramic or Plastic)

NOTES:

1. Both V_{CC} pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte.



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7133S IDT7143S MIN.	IDT7133S IDT7143S MAX.	IDT7133L IDT7143L MIN.	IDT7133L IDT7143L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage (I/O_0 - I/O_{15})	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [3] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7133x45[1] IDT7143x45[1] TYP.[2]	IDT7133x45[1] IDT7143x45[1] MAX.	IDT7133x55 IDT7143x55 TYP.[2]	IDT7133x55 IDT7143x55 MAX.	IDT7133x70 IDT7143x70 TYP.[2]	IDT7133x70 IDT7143x70 MAX.	IDT7133x90 IDT7143x90 TYP.[2]	IDT7133x90 IDT7143x90 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	–	–	–	280	75	260	75	260	mA
				L	–	–	–	260	75	240	75	240	
			COM'L.	S	–	260	75	240	75	240	75	235	
				L	–	240	75	220	75	220	75	215	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	S	–	–	–	80	25	75	25	75	mA
				L	–	–	–	70	25	65	25	65	
			COM'L.	S	–	75	25	70	25	70	25	65	
				L	–	65	25	60	25	60	25	55	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4] Active Port Outputs Open	MIL.	S	–	–	–	180	50	170	50	170	mA
				L	–	–	–	160	50	150	50	150	
			COM'L.	S	–	160	50	150	50	150	50	145	
				L	–	140	50	130	50	130	50	125	
I_{SB3}	Full Standby Current (Both Ports – CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V f = 0[5]	MIL.	S	–	–	–	30	1	30	1	30	mA
				L	–	–	–	10	0.2	10	0.2	10	
			COM'L.	S	–	15	1	15	1	15	1	15	
				L	–	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs, f = 0[5])	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	S	–	–	–	170	45	160	45	155	mA
				L	–	–	–	150	40	140	40	135	
			COM'L.	S	–	150	45	140	45	140	45	135	
				L	–	130	40	120	40	120	40	115	

NOTES:

1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C
3. "x" in part numbers indicates power rating (S or L).
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES [1]

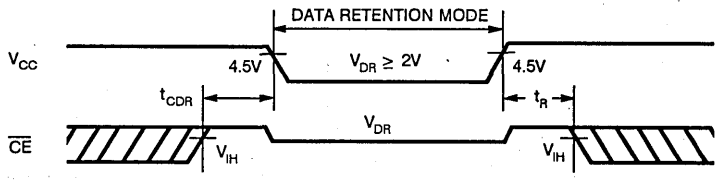
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		IDT7133S/L/IDT7143S/L MIN.	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	V
I_{CCDR}	Data Retention Current		MIL.	–	4000	µA
			COM'L.	–	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	ns
I_{LI}[3]	Input Leakage Current			–	2	µA

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

5

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, & 3

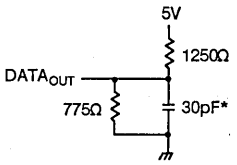


Figure 1. Output Load

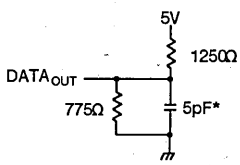


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

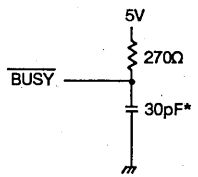


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

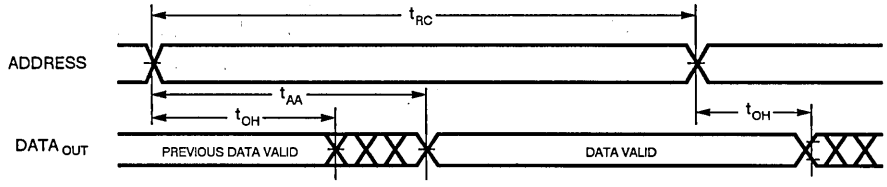
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

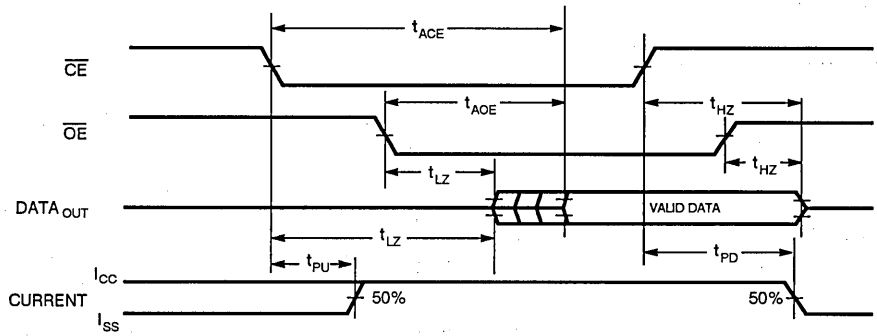
SYMBOL	PARAMETER	IDT7133S/L45 (2) IDT7143S/L45 (2) COM'L ONLY		IDT7133S/L55 IDT7143S/L55		IDT7133S/L70 IDT7143S/L70		IDT7133S/L90 IDT7143S/L90		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
t_{RC}	Read Cycle Time	45	–	55	–	70	–	90	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	–	90	ns
t_{ACE}	Chip Enable Access Time	–	45	–	55	–	70	–	90	ns
t_{AOE}	Output Enable Access Time	–	30	–	35	–	40	–	40	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	10	–	ns
t_{LZ}	Output Low Z Time (1, 3)	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 3)	–	20	–	20	–	25	–	25	ns
t_{PU}	Chip Enable to Power Up Time (3)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (3)	–	50	–	50	–	50	–	50	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (see Figures 1, 2 & 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7133S/L45 [2] IDT7143S/L45 [2] MIN.	MAX.	IDT7133S/L55 IDT7143S/L55 MIN.	MAX.	IDT7133S/L70 IDT7143S/L70 MIN.	MAX.	IDT7133S/L90 IDT7143S/L90 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time[4]	45	–	55	–	70	–	90	–	ns
t_{EW}	Chip Enable to End of Write	30	–	40	–	50	–	85	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	85	–	ns
t_{AS}	Address Setup Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[6]	30	–	40	–	50	–	55	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time[1,3]	–	20	–	20	–	25	–	25	ns
t_{DH}	Data Hold Time[5]	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z[1,3]	–	20	–	20	–	25	–	25	ns
t_{OW}	Output Active From End of Write[1,3,5]	5	–	5	–	5	–	5	–	ns

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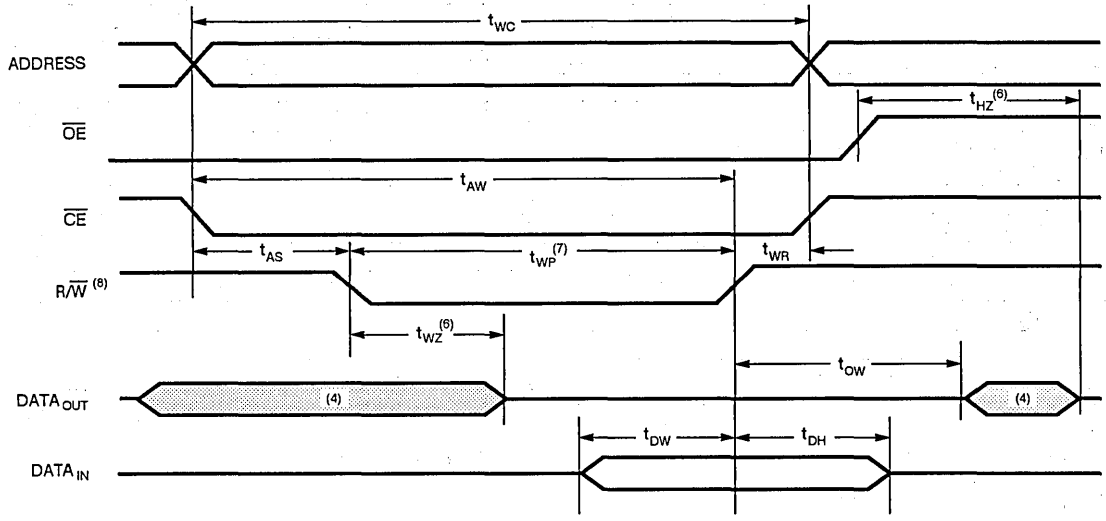
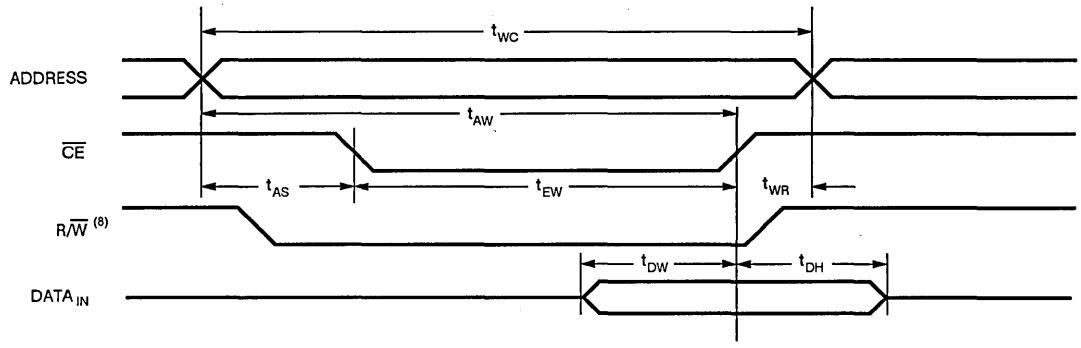
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (see Figures 1, 2 & 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$.
5. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) [1, 2, 3, 7]



WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING) [1, 2, 3, 5]



NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. R/$\overline{W}$ for either upper or lower byte.

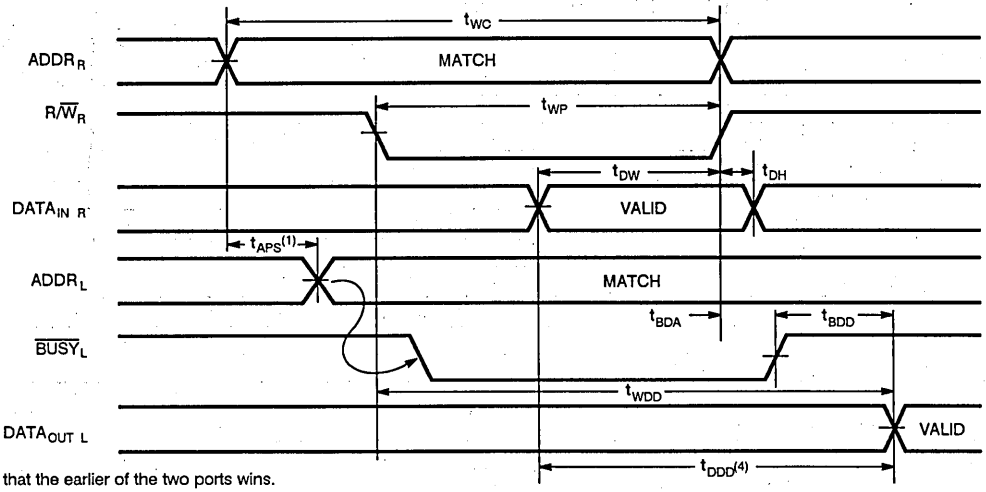
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7133S/L45[1] IDT7143S/L45[1] MIN.	MAX.	IDT7133S/L55 IDT7143S/L55 MIN.	MAX.	IDT7133S/L70 IDT7143S/L70 MIN.	MAX.	IDT7133S/L90 IDT7143S/L90 MIN.	MAX.	UNIT
BUSY TIMING (For MASTER IDT7133)										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	–	45	–	50	–	55	–	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	–	40	–	40	–	45	–	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	–	30	–	35	–	35	–	45	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	–	25	–	30	–	30	–	45	ns
t_{WDD}	Write Pulse to Data Delay[2]	–	80	–	80	–	90	–	100	ns
t_{DDD}	Write Data Valid to Read Data Delay[2]	–	55	–	55	–	70	–	90	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	–	Note 4	–	Note 4	–	Note 4	–	Note 4	ns
t_{APS}	Arbitration Priority Set Up Time[4]	5	–	5	–	5	–	10	–	ns
BUSY INPUT TIMING (For SLAVE IDT7143)										
t_{WB}	Write to $\overline{BUSY}$[5]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$[6]	30	–	30	–	30	–	30	–	ns
t_{WDD}	Write Pulse to Data Delay[7]	–	80	–	80	–	90	–	100	ns
t_{DDD}	Write Data Valid to Read Data Delay[7]	–	55	–	55	–	70	–	90	ns

NOTES:

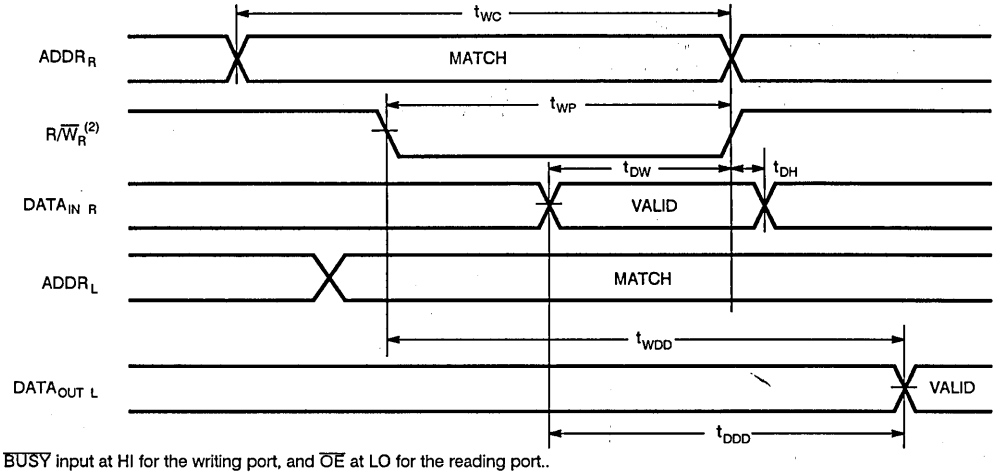
1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH BUSY (For Master IDT7133)"
3. t_{BDD} is calculated parameter and is greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (For Slave IDT7143)"

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ [1, 2, 3] (For MASTER IDT7133)



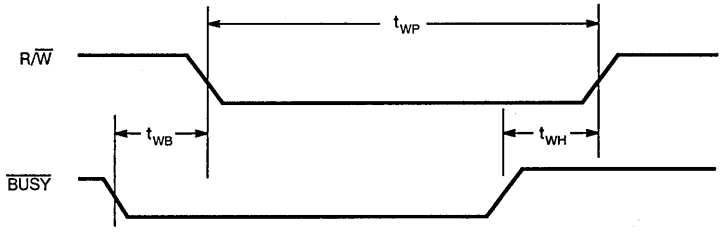
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to for ensuring proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY [1, 2, 3] (For SLAVE IDT7143)



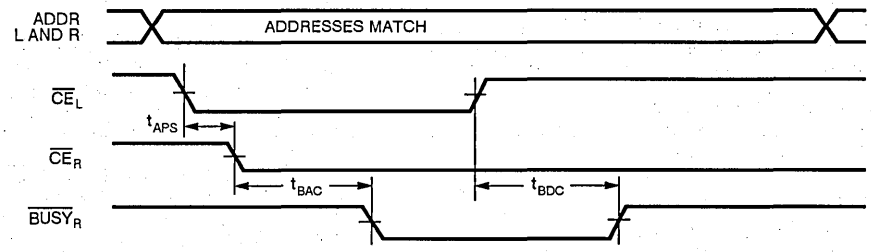
NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port..
2. Write cycle parameters should be adhered to for ensuring proper writing.
3. Device is continously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (For SLAVE IDT7143)

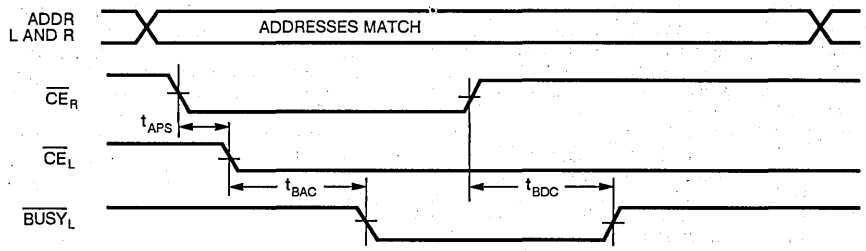


TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:

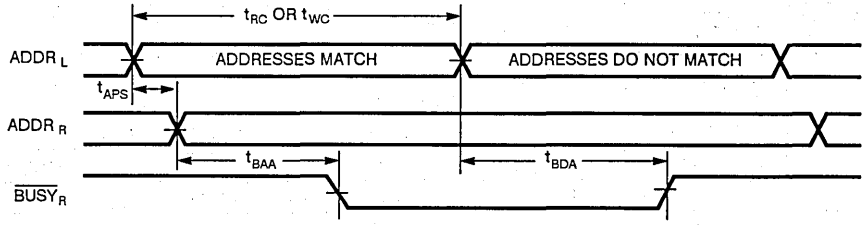


$\overline{CE}_R$ VALID FIRST:

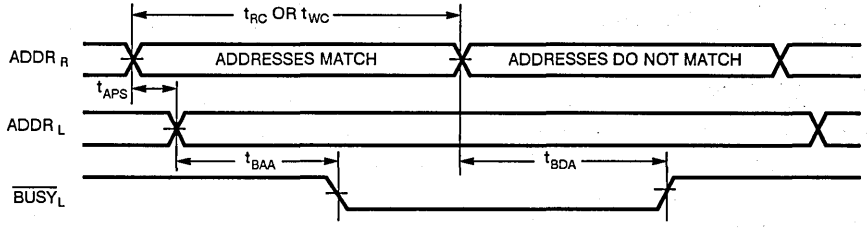


TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1)

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = CE_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TABLE I—NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT [1]						FUNCTION
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	
X	X	H	X	Z	Z	Port Disabled and in Power Down mode, I_{SB2} or I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory,[2] Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte,[3] Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte[3]
H	H	L	H	Z	Z	High Impedance Outputs

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = High, L = Low, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Byte

TABLE II – ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS[1]		FUNCTION
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}-A_{10R}$	L	$\neq A_{0L}-A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R}-A_{10R}$	LL5R	$= A_{0L}-A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R}-A_{10R}$	RL5L	$= A_{0L}-A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R}-A_{10R}$	LW5R	$= A_{0L}-A_{10L}$	L	H	Arbitration Resolved

NOTE:

1. X = Don't Care, L = Low, H = High
   LV5R = Left Address Valid $\geq$ 5ns before right address
   RV5L = Right Address Valid $\geq$ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW $\geq$ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW $\geq$ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

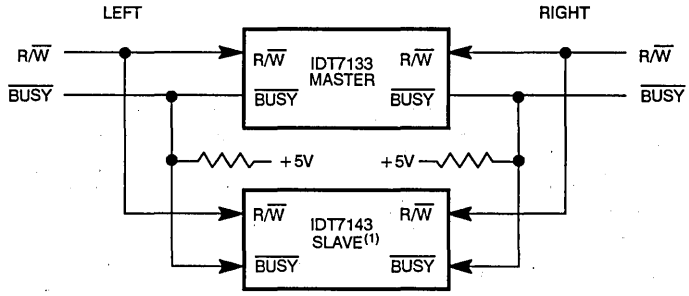
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

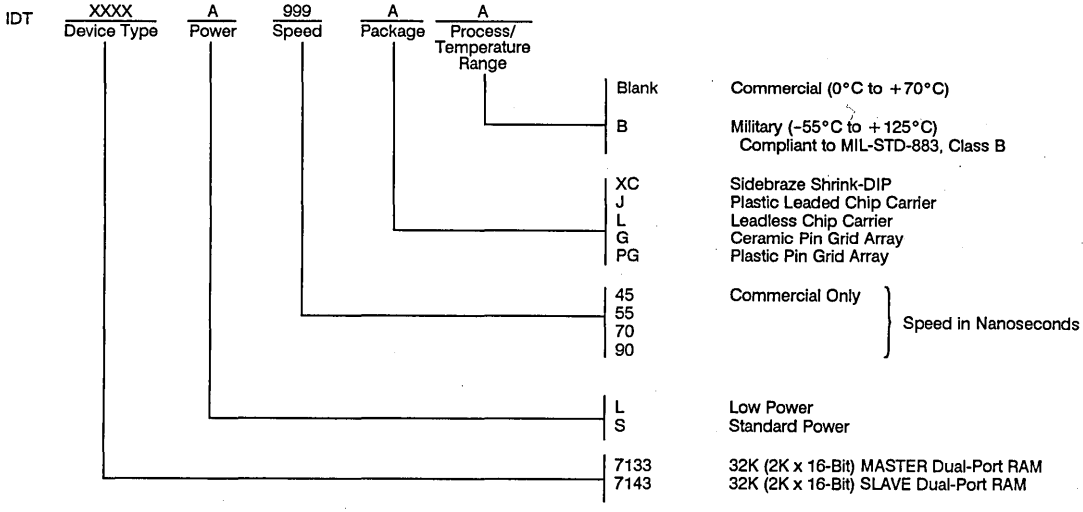
32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:

1. No arbitration in IDT7143 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7143 (SLAVE).

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

IDT 7134S
IDT 7134L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 45/55/70ns (max.)
  - Commercial: 35ns (max.) Preliminary
- Low-power operation
  - IDT7134S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT7134L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7134 is an extremely high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

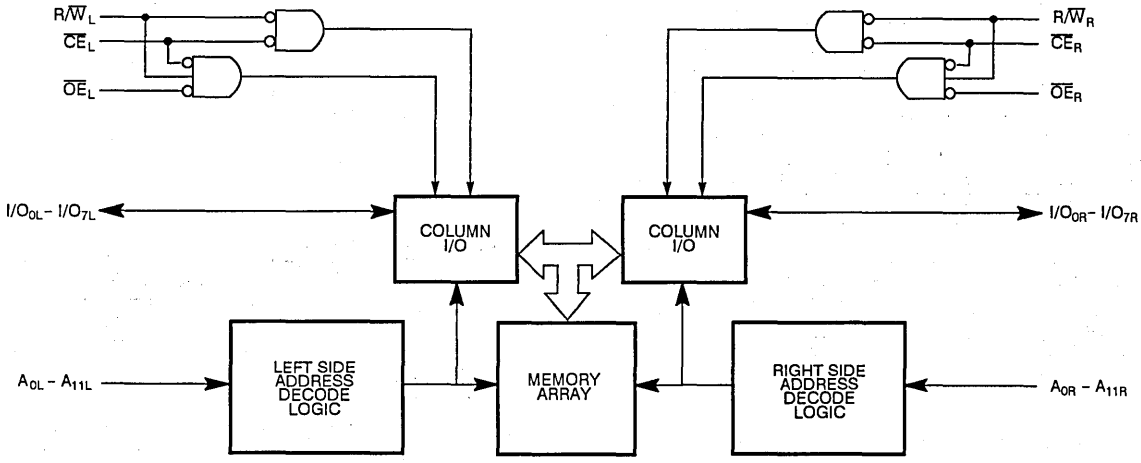
The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-ports typically operate on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200μW from a 2V battery.

The IDT7134 is packaged in either a sidebraze or plastic 48-pin DIP, 48-pin or 52-pin LCC, and 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

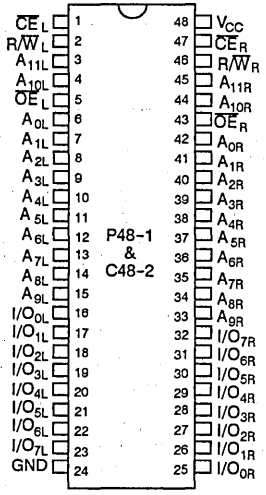
5

FUNCTIONAL BLOCK DIAGRAM

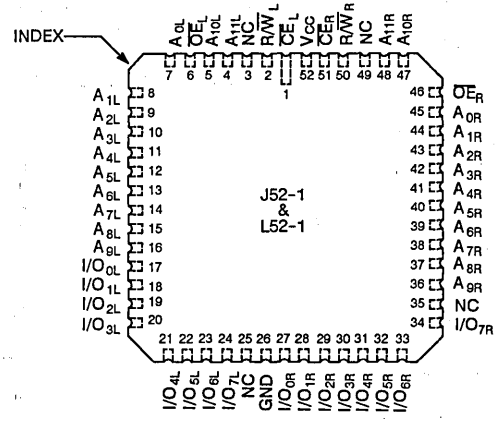


CEMOS is a trademark of Integrated Device Technology, Inc.

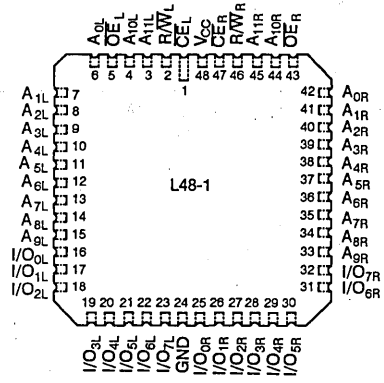
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7134S MIN.	IDT7134S MAX.	IDT7134L MIN.	IDT7134L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

5

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7134x35 [4] TYP.[2]	IDT7134x35 [4] MAX.	IDT7134x45 TYP.[2]	IDT7134x45 MAX.	IDT7134x55 TYP.[2]	IDT7134x55 MAX.	IDT7134x70 TYP.[2]	IDT7134x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[3]	MIL.	S	–	–	100	240	100	230	100	230	mA
				L	–	–	100	200	100	180	100	180	
			COM'L.	S	–	220	100	200	100	200	100	200	
				L	–	180	100	160	100	160	100	160	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	–	–	25	70	25	70	25	70	mA
				L	–	–	25	50	25	50	25	50	
			COM'L.	S	–	75	25	70	25	70	25	70	
				L	–	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	–	–	50	160	50	150	50	150	mA
				L	–	–	50	130	50	120	50	120	
			COM'L.	S	–	140	50	130	50	130	50	130	
				L	–	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V, f = 0[3]	MIL.	S	–	–	1.0	30	1.0	30	1.0	30	mA
				L	–	–	0.2	10	0.2	10	0.2	10	
			COM'L.	S	–	15	1.0	15	1.0	15	1.0	15	
				L	–	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	–	–	50	130	50	120	50	120	mA
				L	–	–	45	100	45	90	45	90	
			COM'L.	S	–	120	45	110	45	110	45	110	
				L	–	100	45	90	45	90	45	90	

NOTES:

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standy I_{SB3}.
4. 0°C to 70°C temperature range.

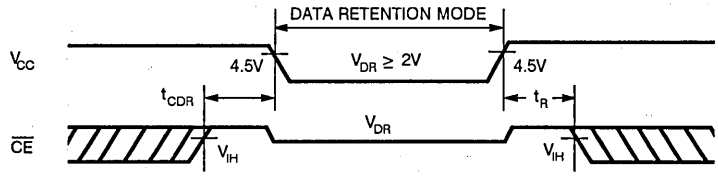
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	100	4000	µA
			COM'L.	–	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

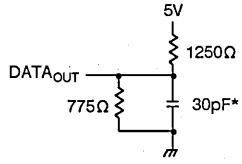


Figure 1. Output Load

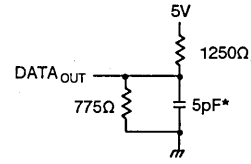


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

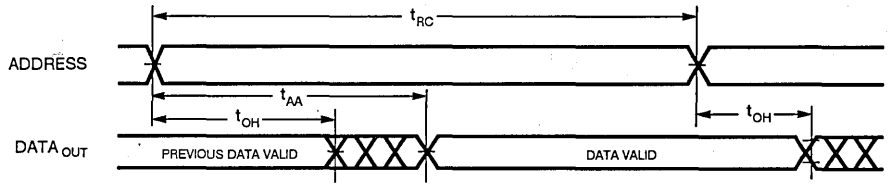
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

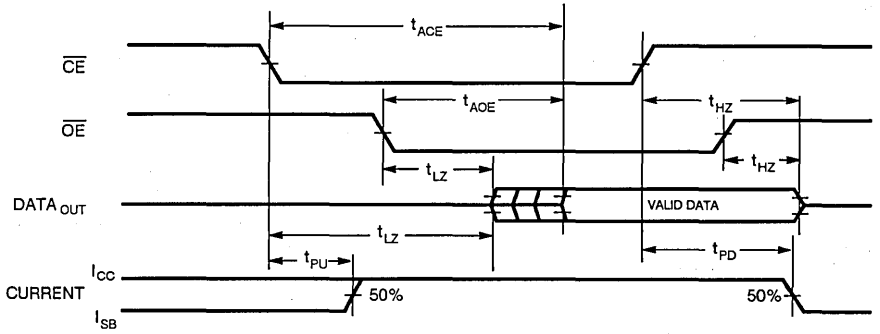
SYMBOL	PARAMETER	IDT7134S35 (3) IDT7134L35 (3) MIN.	MAX.	IDT7134S45 IDT7134L45 MIN.	MAX.	IDT7134S55 IDT7134L55 MIN.	MAX.	IDT7134S70 IDT7134L70 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time	–	35	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	20	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time(1, 2)	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time(1, 2)	–	20	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time(2)	–	50	–	50	–	50	–	50	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

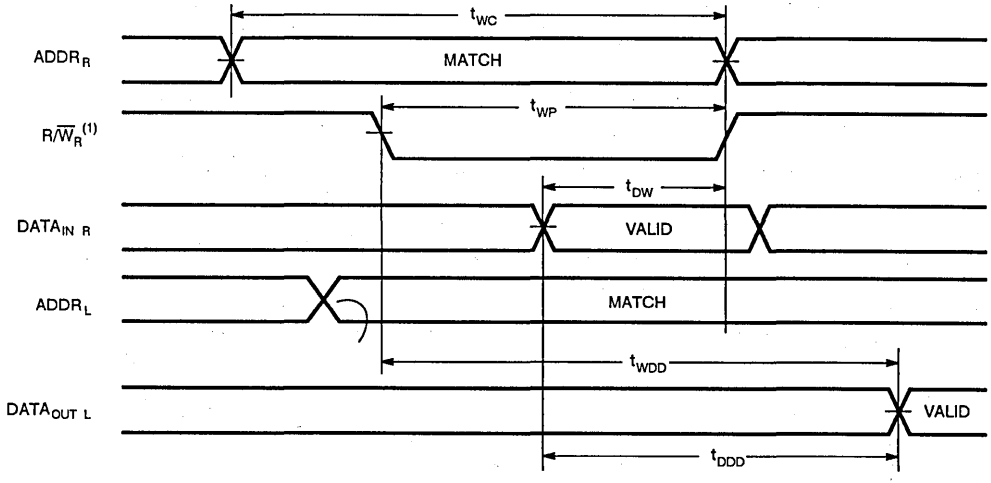
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7134S35 (5) IDT7134L35 (5)		IDT7134S45 IDT7134L45		IDT7134S55 IDT7134L55		IDT7134S70 IDT7134L70		UNIT
		MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX	
WRITE CYCLE										
t_{WC}	Write Cycle Time	35	–	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time (1,2)	–	20	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time (3)	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enabled to Output in High Z (1,2)	–	20	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write (1,2,3)	3	–	3	–	3	–	3	–	ns
t_{WDD}	Write Pulse to Data Delay (4)	–	60	–	70	–	80	–	90	ns
t_{DDD}	Write Data Valid to Read Data Delay (4)	–	35	–	45	–	55	–	70	ns

NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-Port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY"
5. 0°C to 70°C temperature range only.
6. Specified for $\overline{OE}$ at high (Refer to "TIMING WAVEFORM OF WRITE CYCLE", Note 7).

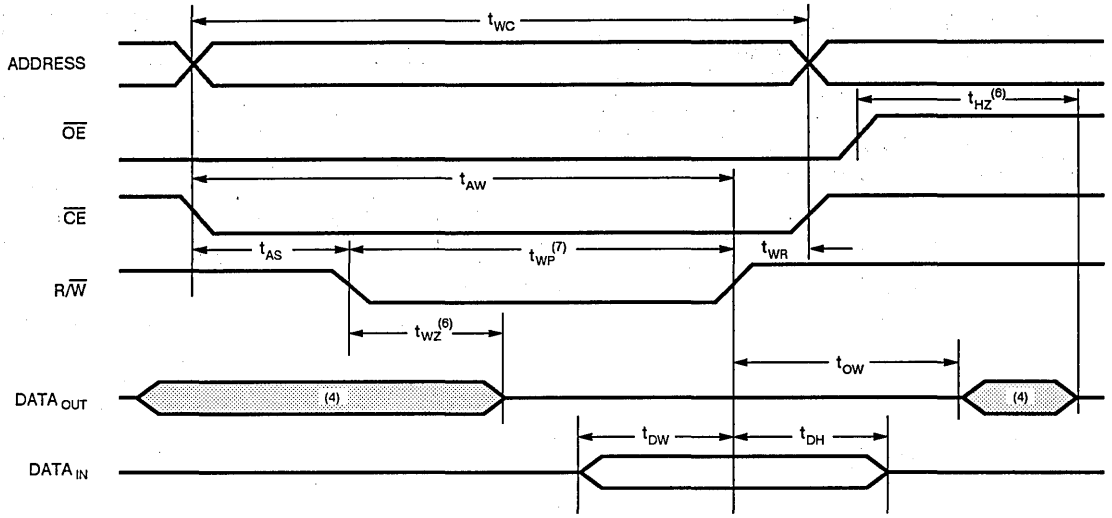
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1)



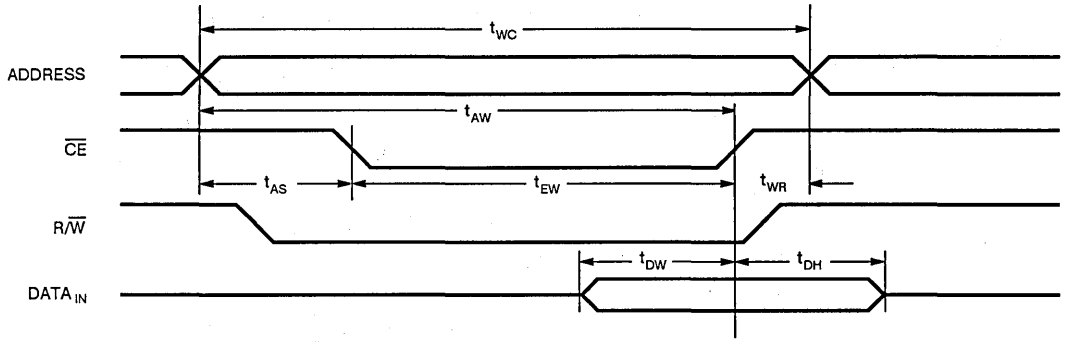
NOTE:

1. Write cycle parameters should be adhered to for ensuring proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1, 2, 3, 4, 6, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1, 2, 3, 5)



NOTES:

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

FUNCTIONAL DESCRIPTION:

The IDT7134 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

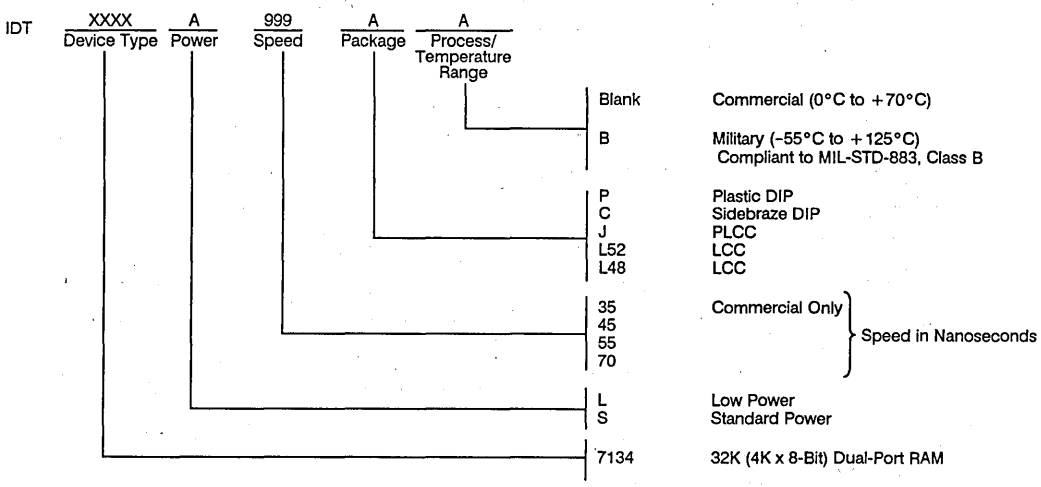
TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTE:

1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$
   H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

IDT 71342S
IDT 71342L

FEATURES:

- High-speed access
  - Military: 45/55/70ns (max.)
  - Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - IDT71342S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71342L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single +5V(±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology this device typically operates on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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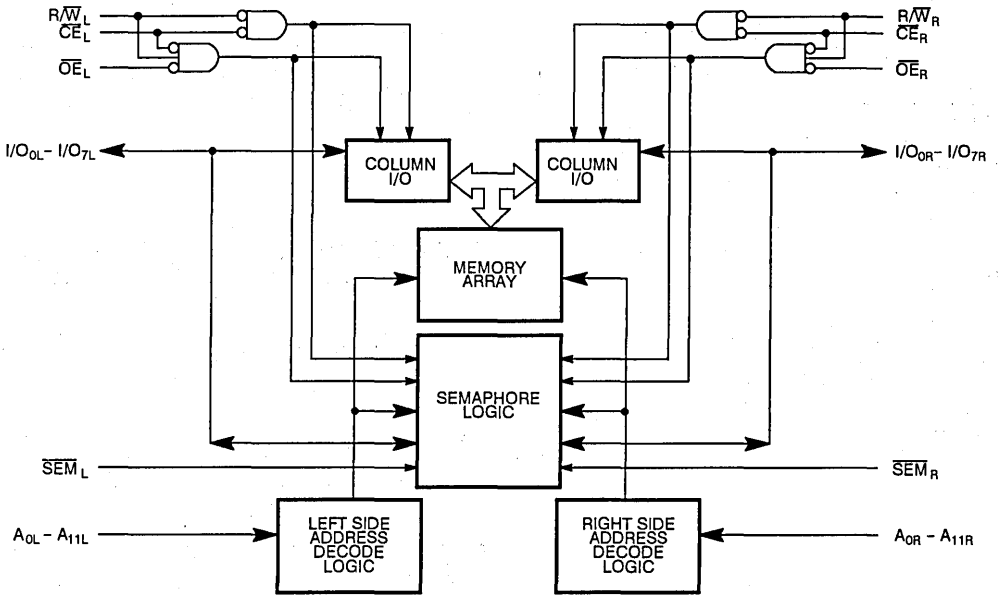
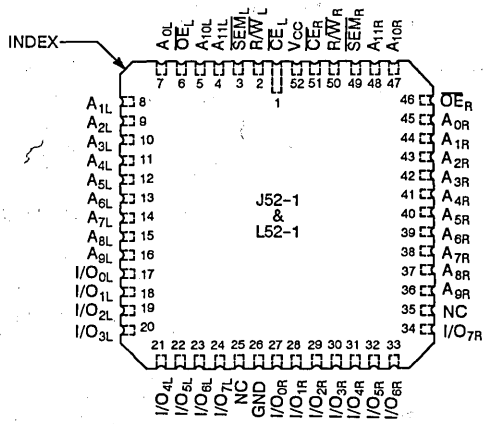
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliablity.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT71342S MIN.	IDT71342S MAX.	IDT71342L MIN.	IDT71342L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	–	0.4	–	0.4	V
		I_{OL} = 8mA	–	0.5	–	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

5

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT71342x35[4] TYP.[2]	IDT71342x35[4] MAX.	IDT71342x45 TYP.[2]	IDT71342x45 MAX.	IDT71342x55 TYP.[2]	IDT71342x55 MAX.	IDT71342x70 TYP.[2]	IDT71342x70 MAX.	UNIT
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open $\overline{SEM}$ = Don't Care f = f_{MAX}[3]	MIL.	S	–	–	100	240	100	230	100	230	mA
				L	–	–	100	200	100	180	100	180	
			COM'L.	S	100	220	100	200	100	200	100	200	
				L	100	180	100	160	100	160	100	160	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ = V_{IH} $\overline{SEM}$ = V_{IL} Outputs Open f = f_{MAX}[3]	MIL.	S	–	–	85	130	85	130	85	130	mA
				L	–	–	85	110	85	110	85	110	
			COM'L.	S	85	145	85	130	85	130	85	130	
				L	85	115	85	100	85	100	85	100	
I_{SB1}	Standby Current (Both Ports – TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R \geq V_{IH}$ $\overline{SEM}_L$ = $\overline{SEM}_R \geq V_{IH}$ f = f_{MAX}[3]	MIL.	S	–	–	25	70	25	70	25	70	mA
				L	–	–	25	50	25	50	25	50	
			COM'L.	S	25	75	25	70	25	70	25	70	
				L	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port – TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_L$ = $\overline{SEM}_R \geq V_{IH}$	MIL.	S	–	–	50	160	50	150	50	150	mA
				L	–	–	50	130	50	120	50	120	
			COM'L.	S	50	140	50	130	50	130	50	130	
				L	50	110	50	100	50	100	50	100	
I_{SB3}	Full Standby Current (Both Ports – All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V $\overline{SEM}_L$ = $\overline{SEM}_R \geq$ V_{CC} -0.2V, f = 0[3]	MIL.	S	–	–	1.0	30	1.0	30	1.0	30	mA
				L	–	–	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1.0	15	1.0	15	1.0	15	
				L	.2	4	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port – All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	–	–	50	130	50	120	50	120	mA
				L	–	–	45	100	45	90	45	90	
			COM'L.	S	45	120	45	110	45	110	45	110	
				L	45	100	45	90	45	90	45	90	

NOTES:

1. "x" in part numbers indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C
3. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby, I_{SB3}.
4. 0°C to +70°C temperature range only.

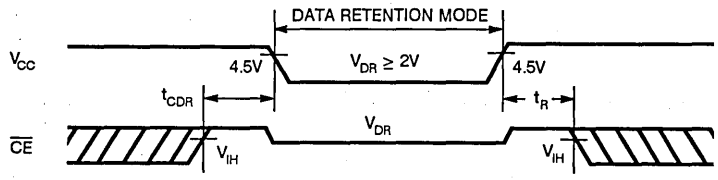
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V $\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	100	4000	µA
			COM'L.	–	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

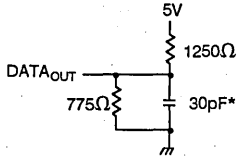


Figure 1. Output Load

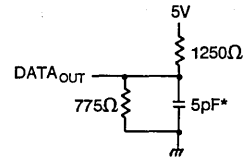


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

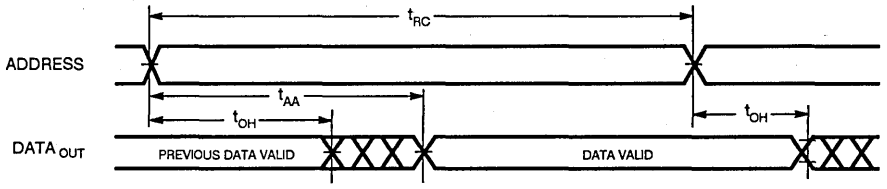
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

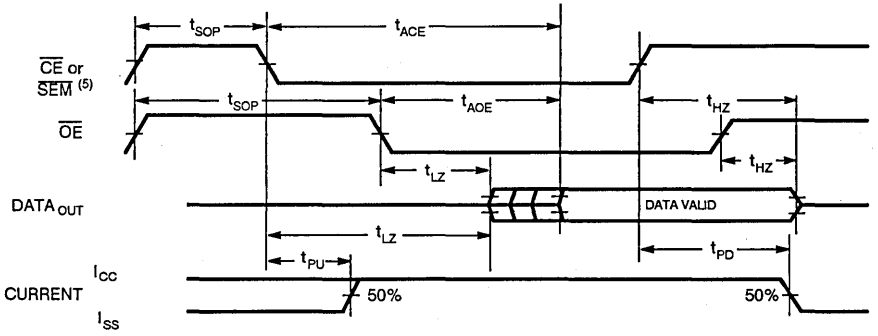
SYMBOL	PARAMETER	IDT71342S35 [5] IDT71342L35 [5] MIN.	MAX.	IDT71342S45 IDT71342L45 MIN.	MAX.	IDT71342S55 IDT71342L55 MIN.	MAX.	IDT71342S70 IDT71342L70 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	–	70	ns
t_{ACE}	Chip Enable Access Time [3]	–	35	–	45	–	55	–	70	ns
t_{AOE}	Output Enable Access Time	–	20	–	25	–	30	–	40	ns
t_{OH}	Output Hold From Address Change	5	–	5	–	5	–	5	–	ns
t_{LZ}	Output Low Z Time [1,2]	5	–	5	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1,2]	–	20	–	25	–	30	–	40	ns
t_{PU}	Chip Enable to Power Up Time [2]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [2]	–	50	–	50	–	50	–	50	ns
t_{SOP}	SEM Flag update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	–	15	–	20	–	20	–	ns
t_{WDD}	Write Pulse to Data Delay [4]	–	60	–	70	–	80	–	90	ns
t_{DDD}	Write Data Valid to Read Data Delay [4]	–	35	–	45	–	55	–	70	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.
4. Port to Port delay through RAM cells from writing port to a reading port.
5. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]

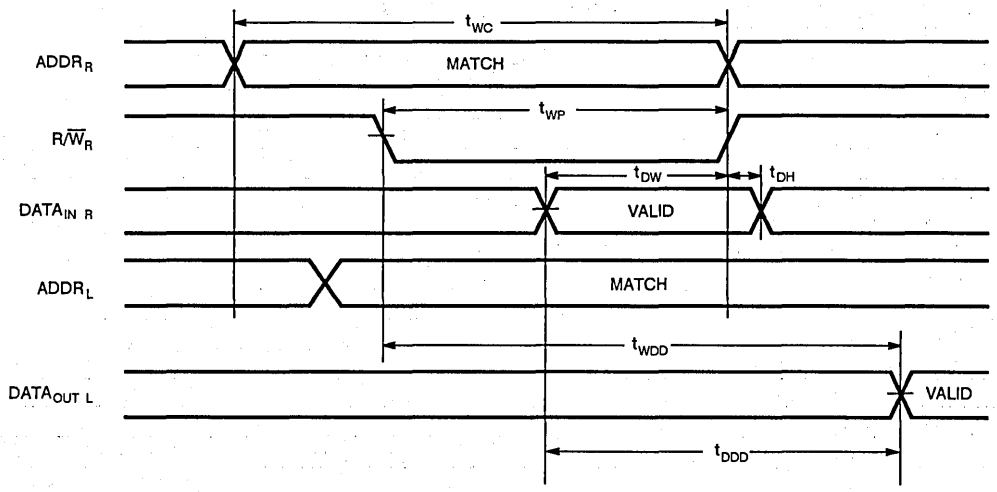


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$
5. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2)



NOTES:
1. Write Cycle parameters should be adhered to, to ensure the proper writing.
2. Device is continously enabled for both ports.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

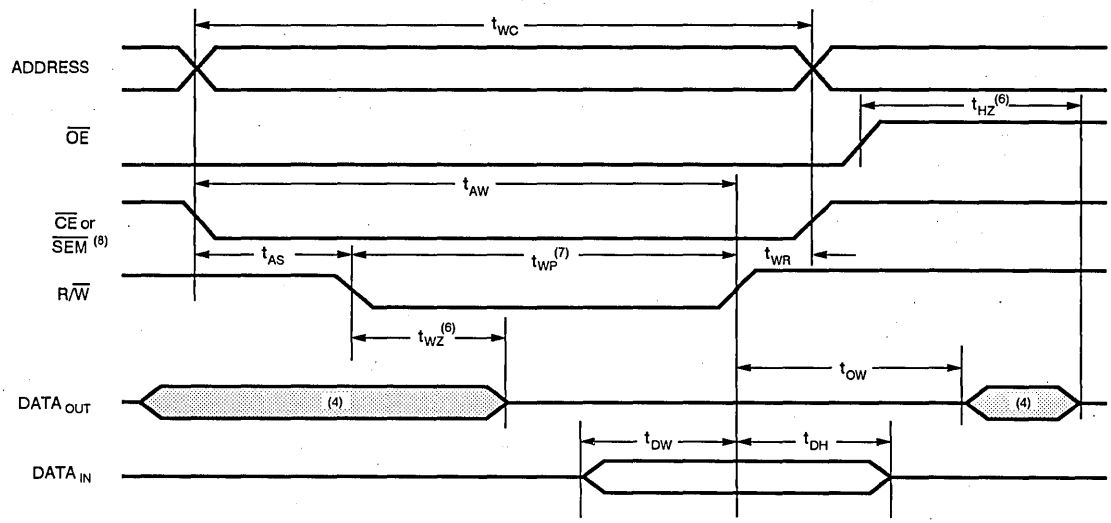
SYMBOL	PARAMETER	IDT71342S35 (5) IDT71342L35 (5) MIN.	MAX.	IDT71342S45 IDT71342L45 MIN.	MAX.	IDT71342S55 IDT71342L55 MIN.	MAX.	IDT71342S70 IDT71342L70 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	35	–	45	–	55	–	70	–	ns
t_{EW}	Chip Enable to End of Write (3)	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	20	–	20	–	25	–	30	–	ns
t_{HZ}	Output High Z Time (1,2)	–	20	–	20	–	25	–	30	ns
t_{DH}	Data Hold Time (4)	3	–	3	–	3	–	3	–	ns
t_{WZ}	Write Enable to Output in High Z (1,2)	–	20	–	20	–	25	–	30	ns
t_{OW}	Output Active From End of Write (1,2,4)	3	–	3	–	3	–	3	–	ns
t_{SWR}	SEM Flag Write to Read Time	10	–	10	–	10	–	10	–	ns
t_{SPS}	SEM Flag Contention Window	10	–	10	–	10	–	10	–	ns

NOTES:

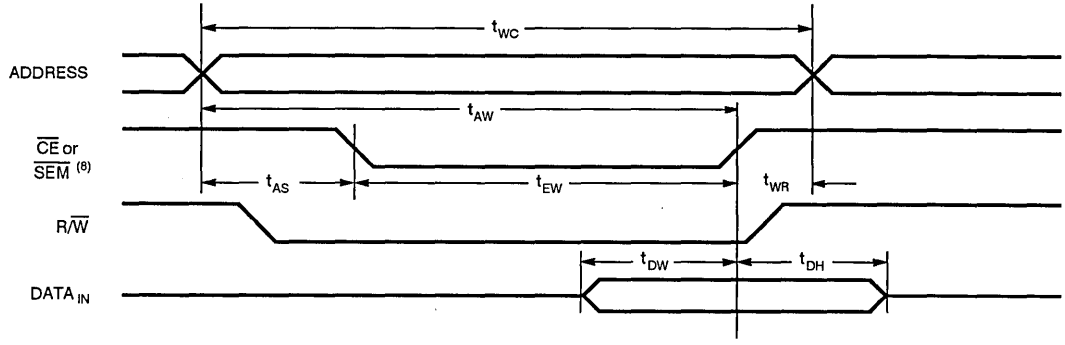
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$. This condition must be valid for entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under alll operating conditions. Although t_{DH} and t_{DH} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 0°C to +70°C temperature range only.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING [1, 2, 3, 7]



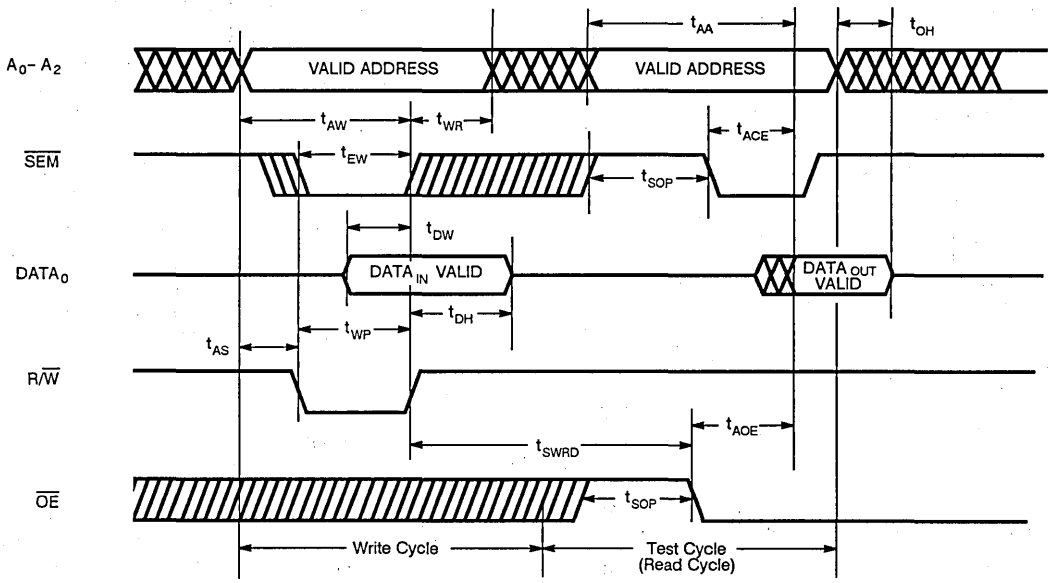
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING [1, 2, 3, 5]



NOTES:

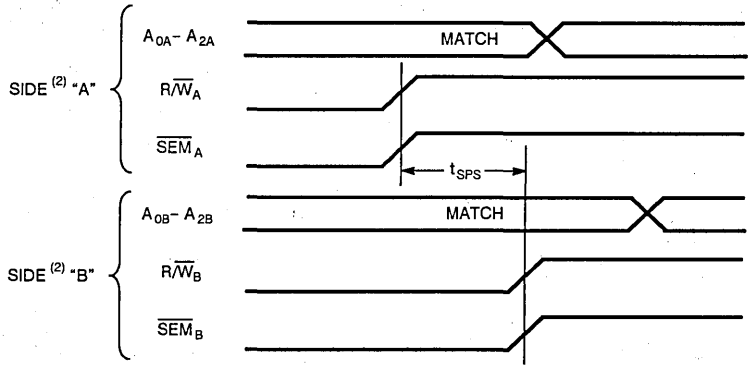
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE [1]



NOTE:
1. $\overline{CE} = V_{IH}$ for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION [1, 3, 4]



NOTES:
1. $D_{OR} = D_{OL} = V_{IL}$, $\overline{CE}_R = \overline{CE}_L = V_{IH}$, semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where R/$\overline{W}_A$ or $\overline{SEM}_A$ goes high until R/$\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast dual-port 4K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table I where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 - A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

TABLE I – NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT (1)					FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
⎍	H	L	X	$DATA_{IN}$	Port Data Bit D_0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data In Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data On Port Written Into Memory
X	L	L	X	–	Not Allowed

NOTE:

1. $A_{OL} - A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
   ⎍ = Low-to-High transition

TABLE II – EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE

FUNCTION	$D_0 - D_7$ LEFT	$D_0 - D_7$ RIGHT	STATUS
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

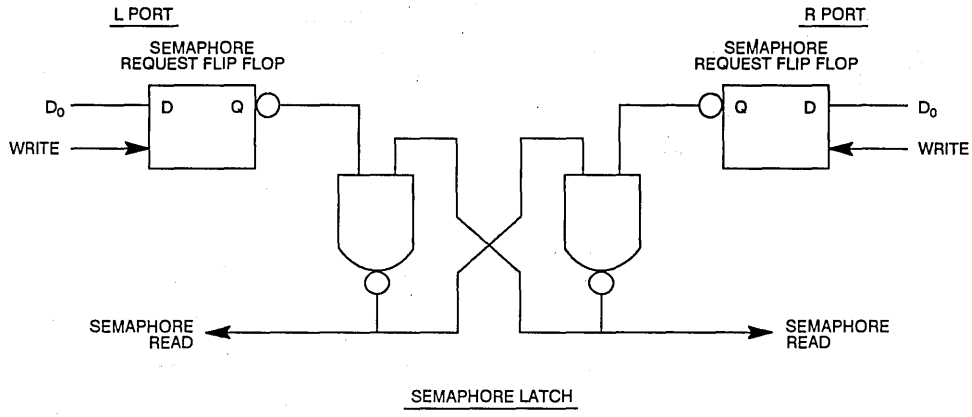
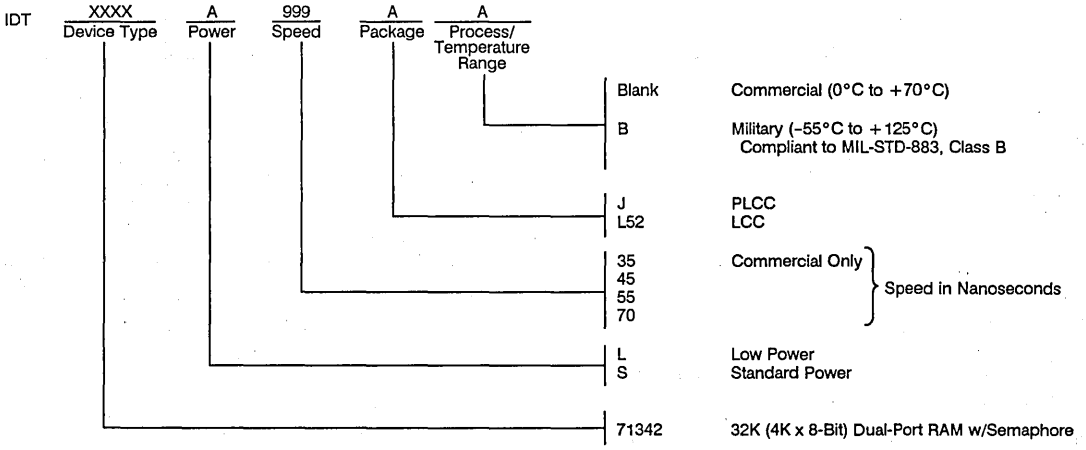


FIGURE 3. IDT71342 Semaphore Logic

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

HIGH-SPEED 4K x 16 DUAL-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7024

FEATURES:

- High-speed access
  - Military: 45/55/70/90ns (max.)
  - Commercial: 30/35/45/55/70/90ns (max.)
- Low-power operation
  - IDT7024S
    Active: ---mW (typ.)
    Standby: --mW (typ.)
  - IDT7024L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility.
- IDT7024 easily expands data bus width to 32 bits or more using the Master/Slave chip select when cascading more than one device
- On-chip port arbitration logic
- Versatile pin-select for Master or Slave:
  $M/\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  $M/\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Fully asychronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA

DESCRIPTION:

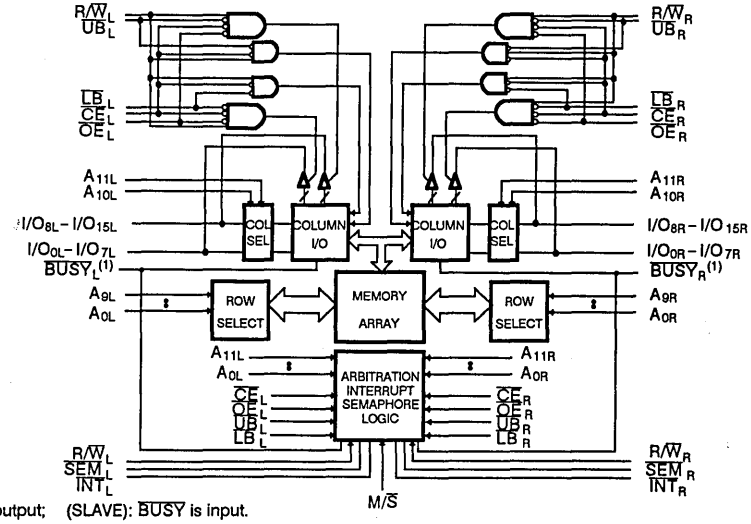
The IDT7024 is a high-speed 4K x 16 dual-port static RAM. The IDT7024 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 30ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7024 is packaged in plastic as well as ceramic 84-pin PGA and 84-pin quad flatpack. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. LB = Lower Byte. UB = Upper Byte.

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DSC-1045/-

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-11L}	A_{0R-11R}	Address
I/O_{0L-15L}	I/O_{0R-15R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Bit Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Bit Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground
$M/\overline{S}$		Master or Slave Select

	A	B	C	D	E	F	G	H	J	K	L
11	63 I/O_{7L}	61 I/O_{5L}	60 I/O_{4L}	58 I/O_{2L}	55 I/O_{0L}	54 $\overline{OE}_L$	51 $\overline{SEM}_L$	48 $\overline{LB}_L$	46 A_{11L}	45 A_{10L}	42 A_{7L}
10	66 I/O_{10L}	64 I/O_{8L}	62 I/O_{6L}	59 I/O_{3L}	56 I/O_{1L}	49 $\overline{UB}_L$	50 $\overline{CE}_L$	47 NC	44 A_{9L}	43 A_{8L}	40 A_{5L}
09	67 I/O_{11L}	65 I/O_{9L}			57 GND	53 V_{CC}	52 $R/\overline{W}_L$			41 A_{6L}	39 A_{4L}
08	69 I/O_{13L}	68 I/O_{12L}								38 A_{3L}	37 A_{2L}
07	72 I/O_{15L}	71 I/O_{14L}	73 V_{CC}						33 $\overline{BUSY}_L$	35 A_{0L}	34 $\overline{INT}_L$
06	75 I/O_{0R}	70 GND	74 GND		7024 4K x 16 DPR IN 84-PIN PGA				32 GND	31 $M/\overline{S}$	36 A_{1L}
05	76 I/O_{1R}	77 I/O_{2R}	78 V_{CC}						28 A_{0R}	29 $\overline{INT}_R$	30 $\overline{BUSY}_R$
04	79 I/O_{3R}	80 I/O_{4R}								26 A_{2R}	27 A_{1R}
03	81 I/O_{5R}	83 I/O_{7R}			7 GND	11 GND	12 $\overline{SEM}_R$			23 A_{5R}	25 A_{3R}
02	82 I/O_{6R}	1 I/O_{9R}	2 I/O_{10R}	5 I/O_{13R}	8 I/O_{15R}	10 $R/\overline{W}_R$	14 $\overline{UB}_R$	17 A_{11R}	20 A_{8R}	22 A_{6R}	24 A_{4R}
01	84 I/O_{8R}	3 I/O_{11R}	4 I/O_{12R}	6 I/O_{14R}	9 $\overline{OE}_R$	15 $\overline{LB}_R$	13 $\overline{CE}_R$	16 NC	18 A_{10R}	19 A_{9R}	21 A_{7R}

84-PIN PGA
TOP VIEW

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

INPUTS						OUTPUTS		MODE
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	$I/O_8 - I/O_{15}$	$I/O_0 - I/O_7$	
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Deselected: Power Down
L	L	X	L	H	H	$DATA_{IN}$	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Sema. Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Sema. Flag
H	↓	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
X	↓	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
L	X	X	L	X	L	–	–	Not Allowed
L	X	X	X	L	L	–	–	Not Allowed

Note:

1. $A_{0L} - A_{13R} \neq A_{0R} - A_{13R}$

Note:

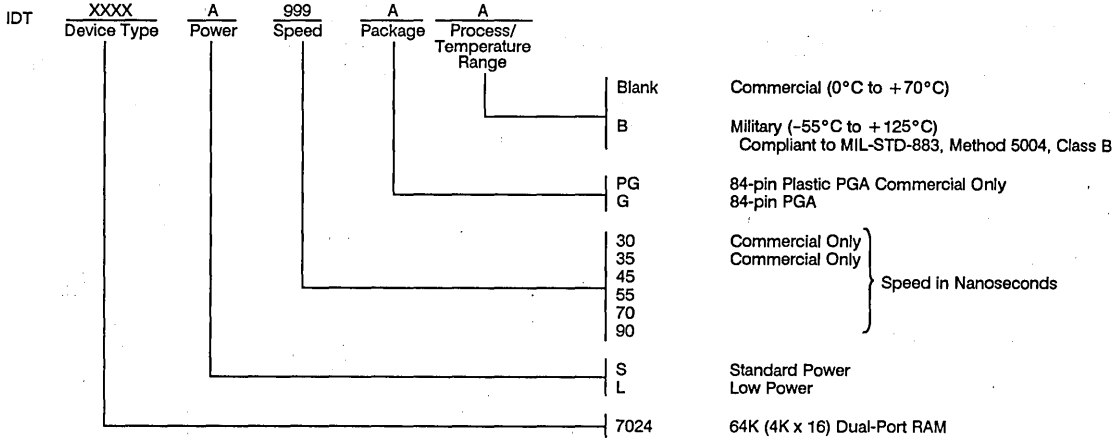
1. All V_{CC} pins have to be connected to power supply.
2. All GND pins have to be connected ground supply.

TRUTH TABLE: ARBITRATION OPTIONS

OPTIONS	INPUTS					OUTPUTS	
	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	M/$\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L L	X L	L X	H H	H H	Output Signal	–
Busy Logic Slave	L L	X L	L X	L L	H H	Input Signal	–
Interrupt Logic	L L	X L	L X	X X	H H	–	Output Signal
Semaphore Logic*	H H	X X	X X	H L	L L	H Hi-Z	–

*Inputs Signals are for Semaphore Flags set and test (Write and Read) operations

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 8K x 8 DUAL-PORT STATIC RAM

ADVANCE INFORMATION IDT 7005

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7005S
    - Active: ---mW (typ.)
    - Standby: ---mW (typ.)
  - IDT7005L
    - Active: ---mW (typ.)
    - Standby: ---mW (typ.)
- IDT7005 easily expands data bus width to 16 bits or more using the Master/Slave chip select when cascading more than one device
- On-chip port arbitration logic
- Versatile pin-select for Master or Slave
  M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Fully asychronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA

DESCRIPTION:

The IDT7005 is a high-speed 8K x 8 dual-port static RAM. The IDT7005 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7005 is packaged in plastic as well as ceramic 68-pin PGA, 68-pin PLCC, and 68-pin LCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

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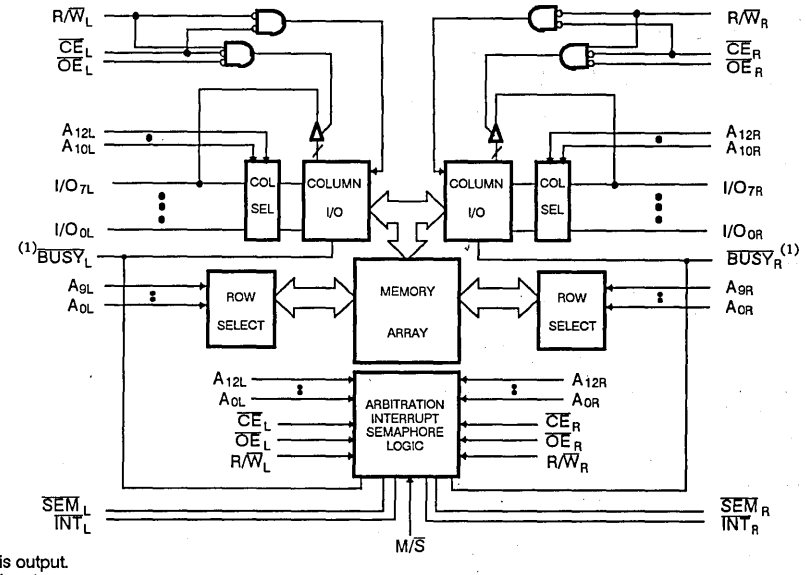
FUNCTIONAL BLOCK DIAGRAM



NOTE:

1. (MASTER): $\overline{BUSY}$ is output.
   (SLAVE): $\overline{BUSY}$ is input.

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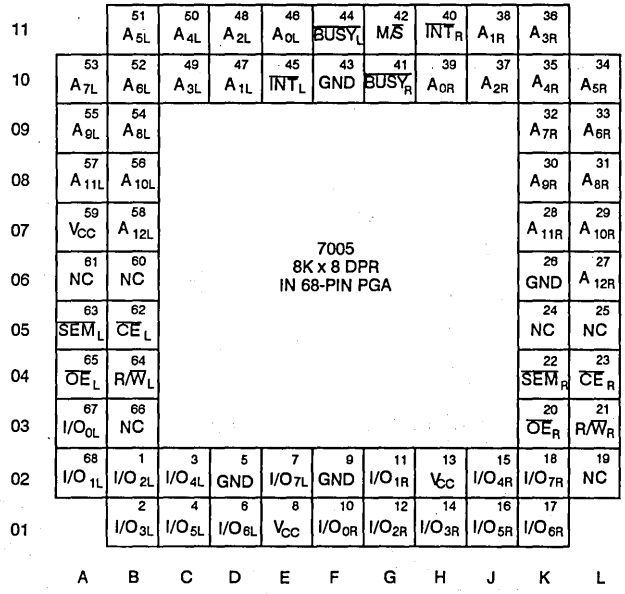
PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-12L}	A_{0R-12R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground



68-PIN PGA
TOP VIEW

Note:
1. All V_{CC} pins have to be connected to power supply.
2. All GND pins have to be connected to ground supply.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

INPUTS (1)				OUTPUTS	MODE
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	
H	X	X	H	Hi-Z	Deselected: Power Down
H	H	L	L	$DATA_{OUT}$	Read Data in Sema. Flag
X	X	H	X	Hi-Z	Outputs Disabled
H	↑	X	L	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
L	H	L	H	$DATA_{OUT}$	Read Memory
L	L	X	H	$DATA_{IN}$	Write to Memory
L	X	X	L	–	Not Allowed

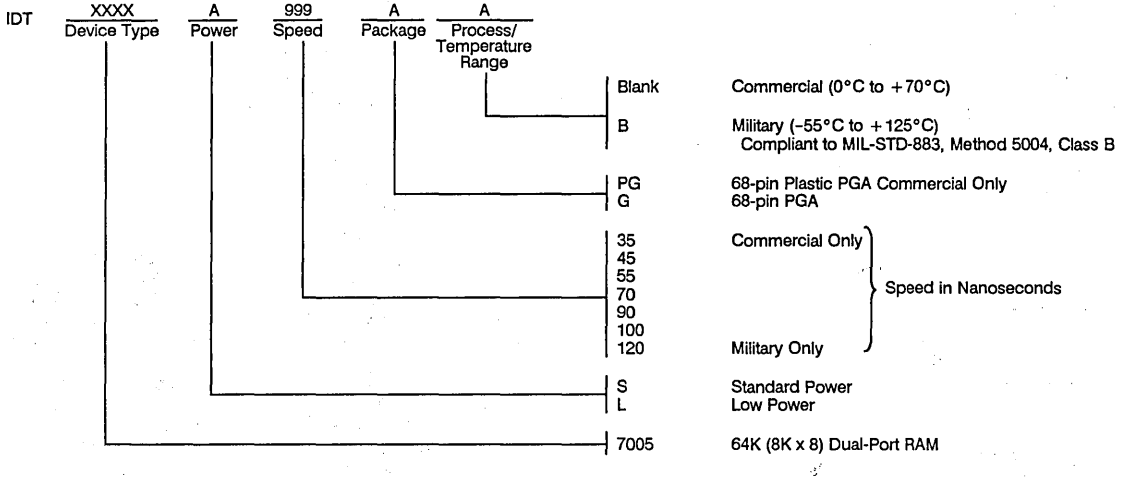
Note:
1. $A_{0L} - A_{12L} \neq A_{0R} - A_{12R}$

TRUTH TABLE: ARBITRATION OPTIONS

OPTIONS	INPUTS			OUTPUTS	
	$\overline{CE}$	$M/\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L	H	H	Output Signal	–
Busy Logic Slave	L	L	H	Input Signal	–
Interrupt Logic	L	X	H	–	Output Signal
Semaphore Logic*	H	H	L	H	–
	H	L	L	Hi-Z	–

*Inputs Signals are for Semaphore Flags set and test (Write and Read) operations

ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7025

FEATURES:

- High-speed access
  - Military: 45/55/70/90ns (max.)
  - Commercial: 30/35/45/55/70/90ns (max.)
- Low-power operation
  - IDT7025S
    Active: ---mW (typ.)
    Standby: --mW (typ.)
  - IDT7025L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave chip select when cascading more than one device
- On-chip port arbitration logic
- Versatile Pin-Select for Master or Slave:
  M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Fully asychronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA

DESCRIPTION:

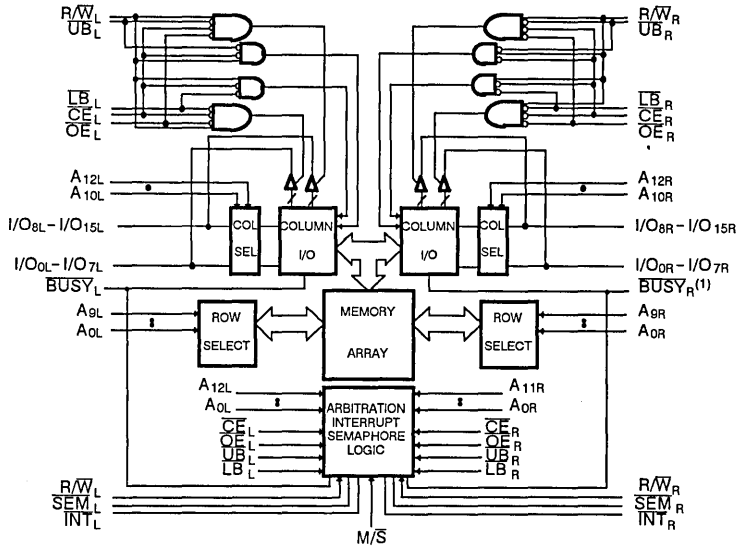
The IDT7025 is a high-speed 8K x 16 dual-port static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 30ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7025 is packaged in plastic as well as ceramic 84-pin PGA and 84-pin quad flatpack. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. (MASTER): $\overline{BUSY}$ is output, (SLAVE): $\overline{BUSY}$ is input.
2. LB = Lower Byte. UB = Upper Byte.

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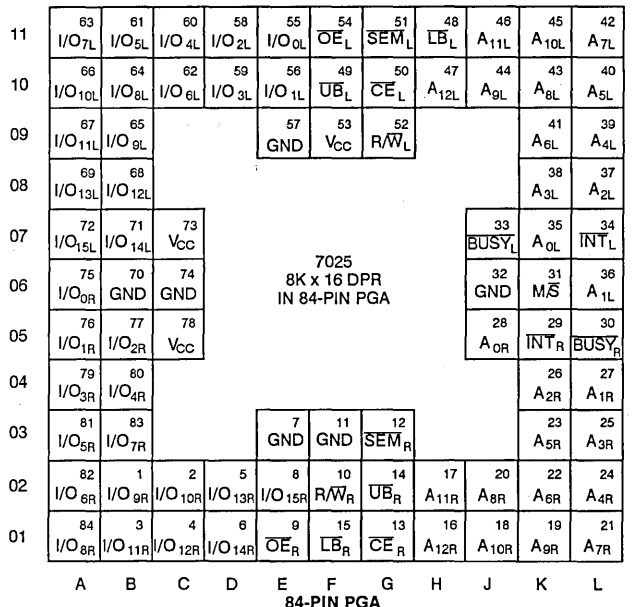
DSC-1046/-

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-12L}	A_{0R-12R}	Address
I/O_{0L-15L}	I/O_{0R-15R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Bit Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Bit Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground



84-PIN PGA
TOP VIEW

Note:
1. All V_{CC} pins have to be connected to power supply.
2. All GND pins have to be connected to ground supply.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

INPUTS (1)						OUTPUTS		MODE
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	$I/O_8 - I/O_{15}$	$I/O_0 - I/O_7$	
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Deselected: Power Down
L	L	X	L	H	H	$DATA_{IN}$	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Sema. Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Sema. Flag
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
L	X	X	L	X	L	–	–	Not Allowed
L	X	X	X	L	L	–	–	Not Allowed

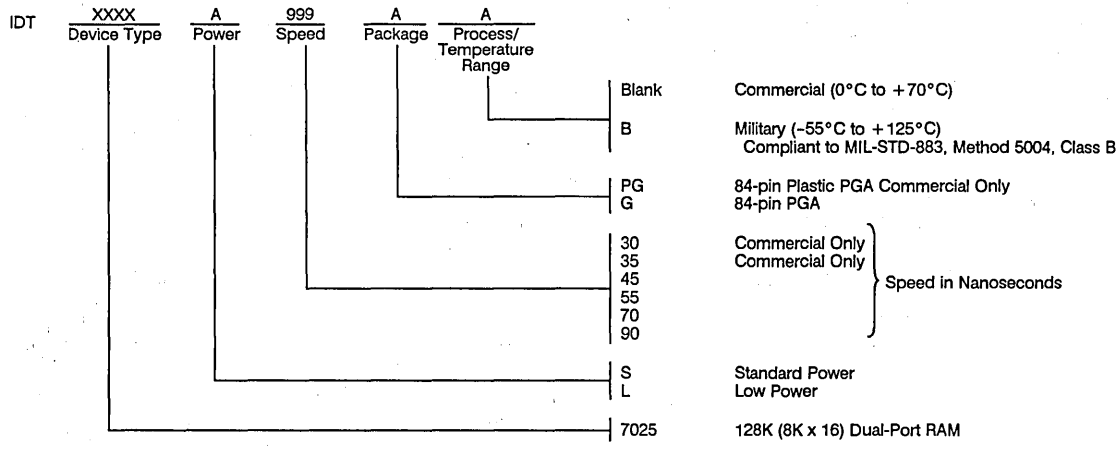
Note:
1. $A_{0L} - A_{12L} \neq A_{0R} - A_{12R}$

TRUTH TABLE: ARBITRATION OPTIONS

OPTIONS	INPUTS					OUTPUTS	
	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$M/\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L L	X L	L X	H H	H H	Output Signal	–
Busy Logic Slave	L L	X L	L X	L L	H H	Input Signal	–
Interrupt Logic	L L	X L	L X	X X	H H	–	Output Signal
Semaphore Logic*	H H	X X	X X	H L	L L	H Hi-Z	–

*Inputs Signals are for Semaphore Flags set and test (Write and Read) operations

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7006

FEATURES:

- High-speed access
  - Military: 45/55/70/90/100/120ns (max.)
  - Commercial: 35/45/55/70/90/100ns (max.)
- Low-power operation
  - IDT7006S
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
  - IDT7006L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave chip select when cascading more than one device
- On-chip port arbitration logic
- Versatile pin-select for Master or Slave:
  M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Fully asychronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA

DESCRIPTION:

The IDT7006 is a high-speed 16K x 8 dual-port static RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7006 is packaged in plastic as well as ceramic 68-pin PGA, 68-pin LCC, and 68-pin PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

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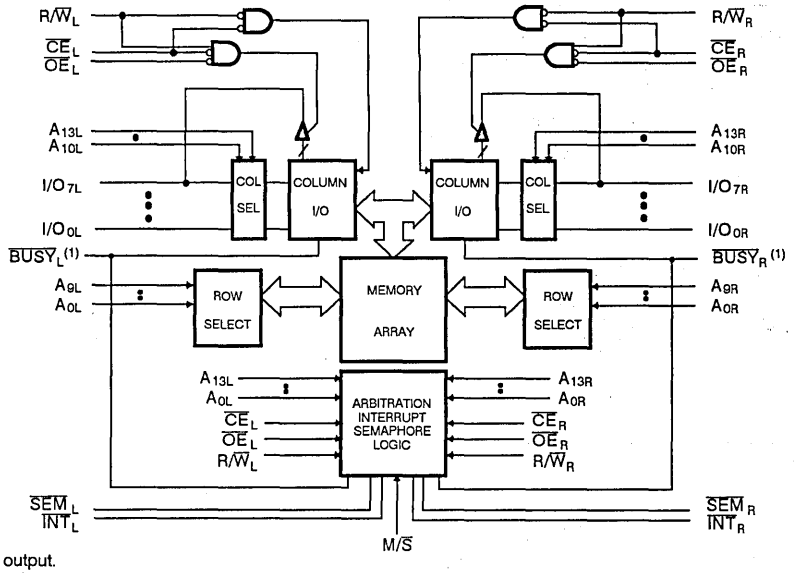
FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. (MASTER): $\overline{BUSY}$ is output.
   (SLAVE): $\overline{BUSY}$ is input.

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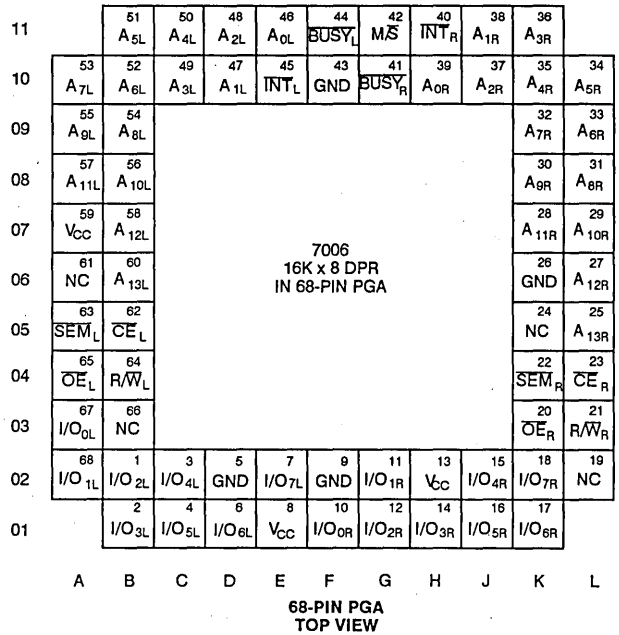
DSC-1044/-

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-13L}	A_{0R-13R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground
$M/\overline{S}$		Master or Slave Select



68-PIN PGA
TOP VIEW

Note:
1. All V_{CC} pins have to be connected to power supply.
2. All GND pins have to be connected to ground supply.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

INPUTS (1)				OUTPUTS	MODE
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	
H	X	X	H	Hi-Z	Deselected: Power Down
H	H	L	L	$DATA_{OUT}$	Read Data in Sema. Flag
X	X	H	X	Hi-Z	Outputs Disabled
H	⎍	X	L	$DATA_{IN}$	Write D_{IN0} into Sema. Flag
L	H	L	H	$DATA_{OUT}$	Read Memory
L	L	X	H	$DATA_{IN}$	Write to Memory
L	X	X	L	–	Not Allowed

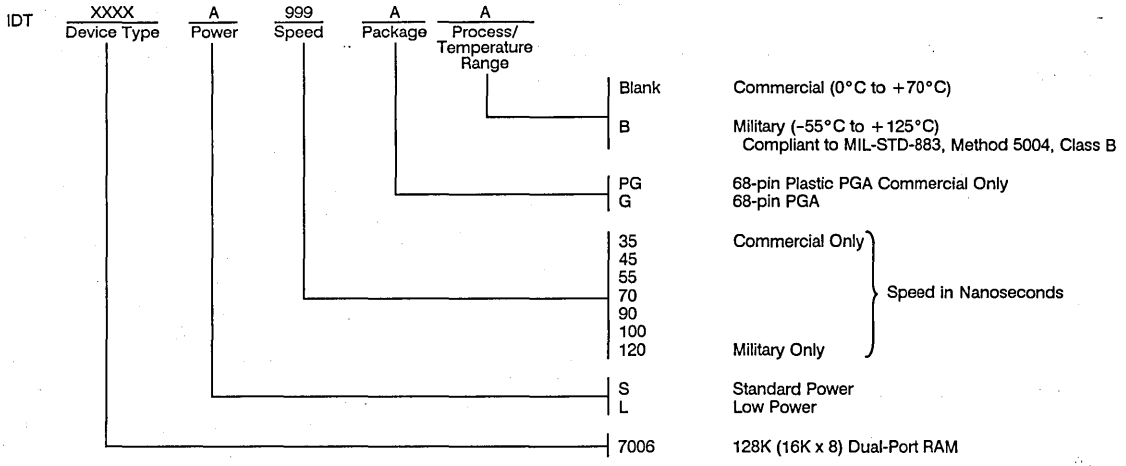
Note:
1. $A_{0L} - A_{13R} \neq A_{0R} - A_{13R}$

TRUTH TABLE: ARBITRATION OPTIONS

OPTIONS	INPUTS			OUTPUTS	
	$\overline{CE}$	$M/\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L	H	H	Output Signal	–
Busy Logic Slave	L	L	H	Input Signal	–
Interrupt Logic	L	X	H	–	Output Signal
Semaphore Logic*	H H	H L	L L	H Hi-Z	–

*Inputs Signals are for Semaphore Flags set and test (Write and Read) operations

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

HIGH-SPEED 1K x 8 FOUR-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7050S
IDT 7050L

FEATURES:

- High-speed access
  - Military: 30/35/45ns (max.)
  - Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - IDT7050S
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
  - IDT7050L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7050 is a high-speed 1K x 8 four-port static RAM designed to be used in systems where multiple access in a common RAM is required. This four-port static RAM offers increased system performance in multiprocessed systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

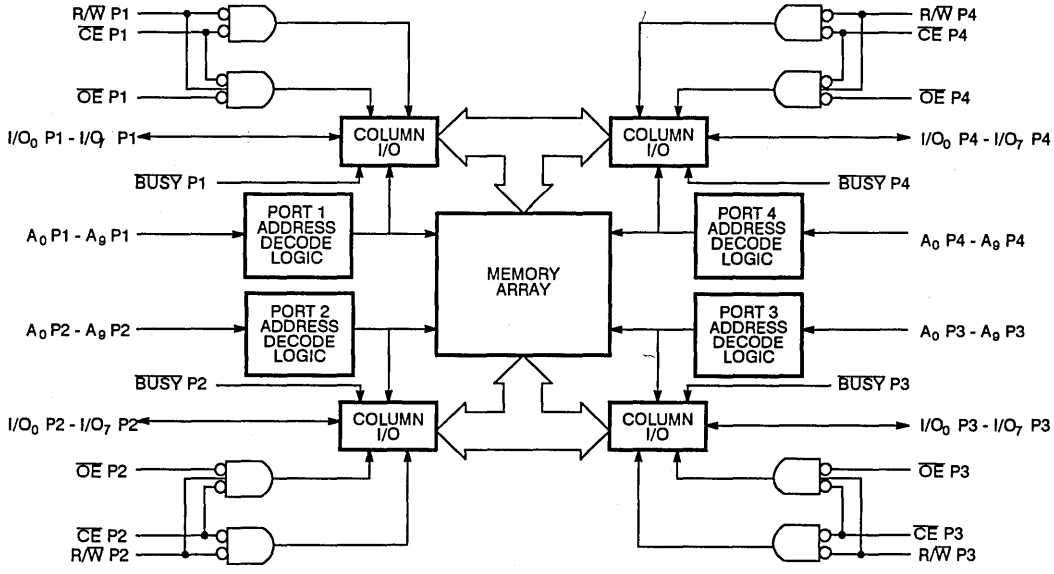
The IDT7050 is also an extremely high-speed 1K x 8 four-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same four-port RAM location.

The IDT7050 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these four ports typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming ---μW from a 2V battery.

The IDT7050 is packaged in either a ceramic or plastic 108-pin PGA and 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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DSC-1068/-

PIN CONFIGURATIONS

SYMBOL	PIN NAME
A0 P1 – A9 P1	Address Lines – Port 1
A0 P2 – A9 P2	Address Lines – Port 2
A0 P3 – A9 P3	Address Lines – Port 3
A0 P4 – A9 P4	Address Lines – Port 4
I/O0 P1 – I/O7 P1	Data I/O – Port 1
I/O0 P2 – I/O7 P2	Data I/O – Port 2
I/O0 P3 – I/O7 P3	Data I/O – Port 3
I/O0 P4 – I/O7 P4	Data I/O – Port 4
R/$\overline{W}$ P1	Read/Write – Port 1
R/$\overline{W}$ P2	Read/Write – Port 2
R/$\overline{W}$ P3	Read/Write – Port 3
R/$\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
V_{CC}	Power
GND	Ground

A	B	C	D	E	F	G	H	J	K	L	M	
81 R/$\overline{W}$ P2	80 NC	77 A7 P2	74 A5 P2	72 A3 P2	69 A0 P2	68 A0 P3	65 A3 P3	63 A5 P3	60 A7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A8 P2	76 NC	73 A4 P2	70 A1 P2	67 A1 P3	64 A4 P3	61 NC	59 A8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A2 P1	86 A1 P1	82 $\overline{CE}$ P2	79 A9 P2	75 A6 P2	71 A2 P2	66 A2 P3	62 A6 P3	58 A9 P3	55 $\overline{CE}$ P3	51 A1 P4	50 A2 P4	10
90 A5 P1	88 A3 P1	85 A0 P1							52 A0 P4	49 A3 P4	47 A5 P4	09
92 NC	91 A6 P1	89 A4 P1							48 A4 P4	46 A6 P4	45 NC	08
95 A8 P1	94 A7 P1	93 V_{CC}			IDT7050 108 Pin PGA				44 GND	43 A7 P4	42 A8 P4	07
96 A9 P1	97 NC	98 $\overline{CE}$ P1			TOP VIEW				39 $\overline{CE}$ P4	40 NC	41 A9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O0 P1							35 V_{SS}	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O1 P1	106 GND							31 GND	34 I/O7 P4	36 $\overline{BUSY}$ P4	04
104 I/O2 P1	105 I/O3 P1	1 I/O6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O2 P4	32 I/O5 P4	33 I/O6 P4	03
107 I/O4 P1	2 I/O7 P1	5 I/O0 P2	7 I/O2 P2	10 I/O4 P2	13 I/O6 P2	16 I/O1 P3	19 I/O3 P3	22 I/O5 P3	24 I/O7 P3	29 I/O3 P4	30 I/O4 P4	02
108 I/O5 P1	3 NC	6 I/O1 P2	9 I/O3 P2	11 I/O5 P2	14 I/O7 P2	15 I/O0 P3	18 I/O2 P3	20 I/O4 P3	23 I/O6 P3	26 I/O0 P4	27 I/O1 P4	01

NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7050S MIN.	IDT7050S MAX.	IDT7050L MIN.	IDT7050L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1,2] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7050x25[3] TYP.	IDT7050x25[3] MAX.	IDT7050x30 TYP.	IDT7050x30 MAX.	IDT7050x35 TYP.	IDT7050x35 MAX.	IDT7050x45 TYP.	IDT7050x45 MAX.	UNIT
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = 0[4]	MIL.	S	–	–	–	360	–	360	–	360	mA
				L	–	–	–	300	–	300	–	300	
			COM'L.	S	–	300	–	300	–	300	–	300	
				L	–	250	–	250	–	250	–	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[5]	MIL.	S	–	–	–	400	–	395	–	390	mA
				L	–	–	–	335	–	330	–	325	
			COM'L.	S	–	350	–	340	–	335	–	330	
				L	–	295	–	285	–	280	–	275	
I_{SB}	Standby Current (All Ports – TTL Level Inputs)	$\overline{CE}$ ≥ V_{IH} f = f_{MAX}[5]	MIL.	S	–	–	–	115	–	110	–	105	mA
				L	–	–	–	85	–	80	–	75	
			COM'L.	S	–	85	–	80	–	75	–	70	
				L	–	70	–	65	–	60	–	55	
I_{SB1}	Full Standby Current (Both Ports – All CMOS Level Inputs)	All Ports $\overline{CE}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[4]	MIL.	S	–	–	–	15	–	15	–	15	mA
				L	–	–	–	4.5	–	4.5	–	4.5	
			COM'L.	S	–	5	–	5	–	5	–	5	
				L	–	1.5	–	1.5	–	1.5	–	1.5	

NOTES:

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for TYP.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

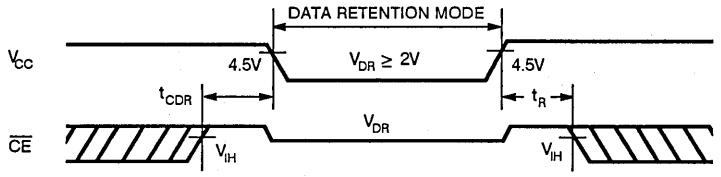
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	–	1800	µA
			COM'L.	–	–	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

5

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

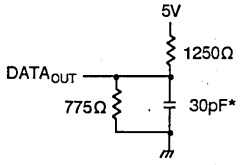


Figure 1. Output Load

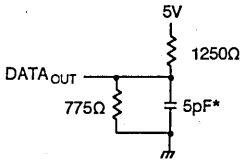


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

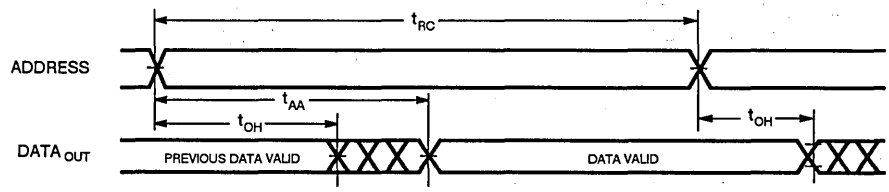
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

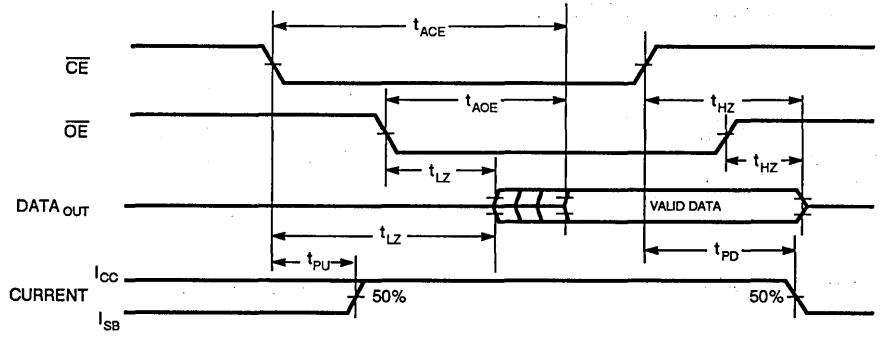
SYMBOL	PARAMETER	IDT7050S25 [1,3] IDT7050L25 [1,3] MIN.	MAX.	IDT7050S30 IDT7050L30 MIN.	MAX.	IDT7050S35 IDT7050L35 MIN.	MAX.	IDT7050S45 IDT7050L45 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	ns
t_{ACE}	Chip Enable Access Time	–	25	–	30	–	35	–	45	ns
t_{AOE}	Output Enable Access Time	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time [1,2]	3	–	3	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1,2]	–	15	–	15	–	15	–	20	ns
t_{PU}	Chip Enable to Power Up Time [2]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [2]	–	20	–	30	–	50	–	50	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1,2,4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1,3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

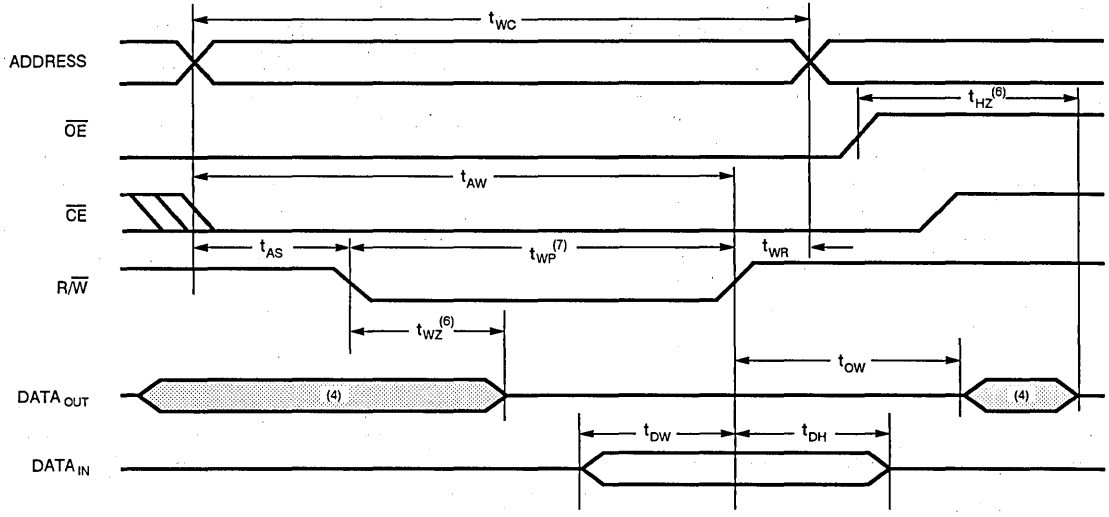
SYMBOL	PARAMETER	IDT7050S25[7] IDT7050L25[7] MIN.	MAX.	IDT7050S30 IDT7050L30 MIN.	MAX.	IDT7050S35 IDT7050L35 MIN.	MAX.	IDT7050S45 IDT7050L45 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	ns
t_{EW}	Chip Enable to End of Write	20	–	25	–	30	–	35	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[3]	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	20	–	ns
t_{HZ}	Output High Z Time[1,2]	–	15	–	15	–	15	–	20	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1,2]	–	15	–	15	–	15	–	20	ns
t_{OW}	Output Active From End of Write[1,2]	0	–	0	–	0	–	0	–	ns
t_{WDD}	Write Pulse to Data Delay[4]	–	40	–	50	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	–	30	–	35	–	40	–	45	ns
BUSY INPUT TIMING										
t_{WB}	Write to $\overline{Busy}$[5]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{Busy}$[6]	15	–	20	–	20	–	20	–	ns

NOTES:

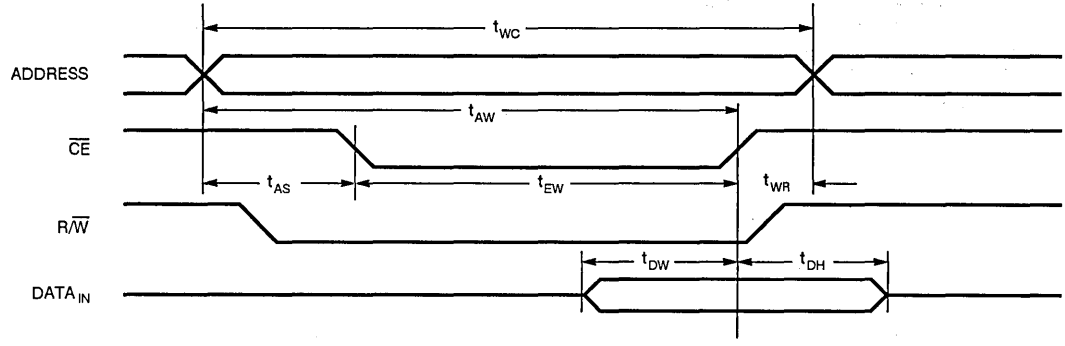
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING [1, 2, 3, 7]



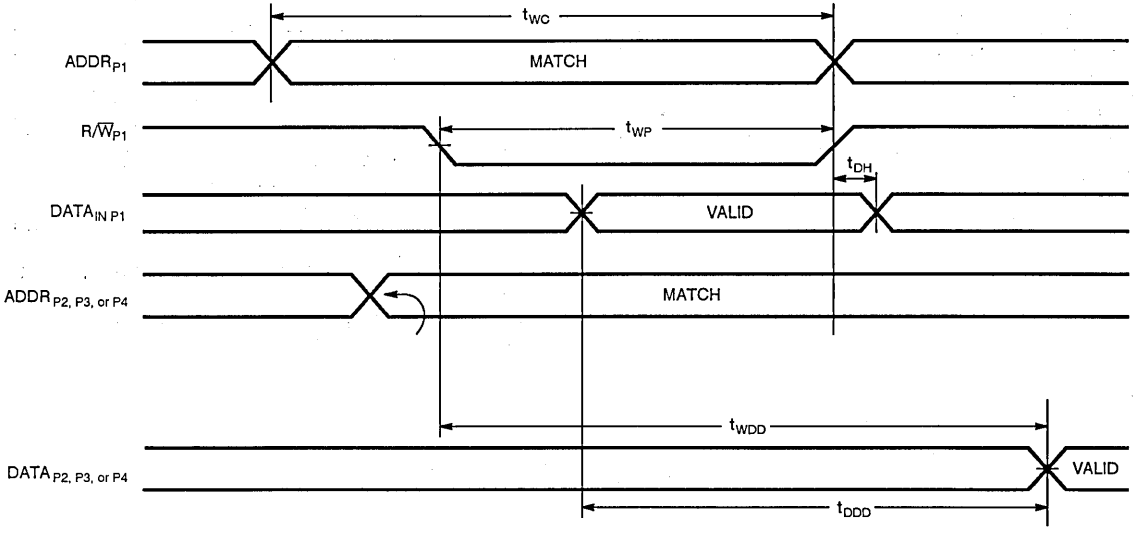
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING [1, 2, 3, 5]



NOTES:

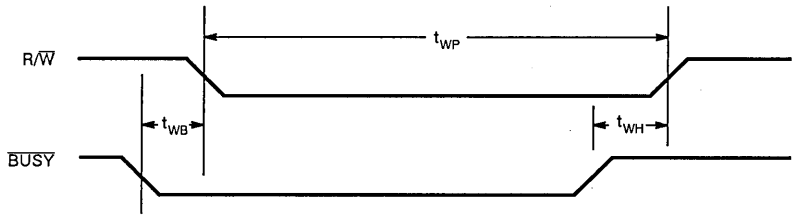
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2, 3)



NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



FUNCTIONAL DESCRIPTION:

The IDT7050 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I—READ/WRITE CONTROL

ANY PORT (1)				FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$, = H Power Down Mode, I_{SB1} or I_{SB}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2,3)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES:

1. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 8 FOUR-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7052S
IDT 7052L

FEATURES:

- High-speed access
  - Military: 30/35/45ns (max.)
  - Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - IDT7052S
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
  - IDT7052L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface-mount
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7052 is a high-speed 2K x 8 four-port static RAM designed to be used in systems where multiple access to a common RAM is required. This four-port static RAM offers increased system performance in multiprocessed systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

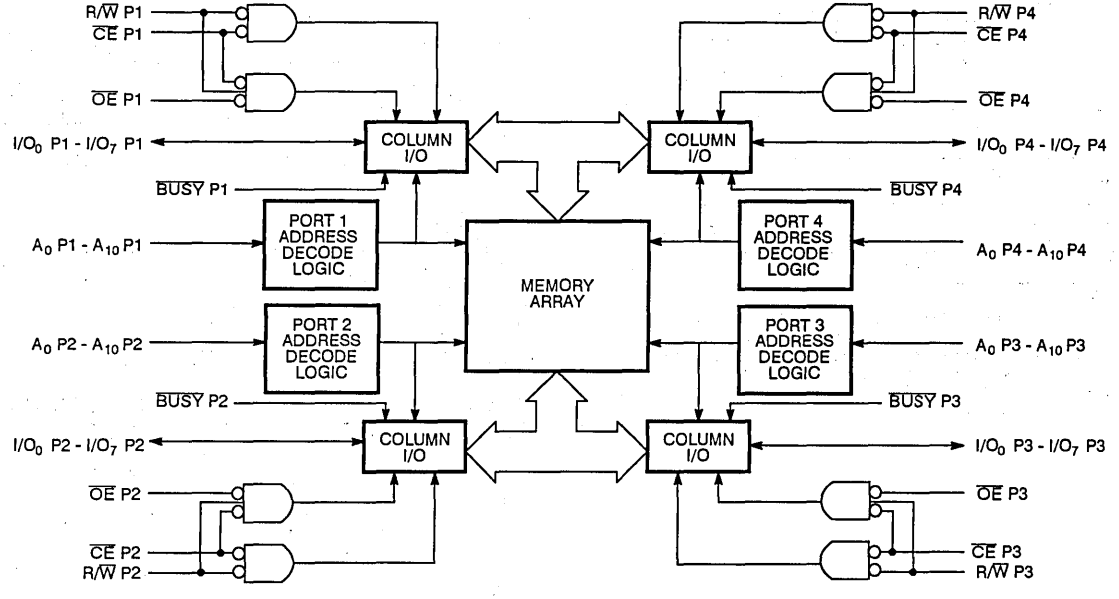
The IDT7052 is also an extremely high-speed 2K x 8 four-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same four-port RAM location.

The IDT7052 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming ---µW from a 2V battery.

The IDT7052 is packaged in either a ceramic or plastic 108-pin PGA and 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

SYMBOL	PIN NAME
A0 P1 – A10 P1	Address Lines – Port 1
A0 P2 – A10 P2	Address Lines – Port 2
A0 P3 – A10 P3	Address Lines – Port 3
A0 P4 – A10 P4	Address Lines – Port 4
I/O0 P1 – I/O7 P1	Data I/O – Port 1
I/O0 P2 – I/O7 P2	Data I/O – Port 2
I/O0 P3 – I/O7 P3	Data I/O – Port 3
I/O0 P4 – I/O7 P4	Data I/O – Port 4
R/$\overline{W}$ P1	Read/Write – Port 1
R/$\overline{W}$ P2	Read/Write – Port 2
R/$\overline{W}$ P3	Read/Write – Port 3
R/$\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
V_{CC}	Power
GND	Ground

A	B	C	D	E	F	G	H	J	K	L	M	
81 R/$\overline{W}$ P2	80 NC	77 A7 P2	74 A5 P2	72 A3 P2	69 A0 P2	68 A0 P3	65 A3 P3	63 A5 P3	60 A7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A8 P2	76 A10 P2	73 A4 P2	70 A1 P2	67 A1 P3	64 A4 P3	61 A10 P3	59 A8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A2 P1	86 A1 P1	82 $\overline{CE}$ P2	79 A9 P2	75 A6 P2	71 A2 P2	66 A2 P3	62 A6 P3	58 A9 P3	55 $\overline{CE}$ P3	51 A1 P4	50 A2 P4	10
90 A5 P1	88 A3 P1	85 A0 P1							52 A0 P4	49 A3 P4	47 A5 P4	09
92 A10 P1	91 A6 P1	89 A4 P1							48 A4 P4	46 A6 P4	45 A10 P4	08
95 A8 P1	94 A7 P1	93 V_{CC}							44 GND	43 A7 P4	42 A8 P4	07
96 A9 P1	97 NC	98 $\overline{CE}$ P1							39 $\overline{CE}$ P4	40 NC	41 A9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O1 P1	106 GND							31 GND	34 I/O7 P4	36 $\overline{BUSY}$ P4	04
104 I/O2 P1	105 I/O3 P1	1 I/O6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O2 P4	32 I/O5 P4	33 I/O6 P4	03
107 I/O4 P1	2 I/O7 P1	5 I/O0 P2	7 I/O2 P2	10 I/O4 P2	13 I/O6 P2	16 I/O1 P3	19 I/O3 P3	22 I/O5 P3	24 I/O7 P3	29 I/O3 P4	30 I/O4 P4	02
108 I/O5 P1	3 NC	6 I/O1 P2	9 I/O3 P2	11 I/O5 P2	14 I/O7 P2	15 I/O0 P3	18 I/O2 P3	20 I/O4 P3	23 I/O6 P3	26 I/O0 P4	27 I/O1 P4	01

IDT7052
108-Pin PGA
TOP VIEW

NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no-connect pin.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7052S MIN.	IDT7052S MAX.	IDT7052L MIN.	IDT7052L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

5

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,2] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7052x25[3] TYP.	IDT7052x25[3] MAX.	IDT7052x30 TYP.	IDT7052x30 MAX.	IDT7052x35 TYP.	IDT7052x35 MAX.	IDT7052x45 TYP.	IDT7052x45 MAX.	UNIT
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = 0[4]	MIL.	S	–	–	–	360	–	360	–	360	mA
				L	–	–	–	300	–	300	–	300	
			COM'L.	S	–	300	–	300	–	300	–	300	
				L	–	250	–	250	–	250	–	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[5]	MIL.	S	–	–	–	400	–	395	–	390	mA
				L	–	–	–	335	–	330	–	325	
			COM'L.	S	–	350	–	340	–	335	–	330	
				L	–	295	–	285	–	280	–	275	
I_{SB}	Standby Current (All Ports – TTL Level Inputs)	$\overline{CE}$ ≥ V_{IH} f = f_{MAX}[5]	MIL.	S	–	–	–	115	–	110	–	105	mA
				L	–	–	–	85	–	80	–	75	
			COM'L.	S	–	85	–	80	–	75	–	70	
				L	–	70	–	65	–	60	–	55	
I_{SB1}	Full Standby Current (All Ports – All CMOS Level Inputs)	All Ports $\overline{CE}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[4]	MIL.	S	–	–	–	15	–	15	–	15	mA
				L	–	–	–	4.5	–	4.5	–	4.5	
			COM'L.	S	–	5	–	5	–	5	–	5	
				L	–	1.5	–	1.5	–	1.5	–	1.5	

NOTES:

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for TYP.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
6. For the case of one port, just divide the above appropriate current by four.

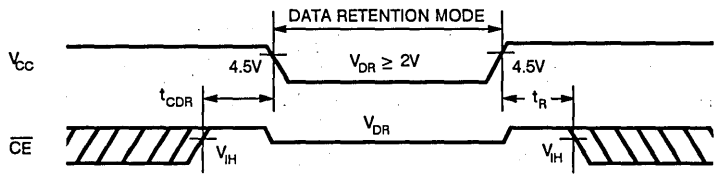
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	–	1800	µA
			COM'L.	–	–	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

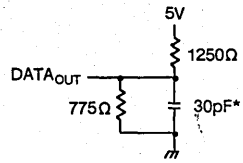


Figure 1. Output Load

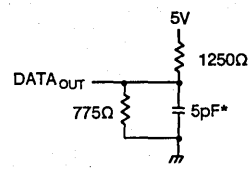


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig.

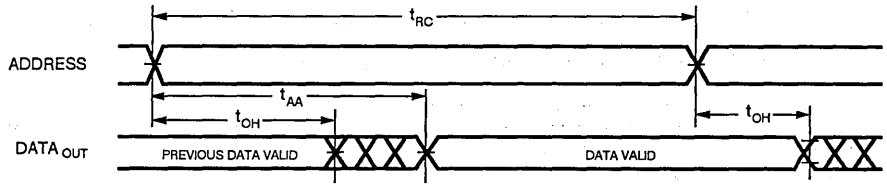
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7052S25 (3) IDT7052L25 (3) MIN.	MAX.	IDT7052S30 IDT7052L30 MIN.	MAX.	IDT7052S35 IDT7052L35 MIN.	MAX.	IDT7052S45 IDT7052L45 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	ns
t_{ACE}	Chip Enable Access Time	–	25	–	30	–	35	–	45	ns
t_{AOE}	Output Enable Access Time	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time (1, 2)	3	–	3	–	5	–	5	–	ns
t_{HZ}	Output High Z Time (1, 2)	–	15	–	15	–	15	–	20	ns
t_{PU}	Chip Enable to Power Up Time (2)	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time (2)	–	20	–	30	–	50	–	50	ns

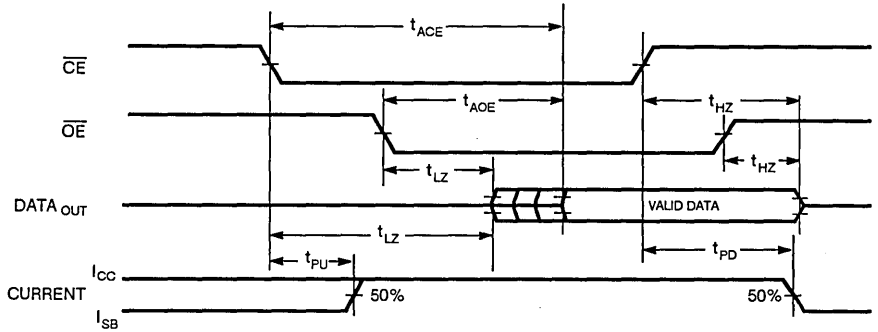
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to 70°C temperature range only.

5

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT (1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

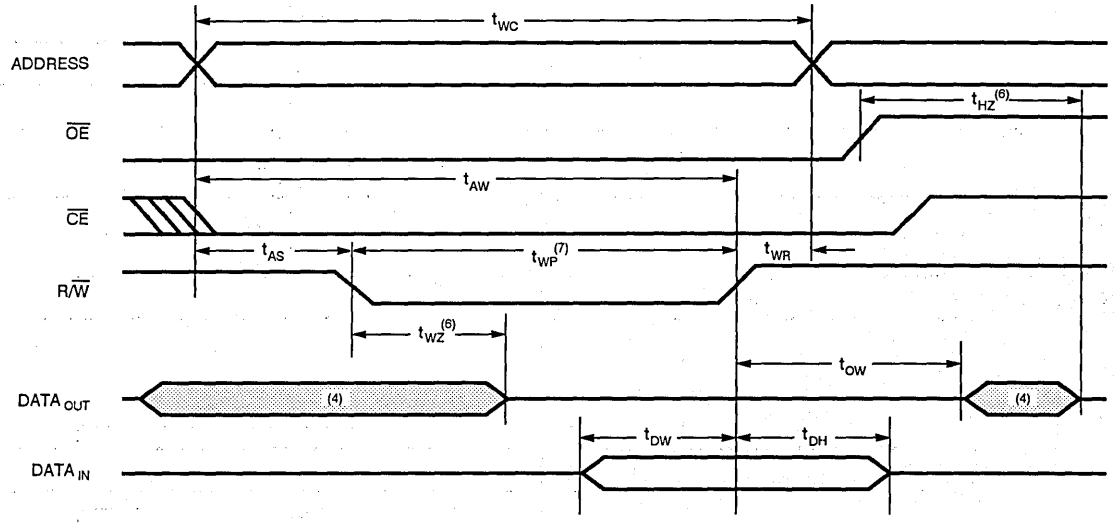
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

SYMBOL	PARAMETER	IDT7052S25 [7] IDT7052L25 [7] MIN.	MAX.	IDT7052S30 IDT7052L30 MIN.	MAX.	IDT7052S35 IDT7052L35 MIN.	MAX.	IDT7052S45 IDT7052L45 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	ns
t_{EW}	Chip Enable to End of Write	20	–	25	–	30	–	35	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width [3]	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	20	–	ns
t_{HZ}	Output High Z Time [1,2]	–	15	–	15	–	15	–	20	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z [1,2]	–	15	–	15	–	15	–	20	ns
t_{OW}	Output Active From End of Write [1,2]	0	–	0	–	0	–	0	–	ns
t_{WDD}	Write Pulse to Data Delay [4]	–	40	–	50	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay [4]	–	30	–	35	–	40	–	45	ns
BUSY INPUT TIMING										
t_{WB}	Write to $\overline{BUSY}$ [5]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{BUSY}$ [6]	15	–	20	–	20	–	20	–	ns

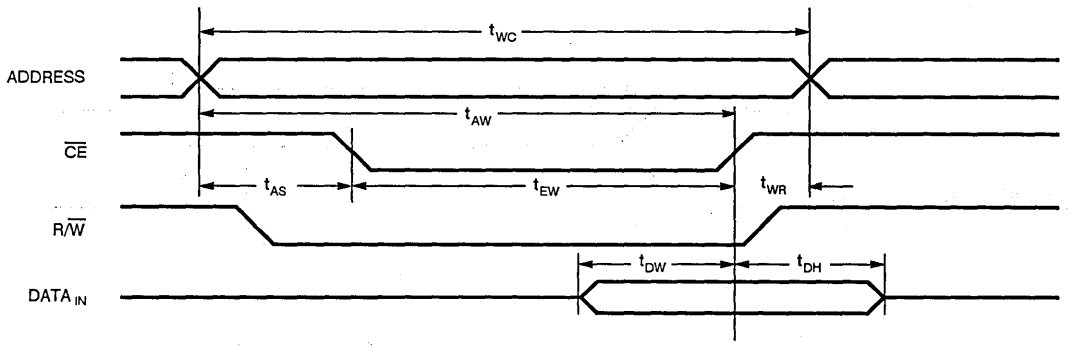
NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "TIMING WAVEFORM OF WRITE CYCLE", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING [1, 2, 3, 7]



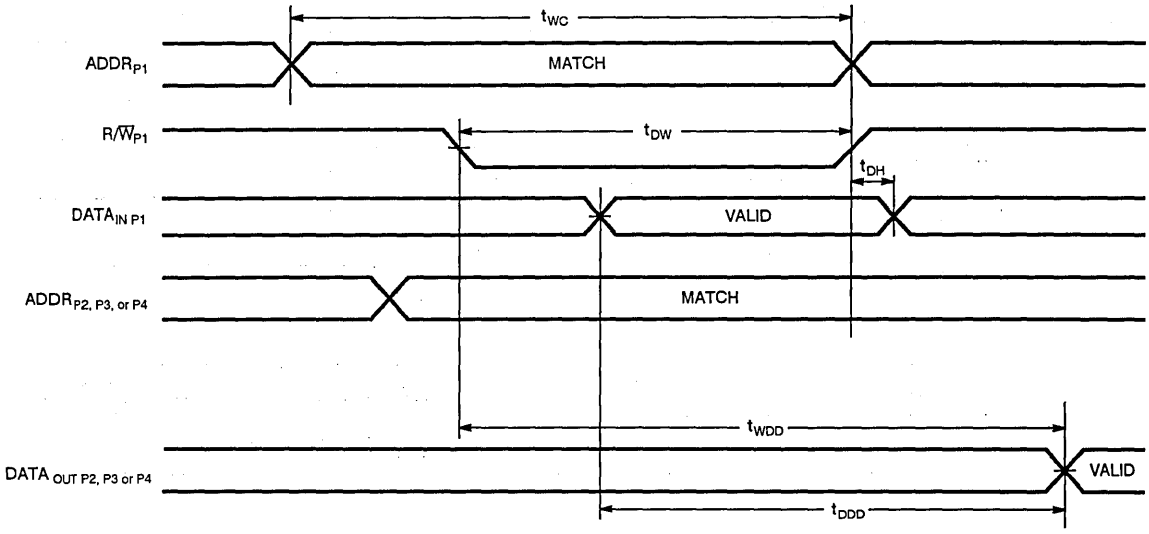
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING [1, 2, 3, 5]



NOTES:

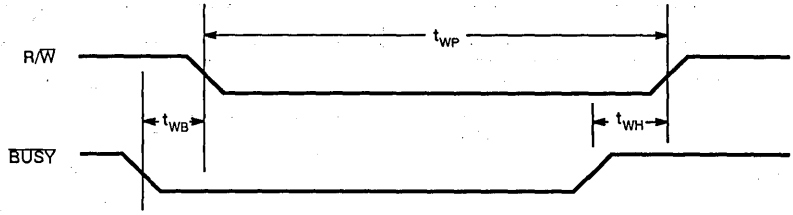
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2, 3)



NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



FUNCTIONAL DESCRIPTION:

The IDT7052 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I—READ/WRITE CONTROL

ANY PORT (1)				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$, = H Power Down Mode, I_{SB} or I_{SB1}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2,3)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES:

1. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
2. If $\overline{BUSY}$ = LOW, Data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

5

FIFO MEMORIES

Integration of IDT's high-speed static RAM technology with internal support logic yields high-performance, high-density FIFO memories. A FIFO is used as a memory buffer between two asynchronous systems with simultaneous read/write access. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses. Since these FIFOs are built with an internal RAM pointer architecture, there is no fall-through time between a write to a memory location and a read from that memory location. System performance is significantly improved over the shift register-based architecture of previous FIFO designs which are handicapped with long fall-through times.

IDT offers the widest selection of monolithic FIFOs, ranging from shallow 64 x 4 and 64 x 5 to the high-density 4K x 9. Shallow FIFOs regulate data flow in tightly coupled computational engines. High density FIFOs store large data blocks in networking, telecommunication and data storage systems. The IDT7200 FIFO family (256 x 9 through the 4K x 9 FIFOs) are all pin and function compatible, making density upgrades simple. All IDT FIFOs can be cascaded to greater word depths and expanded to greater word widths with no external support logic.

A variety of packages are available: standard plastic DIP and CERDIP, surface mount ceramic LCC, PLCC and SOIC and high-reliability Flatpack. Increasing board density is the overwhelming goal of the IDT's package development efforts, as demonstrated by the introduction of the 300 mil THINDIP.

The Parallel-Serial FIFO incorporates a serial input and a serial output shifter for serial-to-parallel bus interface. The Parallel-Serial FIFO also offers six status flags for flexible data throttling.

FIFO modules, composed of four LCC devices mounted on a multi-layer co-fired ceramic substrate, increase densities to 16K x 9 which are pin-compatible with current monolithic versions.

IDT is committed to offering FIFOs of increasing density and speed and enhanced architectural innovations, such as Flexishift and the BiFIFO, for easier system interface.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

IDT 7200S/L
IDT 7201SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 X 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7200 and IDT7201A are pin and functionally compatible with Mostek MK4501, but with Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS ™ technology
- Available in plastic DIP, CERDIP, 300 mil THINDIP, LCC, PLCC and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87531 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7200/7201A are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 35ns (28.5MHz).

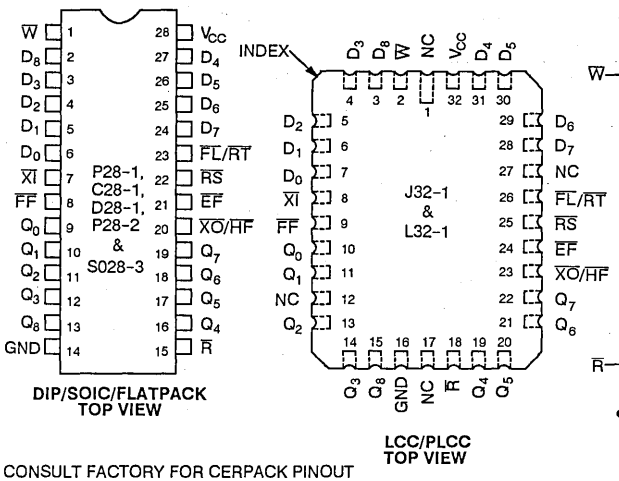
The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7200/1A are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

PIN CONFIGURATIONS

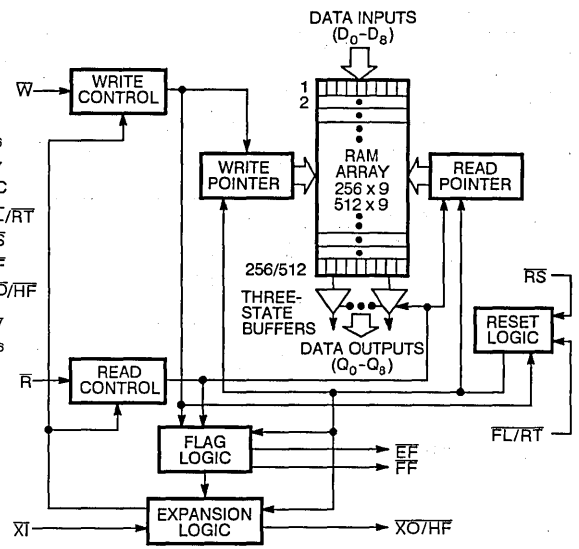


DIP/SOIC/FLATPACK TOP VIEW

LCC/PLCC TOP VIEW

CONSULT FACTORY FOR CERPACK PINOUT

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial and Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 25, 35ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 30, 40ns			IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	–	125 (4)	–	–	140 (4)	–	50	80	–	70	100	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}	–	–	15	–	–	20	–	5	8	–	8	15	mA
$I_{CC3(L)}$ (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
$I_{CC3(S)}$ (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. Tested at f = 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L. 7200x25 7201x25		MIL. 7200x30 7201x30		COM'L. 7200x35 7201x35		MIL. 7200x40 7201x40		MILITARY AND COMMERCIAL 7200x50 7201x50		7200x65 7201x65		7201x80		7201x120		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z [3]	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z [3, 4]	5	–	5	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z [3]	–	18	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time [3]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	30	–	30	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.
5. "x" in part rating indicates power rating (S/SA or L/LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

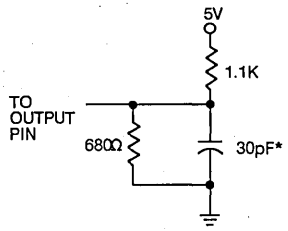


Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0–D_8)

Data inputs for 9-bit wide data.

CONTROLS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for the IDT7200 and 512 writes for the IDT7201A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

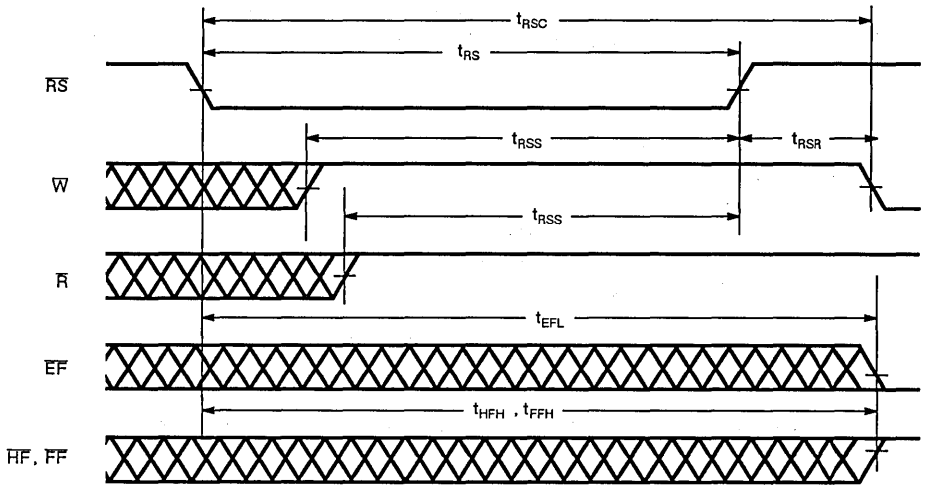
After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a

signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Figure 2. Reset

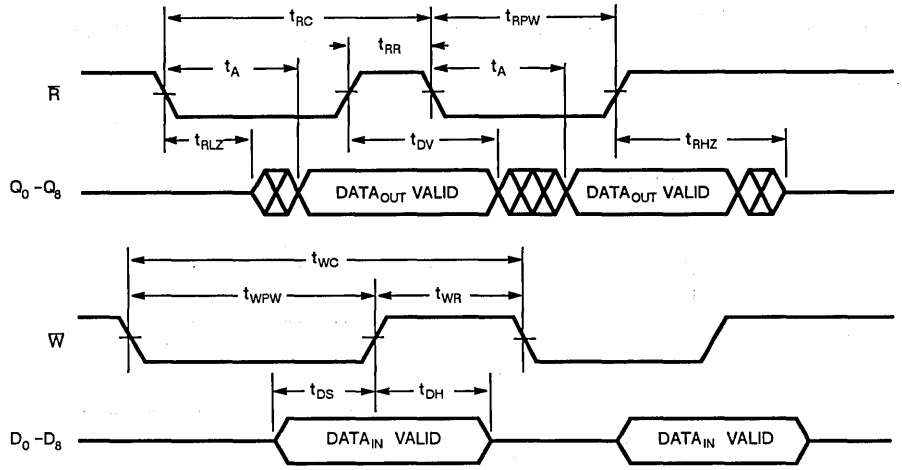


Figure 3. Asynchronous Write and Read Operation

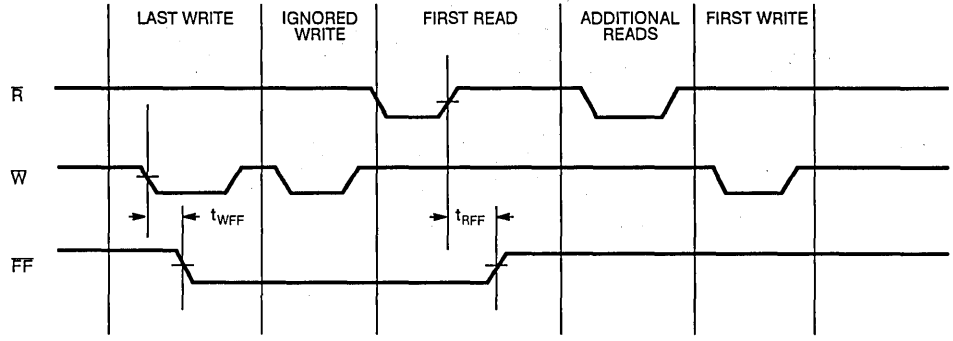


Figure 4. Full Flag From Last Write to First Read

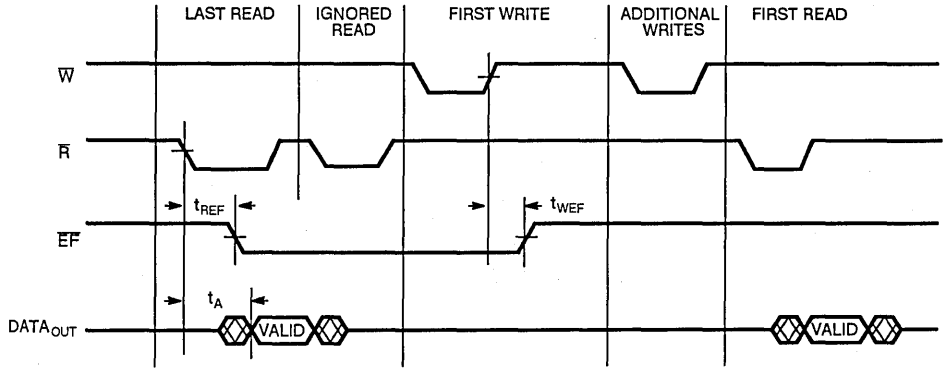
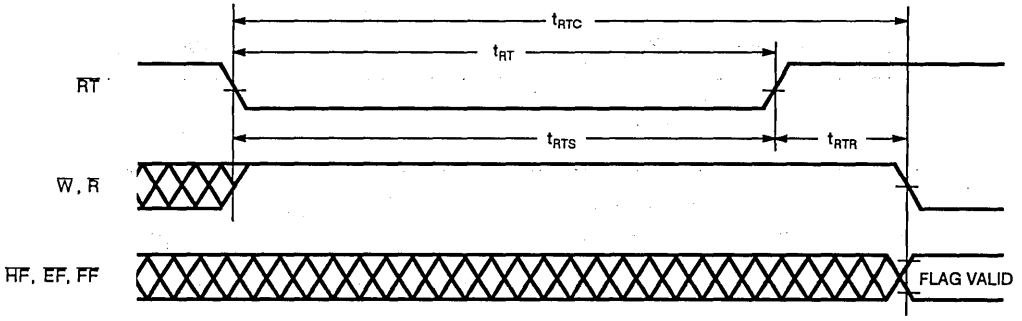


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

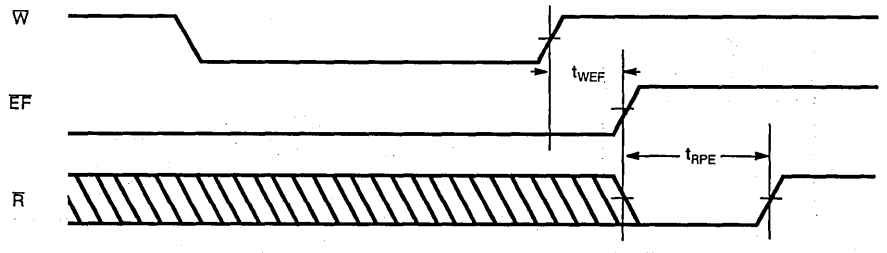


Figure 7. Empty Flag Timing

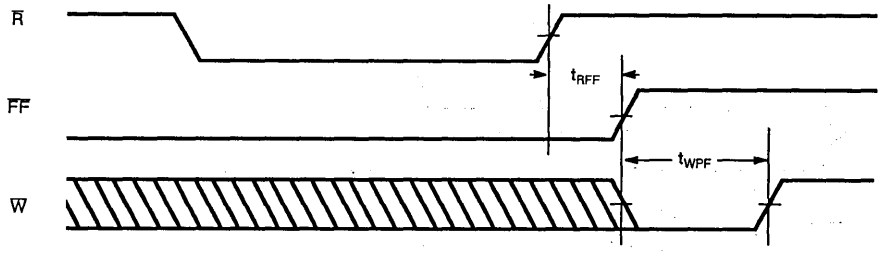


Figure 8. Full Flag Timing

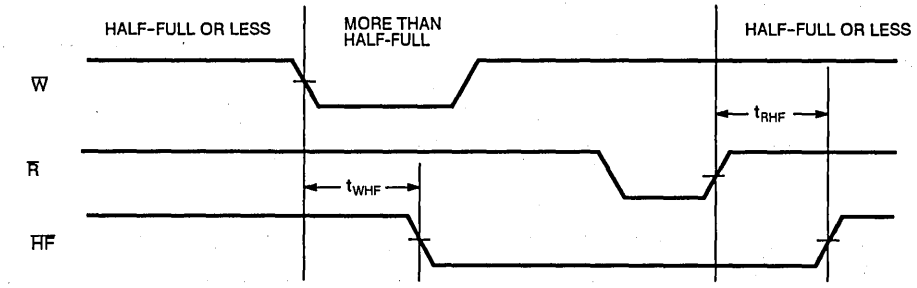


Figure 9. Half-Full Flag Timing

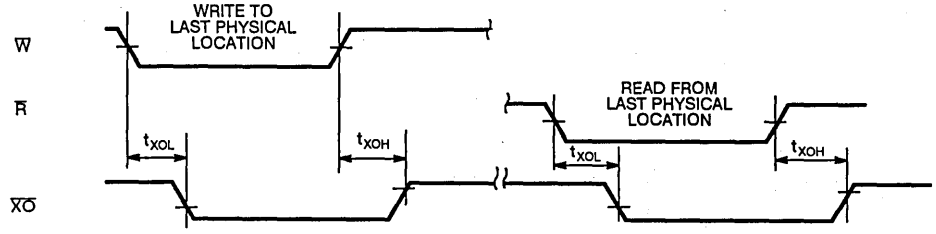


Figure 10. Expansion Out

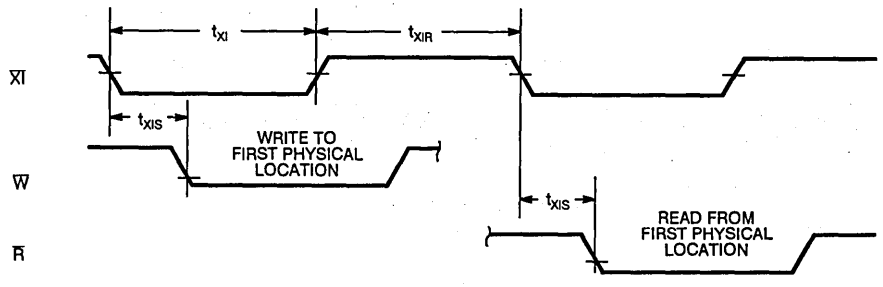


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7200/7201A may be used when the application requirements are for 256/512 words or less. The IDT7200/7201A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

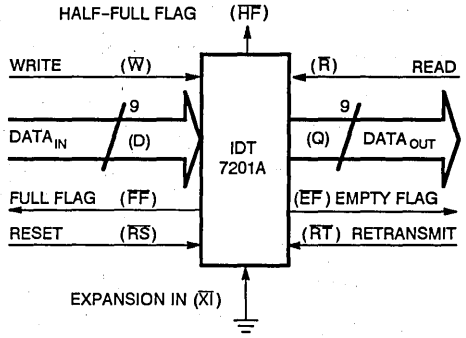
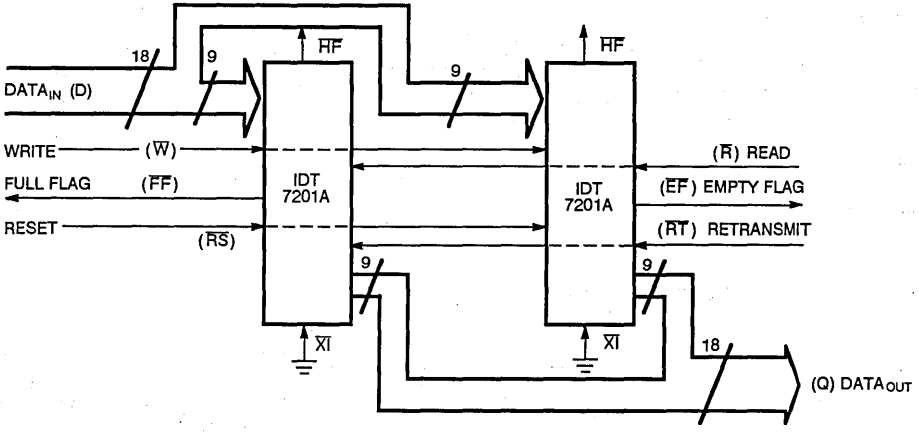


Figure 12. Block Diagram of Single 512x9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$,$\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7201As. Any word width can be attained by adding additional IDT7201As.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 512x18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7200/7201A can easily be adapted to applications where the requirements are for greater than 256/512 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201As. Any depth can be attained by adding additional IDT7200/7201As. The IDT7200/7201A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system, (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs."

TABLE I—RESET AND RETRANSMIT—

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE—

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.

$\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

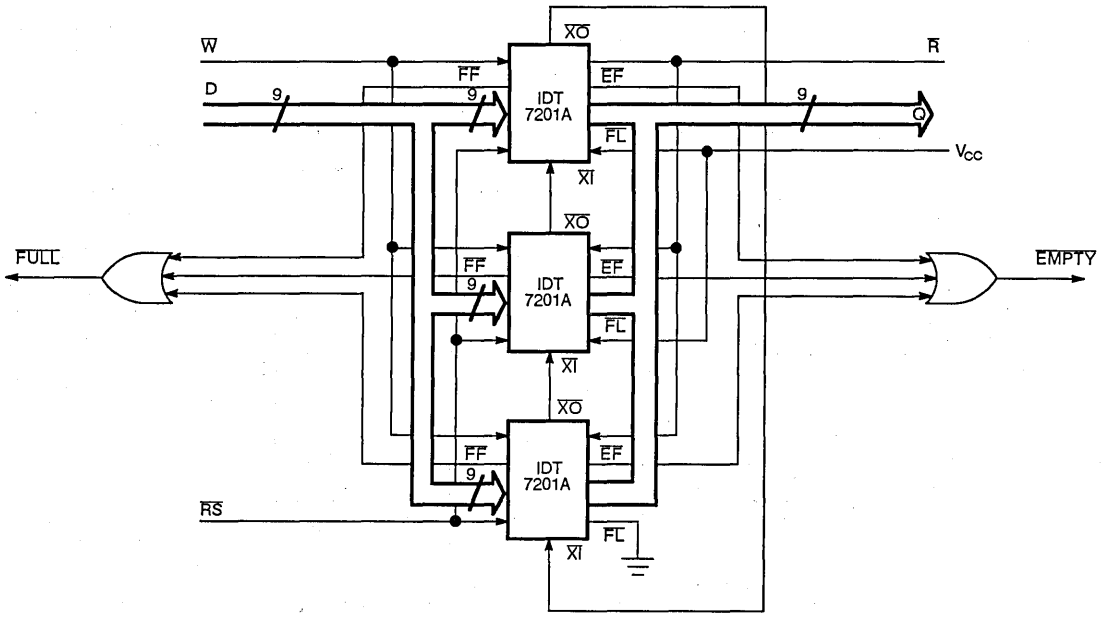
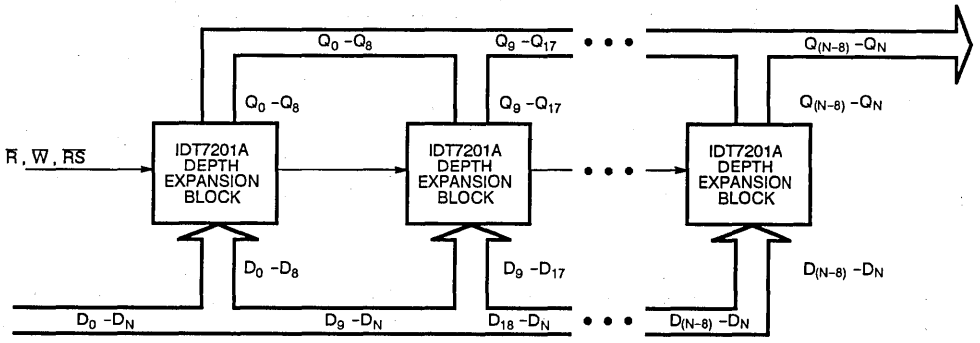


Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

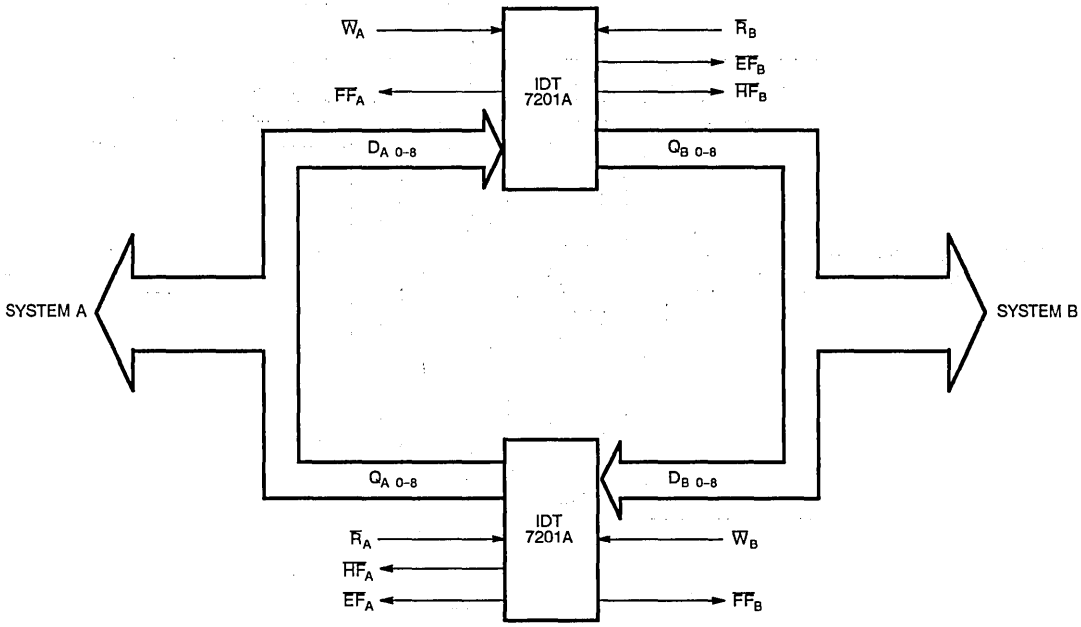


Figure 16. Bidirectional FIFO Mode

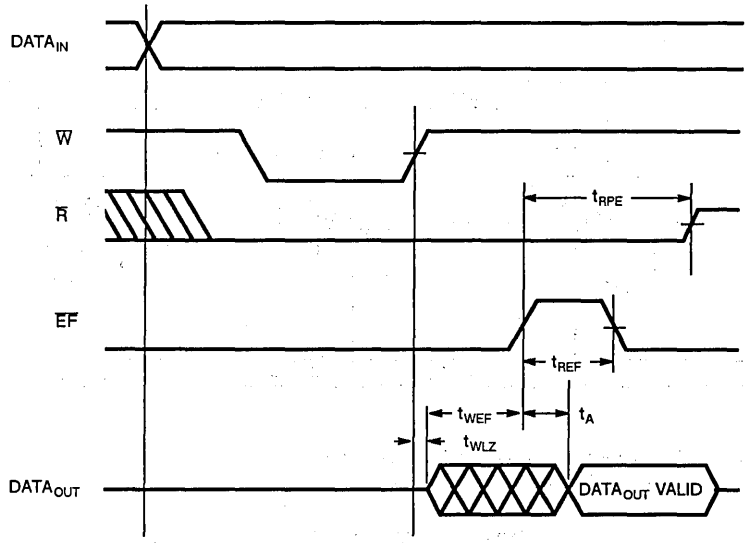


Figure 17. Read Data Flow-Through Mode

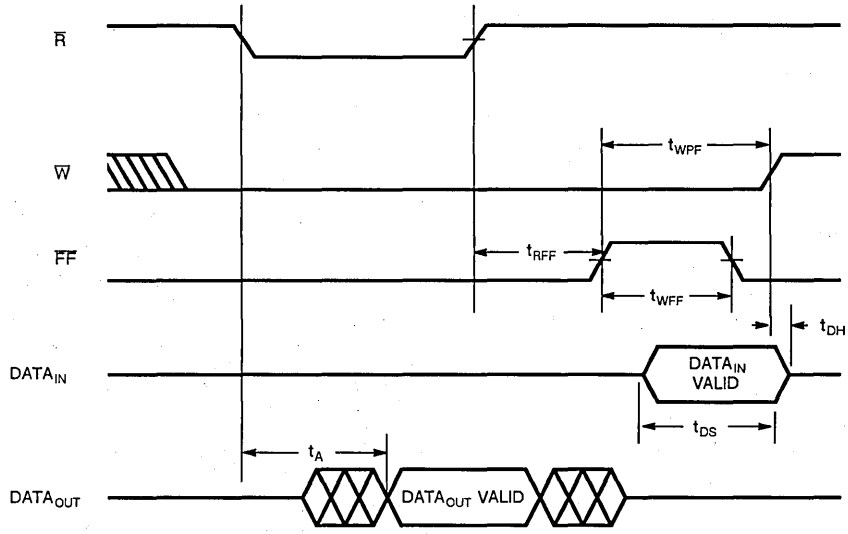


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT — XXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
SO	SOIC
P	Plastic Dip
D	CERDIP
TC	Sidebraze THINDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
TP	Plastic THINDIP
XE	Cerpack
25	Commercial Only
30	Military Only
35	Commercial Only
40	Military Only
50	Access Time (t_A) Speed in Nanoseconds
65	
80	
120	
SA	Standard Power*
LA	Low Power*
7200	256 x 9-Bit FIFO
7201	512 x 9-Bit FIFO

* "A" to be included for 7201 ordering part number only.

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 1024 x 9-BIT

IDT 7202SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 1024 x 9 organization
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin compatible with Mostek MK4501, but with Half-Full Flag capability
- Allows for deep word structure (1024) without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in Plastic DIP, CERDIP, 300 mil THINDIP, LCC, PLCC and Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7202A is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

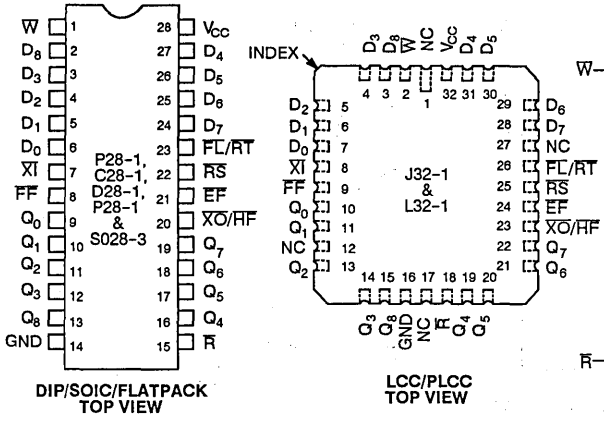
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 35ns (28.5MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7202A is fabricated using IDT's high-speed CEMOS technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

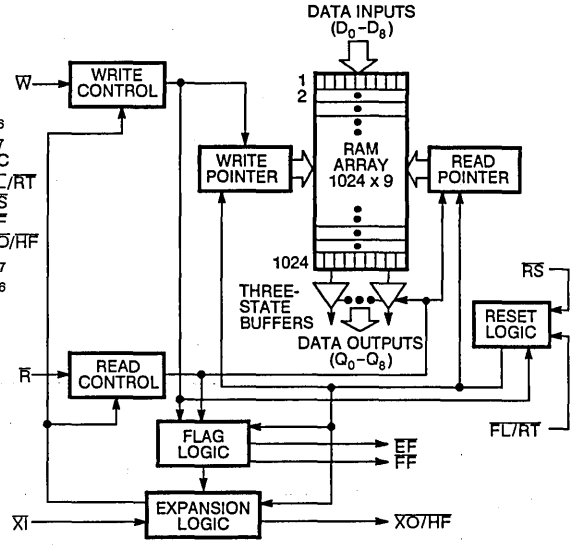
PIN CONFIGURATIONS



DIP/SOIC/FLATPACK TOP VIEW

CONSULT FACTORY FOR CERPACK PINOUT

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL}[1]	Input Low Voltage Commercial and Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7202SA/LA COMMERCIAL t_A = 25, 35ns			IDT7202SA/LA MILITARY t_A = 30, 40ns			IDT7202SA/LA COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7202SA/LA MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI}[1]	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO}[2]	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1}[3]	Active Power Supply Current	–	–	125[4]	–	–	140[4]	–	50	80	–	70	100	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}	–	–	15	–	–	20	–	5	8	–	8	15	mA
I_{CC3} (L)[3]	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
I_{CC3} (S)[3]	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. Tested at f = 20 MHz

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		COM'L.		MIL.		MILITARY AND COMMERCIAL								UNIT
		7202x25		7202x30		7202x35		7202x40		7202x50		7202x65		7202x80		7202x120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z [3]	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z [3, 4]	5	–	5	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z [3]	–	18	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width [2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time [3]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	30	–	30	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.
5. "x" in part rating indicates power rating (SA or LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

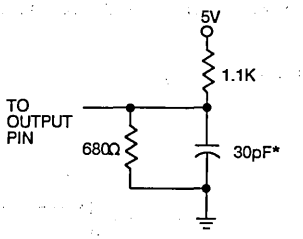

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS

DATA IN (D_0-D_8)

Data inputs for 9-bit wide data.

CONTROLS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0-Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7202A can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-flag ($\overline{FF}$) will go low after 1024 writes.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to

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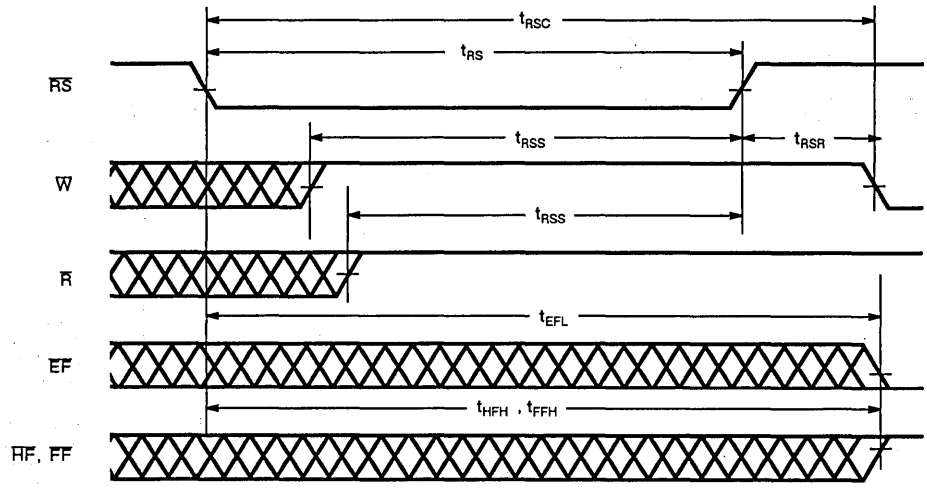
the next device when the previous device reaches the last location of memory.

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

DATA OUTPUTS (Q_0 -Q_8)



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Figure 2. Reset

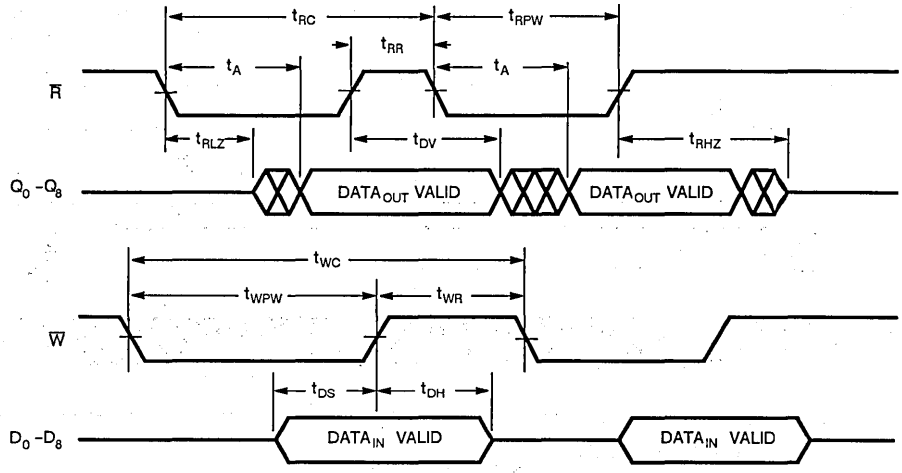


Figure 3. Asynchronous Write and Read Operation

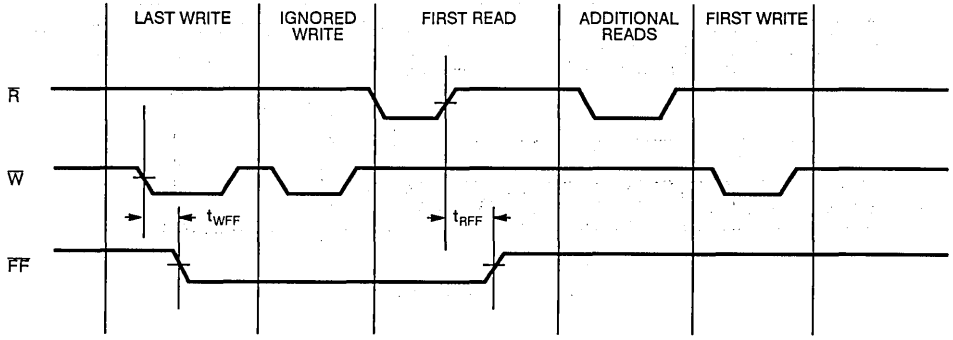


Figure 4. Full Flag From Last Write to First Read

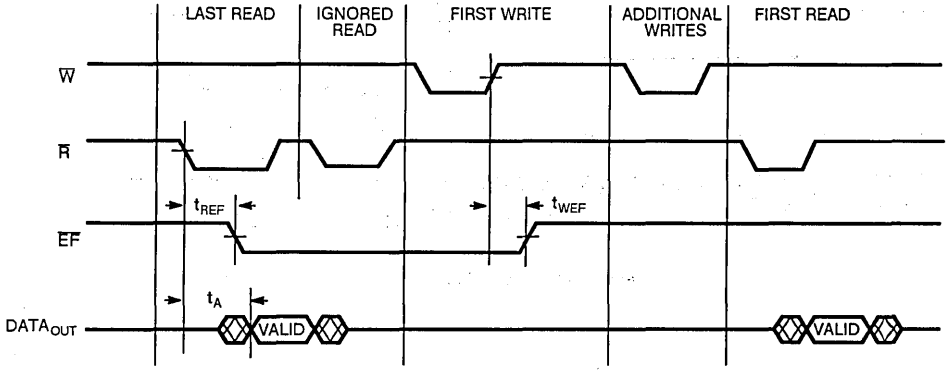
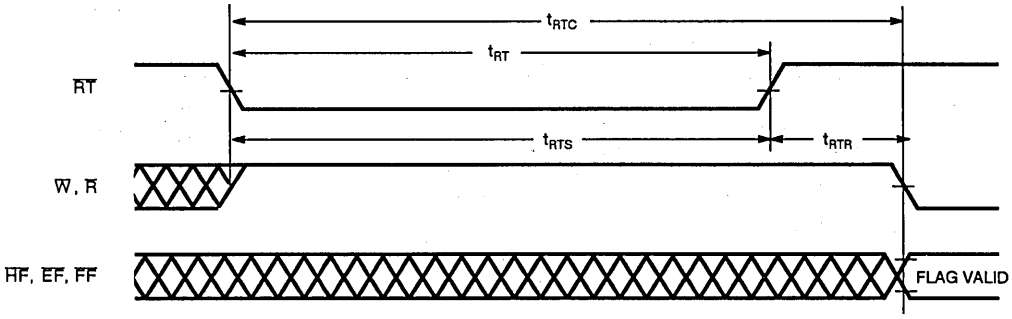


Figure 5. Empty Flag From Last Read to First Write



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

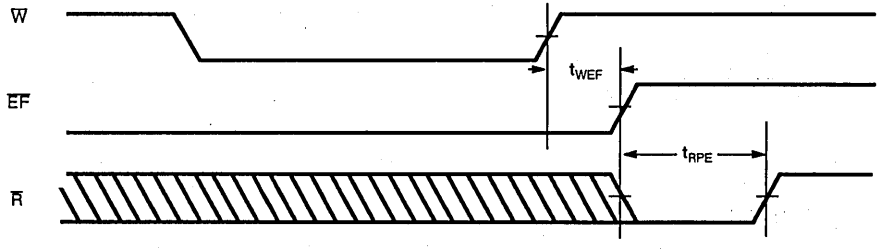


Figure 7. Empty Flag Timing

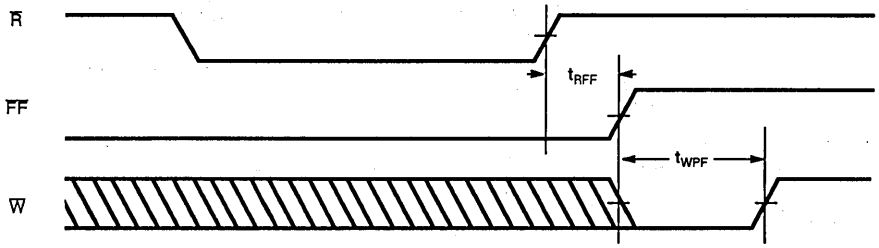


Figure 8. Full Flag Timing

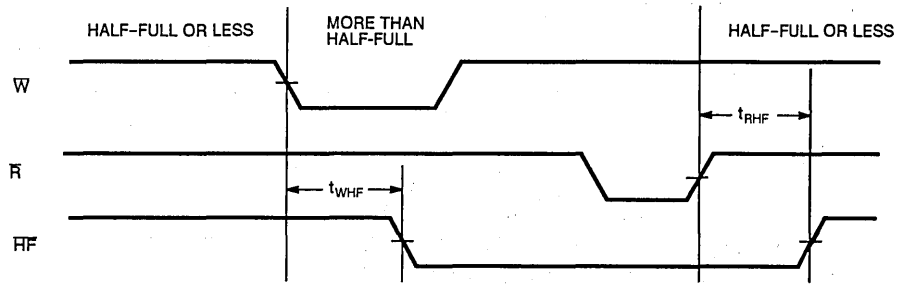


Figure 9. Half-Full Flag Timing

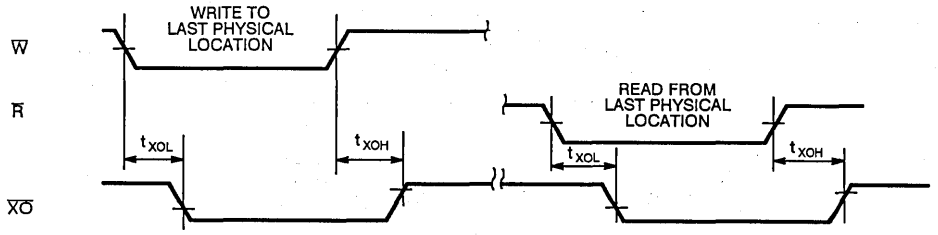


Figure 10. Expansion Out

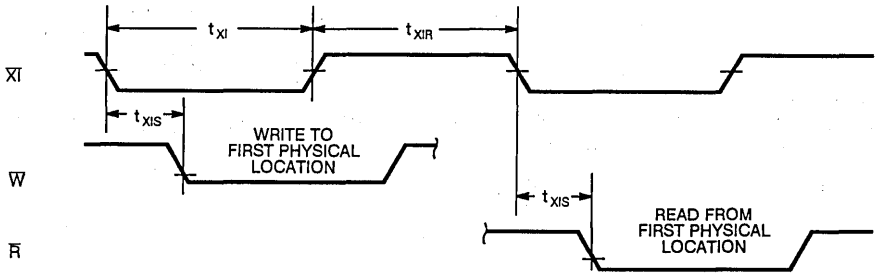


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7202A may be used when the application requirements are for 1024 words or less. The IDT7202A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

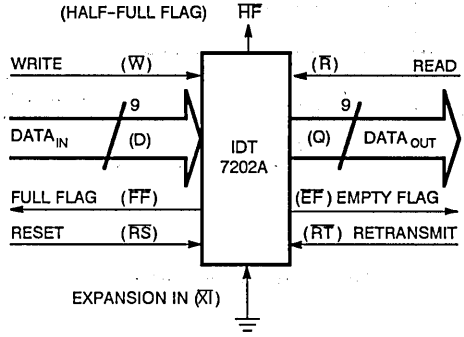
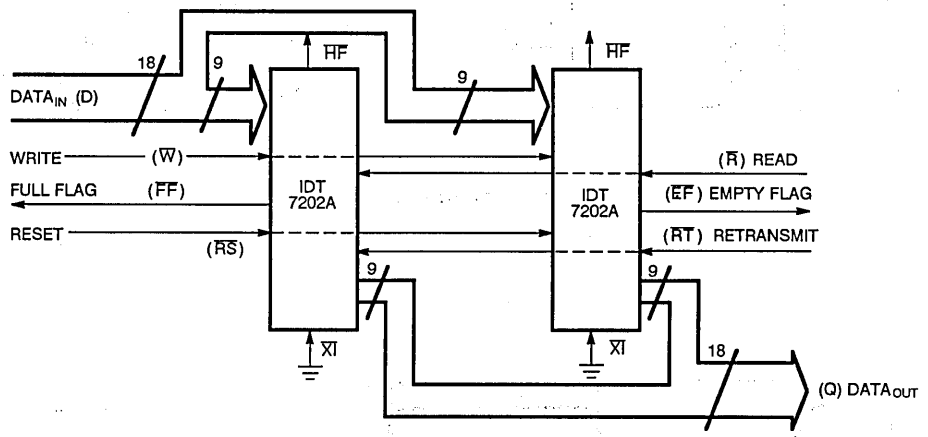


Figure 12. Block Diagram of Single 1024 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7202As. Any word width can be attained by adding additional IDT7202s.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7202A can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 14 demonstrates Depth Expansion using three IDT7202As. Any depth can be attained by adding additional IDT7202As. The IDT7202As operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7202As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

6

TABLE I – RESET AND RETRANSMIT –

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTES:

1. Pointer will increment if flag is high.

TABLE II – RESET AND FIRST LOAD TRUTH TABLE –

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.

$\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

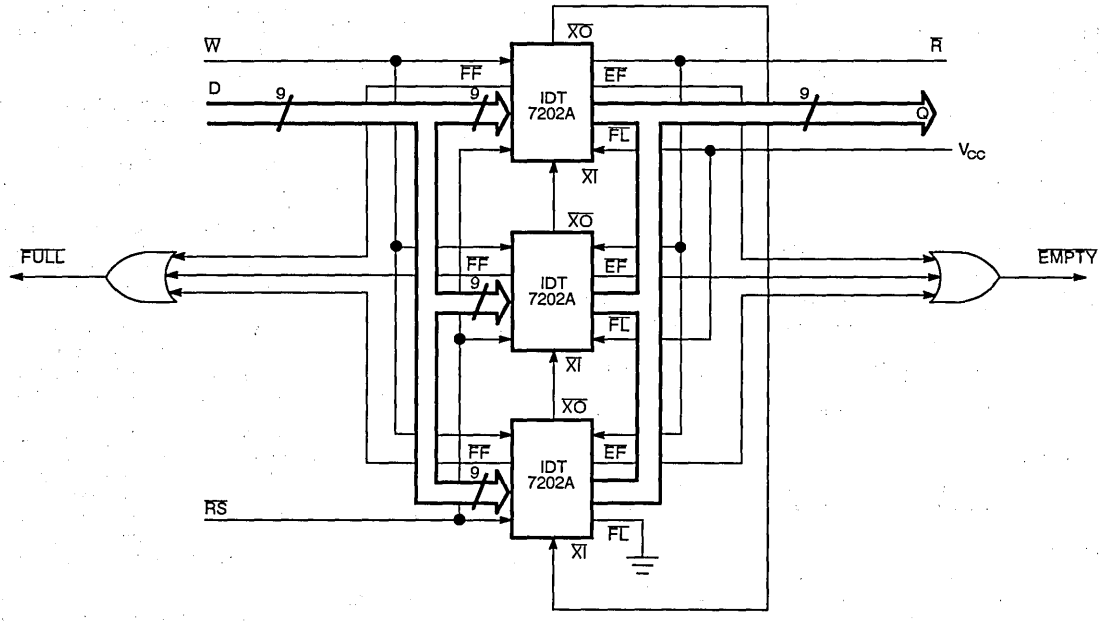
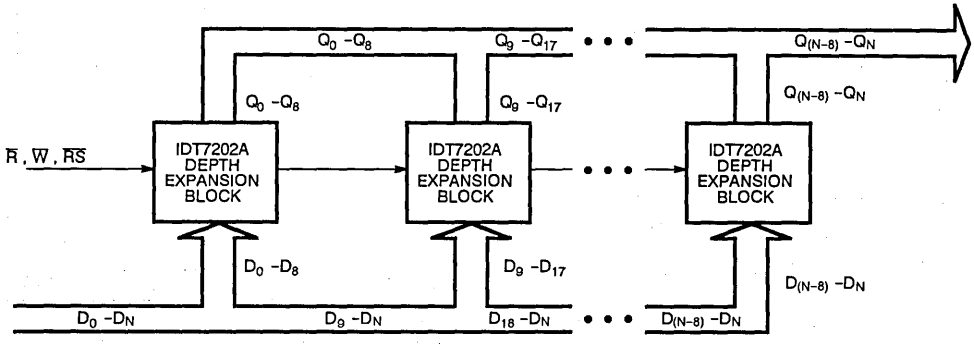


Figure 14. Block Diagram of 3072 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

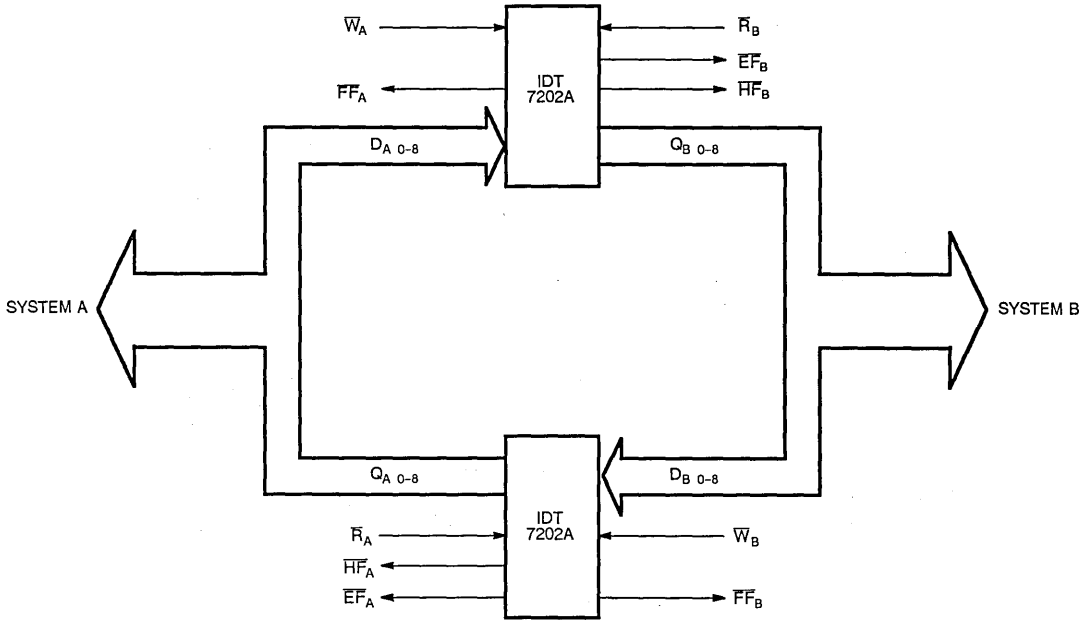


Figure 16. Bidirectional FIFO Mode

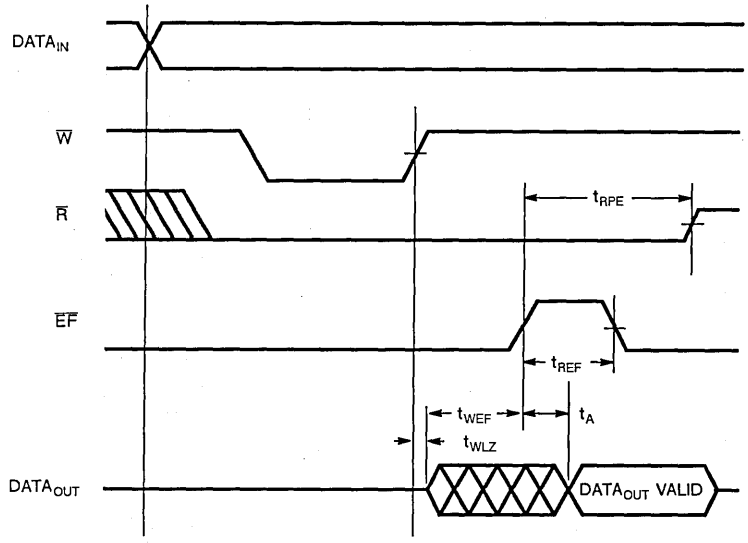


Figure 17. Read Data Flow-Through Mode

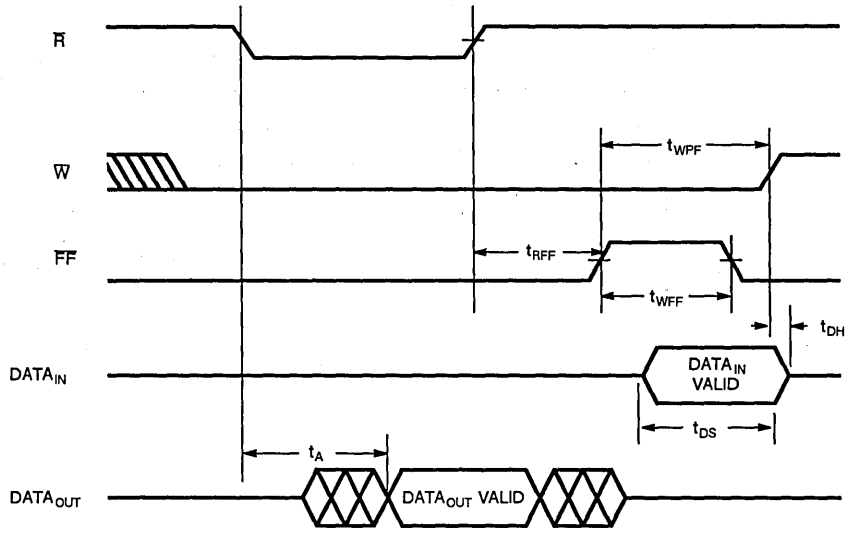
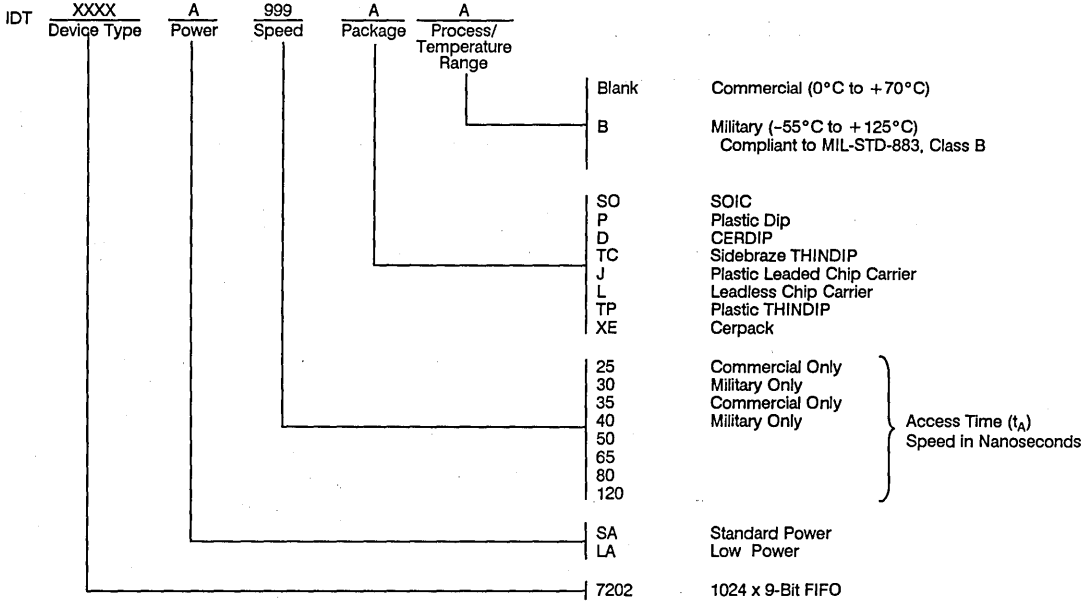


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL FLAGGED FIFO WITH $\overline{OE}$ 1K x 9, 2K x 9, 4K x 9

IDT 72021
IDT 72031
IDT 72041

FEATURES:

- First-In/First-Out dual-port memory
- Bit organization
  - IDT72021 – 1K x 9
  - IDT72031 – 2K x 9
  - IDT72041 – 4K x 9
- Ultra high speed
  - IDT72021 – 25ns access time, 35ns cycle time
  - IDT72031 – 35ns access time, 45ns cycle time
  - IDT72041 – 35ns access time, 45ns cycle time
- Low power CMOS
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost-Empty/Almost-Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

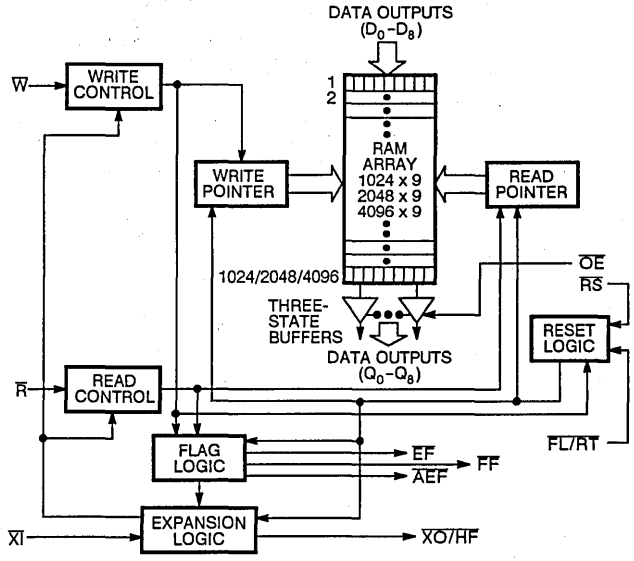
DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's high-performance CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

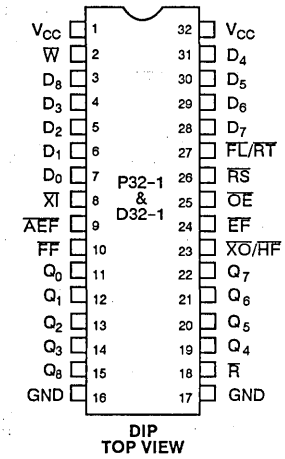
6

FUNCTIONAL BLOCK DIAGRAM

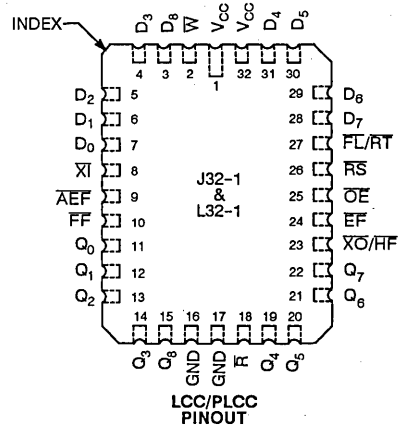


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
PINOUT

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D0-D8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array, $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be high during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	When WRITE is low, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{FF}$ must be high. When the FIFO is full ($\overline{FF}$-low), the internal WRITE operation is blocked.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked. Q0-Q8 are in a high impedance condition.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ and $\overline{W}$ must be high before setting $\overline{FL}/\overline{RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$-low indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three-state buffers inhibit data flow.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q0 - Q8	Outputs	O	Data outputs for 9-bit wide data.

STATUS FLAGS

NUMBER OF WORDS IN FIFO			$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
1K	2K	4K				
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS – IDT72021

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT72021 COMMERCIAL t_A = 25, 35ns			IDT72021 MILITARY t_A = 30, 40ns			IDT72021 COMMERCIAL t_A = 50, 65, 80, 120ns			IDT72021 MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	–	120 (5)	–	–	140 (5)	–	50	80	–	70	100	mA
I_{CC2} (3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	–	–	15	–	–	20	–	5	8	–	8	15	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
I_{CC3} (S) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

DC ELECTRICAL CHARACTERISTICS – IDT72031/041

SYMBOL	PARAMETER	IDT72031 IDT72041 COMMERCIAL t_A = 35ns			IDT72031 IDT72041 MILITARY t_A = 40ns			IDT72031 IDT72041 COMMERCIAL t_A = 50, 65, 80, 120ns			IDT72031 IDT72041 MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	90	140 (6)	–	105	160 (6)	–	75	120	–	100	150	mA
I_{CC2} (3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	–	8	12	–	12	25	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	2	–	–	4	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	8	–	–	12	–	–	8	–	–	12	mA

NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with $\overline{OE}$ = HIGH.
4. (L) - Low Power, (S) - Standard Power
5. Tested at f = 20 MHz.
6. Tested at f = 15.3 MHz.

AC ELECTRICAL CHARACTERISTICS – IDT72021 [1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.	MIL.	COM'L.	MIL.	MILITARY AND COMMERCIAL				UNIT
		72021x25	72021x30	72021x35	72021x40	72021x50	72021x65	72021x80	72021x120	
		MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	MIN. MAX.	
f_S	Shift Frequency	– 28.5	– 25	– 22.2	– 20	– 15	– 12.5	– 10	– 7	MHz
t_{RC}	$\overline{R}$ Cycle Time	35 –	40 –	45 –	50 –	65 –	80 –	100 –	140 –	ns
t_A	Access Time	– 25	– 30	– 35	– 40	– 50	– 65	– 80	– 120	ns
t_{RR}	$\overline{R}$ Recovery Time	10 –	10 –	10 –	10 –	15 –	15 –	20 –	20 –	ns
t_{RPW}	$\overline{R}$ Pulse Width [2]	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z [3]	5 –	5 –	5 –	5 –	10 –	10 –	10 –	10 –	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z [3, 4]	5 –	5 –	5 –	5 –	5 –	5 –	5 –	5 –	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5 –	5 –	5 –	5 –	5 –	5 –	5 –	5 –	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z [3]	– 18	– 20	– 20	– 25	– 30	– 30	– 30	– 35	ns
t_{WC}	$\overline{W}$ Cycle Time	35 –	40 –	45 –	50 –	65 –	80 –	100 –	140 –	ns
t_{WPW}	$\overline{W}$ Pulse Width [2]	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{WR}	$\overline{W}$ Recovery Time	10 –	10 –	10 –	10 –	15 –	15 –	20 –	20 –	ns
t_{DS}	Data Set-up Time	15 –	18 –	18 –	20 –	30 –	30 –	40 –	40 –	ns
t_{DH}	Data Hold Time	0 –	0 –	0 –	0 –	5 –	10 –	10 –	10 –	ns
t_{RSC}	$\overline{RS}$ Cycle Time	35 –	40 –	45 –	50 –	65 –	80 –	100 –	140 –	ns
t_{RS}	$\overline{RS}$ Pulse Width [2]	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{RSS}	$\overline{RS}$ Set-up Time	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10 –	10 –	10 –	10 –	15 –	15 –	20 –	20 –	ns
t_{RTC}	$\overline{RT}$ Cycle Time	35 –	40 –	45 –	50 –	65 –	80 –	100 –	140 –	ns
t_{RT}	$\overline{RT}$ Pulse Width [2]	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10 –	10 –	10 –	10 –	15 –	15 –	20 –	20 –	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	– 25	– 30	– 30	– 35	– 45	– 60	– 60	– 60	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	– 25	– 30	– 30	– 35	– 45	– 60	– 60	– 60	ns
t_{RPE}	$\overline{R}$ Pulse Width After $\overline{EF}$ High	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	– 25	– 30	– 30	– 35	– 45	– 60	– 60	– 60	ns
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low	– 25	– 30	– 30	– 35	– 45	– 60	– 60	– 60	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	25 –	30 –	35 –	40 –	50 –	65 –	80 –	120 –	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	– 35	– 40	– 45	– 50	– 65	– 80	– 100	– 140	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable) [3]	0 12	0 15	0 17	0 20	0 25	0 30	0 30	0 30	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable) [3]	0 12	0 15	0 17	0 20	0 25	0 30	0 30	0 30	ns
t_{AOE}	$\overline{OE}$ Low to Data Valid (Q0-8)	– 15	– 18	– 20	– 25	– 30	– 40	– 40	– 40	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS – IDT72031/041 (1)

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	72031x35 72041x35 MIN.	72031x35 72041x35 MAX.	72031x40 72041x40 MIN.	72031x40 72041x40 MAX.	72031x50 72041x50 MIN.	72031x50 72041x50 MAX.	72031x65 72041x65 MIN.	72031x65 72041x65 MAX.	72031x80 72041x80 MIN.	72031x80 72041x80 MAX.	72031x120 72041x120 MIN.	72031x120 72041x120 MAX.	UNIT
f_s	Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	$\overline{R}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	$\overline{R}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	$\overline{R}$ Pulse Width (2)	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z (3)	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z (3, 4)	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z (3)	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	$\overline{W}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	$\overline{W}$ Pulse Width (2)	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	$\overline{W}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	$\overline{RS}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	$\overline{RS}$ Pulse Width (2)	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	$\overline{RS}$ Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	$\overline{RT}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	$\overline{RT}$ Pulse Width (2)	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	$\overline{R}$ Pulse Width after $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable) (3)	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable) (3)	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{AOE}	$\overline{OE}$ Low to Data Valid (Q0-8)	–	20	–	25	–	30	–	40	–	40	–	40	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read dataflow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

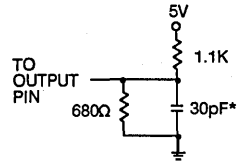


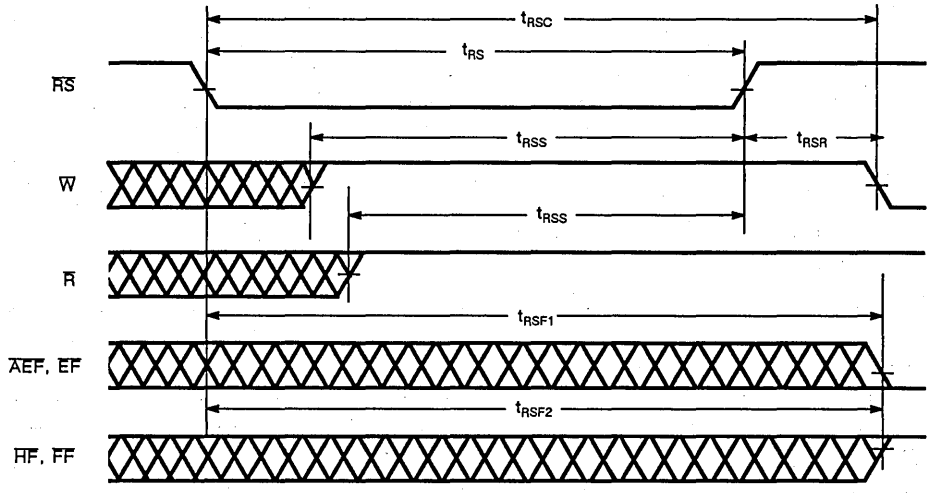
Figure 1. Output Load

*Includes scope and jig capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. These parameters are sampled and not 100% tested.



NOTES:
1. EF, FF, HF, and AEF may change status during Reset, but flags will be valid at t_{RSC}.
2. W and R = V_{IH} around the rising edge of RS.

Figure 2. Reset

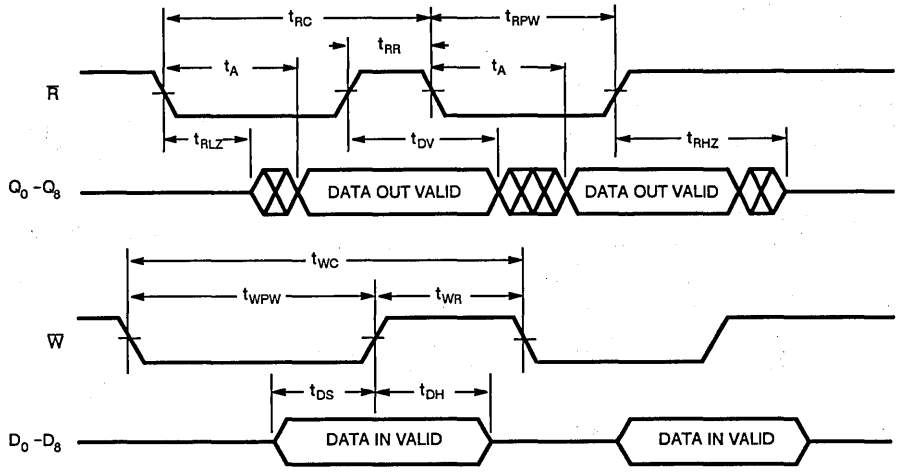


Figure 3. Asynchronous Write and Read Operation

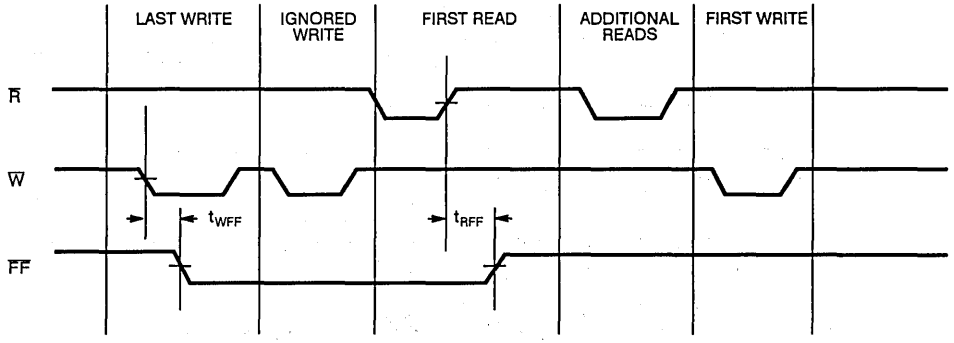


Figure 4. Full Flag From Last Write to First Read

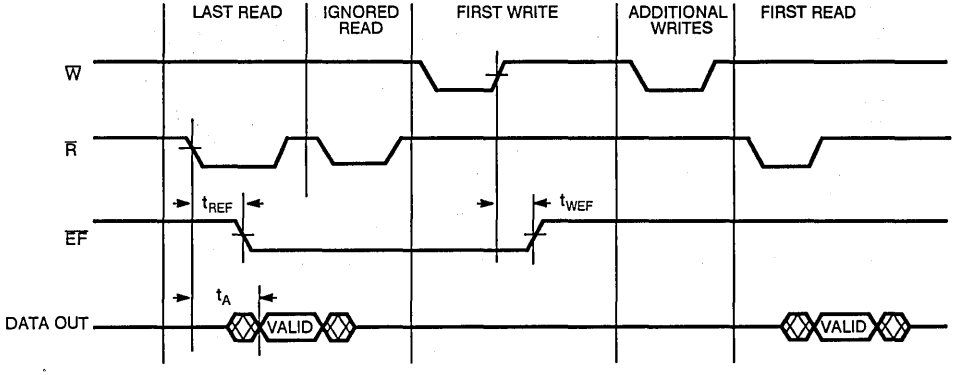
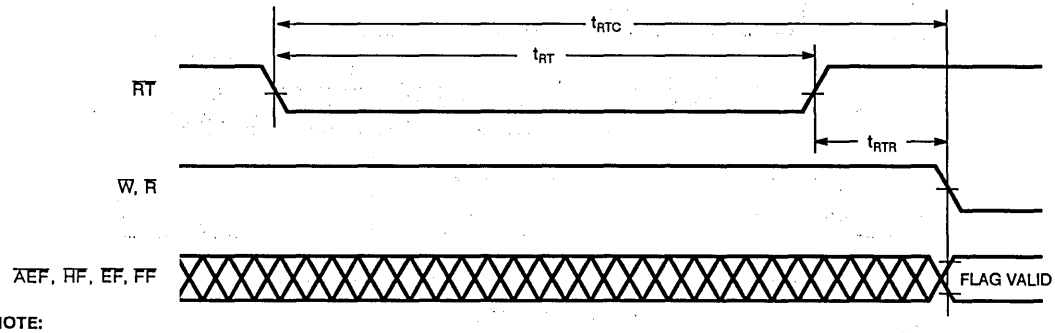


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

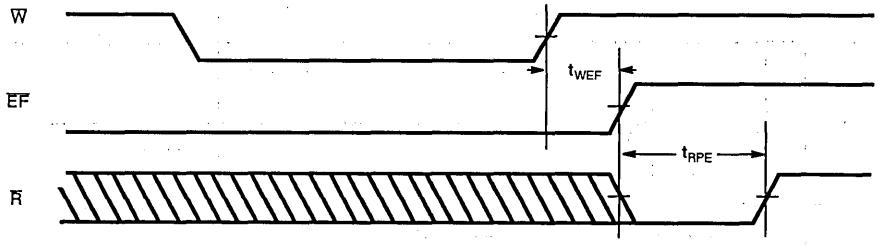


Figure 7. Empty Flag Timing

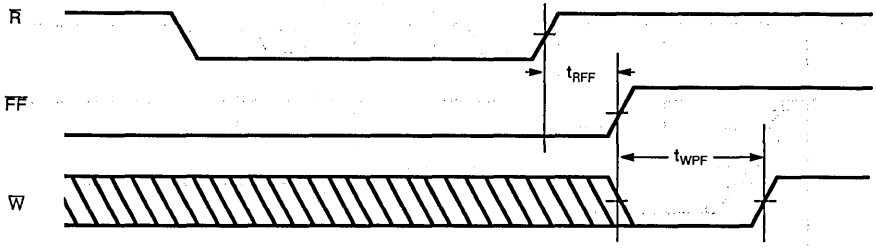


Figure 8. Full Flag Timing

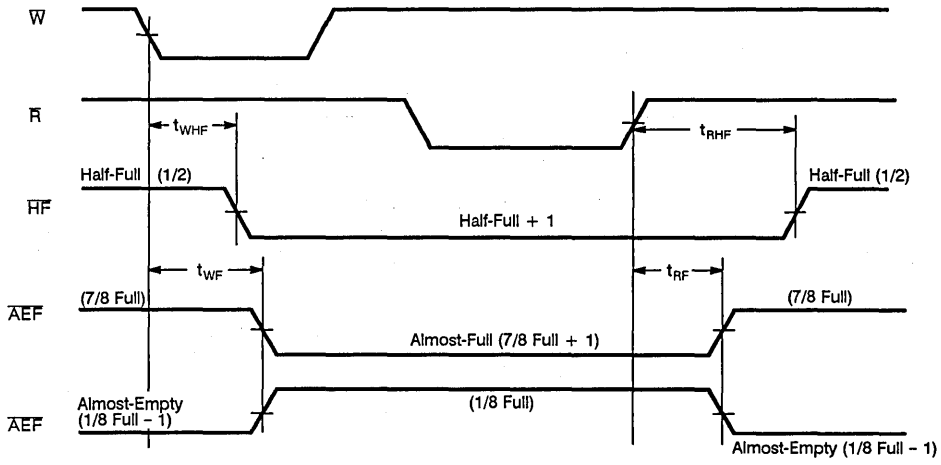


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

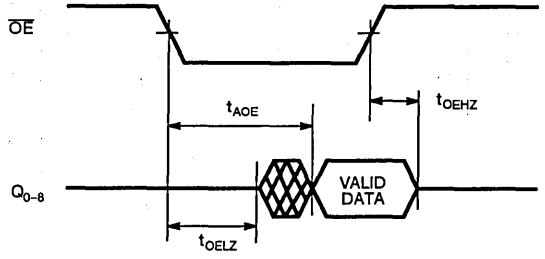


Figure 10. Output Enable Timings

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATIION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion in ($\overline{XI}$) control input is grounded (see Figure 11). In this mode, the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

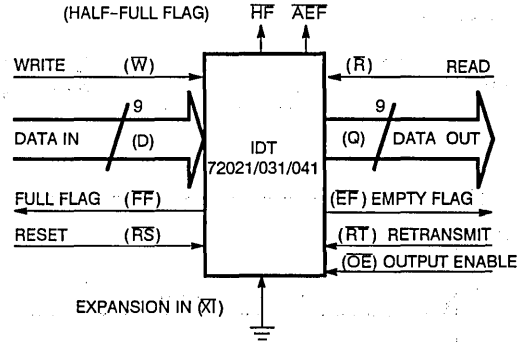
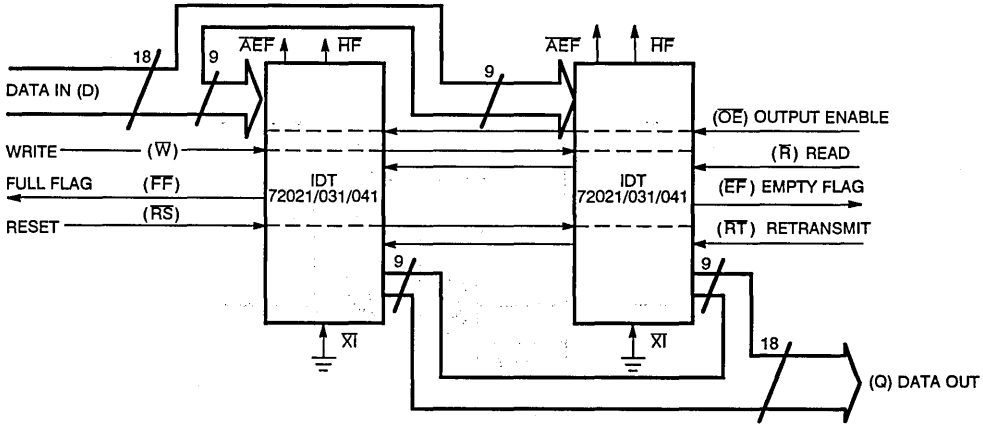


Figure 11. Block Diagram of Single 1K/2K/4K x 9 FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ $\overline{HF}$, and $\overline{AEF}$) can be detected from any one device. Figure 12 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, $\overline{HF}$ and $\overline{AEF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 12. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 13 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 13.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 13.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 14).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 15. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 16), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge. It remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 17), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

6

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X	X

NOTE:

1. Pointer will increment if flag is high.

TABLE II – RESET AND FIRST LOAD TRUTH TABLE

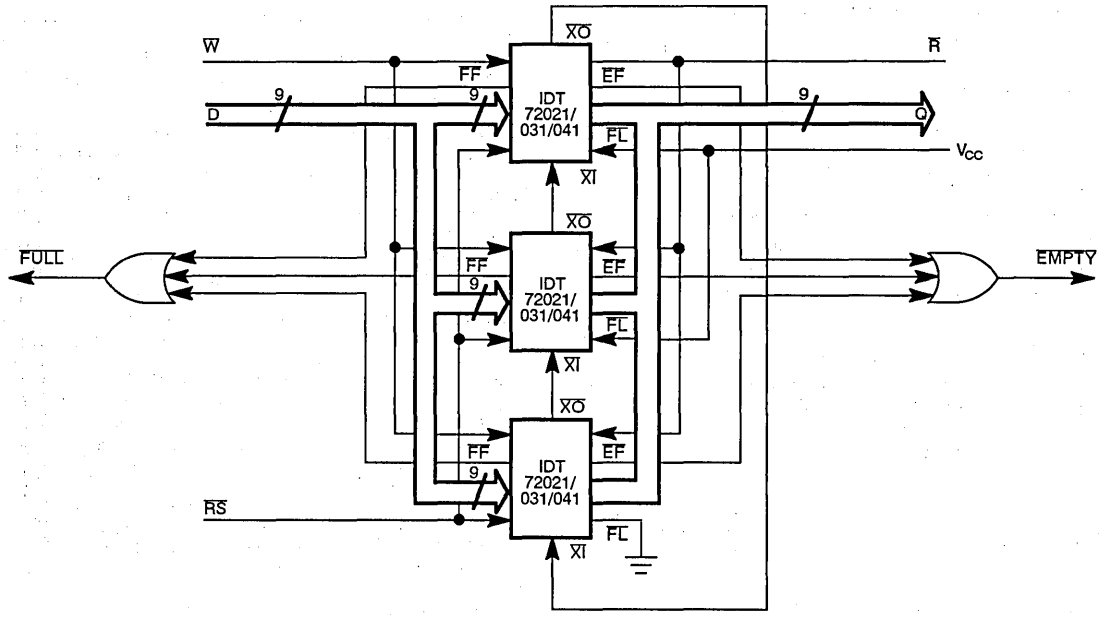
DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:

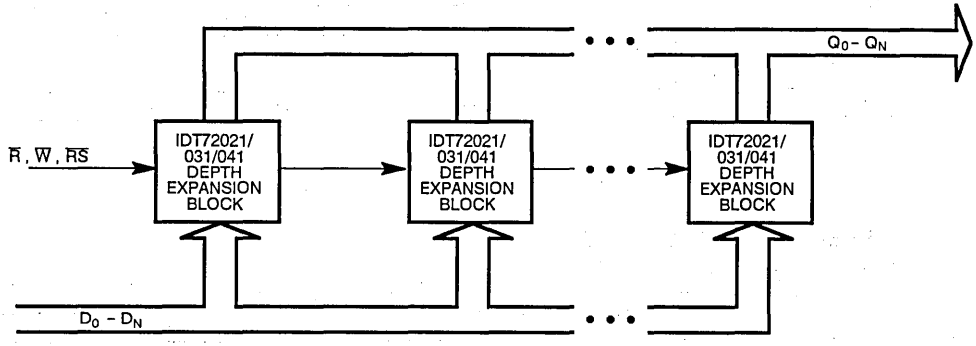
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 13.

$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output; $\overline{AEF}$ = Almost Empty/Almost Full Flag.



NOTE:
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

Figure 13. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 13.
2. For Flag detection see section on Width Expansion and Figure 12.

Figure 14. Compound FIFO Expansion

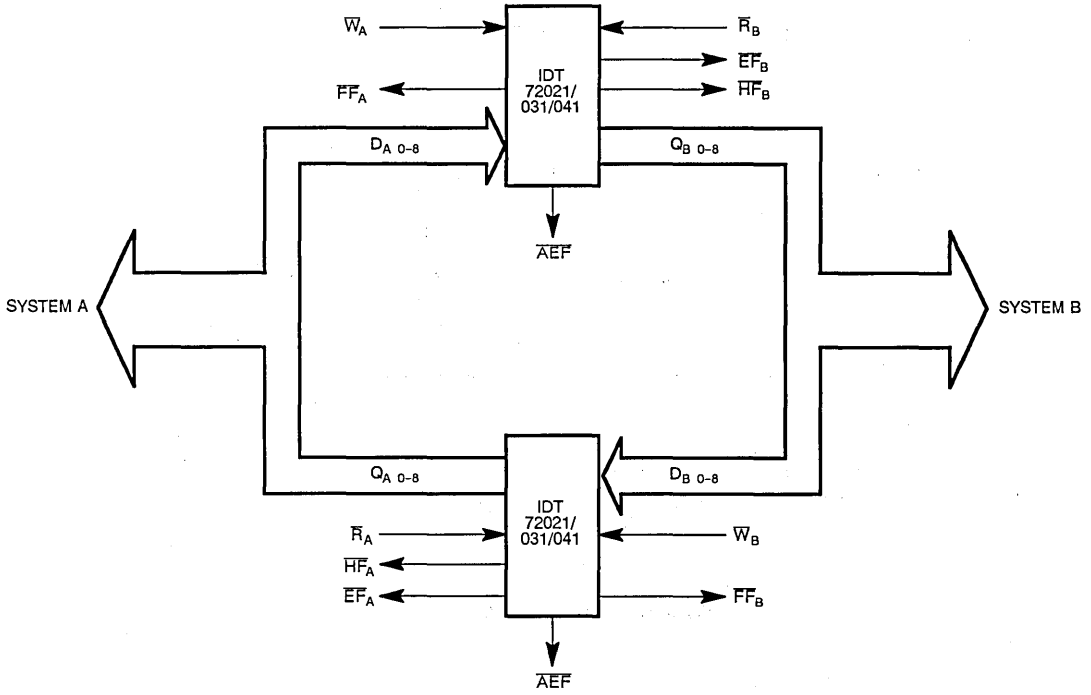


Figure 15. Bidirectional FIFO Mode

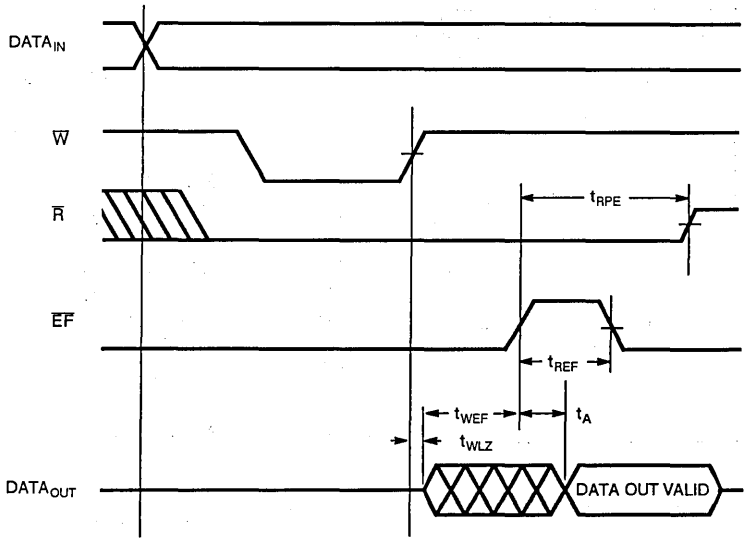


Figure 16. Read Data Flow-Through Mode

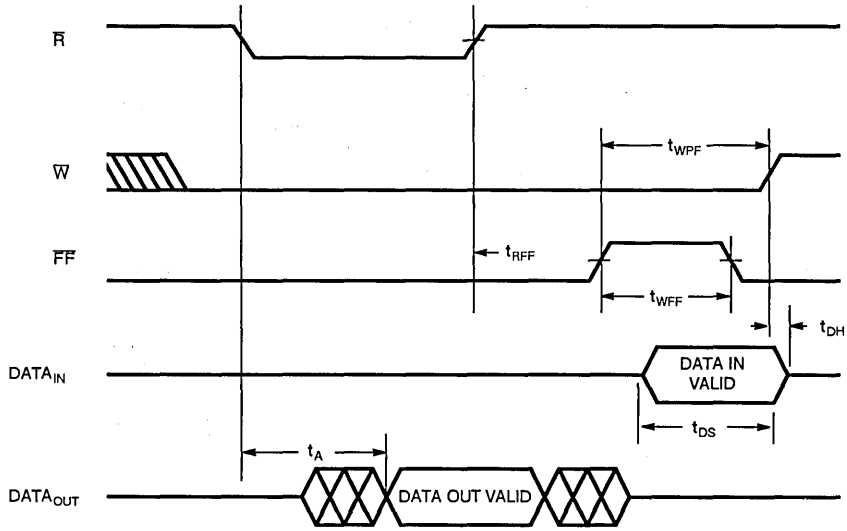
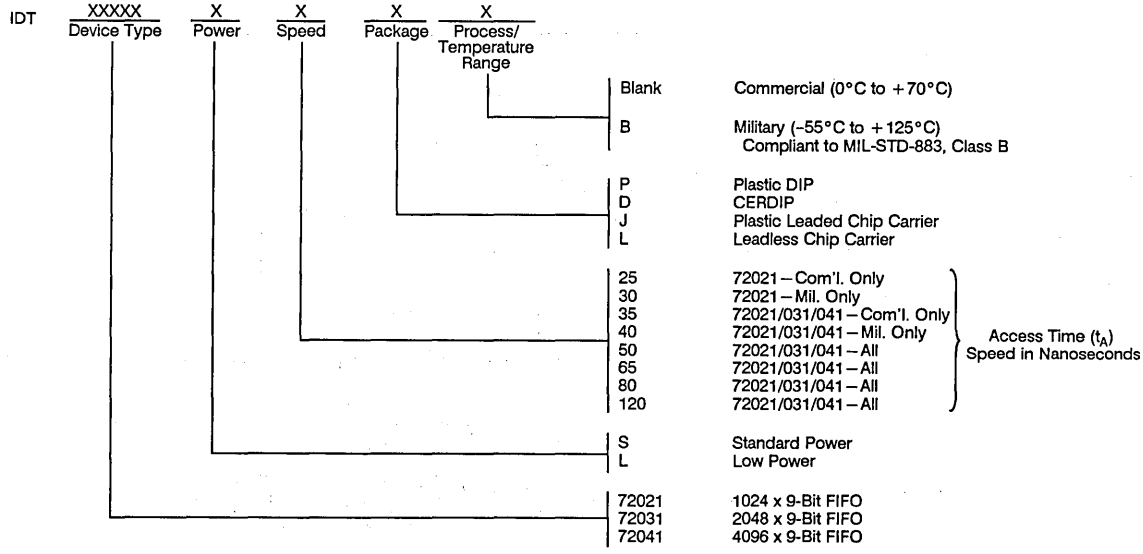


Figure 17. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT 7203S/L
IDT 7204S/L

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  - Active: 660mW (max.)
  - Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201A/7202A
- IDT7204 allows 4096 word structure without expansion
- Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in CERDIP, Plastic DIP, PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7203/7204 are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22.2MHz).

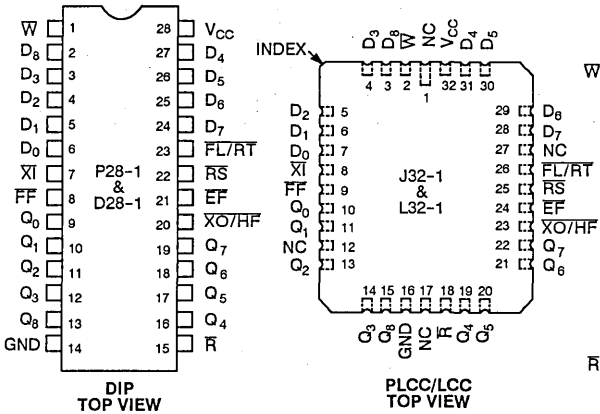
The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7203/7204 is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

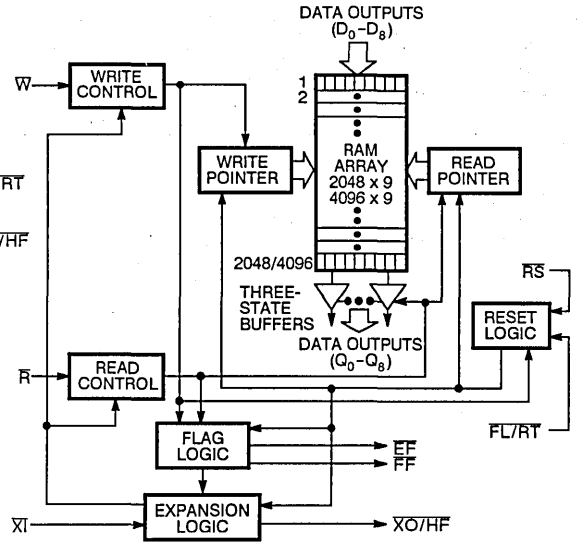
6

PIN CONFIGURATIONS



CONSULT FACTORY FOR CERPACK PINOUT

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL}(1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS – IDT7203/7204

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7203S/L IDT7204S/L COMMERCIAL t_A = 35, 50, 65 80, 120ns			IDT7203S/L IDT7204S/L MILITARY t_A = 40, 50, 65 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI}(1)	Input Leakage Current (Any Input)	-1	–	-1	-10	–	10	µA
I_{LO}(2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
I_{CC1}(3,4)	Active Power Supply Current	–	75	120	–	100	150	mA
I_{CC2}(3)	Average Standby Current, ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3}(L)(3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	2	–	–	4	µA
I_{CC3}(S)(3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	8	–	–	12	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.
4. The 35ns and 40ns I_{CC} measurements are made at 15.3 MHz.

AC ELECTRICAL CHARACTERISTICS – IDT7203/04 [1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		COMMERCIAL AND MILITARY								UNIT
		7203S/L35 7204S/L35		7203S/L40 7204S/L40		7203S/L50 7204S/L50		7203S/L65 7204S/L65		7203S/L80 7204S/L80		7203S/L120 7204S/L120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_s	Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width [2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z [3]	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z [3, 4]	10	–	10	–	5	–	5	–	5	–	5	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z [3]	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width [2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width [2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	Retransmit Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width [2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time [3]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	Write Low to Half- Full Flag Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read dataflow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

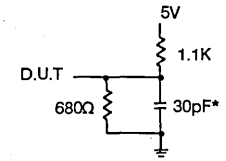


Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN} [3]	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} [2, 3]	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after master Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF FULL FLAG ($\overline{XO}/\overline{HF}$)

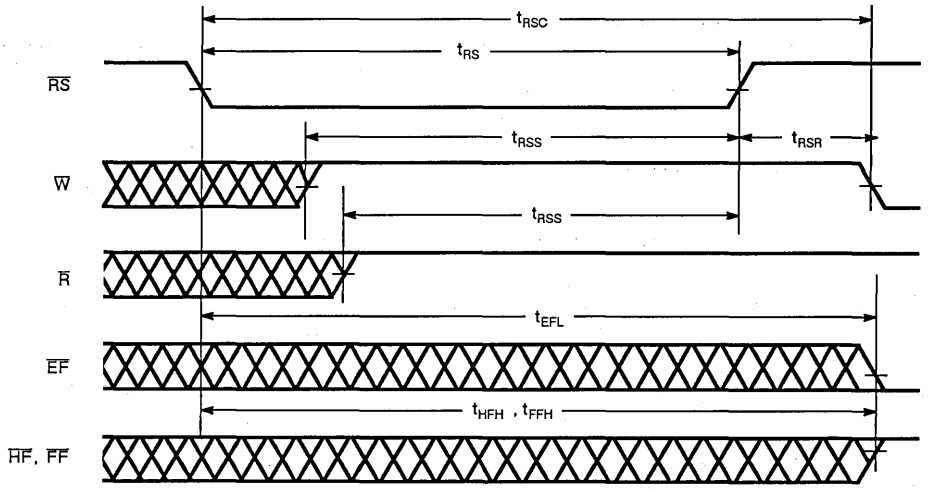
This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS ($Q_0 - Q_8$)

$Q_0 - Q_8$ are data outputs for 9-bit wide data. These output are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:

1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

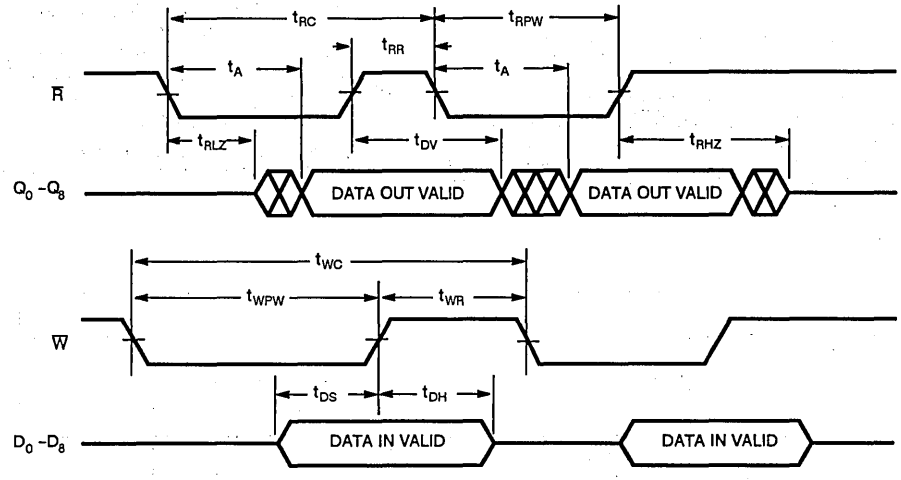


Figure 3. Asynchronous Write and Read Operation

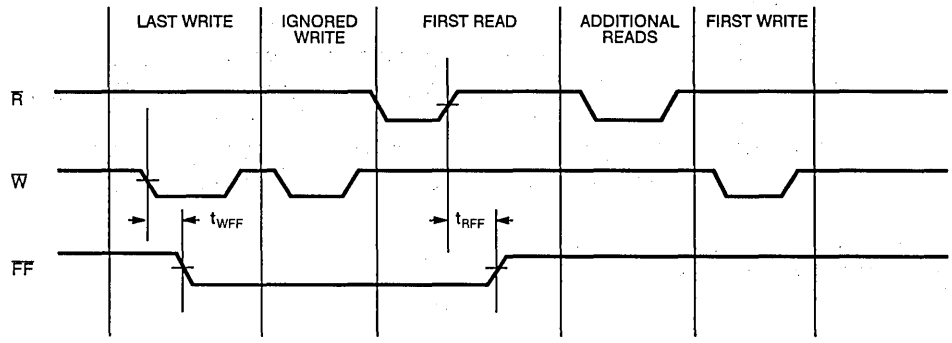


Figure 4. Full Flag From Last Write to First Read

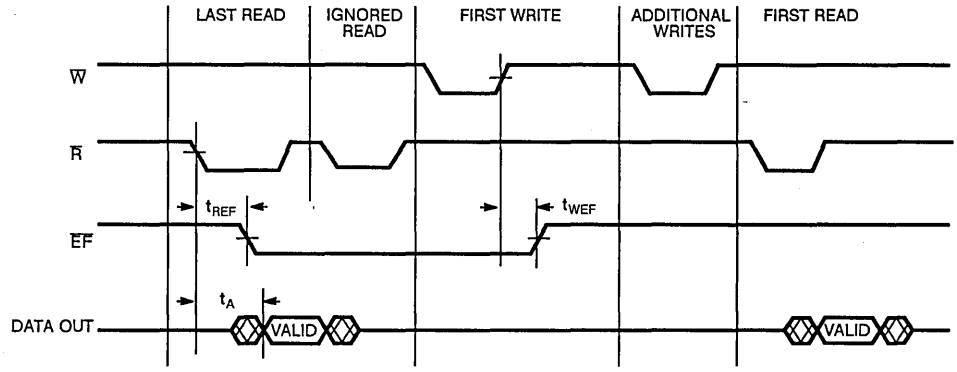
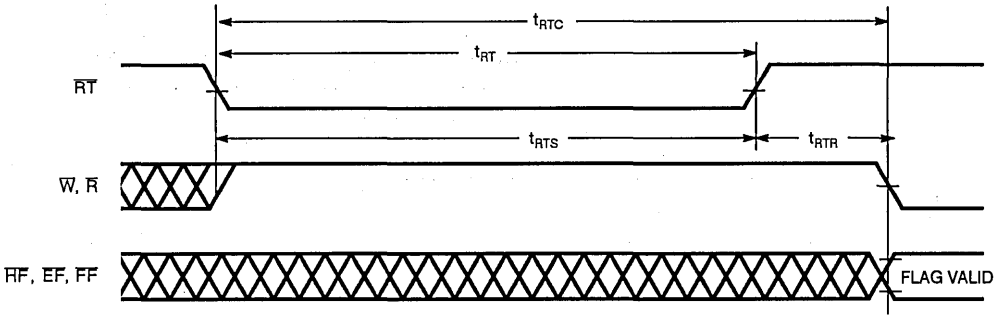


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

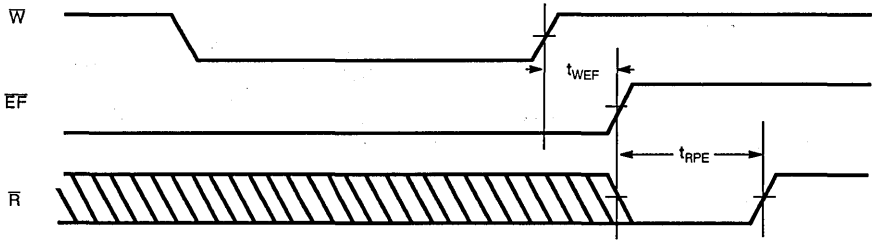


Figure 7. Empty Flag Timing

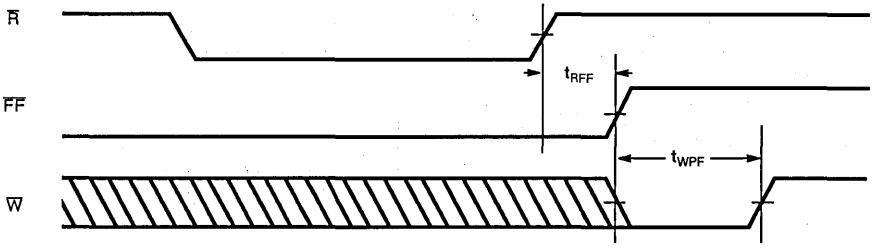


Figure 8. Full Flag Timing

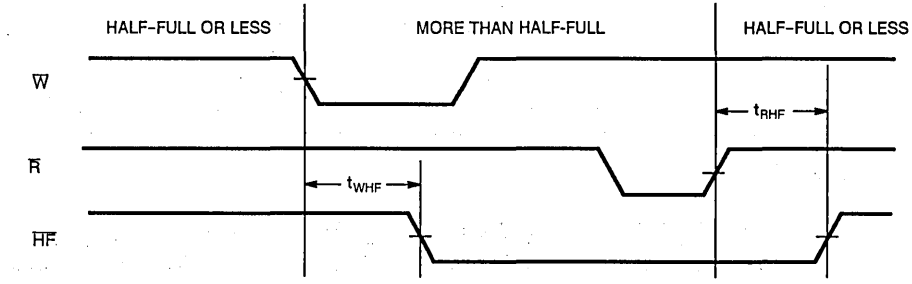


Figure 9. Half-Full Flag Timing

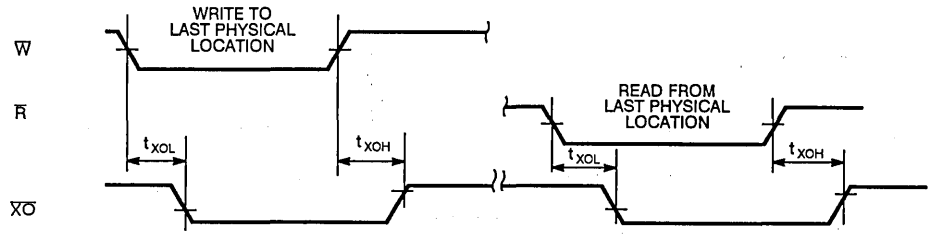


Figure 10. Expansion Out

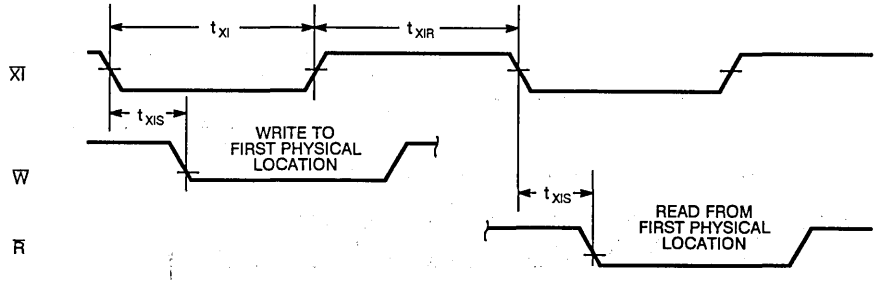


Figure 11. Expansion In

OPERATING MODES:

SINGLE DEVICE MODE

A single IDT7203/7204 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/7204 are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 10). In this mode, the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

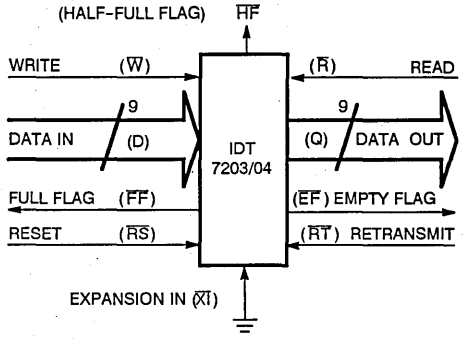
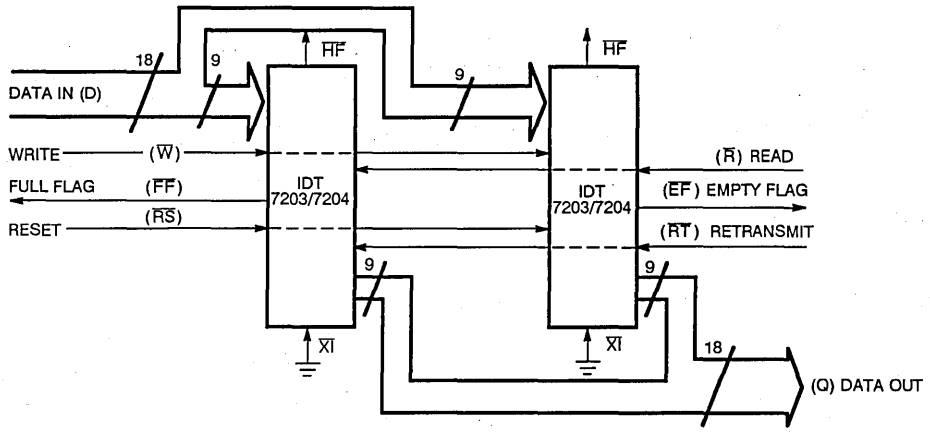


Figure 12. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204s. Any word width can be attained by adding additional IDT7203/7204s.



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7203/7204 can easily be adapted to applications when the requirements are for greater than 2048/4906 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204s. Any depth can be attained by adding additional IDT7203/7204. The IDT7203/7204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204s as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each systems (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES

TABLE I—RESET AND RETRANSMIT—

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE—

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.

$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

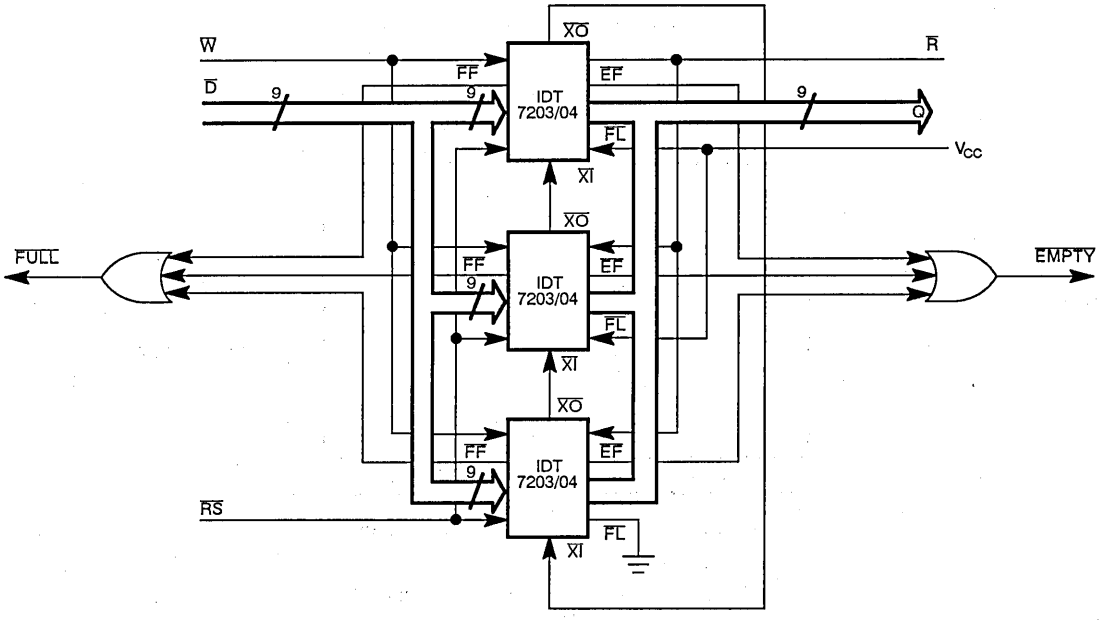
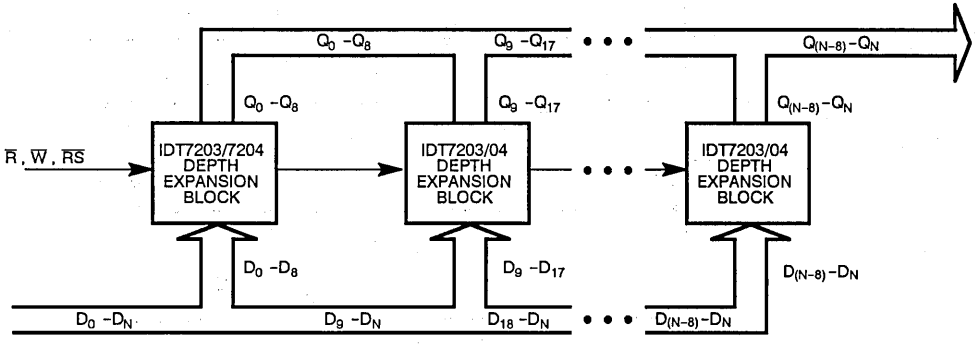


Figure 14. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

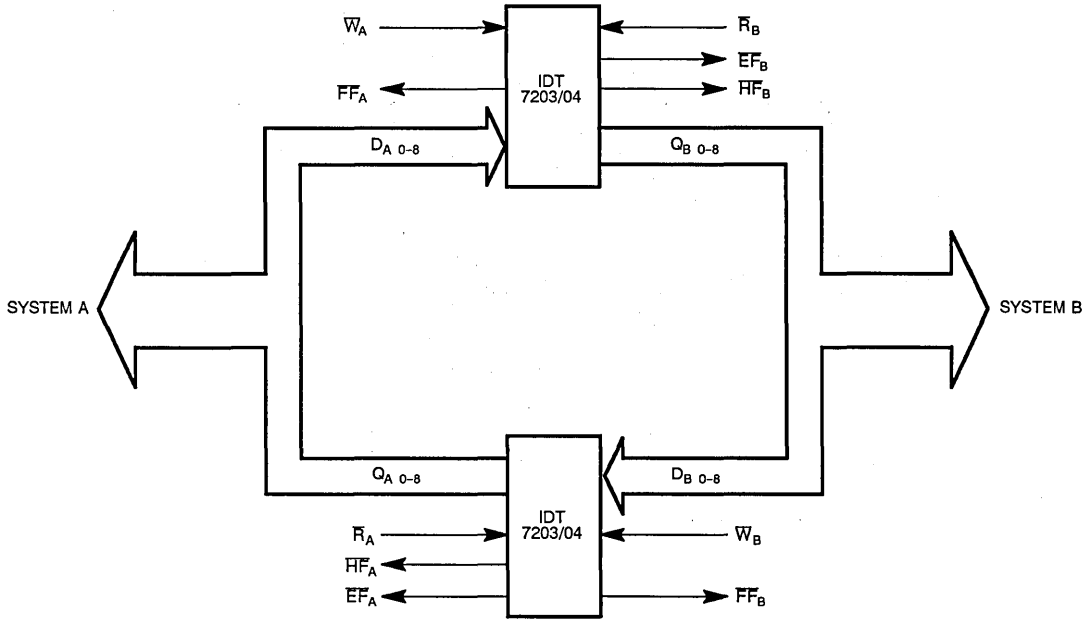


Figure 16. Bidirectional FIFO Mode

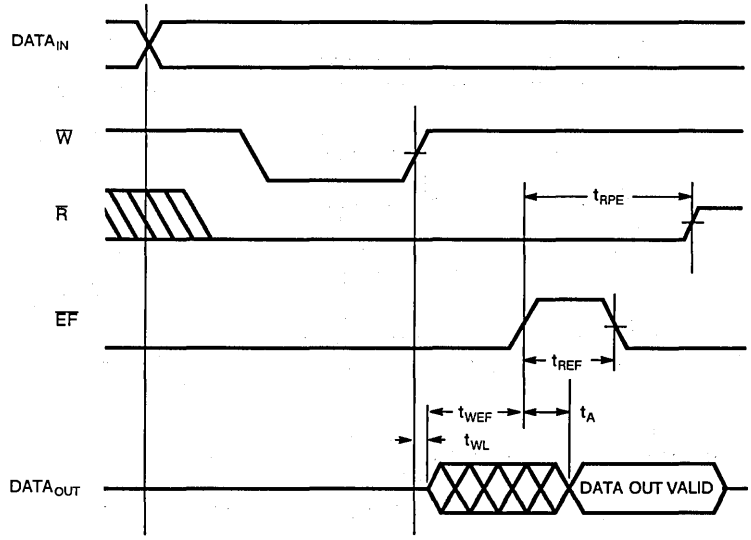


Figure 17. Read Data Flow-Through Mode

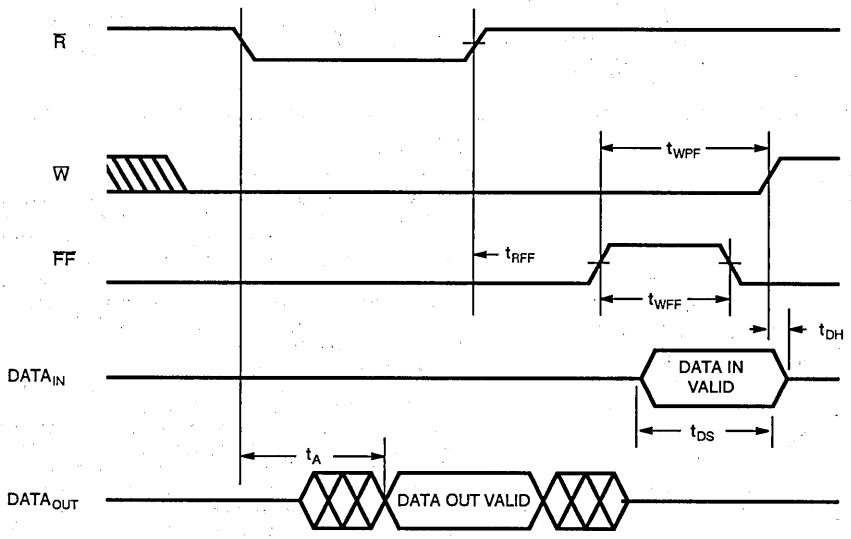


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT — XXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
XE	Cerpack
P	Plastic DIP
D	CERDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
35	Com'l Only
40	Mil Only
50	Access Time (t_A) Speed in Nanoseconds
65	
80	
120	
S	Standard Power
L	Low Power
7203	2048 x 9-Bit FIFO
7204	4096 x 9-Bit FIFO

Integrated Device Technology, Inc.

BiCMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 4K x 9-BIT

ADVANCE INFORMATION
IDT 72B04

FEATURES:

- First-In/First-Out dual-port memory
- 4K x 9-bit organization
- Low power consumption
- Ultra high speed: 15ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin-compatible with IDT7200/01/02/03/04 FIFO family
- Half-Full Flag capability in single device mode
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance submicron BiCEMOS ™ technology
- Available in 28-pin plastic DIP, CERDIP and 32-pin surface mount LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72B04 is a dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

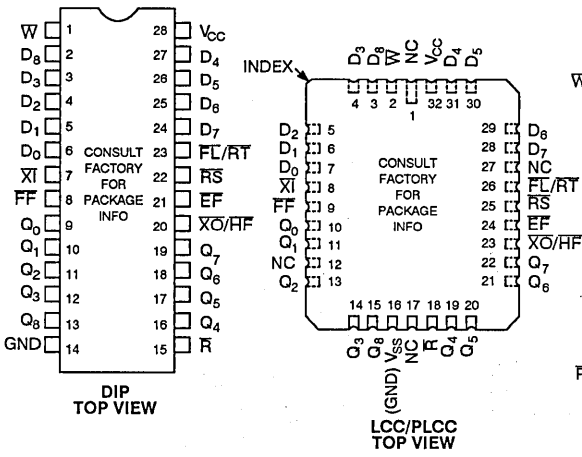
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 25ns (40MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low, to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT72B04 is fabricated using IDT's high-speed BiCEMOS sub-micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4K x 9 organization allows a 4096 deep word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

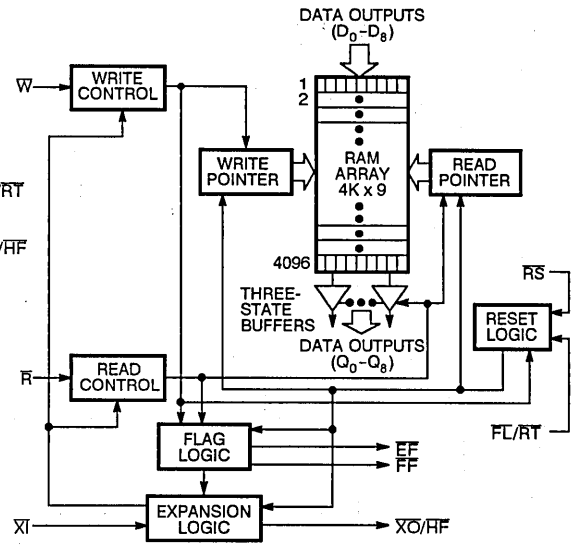
PIN CONFIGURATIONS



DIP
TOP VIEW

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 4K x 18-BIT & 8K x 18-BIT

ADVANCE INFORMATION
IDT 72045
IDT 72055

FEATURES:

- First-In/First-Out dual-port memory
- 4K x 18-bit & 8K x 18-bit organization
- Low power consumption
- Ultra high speed: 50ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Half-Full Flag capability in single device mode
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance submicron CEMOS™ technology
- Available in 48-pin plastic DIP, ceramic DIP and 52-pin surface mount LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72045 and IDT72055 are dual-port memory that utilizes a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

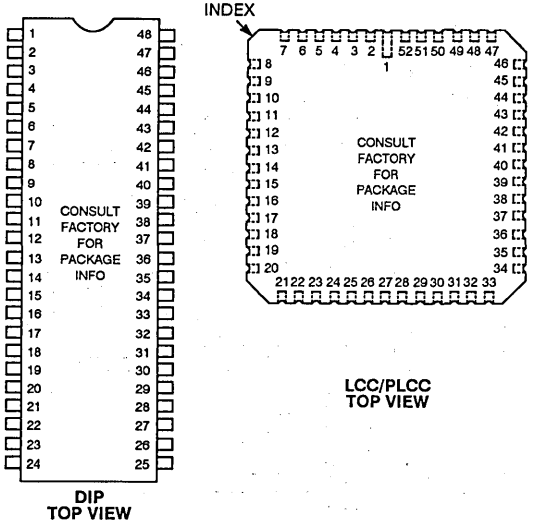
The device utilizes a 18-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low, to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT72045 and IDT72055 are fabricated using IDT's high-speed CEMOS sub-micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4K x 18 organization allows a 4096 deep word structure and the 8K x 18 allows an 8192 word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

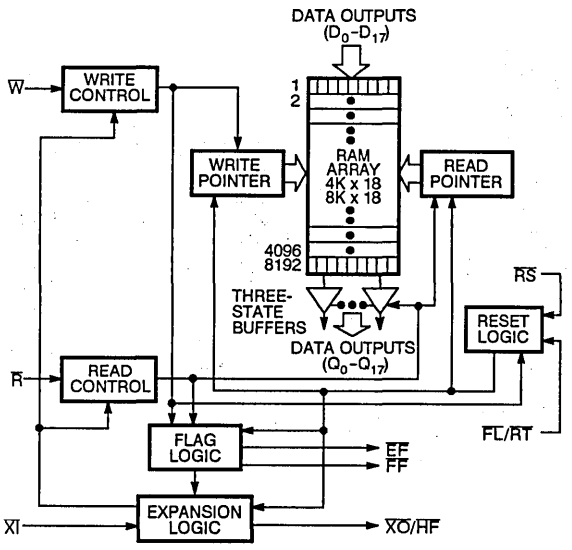
PIN CONFIGURATIONS



DIP
TOP VIEW

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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DSC-2034/-

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 8K x 9-BIT & 16K x 9-BIT

ADVANCE INFORMATION
IDT 7205
IDT 7206

FEATURES:

- First-In/First-Out dual-port memory
- 8K x 9-bit & 16K x 9-bit organization
- Low power consumption
- Ultra high speed: 50ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin-compatible with IDT7200/01/02/03/04 FIFO family
- Half-Full Flag capability in single device mode
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance submicron CEMOS™ technology
- Available in 28-pin plastic DIP, CERDIP and 32-pin surface mount LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7205 and IDT7206 are memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

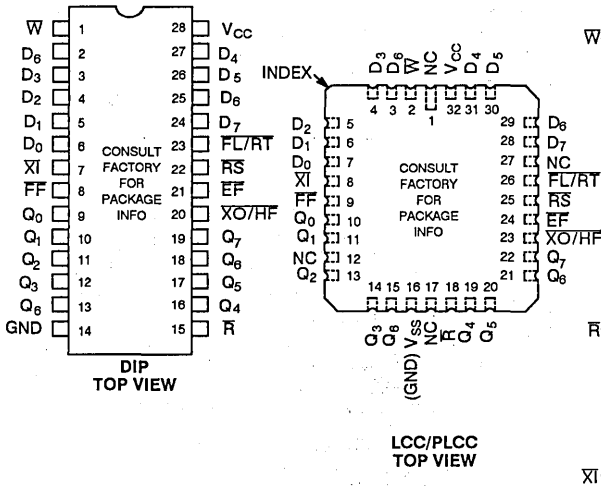
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position, when $\overline{RT}$ is pulsed low, to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7205 and IDT7206 are fabricated using IDT's high-speed CEMOS submicron technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 8K x 9 organization allows a 8192 deep word structure and the 16 x 9 allows a 16384 word structure without the need for expansion.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

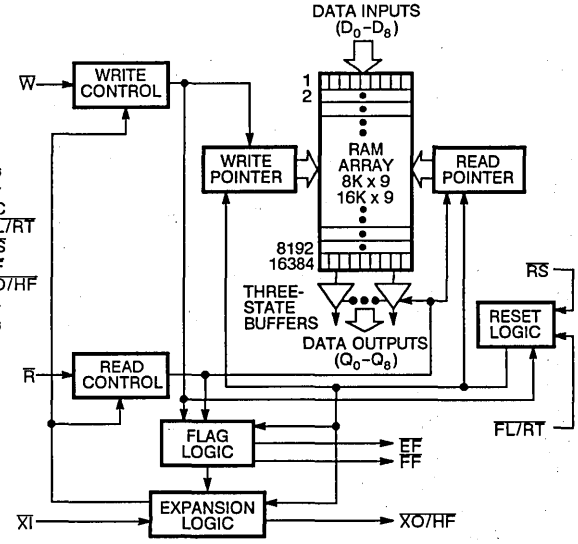
PIN CONFIGURATIONS



DIP
TOP VIEW

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT 72103
IDT 72104

FEATURES:

- 35ns parallel port access time
- 50MHz serial input/output port frequency
- Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel operations
- Easily expandable in depth and width
- Programmable wordlengths from 4 bits to any bit width using Flexishift™ for serial operations without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Full-Minus-One, Empty, Almost-Empty (1/8 from empty), Empty-Plus-One and Half-Full
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Output enable control provided for parallel output port
- Retransmit capability in single device mode
- High-performance CEMOS™ technology
- Available in 40-pin ceramic and plastic DIP, 44-pin LCC and J-Leaded PLCC
- Military product compliant to MIL-STD-883, Class B

APPLICATIONS:

- High-Speed Data Acquisition Systems
- Local Area Network Buffers
- Remote Telemetry Buffers
- Serial Link Buffers
- High-Speed Parallel Bus-to-Bus Serial Communications
- Magnetic Media Controllers
- Single Chip Video Frame Buffers
- FAX/Printer Buffers

DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs that are ideally suited for serial communications, high-density media storage and local area networks.

The devices have four ports: two 9-bit parallel ports and the other two for serial input and serial output. A variety of operations can be performed: Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel. The Parallel-Serial FIFOs can expand in depth or width for any of these modes.

A unique feature that enhances the bandwidth is the handling of serial wordlengths that are not a multiple of 9. The IDT72103/72104 can be configured to handle serial wordlengths from 4 bits to words of any length using multiple devices. This feature is provided without using any additional ICs. For example, a user can configure a 4K x 24 FIFO by using three devices to generate internal increments to the read/write pointers every 24 cycles.

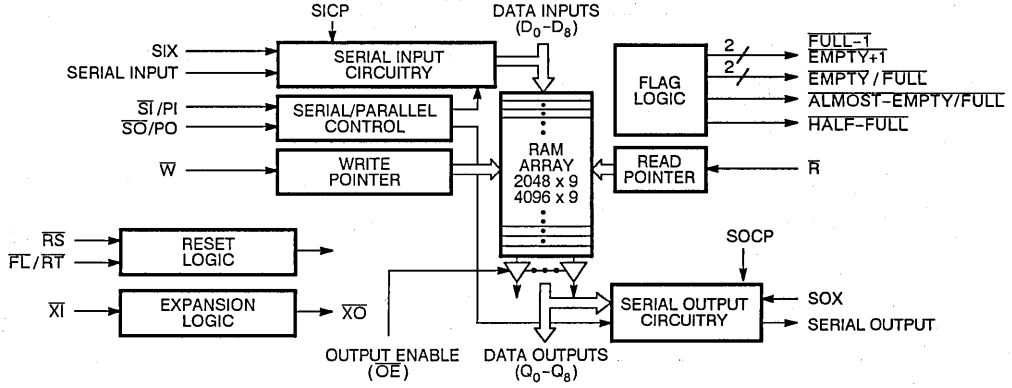
A number of flags are provided to monitor the status of the FIFO. These include Full, Almost-Full (when the FIFO is more than 7/8 full), Full-Minus-One (when the FIFO has one or zero locations left), Empty, Almost-Empty (when the FIFO is less than 1/8 full), Empty-Plus-One (when there is only one or zero samples left in the FIFO) and Half-Full.

Read and Write controls are provided to permit asynchronous and simultaneous operations. An Output Enable control is provided on the parallel output port. Expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/72104 are manufactured using IDT's CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM



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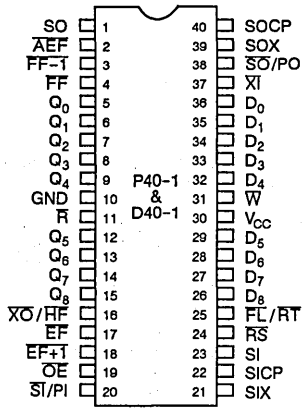
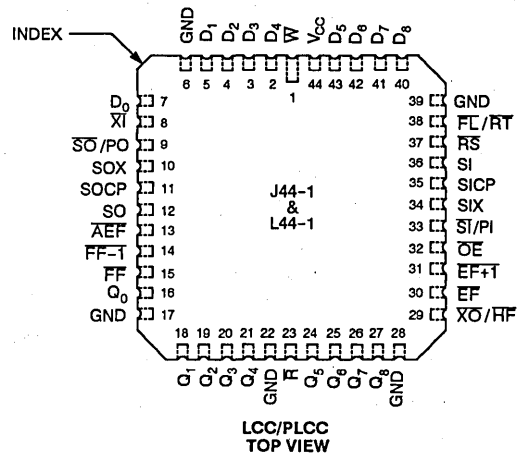
PIN CONFIGURATION



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC}= 5V ±10%, T_A= 0°C to +70°C; Military: V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	IDT72103/IDT72104 COMMERCIAL MIN.	TYP.	MAX.	IDT72103/IDT72104 MILITARY MIN.	TYP.	MAX.	UNIT
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA (5)	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA (6)	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	–	100	160	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current	–	–	8	–	–	12	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{W}$ = $\overline{R}$ = V_{CC} -0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V
5. For SO, I_{OUT} = -8mA.
6. For SO, I_{OUT} = 16mA

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COM'L.		MILITARY		MILITARY AND COMMERCIAL								UNIT
			72103x35 72103x35 MIN.	MAX.	72103x40 72103x40 MIN.	MAX.	72103x50 72104x50 MIN.	MAX.	72103x65 72104x65 MIN.	MAX.	72103x80 72104x80 MIN.	MAX.	72103x120 72104x120 MIN.	MAX.	
f_S	Parallel I/O Shift Frequency	–	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
f_{SOCP}	Serial-Out Shift Frequency	–	–	50	–	50	–	40	–	33	–	28	–	25	MHz
f_{SICP}	Serial-In Shift Frequency	–	–	50	–	50	–	40	–	33	–	28	–	25	MHz
PARALLEL-OUTPUT MODE TIMINGS															
t_A	Access Time	23	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	23	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width	23	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RC}	Read Cycle Time	23	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z[1]	1	5	–	5	–	15	–	15	–	20	–	20	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	23	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	23	–	20	–	25	–	30	–	30	–	35	–	35	ns
t_{DV}	Data Valid from Read Pulse High	23	5	–	5	–	5	–	5	–	5	–	5	–	ns
PARALLEL INPUT MODE TIMINGS															
t_{DS}	Data Set-up Time	24	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	24	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{WC}	Write Cycle Time	24	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width	24	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	24	10	–	10	–	15	–	15	–	20	–	20	–	ns
RESET TIMINGS															
t_{RSC}	Reset Cycle Time	18	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width	18	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	18	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	18	10	–	10	–	15	–	15	–	20	–	20	–	ns
RESET TO FLAGS DELAYS															
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$ and $\overline{EF+1}$ Low	18	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$ and $\overline{FF-1}$ High	18	–	45	–	50	–	65	–	80	–	100	–	140	ns
RESET TO TIME DELAYED OUTPUTS—SERIAL MODE ONLY															
t_{RSQL}	Reset Going Low to Q_{0-8} Low	–	20	–	20	–	35	–	50	–	65	–	105	–	ns
t_{RSQH}	Reset Going High to Q_{0-8} High	–	20	–	20	–	35	–	50	–	65	–	105	–	ns
t_{RSDL}	Reset Going Low to D_{0-8} Low	–	20	–	20	–	35	–	50	–	65	–	105	–	ns
RETRANSMIT TIMINGS															
t_{RTC}	Retransmit Cycle Time	19	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width	19	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	19	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	19	10	–	10	–	15	–	15	–	20	–	20	–	ns
PARALLEL MODE FLAG PROPAGATION DELAYS															
t_{REF}	Read Low to $\overline{EF}$ Low	25	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to $\overline{FF}$ High	26	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	27	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	28	–	45	–	45	–	65	–	80	–	100	–	140	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	1	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to $\overline{EF}$ High	25	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	26	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	27	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	28	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	2	35	–	40	–	50	–	65	–	80	–	120	–	ns

6

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COM'L.		MILITARY		MILITARY AND COMMERCIAL								UNIT
			72103x35 72103x35 MIN.	MAX.	72103x40 72103x40 MIN.	MAX.	72103x50 72104x50 MIN.	MAX.	72103x65 72104x65 MIN.	MAX.	72103x80 72104x80 MIN.	MAX.	72103x120 72104x120 MIN.	MAX.	
DEPTH EXPANSION MODE DELAYS															
t_{XOL}	Read/Write to $\overline{XO}$ Low	20	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	20	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	21	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	21	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	21	15	–	15	–	15	–	15	–	15	–	15	–	ns
SERIAL INPUT MODE TIMINGS															
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	30	12	–	12	–	15	–	15	–	20	–	20	–	ns
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	30	0	–	0	–	0	–	0	–	5	–	5	–	ns
t_{S3}	SIX Set-up Time to SICP Rising Edge	30	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	30	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	30	7	–	7	–	7	–	10	–	12	–	15	–	ns
t_{SICW}	Serial In Clock Width High/Low	30	8	–	8	–	10	–	10	–	15	–	15	–	ns
t_{S5}	$\overline{SI}$/PI Set-up Time to SICP Rising Edge	30	35	–	40	–	50	–	65	–	80	–	120	–	ns
SERIAL OUTPUT MODE TIMINGS															
t_{S6}	$\overline{SO}$/PO Set-up Time to SOCP Rising Edge	29	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{S7}	SOX Set-up Time to SOCP Rising Edge	29	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	29	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	29	7	–	7	–	7	–	10	–	12	–	15	–	ns
t_{SOCW}	Serial Out Clock Width High/Low	29	8	–	8	–	10	–	10	–	15	–	15	–	ns
SERIAL MODE RECOVERY TIMINGS															
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ Goes High	32	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{REFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	32	15	–	15	–	15	–	15	–	20	–	20	–	ns
SERIAL MODE FLAG PROPAGATION DELAYS															
t_{SOCEF}	SOCP Rising Edge (Bit 0 - First Word) to $\overline{EF}$ Low	32	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{SOCFF}	SOCP Rising Edge (Bit 0 - First Word) to $\overline{FF}$ High	31	–	30	–	35	–	40	–	50	–	60	–	60	ns
t_{SOCF}	SOCP Rising Edge (Bit 0 - Second Word) to $\overline{FF}$-1, HF, $\overline{AEF}$, $\overline{EF}$+1 High	31	–	30	–	35	–	40	–	50	–	60	–	60	ns
t_{SICEF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{EF}$ High	34	–	45	–	50	–	65	–	80	–	80	–	80	ns
t_{SICFF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{FF}$ Low	34	–	30	–	35	–	40	–	50	–	60	–	60	ns
t_{SICF}	SICP Rising Edge (Bit 0 - Second Word) to $\overline{EF}$+1, HF, $\overline{AEF}$, $\overline{FF}$-1 High	33	–	45	–	50	–	65	–	80	–	80	–	80	ns
SERIAL INPUT MODE DELAYS															
t_{PD1}	SICP Rising Edge to D (1)	30	5	17	5	17	5	20	5	25	5	30	5	35	ns
SERIAL OUTPUT MODE DELAYS															
t_{PD2}	SOCP Rising Edge to Q(1)	29	5	17	5	17	5	20	5	25	5	30	5	30	ns
t_{SOHZ}	SOCP Rising Edge to SO at High-Z(1)	29	5	16	5	16	5	16	5	20	5	25	5	30	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z (1)	29	5	22	5	22	5	22	5	22	5	30	5	35	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	29	–	18	–	18	–	18	–	22	–	30	–	35	ns
OUTPUT ENABLE/DISABLE DELAYS															
t_{OEHZ}	Output Enable to High-Z (Disable) (1)	22	–	16	–	16	–	16	–	20	–	25	–	30	ns
t_{OELZ}	Output Enable to Low-Z (Enable) (1)	22	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	22	–	20	–	20	–	22	–	25	–	30	–	35	ns

NOTE:

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

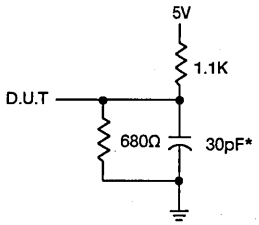


Figure A. Output Load.

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

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GENERAL SIGNAL DESCRIPTIONS:

Inputs:

Data Inputs (D_0-D_8)

In the parallel-in mode ($\overline{SI}$/PI is connected to V_{CC}) D_0-D_8 are the data inputs.

The serial input mode is selected by grounding the $\overline{SI}$/PI pin. The D_{0-8} lines are then outputs which are used to program the width of the serial word.

Reset ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input goes high-to-low. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be high during reset. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of Write if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of Write ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of Read ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read ($\overline{R}$) goes high, the Data Outputs (Q_{0-8}) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Multiple Device mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). In the Single Device mode, this pin acts as the retransmit input. The Single Device mode is initiated by grounding Expansion In ($\overline{XI}$).

The IDT72103/4 can be made to retransmit data when the Retransmit ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read ($\overline{R}$) and Write ($\overline{W}$) must be high during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not available in the Depth Expansion mode and will affect Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the Single Device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

Output Enable ($\overline{OE}$)

The parallel output buffers are tri-stated when $\overline{OE}$ is high.

Outputs:

Data Outputs (Q_0-Q_8)

Data outputs for 9-bit wide data. These outputs are in a high impedance condition wherever Read ($\overline{R}$) is in a high state.

Full Flag ($\overline{FF}$)

Full Flag ($\overline{FF}$) is asserted (LOW) when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by additional write pulses.

Serial-In Mode

When the FIFO is loaded serially, the Serial-In Clock (SICP) asserts the Full Flag. On the second rising edge of SICP, for the last word in the FIFO, the Full Flag is asserted (LOW) and is only deasserted by a subsequent read operation. Note that when the $\overline{FF}$ is asserted, the last SICP for that word will have to be stretched as shown in Figure 33; otherwise, the data may be scrambled in the next write cycle after a word has been read from the FIFO.

Parallel-In Mode

When the FIFO is in Parallel-In mode, the falling edge of Write asserts the Full Flag (LOW). The Full Flag is deasserted (HIGH) by subsequent read operations—either serial or parallel.

Full-1 Flag ($\overline{FF-1}$)

This flag is asserted (LOW) when the FIFO is one word away from being full. It remains asserted when the FIFO is full.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory. After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Multiple Device mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

Almost-Empty or Almost-Full Flag ($\overline{AEF}$)

This flag is asserted (LOW) if there are 0-255 bytes or 1793-2048 bytes in the IDT72103, 2K x 9 FIFO; it is asserted if there are 0-511 or 3585-4096 bytes in the IDT72104, 4K x 9 FIFO.

Empty+1 Flag ($\overline{EF+1}$)

In the parallel output mode, this flag is asserted (LOW) when there is one word or less in the FIFO. It remains LOW when the FIFO is empty.

When in the serial mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ Flag. The $\overline{EF+1}$ goes LOW when the second to the last word is read from the RAM and is ready to be shifted out. The next word to be read is the next to the last word.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO		$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF+1}$[1]	$\overline{EF}$
2K	4K						
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1024	512-2048	H	H	H	H	H	H
1025-1792	2049-3584	H	H	H	L	H	H
1793-2046	3585-4094	H	H	L	L	H	H
2047	4095	H	L	L	L	H	H
2048	4096	L	L	L	L	H	H

NOTE:
1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

Empty Flag

Parallel-Out Mode

When the FIFO is in the Parallel-Out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line causes the Empty Flag ($\overline{EF}$) line to be asserted (LOW). This is shown in Figure 25. The empty flag is then deasserted (HIGH) by either the rising edge of $\overline{W}$ or rising edge of SICP, as shown in Figure 25.

Serial-Out Mode

The use of the Empty Flag ($\overline{EF}$) is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted LOW after the first bit of the last word is shifted out. The $\overline{EF}$ flag is brought HIGH at the end of the next write ($\overline{W}$ goes from LOW-to-HIGH). In order to meet internal set-up times, the $\overline{EF}$ flag must be HIGH for a minimum period of time (t_{REFSO}) before the first shift out of the next word. This is analogous to the read flow-through mode in parallel output operation.

For continuous shifting at the highest clock rates, certain considerations apply. If the $\overline{EF}$ goes LOW during the serial shift of a word, it must be HIGH at least one or two serial clocks before the first bit of the next word is started. Otherwise, the clock must be stopped until $\overline{EF}$ has gone HIGH and the minimum set-up period is met. For continuous operation, the $\overline{EF}$ must be tested two clock cycles from the end of the serial word. For slower shift rates, the $\overline{EF}$ can be tested just before starting to shift the first bit of the next word.

SERIAL SIGNAL DESCRIPTIONS:

Serial Input (SI)

Serial data is read into the serial input register via the Serial Input. In both Depth and Serial Word Width Expansion modes, the Serial Input signals of the different IDT72103/4 devices in the expansion array are connected together.

Serial Output (SO)

Serial data is output on the serial output pin. In both Depth and Serial Word Width Expansion modes the Serial Output signals of the different IDT72103/4 devices in the expansion array are connected together. Following reset, the serial output is tri-stated until the first positive edge of the serial output clock signal. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode, the serial output is tri-stated again after the ninth bit is output.

Serial Input Clock (SICP)

New serial data is read into the serial input register on the rising edge of the Serial Input Clock signal. In both Depth and Serial Word Width Expansion modes, the Serial Input Clock signals of the different IDT72103/4 devices in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of Serial Output Clock signal. In both Depth and Serial Word Width Expansion modes, the Serial Output Clock signals of the different IDT72103/4 parts in the expansion array are connected together.

Serial Input Expansion (SIX)

The Serial Input Expansion pin is tied high for single-device serial-input operation or parallel input operation. In the Serial Input Expansion mode, the SIX pin is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SIX pin (or pins) tied to the D_8 pin of the device that will source the next lower order bits of the serial word.

Serial Output Expansion (SOX)

The Serial Output Expansion pin is tied high for single-device serial-output operation or parallel output operation. In the Serial Output Expansion mode, SOX is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SOX pin (or pins) tied to the Q_8 pin of the device that will source the next lower order bits of the serial word. Data is clocked out Least Significant Bit first.

Serial/Parallel Input ($\overline{SI}$/PI)

The Serial/Parallel Input pin programs whether the IDT72103/4 accepts parallel or serial data as input. When this pin is low, the FIFO expects serial data and the D_0-D_8 pins become outputs used to program the write signal and, therefore, program the serial input word width. For instance, connecting D_8 to $\overline{W}$ will program a serial word width of 7 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The Serial/Parallel Output pin programs whether the IDT72103/4 outputs parallel or serial data. When this pin is low, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to program the read signal and, therefore, program the serial output word width.

Operating the IDT72103/4 FIFO Full and Empty Boundary Conditions

The design of the IDT72103/4 FIFOs gates out write pulses once the FIFO is full and gates out read pulses once the FIFO is empty. Excess writes are ignored and, thus, do not overwrite valid data. Excess reads produce invalid data since the outputs of the FIFO are tri-stated when the Empty Flag is asserted, but but do not read data bytes out of sequence.

The Full and Empty flags signal the full and empty boundary conditions. An internal read cycle cannot begin until the Empty Flag is deasserted and a write cannot begin until the Full Flag is deasserted (Figures 1 and 2).

If Read is low prior to the deassertion of the Empty Flag, or Write is low prior to the deassertion of the Full Flag, they cannot be allowed to go high again until an appropriate minimum read or write pulse time has elapsed (Figure 1—t_{RPE} and Figure 2—t_{WPF}). Failure to observe this boundary condition timing produces internal read and write pulses of excessively short duration and may result in erratic operation.

The parallel outputs are tri-stated unless the Read signal ($\overline{R}$) is low, Output Enable ($\overline{OE}$) is low and the Empty Flag ($\overline{EF}$) is deasserted (HIGH).

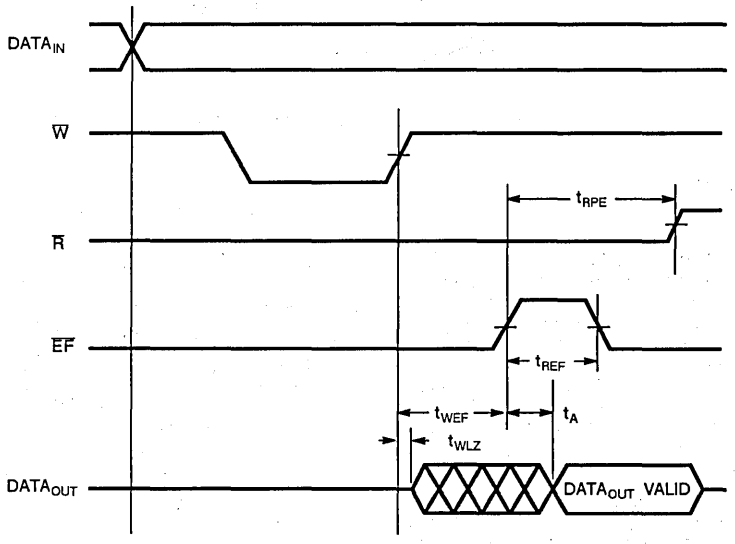


Figure 1. FIFO Empty Boundary Condition Timing

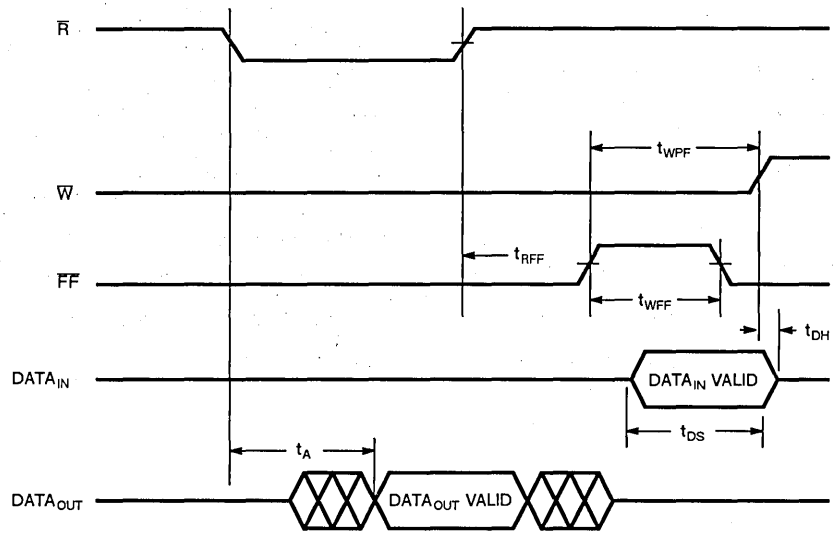


Figure 2. FIFO Full Boundary Condition Timing

Parallel Operating Modes:

Parallel Data Input

By setting SI/PI HIGH, the data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Parallel Data Output

By setting SO/PO HIGH, the Parallel-Out mode is chosen. A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. In the Parallel-Out mode, as shown in Figure 23 the data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$. The enable and disable times for Output Enable are shown in Figure 22.

Single Device Mode

A single IDT72103/4 may be used when the application requirements are for 2048/4096 words or less. The IDT72103/4 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. (See Figure 3.) In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

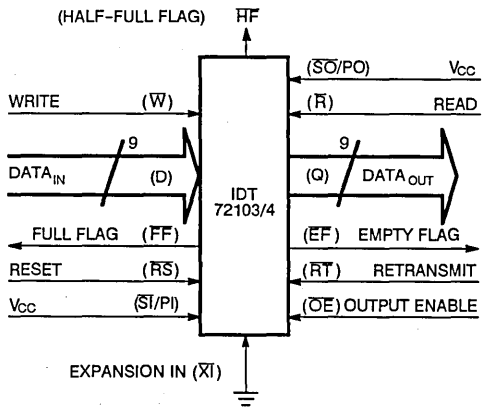
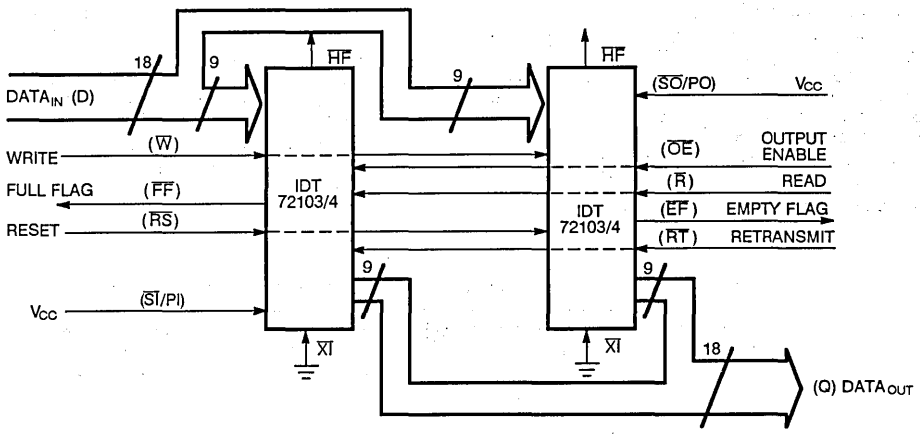


Figure 3. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one device. Figure 4 demonstrates an 18-bit word width by using two IDT72103/4s. Any word width can be attained by adding additional IDT72103/4s.



NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

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Figure 4. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT – SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$	$\overline{FF}$, $\overline{FF-1}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE – DEPTH EXPANSION/COMPOUND EXPANSION MODE

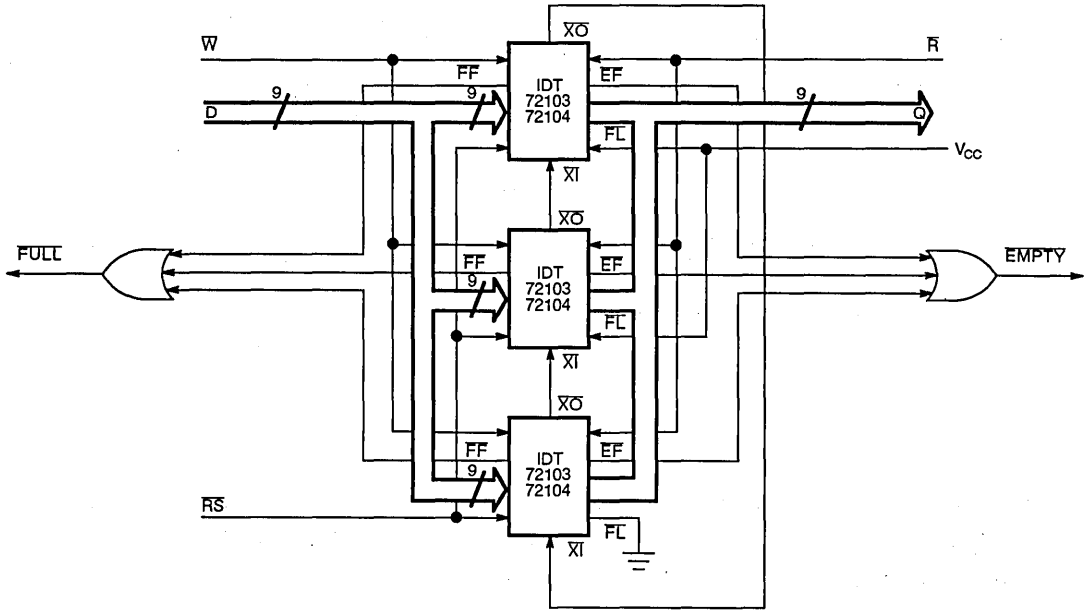
MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input

Depth Expansion (Daisy Chain) Mode

The IDT72103/4 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 5 demonstrates Depth Expansion using three IDT72103/4s. Any depth can be attained by adding additional IDT72103/4s. The IDT72103/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 5.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 5.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.



NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to V_{CC}.

Figure 5. Block Diagram of 6,144 x 9/12,288 x 9-FIFO Memory, Depth Expansion

Bidirectional Mode

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/4 as shown in Figure 6. Both Depth Expansion and Width Expansion may be used in this mode.

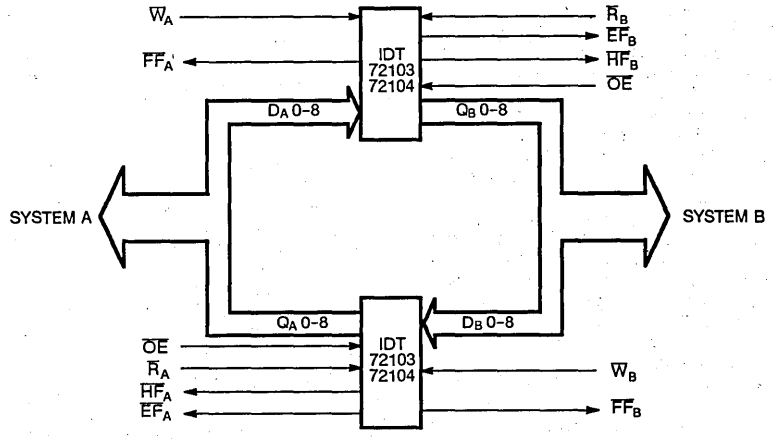
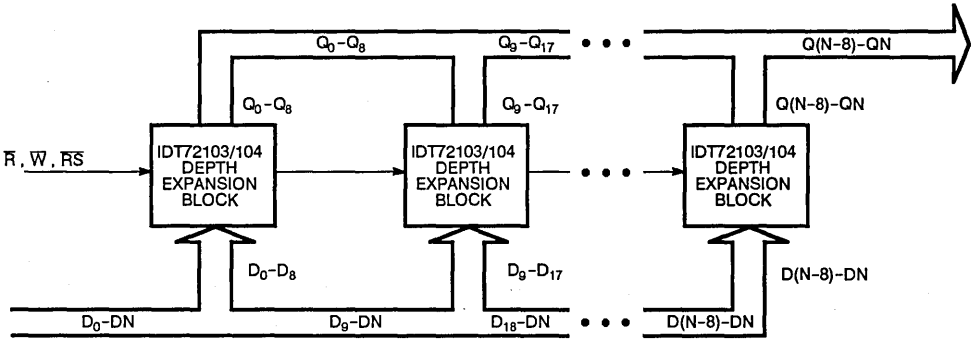


Figure 6. Bidirectional FIFO Mode

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 7).



NOTES:

1. For depth expansion block see DEPTH EXPANSION Section and Figure 5.
2. For Flag detection see WIDTH EXPANSION Section and Figure 4.

Figure 7. Compound FIFO Expansion

Serial Operating Modes

Serial Data Input

The Serial Input mode is selected by grounding the $\overline{SI}$/PI line. The D_{0-8} lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which are meant for connection to the $\overline{W}$ input. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits, connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D_8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D_8 of the next least significant device.

Figure 8 shows the relationship of the SIX, SICP and D_{0-8} lines. In the standalone case (Figure 8), on the first LOW-to-HIGH of SICP, the D_{1-7} lines go LOW and the D_0 line remains HIGH. On the next SICP clock edge, the D_1 goes HIGH, then D_2 and so on. This continues until the D line, which is connected to $\overline{W}$, goes HIGH. On the next clock cycle, after $\overline{W}$ is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D_0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D_8. When D_8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D_0 goes HIGH; then on the next cycle D_1 and so one. A D_1 output from the most significant device is issued to create the $\overline{W}$ for all cascaded devices.

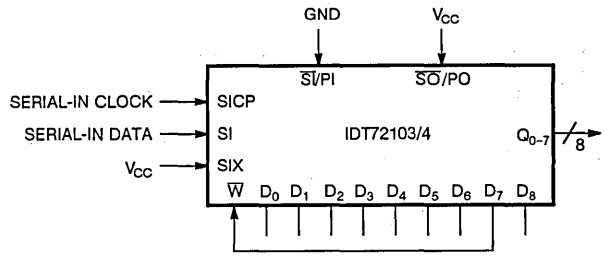
The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q_0. The second bit shifted in is on Q_1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D_{0-8} lines to determine whether to store it or not.

The example shown in Figure 10 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

SINGLE DEVICE SERIAL INPUT CONFIGURATION



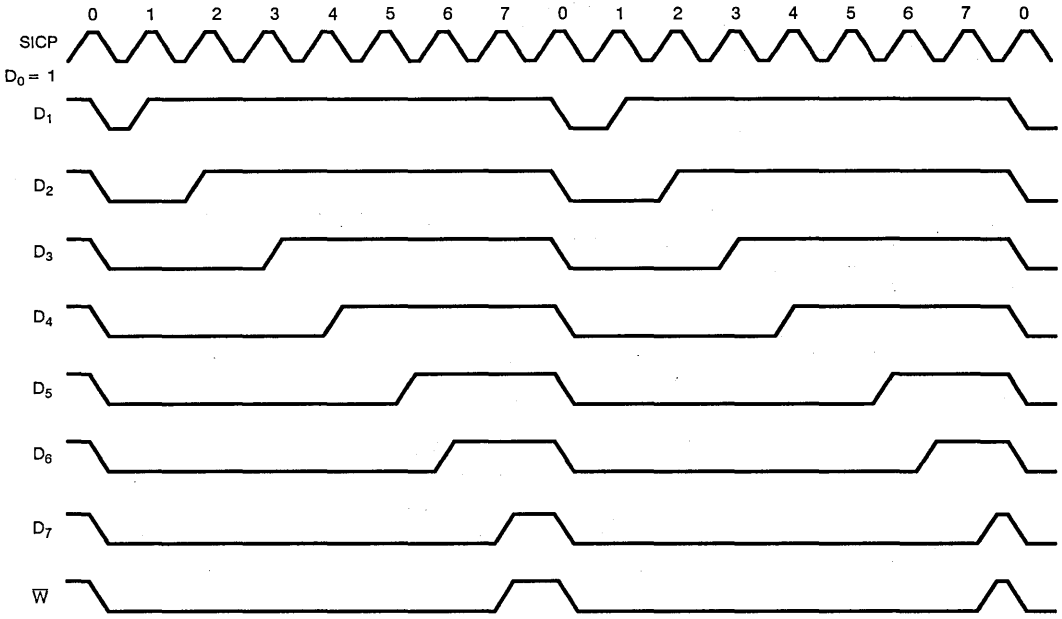


Figure 8. Serial-In Mode Where 8-Bit Parallel Output Data Is Read

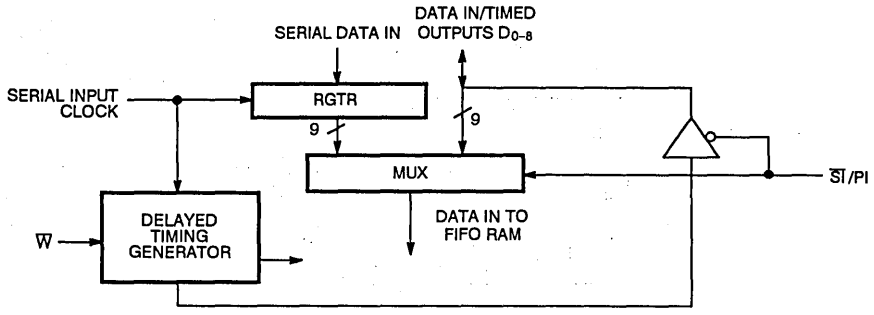


Figure 9. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

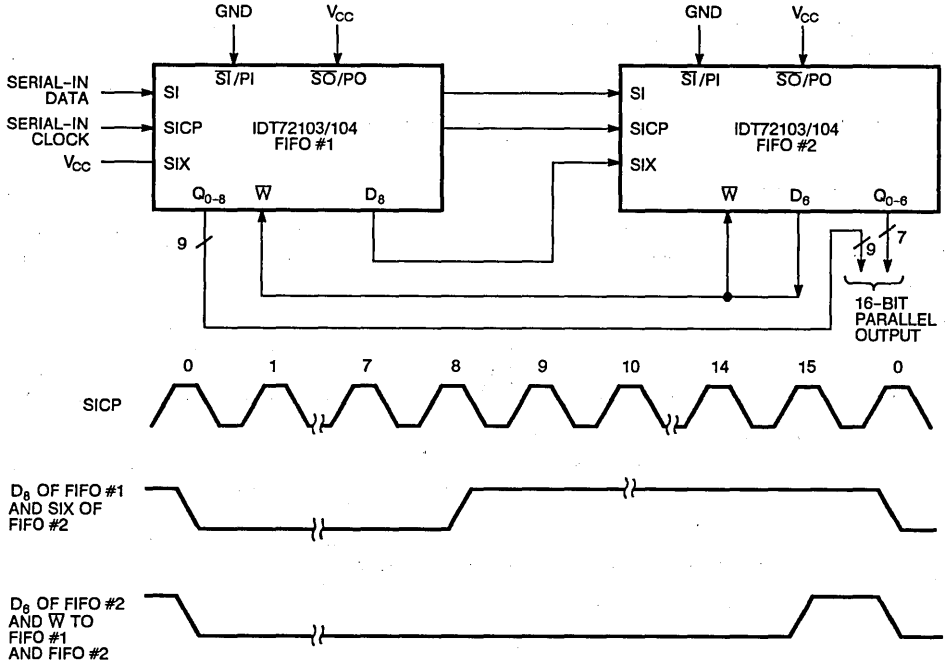
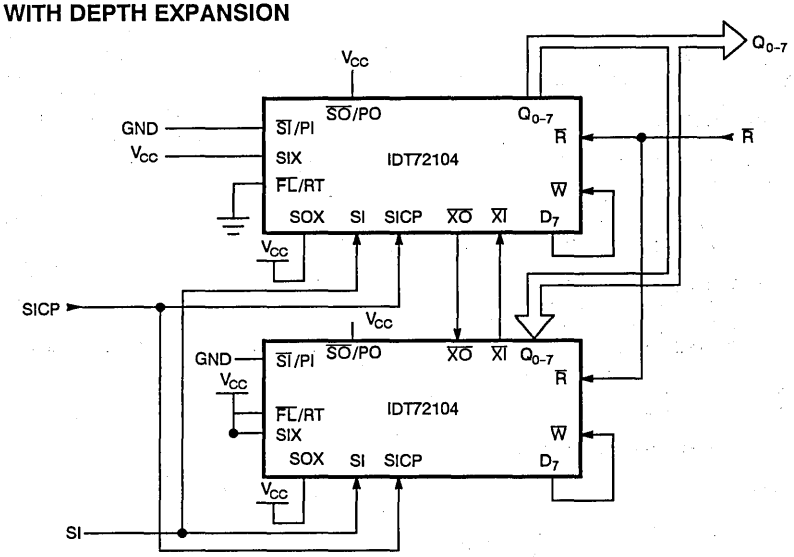


Figure 10. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

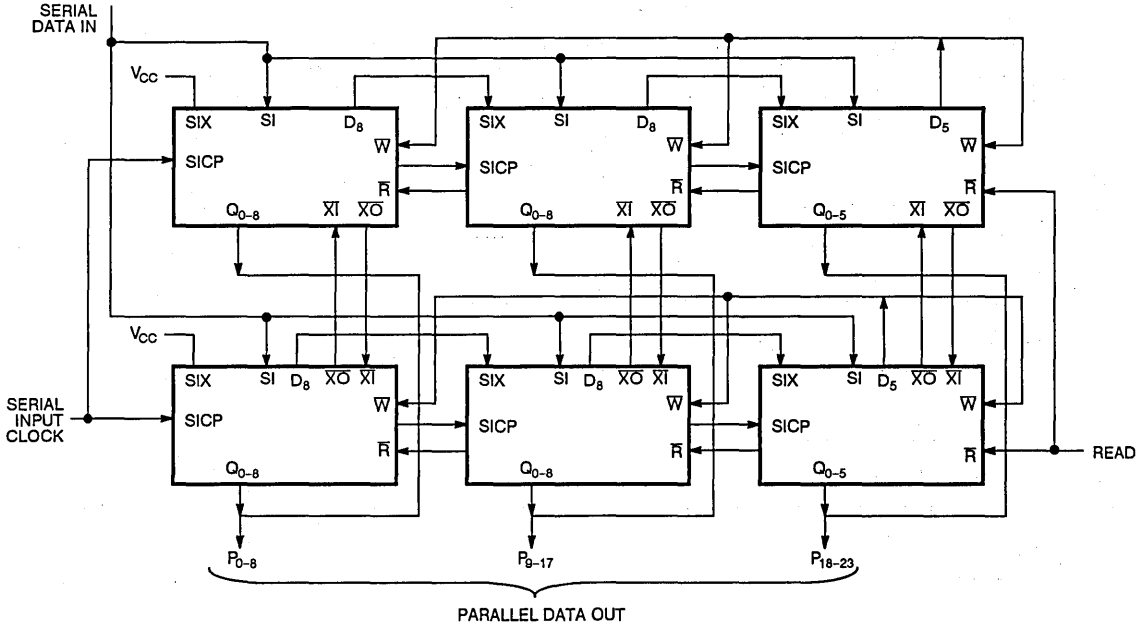
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins are tied to GND and $\overline{SO}$/PO pins are tied to V_{CC}. $\overline{OE}$ is tied LOW. For $\overline{FF}$ and $\overline{EF}$ connections see Figure 17.

Figure 11. An 8K x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins is tied to GND. $\overline{SO}$/PO is tied to V_{CC}. For $\overline{FF}$ and $\overline{EF}$ connections see Figure 17.

Figure 12. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

Serial Data Output

The Serial Output mode is selected by setting the $\overline{SO}$/PO line low. When in the Serial-Out mode, one of the Q_{0-8} lines should be used to control the $\overline{R}$ signal. In the Serial-Out mode, the Q_{0-8} are taps off a digital delay line. By selecting one of these taps and connecting it to the $\overline{R}$ input, the width of the serial word to be read and shifted is programmed. For instance, if the Q_5 line is connected to the $\overline{R}$ input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit first. If the input mode of the FIFO is parallel, the information that was written into the D_0 bit will come out as the fist bit of the serial word. The second bit of the serial stream will be the D_1 bit and so on.

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q_0 go LOW and a new serial word is started. On the next clock cycle, Q_1 will go HIGH, Q_2 on the next clock and so on, as shown in Figure 13. This continues until the Q line, which is connected to $\overline{R}$, goes HIGH at which point all of the Q lines go LOW on the next clock and a new serial word is started.

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to Q_8 of the previous devices, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the lines go LOW except for Q_0. Just as in the standalone case, on each consecutive clock cycle, each Q line goes HIGH in order of least to most significant. When Q_8 (which is connected to the SOX input of the next device) goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all $\overline{R}$ inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three-statable, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 15 shows an example of the interconnections for a 16-bit serialized FIFO.

SINGLE DEVICE SERIAL OUTPUT CONFIGURATION

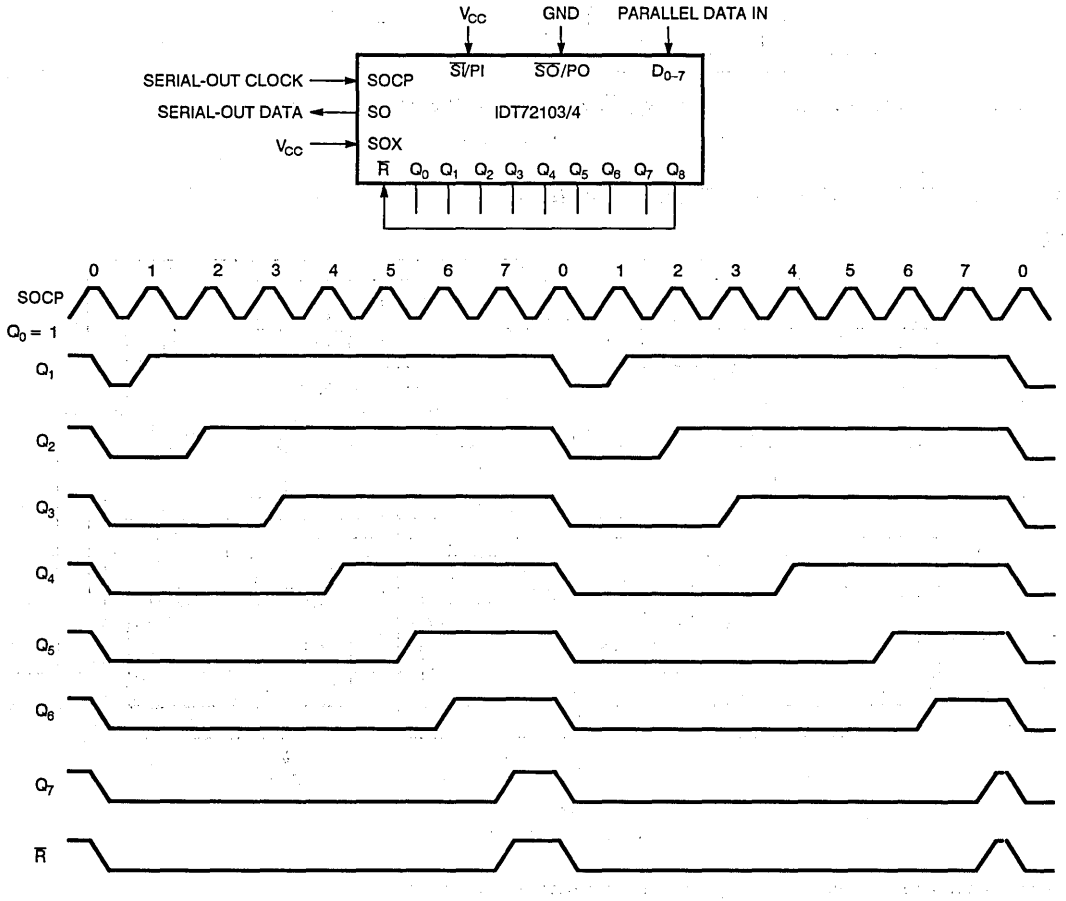


Figure 13. Serial-Out Configuration Where Input Data is Loaded in 8-Bit Quantities and Read Out Serially

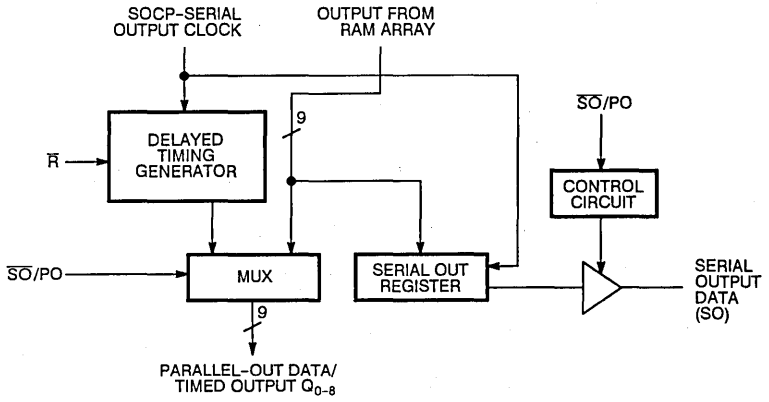


Figure 14. Serial-Output Circuitry

6

SERIAL-OUT WIDTH EXPANSION

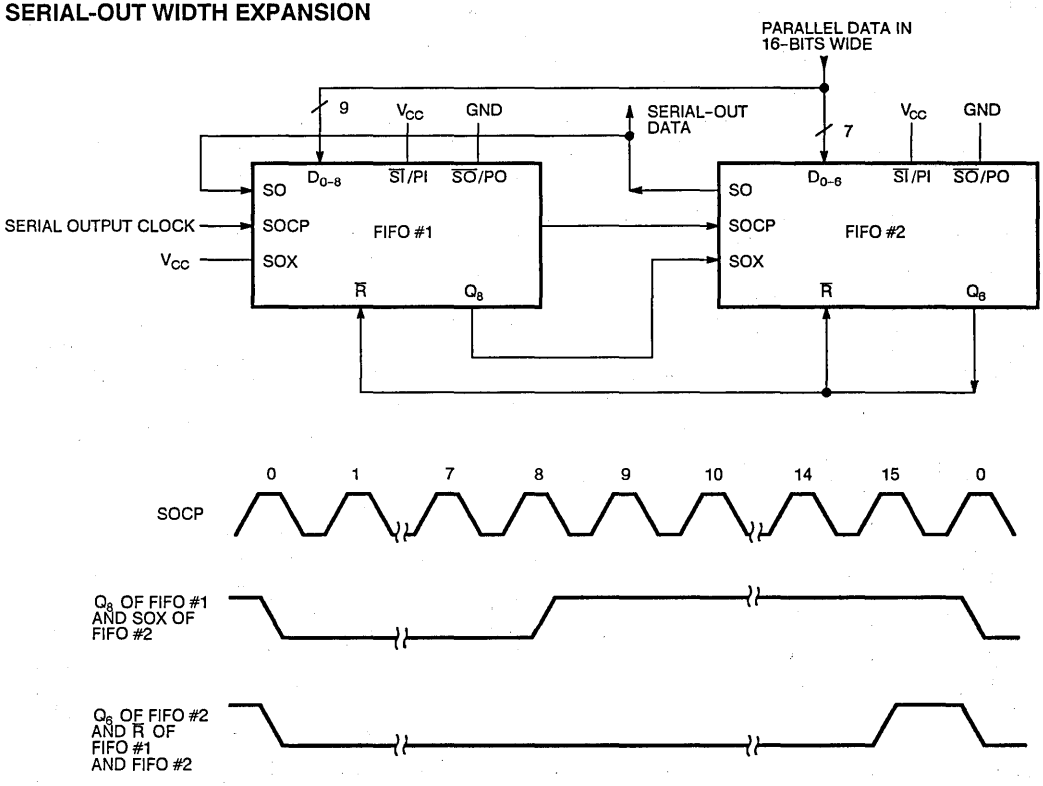
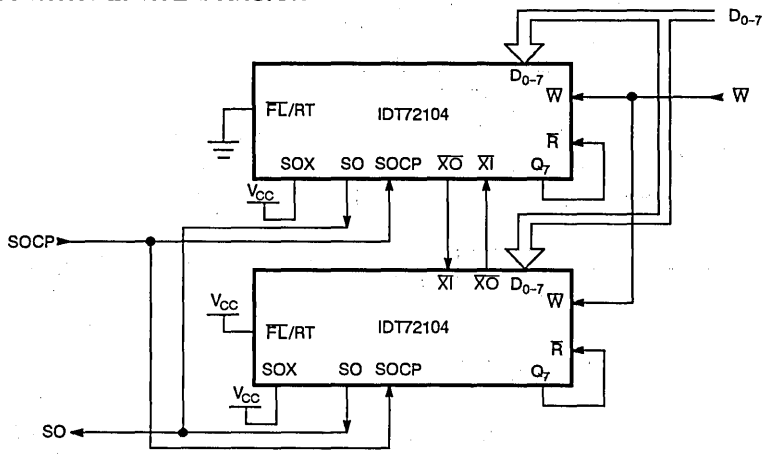


Figure 15. Serial Output for 16-Bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2

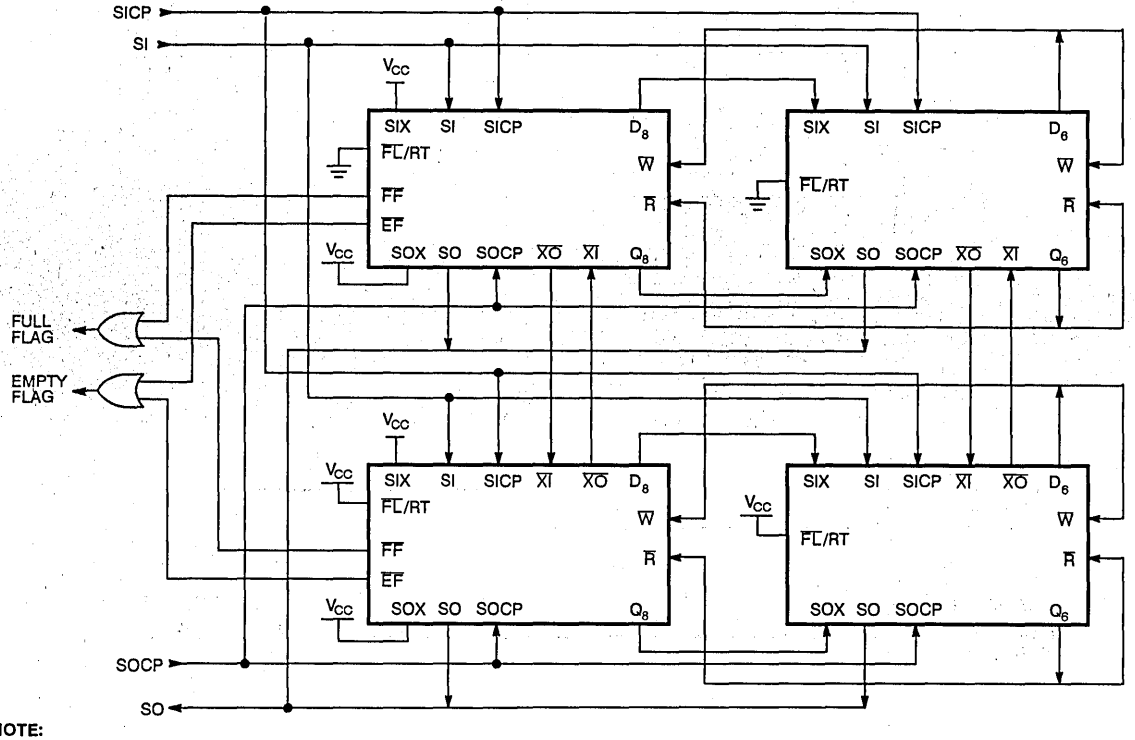
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to V_{CC} and SO/PO pins are tied to GND. OE is tied LOW. For FF and EF connections see Figure 17.

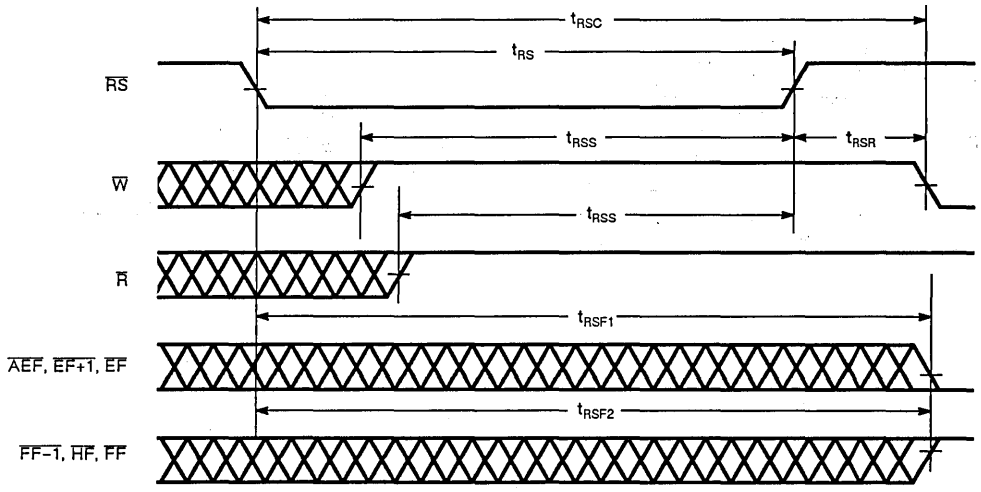
Figure 16. An 8K x 8 Parallel-In Serial-Out FIFO

SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION



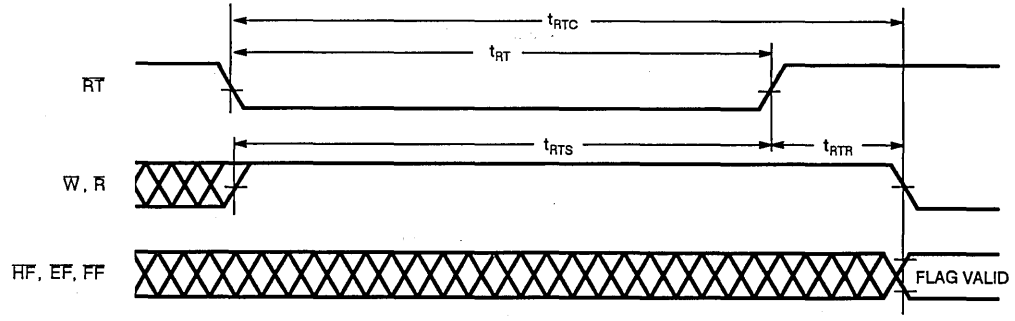
NOTE:
1. All RS pins are connected together. All OE pins are connected LOW. All SI/PI and SO/PO pins are grounded.

Figure 17. A 128K x 1 Serial-In Serial-Out FIFO



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Figure 18. Reset



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$, $\overline{AEF}$, $\overline{FF-1}$ and $\overline{EF+1}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 19. Retransmit

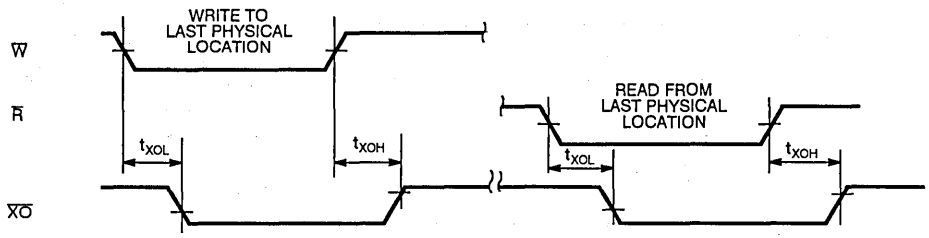


Figure 20. Expansion-Out

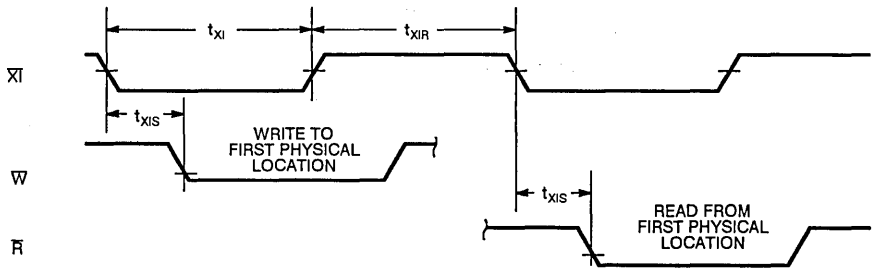


Figure 21. Expansion-In

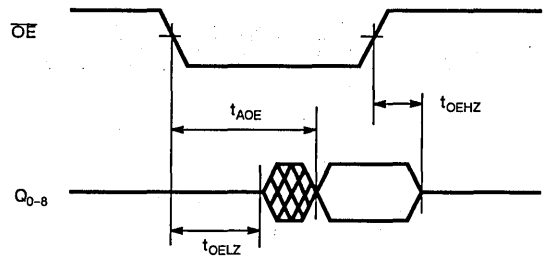


Figure 22. Output Enable Timings

PARALLEL TIMINGS – READ/WRITE

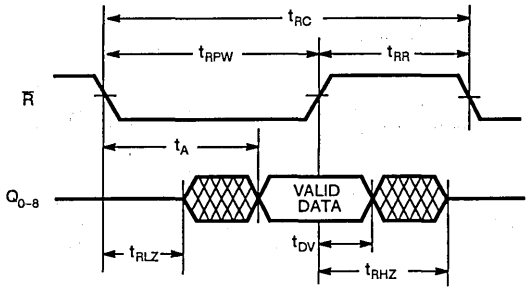


Figure 23. Read Operation in Parallel Data Out Mode

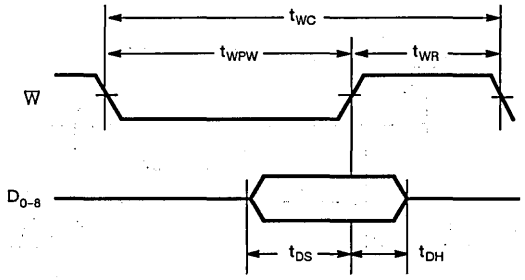
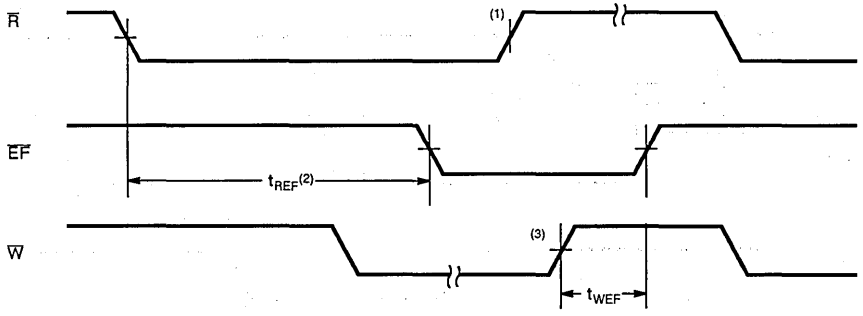


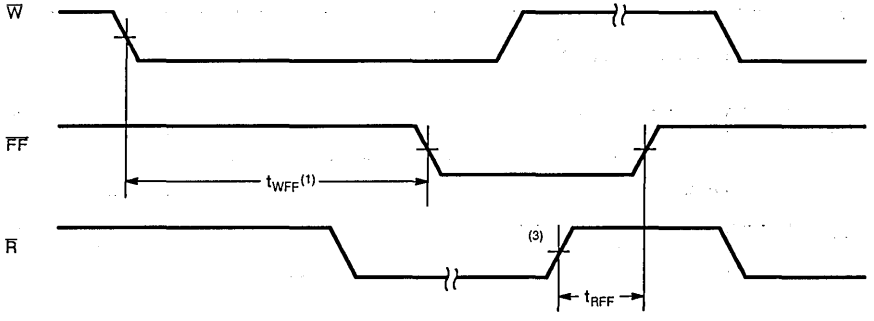
Figure 24. Write Operation in Parallel Data In Mode

PARALLEL TIMINGS – FLAGS



NOTES:
1. Data is valid on this edge.
2. The Empty Flag is asserted by $\overline{R}$ in the Parallel-Out mode and is specified by t_{REF}. The $\overline{EF}$ flag is deasserted by the rising edge of $\overline{W}$.
3. First rising edge of Write after $\overline{EF}$ is set.

Figure 25. Empty Flag Timings in Parallel-Out Mode



NOTE:
1. For the assertion time, t_{WFF} is used when data is written in the Parallel mode. The $\overline{FF}$ is deasserted by the rising edge of $\overline{R}$.

Figure 26. Full Flag Timings in Parallel-In Mode

PARALLEL TIMINGS – FLAGS

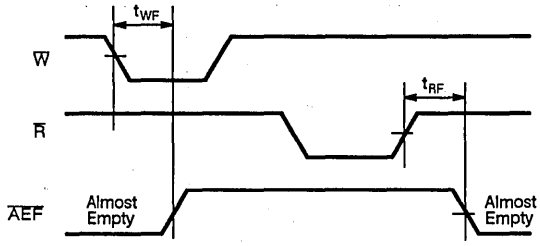


Figure 27A. Almost Empty Flag Region

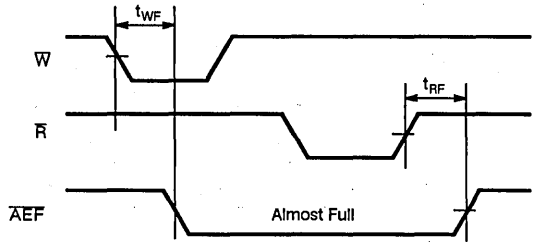


Figure 27B. Almost Full Flag Region

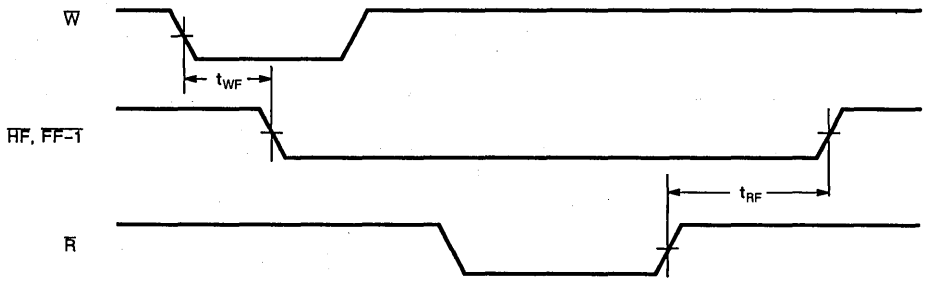


Figure 27C. HF, and FF–1 Flag Timing

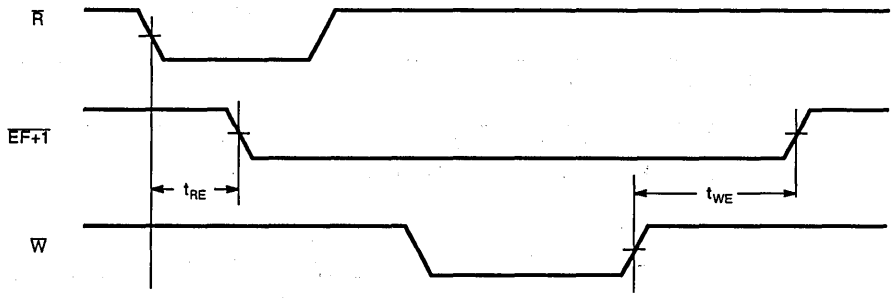
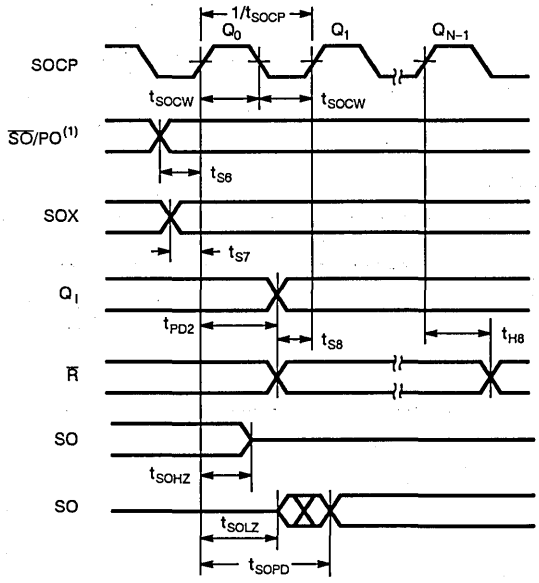


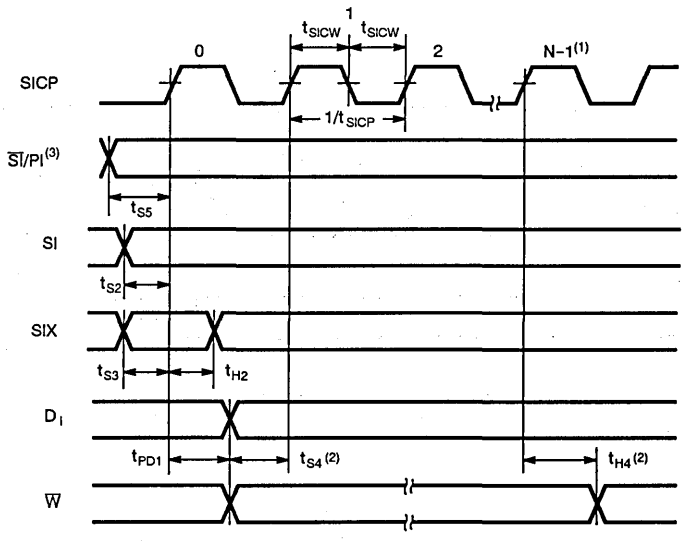
Figure 28. Empty + 1 Flag Timings

SERIAL TIMINGS – READ/WRITE



NOTE:
1. After SO/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

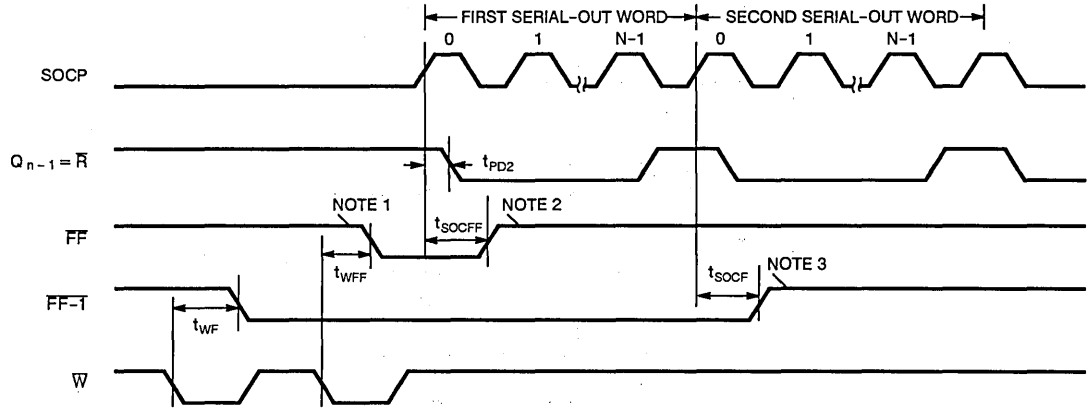
Figure 29. Read Operation in Serial-Out Mode



NOTES:
1. For the Standalone mode, N ≥ 4 and the input bits are numbered 0 to N-1.
2. For the recommended interconnections, D_I is to be directly tied to $\overline{W}$ and the t_{S4} and t_{H4} requirements will be satisfied. For users that modify $\overline{W}$ externally, t_{S4} and t_{H4} have to be met.
3. After $\overline{SI}$/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

Figure 30. Write Operation in Serial-In Mode

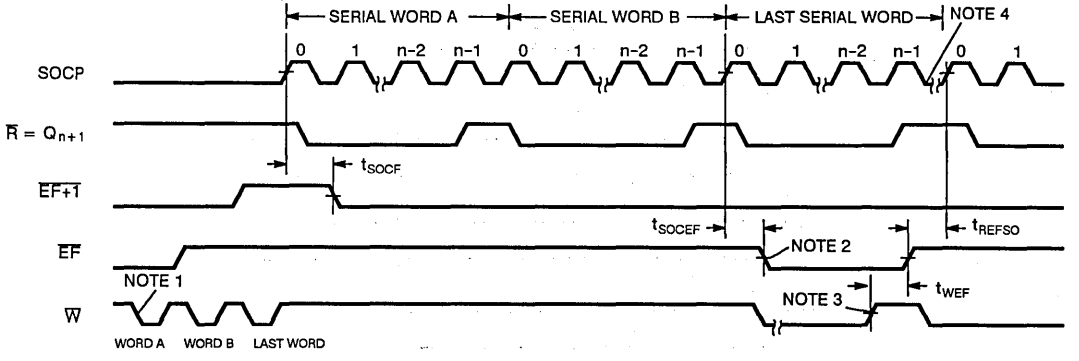
SERIAL TIMINGS – FLAGS



NOTES:

1. The FIFO is full and a new read sequence is starting.
2. On the first rising edge of SOCP, the $\overline{FF}$ is de-asserted. In the Serial-In mode, a new write operation can begin after t_{RFFS1} after $\overline{FF}$ goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after $\overline{FF}$ flag goes HIGH.
3. The $\overline{FF-1}$ Flag is deasserted after the first SOCP of the second serial word.

Figure 31. Full Flag and Full–1 Flag Deassertion in the Serial-Out Mode

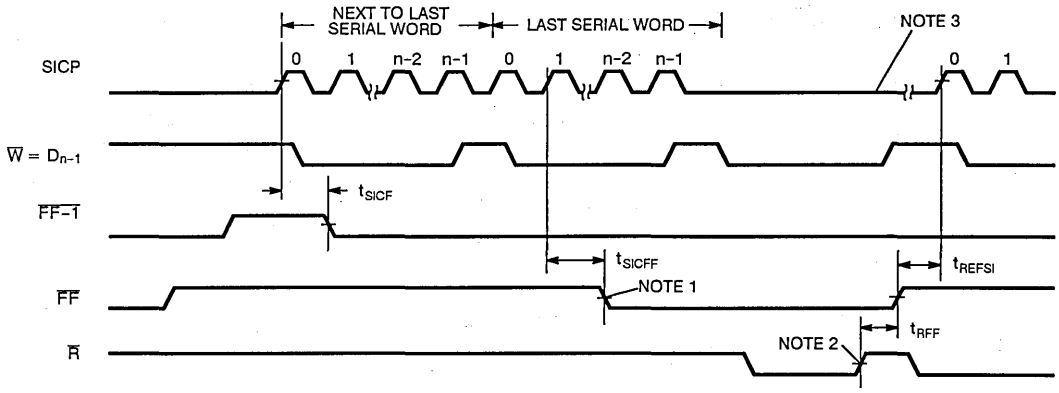


NOTES:

1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag is asserted in the Serial-Out mode by using the t_{SOCEF} parameter. This parameter is measured in the worst case from the rising edge of the SOCP used to clock data bit 0. Whenever $\overline{EF}$ goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the $\overline{EF}$ flag is deasserted by the rising edge of $\overline{W}$. In the Serial-In mode, the $\overline{EF}$ flag is deasserted by the rising edge of W.
3. First Write rising edge after $\overline{EF}$ is set.
4. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 32. Empty Flag and Empty+1 Flag Assertion in the Serial-Out Mode, FIFO Being Emptied

SERIAL TIMINGS – FLAGS

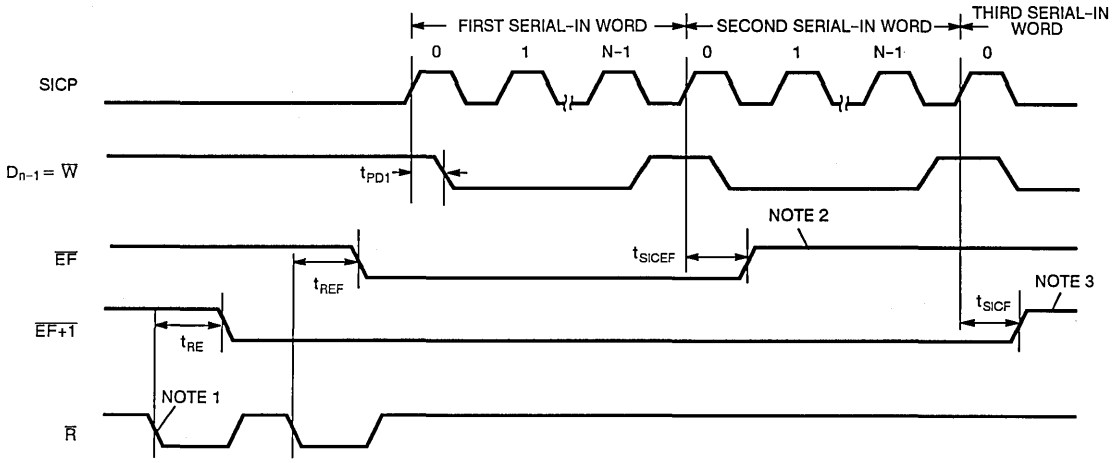


6

NOTES:

1. The Full Flag is asserted in the Serial-In mode by using the t_{SICFF} parameter. This parameter is measured in the worst case from the rising edge of SICP followed by a ($t_{PD1} + t_{WFF}$) delay from the first rising edge of SICP of the last word.
2. First Read rising edge after $\overline{FF}$ is set.
3. SICP should not be clocked until $\overline{FF}$ goes HIGH.

Figure 33. Full Flag and Full-1 Flag Assertion in the Serial-In Mode, FIFO Being Filled

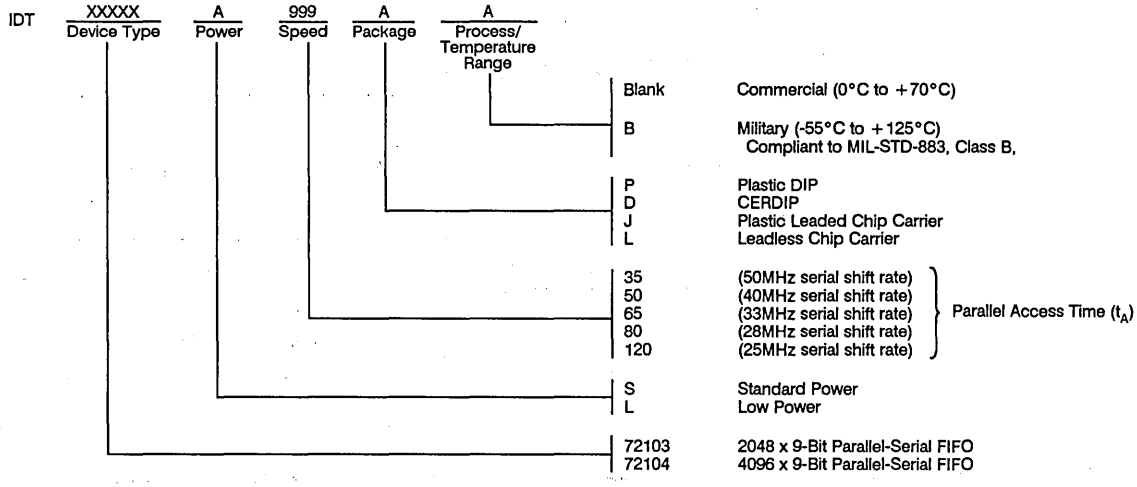


NOTES:

1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is deasserted when an entire word has been loaded into the internal RAM. It can occur after the first rising edge of SICP of the second Serial-In word. In the Serial-Out mode, a new read operation can begin t_{REFSO} after $\overline{EF}$ goes HIGH. In the Parallel-Out mode, a new read operation can occur immediately after $\overline{FF}$ goes HIGH.
3. The Empty + 1 Flag is deasserted after the first rising edge of SICP of the third Serial-In word.

Figure 34. Empty Flag and Empty + 1 Flag Deassertion in Serial-In Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

256 x 16, 512 x 16, 1024 x 16 PARALLEL-TO-SERIAL CMOS FIFO

PRELIMINARY
IDT 72105
IDT 72115
IDT 72125

FEATURES:

- 25ns parallel port access time
- 50MHz serial output port shift rate
- Easily expandable in depth and width
- Asynchronous and simultaneous read write
- Dual-ported zero fall-through time architecture
- Five flags to signal FIFO status: Empty, Full, Half-full, Almost-empty and Almost-full
- Least Significant or Most Significant bit first read selectable
- Low power consumption
- Available in 28-pin 300mil Plastic and Sidebraze THINDIP and surface mount 28-pin SOIC
- Produced with advanced submicron CEMOS™ high-performance technology

DESCRIPTION:

The IDT72105, IDT72115 and IDT72125 are high-speed, low power parallel-to-serial FIFOs. These FIFOs fit well in output peripherals as a data buffer. Some typical applications are in laser printers, FAX machines, local area networks (LANs), video storage, and disk or tape controllers.

The IDT72105/15/25 have a 16-bit parallel input port and a serial output port. Wider and Deeper parallel-to-serial data buffers can be built using multiple chips. IDT's unique serial expansion logic (RSIX, RSOX, $\overline{FL}$/DIR) makes both depth and width expansion possible using a minimum number of pins.

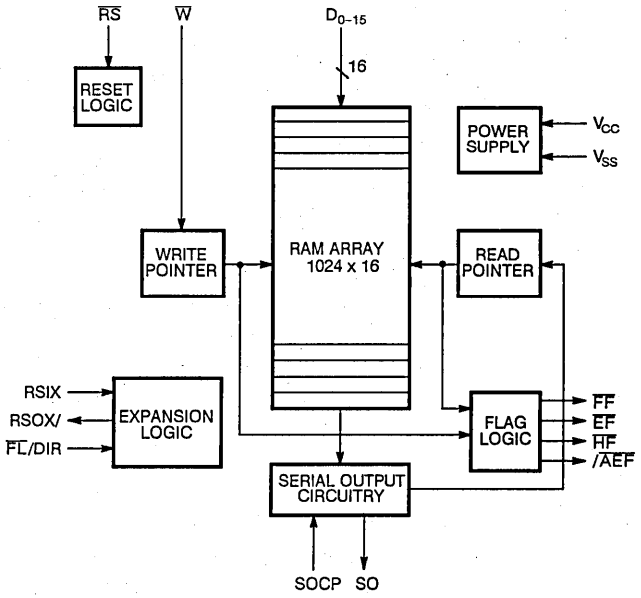
Serial output is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant bit can be read first by programming the DIR pin after Reset.

Five flags, empty, full, half-full, almost-empty and almost-full are provided to monitor the FIFOs. The full and empty flags prevent any FIFO data overflow or underflow conditions. The half-full flag is available in both single and expansion configurations. The almost-empty and almost-full are only available in the single device configuration.

The IDT72105/15/25 are fabricated using IDT's high-speed submicron CEMOS™ technology.

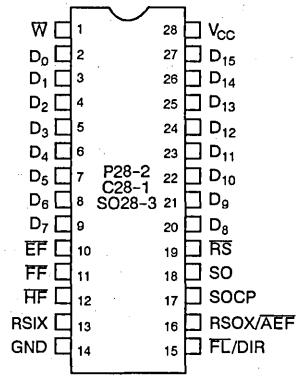
6

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
$D_0 - D_{15}$	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/ Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) function is programmed during operation after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high , the device is not empty.
$\overline{HF}$	Half Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half full. When $\overline{HF}$ is HIGH, the device is empty to half full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion, Almost Empty, Almost Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty to 1/8 full - 1 or 7/8 full + 1to full. When $\overline{AEF}$ is HIGH, the device is1/8 full up to 7/8 full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
V_{CC}	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

STATUS FLAGS

NUMBER OF WORDS IN FIFO			$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
IDT72105	IDT72115	IDT72125				
0	0	0	H	L	H	L
1-31	1-63	1-127	H	L	H	H
32-128	64-256	128-512	H	H	H	H
129-224	257-448	513-896	H	H	L	H
225-255	449-511	897-1023	H	L	L	H
256	512	1024	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL} (1)	Input Low Voltage	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT72105 IDT72115 IDT72125 COMMERCIAL MIN.	TYP.	MAX.	UNIT
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA (5)	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA (6)	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = V_{IH})	–	8	12	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	8	mA

NOTES:
1. Measurements with $0.4 \le V_{IN} \le V_{OUT}$.
2. $\overline{RS} \le V_{IL}$, $0.4 \le V_{OUT} \le V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = $\overline{R}$ = V_{CC} -0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V
5. For SO, I_{OUT} = -4mA
6. For SO, I_{OUT} = 16mA

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	FIGURE	72105x25 72115x25 72125x25		72105x50 72115x50 72125x50		72105x80 72115x80 72125x80		72105x120 72115x120 72125x120		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_S	Parallel Shift Frequency	–	–	22.2	–	15	–	10	–	7	MHz
t_{SOCP}	Serial Shift Frequency	–	–	50	–	40	–	28	–	25	MHz
t_{WC}	Write Cycle Time	1	35	–	65	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width	1	25	–	50	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	1	10	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	1	10	–	15	–	15	–	20	–	ns
t_{DH}	Data Hold Time	1	0	–	5	–	5	–	10	–	ns
t_{SOCP}	Serial Clock Cycle Time	2	20	–	25	–	35	–	40	–	ns
t_{SOCW}	Serial Clock Width High/Low	2	8	–	10	–	15	–	18	–	ns
t_{SOPD}	SOCP Rising Edge to SO Valid Data	2	–	10	–	12	–	17	–	20	ns
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	2	3	10	3	12	3	17	3	20	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	2	3	10	3	12	3	17	3	20	ns
t_{WEF}	Write High to $\overline{EF}$ High	4,5	–	20	–	25	–	35	–	40	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	3,6	–	30	–	40	–	50	–	60	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	7	–	30	–	40	–	50	–	60	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	6	25	–	50	–	80	–	120	–	ns
t_{SOCEF}	SOCP Rising Edge to $\overline{EF}$ Low	4,5	–	20	–	25	–	35	–	40	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	3,6	–	30	–	40	–	50	–	60	ns
t_{SOCF}	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	7	–	30	–	40	–	50	–	60	ns
t_{REFSO}	SOCP Delay After $\overline{EF}$ High	5	35	–	65	–	100	–	140	–	ns
t_{RSC}	Reset Cycle Time	8	35	–	65	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width	8	25	–	50	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	8	25	–	50	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	8	10	–	15	–	20	–	20	–	ns
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	5	–	7	–	10	–	10	–	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	–	0	–	5	–	5	–	ns
t_{DIRS}	DIR Set-up Time to SOCP Rising Edge	9	5	–	7	–	10	–	10	–	ns
t_{DIRH}	DIR Hold Time from SOCP Rising Edge	9	0	–	0	–	5	–	5	–	ns
t_{SOXD1}	SOCP Rising Edge to RSOX Rising Edge	9	3	11	3	15	3	20	3	20	ns
t_{SOXD2}	SOCP Rising Edge to RSOX Falling Edge	9	3	11	3	15	3	20	3	20	ns
t_{SIXS}	RSIX Set-up Time to SOCP Rising Edge	9	5	–	7	–	10	–	10	–	ns
t_{SIXH}	RSIX Hold Time from SOCP Rising Edge	9	0	–	0	–	5	–	5	–	ns

NOTE:

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

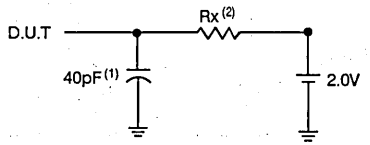


Figure A. Output Load.

1. Includes jig and scope capacitances.
2. For SO, Rx = 100Ω. For all other outputs, Rx = 200Ω.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to location zero. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

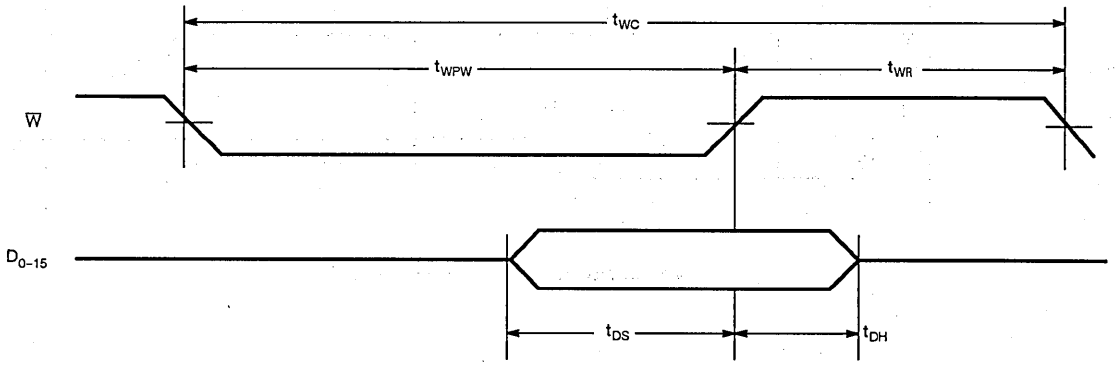


Figure 1. Write Operation

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.

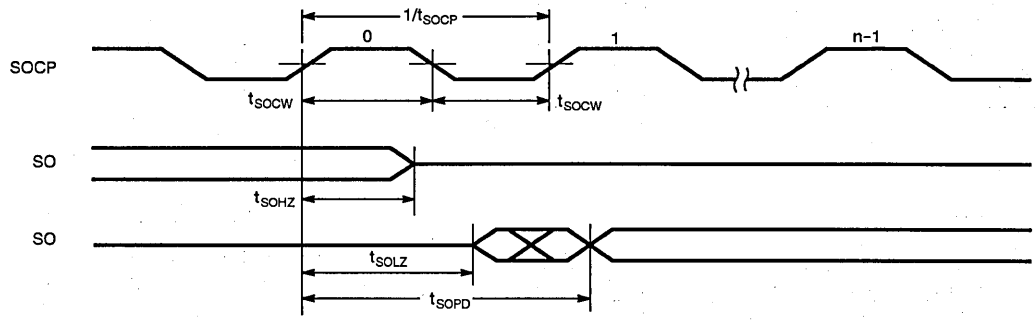


Figure 2. Read Operation

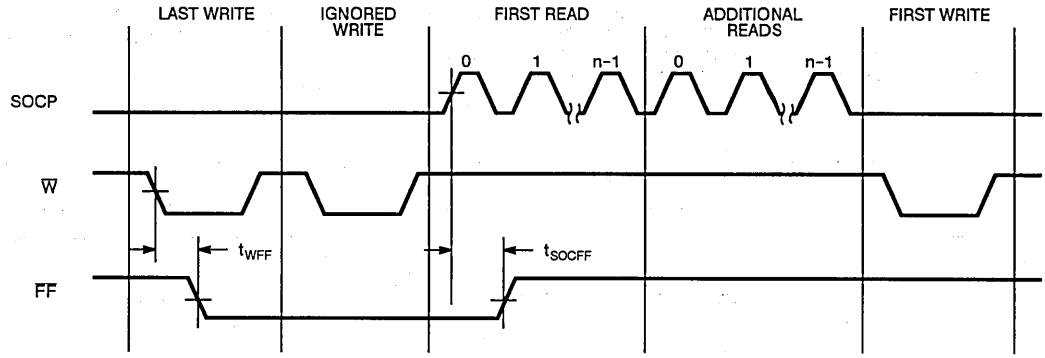


Figure 3. Full Flag from Last Write to First Read

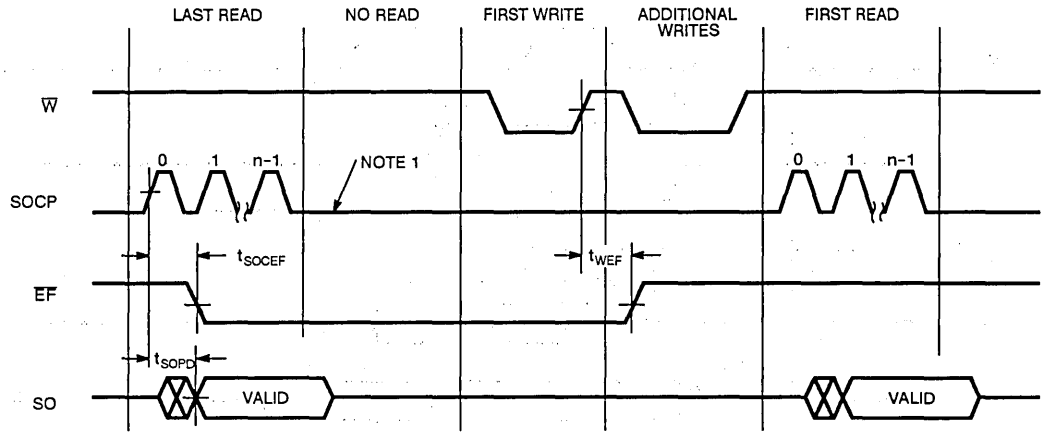


Figure 4. Empty Flag from Last Read to First Write

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

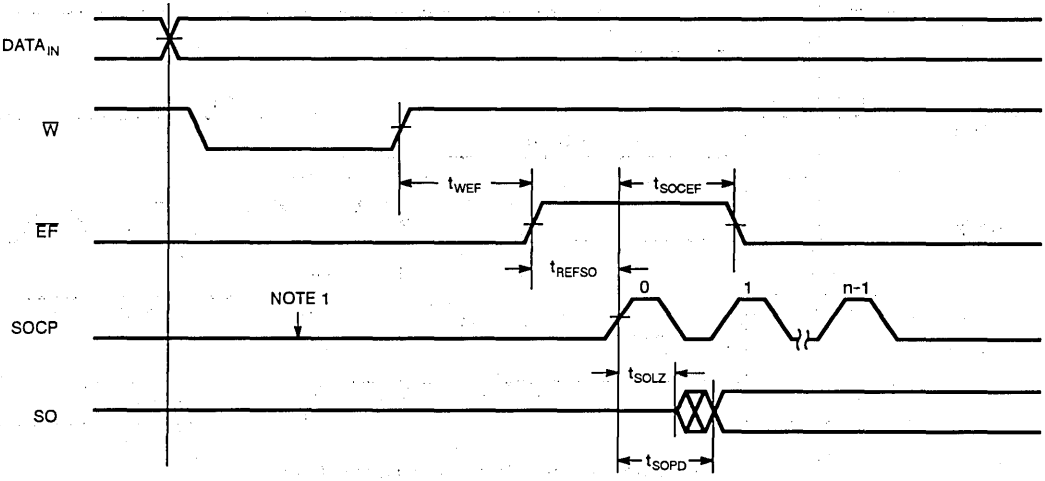


Figure 5. Empty Boundry Condition Timing

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

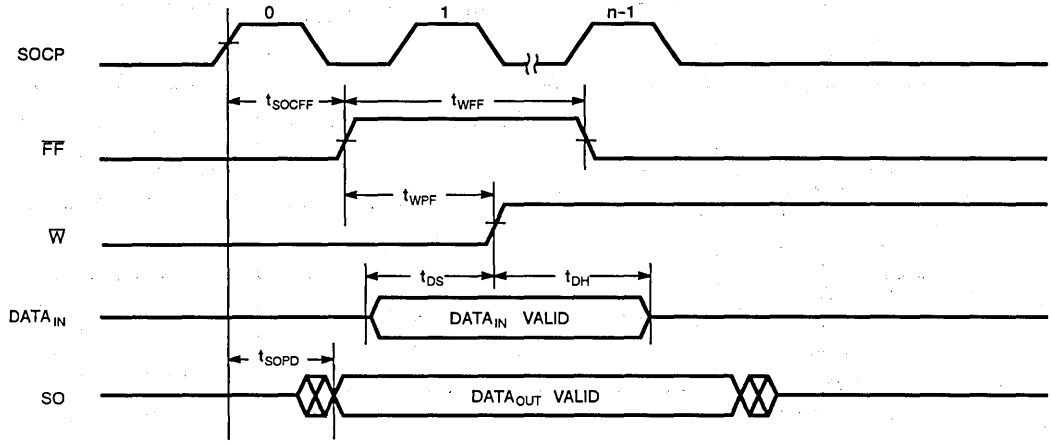


Figure 6. Full Boundary Condition Timing

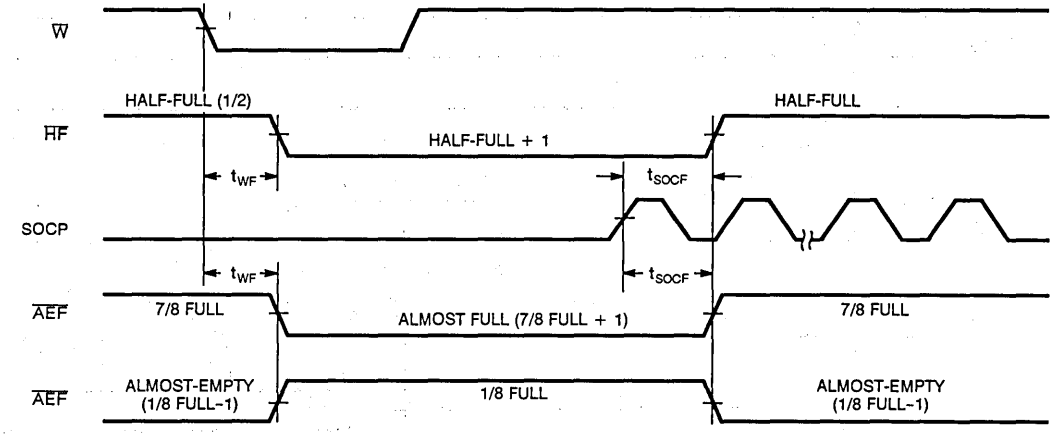


Figure 7. Half Full, Almost Full and Almost Empty Timings

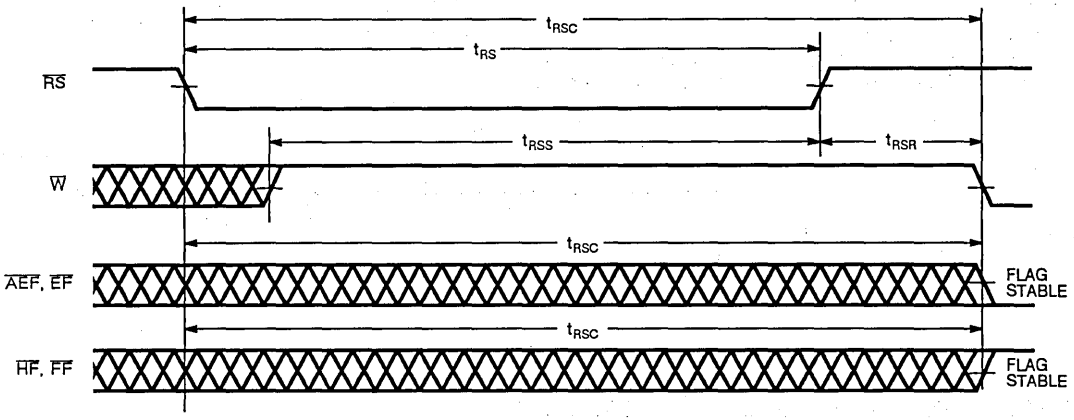


Figure 8. Reset

NOTE:
1. EF, FF, HF and AEF may change status during Reset, but flags will be valid at t_{RSC}.

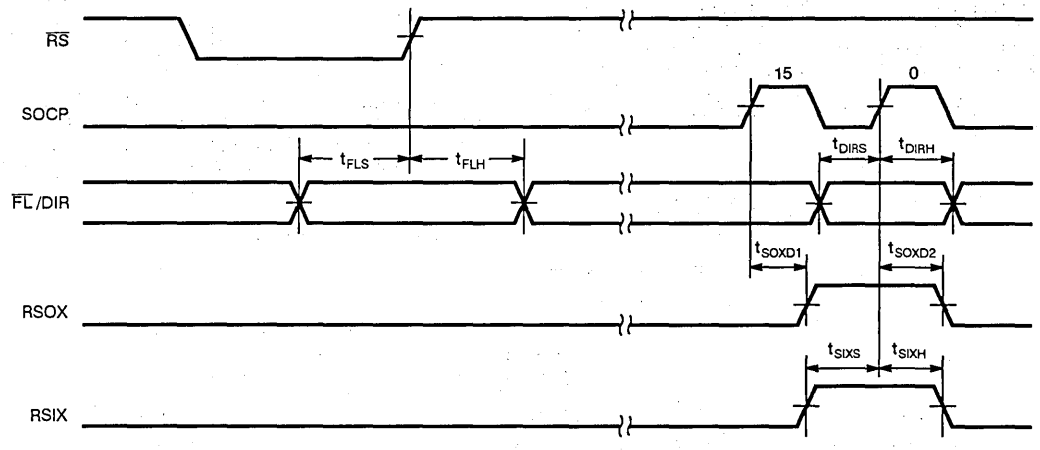


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$, and outputs the Almost Empty and Almost Full Flag.

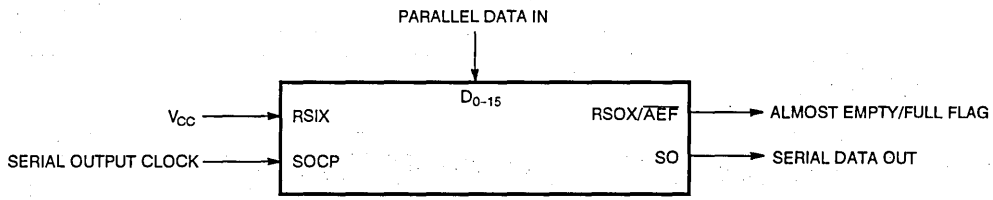


Figure 10. Single Device Configuration

TABLE 1: RESET AND FIRST LOAD TRUE TABLE – SINGLE DEVICE CONFIGURATION

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	DIR	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0, 1	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together as shown in Figure 11 and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost Empty and Almost Full Flag is not available due to using the RSOX pin for expansion.

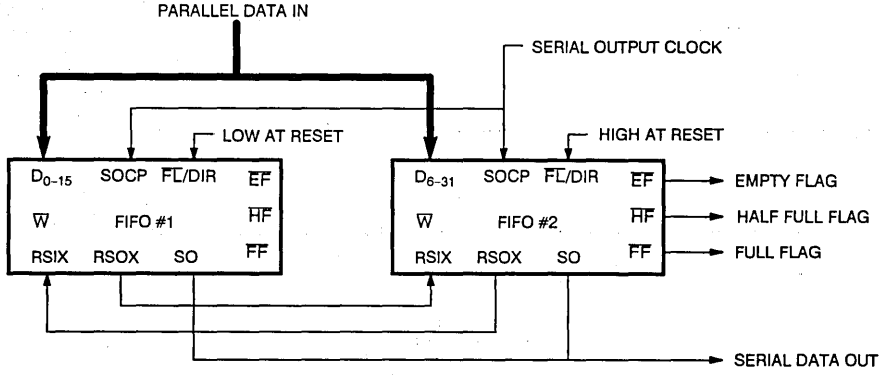


Figure 11. Width Expansion for 32-bit Parallel Data In

Depth Expansion (Daisy Chain) Mode

The IDT 72105/15/25 can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25 and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO to write data into. A byte of data should be written sequentially into each FIFO so that the RSOX/RSIX handshake can control reading out the data in the correct sequence. The IDT72105/15/25 operate in the Depth Expansion Mode when the following conditions are met:

1. The first device must be designated by programming $\overline{FL}$ LOW at Reset. All other devices to be programmed HIGH.
2. The Read Serial Out Expansion (RSOX) of each device must be tied to the Read Serial In Expansion (RSIX of the next device in the manner shown).
3. External logic is needed to generate composite $\overline{Empty}$, Half Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost Empty and Almost Full Flag is not available due to using the RSOX pin for expansion.

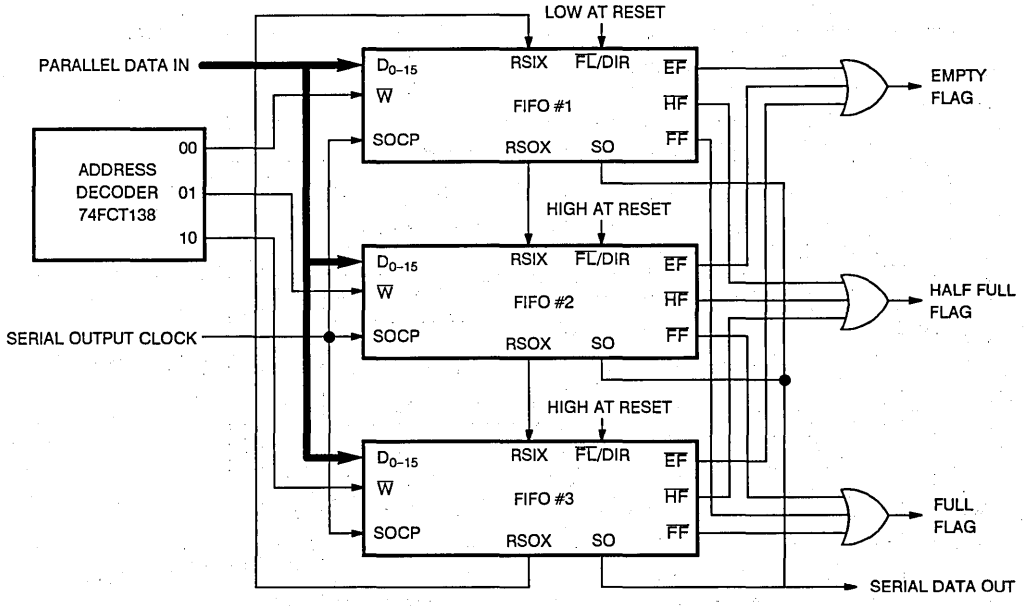


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE – WIDTH/DEPTH COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	DIR	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0, 1	X	X	X	X

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/DIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half Full Flag Output, $\overline{FF}$ = Full Flag Output

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

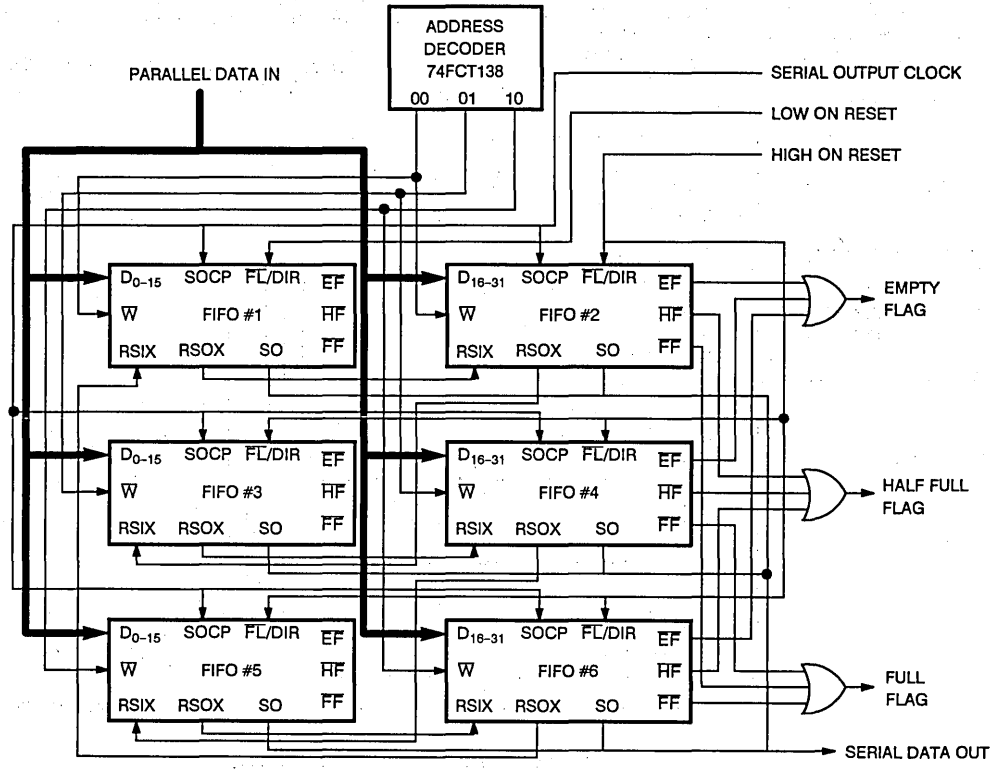
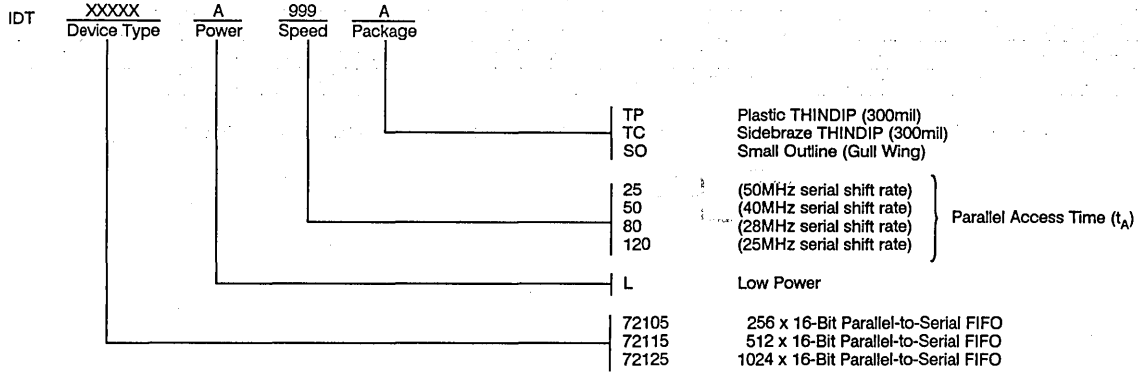


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT 72131
IDT 72141

FEATURES:

- 35ns parallel port access time
- 50MHz serial port shift rate
- Easily expandable in depth and width
- Programmable word lengths including 7-9, 16-18, and 32-36 bits using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost-Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Retransmit capability in single device mode
- Produced with high performance, low-power CEMOS™ technology
- Available in 28-pin ceramic and plastic DIP, 32-pin LCC and J-leaded PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDT's serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

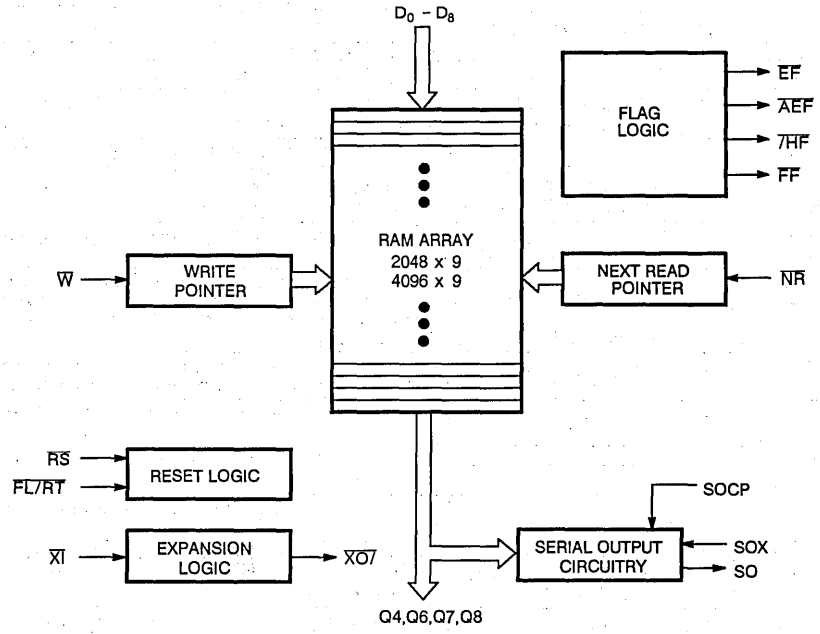
The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDT's unique Flexishift™ serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost-empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

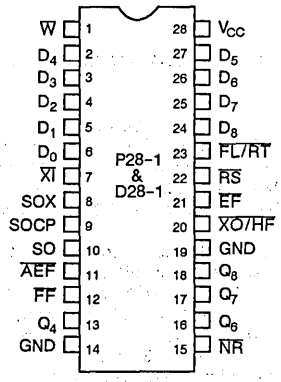
6

FUNCTIONAL BLOCK DIAGRAM

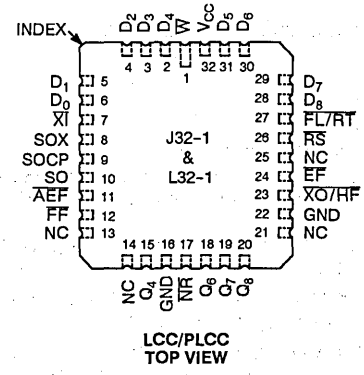


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
$D_0 - D_8$	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high and SCOP low during $\overline{RS}$ cycle. SOCP must have also completed its serial word so that $\overline{NR}$ is high.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width, connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. SOCP and W must be high before setting $\overline{FL/RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, SOX is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SOX pin tied to the Q_8 pin of the device that will source the next lower order bits of the serial word. Data is then clocked out least significant bit first. For single device operation, SOX is tied high.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 or Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Single Ground at 10V.

STATUS FLAGS

NUMBER OF WORDS IN FIFO		$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
IDT72131	IDT72141				
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC}= 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	IDT72131/IDT72141 COMMERCIAL			IDT72131/IDT72141 MILITARY			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	–	100	160	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current	–	–	8	–	–	12	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $\overline{W}$ = $\overline{R}$ = V_{CC}-0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	COM'L		MIL.		MILITARY AND COMMERCIAL								UNIT
		72131x35 72141x35		72131x40 72141x40		72131x50 72141x50		72131x65 72141x65		72131x80 72141x80		72131x120 72141x120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_S	Parallel Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{SOCP}	Serial-Out Shift Frequency	–	50	–	50	–	40	–	33	–	28	–	25	MHz
PARALLEL INPUT MODE TIMINGS														
t_{DS}	Data Set-up Time	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{WC}	Write Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{WEF}	Write High to $\overline{EF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
SERIAL OUTPUT MODE TIMIMGS														
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	5	16	5	16	5	26	5	20	5	25	5	35	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	5	22	5	22	5	22	5	22	5	30	5	35	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	–	18	–	18	–	18	–	22	–	30	–	35	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{SOCW}	Serial In Clock Width High/Low	8	–	8	–	10	–	10	–	15	–	15	–	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 – First Word) to $\overline{EF}$ Low	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	–	30	–	35	–	40	–	50	–	60	–	65	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	–	30	–	35	–	40	–	50	–	60	–	65	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
RESET TIMINGS														
t_{RSC}	Reset Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
RETRANSMIT TIMINGS														
t_{RTC}	Retransmit Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
DEPTH EXPANSION MODE DELAYS														
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_X	$\overline{XI}$ Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTE: 1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

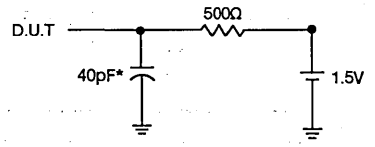


Figure A. Output Load.

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

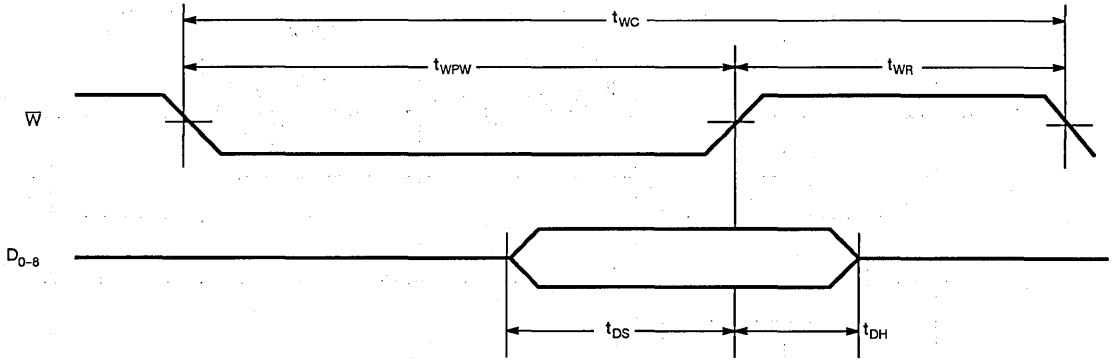


Figure 1. Write Operation

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked while the Empty Flag is low. If it is, then two things will occur. One, invalid data will be read by SOCP and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D_0, then D_1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q_4, Q_6, Q_7, or Q_8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.

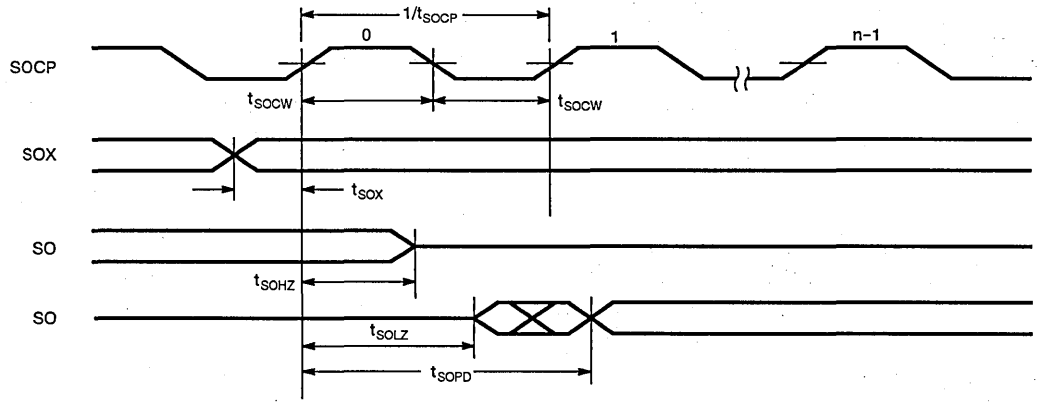


Figure 2. Read Operation

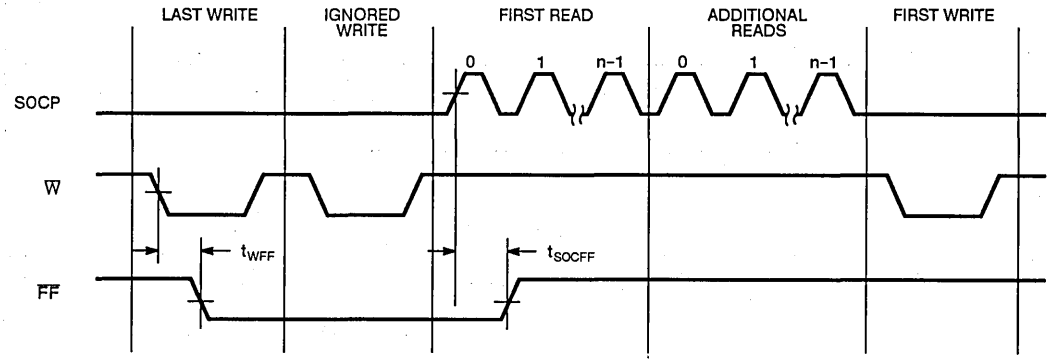


Figure 3. Full Flag from Last Write to First Read

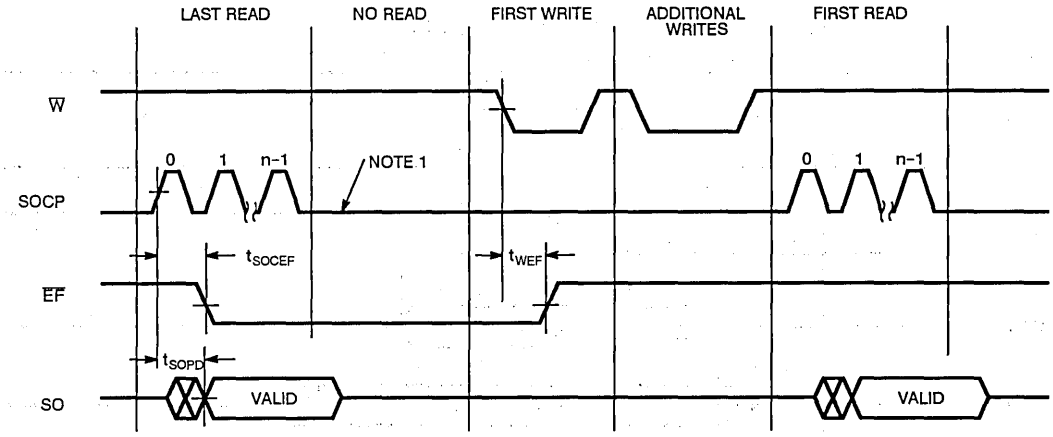


Figure 4. Empty Flag from Last Read to First Write

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

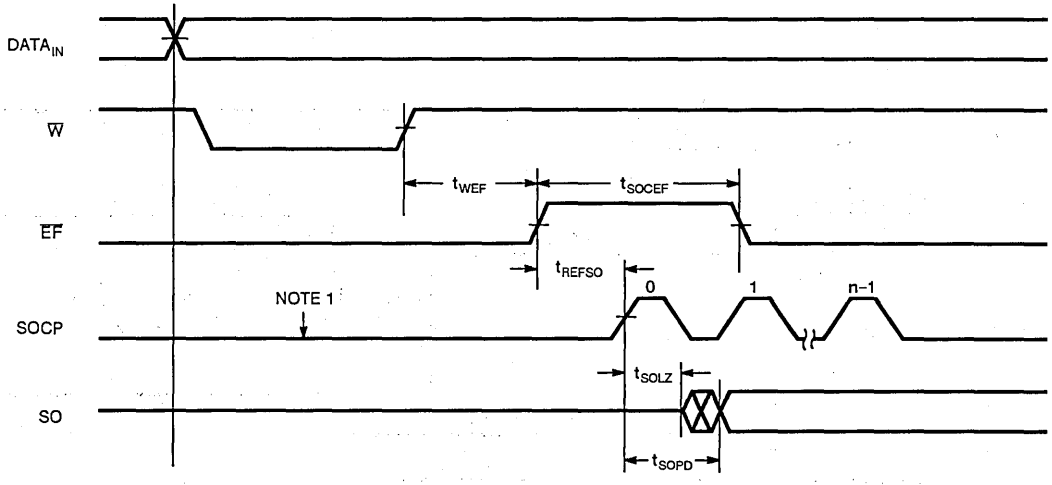


Figure 5. Empty Boundry Condition Timing

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

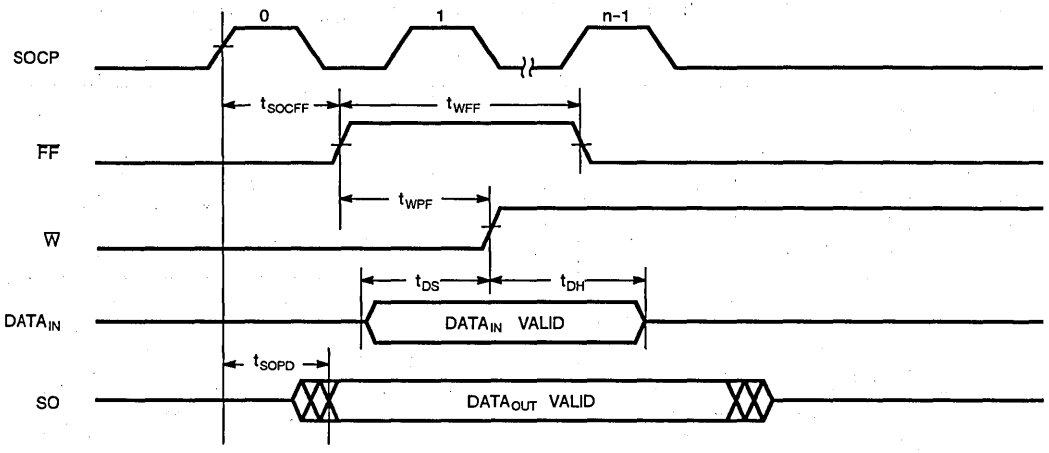


Figure 6. Full Boundry Condition Timing

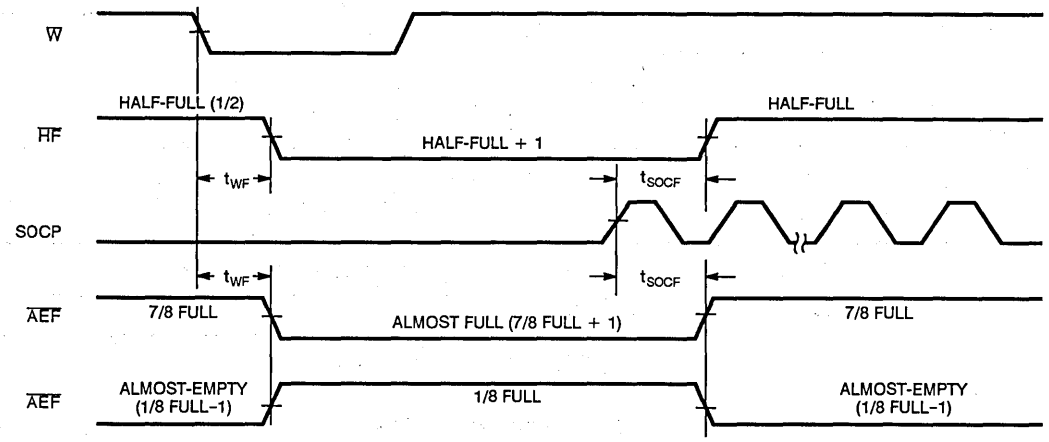


Figure 7. Half Full, Almost Full and Almost Empty Timings

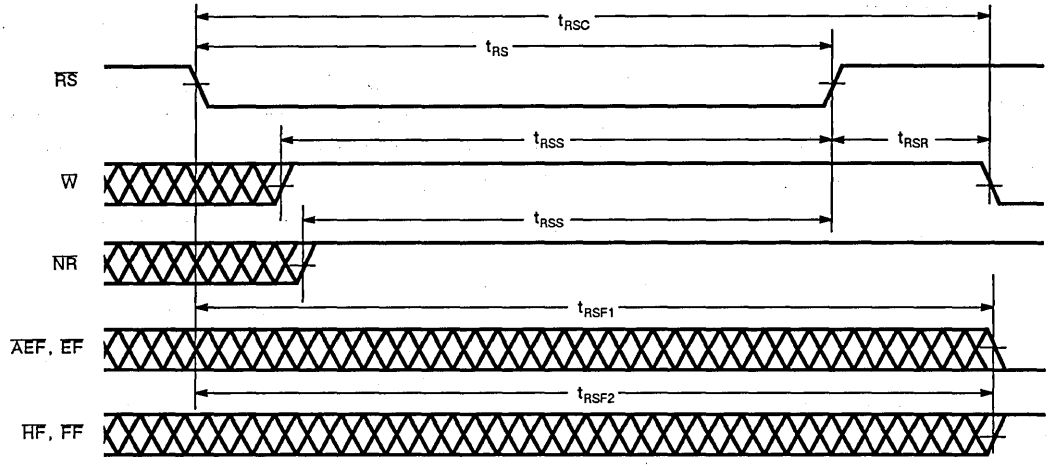


Figure 8. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{NR}$ is set high by SOCP staying low at the completion of a serial word.

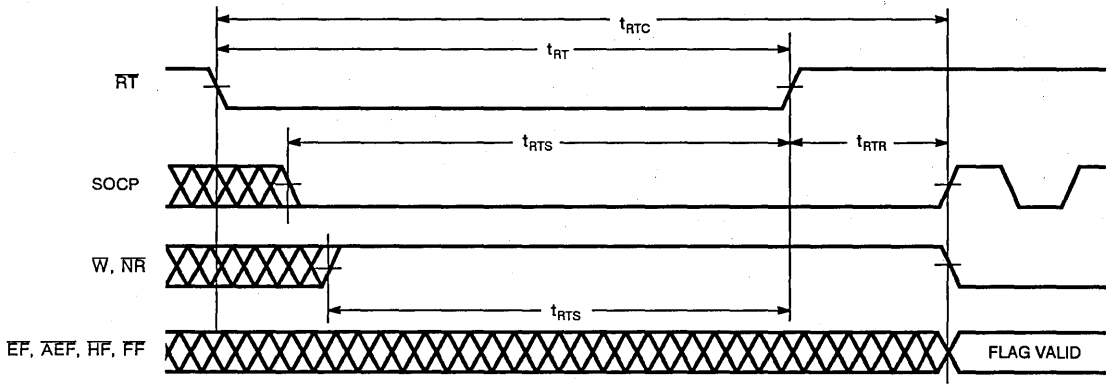


Figure 9. Retransmit

NOTE:
1. $\overline{EF}$, $\overline{AEF}$, $\overline{HF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

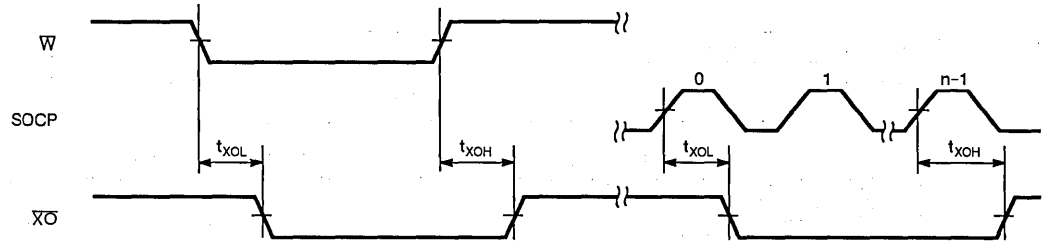


Figure 10. Expansion-Out

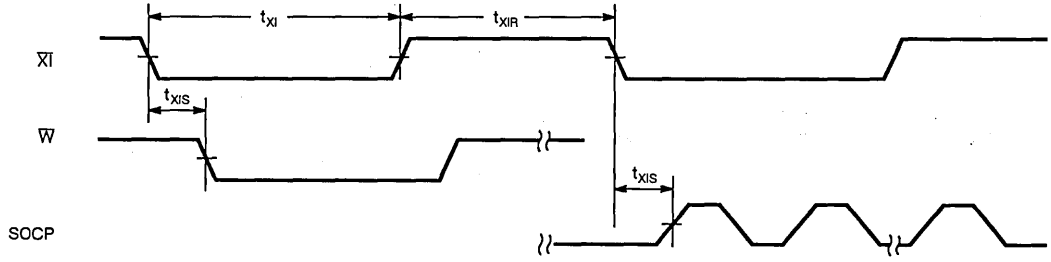


Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q_4, Q_8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SOCP clock pulse. This continues until the Q line connected to NR goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

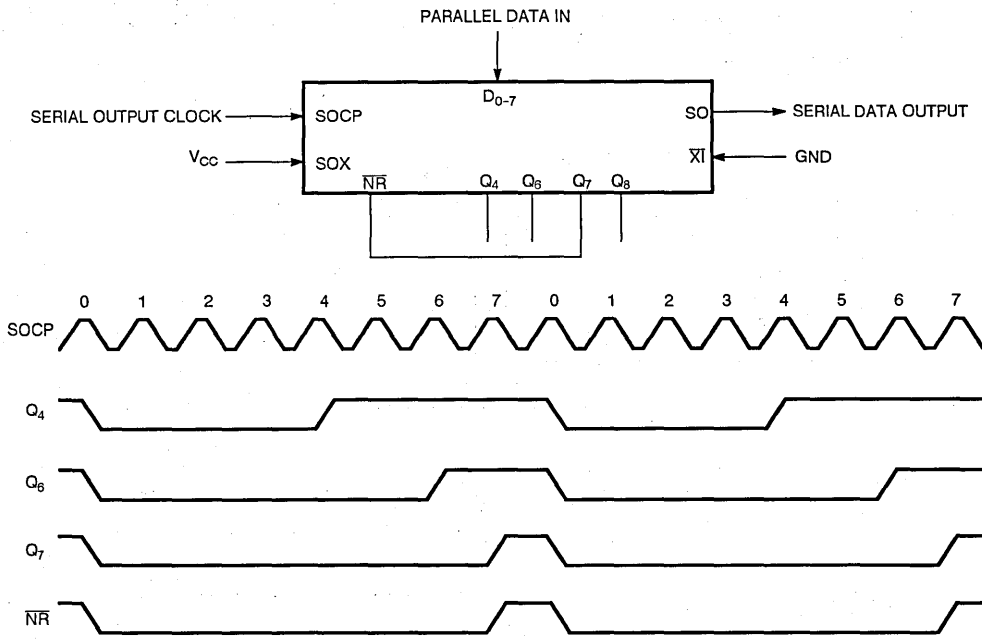


Figure 12. Eight-Bit Word Single Device Configuration

TRUTH TABLES
TABLE 1: RESET AND RETRANSMIT– SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all the lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

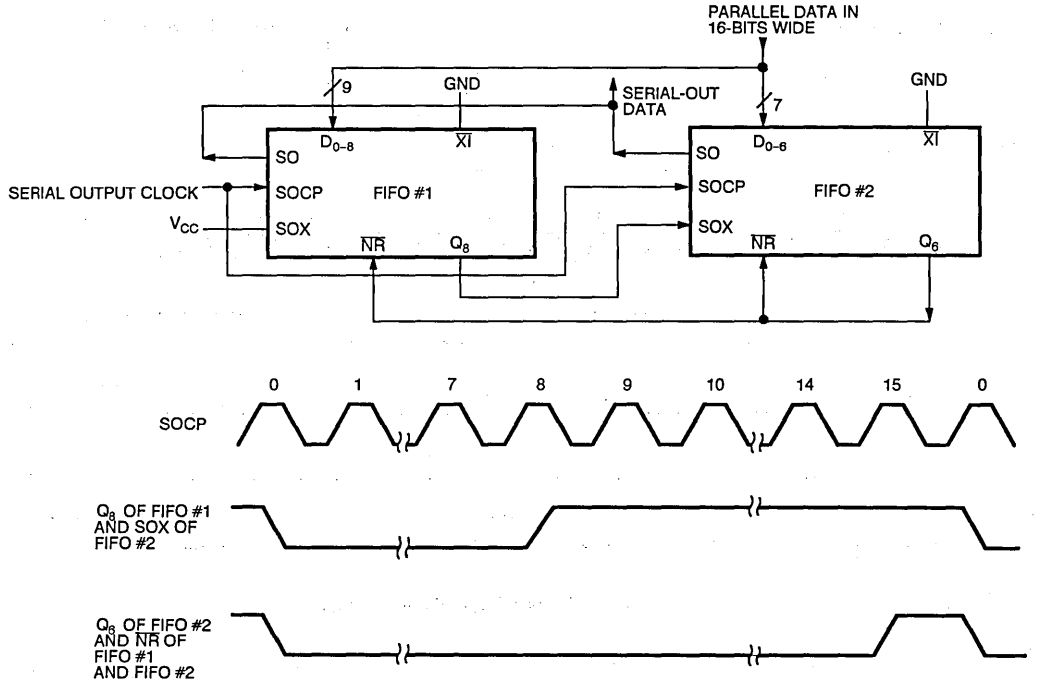


Figure 13. Width Expansion for 16-bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2

Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41. The IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

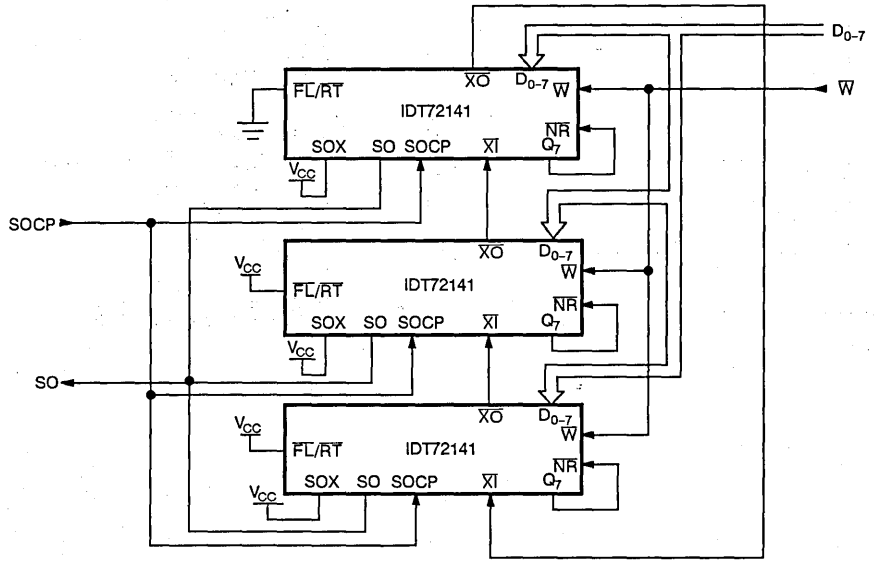


Figure 14. An 12K x 8 Parallel-In Serial-Out FIFO

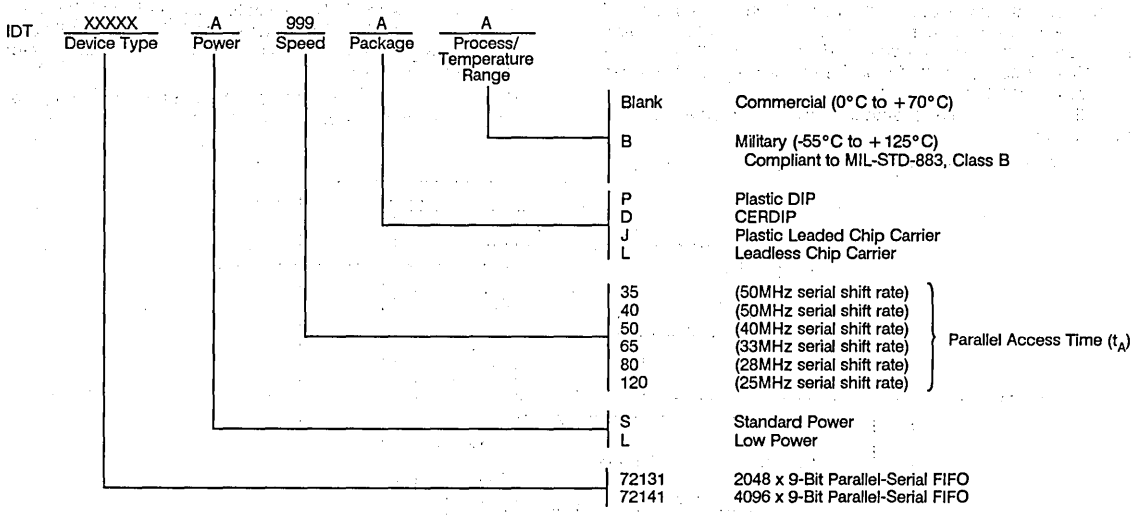
TABLE 2: RESET AND FIRST LOAD TRUTH TABLE – DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS SERIAL-TO-PARALLEL FIFO 2048 x 9 BIT & 4096 x 9 BIT

IDT 72132
IDT 72142

FEATURES:

- 35ns parallel port access time
- 50 MHz serial port shift rate
- Easily expandable in depth and width
- Programmable word lengths including 8, 9, 16-18, and 32-36 bits using Flexishift™ serial input without any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost-Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CEMOS™ technology
- Available in a 28-pin ceramic and plastic DIP, 32-pin LCC and J-leaded PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDT's parallel-to-serial FIFOs (IDT72131/72141) for bidirectional serial data buffering.

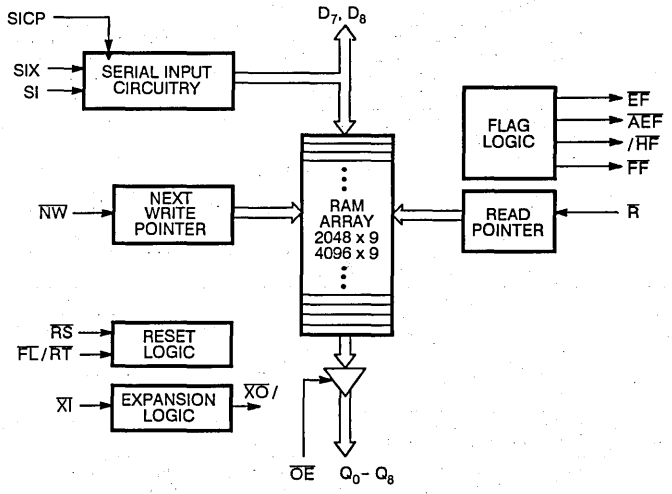
The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDT's unique Flexishift™ serial expansion logic (SIX, NW) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost-Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

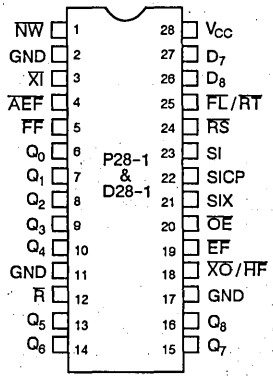
6

FUNCTIONAL BLOCK DIAGRAM

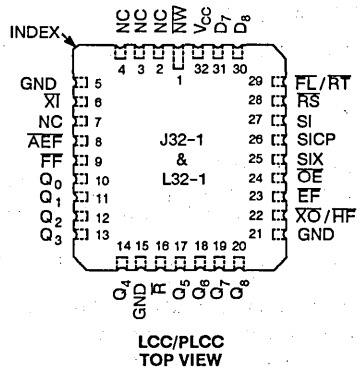


CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
SI	Serial Input	I	Serial data is shifted in least significant bit first. In the serial cascade mode, the Serial Input (SI) pins are tied together and SIX plus D7, D8 determine which device stores the data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ must be high during a $\overline{RS}$ cycle.
$\overline{NW}$	Next Write	I	To program the Serial In word width, connect $\overline{NW}$ with one of the Data Set pins (D7, D8)
SICP	Serial Input Clock	I	Serial data is read into the serial input register on the rising edge of SICP. In both Depth and Serial Word Width Expansion modes, all of the SICP pins are tied together.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of SICP. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked and Q0 - Q8 are in a high impedance condition.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. SOCP and W must be high before setting $\overline{FL}/\overline{RT}$ low. Retransmit is not possible in depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SIX	Serial Input Expansion	I	In the Expansion mode, SIX pin is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SIX pin (or pins) tied to the D8 pin of the device that will source the next lower order bits of the serial word. For single device operation, SIX is tied high.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three state buffers inhibit data flow.
Q0 - Q8	Data Output	O	Data outputs for 9-bit wide data
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and data must not be clocked in by SOCP. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Almost-Empty/ Almost-Full Flag	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
D7, D8	Data Set	O	The appropriate Data Set pin (D7, D8) is connected to $\overline{NW}$ to program the Serial In data word width. For example: Q7 - $\overline{NW}$ programs a 8-bit word width, Q8 - $\overline{NW}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

STATUS FLAGS

NUMBER OF WORDS IN FIFO		$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
IDT72132	IDT72142				
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC}= 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC}= 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT72132/IDT72142 COMMERCIAL			IDT72132/IDT72142 MILITARY			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	–	100	160	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current	–	–	8	–	–	12	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $\overline{R}$ = V_{CC}-0.2V; all other inputs ≥ V_{CC}-0.2V or ≤ 0.2V

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		MILITARY AND COMMERCIAL										UNIT
		72132x35 72142x35		72132x40 72142x40		72132x50 72142x50		72132x65 72142x65		72132x80 72142x80		72132x120 72142x120				
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_S	Parallel Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7			MHz
t_{SICP}	Serial-In Shift Frequency	–	50	–	50	–	40	–	33	–	28	–	25			MHz
t_A	Access Time	–	35	–	40	–	50	–	65	–	80	–	120			ns
t_{RR}	Read Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–			ns
t_{RPW}	Read Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RC}	Read Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–			ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	5	–	5	–	10	–	10	–	10	–	10	–			ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	–	20	–	25	–	30	–	30	–	35	–	35			ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–			ns
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	–	15	–	15	–	15	–	20	–	25	–	30			ns
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	–	5	–	5	–	5	–	5	–	5	–			ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	–	20	–	20	–	22	–	25	–	30	–	35			ns
t_{SIS}	Serial Data in Set-up Time to SICP Rising Edge	12	–	12	–	15	–	15	–	20	–	20	–			ns
t_{SIH}	Serial Data in Hold Time to SICP Rising Edge	0	–	0	–	0	–	0	–	5	–	5	–			ns
t_{SIX}	SIX Set-Up Time to SICP Rising Edge	5	–	5	–	5	–	5	–	5	–	5	–			ns
t_{SICW}	Serial in Clock Width High/Low	8	–	8	–	10	–	10	–	15	–	15	–			ns
t_{SICEF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{EF}$ High	–	45	–	50	–	65	–	80	–	80	–	80			ns
t_{SICFF}	SICP Rising Edge (Bit 0 - First Word) to $\overline{FF}$ Low	–	30	–	35	–	40	–	50	–	60	–	60			ns
t_{SICF}	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	–	45	–	50	–	65	–	80	–	80	–	80			ns
t_{RFFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	15	–	15	–	15	–	15	–	20	–	20	–			ns
t_{REF}	Read Low to $\overline{EF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60			ns
t_{RFF}	Read High to $\overline{FF}$ High	–	30	–	35	–	45	–	60	–	60	–	60			ns
t_{RF}	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140			ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RSC}	Reset Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–			ns
t_{RS}	Reset Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RSS}	Reset Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RSR}	Reset Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–			ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140			ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	–	45	–	50	–	65	–	80	–	100	–	140			ns
t_{RTC}	Retransmit Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–			ns
t_{RT}	Retransmit Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RTS}	Retransmit Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–			ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	35	–	40	–	50	–	65	–	80	–	120			ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	35	–	40	–	50	–	65	–	80	–	120			ns
t_{XI}	$\overline{XI}$ Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–			ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–			ns
t_{XIS}	$\overline{XI}$ Set-up Time	16	–	15	–	15	–	15	–	15	–	15	–			ns

NOTE:

1. Guaranteed by design minimum times, not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

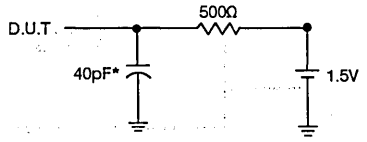


Figure A. Output Load.

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Serial Data Input

The serial data is input on the SI pin. The data is clocked in on the rising edge of SICP providing the Full Flag ($\overline{FF}$) is not asserted. If the Full Flag is asserted then the next data word is inhibited from moving into the RAM array. NOTE: SICP should not be clocked while the Full Flag is low. If it is, then the input data will be lost.

The serial word is shifted in Least Significant Bit first. Thus, when the FIFO is read, the Least Significant Bit will come out on Q0 and the second bit is on Q1 and so on. The serial word width must be programmed by connecting the appropriate Data Set line (D7, D8) to the $\overline{NW}$ input. The data set lines are taps of a digital delay line. Selecting one of these taps, programs the width of the serial word to be read in.

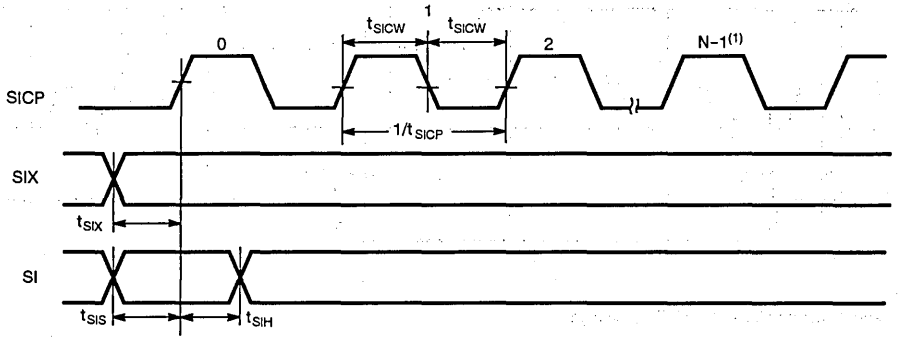


Figure 1. Write Operation

Parallel Data Output

A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. The data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$.

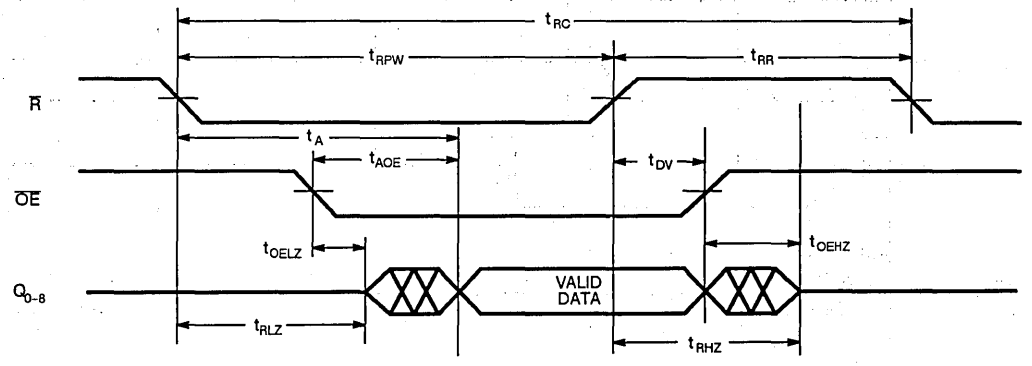


Figure 2. Read Operation

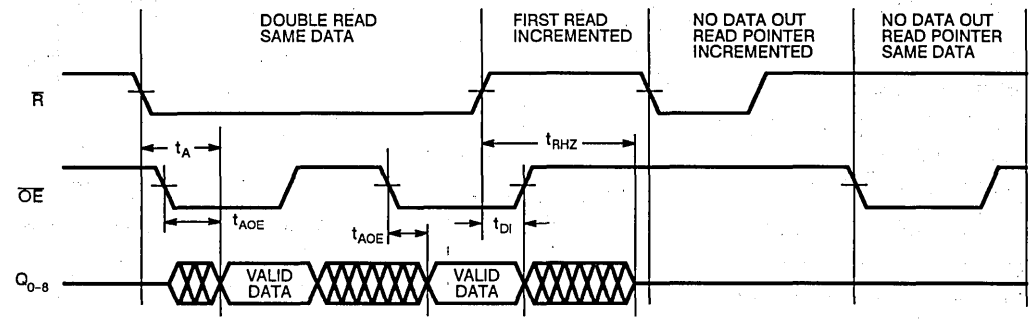
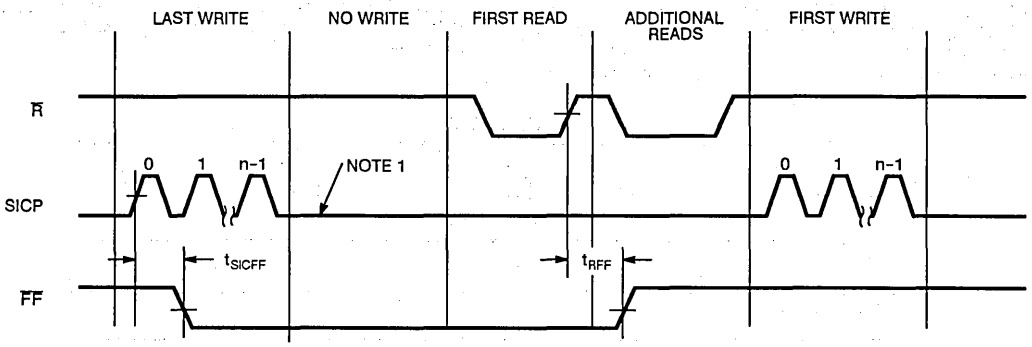


Figure 3. Read and Output Enable Timings



NOTE:
1. SICP should not be clocked until $\overline{FF}$ goes high.

Figure 4. Full Flag from Last Write to First Read

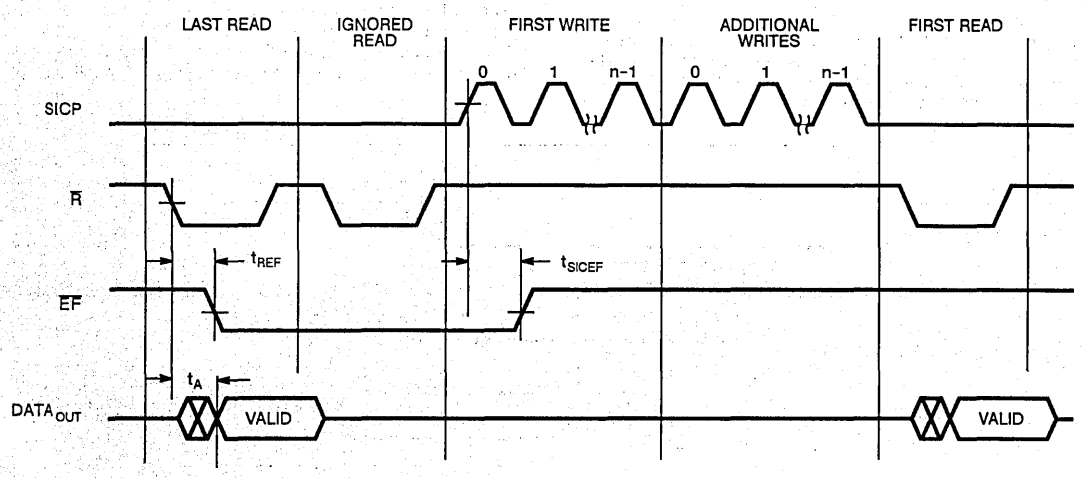


Figure 5. Empty Flag from Last Read to First Write

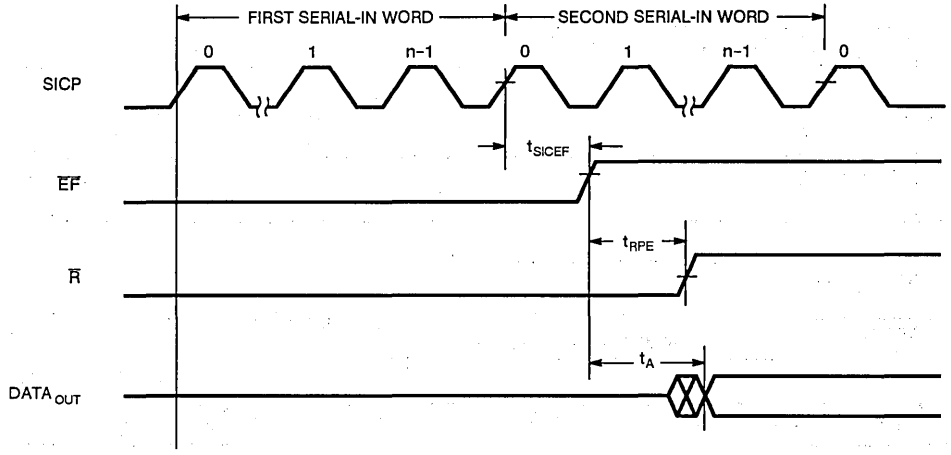
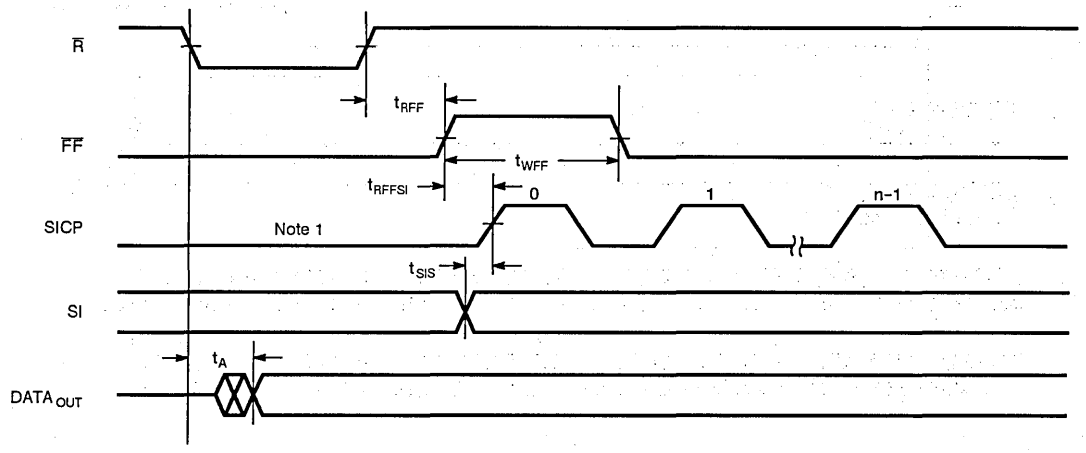


Figure 6. Empty Boundry Condition Timing



NOTE:
1. SICP must remain low until after $\overline{FF}$ goes high.

Figure 7. Full Boundry Condition Timing

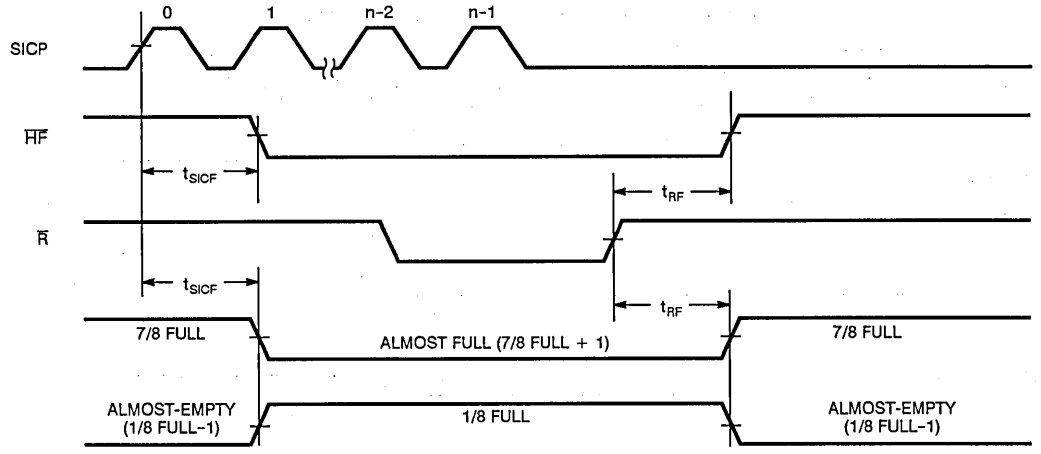
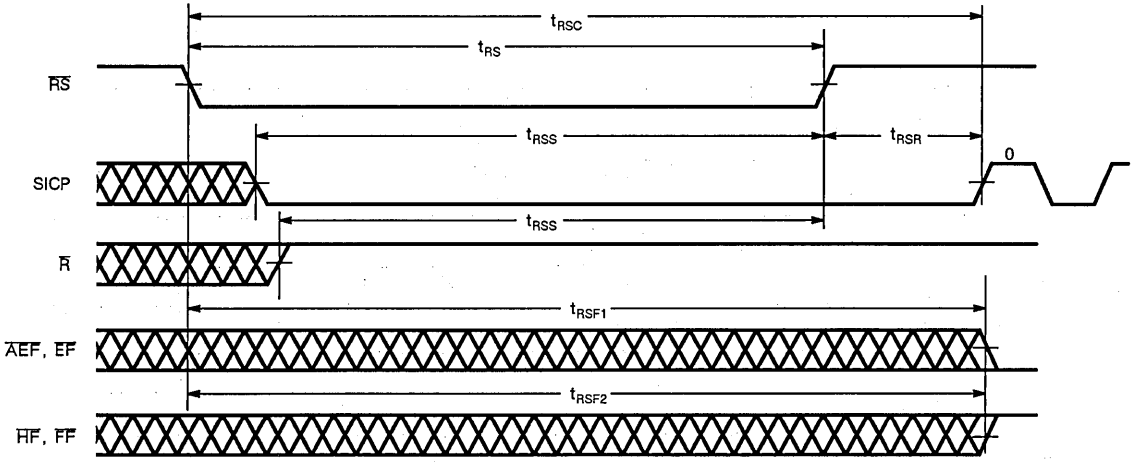
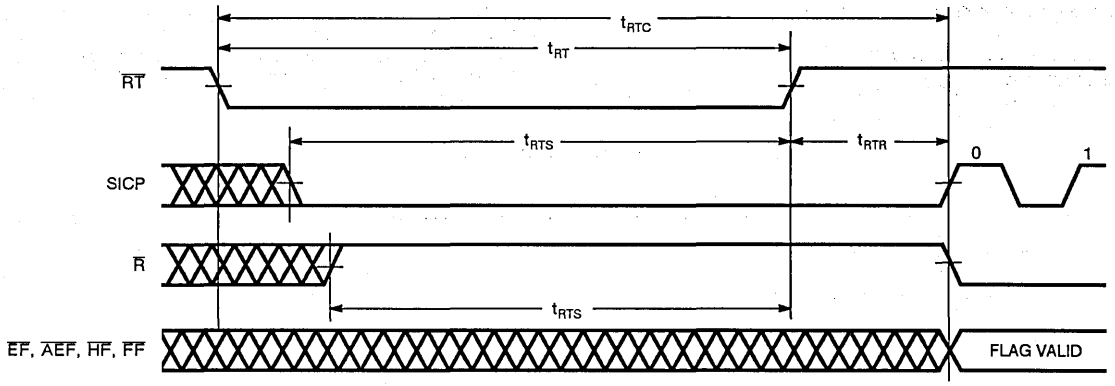


Figure 8. Half Full, Almost Full and Almost Empty Timings



NOTE:
1. EF, FF and HF may change status during Reset, but flags will be valid at t_{RSC}.

Figure 9. Reset



NOTE:
1. $\overline{EF}$, $\overline{AEF}$, $\overline{HF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 10. Retransmit

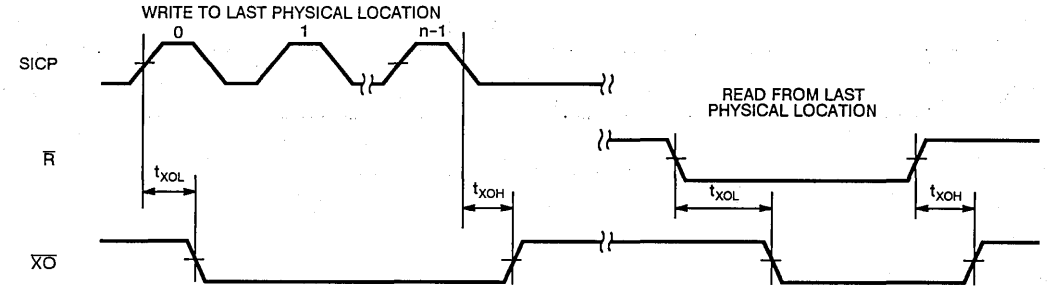


Figure 11. Expansion-Out

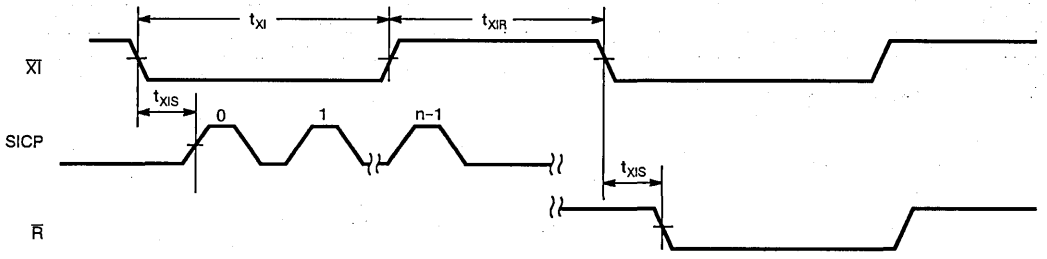


Figure 12. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SIX line is tied HIGH and not used. On the first LOW-to-HIGH of the SICP clock, both of the Data Set lines (D_7, D_8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SICP clock pulse. This continues until the D line connected to $\overline{NW}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SICP.

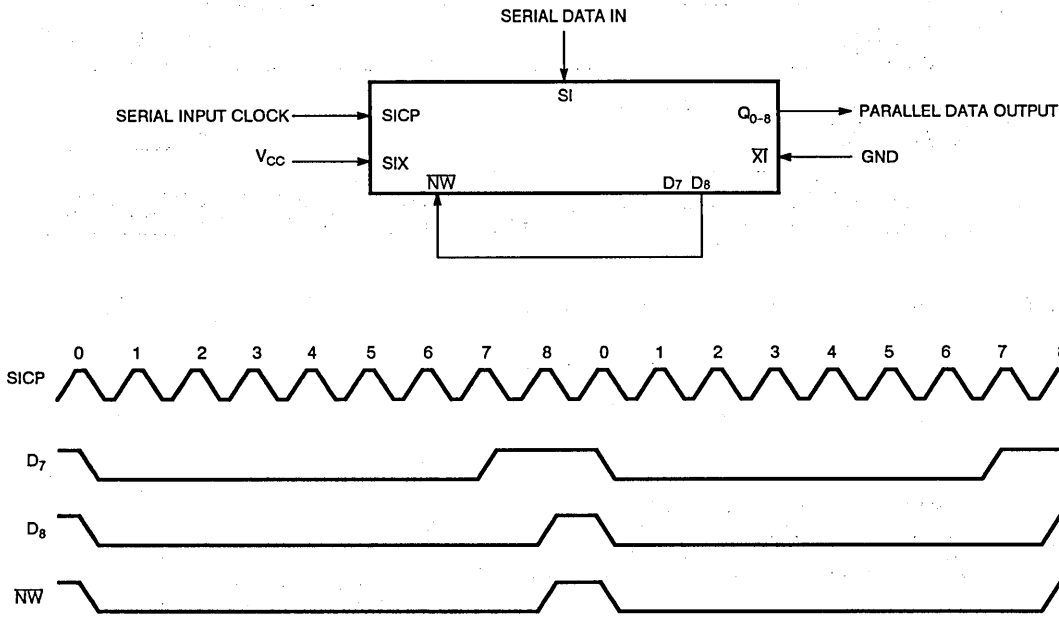


Figure 13. Nine-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT– SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SIX line of the least significant device HIGH and the SIX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SICP, both the Data Set lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant.

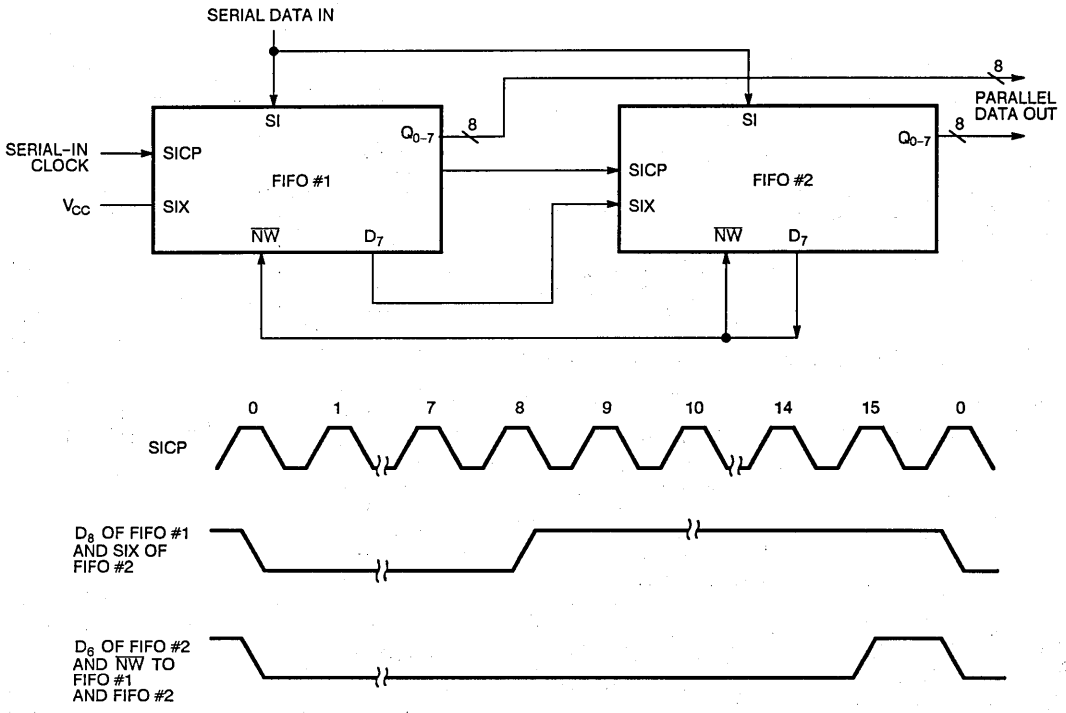


Figure 14. Serial-In to Parallel-Out Data of 16 Bits

Depth Expansion (Daisy Chain) Mode

The IDT72132/42 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 15 demonstrates Depth Expansion using three IDT72132/42. Any depth can be attained by adding additional IDT72132/42. The IDT72132/42 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have in the high state.
3. The Expansion Out ($\overline{XO}$) pin and Expansion In ($\overline{XI}$) pin of each device must be tied together.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite ($\overline{FF}$) or ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

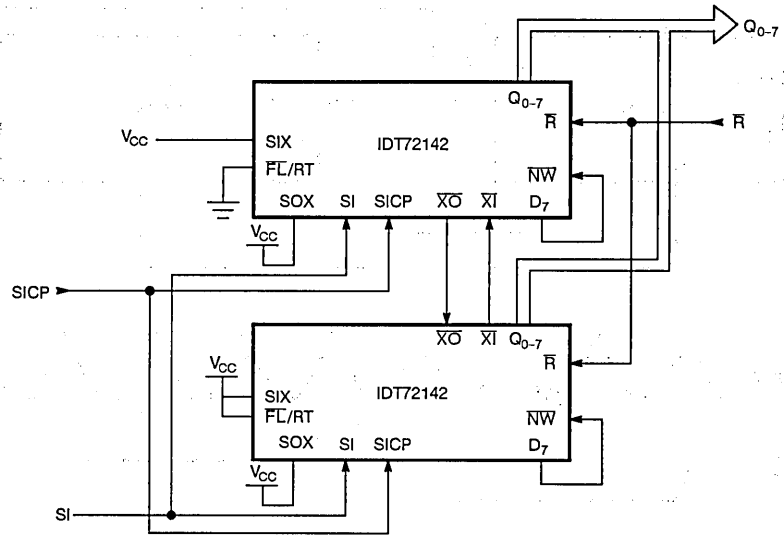


Figure 15. An 8K x 8 Serial-In Parallel-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE – DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION

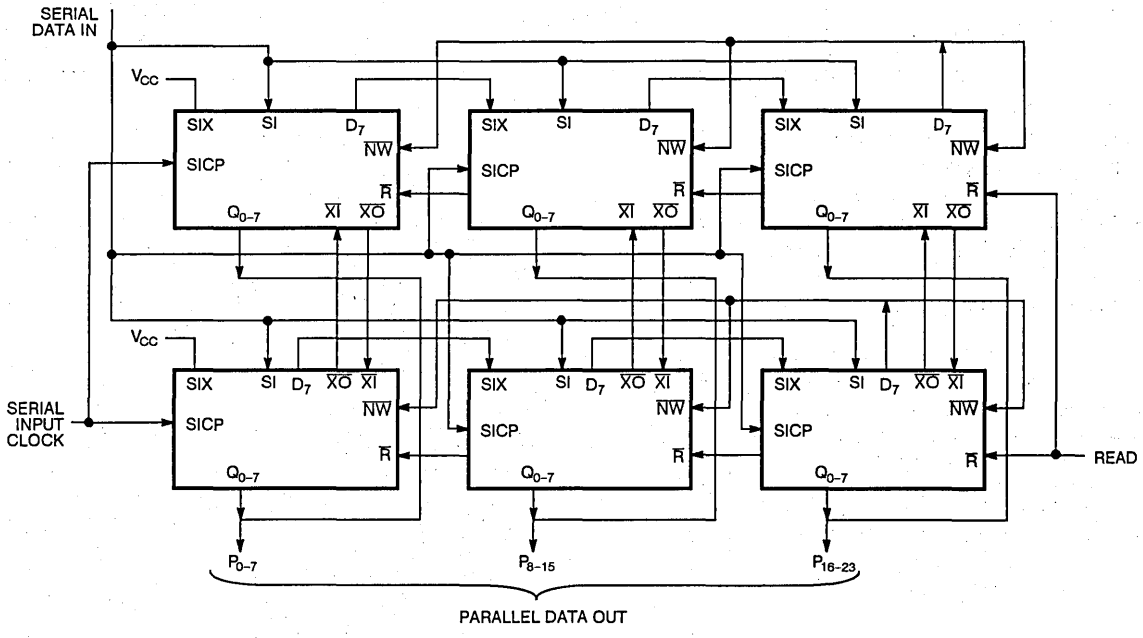


Figure 16. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72142s

ORDERING INFORMATION

IDT — XXXXX Device Type — A Power — 999 Speed — A Package — A Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
35	(50MHz serial shift rate)
40	(50MHz serial shift rate)
50	(40MHz serial shift rate)
65	(33MHz serial shift rate)
80	(28MHz serial shift rate)
120	(25MHz serial shift rate)
	Parallel Access Time (t_A)
S	Standard Power
L	Low Power
72132	2048 x 9-Bit Parallel-Serial FIFO
72142	4096 x 9-Bit Parallel-Serial FIFO

Integrated Device Technology, Inc.

1024 x 18-BIT 512 x 18-BIT CMOS SYNCHRONOUS FIFO

ADVANCE INFORMATION
IDT72215M/S
IDT72225M/S

FEATURES:

- 1024 x 18-bit and 512 x 18-bit memory array structures
- 20ns read/write cycle time
- Easily expandable in depth and width
- Read and write clocks can be independent or coincident
- Dual-ported zero fall-through time architecture
- Empty and full flags signal FIFO status
- Programmable almost-empty and almost-full flags can be set to any depth
- Almost-empty and almost-full flags work in depth expansion
- Output enable puts output data bus in high-impedance state
- Low power consumption
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in a 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

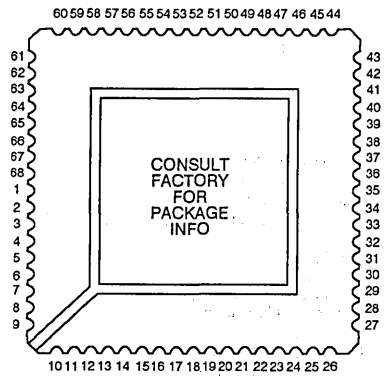
The IDT72215 and IDT72225 are very high-speed, low-power first-in, first-out (FIFO) memories with synchronous read and write controls. The IDT72215 has a 512 x 18-bit memory array, while the IDT72225 has a 1024 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is clocked into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run independent of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

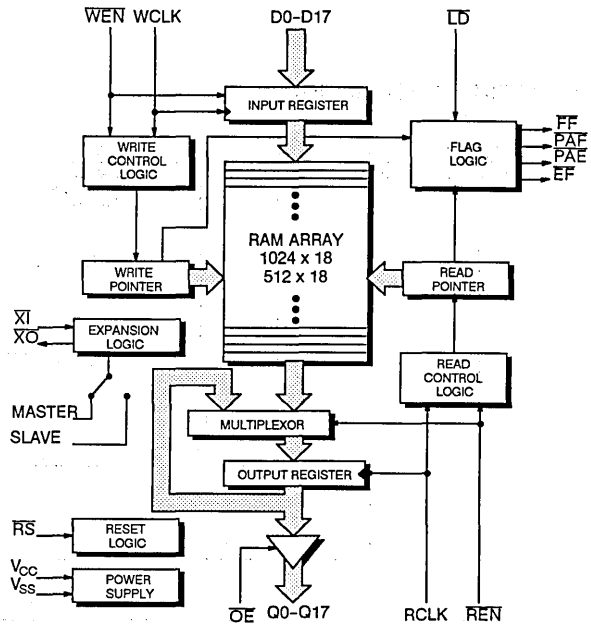
The synchronous FIFOs have two fixed flags, empty ($\overline{EF}$) and full ($\overline{FF}$), and two programmable flags, almost-empty ($\overline{PAE}$) and almost-full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$).

The IDT72215 and IDT72225 are depth expandable using a daisy-chain technique. The pins $\overline{XI}$ and $\overline{XO}$ are used to expand the FIFOs. To permit programmable flags in depth expansion, a master component (IDT72215/225M) controls the flags, and the flags are ignored on all the other slave components (IDT72215/225S).

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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DSC-2037/-

Integrated Device Technology, Inc.

CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

IDT 72401
IDT 72402
IDT 72403
IDT 72404

FEATURES:

- First-In/First-Out dual-port memory
- 64 x 4 organization (IDT72401/03)
- 64 x 5 organization (IDT72402/04)
- IDT72401/02 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low power consumption
  - Active: 175mW (typ.)
- Maximum shift-rate—45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth at 35MHz
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in CERDIP, plastic DIP and SOIC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86846 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous, high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous, high-performance First-In/First-Out memories organized as 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input (D_0-$D_{3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output contains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The Output Ready signal can also be used to cascade multiple devices together.

Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

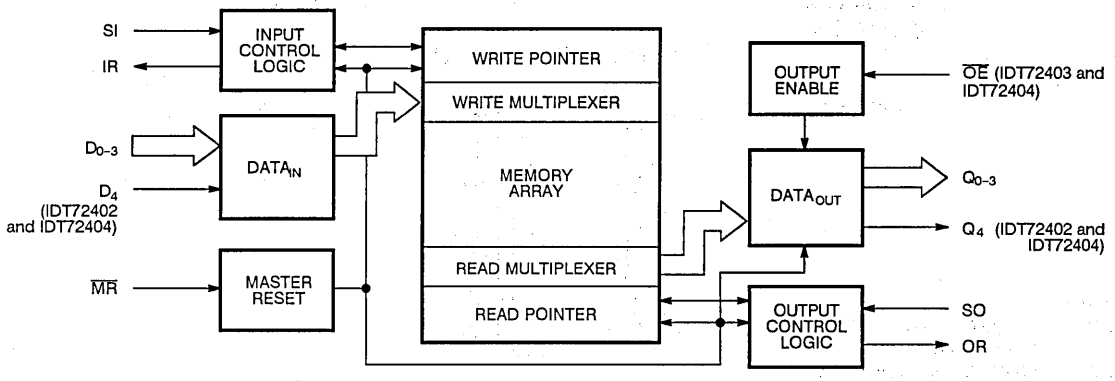
Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM



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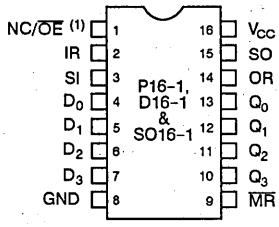
DSC-2011/1

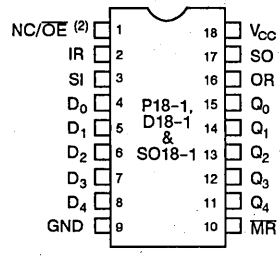
PIN CONFIGURATIONS

IDT72401
IDT72403

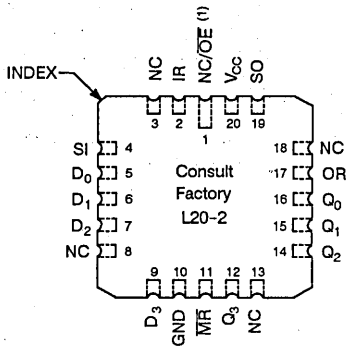


DIP/SOIC
TOP VIEW

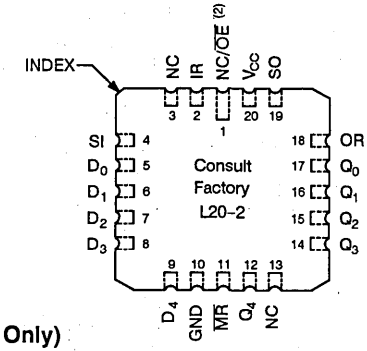
IDT72402
IDT72404



DIP/SOIC
TOP VIEW

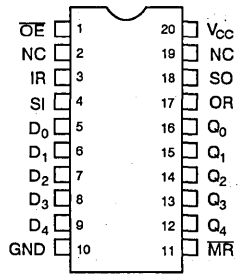


LCC
TOP VIEW



LCC
TOP VIEW

Cerpack (IDT72404 Only)



TOP VIEW

NOTES:
1. Pin 1: NC – No Connection IDT72401
   $\overline{OE}$ – IDT72403
2. Pin 1: NC – No Connection IDT72402
   $\overline{OE}$ – IDT72404

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL} (1)	Input High Voltage	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IC} (1)	Input Clamp Voltage		–	–	–
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}	-10	–	µA
I_{IH}	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}	–	+10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V
I_{OS} (2)	Output Short-Circuit Current	V_{CC} = Max., V_O = GND	-20	-90	mA
I_{HZ}	Off-State Output Current (IDT72403 and IDT72404)	V_{CC} = Max., V_O = 2.4V	–	+20	µA
I_{LZ}		V_{CC} = Max., V_O = 0.4V	-20	–	µA
I_{CC} (3, 4)	Supply Current	V_{CC} = Max.: f = 10MHz Commercial Military	– –	35 45	mA

NOTES:
1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Guaranteed but not tested.
3. I_{CC} measurements are made with outputs open. $\overline{OE}$ is HIGH for IDT72403/72404.
4. For frequencies greater than 10MHz, I_{CC} = 35mA + (1.5mA x [f - 10MHz]) commercial, and I_{CC} = 40mA + (1.5mA x [f - 10MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL		MILITARY AND COMMERCIAL								UNIT
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45 MIN.	MAX.	IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35 MIN.	MAX.	IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25 MIN.	MAX.	IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15 MIN.	MAX.	IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10 MIN.	MAX.	
t_{SIH}[1]	Shift In HIGH Time	2	9	–	9	–	11	–	11	–	11	–	ns
t_{SIL}	Shift In LOW Time	2	11	–	17	–	24	–	25	–	30	–	ns
t_{IDS}	Input Data Set-up	2	0	–	0	–	0	–	0	–	0	–	ns
t_{IDH}	Input Data Hold Time	2	13	–	15	–	20	–	30	–	40	–	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	–	9	–	11	–	11	–	11	–	ns
t_{SOL}	Shift Out LOW Time	5	11	–	17	–	24	–	25	–	25	–	ns
t_{MRW}	Master Reset Pulse	8	20	–	25	–	25	–	25	–	30	–	ns
t_{MRS}	Master Reset Pulse to SI	8	10	–	10	–	10	–	25	–	35	–	ns
t_{SIR}	Data Set-up to IR	4	3	–	3	–	5	–	5	–	5	–	ns
t_{HIR}	Data Hold from IR	4	13	–	15	–	20	–	30	–	30	–	ns
t_{SOR}[4]	Data Set-up to OR HIGH	7	0	–	0	–	0	–	0	–	0	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL		MILITARY AND COMMERCIAL								UNIT
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45 MIN.	MAX.	IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35 MIN.	MAX.	IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25 MIN.	MAX.	IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15 MIN.	MAX.	IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10 MIN.	MAX.	
f_{IN}	Shift In Rate	2	–	45	–	35	–	25	–	15	–	10	MHz
t_{IRL}[1]	Shift In to Input Ready LOW	2	–	18	–	18	–	21	–	35	–	40	ns
t_{IRH}[1]	Shift In to Input Ready HIGH	2	–	18	–	20	–	28	–	40	–	45	ns
f_{OUT}	Shift Out Rate	5	–	45	–	35	–	25	–	15	–	10	MHz
t_{ORL}[1]	Shift Out to Output Ready LOW	5	–	18	–	18	–	19	–	35	–	40	ns
t_{ORH}[1]	Shift Out to Output Ready HIGH	5	–	18	–	20	–	34	–	40	–	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	–	5	–	5	–	5	–	5	–	ns
t_{ODS}	Output Data Shift (Next Word)	5	–	20	–	25	–	35	–	55	–	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	–	25	–	28	–	40	–	65	–	65	ns
t_{MRORL}	Master Reset to OR LOW	8	–	25	–	28	–	35	–	35	–	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	–	25	–	28	–	35	–	35	–	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	–	20	–	20	–	25	–	35	–	40	ns
t_{OOE}[3]	Output Valid from $\overline{OE}$ LOW	9	–	12	–	15	–	20	–	30	–	35	ns
t_{HZOE}[3,4]	Output HIGH-Z from $\overline{OE}$ HIGH	9	–	12	–	12	–	15	–	25	–	30	ns
t_{IPH}[2,4]	Input Ready Pulse HIGH	4	9	–	9	–	11	–	11	–	11	–	ns
t_{OPH}[2,4]	Output Ready Pulse HIGH	7	9	–	9	–	11	–	11	–	11	–	ns

NOTES:

1. Since the FIFO is a very high-speed device, care must be exercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 and IDT72404 only.
4. Guaranteed by design but not currently tested.

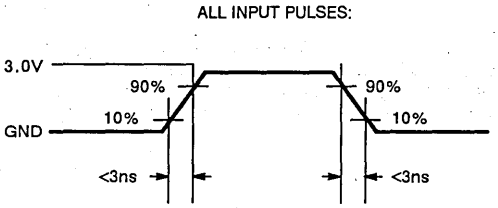
AC TEST CONDITIONS

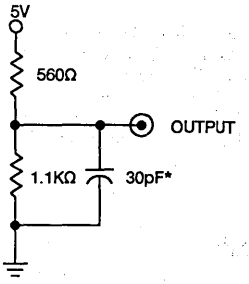
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently tested.





*Includes jig and scope capacitances.

Figure 1. AC Test Load

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT ($D_{0-3,4}$)

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input. The IDT72402 and IDT72404 have a 5-bit data input.

CONTROLS

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the $D_{0-3,4}$ lines.

SHIFT OUT (SO)

Shift Out controls the output of data out of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output ($Q_{0-3,4}$) lines.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output ($Q_{0-3,4}$) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE ($\overline{OE}$) (IDT72403 AND IDT72404 ONLY)

Output Enable is used to read FIFO data onto a bus. Output Enable is active LOW.

OUTPUTS

DATA OUTPUT ($Q_{0-3,4}$)

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output. The IDT72402 and IDT72404 have a 5-bit data output.

FUNCTIONAL DESCRIPTION

These 64 x 4 and 64 x 5 FIFOs are designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO Reset

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs ($Q_{0-3,4}$) will be LOW.

Data Input

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH, indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

Data Output

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFO's output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out. Previous data remains on the output until the HIGH-to-LOW transition of Shift Out (SO).

Fall-Through Mode

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO.

Since these FIFOs are based on an internal dual-port RAM architecture with separate read and write pointers, the fall-through time (t_{FT}) is one cycle long. A word may be written into the FIFO on a clock cycle and can be accessed on the next clock cycle.

TIMING DIAGRAMS

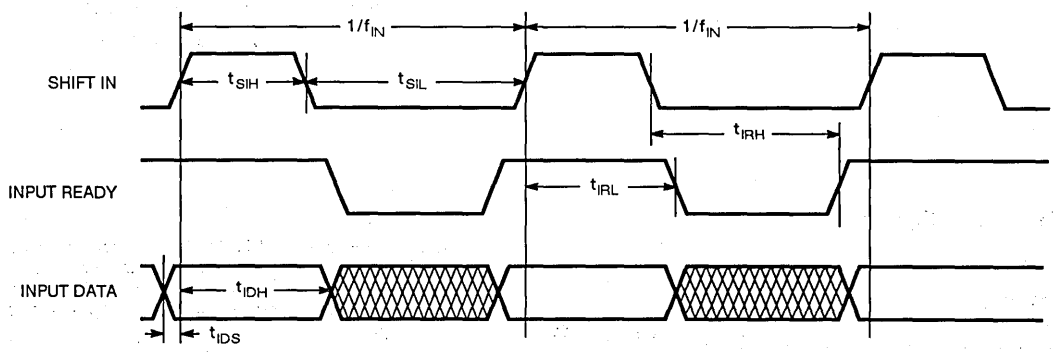
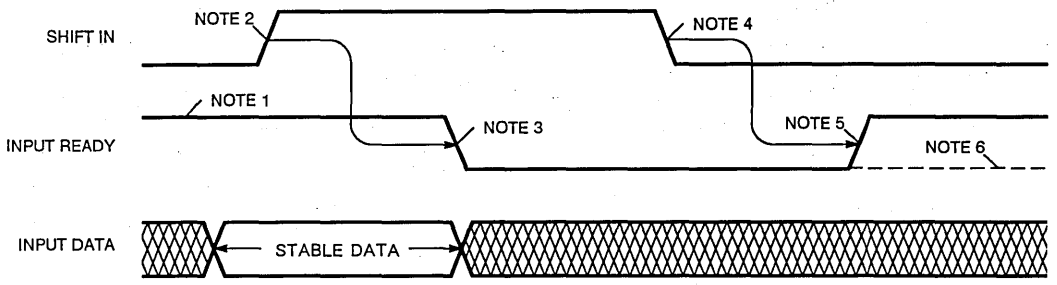


Figure 2. Input Timing

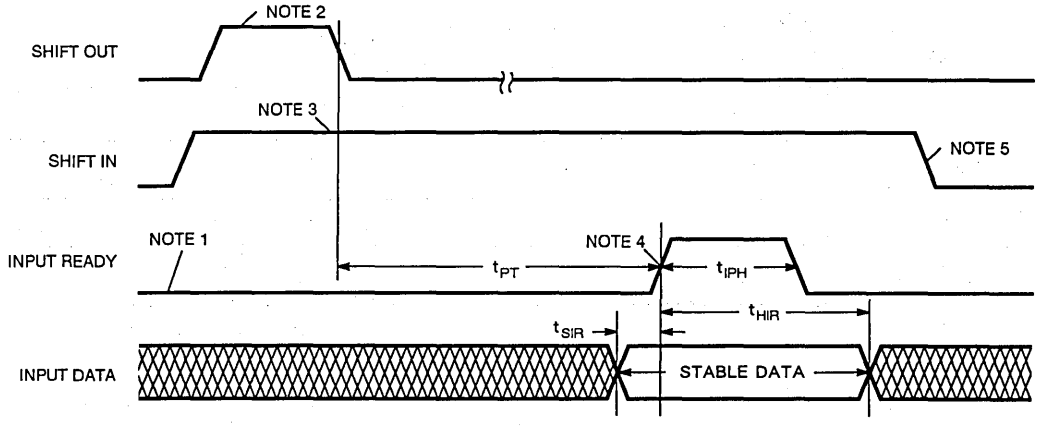
TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the Input Ready remains LOW.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

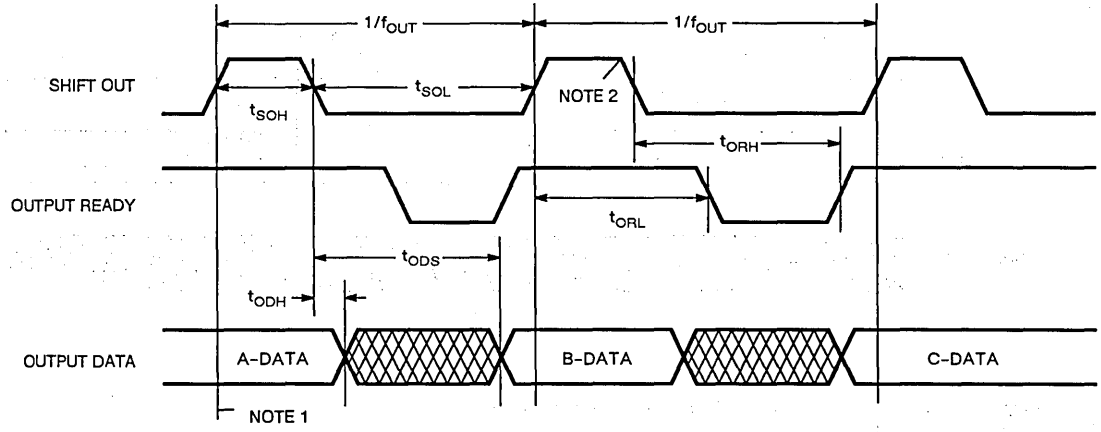
Figure 3. The Mechanism of Shifting Data Into the FIFO



NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented.

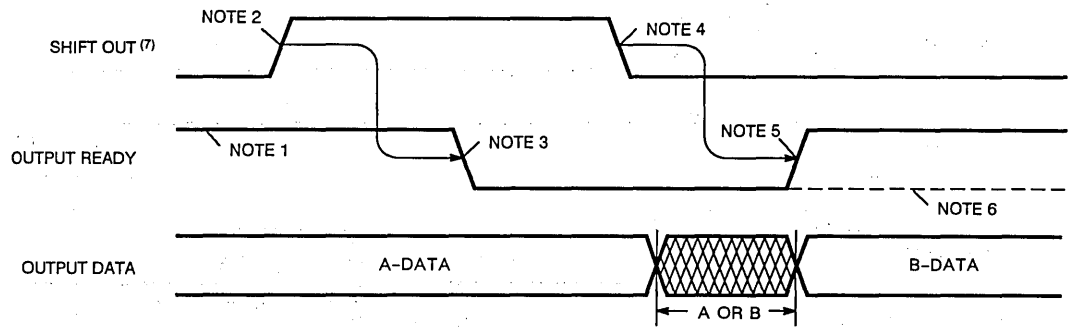
Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

TIMING DIAGRAMS (Continued)



NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

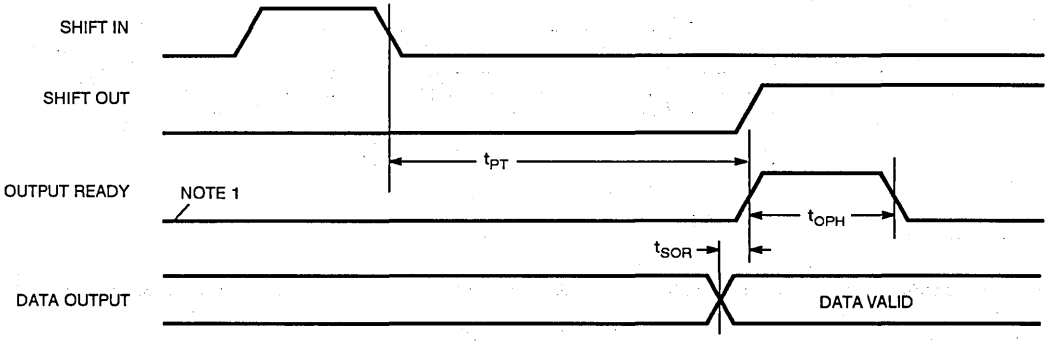
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then Output Ready stays LOW and the A DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

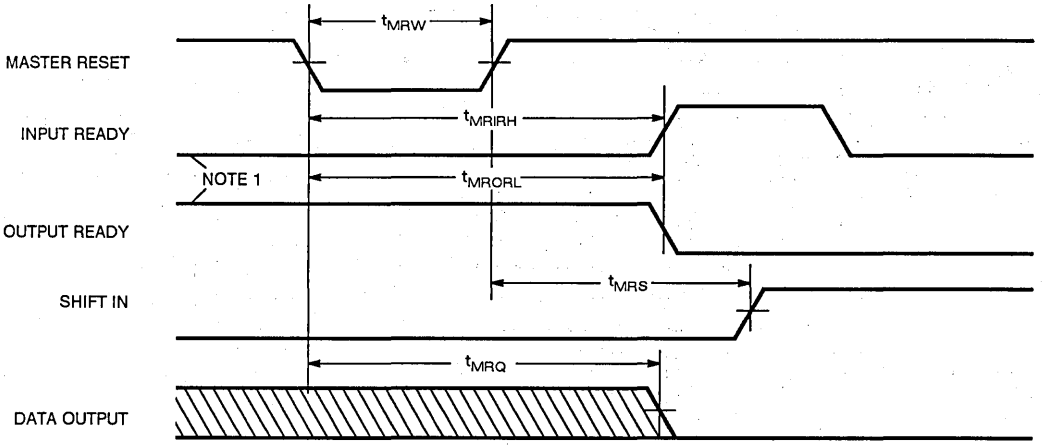
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



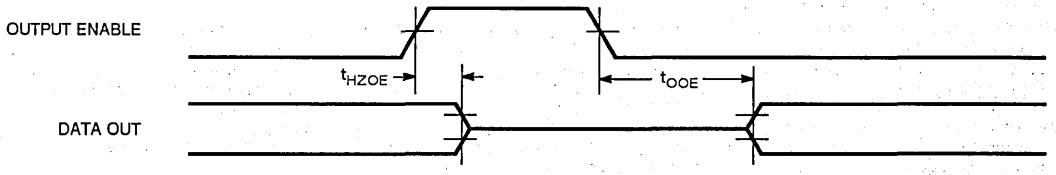
NOTE:
1. FIFO initially empty.

Figure 7. t_{PT} and t_{OPH} Specification



NOTE:
1. Worst case, FIFO initially full.

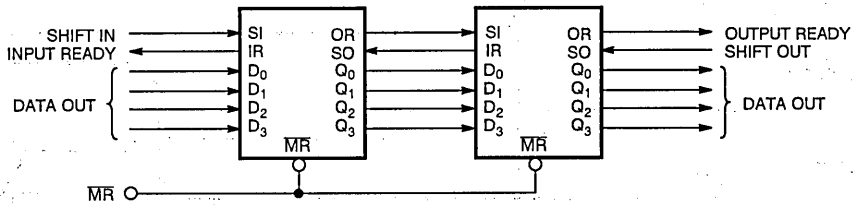
Figure 8. Master Reset Timing



NOTE:
1. High-Z transitions are referenced to the steady-state V_{OH} – 500mV and V_{OL} + 500mV levels on the output. t_{HZOE} is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

Figure 9. Output Enable Timing, IDT72403 and IDT72404 Only

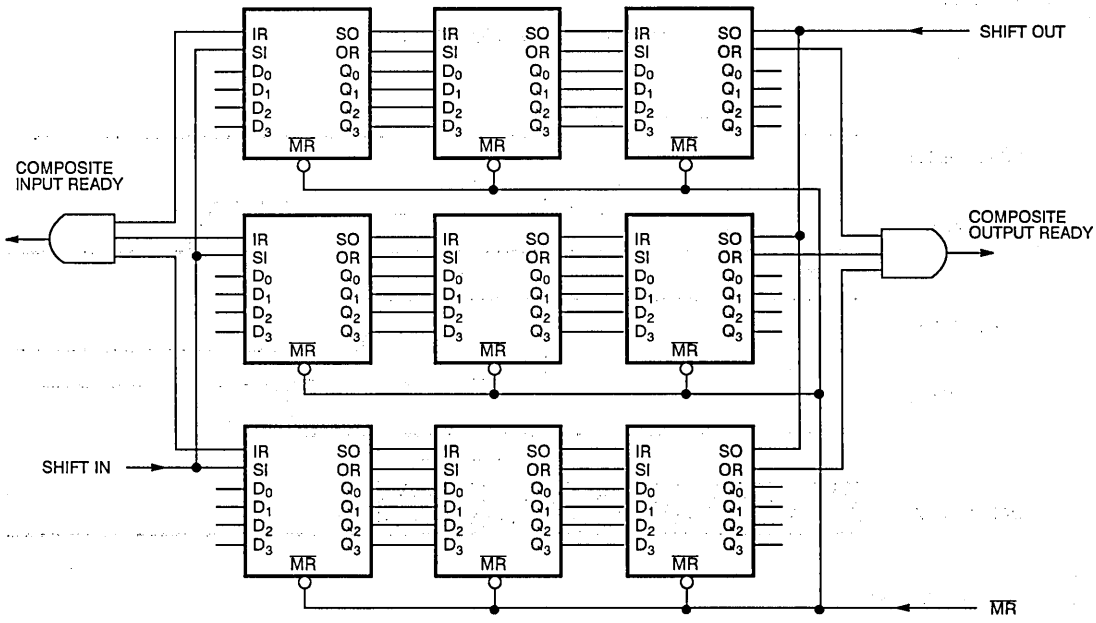
APPLICATIONS



NOTE:

1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 10. 128 x 4 Depth Expansion

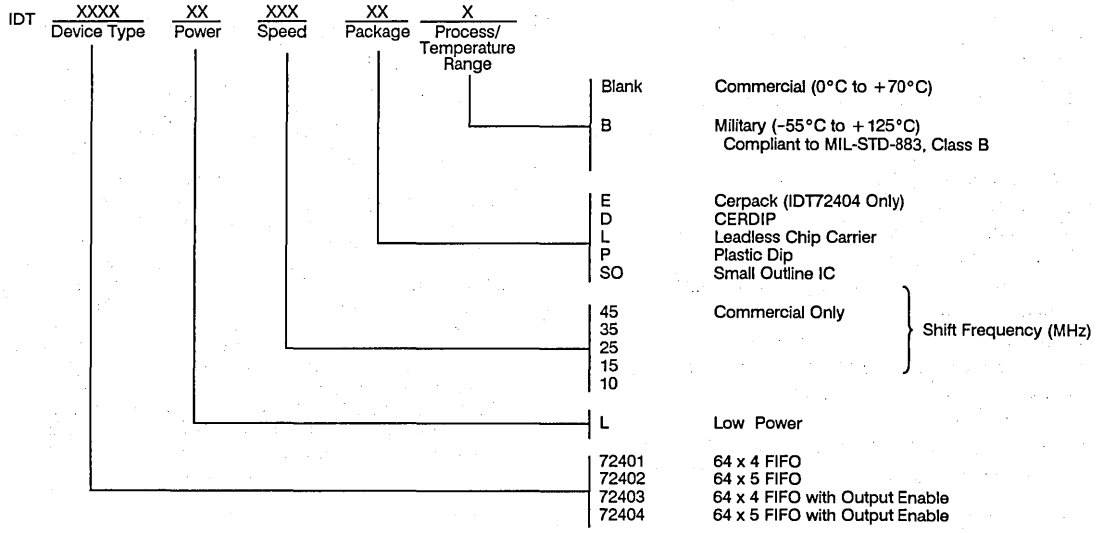


NOTES:

1. When the memory is empty, the last word read will remain on the outputs until the Master Reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the Master Reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the Master Reset goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the Master Reset is ended, IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT 72413

FEATURES:

- First-In/First-Out dual-port memory—45MHz
- 64 x 5 organization
- Low power consumption
  - Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth at 25MHz and 35MHz
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CEMOS ™ technology
- Available in plastic DIP, CERDIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72413 is a 64 x 5, high-speed First-In/First-Out (FIFO) that loads and empties data on a first-in/first-out basis. It is expandable in bit width. The IDT72413 25MHz and 35MHz versions are cascadable in depth.

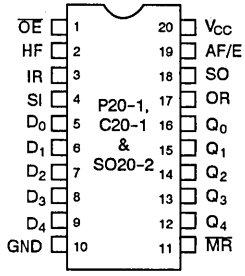
The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

The IDT72413 is pin and functionally compatible to the MMI 67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers

The IDT72413 is fabricated using IDT's high-performance CEMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

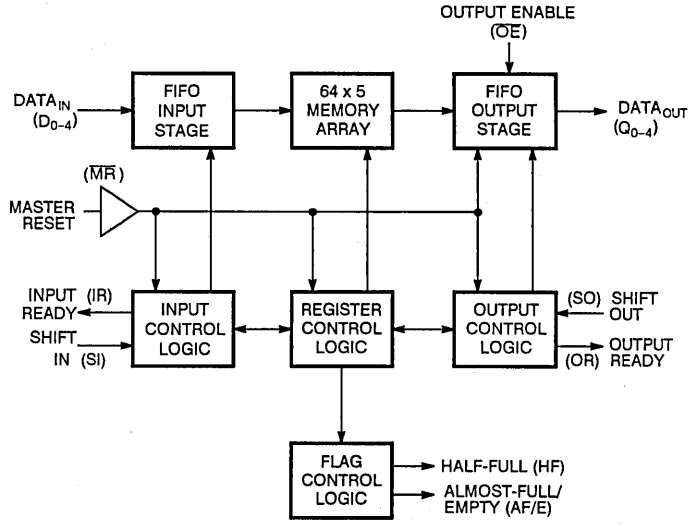
PIN CONFIGURATION



DIP/SOIC
TOP VIEW

LCC
(CONSULT FACTORY)
L20-2

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}[1]	Input Low Voltage	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	MAX.	UNIT
V_{IC}[1]	Input Clamp Voltage				–	–	
I_{IL}	Low-Level Input Current	V_{CC} = Max.; GND ≤ V_I ≤ V_{CC}			-10	–	µA
I_{IH}	High-Level Input Current	V_{CC} = Max.; GND ≤ V_I ≤ V_{CC}			–	10	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min.	I_{OL} (Q_{0-4})	MIL.	12mA	–	0.4	V
				COM'L.	24mA			
			I_{OL} (IR, OR)[2]		8mA			
			I_{OL} (HF, AF/E)		8mA			
V_{OH}	High-Level Output Voltage	V_{CC} = Min.	I_{OH} (Q_{0-4})		-4mA	2.4	–	V
			I_{OH} (IR, OR)		-4mA			
			I_{OH} (HF, AF/E)		-4mA			
I_{OS}[3]	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V			-20	-90	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max.	V_O = 2.4V			–	+20	µA
I_{LZ}		V_{CC} = Max.	V_O = 0.4V			-20	–	
I_{CC}[4]	Supply Current	V_{CC} = Max. Inputs LOW, $\overline{OE}$ = HIGH, f = 25MHz		MIL.		–	70	mA
				COM'L.		–	60	mA

NOTES:
1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25MHz.
3. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second. Guaranteed by design but not currently tested.
4. Frequencies greater than 25MHz, I_{CC} = 60mA + (1.5mA x [f - 25MHz]) commercial and I_{CC} = 70mA + (1.5mA x [f - 25MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	MILITARY AND COMMERCIAL				COMMERCIAL		UNIT
			IDT72413L45		IDT72413L35		IDT72413L25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{SIH}[1]	Shift In HIGH Time	2	9	–	9	–	16	–	ns
t_{SIL}[1]	Shift In LOW Time	2	11	–	17	–	20	–	ns
t_{IDS}	Input Data Set-Up	2	0	–	0	–	0	–	ns
t_{IDH}	Input Data Hold Time	2	13	–	15	–	25	–	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	–	9	–	16	–	ns
t_{SOL}	Shift Out LOW Time	5	11	–	17	–	20	–	ns
t_{MRW}	Master Reset Pulse	8	20	–	30	–	35	–	ns
t_{MRS}[3]	Master Reset to SI	8	20	–	35	–	35	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C, Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	FIGURE	MILITARY AND COMMERCIAL				COMMERCIAL		UNIT
			IDT72413L45		IDT72413L35		IDT72413L25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{IN}	Shift In Rate	2	–	45	–	35	–	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	–	18	–	18	–	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	–	18	–	20	–	25	ns
f_{OUT}	Shift Out Rate	5	–	45	–	35	–	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	–	18	–	18	–	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	–	18	–	20	–	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	–	5	–	5	–	ns
t_{ODS}	Output Data Shift Next Word	5	–	20	–	20	–	20	ns
t_{PT}[3]	Data Throughput or "Fall-Through"	4, 7	–	25	–	28	–	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	–	25	–	28	–	30	ns
t_{MRIRH}[3]	Master Reset ↑ to Input Ready HIGH	8	–	25	–	28	–	30	ns
t_{MRIRL}[2]	Master Reset ↓ Input Ready LOW	8	–	25	–	28	–	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	–	20	–	25	–	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	–	25	–	28	–	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	–	25	–	28	–	40	ns
t_{IPH}[3]	Input Ready Pulse HIGH	4	5	–	5	–	5	–	ns
t_{OPH}[3]	Output Ready Pulse HIGH	7	5	–	5	–	5	–	ns
t_{ORD}[3]	Output Ready ↑ HIGH to Valid Data	5	–	5	–	5	–	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	–	28	–	28	–	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	–	28	–	28	–	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	–	28	–	28	–	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	–	28	–	28	–	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	–	28	–	28	–	40	ns
t_{HFL}	Shift Out ↑ to HF LOW	11	–	28	–	28	–	40	ns
t_{PHZ}[3]	Output Disable Delay	12	–	12	–	12	–	15	ns
t_{PLZ}[3]		12	–	12	–	12	–	15	ns
t_{PZL}[3]	Output Enable Delay	12	–	15	–	15	–	20	ns
t_{PZH}[3]		12	–	15	–	15	–	20	ns

NOTES:

1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. If the FIFO is not full, (IR = HIGH), $\overline{MR}\downarrow$ forces IR to go LOW, and $\overline{MR}\uparrow$ causes IR to go HIGH.
3. Guaranteed by design, but not currently tested.

AC TEST CONDITIONS

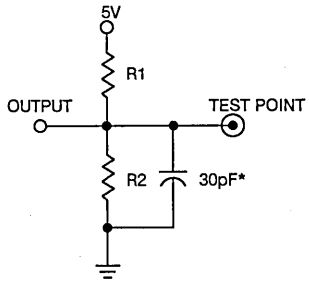
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

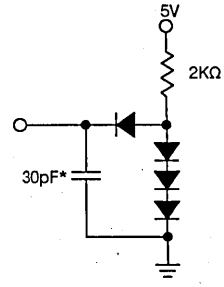
SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently tested.

STANDARD TEST LOAD



DESIGN TEST LOAD



*Includes jig and scope capacitances.

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

Figure 1. Output Load

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FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFO's output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D_{0-4} lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the output data from the FIFO.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable is used to enable the FIFO outputs onto a bus. Output Enable is active LOW.

ALMOST-FULL/EMPTY FLAG (AFE)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

TIMING DIAGRAMS

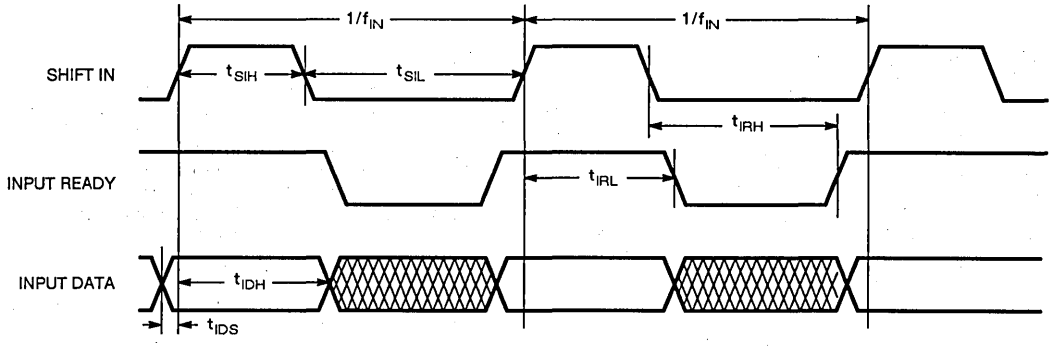
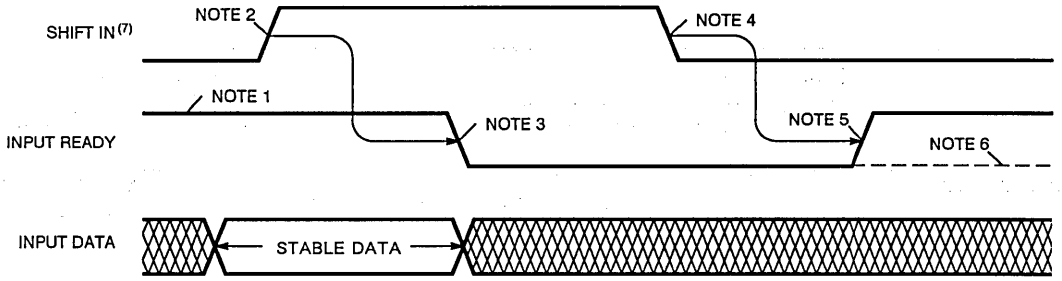


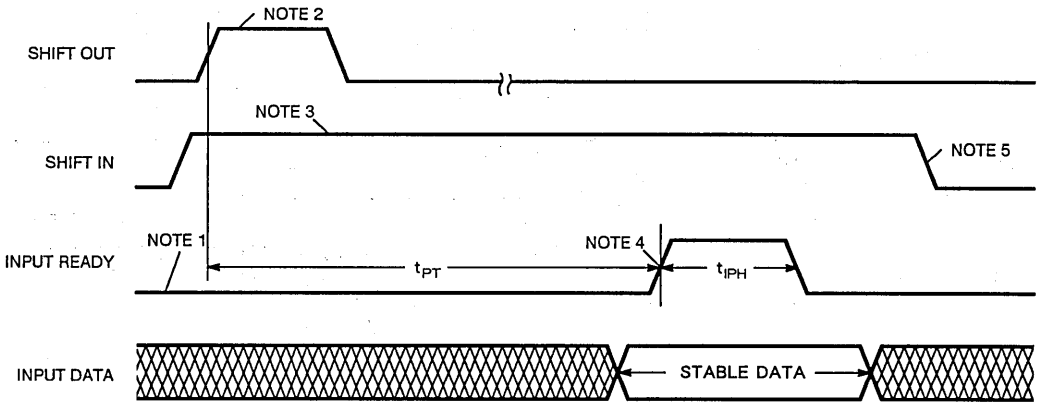
Figure 2. Input Timing

TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

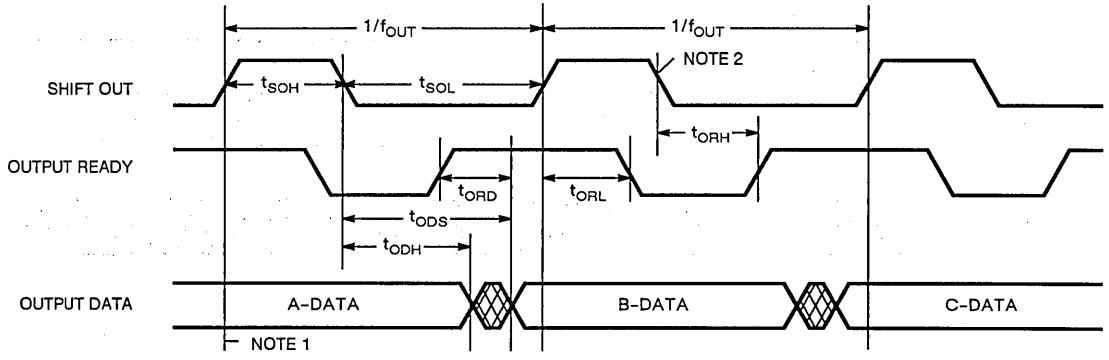
Figure 3. The Mechanism of Shifting Data Into the FIFO



NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

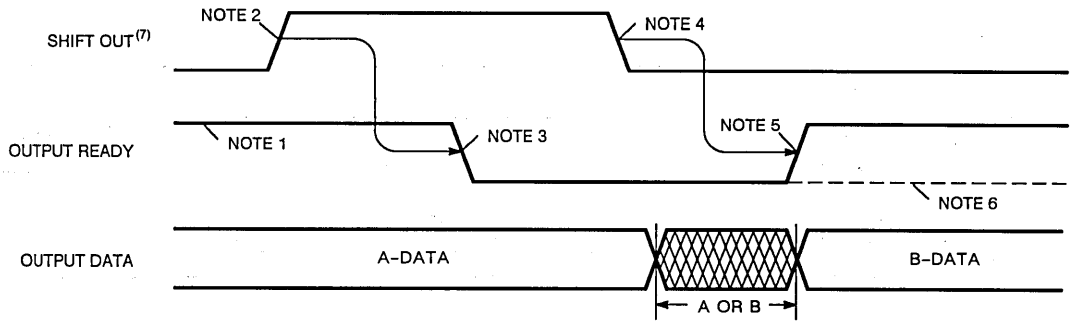
Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

TIMING DIAGRAMS (Continued)



NOTES:
1. This diagram is loaded consecutively, A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

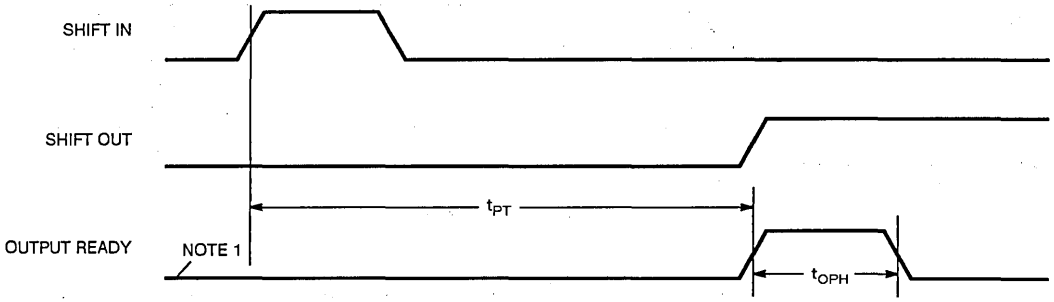
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after t_{ORD} ns.
6. If the FIFO has only one word loaded (A-DATA), Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

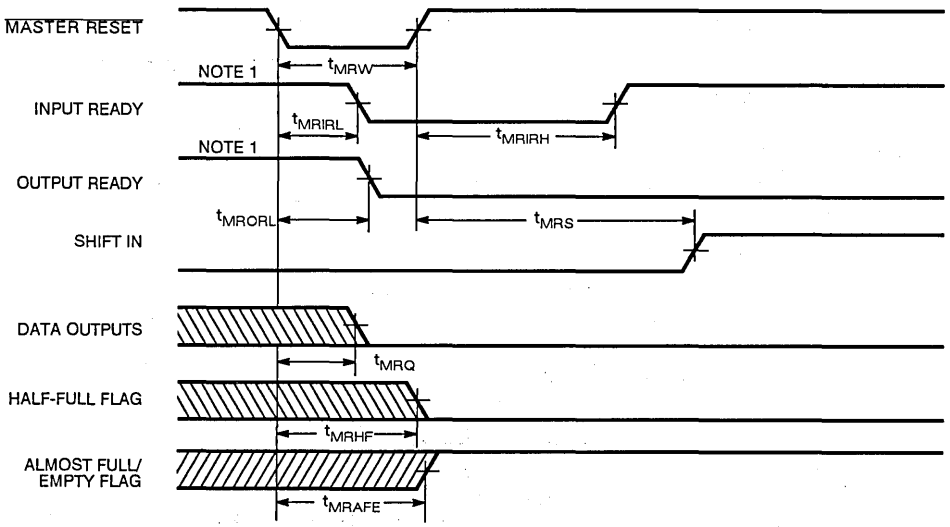
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO initially empty.

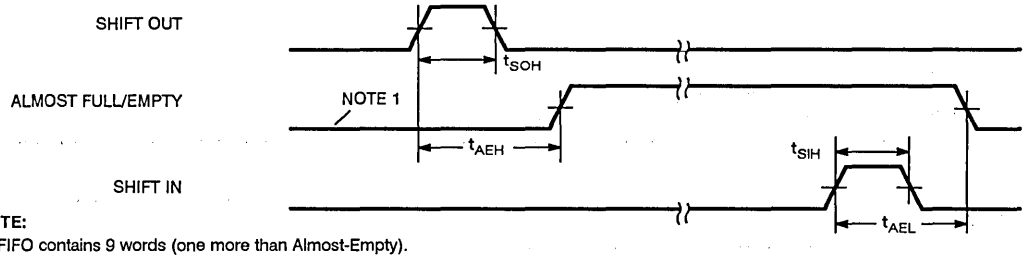
Figure 7. t_{PT} and t_{OPH} Specification



NOTE:
1. FIFO is partially full.

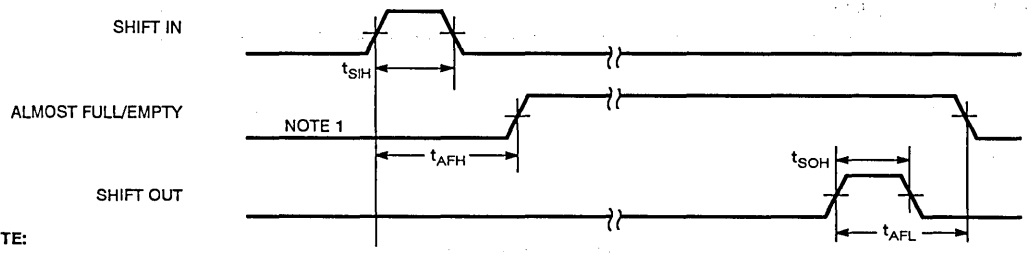
Figure 8. Master Reset Timing

TIMING DIAGRAMS (Continued)



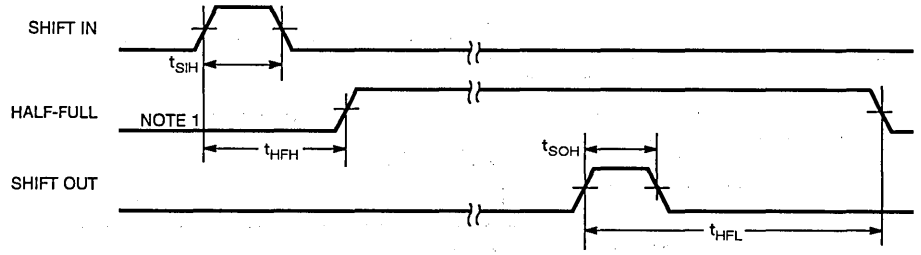
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. t_{AEH} and t_{AEL} Specifications



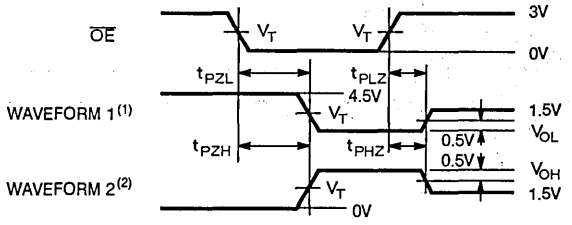
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. t_{AFH} and t_{AFL} Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

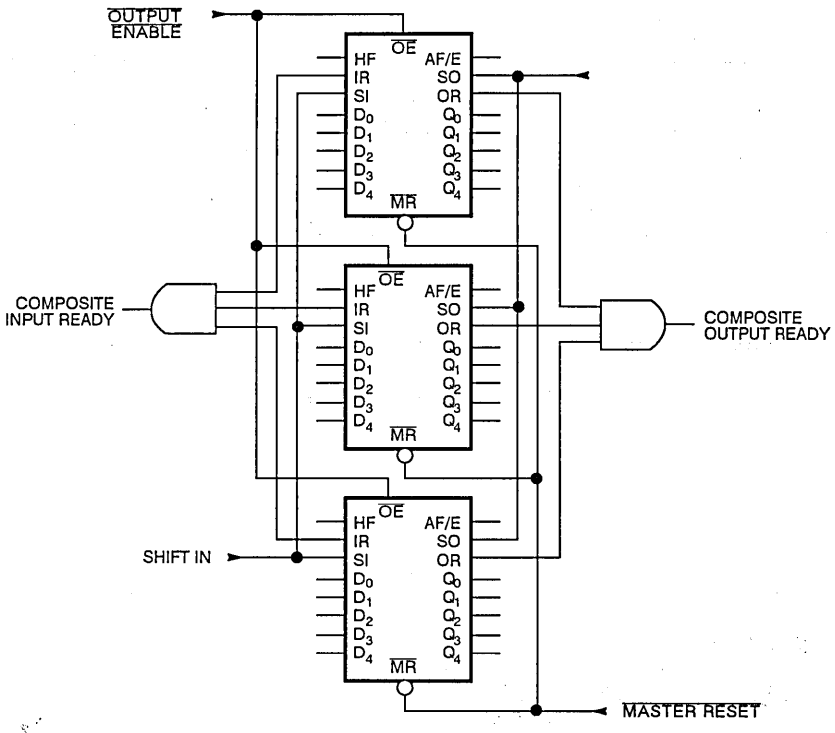
Figure 11. t_{HFL} and t_{HFH} Specifications



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 12. Enable and Disable

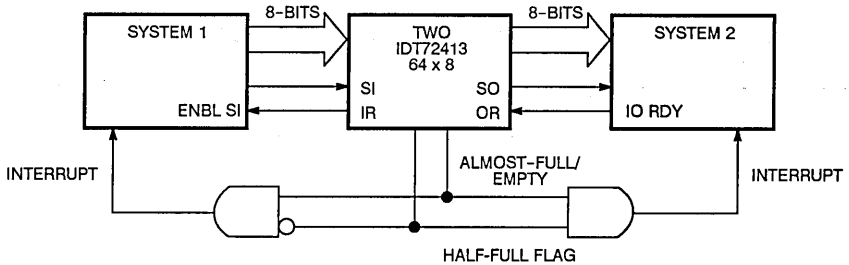
APPLICATIONS



NOTE:

1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

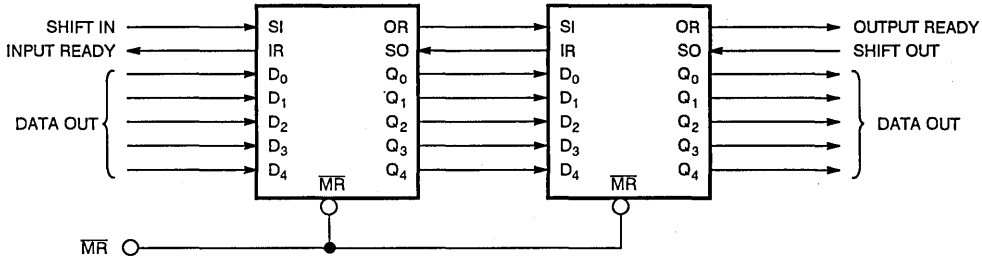
Figure 13. 64x15 FIFO with IDT72413



NOTE:

1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

Figure 14. Application for IDT72413 for Two Asynchronous Systems

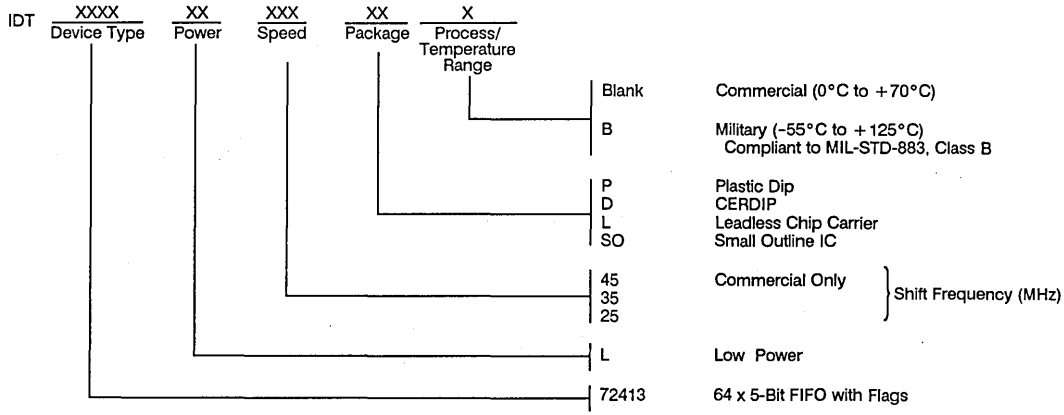


NOTE:

1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



Integrated Device Technology, Inc.

1K x 18-BIT – 2K x 9-BIT CMOS BiFIFO

PRELIMINARY
IDT 7252
IDT 72520

FEATURES:

- Bidirectional First-In/First-Out (FIFO) memory
- Side-by-side 1K x 18-bit and 2K x 9-bit FIFO organization
- 35ns access time
- Facilitates processor-to-peripheral and processor-to-processor communication
- Matches bus widths: 16-bit to 8-bit and 32-bit to 8-bit buses
- Asynchronous and simultaneous read and write operations
- Parity check and generate
- Width expandable to 36-bits
- Hardware Reread and Rewrite
- Hardware Load Reread and Load Rewrite for IDT72520
- Hardware Reset for IDT72520
- Build-in pass-through path
- On-chip DMA for easy peripheral interfacing
- Available in 48-pin DIP for IDT7252 and 52-pin LCC and PLCC for IDT72520
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7252 and IDT72520 BiFIFOs are compact, highly integrated solutions for simplifying data transfer between two processors or a processor and peripheral of different bus bandwidths. With access speed of 35ns, the BiFIFO can quadruple system performance of the peripheral interface by eliminating mismatched bus widths. The BiFIFO can handle data transfer between 16-bit to 8-bit, 32-bit to 8-bit buses and 32-bit to 16-bit buses.

Both ports can be operated concurrently, essentially operating as two FIFOs in one chip. Port A is organized in 1K x 18-bit and port B is organized is 2K x 9-bit, with the ninth bit of this FIFO used for parity check or generate. A unique data pass through mode allows for synchronous communication between two devices. To improve system performance when interfacing to peripherals which support DMA operations, a Request (REQ) and Acknowledge ($\overline{ACK}$) handshake is included.

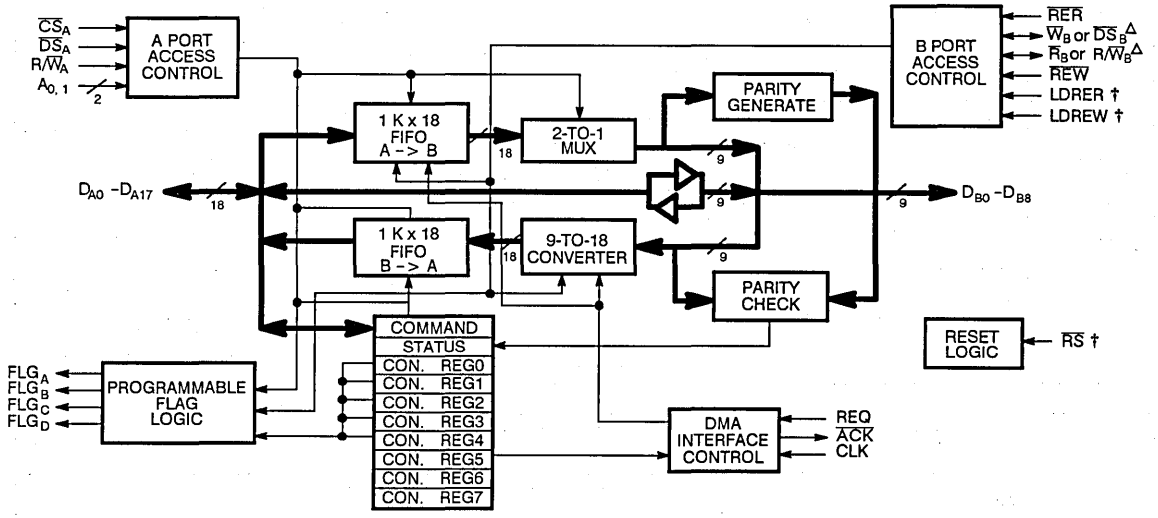
Four external flag pins can be used to configure and access any one of sixteen internal flags (Four in each FIFO for both positive and negative polarity). The four internal flags are Empty, Empty + Offset, Full and Full-Offset. The offset value and flag polarity can be determined by the users.

The BiFIFO incorporates a Reread ($\overline{RER}$) and Rewrite($\overline{REW}$). Upon signaling the $\overline{RER}$ input, the read pointer is reset with the value of $\overline{RER}$ pointer and data is read again. With signaling $\overline{REW}$, the write pointer is reset with value of $\overline{REW}$ pointer and data is written again. These internal read and write pointers can be set by the user through a control register. In addition, the IDT72520 has hardware Load Reread, Load Rewrite and Reset capabilities.

The BiFIFO is available in a 48-pin DIP for IDT7252, and 52-pin LCC and PLCC for IDT72520. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM



Δ Option as Motorola Interface Mode.
† Available In IDT72520

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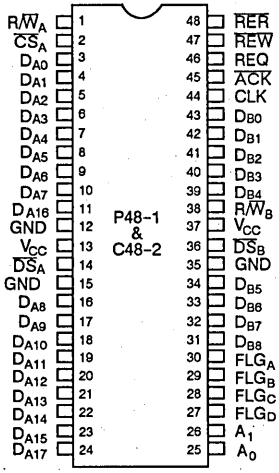
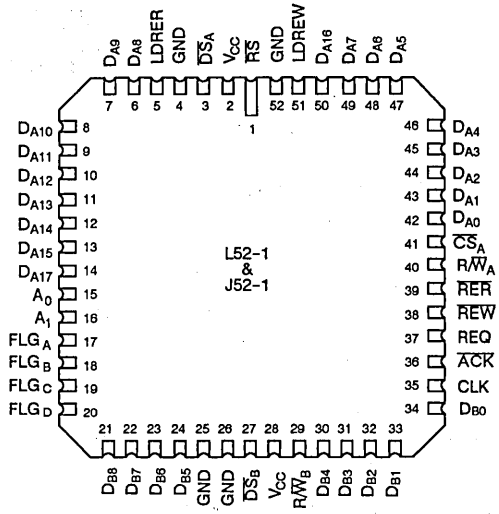
PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D_{A0} – D_{A15}	Data A	I/O	Data inputs & outputs for 16-bits of the 18-bit Port A.
D_{A16}– D_{A17}	Parity A	I/O	D_{A16} is parity bit for D_{A0} – D_{A7}. D_{A17} is the parity bit for D_{A8}– D_{A15}.
D_{B0} – D_{B7}	Data B	I/O	Data inputs & outputs for 8 bits of the 9-bit Port B.
D_{B8}	Parity B	I/O	D_{B8} is parity bit for D_{B0}– D_{B7}.
$\overline{CS}_A$	Chip Select	I	Port A is access when chip select is LOW.
$\overline{DS}_A$	Data Strobe	I	Port A is accessed when $\overline{DS}_A$ is LOW, thereby activating Read or Write based upon selection of $R/\overline{W}_A$.
$\overline{DS}_B$	Data Srobe	I/O	Port B is accessed when $\overline{DS}_B$ is LOW.
$R/\overline{W}_A$	Read/Write	I	Controls Read or Write operation of Port A when $\overline{DS}_A$ is LOW.
$R/\overline{W}_B$	Read/Write	I/O	Controls Read or Write operation of Port B when $\overline{DS}_B$ is LOW.
$\overline{RER}$	Reread	I	Loads Read pointer with value of $\overline{RER}$ pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads Write pointer with value of $\overline{REW}$ pointer when LOW.
LDRER	Load Reread	I	Saves the Read pointer value in the Reread pointer. Active HIGH input pin for IDT72520. IDT7252 access through internal register only.
LDREW	Load Rewrite	I	Saves the Write pointer value in the Rewrite Pointer. Active HIGH input pin for IDT72520. IDT7252 access through internal register only.
$\overline{RS}$	Reset	I	IDT72520 is reset through hardware pin, power up or through bit on register. Reset for IDT7252 is performed on power up or through software command. During reset, both internal Read and Write pointers are set to the first location.
REQ	Request	I	Port B input signal requesting a data transfer between B port and Peripheral through DMA handshake.
$\overline{ACK}$	Acknowledge	O	DMA handshake response to the active signal from REQ input.
CLK	Clock	I	Input clock pin (70% duty cycle max.).
A_0 , A_1	Address	I	With $\overline{CS}_A$ LOW, address lines and R/W_A select one of the 6 modes, FIFO A->B, FIFO B->A, Direct pass-through path, configuration registers, status register, and command register.
FLG_A - FLG_D	Flags	O	These four pins output four of sixteen flags (Empty, Empty+Offset, Full, Full-Offset) for A->B, and for B->A in two polarities. Flags are programmed via the configuration registers.
V_{CC}	Power Supply		Two power supply pins, 5V.
GND	Ground		Three GND pins at 0V for IDT7252. Four GND pins at 0V for IDT72520.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL}[1]	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7252L IDT72520L COMMERCIAL T_A = 35, 50, 80ns			IDT7252L IDT72520L MILITARY T_A = 40, 50, 80ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL}[1]	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL}[2]	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	–	–	0.4	–	–	0.4	V
I_{CC1}[3]	Average V_{CC} Power Supply Current	–	90	160	–	120	170	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L)[3]	Power Down Current (All Input = V_{CC} = -0.2V)	–	–	2	–	–	4	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $R \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

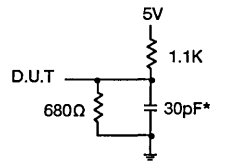


Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}[3]	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}[2, 3]	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES:

1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		MILITARY AND COMMERCIAL				UNIT	FIGURE
		7252x35 72520x35		7252x40 72520x40		7252x50 72520x50		7252x80 72520x80			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
TIMINGS (A-Side 18-Bit)											
ta_A	Access Time	35	–	40	–	50	–	80	–	ns	1
ta_{RLZ}	Read Pulse Low to Data Bus at Low Z	5	–	5	–	5	–	10	–	ns	1, 6
ta_{RHZ}	Read Pulse High to Data Bus at High Z	–	20	–	25	–	30	–	30	ns	1, 6
ta_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	ns	1, 6
ta_{RC}	Read Cycle Time	45	–	50	–	65	–	100	–	ns	1
ta_{RPW}	Read Pulse Width	35	–	40	–	50	–	80	–	ns	1
ta_{RR}	Read Recovery Time	10	–	10	–	15	–	20	–	ns	1
ta_{S1}	$\overline{CS}$, A , A , R/$\overline{W}$ Set-Up Time	5	–	5	–	5	–	10	–	ns	1
ta_{H1}	$\overline{CS}$, A , A , R/$\overline{W}$ Hold Time	5	–	5	–	5	–	10	–	ns	1
ta_{DS}	Data Set-Up Time	18	–	20	–	30	–	40	–	ns	1, 2
ta_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	ns	1, 2
ta_{WC}	Write Cycle Time	45	–	50	–	65	–	100	–	ns	1
ta_{WPW}	Write Pulse Width	35	–	40	–	50	–	80	–	ns	1, 2
ta_{WR}	Write Recovery Time	10	–	10	–	15	–	20	–	ns	1
ta_{WRCOM}	Write Recovery Time after Command	35	–	40	–	50	–	80	–	ns	2

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC}= 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		MILITARY AND COMMERCIAL				UNIT	FIGURE
		7252x35 72520x35		7252x40 72520x40		7252x50 72520x50		7252x80 72520x80			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
TIMINGS (B-Side 9-Bit)											
tb_{A1}	Access Time With No Parity	35	–	40	–	50	–	80	–	ns	3
tb_{A2}	Access Time With Parity	42	–	48	–	60	–	90	–	ns	3
tb_{RLZ}	Read Pulse Low to Data Bus at Low Z	5	–	5	–	5	–	10	–	ns	3, 6
tb_{RHZ}	Read Pulse High to Data Bus at High Z	–	20	–	25	–	30	–	30	ns	3, 6
tb_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	10	–	ns	3, 6
tb_{RC}	Read Cycle Time	45	–	50	–	65	–	100	–	ns	3
tb_{RPW}	Read Pulse Width	35	–	40	–	50	–	80	–	ns	3
tb_{RR}	Read Recovery Time	10	–	10	–	15	–	20	–	ns	3
tb_{S1}	R/$\overline{W}$ Set-Up Time	5	–	5	–	5	–	10	–	ns	3
tb_{H1}	R/$\overline{W}$ Hold Time	5	–	5	–	5	–	10	–	ns	3
tb_{DS1}	Data Set-Up Time With No Parity	18	–	20	–	30	–	40	–	ns	3
tb_{DH1}	Data Hold Time With No Parity	0	–	0	–	5	–	10	–	ns	3
tb_{DS2}	Data Set-Up Time With Parity	22	–	25	–	35	–	45	–	ns	3
tb_{DH2}	Data Hold Time With Parity	0	–	0	–	5	–	10	–	ns	3
tb_{WC}	Write Cycle Time	45	–	50	–	65	–	100	–	ns	3
tb_{WPW}	Write Pulse Width	35	–	40	–	50	–	80	–	ns	3
tb_{WR}	Write Recovery Time	10	–	10	–	15	–	20	–	ns	3
tb_{DSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW Set-Up and Recovery Time	10	–	10	–	15	–	15	–	ns	4
tb_{PER}	Parity Error	25	–	25	–	30	–	30	–	ns	8
REQ-ACK (B-Side 9-Bit)											
tb_{CKC}	Clock Cycle Time	17.5	–	20	–	25	–	40	–	ns	5
tb_{CKH}	Clock Pulse HIGH	6	–	8	–	10	–	16	–	ns	5
tb_{CKL}	Clock Pulse LOW	6	–	8	–	10	–	16	–	ns	5
tb_{REQS}	Request Set-Up Time	5	–	5	–	10	–	10	–	ns	5
tb_{REQH}	Request Hold Time	5	–	5	–	5	–	5	–	ns	5
tb_{ACKL}	Delay From Rising Clock Edge to ACK Switching	18	–	20	–	25	–	35	–	ns	5

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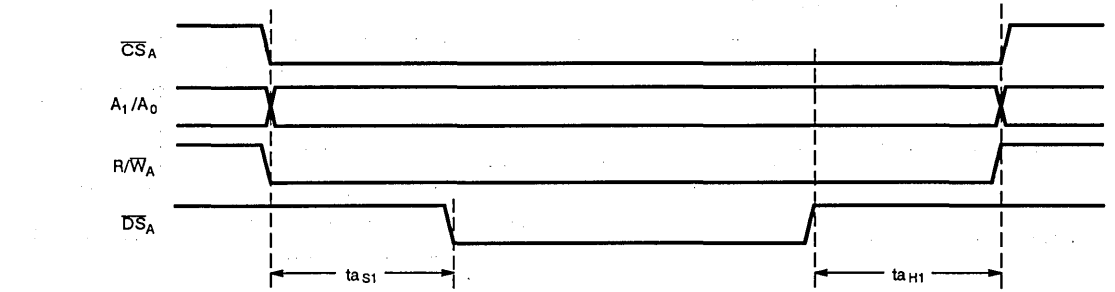
AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

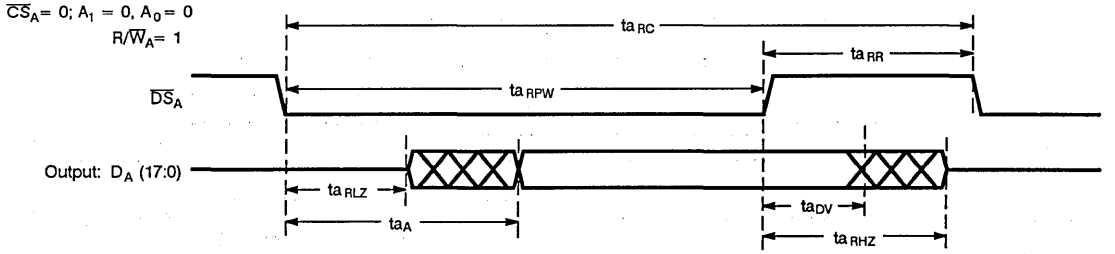
SYMBOL	PARAMETER	COM'L.		MIL.		MILITARY AND COMMERCIAL				UNIT	FIGURE
		7252x35 72520x35		7252x40 72520x40		7252x50 72520x50		7252x80 72520x80			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
BYPASS MODE											
tb_{BYA}	B->A Bypass Access	20		25		30		40		ns	6
tb_{BYD}	B->A Bypass Delay	15		17		20		30		ns	6
tb_{BYH}	B->A Data Hold	5		5		5		10		ns	6
tb_{BYA}	A->B Bypass Access	20		25		30		40		ns	6
tb_{BYD}	A->B Bypass Delay	15		17		20		30		ns	6
tb_{BYH}	A->B Data Hold	5		5		5		10		ns	6
FLAGS TIMINGS											
tb_{REF}	$\overline{R}$ LOW to $\overline{EF}$ LOW		35		35		45		60	ns	7
tb_{WEF}	$\overline{W}$ HIGH to $\overline{EF}$ HIGH		35		35		45		60	ns	7
tb_{RFF}	$\overline{R}$ HIGH to $\overline{FF}$ HIGH		35		35		45		60	ns	7
tb_{WFF}	$\overline{W}$ LOW to $\overline{FF}$ LOW		35		35		45		60	ns	7
tb_{RAEF}	$\overline{R}$ Low to Almost $\overline{EF}$ LOW		50		50		60		75	ns	7
tb_{WAEF}	$\overline{W}$ High to Almost $\overline{EF}$ High		50		50		60		75	ns	7
tb_{RAFF}	$\overline{R}$ High to Almost $\overline{FF}$ High		50		50		60		75	ns	7
tb_{WAFF}	$\overline{W}$ Low to Almost $\overline{FF}$ Low		50		50		60		75	ns	7

NOTE: $\overline{R}$ or $\overline{W}$ is internal signal derived from $\overline{DS}_A$ & $R/\overline{W}_A$ or $\overline{DS}_B$ & $R/\overline{W}_B$.



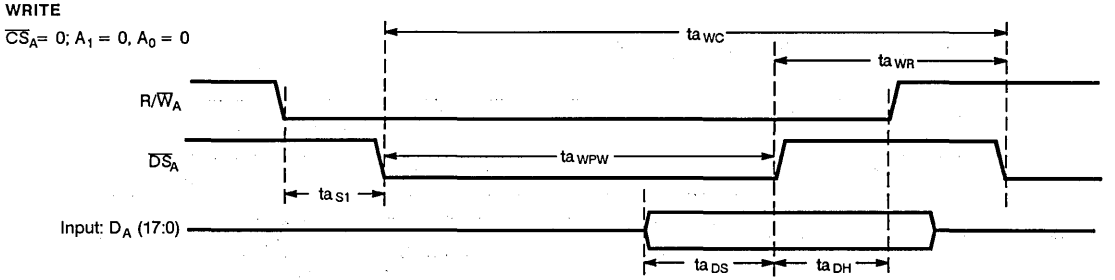
READ

$\overline{CS}_A$= 0; A_1 = 0, A_0= 0
$R/\overline{W}_A$= 1



WRITE

$\overline{CS}_A$= 0; A_1 = 0, A_0 = 0



Note: Refer to Address Control (Table 1) for other selection

Figure 1. Read and Write Timings (A-Side)

A_1 = 1, A_0 = 1

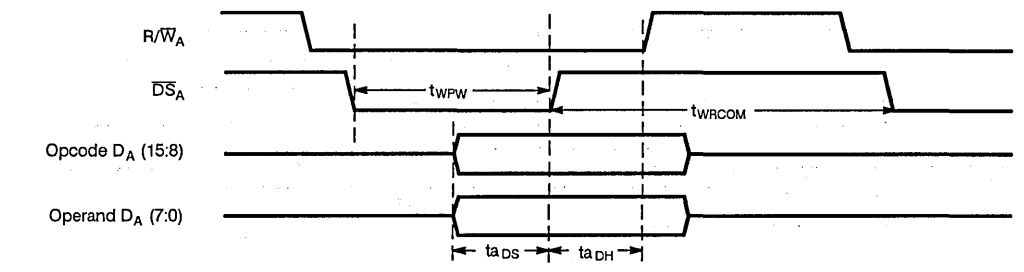
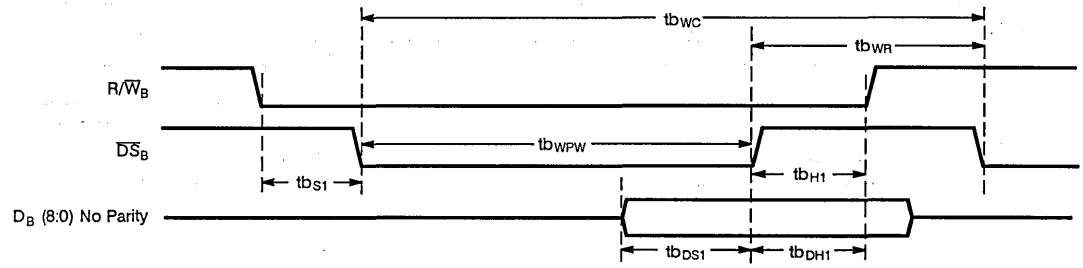


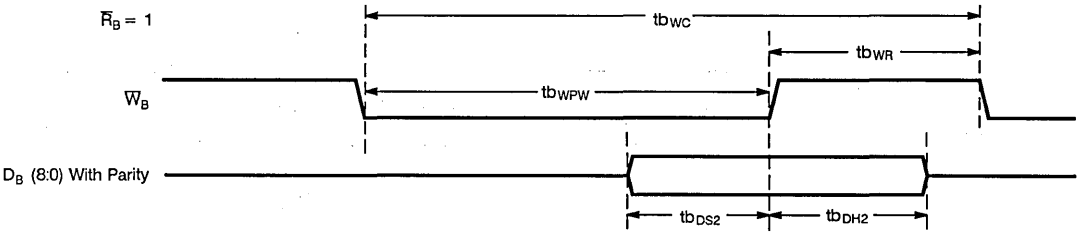
Figure 2. Carry Out Command Timing (A-Side Only)

WRITE

Case 1: When access controls are $R/\overline{W}_B$ and $\overline{DS}_B$

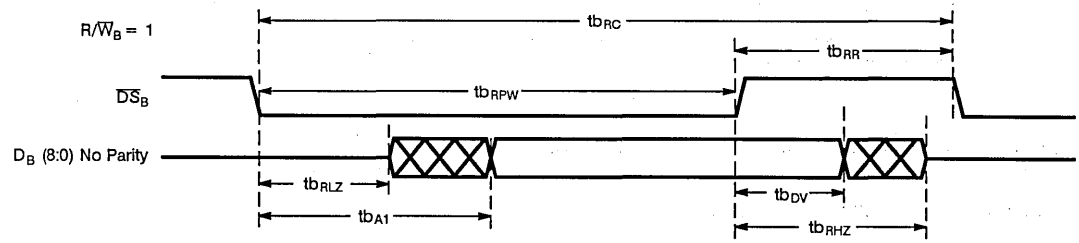


Case 2: When access controls $R/\overline{W}_B$ and $\overline{DS}_B$ are programmed as $\overline{R}_B$ and $\overline{W}_B$



READ

Case 1: When access controls are $R/\overline{W}_B$ and $\overline{DS}_B$



Case 2: When access controls $R/\overline{W}_B$ and $\overline{DS}_B$ are programmed as $\overline{R}_B$ and $\overline{W}_B$

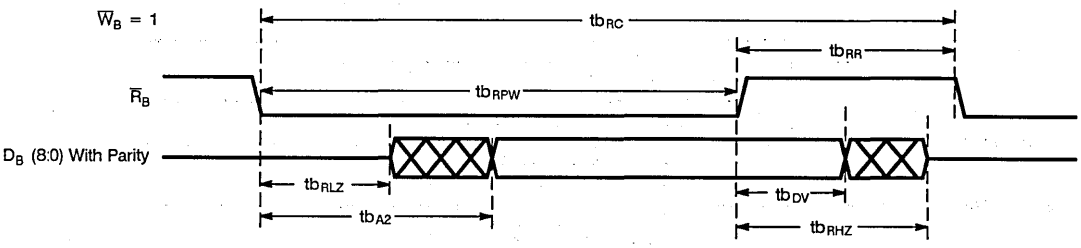
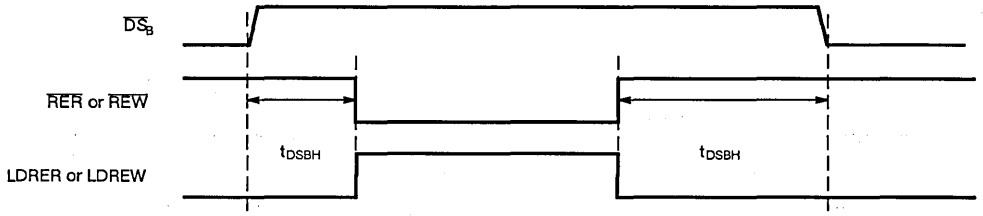


Figure 3. Read and Write Timings (B-Side)

Case 1: Access controls are $R/\overline{W}_B$ and $\overline{DS}_B$



Case 2: Access controls $R/\overline{W}_B$ and $\overline{DS}_B$ pins are programmed as $\overline{R}_B$ and $\overline{W}_B$

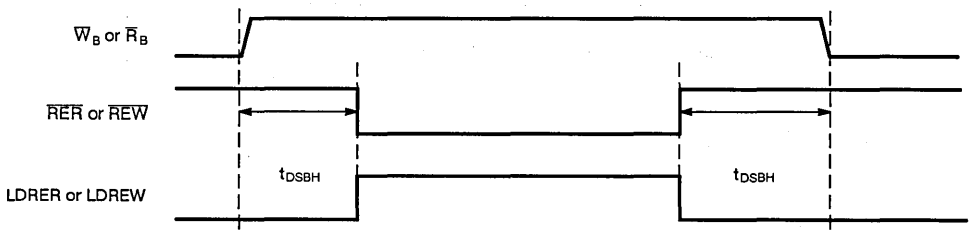
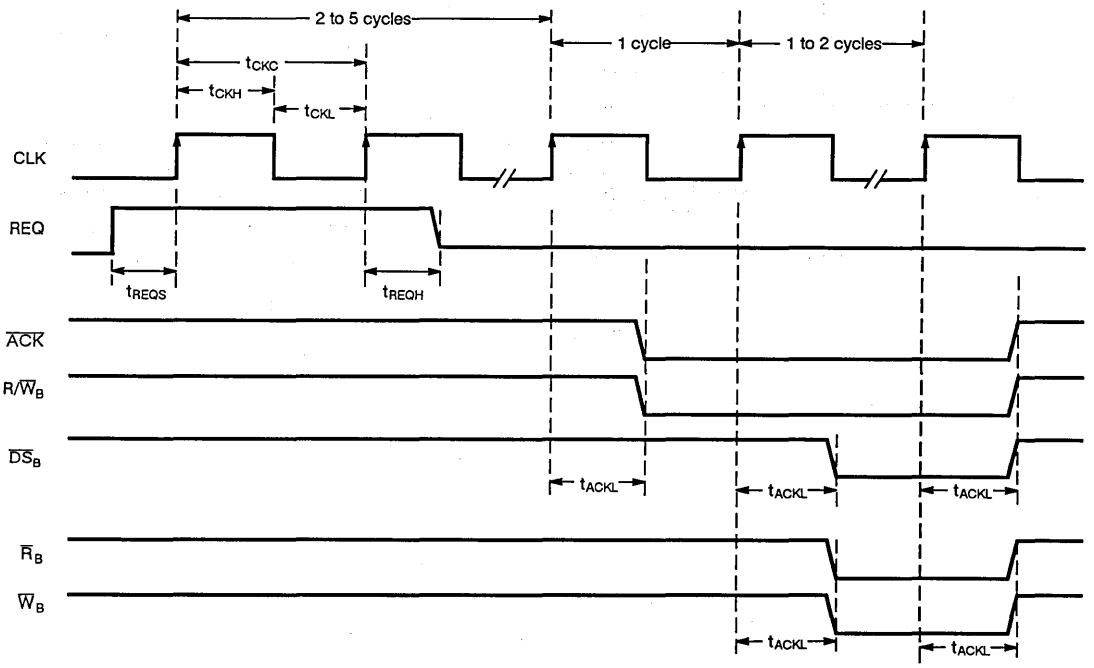


Figure 4. Reread, Rewrite, Load Reread, Load Rewrite Timings (B-Side)



Note: Depends on the Intel or Motorola mode bit, BiFIFO either generates $\overline{DS}_B$ and $R/\overline{W}_B$ or $\overline{R}_B$ and $\overline{W}_B$

Figure 5. Request and Acknowledge Timings (B-Side Only)

BYPASS

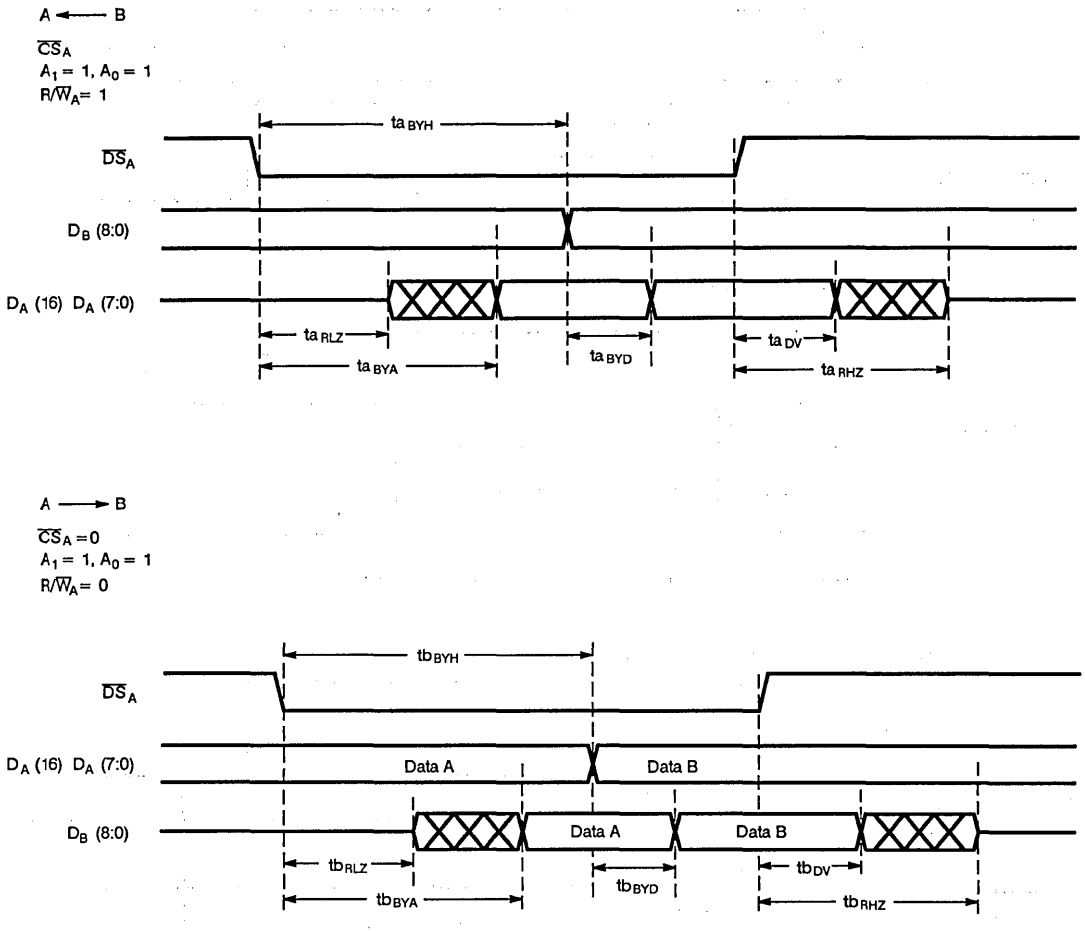
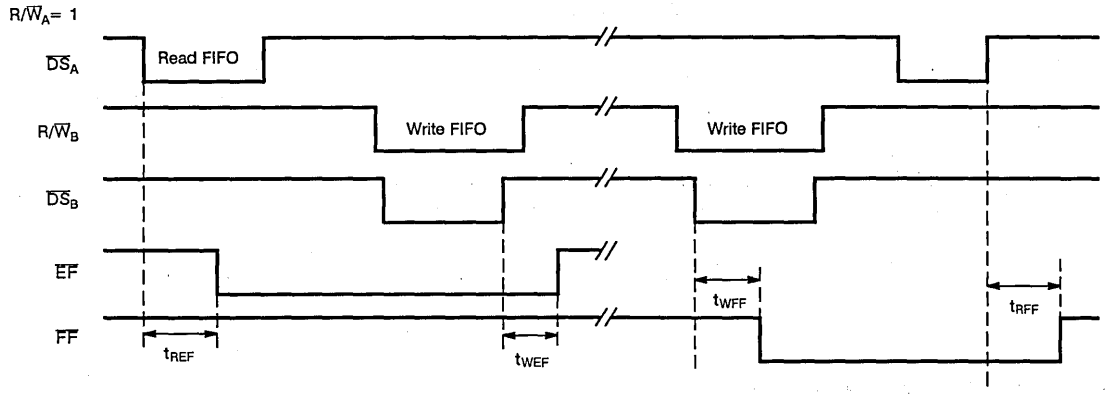


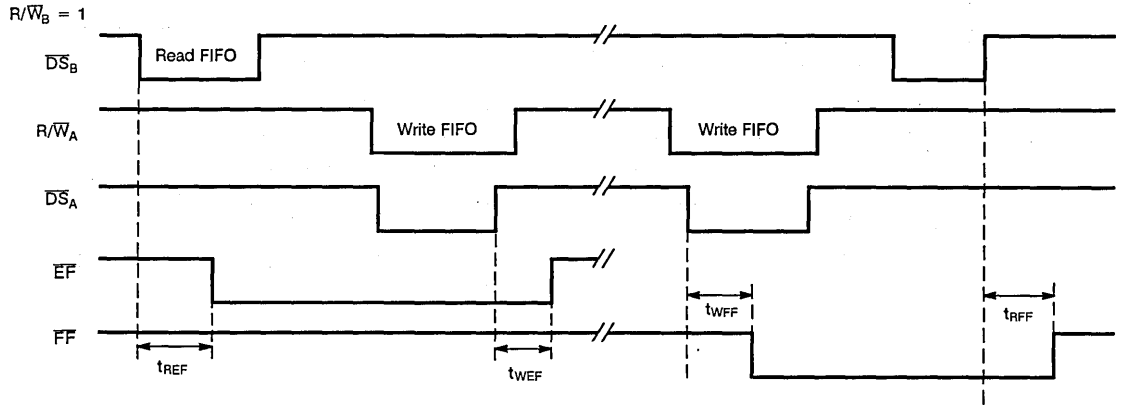
Figure 6. Bypass Timings

FIFO B ⟶ A: Empty and Full Flags



Note: t_{RAEF}, t_{WAEF}, t_{RAFF}, t_{WAFF} are the same to the above timings.

FIFO B ⟵ A: Empty and Full Flags

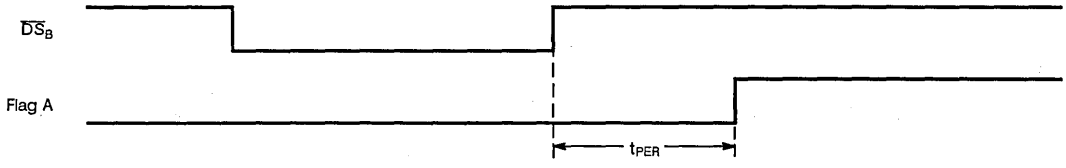


Note: t_{RAEF}, t_{WAEF}, t_{RAFF}, t_{WAFF} are the same to the above timings.

Figure 7. Flag Timings

PARITY ERROR

Set Parity Error: Flag A is programmed to output read or write parity error on B side



Clear Parity Error: By issuing a command on A side

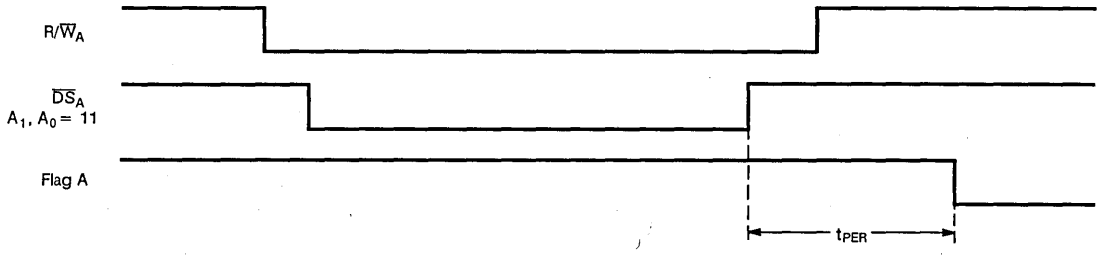
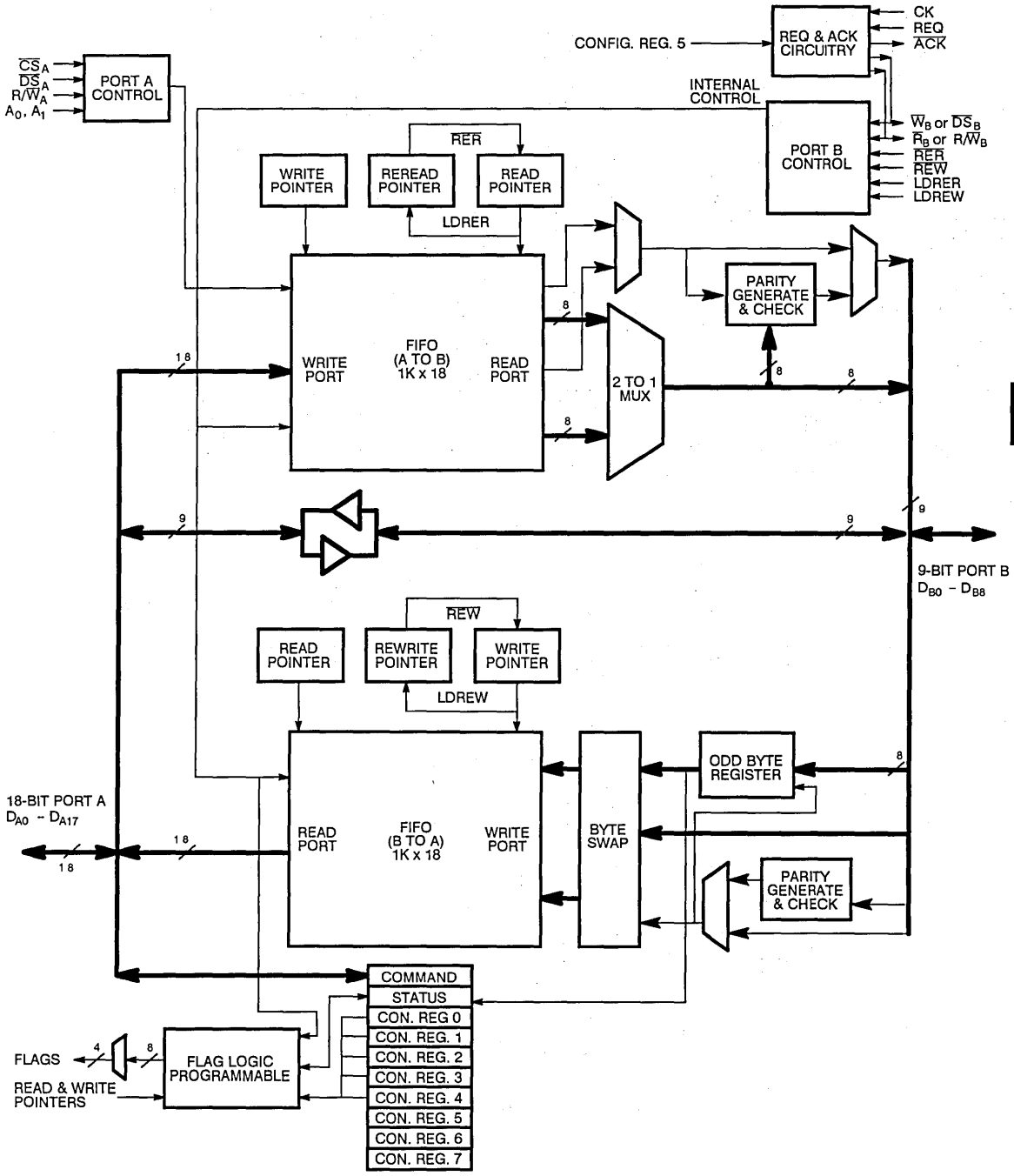


Figure 8. Parity Timings (B-Side Only)

DETAILED BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

FIFOs are used to link processors and peripherals together asynchronously to transfer data. Often the data on each side must be passed in both directions and requires two FIFOs arranged side-by-side. Furthermore, CPUs are usually 16 or 32 bits wide while peripherals' width is typically 8-bit, causing a mismatch in bus bandwidths. The BiFIFO is an integrated solution to this class of applications: offering both asynchronous bidirectional data buffering and bus matching capabilities.

The BiFIFO contains two 1K by 18 FIFOs connected side by side to two data ports: A and B. Port A is 18-bit wide while port B, with a 2-to-1 multiplexer, is 9-bit wide. A word (2 bytes) written into port A requires two reads from port B to retrieve both bytes. Similarly, a word is sent into port B one byte at a time and read as a whole word form A side.

The BiFIFO also contains several innovative, programmable features:

- Width Expansion: Width expandable to match 32-bit to 8-bit buses configuration by using two BiFIFOs, programmed as "Master" and "Slave" devices; or match 32-bit to 16-bit buses configuration by using 2 BiFIFOs.
- DMA Style Handshake: Option available on port B side to control read and write activities when connected to peripherals with REQUEST and ACKNOWLEDGE kind of handshake.
- Block Transmit: Capability to Reread and Rewrite from port B.
- Flags: Four empty, full and programmable flags (empty + offset, full-offset) per FIFO, can be multiplexed into four flag pins.
- Parity: Parity generate or check on port B.
- Pass-Through: On-chip transceiver to pass through the FIFOs for direct and synchronous communication between two data ports.
- Odd Byte: 8 bits can be read into port B without using FIFO. An odd byte written into B port can be accessed by reading STATUS register.

These features can be selected by programming a set of six internal Configuration Registers or by "executing a command" from port A. There are six possible modes of operation from port A, depending on $\overline{CS}_A$, and A_1 and A_0 pins:

1. Port A disabled ($\overline{CS}_A = 0$).
2. FIFO access.
3. Direct access to port B, pass through FIFOs.
4. Program Configuration Registers.
5. Read Status Registers.
6. Carry out a command.

Reset

IDT72520 can be reset through hardware pin, power up or through bit on register. Reset for IDT7252 is performed on power up or through software command, no hardware pin is available. During reset, both internal Read and Write pointers are set to the first location.

Width Expansion

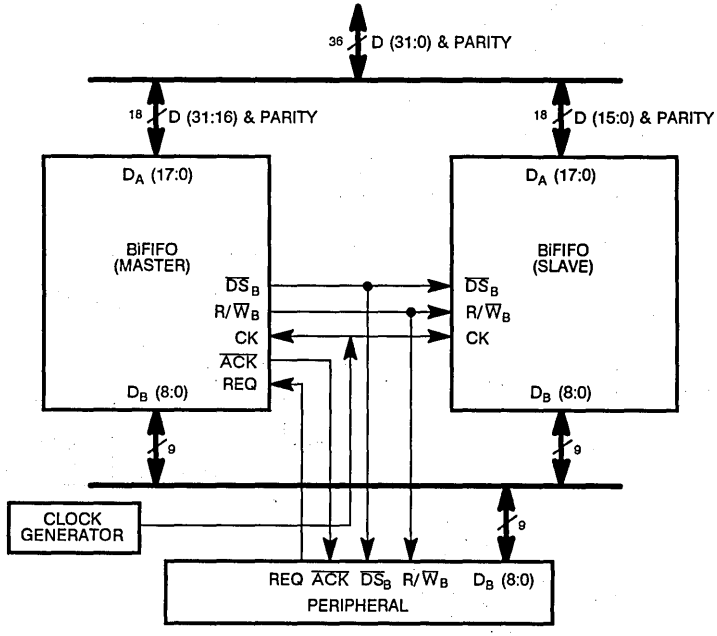


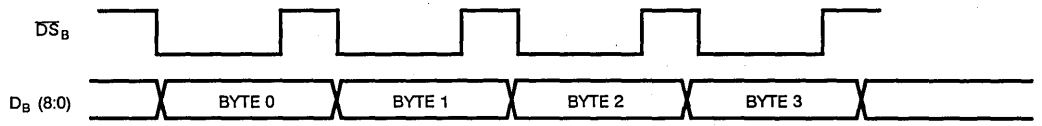
Figure 9. 32-Bit to 8-Bit BIFIFO EXPANSION (peripheral mode)

In the 32-8 expansion configuration (for both CPU and peripheral modes) the byte arrangement on the A side and data access on the B side is as follows:

A Side: The byte arrangement: (BYTE-ORDER bit in CONFIG. register is programmed as 0)

D (31:24) BYTE 3	D (23:16) BYTE 2	D (15:8) BYTE 1	D (7:0) BYTE 0
MASTER BiFIFO		SLAVE BiFIFO	

B Side: The order of data being accessed: (SLAVE BiFIFO is always read or written first)



DMA Style Handshake Mechanism

There are two operational modes for the 8-bit (port B) interface. The modes are tailored to facilitate connection with intelligent devices such as CPUs which can generate read and write strobes, or less intelligent devices such as peripherals which require that read and write strobes be generated for them (see Figure 10).

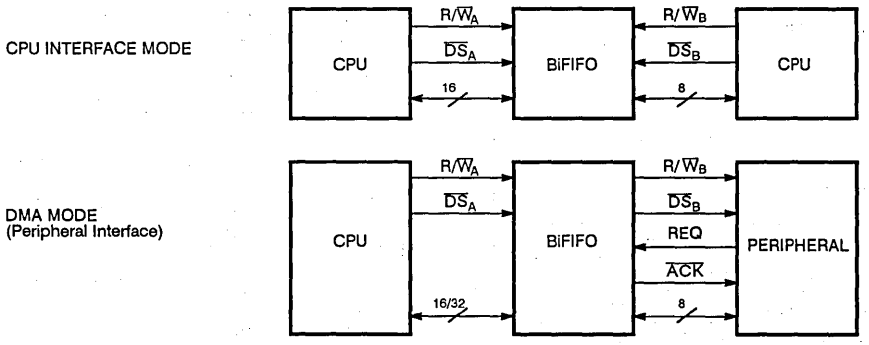


Figure 10. Interface Modes

The BiFIFO responds to an active signal on the REQ input by strobing the $\overline{ACK}$ and $\overline{DS}_B$ lines and asserting the R/$\overline{W}_B$ output. All timing is relative to a shift register clock generated by CLK or CLK divided by two. When in the DMA (peripheral) mode and the pass-through buffers are used for a synchronous transfer, the read/write strobe from the A port are passed through to the B port.

Parity

The BiFIFO supports parity in two fashions: Check or Generate

In the parity check mode, the parity check circuitry monitors data passed through the Data B bus and sets the parity error flag. While transferring data from the Data B bus into the B- > A FIFO, an error sets the Write Parity error flag. Transferring the data from the A- > B FIFO through the Data B bus, an error sets the Read Parity error flag. The OR of these two flags is available as an option for output on the flag A pin.

In the Generate mode, the ninth bit of data on the B side of the A- > B FIFO is ignored and the Parity Check is disabled. The parity generate circuit output is placed on the ninth bit of the Data B bus output during a data transfer from the A- > B FIFO On writing into the B- > A FIFO from the Data B bus the parity is generated and stored.

The pass-through bus is treated in the same way that the FIFO data is treated.

Pass-Through (Synchronous Access)

The BiFIFO includes a unique data path that bypasses the FIFOs such that a processor can talk synchronously with the peripheral to initialize it and then communicate asynchronously via the FIFOs. The parity generate and check circuitry (if selected) also comes into play during the synchronous transfer of data via the pass-through buffers. When in the peripheral (DMA) pass-through

mode, the DS_B and $R/\overline{W}_B$ pins are outputs and reflect the action of the $\overline{DS}_A$ and $R/\overline{W}_A$ inputs. Only lower byte D_A (16) and D_A (7:0) are passed-through to D_B (8:0). In the 32-8 expansion configuration, when using the bypass mode, the Master device should be in DMA mode while the Slave should be in CPU mode, so that only the Master's transceiver is activated. During regular FIFO read and write modes, both master and slave should be in DMA mode. REQ should be low during initialization of BiFIFO and peripheral.

REGISTER DESCRIPTION

Address Control

The address lines indicate the resource to be accessed. There are six items that can be accessed: the FIFO B->A, FIFO A->B, 8-bit data bus, the flag configuration registers, status and command (see Table 1).

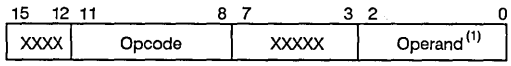
$\overline{CS}_A$	A_1	A_0	READ	WRITE
0	0	0	FIFO B->A	FIFO A->B
0	0	1	8-bit bus direct	8-bit bus direct
0	1	0	Configuration Register	Configuration Register
0	1	1	Status	Command
1	X	X	X	X

Note: Port B use $\overline{DS}_B$ and $R/\overline{W}_B$ in the same way that Port A generates internal strobes.

Table 1. Address Control for Port A.

Command Register

The command feature allows the user to direct the BiFIFO to do something in real-time rather than setting up configuration registers in an idle condition. The command port format and a list of commands is shown in Table 2. The commands are accessed through the command port (A_1, A_0 = 11).



Opcode	Function
0	Reset BiFIFO functions (see operands)
1	Select Configuration Register (see Table 3)
2	Load Read point with Reread pointer value
3	Load Write pointer with Rewrite pointer value
4	Load Reread pointer with Read pointer value
5	Load Rewrite pointer with Write pointer value
6	Set DMA transfer direction (see operand)
7	Select Status register format (operand)
8	Increment read pointer on B side
9	Increment write pointer on B side
A	Clear write parity Error flag
B	Clear read parity Error flag

Operands (1)	Function
000	No operation
001	Reset FIFO B->A (Read, Write, and Rewrite pointers)
010	Reset FIFO A->B (Read, Write, and Reread pointers)
011	Reset B->A and A->B
100	Reset REQ circuitry
101	No operation
110	No operation
111	Reset all (2)

XX0 Write FIFO B->A
XX1 Read FIFO A->B
XX0 Status format 0 (see Table 7)
XX1 Status format 1 (see Table 7)

NOTES:

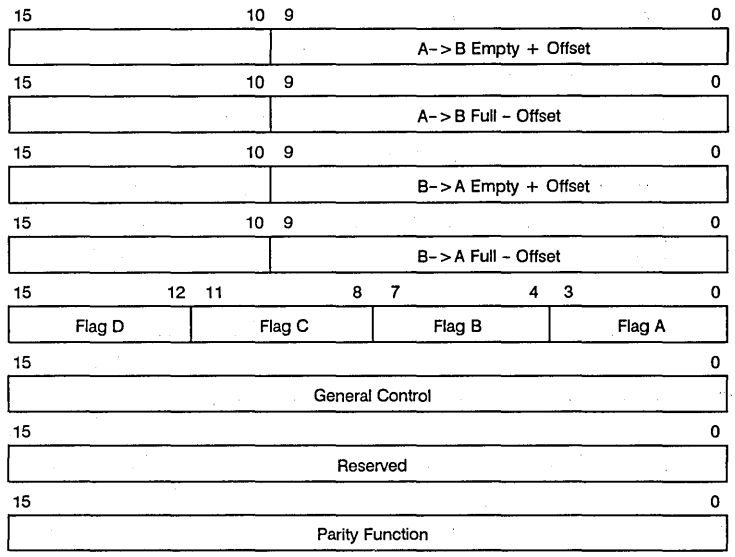
1. If operands are not shown for opcode, then they are in don't care condition.
2. Reset both FIFOs, REQ, Configuration Registers 0,1,2,3,5,7. Reset Configuration Register 4 to default. DMA direction B→A. Clear parity error flags. Select Status Format 0.

Table 2. Command Function and Operand

Configuration Registers

Several configuration registers control the BiFIFO operation (Table 3). The configuration registers are accessed by executing a command to point to a particular location, then reading or writing the content via address 2 (A_1, A_0 = 10). On reset, all registers, except Register 4 (Table 3, 4), default to Zero.

Operands	Selection	
000	Reg 0:	A->B Empty + Offset
001	Reg 1:	A->B Full - Offset
010	Reg 2:	B->A Empty + Offset
011	Reg 3:	B->A Full - Offset
100	Reg 4:	Flag D, Flag C, Flag B, Flag A
101	Reg 5:	General Control
110	Reg 6:	Reserved
111	Reg 7:	Parity Function



Note: 0110 0100 0010 0000 is default for Register 4. All others default to 0.

Table 3. Configuration Registers

Configuration Registers 0 through 3: These program the offset for the almost empty and almost full flags. The values in these registers are unsigned positive numbers.

Configuration Register 4: This is used to select internal flags for the external flag pins A through D. The register is divided into four fields of four bits each. The four bit fields not only select which flag to output but also the polarity at the output. This creates an easier interface to processors and peripherals (see Table 4).

SEL	SELECTED FLAG
0000	$\overline{\text{Empty A->B}}$
0001	$\overline{\text{Empty + Offset A->B}}$
0010	$\overline{\text{Full A->B}}$
0011	$\overline{\text{Full - Offset A->B}}$
0100	$\overline{\text{Empty B->A}}$
0101	$\overline{\text{Empty + Offset B->A}}$
0110	$\overline{\text{Full B->A}}$
0111	$\overline{\text{Full-Offset B->A}}$

SEL	SELECTED FLAG
1000	Empty A->B
1001	Empty + Offset A->B
1010	Full A->B
1011	Full - Offset A->B
1100	Empty B->A
1101	Empty + Offset B->A
1110	Full B->A
1111	Full-Offset B->A

Table 4. Flag Polarity and Selection Codes

Configuration Register 5: This contains fields to control various functions (see Table 5).

BIT	FUNCTION		
0	Select: DS_B & R/W_B or R_B & W_B	0	Provides the strobes as R_B & W_B (Intel Mode)
		1	DS_B & R/W_B (Motorola Mode)
1	Byte order of 16-bit word	0	Lower byte D_A (7:0) of a word is read or written first on Port B
		1	Higher byte D_A (15:8)
2	Enable Reread	0	Disable Reread
		1	Enable Reread
3	Enable Rewrite	0	Disable Rewrite
		1	Enable Rewrite
4	REQ polarity	0	REQ active HIGH
		1	REQ active LOW
5	ACK polarity	0	ACK active LOW
		1	ACK active HIGH
6-7	REQ/ACK Timing	00	2 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		01	3 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		10	4 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		11	5 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
8	Read & Write Strobe	0	Read and write strobe: 1 cycle LOW
		1	Read and write strobe: 2 cycle LOW
9	Clock Frequency (Internal)	0	CLK signal generates the REQ/ACK sequence
		1	CLK signal divided by two
10	Interface Mode Select	0	CPU interface mode
		1	DMA (peripheral interface) mode
11-12	Expansion Mode	00	Standalone mode
		01	Reserved
		10	Expanded least significant (Slave)
		11	(Expanded most significant (Master)
13	Unused	Note: All default to 0.	
14	Unused		
15	Unused		

Table 5. Register 5 Format

Configuration Register 6: This register is unused.

Configuration Register 7: This is used to select parity functions (Table 6).

BIT	FUNCTION		
0-7	Unused		
8	Parity in Control B->A	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
9	Parity Out Control A->B	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even	0	Odd
		1	Even
11	Select Parity Error on Flag A pin	0	No Parity Error
		1	Parity Error
15-12	Unused	Note: All default to 0.	

Table 6. Parity Function

Status Register

There are two formats for the status register (Table 7) which are selected using the Select Status Format command (opcode 7 of Table 2). Once a format has been selected it remains in force until reprogrammed by the select command.

Bit	Status Register Format 0
0	Even Byte Latch Bits 0-7
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Format: 0
12	A->B Full
13	A->B Full - Offset
14	B->A Empty
15	B->A Empty + Offset

Bit	Status Register Format 1
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A->B Empty
5	A->B Empty + Offset
6	B->A Full
7	B->A Full - Offset
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Format: 1
12	A->B Full
13	A->B Full - Offset
14	B->A Empty
15	B->A Empty + Offset

Note: All default to 0.

Table 7. Status Register Format

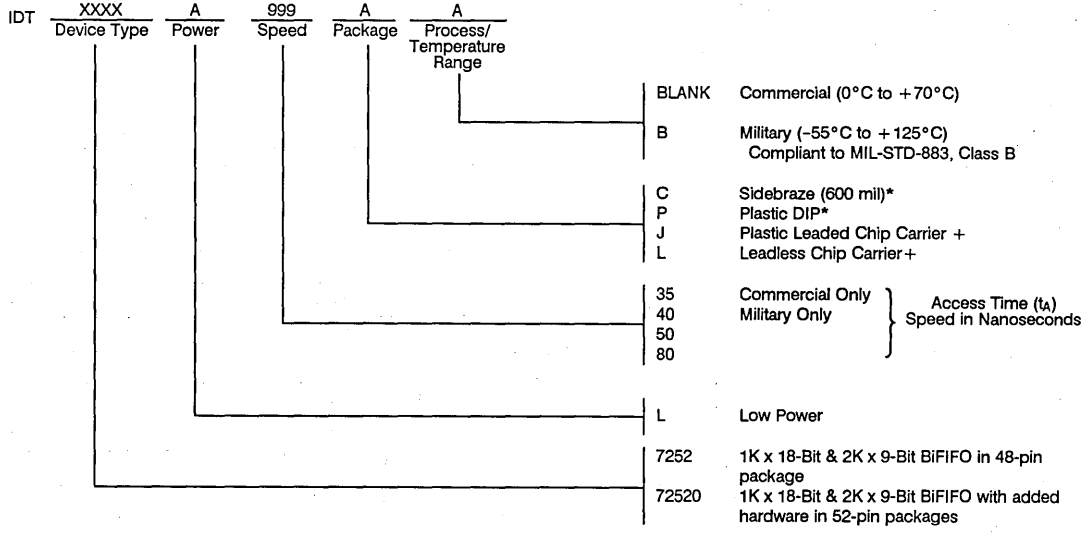
On reset and the default condition, the format 0 is selected. Once a format has been selected, the register is read via address A_1 , $A_0 = 11$.

In format 0, bits 0 through 7 are the contents of the odd byte latch. Taken together with the valid bit (bit 8), the processor can determine if there is a byte written into the BiFIFO and what the byte is. When Bit 8 = 0, a byte is written into the BiFIFO but not yet in the B->A FIFO memory.

In format 1, bits 0 through 2 are reserved. Bit 3 is the DMA direction selected via the command register: 0 for A->B and 1 for B->A. Bits 4 to 7 reflect the status FIFOs on the Data B side.

The reset of the bits are the same for format 0 and 1. Bit 9 is the Write Parity Error flag active High. The Write Parity Error flag is associated with data written into the B->A FIFO on the Data B bus. Bit 10 is the Read Parity Error flag active High. The Read Parity Error flag is associated with data read from the A->B FIFO on the Data B bus. The parity error flag once set remain set until cleared using the clear parity error commands. Bit 11 is the status format selected. The status format verifies the present Status Register Format the user is in. Bits 12 to 15 reflect the Data A side of the FIFOs.

ORDERING INFORMATION



*IDT7252 Only
+IDT72520 Only

Integrated Device Technology, Inc.

1K x 18-BIT CMOS BiFIFO

PRELIMINARY
IDT 72521

FEATURES:

- Bi-directional First-In/First Out (FIFO) memory
- Back-to-back 1K x 18-bit FIFO organization
- 35ns access time
- Facilitates processor-to-peripheral and processor-to-processor communication
- Matches bus widths: 16-bit to 16-bit and 32-bit to 32-bit buses
- Asynchronous and simultaneous read and write operations
- Width expandable to 36 bits
- Six general purpose programmable I/O pins
- Hardware Reread and Rewrite
- Hardware Load Reread and Load Rewrite for data retransmission
- Hardware Reset
- Built-in pass-through path
- On-chip DMA for easy peripheral interfacing
- Available in 68-pin PGA, and 68-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72521 BiFIFO is a compact, highly integrated solution for simplifying data transfer between two processors or a processor and peripheral. With access speed of 35ns, the BiFIFO can improve system performance of the peripheral interface by virtue of its concurrent transfer capability. The BiFIFO can handle data transfer between 16-bit to 16-bit or 32-bit to 32-bit buses.

Both ports, organized in 1K x 18-bit, can be operated concurrently, essentially operating as two FIFOs in one chip. A data pass-through mode allows for command and status transfer between two devices. To improve system performance when interfacing to peripherals which support DMA operations, a Request (REQ) and Acknowledge ($\overline{ACK}$) handshake is included.

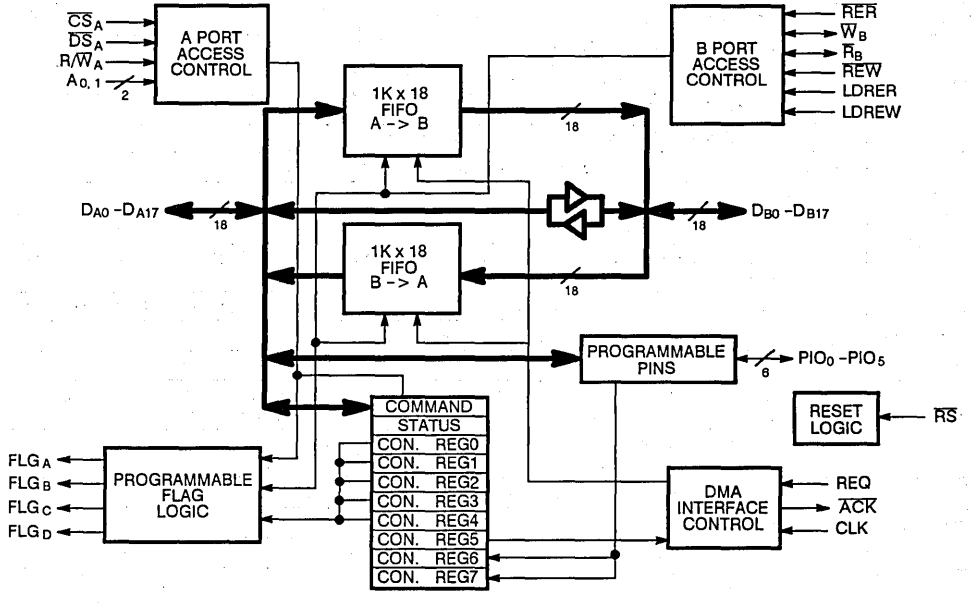
Four external flag pins can be used to configure and access any one of sixteen internal flags (four in each FIFO with both positive and negative polarity). The four internal flags are Empty, Empty + Offset, Full and Full-Offset. The offset value and flag polarity can be programmed through internal registers.

The BiFIFO incorporates Reread ($\overline{RER}$) and Rewrite ($\overline{REW}$). The internal read and write pointers can be set by the user through a control register. Upon signaling the $\overline{RER}$ input, the read pointer is set with value of $\overline{RER}$ pointer and data is read again. With signaling $\overline{REW}$, the write pointer is set with value of $\overline{REW}$ pointer and data is written again. These internal read and write pointers can be set by the user through a control register. In addition, the BiFIFO has hardware Load Reread, Load Rewrite and Reset capabilities.

The BiFIFO is available in a 68-pin PGA and 68-pin LCC and PLCC packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM



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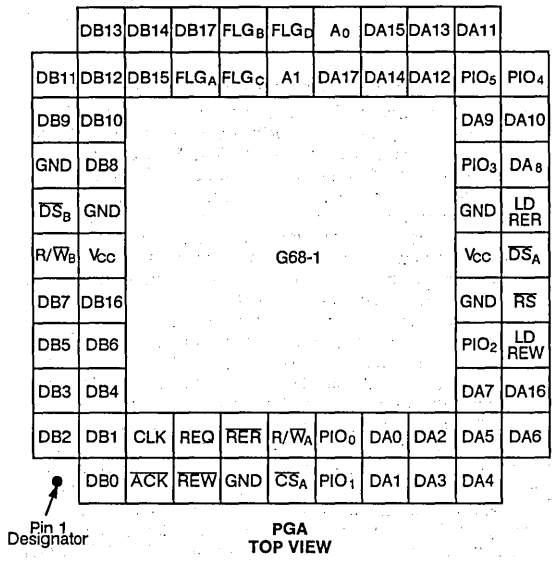
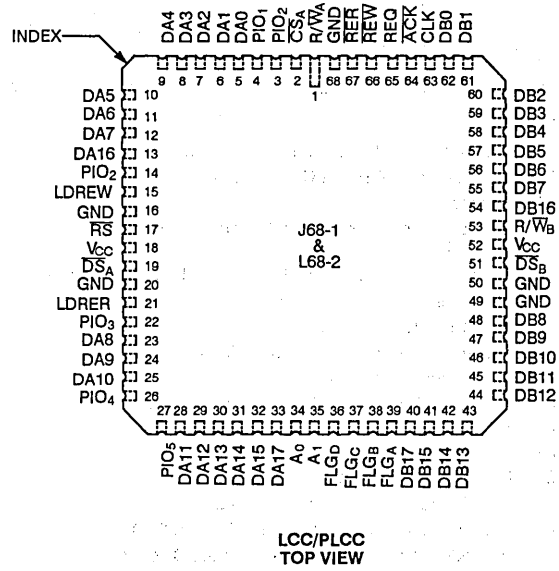
PIN CONFIGURATIONS





PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
$D_{A0} - D_{A17}$	Data A	I/O	Data inputs & outputs for 18-bit Port A.
$D_{B0} - D_{B17}$	Data B	I/O	Data inputs & outputs for 18-bit Port B.
$\overline{CS}_A$	Chip Select	I	Port A is accessed when chip select is LOW.
$\overline{DS}_A$	Data Strobe	I	Port A is accessed when $\overline{DS}_A$ is LOW, thereby activating Read or Write based upon selection of $R/\overline{W}_A$.
$\overline{DS}_B$	Data Srobe	I/O	Port B is accessed when $\overline{DS}_B$ is LOW.
$R/\overline{W}_A$	Read/Write	I	Controls Read or Write operation of Port A when $\overline{DS}_A$ is LOW.
$R/\overline{W}_B$	Read/Write	I/O	Controls Read or Write operation of Port B when $\overline{DS}_B$ is LOW.
$\overline{RER}$	Reread	I	Loads Read pointer with value of $\overline{RER}$ pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads Write pointer with value of $\overline{REW}$ pointer when LOW.
LDRER	Load Reread	I	Saves the Read pointer value in the Reread pointer.
LDREW	Load Rewrite	I	Saves the Write pointer value in the Rewrite Pointer.
$\overline{RS}$	Reset	I	Reset is performed through hardware pin, power up or by a bit in an internal register. During reset, both internal Read and Write pointers are set to the first location
REQ	Request	I	Port B input signal requesting a data transfer between B port and Peripheral through DMA handshake.
$\overline{ACK}$	Acknowledge	O	DMA handshake response to the active signal from REQ input.
CLK	Clock	I	Input clock pin (70% duty cycle max.).
A_0, A_1	Address	I	With $\overline{CS}_A$ LOW, address lines and $R/\overline{W}_A$ select one of the 6 modes, FIFO A->B, FIFO B->A, Direct pass-through path, configuration registers, status register, and command register.
$FLG_A - FLG_D$	Flags	O	These four pins output four of sixteen flags (Empty, Empty+Offset, Full, Full-Offset) for either A->B, or for B->A in two polarities. Flags are programmed via the configuration registers.
$PIO_0 - PIO_5$	Program Bits	I/O	Six general purpose programmable pins as either input or output ports.
V_{CC}	Power Supply		Two power supply pins, 5V.
GND	Ground		Five GND pins at 0V.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL}[1]	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT72521L COMMERCIAL T_A = 35, 50, 80ns			IDT72521L MILITARY T_A = 40, 50, 80ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL}[1]	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL}[2]	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	–	–	0.4	–	–	0.4	V
I_{CC1}[3]	Average V_{CC} Power Supply Current	–	90	160	–	120	170	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L)[3]	Power Down Current (All Input = V_{CC} = -0.2V)	–	–	2	–	–	4	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

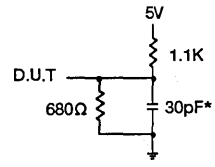


Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}[3]	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}[2, 3]	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES:

1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	FIG.	COM'L.		MIL.		MILITARY AND COMMERCIAL				UNIT
			72521x35		72521x40		72521x50		72521x80		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TIMINGS (A-Side 18-Bit)											
ta_A	Access Time	1	35	–	40	–	50	–	80	–	ns
ta_{RLZ}	Read Pulse Low to Data Bus at Low Z	1, 6	5	–	5	–	5	–	110	–	ns
ta_{RHZ}	Read Pulse High to Data Bus at High Z	1, 6	–	20	–	25	–	30	–	30	ns
ta_{DV}	Data Valid from Read Pulse High	1, 6	5	–	5	–	5	–	5	–	ns
ta_{RC}	Read Cycle Time	1	45	–	50	–	65	–	100	–	ns
ta_{RPW}	Read Pulse Width	1	35	–	40	–	50	–	80	–	ns
ta_{RR}	Read Recovery Time	1	10	–	10	–	15	–	20	–	ns
ta_{S1}	$\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ Set-Up Time	1	5	–	5	–	5	–	10	–	ns
ta_{H1}	$\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ Hold Time	1	5	–	5	–	5	–	10	–	ns
ta_{DS}	Data Set-Up Time	1, 2	18	–	20	–	30	–	40	–	ns
ta_{DH}	Data Hold Time	1, 2	0	–	0	–	5	–	10	–	ns
ta_{WC}	Write Cycle Time	1	45	–	50	–	65	–	100	–	ns
ta_{WPW}	Write Pulse Width	1, 2	35	–	40	–	50	–	80	–	ns
ta_{WR}	Write Recovery Time	1	10	–	10	–	15	–	20	–	ns
ta_{WRCOM}	Write Recovery Time after Command	2	35	–	40	–	50	–	80	–	ns

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	FIG.	COM'L. 72521x35		MIL. 72521x40		MILITARY AND COMMERCIAL 72521x50		72521x80		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TIMINGS (B-Side 9-Bit)											
tb_A	Access Time	3	35	–	40	–	50	–	80	–	ns
tb_{RLZ}	Read Pulse Low to Data Bus at Low Z	3, 6	5	–	5	–	5	–	10	–	ns
tb_{RHZ}	Read Pulse High to Data Bus at High Z	3, 6	–	20	–	25	–	30	–	30	ns
tb_{DV}	Data Valid from Read Pulse High	3, 6	5	–	5	–	5	–	5	–	ns
tb_{RC}	Read Cycle Time	3	45	–	50	–	65	–	100	–	ns
tb_{RPW}	Read Pulse Width	3	35	–	40	–	50	–	80	–	ns
tb_{RR}	Read Recovery Time	3	10	–	10	–	15	–	20	–	ns
tb_{S1}	R/$\overline{W}_B$ Set-Up Time	3	5	–	5	–	5	–	10	–	ns
tb_{H1}	R/$\overline{W}_B$ Hold Time	3	5	–	5	–	5	–	10	–	ns
tb_{DS}	Data Set-Up Time	3	18	–	20	–	30	–	40	–	ns
tb_{DH}	Data Hold Time	3	0	–	0	–	5	–	10	–	ns
tb_{WC}	Write Cycle Time	3	45	–	50	–	65	–	100	–	ns
tb_{WPW}	Write Pulse Width	3	35	–	40	–	50	–	80	–	ns
tb_{WR}	Write Recovery Time	3	10	–	10	–	15	–	20	–	ns
tb_{DSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW Set-Up and Recovery Time	4	10	–	10	–	15	–	15	–	ns
REQ-ACK (B-Side 9-Bit)											
tb_{CKC}	Clock Cycle Time	5	17.5	–	20	–	25	–	40	–	ns
tb_{CKH}	Clock Pulse HIGH	5	6	–	8	–	10	–	16	–	ns
tb_{CKL}	Clock Pulse LOW	5	6	–	8	–	10	–	16	–	ns
tb_{REQS}	Request Set-Up Time	5	5	–	5	–	10	–	10	–	ns
tb_{REQH}	Request Hold Time	5	5	–	5	–	5	–	5	–	ns
tb_{ACKL}	Delay From Rising Clock Edge to ACK Switching	5	18	–	20	–	25	–	35	–	ns

6

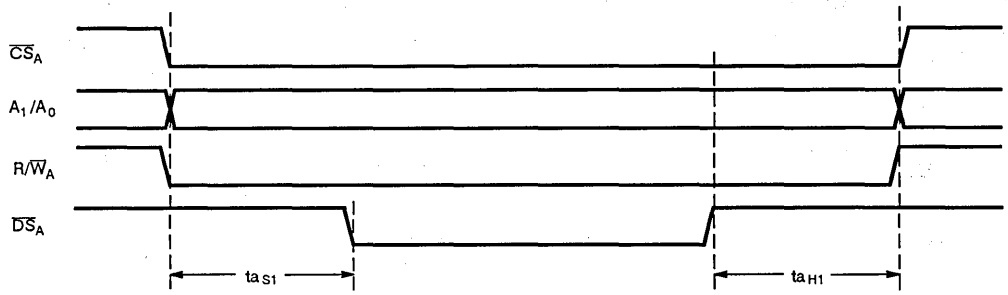
AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

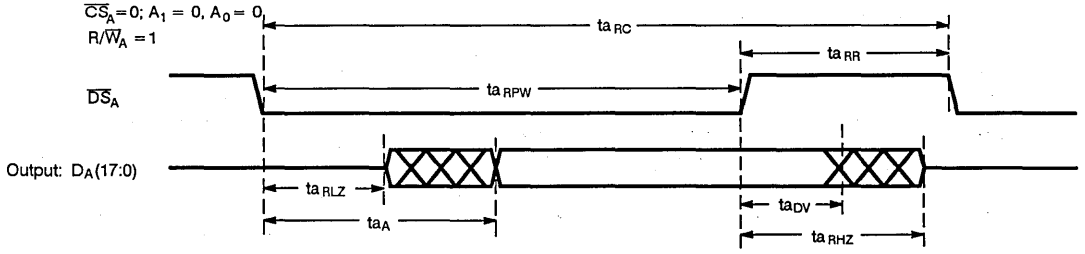
SYMBOL	PARAMETER	FIG.	COM'L.		MIL.		MILITARY AND COMMERCIAL				UNIT
			72521x35		72521x40		72521x50		72521x80		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
BYPASS MODE											
ta_{BYA}	B->A Bypass Access	6	20		25		30		40		ns
ta_{BYD}	B->A Bypass Delay	6	15		17		20		30		ns
ta_{BYH}	B->A Data Hold	6	5		5		5		10		ns
tb_{BYA}	A->B Bypass Access	6	20		25		30		40		ns
tb_{BYD}	A->B Bypass Delay	6	15		17		20		30		ns
tb_{BYH}	A->B Data Hold	6	5		5		5		10		ns
FLAGS TIMINGS											
t_{REF}	$\overline{R}$ LOW to $\overline{EF}$ LOW	7	35		35		45		60		ns
t_{WEF}	$\overline{W}$ HIGH to $\overline{EF}$ HIGH	7	35		35		45		60		ns
t_{RFF}	$\overline{R}$ HIGH to $\overline{FF}$ HIGH	7	35		35		45		60		ns
t_{WFF}	$\overline{W}$ LOW to $\overline{FF}$ LOW	7	35		35		45		60		ns
t_{RAEF}	$\overline{R}$ Low to Almost $\overline{EF}$ LOW	7	50		50		60		75		ns
t_{WAEF}	$\overline{W}$ High to Almost $\overline{EF}$ High	7	50		50		60		75		ns
t_{RAFF}	$\overline{R}$ High to Almost $\overline{FF}$ High	7	50		50		60		75		ns
t_{WAFF}	$\overline{W}$ Low to Almost $\overline{FF}$ Low	7	50		50		60		75		ns
PROGRAMMABLE I/O TIMINGS											
t_{PIOA}	PIO Access Time	8	25	–	25	–	30	–	30	–	ns
t_{PIOS}	B->A Set-Up Time	8	5	–	5	–	10	–	10	–	ns
t_{PIOH}	B->A Hold Time	8	5	–	5	–	10	–	10	–	ns

NOTE:

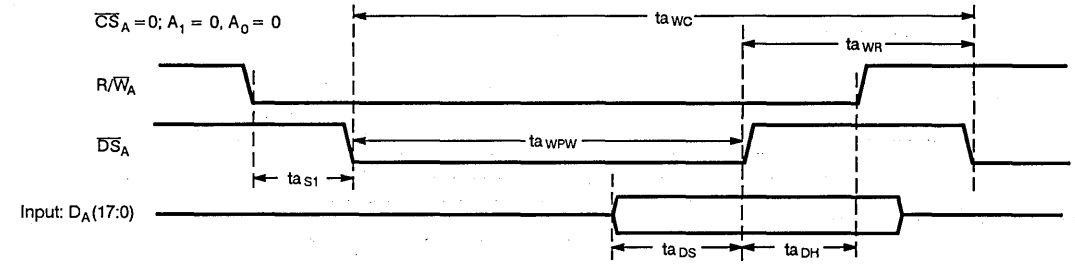
1. $\overline{R}$ or $\overline{W}$ is internal signal derived from $\overline{DS}_A$ & $R/\overline{W}_A$ or $\overline{DS}_A$ & $R/\overline{W}_B$.



READ



WRITE



Note: Refer to Address Control (Table 1) for other selection

Figure 1. Read and Write Timings (A-Side)

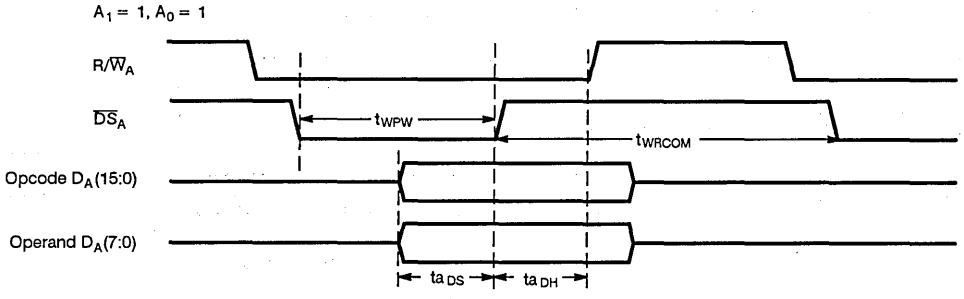
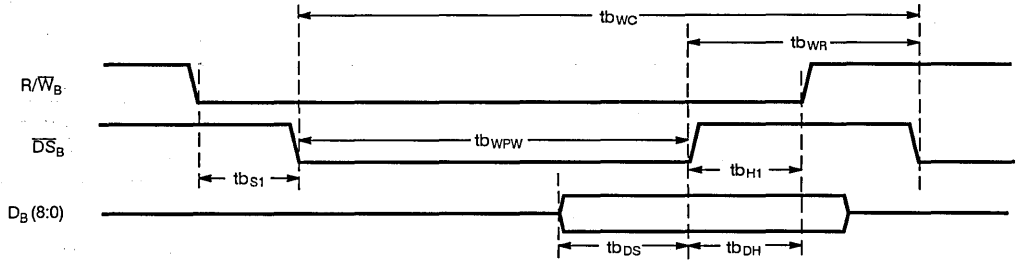


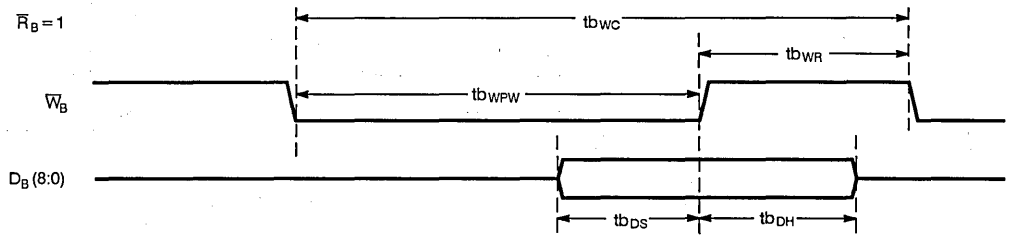
Figure 2. Carry Out Command Timing (A-Side Only)

WRITE

Case 1: When access controls are $R/\overline{W}_B$ and $\overline{DS}_B$

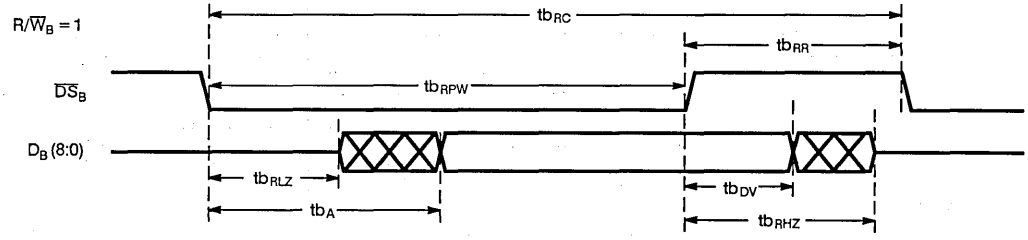


Case 2: When access controls $R/\overline{W}_B$ and $\overline{DS}_B$ are programmed as $\overline{R}_B$ and $\overline{W}_B$



READ

Case 1: When access controls are $R/\overline{W}_B$ and $\overline{DS}_B$



Case 2: When access controls $R/\overline{W}_B$ and $\overline{DS}_B$ are programmed as $\overline{R}_B$ and $\overline{W}_B$

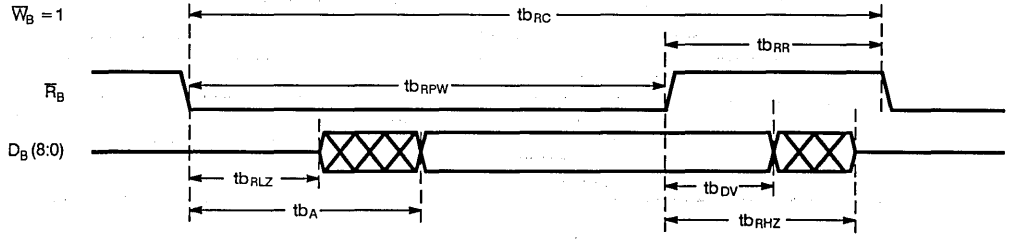
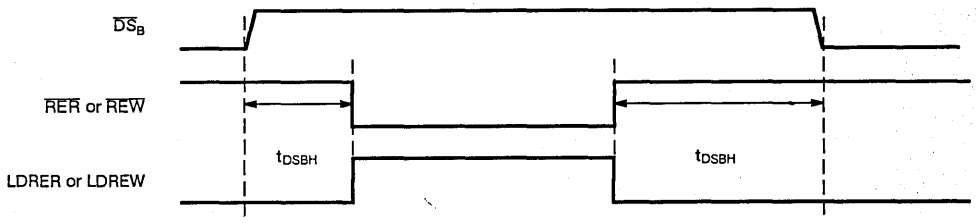


Figure 3. Read and Write Timings (B-Side)

Case 1: Access controls are R/$\overline{W}_B$ and $\overline{DS}_B$



Case 2: Access controls R/$\overline{W}_B$ and $\overline{DS}_B$ pins are programmed as $\overline{R}_B$ and $\overline{W}_B$

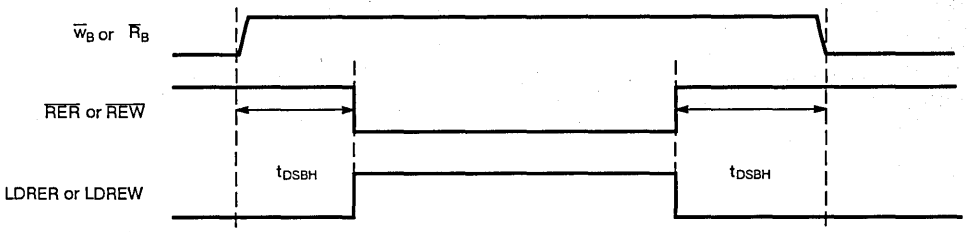
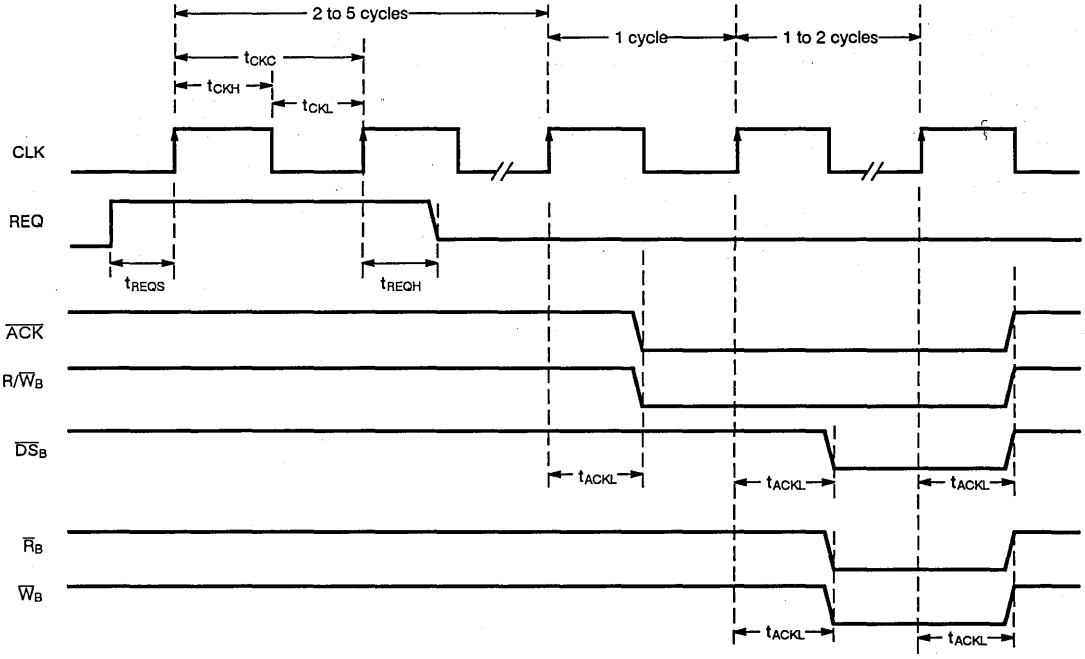


Figure 4. Reread, Rewrite, Load Reread, Load Rewrite Timings (B-Side)



te: Depends on the Intel or Motorola mode bit, BiFIFO either generates $\overline{DS}_B$ and R/$\overline{W}_B$ or $\overline{R}_B$ and $\overline{W}_B$ in the Request and Acknowledge mode

Figure 5. Request and Acknowledge Timings (B-Side Only)

BYPASS

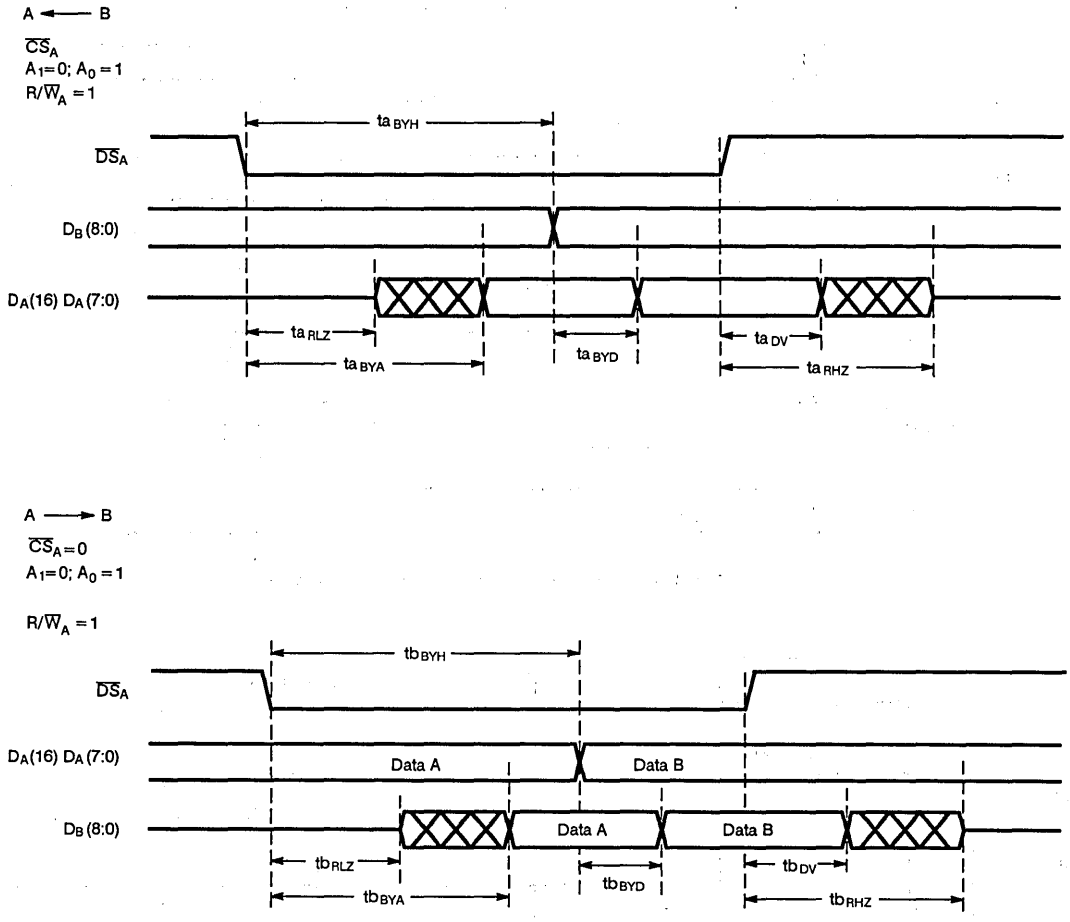
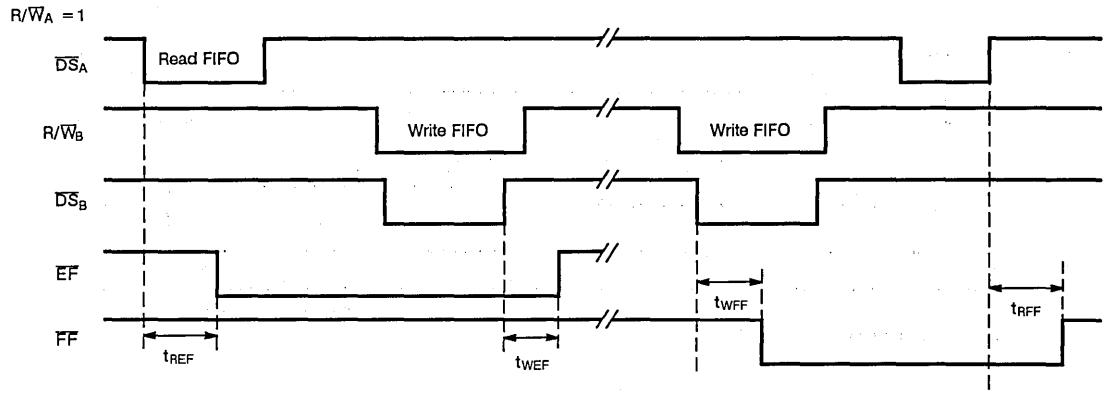


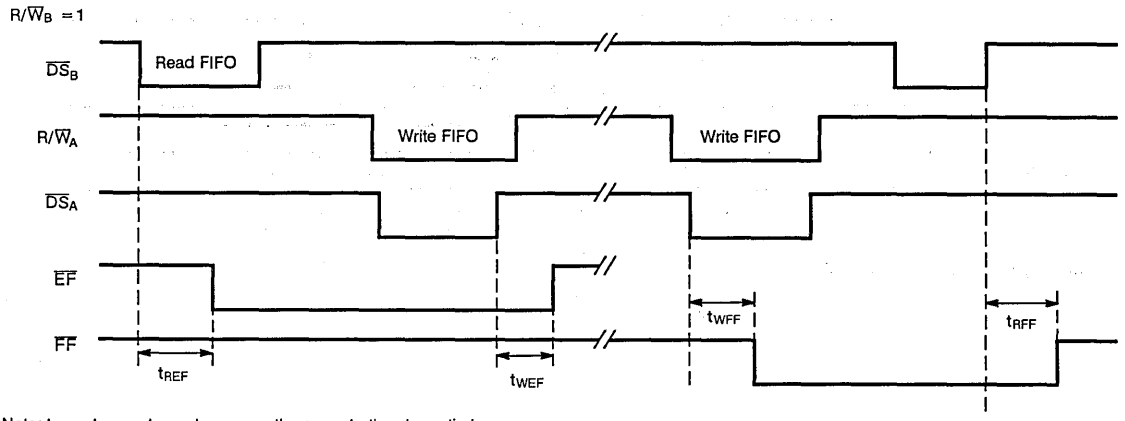
Figure 6. Bypass Timings

FIFO B ⟶ A: Empty and Full Flags



Note: t_{RAEF}, t_{WAEF}, t_{RAFF}, t_{WAFF} are the same to the above timings.

FIFO B ⟵ A: Empty and Full Flags

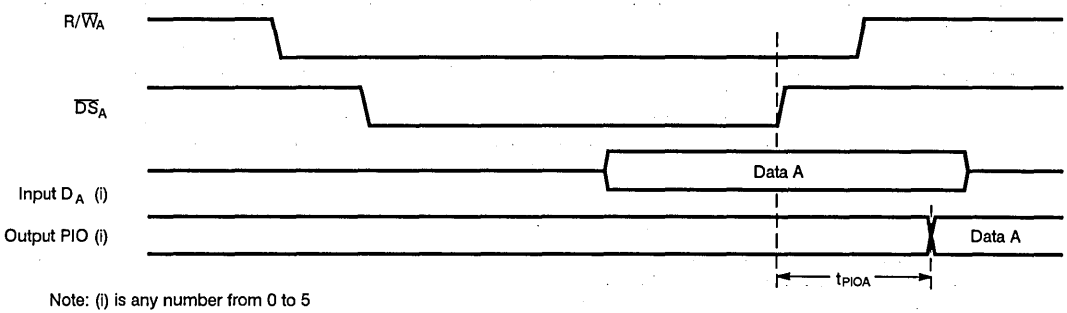


Note: t_{RAEF}, t_{WAEF}, t_{RAFF}, t_{WAFF} are the same to the above timings.

Figure 7. Flag Timings

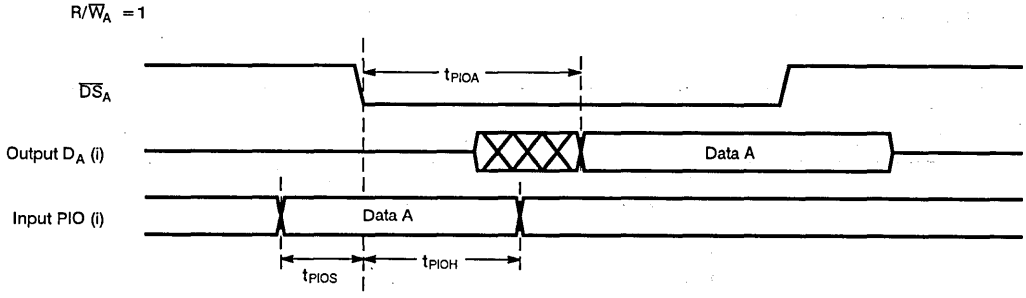
PROGRAMMABLE INPUT/OUTPUT (PIO)

A ⟶ B: Write Into Register 6



Note: (i) is any number from 0 to 5

A ⟵ B: Read from Register 6



Note: (i) is any number from 0 to 5

Figure 8. Programmable I/O Timings

FUNCTIONAL DESCRIPTION

FIFOs are used to link processors and peripherals together asynchronously to transfer data. Often the data on each side must be passed in both directions and requires two FIFOs arranged side-by-side. The BiFIFO is an integrated solution to this class of applications offering asynchronous bidirectional data buffering. The BiFIFO contains two 1K by 18 FIFOs connected side by side to two data ports: A and B.

The BiFIFO also contains several innovative, programmable features:

- DMA Style Handshake: Option available on port B side to control read and write activities when connected to peripherals with REQUEST and ACKNOWLEDGE kind of handshake.
- Block Transmit: Capability to Reread and Rewrite from port B.
- Flags: Four empty, full and programmable flags (empty+ offset, full-offset) per FIFO, can be multiplexed into four flag pins.
- Programmable I/O: Six general purpose programmable pins each can be an output or input or input ports.
- Pass-Through: On-chip transceiver to pass through the FIFOs for direct and synchronous communication between two data ports.

These features can be selected by programming a set of six internal Configuration Registers or by "executing a command" from port A. There are six possible modes of operation from port A, depending on $\overline{CS}_A$, A1 and A0 pins:

1. Port A disabled ($\overline{CS}_A = 0$)
2. FIFO access.
3. Direct access to port B, pass through FIFOs.
4. Program Configuration Registers.
5. Read Status Registers.
6. Carry out a command.

DMA Style Handshake Mechanism

There are two operational modes for the 8-bit (port B) interface. The modes are tailored to facilitate connection with intelligent devices such as CPUs which can generate read and write strobes, or less intelligent devices such as peripherals which require that read and write strobes be generated for them (see Figure 9).

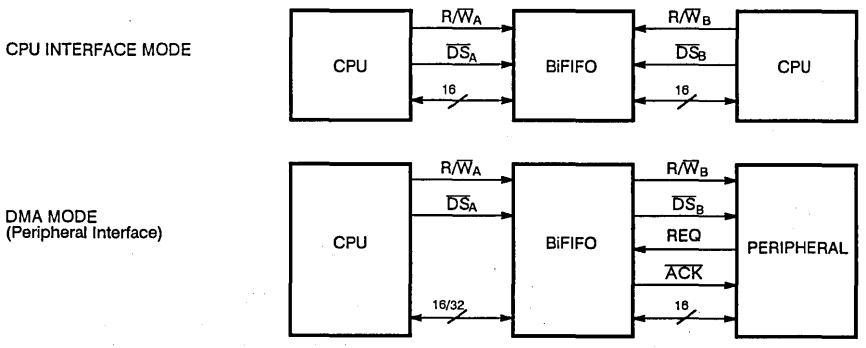


Figure 9. Interface Modes

The BiFIFO responds to an active signal on the $\overline{REQ}$ input by strobing the $\overline{ACK}$ and $\overline{DS}_B$ lines and asserting the R/$\overline{W}_B$ output. All timing is relative to a shift register clock generated by CLK or CLK divided by two. When in the DMA (peripheral) mode and the pass-through buffers are used for a synchronous transfer, the read/write strobe from the A port are passed through to the B port.

Reset

The IDT72521 can be reset through hardware pin, power up or through bit on register. During reset, both internal Read and Write pointers are set to the first location.

Programmable I/O

There are six programmable I/O pins: PIO (5:0). When programmed as inputs, PIO (5:0) can be read from port A's D_A (5:0). When PIO (5:0) are outputs, any data written into D_A (5:0) will show up on PIO (5:0). The data direction is individually selectable by programming the Register 7 (see Figure 10).

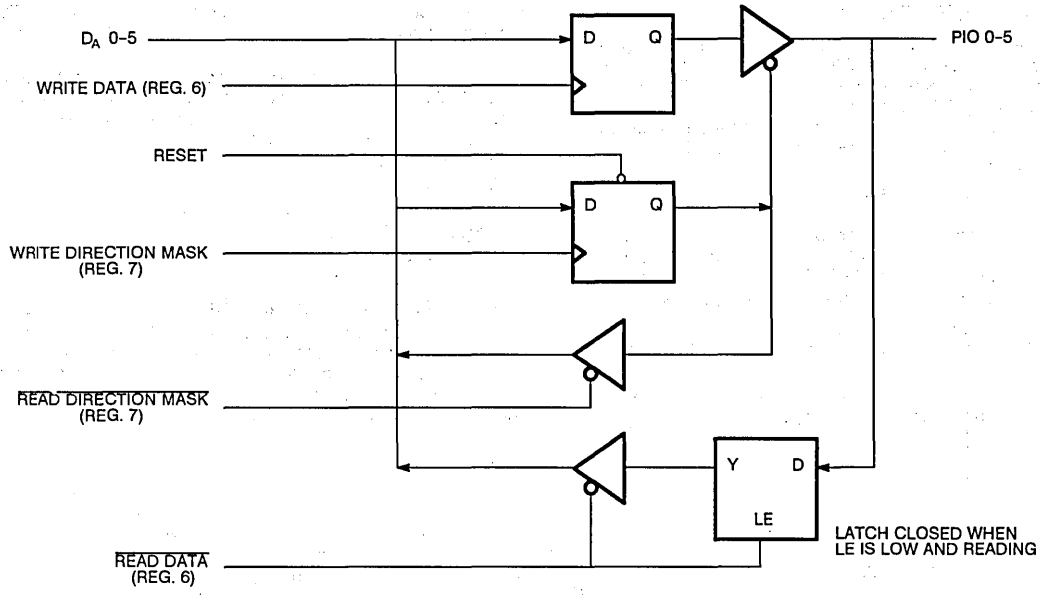


Figure 10. Programmable Input/Output

Pass-Through (Synchronous Access)

The BiFIFO includes a unique data path that bypasses the FIFOs such that a processor can talk synchronously with the peripheral to initialize it and then communicate asynchronously via the FIFOs. The parity generate and check circuitry (if selected) also comes into play during the synchronous transfer of data via the pass-through buffers. When in the peripheral (DMA) pass-through mode, the $\overline{DS_B}$ and $R/\overline{W_B}$ pins are outputs and reflect the action of the $\overline{DS_A}$ and $R/\overline{W_A}$ inputs. REQ should be low during initialization of BiFIFO and peripheral.

REGISTER DESCRIPTION

Address Control

The address lines indicate the resource to be accessed. There are six items that can be accessed: the FIFO B->A, FIFO A->B, 8-bit data bus, the flag configuration registers, status and command (see Table 1).

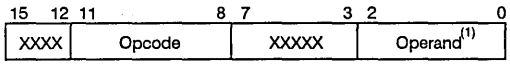
$\overline{CS_A}$	A_1	A_0	READ	WRITE
0	0	0	FIFO B->A	FIFO A->B
0	0	1	18-bit bus direct	18-bit bus direct
0	1	0	Configuration Register	Configuration Register
0	1	1	Status	Command
1	X	X	X	X

Note: Port B uses $\overline{DS_B}$ and $R/\overline{W_B}$ in the same way that Port A generates internal strobes.

Table 1. Address Control for Port A.

Command Register

The command feature allows the user to direct the BiFIFO to do something in real-time rather than setting up configuration registers in an idle condition. The command port format and a list of commands is shown in Table 2. The commands are accessed through the command port (A_1, $A_0 = 11$).



Opcode	Function
0	Reset BiFIFO functions (see operands)
1	Select Configuration Register (see Table 3)
2	Load Read point with Reread pointer value
3	Load Write pointer with Rewrite pointer value
4	Load Reread pointer with Read pointer value
5	Load Rewrite pointer with Write pointer value
6	Set DMA transfer direction (see operand)
7	Reserved
8	Increment read pointer on B side
9	Increment write pointer on B side
A	Reserved
B	Reserved

Operands(1)	Function
000	No operation
001	Reset FIFO B->A (Read, Write, and Rewrite pointers)
010	Reset FIFO A->B (Read, Write, and Reread pointers)
011	Reset B->A and A->B
100	Reset REQ circuitry
101	No operation
110	No operation
111	Reset all(2)

XX0	Write FIFO B->A
XX1	Read FIFO A->B

NOTES:
1. If operands are not shown for opcode, then they are in don't care condition.
2. Reset both FIFOs, REQ, Configuration Registers 0, 1, 2, 3, 5, 7. Reset Configuration Register 4 to default. DMA direction B→A. Clear Parity Error flags.

Table 2. Command Function and Operand

Configuration Registers

Several configuration registers control the BiFIFO operation (Table 3). The configuration registers are accessed by executing a command to point to a particular location, then reading or writing the content via address 2 (A_1, A_0 = 10). On reset, all registers except Register 4 (Tables 3, 4) default to Zero.

Operands	Selection	
000	Reg 0:	A->B Empty + Offset
001	Reg 1:	A->B Full - Offset
010	Reg 2:	B->A Empty + Offset
011	Reg 3:	B->A Full - Offset
100	Reg 4:	Flag D / Flag C / Flag B / Flag A
101	Reg 5:	General Control
110	Reg 6:	I/O Output Control
111	Reg 7:	I/O Direction Control

NOTE: 0110 0100 0010 0000 is default for Register A. All others default to 0.

Table 3. Configuration Registers

Configuration Registers 0 through 3: These program the offset for the almost empty and almost full flags. The values in these registers are unsigned positive numbers.

Configuration Register 4: This is used to select internal flags for the external flag pins A through D. The register is divided into four fields of four bits each. The four bit fields not only select which flag to output but also the polarity at the output. This creates an easier interface to processors and peripherals (see Table 4).

SEL	SELECTED FLAG
0000	$\overline{\text{Empty A->B}}$
0001	$\overline{\text{Empty + Offset A->B}}$
0010	$\overline{\text{Full A->B}}$
0011	$\overline{\text{Full - Offset A->B}}$
0100	$\overline{\text{Empty B->A}}$
0101	$\overline{\text{Empty + Offset B->A}}$
0110	$\overline{\text{Full B->A}}$
0111	$\overline{\text{Full-Offset B->A}}$

SEL	SELECTED FLAG
1000	Empty A->B
1001	Empty + Offset A->B
1010	Full A->B
1011	Full - Offset A->B
1100	Empty B->A
1101	Empty + Offset B->A
1110	Full B->A
1111	Full-Offset B->A

Table 4. Flag Polarity and Selection Codes

Configuration Register 5: This contains fields to control various functions (see Table 5).

BIT	FUNCTION		
0	Select: DS_B & R/W_B or R_B & W_B	0	Provides the strobes as R_B & W_B (Intel Mode)
		1	DS_B & R/W_B (Motorola Mode)
1	Unused		
2	Enable Reread	0	Disable Reread
		1	Enable Reread
3	Enable Rewrite	0	Disable Rewrite
		1	Enable Rewrite
4	REQ polarity	0	REQ active HIGH
		1	REQ active LOW
5	ACK polarity	0	ACK active LOW
		1	ACK active HIGH
6-7	REQ/ACK Timing	00	2 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		01	3 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		10	4 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
		11	5 clock cycle between REQ ▲ & $\overline{ACK}$ ▼
8	Read & Write Strobe	0	Read and write strobe: 1 cycle LOW
		1	Read and write strobe: 2 cycle LOW
9	Clock Frequency (Internal)	0	CLK signal generates the REQ/ACK sequence
		1	CLK signal divided by two
10	Interface Mode Select	0	CPU interface mode
		1	DMA (peripheral interface) mode
11-15	Unused	**Note:** All default to 0.	

Table 5. Register 5 Format

Configuration Register 6: The configuration register 6 is used to store data to be output on the I/O pins. Data to be output is written into the bit position: 0 to 5. The bit positions 6 through 15 are unused. This register can only be written.

15 ... 6	5	4	3	2	1	0
BIT 6-15 ARE UNUSED	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

Table 6. I/O Output Control

Configuration Register 7:

This configuration register 7 is the mask register which is used to control the direction of the I/O pins. This register can be read or written from the A side. Each bits of the register 6 controls the direction of the I/O pin respectively. A logic zero selects the corresponding I/O pin as an input. A logic one selects the I/O pin as an output. The default is logic zero.

15 6	5	4	3	2	1	0
BIT 6-15 ARE UNUSED	MI/O5	MI/O4	MI/O3	MI/O2	MI/O1	MI/O0

Table 7. I/O Direction Control

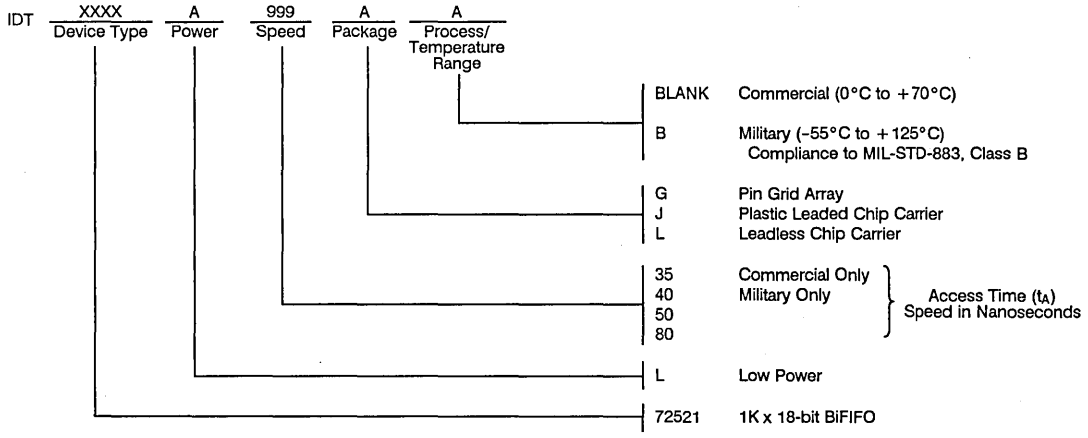
Status Register

Bit 0 through 2 are unused. Bit 3 is the DMA direction selected via the command register: 0 for A->B and 1 for B->A. The bit 4 through 7 are flag status which are: Empty A->B, Empty+Offset A->B, Full-Offset B->A and Full B->A. The bits 8 through 11 are unused. The status bits for the Data A side of the FIFOs are found in bits 12 to 15: Full-Offset A->B, Full A->B, Empty B->A, and Empty+Offset B->A.

Bit	Status Register
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A->B Empty
5	A->B Empty + Offset
6	B->A Full
7	B->A Full - Offset
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	A->B Full
13	A->B Full - Offset
14	B->A Empty
15	B->A Empty + Offset

Table 8. Status Register Format

ORDERING INFORMATION



6

DIGITAL SIGNAL PROCESSING

Digital Signal Processing (DSP) building block components ease the high bandwidth digital processing of analog signals using complex algorithms. Integrated Device Technology's advances in VLSI design and CMOS technology have accelerated development of high-speed DSP building block components which address similar advances in DSP algorithms. All IDT DSP components are designed with a three-bus architecture, ideal for high bus bandwidth systems.

Fixed-point multipliers, multiplier-accumulators, multi-level pipeline register files and DSP arithmetic-logic units offer high-performance functions for 12-bit and 16-bit data. IDT offers the fastest fixed-point building blocks in the industry for the most demanding DSP system requirements.

IDT's goal is to provide the highest level of integration and highest performance components for the most demanding DSP systems.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIER WITH 32-BIT OUTPUT

PRELIMINARY
IDT 7317

FEATURES

- 16 x 16-bit parallel multiplier with 32-bit output available immediately
- 20ns clocked multiply time
- Low power consumption: 400mW Max.
- One clock and three register enables
- Unsigned, Two's Complement or Mixed-Mode operations
- Flexible output scaling shifter
- Pipeline or Flow-through modes
- TTL-compatible input/output
- Three-state outputs
- Produced with advanced submicron CEMOS™ technology
- Available in 84-pin PLCC and 84-lead Pin Grid Array (PGA)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT7317 is high-speed, low-power 16 x 16-bit multiplier that has double the throughput of comparable devices by virtue of a full 32-bit output product bus. The Most Significant Product (MSP) and Least Significant Product (LSP) can be independently enabled on an external 16-bit bus or simultaneously enabled on an external 32-bit bus. IDT's high-performance CEMOS™ technology produces very fast (20ns) clocked multiply times.

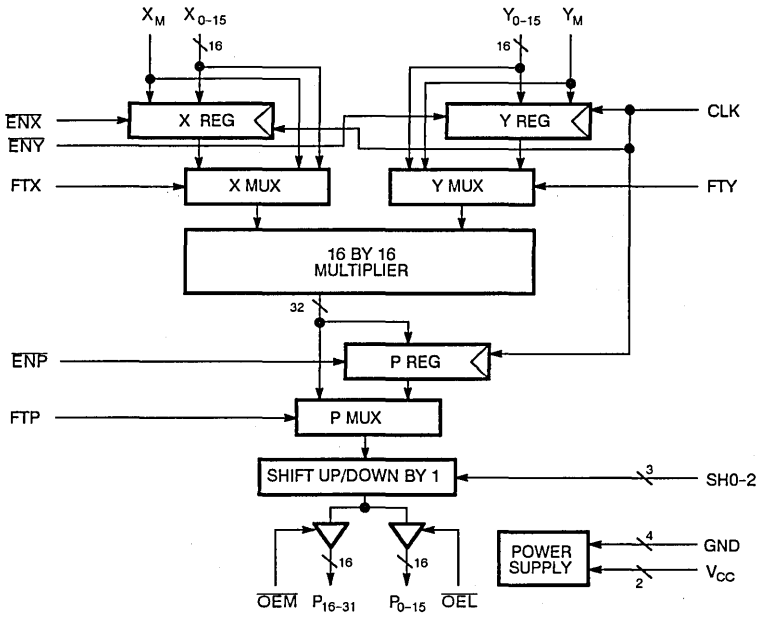
The output structure includes a programmable one-bit shifter for improved dynamic range algorithms using block floating point. This multiplier offers flexible configurations for clocked and flowed-through multiplications.

The IDT7317 is ideal for digital signal processing (DSP) applications requiring single-cycle 32-bit integer products. Some typical applications for this multiplier are 1-D and 2-D fast Fourier transforms (FFT), matrix multiplications, FIR and IIR filtering.

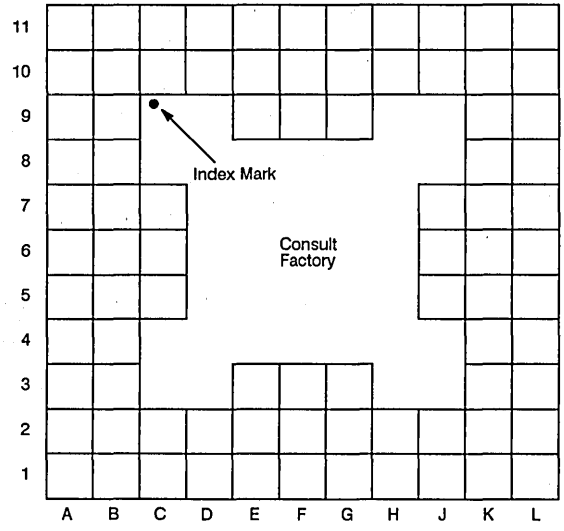
Military versions of the IDT7317 are manufactured in compliance with the latest revision of MIL-STD-883, Class B for high-reliability systems.

7

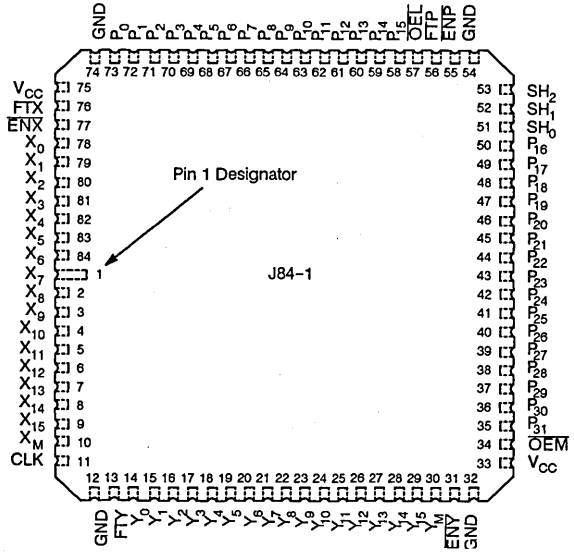
FUNCTIONAL BLOCK DIAGRAMS



CEMOS is a trademark of Integrated Device Technology, Inc.



PGA TOP VIEW



PLCC TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$X_0 - X_{15}$	I	Sixteen multiplicand data inputs.
XM	I	Mode control for X data input port. A LOW designates unsigned data input and a HIGH designates two's complement data input.
$Y_0 - Y_{15}$	I	Sixteen multiplier data inputs.
YM	I	Mode control for Y data input port. A LOW designates unsigned data input and a HIGH designates two's complement data input.
CLK	I	The rising edge of the clock loads all registers.
$\overline{ENX}$	I	Register enable for the X data input port along with the XM pin.
$\overline{ENY}$	I	Register enable for the Y data input port along with the YM pin.
$\overline{ENP}$	I	Register enable for the P output product.
FTX	I	When this control is HIGH, the X register is transparent; X input data and XM are not clocked.
FTY	I	When this control is HIGH, the Y register is transparent; Y input data and YM are not clocked.
FTP	I	When this control is HIGH, the P register is transparent; P output data is not clocked.
$SH_0 - SH_2$	I	Controls output product shifting. Shifting is controlled as follows:

SH_2	SH_1	SH_0	ACTION
0	X	X	no shift.
1	0	0	arithmetic shift left (up) by 1 position with 0 fill.
1	0	1	logical shift left (up) by 1 position with 0 fill.
1	1	0	arithmetic shift right (down) by 1 position with sign extension.
1	1	1	logical shift right (down) by 1 position with 0 fill.

$\overline{OEM}$	I	Three-state enable for most significant product ($P_{16} - P_{31}$).
$\overline{OEL}$	I	Three-state enable for least significant product ($P_0 - P_{15}$).
$P_0 - P_{15}$	O	Sixteen least significant product outputs.
$P_{16} - P_{31}$	O	Sixteen most significant product outputs.
V_{CC}		Two power pins at +5V potential nominal.
GND		Four ground pins.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open; f = 20MHz	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	15	35	–	15	45	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	2	10	–	2	15	mA
I_{CC}/f (2,3)	Increase in Power Supply Current MHz	V_{CC} = Max., f > 20MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 20MHz and V_{IN} = 0 to 3V. For frequencies greater than 20MHz, the following equation are used; for the commercial range, I_{CC} = 60 +4(f-20)mA; for the military range, I_{CC} = 80 + 6(f-20)mA; f is the operating frequency in MHz.
3. These limits are guaranteed but not tested..

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7317L20		7317L35		7317L55		7317L75		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MUC}	Unlocked Multiply Time[2]	–	35	–	55	–	75	–	100	ns
t_{MC}	Clocked Multiply Time[2]	–	20	–	35	–	55	–	75	ns
t_{SD}	X,Y Input Data Set-up Time[2]	8	–	10	–	13	–	18	–	ns
t_{HD}	X,Y Input Data Hold Time[2]	2	–	2	–	2	–	2	–	ns
t_{SE}	Clock Enable Set-up Time[2]	8	–	8	–	8	–	8	–	ns
t_{HE}	Clock Enable Hold Time[2]	2	–	2	–	2	–	2	–	ns
t_{PWH}	Clock Pulse Width High[2]	9	–	10	–	15	–	20	–	ns
t_{PWL}	Clock Pulse Width Low[2]	9	–	10	–	15	–	20	–	ns
t_{PDP}	Clock Output to P[2]	–	18	–	25	–	30	–	35	ns
t_{ENA}	3-State Enable Time[1]	–	18	–	25	–	30	–	35	ns
t_{DIS}	3-State Disable Time[1]	–	15	–	22	–	25	–	30	ns

NOTE:
1. Transition is measured +500mV from steady-state voltage with loading specified in Figure 1. V_X = 0 V and 2.6 V.
2. I_{OL} = 3.2 mA and I_{OH} = −0.8 mA during AC tests.

AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	7317L25		7317L40		7317L65		7317L90		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{MUC}	Unlocked Multiply Time[2]	–	38	–	60	–	85	–	125	ns
t_{MC}	Clocked Multiply Time[2]	–	25	–	40	–	65	–	90	ns
t_{SD}	X,Y Input Data Set-up Time[2]	12	–	15	–	20	–	25	–	ns
t_{HD}	X,Y Input Data Hold Time[2]	2	–	3	–	3	–	3	–	ns
t_{SE}	Clock Enable Set-up Time[2]	12	–	15	–	15	–	15	–	ns
t_{HE}	Clock Enable Hold Time[2]	2	–	3	–	3	–	3	–	ns
t_{PWH}	Clock Pulse Width High[2]	10	–	12	–	15	–	25	–	ns
t_{PWL}	Clock Pulse Width Low[2]	10	–	12	–	15	–	25	–	ns
t_{PDP}	Clock Output to P[2]	–	20	–	25	–	30	–	40	ns
t_{ENA}	3-State Enable Time[1]	–	20	–	25	–	30	–	40	ns
t_{DIS}	3-State Disable Time[1]	–	18	–	22	–	30	–	35	ns

NOTE:
1. Transition is measured +500mV from steady-state voltage with loading specified in Figure 1. V_X = 0 V and 2.6 V.
2. I_{OL} = 3.2 mA and I_{OH} = −0.8 mA during AC tests.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

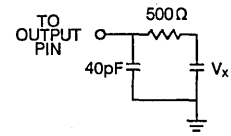


Figure 1. AC Output Test Load (V_X = 2.0V except for t_{DIS} and t_{ENA})

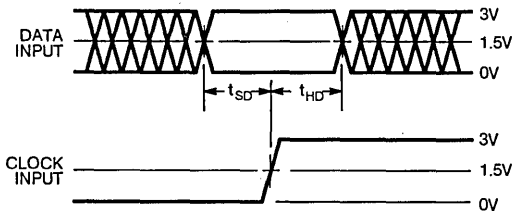


Figure 2. Set-Up And Hold Time

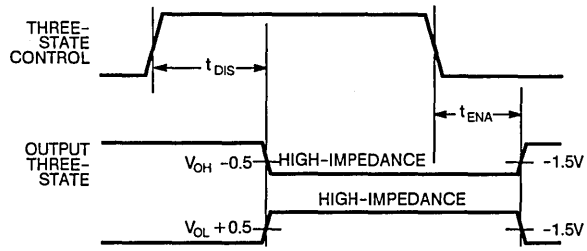


Figure 3. Three-State Control Timing Diagram

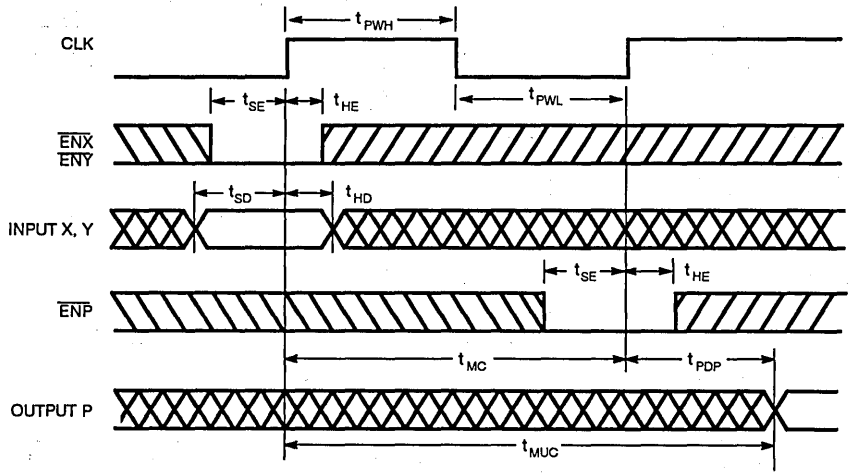


Figure 4. IDT7317 Timing Diagram

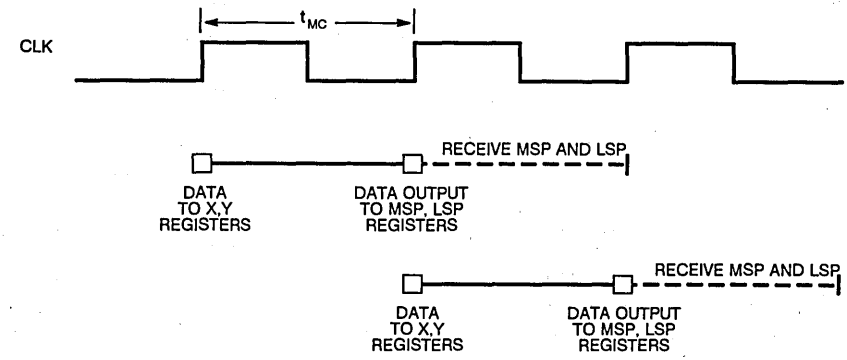


Figure 5. Simplified Timing Diagram–Typical Application

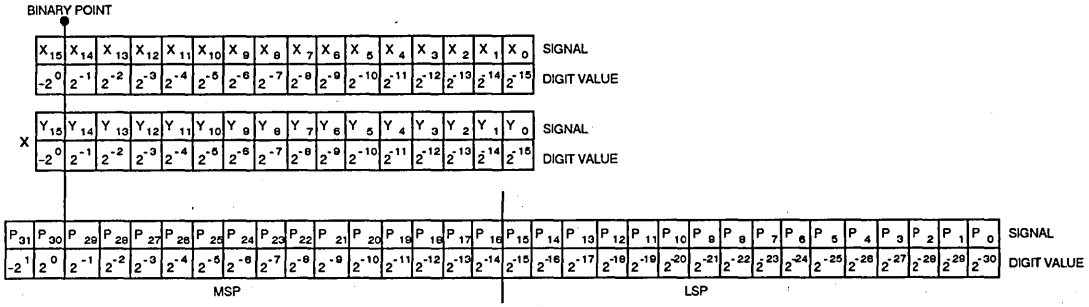


Figure 6. Fractional Two's Complement Notation

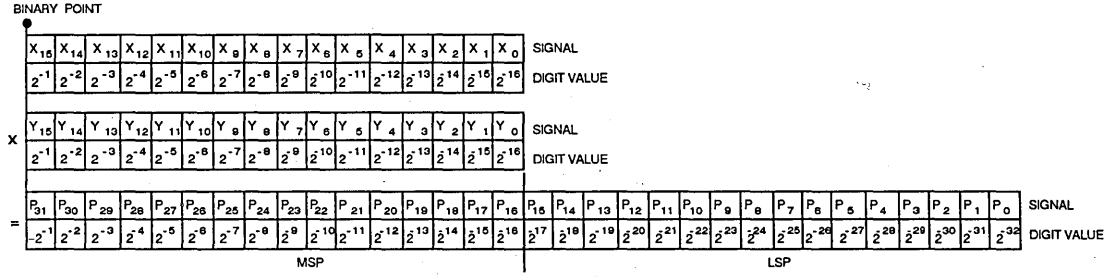


Figure 7. Fractional Unsigned Magnitude Notation

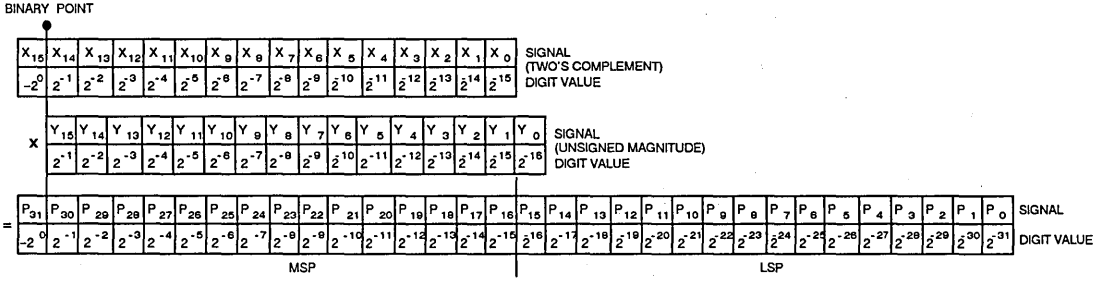


Figure 8. Fractional Mixed Mode Notation

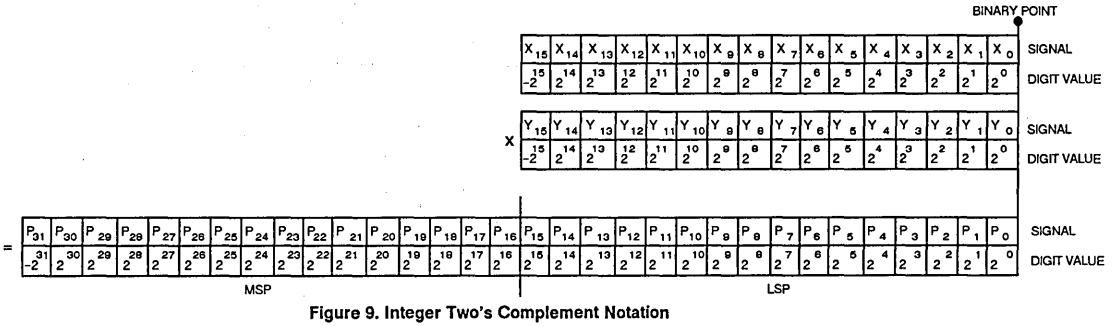


Figure 9. Integer Two's Complement Notation

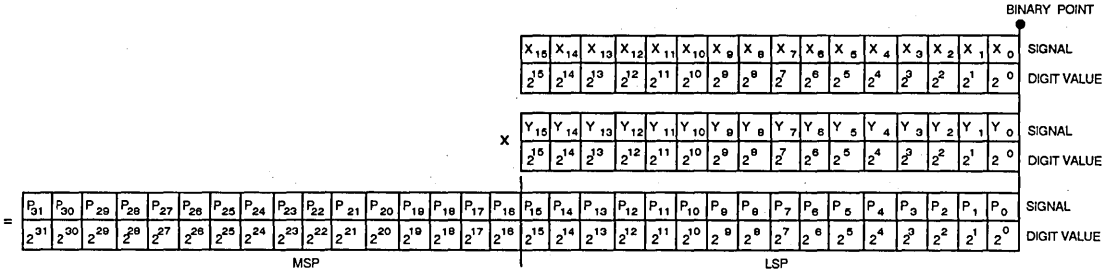


Figure 10. Integer Unsigned Magnitude Notation

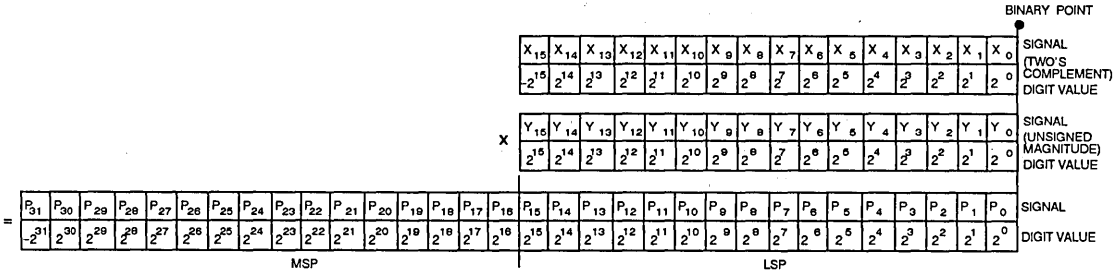
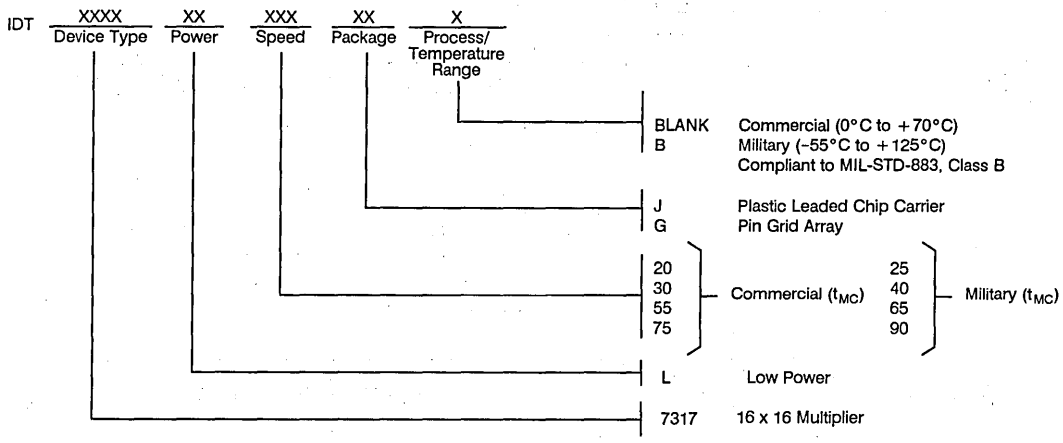


Figure 11. Integer Mixed Mode Notation

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

PRELIMINARY
IDT 7320
IDT 7321

FEATURES:

- IDT7320: Eight 16-bit high-speed pipeline registers
- IDT7321: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 12ns to 20ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Applications as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT7320 and IDT7321 are multilevel pipeline registers. With IDT's high-performance CEMOS technology, the IDT7320 and IDT7321 have access times of 12ns.

The IDT7320 contains eight 16-bit registers which can be configured as one 8-level, two 4-level, four 2-level or eight 1-level pipeline registers.

The IDT7321 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT7321. Three input control pins (SEL_0 - SEL_2) select which of the multiplexer inputs are directed to the output (Y_0 - Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations such as those in digital signal processing (DSP). The IDT7320 and IDT7321 can also be used as quick access scratch pad registers for general purpose computing.

The two pipeline registers are packaged in 48-pin plastic and ceramic DIPs for through-hole designs as well as 52-pin PLCC and LCC for surface mount designs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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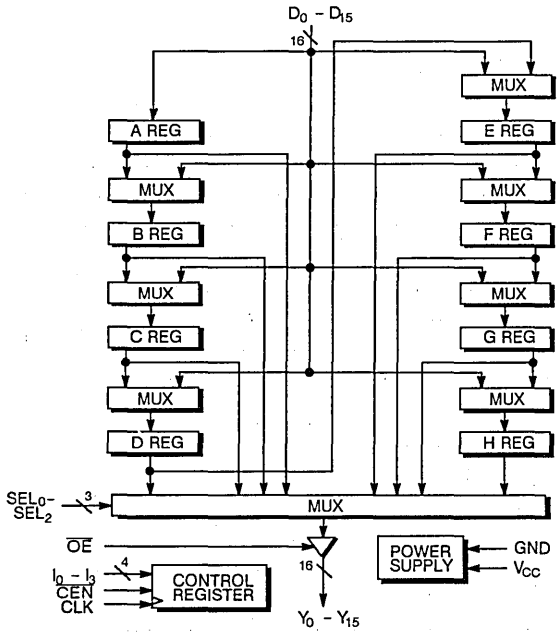
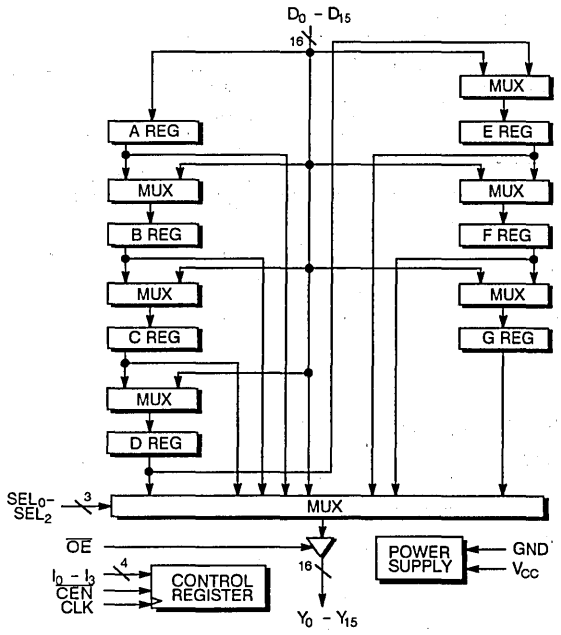
FUNCTIONAL BLOCK DIAGRAMS



IDT7320



IDT7321

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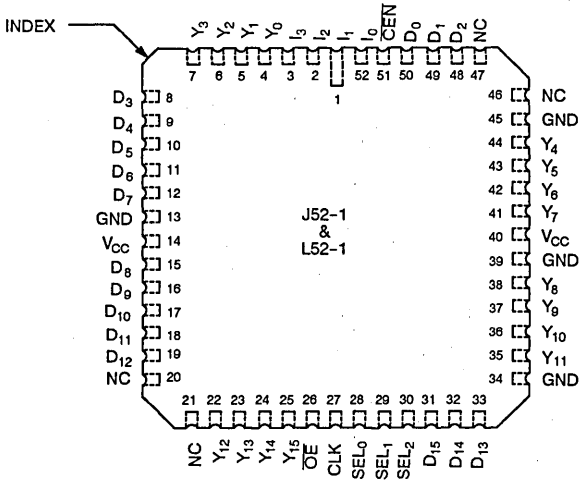
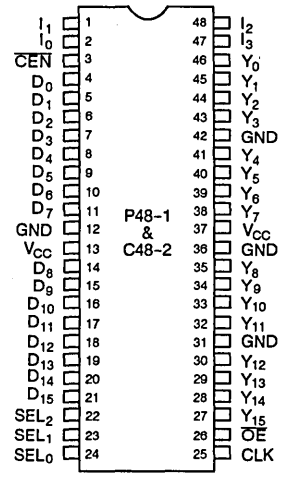
PIN CONFIGURATIONS



PLCC/LCC
TOP VIEW



DIP
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction $I_0 - I_3$ is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
V_{CC}		Power supply pin, 5V.
GND		Ground pins, 0V.

IDT7320 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y OUTPUT
0	0	0	A → $Y_0 - Y_{15}$
0	0	1	B → $Y_0 - Y_{15}$
0	1	0	C → $Y_0 - Y_{15}$
0	1	1	D → $Y_0 - Y_{15}$
1	0	0	E → $Y_0 - Y_{15}$
1	0	1	F → $Y_0 - Y_{15}$
1	1	0	G → $Y_0 - Y_{15}$
1	1	1	H → $Y_0 - Y_{15}$

IDT7321 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y OUTPUT
0	0	0	A → $Y_0 - Y_{15}$
0	0	1	B → $Y_0 - Y_{15}$
0	1	0	C → $Y_0 - Y_{15}$
0	1	1	D → $Y_0 - Y_{15}$
1	0	0	E → $Y_0 - Y_{15}$
1	0	1	F → $Y_0 - Y_{15}$
1	1	0	G → $Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

IDT7320 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	MNEMONIC	FUNCTION	PIPELINE LEVELS
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	–

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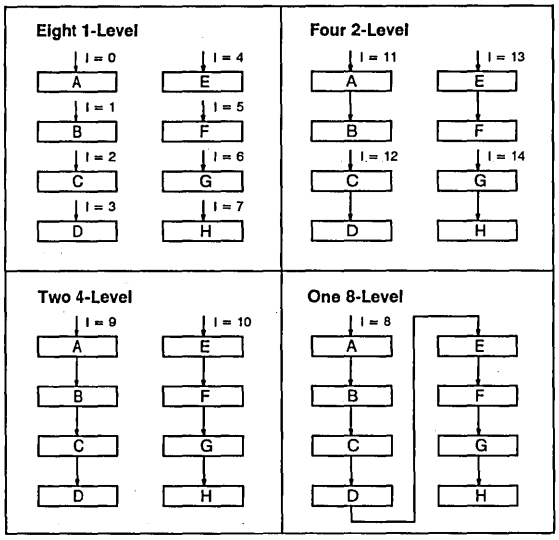
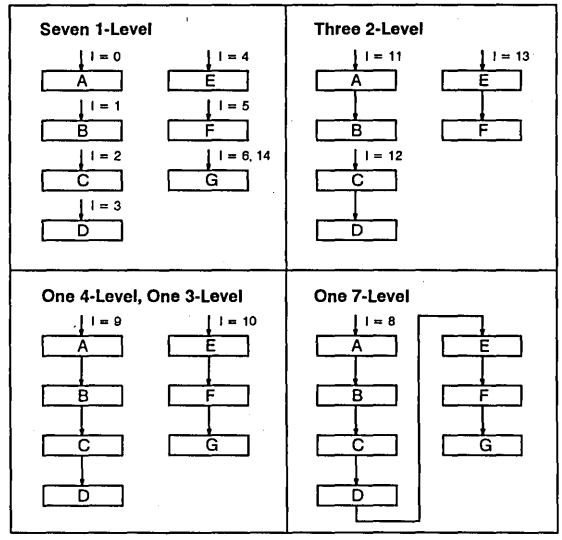
IDT7321 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	MNEMONIC	FUNCTION	PIPELINE LEVELS
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	–
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	–

IDT7320 PIPELINE CONFIGURATIONS



IDT7321 PIPELINE CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}	Operating Power Supply Current	Outputs Open; f = 67MHz							
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$							
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V							
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15.0mA (COM'L.), I_{OH} = -12.0mA (MIL.)	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0mA (COM'L.), I_{OL} = 20.0mA (MIL.)		–	0.4	–	–	0.4	V

NOTE:

1. Typical implies V_{CC} = 5V and T_A = +25°C.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

PARAMETER	7320L10 7321L10		7320L12 7321L12		7320L15 7321L15		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLK to Y_0 – Y_{15} Propagation Delay	–	–	–	12	–	15	ns
SEL_0 – SEL_2 to Y_0 – Y_{15} Propagation Delay	–	–	–	12	–	15	ns
D_0 – D_{15} to CLK Setup Time	–	–	3	–	4	–	ns
D_0 – D_{15} to CLK Hold Time	–	–	1	–	2	–	ns
I_0 – I_3 to CLK Setup Time	–	–	4	–	5	–	ns
I_0 – I_3 to CLK Hold Time	–	–	2	–	2	–	ns
$\overline{OE}$ Enable Time	–	–	–	9	–	10	ns
$\overline{OE}$ Disable Time	–	–	–	8	–	9	ns
CLK Pulse Width HIGH	–	–	4	–	5	–	ns
CLK Pulse Width LOW	–	–	4	–	5	–	ns
CLK Period	–	–	–	12	–	15	ns

AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to 125°C)

PARAMETER	7320L12 7321L12		7320L15 7321L15		7320L20 7321L20		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLK to Y_0 – Y_{15} Propagation Delay	–	–	–	15	–	20	ns
SEL_0 – SEL_2 to Y_0 – Y_{15} Propagation Delay	–	–	–	15	–	20	ns
D_0 – D_{15} to CLK Setup Time	–	–	4	–	5	–	ns
D_0 – D_{15} to CLK Hold Time	–	–	2	–	3	–	ns
I_0 – I_3 to CLK Setup Time	–	–	5	–	6	–	ns
I_0 – I_3 to CLK Hold Time	–	–	2	–	3	–	ns
$\overline{OE}$ Enable Time	–	–	–	10	–	13	ns
$\overline{OE}$ Disable Time	–	–	–	9	–	13	ns
CLK Pulse Width HIGH	–	–	5	–	6	–	ns
CLK Pulse Width LOW	–	–	5	–	6	–	ns
CLK Period	–	–	–	15	–	20	ns

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

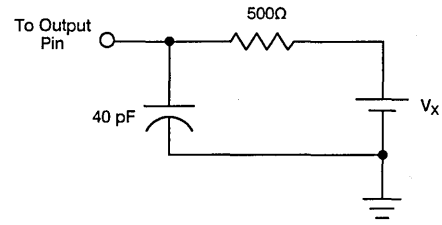
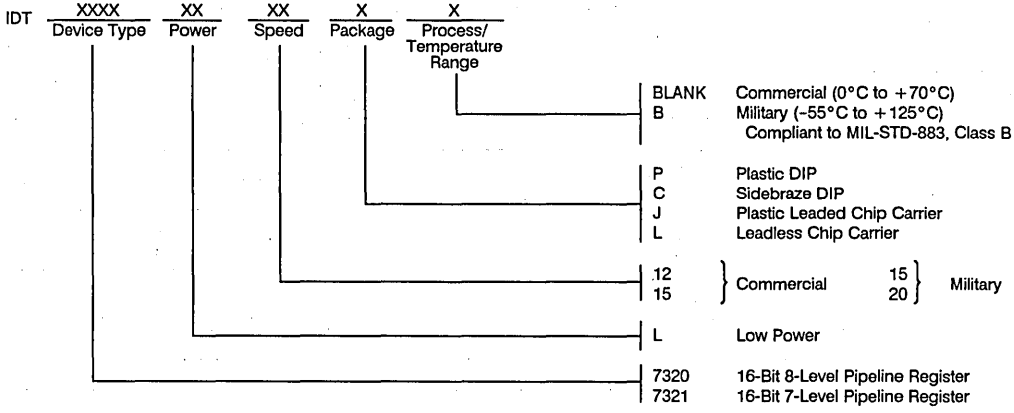


Figure 1. AC Output Test Load (V_X = 2.0V except for $\overline{OE}$ enable/disable)

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

PRELIMINARY
IDT 7381
IDT 7383

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - 54/74S381 instruction set (8 functions)
  - Replaces Gould S614381 or Logic Devices L4C381
  - Cascadable with or without carry look-ahead
- IDT7383:
  - 32 advanced ALU functions
- – Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 68-lead PGA and 68-pin surface mount PLCC, LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Units (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CEMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations and the R, S input selections to the ALU. The R and S ALU inputs can be A, B, F, 0 or all 1s. This ALU has a carry out pin for cascading.

The IDT7381 and IDT7383 are available in 68-pin PLCC, LCC or PGA packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

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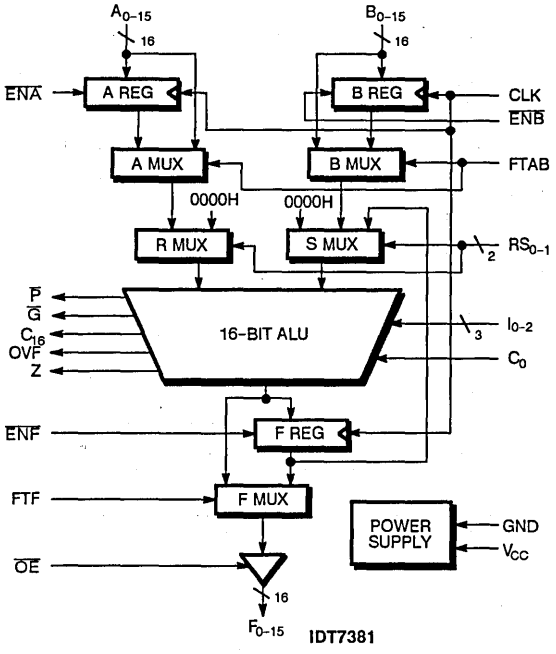
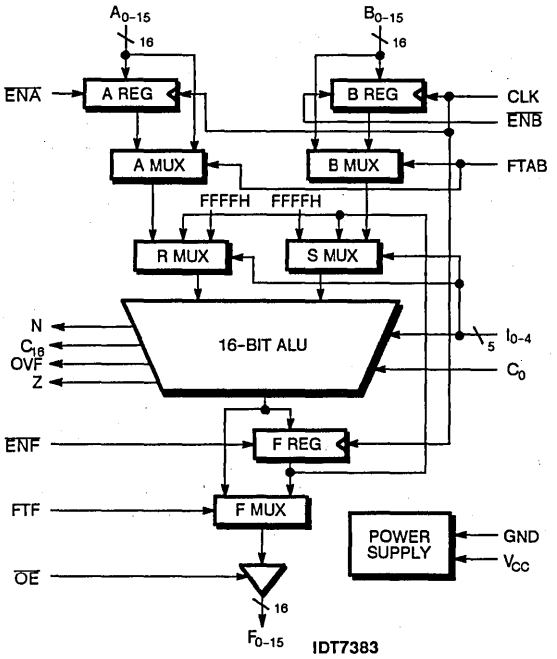
FUNCTIONAL BLOCK DIAGRAM

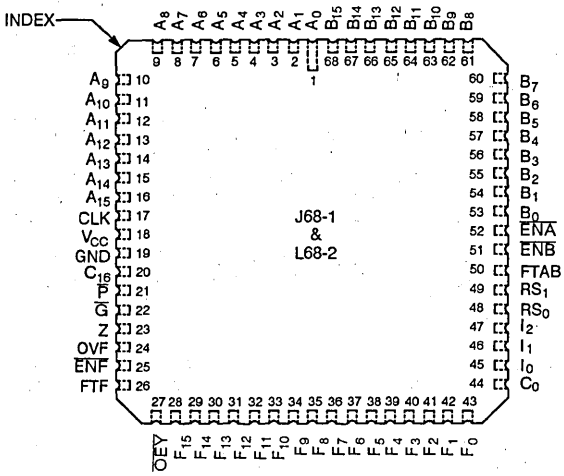




CEMOS is a trademark of Integrated Device Technology, Inc.

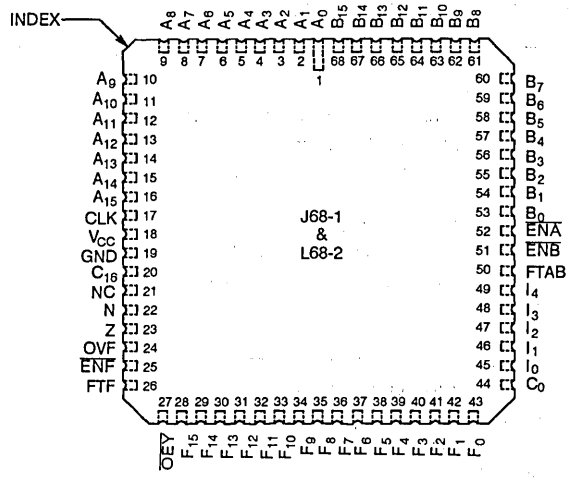
PIN CONFIGURATIONS

IDT7381

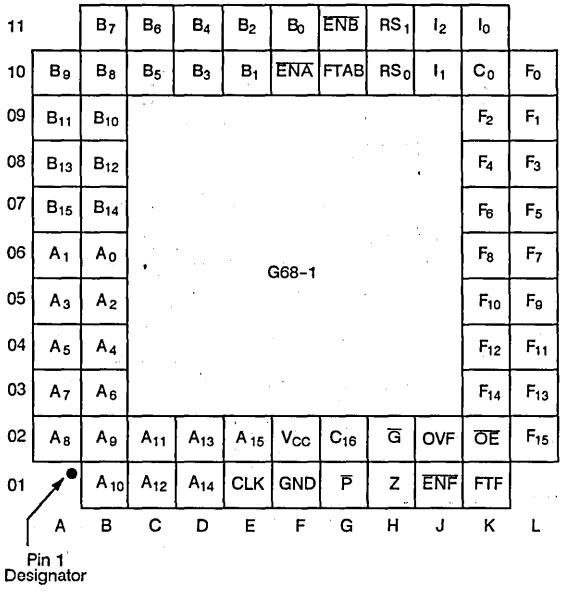


PLCC/LCC
TOP VIEW

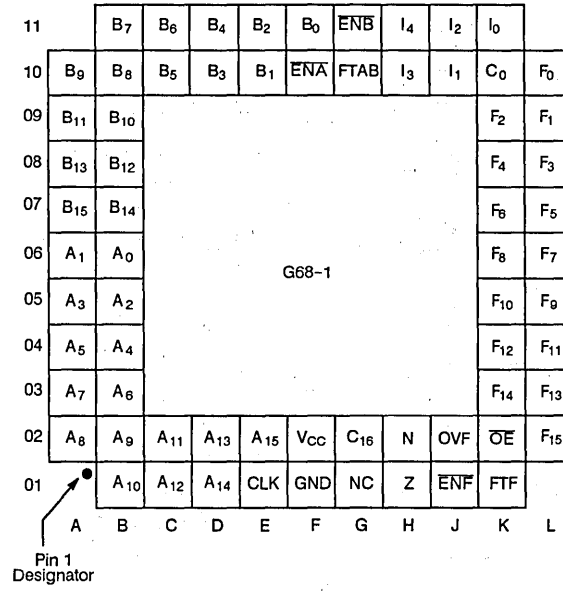
IDT7383



PLCC/LCC
TOP VIEW



PGA
TOP VIEW



PGA
TOP VIEW

PIN DESCRIPTIONS

IDT7381 AND IDT7383 PINS

PIN NAME	I/O	DESCRIPTION
$A_0 - A_{15}$	I	Sixteen-bit data input port.
$B_0 - B_{15}$	I	Sixteen-bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow-through control pin. When this pin is high, both register A and B are transparent.
$F_0 - F_{15}$	O	Sixteen-bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow-through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascaded configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow.
Z	O	This pin indicates a zero output result.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V.

IDT7381 PINS

PIN NAME	I/O	DESCRIPTION
$RS_0 - RS_1$	I	Two control pins used to select input operands for the R and S multiplexers.
$I_0 - I_2$	I	Three control pins to select the ALU function performed.
$\overline{P}$	O	Indicates the carry propagate output state of the ALU.
$\overline{G}$	O	Indicates the carry generate output state of the ALU.

IDT7381 R AND S MUX TABLE

RS_1	RS_0	R MUX	S MUX
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	FUNCTION
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

PIN DESCRIPTIONS (Continued)

IDT7383 PINS

PIN NAME	I/O	DESCRIPTION
$I_0 - I_4$	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	FUNCTION
0	0	0	0	0	$F = A + B + C_0$
0	0	0	0	1	F = A or B
0	0	0	1	0	$F = A + \overline{B}$ or C_0
0	0	0	1	1	$F = \overline{A} + B + C_0$
0	0	1	0	0	$F = A + C_0$
0	0	1	0	1	$F = \overline{A}$ or F
0	0	1	1	0	$F = A - 1 + C_0$
0	0	1	1	1	$F = \overline{A} + C_0$
0	1	0	0	0	$F = A + F + C_0$
0	1	0	0	1	F = A or F
0	1	0	1	0	$F = A + \overline{F} + C_0$
0	1	0	1	1	$F = \overline{A} + F + C_0$
0	1	1	0	0	$F = F + B + C_0$
0	1	1	0	1	$F = \overline{A}$ or B
0	1	1	1	0	$F = F + \overline{B} + C_0$
0	1	1	1	1	$F = \overline{F} + B + C_0$
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	$F = \overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	$F = \overline{A}$ and F
1	0	1	1	1	F = all 1's
1	1	0	0	0	$F = B + C_0$
1	1	0	0	1	F = A and $\overline{B}$
1	1	0	1	0	$F = \overline{B} + C_0$
1	1	0	1	1	$F = B - 1 + C_0$
1	1	1	0	0	$F = F + C_0$
1	1	1	0	1	F = A or $\overline{B}$
1	1	1	1	0	$F = F - 1 + C_0$
1	1	1	1	1	$F = \overline{F} + C_0$

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.[1]	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.[1]	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}	Operating Power Supply Current	Outputs Open; f = 25 MHz	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	15	35	–	15	45	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq 0.2V$	–	2	10	–	2	15	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0mA	–	–	0.4	–	–	0.4	V

NOTE:

1. Typical implies V_{CC} = 5V, T_A = +25°C

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

MAXIMUM COMBINATIONAL PROPAGATION DELAYS

FROM INPUT	TO OUTPUT								UNITS
	7381L20 7383L20		7381L25 7383L25		7381L40 7383L40		7381L55 7383L55		
	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	
FTAB = 0, FTF = 0									
CLK	9	18	11	23	18	36	25	50	ns
C_0	–	13	–	16	–	26	–	36	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	18	–	23	–	36	–	50	ns
FTAB = 0, FTF = 1									
CLK	18	18	23	23	36	36	50	50	ns
C_0	14	13	18	16	28	26	39	36	ns
$I_0 - I_4$, RS_0, RS_1(1)	20	18	25	23	40	36	55	50	ns
FTAB = 1, FTF = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	–	16	–	20	–	32	–	44	ns
CLK	9	–	11	–	18	–	25	–	ns
C_0	–	13	–	16	–	26	–	36	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	18	–	23	–	36	–	50	ns
FTAB = 1, FTF = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	17	16	21	20	34	32	47	44	ns
CLK	–	–	–	–	–	–	–	–	ns
C_0	14	13	18	16	28	26	39	36	ns
$I_0 - I_4$, RS_0, RS_1(1)	20	18	25	23	40	36	55	50	ns

MINIMUM SETUP AND HOLD TIMES RELATIVE TO CLOCK (CLK)

INPUT	7381L20 7383L20		7381L25 7383L25		7381L40 7383L40		7381L55 7383L55		UNITS
	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	
FTAB = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	4	0	5	0	8	0	11	0	ns
C_0	13	0	16	0	26	0	36	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	19	0	24	0	38	0	52	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	4	0	5	0	8	0	11	0	ns
FTAB = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	20	0	25	0	40	0	55	0	ns
C_0	20	0	25	0	40	0	55	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	20	0	25	0	40	0	55	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	–	–	–	–	–	–	–	–	ns

MINIMUM CLOCK CYCLE TIMES AND PULSE WIDTHS

PARAMETER	7381L20 7383L20	7381L25 7383L25	7381L40 7383L40	7381L55 7383L55	UNITS
Clock LOW Time	5	6	10	14	ns
Clock HIGH Time	5	6	10	14	ns
Clock Period	20	25	40	55	ns

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

PARAMETER	7381L20 7383L20	7381L25 7383L25	7381L40 7383L40	7381L55 7383L55	UNITS
Enable Time	8	10	16	22	ns
Disable Time	8	10	16	22	ns

NOTES:

1. For IDT7381, pins $I_0 - I_2$, RS_0, RS_1 apply. For IDT7383, pins $I_0 - I_4$ apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z, C_{16} for IDT7383.

AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

MAXIMUM COMBINATIONAL PROPAGATION DELAYS

FROM INPUT	TO OUTPUT								UNITS
	7381L25 7383L25		7381L30 7383L30		7381L40 7383L40		7381L55 7383L55		
	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	$F_0 - F_{15}$	FLAGS(2)	
FTAB = 0, FTF = 0									
CLK	15	29	17	36	22	43	30	60	ns
C_0	–	21	–	25	–	31	–	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	29	–	36	–	43	–	60	ns
FTAB = 0, FTF = 1									
CLK	29	29	36	36	43	43	60	60	ns
C_0	23	21	28	25	34	31	47	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	29	39	36	48	43	66	60	ns
FTAB = 1, FTF = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	–	26	–	31	–	38	–	53	ns
CLK	15	–	17	–	22	–	30	–	ns
C_0	–	21	–	25	–	31	–	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	–	29	–	36	–	43	–	60	ns
FTAB = 1, FTF = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	28	26	33	31	41	38	56	53	ns
CLK	–	–	–	–	–	–	–	–	ns
C_0	23	21	28	25	34	31	47	43	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	29	39	36	48	43	66	60	ns

MINIMUM SETUP AND HOLD TIMES RELATIVE TO CLOCK (CLK)

INPUT	7381L25 7383L25		7381L30 7383L30		7381L40 7383L40		7381L55 7383L55		UNITS
	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	SETUP	HOLD	
FTAB = 0									
$A_0 - A_{15}$, $B_0 - B_{15}$	7	0	8	0	10	0	13	0	ns
C_0	21	0	25	0	31	0	43	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	31	0	37	0	46	0	62	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	8	0	10	0	13	0	ns
FTAB = 1									
$A_0 - A_{15}$, $B_0 - B_{15}$	33	0	39	0	48	0	66	0	ns
C_0	33	0	39	0	48	0	66	0	ns
$I_0 - I_4$, RS_0, RS_1(1)	33	0	39	0	48	0	66	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	–	–	–	–	–	–	–	–	ns

MINIMUM CLOCK CYCLE TIMES AND PULSE WIDTHS

PARAMETER	7381L25 7383L25	7381L30 7383L30	7381L40 7383L40	7381L55 7383L55	UNITS
Clock LOW Time	6	8	10	14	ns
Clock HIGH Time	6	8	10	14	ns
Clock Period	25	30	40	55	ns

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

PARAMETER	7381L25 7383L25	7381L30 7383L30	7381L40 7383L40	7381L55 7383L55	UNITS
Enable Time	13	16	19	26	ns
Disable Time	13	16	19	26	ns

NOTES:

1. For IDT7381, pins $I_0 - I_2$, RS_0, RS_1 apply. For IDT7383, pins $I_0 - I_4$ apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z, C_{16} for IDT7383.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

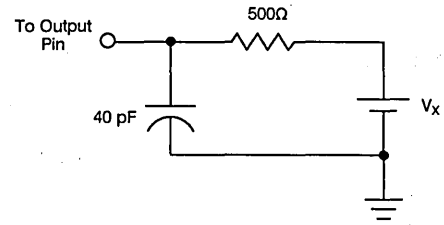
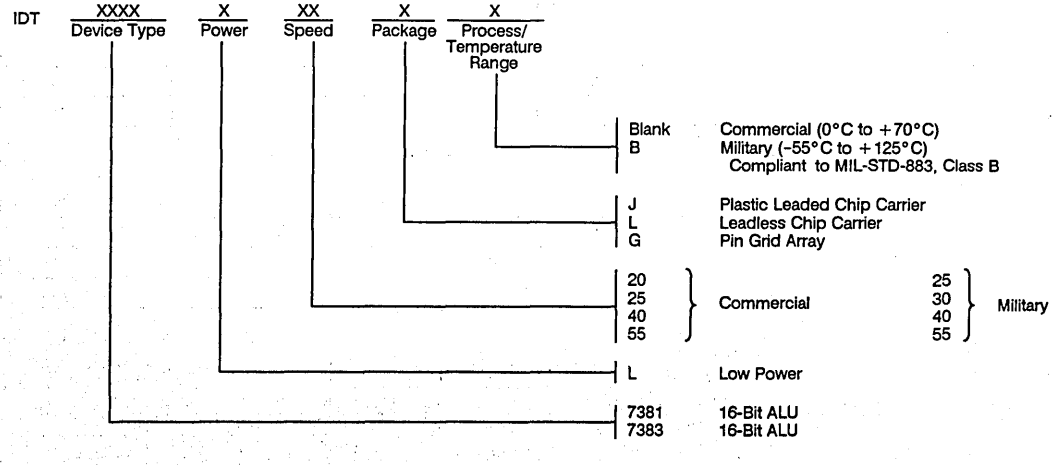


Figure 1. AC Output Test Load (V_X = 2.0V except for $\overline{OE}$ enable/disable)

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

ADVANCE INFORMATION
IDT 7384

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar, or image processing applications
- Includes flexible funnel shifter
- Pipeline or flow-through modes
- Multi-level pipeline register on one input port
- Three accumulators with an internal feedback path
- Scaling shifter on output stage for dynamic range control
- Rounding on output stage
- Bit reversal on output stage for FFT address generation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS ™ technology
- Available in 84-lead PGA and 84-pin surface mount PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7384 is a high-speed cascadable Arithmetic Logic Unit (ALU). This three-bus device has a 4-level pipeline register on one input port (A port) and a single input register on the other input port (B port). An ultra-fast 16-bit ALU, a funnel shifter with merge capabilities, and three accumulators make up the heart of the IDT7384. With IDT's high-performance CEMOS ™ technology, the IDT7384 can do arithmetic or logic operations in 20ns. Results of ALU operations can be scaled, rounded, or bit reversed for FFT address generation using the IDT7384 output stage.

The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F accumulators can also be set into clocked or flow-through mode. The A port has a 4-level pipeline register that can be configured as 1 four-level, 2 two-level, or 4 single-level pipelines. The three LDA0-LDA2 control pins set the configuration and the register loaded.

The IDT7384 has five function pins to select 1 of 32 arithmetic or logic operations and the R, S input selections to the ALU. The R and S ALU inputs can be A, B, F, or all 1's. This ALU has a carry out pin for cascading. Three accumulators are provided on the IDT7384 for intermediate result storage.

The IDT7384 funnel shifter will do logical shifts, rotates, and rotates with merges. The 16-bit R-multiplexer and S-multiplexer inputs can be concatenated in either order for 32-bit logical shifts. A 16-bit result is extracted at the funnel shifter output. The R-multiplexer input can be rotated or rotated and merged with the F-feedback bus using the S-multiplexer input as a mask.

The output stage of this ALU can round the F result up or down by one bit. The F result can also be arithmetically or logically shifted by one bit under the IDT7384 output control (FS0-FS5). Bit reversal can be performed on the F result to generate fast Fourier transform (FFT) addresses.

An output enable is provided for three-state control of the output port on a bus.

The IDT7384 is available in 84-pin PLCC or PGA packages. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B for high reliability systems.

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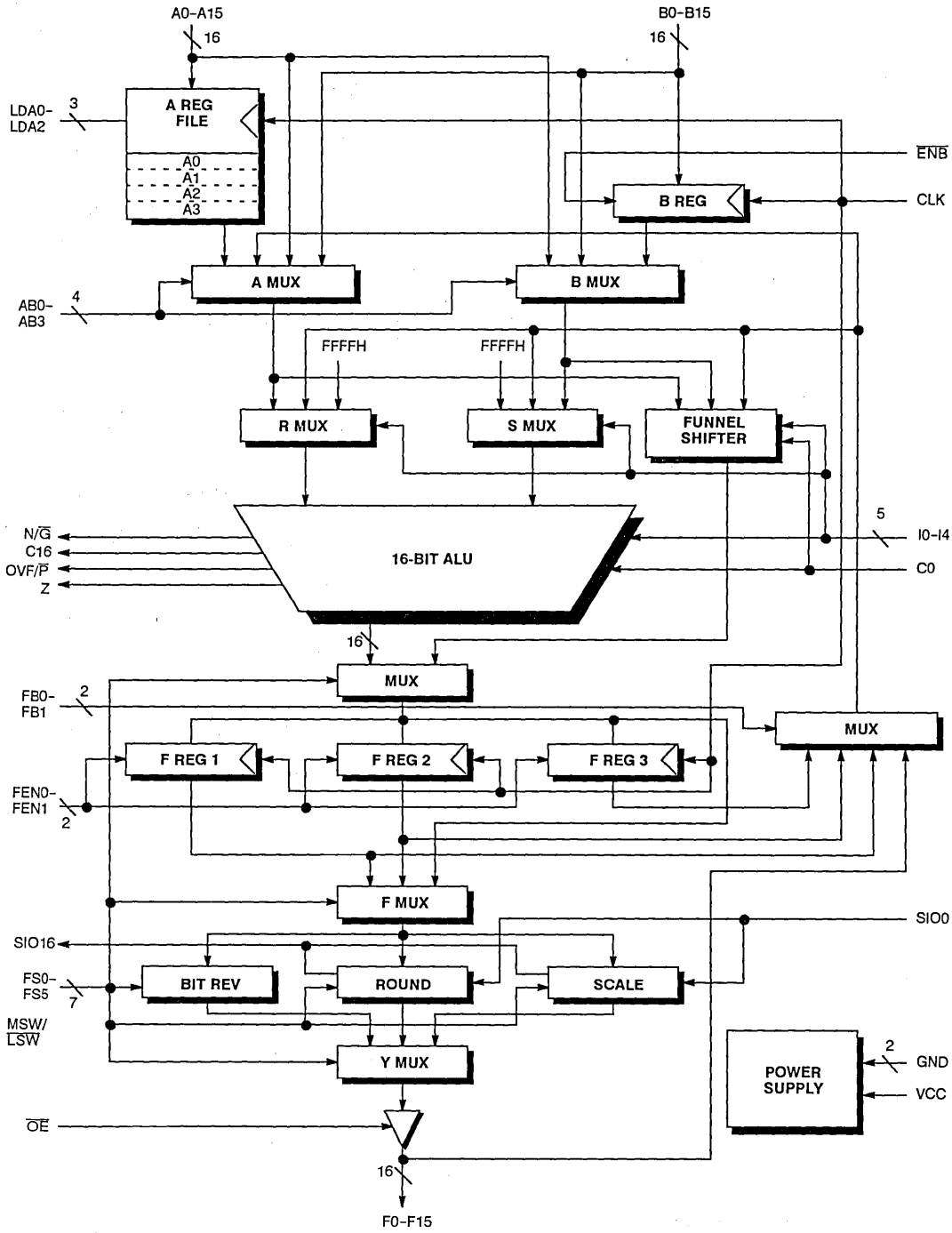
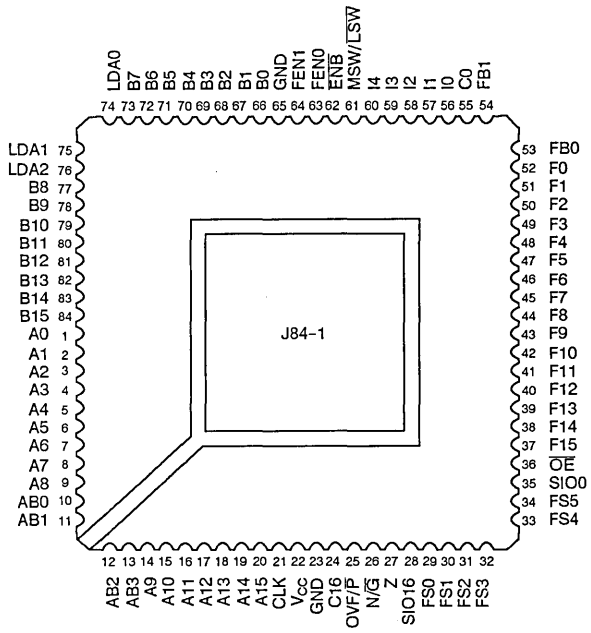
DSC-2036/-

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PLCC
TOP VIEW

FS_3	FS_1	FS_0	Z	C16	GND	A_{15}	A_{12}	A_{10}	A_9	AB_1
SIO0	FS_4	FS_2	SIO16	$\overline{OVF}/P$	A_{13}	A_{14}	A_{11}	AB_3	AB_2	A_8
$\overline{OE}$	FS_5			$N/\overline{G}$	V_{CC}	CLK			AB_0	A_7
F_{14}	F_{15}								A_6	A_5
F_{11}	F_{12}	F_{10}						A_1	A_3	A_2
F_8	F_{13}	F_9			G84-1			A_0	B_{15}	A_4
F_7	F_6	F_5						B_{12}	B_{13}	B_{14}
F_4	F_3								B_{10}	B_{11}
F_2	F_0			I_4	FEN1	GND			LDA2	B_9
F_1	FB_1	C_0	I_2	$\overline{MSW}/LSW$	FEN0	B_1	B_4	B_7	LDA1	B_8
FB_0	I_0	I_1	I_3	$\overline{ENB}$	B_2	B_0	B_3	B_5	B_6	LDA0

PIN 1 DESIGNATOR

PGA
TOP VIEW

BIT-SLICE MICROPROCESSOR DEVICES (MICROSLICE) AND MEMORY SUPPORT

MICROSLICE

Microprogrammable microprocessor building blocks offer the system designer the ultimate in system hardware and software performance and flexibility. Integrated Device Technology through architectural enhancements and high-performance, low power CEMOS technology advance bit-slice performance levels far beyond competitive components.

The IDT49C400 building block family exemplify this performance leadership, providing increased circuit density over bipolar building blocks at equivalent and faster speeds. Featured in this product family are the world's fastest 16-bit microprocessors and sequencers. Also, IDT manufactures pin-compatible CMOS 2900 products, the IDT39C00 family, which offer speed upgrades of up to 50% faster than equivalent bipolar components.

In addition to providing high performance and increased levels of integration, low power CMOS technology permits the aggressive adaptation of surface mount packages, especially 25mil center pin to pin spacing packages. The IDT49C402 is the first product available in a 25mil center 68-pin ceramic quad flatpack, with a footprint of 0.470 square inches, 53% smaller than a Pin Grid Array or a Plastic Leaded Chip Carrier (PLCC).

MEMORY SUPPORT

Error Detection and Correction (EDC) plays a major role in ensuring data integrity for large, high-speed memory arrays. IDT pioneered CMOS EDC units in 1986 with the introduction of the 39C60, 16-bit EDC, detecting errors in 20ns maximum. The industry standard IDT49C460 has established a new level for high performance EDC, with 16ns maximum detect times. And the IDT49C460 is the only 32-bit EDC cascadable to 64-bit, ideal for today's high bandwidth memory systems.

With the announcement of the Flow-thru EDC™ IDT49C465, IDT has established the next industry standard for high performance memory error detection and correction. Using a flow through architecture, memory system data correction throughput is effectively doubled in 64-bit applications.

IDT will continue to introduce speed upgrades to existing products and offer new architectural enhancements to improve system performance.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT 49C402
IDT 49C402A
IDT 49C402B

MICROSLICE™ PRODUCT

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B 55% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin plastic and ceramic PGA, Shrink-DIP (600 mil, 70 mil centers), LCC (25 and 50 mil centers) and Ceramic Quad Flatpack (25 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU and new combinations of destination functions with the RAM A port output available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64 words by 16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

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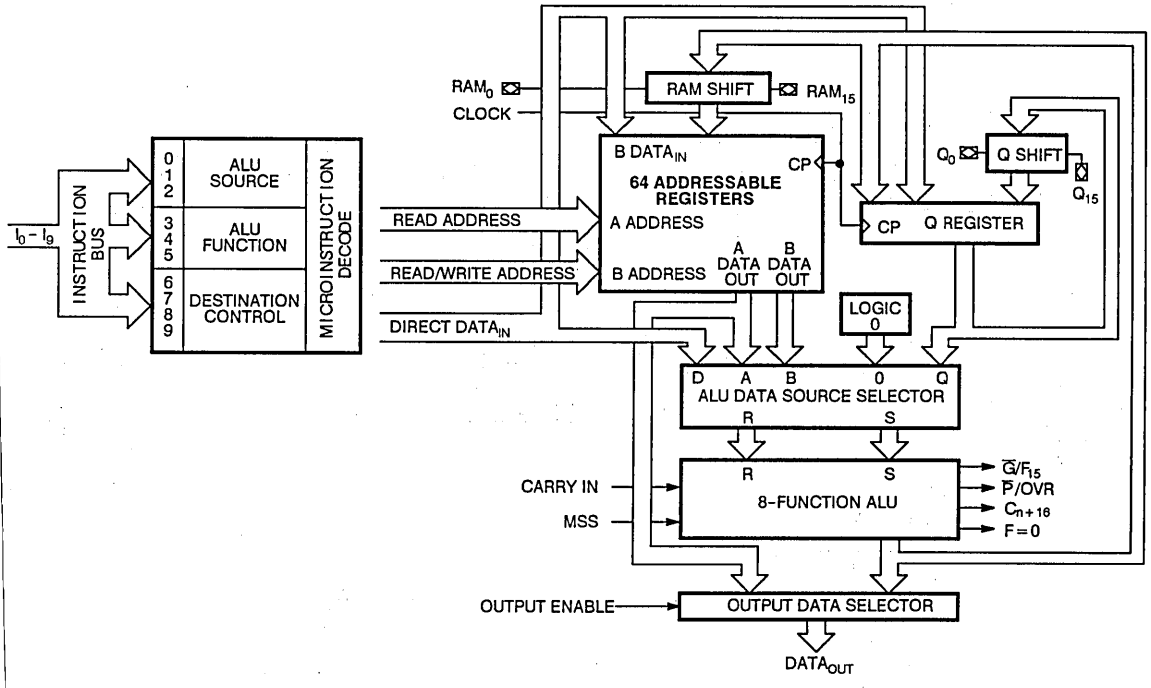
FUNCTIONAL BLOCK DIAGRAM



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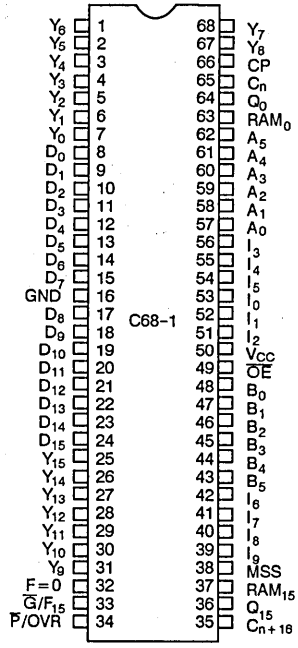
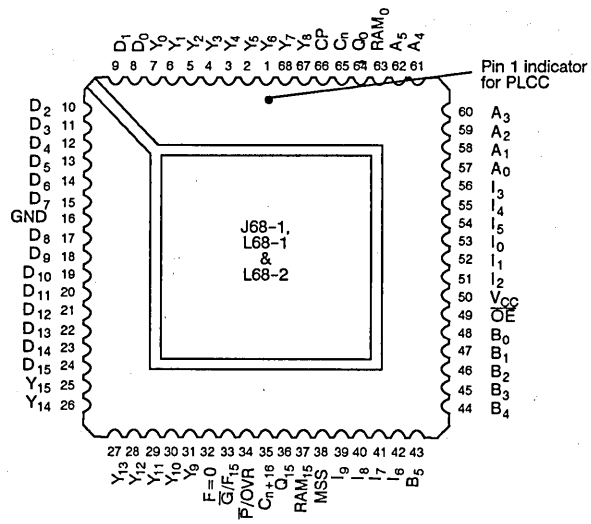
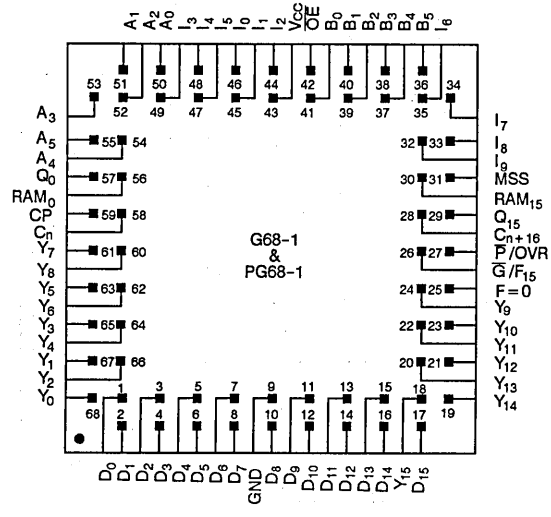
PIN CONFIGURATIONS



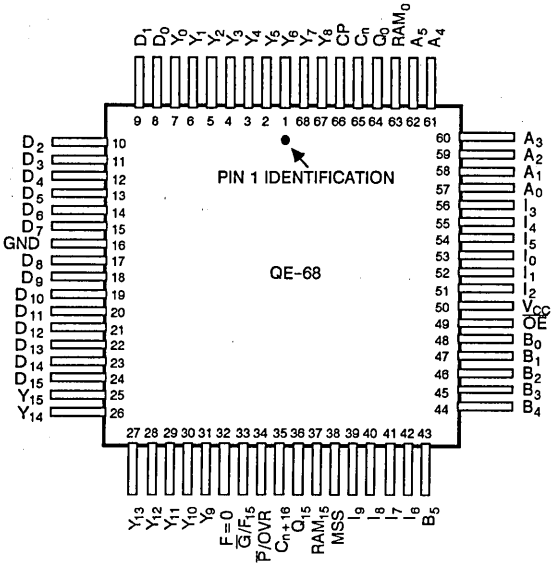
DIP
TOP VIEW



LCC/PLCC
TOP VIEW



PGA
TOP VIEW



CERQUAD
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B_0-B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0-D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0-Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15} the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0-F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice.

DEVICE ARCHITECTURE:

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the (1) register file (64 x 16 dual-port RAM) with shifter, (2) ALU and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 64 RAM registers can be read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involve the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$ or as

inputs to the RAM register file and Q Register under control of the $I_{(6, 7, 8, 9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6, 7, 8, 9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6, 7, 8, 9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5, 4, 3}$	OCTAL $I_{2, 1, 0}$	C_n = L GROUP	C_n = L FUNCTION	C_n = H GROUP	C_n = H FUNCTION
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q - 1	PASS	Q
1	3		B - 1		B
1	4		A - 1		A
2	7		D - 1		D
2	2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2	3		-B - 1		-B
2	4		-A - 1		-A
1	7		-D - 1		-D
1	0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1	1		B - A - 1		B - A
1	5		A - D - 1		A - D
1	6		Q - D - 1		Q - D
2	0		A - Q - 1		A - Q
2	1		A - B - 1		A - B
2	5		D - A - 1		D - A
2	6		D - Q - 1		D - Q

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5, 4, 3}$	OCTAL $I_{2, 1, 0}$	GROUP	FUNCTION
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX-OR	$A \veebar Q$
6	1		$A \veebar B$
6	5		$D \veebar A$
6	6		$D \veebar Q$
7	0	EX-NOR	$\overline{A \veebar Q}$
7	1		$\overline{A \veebar B}$
7	5		$\overline{D \veebar A}$
7	6		$\overline{D \veebar Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A} \wedge Q$
5	1		$\overline{A} \wedge B$
5	5		$\overline{D} \wedge A$
5	6		$\overline{D} \wedge Q$

SOURCE OPERAND AND ALU FUNCTION MATRIX [1]

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL 0	1	2	3	4	5	6	7
		ALU SOURCE							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	C_n = L R Minus S	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ⊽ Q	A ⊽ B	Q	B	A	D ⊽ A	D ⊽ Q	D
7	R EX-NOR S	$\overline{A \barwedge Q}$	$\overline{A \barwedge B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \barwedge A}$	$\overline{D \barwedge Q}$	$\overline{D}$

NOTE:
1. + = Plus; - = Minus; ∧ = AND; ⊽ = EX-OR; V = OR

ALU DESTINATION CONTROL [1]

MNEMONIC	MICROCODE I_9	I_8	I_7	I_6	HEX CODE	RAM FUNCTION SHIFT	RAM FUNCTION LOAD	Q REGISTER FUNCTION SHIFT	Q REGISTER FUNCTION LOAD	Y OUTPUT	RAM SHIFTER RAM_0	RAM SHIFTER RAM_{15}	Q SHIFTER Q_0	Q SHIFTER Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F→Q	F	X	X	X	X	Existing 2901 Functions
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F→B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F→B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	New Added IDT49C402 Functions
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

NOTE:
1. X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	-30	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H	MIL.	–	150	265	mA
			COM'L.	–	150	215	
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L	MIL.	–	80	135	mA
			COM'L.	–	80	110	
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	0.3	0.6	mA/ Input
			COM'L.	–	0.3	0.5	
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	2.0	3.0	mA/ MHz
			COM'L.	–	2.0	2.5	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	135	255	mA
			COM'L.	–	135	190	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	145	265	
			COM'L.	–	145	200	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

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IDT49C402B
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402B over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.[6]	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	23	19	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	42	49	MHz
Minimum Clock LOW Time	11	9	ns
Minimum Clock HIGH Time	11	9	ns
Minimum Clock Period	24	20	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15} OVR				C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	31	28	29	26	31	28	31	28	28	26	31	28	32	29	–	–	ns
D	26	23	23	21	23	21	25	22	22	20	26	23	24	23	–	–	ns
C_n	22	20	–	–	20	18	19	17	15	14	22	20	18	17	–	–	ns
$I_{0, 1, 2}$	28	26	24	22	28	26	27	25	23	21	28	26	26	24	–	–	ns
$I_{3, 4, 5}$	28	26	22	21	27	25	27	25	22	20	28	26	25	23	–	–	ns
$I_{6, 7, 8, 9}$	20	18	–	–	–	–	–	–	–	–	–	–	16	14	16	14	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	24	22	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	27	25	25	22	26	24	27	25	25	23	27	25	27	25	20	18	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	10	9	2[3]	1[3]	20, 9 + TPWL[4]		2	1	ns
B Destination Address	10	9	Do not change [2]				2	1	ns
D	– [1]	–	–	–	12/22 [5]	10/20 [5]	2	1	ns
C_n	–	–	–	–	16	14	0	0	ns
$I_{0, 1, 2}$	–	–	–	–	26	24	0	0	ns
$I_{3, 4, 5}$	–	–	–	–	26	24	0	0	ns
$I_{6, 7, 8, 9}$	10	9	Do not change [2]				0	0	ns
$RAM_{0, 15}$, $Q_{0, 15}$	–	–	–	–	12	10	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→ H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→ H transition, regardless of when the H → L transition occurs. TPWL is the minimum clock Low time.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design.

IDT49C402A
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.[6]	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	28	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0, 1, 2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3, 4, 5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6, 7, 8, 9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

8

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	11	10	2[3]	1[3]	21, 10 + TPWL[4]		2	1	ns
B Destination Address	11	10	Do not change[2]				2	1	ns
D	–[1]	–	–	–	12/22[5]	10/20[5]	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0, 1, 2}$	–	–	–	–	28	25	0	0	ns
$I_{3, 4, 5}$	–	–	–	–	28	25	0	0	ns
$I_{6, 7, 8, 9}$	11	10	Do not change[2]				0	0	ns
$RAM_{0, 15}$, $Q_{0, 15}$	–	–	–	–	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→ H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design.

IDT49C402
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.[6]	COM'L.	UNIT
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS[1] C_L = 50pF

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0, 1, 2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3, 4, 5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6, 7, 8, 9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Source Address	20	18	2[3]	1[3]	50, 20 + TPWL[4]		2	1	ns
B Destination Address	20	18	Do not change [2]				2	1	ns
D	– [1]	–	–	–	30/40 [5]	26/36 [5]	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0, 1, 2}$	–	–	–	–	45	41	0	0	ns
$I_{3, 4, 5}$	–	–	–	–	45	41	0	0	ns
$I_{6, 7, 8, 9}$	12	11	Do not change [2]				0	0	ns
$RAM_{0, 15}$, $Q_{0, 15}$	–	–	–	–	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→ H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→ H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design.

IDT49C402B
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	20	18	18	16

IDT49C402A
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	22	20	20	18

IDT49C402
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

TEST LOAD CIRCUIT

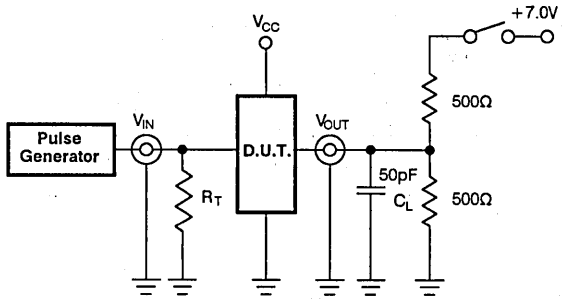


Figure 1. Switching Test Circuit (All Outputs)

INPUT/OUTPUT INTERFACE CIRCUIT

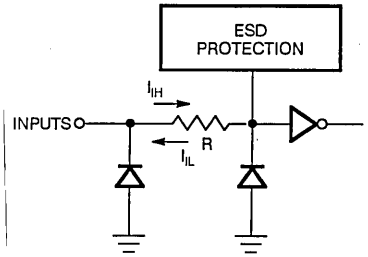


Figure 2. Input Structure (All Inputs)

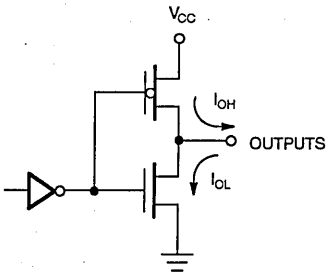


Figure 3. Output Structure (All Outputs Except F = 0)

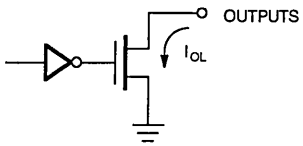


Figure 4. Output Structure (F = 0)

CRITICAL SPEED PATH ANALYSIS

Critical speed paths are for the IDT49C402A versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402A operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

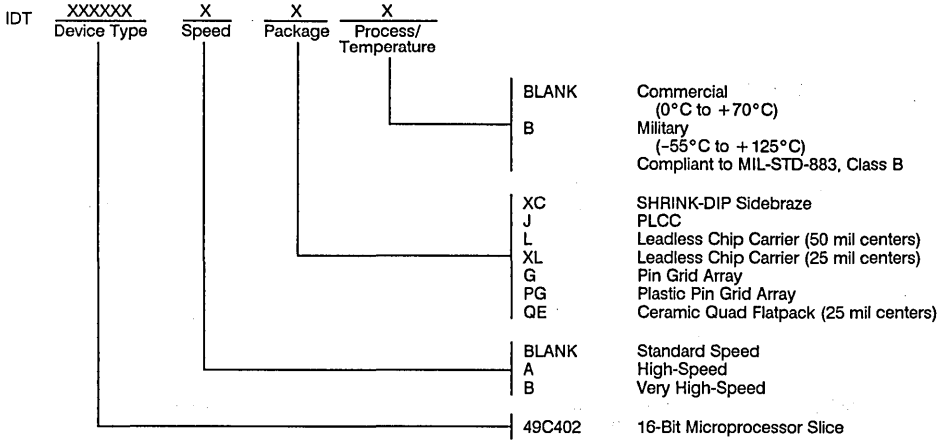
TIMING COMPARISON: IDT49C402A vs 2901C w/2902A

16-BIT µP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNIT
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥71	≥71	≥83.5	≥83.5	ns
IDT49C402A	37	36	41	40	ns
Speed Savings	34	35	42.5	43.5	ns

TIMING COMPARISON: IDT49C402 vs 2901C w/2902A

16-BIT µP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNIT
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥71	≥71	≥83.5	≥83.5	ns
IDT49C402	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT 49C403
IDT 49C403A

FEATURES:

- Monolithic 16-bit CMOS μP Slice
- Replaces four 2903As/29203s and a 2902A
- Fast
  - 50% faster than four 2903As/29203s and a 2902
- Low power CMOS
  - Commercial: 250mA (max.)
  - Military: 275mA (max.)
- Performs binary and BCD Arithmetic
- Expanded two-address architecture with independent, simultaneous access to two, expandable 64 x 16 register files
- Word/Byte Control
- Expanded 4 x 16 Q Register
- Performs Byte Swap and Word/Byte Operation
- Fully cascadable without the need for additional carry lookahead
- Incorporates three 16-bit Bidirectional Busses
- Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and Writes to Register File
- High Output Drive
  - Commercial: 16mA (max.)
  - Military: 12mA (max.)
- Available in 108-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C403 is a high-speed, fully cascadable 16-bit CMOS microprocessor slice. It combines the standard function of four 2903s/29203s and one 2902 with additional control features aimed at enhancing the performance of all bit-slice microprocessor designs.

Included in this extremely low power, yet fast IDT49C403 device are 3 bidirectional data buses, 64 word x 16-bit two-port expandable RAM, 4 word x 16-bit Q Register, parity generation, sign extension, multiplication/division and normalization logic. Additionally, the IDT49C403 offers the special feature of enhanced byte support through both word/byte control and byte swap control.

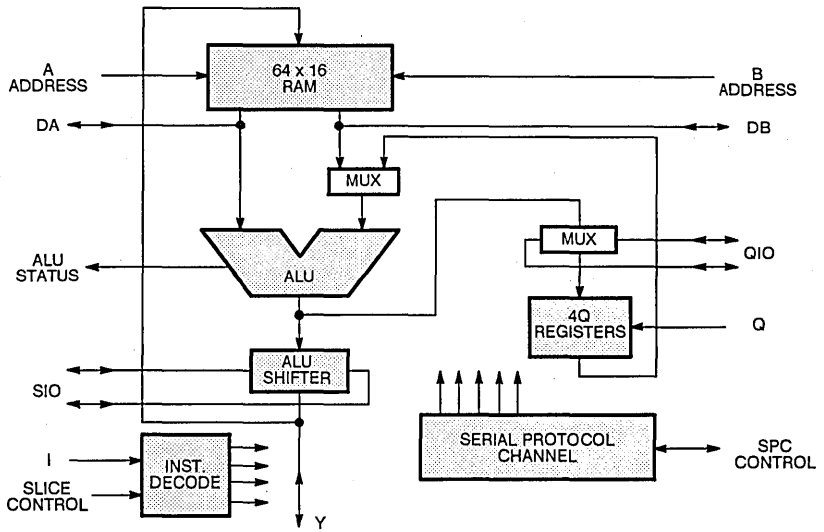
The IDT49C403 easily supports fast 100ns microcycles and will enhance the speed of all existing quad 2903A/29203 systems by 50%. Being specified at an extremely low 250mA, the IDT device offers an immediate system power savings and improved reliability.

Also featured on the IDT49C403 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

8

FUNCTIONAL BLOCK DIAGRAM



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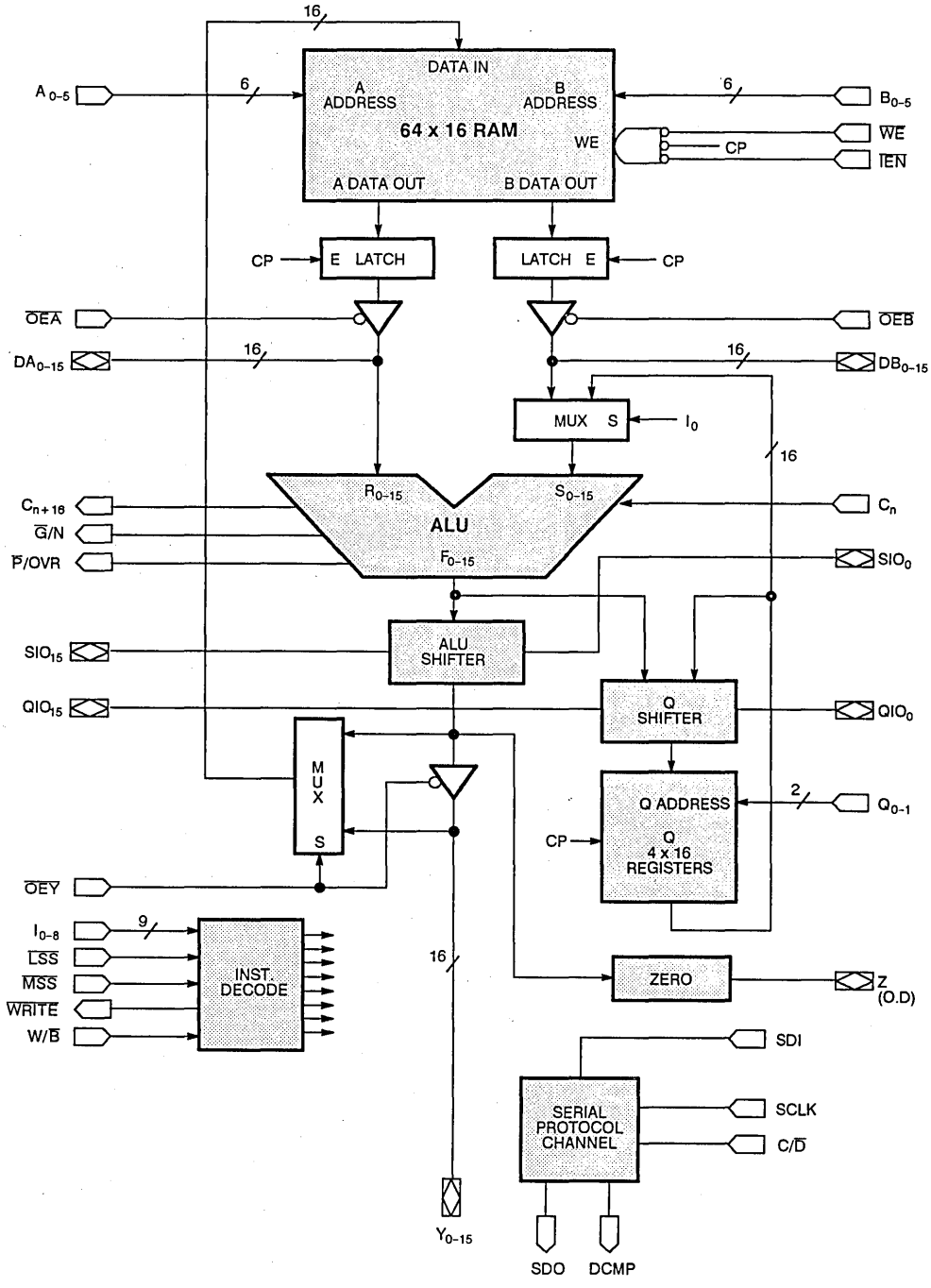
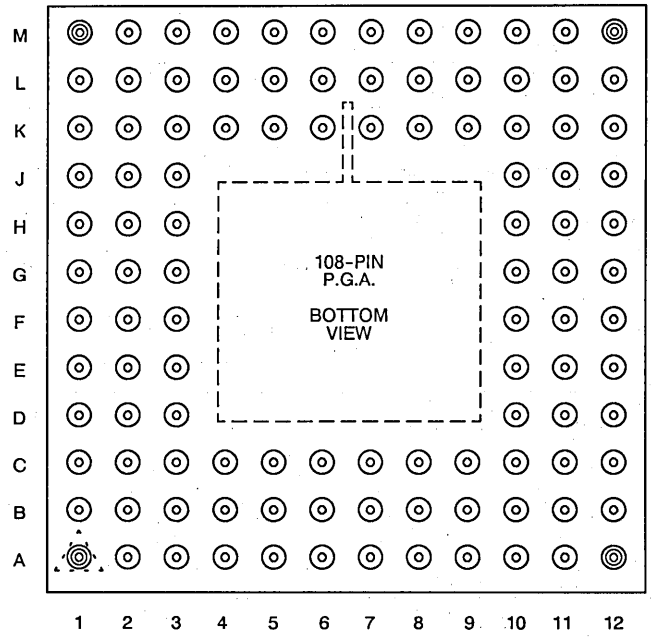
DETAILED BLOCK DIAGRAM



PIN CONFIGURATION



PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
A1	N/C	B4	DB7	C7	DCMP	E10	$\overline{W}/B$	H1	DA2	K4	DA8	L7	$\overline{WE}$	M10	Q_0
A2	V_{CC}	B5	DB4	C8	I_5	E11	$\overline{OEY}$	H2	DA3	K5	DA12	L8	B_2	M11	V_{CC}
A3	$\overline{OEB}$	B6	DB1	C9	$\overline{IEN}$	E12	SIO_0	H3	DA5	K6	N/C	L9	B_5	M12	N/C
A4	DB5	B7	$\overline{MSS}$	C10	Y_2	F1	GND	H10	Y_{13}	K7	B_0	L10	Q_1		
A5	DB3	B8	I_7	C11	Y_5	F2	DB15	H11	Y_{11}	K8	B_4	L11	SCLK		
A6	DB0	B9	C_{n+16}	C12	Y_6	F3	DB14	H12	Y_{10}	K9	$\overline{WRITE}$	L12	$C/\overline{D}$		
A7	GND	B10	$\overline{P}$/OVR	D1	DB11	F10	QIO_0	J1	DA4	K10	GND	M1	V_{CC}		
A8	I_8	B11	Y_1	D2	DB9	F11	SIO_{15}	J2	DA6	K11	SDO	M2	A_5		
A9	I_6	B12	Y_3	D3	I_3	F12	QIO_{15}	J3	A_1	K12	Y_{15}	M3	DA10		
A10	$\overline{G}$/N	C1	DB8	D10	Y_4	G1	$\overline{OEA}$	J10	SDI	L1	A_2	M4	DA13		
A11	Y_0	C2	I_4	D11	Y_7	G2	DA0	J11	Y_{14}	L2	A_4	M5	DA15		
A12	V_{CC}	C3	GND	D12	Z	G3	DA1	J12	Y_{12}	L3	DA9	M6	GND		
B1	I_2	C4	I_0	E1	DB13	G10	Y_9	K1	DA7	L4	DA11	M7	CP		
B2	I_1	C5	DB6	E2	DB12	G11	Y_8	K2	A_0	L5	DA14	M8	B_1		
B3	C_n	C6	DB2	E3	DB10	G12	GND	K3	A_3	L6	$\overline{LSS}$	M9	B_3		

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A_{0-5}	I	Six address inputs to the RAM containing the address of the RAM word appearing at output port A.
B_{0-5}	I	Six address inputs to the RAM which selects one of the words in the RAM, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the $\overline{WE}$ input and CP input are low.
DA_{0-15}	I/O	Sixteen bi-directional data pins acting as operands R for entering external data into the ALU. DA_0 is the LSB. The DA lines also function as an external output for RAM port A.
DB_{0-15}	I/O	Sixteen bi-directional data pins for entering external data into the ALU. The DB lines act as either RAM port B output data, or as input operands S to the ALU.
$\overline{WE}$	I	The RAM write enable input, which when LOW causes the Y I/O port data to be written into the RAM when the CP input is low. When $\overline{WE}$ is HIGH writing data into the RAM is inhibited.
$\overline{OEA}$	I	Output enable, which, when HIGH selects DA_{0-15} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-15} output data.
$\overline{OEB}$	I	Output enable, which, when HIGH selects DB_{0-15} as the ALU S operand, and, when LOW, selects RAM output B as the ALU S operand and the DB_{0-15} output data.
SIO_0 SIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. SIO_0 is an input and SIO_{15} is an output during a shift-up operation. SIO_{15} is an input and SIO_0 is an output during a shift-down operation. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
QIO_0 QIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the Q registers shifter. They operate like SIO_0 and SIO_{15} pins. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
C_n	I	Carry-in input to the ALU.
$\overline{IEN}$	I	Instruction enable input. When LOW, it enables writing into the Q register and the Sign Compare flip-flop. When HIGH, the Q register and the Sign Compare flip-flop are in hold mode. $\overline{IEN}$ does not affect $\overline{WRITE}$, but internally disables the RAM write enable.
$\overline{LSS}$	I	Input pin, when held LOW, causes the chip to act as either stand alone slice (SA) or the least significant slice (LSS), When $\overline{LSS}$ is held HIGH, the chip acts as either an intermediate slice or most significant slice.
$\overline{MSS}$	I	Input pin, when held LOW, programs the chip to act as either stand alone slice (SA) or the most significant slice (MSS), and holding it HIGH programs the chip to act either as an intermediate slice (IS) or the least significant slice (LSS).
$\overline{WRITE}$	O	The $\overline{WRITE}$ signal is LOW when an instruction which causes data to be written into the RAM is being executed. This pin is normally connected to the $\overline{WE}$ pin.
C_{n+16}	O	This output indicates the carry out of the ALU. Refer to Tables 6a and 6b for an exact definition of this pin.
Z	I/O	An open drain bidirectional pin. When HIGH it indicates that all outputs are LOW. Z is used as an input pin for some special functions. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{G}$/N	O	$\overline{G}$ indicates the carry generate function at the least significant and intermediate slices, and indicates the sign, N, of the ALU result at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{OEY}$	I	A control input pin. When LOW the ALU shifter output data is enabled onto the Y_{0-15} lines. When HIGH the Y_{0-15} three-state output buffers are disabled.
CP	I	Clock input. The Sign Compare flip-flop and the Q register are clocked on the LOW-to-HIGH transition of the CP signal. When $\overline{WE}$ and CP are LOW, data is written into the RAM.
$\overline{P}$/OVR	O	$\overline{P}$ indicates the carry propagate function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
Y_{0-15}	I/O	Sixteen bi-directional data pins. Controlled by $\overline{OEY}$ input, the ALU shifter output data can be enabled onto these lines, or external data is written directly into the RAM using these lines as data inputs.
I_{0-8}	I	The nine instruction inputs used to select the IDT49C403 operation to be performed.
Q_{0-1}	I	Two address pins to select one of the four Q registers.
W/$\overline{B}$	I	Word/$\overline{Byte}$ control pin. Used only in the standard function mode, it selects Word mode when held HIGH and Byte mode when held LOW. Must be tied HIGH when the special functions are being used.
SDI	I	Serial Data Input pin, used for receiving diagnostic data and commands from a host system or from the SDO pin of a cascaded processor.
SDO	O	Serial Data Output pin, used for transmitting diagnostic data and commands to a host system or a cascaded processor via its SDI pin.
C/$\overline{D}$	I	Input pin, when LOW defines the bit pattern being received at the SDI pin as Data, and when HIGH defines the incoming pattern as a Command for executing diagnostic functions. This pin should be tied HIGH when the diagnostics feature is not being used.
SCLK	I	Input pin used for clocking in diagnostic data and command information at the SDI pin. This pin should be tied LOW when the diagnostics function is not being used.
DCMP	O	Output pin, which, when HIGH indicates that the internal comparison between the Y or Q bus data and the data from the diagnostics data register resulted in a TRUE (they were equal). This feature is used for breakpoint detection. It is an open-drain pin and can be wire AND with other DCMP pins.

DEVICE ARCHITECTURE

The IDT49C403 CMOS microprocessor slice is configured sixteen bits wide and is cascadable to any number of bits (32, 48, 64, etc.). Key elements which make up this sixteen-bit microprocessor slice are: (1) the RAM file (a 64 x 16 dual-port RAM) with latches on both outputs. (2) a high-performance ALU with shifter, (3) a flexible Q register file (4 x 16 bits) with shifter input, (4) a nine-bit instruction decoder, and (5) Serial Protocol Channel.

The IDT49C403 incorporates Serial Protocol Channel (SPC™). For system testing and debugging purposes SPC is a method by which data can be entered into and extracted from a device through a serial data input output, thus providing access to all internal registers.

REGISTER FILE

The Register File is composed of 64 x 16 bit RAM locations. The RAM data is read from the A-port as controlled by the 6-bit A address field input. Simultaneously, data can be read from the B port as defined by the 6-bit B address field input. If the same address is applied at both the A input field and the B input field, identical data will appear at the two respective output ports. Data is written into the RAM when $\overline{WE}$, $\overline{IEN}$ and the clock CP are LOW. Both the RAM output data latches are transparent while CP is HIGH and latch the data when CP is LOW. The three-state output enable $\overline{OEB}$ allows RAM B port data to be read at the DB I/O port, while $\overline{OEA}$ performs the same function for the A port data at the DA I/O port.

New data is written into the RAM word defined by the B address field. External data at the Y I/O port can be written directly into the RAM, or the ALU shifter output data can be enabled onto the Y I/O port and written into the RAM.

ALU

The ALU can perform seven arithmetic and nine logic operations on the two 16-bit input words S and R. Multiplexers at the ALU inputs allow selection of various pairs of ALU source operands. The $\overline{OEA}$ input selects either external DA data or RAM A port output data as the 16-bit R source operand. The $\overline{OEB}$ and I_0 inputs provide selection of either RAM B port output, external DB data or the Q register file output as the 16-bit S source operand. Also, during certain ALU operations, zeroes are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an external and an internal source, or from two internal sources. Table 1 shows all possible pairs of source operands as selected by $\overline{OEA}$, $\overline{OEB}$, and I_0 inputs.

Table 1. ALU Operand Sources(1)

$\overline{OEA}$	I_0	$\overline{OEB}$	ALU OPERAND R	ALU OPERAND S
L	L	L	Ram Output A	Ram Output B
L	L	H	Ram Output A	DB_{0-15}
L	H	X	Ram Output A	Q Register
H	L	L	DA_{0-15}	Ram Output B
H	L	H	DA_{0-15}	DB_{0-15}
H	H	X	DA_{0-15}	Q Register

NOTE:
1. L = LOW, H = HIGH, X = DON'T CARE

The ALU performs special functions when instruction bits I_3, I_2, I_1, and I_0 are LOW. Table 5 defines these special functions and the operation which the ALU performs for each instruction. When the ALU executes instructions other than the special functions, the operation is defined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the operation as a function of these four instruction bits.

Table 2. IDT49C403 ALU Functions(1)

I_4	I_3	I_2	I_1	I_0	ALU FUNCTIONS
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	$F = S-R-1+C_n$
L	L	H	L	X	$F = R-S-1+C_n$
L	L	H	H	X	$F = R+S+C_n$
L	H	L	L	X	$F = S+C_n$
L	H	L	H	X	$F = \overline{S}+C_n$
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	$F = R+C_n$
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	$F = \overline{R}+C_n$
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = \overline{R}$ AND S
H	L	H	L	X	$F_i = R_i$ EXCLUSIVE NOR S_i
H	L	H	H	X	$F_i = R_i$ EXCLUSIVE OR S_i
H	H	L	L	X	$F_i = R_i$ AND S_i
H	H	L	H	X	$F_i = R_i$ NOR S_i
H	H	H	L	X	$F_i = R_i$ NAND S_i
H	H	H	H	X	$F_i = R_i$ OR S_i

NOTE:
1. L = LOW, H = HIGH, i = 0 to 15, X = Don't Care

The IDT49C403 may be cascaded in either a ripple carry or carry lookahead fashion. When configured as cascaded ALUs, the IDT49C403s must be programmed to be a most significant slice (MSS), an intermediate slice (IS), or a least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals that are necessary in a cascaded system are available as outputs on the IDT49C403 least significant and intermediate slices.

The IDT49C403 provides a carry-out signal C_{n+16} which is available as an output of each slice. The carry-in, C_n, and carry-out, C_{n+16}, are both active HIGH. Two other status outputs are generated by the ALU. These are the negative, N, and the overflow, OVR. The N output indicates positive or negative results, while the OVR output indicates that the arithmetic operation performed exceeded the available two's complement range. Thus the pins $\overline{G}$/N and $\overline{P}$/OVR indicate carry generate or propagate on the least significant and intermediate slice, and sign and overflow on the most significant slice.

Refer to Tables 6a and 6b for an exact definition of these four signals.

ALU DESTINATION CONTROL

The following tables show how the shifter at the output of the ALU should function for non-special instructions. The main addition with respect to the IDT39C203 is the built in byte capability.

The 49C403 has two write enables internally. One for the upper byte and one for the lower byte. The enables are controlled by the instruction decode, external $\overline{WE}$ and the W/$\overline{B}$ input. For convenience to the user, the unused bits on the Y bus (MSB, ..., 8) are zero during byte operation. The $\overline{WE}$ input must be directly connected to the WRITE output, or indirectly through some amount of gating (i.e., expansion RAM decoding gates).

8

The sign extend function is an exception to the rule with regard to the internal byte write enables. When executed, all of the write enables are active, irrespective of W/$\overline{B}$. In the SA and LSS slices, the contents of bit 7 is replicated on bits 8 to 15 and SIO_{15} in the byte mode. In the word mode bit 15 is placed on SIO_{15}. In this way an 8-bit word (byte) or a 16-bit word can be extended to the entire width of the native data path. Extends of larger words than these, such as 24 and 32 bits, can be achieved by steering the $\overline{MSS}$ and $\overline{LSS}$ inputs of the IS slices to inform which device has the sign bit to extend. As Sign Extend requires internal gating of the write enables to the upper and lower portions of RAM, the instruction will not work with locations in memory expansion RAM.

ALU SHIFTER

The ALU shifter shifts the ALU output data under instruction control. It can shift up one bit position (2F), shift down one bit position (F/2), or pass the ALU output non-shifted (F). An arithmetic shift operation shifts the data around the most significant (Sign) bit of the most significant slice and a logical shift operation shifts the data through the most significant bit. Figure 1 shows these shift patterns. The SIO_0 and SIO_{15} are bidirectional serial shift input/output pins. During a shift-up operation, SIO_0 is generally an input while SIO_{15} is an output, whereas during a shift-down operation SIO_0 is generally an output while SIO_{15} acts as an input. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.

The ALU shifter also provides sign extension and parity generating/checking capabilities. Under instruction control, the SIO_0 (Sign) input can be extended through $Y_0, Y_1, Y_2, ...Y_{15}$ and propagated to the SIO_{15} output. A cascadable, five-bit parity generator/checking generates parity for the $F_0, F_1, F_2, ...F_{15}$ ALU outputs and SIO_{15} input and, under instruction control, is made available at the SIO_0 output.

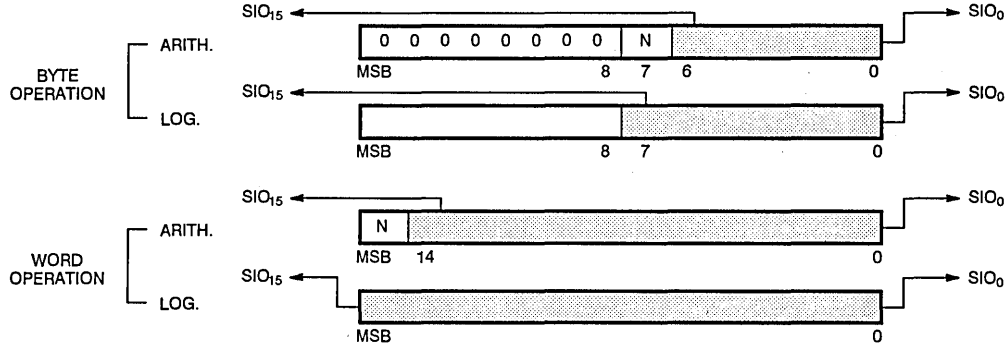


Figure 1. IDT49C403 Arithmetic and Logical Shift Operations

Table 5 defines the special functions and the operation the ALU shifter performs for each instruction. For instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, and I_5. Table 4 (a, b, c, d) defines the ALU shifter operation as a function of these four bits.

WORD/BYTE CONTROL AND BYTE SWAP

In addition to the special ALU functions, the IDT49C403 also provides a Word and Byte control and Byte Swap features.

The W/$\overline{B}$ pin at the Instruction Decoder input selects ALU operation on either a Word or a Byte. When W/$\overline{B}$ is HIGH, the ALU operates on a Word and, when W/$\overline{B}$ is LOW, the ALU operates on a Byte. Table 4 (a, b, c, d) shows the ALU Destination Controls for Word and Byte operations for each instruction mode.

The Byte Swap special function allows the positions of the Upper and Lower bytes to be swapped before entering them as the ALU S operand. The ALU function then adds C_n to this swapped word as its F output. Table 5 shows the instruction set that allows the ALU to operate the Byte Swap feature.

Q REGISTER FILE

The Q register is a separate 4-word by 16-bit file intended primarily for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. The ALU output, F, can be loaded into the Q register and/or the Q register output can be selected as one of the ALU S operands. The shifter at the input to the Q register performs only logical shifts. It can shift-up the data one bit position (2Q) or down one bit position (Q/2). For a shift-up operation, QIO_0 acts as an input while QIO_{15} acts as an output; whereas, for a shift-down operation, QIO_0 is an output and QIO_{15} is an input. By connecting QIO_{15} of the most significant slice to SIO_0 of the least significant slice, double-length arithmetic and logical shifting is possible with cascaded IDT49C403s.

The Q_0 and Q_1 inputs enable selection of any one of the four 16-bit Q register files. Once a specific Q register has been selected, access to the other three Q registers is disabled and can be gained only after changing Q_0 and Q_1 levels to enable a different Q register.

Table 5 defines the special functions and the operations which the Q register and shifter perform for selected instruction inputs. While executing instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5. Table 4 (a, b, c, d) defines the Q register and shifter operation as a function of these four bits.

INSTRUCTION DECODER

The internal control signals necessary for the operation of the IDT49C403 are generated by the instruction decoder as a function of the nine instruction inputs, I_{0-8}; the instruction enable input, $\overline{IEN}$; the $\overline{LSS}$ input; the $\overline{MSS}$ input; the W/$\overline{B}$ input and the $\overline{WRITE}$ output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is executed. Refer to Tables 4 (a, b, c, d) and 5 for

a definition of the $\overline{WRITE}$ output as a function of the instruction inputs.

When $\overline{IEN}$ is HIGH, the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q register and Sign Compare Flip-Flop can be written according to the IDT49C403 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

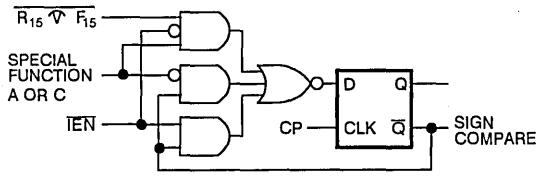


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

The IDT49C403 can be programmed to operate in either a cascaded application or in the standalone mode. Table 3 shows its four programmed modes.

Table 3. SLICE Programming

SLICE PROGRAM INPUTS		MODE OF OPERATION
$\overline{MSS}$	$\overline{LSS}$	
LOW	LOW	Stand Alone Slice (SA)
LOW	HIGH	Most Significant Slice (MSS)
HIGH	HIGH	Intermediate Slice (IS)
HIGH	LOW	Least Significant Slice (LSS)

SPECIAL FUNCTIONS

Seventeen special functions are provided on the IDT49C403 which permit the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD Add, Subtract, and Divide by Two
- Single and Double-precision BCD-to Binary and Binary-to-BCD Conversion
- Byte Swap

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations.

Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers respectively, in 'n' clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction rather than addition is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude—two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

In addition to BCD arithmetic special functions to add or subtract two BCD numbers, a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions permit single and double-precision algorithms to convert from BCD-to-Binary and from Binary-to-BCD.

The Byte Swap feature allows the swapping of Lower and Upper bytes of a word before presenting them as the ALU S operand. The ALU then adds the carry C_n to this swapped word to form its F output. This feature functions only for the ALU S operand.

SERIAL DIAGNOSTICS

The Serial Protocol Channel™ (SPC) is a flexible on-chip feature of the IDT49C403 and is a set of pins by which data can be entered into and extracted from a device through a serial data input and output port.

SPC can be used at many points in the life of a product for diagnostic purposes such as system level design debug and development; system test during manufacturing and field maintenance debug and test. It allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system. Serial diagnostics is primarily a scheme utilizing only four pins to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults.

Detailed SPC Architecture of the IDT49C403 Bit-Slice Microprocessor

The IDT49C403, a quad Am2903/29203 16-bit microprocessor slice, which includes an ALU and register file, is one of the devices on which IDT has incorporated the Serial Protocol Channel. The implementation of SPC on the IDT49C403 is shown in Figure 3.

Only four SPC pins (SDI, SDO, SCLK and C/$\overline{D}$) are used to serially access the I/O pad cells, as well as the internal ALU registers and buses. To control or monitor a section (such as the ALU), the appropriate command is loaded into the SPC command register. The desired function is then executed and the status information captured in the data register. The status information can then be serially shifted out and observed to verify proper system functionality.

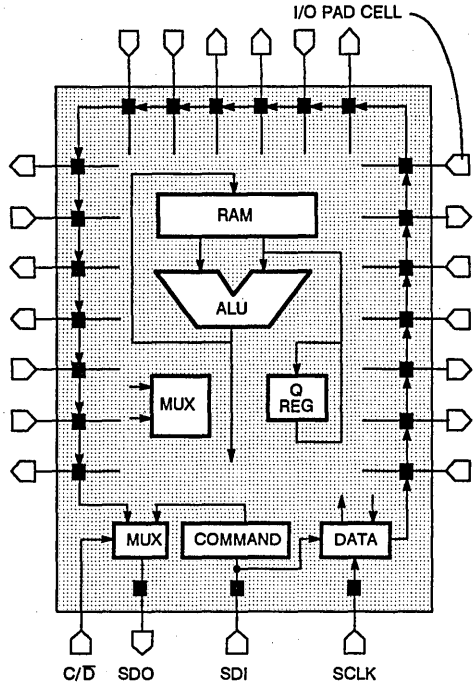


Figure 3. Conceptual Diagram of IDT49C403 Die Incorporating SPC Scan Path

The block diagram in Figure 4 shows the detailed SPC architecture for the IDT49C403. It primarily consists of serial registers for command, data, addresses and decode/control logic. The SPC command register consists of a four-bit field (signals 4-7) and four discrete control lines (signals 3, 2, 1, 0). The four-bit field coordinates the transfer of data between RAM and the SPC data register, as well as controls an on-chip break detect mechanism. The other discrete signals control the serial scan path through the I/O cells.

The SPC data register is in series with a RAM address register and I/O pad scan. The SPC data register is connected to the internal bus to gain access to the RAM register file as well as a data break point feature. The point of connection is the Y bus from the ALU back into the RAM.

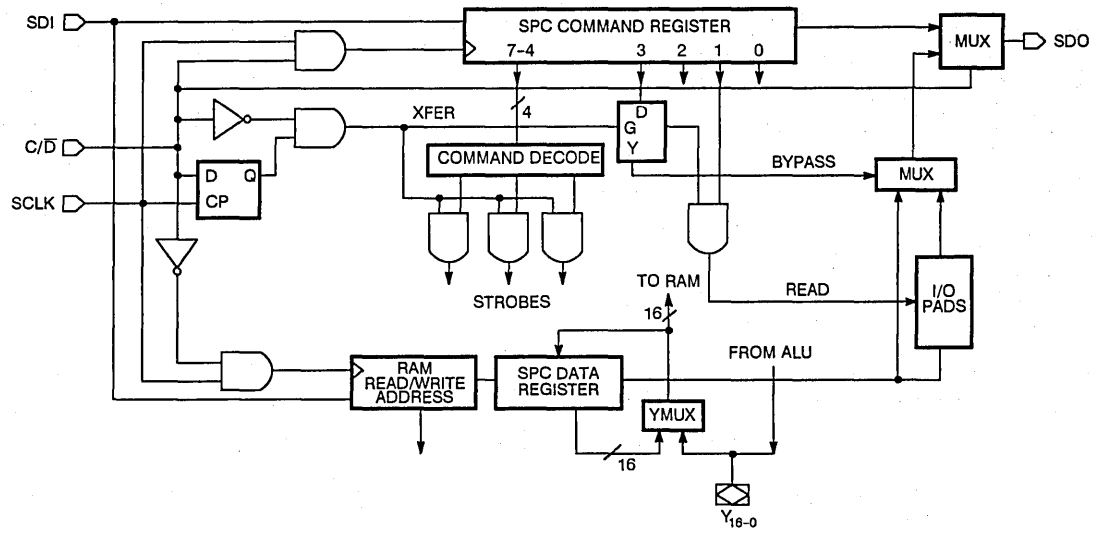


Figure 4. Internal Organization of the SPC

The multiplexer at the output transmits information via the SDO pin selecting data from either the SPC data register and the I/O pads or the command string from the SPC command register.

IDT49C403 SPC Command Opcodes

The SPC command register consists of an 8-bit field, as shown in Figure 5. Bit 1 enables the READ function of the I/O pad cells. Bit 3 enables the BYPASS function to bypass the I/O pad cells and scan out only the RAM address and data registers. Bits 0 and 2 are reserved. Bits 4 through 7 form the opcode field for reading and writing into the device.

The 4-bit command opcode field gives 16 possible command opcodes. The first 8 are reserved for writing data from the SPC data register into the registers and RAM on the device. The second 8 opcodes are reserved for reading data from registers and RAM into the 16-bit SPC data register.

COMMAND OPCODES	
OPCODE	**FUNCTION**
0	Write RAM
1	Write Q Registers
2	Write Break Control
3	Write Break Data
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Read RAM
9	Read Q Registers
10	Read Break Control
11	Read Break Data
12	View Y
13	Reserved
14	Reserved
15	NOP

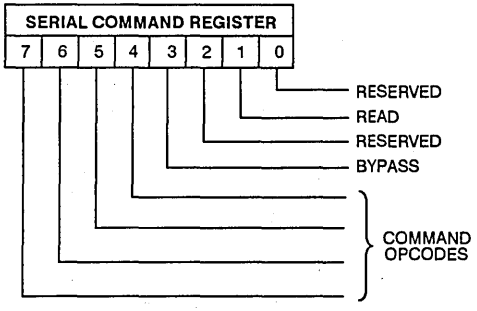


Figure 5. SPC Command Register and Opcodes for the IDT49C403

The command with opcode 0 causes a write to the internal device RAM. Opcode 1 is used to write to the Q registers. Opcodes 2 and 3 are used to write data from SPC data register into the break data register and break control registers, respectively. Opcodes 4 through 7 are reserved opcodes.

Opcode 8 is used for reading RAM data into the SPC data register. Opcode 9 is used to read a value out of the Q registers. (Here, also, the address register supplies the address of the Q register to be accessed). Opcodes 10 and 11 are used for reading the break control register and the break data register, respectively. Opcode 12 is used to strobe data from the Z bus into the 16-bit diagnostics data register. Opcodes 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes, if executed, perform a no-operation; however, they should not be relied upon to always perform NOPs as future upgrades may make use of reserved opcodes.

Accessing the Contents of the IDT49C403 Register File

To read data from the device's internal RAM or other logic circuitry into the SPC data register, the address and don't care bits (for the SPC data register) are shifted in. The command is shifted into the SPC command register. The command register must be decoded to determine what data paths are to be steered in order to get data into the SPC data register. The read strobe, generated by the strobe logic, must then strobe this data (in parallel) into the SPC data register. The data can now be shifted out via the SDO pin and its contents disassembled and observed.

To perform the write operation, address and data must first be shifted into the SPC data register. The command is then shifted into the SPC command register via the command mode. This register provides information as to what data paths are to be steered. The address is supplied by the address register in the data scan path. The write strobe is then generated between the time the C/$\overline{D}$ line is lowered and the SCLK line is raised. This is the strobe which actually clocks the data into the RAM or register in the device.

Pad Cell Scan Path

Each I/O cell on the IDT49C403 contains a flip-flop which can be used to store the state of that cell and then be scanned out. Figure 6 shows the logic configuration. The READ line is enabled by a bit in the SPC command register and gated by the XFER signal, thus loading the scan flip-flops in parallel. The SCLK is then used to scan the data out of the SDO pin in series with the address and SPC data registers.

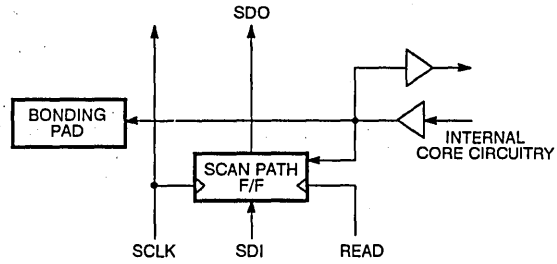


Figure 6. Serial Scan in the I/O Cell

The BYPASS bit in the SPC command register selects whether the shifting of the I/O cells will be bypassed such that only the RAM address and data registers are scanned out. When the READ bit is HIGH, data is transferred from the pins to the scan register when SCLK transitions HIGH after C/D has transitioned LOW. The BYPASS bit in the command register is active HIGH so that a HIGH level bypasses scanning the I/O cells.

Figure 7 shows the order in which the I/O pad cells are scanned. The clocking will shift out the data on the Y_{15} pin first and continue in series until the WRITE pin is shifted out last.

0	Y15
1	Y14
2	Y13
3	Y12
4	Y11
5	Y10
6	Y9
7	Y8
8	QIO15
9	SIO15
10	QIO0
11	SIO0
12	$\overline{OEY}$
13	Z
14	W/$\overline{B}$
15	Y7
16	Y6
17	Y5
18	Y4
19	Y3
20	Y2
21	Y1
22	Y0
23	$\overline{IEN}$
24	P/$\overline{N}$

25	G/$\overline{N}$
26	CN16
27	15
28	16
29	17
30	18
31	DCMP
32	$\overline{MSS}$
33	DB0
34	DB1
35	DB2
36	DB3
37	DB4
38	DB5
39	DB6
40	DB7
41	$\overline{OEB}$
42	CN
43	I0
44	I1
45	I2
46	I3
47	I4
48	DB8
49	DB9

50	DB10
51	DB11
52	DB12
53	DB13
54	DB14
55	DB15
56	$\overline{OEA}$
57	DA0
58	DA1
59	DA2
60	DA3
61	DA4
62	DA5
63	DA6
64	DA7
65	A0
66	A1
67	A2
68	A3
69	A4
70	A5
71	DA8
72	DA9
73	DA10
74	DA11

75	DA12
76	DA13
77	DA14
78	DA15
79	$\overline{LSS}$
80	CP
81	$\overline{WE}$
82	B0
83	B1
84	B2
85	B3
86	B4
87	B5
88	Q0
89	Q1
90	$\overline{WRITE}$

Figure 7. Shift Order of I/O Pad Cells

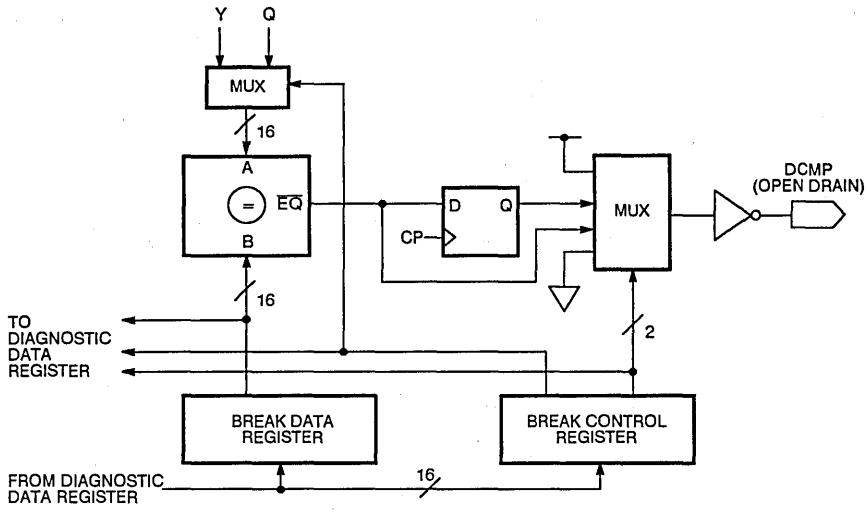


Figure 8. Breakpoint Detect Circuitry

Breakpoint Detection on the IDT49C403

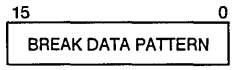
Figure 8 shows the diagnostics breakpoint detection circuit on the IDT49C403. This circuit is designed to allow the user to monitor certain key data buses and detect the data patterns on the Y and Q buses. When a data pattern is detected, a breakpoint compare signal is generated on the DCMP pin and is used to halt the system operation. The DCMP is an open drain signal and should be wire-ORed with DCMP lines of other similar devices and monitored by the main sequencer in the system. The breakpoint detection mechanism thus allows for an easier debug of microcode with regard to the data path.

At the heart of the breakpoint detection circuit is a comparator which compares data from the break data register with data from either the Y bus or the Q bus. The break control register determines which of the two buses is selected for a comparison. The break control register also steers a multiplexer at the output of the comparator. This multiplexer selects between the equal-to signal, latched equal-to, V_{CC} or GND. The latched equal-to input into the multiplexer gives the user the ability to pipeline the match signal, thus shortening the system cycle time in the diagnostics mode. The V_{CC} and GND inputs to the multiplexer allow the programmer to disable the break compare feature by forcing the DCMP pin either LOW or HIGH, respectively.

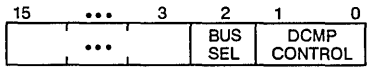
When a match is made, the DCMP line goes HIGH. Thus, if any one slice in a cascade application does not match, the wire-ANDed DCMP will be low. Selecting V_{CC} via the multiplexer will disable matches altogether. To select GND, disable any one slice from the comparison.

Figure 9 shows the format of the break data and break control register. The break data pattern is 16 bits wide, with bit 16 being the most significant bit and last to be shifted in. The Break Control register contains three fields. Bits 0 and 1 control the DCMP output and bit 2 selects between the Y and the Q bus to be compared with the break data register. Bits 3 to 15 are reserved for future expansion.

BREAK DATA REGISTER FORMAT



BREAK CONTROL REGISTER FORMAT



BREAK POINT CONTROL ACCESS

BUS SEL	BUS
0	Y
1	Q

DCMP CONTROL		DCMP STATUS
0	0	LOW
0	1	PIPELINED
1	0	NON-PIPELINED
1	1	HIGH

Figure 9. Breakpoint Control Registers and Opcodes

The SPC version allows data to be transferred into and out of a device and can also accommodate addresses and commands using the same number of pins. This is accomplished with a reconfiguration of the function of the diagnostic pins and internal logic. With this vastly expanded capability, SPC can conveniently be used in RAMs, peripherals an complex logic functions. These new capabilities allow the user to monitor and modify all of the storage elements and pins of a device. With a simple hardware interface and appropriate software, any type personal or mini computer can be turned into a development system for IDT parts with serial diagnostics.

Figure 10 shows the Serial Protocol Channel being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer) as well as data registers around the IDT49C403. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine.

The block diagram of the diagnostics ring shows how the devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

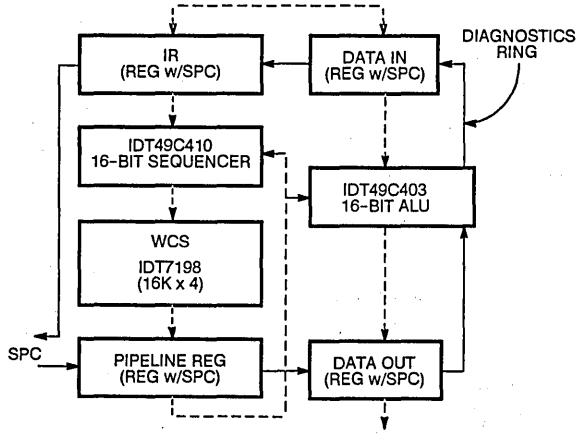


Figure 10. Typical Microprogram Application with SPC

Table 4a. ALU Destination Control (Word Mode) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15}	QIO_0
L L L L	Arith. F/2→Y	0	Input				F_0	L	Hold	Z	Z
L L L H	Log. F/2→Y	1						L	Hold	Z	Z
L L H L	Arith. F/2→Y	2						L	Log. Q/2→Q	Input	Q_0
L L H H	Log. F/2→Y	3						L	Log. Q/2→Q	Input	Q_0
L H L L	F→Y	4					Parity	L	Hold	Z	Z
L H L H	F→Y	5						H	Log. Q/2→Q	Input	Q_0
L H H L	F→Y	6						H	F→Q	Z	Z
L H H H	F→Y	7						L	F→Q	Z	Z
H L L L	Arith. 2F→Y	8	F_{14}	F_{14}	F_{15}	F_{15}	Input	L	Hold	Z	Z
H L L H	Log. 2F→Y	9	F_{15}	F_{15}				L	Hold	Z	Z
H L H L	Arith. 2F→Y	A	F_{14}	F_{14}				L	Log. 2Q →Q	Q_{15}	Input
H L H H	Log. 2F→Y	B	F_{15}	F_{15}				L	Log. 2Q →Q	Q_{15}	Input
H H L L	F→Y	C						H	Hold	Z	Z
H H L H	F→Y	D						H	Log. 2Q →Q	Q_{15}	Input
H H H L	Sign Extend	E		SIO_0	SIO_0			L	Hold	Z	Z
H H H H	F→Y	F		F_{15}	F_{15}			L	Hold	Z	Z

Table 4b. ALU Destination Control (Byte Mode) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0 SA	SIO_0 MSS	SIO_0 IS	SIO_0 LSS	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15} MSS/IS	QIO_{15} SA/LSS	QIO_0 MSS/IS	QIO_0 SA/LSS
L L L L	Arith. F/2→Y	0	Input				F_0	SIO_{15}	SIO_{15}	F_0	L	Hold	Z			
L L L H	Log. F/2→Y	1									L	Hold	Z			
L L H L	Arith. F/2→Y	2									L	Log. Q/2→Q	Input		QIO_{15}	Q_0
L L H H	Log. F/2→Y	3									L	Log. Q/2→Q	Input		QIO_{15}	Q_0
L H L L	F→Y	4					Parity			Parity	L	Hold	Z			
L H L H	F→Y	5									H	Log. Q/2→Q	Input		QIO_{15}	Q_0
L H H L	F→Y	6									H	F→Q	Z			
L H H H	F→Y	7									L	F→Q				
H L L L	Arith. 2F→Y	8	F_8	SIO_0	SIO_0	F_8	Input				L	Hold				
H L L H	Log. 2F→Y	9	F_7			F_7					L	Hold				
H L H L	Arith. 2F→Y	A	F_8			F_8					L	Log. 2Q →Q	QIO_0	Q_7	Input	
H L H H	Log. 2F→Y	B	F_7			F_7					L	Log. 2Q →Q	QIO_0	Q_7	Input	
H H L L	F→Y	C									H	Hold	Z			
H H L H	F→Y	D									H	Log. 2Q →Q	QIO_0	Q_7	Input	
H H H L	Sign Extend	E									L	Hold	Z			
H H H H	F→Y	F									L	Hold	Z			

Parity = F_{15} ⊕ F_{14} ..... ⊕ F_3 ⊕ F_2 ⊕ F_1 ⊕ F_0 ⊕ SIO_{15}
⊕ = Exclusive OR

L = LOW
H = HIGH
Z = High Impedance

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

Table 4c. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15}								Y_{15}								Y_{14}							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	Input →								0	F_{15}	0	F_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	F_{15}	0	F_{15}
L L L H	Log. F/2→Y	1										SIO_{15}		SIO_{15}						F_{15}		F_{15}				
L L H L	Arith. F/2→Y	2										F_{15}		F_{15}						SIO_{15}		SIO_{15}				
L L H H	Log. F/2→Y	3										SIO_{15}		SIO_{15}						F_{15}		F_{15}				
L H L L	F→Y	4										F_{15}		F_{15}		F_{15}		F_{15}		F_{14}		F_{14}		F_{14}		F_{14}
L H L H	F→Y	5																								
L H H L	F→Y	6																								
L H H H	F→Y	7																								
H L L L	Arith. 2F→Y	8	F_6	F_{14}	SIO_0	F_{14}	SIO_0	F_{15}	F_6	F_{15}						F_{14}		F_{14}		F_{13}		F_{13}		F_{13}		F_{13}
H L L H	Log. 2F→Y	9	F_7	F_{15}		F_{15}			F_7			F_{14}		F_{14}												
H L H L	Arith. 2F→Y	A	F_6	F_{14}		F_{14}			F_6			F_{15}		F_{15}												
H L H H	Log. 2F→Y	B	F_7	F_{15}		F_{15}			F_7			F_{14}		F_{14}												
H H L L	F→Y	C										F_{15}		F_{15}		F_{15}		F_{15}		F_{14}		F_{14}		F_{14}		F_{14}
H H L H	F→Y	D										F_{15}		F_{15}												
H H H L	Sign Extend	E			SIO_0		SIO_0				F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7		F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7	
H H H H	F→Y	F			F_{15}		F_{15}				0		0	F_{15}	0	F_{15}	0		0		0	F_{14}	0	F_{14}	0	

Table 4c. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	Y_{13-9}								Y_8								Y_7							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	0	F_{I+1}	0	F_{I+1}	0	F_{I+1}	0	F_{I+1}	0	F_9	0	F_9	0	F_9	0	F_9	F_7	F_8	0	F_8	0	F_8	F_7	F_8
L L L H	Log. F/2→Y	1																	SIO_{15}						SIO_{15}	
L L H L	Arith. F/2→Y	2																	F_7						F_7	
L L H H	Log. F/2→Y	3																	SIO_{15}						SIO_{15}	
L H L L	F→Y	4		F_I		F_I		F_I		F_I		F_8		F_8		F_8		F_8	F_7	F_7		F_7		F_7	F_7	F_7
L H L H	F→Y	5																								
L H H L	F→Y	6																								
L H H H	F→Y	7																								
H L L L	Arith. 2F→Y	8		F_{I-1}		F_{I-1}		F_{I-1}		F_{I-1}		F_7		F_7		F_7		F_7	F_6	F_6		F_6		F_6	F_6	F_6
H L L H	Log. 2F→Y	9																	F_6						F_6	
H L H L	Arith. 2F→Y	A																	F_7						F_7	
H L H H	Log. 2F→Y	B																	F_6						F_6	
H H L L	F→Y	C		F_I		F_I		F_I		F_I		F_8		F_8		F_8		F_8	F_7	F_7		F_7		F_7	F_7	F_7
H H L H	F→Y	D				F_I		F_I						F_8		F_8						F_7		F_7		
H H H L	Sign Extend	E	F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7		F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7				SIO_0	SIO_0	SIO_0	SIO_0		
H H H H	F→Y	F	0		0	F_I	0	F_I	0		0		0	F_8	0	F_8	0				0	F_7	0	F_7		

Table 4c. ALU Destination Control (cont'd.) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	Y_6								Y_{5-1}								Y_0							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	SIO_{15}	F_7	0	F_7	0	F_7	SIO_{15}	F_7	F_{i+1}	F_{i+1}	0	F_{i+1}	0	F_{i+1}	F_{i+1}	F_{i+1}	F_1	F_1	0	F_1	0	F_1	F_1	F_1
L L L H	Log. F/2→Y	1	F_7						F_7																	
L L H L	Arith. F/2→Y	2	SIO_{15}						SIO_{15}																	
L L H H	Log. F/2→Y	3	F_7						F_7																	
L H L L	F→Y	4	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
L H L H	F→Y	5																								
L H H L	F→Y	6																								
L H H H	F→Y	7																								
H L L L	Arith. 2F→Y	8	F_5	F_5		F_5		F_5	F_5	F_5	F_{i-1}	F_{i-1}		F_{i-1}		F_{i-1}	F_{i-1}	F_{i-1}	SIO_0	SIO_0		SIO_0		SIO_0	SIO_0	SIO_0
H L L H	Log. 2F→Y	9																								
H L H L	Arith. 2F→Y	A																								
H L H H	Log. 2F→Y	B																								
H H L L	F→Y	C	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
H H L H	F→Y	D				F_6		F_6						F_i		F_i						F_0		F_0		
H H H L	Sign Extend	E			SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0		
H H H H	F→Y	F			0	F_6	0	F_6					0	F_i	0	F_i					0	F_0	0	F_0		

i = 1 to 6 (for F_{5-1})
i = 9 to 14 (for F_{13-9})

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

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Table 4c. ALU Destination Control (cont'd.) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_0							
			SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	F_0	F_0	SIO_{15}	F_0	SIO_{15}	F_0	F_0	F_0
L L L H	Log. F/2→Y	1								
L L H L	Arith. F/2→Y	2								
L L H H	Log. F/2→Y	3								
L H L L	F→Y	4	Parity	Parity		Parity		Parity	Parity	Parity
L H L H	F→Y	5								
L H H L	F→Y	6								
L H H H	F→Y	7								
H L L L	Arith. 2F→Y	8	Input →							
H L L H	Log. 2F→Y	9								
H L H L	Arith. 2F→Y	A								
H L H H	Log. 2F→Y	B								
H H L L	F→Y	C								
H H L H	F→Y	D								
H H H L	Sign Extend	E								
H H H H	F→Y	F								

Table 4d. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	Q REGISTER AND SHIFTER FUNCTION	HEX	QIO_{15}				Q_{15}				Q_{14-9}				Q_8			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Z →				Hold →				Hold →				Hold →			
L L L H	Hold	1	Z →				↓				↓				↓			
L L H L	Log. Q/2→Q	2	Input →				QIO_{15}		QIO_{15}		Q_{I+1}		Q_{I+1}		Q_9		Q_9	
L L H H	Log. Q/2→Q	3	Input →				QIO_{15}		QIO_{15}		Q_{I+1}		Q_{I+1}		Q_9		Q_9	
L H L L	Hold	4	Z →				Hold		Hold		Hold		Hold		Hold		Hold	
L H L H	Log. Q/2→Q	5	Input →				QIO_{15}		QIO_{15}		Q_{I+1}		Q_{I+1}		Q_9		Q_9	
L H H L	F→Q	6	Z →				F_{15}		F_{15}		F_I		F_I		F_8		F_8	
L H H H	F→Q	7	↓				F_{15}		F_{15}		F_I		F_I		F_8		F_8	
H L L L	Hold	8					Hold		Hold		Hold		Hold		Hold		Hold	
H L L H	Hold	9					Hold		Hold		Hold		Hold		Hold		Hold	
H L H L	Log. 2Q→Q	A	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{I-1}		Q_{I-1}		Q_7		Q_7	
H L H H	Log. 2Q→Q	B	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{I-1}		Q_{I-1}		Q_7		Q_7	
H H L L	Hold	C	Z →				Hold		Hold		Hold		Hold		Hold		Hold	
H H L H	Log. 2Q→Q	D	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{I-1}		Q_{I-1}		Q_7		Q_7	
H H H L	Hold	E	Z →				Hold		Hold		Hold		Hold		Hold		Hold	
H H H H	Hold	F	Z →				Hold		Hold		Hold		Hold		Hold		Hold	

Table 4d. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

I_8 I_7 I_6 I_5	Q REGISTER AND SHIFTER FUNCTION	HEX	Q_7				Q_{6-1}				Q_0				QIO_0			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Hold →				Hold →				Hold →				Z →			
L L L H	Hold	1	↓				↓				↓				Z →			
L L H L	Log. Q/2→Q	2	Q_8	QIO_{15}	Q_8		Q_{I+1} →				Q_1 →				QIO_{15}	Q_0 →		
L L H H	Log. Q/2→Q	3	Q_8	QIO_{15}	Q_8		Q_{I+1} →				Q_1 →				QIO_{15}	Q_0 →		
L H L L	Hold	4	Hold →				Hold →				Hold →				Z →			
L H L H	Log. Q/2→Q	5	Q_8	QIO_{15}	Q_8		Q_{I+1} →				Q_1 →				QIO_{15}	Q_0 →		
L H H L	F→Q	6	F_7 →				F_I →				F_0 →				Z →			
L H H H	F→Q	7	F_7 →				F_I →				F_0 →				↓			
H L L L	Hold	8	Hold →				Hold →				Hold →							
H L L H	Hold	9	Hold →				Hold →				Hold →							
H L H L	Log. 2Q→Q	A	Q_6 →				Q_{I-1} →				QIO_0 →				Input →			
H L H H	Log. 2Q→Q	B	Q_6 →				Q_{I-1} →				QIO_0 →				Input →			
H H L L	Hold	C	Hold →				Hold →				Hold →				Z →			
H H L H	Log. 2Q→Q	D	Q_6 →				Q_{I-1} →				QIO_0 →				Input →			
H H H L	Hold	E	Hold →				Hold →				Hold →				Z →			
H H H H	Hold	F	Hold →				Hold →				Hold →				Z →			

Parity = F_{15} ⊕ F_{14} ..... ⊕ F_3 ⊕ F_2 ⊕ F_1 ⊕ F_0 ⊕ SIO_{15}

⊕ = Exclusive OR

I = 1 to 6 (for Q_{6-1})

I = 9 to 14 (for Q_{14-9})

Z = High Impedance

SA = Stand Alone

MSS = Most Significant Slice

IS = Intermediate Slice

LSS = Least Significant Slice

Table 5. Special Functions [7]

HEX $I_8\ I_7\ I_6\ I_5$	I_4	HEX $I_3\ I_2\ I_1\ I_0$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_{15}		SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_{15}	QIO_0	$\overline{WRITE}$
						MSS	OTHER SLICES					
0	L	0	Unsigned Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (1)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	L	0	BCD-to-Binary Conversion	(4)	Log F/2→Y	Input	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	H	0	Multiprecision BCD-to-Binary	(4)	Log F/2→Y	Input	Input	F_0	Hold	HZ	Q_0	L
2	L	0	Two's Complement Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y (2)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F=S-2+C_n$	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
4	L	0	Increment by One or Two	$F=S+1+C_n$	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
4	H	0	Byte Swap + C_n	$F=(S_{LB}, S_{UB})+C_n$	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
5	L	0	Sign/Magnitude Two's Complement	$F=S+C_n$ if $Z=L$ $F=\overline{S}+C_n$ if $Z=H$	F/2→Y (3)	Input	Input	Parity	Hold	HZ	HZ	L
6	L	0	Two's Complement Multiply, Last Cycle	$F=S+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log F/2→Y (2)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
7	L	0	BCD Divide by Two	(4)	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
8	L	0	Single Length Normalize	$F=S+C_n$	F→Y	F_{15}	F_{15}	HZ	Log 2Q→Q	Q_{15}	Input	L
9	L	0	Binary-to-BCD Conversion	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
9	H	0	Multiprecision Binary-to-BCD	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Hold	HZ	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F=S+C_n$	Log 2F→Y	R_{15} V F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
B	L	0	BCD Add	$F=R+S+C_n$ BCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L
C	L	0	Two's Complement Divide	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log 2F→Y	R_{15} V F	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
D	L	0	BCD Subtract	$F=R-S-1+C_n$ BCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L
E	L	0	Two's Complement Divide Correction and Remainder	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	F→Y	F_{15}	F_{15}	HZ	Log 2Q→Q	Q_{15}	Input	L
F	L	0	BCD Subtract	$F=S-R-1+C_n$BCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L

NOTES:

1. At the most significant slice only, the C_{n+16} signal is internally gated to the Y output.
2. At the most significant slice only, F_{15} ⩛ OVR is internally gated to the Y output.
3. At the most significant slice only, S_{15} ⩛ F_{15} is generated at the Y output.
4. On each nibble, F = S if magnitude of S is less than 8, and F = S minus three if magnitude of S is 8 or greater.
5. On each nibble, F = S if magnitude of S is less than 5, and F = S plus three if magnitude of S is 5 or greater. Addition is modulo 16.
6. Additions and Subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})\,(\overline{P}_{4I+0} + \overline{G}_{4I+2})\,(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propage: $P = PN_3\ PN_2\ PN_1\ PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})\,(\overline{G}_{4I+0} + \overline{G}_{4I+1})\,(\overline{P}_{4I+1} + \overline{G}_{4I+2})\,(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3\ V\ GN_2\ PN_3\ V\ GN_1\ PN_2\ PN_3 V\ GN_0\ PN_1\ PN_2\ PN_3$

L = LOW LB = Lower Byte ⩛ = Exclusive OR
H = HIGH UB = Upper Byte Parity = SIO_{15} ⩛ F_{15} ⩛ F_{14} ⩛ F_{13} ⩛ ..... ⩛ F_0
HZ = High Impedance

Table 6a. IDT49C403 Status Outputs (Word Mode)

HEX I_8 I_7 I_6 I_5	HEX I_4 I_3 I_2 I_1	I_0	G_i (i=0 to 15)	P_i (i=0 to 15)	C_{n+15}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)			
						MSS/SA	OTHER SLICES	MSS/SA	OTHER SLICES	MSS	ISS	LSS	SA
X	0	H	0	1	0	0	0	F_{15}	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee SI$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	Ri	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
0	0	L	0 if Z=L $Ri \wedge Si$ if Z=H	Si if Z=L $Ri \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
1	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
1	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
2	0	L	0 if Z=L $Ri \wedge Si$ if Z=H	Si if Z=L $Ri \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
3	0	L	(6)	(7)	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	0	L	(1)	(2)	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	8	L	(1)	(2)	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f(Y)	f(Y)	f(Y)
5	0	L	0	$\overline{Si}$ if Z=L $\overline{Si}$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15} if Z=L $F_{15} \veebar S_{15}$ if Z=H	$\overline{G}$	S_{15}	Input	Input	S_{15}
6	0	L	0 if Z=L $\overline{Ri} \wedge Si$ if Z=H	Si if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
7	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
8	0	L	0	Si	(4)	$Q_2 \veebar Q_1$	$\overline{P}$	Q_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	0	L	0	Si	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
A	0	L	0	Si	(3)	$F_2 \veebar F_1$	$\overline{P}$	F_{15}	$\overline{G}$	(5)	(5)	(5)	(5)
B	0	L	$Ri \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	(8)	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
C	0	L	$Ri \wedge Si$ if Z=L $\overline{Ri} \wedge Si$ if Z=H	$Ri \vee Si$ if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
D	0	L	$Ri \wedge \overline{Si}$	$Ri \vee \overline{Si}$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
E	0	L	$Ri \wedge Si$ if Z=L $\overline{Ri} \wedge Si$ if Z=H	$Ri \vee Si$ if Z=L $\overline{Ri} \vee Si$ if Z=H	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
F	0	L	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+15} \veebar C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)

Continued next page

NOTES:

1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3,\ldots,15} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3,\ldots,15} = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$
3. At the most significant slice, $C_{n+16} = Q_{15} \oplus Q_{14}$. At other slices $C_{n+16} = G \vee PC_n$
4. At the most significant slice, $C_{n+16} = F_{15} \oplus F_{14}$. At other slices $C_{n+16} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots \overline{Q}_{15}\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3 \ldots \overline{F}_{15}$
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3,\ldots,15} = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = S_{0,1,2,3,\ldots,15}$
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3,\ldots,15} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3,\ldots,15} = 1$
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})(\overline{P}_{4I+0} + \overline{G}_{4I+2})(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propagate: $P = PN_3\ PN_2\ PN_1\ PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})(\overline{G}_{4I+0} + \overline{G}_{4I+1})(\overline{P}_{4I+1} + \overline{G}_{4I+2})(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3 \vee GN_2\ PN_3 \vee GN_1\ PN_2\ PN_3 \vee GN_0\ PN_1\ PN_2\ PN_3$

V = OR
$\wedge$ = AND
$\oplus$ = Exclusive-OR
$P = P_{15}P_{14} \ldots\ldots P_3P_2P_1P_0$
$G = G_{15} \vee G_{14}P_{15} \vee G_{13}P_{14}P_{15} \vee G_{12}P_{13}P_{14}P_{15} \vee G_{11}P_{12}P_{13}P_{14}P_{15} \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_{15}$

$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_{15}$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_{15}$
L = LOW = 0
H = HIGH = 1

Table 6b. IDT49C403 Status Outputs (Byte Mode)

HEX $I_8\ I_7\ I_6\ I_5$	HEX $I_4\ I_3\ I_2\ I_1$	I	Q_I (i=0 to 7)	P_I (i=0 to 7)	C_{n+7}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)			
						MSS/SA	OTHER SLICES	MSS/SA	OTHER SLICES	MS	ISS	LSS	SA
X	0	H	0	1	0	0	0	F_7	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee SI$	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	Ri	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	$G \vee PC_n$	$C_{n+7} \oplus C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)

NOTES:

$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_7$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_7$
L = LOW = 0
H = HIGH = 1

V = OR
$\wedge$ = AND
$\oplus$ = Exclusive OR
$P = P_7P_6 \ldots\ldots P_3P_2P_1P_0$
$G = G_7 \vee G_6P_7 \vee G_5P_6P_7 \vee G_4P_5P_6P_7 \vee G_3P_4P_5P_6P_7 \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_7$

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level (4)			2.0	–	–	V
V_{IL}	Input LOW Level (4)			–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 12mA MIL.	–	0.3	0.5	
			I_{OL} = 16mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–	-40	µA
			V_O = V_{CC} (max.)	–	–	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment. Guaranteed by Design.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		–	150	250	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		–	50	100	mA
I_{CCT}	Quiescent Input Power Supply [5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	3.6	7.7	mA/MHz
			COM'L.	–	3.6	5.2	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	136	252	mA
			COM'L.	–	136	227	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	150	275	
			COM'L.	–	150	250	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

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IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of -55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 7. Clock and Write Pulse Characteristics All Functions

	COM'L.	MIL.	UNIT
Minimum Clock Low Time	10	11	ns
Minimum Clock High Time	10	11	ns
MInimum Time CP and WE both Low to Write	10	11	ns

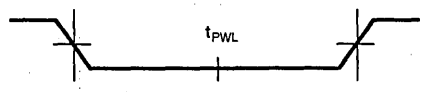
NOTE:
Guaranteed by Design.

Table 8. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L.	ENABLE MIL.	DISABLE COM'L.	DISABLE MIL.	UNIT
$\overline{OE}_Y$	Y	12	20	10	12	ns
$\overline{OE}_B$	DB	14	22	12	13	ns
$\overline{OE}_A$	DA	15	22	13	14	ns
I_8	SIO	23	25	12	13	ns
I_8	QIO	16	24	21	22	ns
$I_{8,7,6,5}$	QIO	17	28	19	22	ns
$I_{4,3,2,1,0}$	QIO	21	31	19	22	ns

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 9. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	UNIT	COMMENTS
Y	CP	–	–	–	–	8	9	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	7	8	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	10	11	0	0	ns	Write into RAM
A, B Source	CP	11	12	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0,15}$	CP	–	–	–	–	5	6			ns	Shift Q
$I_{8,7,6,5}$	CP	–	–	–	–	23	25	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	7	8	(3)		–	–			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4,3,2,1,0}$	CP	–	–	–	–	16	18			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	8	9	2	2	ns	Write into Q
C_n	CP	–	–	–	–	28	30	0	0	ns	ALU Carry In to RAM

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE STANDARD AND INCREMENT (SF-4) /DECREMENT (SF-3) BY ONE OR TWO INSTRUCTIONS

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	41	48	44	48	44	48	42	45	47	58	47	57	26	33	–	–	–	–	41	48	40	48	52	56	ns
DA, DB	Any	34	38	28	33	28	34	29	31	36	42	34	40	–	–	–	–	–	–	24	29	27	33	46	50	ns
C_n	Any	27	35	15	19	–	–	22	24	26	29	23	28	–	–	–	–	–	–	24	29	26	30	26	30	ns
I_{8-0}	Any	38	43	32	34	23	35	48	51	36	38	42	45	–	–	18	25	24	27	28	38	37	40	41	50	ns
CP	Any	43	46	44	48	39	42	39	42	51	55	54	58	20	25	–	–	26	30	36	39	37	40	41	45	ns
MSS	Any	21	35	–	–	21	23	38	43	21	25	20	23	–	–	–	–	–	–	–	–	20	23	–	–	ns
$SIO_{0,15}$	Any	21	27	–	–	–	–	17	19	–	–	–	–	–	–	–	–	–	–	–	–	19	23	16	20	ns

MULTIPLY INSTRUCTIONS (SF-0, 2 & 6)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	–	–	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	–	–	43	50	41	48	–	–	–	–	–	–	29	35	ns
C_n	Any	32	42	18	23	–	–	–	–	31	35	28	34	–	–	–	–	–	–	29	35	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	ns
CP	Any	52	55	53	58	47	50	–	–	61	66	65	70	24	30	–	–	31	36	43	47	ns
Z ($\overline{OE}_Y$ = low)	Any	47	48					–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

Unsigned Multiply

SF 0: F=S+C_n If Z=L
F=S+R+C_n If Z=H
Y15=C_n + 16 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply

SF 2: F=S+C_n If Z=L
F=S+R+C_n If Z=H
Y15=F15 V OVR (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply Last Cycle

SF 6: F=S+C_n If Z=L
F=S-R-1+C_n If Z=H
Y15=OVR V F15 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE
BCD INSTRUCTIONS (SF-1, 7, 9, B, D & F)

FROM	SLICE	TO Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	48	58	62	67	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	29	35	32	40	55	64	ns
C_n	Any	32	42	18	23	–	–	26	29	31	35	28	34	–	–	–	–	–	–	29	35	31	36	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	44	48	49	60	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	43	47	44	48	49	54	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF 1) Binary to BCD conversion (SF 9) BCD substract (SF F)
BCD divide by two (SF 7) BCD add (SF B)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF-5)

FROM	SLICE	TO Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	29	35	ns
C_n	Any	32	42	18	23	–	–	–	–	31	35	28	34	–	–	–	–	–	–	29	35	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	43	47	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

SF 5: F=S+C_n if Z=L Y=F
F=S+C_n if Z=H Q=Q
Y15=S15 ⊕ F15 (MSS) N=F15; Z=L
Z=S15 (MSS) N=F15 ⊕ S15; Z=H

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SF-A, C & E)

FROM	SLICE	TO: Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_{15}		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	32	40	ns
C_n	Any	32	42	18	23	–	–	26	29	31	35	28	34	–	–	–	–	–	–	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	44	48	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	44	48	ns
Z ($\overline{OE}$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: F = S + C_n
N = F15 (MSS)
SIO15 = F15 ⊕ R15 (MSS)
C_n + 16 = F15 ⊕ F14 (MSS)
OVR = $\overline{F2 \oplus F1 \text{ (MSS)}}$
Z = Q0 Q1 Q2 Q3 . . . Q15 F0 F1 F2 F3 . . . F15
Y = Log 2F
Q = Log 2Q

Two's Complement Divide

SFC: F = S + R + C_n if Z = L
F = S − R − 1 + C_n if Z = H
SIO15 = F15 ⊕ R15 (MSS)
Z = F15 ⊕ R15 (MSS) from previous cycle
Y = Log 2F
Q = Log 2Q

Two's Complement Divide Correction and Remainder

SFE: S = C_n if Z = L
S − R − 1 + C_n if Z = H
Z = F15 ⊕ R15 (MSS) from previous cycle
Y = F
Q = Log 2Q

SINGLE LENGTH NORMALIZATION (SF-8)

FROM	SLICE	TO: Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_{15}		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	–	–	–	–	–	–	31	40	–	–	–	–	48	58	ns
DA, DB	Any	41	46	34	40	34	41	–	–	–	–	–	–	–	–	–	–	–	–	32	40	ns
C_n	Any	32	42	18	23	–	–	–	–	–	–	–	–	–	–	–	–	–	–	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	44	48	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	44	48	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403 over the commercial operating range of 0 to 70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of -55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 10. Clock and Write Pulse Characteristics All Functions

	COM'L.	MIL.	UNIT
Minimum Clock Low Time	12	13	ns
Minimum Clock High Time	12	13	ns
MInimum Time CP and WE both Low to Write	12	13	ns

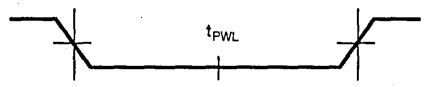
NOTE:
Guaranteed by design.

Table 11. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L.	ENABLE MIL.	DISABLE COM'L.	DISABLE MIL.	UNIT
$\overline{OE}_Y$	Y	15	24	12	14	ns
$\overline{OE}_B$	DB	17	26	15	16	ns
$\overline{OE}_A$	DA	18	26	16	17	ns
I_8	SIO	28	30	15	16	ns
I_8	QIO	20	29	25	27	ns
$I_{8,7,6,5}$	QIO	21	34	22	26	ns
$I_{4,3,2,1,0}$	QIO	25	37	22	26	ns

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 12. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	UNIT	COMMENTS
Y	CP	–	–	–	–	10	11	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	8	9	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	12	13	0	0	ns	Write into RAM
A, B Source	CP	14	15	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0,15}$	CP	–	–	–	–	6	7			ns	Shift Q
$I_{8,7,6,5}$	CP	–	–	–	–	27	30	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	8	9	(3)	(3)	(3)	(3)			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4,3,2,1,0}$	CP	–	–	–	–	19	21			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	10	11	2	2	ns	Write into Q
C_n	CP	–	–	–	–	34	36	0	0	ns	ALU Carry In to RAM

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE STANDARD AND INCREMENT (SF-4) /DECREMENT (SF-3) BY ONE OR TWO INSTRUCTIONS

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	53	53	57	53	57	50	54	56	65	56	64	32	37	–	–	–	–	50	54	48	54	63	67	ns
DA, DB	Any	40	43	34	36	34	38	35	37	43	47	40	45	–	–	–	–	–	–	29	33	33	37	55	59	ns
C_n	Any	33	39	18	21	–	–	27	29	32	34	28	30	–	–	–	–	–	–	29	33	32	34	32	34	ns
I_{8-0}	Any	46	49	39	41	39	41	56	59	43	46	51	54	–	–	21	28	29	32	34	43	45	47	49	56	ns
CP	Any	51	55	53	56	47	51	47	51	62	66	65	70	24	28	–	–	32	34	43	46	45	47	49	53	ns
MSS	Any	26	39	–	–	26	28	46	50	26	28	24	26	–	–	–	–	–	–	–	–	24	26	–	–	ns
$SIO_{0,15}$	Any	25	30	–	–	–	–	20	21	–	–	–	–	–	–	–	–	–	–	–	–	23	26	19	23	ns

MULTIPLY INSTRUCTIONS (SF-0, 2 & 6)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	–	–	67	78	67	77	38	44	–	–	–	–	60	65	ns
DA, DB	Any	48	52	41	43	41	46	–	–	52	56	48	54	–	–	–	–	–	–	35	40	ns
C_n	Any	40	47	22	25	–	–	–	–	38	41	34	36	–	–	–	–	–	–	35	40	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	41	52	ns
CP	Any	61	66	64	67	58	61	–	–	74	79	78	84	29	34	–	–	38	41	52	55	ns
Z ($\overline{OE}_Y$ = low)	Any	65	70					–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

Unsigned Multiply

SF 0: F=S+C_n If Z=L
F=S+R+C_n If Z=H
Y15=C_n+16 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply

SF 2: F=S+C_n If Z=L
F=S+R+C_n If Z=H
Y15=F15 V OVR (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply Last Cycle

SF 6: F= S+C_n If Z=L
F=S-R-1+C_n If Z=H
Y15=OVR V F15 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE
BCD INSTRUCTIONS (SF-1, 7, 9, B, D & F)

FROM	SLICE	TO Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	60	65	58	65	76	80	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	35	40	40	44	66	71	ns
C_n	Any	40	47	22	25	–	–	32	35	38	41	34	36	–	–	–	–	–	–	35	40	38	41	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	61	52	55	61	65	–	–	25	34	35	38	41	52	54	56	59	67	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	52	55	54	56	59	64	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF1) Binary to BCD conversion (SF9) BCD substract (SFF)
BCD divide by two (SF7) BCD add (SFB)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF-5)

FROM	SLICE	TO Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	60	65	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	35	40	ns
C_n	Any	40	47	22	25	–	–	–	–	38	41	34	36	–	–	–	–	–	–	35	40	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	41	52	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	52	55	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

SF 5: F=S+C_n if Z=L
F=S+C_n if Z=H
Y15=S15 ⊕ F15 (MSS)
Z=S15 (MSS)

Y=F
Q=Q
N=F15; Z=L
N=F15 ⊕ S15; Z=H

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SF-A, C & E)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_{15}		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	58	65	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	40	44	ns
C_n	Any	40	47	22	25	–	–	32	35	38	41	34	36	–	–	–	–	–	–	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	54	56	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	54	56	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: F=S+C_n
N=F15 (MSS)
SIO15=F15 ↑ R15 (MSS)
C_n+16=F15 ↑ F14 (MSS)
OVR=F2 ↑ F1 (MSS)
Z=$\overline{Q0}$ $\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$ . . . $\overline{Q15}$ F0 F1 F2 F3 . . . F15
Y=Log 2F
Q=Log 2Q

Two's Complement Divide

SFC: F=S+R+C_n If Z=L
F=S–R–1+C_n If Z=H
SIO15=$\overline{F15}$ ↑ $\overline{R15}$ (MSS)
Z=$\overline{F15}$ ↑ $\overline{R15}$ (MSS) from previous cycle
Y=Log 2F
Q=Log 2Q

Two's Complement Divide Correction and Remainder

SFE: S=C_n If Z=L
S–R–1+C_n If Z=H
Z=$\overline{F15}$ ↑ $\overline{R15}$ (MSS) from previous cycle
Y=F
Q=Log 2Q

SINGLE LENGTH NORMALIZATION (SF-8)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_{15}		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	–	–	–	–	–	–	38	44	–	–	–	–	58	65	ns
DA, DB	Any	48	52	41	43	41	46	–	–	–	–	–	–	–	–	–	–	–	–	40	44	ns
C_n	Any	40	47	22	25	–	–	–	–	–	–	–	–	–	–	–	–	–	–	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	54	56	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	54	56	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested but is guaranteed by correlation to the Standard Function Table.

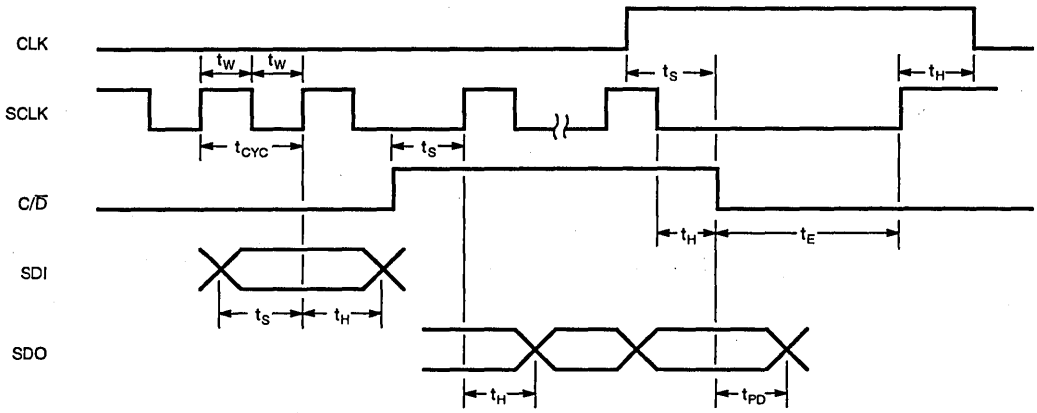


Figure 11. IDT49C403 SPC Timing Waveforms

IDT49C403/A SPC AC TIMING

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
t_{PD}	SCLK TO SDO	R_L = 500Ω C_L = 50pF	3	15	ns
t_{PD}	C/$\overline{D}$ to SDO		3	50	ns
t_S	C/$\overline{D}$ to SCLK		5	–	ns
t_S	CLK to C/$\overline{D}$		20	–	ns
t_S	SDI to SCLK		10	–	ns
t_H	C/$\overline{D}$ to SCLK		5	–	ns
t_H	CLK to SCLK		5	–	ns
t_H	SDI to SCLK		5	–	ns
t_W	Pulse Width SCLK		20	–	ns
t_{CYC}	SCLK Period		50	–	ns
t_E	Execution, C/$\overline{D}$ to SCLK		50	–	ns

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C403 INPUT/OUTPUT INTERFACE CIRCUITRY

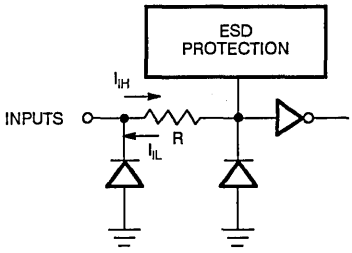


Figure 12. Input Structure (All Inputs)

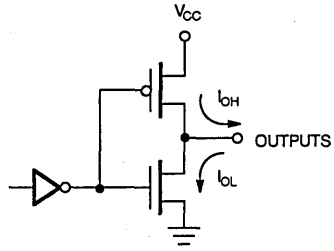


Figure 13. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

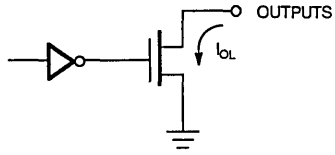
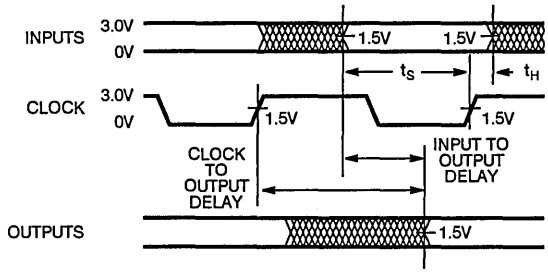


Figure 14. Open Drain Structure

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT

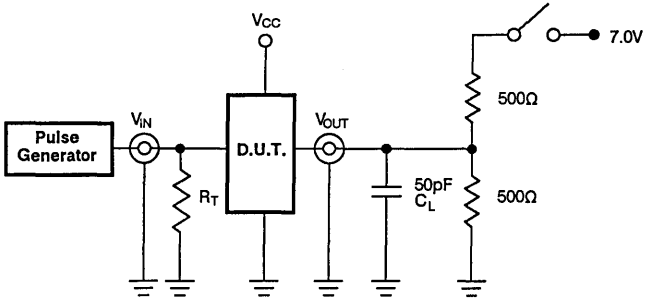


Figure 15. Test Load Circuit

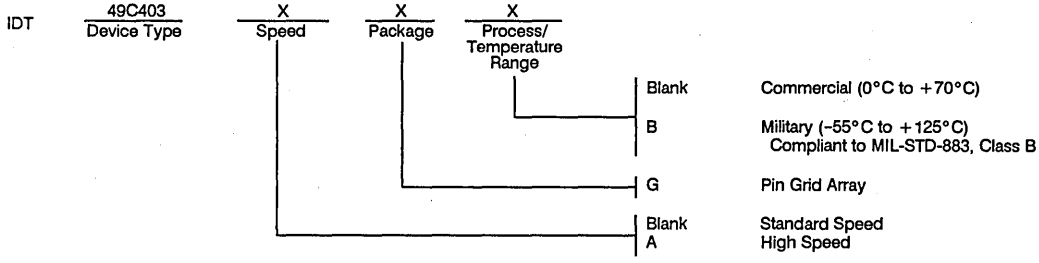
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the pulse generator

ORDERING INFORMATION



Integrated Device Technology, Inc.

16-BIT CMOS MICROPROGRAM SEQUENCER

IDT 49C410
IDT 49C410A

MICROSLICE™ PRODUCT

FEATURES:

- 16-bit wide address path
  - Address up to 65,536 words of microprogram memory
- 16-bit loop counter
  - Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS™
  - I_{CC} (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - IDT49C410 meets 2910A speeds
  - IDT49C410A 30% speed upgrade
- 33-deep stack
  - Accommodates highly nested microcode
- 16 powerful microinstructions
  - Executes 16 sequence control instructions
- Available in 48-pin 600 mil plastic and sidebraze, 48-pin 400 mil SHRINK-DIP, 52-pin PLCC and 48-pin Flatpack
- Three enables control branch address sources
- Four address sources
- 2910A instruction compatibility
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88643 is listed for this function

DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2910A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capacity of 65,536.

During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (µPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in/first-out stack (F).

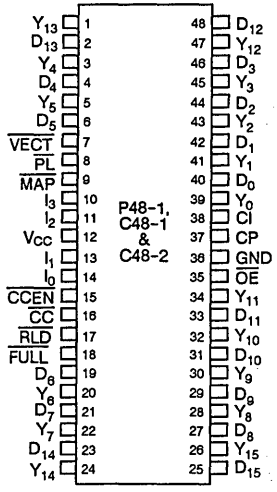
The IDT49C410s are fabricated using CEMOS, a CMOS technology designed for high performance and high reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2910A.

The IDT49C410s are available in 48-pin DIPs (600 mil x 100 mil centers or space-saving 400 mil x 70 mil centers), 52-pin PLCC and 48-pin flatpacks.

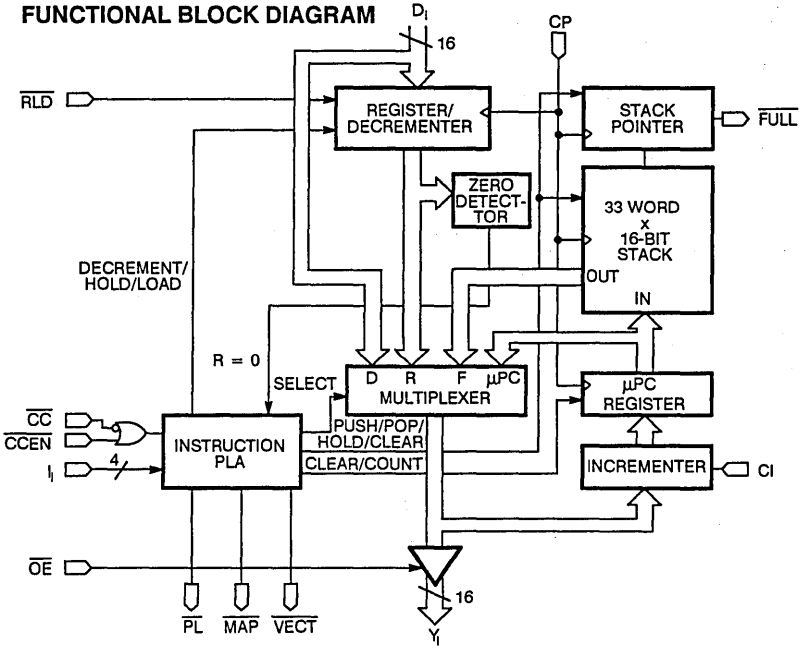
8

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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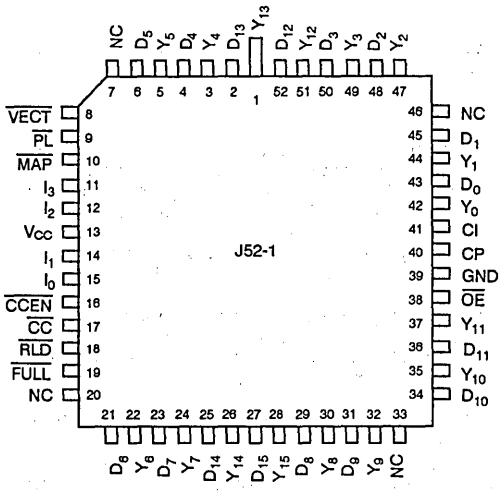
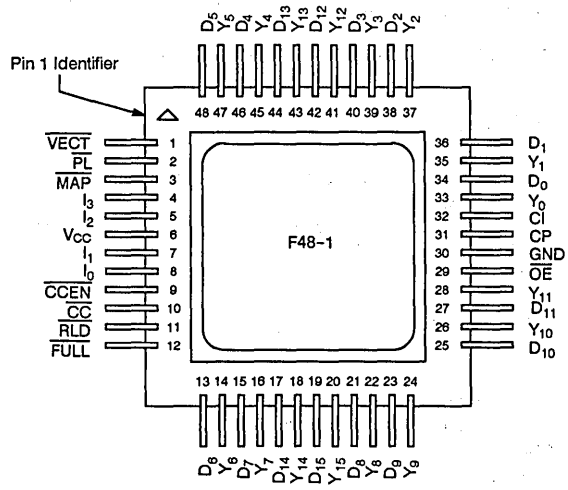
PIN CONFIGURATIONS



PLCC
TOP VIEW



FLATPACK
TOP VIEW

IDT49C410 PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
D_I	I	Direct input to register/counter and multiplexer, D_0 is LSB.
I_I	I	Selects one of sixteen instructions.
$\overline{CC}$	I	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of Y_I outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
Y_I	O	Address to microprogram memory. Y_0 is LSB, Y_{15} is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

PRODUCT DESCRIPTION

The IDT49C410s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 64K words of microprogram.

The heart of the microprogram sequencer is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of sixteen D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable as well as the four microinstruction control inputs. When the load control ($\overline{RDL}$) is LOW, the data at the D-inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT49C410s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 16-bit incrementer followed by a 16-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are sixteen D-inputs on the IDT49C410s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 16-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT49C410s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT49C410s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT49C410s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{FULL}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of 0. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed so as not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

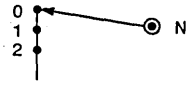
The IDT49C410s' internal 16-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 16-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT49C410s provide a 16-bit address at the Y outputs that are under control of the $\overline{OE}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

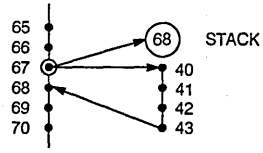
In summary, the IDT49C410s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

FIGURE 1. IDT49410 FLOW DIAGRAMS

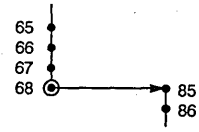
0 Jump Zero (JZ)



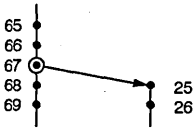
1 Cond JSB PL (CJS)



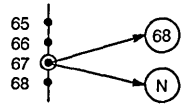
2 Jump Map (JMAP)



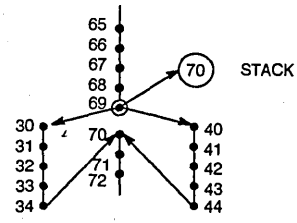
3 Cond Jump PL (CJP)



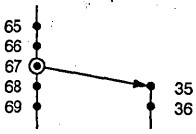
4 Push/Cond LD CNTR (PUSH)



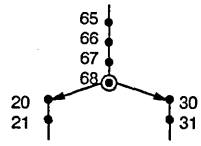
5 Cond JSB R/PL (JSRP)



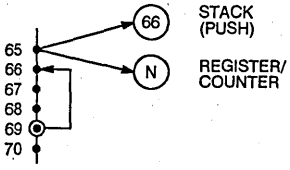
6 Cond Jump Vector (CJV)



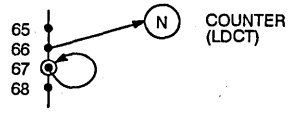
7 Cond JUMP R/PL (JRP)



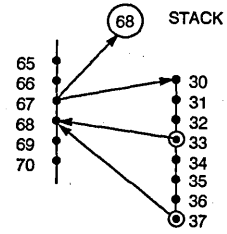
8 Repeat Loop, CNTR ≠ 0 (RFCT)



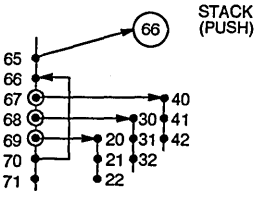
9 Repeat PL, CNTR ≠ 0 (RPCT)



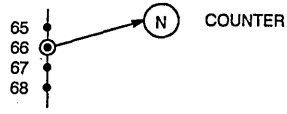
10 Cond Return (CRTN)



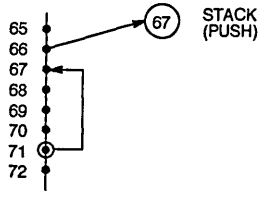
11 Cond Jump PL & POP (CJPP)



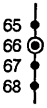
12 LD CNTR & Continue (LDCT)



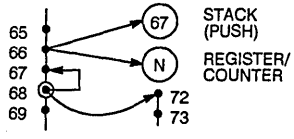
13 Test End Loop (LOOP)



14 Continue (CONT)



15 Three-Way Branch (TWB)



IDT49C410 OPERATION

The IDT49C410s are CMOS pin-compatible implementations of the Am2910 and Am2910A microprogram sequencers. The IDT49C410 sequencers are functionally identical except that they are 16 bits wide and provide a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer which determines the Y outputs and in controlling the signals that can be used to enable various branch address sources. ($\overline{PL}$,$\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock.Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT49C410s is a last-in/first-out memory that is 16 bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the $\overline{FULL}$ flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT49C410 INSTRUCTION SET

This data sheet contains a block diagram of the IDT49C410 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3-I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 64K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs, as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT49C410s can be from one of four sources. These include the internal microprogram counter; the last-in/first-out stack; the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT49C410s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT49C410s shown in figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of the stack pointer is incremented. If the test is failed, then this conditional Jump to Subroutine instruction behaves as a simple continue. That is, the contents of microinstruction address 68 are executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT49C410 microprogram sequencers is that of Conditional Jump to Address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken. If the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that, if the test is passed, the next microinstruction to be executed is the contents of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the

test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

IDT49C410 INSTRUCTION OPERATIONAL SUMMARY

I_3-I_0	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Change; DEC = Decrement

INSTRUCTION 5 – CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction, the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 – CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction, as defined from some external source. This instruction is similar to the Jump Map instruction except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 16-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 – CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 – REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/conditional load counter

instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed to the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 – REPEAT PIPELINE, COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 – CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 – CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagrams for the IDT49C410s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and since the loop in being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 – LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value of the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 – TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number if times, the stack is not popped. If the conditional test input is passed, the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary in order to have the correct address on the stack before the loop operation. For this reason, the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 – CONTINUE (CONT)

The Continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 – THREE WAY BRANCH (TWB)

The Three Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT49C410 flow diagrams and is also described in full detail in the IDT49C410s' instruction operational summary. Operation of the instruction is such that, any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left; the stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, then the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT49C410s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, then this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT49C410 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Output HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Output LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IL}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{HC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-30	–	–	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_C = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)(5)	V_{CC} = Max., V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	1.0	3.0	mA/ MHz
			COM'L.	–	1.0	1.5	
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	45	80	mA
			COM'L.	–	45	65	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	50	90	
			COM'L.	–	50	75	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH} (CD_H) + I_{CCQL} (1 - CD_H) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input Frequency

8

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le$ 0V and $V_{IH} \ge$ 3V for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C410A
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	6	7	0	0	ns
$D_I \rightarrow PC$	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	12	15	–	–	–	–	ns
I_{0-3}	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ (1)	10/10	13/13	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

IDT49C410
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	
$D_I \rightarrow R$	16	16	0	0	ns
$D_I \rightarrow PC$	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

II. COMBINATIONAL DELAYS

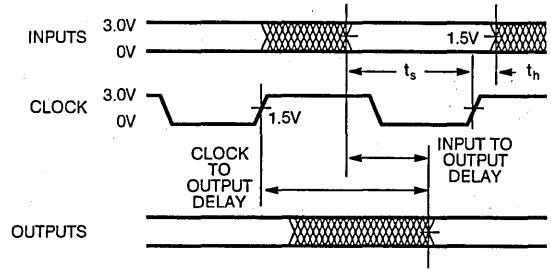
INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNIT
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	20	25	–	–	–	–	ns
I_{0-3}	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ (1)	25/27	25/30	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNIT
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

SWITCHING WAVEFORMS



IDT49C410 INPUT/OUTPUT INTERFACE CIRCUITRY

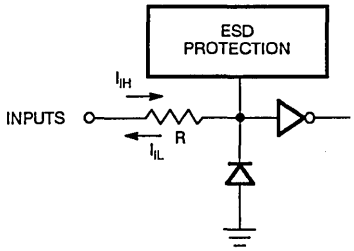


Figure 1. Input Structure

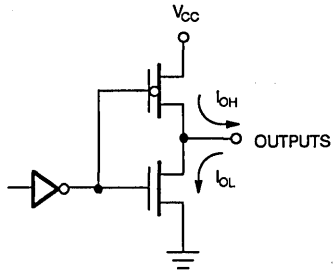


Figure 2. Output Structure

TEST LOAD CIRCUIT

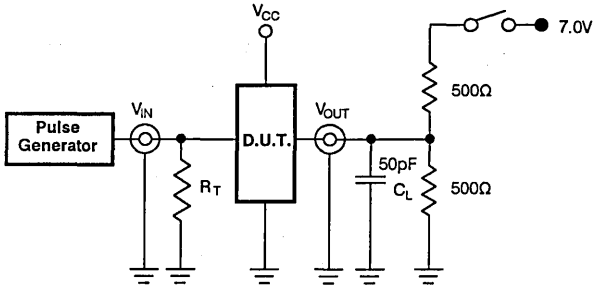


Figure 3. Switching Test Circuits

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

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ORDERING INFORMATION

IDT — 49C410 (Device Type) — X (Speed) — X (Package) — X (Process/Temperature Range)

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
P	Plastic DIP
XC	Sidebraze SHRINK-DIP
C	Sidebraze DIP
J	PLCC
F	Flatpack
Blank	16-Bit Microprogram Sequencer
A	Fast 16-Bit Microprogram Sequencer

Integrated Device Technology, Inc.

16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT 39C60
IDT 39C60-1
IDT 39C60A
IDT 39C60B

MICROSLICE™ PRODUCT

FEATURES:

- Low power CEMOS™
  - Military: 100mA (max.)
  - Commercial: 85mA (max.)
- Fast
  - Data in to error detect
    IDT39C60A: 20ns (max.), IDT39C60B: 16ns (max.)
    IDT39C60-1: 25ns (max.)
    IDT39C60: 32ns (max.)
  - Data in to corrected data out
    IDT39C60A: 30ns (max.), IDT39C60B: 25ns (max.)
    IDT39C60-1: 52ns (max.)
    IDT39C60: 65ns (max.)
- Improves system memory reliability
  - Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - Data words up to 64 bits
- Built-in diagnostics
  - Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC
- Pin-compatible to all versions of the 2960
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88613 available for this function

DESCRIPTION:

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check bits on a 16-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

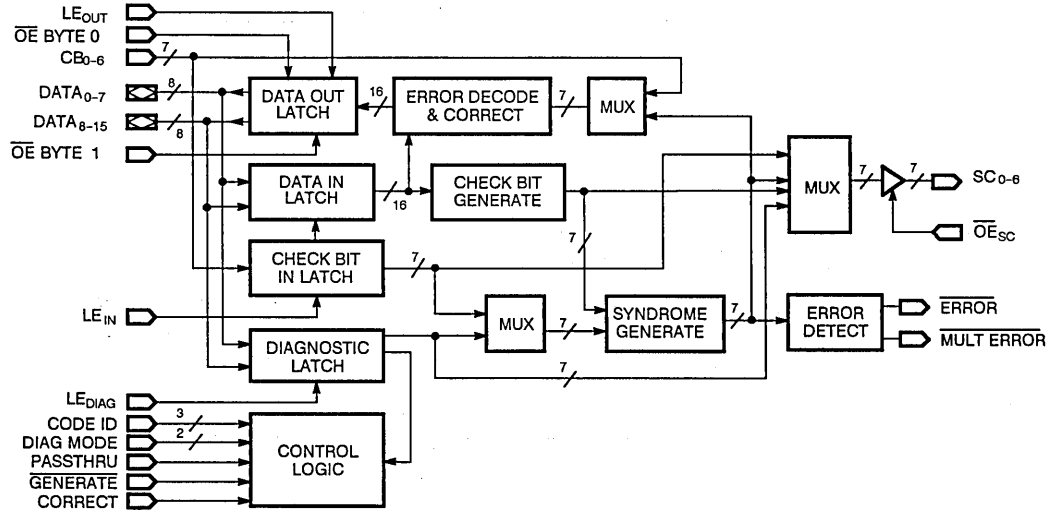
The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All parts incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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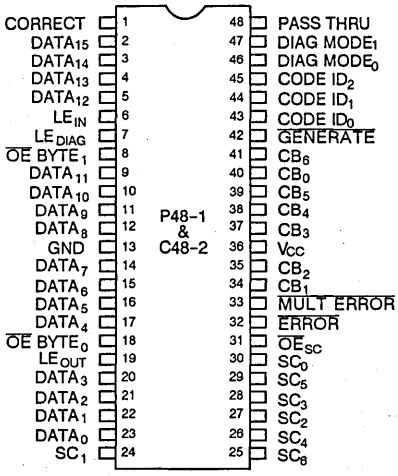
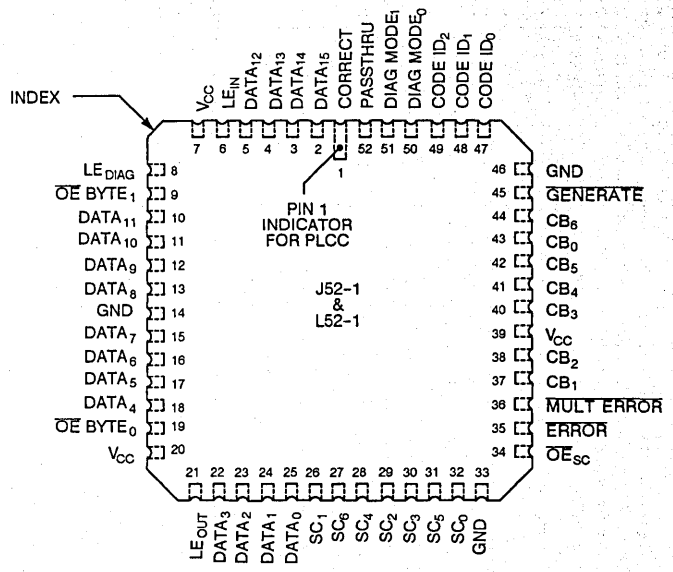
PIN CONFIGURATION



DIP
TOP VIEW
(600 mil x 100 mil CENTERS)



PLCC/LCC
TOP VIEW
(750 mil x 750 mil)

8

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-15}$	I/O	16 bidirectional data lines. They provide input to the Data Input Latch and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
CB_{0-6}	I	Seven check bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE_{IN}	I	Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{GENERATE}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC_{0-6}	O	Syndrome/Check Bit outputs. These seven lines hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{ERROR}$	O	Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{ERROR}$ must be implemented externally.)
$\overline{MULT\ ERROR}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{MULT\ ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{MULT\ ERROR}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE_{OUT}	I	Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{OE}\ BYTE_0$ $\overline{OE}\ BYTE_1$	I	Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output at a time.
PASS THRU	I	Pass Thru input. This line, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
$DIAG\ MODE_{0-1}$	I	Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.
$CODE\ ID_{0-2}$	I	Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals $CODE\ ID_{0-2}$, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.
LE DIAG	I	Latch Enable – Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for $CODE\ ID_{0-2}$, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU.

PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- Data Input Latch
- Data Output Latch
- Diagnostic Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input Latch which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostic modes.

The Data Output Latch is split into 2 bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASSTHRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs. If one or more errors are detected, $\overline{\text{ERROR}}$ goes low. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC Unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{2-0}, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.

Code 32/39 refers to a 32-bit data field with 7 check bits.

Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{2-0} of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

C_0, C_1, C_2, C_3, C_4	for the 8-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5$	for the 16-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG $MODE_{1-0}$, define 4 basic areas of operation, with $\overline{\text{GENERATE}}$, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID_{2-0} defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC_{0-6}. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-6}. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG $MODE_{1-0}$, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal control mode, the data loaded into the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

TABLE 1.
HAMMING CODE AND SLICE IDENTIFICATION

CODE ID_2	CODE ID_1	CODE ID_0	HAMMING CODE AND SLICE SELECTED
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE 2.
DIAGNOSTIC MODE CONTROL

DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

TABLE 3.
IDT39C60 OPERATING MODES

OPERATING MODE	DM1	DM0	$\overline{GENERATE}$	CORRECT	PASS-THRU	DATA OUT LATCH (LE_{OUT} = HIGH)	SC_{0-6} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ / $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	0	–	Check Bits Generated from Data In Latch	High
Detect	0 0	0 1	1	0	0	Data In Latch	Syndrome Bits Data In/Check Bit Latch	Error Dep[1]
Correct	0 0	0 1	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Check Bit Latch	Error Dep
PASSTHRU	0 0 1	0 1 0	X	X	1	Data In Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	0	–	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	0	Data In Latch	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Initialization Mode	1	1	X	X	X	Data In Latch Set to 0000	Check Bits Generated from Data In Latch (0000)	–
Internal Mode	ID_{2-0} = 001 (Control Signals ID_{2-0}, DIAG $MODE_{1-0}$, CORRECT and PASSTHRU are taken from the Diagnostic Latch)							

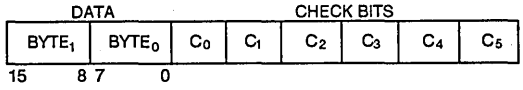
NOTE:

1. ERROR DEP (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC Unit, connected as shown in Figure 2, provides all logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicated 6 check bits are required. The CB_6 pin is, therefore, a "Don't Care" and ID_2, ID_1, ID_0 = 000.



USES MODIFIED HAMMING CODE 16/22
16 DATA BITS WITH 6 CHECK BITS

Figure 1. 16-Bit Data Format

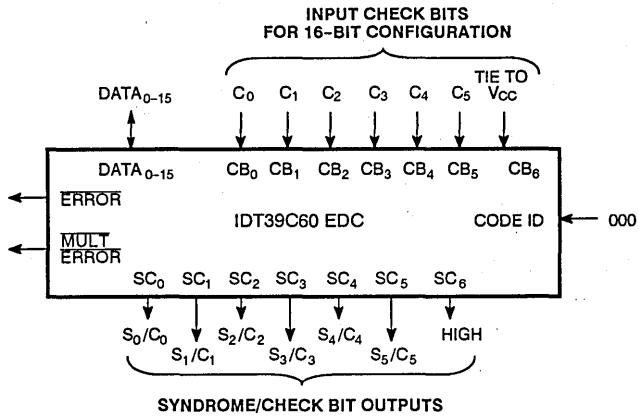


Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function or the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate mode.

TABLE 4. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART[1]

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:

1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

TABLE 5.
SYNDROME DECODE TO BIT-IN-ERROR (16-BIT CONFIGURATION)

					HEX	0	1	2	3
	SYNDROME BITS				S_5 S_4	0 0	0 1	1 0	1 1
HEX	S_3	S_2	S_1	S_0					
0	0	0	0	0		*	C4	C5	T
1	0	0	0	1		C0	T	T	14
2	0	0	1	0		C1	T	T	M
3	0	0	1	1		T	2	8	T
4	0	1	0	0		C2	T	T	15
5	0	1	0	1		T	4	10	T
6	0	1	1	0		T	3	9	T
7	0	1	1	1		M	T	T	M
8	1	0	0	0		C3	T	T	M
9	1	0	0	1		T	5	11	T
A	1	0	1	0		T	6	12	T
B	1	0	1	1		1	T	T	M
C	1	1	0	0		T	7	13	T
D	1	1	0	1		0	T	T	M
E	1	1	1	0		M	T	T	M
F	1	1	1	1		T	M	M	T

NOTES:
* = No errors detected
# = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 6.
DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit_0
1	Diagnostic Check Bit_1
2	Diagnostic Check Bit_2
3	Diagnostic Check Bit_3
4	Diagnostic Check Bit_4
5	Diagnostic Check Bit_5
6, 7	Don't Care
8	CODE ID_0
9	CODE ID_1
10	CODE ID_2
11	DIAG $MODE_0$
12	DIAG $MODE_1$
13	CORRECT
14	PASS THRU
15	Don't Care

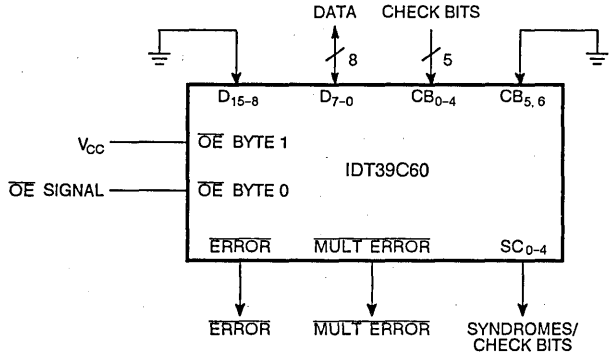


Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC Units, connected as shown in Figure 5, provide all logic needed for single bit error correction and double bit error detection of a 32-bit data field. The Identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID_2, ID_1, ID_0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{OE}_{SC}$ always enables the SC_{0-6} outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format of 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of syndrome bits from byte 2/3 into the byte 1/0 unit. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the 7 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the Data Bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate mode.

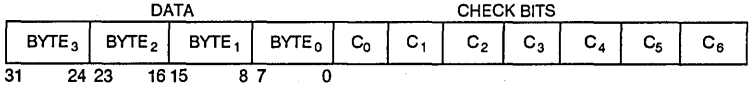
TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR (32-BIT)

					HEX	0	1	2	3	4	5	6	7
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	M
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 8.
KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-BIT PROPAGATION DELAY		COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected DATA Out	(DATA to SC) + (CB to SC, Code ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{ERROR}$ for 32 Bits	(DATA to SC) + (CB to $\overline{ERROR}$, CODE ID 011)
DATA	$\overline{MULT\ ERROR}$ for 32 Bits	(DATA to SC) + (CB to $\overline{MULT\ ERROR}$, CODE ID 011)



USES MODIFIED HAMMING CODE 32/39
32 DATA BITS WITH 7 CHECK BITS

Figure 4. 32-Bit Data Format

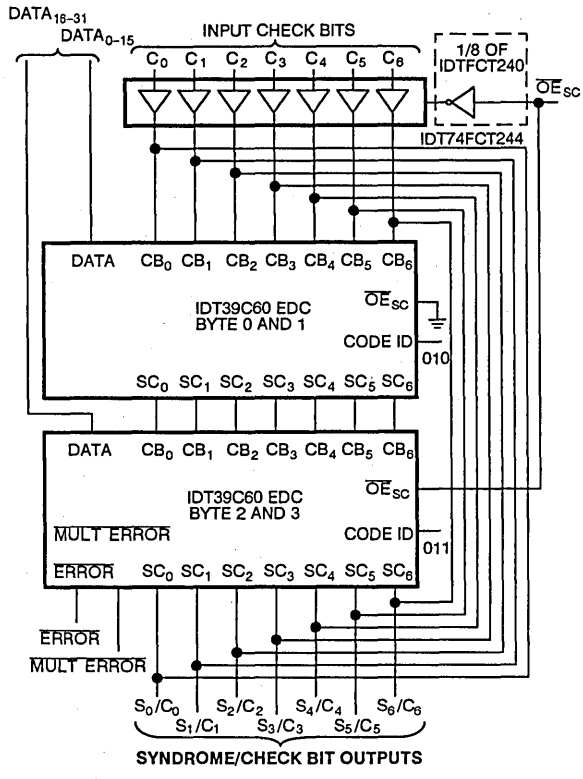


Figure 5. 32-Bit Configuration

TABLE 9. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit_0
1	Diagnostic Check Bit_1
2	Diagnostic Check Bit_2
3	Diagnostic Check Bit_3
4	Diagnostic Check Bit_4
5	Diagnostic Check Bit_5
6	Diagnostic Check Bit_6
7	Don't Care
8	Slice 0/1 – CODE ID_0
9	Slice 0/1 – CODE ID_1
10	Slice 0/1 – CODE ID_2
11	Slice 0/1 – DIAG $MODE_0$
12	Slice 0/1 – DIAG $MODE_1$
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID_0
25	Slice 2/3 – CODE ID_1
26	Slice 2/3 – CODE ID_2
27	Slice 2/3 – DIAG $MODE_0$
28	Slice 2/3 – DIAG $MODE_1$
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE 10. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC Units connected with the MSI gates, as shown in Figure 6, provide the logic needed for single bit error correction and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{ERROR}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{MULT\ ERROR}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of eight bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the Exclusive-OR gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs labeled C_0 to C_7.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal control mode substitutes the indicated bit position for the external control signals.

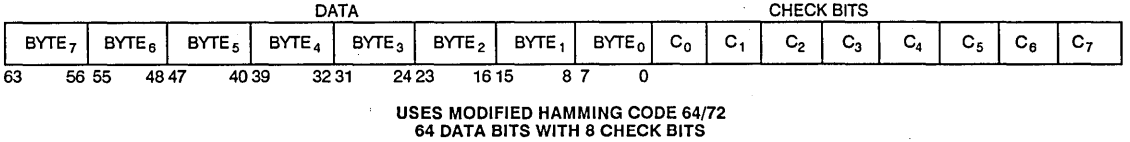


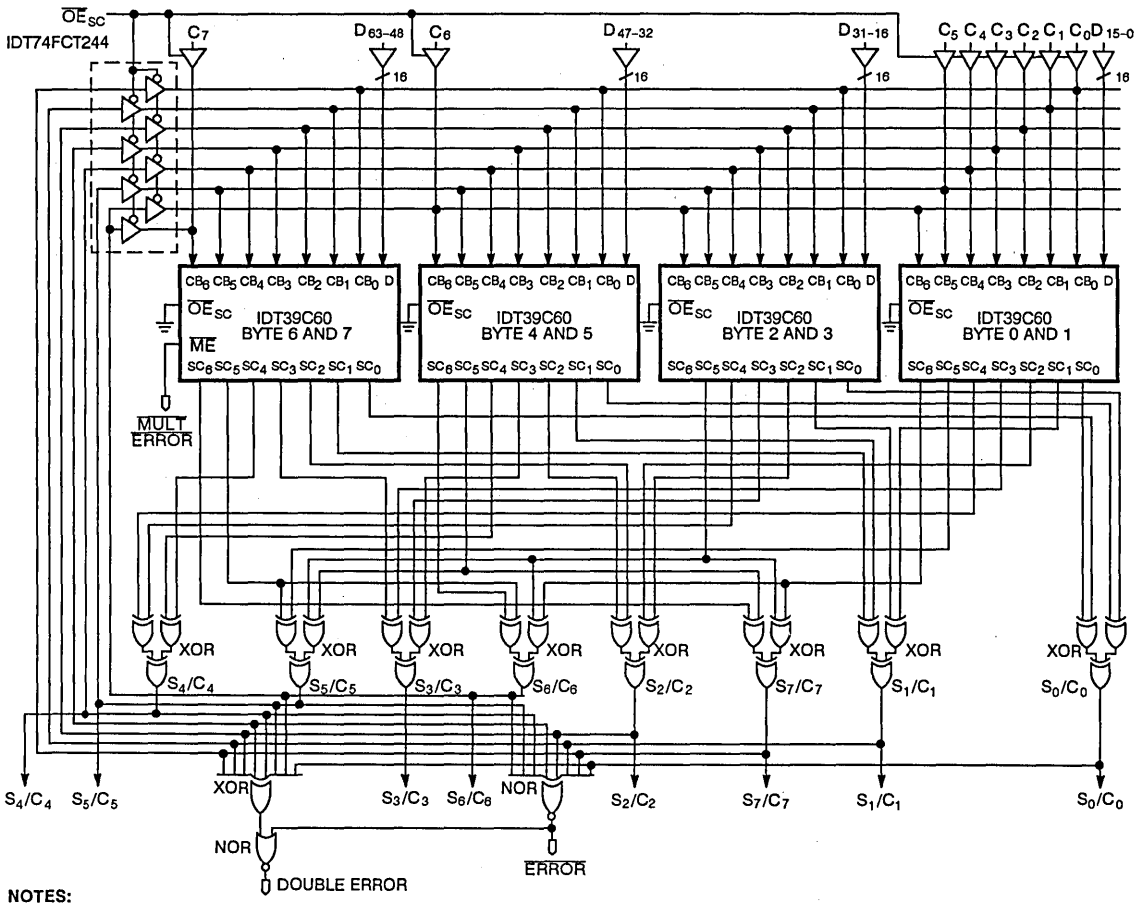
Figure 6. 64-Bit Data Format

TABLE 11. SYNDROME DECODE TO BIT-IN-ERROR (64-BIT CONFIGURATION)

	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	SYNDROME S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	BITS S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S_3 S_2 S_1 S_0																
0	0 0 0 0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0 0 0 1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0 0 1 0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0 0 1 1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0 1 0 0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0 1 0 1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0 1 1 0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0 1 1 1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1 0 0 0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1 0 0 1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1 0 1 0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1 0 1 1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1 1 0 0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1 1 0 1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1 1 1 0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1 1 1 1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTE:

* = No errors detected, T = Two errors detected, Number = The number of the single bit-in-error, M = Three or more errors detected



NOTES:

1. In PASSTHRU mode the contents of the Check Latch appear on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

TABLE 12. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer DELAY) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64-Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64-Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE 13. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART [1]

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

8

TABLE 14.
DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit $_0$
1	Diagnostic Check Bit $_1$
2	Diagnostic Check Bit $_2$
3	Diagnostic Check Bit $_3$
4	Diagnostic Check Bit $_4$
5	Diagnostic Check Bit $_5$
6, 7	Don't Care
8	Slice 0/1 – CODE ID$_0$
9	Slice 0/1 – CODE ID$_1$
10	Slice 0/1 – CODE ID$_2$
11	Slice 0/1 – DIAG MODE$_0$
12	Slice 0/1 – DIAG MODE$_1$
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID$_0$
25	Slice 2/3 – CODE ID$_1$
26	Slice 2/3 – CODE ID$_2$
27	Slice 2/3 – DIAG MODE$_0$
28	Slice 2/3 – DIAG MODE$_1$
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASSTHRU
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit$_6$
39	Don't Care
40	Slice 4/5 – CODE ID$_0$
41	Slice 4/5 – CODE ID$_1$
42	Slice 4/5 – CODE ID$_2$
43	Slice 4/5 – DIAG MODE$_0$
44	Slice 4/5 – DIAG MODE$_1$
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASSTHRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit$_7$
56	Slice 6/7 – CODE ID$_0$
57	Slice 6/7 – CODE ID$_1$
58	Slice 6/7 – CODE ID$_2$
59	Slice 6/7 – DIAG MODE$_0$
60	Slice 6/7 – DIAG MODE$_1$
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASSTHRU
63	Don't Care

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 ($S_0, S_1, S_2, S_3, S_4, S_5$) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.

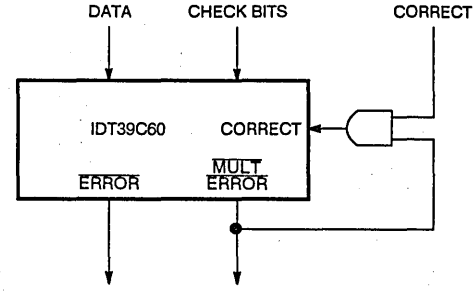


Figure 8. Inhibition of Data Modification

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

DEFINITIONS

D_i ← $DATA_i$ if LE_{IN} is HIGH or the output of bit i of the Data Input Latch if LE_{IN} is LOW
C_i ← CB_i if LE_{IN} is HIGH or the output of bit i of the Check Bit Latch if LE_{IN} is LOW
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)
PA ← $D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$
PB ← $D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$
PC ← $D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14}$
PD ← $D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$
PE ← $D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$
PF ← $D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15}$
PG_1 ← $D_1 \oplus D_4 \oplus D_6 \oplus D_7$
PG_2 ← $D_1 \oplus D_2 \oplus D_3 \oplus D_5$
PG_3 ← $D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$
PG_4 ← $D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR}$: ← $(\overline{S6} \cdot \overline{(ID_1 + ID_2)}) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU
$\overline{MULT\ ERROR}$:
(16 and 32-Bit Modes) ← $\overline{((\overline{S6} \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (ERROR)}$ + TOME + GENERATE + PASSTHRU + INITIALIZE
$\overline{MULT\ ERROR}$: (64-Bit Modes) ← TOME + GENERATE + PASSTHRU + INITIALIZE

TABLE 15. TOME (THREE OR MORE ERRORS)[1]

				HEX	0		1		2		3		4		5		6		7	
				S_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
			SYNDROME[2] BITS	S_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
HEX		S_2	S_1	S_0	S_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	8	0	0	0								1		1	1		1			1
1	9	0	0	1		1			1			1	1	1	1		1		1	1
2	A	0	1	0			1				1	1	1						1	1
3	B	0	1	1	1						1	1	1						1	1
4	C	1	0	0		1						1	1	1						1
5	D	1	0	1	1	1						1	1	1						1
6	E	1	1	0	1			1		1	1	1	1			1		1	1	
7	F	1	1	1	1			1		1	1	1	1			1		1	1	1

NOTES:

1. S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. S6 ← C6, S5 ← C5, . . . S1 ← C1, S0 ← C0.
2. The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC OUTPUTS

Tables 16, 17, 18, 19, 20 show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE 16. GENERATE MODE (Check Bits)

GENERATE MODE (CHECK BITS)	CODE ID_{2-0}						
	000	010	011	100	101	110	111
SC_0 ←	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1 ←	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
SC_2 ←	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
SC_3 ←	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
SC_4 ←	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
SC_5 ←	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
SC_6 ←	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

TABLE 17. DETECT AND CORRECT MODES (Syndromes)

DETECT AND CORRECT MODES (SYNDROMES)	CODE ID_{2-0}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 18. DIAGNOSTIC DETECT AND CORRECT MODE

DIAGNOSTIC DETECT AND CORRECT MODE	CODE ID_{2-0}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 19. DIAGNOSTIC GENERATE MODE

DIAGNOSTIC GENERATE MODE	CODE ID_{2-0}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 20. PASSTHRU MODE

PASSTHRU MODE	CODE ID_{2-0}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	C_0	C_0	CB_0	C_0	1	1	1
$SC_1 \leftarrow$	C_1	C_1	CB_1	C_1	1	1	1
$SC_2 \leftarrow$	C_2	C_2	CB_2	C_2	1	1	1
$SC_3 \leftarrow$	C_3	C_3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C_4	C_4	CB_4	C_4	1	1	1
$SC_5 \leftarrow$	C_5	C_5	CB_5	C_5	1	1	1
$SC_6 \leftarrow$	1	C_6	CB_6	1	1	C_6	C_6

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 21. CODE ID_{2-0} = 000 (1)

		S_5	0	0	0	0	1	1	1	1
		S_4	0	0	1	1	0	0	1	1
S_2	S_1	S_3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted S combinations are no correction.

TABLE 22. CODE ID_{2-0} = 010 (1)

		C_6	0	0	0	0	1	1	1	1
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted C_n combinations are no correction.

TABLE 23. CODE ID_{2-0} = 011 (1)

		S_6	0	0	0	0	1	1	1	1
		S_5	0	0	0	0	1	1	1	1
		S_4	0	0	1	1	0	0	1	1
S_2	S_1	S_3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted S combinations are no correction.

TABLE 24. CODE ID_{2-0} = 100 (1)

		C_0	0	0	0	0	1	1	1	1
		C_6	0	0	0	0	1	1	1	1
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted C_n combinations are no correction.

TABLE 25. CODE ID_{2-0} = 101 (1)

		C_0	0	0	0	0	1	1	1	1
		C_6	0	0	0	0	1	1	1	1
		C_5	0	0	0	0	1	1	1	1
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted C_n combinations are no correction.

TABLE 26. CODE ID_{2-0} = 110 (1)

		C_0	0	0	0	0	1	1	1	1
		C_6	1	1	1	1	0	0	0	0
		C_5	0	0	0	0	1	1	1	1
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		–	–	–	5	–	11	14	–
0	1		–	1	2	6	8	12	–	–
1	0		–	–	3	7	9	13	15	–
1	1		–	0	4	–	10	–	–	–

NOTE:
1. Unlisted C_n combinations are no correction.

TABLE 27. CODE ID_{2-0} = 111 (1)

		C_0	0	0	0	0	1	1	1	1
		C_6	1	1	1	1	0	0	0	0
		C_5	1	1	1	1	0	0	0	0
		C_4	0	0	1	1	0	0	1	1
C_2	C_1	C_3	0	1	0	1	0	1	0	1
0	0		–	11	14	–	–	–	–	5
0	1		8	12	–	–	–	1	2	6
1	0		9	13	15	–	–	–	3	7
1	1		10	–	–	–	–	0	4	–

NOTE:
1. Unlisted C_n combinations are no correction.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -6mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 8mA MIL.	–	0.3	0.5	
			I_{OL} = 8mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-20	–	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0		–	3.0	5.0	mA
I_{CCT}	Quiescent Input Power Supply [5] Current (per Input @ TTL High)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		–	0.3	0.5	mA/Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	5.0	8.5	mA/MHz
			COM'L.	–	5.0	7.0	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	53	90	mA
			COM'L.	–	53	75	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = 3.4V, V_{IN} = 0.4V	MIL.	–	60	100	
			COM'L.	–	60	85	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{OP} = Operating frequency

8

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUITRY

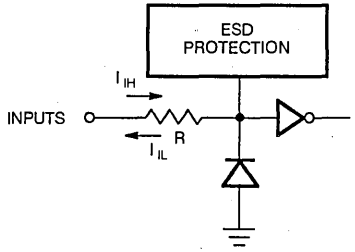


Figure 10. Input Structure (All Inputs)

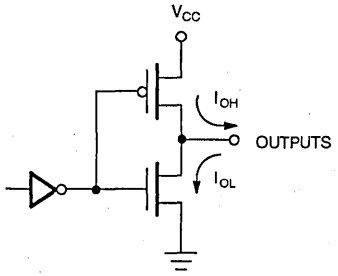
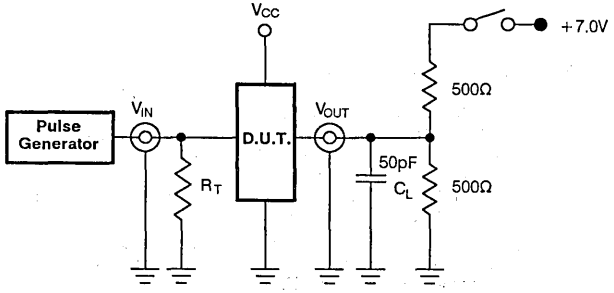


Figure 11. Output Structure

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 12

TEST LOAD CIRCUITS



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

IDT39C60B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	18	25(1)	18	20
CB_{0-6} (CODE ID_{2-0} 000, 011)	12	22	17	20
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	12	16	17	20
$\overline{GENERATE}$	13	22	12	16
CORRECT (Not Internal Control Mode)	–	17	–	–
DIAG MODE (Not Internal Control Mode)	20	22	16	19
PASSTHRU (Not Internal Control Mode)	20	22	16	19
CODE ID_{2-0}	20	22	22	24
LE_{IN} (From latched to transparent)	20	28	20	22
LE_{OUT} (From latched to transparent)	–	11	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	20	28	20	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	24	33	24	27
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	24	33	24	27

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	21	0
$\overline{GENERATE}$	LE_{OUT}	26	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
CODE ID_{2-0}	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

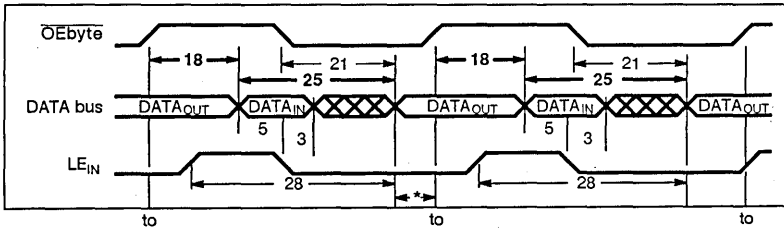
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	21	18
$\overline{OE}_{SC}$	SC_{0-6}	21	18

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	11

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 51ns (fmax = 19.6MHz)

IDT39C60B COMMERCIAL—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM TO	MIN./ MAX.
OEbyte = High to DATA out Disabled	Max.
OEbyte = Low to DATA out Enabled	Max.
DATA in to Corrected DATA out	Max.
DATA in Set-up to LE in = Low	Min.
DATA in Hold to LE in = Low	Min.
LE in = High to DATA out	Max.
* = (Memory/System dependent)	

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IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	20	30(1)	20	23
CB_{0-6} (CODE ID_{2-0} 000, 011)	14	25	20	23
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	14	18	20	23
$\overline{GENERATE}$	15	25	14	17
CORRECT (Not Internal Control Mode)	–	20	–	–
DIAG MODE (Not Internal Control Mode)	22	25	18	21
PASSTHRU (Not Internal Control Mode)	22	25	18	21
CODE ID_{2-0}	23	28	25	28
LE_{IN} (From latched to transparent)	22	32	22	25
LE_{OUT} (From latched to transparent)	–	13	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	22	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	28	38	28	31
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	28	38	28	31

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	21	0
$\overline{GENERATE}$	LE_{OUT}	26	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
CODE ID_{2-0}	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

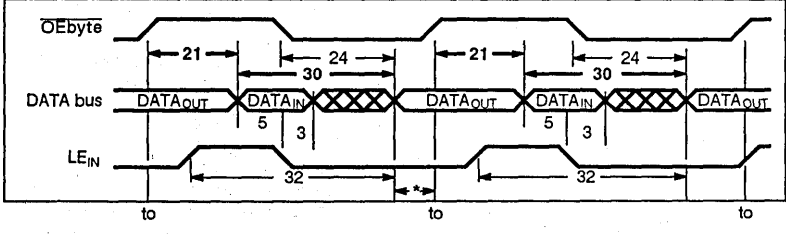
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	24	21
$\overline{OE}_{SC}$	SC_{0-6}	24	21

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 61ns (fmax = 16.4MHz)

IDT39C60A COMMERCIAL—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM	TO	MIN./ MAX.
OEbyte = High to DATA out Disabled		Max.
OEbyte = Low to DATA out Enabled		Max.
DATA in to Corrected DATA out		Max.
DATA in Set-up to LE in = Low		Min.
DATA in Hold to LE in = Low		Min.
LE in = High to DATA out		Max.
* = (Memory/System dependent)		

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	22	35(1)	24	27
CB_{0-6} (CODE ID_{2-0} 000, 011)	17	28	24	27
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	17	20	24	27
$\overline{GENERATE}$	20	28(2)	18	21
CORRECT (Not Internal Control Mode)	–	25	–	–
DIAG MODE (Not Internal Control Mode)	25	28	21	24
PASSTHRU (Not Internal Control Mode)	25	28	21	24
CODE ID_{2-0}	26	31	28	31
LE_{IN} (From latched to transparent)	24	37	26	29
LE_{OUT} (From latched to transparent)	–	16	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	37(2)	26	29
Internal Control Mode: LE_{DIAG} (From latched to transparent)	30	43(2)	32	35
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	30	43(2)	32	35

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	27	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	24	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	24	0
$\overline{GENERATE}$(2)	LE_{OUT}	29	0
CORRECT	LE_{OUT}	25	0
DIAG MODE	LE_{OUT}	25	0
PASSTHRU	LE_{OUT}	25	0
CODE ID_{2-0}	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	30	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

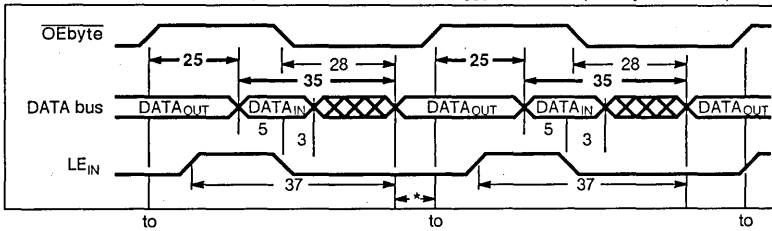
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	28	25
$\overline{OE}_{SC}$	SC_{0-6}	28	25

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 70ns (fmax = 14.3MHz)

IDT39C60A MILITARY—DATA $_{IN}$ TO CORRECTED DATA $_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM	TO	MIN./ MAX.
OEbyte = High to DATA out Disabled		Max.
OEbyte = Low to DATA out Enabled		Max.
DATA in to Corrected DATA out		Max.
DATA in Set-up to LE in = Low		Min.
DATA in Hold to LE in = Low		Min.
LE in = High to DATA out		Max.
* = (Memory/System dependent)		

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52(1)	25	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	23	50	23	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	34	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
$CODE\ ID_{2-0}$	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	–	31	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	34	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
$CODE\ ID_{2-0}$	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

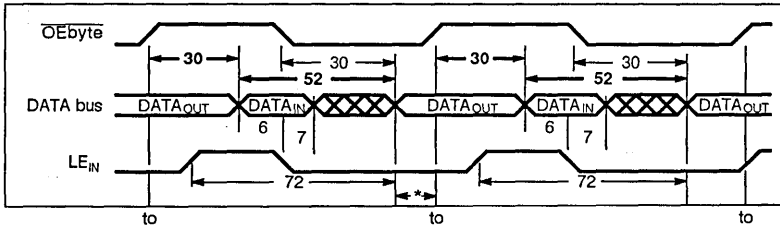
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 92ns (fmax = 10.9MHz)

IDT39C60-1 COMMERCIAL—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM	TO	MIN./ MAX.
OEbyte = High to DATA out Disabled		Max.
OEbyte = Low to DATA out Enabled		Max.
DATA in to Corrected DATA out		Max.
DATA in Set-up to LE in = Low		Min.
DATA in Hold to LE in = Low		Min.
LE in = High to DATA out		Max.
* = (Memory/System dependent)		

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the military operating range of -55°C to + 125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

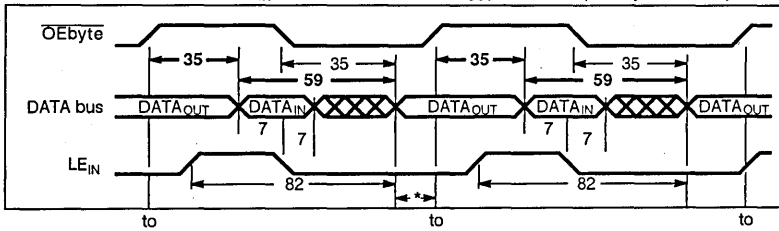
C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	31	59(1)	28	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	25	55	25	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	38	31	37
$\overline{GENERATE}$	38	69(2)	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	39	82	43	66
LE_{OUT} (From latched to transparent)	–	33	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88(2)	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106(2)	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106(2)	74	96

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

IDT39C60-1 MILITARY—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 104ns (fmax = 9.6MHz)

TIMING PARAMETER FROM	TO	MIN./ MAX.
OEbyte = High to DATA out Disabled		Max.
OEbyte = Low to DATA out Enabled		Max.
DATA in to Corrected DATA out		Max.
DATA in Set-up to LE in = Low		Min.
DATA in Hold to LE in = Low		Min.
LE in = High to DATA out		Max.
* = (Memory/System dependent)		

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	39	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	30	0
$\overline{GENERATE}$ (2)	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65(1)	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	–	31	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	44	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

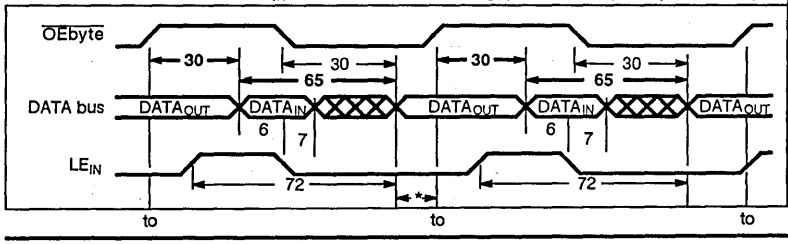
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 105ns (fmax = 9.5MHz)

IDT39C60 COMMERCIAL—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM	TO	MIN./ MAX.
OEbyte = High	to DATA out Disabled	Max.
OEbyte = Low	to DATA out Enabled	Max.
DATA in	to Corrected DATA out	Max.
DATA in Set-up	to LE in = Low	Min.
DATA in Hold	to LE in = Low	Min.
LE in = High	to DATA out	Max.

* = (Memory/System dependent)

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	ERROR	MULT ERROR
$DATA_{0-15}$	35	73(1)	36	56
CB_{0-6} ($CODE\ ID_{2-0}$ 000, 011)	30	61	31	50
CB_{0-6} ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	69(2)	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
$CODE\ ID_{2-0}$	69	100	68	90
LE_{IN} (From latched to transparent)	44	82	43	66
LE_{OUT} (From latched to transparent)	–	33	–	–
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88(2)	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106(2)	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106(2)	74	96

NOTE:

1. $DATA_{IN}$ to Corrected $DATA_{OUT}$ measurement requires timing as shown below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	50	5
CB_{0-6} ($CODE\ ID$ 000, 011)	LE_{OUT}	38	0
CB_{0-6} ($CODE\ ID$ 010, 100, 101, 110, 111)	LE_{OUT}	30	0
$\overline{GENERATE}$ (2)	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
$CODE\ ID_{2-0}$	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

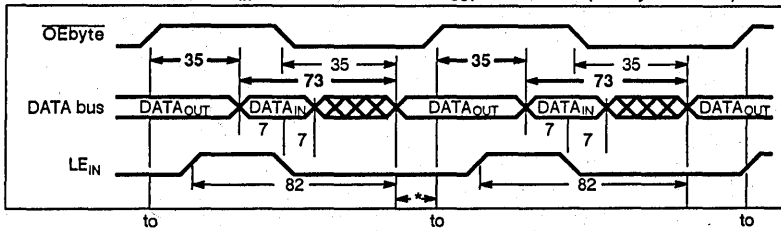
INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

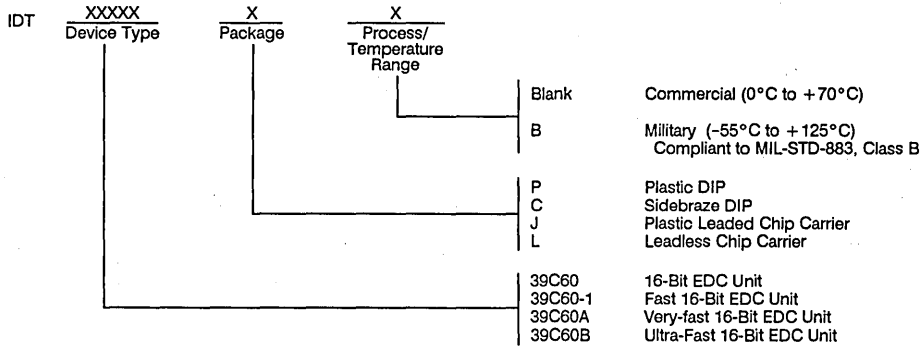
NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 118ns (fmax = 8.5MHz)

IDT39C60 MILITARY—$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ TIMING (Two cycles shown)



TIMING PARAMETER FROM TO	MIN./ MAX.
OEbyte = High to DATA out Disabled	Max.
OEbyte = Low to DATA out Enabled	Max.
DATA in to Corrected DATA out	Max.
DATA in Set-up to LE in = Low	Min.
DATA in Hold to LE in = Low	Min.
LE in = High to DATA out	Max.
* = (Memory/System dependent)	

ORDERING INFORMATION



Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT 49C460
IDT 49C460A
IDT 49C460B
IDT 49C460C

FEATURES:

- Fast

	Detect	Correct
– IDT49C460C	16ns (max.)	24ns (max.)
– IDT49C460B	25ns (max.)	30ns (max.)
– IDT49C460A	30ns (max.)	36ns (max.)
– IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - – Commercial: 95mA (max.)
  - – Military: 125mA (max.)
- Improves system memory reliability
  - – Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - – Data words up to 64-bits
- Built-in diagnostics
  - – Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - – Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, PPGA, LCC, PLCC and Ceramic Quad Flat-pack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

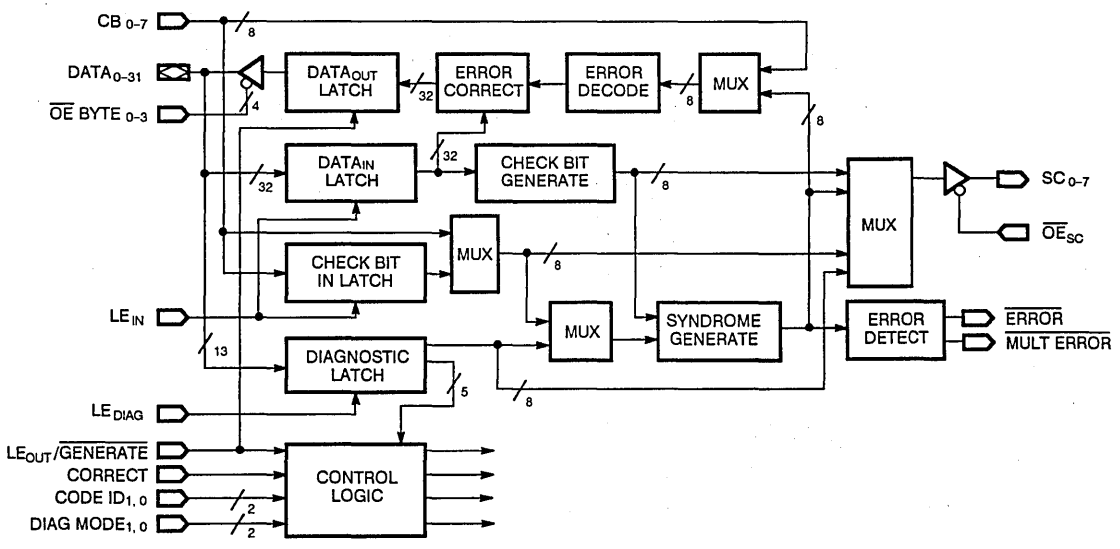
The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, both ceramic and plastic, LCC (25 mil and 50 mil centers), PLCC and Ceramic Quad Flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

8

FUNCTIONAL BLOCK DIAGRAM



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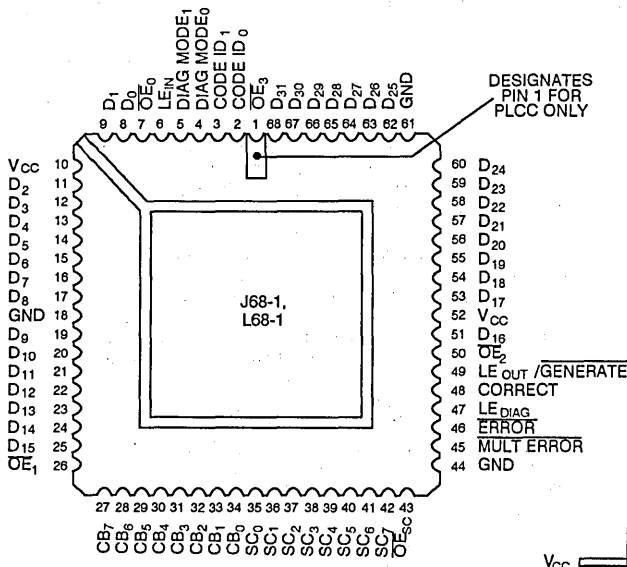
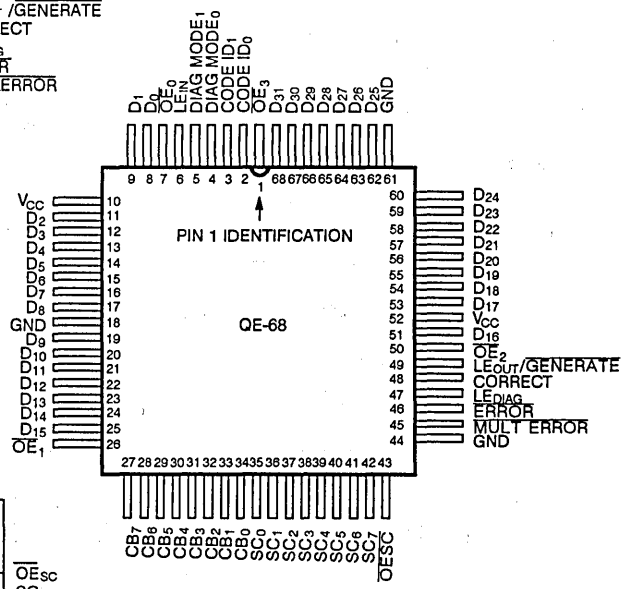
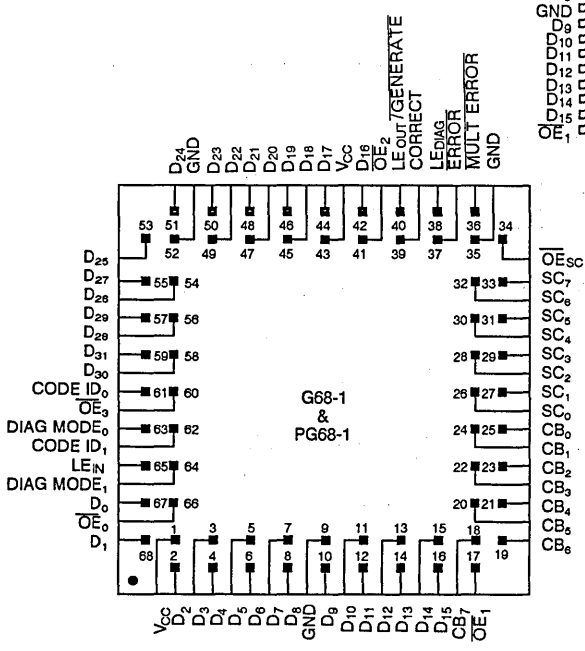
PIN CONFIGURATION



PLCC/LCC
TOP VIEW



CERQUAD
TOP VIEW



PGA
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-31}$	I/O	32 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines. Used to input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
$\overline{LE_{OUT}}$/ $\overline{GENERATE}$	I	A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE_{SC}}$	I	Output Enable – Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT\ ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}$ $BYTE_{0-3}$	I	Output Enable – Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
$DIAG\ MODE_{1,0}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
$CODE\ ID_{1,0}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special $CODE\ ID_{1,0}$ input 01 is also used to instruct the EDC that the signals $CODE\ ID_{1,0}$, $DIAG\ MODE_{1,0}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for $CODE\ ID_{1,0}$, $DIAG\ MODE_{1,0}$ and CORRECT.

EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH:

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in another byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT INPUT LATCH:

Eight check bits are loaded under control of LE_{IN}. Check bits are used in the Error Detection and Error Correction modes.

CHECK BIT GENERATION LOGIC:

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC:

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits means the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC:

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are HIGH. $\overline{ERROR}$ will go low if one error is detected. $\overline{MULT\ ERROR}$ and $\overline{ERROR}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC:

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS:

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch in the PASSTHRU mode. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH:

The diagnostic latch is loadable, under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC:

Specifies what mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{GENERATE}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

WORD SIZE SELECTION:

The 2 code identification pins, CODE $ID_{1,0}$ are used to determine the data word size that is 32 or 64 bits. Table 5 defines all possible slice identification codes. They also select the Internal Control Mode.

CHECK AND SYNDROME BITS:

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

$C_0, C_1, C_2, C_3, C_4, C_5, C_6$ for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

TABLE 2.
DIAGNOSTIC MODE CONTROL

CORRECT	DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

TABLE 3.
IDT49C460 OPERATING MODES

OPERATING MODE	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	DATA OUT LATCH	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ / $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW(1)	Check Bits Generated from Data In Latch	High
Detect	0 0	0 1	1	0	Data In Latch	Syndrome Bits Data In/ Check Bit Latch	Error Dep(2)
Correct	0 0	0 1	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	Data In Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	–	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	Data In Latch	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	1	1	Data In Latch set to 0000	–	–
Internal Mode	CODE $ID_{1,0}$ = 01 (Control Signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$, and CORRECT are taken from Diagnostic Latch.)						

NOTES:

1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the Data Out Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate), does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

8

OPERATING MODE SELECTION:

Tables 2 and 3 describe the 9 operating modes of the IDT49C460s. The Diagnostic Mode pins—DIAG $MODE_{0,1}$—define four basic areas of operation. $\overline{GENERATE}$ and CORRECT further divide operation into 8 functions, with CODE $ID_{1,0}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC_{0-7}. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs $\overline{ERROR}$ and $\overline{MULT\ ERROR}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-7}. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG $MODE_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even CODE $ID_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

TABLE 5. SLICE IDENTIFICATION

CODE ID_1	CODE ID_0	SLICE SELECTED
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0-31)
1	1	64-Bit, Upper 32-Bit (32-63)

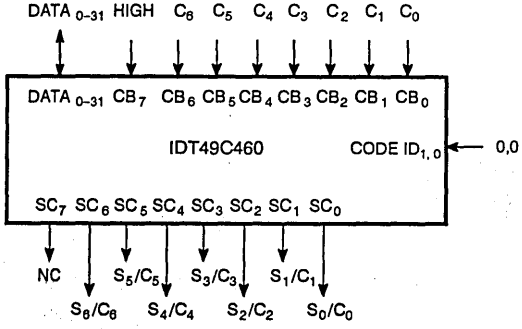


Figure 1. 32-Bit Configuration

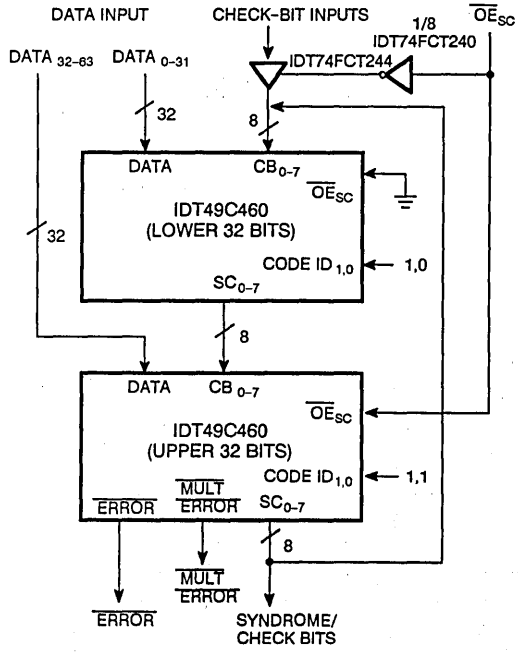


Figure 2. 64-Bit Configuration

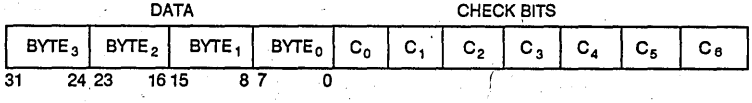


Figure 3. 32-Bit Data Format

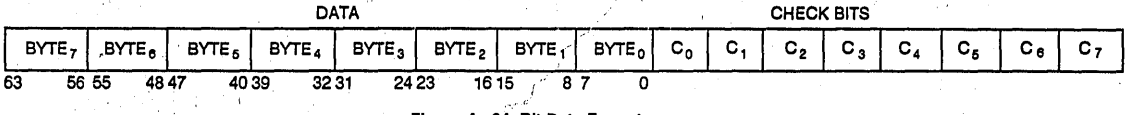


Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION:

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the Pass Thru or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 4 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

TABLE 4. 32-BIT DIAGNOSTIC LATCH CODING FORMAT

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13-31	DON'T CARE

TABLE 6. 32-BIT MODIFIED HAMMING CODE—CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

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TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR (32-BIT)

					HEX	0	1	2	3	4	5	6	7
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

64-BIT DATA WORD CONFIGURATION:

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error correction and double bit error detection of a 64-bit data field. Table 5 gives the CODE $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE $ID_{1,0}$ = 11. Control signals not indicated are connected to both units in parallel. The EDC with the CODE $ID_{1,0}$ = 10 has the $\overline{OE}_{SC}$ grounded. The $\overline{OE}_{SC}$ selects the syndrome bits from the EDC with CODE $ID_{1,0}$ = 11 and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE $ID_{1,0}$ = 10, while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE $ID_{1,0}$ = 11.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE $ID_{1,0}$ = 10 through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the upper EDC unit to the lower EDC unit. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function or the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

TABLE 8A.
64-BIT DIAGNOSTIC LATCH-CODING FORMAT (DIAGNOSTIC DETECT AND CORRECT MODE)

BIT	INTERNAL FUNCTION
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32-39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

TABLE 8B.
64-BIT DIAGNOSTIC LATCH—CODING FORMAT (DIAGNOSTIC GENERATE MODE)

BIT	INTERNAL FUNCTION
0-7	DON'T CARE
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

TABLE 9. SYNDROME DECODE TO BIT-IN-ERROR (64-BIT CONFIGURATION)

					HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:

* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

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TABLE 10.
KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FOR IDT49C460 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected DATA Out	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

TABLE 11. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODING

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

SC OUTPUTS

The tables below indicate how the SC_{0-7} outputs are generated in each control mode for various CODE IDs (Internal Control Mode not applicable).

GENERATE	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0	PH1	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA	PA	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB	PB	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC	PC	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD	PD	PD $\oplus$ CB_4
$SC_5 \leftarrow$	PE	PE	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF	PF	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF	PG $\oplus$ CB_7
	FINAL CHECK BITS	PARTIAL CHECK BITS	FINAL CHECK BITS

CORRECT/ DETECT	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0 $\oplus$ C0	PH1 $\oplus$ C0	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA $\oplus$ C1	PA $\oplus$ C1	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB $\oplus$ C2	PB $\oplus$ C2	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC $\oplus$ C3	PC $\oplus$ C3	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD $\oplus$ C4	PD $\oplus$ C4	PC $\oplus$ CB_4
$SC_5 \leftarrow$	PE $\oplus$ C5	PE $\oplus$ C5	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF $\oplus$ C6	PF $\oplus$ C6	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF $\oplus$ C7	PG $\oplus$ CB_7
	FINAL SYNDROME	PARTIAL SYNDROME	FINAL SYNDROME

DIAGNOSTIC GENERATE	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	DL0	DL0	DL32
$SC_1 \leftarrow$	DL1	DL1	DL33
$SC_2 \leftarrow$	DL2	DL2	DL34
$SC_3 \leftarrow$	DL3	DL3	DL35
$SC_4 \leftarrow$	DL4	DL4	DL36
$SC_5 \leftarrow$	DL5	DL5	DL37
$SC_6 \leftarrow$	DL6	DL6	DL38
$SC_7 \leftarrow$	–	DL7	DL39
	FINAL CHECK BITS	PARTIAL CHECK BITS	FINAL CHECK BITS

DIAGNOSTIC CORRECT/ DETECT	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	PH0 $\oplus$ DL0	PH1 $\oplus$ DL0	PH2 $\oplus$ CB_0
$SC_1 \leftarrow$	PA $\oplus$ DL1	PA $\oplus$ DL1	PA $\oplus$ CB_1
$SC_2 \leftarrow$	PB $\oplus$ DL2	PB $\oplus$ DL2	PB $\oplus$ CB_2
$SC_3 \leftarrow$	PC $\oplus$ DL3	PC $\oplus$ DL3	PC $\oplus$ CB_3
$SC_4 \leftarrow$	PD $\oplus$ DL4	PD $\oplus$ DL4	PD $\oplus$ CB_4
$SC_5 \leftarrow$	PE $\oplus$ DL5	PE $\oplus$ DL5	PE $\oplus$ CB_5
$SC_6 \leftarrow$	PF $\oplus$ DL6	PF $\oplus$ DL6	PF $\oplus$ CB_6
$SC_7 \leftarrow$	–	PF $\oplus$ DL7	PG $\oplus$ CB_7
	FINAL SYNDROME	PARTIAL SYNDROME	FINAL SYNDROME

PASSTHRU	CODE $ID_{1,0}$		
	00	10	11
$SC_0 \leftarrow$	C0	C0	CB_0
$SC_1 \leftarrow$	C1	C1	CB_1
$SC_2 \leftarrow$	C2	C2	CB_2
$SC_3 \leftarrow$	C3	C3	CB_3
$SC_4 \leftarrow$	C4	C4	CB_4
$SC_5 \leftarrow$	C5	C5	CB_5
$SC_6 \leftarrow$	C6	C6	CB_6
$SC_7 \leftarrow$	–	C7	CB_7

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE $ID_{1, 0}$ position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

SYNDROME DECODE TO BIT CORRECTED (32-BIT CONFIGURATION) CODE ID $_{1-0}$ = 00

					HEX	0	1	2	3	4	5	6	7
					S_6	0	0	0	0	1	1	1	1
	SYNDROME BITS				S_5	0	0	1	1	0	1	1	1
					S_4	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0									
0	0	0	0	0		–	–	–	–	–	–	–	30
1	0	0	0	1		–	–	–	14	–	–	–	–
2	0	0	1	0		–	–	–	–	–	2	24	–
3	0	0	1	1		–	18	8	–	–	–	–	–
4	0	1	0	0		–	–	–	15	–	3	25	–
5	0	1	0	1		–	19	9	–	–	–	–	31
6	0	1	1	0		–	20	10	–	–	–	–	–
7	0	1	1	1		–	–	–	–	–	4	26	–
8	1	0	0	0		–	–	–	–	–	5	27	–
9	1	0	0	1		–	21	11	–	–	–	–	–
A	1	0	1	0		–	22	12	–	1	–	–	–
B	1	0	1	1		17	–	–	–	–	6	28	–
C	1	1	0	0		–	23	13	–	–	–	–	–
D	1	1	0	1		–	–	–	–	–	7	29	–
E	1	1	1	0		16	–	–	–	–	–	–	–
F	1	1	1	1		–	–	–	–	0	–	–	–

NOTE:
1. S_7 = 1 in CODE $ID_{1,0}$ = 00

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

PA = D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D20 ⊕ D22 ⊕ D24 ⊕ D26 ⊕ D28

PB = D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D19 ⊕ D20 ⊕ D23 ⊕ D25 ⊕ D26 ⊕ D29 ⊕ D31

PC = D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D16 ⊕ D17 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D27 ⊕ D28 ⊕ D29

PD = D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D30 ⊕ D31

PE = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PF = D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PG = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23

PH0 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

PH1 = D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30

PH2 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D10 ⊕ D12 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D20 ⊕ D22 ⊕ D23 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

SYNDROME DECODE TO BIT CORRECTED (64-BIT CONFIGURATION)

					HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	SYNDROME BITS				S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	–	C6	–	–	62	C7	–	–	46	–	–	–	–
1	0	0	0	1		C0	–	–	14	–	–	–	–	–	–	–	–	–	–	–	30
2	0	0	1	0		C1	–	–	–	–	34	56	–	–	50	40	–	–	–	–	–
3	0	0	1	1		–	18	8	–	–	–	–	–	–	–	–	–	–	2	24	–
4	0	1	0	0		C2	–	–	15	–	35	57	–	–	51	41	–	–	–	–	31
5	0	1	0	1		–	19	9	–	–	–	–	63	–	–	–	47	–	3	25	–
6	0	1	1	0		–	20	10	–	–	–	–	–	–	–	–	–	–	4	26	–
7	0	1	1	1		–	–	–	–	–	36	58	–	–	52	42	–	–	–	–	–
8	1	0	0	0		C3	–	–	–	–	37	59	–	–	53	43	–	–	–	–	–
9	1	0	0	1		–	21	11	–	–	–	–	–	–	–	–	–	–	5	27	–
A	1	0	1	0		–	22	12	–	33	–	–	–	49	–	–	–	–	6	28	–
B	1	0	1	1		17	–	–	–	–	38	60	–	–	54	44	–	1	–	–	–
C	1	1	0	0		–	23	13	–	–	–	–	–	–	–	–	–	–	7	29	–
D	1	1	0	1		–	–	–	–	–	39	61	–	–	55	45	–	–	–	–	–
E	1	1	1	0		16	–	–	–	–	–	–	–	–	–	–	–	0	–	–	–
F	1	1	1	1		–	–	–	–	32	–	–	–	48	–	–	–	–	–	–	–

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level[4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level[4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5.0	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10.0	µA
			V_O = V_{CC} (Max.)	–	0.1	10.0	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V[3]		-30.0	–	–	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

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DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{OP} = 0		–	3.0	5	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)(5)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	6	10	mA/ MHz
			COM'L.	–	6	7	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	–	60	110	mA
			COM'L.	–	60	80	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	70	125	
			COM'L.	–	70	95	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency in Megahertz.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq$ 0V and $V_{IH} \geq$ 3V for AC tests.

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460C over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT	TO OUTPUT				UNITS
		SC_{0-7}	$DATA_{0-31}$	ERROR	MULT ERROR	
	$DATA_{0-31}$	19	24	16	20	ns
	CB_{0-7} (CODE ID 00, 11)	14	21	12	16	ns
	CB_{0-7} (CODE ID 10)	14	16	19	21	ns
	LE_{OUT}/GENERATE ↗	–	12	↘ 18	↘ 18	ns
	LE_{OUT}/GENERATE ↘	18	–	↗ 18	↗ 18	ns
	CORRECT Not Internal Control Mode	–	16	–	–	ns
	DIAG MODE Not Internal Control Mode	16	26	16	20	ns
	$CODE\ ID_{1,0}$	18	23	17	21	ns
	LE_{IN} ↗ From latched to transparent	22	28	24	22	ns
	LE_{DIAG} ↗ From latched to transparent; Not Internal Control Mode	15	24	15	19	ns
Internal Control Mode	LE_{DIAG} ↗ From latched to transparent	16	22	15	18	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	15	25	13	16	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)	SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$	↘	LE_{IN}	3	4	ns
CB_{0-7}	↘	LE_{IN}	2	4	ns
$DATA_{0-31}$	↘	LE_{OUT}/GENERATE	6	0	ns
CB_{0-7} (CODE ID 00, 11)	↘	LE_{OUT}/GENERATE	14	0	ns
CB_{0-7} (CODE ID 10)	↘	LE_{OUT}/GENERATE	8	0	ns
CORRECT ↗	↘	LE_{OUT}/GENERATE	8	–	ns
DIAG MODE	↘	LE_{OUT}/GENERATE	17	0	ns
$CODE\ ID_{1,0}$	↘	LE_{OUT}/GENERATE	10	0	ns
LE_{IN} ↗	↘	LE_{OUT}/GENERATE	19	–	ns
$DATA_{0-31}$		LE_{DIAG}	3	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ $BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	6		ns

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IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT								UNITS
			SC_{0-7}		$DATA_{0-31}$		$\overline{ERROR}$		$\overline{MULT\ ERROR}$		
	$DATA_{0-31}$		25		30		25		27		ns
	CB_{0-7} (CODE ID 00, 11)		14		30		17		20		ns
	CB_{0-7} (CODE ID 10)		16		18		19		21		ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–		12		↘	23	↘	23	ns
		↘	21		–		↗	23	↗	23	ns
	CORRECT Not Internal Control Mode		–		23		–		–		ns
	DIAG MODE Not Internal Control Mode		17		26		20		24		ns
	$CODE\ ID_{1,0}$		18		26		21		26		ns
	LE_{IN} From latched to transparent	↗	27		38		30		3		ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	15		29		19		22		ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	16		32		19		24		ns
	$DATA_{0-31}$ Via Diagnostic Latch		16		32		20		25		ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	4	4	ns
CB_{0-7}		↘	LE_{IN}	4	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	11	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	20	–	ns
$DATA_{0-31}$			LE_{DIAG}	4	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT			TO OUTPUT	ENABLE		DISABLE		UNITS
	ENABLE	DISABLE		MIN.	MAX.	MIN.	MAX.	
$\overline{OE}\ BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	9		ns

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460B over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT								UNITS
			SC_{0-7}		$DATA_{0-31}$		$\overline{ERROR}$		$\overline{MULT\ ERROR}$		
	$DATA_{0-31}$		28		33		28		30		ns
	CB_{0-7} (CODE ID 00, 11)		17		33		20		23		ns
	CB_{0-7} (CODE ID 10)		19		23		22		24		ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–		15	↘	26	↘	26		ns
		↘	24		–	↗	26	↗	26		ns
	CORRECT Not Internal Control Mode		–		26		–		–		ns
	DIAG MODE Not Internal Control Mode		20		29		23		27		ns
	$CODE\ ID_{1,0}$		21		29		24		29		ns
	LE_{IN} From latched to transparent	↗	30		41		33		36		ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	18		32		22		25		ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	19		35		22		27		ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		19		35		23		28		ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	4	4	ns
CB_{0-7}		↘	LE_{IN}	4	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	14	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	23	–	ns
$DATA_{0-31}$			LE_{DIAG}	4	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT			TO OUTPUT	ENABLE		DISABLE		UNITS
	ENABLE	DISABLE		MIN.	MAX.	MIN.	MAX.	
$\overline{OE}\ BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	25	10	21	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	27	10	22	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

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IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT ERROR	TO OUTPUT MULT ERROR	UNITS
	$DATA_{0-31}$		27	36	30	33	ns
	CB_{0-7} (CODE ID 00, 11)		16	34	19	23	ns
	CB_{0-7} (CODE ID 10)		16	20	19	21	ns
	LE_{OUT}/GENERATE	↗	–	12	↘ 25	↘ 25	ns
		↘	21	–	↗ 25	↗ 25	ns
	CORRECT Not Internal Control Mode		–	23	–	–	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	$CODE\ ID_{1,0}$		18	26	21	26	ns
	LE_{IN} From latched to transparent	↗	27	38	30	33	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	15	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	16	32	29	24	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		16	32	20	25	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	5	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	LE_{OUT}/GENERATE	23	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	LE_{OUT}/GENERATE	15	0	ns
CB_{0-7} (CODE ID 10)		↘	LE_{OUT}/GENERATE	15	0	ns
CORRECT	↗	↘	LE_{OUT}/GENERATE	11	–	ns
DIAG MODE		↘	LE_{OUT}/GENERATE	17	0	ns
$CODE\ ID_{1,0}$		↘	LE_{OUT}/GENERATE	17	0	ns
LE_{IN}	↗	↘	LE_{OUT}/GENERATE	25	–	ns
$DATA_{0-31}$			LE_{DIAG}	5	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ $BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	23	10	19	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	24	10	20	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	9		ns

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT $\overline{ERROR}$	TO OUTPUT $\overline{MULT\ ERROR}$	UNITS
	$DATA_{0-31}$		30	39	33	36	ns
	CB_{0-7} (CODE ID 00, 11)		19	37	22	26	ns
	CB_{0-7} (CODE ID 10)		19	23	22	24	ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–	15	↘ 28	↘ 28	ns
		↘	24	–	↗ 28	↗ 28	ns
	CORRECT Not Internal Control Mode		–	26	–	–	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	$CODE\ ID_{1,0}$		21	29	24	29	ns
	LE_{IN} From latched to transparent	↗	30	41	33	36	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	18	32	22	25	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	19	35	22	27	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		19	35	23	28	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	5	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	27	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	14	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	28	–	ns
$DATA_{0-31}$			LE_{DIAG}	5	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ BYTE$_{0-3}$	↘	↗	$DATA_{0-31}$	10	25	10	21	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	27	10	22	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT SC_{0-7}	TO OUTPUT $DATA_{0-31}$	TO OUTPUT ERROR	TO OUTPUT MULT ERROR	UNITS
	$DATA_{0-31}$		37	49	40	45	ns
	CB_{0-7} (CODE ID 00, 11)		22	46	26	31	ns
	CB_{0-7} (CODE ID 10)		22	30	26	29	ns
	LE_{OUT}/GENERATE	↗	–	17	↘ 30	↘ 30	ns
		↘	29	–	↗ 30	↗ 30	ns
	CORRECT Not Internal Control Mode		–	31	–	–	ns
	DIAG MODE Not Internal Control Mode		23	35	27	33	ns
	$CODE\ ID_{1,0}$		25	35	29	35	ns
	LE_{IN} From latched to transparent	↗	37	51	41	45	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	21	38	26	30	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	22	42	26	33	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		22	42	27	34	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	6	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	LE_{OUT}/GENERATE	30	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	LE_{OUT}/GENERATE	20	0	ns
CB_{0-7} (CODE ID 10)		↘	LE_{OUT}/GENERATE	20	0	ns
CORRECT	↗	↘	LE_{OUT}/GENERATE	16	–	ns
DIAG MODE		↘	LE_{OUT}/GENERATE	23	0	ns
$CODE\ ID_{1,0}$		↘	LE_{OUT}/GENERATE	23	0	ns
LE_{IN}	↗	↘	LE_{OUT}/GENERATE	31	–	ns
$DATA_{0-31}$			LE_{DIAG}	6	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ $BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	27	10	23	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	28	10	24	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	12		ns

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

PROPAGATION DELAYS C_L = 50pF.

	FROM INPUT		TO OUTPUT				UNITS
			SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$	
	$DATA_{0-31}$		40	52	44	48	ns
	CB_{0-7} (CODE ID 00, 11)		25	49	29	34	ns
	CB_{0-7} (CODE ID 10)		25	33	29	32	ns
	$LE_{OUT}/\overline{GENERATE}$	↗	–	20	↘ 33	↘ 33	ns
		↘	32	–	↗ 33	↗ 33	ns
	CORRECT Not Internal Control Mode		–	34	–	–	ns
	DIAG MODE Not Internal Control Mode		26	38	30	36	ns
	$CODE\ ID_{1,0}$		28	38	32	38	ns
	LE_{IN} From latched to transparent	↗	40	54	44	48	ns
	LE_{DIAG} From latched to transparent; Not Internal Control Mode	↗	24	42	29	33	ns
Internal Control Mode	LE_{DIAG} From latched to transparent	↗	25	47	29	36	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch		25	47	30	37	ns

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT		TO (LATCHING DATA)		SET-UP TIME MIN.	HOLD TIME MIN.	UNITS
$DATA_{0-31}$		↘	LE_{IN}	6	4	ns
CB_{0-7}		↘	LE_{IN}	5	4	ns
$DATA_{0-31}$		↘	$LE_{OUT}/\overline{GENERATE}$	36	0	ns
CB_{0-7} (CODE ID 00, 11)		↘	$LE_{OUT}/\overline{GENERATE}$	24	0	ns
CB_{0-7} (CODE ID 10)		↘	$LE_{OUT}/\overline{GENERATE}$	24	0	ns
CORRECT	↗	↘	$LE_{OUT}/\overline{GENERATE}$	20	–	ns
DIAG MODE		↘	$LE_{OUT}/\overline{GENERATE}$	28	0	ns
$CODE\ ID_{1,0}$		↘	$LE_{OUT}/\overline{GENERATE}$	28	0	ns
LE_{IN}	↗	↘	$LE_{OUT}/\overline{GENERATE}$	37	–	ns
$DATA_{0-31}$			LE_{DIAG}	6	3	ns

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

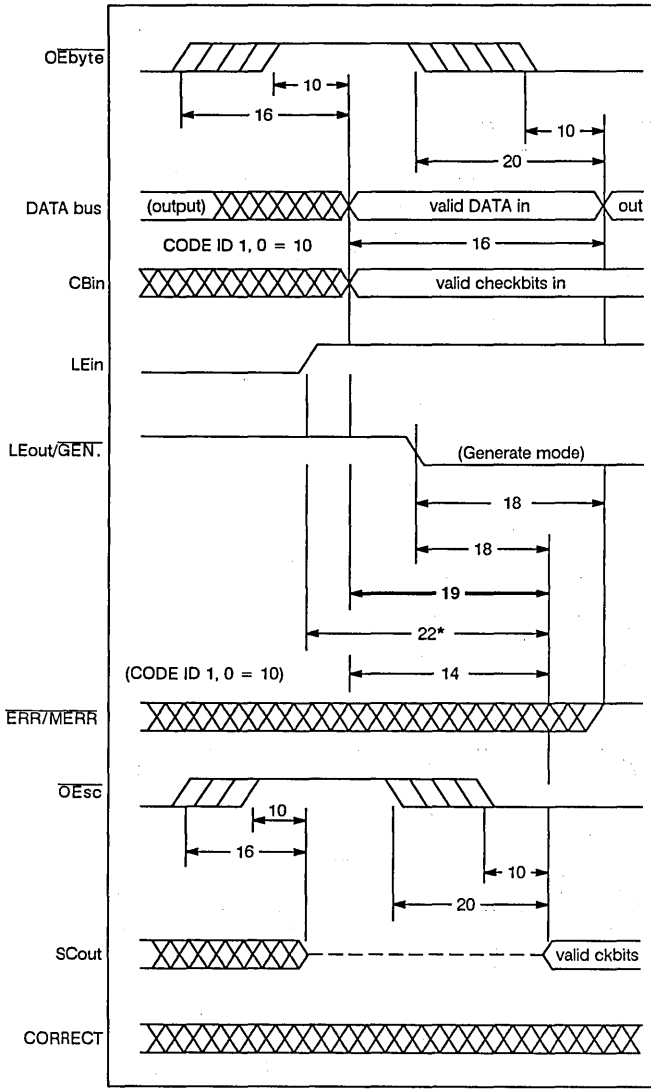
FROM INPUT	ENABLE	DISABLE	TO OUTPUT	ENABLE MIN.	ENABLE MAX.	DISABLE MIN.	DISABLE MAX.	UNITS
$\overline{OE}$ $BYTE_{0-3}$	↘	↗	$DATA_{0-31}$	10	29	10	25	ns
$\overline{OE}_{SC}$	↘	↗	SC_{0-7}	10	30	10	26	ns

MINIMUM PULSE WIDTHS

	MIN.		
LE_{IN}, LE_{OUT}, LE_{DIAG}	15		ns

**IDT49C460C TIMING:
DATA SHEET PARAMETERS**

GENERATE Mode
(from DETECT or CORRECT Mode)



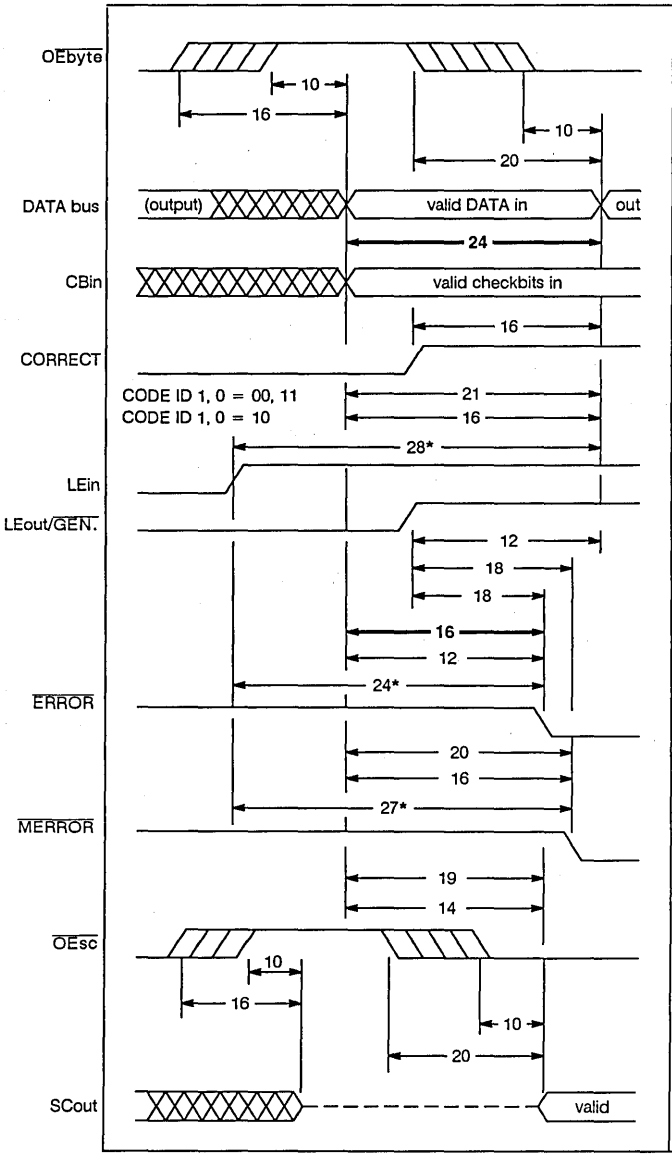
PROPAGATION DELAY FROM	TO	MIN./MAX.
$\overline{OEbyte}$	= High to DATA out Disabled	Min.
$\overline{OEbyte}$	= High to DATA out Disabled	Max.
$\overline{OEbyte}$	= Low to DATA out Enabled	Min.
$\overline{OEbyte}$	= Low to DATA out Enabled	Max.
CB in	to DATA out	Max.
(CODE ID 1, 0 = 10)		
LEout/$\overline{GENERATE}$	= Low to $\overline{ERROR}$/$\overline{MERROR}$ = High	Max.
LEout/$\overline{GENERATE}$	= Low to SC out	Max.
DATA in	**to SC out**	**Max.**
*LE in	= High to SC out*	Max.
CB in	to SC out	Max.
(forced high)		
$\overline{OEsc}$	= High to SC out Disabled	Min.
$\overline{OEsc}$	= High to SC out Disabled	Max.
$\overline{OEsc}$	= Low to SC out Enabled	Min.
$\overline{OEsc}$	= Low to SC out Enabled	Max.
(check bits exit)		
(don't care)		

NOTES:
1. BOLD indicates critical parameters.
2. Valid "DATA" and valid "CBin" are shown to occur simultaneously, since both busses are latched and opened by the "LEin" input.

*Assumes DATA bus becomes input 4ns before LEin goes high.

IDT49C460C TIMING: DATA SHEET PARAMETERS

DETECT or CORRECT Mode (from GENERATE Mode)

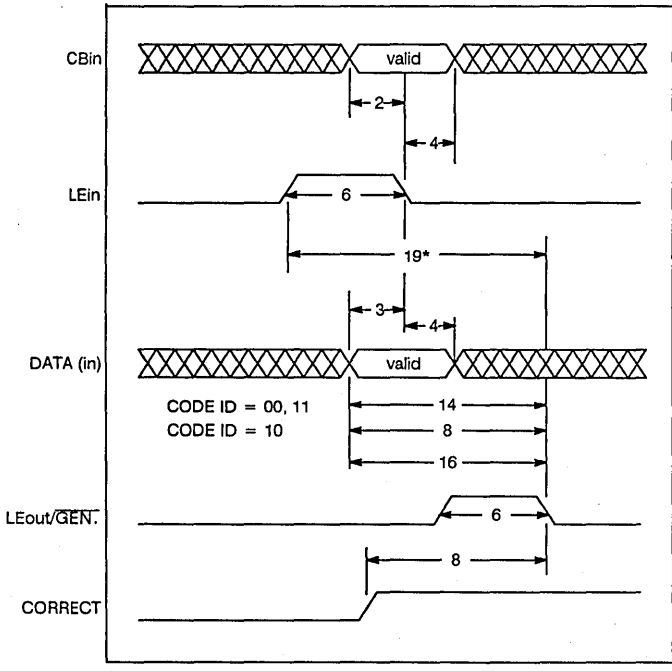


PROPAGATION DELAY FROM	TO	MIN./MAX.
$\overline{OEbyte}$	= High to DATA out Disabled	Min.
$\overline{OEbyte}$	= High to DATA out Disabled	Max.
$\overline{OEbyte}$	= Low to DATA out Enabled	Min.
$\overline{OEbyte}$	= Low to DATA out Enabled	Max.
(corrected DATA if Correct mode) (DATA in if Detect mode)		
DATA in	**to DATA out**	**Max.**
CORRECT	= High to DATA out	Max.
CB in	to DATA out	Max.
CB in	to DATA out	Max.
*LE in	= High to DATA out*	Max.
LEout/$\overline{GENERATE}$	= High to DATA out	Max.
LEout/$\overline{GENERATE}$	= High to $\overline{MERROR}$ = Low	Max.
LEout/$\overline{GENERATE}$	= High to $\overline{ERROR}$ = Low	Max.
DATA in	**to $\overline{ERROR}$ = Low**	**Max.**
CB in	to $\overline{ERROR}$ = Low	Max.
*LE in	= High to $\overline{ERROR}$ = Low*	Max.
(Low = error)		
DATA in	to $\overline{MERROR}$ = Low	Max.
CB in	to $\overline{MERROR}$ = Low	Max.
*LE in	= High to $\overline{MERROR}$ = Low*	Max.
(Low = error)		
DATA in	to SC out	Max.
CB in	to SC out	Max.
$\overline{OEsc}$	= High to SC out Disabled	Min.
$\overline{OEsc}$	= High to SC out Disabled	Max.
$\overline{OEsc}$	= Low to SC out Enabled	Min.
$\overline{OEsc}$	= Low to SC out Enabled	Max.
(syndrome bits come out)		

NOTES:
1. BOLD indicates critical parameters.
*Assumes "CB in" and/or "DATA in" are valid at least 4ns before "LE in" goes high.

IDT49C460C TIMING: DATA SHEET PARAMETERS

SET-UP and HOLD Times and Minimum PULSE WIDTHS



SET-UP/HOLD TIME OF WITH RESPECT TO	MIN./MAX.
CB in Set-up to LE in = Low	Min.
CB in Hold to LE in = Low	Min.
LE in width	Min.
LE in = High to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
DATA Set-up to LE in = Low	Min.
DATA Hold to LE in = Low	Min.
CB in Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
CB in Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
DATA Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.
LEout/$\overline{\text{GENERATE}}$ Width	Min.
CORRECT Set-up to LEout/$\overline{\text{GENERATE}}$ = Low	Min.

NOTES:

1. BOLD indicates critical parameters.

*Enable to enable timing requirement to ensure that the last DATA word applied to "DATA in" is made available as "DATA out"; assumes that "DATA in" is valid at least 4ns before "LE in" goes high.

INPUT/OUTPUT INTERFACE CIRCUIT

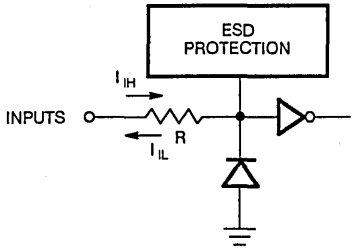


Figure 11. Input Structure (All Inputs)

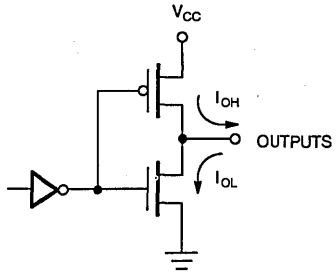


Figure 12. Output Structure

TEST LOAD CIRCUIT

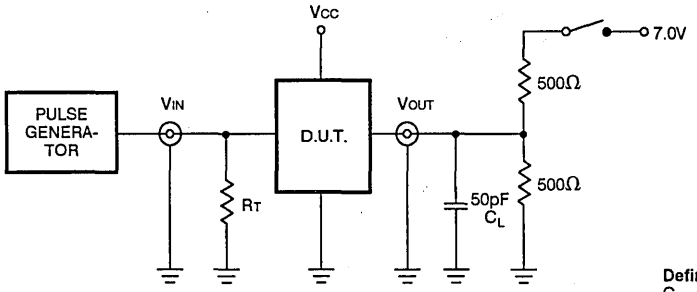


Figure 13.

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other outputs	Open

Definitions:
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of pulse generator.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 13

ORDERING INFORMATION

IDT — 49C460 (Device Type) — X (Speed) — X (Package) — X (Process/Temperature Range)

BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
L	Leadless Chip Carrier (50 mil centers)
G	Pin Grid Array
J	Plastic Leaded Chip Carrier
PG	Plastic Pin Grid Array
QE	Ceramic Quad Flat Pack
Blank	Standard Speed
A	High-Speed
B	Very High-Speed
C	Ultra-High-Speed
49C460	32-Bit E.D.C.

Integrated Device Technology, Inc.

32-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

ADVANCE INFORMATION
IDT 49C465

MICROSLICE™ PRODUCT

FEATURES:

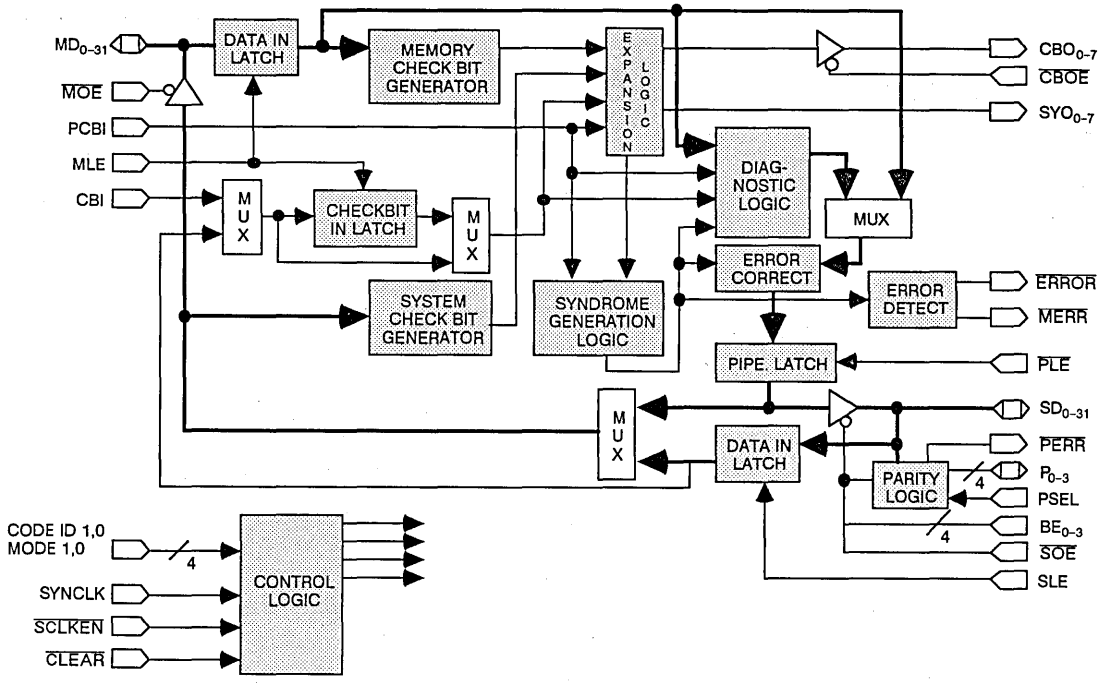
- 32-bit Wide Flow-thru EDC Unit
- Expandable to 64-bits
- Single-chip 64-bit Generate Mode
- Separate System and Memory Busses
- On-chip Pipeline Register With External Control
- Corrects All Single-bit Errors
- Detects All Double-bit Errors, Some Multiple-bit Errors
- Error Detection Time—20ns
- Error Correction Time—25ns
- Internal Syndrome Register
- Four-bit Error Counter and Error Data Register On-chip
- Parity Generation on System Data Bus
- Low Power CMOS—100mA typical
- 144-pin PGA & 164-pin Ceramic Quad Flatpack Packages

DESCRIPTION:

The IDT49C465 is a 32-bit, two-data bus, Flow-thru EDC™ unit. The chip provides single-error correction, and multiple-error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading 2 units, without the need for additional external logic. The Flow-thru EDC has been optimized for speed and simplicity of control.

The EDC unit has been designed to be used in either of two configurations in an error correcting memory system. The bi-directional configuration is most appropriate for systems using bi-directional memory busses. A second system configuration utilizes external octal buffers, and is particularly well suited for systems using memory with separate I/O busses.

FUNCTIONAL BLOCK DIAGRAM



MICROSLICE and Flow-thru EDC are trademarks of Integrated Device Technology, Inc.

SYSTEM CONFIGURATIONS

The IDT49C465 EDC unit can be used in various configurations in an EDC system. The basic configurations are shown below.

Figure 1 illustrates a bi-directional configuration, which is most appropriate for systems using bi-directional memory busses. It is the simplest configuration to understand and use. During a correction cycle, the corrected data word can be simultaneously output on both the system bus and memory bus. Logically, no other parts are required for the correction function. During partial-word-write operations, the new bytes are internally combined with the corrected old bytes for checkbit generation and writing to memory.

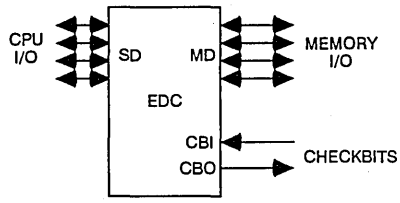


Figure 1. Bi-Directional Configuration

Figure 2 illustrates a separate I/O configuration. This is appropriate for systems using separate I/O memory busses. This configuration allows separate input and output memory busses to be used. Corrected data is output on the SD outputs for the system and rewrite to memory. Partial word-write bytes are combined externally for writing and checkbit generation.

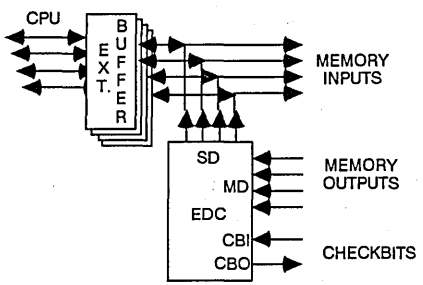


Figure 2. Separate I/O Configuration

Figure 3 illustrates a third configuration which utilizes external buffers and is also well suited for systems using memory with separate I/O busses. Internally, the checkbit generation function and the correction function are fully independent of each other and it is possible to correct memory data and generate checkbits from new system data simultaneously. Since data from memory does not need to pass through the part, the EDC system may operate in "bus-watch" mode. As in the separate I/O configuration, corrected data from the EDC is output on the SD outputs.

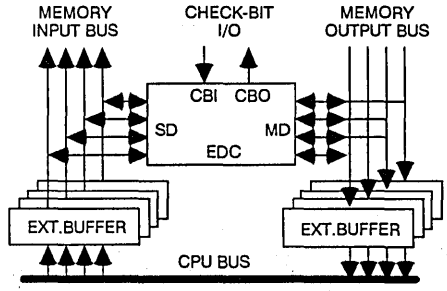


Figure 3. By-passed Configuration

Figure 4 illustrates the single-chip generate-only mode for very fast 64-bit checkbit generation, in systems that use separate checkbit-generate and detect-correct units. If this is not desired, 64-bit checkbit generation and correction can be done with just 2 EDC units. 64-bit correction is also straight-forward, fast and requires no extra hardware for the expansion.

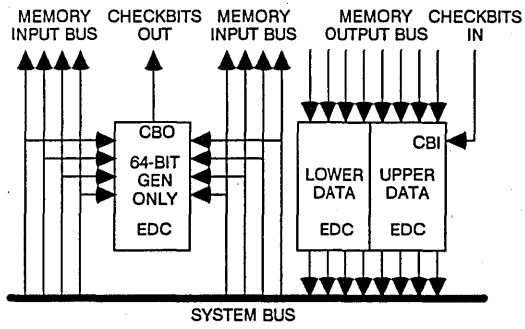


Figure 4. 64-bit Generate-only Mode

FUNCTIONAL DESCRIPTION

32-BIT MODE (CODE ID 1,0 = 00)

The error detection/ correction codes used consist of a modified Hamming code. The code is identical to that used on the IDT49C460.

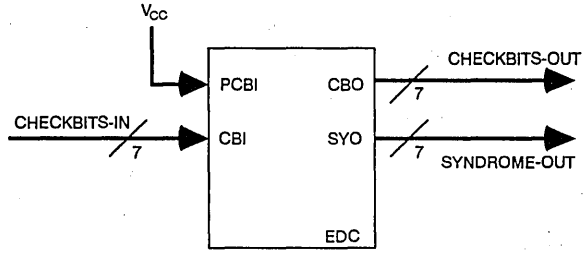


Figure 5. 32-bit Mode

64-BIT MODE (CODE ID 1,0 = 10 & 11)

The expansion bus topology is shown in Figure 6. This topology allows the syndrome bits used by the correction logic to be generated simultaneously in both parts used in the expansion. During a 64-bit detection or correction operation, "Partial-Checkbit" data and "Partial-Syndrome" data is simultaneously exchanged between the two EDC units in opposite directions on dedicated expansion buses. This results in very short 64-bit detection and correction times. Typical detect time is 30ns and typical correct time is 35ns.

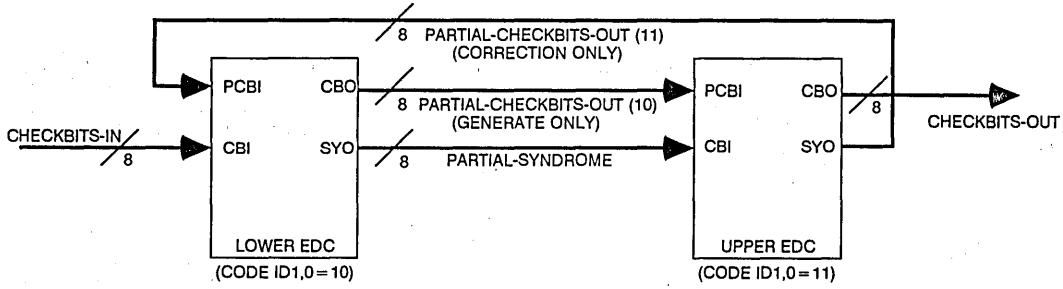


Figure 6. 64-bit Mode - 2 Cascaded IDT49C465 Devices

64-BIT GENERATE-ONLY MODE (CODE ID 1,0 = 01)

If the IDentity pins CODE ID 1,0 = 01, a single EDC is placed in the 64-bit generate-only mode. In this mode, the lower 32 bits of the 64-bit data word enter the device on the MD_{0-31} inputs and the upper 32 bits enter the device on the SD_{0-31} inputs. This provides the device with the full 64-bit word from memory. The resultant generated checkbits are output on the CBO_{0-7} outputs.

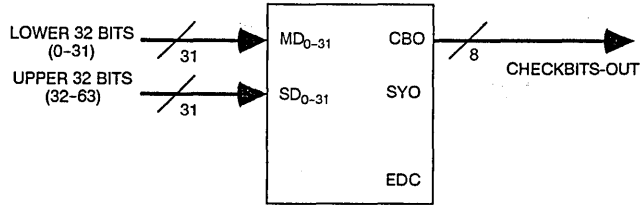


Figure 7. 64-bit Generate-only Mode (Single-chip)

PIN DESCRIPTIONS

SYMBOL	I/O	DESCRIPTION
I/O BUSSES AND CONTROLS		
MD_{0-31}	I/O	**Memory Data:** These I/O pins accept a 32-bit data word from memory for error detection and/or correction. They also output data to be written to memory when the EDC unit is used in the bi-directional mode.
MLE	I	**Memory Latch Enable:** MLE is used to latch data at the MD inputs and checkbits at the CBI inputs. When identified as the #2 slice in a 64-bit cascade, the checkbit latch is bypassed. The latch is transparent when MLE is high; data is latched when MLE is low.
$\overline{MOE}$	I	**Memory Output Enable*:** $\overline{MOE}$ enables Memory Data output drivers when low.
SD_{0-7} SD_{8-15} SD_{16-23} SD_{24-31}	I/O	**System Data:** Data from MD_{0-31} appears at these pins corrected if MODE 0, 1 = 11, or uncorrected in the other 3 modes. The BEn inputs must be asserted and the $\overline{SOE}$ pin must be low to enable the SD output buffers during a read cycle. In a write or partial-write cycle for separate I/O memory systems, the byte not-to-be modified appears at SDn to SD + 7 if BEn is high, and $\overline{SOE}$ is low for re-writing to memory. The new bytes to be written are input by the SDn pins, if BEn is low for writing checkbits to memory. In a write or partial-write cycle for bi-directional memory systems, the byte not to be modified is re-directed to the MD I/O pins if BEn is high, for checkbit generation and rewriting to memory via the MD I/O pins. $\overline{SOE}$ must be high to avoid enabling the output drivers to the system bus in this mode. The new bytes to be written are input by the SDn pins for checkbit generation and writing to memory. BEn must be low to properly direct the input data from the System Data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
$\overline{PLE}$	I	**PipeLine Enable*:** $\overline{PLE}$ is an input which controls a pipeline latch on the SD bus outputs. The latch is transparent when $\overline{PLE}$ is low; the data is latched when $\overline{PLE}$ is high.
SLE	I	**System Latch Enable:** SLE is an input used to latch data at the SD inputs. The latch is transparent when SLE is high; the data is latched when SLE is low.
$\overline{SOE}$	I	**System Output Enable*:** Enables System output drivers if corresponding ByteEnable inputs are active (see Byte Enable Select).
BE_{0-3}	I	**Byte Enables:** In systems using separate I/O memory buses, BEn is used to enable the SD outputs for byte n. In systems using Bi-directional I/O memory buses, the BEn pins also control the Memory-Data-byte mux. When BEn is high, the corrected or uncorrected data from the memory data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BEn is low, the data from the system data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used during partial-word-write operations. BE_0 controls SD_{0-7} BE_1 controls SD_{8-15} BE_2 controls SD_{16-23} BE_3 controls SD_{24-31}
P_{0-3}	I/O	**Parity I/O:** The parity I/O pins for bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins serve as parity inputs and are used in generating the parity error signal under certain conditions (see byte enable definitions). The parity is even or odd depending on the state of the Parity SELect pin (PSEL).
PSEL	I	**Parity SELect:** If the Parity SELect pin is low, the parity is even. If the Parity SELect pin is high, the parity is odd.
INPUTS		
CBI	I	**CheckBits-In** (00, 01) CheckBits-In-1 (10) Partial-Syndrome-In (11): In a single EDC system or in the #1 position of a cascaded EDC system, these inputs accept the checkbits (0 to 7) from the RAM. In the #2 position in a cascaded EDC system, these inputs accept the "Partial-Syndromes" from the #1 EDC unit.
$\overline{CLEAR}$	I	$\overline{CLEAR}$: When the $\overline{CLEAR}$ pin is pulled low, the error data register, the syndrome register, and the error counter are cleared.
$CODE\ ID_{1,0}$	I	**CODE IDentity:** Inputs which identify the slice position/ functional mode of the 49C465. (00) Single 32-bit EDC unit (10) Position 1 of a 64-bit cascade (01) 64-bit "Checkbit-generate-only" unit (11) Position 2 of a 64-bit cascade
$MODE_{1,0}$	I	**MODE select:** Selects one of four operating modes. When mode changes are made, care must be taken not to change both MODE bits simultaneously.
	(00)	**Error Data/Zero Source:** Allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by toggling $\overline{CLEAR}$ low. Clearing the Error-Data Register provides a source of all-zero-data for hardware initialization of memory if this desired. The Syndrome register and Error-Data Register record the syndrome and uncorrected data from the first error that occurs after they are reset by the $\overline{CLEAR}$ pin. Specifically, the syndrome register and Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated (ERROR = low), and the error counter indicates zero.
	(10)	**Generate/Detect:** In this mode, error correction is disabled. Error generation and detection are normal.
	(01)	**Output Syndrome/Insert diagnostic check-bits:** In this mode, the contents of the syndrome register and error counter are made available for output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error logging purposes. The syndrome register and the Error Data register are updated when there is a positive edge on SYNCLK, an error condition is indicated and the error counter indicates zero errors. Thus, the syndrome register saves the syndrome that was present when the first error occurred after the error counter was cleared. The syndrome register and the error counter are cleared by toggling $\overline{CLEAR}$ low. The error counter lets the system tell if more than one error has occurred since the last time the syndrome or error data register was read.
	(11)	**Normal:** Normal EDC operation.

8

PIN DESCRIPTIONS (Cont'd.)

SYMBOL	I/O	DESCRIPTION
INPUTS (Cont'd.)		
$PCBI_{0-7}$	I	**Partial-CheckBits-In** (10) Partial-CheckBits-In (11): In a single EDC system, these inputs are tied to VCC. In a cascaded EDC system, the "Partial-Checkbits" bits used by the #1 part are accepted by these inputs. In the #2 position of a cascaded EDC system, "Partial checkbits" generated by the #1 part are accepted by these inputs.
RES	I	**REServed:** The REServed pin is a dedicated test input, and must be tied to Vss.
SYNCLK	I	**SYNdrome CLocK:** If $\overline{ERROR}$ is low, and the error counter indicates zero errors, syndrome bits are clocked into the syndrome register, and data from the outputs of the Memory Data latch are clocked into the error data register, on the low-to-high edge of SYNCLK. If $\overline{ERROR}$ is low, the error counter will increment on the low-to-high edge of SYN CLK, unless the error counter indicates fifteen errors.
$\overline{SCLKEN}$	I	**$\overline{SYNCLK\ ENABLE}$:** The $\overline{SCLKEN}$ enables the SYNCLK signal. SYNCLK is ignored (internally low) if $\overline{SCLKEN}$ is high.
OUTPUTS AND ENABLES		
CBO_{0-7}	O	**CheckBits-Out** (00, 01) Partial-CheckBits-Out (10) Checkbits-Out (11): In a single EDC system, the checkbits are output to memory on these outputs. In the #1 position in a cascaded EDC system, the "Partial-checkbits" used by the #2 slice are output by these outputs. In the #2 position in a cascade, the checkbits appear at these outputs.
$\overline{CBOE}$	I	**CheckBits Out Enable*:** Enables checkbit output drivers when low.
SYO_{0-7}	O	**SYndrome-Out** (00) Partial-SYndrome-Out (10) Partial-Checkbits-Out (11): In a 32-bit EDC system, the syndrome bits can be output from these outputs if desired. In the #1 position in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs. In the #2 position in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs.
$\overline{ERROR}$	O	**$\overline{ERROR}$:** When in 'normal' mode, a low on this pin indicates that one or more errors have been detected.
$\overline{MERROR}$	O	**$\overline{Multiple\ ERROR}$:** When low, this pin indicates that two or more errors have been detected.
$\overline{PERR}$	O	**$\overline{Parity\ ERRor}$:** When low, this pin indicates a parity error.Parity error is not gated or latched internally (see Byte Enable definitions).
POWER SUPPLY PINS		
VCC_{1-10}	P	+5 Volts
VSS_{1-12}	P	Ground

DIAGNOSTIC FEATURES

Direct Checkbit Readback—Internal data paths allow both the checkbit output bus and the checkbit input bus to be read directly by the system bus for diagnostic purposes. The two checkbit busses are read via the System Data bus by entering the 'Syndrome Output' mode and enabling the System Data output drivers.

Direct Read-Path Checkbit Injection—In the "Output-Syndrome" Mode, $bits_{0-7}$ of the System Data latch are presented to the inputs of the CheckBit Input latch. If $\overline{MLE}$ is strobed, the checkbit latch will be loaded with this value, in place of the checkbits from memory. This allows the correction function of the EDC to be verified "on-board".

"Generate/Detect-only" Mode—When the EDC unit is in the "Generate/Detect-only" mode, data is not corrected or altered by the error correction network.

Error Counter—The four-bit on-board error counter is incremented if: the error counter contents does not indicate "F" HEX and there is a positive transition on the SYNCLK input when the $\overline{ERROR}$ signal is low. This counter is cleared by pulling the $\overline{CLEAR}$ input low. The counter is read via the System Data bus by entering the Syndrome output mode and enabling the System Data output drivers.

Error Data Register—The uncorrected data from the Memory Data register output bus is stored in the Error Data Register if: the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{ERROR}$ signal is low. Thus, the Error Data Register contains memory data corresponding to the first error to occur since the register was cleared. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the 'Error-Data-Output' mode and enabling the System Data output drivers. This register can be used as an "all-zero-data" data source for memory initialization, in systems where the initialization process is to be done entirely by the memory controller without interaction with the operating system.

Syndrome Register—After an error has been detected, the syndrome bits generated are clocked into the internal syndrome register if: the error counter contents indicates "0", and there is a positive transition on the SYNCLK input when the $\overline{ERROR}$ signal is low. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the 'Syndrome Output' mode and enabling the System Data output drivers.

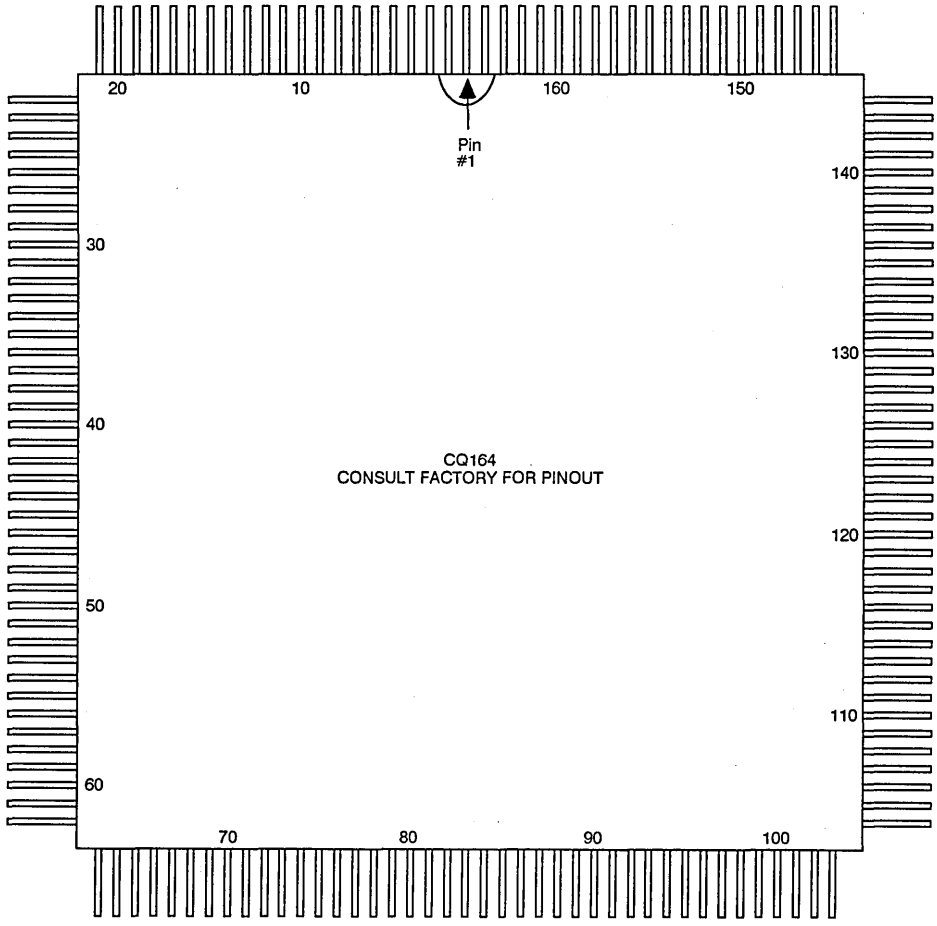
PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q
15	V_{CC}	SD_2	SY_{16}	SY_{15}	SY_{13}	CODE ID 1	CODE ID 0	MODE ID1	$\overline{MERR}$	$\overline{ERROR}$	SY_{05}	SY_{03}	SY_{01}	MD_1	V_{CC}
14	SD_6	SD_4	SD_1	SY_{17}	SY_{14}	SY_{11}	SY_{10}	MODE ID0	SY_{06}	SY_{04}	SY_{02}	MD_0	MD_2	V_{CC}	MD_5
13	SD_9	SD_5	BE_0	SD_3	SD_0	SY_{12}	GND	GND	SY_{07}	GND	SY_{00}	V_{CC}	MD_3	MD_6	MD_9
12	SD_{11}	SD_7	V_{CC}										MD_4	MD_8	GND
11	SD_{12}	SD_{10}	SD_8										MD_7	MD_{10}	MD_{11}
10	SD_{15}	BE_1	GND										MD_{12}	MD_{13}	MD_{15}
9	SLE	SD_{13}	SD_{14}										$\overline{MOE}$	MD_{14}	MLE
8	$\overline{SOE}$	$\overline{PLE}$	GND				G144-1						GND	MD_{17}	MD_{16}
7	SD_{17}	SD_{19}	SD_{16}										MD_{20}	MD_{21}	MD_{18}
6	SD_{18}	BE_2	SD_{20}										GND	MD_{23}	MD_{19}
5	SD_{21}	SD_{22}	SD_{25}										MD_{27}	MD_{25}	MD_{22}
4	GND	SD_{24}	BE_3										V_{CC}	MD_{28}	MD_{24}
3	SD_{23}	SD_{26}	SD_{28}	V_{CC}	CBO_0	$\overline{CBOE}$	CBO_7	GND	GND	$\overline{SCLK}$ EN	GND	CBI_6	CBI_7	MD_{30}	MD_{26}
2	SD_{27}	V_{CC}	SD_{29}	SD_{31}	CBO_2	CBO_4	CBO_6	P_3	TEST	SYN CLK	CBI_0	CBI_3	CBI_4	MD_{31}	MD_{29}
1	V_{CC}	SD_{30}	CBO_1	CBO_3	CBO_5	PSEL	$\overline{PERR}$	P_2	P_1	P_0	$\overline{CLR}$	CBI_1	CBI_2	CBI_5	V_{CC}

Pin # 1

144-PGA PINOUT
TOP VIEW

PIN CONFIGURATIONS



164-CERAMIC QUAD FLATPACK PINOUT
(CQFP—PITCH = .025")
TOP VIEW

REDUCED INSTRUCTION SET COMPUTER (RISC) PROCESSORS

The power of RISC

RISC concepts run counter to many of the microprocessor architectural and design theories of the last two decades. RISC theory concludes that less is better and faster. This reverses the trend to add more instruction capability and hardware functions to the already complex structure of the microprocessor.

RISC research began in the mid-1970s at IBM. Researchers discovered that although microprocessors and their instruction sets were growing more complex, high-level language compilers typically used only a fraction of those instructions. When they analyzed how the software used hardware resources, it was further discovered that most of the software consisted of very simple instructions. Complex instructions found in CISC architectures were used infrequently. In fact, 20 percent of a computer's instructions controlled 80 percent of its processing work.

Further developments at IBM, Stanford and the University of California at Berkeley confirmed these conclusions and led to the emergence of RISC technology. Although debate continues over the various RISC architectures, research at Stanford introduced the concept of using compilers to optimize the speed and efficiency of program execution. The focus on using optimizing compilers to maximize the performance of the RISC architecture is the essence of the R3000 design philosophy.

RISC or CISC?

What makes RISC so powerful? A design methodology that demands a "hand-in-glove" development across many disciplines—from custom VLSI, CPU organization and systems architecture to operating systems and compiler designs. Unlike CISC processors, the RISC architecture design was not handicapped by having to be backward compatible with prior generations of software. The conventional CISC design approach often sacrifices performance to retain compatibility.

Further, the RISC instruction set is simplified and thereby executes faster than CISC instruction sets. Only those instructions that are most frequently used are included. With fewer instructions, the streamlined architecture results in a smaller die that allows faster clock rates. A design goal of RISC is to minimize the CPU cycles required for each instruction, approaching the performance of one cycle or less per instruction. Even today's most advanced CISC processors average over 5 cycles per instruction. IDT's R3000 RISC processor, in comparison, averages only 1.25 cycles per instruction, the lowest in the industry.

The R3000* family of RISC processors, including the IDT79R3000 Central Processing (Unit) (CPU), the IDT79R3010 Floating Point Accelerator (FPA), and the IDT79R3020 Write Buffers, was developed at MIPS Computer Systems. MIPS was an early pioneer in RISC technology. They introduced the first commercially available RISC processor in 1985, the R2000, based upon research completed at Stanford University in the 70's. The R3000 family offers a path to significant improvements in system performance without the increasingly complex circuitry used to improve the performance of CISC processors.

IDT Components for Cache and Memory Interface

IDT offers a broad range of cache RAMs and high-speed logic to complement the R2000/R3000 RISC components and provide a fully integrated approach to RISC design. SRAMs available include densities from 16K to 1 megabit and feature access times as low as 20 nanoseconds (ns) for standard CMOS and 10ns for BiCEMOS/ECL SRAMs.

Devices specifically developed for RISC systems include IDT's new 71586 4K by 16 latched SRAM. This combination device helps eliminate propagation delay in the cache-logic interface and thereby boost sytem speed. These standard and proprietary devices can be configured by cache size and speed to match a wide variety of applications from embedded control to high-performance workstations. IDT components typically used for cache and memory interface in the R3000 system include:

	PART NUMBER	DESCRIPTION	SPEED
Cache Memory	• IDT6116	2K x 8 SRAM	20ns Access Time
	• IDT71586	4K x 16 Latch/SRAM	35ns Access Time
	• IDT7198	16K x 4 SRAM	20ns Access Time
	• IDT7164	8K x 8 SRAM	25ns Access Time
	• IDT71258	64K x 4 SRAM	25ns Access Time
Bus Interface Logic	• IDT74FCT373A	Octal Latch	
	• IDT74FCT374A	Octal Register	
	• IDT74FCT240A	Octal Buffer	
	• IDT74FCT244A	Octal Buffer	
	• IDT74FCT646A	Bi-directional Latch	
	• IDT74FCT823A	9-bit Register	

*The R2000A series is also available from IDT. The R2000A CPU is a subset of the R3000 and is object code compatible.

RISC Subsystem Modules and Peripheral Support

IDT is introducing a number of R3000 CPU subsytem modules as well as high-speed SRAM cache-modules targeted for RISC-based sytems. These surface mount modules decrease motherboard complexity and thereby decrease overall system cost. Because IDT modules and their components are fully tested, the need for component testing is eliminated. All individual components are selected and tested for their sub-system speed-timing compatibility. Modules also expedite sytem development and therefore decrease time-to-market.

RISC MODULES AND PERIPHERAL COMPONENTS

	PART NUMBER	DESCRIPTION
Peripheral Support	• IDT49C460 • IDT49C465 • IDT7252	32-bit EDC 32-bit Flow through EDC Bi-directional FIFO Peripheral Interface Card (32-bit bus to 8-bit bus)
Cache Memory Modules	Standard Versions: • IDT7MB6039 • IDT7MB6042 • IDT7MB6044 Multi processing: • IDT7MB6049 • IDT7MB6051	 Dual 16K x 60 Dual 8K x 60 Dual 4K x 60 Dual 16K x 60 Dual 8K x 60
CPU Communication Devices	• IDT7202 • IDT7203 • IDT7204 • IDT7205 • IDT7130 • IDT7132 • IDT7133 • IDT7134 • IDT71342	1K x 9 FIFO 2K x 9 FIFO 4K x 9 FIFO 8K x 9 FIFO (in development) 1K x 8 Dual Port SRAM with interrupts 2K x 8 Dual Port SRAM 2K x 16 Dual Port SRAM 4K x 8 Dual Port SRAM 4K x 8 Dual Port with Semaphores

TABLE OF CONTENTS

Integrated Device Technology, Inc.

RISC CPU PROCESSOR

PRELIMINARY
IDT 79R2000A

FEATURES:

- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-chip Cache Control—The R2000A provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 64 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64 entry Transition Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space.
- Coprocessor Interface—The R2000A generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers available include: C, FORTRAN, Pascal, PL/1, COBOL, Ada
- UNIX™ System V.3 and BSD 4.3 operating systems supported.
- High-speed CEMOS™ technology
- Pin, function and software compatible with the MIPS Computer Systems R2000A RISC CPU.
- 12.5MHz or 16.7MHz clock rate yields 10 to 13 MIPS sustained throughput.
- Military product compliant to MIL-STD -883, Class B

DESCRIPTION:

Please see the 79R3000 data sheet for complete description. The R3000 is a superset of the R2000A and is available in 16.7, 20, and 25MHz clock rates. For the differences between the R2000A and R3000 please see the "R3000 Family Hardware User's Manual" or the R3000 data sheet section entitled "Backward Compatibility with 79R2000A".

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CEMOS is a trademark of Integrated Device Technology, Inc.
UNIX is a registered trademark of AT&T.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	CpCond 2	CpCond 3	Intr* 2	Intr* 5	Wr Busy*	Reset*	VCC10
B	AdrLo 3	reser-ved2	AdrLo 7	AdrLo 9	AdrLo 12	reser-ved3	AdrLo 13	CpCond 1	Intr* 1	Intr* 3	Cp Busy*	Bus Error*	reser-ved4	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	Gnd13	Gnd12	VCC11	Intr* 0	Intr* 4	Rd Busy	Gnd11	Tag13	TagP0	Tag18
D	Data1	AdrLo 2	Gnd0										Tag14	Tag17	Tag19
E	Data P0	Data0	AdrLo 1										Tag16	Tag20	VCC9
F	VCC0	Data7	Data2										Gnd10	Tag21	Tag23
G	Data4	Data3	Gnd1										Gnd9	Tag22	TagP1
H	Data6	Data5	Data8										VCC8	Tag25	Tag24
J	Data 10	Data P1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	Gnd2										Gnd8	Tag P2	Tag27
L	VCC1	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	Data P2										Gnd7	Acc Typ1	VCC7
N	Data 14	Data 18	Data 19	Gnd3	Data 24	Data P3	VCC3	VCC4	Gnd5	Gnd6	DRd	MemWr*	MemRd*	Run*	TagV
P	Data 23	Data 20	reser-ved0	Data 22	Data 26	Data 27	reser-ved1	Data 30	Clk2x Sys	Clk2x Rd	Dclk*	IRd	IWr	Cp Sync*	Acc Typ0
Q	VCC2	Data 21	Data 25	Data 31	Data 28	Gnd4	Data 29	Exc*	Clk2x Phi	Clk2x Smp	Sys Out*	VCC5	IClk*	DWr	VCC6

ABSOLUTE MAXIMUM RATINGS [1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage [2]	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5 volts.
3. Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

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DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OHT}	Output HIGH Voltage(4)	V_{CC} = Min., I_{OH} = -8mA	2.4	–	2.4	–	V
V_{OLT}	Output LOW Voltage(4)	V_{CC} = Min., I_{OL} = 8mA	–	0.8	–	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 5)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	500	–	575	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OHT}	Output HIGH Voltage(4)	V_{CC} = Min., I_{OH} = -8mA	2.4	–	2.4	–	V
V_{OLT}	Output LOW Voltage(4)	V_{CC} = Min., I_{OL} = 8mA	–	0.8	–	0.8	V
V_{IH}	Input HIGH Voltage(5)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 5)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	575	–	675	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2sRd, Clk2xPhi, CpBusy, and RESET*.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals.
5. V_{IH} should not be held above V_{CC} + 0.5 Volts.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
RUN OPERATION							
TDEn	Data Enable[3]		–	-2.5	–	-2	ns
TDDis	Data Disable[3]		–	-1.5	–	-1	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TWrDly	Write Delay	Load = 25pF	–	7.5	–	5	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRSDS	Reset Pin Set-up		18	–	15	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TCBS	CpBusy Set-up		15	–	13	–	ns
TCBH	CpBusy Hold		-2.5	–	-2.5	–	ns
TAcTy	Access Type (1:0)	Load = 25pF	–	10	–	7	ns
TAT2	Access Type (2)	Load = 25pF	–	20	–	17	ns
TMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TExe	Exception	Load = 25pF	–	10	–	7	ns
STALL OPERATION							
TSAVal	Address Valid	Load = 25pF	–	38	–	30	ns
TSAcTy	Access Type	Load = 25pF	–	35	–	27	ns
TMRdI	Memory Read Initiate	Load = 25pF	–	35	–	27	ns
TMRdT	Memory Read Terminate	Load = 25pF	–	10	–	7	ns
TSd	Run Terminate	Load = 25pF	–	25	–	17	ns
TRun	Run Initiate	Load = 25pF	–	15	–	12	ns
TSMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TSEx	Exception Valid	Load = 25pF	–	28	–	20	ns
RESET INITIALIZATION							
Trst	Reset Pulse Width		6	–	6	–	TckP
TrstPLL	Reset timing, Phase-lock on[5]		3000	–	3000	–	TckP
Trstcp	Reset timing, Phase-lock off[5]		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual".
5. Those parameters apply only when the 79R2010A Floating Point Compression is connected to the CPU.

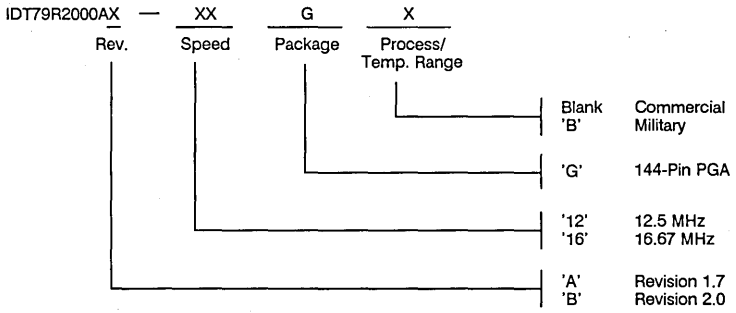
AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
RUN OPERATION							
TDEn	Data Enable[3]		–	-2.5	–	-2	ns
TDDis	Data Disable[3]		–	-1.5	–	-1	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TWrDly	Write Delay	Load = 25pF	–	7.5	–	5	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRSDS	Reset Pin Set-up		18	–	15	–	ns
TDH	Data Hold		-4	–	-4	–	ns
TCBS	CpBusy Set-up		15	–	13	–	ns
TCBH	CpBusy Hold		-4	–	-4	–	ns
TAcTy	Access Type (1:0)	Load = 25pF	–	10	–	7	ns
TAT2	Access Type (2)	Load = 25pF	–	20	–	17	ns
TMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TExe	Exception	Load = 25pF	–	10	–	7	ns
STALL OPERATION							
TSAVal	Address Valid	Load = 25pF	–	38	–	30	ns
TSAcTy	Access Type	Load = 25pF	–	35	–	27	ns
TMRdI	Memory Read Initiate	Load = 25pF	–	35	–	27	ns
TMRdT	Memory Read Terminate	Load = 25pF	–	10	–	7	ns
TSd	Run Terminate	Load = 25pF	–	25	–	17	ns
TRun	Run Initiate	Load = 25pF	–	15	–	12	ns
TSMWr	Memory Write	Load = 25pF	–	35	–	27	ns
TSEx	Exception Valid	Load = 25pF	–	28	–	20	ns
RESET INITIALIZATION							
Trst	Reset Pulse Wdith		6	–	6	–	TckP
TrstPLL	Reset timing, Phase-lock on[5]		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off[5]		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual".
5. Those parameters apply only when the 79R2010A Floating Point Compression is connected to the CPU.

ORDERING INFORMATION



9

Integrated Device Technology, Inc.

RISC FLOATING POINT ACCELERATOR (FPA)

PRELIMINARY
IDT 79R2010A

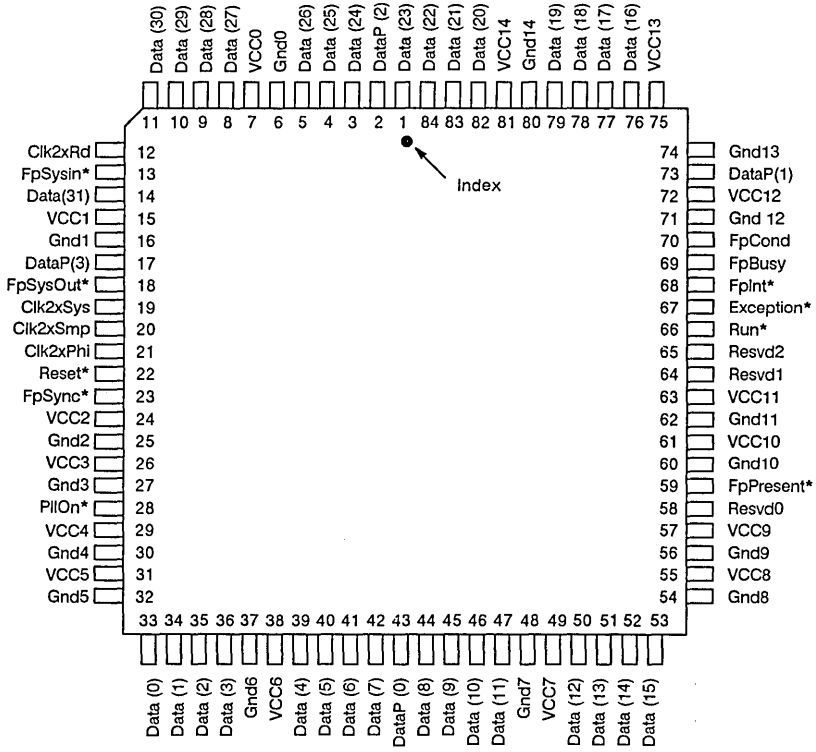
FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Peak Speed: 13-17 mips (loads, stores and moves)
- Peak Speed: 6-8 MFLOPS (single- or Double-precision)
- Cycle Time: 60-80 ns (12.5 or 16.7 MHz)
- Direct High-Speed Interface to IDT79R2000A Processor
- Supports Full Conformance With IEEE 754-1985 Floating-Point Specification.
- Floating-Point Registers: Sixteen 64-bit registers.
- High-Speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer System's R2010A RISC FPA.
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

Please see the Data Sheet for 79R3010 for complete description.

PIN CONFIGURATION (TOP VIEW)



84-PIN J-BEND CERQUAD

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ABSOLUTE MAXIMUM RATINGS (1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage (2)	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5 volts.
3. Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

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DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min., I_{OL} = 1.5mA	–	0.5	–	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 6)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
V_{IHC}	Input HIGH Voltage(4, 6)		4.0	–	4.0	–	V
V_{ILC}	Input LOW Voltage(1, 4)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	550	–	625	mA
C_{LD}	Load Capacitance		–	50	–	50	pF
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	-10	10	-10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	10	-10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = 0°C to +125°C, V_{CC} = +5V± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.5	–	0.5	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min., I_{OL} = 1.5mA	–	0.5	–	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 6)		3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	–	0.4	V
V_{IHC}	Input HIGH Voltage(4, 6)		4.0	–	4.0	–	V
V_{ILC}	Input LOW Voltage(1, 4)		–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	675	–	720	mA
C_{LD}	Load Capacitance		–	50	–	50	pF
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	-10	10	-10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	-10	10	-10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2sRd, Clk2xPhi, CpBusy, and Reset".
3. These parameters do not belong to the clock inputs.
4. V_{IHC} and V_{ILS} apply to Run and Exception*.
5. V_{OLFP} applies to the FPPresent* pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
TIMING PARAMETERS							
TDEn	Data Enable[3]		–	-2.5	–	-2	ns
TDDis	Data Disable[3]		0	–	0	–	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TDS	Data Set-up		11.5	–	9	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TFpCond	Fp Condition		–	45	–	35	ns
TFpBusy	Fp Busy		–	20	–	15	ns
TFpInt	Fp Interrupt		–	55	–	40	ns
TFpMov	Fp Move To		–	45	–	35	ns
TExS	Exception Set-up		15	–	10	–	ns
TExH	Exception Hold		0	–	0	–	ns
TRunS	Run Set-up		15	–	10	–	ns
TRunH	Run Hold		-2	–	-2	–	ns
RESET INITIALIZATION							
TrstPLL	Reset timing, Phase-lock on		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual"

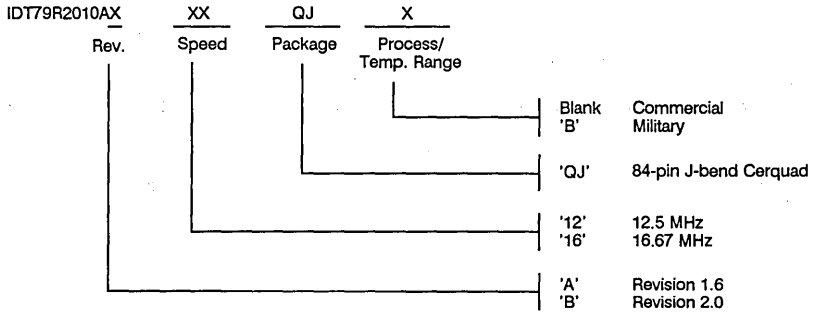
AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to +125°C, V_{CC} = +5V± 10%)

SYMBOL	PARAMETER	TEST CONDITION	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
CLOCK							
TCkHigh	Input Clock High	Transition < 5ns	18	–	12.5	–	ns
TCkLow	Input Clock Low	Transition < 5ns	18	–	12.5	–	ns
TCkP	Input Clock Period		40	500	30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		11	tcyc/4	9	tcyc/4	ns
TIMING PARAMETERS							
TDEn	Data Enable (3)		–	-2.5	–	-2	ns
TDDis	Data Disable (3)		0	–	0	–	ns
TDVal	Data Valid	Load = 25pF	–	3.5	–	3	ns
TDS	Data Set-up		11.5	–	9	–	ns
TRsDS	Reset Set-up		18	–	15	–	ns
TDH	Data Hold		-2.5	–	-2.5	–	ns
TFpCond	Fp Condition		–	45	–	35	ns
TFpBusy	Fp Busy		–	20	–	15	ns
TFpInt	Fp Interrupt		–	55	–	40	ns
TFpMov	Fp Move To		–	45	–	35	ns
TExS	Exception Set-up		15	–	10	–	ns
TExH	Exception Hold		0	–	0	–	ns
TRunS	Run Set-up		15	–	10	–	ns
TRunH	Run Hold		-2	–	-2	–	ns
RESET INITIALIZATION							
TrstPLL	Reset timing, Phase-lock on		3000	–	3000	–	TckP
Trst	Reset timing, Phase-lock off		128	–	128	–	TckP
CAPACITIVE LOAD DERATION							
CLD	Load Derate		0.5	2.5	0.5	2	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual"

ORDERING INFORMATION



9

Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

PRELIMINARY
IDT 79R2020A

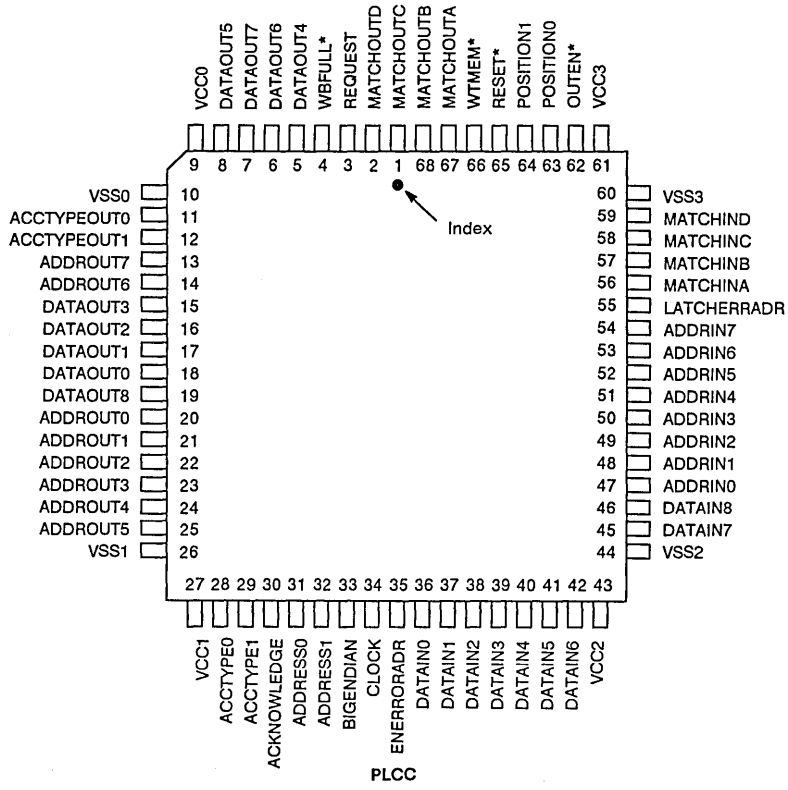
FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R2000A RISC CPU processor
- Allows for write operations by the RISC processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin and functionally compatible with the MIPS Computer Systems R2020A Write Buffer
- Used in a 12.5 or 16.7 MHz IDT79R2000 system configuration
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

Please see the Data Sheet for 79R3020 for complete description.

PIN CONFIGURATION (TOP VIEW)



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ABSOLUTE MAXIMUM RATINGS (1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage (2)	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5 volts.
3. Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage (1)		2.4	–	2.4	–	V
V_{IL}	Input LOW Voltage (2)		–	0.8	–	0.8	V
C_{IN}	Input Capacitance		10	–	10	–	pF
C_{OUT}	Output Capacitance		10	–	10	–	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	50	–	50	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:
1. V_{IH} should not be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = -3.0V for less than 15ns. V_{IL} should not fall below -0.5V for longer periods.

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage (1)		2.4	–	2.4	–	V
V_{IL}	Input LOW Voltage (2)		–	0.8	–	0.8	V
C_{IN}	Input Capacitance		10	–	10	–	pF
C_{OUT}	Output Capacitance		10	–	10	–	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	90	–	90	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:
1. V_{IH} should not be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = -3.0V for less than 15ns. V_{IL} should not fall below -0.5V for longer periods.

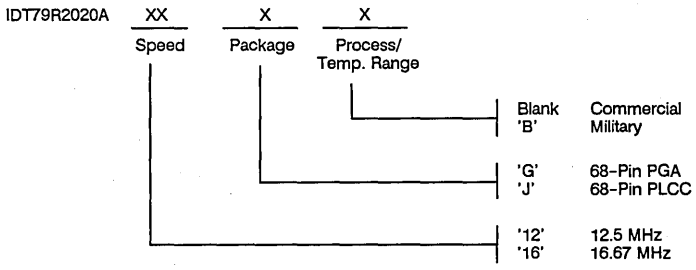
AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	12.5 MHz		16.67 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	
t1	Addrin (3:0) to Clock falling set-up	12	–	8	–	ns
t2	Addrin (3:0) to Clock falling hold	4	–	4	–	ns
t3	Address 1:0 to Clock falling set-up	12	–	8	–	ns
t4	Address 1:0 to Clock falling hold	4	–	4	–	ns
t5	Access Type 1:0 to Clock rising set-up	10	–	7	–	ns
t6	Access Type 1:0 to Clock rising hold	4	–	3	–	ns
t7	Addrin (7:4) to Clock rising set-up	10	–	7	–	ns
t8	Addrin (7:4) to Clock rising hold	4	–	3	–	ns
t9	DataIn (8:0) to Clock rising set-up	10	–	7	–	ns
t10	DataIn (8:0) to Clock rising hold	4	–	3	–	ns
t11	WrtMem* to Clock rising set-up	14	–	10	–	ns
t12	WrtMem* to Clock rising hold	8	–	6	–	ns
t13	Request from Clock rising	–	35	–	32	ns
t14	Acknowledge to Clock rising set-up	15	–	12	–	ns
t15	Acknowledge to Clock rising hold	7	–	7	–	ns
t16	LatchErrAdr rising to Acknowledge	5	–	5	–	ns
t17	WbFull* active from Clock rising	–	35	–	32	ns
t18	WbFull* inactive from Clock rising	–	35	–	32	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	5	20	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	5	20	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	35	–	25	ns
t22	MatchIn (ABCD) from Clock rising set-up	15	–	10	–	ns
t23	MatchIn (ABCD) from Clock rising hold	4	–	3	–	ns
t24	EnErrAdr* to Data (error latch) valid	5	20	2	15	ns
t25	EnErrAdr* to Data (error latch) tri-state	5	20	2	15	ns
t26	Address/Data out from Clock rising	–	35	–	32	ns
t27	Reset* to Clock rising, set-up	9	–	8	–	ns
t28	Reset* from Clock rising, hold	4	–	3	–	ns
t29	Reset* low pulse width	12	–	10	–	ns
t30	WbFull* High from Clock rising (after Reset*)	3	24	3	22	ns
t31	Request* High from Reset* low	3	22	3	20	ns
t32	Access Type 1:0 low from Reset* low	3	28	3	28	ns
t33	Match Out (ABCD) low from Reset* low	3	23	3	21	ns

AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	12	–	8	–	ns
t2	Addrin (3:0) to Clock falling hold	4	–	4	–	ns
t3	Address 1:0 to Clock falling setup	12	–	8	–	ns
t4	Address 1:0 to Clock falling hold	4	–	4	–	ns
t5	Access Type 1:0 to Clock rising setup	10	–	7	–	ns
t6	Access Type 1:0 to Clock rising hold	4	–	3	–	ns
t7	Addrin (7:4) to Clock rising setup	10	–	7	–	ns
t8	Addrin (7:4) to Clock rising hold	4	–	3	–	ns
t9	DataIn (8:0) to Clock rising setup	10	–	7	–	ns
t10	DataIn (8:0) to Clock rising hold	4	–	3	–	ns
t11	WrtMem to Clock rising setup	14	–	10	–	ns
t12	WrtMem to Clock rising hold	8	–	6	–	ns
t13	Request from Clock rising	–	35	–	32	ns
t14	Acknowledge to Clock rising setup	15	–	12	–	ns
t15	Acknowledge to Clock rising hold	7	–	7	–	ns
t16	LatchErrAdr rising to Acknowledge	5	–	5	–	ns
t17	WbFull active from Clock rising	–	35	–	32	ns
t18	WbFull inactive from Clock rising	–	35	–	32	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	5	20	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	5	20	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	35	–	25	ns
t22	MatchIn (ABCD) from Clock rising setup	15	–	10	–	ns
t23	MatchIn (ABCD) from Clock rising hold	4	–	3	–	ns
t24	EnErrAdr to Data (error latch) valid	5	20	2	15	ns
t25	EnErrAdr to Data (error latch) tri-state	5	20	2	15	ns
t26	Address/Data out from Clock rising	–	35	–	32	ns
t27	Reset* to Clock rising, set-up	9	–	8	–	ns
t28	Reset* from Clock rising, hold	4	–	3	–	ns
t29	Reset* low pulse width	12	–	10	–	ns
t30	WbFull* High from Clock rising (after Reset*)	3	24	10	22	ns
t31	Request* High from Reset* low	3	22	10	20	ns
t32	Access Type 1:0 low from Reset* low	3	28	12	28	ns
t33	Match Out (ABCD) low from Reset* low	3	23	10	21	ns

ORDERING INFORMATION



9

Integrated Device Technology, Inc.

RISC CPU PROCESSOR

PRELIMINARY
IDT 79R3000

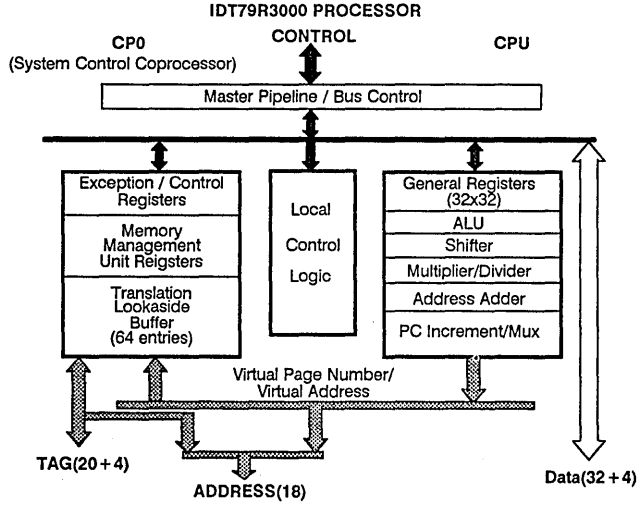
FEATURES:

- Enhanced instruction set compatible version of the IDT79R2000 RISC CPU.
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- On-Chip Cache Control—The IDT79R3000 provides a high bandwidth memory interface that handles separate external Instruction and Data Caches ranging in size from 4 to 256 Kbytes each. Both the caches are accessed during a single CPU cycle. All cache control is on-chip.
- On-Chip Memory Management Unit—A fully-associative, 64 entry Translation Lookaside Buffer (TLB) provides fast address translation for virtual-to-physical memory mapping of the 4 Gigabyte virtual address space.
- Coprocessor Interface—The IDT79R3000 generates all addresses and handles memory interface control for up to three additional tightly coupled external processors.
- Optimizing Compilers are available for C, Fortran, Pascal, COBOL, Ada, and PL/1.
- UNIX™ System V.3 and BSD 4.3 operating systems supported.
- High-speed CEMOS™ technology.
- Instruction set compatible with the IDT79R2000 RISC CPU.
- 16.7MHz and 25MHz clock rates yield 12 and 20 MIPS sustained throughput.
- Supports independent multiword block refill of both the instruction and data caches with variable block sizes.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs (up to 64 different sources), 2 software interrupts, with single cycle latency to interrupt handler routine.
- Flexible multiprocessing support on chip with no impact on uniprocessor designs.
- Military product compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT 79R3000 RISC Microprocessor consists of two tightly-coupled processors integrated on a single chip. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor performance. The second processor is a system control coprocessor, called CP0, containing a fully-associative 64 entry TLB (Translation Lookaside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4 Gigabyte virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 200 Mbytes/second using industry standard static RAMs.

This data sheet provides an overview of the features and architecture of the 79R3000 CPU, Revision 2.0. A more detailed description of the operation of the device is incorporated in the "R3000 Family Hardware User Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT. Documentation providing details of the software and development environments supporting this processor are also available from IDT.



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UNIX is a registered trademark of AT & T.

IDT79R3000 CPU Registers

The IDT 79R3000 CPU provides 32 general purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers that hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hardwired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the *Status* and *Cause* registers incorporated within the System Control Coprocessor (CP0).

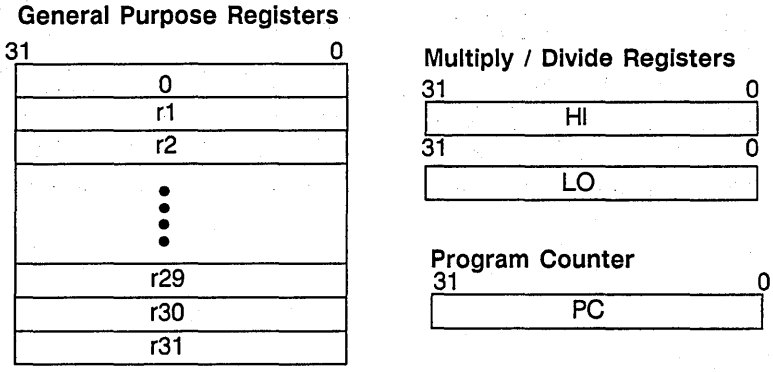

Figure 2. IDT79R3000 CPU Registers

Instruction Set Overview

All IDT 79R3000 instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding thus minimizing instruction execution time. The 79R3000 processor initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions, and Branch instructions which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions. This methodology resulted in the R3000 having the highest performance of any available microprocessor.

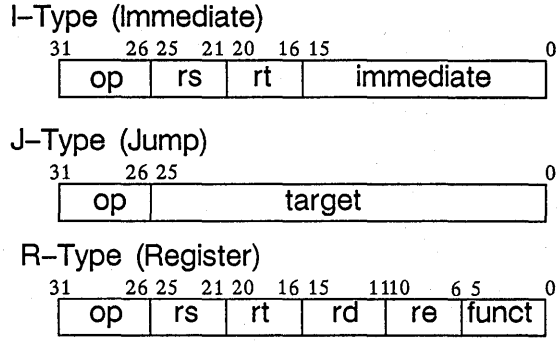

Figure 3. IDT79R3000 Instruction Formats

The IDT79R3000 instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

Loads and Stores can be performed on byte, half-word, word, or unaligned word data (32 bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.

- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats.

  Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The 79R3000 instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.

- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).

- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.

- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

  Table 1 lists the instruction set of the IDT79R3000 processor.

OP	DESCRIPTION
	Load/Store Instructions
LB	Load Byte
LBU	Load Byte Unsigned
LH	Load Halfword
LHU	Load Halfword Unsigned
LW	Load Word
LWL	Load Word Left
LWR	Load Word Right
SB	Store Byte
SH	Store Halfword
SW	Store Word
SWL	Store Word Left
SWR	Store Word Right
	Arithmetic Instructions (ALU Immediate)
ADDI	Add Immediate
ADDIU	Add Immediate Unsigned
SLTI	Set on Less Than Immediate
SLTIU	Set on Less Than Immediate Unsigned
ANDI	AND Immediate
ORI	OR Immediate
XORI	Exclusive OR Immediate
LUI	Load Upper Immediate
	Arithmetic Instructions (3-operand, register-type)
ADD	Add
ADDU	Add Unsigned
SUB	Subtract
SUBU	Subtract Unsigned
SLT	Set on Less Than
SLTU	Set on Less Than Unsigned
AND	AND
OR	OR
XOR	Exclusive OR
NOR	NOR
	Shift Instructions
SLL	Shift Left Logical
SRL	Shift Right Logical
SRA	Shift Right Arithmetic
SLLV	Shift Left Logical Variable
SRLV	Shift Right Logical Variable
SRAV	Shift Right Arithmetic Variable

OP	DESCRIPTION
	Multiply/Divide Instructions
MULT	Multiply
MULTU	Multiply Unsigned
DIV	Divide
DIVU	Divide Unsigned
MFHI	Move From HI
MTHI	Move To HI
MFLO	Move From LO
MTLO	Move To LO
	Jump and Branch Instructions
J	Jump
JAL	Jump and Link
JR	Jump to Register
JALR	Jump and Link Register
BEQ	Branch on Equal
BNE	Branch on Not Equal
BLEZ	Branch on Less than or Equal to Zero
BGTZ	Branch on Greater Than Zero
BLTZ	Branch on Less Than Zero
BGEZ	Branch on Greater than or Equal to Zero
BLTZAL	Branch on Less Than Zero and Link
BGEZAL	Branch on Greater than or Equal to Zero and Link
	Special Instructions
SYSCALL	System Call
BREAK	Break
	Coprocessor Instructions
LWCz	Load Word from Coprocessor
SWCz	Store Word to Coprocessor
MTCz	Move To Coprocessor
MFCz	Move From Coprocessor
CTCz	Move Control to Coprocessor
CFCz	Move Control From Coprocessor
COPz	Coprocessor Operation
BCzT	Branch on Coprocessor z True
BCzF	Branch on Coprocessor z False
	System Control Coprocessor (CP0) Instructions
MTC0	Move To CP0
MFC0	Move From CP0
TLBR	Read indexed TLB entry
TLBWI	Write Indexed TLB entry
TLBWR	Write Random TLB entry
TLBP	Probe TLB for matching entry
RFE	Restore From Exception

Table 1. IDT79R3000 Instruction Summary

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IDT79R3000 System Control Coprocessor (CP0)

The IDT79R3000 can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the IDT79R3000 chip and supports the virtual memory system and exception handling functions of the IDT79R3000. The virtual memory system is implemented using a Translation Lookaside Buffer and a group of programmable registers as shown in Figure 4.

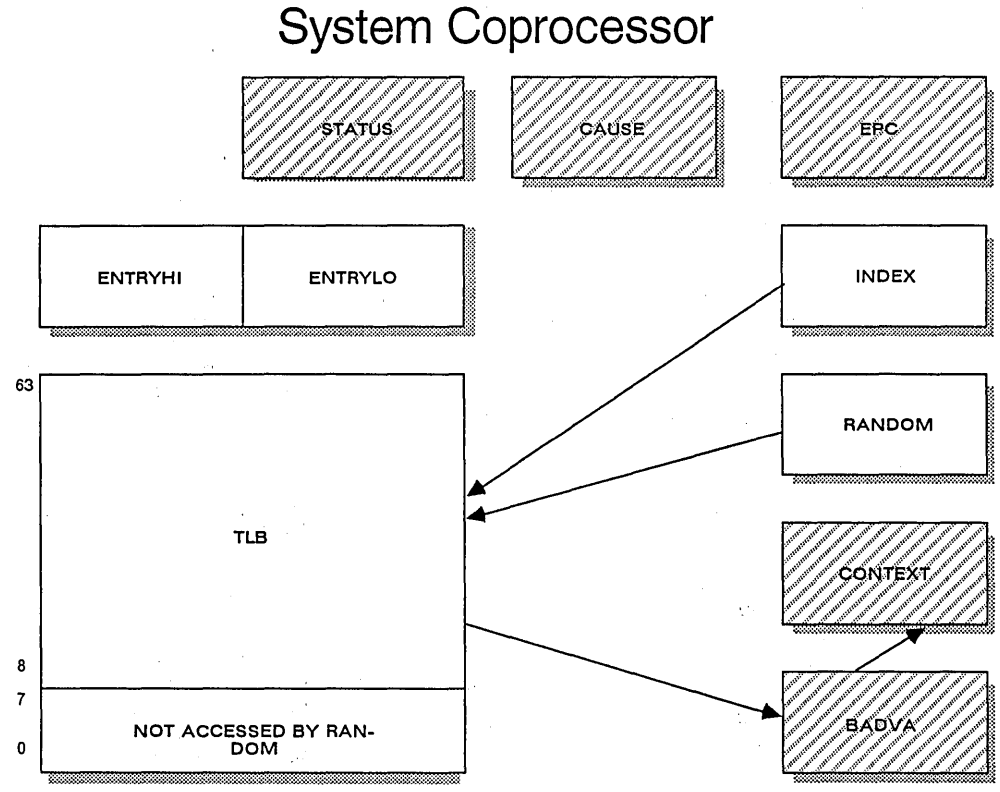


Figure 4. The System Coprocessor Registers

System Control Coprocessor (CP0) Registers

The CP0 registers shown in Figure 4 are used to control the memory management and exception handling capabilities of the IDT79R3000. Table 2 provides a brief description of each register.

REGISTER	DESCRIPTION
EntryHi	High half of a TLB entry
EntryLo	Low half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification

Table 2. System Control Coprocessor (CP0) Registers

Memory Management System

The IDT79R3000 has an addressing range of 4 Gbytes. However, since most IDT79R3000 systems implement a physical memory smaller than 4 Gbytes, the IDT79R3000 provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4 GByte address space is divided into 2 GBytes which can be accessed by both the users and the kernel, and 2 GBytes for the kernel only.

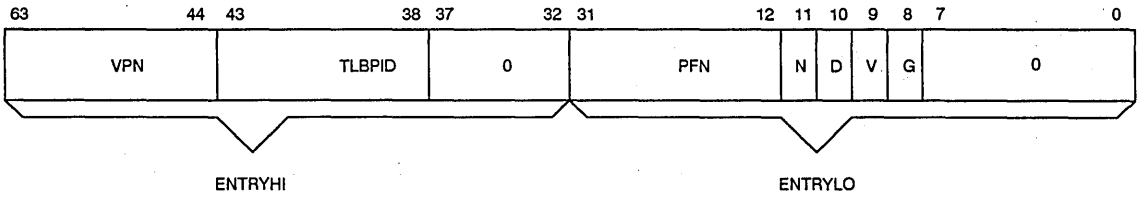
The TLB (Translation Lookaside Buffer)

Virtual memory mapping is assisted by the Translation Lookaside Buffer (TLB). The on-chip TLB provides very fast virtual memory access and is well-matched to the requirements of multitasking operating systems. The fully-associative TLB contains 64 entries, each of which maps a 4-Kbyte page, with controls for read/write access, cacheability, and process identification. The TLB allows each user to access up to 2 Gbytes of virtual address space.

Figure 5 illustrates the format of each TLB entry. The Translation operation involves matching the current Process ID (PID) and upper 20 bits of the address against PID and VPN (Virtual Page Number) fields in the TLB. When both match (or the TLB entry is Global), the VPN is replaced with the PFN (Physical Frame Number) to form the physical address.

TLB misses are handled in software, with the entry to be replaced determined by a simple RANDOM function. The routine to process a TLB miss in the UNIX environment requires only 10-12 cycles, which compares favorably with many CPUs which perform the operation in hardware.

TLB ENTRY FORMAT



VPN – Virtual Page number

TLBPID – Process ID

PFN – Physical frame number

N – Non-cacheable flag

D – Dirty flag (Write protect)

V – Valid entry flag

G – Global flag (ignore PID)

O – Reserved

Figure 5. TLB Entry Format

IDT79R3000 Operating Modes

The IDT79R3000 has two operating modes: *User* mode and *Kernel* mode. The IDT79R3000 normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception *(RFE)* instruction is executed. The manner in which memory addresses are translated or *mapped* depends on the operating mode of the IDT79R3000. Figure 6 shows the MMU translation performed for each of the operating modes.

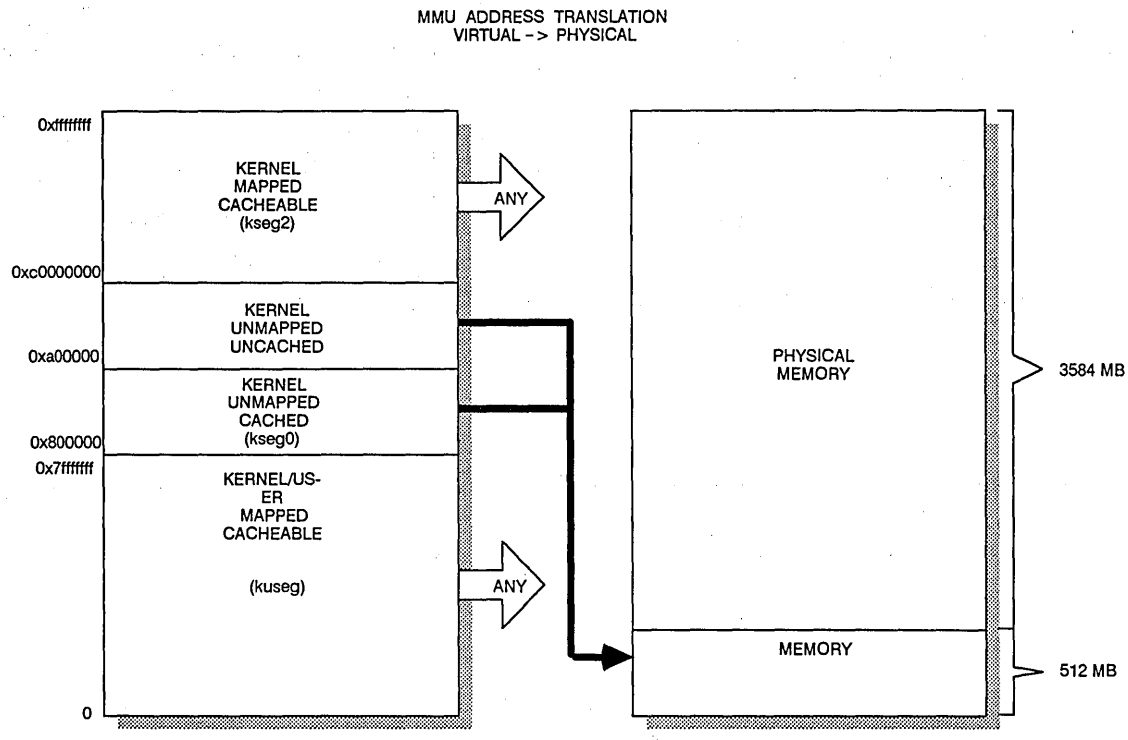


Figure 6. IDT79R3000 Virtual Address Mapping

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2 Gbyte is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. All references to this segment are mapped through the TLB. Use of the cache for up to 64 processes is determined by bit settings for each page within the TLB entries.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512 Mbyte segment use cache memory but are not mapped through the TLB. Instead, they always map to the first 0.5 GBytes of physical address space.
- *kseg1*—references to this 512 Mbyte segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5 GByte segment of physical address space as *kseg0*.
- *kseg2*—references to this 1 Gbyte segment are always mapped through the TLB and use of the cache is determined by bit settings within the TLB entries.

IDT79R3000 Pipeline Architecture

The execution of a single IDT79R3000 instruction consists of five primary steps:

1) **IF** — Fetch the instruction (I-Cache).
2) **RD** — Read any required operands from CPU registers while decoding the instruction.
3) **ALU** — Perform the required operation on instruction operands.
4) **MEM** — Access memory (D-Cache).
5) **WB** — Write back results to register file.

Each of these steps requires approximately one CPU cycle as shown in Figure 7 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

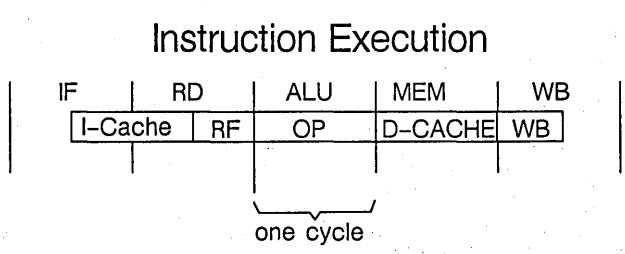


Figure 7. Instruction Execution Sequence

The IDT79R3000 uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 8.

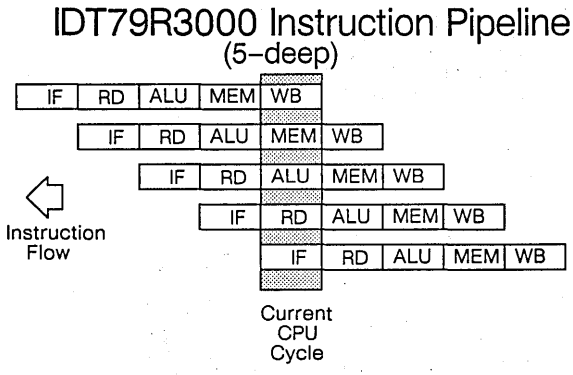


Figure 8. IDT79R3000 Instruction Pipeline

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

The high performance capabilities of the IDT79R3000 processor demand system configurations incorporating techniques frequently employed in large, mainframe computers but seldom encountered in systems based on more traditional microprocessors.

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. This approach to achieving this goal incorporates a number of RISC techniques including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers. Many of the advantages obtained from these techniques can, however, be negated by an inefficient memory system.

Figure 9 illustrates memory in a simple microprocessor system. In this system, the CPU outputs addresses to memory and reads instructions and data from memory or writes data to memory. The address space is completely undifferentiated: instructions, data, and I/O devices are all treated the same. In such a system, a primary limiting performance factor is memory bandwidth.

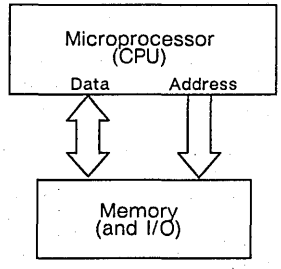


Figure 9. A Simple Microprocessor Memory System

Figure 10 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the IDT79R3000's performance capabilities. The key features of this system are:

- **External Cache Memory**—Local, high-speed memory (called *cache* memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory. Some microprocessors provide a limited amount of cache memory on the CPU chip itself. The external caches supported by the IDT79R3000 can be much larger; while a small cache can improve performance of some programs, significant improvements for a wide range of programs require large caches.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The IDT79R3000 supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU using caches constructed with commercially available IDT static RAM devices.

In order to maximize bandwidth in the cache while minimizing the requirement for SRAM access speed, the R3000 divides a single-processor clock cycle into two phases. During one phase, the address for the data cache access is presented while data previously addressed in the instruction cache is read; during the next phase, the data operation is completed while the instruction cache is being addressed. Thus, both caches are read in a single processor cycle using only one set of address and data pins.

- **Write Buffer**—In order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the IDT79R3000 is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the IDT79R3000 supports an interface to a write buffer. The IDT79R3020 Write Buffer captures data (and associated addresses) output by the CPU and ensures that the data is passed on to main memory.

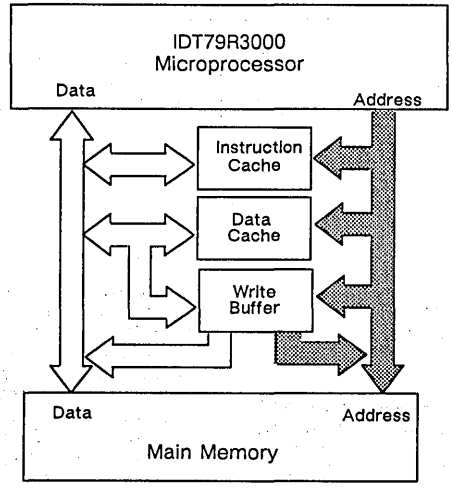


Figure 10. An IDT79R3000 System with a High-Performance Memory System

IDT79R3000 Processor Subsystem Interfaces

Figure 11 illustrates the three subsystem interfaces provided by the IDT79R3000 processor:

- **Cache control** interface (on-chip) for separate data and instruction caches permits implementation of off-chip caches using standard IDT SRAM devices. The 79R3000 directly controls the cache memory with a minimum of external components. Both the instruction and data cache can vary from 0 to 256K Bytes (64 K entries). The 79R3000 also includes the TAG control logic which determines whether or not the entry read from the cache is the desired data.

  The 79R3000 cache controller implements a direct mapped cache for high net performance (bandwidth). It has the ability to refill multiple words when a cache miss occurs, thus reducing the effective miss rate to less than 2% for large caches. When a cache miss occurs, the 79R3000 can support refilling the cache in 1, 4, 8, 16, or 32 word blocks to minimize the effective penalty of having to access main memory. The 79R3000 also incorporates the ability to perform instruction streaming; while the cache is refilling, the processor can resume execution once the missed word is obtained from main memory. In this way, the processor can continue to execute concurrently with the cache block refill.
- **Memory controller** interface for system (main) memory. This interface also includes the logic and signals to allow operation with a write buffer to further improve memory bandwidth. In addition to the standard full word access, the memory controller supports the ability to write bytes and half-words by using partial word operations. The memory controller also supports the ability to retry memory accesses if, for example, the data returned from memory is invalid and a bus error needs to be signalled.

- **Coprocessor Interface**—The IDT79R3000 features a tightly coupled co-processor interface in which all co-processors maintain synchronization with the main processor; reside on the same data bus as the main processor; and participate in bus transactions in an identical manner to the main processor. The IDT79R3000 generates all required cache and memory control signals, including cache and memory addresses for attached coprocessors. As a result, only the data bus and a few control signals need to be connected to a coprocessor.

  The interface supports three types of coprocessor instructions: loads/stores, coprocessor operations, and processor-coprocessor transfers. Note that coprocessor loads and stores occur directly between the coprocessor and memory, without requiring the data to go through the CPU.

  Synchronization between the CPU and external coprocessors is achieved using a Phased-Lock Loop interface to the coprocessor. The coprocessor physical interface also includes coprocessor condition signals (CpCondn), which are used in coprocessor branch instructions, and a coprocessor busy signal (CpBusy) which is used to stall the CPU if the coprocessor needs to hold off subsequent operations.

  Finally, a precise exception interface is defined between the CPU and coprocessors using the external interrupt inputs of the CPU. This allows a coprocessor exception, even if it was the result of a multi-cycle operation, to be traced to the precise coprocessor operation which caused it. This is an important feature for languages which can define specific error handlers for each task.

  The interface supports up to four separate coprocessors. Coprocessor 0 is defined to be the system control coprocessor, and resides on the same chip as the CPU unit. Coprocessor 1 is the Floating Point Accelerator, IDT 79R3010. Coprocessors 2 and 3 are available to support an interface to application specific functions.

Multiprocessing Support

The IDT79R3000 supports multiprocessing applications in a simple but effective way. Multiprocessing applications require cache coherency across the multiple processors. The IDT79R3000 offers two signals to support cache coherency: the first, MPStall, stalls the processor within two cycles of being received and keeps it from accessing the cache. The second signal, MPInvalidate, causes the processor to write data on the data cache bus which indicates the externally addressed cache entry is invalid. Thus, a subsequent access to that location would result in a cache miss, and the data would be obtained from main memory.

The two MP signals would be generated by a external logic which utilizes a secondary cache to perform bus snooping functions. The 79R3000 does not impose an architecture for this secondary cache, but rather is flexible enough to support a variety of application specific architectures and still maintain cache coherency. Further, there is no impact on designs which do not require this feature.

Advanced Features

The IDT79R3000 offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which force cache hits to occur regardless of the contents of the tag fields.

Further features of the IDT79R3000 are configured during the last four cycles prior to the negation of the RESET input. These functions include the ability to select cache sizes and cache refill block sizes; the ability to utilize the multiprocessor interface; whether or not instruction streaming is enabled; whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, etc. Table 3 shows the configuration options selected at Reset. These are further discussed in the "Hardware User's Manual".

Backward Compatibility with 79R2000

The IDT79R3000 can be used in sockets designed for the 79R2000A. The pin-out of the 79R3000 has been selected to ensure this compatibility, with new functions mapped onto previously unused pins. The instruction set is compatible with that of the 79R2000 at the binary level. As a result, code written for the older processor can be executed. New features, such as block refill, instruction streaming, etc. can be selectively disabled.

In most 79R2000A applications, the 79R3000 can be placed in the socket with no modification to initialization settings. The initialization of the 79R3000 includes whether or not the device should operate as a 79R2000A. Systems using 79R2000A would normally have this input configured so that the device would default to this mode. Further application assistance on this topic is available from IDT.

A Special Note on Packaging

Both the flat pack and the PGA packages for the 79R3000 incorporate separate power and ground planes to eliminate noise associated with high frequency operation. This, coupled with the numerous power and ground pins provided on the device, helps to ensure very reliable operation.

INPUT	W CYCLE	X CYCLE	Y CYCLE	Z CYCLE
Int0*	DBlkSize0*	DBlkSize1*	Extend Cache	BigEndian*
Int1*	IBlkSize0*	IBlkSize1*	Reserved	TriState*
Int2*	Reserved	IStream	Reserved	NoCache*
Int3*	Reserved	StorePartial	MultiProcessor	BusDriveOn
Int4*	PhaseDelayOn*	PhaseDelayOn*	PhaseDelayOn*	PhaseDelayOn*
Int5*	R3000 Mode*	R3000 Mode*	R3000 Mode*	R3000 Mode*

Table 3: IDT79R3000 Mode Selectable Features

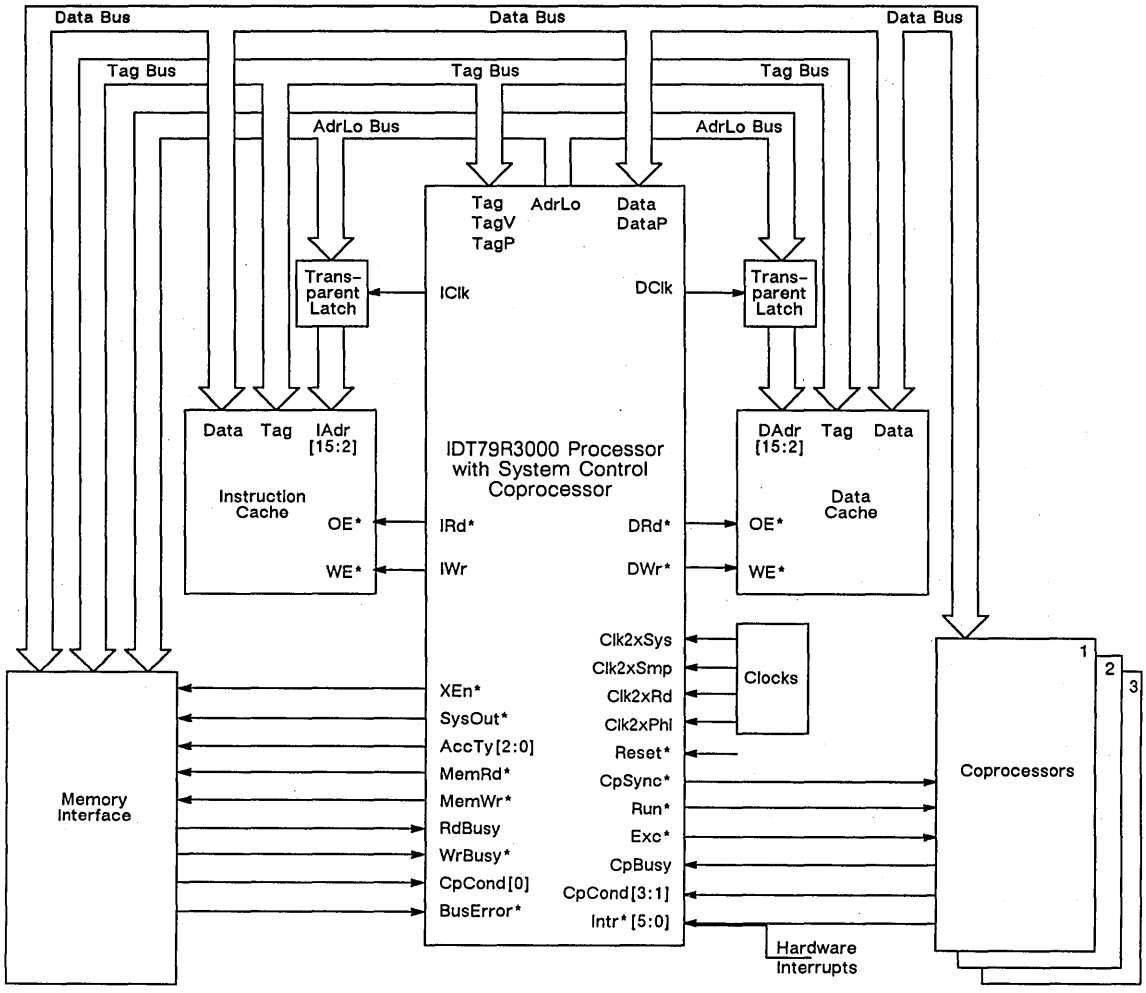
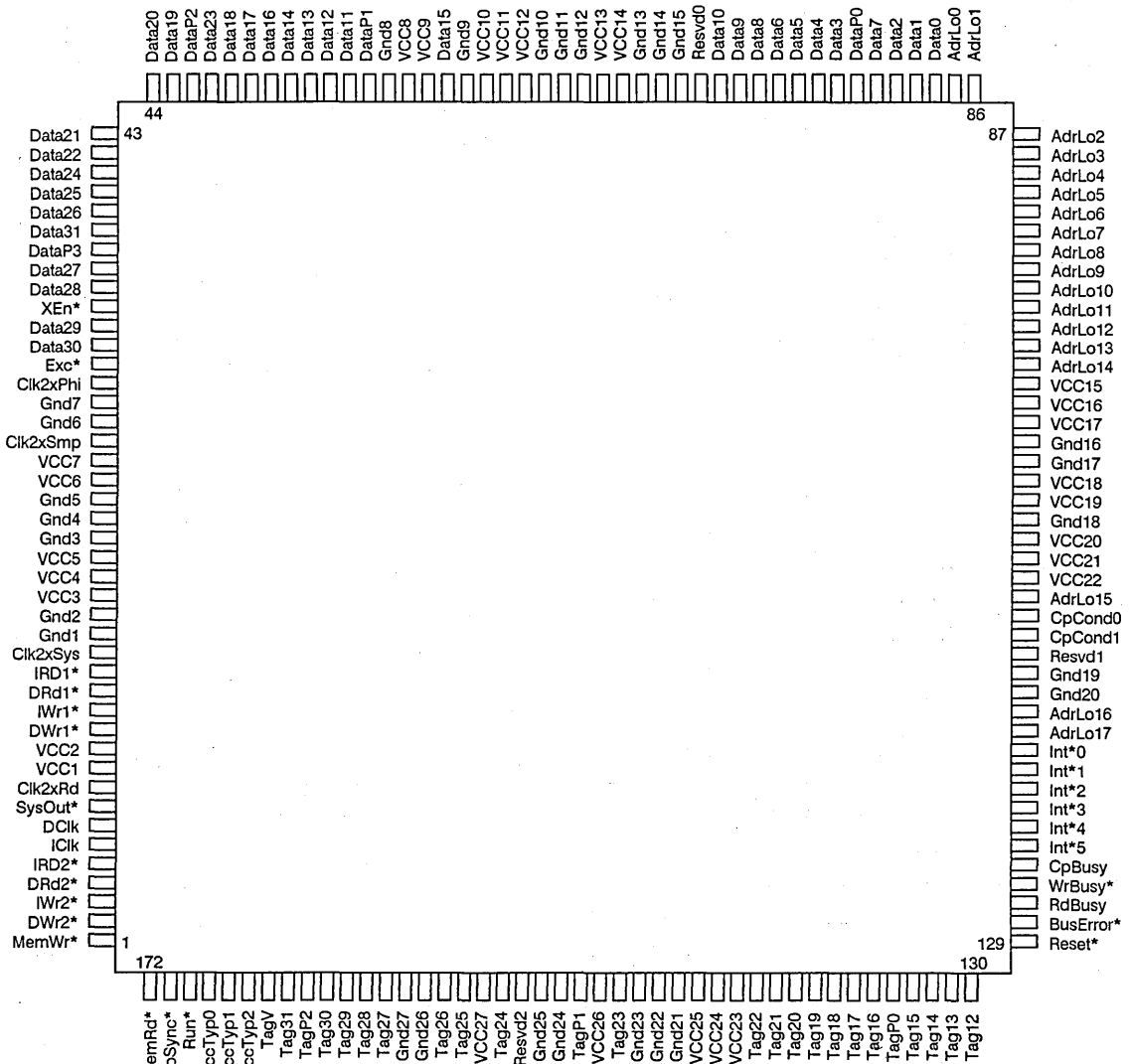


Figure 11. IDT79R3000 Subsystem Interfaces Example; 64 KB Cache

PIN CONFIGURATION

172-PIN CERAMIC FLATPACK
(Cavity Side View)



9

13PIN CONFIGURATION

144-Pin PGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VCC14	AdrLo 6	AdrLo 10	AdrLo 11	VCC12	AdrLo 14	AdrLo 15	CpCond 0	AdrLo (1) 16	AdrLo (1) 17	Intr* 2	Intr* 5	Wr Busy*	Reset*	VCC10
B	AdrLo 3	Drd1*	AdrLo 7	AdrLo 9	AdrLo 12	Ird1*	AdrLo 13	CpCond 1	Intr* 1	Intr* 3	Cp Busy	Bus Error*	Dwr1*	Tag12	Tag15
C	AdrLo 0	AdrLo 4	VCC13	AdrLo 5	AdrLo 8	Gnd13	Gnd12	VCC11	Intr* 0	Intr* 4	Rd Busy	Gnd11	Tag13	TagP0	Tag18
D	Data 1	AdrLo 2	Gnd0										Tag14	Tag17	Tag19
E	DataP 0	Data 0	AdrLo 1										Tag16	Tag20	VCC9
F	VCC0	Data 7	Data 2										Gnd10	Tag21	Tag23
G	Data 4	Data 3	Gnd1										Gnd9	Tag22	TagP1
H	Data 6	Data 5	Data 8										VCC8	Tag25	Tag24
J	Data 10	DataP 1	Data 9										Tag28	Tag29	Tag26
K	Data 15	Data 11	Gnd2										Gnd8	Tag P2	Tag27
L	VCC1	Data 12	Data 17										Acc Typ2	Tag31	Tag30
M	Data 13	Data 16	DataP 2										Gnd7	Acc Typ1	VCC7
N	Data 14	Data 18	Data 19	Gnd3	Data 24	Data P3	VCC3	VCC4	Gnd5	Gnd6	DRd2*	MemWr*	MemRd*	Run*	TagV
P	Data 23	Data 20	IWr1*	Data 22	Data 26	Data 27	XEn*	Data 30	Clk2x Sys	Clk2x Rd	DClk	IRd2*	IWr2*	Cp Sync*	Acc Typ0
Q	VCC2	Data 21	Data 25	Data 31	Data 28	Gnd4	Data 29	Excep tion*	Clk2x Phi	Clk2x Smp	SysOut*	VCC5	IClk	DWr2*	VCC6

NOTE:

1. AdrLo 16 & 17 are multi-function pins which are controlled by mode select programming on interrupt pins at reset time.
   AdrLo16: MP Invalidate, CpCond (2).
   AdrLo17: MP Stall, CpCond (3).

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0-31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors.
DataP (0-3)	I/O	A 4-bit bus containing even parity over the data bus.
Tag (12-31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches, and memory interface.
TagV	I/O	The tag validity indicator.
TagP (0-2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag.
AdrLo (0-17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface. (AdrLo 16: CpCond (2), AdrLo 17: CpCond (3) set by reset initialization).
IRd1*	O	Read enable for the instruction cache.
IWr1*	O	Write enable for the instruction cache.
IRd2*	O	An identical copy of IRd1* used to split the load.
IWr2*	O	An identical copy of IWr1* used to split the load.
IClk	O	The instruction cache address latch clock. This clock runs continuously.
DRd1*	O	The read enable for the data cache.
DWr1*	O	The write enable for the data cache.
DRd2*	O	An identical copy of DRd1* used to split the load.
DWr2*	O	An identical copy of DWr1* used to split the load.
DClk	O	The data cache address latch clock. This clock runs continuously.
XEn*	O	The read enable for the Read Buffer.
AccTyp (0-2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus, whether or not a data transfer is occurring, and the purpose of the transfer.
MemWr*	O	Signals the occurrence of a main memory write
MemRd*	O	Signals the occurrence of a main memory read.
BusError*	I	Signals the occurrence of a bus error during a main memory read or write.
Run*	O	Indicates whether the processor is in the run or stall state.
Exception*	O	Indicates that the instruction about to commit state should be aborted and other exception related information.
SysOut*	O	A reflection of the internal processor clock used to generate the system clock.
CpSync*	O	A clock which is identical to SysOut* and used by coprocessors for timing synchronization with the CPU.
RdBusy*	I	The main memory read stall termination signal. In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read. RdBusy is sampled by the processor only during memory read stalls.
WrBusy*	I	The main memory write stall initiation/termination signal.
CpBusy	I	The coprocessor busy stall initiation/termination signal.
CpCond (0-1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor.
CpCond (2-3)	I	Conditional branch status from coprocessors to the processor. Function is provided on AdrLo 16/17 pins and is selected at reset time.
MPStall	I	Multiprocessing Stall. Signals to the processor that it should stall accesses to the caches in a multiprocessing environment. This is physically the same pin as CpCond2; its use is determined at RESET initialization.
MPInvalidate	I	Multiprocessing Invalidate. Signals to the processor that it should issue invalidate data on the cache data bus. The address to be invalidated is externally provided. This is the same pin as CpCond3; its use is determined at RESET initialization.
Int* (0-5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor. At reset time, mode select values are read in.
Clk2xSys	I	The master double frequency input clock used for generating SysOut*.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors.
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase1 and phase2.
Reset*	I	Synchronous initialization input used to force execution starting from the reset memory address. Reset* must be deasserted synchronously but asserted asynchronously. The deassertion of reset* must be synchronized by the leading edge of SysOut.

ABSOLUTE MAXIMUM RATINGS [1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage [2]	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output sould be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.5	–	0.5	–	0.5	V
V_{OHT}	Output HIGH Voltage [4]	V_{CC} = Min, I_{OH} = -8mA	2.4	–	2.4	–	2.4	–	V
V_{OLT}	Output LOW Voltage [4]	V_{CC} = Min, I_{OL} = 8mA	–	0.8	–	0.8	–	0.8	V
V_{IH}	Input HIGH Voltage [5]		2.0	–	2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage [1]		–	0.8	–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage [2, 5]		3.0	–	3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage [1, 2]		–	0.4	–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max	–	575	–	640	–	700	mA
C_{LD}	Load Capacitance		–	50	–	50	–	50	pF
I_{IH}	Input HIGH Leakage [3]	V_{IH} = V_{CC}	–	10	–	10	–	10	µA
I_{IL}	Input LOW Leakage [3]	V_{IL} = Gnd	-10	–	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and Reset*.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.5	V
V_{OHT}	Output HIGH Voltage (4)	V_{CC} = Min, I_{OH} = -8mA	2.4	–	V
V_{OLT}	Output LOW Voltage (4)	V_{CC} = Min, I_{OL} = 8mA	–	0.8	V
V_{IH}	Input HIGH Voltage (5)		2.0	–	V
V_{IL}	Input LOW Voltage (1)		–	0.8	V
V_{IHS}	Input HIGH Voltage (2, 5)		3.0	–	V
V_{ILS}	Input LOW Voltage (1, 2)		–	0.4	V
C_{IN}	Input Capacitance		–	10	pF
C_{OUT}	Output Capacitance		–	10	pF
I_{CC}	Operating Current	V_{CC} = Max	–	675	mA
C_{LD}	Load Capacitance		–	50	pF
I_{IH}	Input HIGH Leakage (3)	V_{IH} = V_{CC}	–	10	µA
I_{IL}	Input LOW Leakage (3)	V_{IL} = Gnd	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and Reset*.
3. These parameters do not apply to the clock inputs.
4. V_{OHT} and V_{OLT} apply to the bidirectional data and tag busses only. Note that V_{IH} and V_{IL} also apply to these signals.
5. V_{IH} should not be held above V_{CC} + 0.5 volts.

9

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
Clock									
T_{CkHigh}	Input Clock High	Transition < 5ns	12.5	–	10	–	8	–	ns
T_{CkLow}	Input Clock Low	Transition < 5 ns	12.5	–	10	–	8	–	ns
T_{CkP}	Input Clock Period		30	500	25	500	20	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		9	tcyc/4	7	tcyc/4	5	tcyc/4	ns
Run Operation									
T_{DEn}	Data Enable(3)		–	-2	–	-2	–	-1.5	ns
T_{DDis}	Data Disable(3)		–	-1	–	-1	–	-0.5	ns
T_{DVal}	Data Valid	Load = 25pF	–	3	–	3	–	2	ns
T_{WrDly}	Write Delay	Load = 25pF	–	5	–	4	–	3	ns
T_{DS}	Data Set-up		9	–	8	–	6	–	ns
T_{RSDS}	Reset Pin Set-up		15	–	15	–	10	–	ns
T_{DH}	Data Hold		-2.5	–	-2.5	–	-2.5	–	ns
T_{CBS}	CpBusy Set-up		13	–	11	–	9	–	ns
T_{CBH}	CpBusy Hold		-2.5	–	-2.5	–	-2.5	–	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	–	7	–	6	–	5	ns
T_{AT2}	Access Type (2)	Load = 25pF	–	17	–	14	–	12	ns
T_{MWr}	Memory Write	Load = 25pF	–	27	–	23	–	18	ns
T_{Exe}	Exception	Load = 25pF	–	7	–	7	–	5	ns
Stall Operation									
T_{SAVal}	Address Valid	Load = 25pF	–	30	–	23	–	20	ns
T_{SAcTy}	Access Type	Load = 25pF	–	27	–	23	–	18	ns
T_{MRdI}	Memory Read Initiate	Load = 25pF	–	27	–	23	–	18	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	–	7	–	7	–	5	ns
T_{Sd}	Run Terminate	Load = 25pF	–	17	–	15	–	11	ns
T_{Run}	Run Initiate	Load = 25pF	–	7	–	6	–	4	ns
T_{SMWr}	Memory Write	Load = 25pF	–	27	–	23	–	18	ns
T_{SEx}	Exception Valid	Load = 25pF	–	20	–	18	–	15	ns
Reset Initialization									
T_{RST}	Reset Pulse Width		6	–	6	–	6	–	TckP
T_{rstPLL}	Reset timing, Phase-lock on(5)		3000	–	3000	–	3000	–	TckP
T_{rstcp}	Reset timing, Phase-lock off(5)		128	–	128	–	128	–	TckP
Capacitive Load Deration									
CLD	Load Derate		0.5	2	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual."
5. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU.

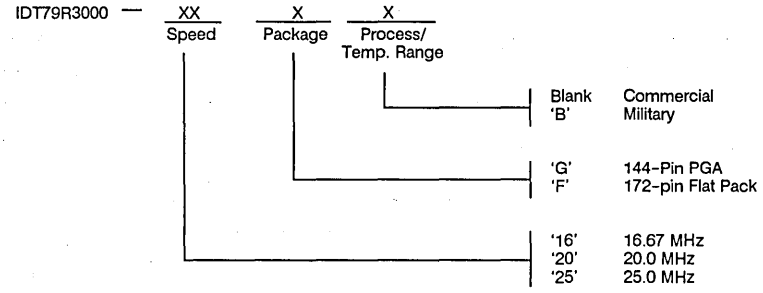
AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
Clock					
T_{CkHigh}	Input Clock High	Transition < 5ns	12.5	–	ns
T_{CkLow}	Input Clock Low	Transition < 5 ns	12.5	–	ns
T_{CkP}	Input Clock Period Clk2xSys to Clk2xSmp Clk2xSmp to Clk2xRd Clk2xSmp to Clk2xPhi		30 0 0 9	500 tcyc/4 tcyc/4 tcyc/4	ns ns ns ns
Run Operation					
T_{DEn}	Data Enable(3)		–	-2	ns
T_{DDis}	Data Disable(3)		–	-1	ns
T_{DVal}	Data Valid	Load = 25pF	–	3	ns
T_{WrDly}	Write Delay	Load = 25pF	–	5	ns
T_{DS}	Data Set-up		9	–	ns
T_{RSDS}	Reset Pin Set-up		15	–	ns
T_{DH}	Data Hold		-2.5	–	ns
T_{CBS}	CpBusy Set-up		13	–	ns
T_{CBH}	CpBusy Hold		-2.5	–	ns
T_{AcTy}	Access Type (1:0)	Load = 25pF	–	7	ns
T_{AT2}	Access Type (2)	Load = 25pF	–	17	ns
T_{MWr}	Memory Write	Load = 25pF	–	27	ns
T_{Exe}	Exception	Load = 25pF	–	7	ns
Stall Operation					
T_{SAVal}	Address Valid	Load = 25pF	–	30	ns
T_{SAcTy}	Access Type	Load = 25pF	–	27	ns
T_{MRdI}	Memory Read Initiate	Load = 25pF	–	27	ns
T_{MRdt}	Memory Read Terminate	Load = 25pF	–	7	ns
T_{Sd}	Run Terminate	Load = 25pF	–	17	ns
T_{Run}	Run Initiate	Load = 25pF	–	7	ns
T_{SMWr}	Memory Write	Load = 25pF	–	27	ns
T_{SEx}	Exception Valid	Load = 25pF	–	20	ns
Reset Initialization					
T_{RST}	Reset Pulse Width		6	–	TckP
T_{rstPLL}	Reset timing, Phase-lock on(5)		3000	–	TckP
T_{rstcp}	Reset timing, Phase-lock off(5)		128	–	TckP
Capacitive Load Deration					
CLD	Load Derate		0.5	2	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual."
5. These parameters apply when the 79R3010 Floating Point Coprocessor is connected to the CPU.

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC FLOATING-POINT ACCELERATOR (FPA)

PRELIMINARY
IDT 79R3010

FEATURES:

- Hardware Support of Single- and Double-Precision Operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- Sustained performance:
  - 7 MFLOPS single precision LINPACK
  - 4 MFLOPS double precision LINPACK
- Cycle Time:
  - 40ns (25MHz)
  - 60ns (16.67MHz)
  - 80ns (12.5MHz)
- Direct, high-speed interface with IDT79R3000 Processor.
- Supports Full Conformance With IEEE 754-1985 Floating-Point Specification.
- Full 64-bit operation using sixteen 64-bit data registers.
- High-speed CEMOS™ technology.
- Pin, function and software compatible with the IDT79R2010A RISC FPA.
- Military product compliant to MIL-STD-883, Class B.
- 32-bit status/control register providing access to all IEEE-Standard exception handling.
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA.
- Overlapped operation of independent floating point ALUs.

DESCRIPTION:

The IDT79R3010 Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000 Processor and extends the IDT79R3000's instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010 FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

This data sheet provides an overview of the features and architecture of the 79R3010 FPA, Revision 2.0. A more detailed description of the operation of the device is incorporated in the "R3000 Family Hardware User's Manual", and a more detailed architectural overview is provided in the "mips RISC Architecture" book, both available from IDT.

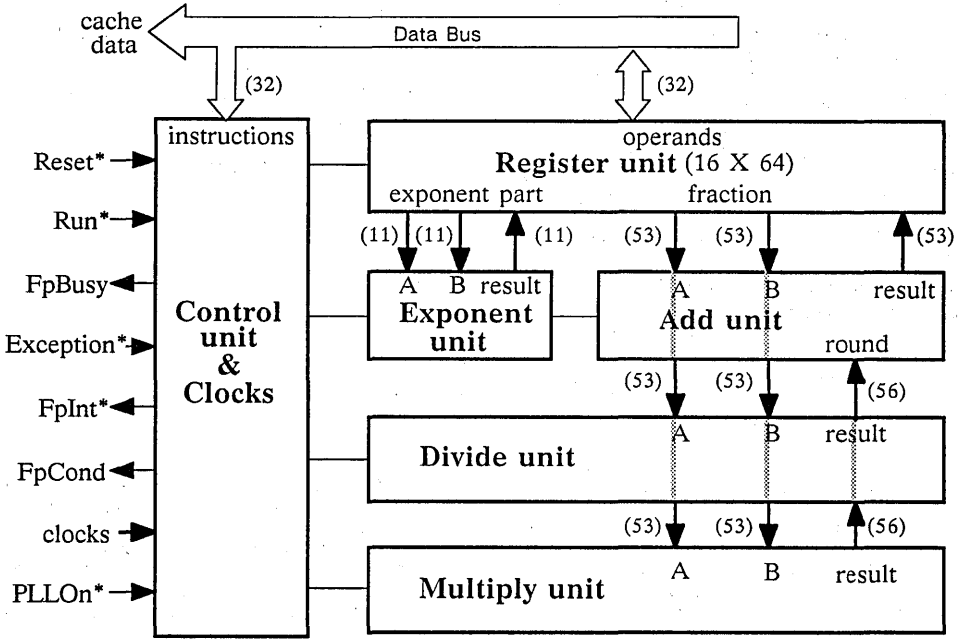


Figure 1. IDT79R3010 Functional Block Diagram

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IDT79R3010 FPA REGISTERS

The IDT79R3010 FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the systems programmers as an extension of the CPU internal registers. The FPA registers are shown in Figure 2.

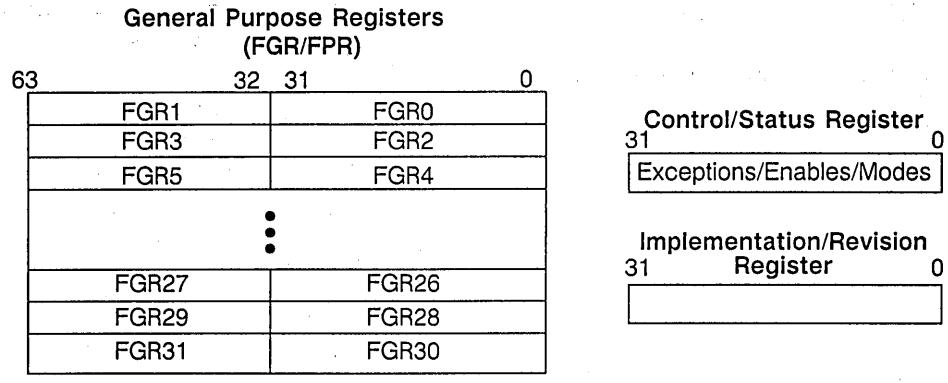


Figure 2. IDT79R3010 FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR).

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R3000 processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R3000 main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R3000 Processor registers and the IDT79R3010 FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

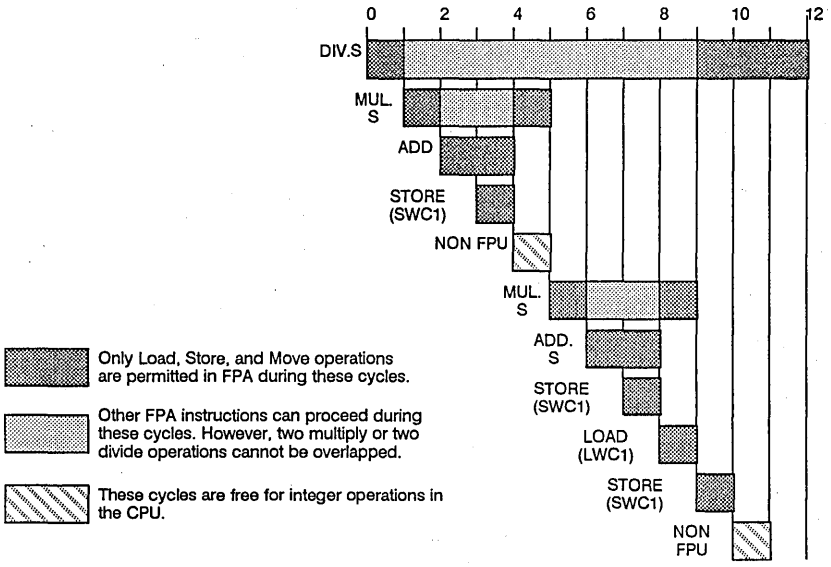


Figure 3: Example of Overlapping Floating Point Operation

Exceptions

The IDT79R3010 FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

INSTRUCTION SET OVERVIEW

All IDT79R3010 instructions are 32 bits long and they can be divided into the following groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA, which is typically used as CpCond1 on the CPU for use in coprocessor branch operations.

Table 1 lists the instruction set of the IDT79R3010 FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	ADD.fmt	Floating-point Add
SWC1	Store Word from FPA	SUB.fmt	Floating-point Subtract
MTC1	Move Word to FPA	MUL.fmt	Floating-point Multiply
MFC1	Move Word from FPA	DIV.fmt	Floating-point Divide
CTC1	Move Control word to FPA	ABS.fmt	Floating-point Absolute value
CFC1	Move Control word from FPA	MOV.fmt	Floating-point Move
		NEG.fmt	Floating-point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating-point Convert to Single FP	C.cond.fmt	Floating-point Compare
CVT.D.fmt	Floating-point Convert to Double FP		
CVT.W.fmt	Floating-point Convert to fixed-point		

Table 1. IDT79R3010 Instruction Summary

IDT79R3010 PIPELINE ARCHITECTURE

The IDT79R3010 FPA provides an instruction pipeline that parallels that of the IDT79R3000 processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R3010 instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the instruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the data on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R3000 main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

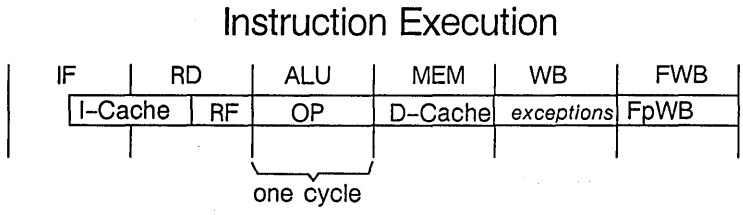


Figure 4. Instruction Execution Sequence

The IDT79R3010 uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

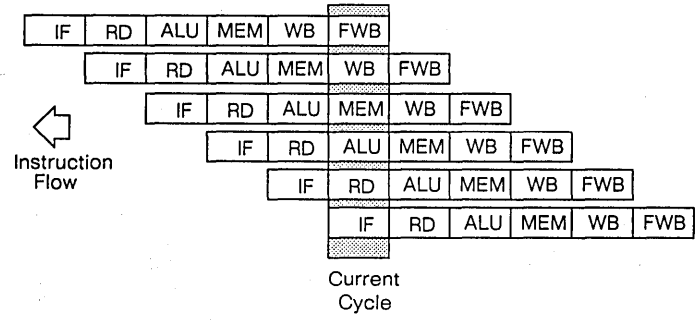
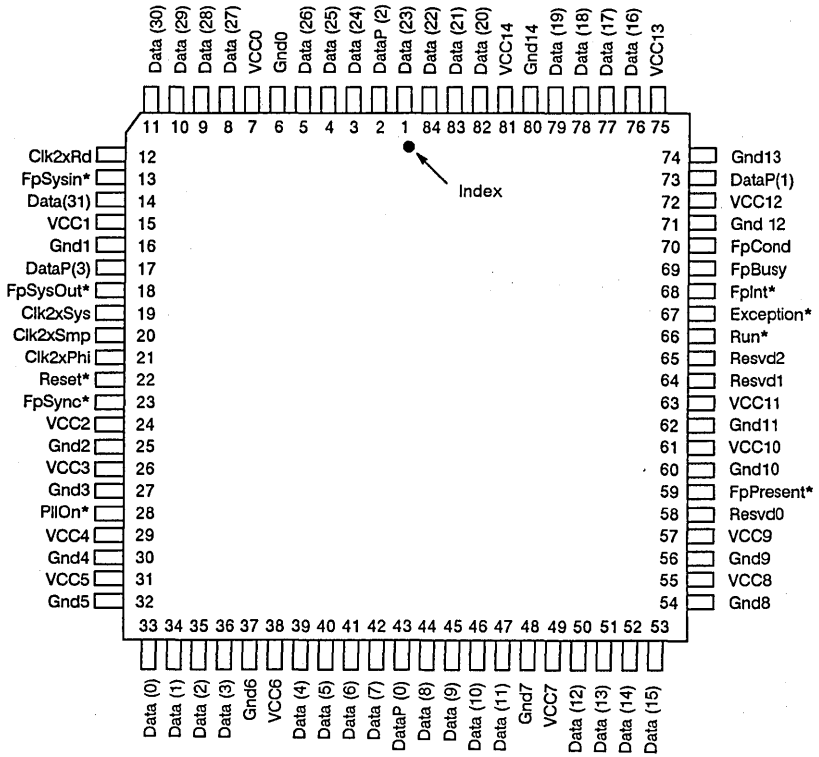


Figure 5. IDT79R3010 Instruction Pipeline

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

PIN CONFIGURATION

(Top View)



84-Pin J Bend CERQUAD

9

PIN CONFIGURATION

84-PIN CPGA FOR 79R3010

PIN GRID ARRAY (Cermamic, Cavity Down) – BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Vcc	Data 17	DataP 1	Vss	FP Cond	FPInt*	Vss	Run*	Rsrvd 1	Vcc	Vss
L	Data 21	Data 20	Data 18	Data 16	Vcc	FPBusy	Excep-tion	Vcc	Rsrvd 2	FP Present *	Data 15	Data 14
K	Vss	Vcc	Data 19							Rsrvd 0	Vcc	Vss
J	Data 23	Data 22									Data 13	Data 12
H	Data 24	DataP 2									Data 11	Data 10
G	Data 26	Data 25									Vcc	Vss
F	Vss	Vcc									Data 8	Data 9
E	Data 27	Data 28									Data 7	DataP 0
D	Data 29	Data 30									Data 5	Data 6
C	Vss	Vcc	Clk2x Rd							Data 2	Vcc	Vss
B	Fp SysIn*	Data 31	DataP 3	Vcc	Clk2x Sys	Vcc	Clk2x Phi	Vcc	PllOn*	Data 1	Data 3	Data 4
A	Vss	Vcc	FpSys Out*	Vss	Clk2x Smp	Vss	Reset*	Vss	FP Sync*	Data 0	Vcc	Vss

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0-31)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP (0-3)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
Run*	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
Exception*	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparison operation.
FpInt*	O	Signal to the CPU indicating that a floating-point exception has occurred for the current FPA instruction.
Reset*	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. Reset* must be synchronized by the leading edge of SysOut from the CPU.
PllOn*	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
FpPresent*	O	Output which is pulled to ground through an impedance of approximately 0.5k ohms. By providing an external pullup on this line an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating FpSysOut*.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2,
FpSysOut*	O	Synchronization clock from the FPA.
FpSysIn*	I	Input used to receive the synchronization clock from the FPA.
FpSync*	I	Input used to receive the synchronization clock from the CPU.

ABSOLUTE MAXIMUM RATINGS (1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage (2)	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns.
   V_{IN} maximum should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.5	–	0.5	–	0.5	V
V_{OLFP}	Output LOW Voltage (5)	V_{CC} = Min, I_{OL} = 1.5mA	–	0.5	–	0.5	–	0.5	V
V_{IH}	Input HIGH Voltage (6)		2.0	–	2.0	–	2.0	–	V
V_{IL}	Input LOW Voltage (1)		–	0.8	–	0.8	–	0.8	V
V_{IHS}	Input HIGH Voltage (2, 6)		3.0	–	3.0	–	3.0	–	V
V_{ILS}	Input LOW Voltage (1, 2)		–	0.4	–	0.4	–	0.4	V
V_{IHC}	Input HIGH Voltage (4, 6)		4.0	–	4.0	–	4.0	–	V
V_{ILC}	Input LOW Voltage (1, 4)		–	0.4	–	0.4	–	0.4	V
C_{IN}	Input Capacitance		–	10	–	10	–	10	pF
C_{OUT}	Output Capacitance		–	10	–	10	–	10	pF
I_{CC}	Operating Current	V_{CC} = Max	–	625	–	675	–	750	mA
C_{LD}	Load Capacitance		–	50	–	50	–	50	pF
I_{IH}	Input HIGH Leakage (3)	V_{iH} = V_{CC}	-10	10	-10	10	-10	10	µA
I_{IL}	Input LOW Leakage (3)	V_{IL} = Gnd	-10	10	-10	10	-10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and Reset*.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to Run* and Exception*.
5. V_{OLFP} applies to the FPPresent* pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.5	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	–	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	–	V
V_{IL}	Input LOW Voltage(1)		–	0.8	V
V_{IHS}	Input HIGH Voltage(2, 6)		3.0	–	V
V_{ILS}	Input LOW Voltage(1, 2)		–	0.4	V
V_{IHC}	Input HIGH Voltage(4, 6)		4.0	–	V
V_{ILC}	Input LOW Voltage(1, 4)		–	0.4	V
C_{IN}	Input Capacitance		–	10	pF
C_{OUT}	Output Capacitance		–	10	pF
I_{CC}	Operating Current	V_{CC} = Max	–	720	mA
C_{LD}	Load Capacitance		–	50	pF
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	-10	10	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = Gnd	-10	10	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	µA

NOTES:

1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, CpBusy, and Reset*.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to Run* and Exception*.
5. V_{OLFP} applies to the FPPresent* pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5 Volts.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
Clock									
T_{CkHigh}	Input Clock High	Transition < 5ns	12	–	10	–	8	–	ns
T_{CkLow}	Input Clock Low	Transition < 5ns	12	–	10	–	8	–	ns
T_{CkP}	Input Clock Period		30	500	25	500	20	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		9	tcyc/4	7	tcyc/4	5	tcyc/4	ns
Timing Parameters									
T_{DEn}	Data Enable(3)		–	-2	–	-2	–	-1.5	ns
T_{DDis}	Data Disable(3)		0	–	0	–	0	–	ns
T_{DVal}	Data Valid	Load = 25pF	–	3	–	3	–	2	ns
T_{DS}	Data Set-up		9	–	8	–	6	–	ns
T_{RsDS}	Reset Set-up		15	–	15	–	10	–	ns
T_{DH}	Data Hold		-2.5	–	-2.5	–	-2.5	–	ns
T_{FpCond}	Fp Condition		–	35	–	30	–	25	ns
T_{FpBusy}	Fp Busy		–	15	–	13	–	10	ns
T_{FpInt}	Fp Interrupt		–	40	–	35	–	25	ns
T_{FpMov}	Fp Move To		–	35	–	30	–	25	ns
T_{ExS}	Exception Set-up		10	–	9	–	7	–	ns
T_{ExH}	Exception Hold		0	–	0	–	0	–	ns
T_{RunS}	Run Set-up		10	–	9	–	7	–	ns
T_{RunH}	Run Hold		-2	–	-2	–	-2	–	ns
Reset Initialization									
T_{rstPLL}	Reset timing, Phase-lock on		3000	–	3000	–	3000	–	TckP
T_{rst}	Reset timing, Phase-lock off		128	–	128	–	128	–	TckP
Capacitive Load Deration									
CLD	Load Derate		0.5	2	0.5	1	0.5	1	ns/25pF

NOTES:

1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual."

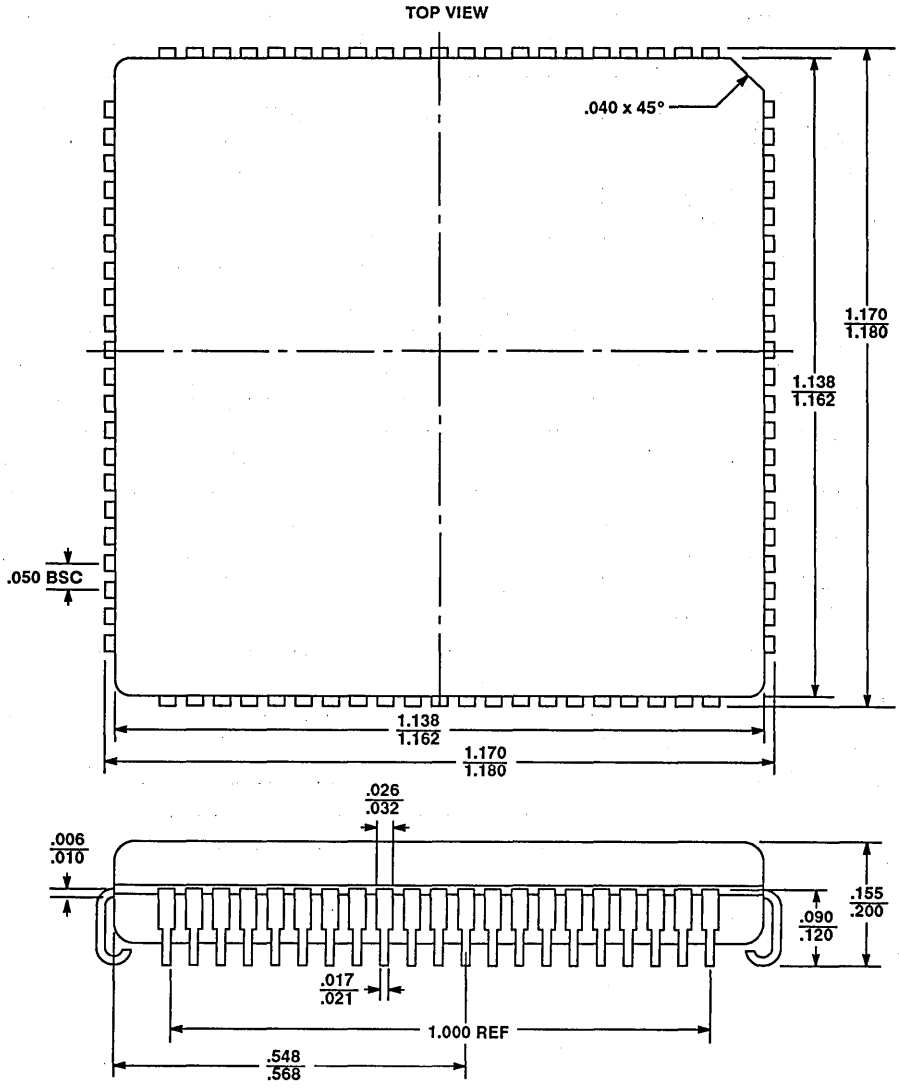
AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
Clock					
T_{CkHigh}	Input Clock High	Transition < 5ns	12	–	ns
T_{CkLow}	Input Clock Low	Transition < 5ns	12	–	ns
T_{CkP}	Input Clock Period		30	500	ns
	Clk2xSys to Clk2xSmp		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi		9	tcyc/4	ns
Timing Parameters					
T_{DEn}	Data Enable(3)		–	-2	ns
T_{DDis}	Data Disable(3)		0	–	ns
T_{DVal}	Data Valid	Load = 25pF	–	3	ns
T_{DS}	Data Set-up		9	–	ns
T_{RsDS}	Reset Set-up		15	–	ns
T_{DH}	Data Hold		-2.5	–	ns
T_{FpCond}	Fp Condition		–	35	ns
T_{FpBusy}	Fp Busy		–	15	ns
T_{FpInt}	Fp Interrupt		–	40	ns
T_{FpMov}	Fp Move To		–	35	ns
T_{ExS}	Exception Set-up		10	–	ns
T_{ExH}	Exception Hold		0	–	ns
T_{RunS}	Run Set-up		10	–	ns
T_{RunH}	Run Hold		-2	–	ns
Reset Initialization					
T_{rstPLL}	"Reset timing, Phase-lock on"		3000	–	TckP
T_{rst}	"Reset timing, Phase-lock off"		128	–	TckP
Capacitive Load Deration					
CLD	Load Derate		0.5	2	ns/25pF

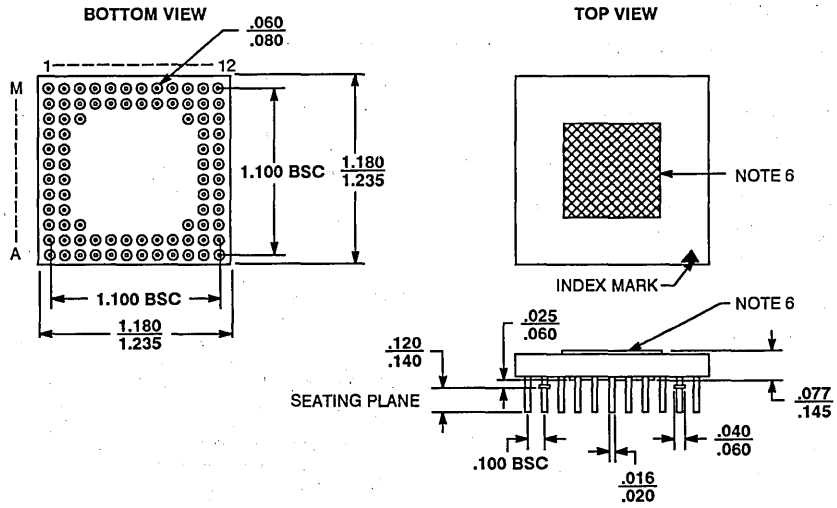
NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. These parameters reference timing diagrams shown in the "Hardware User's Manual."

9

PACKAGE DIMENSIONS
84-LEAD CERQUAD (J BEND)



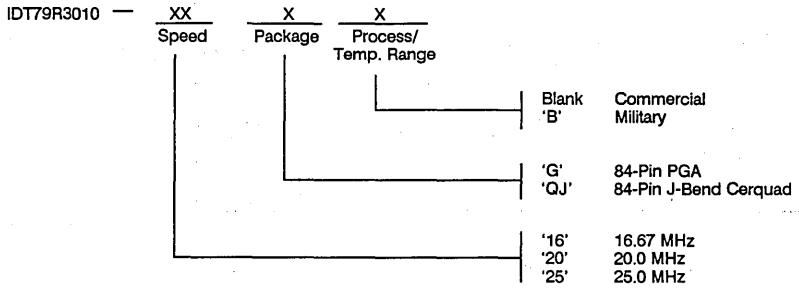
PACKAGE DIMENSIONS
84-PIN PGA (CAVITY DOWN)



NOTES:
1. All dimensions are in inches, unless otherwise specified.
2. BSC—Basic Pin Spacing between centers.
3. Symbol "M" represents the PGA matrix size.
4. Symbol "N" represents the number of pins.
5. Chamferred corners are IDT's option.
6. Cross hatched area indicates integral metallic heat sink.

9

ORDERING INFORMATION



Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

PRELIMINARY
IDT 79R3020

FEATURES

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

Whenever the processor performs a write operation, the Write Buffer captures the output data and its address (including the access type bits). The Write Buffer can hold up to four data-address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-Write Buffer interface
- the Write Buffer-main memory interface
- a miscellaneous, Write Buffer-board control interface.

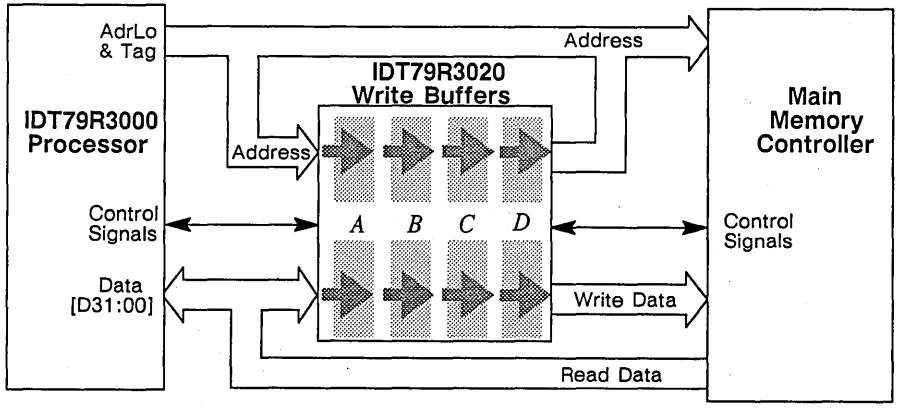


Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System

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DSC-9023/1

WRITE BUFFER - IDT79R3000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the Write Buffer interface to the IDT79R3000 (all descriptions assume that four IDT79R3020 Write Buffers are used to implement a 32-bit, buffered interface). The AdrLo bus and Tag bus bits from the processor are both connected to the Write Buffer to form a 32-bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the Write Buffer. The paragraphs that follow describe the Write Buffer-processor interface signals and the timing of processor-to-Write Buffer data transfers.

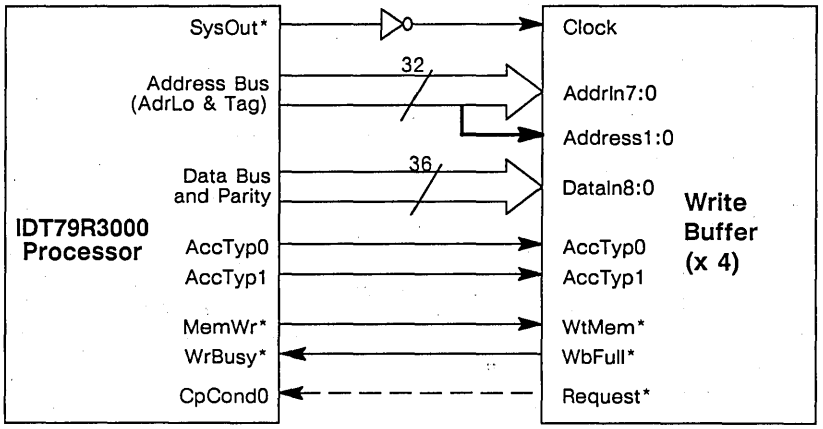


Figure 2. Write Buffer-IDT79R3000 Processor Interface

Write Buffer-Processor Interface Signals

Clock

An inverted version of the IDT79R3000's SysOut* signal from the IDT79R3000 processor that synchronizes data transfers. The Write Buffer uses the trailing edge of *Clock* to latch the contents of the AdrLo bus and uses the leading *Clock* edge to latch the contents of the Data and Tag buses.

DataIn8:0

Nine input data lines from the IDT79R3000 processor's Data bus (eight bits of data and one bit of parity).

AddrIn7:0

Eight input address lines from the IDT79R3000 processor. The address lines are taken from the AdrLo and Tag buses.

Address1:0

The two least significant address bits from the IDT79R3000 processor. These two address bits must be connected to all four Write Buffers and are used in conjunction with the access type (*AccTyp1:0*) signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular Write Buffer.

AccTypIn1:0

The access type signals from the IDT79R3000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

WtMem*

This input is connected to the MemWr* signal from the IDT79R3000 processor that is asserted whenever the processor is performing a store (write) operation.

Request*

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The Request* signal can also be connected to the CpCond0 input of the IDT79R3000 and can then be tested by software to determine if there is any data in the Write Buffer. Since Request* is deasserted if there is no data in the Write Buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

WbFull*

The Write Buffer asserts this signal to the IDT79R3000's WrBusy* input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R3000 processor performs a write-busy stall if it needs to store data while the WbFull*/WrBusy* signal is asserted.

Data & Address Connections

Figure 3 illustrates how four Write Buffers are connected to the address and data outputs of the IDT79R3000 processor.

Address Inputs

Each Write Buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R3000's AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R3000's Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to Write Buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

Data Inputs

Each Write Buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R3000's Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits

connected to the device. This arrangement is required since data selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later.

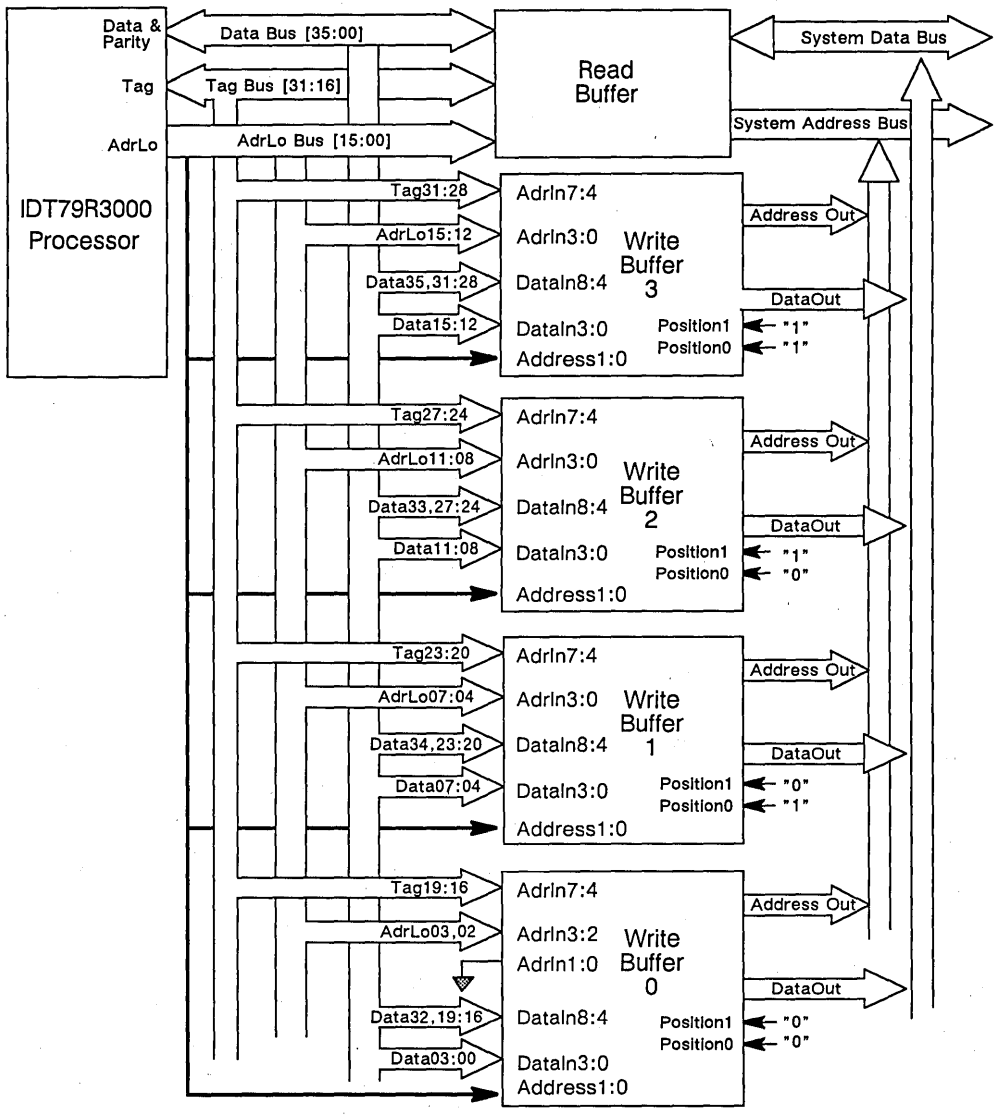


Figure 3. Write Buffer Data and Address Line Connections

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

Write Buffer - Processor Timing

Transfers between the processor and the Write Buffers occur synchronously: the Clock signal from the processor is input to the Write Buffers and used to clock the address and data information into the Write Buffers' latches. Figure 4 illustrates the timing for the processor-Write Buffer interface.

When the WrtMem* signal is asserted, the low-order address bits, and the Address 1:0 inputs, are latched on the trailing edge of the Clock signal (1). The rising edge of Clock (2) is used to latch the high-order address bits, the access type inputs and the contents of the data bus.

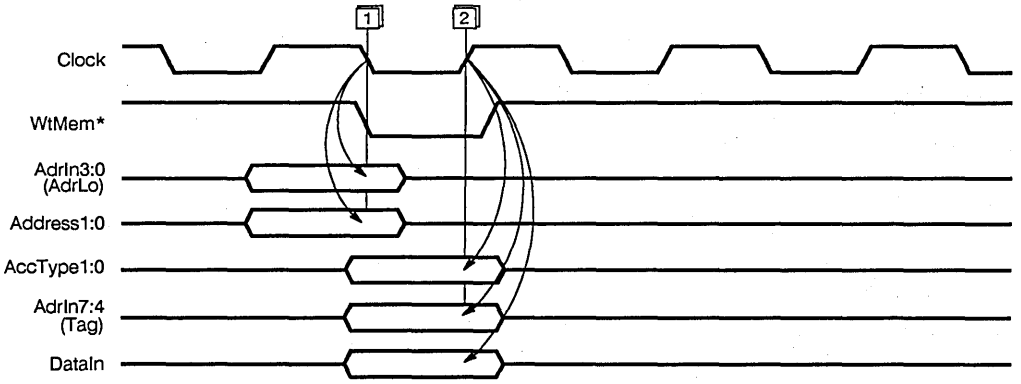


Figure 4. Processor—Write Buffer Interface Timing

WRITE BUFFER - MAIN MEMORY INTERFACE

Figure 5 shows the signals comprising the Write Buffer interface to main memory. This interface is essentially decoupled from the Write Buffer-processor interface: although some synchronization of the memory interface signals and the Clock signal is required, the handshaking signals in this interface have no direct connection to the operation of the Write Buffer-processor interface.

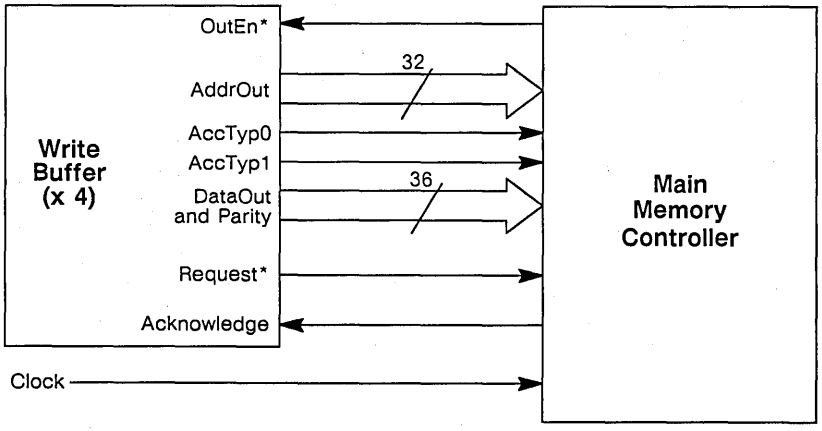


Figure 5. Write Buffer-Main Memory Interface

Write Buffer - Main Memory Interface Signals

Each Write Buffer provides the following signals that comprise the interface to a main memory controller:

AddrOut 7:0

Eight address line output from each Write Buffer.

DataOut 8:0

Nine data lines from each Write Buffer (eight bits of data and one bit of parity).

AccTyp 1:0

The access type signals from the Write Buffer specifying the size of a data access: word, tri-byte, half-word, or byte.

OutEn*

The memory controller asserts this write input to enable the tri-state outputs of the IDT79R3020 address and data signals.

Request*

The Write Buffer asserts this signal to inform the main memory system that it has data to be written to memory.

Acknowledge

The main memory system asserts this signal when it has captured the data presented by the Write Buffer on the DataOut lines.

Write Buffer - Main Memory Interface Timing

Figure 6 illustrates the timing for the transfer of data from the Write Buffer to the main memory system. The sequence illustrated in this figure is as follows:

1. When the Write Buffer has a data-address pair for transfer to the memory system, it asserts the Request* signal.
2. When memory system is ready to handle the Write Buffer data, it asserts the OutEn* signal to enable the Write Buffers' address and data outputs onto the system buses.
3. When memory system no longer requires the Write Buffer address and data outputs, it asserts the Acknowledge signal. The Write Buffer responds to this signal by discarding the address-data pair that was just output.
4. The memory system can deassert the OutEn* signal to return the Write Buffers' address and data outputs to their tristate condition.
5. Since the Request* signal remains asserted, the memory system asserts the OutEn* signal again to enable the next address-data pair onto the system buses.
6. When memory system has accepted the second address-data pair, it again asserts the Acknowledge signal. If the Write Buffer is now empty, it responds to this signal by deasserting the Request* signal.

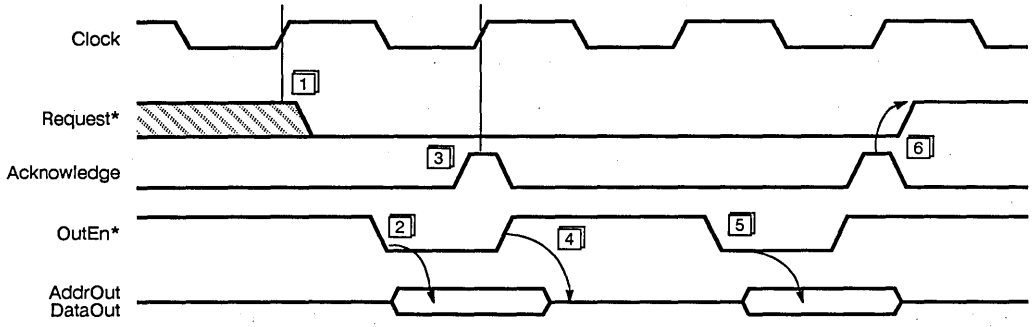


Figure 6. Write Buffer—Main Memory Interface Timing

Note that the buffer's interface to main memory is not completely asynchronous: assertion of the Request* signal by the Write Buffer is synchronized with the rising edge of Clock, and the Acknowledge signal input by main memory has a minimum set up and hold time in relation to the Clock signal.

MISCELLANEOUS WRITE BUFFER - BOARD LOGIC INTERFACE

The Write Buffers support several functions that utilize signals that do not fit neatly into the descriptions of either the processor or main memory interfaces. These functions and signals typically involve miscellaneous logic on a CPU board and include the following:

- byte gathering
- configuration connections (Big Endian, Position 1:0)
- address matching logic
- error address latch logic

The sections that follow describe each of these categories.

Byte Gathering

The Write Buffers perform byte (half-word, tri-byte and word) gathering to decrease the number of write transfers to same location; that is, sequential writes to the same WORD address have their data combined into the same address-data pair buffer.

Byte gathering is prohibited in the address-data pair that is currently available to the memory controller. Thus, the first write into an empty Write Buffer will not have subsequent writes gathered into it because it is currently available for output to memory. Writes to the same location (byte) may be overwritten in the Write Buffer if the gathering is not prohibited by the preceding rule.

The Write Buffers present address-data pairs to the main memory controller in the sequence in which they were received from the processor except in the case of gathered data, where bytes or half words can be collected and written to main memory in a single write operation. If the address-data pair buffer is scheduled to be output, then gathering is inhibited and the buffer contents are presented to the main memory controller. Subsequent writes are then placed in another buffer. No reliance should be placed in any aspect of gathering (except that it only involves sequential writes to the same word address) as it is not readily deterministic. Non-sequential writes to the same word address are not gathered.

Note that gathering can require that two main memory controller references be used to empty a single Write Buffer entry. For example, this can occur if Bytes 0 and 3 of a word are sequentially written. Where order in writing is important, such as in I/O controllers, software should avoid sequential accesses to the same word. In cases where write-read access ordering is important but reading of the write location is not desired, such as during I/O, then a write followed by a write to a dummy location followed by a read of the dummy location will insure the first write has occurred before continuing. Alternatively, the REQUEST signal can be tested to determine that the Write Buffer is empty.

Configuration Logic Connections

Because of their byte gathering capability, each buffer device internally maintains a record of each valid byte in an address/data pair. To do this, each device must have a way of determining which data bits within a word it is handling. The following signals determine how the write buffers handle data that is written to the devices:

- *Position 1, Position 0* - these signals (in conjunction with Big Endian*) determine how each Write Buffer decodes the Address 1/0 and AccType 1/0 to determine if it should store the data inputs. Refer to Figure 3 for an illustration of how data bits are assigned to Write Buffer devices based on their *position*.
- *Big Endian** - When asserted, byte 0 is the leftmost, most significant byte (big-endian): when deasserted, byte 0 is the rightmost, least-significant byte (little-endian).
- *Address 1, Address 0* - these signals (taken from the AdrLo bus) must be connected to all buffer devices since they determine which byte within a word is being accessed.

- *AccType 1, AccType 0* - these inputs signals specify the data size of a write operation as shown in Table 1.

Table 1 shows how these signals operate to specify how bytes are saved within the Write Buffers.

Access Type 1 0	Address 1 0	Bytes Accessed: 31 Big-Endian 0	Bytes Accessed: 31 Little-Endian 0
1 1 (word)	0 0	0 1 2 3	3 2 1 0
1 0 (triple-byte)	0 0	0 1 2	2 1 0
	0 1	1 2 3	3 2 1
0 1 (halfword)	0 0	0 1	1 0
	1 0	2 3	3 2
0 0 (byte)	0 0	0	0
	0 1	1	1
	1 0	2	2
	1 1	3	3

Table 1. Byte Specifications for Write Operations

The lower two address bits of the device in position zero (as determined by the two POSITION inputs) are inhibited; that is, they are not stored directly as they are output on the AdrLo bus. Instead, on output, the lower two address bits are generated from the indication of the positions of the valid data bytes as determined by above table.

MatchOut/Matchin Logic and Read Conflicts

Whenever the processor references main memory (either a write or a read reference), the Write Buffers compare the word address from the CPU with the word addresses stored in the buffers. If any word address matches, the buffers asserts signals that can be used by the main memory controller to ensure that the Write Buffer is emptied before the read access with the conflicting address has been performed.

Figure 7 illustrates the Write Buffer signals involved in address comparison logic. Each write buffer provides four output signals (MatchOut A, B, C, and D) which correspond to the four buffer ranks (A, B, C, D) in each device as shown in Figure 1. These MatchOut signals can be externally NAND'ed as shown in Figure 7 to determine if the address being input matches those in any rank of the Write Buffer.

9

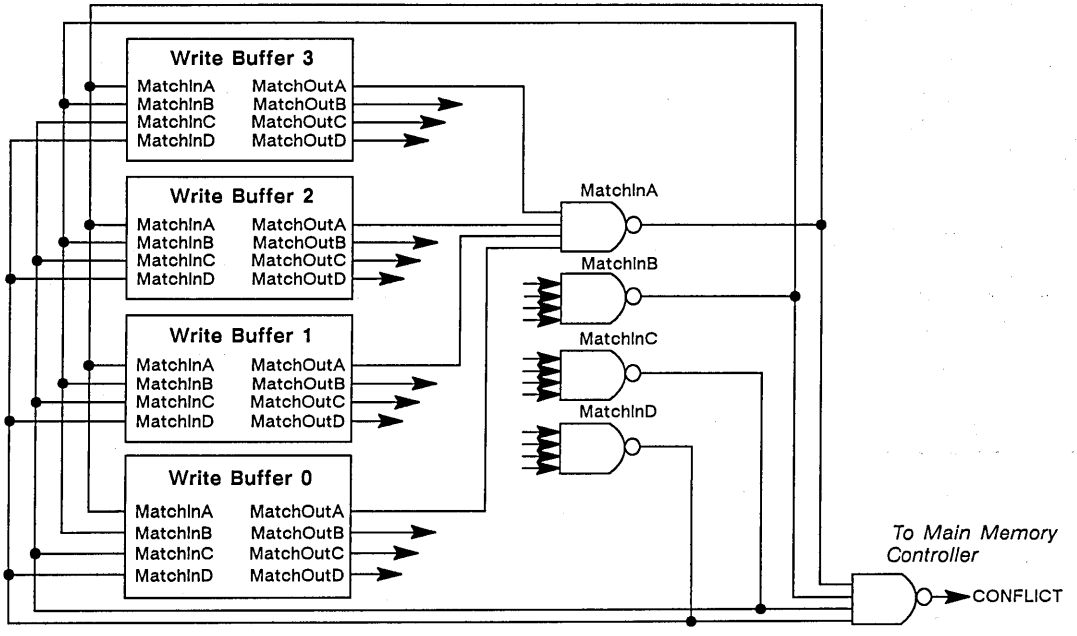


Figure 7. Write Buffer MatchOut/MatchIn Logic

The outputs of the NAND gates are fed into Write Buffers via the MatchIn A, B, C, and D signals and are used within each device as part of the byte gathering logic. The NAND gate outputs can be NAND'ed together as shown in Figure 7 with the resultant signal used (in conjunction with the processor's MEMRD signal) to alert the main memory controller logic that there is a pending buffered write that conflicts with a just-issued read. The main memory controller can then delay the read access until the Request signal is deasserted indicating that the Write Buffer has been emptied.

Error Address Latch

The write buffer incorporates an internal latch that can be loaded with one of the buffered addresses and subsequently enabled out onto the data lines. This feature can be used by error handling routines to read an address back from the Write Buffer and analyze or recover from certain bus errors. Figure 8 shows the signals involved in operation of this latch.

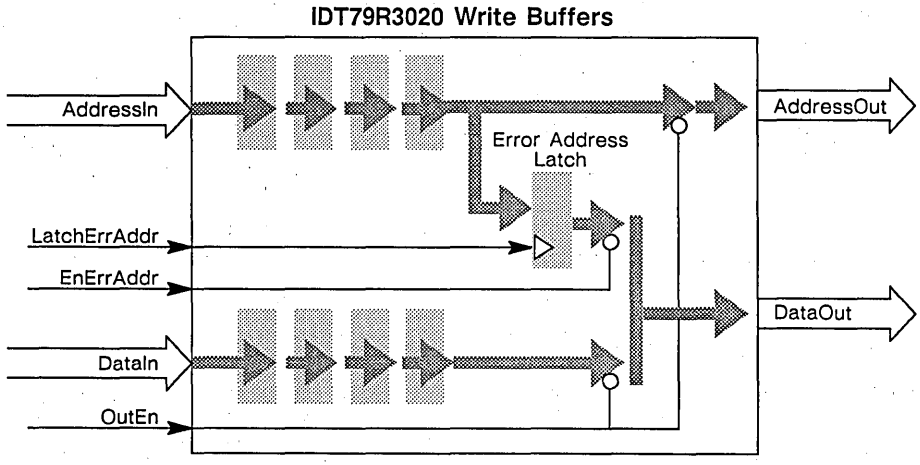


Figure 8. The Write Buffer Error Address Latch

When the LatchErrAddr signal is asserted, the address currently available to the address outputs of the Write Buffer is latched into the internal latch. This address can then be output on the DataOut lines by asserting the EnErrAdr signal so that the processor can read the address in as data. Refer to the AC specifications for timing parameters of the signals associated with the error address latch.

ABSOLUTE MAXIMUM RATINGS (1, 3)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage (2)	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} maximum should not exceed V_{CC} + 0.5 volts.
3. Not more than one output should be shorted at a time. Duration to the short should no exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to 70°C, V_{CC} = +5.0 V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.4	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage(1)		2.4	–	2.4	–	2.4	–	V
V_{IL}	Input LOW Voltage(2)		–	0.8	–	0.8	–	0.8	V
C_{IN}	Input Capacitance		10	–	10	–	10	–	pF
C_{OUT}	Output Capacitance		10	–	10	–	10	–	pF
I_{CC}	Operating Current	V_{CC} = Max	–	50	–	60	–	70	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	–	10	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = Gnd	-10	–	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	-40	40	µA

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to 125°C, V_{CC} = +5.0 V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -4mA	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	–	0.4	V
V_{IH}	Input HIGH Voltage(1)		2.4	–	V
V_{IL}	Input LOW Voltage(2)		–	0.8	V
C_{IN}	Input Capacitance		10	–	pF
C_{OUT}	Output Capacitance		10	–	pF
I_{CC}	Operating Current	V_{CC} = Max	–	90	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = Gnd	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	µA

NOTES:

1. V_{IH} should be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 Volts for longer periods.

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5.0 V ± 5%

SYMBOL	PARAMETER	16.67 MHz MIN.	16.67 MHz MAX.	20.0 MHz MIN.	20.0 MHz MAX.	25.0 MHz MIN.	25.0 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	–	7	–	6	–	ns
t2	Addrin (3:0) from Clock falling hold	4	–	4	–	4	–	ns
t3	Address 1:0 to Clock falling setup	8	–	7	–	6	–	ns
t4	Address 1:0 from Clock falling hold	4	–	4	–	4	–	ns
t5	Access Type 1:0 to Clock rising setup	7	–	6	–	5	–	ns
t6	Access Type 1:0 from Clock rising hold	3	–	3	–	2	–	ns
t7	Addrin (7:4) to Clock rising setup	7	–	5	–	5	–	ns
t8	Addrin (7:4) from Clock rising hold	3	–	3	–	2	–	ns
t9	DataIn (8:0) to Clock rising setup	7	–	5	–	5	–	ns
t10	DataIn (8:0) from Clock rising hold	3	–	3	–	2	–	ns
t11	WrtMem* to Clock rising setup	10	–	8	–	7	–	ns
t12	WrtMem* from Clock rising hold	6	–	5	–	4	–	ns
t13	Request from Clock rising	–	32	–	30	–	27	ns
t14	Acknowledge to Clock rising setup	12	–	11	–	10	–	ns
t15	Acknowledge from Clock rising hold	7	–	6	–	5	–	ns
t16	LatchErrAdr to Acknowledge rising	5	–	5	–	5	–	ns
t17	WbFull* active from Clock rising	–	32	–	30	–	27	ns
t18	WbFull* inactive from Clock rising	–	32	–	30	–	27	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	25	–	24	–	23	ns
t22	MatchIn (ABCD) to Clock rising setup	10	–	9	–	8	–	ns
t23	MatchIn (ABCD) from Clock rising hold	3	–	3	–	3	–	ns
t24	EnErrAdr* to Data (error latch) valid	2	15	2	15	2	15	ns
t25	EnErrAdr* to Data (error latch) tri-state	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	–	32		30	–	27	ns
t27	Reset* to Clock rising, set-up	8	–	7	–	5	–	ns
t28	Reset* from Clock rising, hold	3	–	2	–	1	–	ns
t29	Reset low pulse width	10	–	10	–	10	–	ns
t30	WbFull* High from Clock rising (after Reset*)	3	22	3	21	3	20	ns
t31	Request* High from Reset* low	3	20	3	19	3	18	ns
t32	Access Type 1:0 low from Reset* low	3	28	3	26	3	25	ns
t33	Match Out (ABCD) Low from Reset* low	3	21	3	20	3	20	ns

AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to 125°C, V_{CC} = +5.0V ± 10%

SYMBOL	PARAMETER	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
t1	Addrin (3:0) to Clock falling setup	8	–	ns
t2	Addrin (3:0) from Clock falling hold	4	–	ns
t3	Address 1:0 to Clock falling setup	8	–	ns
t4	Address 1:0 from Clock falling hold	4	–	ns
t5	Access Type 1:0 to Clock rising setup	7	–	ns
t6	Access Type 1:0 from Clock rising hold	3	–	ns
t7	Addrin (7:4) to Clock rising setup	7	–	ns
t8	Addrin (7:4) from Clock rising hold	3	–	ns
t9	DataIn (8:0) to Clock rising setup	7	–	ns
t10	DataIn (8:0) from Clock rising hold	3	–	ns
t11	WrtMem* to Clock rising setup	10	–	ns
t12	WrtMem* from Clock rising hold	6	–	ns
t13	Request from Clock rising	–	32	ns
t14	Acknowledge to Clock rising setup	12	–	ns
t15	Acknowledge to Clock rising hold	7	–	ns
t16	LatchErrAdr to Acknowledge rising	5	–	ns
t17	WbFull* active from Clock rising	–	32	ns
t18	WbFull* inactive from Clock rising	–	32	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	25	ns
t22	MatchIn (ABCD) to Clock rising setup	10	–	ns
t23	MatchIn (ABCD) from Clock rising hold	3	–	ns
t24	EnErrAdr* to Data (error latch) valid	2	15	ns
t25	EnErrAdr* to Data (error latch) tri-state	2	15	ns
t26	Address/Data out from Clock rising	–	32	ns
t27	Reset* to Clock rising, set-up	8	–	ns
t28	Reset* from Clock rising, hold	3	–	ns
t29	Reset low pulse width	10	–	ns
t30	WbFull* High from Clock rising, (after Reset*)	3	22	ns
t31	Request* High from Reset* low	3	20	ns
t32	Access Type 1:0 Low from Reset* low	3	28	ns
t33	Match Out (ABCD) Low from Reset* low	3	21	ns

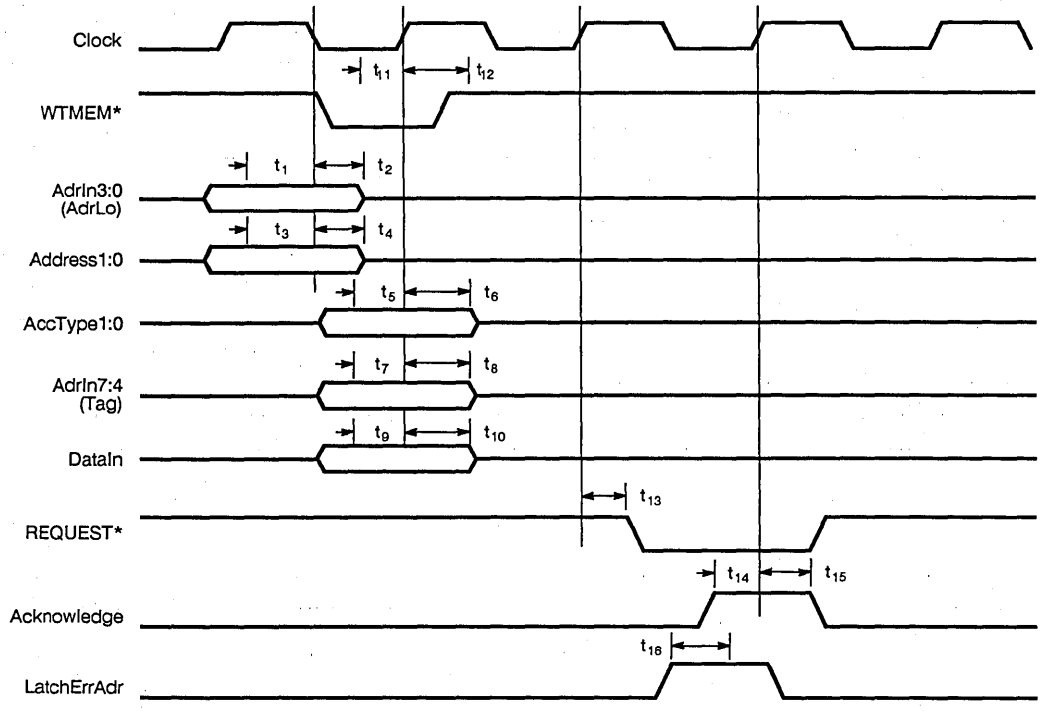


Figure 9. Write Buffer Timing Specifications

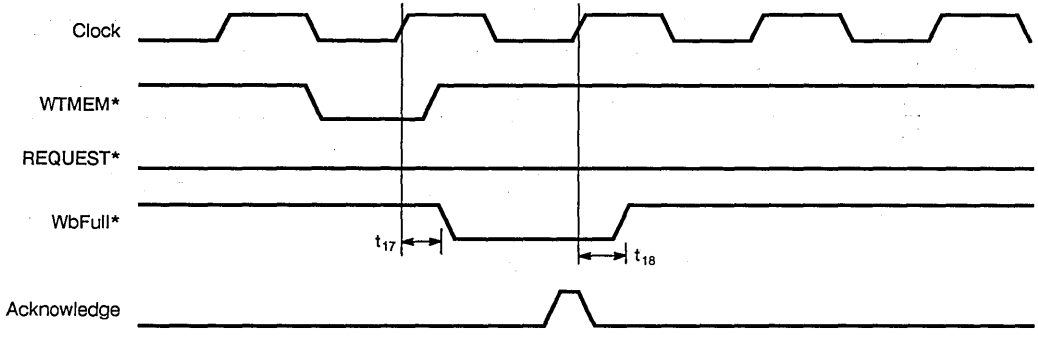


Figure 10. WBFULL* Signal Timing Specifications

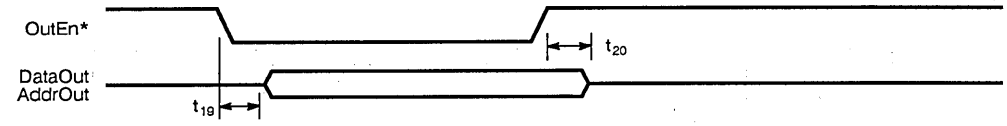


Figure 11. OUTEN* Timing Specifications

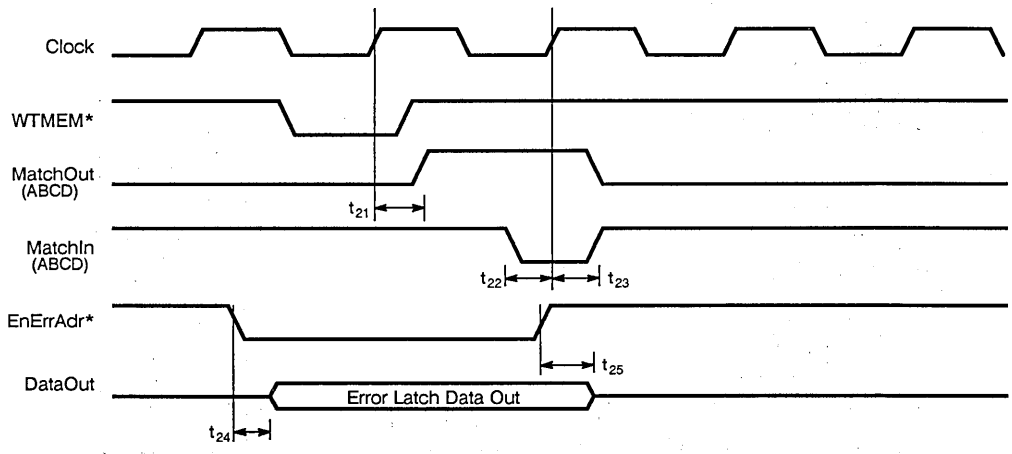


Figure 12. Match and Error Latch Timing Specifications

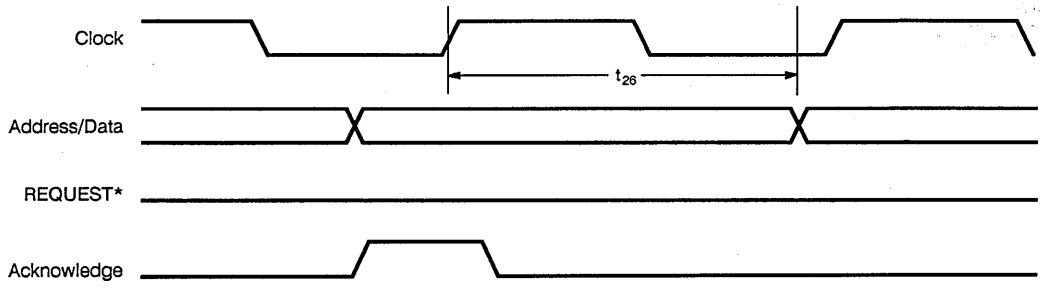


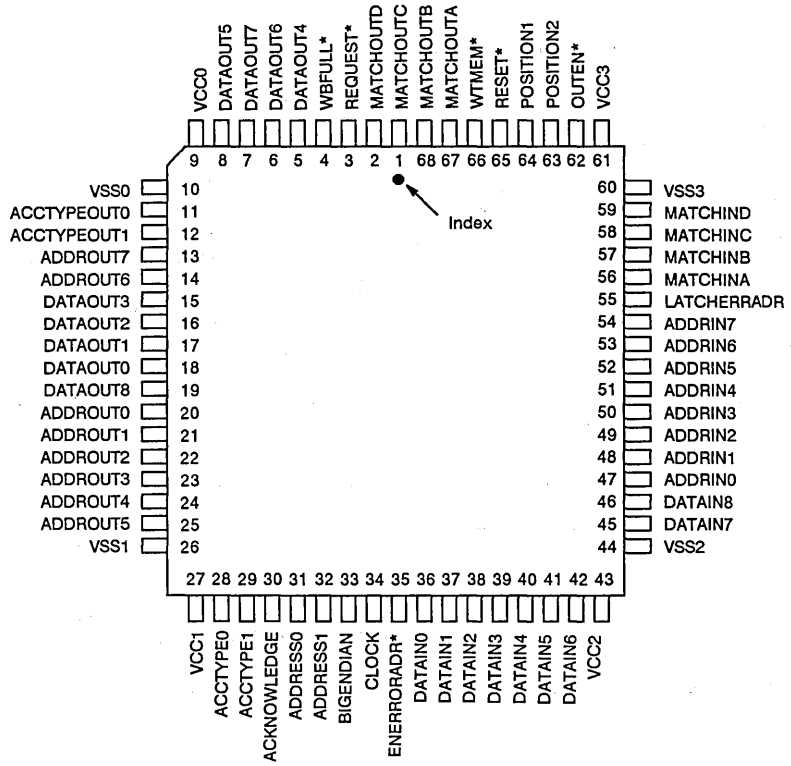
Figure 13. Address/Data Out

68-Pin CPGA for R3020
Pin Grid Array (Ceramic) – Bottom View

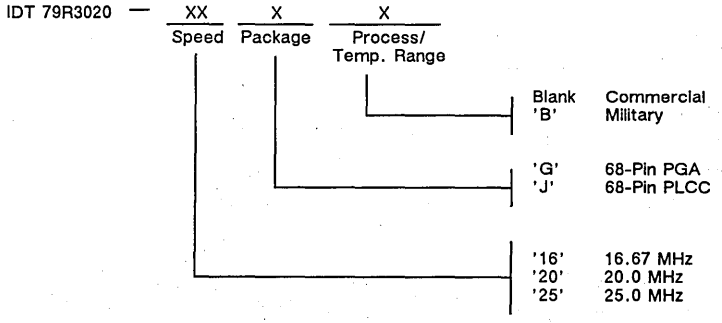
	1	2	3	4	5	6	7	8	9	10	11
L		ACC-TYPE0	AC-KNOWL-EDGE	AD-DRESS1	CLOCK	DATA-IN0	DATA-IN2	DATA-IN4	DATA-IN6	VCC2	
K	GND1	VCC1	ACC-TYPE1	AD-DRESS0	BIGEN-DIAN	EN-ERROR-ADR *	DATA-IN1	DATA-IN3	DATA-IN5	GND2	DATA-IN7
J	ADDR-OUT5	ADDR-OUT4								DATA-IN8	ADDR-IN0
H	ADDR-OUT3	ADDR-OUT2								ADDR-IN1	ADDR-IN2
G	ADDR-OUT1	ADDR-OUT0								ADDR-IN3	ADDR-IN4
F	DATA-OUT8	DATA-OUT0								ADDR-IN5	ADDR-IN6
E	DATA-OUT1	DATA-OUT2								ADDR-IN7	LATCH-ERR-ADR
D	DATA-OUT3	ADDR-OUT6								MATCH-INA	MATCH-INB
C	ADDR-OUT7	ACC-TYPE OUT1								MATCH-INC	MATCH-IND
B	ACC-TYPE OUT0	GND0	DATA-OUT7	DATA-OUT4	RE-QUEST *	MATCH-OUTC	MATCH-OUTA	RESET *	PO-SITION0	VCC3	GND3
A		VCC0	DATA-OUT5	DATA-OUT6	WBFULL *	MATCH-OUTD	MATCH-OUTB	WTMEM *	PO-SITION1	OUTEN *	

* = TRI-STATE OUTPUT
35 INPUTS, 25 OUTPUTS
4 VCC, 4 VSS

PIN CONFIGURATION
Plastic Leaded Chip Carrier
(Top View)



ORDERING INFORMATION



Integrated Device Technology, Inc.

SYSTEM PROGRAMMERS PACKAGE (SPP)

INTRODUCTION:

The System Programmer's package (SPP) provides tools for software developers who need to write programs for an IDT79R3000 processor that doesn't have its own operating system or a disk. The SPP consists of development commands (which you use from your host development machine) and test machine standalone environment programs. Standalone programs can be diagnostics, your own operating system kernel, device drivers or embedded applications.

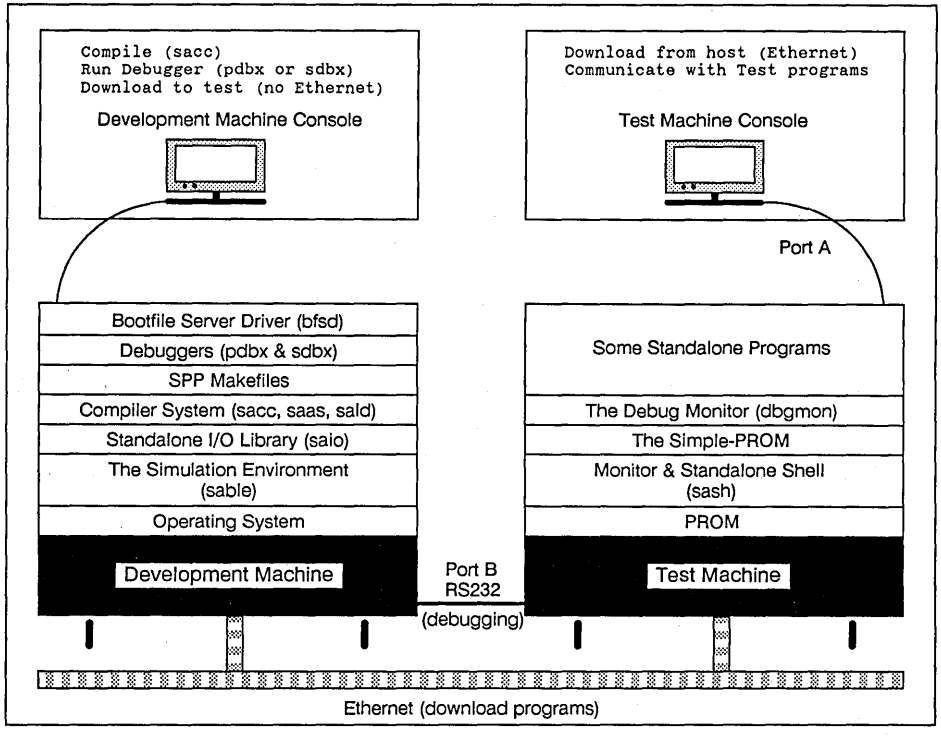
FEATURES:

- Standalone PROM system bring-up tool
- Available in source form for customization
- Provides sophisticated monitor capabilities for download
- Links with symbolic debugger on host system
- UNIX tools to compile, build and download
- Debug monitor (dbgmon)
- PROM code (3 versions)
- UNIX system call subset
- Device drivers in source form
- Power on diagnostics suite

APPLICATIONS:

- Write and compile standalone programs on host development machine
- Debug standalone programs in an environment called "sable", which simulates the processor
- Debug standalone programs on your test machine from the development machine
- Download the final product to the test machine
- Boot and run programs on the test machine

DEVELOPMENT ENVIRONMENT



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The Simulation Environment (sable)

Sable runs on host development machines. It simulates the processor, all machine instructions, cache, translation buffer behavior, a simple disk and a simple console terminal interface.

Sable expedites development of standalone programs and operating systems because you can develop software without needing prototype hardware. Programs that you compile with sacc and saas run in the environment. To do source-level debugging of programs that run under sable, you need to use sdbx which is a version of dbx that works with sable.

The Standalone I/O Library (saio)

When you write programs on the development machine for the standalone environment or for sable, you need to use the standalone I/O library (saio). These UNIX system-like routines support access to disks, tape, Ethernet and UARTS. The library also provides most standard libc and stdio routines.

The Compiler System (sacc, saas, sald)

To compile most programs (for example, diagnostics) that will run in the standalone environment on the test machine or under sable, you can use sacc for C programs and saas for assembly language programs. Sald links and loads the saio library for you. These shell script commands reside in /usr/spp on the development machine.

Debuggers (sdbx, pdbx)

The SPP provides two versions of dbx (pdbx and sdbx) to help you debug standalone programs. These versions provide all regular dbx features.

Use dbx to debug programs that execute on your local machine, sdbx to debug programs running under sable, and pdbx to debug programs on another machine (usually, your test machine). This last method lets you use all the tools of the development environment to debug programs on real hardware. When you debug programs on the test machine, debugging information flows between the development machine and the test machine over an RS232 line.

Bootfile Server Driver (bfsd)

The Ethernet bootfile server driver (bfsd) provides remote file access to remote machines. Typically, you will use bfsd to download bootable images from the development machine to a test machine that does not have a disk.

Bfsd services file requests from standalone programs built with the standalone I/O (saio) library. You can use bfsd to boot operating system kernels, diagnostic programs and standalone programs.

The Monitor and Standalone Shell (sash)

The PROM Monitor provides the tools to examine and change PROM memory, download programs over serial lines (RS232), boot programs from disk, tape and Ethernet, and alter configuration, power-up options in non-volatile RAM.

The standalone shell (sash) is a version of the PROM Monitor that supports more devices, file system formats, and commands than the standard Monitor. You load the sash from the PROM Monitor.

The Simple-PROM

The Simple-PROM is a simplified combination of the PROM Monitor and Debug Monitor (dbgmon). It relies only on the presence of the processor and a UART. The simple-PROM makes no other assumptions regarding hardware configurations and board level features.

The Simple-PROM helps you develop board-level products quickly for the processor. You can also customize the Simple-PROM to your own environment.

The Debug Monitor (dbgmon)

The Debug Monitor (dbgmon) is the standalone environment debugger. You can co-load dbgmon with any standalone program or operating system. The dbgmon lets you examine and alter memory and registers, set breakpoints, examine translation buffer entires, disassemble instructions and execute programs one instruction at a time.

If you use the dbgmon with pdbx, you can do source-level, symbolic debugging of any standalone program or operating system that runs on your test machine.

Integrated Device Technology, Inc.

R3000 MAC II BOARD

ADVANCE INFORMATION
IDT7RS201

FEATURES:

- NuBus ™ card for a Macintosh or MAC IIx provides a standalone single-user environment for code development for the IDT79R3000
- Utilizes IDT79R3000 32-bit Microprocessor
- Incorporates two caches of 16K words each for Instruction and Data
- Supplied with UNIX ™ Operating System (RISC/os™) which includes such tools as:
  - "C" Language Compiler
  - IDT79R3000 assembler
  - Symbolic Debugger
  - Program Performance Profiler (Pixie)
- Systems Programmer Package available for execution on this board includes the following features:
  - Instruction set simulator (Sable)
  - CPU/FPU diagnostics suite
  - Host to target cross Symbolic Code debugger
  - Cache performance evaluation tools
  - Retargetable monitor PROM source code
- Other Languages available are:
  - PL/1
  - Pascal
  - COBOL
  - FORTRAN
  - Ada
- Macintosh™ Operating System User Interface accessible to users so that other Apple Macintosh tools can be operated.

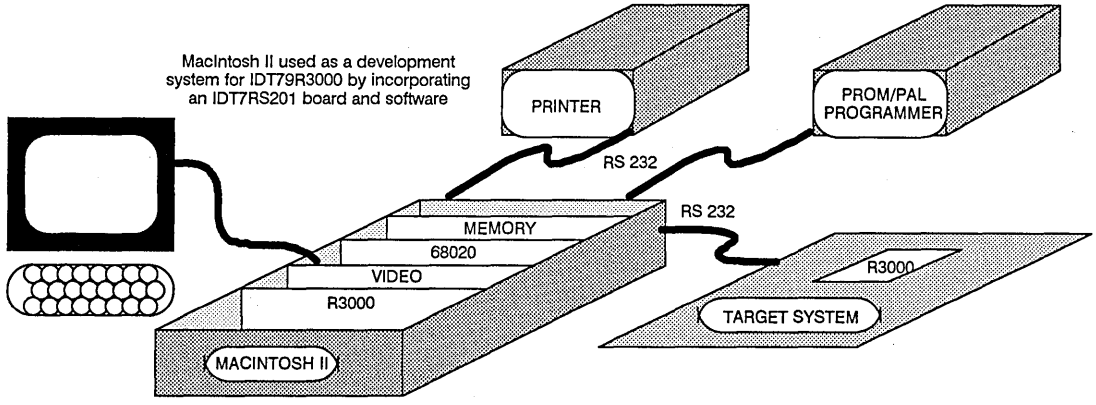
DESCRIPTION:

This board is designed to run the UNIX operating systems, compilers and tools in a single-user standalone mode for development of code for the IDT79R3000. It is composed of a IDT79R3000 32-bit microprocessor, 2 caches for instruction and data as well as a Macintosh II NuBus interface. When inserted into a Macintosh II, the IDT79RS201 board becomes an auxiliary processor responsible for running the UNIX operating system. The 68020, in the Macintosh II mother board, acts as an I/O server and runs the Macintosh OS. The main memory of the Macintosh II is accessible to both processors and is used as communication memory as well as for holding programs for both processors.

The IDT79RS201 incorporates a IDT79R3000 as well as two caches. When a cache miss is encountered, the 32-bit NuBus interface is utilized to fetch the word from the shared memory of the Macintosh II. Words stored in memory are automatically written through the Macintosh II interface and into main memory. In this manner, the IDT79RS201 board provides high performance in the NuBus environment.

The Macintosh 68020 is used as an I/O processor to handle the I/O requests of the UNIX operating system that is executed by the IDT79RS201 board. Requests to the 68020 are made through shared memory buffers which provide support for passing disk blocks and character string data. The 68020 then serves the requests for the disk I/O by executing device drivers in the Macintosh OS. The user directed character I/O is handled by a terminal emulator running in parallel on the Macintosh II and serves to emulate a character oriented CRT. Other serial I/O is passed on to the actual serial I/O ports of the Macintosh II and allows for the downloading of data into devices such as printers and PROM formatters.

The "C" compiler, that comes standard with the IDT79RS201, is Kernighan/Ritchie (System V) and includes additional features such as: Enumerations, Volatile data type, Function prototypes, etc. The compiler incorporates some clarifications of hazy spots from dpANS C. The source-level debugger, that comes with this development package, allows the user to single-step and trace at both the "C" level as well as the machine level for code development. The user is allowed to create macros of frequently used debug sequences and keep a history of previous debug steps taken for later re-execution. The performance profiling tools provided allow the programer to produce histograms of procedure calls and source-code statements. The profiler reports procedures and lines of source-code that are not executed for test coverage purposes.



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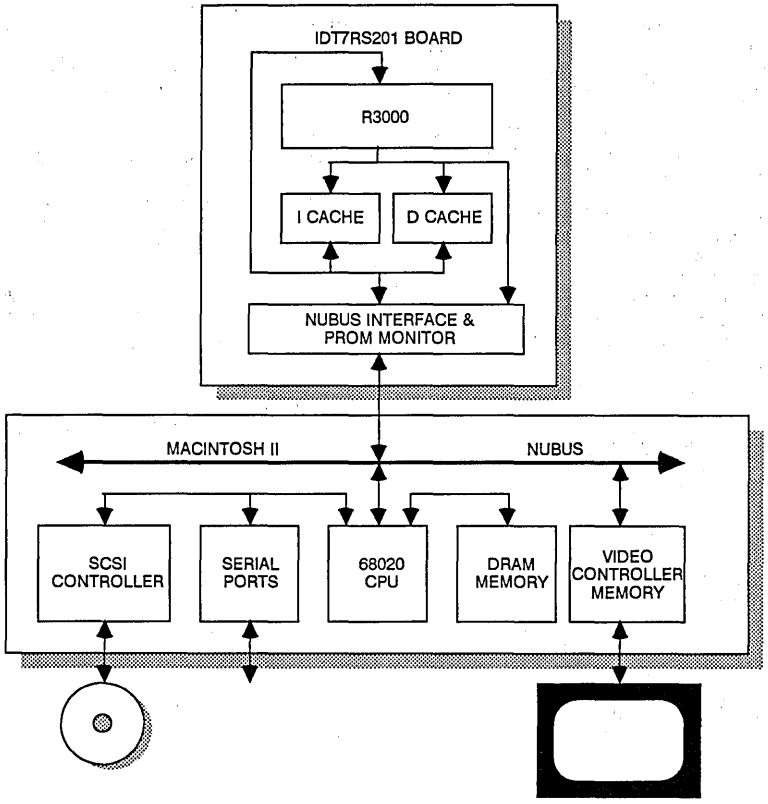

System block diagram of R3000 board interfaced to the Macintosh II.

RISC Optimizing Compilers

The RISCompilers provide an effective programming environment with a family of compilers that share unique optimization technology. The basic compiler and optimization techniques were developed simultaneously with the RISC processor architecture and instruction set.

A common goal was to increase computing performance and efficiency. The resulting RISC hardware and software work smoothly together to deliver a new level of excellence in program development and execution.

Designed to run with the UNIX operating system, these RISCompilers incorporate industry standards in all areas. Optimizing compilers now available include:

C	Kernighan/Ritchie (System V) Hazy spots clarified from dpANS C Allows UNIX to be optimized Function prototypes—graphics, etc
FORTRAN77	Fortran77, validated Common extensions & dialects DEC VMS features FORTRAN66 compatibility features Support for unaligned data items Fast accurate math library
Pascal	Extensions dpANS where appropriate Separate compilation Single and double precision floats Bit manipulation Interfaces well with C
COBOL 85	Shares library and compiler with PL/1 Decimal handled by tuned subroutines Based upon LPI-COBOL
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PL/1	PL/1 Subset G A few extensions like SELECT Used to port 1.8 M line program Based upon LPI-PL/1

System Programmer's Package (SPP) for Software Development and System Integration

The System Programmer's Package (SPP) is a powerful tool kit for developing system software and integrating hardware/software on the target system. SPP provides everything needed to create complete software systems in a native environment without prototype hardware. SPP features include:

- Simulation environment for developing software before hardware exists.
- UNIX tools to compile, simulate, build and download code to the target hardware. There are sets of utilities for building routines such as I/O drivers.
- Run-time routines to install/modify for the final product.
- Debug monitor for target hardware/software integration. Capabilities to examine and alter registers and memory, set breakpoints and perform single-line assembly and disassembly.
- Applications profiling and cache usage simulator. Profiling feature determines time spent in various parts of the program helping to identify program bottlenecks.

Integrated Device Technology, Inc.

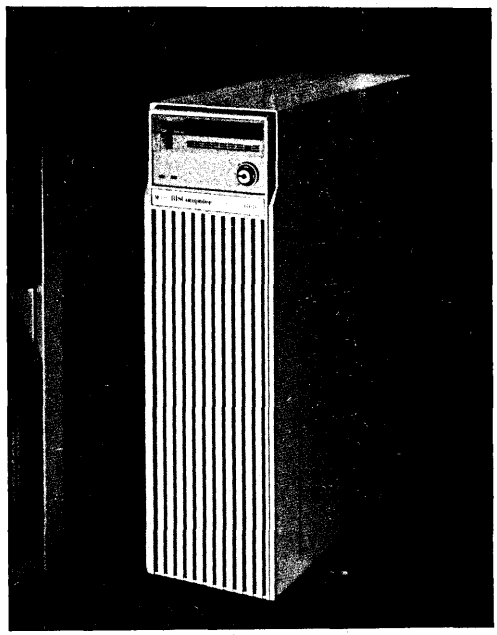
M/120 RISComputer DEVELOPMENT SYSTEM

PRELIMINARY INFORMATION

FEATURES:

- Development system that supports multiple users for software development and debugging. Direct connections for up to 36 serial ports.
- Two basic types available:
  - M/120-3 with 12MHz CPU rated at 9 mips processing power
  - M/120-5 with 16.7MHz CPU rated at 12 mips processing power
- All systems come standard with UNIX™ (RISC/os™), C language RISCompiler, and basic debugging tools.
- Optional optimizing compilers currently available include: FORTRAN, Pascal, COBOL, PL/1, Ada
- System Programmer's Package (SPP) available for advanced development environments
- Four AT slots provide for expansion with cost effective peripherals.
- Third-party software available through Synthesis Software Solutions, Inc., an independent company providing software for MIPS™ based systems
- Compact 23" high package for convenient location in the workplace
- 8MB to 48MB main memory for large programs and multiple users
- Integral Ethernet for high speed LAN connectivity
- SVID complaint UNIX operating system converging System V and BSD
- Binary compatible with other MIPS M-Series RISComputers™
- Supports networking standards, including Ethernet, TCP/IP, and Network File System (NFS™)

The M/120 RISComputer Development System



DESCRIPTION:

The M/120 development system provides a stable software development and debug environment for designing R3000 RISC based systems. Utilizing the MIPS' port of UNIX (RISC/os), and highly optimized RISCompilers, the development system allows the user to begin software development and integration well in advance of operational hardware.

All systems come standard with the RISC/os which includes the assembler, the C optimizing compiler, and the linker, loader and symbolic debugger. The RISC/os also includes the Network File System (NFS) for networking support and utilities converging UNIX System V.3 and BSD 4.3 versions of UNIX in order to support the largest set of UNIX application programs.

The entire suite of MIPS language products is available on M/120 systems. In addition to the C language, the M/120 supports FORTRAN with VMS™ extensions, Pascal, COBOL, Ada, and PL/1. All these language compilers include multi-level optimizations designed to maximize program execution speed.

9

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RISC/os is a registered trademark of MIPS Computer Systems, Inc.
MIPS is a registered trademark of MIPS Computer Systems, Inc.
NFS is a registered trademark of Sun Microsystems.
UNIX is a registered trademark of AT&T.
VMS is a registered trademark of Digital Equipment Corp.

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RISC Optimizing Compilers

The RISCompilers provide an effective programming environment with a family of compilers that share unique optimization technology. The basic compiler and optimization techniques were developed simultaneously with its RISC architecture and instruction set. The resulting RISC hardware and software work smoothly together to deliver a new level of excellence in program development and execution.

Designed to run with the UNIX operating system, these RISCompilers incorporate industry standards in all areas. Optimizing compilers now available include:

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- Run-time routines to install/modify for the final product.
- Debug monitor for target hardware/software integration. Capabilities to examine and alter registers and memory, set breakpoints and perform single-line assembly and disassembly.
- Applications profiling and cache usage simulator. Profiling feature determines time spent in various parts of the program helping to identify program bottlenecks.

M/120 Development System Configurations:

Model#	Description
8102	M/120-5 RISComputer Development System includes: • 16.7MHz CPU with Floating Point Accelerator • 8MB main memory • Ethernet controller • SCSI controller • 128K of I&D caches • Four serial ports • 328MB 5.25" disk • 120MB cartridge tape • Four AT bus slots • Networking software • RISC/os with C compiler
8101	Same as Model 8102, but with 156MB disk.
8114	Same as Model 8102, but with 16MB disk main memory and console VDT.
8104	M/120-3 RISComputer Development System with 12MHz CPU; other configuration items same as Model 8102.
8103	Same as Model 8104, but with 156MB disk.

Note: Additional memory, disk peripherals, and interface options, such as Ethernet or serial I/O, are also available from IDT.

Integrated Device Technology, Inc.

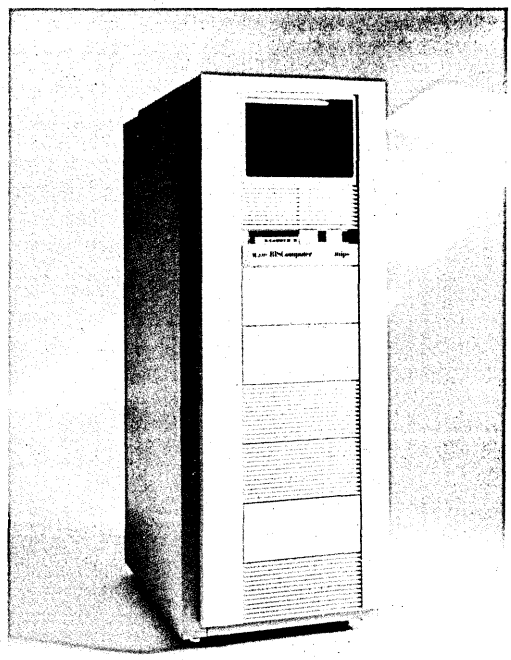
M/2000 RISComputer DEVELOPMENT SYSTEM

PRELIMINARY INFORMATION

FEATURES:

- High performance development system with connections for up to 64 serial lines to support large projects doing software development and debugging of R3000-based designs
- Two basic types available:
  - M/2000 -8 with 25MHz R3000 CPU rated at 20 mips processing power
  - M/2000 -6 with 20MHz R3000 CPU
- Each system includes the R3000, the R3010 FPA, and 128KB of high-speed cache for instructions and data
- All systems come standard with MIPS'™ port of UNIX™ (RISC/os™), C language optimizing RISCompiler, and basic debugging tools
- Optional optimizing compilers currently available include: FORTRAN, Pascal, COBOL, PL1, Ada
- System Programmer's Package (SPP) available for advanced development environments
- Thirteen slots available for expansion with high performance peripherals
- Third-party software available through Synthesis Software Solutions, Inc., an independent company providing software for R3000-based systems
- 16MB to 128MB main memory for large programs and multiple users
- SVID complaint UNIX operating system converging System V and BSD
- Binary compatible with other MIPS M-Series RISComputers™
- Supports networking standards, including Ethernet, TCP/IP, and Network File System (NFS™)

The M/2000 RISComputer Development System



DESCRIPTION:

The M/2000 development system provides a high performance environment for software development and debugging to support large projects designing R3000 RISC-based systems. Utilizing the MIPS' port of UNIX (RISC/os), and highly optimizing RISCompilers, the development system allows the users to begin software development and integration well in advance of operational hardware.

All systems come standard with the RISC/os which includes the assembler, the C optimizing compiler, and the linker, loader and symbolic debugger. The RISC/os also includes the Network File System (NFS) for networking support and utilities converging UNIX System V.3 and BSD 4.3 versions of UNIX in order to support the largest set of UNIX application programs.

The entire suite of MIPS language products is available on M/2000 systems. In addition to the C language, the M/2000 supports FORTRAN with VMS™ extensions, Pascal, COBOL, Ada, and PL1. All these language compilers include multi-level optimizations designed to maximize program execution speed.

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RISC Optimizing Compilers

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- Run-time routines to install/modify for the final product.
- Debug monitor for target hardware/software integration. Capabilities to examine and alter registers and memory, set breakpoints and perform single-line assembly and disassembly.
- Applications profiling and cache usage simulator. Profiling feature determines time spent in various parts of the program helping to identify program bottlenecks.

M/2000 Development System Configurations:

Model#	Description
8302	M/2000-8 RISComputer Development System includes: • 25MHz CPU with Floating Point Accelerator • 32MB main memory • Two 715MB formatted disks • 120MB cartridge tape • 128KB of I&D cache • Console port • 13 slots for expansion • Block mode Ethernet controller • RISC/os with C compiler
8301	Same as Model 8302, but without 1/2" tape drive.
8304	Same as Model 8302, but with one 715MB disk drive.
8303	Same as Model 8304, but without 1/2" tape drive.
8305	M/2000-6 RISComputer Development System includes: • 20MHz CPU with Floating Point Accelerator • 32MB main memory • One 715MB formatted 8" disk • 120MB cartridge tape • 128K of I&D caches • Console port • Ten VME bus slots Three memory slots • Block mode Ethernet controller • RISC/os with C compiler
8306	Same as Model 8305 but without 1/2" mag tape drive.
8307	Same as Model 8305 but with 16MB main memory.
8308	Same as Model 8306 but with 16MB main memory.

Note: Additional memory, disk peripherals, tape peripherals, and interface options, such as Ethernet or serial I/O, are also available from IDT.

INTRODUCTION

Integrated Device Technology offers leadership families of MEMORY & BUS INTERFACE devices that take advantage of two different IDT technology platforms.

The FCT (Fast CEMOS™ TTL-compatible) logic family takes advantage of IDT's leading edge CMOS technology. This technology utilizes sub 1 micron channel lengths and double layer metal processing.

The FBT (Fast BiCEMOS™ TTL-compatible) logic family is manufactured using an advanced dual metal Bicmos technology that combines sub 1 micron CMOS technology with high performance bipolar transistors.

THE FCT LOGIC FAMILY

This logic family was designed to allow easy upgrade of older bipolar 54/74F and AM29800 series designs to their performance equivalents in CMOS. The FCT family comes in two versions; The standard version (FCT), and the low switching noise version (FCTT). Each version has various speed grades. Key features of this family are:

- FCT/FCTT is a direct replacement of FAST™ family products.
- FCT/FCTT is a direct replacement of AM29800 family products.
- FCTA series is up to 50% faster than FCT speeds.
- FCTAT series is equivalent to FCTA speed with improved switching noise.
- FCTCT series is 25% faster than FCTA/FCTAT speeds.
- FCTT series is equivalent to FCT speeds with low switching noise.
- High output drive to 64mA (commercial) and 48mA (military).
- Substantially lower input current levels (5μA maximum).
- Compliant with JEDEC Standard No. 18 for 54/74FCTXXX logic.
- Excellent ESD and Latch-up immunity.

THE FBT LOGIC FAMILY

This logic family is manufactured using an advanced BiCEMOS, dual metal technology. This technology allows the highest device speeds to be gained while minimizing simultaneous switching noise and maintaining CMOS power levels. Key features of this family are:

- FBT series is 25% faster than FCTA speeds.
- Output drive to 64mA (Commercial) and 48mA (Military).
- CMOS power levels (5μW typical static).
- TTL compatible input and output levels.
- High output impedance in power-off state.
- JEDEC standard pinout for DIP, SOIC and LCC packages.

QUALITY

All IDT logic devices are manufactured and assembled on a MIL-STD-883, Class B compliant line. Key features of the military products include:

- Fully compliant to MIL-STD-883, Class B.
- Offer numerous devices to DESC drawings.
- Available in Radiation Tolerant and Enhanced versions.
- Packages include Hermetic DIP, LCC and CERPACK.

Commercial products are manufactured using the same production line and stringent quality requirements acquired from building military products. All commercial products are available in dual in-line as well as surface mount packages.

PRODUCT MATRIX

SWITCHING NOISE			
STANDARD		FCTA	
IMPROVED	FBT/FCTCT	FCTAT	FCT
LOW			FCTT

ULTRA-HIGH SPEED	HIGH SPEED	FAST
SPEED GRADE		

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FAST is trademark of National Semiconductor.

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Integrated Device Technology, Inc.

ULTRA HIGH-SPEED BiCMOS LOGIC

ADVANCE INFORMATION FBT SERIES

FEATURES:

- BiCEMOS™ FBT series 25% faster than FCTA speeds
- Equivalent to FCTA output drive over full temperature and voltage supply extremes
- I_{OL} up to 64mA (Commercial) and 48mA (Military)
- CMOS power levels (1mW typical static)
- TTL compatible input and output levels
- High output impedance in power-off state
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military Product Compliant to Mil-Std-883, Class B

DESCRIPTION:

The FBT series of BiCMOS devices are built using advanced BiCEMOS, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

These devices meet true bipolar TTL output levels. A combination of reduced bipolar output swing and unique BiCMOS output circuitry helps minimize simultaneous switching noise. The output buffers are designed to offer high output impedance in the power-off state. This feature makes these devices ideal for card edge interface.

PRODUCTS TO BE OFFERED:

The following advanced information on our FBT series include the Absolute Maximum Ratings and DC Electrical Characteristics. For more detailed information on other specifications (Pin Description, Block Diagram, Truth Table, and Power Supply Characteristics), refer to data sheets in the 1989 Data Book Supplement. Switching Characteristics are not available at this time.

IDT54/74FBT240 refer to IDT54/74FCT240A specifications on page S10-82
IDT54/74FBT241 refer to IDT54/74FCT241A specifications on page S10-86
IDT54/74FBT244 refer to IDT54/74FCT244A specifications on page S10-86
IDT54/74FBT245 refer to IDT54/74FCT245A specifications on page S10-92
IDT54/74FBT373 refer to IDT54/74FCT373A specifications on page S10-105
IDT54/74FBT374 refer to IDT54/74FCT374A specifications on page S10-109
IDT54/74FBT540 refer to IDT54/74FCT540A specifications on page S10-122
IDT54/74FBT541 refer to IDT54/74FCT541A specifications on page S10-122
IDT54/74FBT821 refer to IDT54/74FCT821A specifications on page S10-152
IDT54/74FBT823 refer to IDT54/74FCT823A specifications on page S10-152
IDT54/74FBT827 refer to IDT54/74FCT827A specifications on page S10-158
IDT54/74FBT841 refer to IDT54/74FCT841A specifications on page S10-171
IDT54/74FBT843 refer to IDT54/74FCT843A specifications on page S10-171

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BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} [2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} [3]	Terminal Voltage with Respect to GND	-0.5 to +5.5	-0.5 to +5.5	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER [1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V	Except I/O Pins	–	–	10	µA
			I/O Pins	–	–	60	
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = .5V	Except I/O Pins	–	–	-10	µA
			I/O Pins	–	–	-60	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	–	–	50	µA
I_{OZL}			V_O = .5V	–	–	-50	
I_I	Input HIGH Current	V_{CC} = Max. V_I = 5.5V		–	–	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} For Non-800 Series Devices	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	–	V
			I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.0	3.0	–	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	–	0.3	0.55	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} For 800 Series Devices	I_{OH} = -15mA	2.4	3.3	–	V
			I_{OH} = -24mA	2.0	3.0	–	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	–	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		–	200	–	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V V_O = 4.5V		–	–	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		–	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

Integrated Device Technology, Inc.

HIGH-SPEED CMOS LOGIC

ADVANCE INFORMATION FCTXXXCT TTL OUTPUT ONLY SERIES

FEATURES:

- FCTXXXCT series 25% faster than FCTAT speeds
- CMOS devices with TRUE TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} up to 64mA (Commercial) and 48mA (Military)
- CMOS power levels (1mW typical static)
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military Product Compliant to MIL-STD-883, Class B
- Available in Rad Hard and Rad Tolerant Versions

DESCRIPTION:

The FCTXXXCT is a high-speed CMOS logic family designed with true TTL level input and output voltages. The reduced voltage swing (3.4 Volts rail to rail) results in lower AC switching noise. Effectively, the FCTXXXCT products combine the high-speed, low power advantages of CMOS logic products. FCTXXXCT is 25% faster than FCTA and FCTXXXAT.

The FCTXXXCT series of CMOS devices are built using advanced CEMOS ™, a dual metal CMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

Information on our FCTXXXCT series includes the Absolute Maximum Ratings and DC Electrical Characteristics. For more detailed information on specifications (Pin Description, Block Diagram, Truth Table and Power Supply Characteristics), refer to the appropriate data sheets in the 1989 Data Book Supplement. Switching Characteristics are not available at this time.

Products to be offered:

IDT54/74FCT240CT refer to IDT54/74FCT240/A page S10-82
IDT54/74FCT241CT refer to IDT54/74FCT241/A page S10-86
IDT54/74FCT244CT refer to IDT54/74FCT244/A page S10-86
IDT54/74FCT245CT refer to IDT54/74FCT245/A page S10-92
IDT54/74FCT373CT refer to IDT54/74FCT373/A page S10-105
IDT54/74FCT374CT refer to IDT54/74FCT374/A page S10-109
IDT54/74FCT540CT refer to IDT54/74FCT540/A page S10-122
IDT54/74FCT541CT refer to IDT54/74FCT541/A page S10-122
IDT54/74FCT646CT refer to IDT54/74FCT646/A page S10-140
IDT54/74FCT821CT refer to IDT54/74FCT821/A page S10-152
IDT54/74FCT823CT refer to IDT54/74FCT823/A page S10-152
IDT54/74FCT827CT refer to IDT54/74FCT827/A page S10-158
IDT54/74FCT841CT refer to IDT54/74FCT841/A page S10-171
IDT54/74FCT843CT refer to IDT54/74FCT843/A page S10-171
IDT54/74FCT845CT refer to IDT54/74FCT845/A page S10-171

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	–	–	5	µA
		V_I = 2.7V	I/O Pins	–	–	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	–	–	-5	µA
		V_I = .5V	I/O Pins	–	–	-15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	–	–	10	µA
I_{OZL}			V_O = .5V	–	–	-10	
I_I	Input HIGH Current	V_{CC} = Max. V_I = V_{CC} (Max.)		–	–	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	–	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	–	V
			I_{OH} = -12mA MIL. I_{OL} = -15mA COM'L.	2.0	3.0	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Line Drivers	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	–	0.3	0.55	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Standard, 3-State, and 800 Series	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	–	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} ≥ GND or V_{CC}		–	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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Integrated Device Technology, Inc.

HIGH-SPEED CMOS LOGIC

ADVANCE INFORMATION FCTXXXT/AT TTL OUTPUT ONLY SERIES

FEATURES:

- FCTXXXT series equivalent to FCT and FAST™ speeds and drive
- FCTXXXAT series equivalent to FCTA speeds and drive
- CMOS devices with TRUE TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} up to 64mA (Commercial) and 48mA (Military)
- CMOS power levels (1mW typical static)
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military Product Compliant to MIL-STD-883, Class B
- Available in Rad Hard and Rad Tolerant Versions

DESCRIPTION:

The FCTXXXT and FCTXXXAT are high-speed CMOS logic products designed with true TTL level input and output voltages. The reduced voltage swing (3.4 Volts rail to rail) results in lower AC switching noise. Effectively, the FCTXXXT and FCTXXXAT products combine the high-speed, low power advantages of CMOS logic products with the lower AC switching noise of traditional Bipolar logic families.

The FCTXXXT and FCTXXXAT series of CMOS devices are built using advanced CEMOS™, a dual metal CMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

Information on our FCTXXXT and FCTXXXAT series include the Absolute Maximum Ratings and DC Electrical Characteristics. For more detailed information on specifications (Pin Description, Block Diagram, Truth Table and Power Supply and Switching Characteristics), refer to the appropriate data sheets in the 1989 Data Book Supplement.

Products to be offered:

IDT54/74FCT240T/AT refer to IDT54/74FCT240/A page S10-82
IDT54/74FCT241T/AT refer to IDT54/74FCT241/A page S10-86
IDT54/74FCT244T/AT refer to IDT54/74FCT244/A page S10-86
IDT54/74FCT245T/AT refer to IDT54/74FCT245/A page S10-92
IDT54/74FCT373T/AT refer to IDT54/74FCT373/A page S10-105
IDT54/74FCT374T/AT refer to IDT54/74FCT374/A page S10-109
IDT54/74FCT540T/AT refer to IDT54/74FCT540/A page S10-122
IDT54/74FCT541T/AT refer to IDT54/74FCT541/A page S10-122
IDT54/74FCT646T/AT refer to IDT54/74FCT646/A page S10-140
IDT54/74FCT821T/AT refer to IDT54/74FCT821/A page S10-152
IDT54/74FCT823T/AT refer to IDT54/74FCT823/A page S10-152
IDT54/74FCT827T/AT refer to IDT54/74FCT827/A page S10-158
IDT54/74FCT841T/AT refer to IDT54/74FCT841/A page S10-171
IDT54/74FCT843T/AT refer to IDT54/74FCT843/A page S10-171

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DSC-4067/-

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	–	–	5	µA
		V_I = 2.7V	I/O Pins	–	–	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	–	–	-5	µA
		V_I = .5V	I/O Pins	–	–	-15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	–	–	10	µA
I_{OZL}			V_O = .5V	–	–	-10	
I_I	Input HIGH Current	V_{CC} = Max. V_I = V_{CC} (Max.)		–	–	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	–	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL. I_{OH} = -8mA COM'L.	2.4	3.3	–	V
			I_{OH} = -12mA MIL. I_{OL} = -15mA COM'L.	2.0	3.0	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Line Drivers	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	–	0.3	0.55	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Standard, 3-State, and 800 Series	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	–	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} ≥ GND or V_{CC}		–	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

ADVANCE INFORMATION
IDT 54/74FCT151T
IDT 54/74FCT151AT

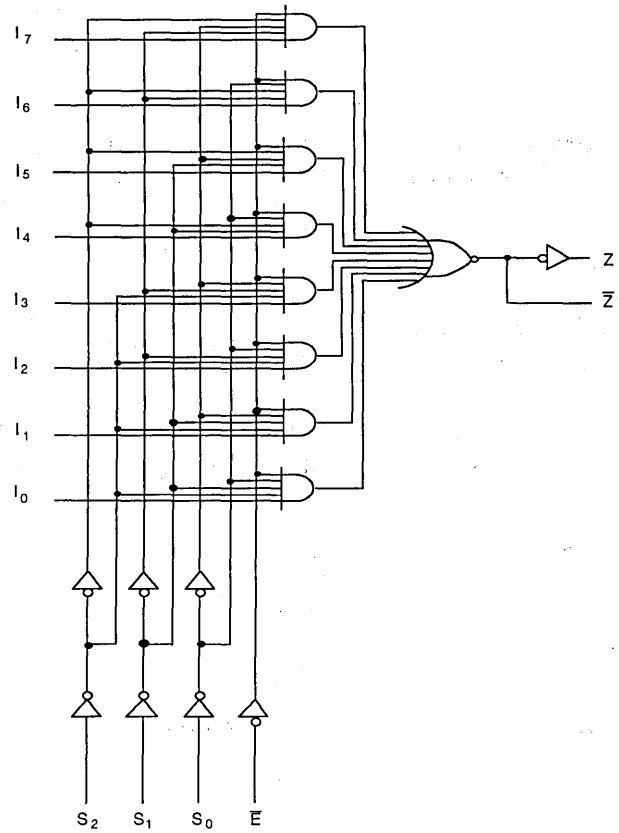
FEATURES:

- IDT54/74FCT151T equivalent to FAST™ speed
- IDT54/74FCT151AT 25% faster than FAST™ speed
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT151T is an 8-input multiplexer built using advanced CEMOS™, a dual metal CMOS technology. The FCT151T has the ability to select one line of data from up to eight sources. It can be used as a function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

FUNCTIONAL BLOCK DIAGRAM



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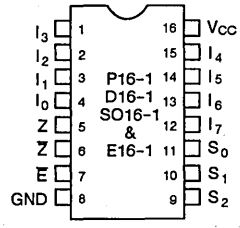
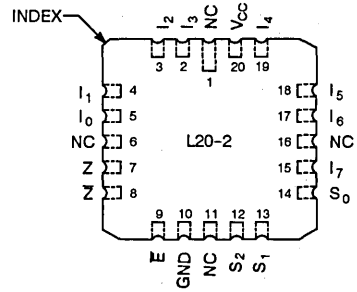
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$I_1 - I_7$	Data Inputs
$S_0 - S_2$	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Data Output
$\overline{Z}$	Inverted Data Output

TRUTH TABLE

INPUTS				OUTPUTS	
S2	S1	S0	$\overline{E}$	Z	$\overline{Z}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High Voltage Level
L = Low Voltage Level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.4V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	–	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL.	2.4	3.3	–	V
			I_{OH} = -8mA COM'L.	2.4	3.3	–	
			I_{OH} = -12mA MIL.	2.0	3.0	–	
			I_{OH} = -15mA COM'L.	2.0	3.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	–	0.3	0.5	V
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis	V_{CC} = 5V		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		–	.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_1 = 0		–	.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_1 = 10MHz 50% Duty Cycle $\overline{E}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	5.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT151T					IDT54/74FCT151AT					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$	C_L = 50pF R_L = 500Ω	5.0	1.5	9.0	1.5	10	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$		7.7	1.5	10.5	1.5	11.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		4.8	1.5	7.0	1.5	7.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		5.4	1.5	9.5	1.5	11	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to $\overline{Z}$		2.9	1.5	6.5	1.5	7.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to Z		5.2	1.5	7.5	1.5	9	–	–	–	–	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

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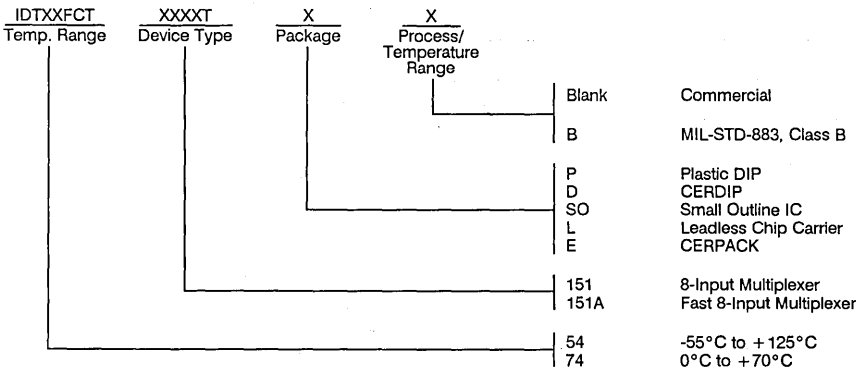
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER

PRELIMINARY
IDT 54/74FCT157T
IDT 54/74FCT157AT

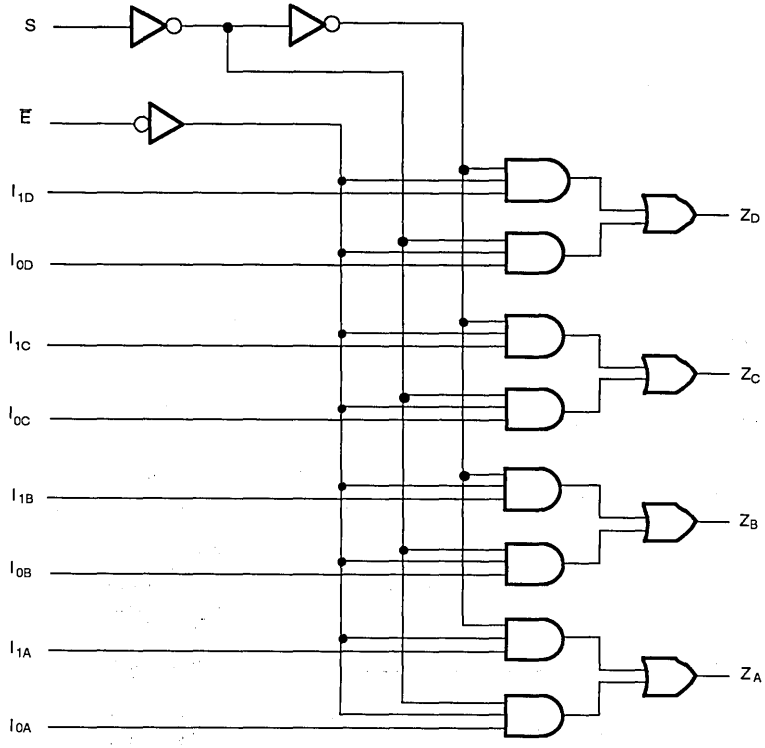
FEATURES:

- IDT54/74FCT157T equivalent to FAST™ speed
- IDT54/74FCT157AT 25% faster than FAST™ speed
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT157T/AT is a quad 2-input multiplexer built using advanced CEMOS™, a dual metal CMOS technology. Four bits of data can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverting) form. The 157 can also be used to generate any four of the 16 different functions to two different variables.

FUNCTIONAL BLOCK DIAGRAM



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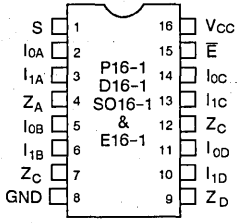
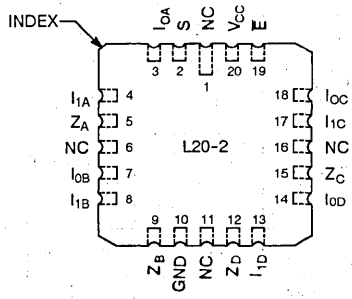
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
I_{0A} - I_{0D}	Source 0 Data Inputs
I_{1A} - I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW)
S	Select Input
Z_A - Z_D	Outputs

TRUTH TABLE

INPUT				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	–	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL.	2.4	3.3	–	V
			I_{OH} = -8mA COM'L.	2.4	3.3	–	
			I_{OH} = -12mA MIL.	2.0	3.0	–	
			I_{OH} = -15mA COM'L.	2.0	3.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis	–		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		–	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{E}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{E}$ = GND Four Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	2.7	8.0[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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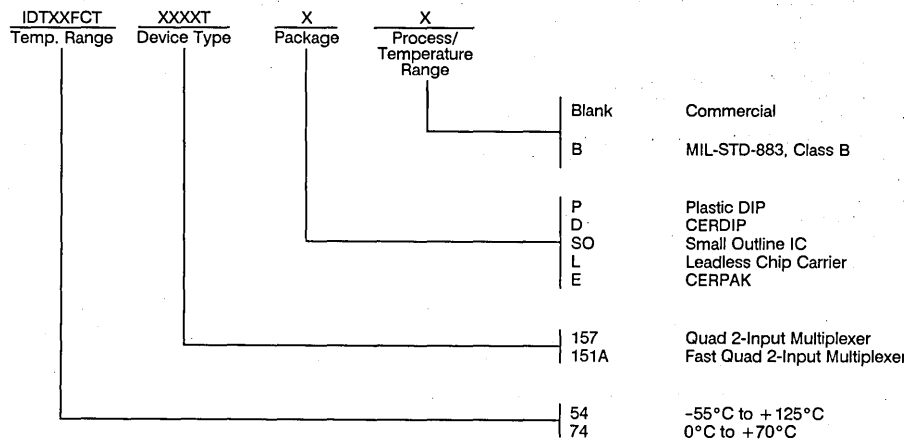
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT157T					IDT54/74FCT157AT					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay In to Zn	C_L = 50pF R_L = 500Ω	4.5	1.5	6.0	1.5	7.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Zn		7.0	1.5	10.5	1.5	12.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn		7.5	1.5	11.0	1.5	12.0	–	–	–	–	–	ns

NOTES:

1. See test circuit and waveforms
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER (3-STATE)

PRELIMINARY
IDT 54/74FCT251T
IDT 54/74FCT251AT

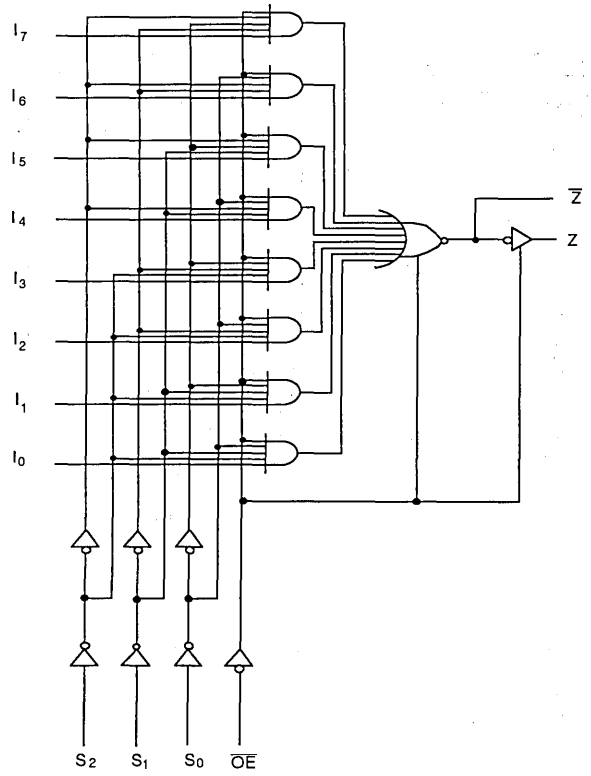
FEATURES:

- IDT54/74FCT251T equivalent to FAST™ speed
- IDT54/74FCT251AT 25% faster than FAST™ speed.
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT251T is an 8-input multiplexer with 3-state outputs built using advanced CEMOS™, a dual metal CMOS technology. The 251 has the ability to select one line of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

FUNCTIONAL BLOCK DIAGRAM



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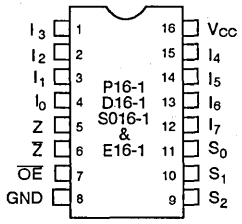
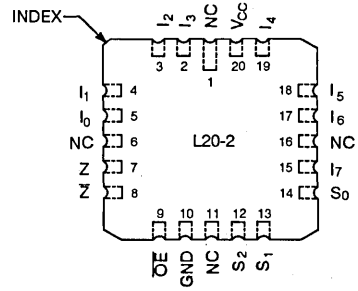
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
S_0 - S_2	Select Inputs
$\overline{OE}$	3-State Output Enable Input (Active LOW)
I_0 - I_7	Multiplexer Inputs
Z	3-State Multiplexer Output
$\overline{Z}$	Complementary 3-State Multiplexer Output

TRUTH TABLE

INPUTS				OUTPUT	
S_2	S_1	S_0	$\overline{OE}$	Z	$\overline{Z}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10	
			V_O = 0.5V	–	–	-10	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC}= Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	–	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL.	2.4	3.3	–	V
			I_{OH} = −8mA COM'L.	2.4	3.3	–	
			I_{OH} = −12mA MIL.	2.0	3.0	–	
			I_{OL} = −15mA COM'L.	2.0	3.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis	–		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		–	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	5.0	

NOTES:

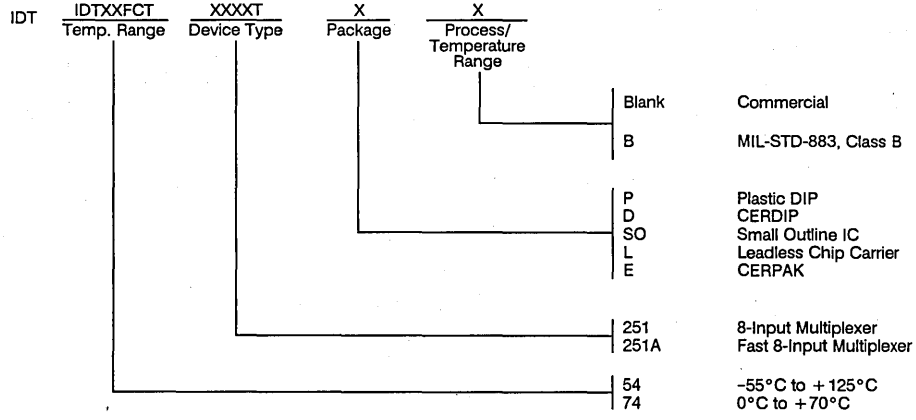
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT251T					IDT54/74FCT251AT					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$	C_L = 50pF R_L = 500Ω	5.9	1.5	9.0	1.5	9.5	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay S_N to Z		9.5	1.5	11.0	1.5	14	–	–	–	–	–	ns
t_{PHL} t_{PLH}	Propagation Delay I_N to $\overline{Z}$		4.0	1.5	7.0	1.5	8.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to Z		7.0	1.5	7.0	1.5	8.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$		6.4	1.5	9.0	1.5	10.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{Z}$		5.0	1.5	7.5	1.5	8.5	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z		6.7	1.5	9.0	1.5	10.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z		4.5	1.5	7.0	1.5	7.0	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER (3-STATE)

PRELIMINARY
IDT 54/74FCT257T
IDT 54/74FCT257AT

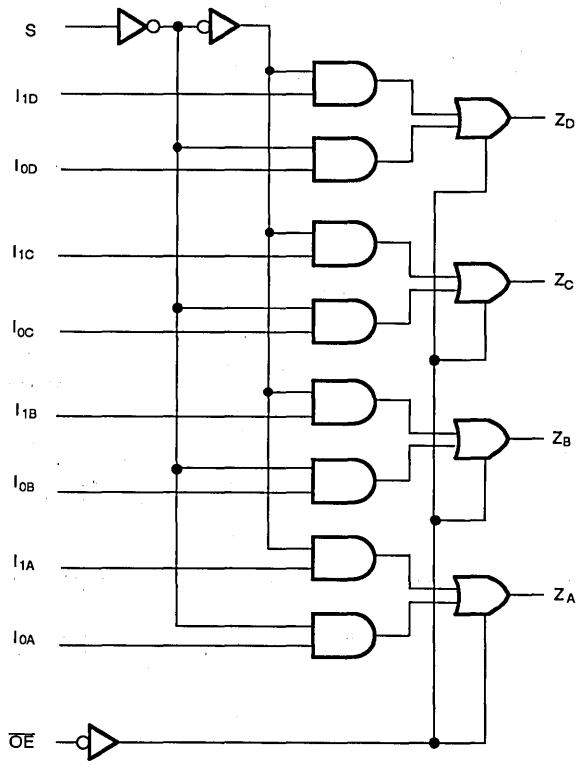
FEATURES:

- IDT54/74FCT257T equivalent to FAST™ speed
- IDT54/74FCT257AT 25% Faster than FAST™
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT257T/AT is a quad 2-input multiplexer built using advanced CEMOS™, a dual metal CMOS technology. Four bits of data can be selected using the Common Data Select inputs. The four outputs present the selected data in the true (non-inverting) form. The outputs may be switched to a high impedance state with HIGH on Output Enable ($\overline{OE}$) input, allowing for direct interface with bus-oriented systems.

FUNCTIONAL BLOCK DIAGRAM



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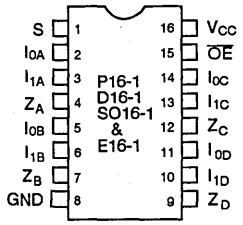
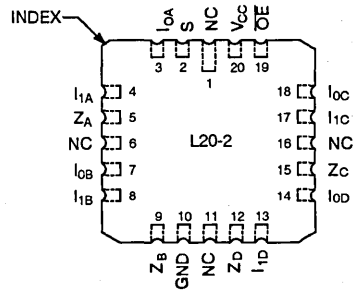
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$I_{0A} - I_{0D}$	Source 0 Data Inputs
$I_{1A} - I_{1D}$	Source 1 Data Inputs
$Z_A - Z_D$	3-State Multiplexer Outputs

TRUTH TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Z_N
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} Terminals Only.
3. Output and I/O Terminals Only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL.	2.4	3.3	–	V
			I_{OH} = -8mA COM'L.	2.4	3.3	–	
			I_{OH} = -12mA MIL.	2.0	3.0	–	
			I_{OH} = -15mA COM'L.	2.0	3.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis	–		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = MAX., V_{IN} = GND or V_{CC}			0.2	1.5	mA

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Four Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.7	4.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	2.7	8.0[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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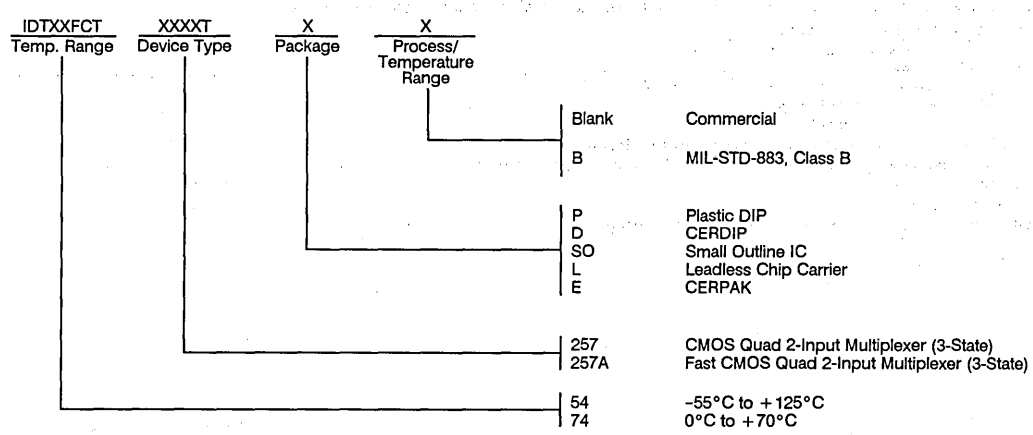
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT257T					IDT54/74FCT257AT					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay I_N to Z_N	C_L = 50pF R_L = 500Ω	4.5	1.5	5.0	1.5	8.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay S to Z_N		7.5	1.5	10.5	1.5	12.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time		6.0	1.5	8.5	1.5	10.0	–	–	–	–	–	ns
t_{HZ} t_{LZ}	Output Disable Time		4.3	1.5	6.0	1.5	8.0	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVER (3-STATE)

PRELIMINARY
IDT 54/74FCT620T/AT
IDT 54/74FCT623T/AT

FEATURES:

- IDT54/74FCT620/623 equivalent to FAST™ speed
- IDT54/74FCT620AT/623AT 25% faster than FAST™ speed
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (Commercial) and 48mA (Military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

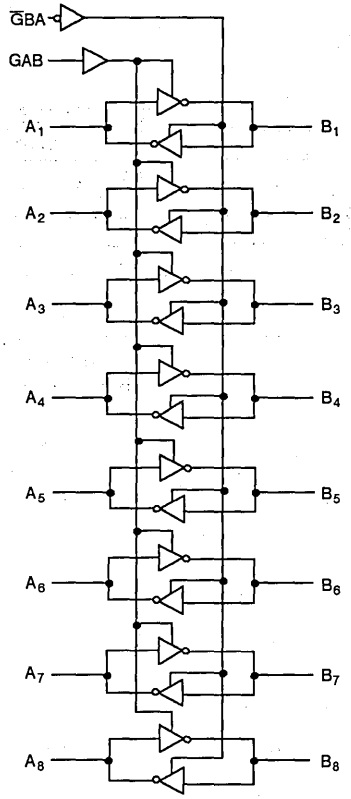
DESCRIPTION:

The IDT54/74FCT623 is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The 'FCT620 is the inverting option of the 'FCT623.

FUNCTIONAL BLOCK DIAGRAM



'FCT620T

'FCT623T is the non-inverting option.

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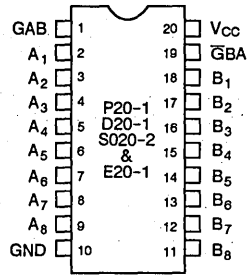
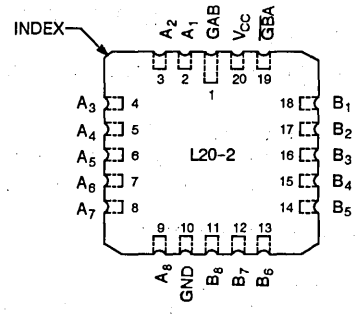
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{G}BA$, GAB	Enable Inputs
A_1 - A_8	A Inputs or 3-State Outputs
B_1 - B_8	B Inputs of 3-State Outputs

TRUTH TABLE

ENABLE	INPUTS	FUNCTION	
$\overline{G}BA$	GAB	'FCT620	'FCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

H = High voltage level
L = Low voltage level
Z = High-impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input & V_{CC} terminals.
3. Output & I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pin only)	V_{CC} = Max.	V_O = V_{CC}	–	–	15	µA
			V_O = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_O = 0.5V	–	–	-15(4)	
			V_O = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -6mA MIL.	2.4	3.3	–	V
			I_{OH} = -8mA COM'L.	2.4	3.3	–	
			I_{OH} = -12mA MIL.	2.0	3.0	–	
			I_{OH} = -15mA COM'L.	2.0	3.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis	–		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = MAX., V_{IN} = GND or V_{CC}			0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 2.0V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_1 = 0		–	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_1 = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.2	6.0	
		V_{CC} = Max. Outputs Open f_1 = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \geq V_{LC}$ (FCT)	–	3.95	7.8[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	6.2	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT620T [4]					IDT54/74FCT620AT [4]					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay An to Bn	C_L = 50pF R_L = 500Ω	3.5	1.5	7.0	1.5	8.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay Bn to An		3.5	1.5	7.0	1.5	8.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}$BA to An		6.5	1.5	9.0	1.5	10.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$BA to An		4.5	1.5	8.0	1.5	9.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time GAB to Bn		6.5	1.5	9.0	1.5	10.5	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time GAB to Bn		5.0	1.5	8.0	1.5	9.0	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.
4. These are preliminary numbers only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT623T [4]					IDT54/74FCT623AT [4]					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay An to Bn	C_L = 50pF R_L = 500Ω	4.0	1.5	7.5	1.5	9.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay Bn to An		4.0	1.5	7.5	1.5	9.5	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}$BA to An		6.5	1.5	9.0	1.5	10.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$BA to An		5.0	1.5	8.0	1.5	9.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time GAB to Bn		6.5	1.5	9.0	1.5	10.5	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time GAB to Bn		5.0	1.5	8.0	1.5	9.0	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.
4. These are preliminary numbers only.

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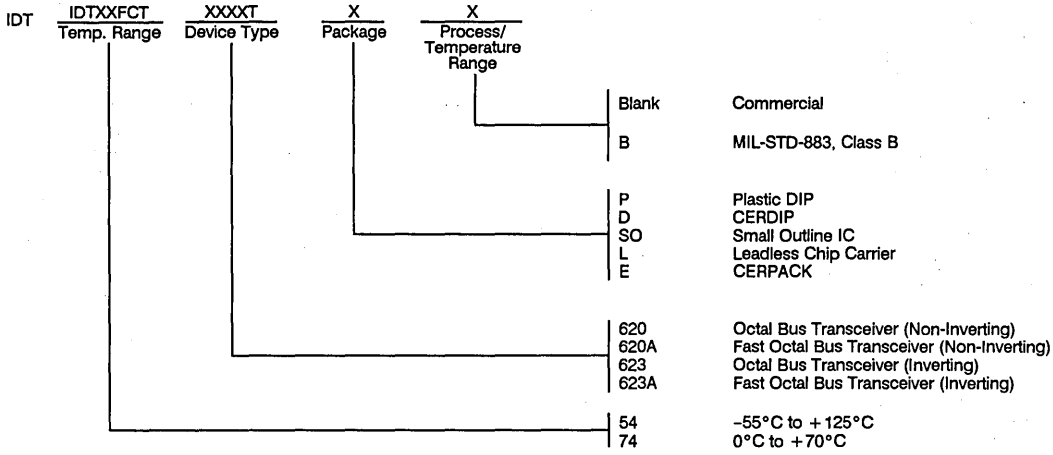
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVER (OPEN DRAIN)

PRELIMINARY
IDT 54/74FCT621T/AT
IDT 54/74FCT622T/AT

FEATURES:

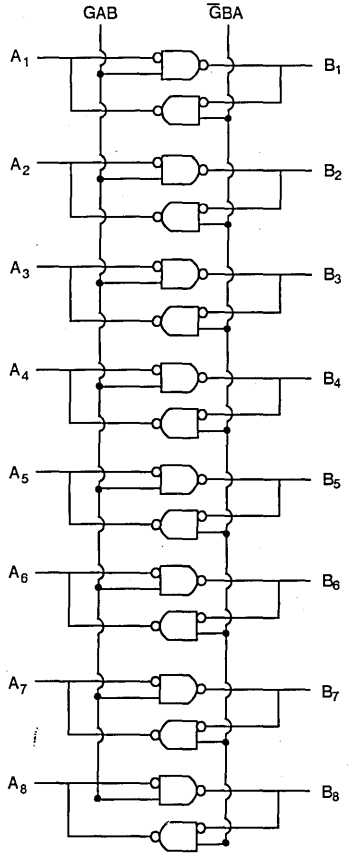
- IDT54/74FCT621/622 equivalent to FAST™ speed
- IDT54/74FCT621/622A 25% faster than FAST™ speed
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT621 is an octal transceiver with non-inverting Open-Drain bus compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'FCT622 is the inverting option of the '621.

The dual-enable configuration can be used to disable the device and isolate the buses or, by simultaneously enabling $\overline{G}BA$ & GAB, to store data.

FUNCTIONAL BLOCK DIAGRAM



'FCT621T

*'FCT622T is inverting option of the 'FCT621T

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FAST is a trademark of Fairchild Semiconductor Co.

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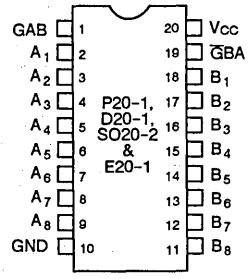
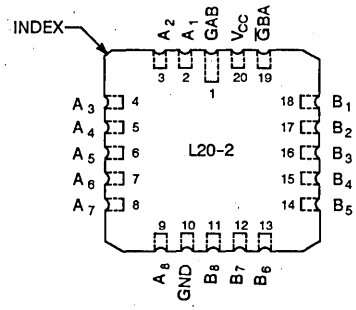
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{G}BA$, GAB	Enable Inputs
$A_1 - A_8$	A inputs or open drain outputs
$B_1 - B_8$	B inputs or open drain outputs

TRUTH TABLE

ENABLE	INPUTS	FUNCTIION	
$\overline{G}BA$	GAB	'FCT621	'FCT622
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to b bus
H	L	OFF	OFF
L	H	B data to A bus A data to B bus	$\overline{B}$ data to A bus $\overline{A}$ data to B bus

H = High Voltage Level
L = Low Voltage Level
OFF = High if pull-up resistor is connected to Open-Collector output

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input High Current (I/O pins only)	V_{CC} = Max.	V_O = V_{CC}	–	–	15	µA
			V_O = 2.7V	–	–	15(4)	
I_{IL}	Input Low Current (I/O pins only)		V_O = 0.5V	–	–	-15(4)	
			V_O = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{IN} = V_{IH} or V_{IL}	V_{OH} = V_{CC} (Max.)	–	–	20	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	–	0.3	0.5	V
			I_{OL} = 64mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis	–		–	200	–	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}			0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Bit Toggling at f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.2	6.0	
		V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \geq V_{LC}$ (FCT)	–	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.2	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT621					IDT54/74FCT621A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	9.5 6.0	5.5 1.5	13.0 8.5	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		9.0 5.5	5.5 1.5	12.5 8.0	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{GBA}$ to A		10.0 6.5	5.5 1.5	14.0 11.0	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay GAB to B		12.0 6.5	6.0 1.5	17.0 10.0	–	–	–	–	–	–	–	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT622					IDT54/74FCT622A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	11.0 4.0	8.0 1.5	13.5 6.0	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		10.0 3.5	7.5 1.5	12.5 5.5	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{GBA}$ to A		10.5 6.0	8.0 1.5	12.5 10.5	–	–	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay GAB to B		12.5 5.5	10.0 1.5	15.5 9.5	–	–	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

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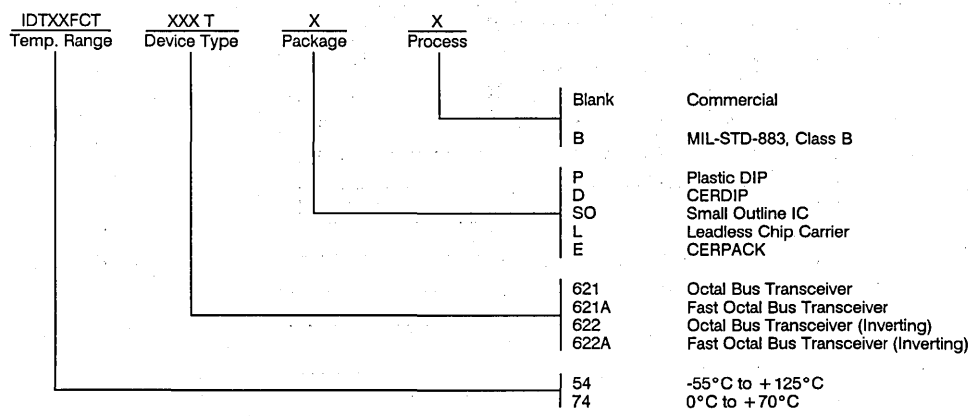
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT 29FCT52A/B
IDT 29FCT53A/B
(Replaces 39C52/B and 39C53/B)

FEATURES:

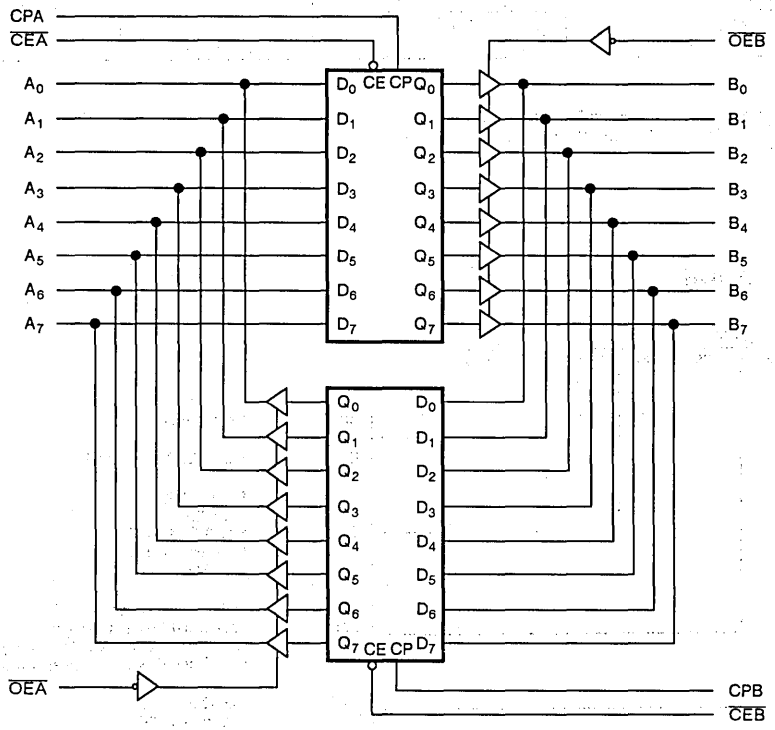
- Equivalent to AMD's Am2952/53 and Fairchild's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed; **IDT29FCT52B/53B 25% faster than FAST™**
- I_{OL} = 64mA (commercial) and 48mA (military)
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC, 28-pin LCC and PLCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52 and IDT29FCT53 are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual-metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52 is a non-inverting option of the IDT29FCT53.

FUNCTIONAL BLOCK DIAGRAM



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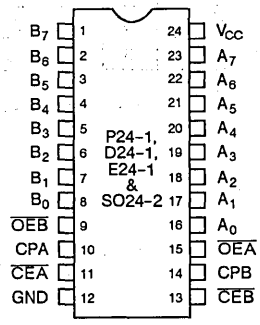
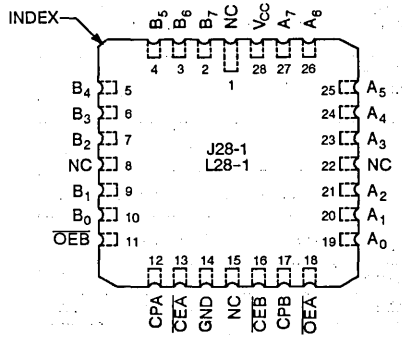
FAST is a trademark of Fairchild Semiconductor Company

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high impedance state.

REGISTER FUNCTION TABLE
(Applies to A or B Register)

INPUTS			INTERNAL Q	FUNCTION
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

$\overline{OE}$	INTERNAL Q	Y-OUTPUTS		FUNCTION
		IDT29FCT52A/B	IDT29FCT53A/B	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V(4)	–	–	5	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V(4)	–	–	-5	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V(4)	–	–	15	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V(4)	–	–	-15	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,(3) V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.0	–	
			I_{OH} = -24mA COM'L.	2.4	4.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{CC} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ [4] $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ [5] $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8	
			V_{IN} = 3.4V[5] or V_{IN} = GND	–	6.0	16.8	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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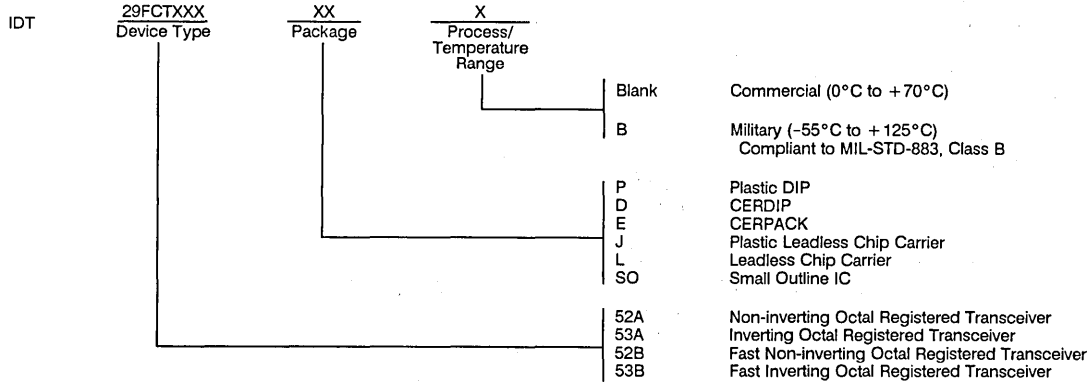
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS[1]	IDT29FCT52A/53A					IDT29FCT52B/53B					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	C_L = 50pF R_L = 500Ω	5.5	2.0	10.0	2.0	11.0	4.5	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		5.5	1.5	10.5	1.5	13.0	4.5	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		5.5	1.5	10.0	1.5	10.0	4.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up time HIGH or LOW A_n, B_n to CPA, CPB		1.0	2.5	–	2.5	–	1.0	2.5	–	2.5	–	ns
t_H	Hold time HIGH or LOW A_n, B_n to CPA, CPB		0.5	2.0	–	2.0	–	0.5	1.5	–	1.5	–	ns
t_{SU}	Set-up time HIGH or LOW. $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		–	3.0	–	3.0	–	–	3.0	–	3.0	–	ns
t_H	Hold time HIGH or LOW. $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_W	Pulse Width, HIGH or LOW CPA or CPB		–	3.0	–	3.0	–	–	3.0	–	3.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

PRELIMINARY
IDT 29FCT520A/B
IDT 29FCT521A/B

FEATURES:

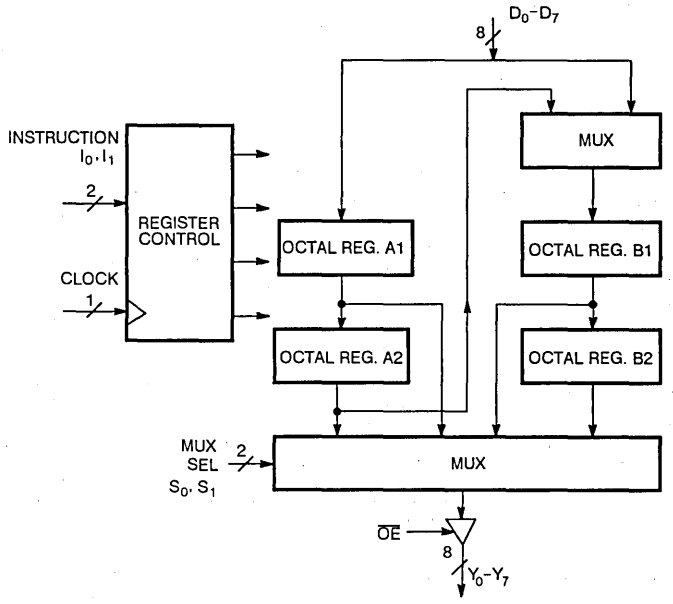
- Equivalent to AMD's Am29520/21 bipolar Multilevel Pipeline Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than AMD's bipolar (5μA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520A/B and IDT29FCT521A/B each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520A/B when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521A/B, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). Transfer also causes the first level to change. In either part I = 3 is for hold.

FUNCTIONAL BLOCK DIAGRAM



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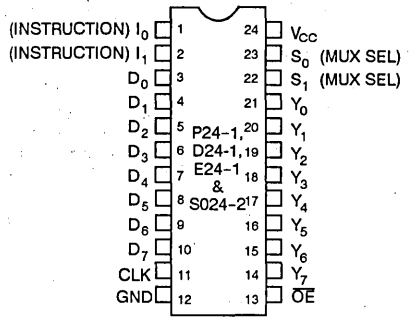
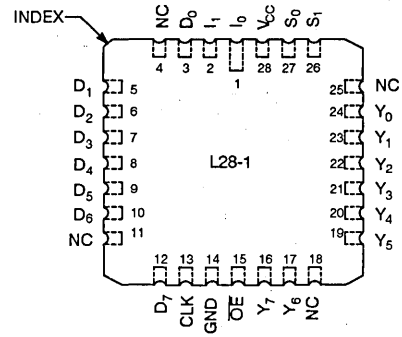
PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

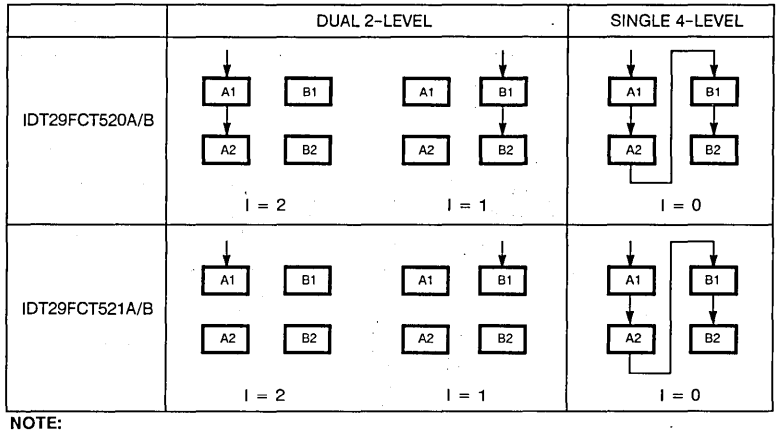
PIN DESCRIPTION

PIN NO.(1)	NAME	I/O	DESCRIPTION
3-10	D_0 - D_7	I	Register input port.
11	CLK	I	Clock input. Enter data into registers on LOW-to-HIGH transitions.
1, 2	I_0, I_1	I	Instruction inputs. See Figure 1 and Instruction Control Tables.
23, 22	S_0, S_1	I	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
13	$\overline{OE}$	I	Output enable for 3-state output port.
14-21	Y_7 - Y_0	O	Register output port

NOTE:
1. DIP configuration.

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1



NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	2.3	4	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.8	6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits and Four Controls Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	9.8	17.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	13.0	30.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS[1]	IDT29FCT520A/21A					IDT29FCT520B/21B[4]					UNIT
			TYP[3]	COM'L.		MIL.		TYP[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHL} t_{PLH}	Clock to Data Output	R_L = 500Ω C_L = 50pF	7.0	2.0	14.0	2.0	16.0	–	2.0	7.5	2.0	8.0	ns
t_{PHL} t_{PLH}	S_0, S_1 to Data Output		7.0	2.0	13.0	2.0	15.0	–	2.0	7.5	2.0	8.0	ns
t_{SU}	Set-up Time Input Data to Clock		–	5.0	–	6.0	–	–	2.5	–	2.8	–	ns
t_H	Hold Time Input Data to Clock		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_{SU}	Set-up Time Instruction to Clock		–	5.0	–	6.0	–	–	4.0	–	4.5	–	ns
t_H	Hold Time Instruction to Clock		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	12.0	1.5	13.0	–	1.5	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	15.0	1.5	16.0	–	1.5	7.5	1.5	8.0	ns
t_W	Clock Pulse Width HIGH or LOW	–	4.0	7.0	–	8.0	–	–	5.5	–	6.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. Preliminary information only.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, it may be necessary to use $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for ATE testing purposes.

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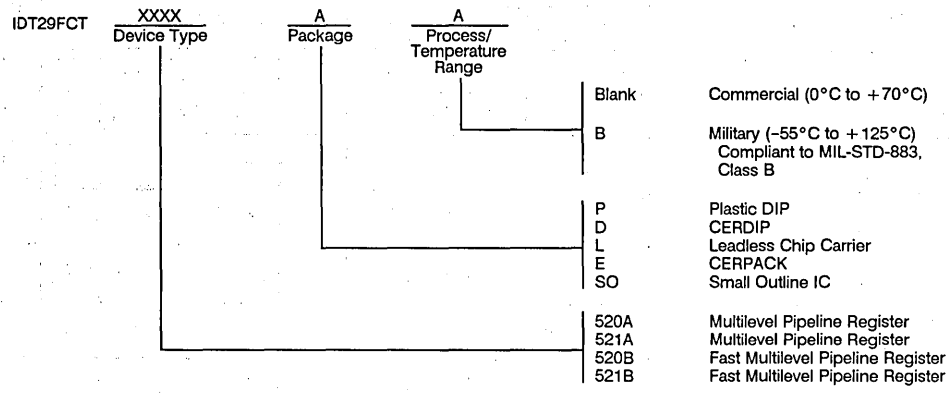
ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED TRI-PORT BUS MULTIPLEXER

PRELIMINARY
IDT 49FCT804/A

FEATURES:

- High-speed, 10 bit x 3 port Bus Multiplexer
- Allows bidirectional communication between any 2 ports
- 10 bits provide extra addressing capability
- Latched inputs for asynchronous storage of incoming data
- Controls designed for shared memory applications
- I_{OL} = 48mA (Commercial), 32mA (Military)
- CMOS Power Levels (5μW typ. static)
- TTL input and output level compatible
- Available in DIP, PLCC and LCC
- Military Product Available to MIL-STD-883, Class B
- Product Available in Rad Tolerant and Rad Enhanced Versions

DESCRIPTION:

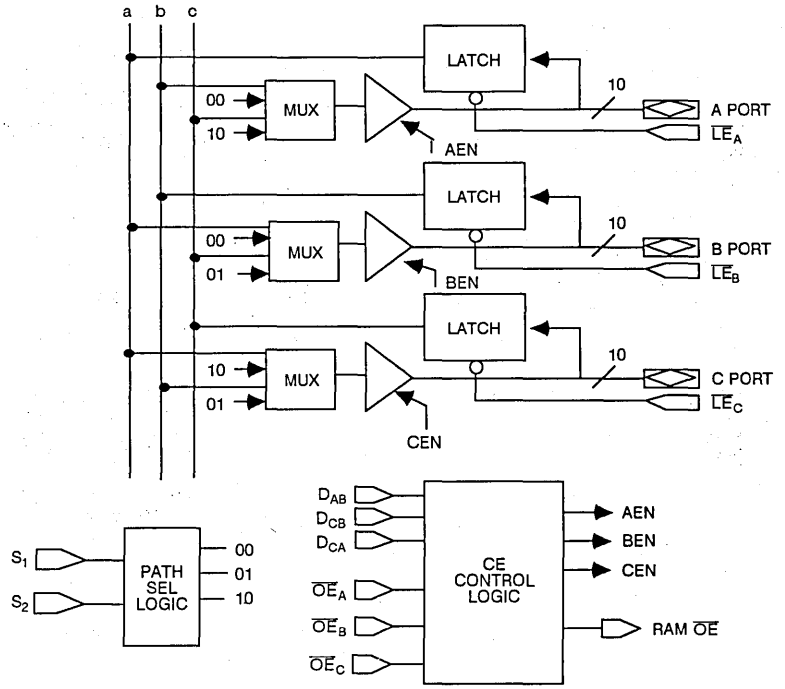
The Busmux is a multiport device intended for inter-bus communication in a multiprocessing, DSP, Array processing or Networking Environment. It offers significant space savings and performance benefit over discrete implementations of the function.

The architecture consists of 3 I/O ports. The input of each port has a transparent latch controlled by a Latch Enable input ($\overline{LE}$). The output of each latch is connected to an internal bus. The output of each port consists of a multiplexer and a tri-state buffer. The multiplexer will select one of the other two busses under control of Path Select Logic inputs (S1, S0).

The direction of signal flow is determined by Direction Control inputs (D_{XX}). The output enable pins of each port ($\overline{OE}_X$) provide independent tri-state control. In addition, when both Path Select Logic inputs (S1, S0) are high, all three ports are in a high impedance state.

For shared memory applications the device is configured to use ports A and C for 2 system busses and port B for the shared memory bus. The RAM output enable (RAM $\overline{OE}$) output is asserted when the signal path is from B to A or B to C. It is disasserted under all other conditions.

FUNCTIONAL BLOCK DIAGRAM



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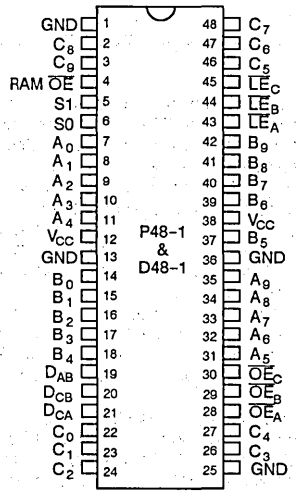
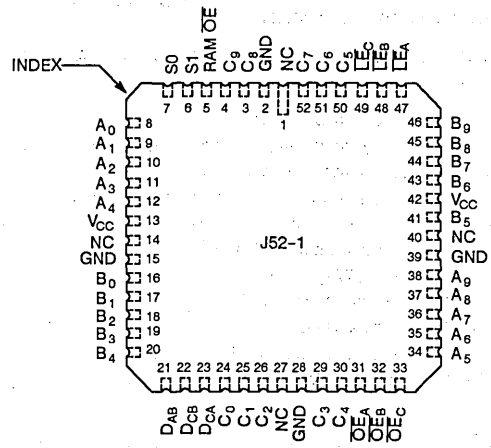
DSC-4066/-

PIN CONFIGURATIONS

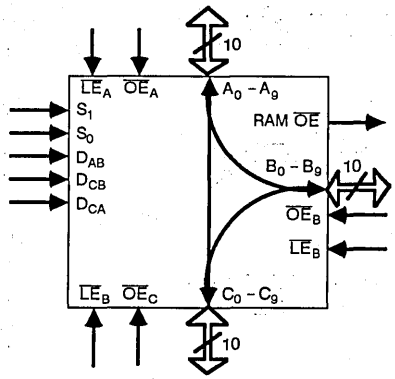


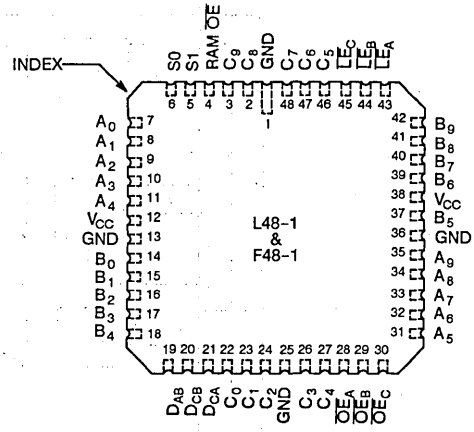
DIP
TOP VIEW



PLCC
TOP VIEW

LOGIC SYMBOL





48-PIN LCC/FLATPACK
TOP VIEW

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
A0 - A9	I/O	A port I/O
B0 - B9	I/O	B port I/O
C0 - C9	I/O	C port I/O
RAM $\overline{OE}$	O	Asserted (low) when B to A or B to C paths are enabled
$\overline{LE}_A$	I	Active low enable for A port input latch
$\overline{LE}_B$	I	Active low enable for B port input latch
$\overline{LE}_C$	I	Active low enable for C port input latch
S0 - S1	I	Path selection inputs
DAB	I	Direction control for AB path
DCB	I	Direction control for CB path
DCA	I	Direction control for CA path
$\overline{OE}_A$	I	Output enable control for A port
$\overline{OE}_B$	I	Output enable control for B port
$\overline{OE}_C$	I	Output enable control for C port
GND 1 - 3	PWR	One ground for each port (Noisy ground)
GND 4	PWR	Signal ground (Quiet ground)
VCC 1 - 2	PWR	+5V power supply

TRUTH TABLE—BUS CONTROL

					$\overline{OE}$ = 0	$\overline{LE}$ = 0		
S1	S0	DAB	DCB	DCA	A PORT	B PORT	C PORT	RAM $\overline{OE}$
0	0	0	X	X	O	I	Z	L
0	0	1	X	X	I	O	Z	H
0	1	X	1	X	Z	O	I	H
0	1	X	0	X	Z	I	O	L
1	0	X	X	0	I	Z	O	H
1	0	X	X	1	O	Z	I	H
1	1	X	X	X	Z	Z	Z	H

LATCH OPERATION

$\overline{LE}$	OPERATION
0	Transparent
1	Port Data Latched

NOTE:
H = High, L = Low, I = In, O = Out, Z = High Impedance, X = Don't Care

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.50	
			I_{OL} = 48mA COM'L.	–	0.3	0.50	
V_H	Input Hysteresis	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS FOR 'FCT804

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_X$ = $\overline{LE}_X$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_X$ = $\overline{LE}_X$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_X$ = $\overline{LE}_X$ = GND Ten Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.8	7.8[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	6.3	17.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT49FCT804					IDT49FCT804A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHL} t_{PLH}	Propagation Delay Port to Port	C_L = 50pF R_L = 500Ω	–	1.5	9.0	1.5	10.0	–	–	–	–	–	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Port		–	1.5	12	1.5	13.0	–	–	–	–	–	ns
t_{PHL} t_{PLH}	Propagation Delay S0 to S1 to Port		–	1.5	9.0	1.5	10	–	–	–	–	–	ns
t_{PZL} t_{PZH}	Output Enable Time Dxx or $\overline{OE}$ to Port[4]		–	1.5	11.5	1.5	13.0	–	–	–	–	–	ns
t_{PLZ} t_{PHZ}	Output Disable Time Dxx or $\overline{OE}$ to Port[4]		–	1.5	9	1.5	11	–	–	–	–	–	ns
t_{SU}	Set-up Time Port Data to LE		–	2	–	2.5	–	–	–	–	–	–	ns
t_H	Hold time Port Data to LE		–	2	–	2.5	–	–	–	–	–	–	ns
t_{PW}	LE Pulse Width HIGH or LOW		–	6	–	6	–	–	–	–	–	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. Dxx to port guaranteed but not tested.

SHARED RAM APPLICATION

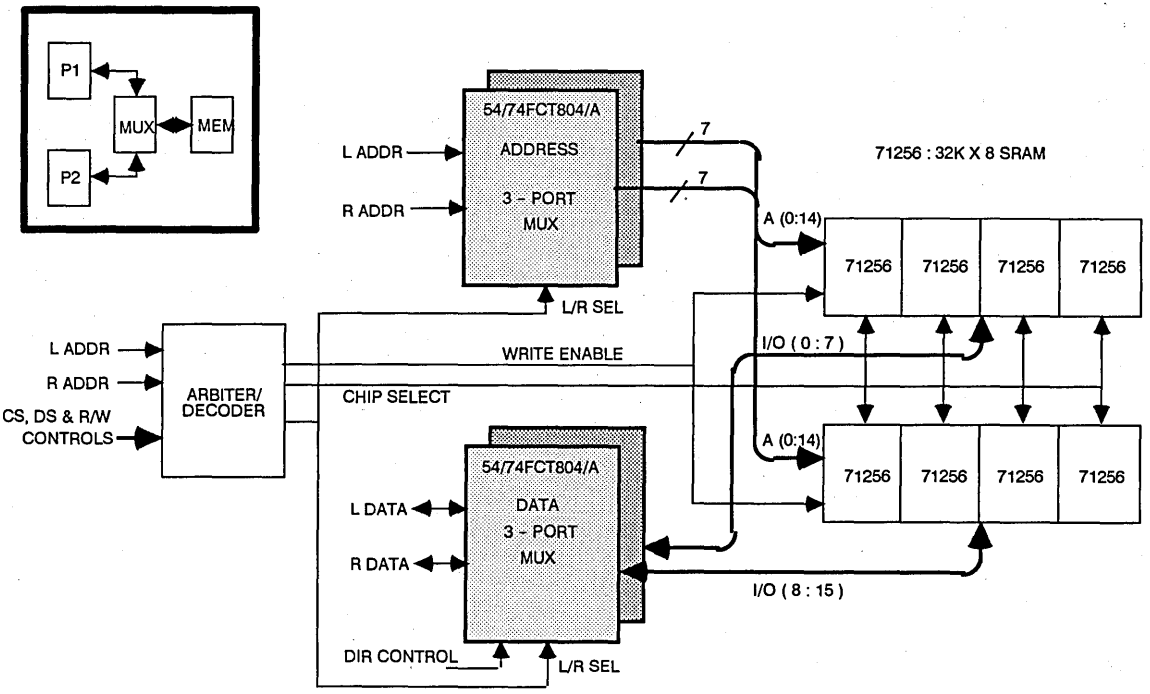
128K x 8 SHARED RAM

This application illustrates the use of IDT49FCT804 Bus Multiplexer in a shared memory application. In this example, two processors share a 128Kbyte memory bank. A pair of IDT49FCT804 multiplexers are used for address selection. The address busses from the two processors are connected to A and C ports respectively. The B port serves as the memory address bus. With all Latch Enable and Output Enable signals asserted, address from A or C ports is routed to B port under the control of S0 which receives its input from an external arbiter/decoder (S1 = 0 and D_{AB} = D_{CB} = 1).

Two more IDT49FCT804 multiplexers route data between the processor data busses connected to A and C ports and the memory data bus connected to the B port. Again, address bus selection is under the control of input S0. Inputs D_{AB} and D_{CB} provide direction control for READ and WRITE operations. The RAM $\overline{OE}$ signal is asserted during the READ operation.

An external arbiter/decoder performs arbitration between two processor requests and provides chip select & write enable signals for the memory array.

128K x 8 SHARED RAM



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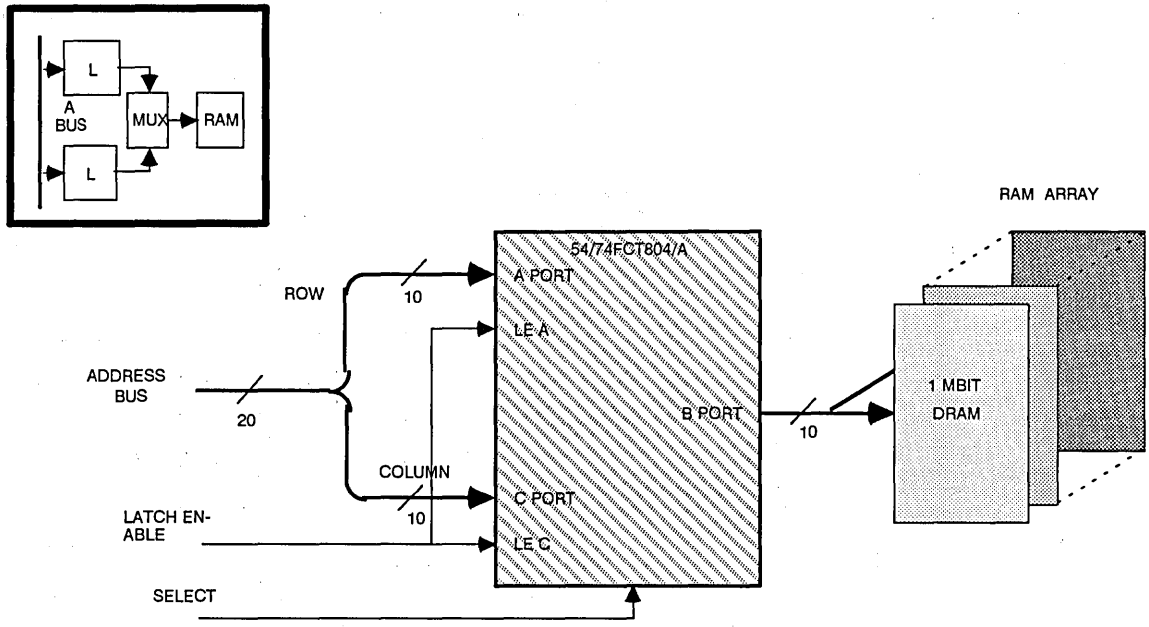
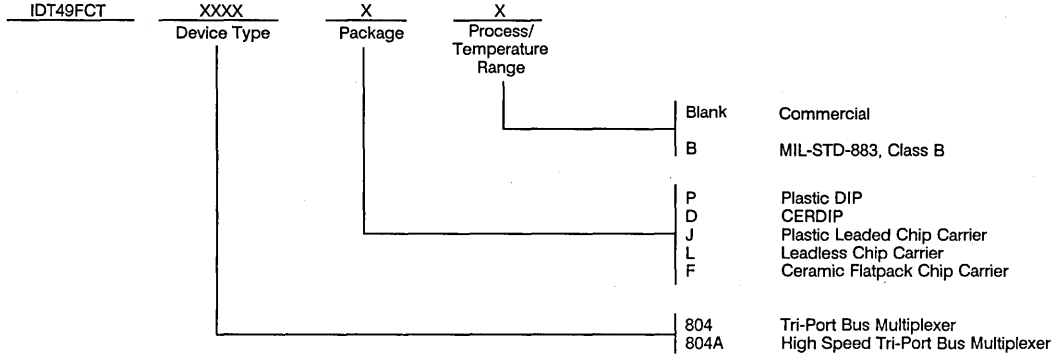
DRAM ADDRESS MULTIPLEXER APPLICATION

This application illustrates the use of IDT49FCT804 Bus Multiplexer for row and column addressing in a large DRAM array. In this example, the full 10 bit capability of the Bus Multiplexer is used to address a 1 MBit DRAM array. The row address lines are connected to the A port and the column address lines are connected to the C port. All address signals are latched simultaneously in the A and C port input latches. Under the control of path selection input S0 (S1 = LOW), the row and column addresses are sent sequentially to the DRAM array.

DRAM ADDRESS MULTIPLEXER APPLICATION



ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED OCTAL REGISTER WITH SPC™

PRELIMINARY
IDT 49FCT818
IDT 49FCT818A

FEATURES:

- High-speed, non-inverting 8-bit parallel register for any data path, control path or pipelining application
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC™) provides
  - Controllability:
    - Serial scan in new machine state
    - Load new machine state "on the fly"
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Direct observe D and Y buses
    - Serial scan out current machine state
    - Capture machine state "on the fly"
- I_{OL} = 32mA (commercial) and 24mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than 29818 and 54/74AS818 (5μA max.)
- Available in plastic and sidebraze DIP, SOIC, LCC and CERPACK
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

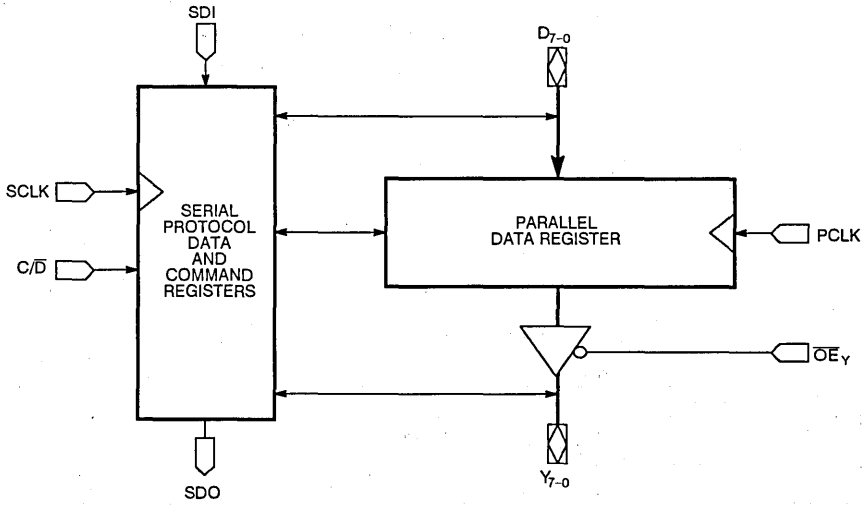
DESCRIPTION:

The IDT49FCT818 is a high-speed, general purpose octal register with Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required.

The SPC command and data registers are used to observe and control the octal data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system. Here normal data, address, status and control registers are replaced with the IDT49FCT818. The loop can be used to scan in a complete test routine starting point (data, address, etc). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results.

As well as diagnostic operations, SPC can be used for initializing at power-on time functions such as Writable Control Store (WCS).

FUNCTIONAL BLOCK DIAGRAM



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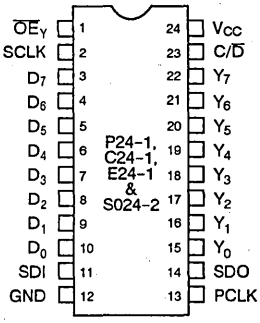
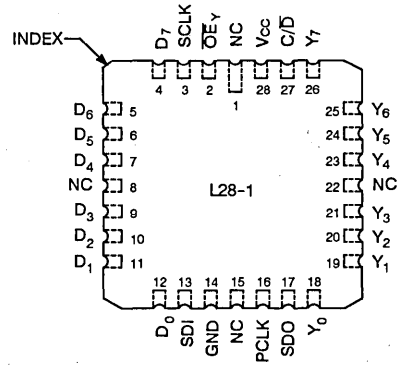
CEMOS and SPC are trademarks of Integrated Device Technology, Inc.

DSC-4003/-1

PIN CONFIGURATIONS

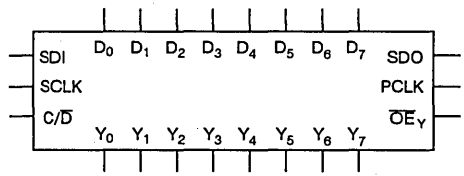


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE

C/$\overline{D}$	SCLK	PCLK	$\overline{OE}_Y$	D	Y	FUNCTION
X	X	X	H	X	High Z	Tri-state Y
X	X	↓	L	H	H	Clock D to Y
X	X	↓	L	L	L	Clock D to Y
H	↓	X	X	X	X	Shift bit into SPC Command register
L	↓	X	X	X	X	Shift bit into SPC Data register
↓	↓	H or L (Static)	X	X	X	Execute SPC command during time between C/$\overline{D}$ & SCLK

NOTE:
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↓ = Transition, H to L or L to H

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
D_{7-0}	I/O	Parallel Data Register Input Pins (D_0 = LSB, D_7 = MSB)
Y_{7-0}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_7 = MSB)
$\overline{OE}_Y$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 & 14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 24mA MIL.	–	0.3	0.5	
			I_{OL} = 32mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clocks Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_Y$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = SDI = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = SDI = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT818				IDT49FCT818A[3]				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHL} t_{PLH}	T1	PCLK ↑ to Y	C_L = 50pF R_L = 500Ω	3.0	12.5	3.0	14.0	3.0	9.0	3.0	10.0	ns
	T2	SCLK ↑ to SDO		3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T3	SDI to SDO (in stub mode)		3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T4	C/$\overline{D}$ ↓ to Y ($\overline{OE}_Y$ = Low Inst. 8 & 14)		3.0	16.0	3.0	18.0	3.0	13.0	3.0	14.0	
	T5	SCLK ↑ to Y ($\overline{OE}_Y$ = High, Inst. 8)		3.0	20.0	3.0	22.0	3.0	13.0	3.0	14.0	
	T6	C/$\overline{D}$ to SDO (Inst. 0, 1, 2 & 4)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	
t_{SU}	S1	D to PCLK ↑		2.5	–	3.0	–	2.5	–	3.0	–	ns
	S2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–	12.0	–	14.0	–	
	S3	SDI to SCLK ↑		4.0	–	5.0	–	4.0	–	5.0	–	
	S4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)		2.0	–	2.5	–	2.0	–	2.5	–	
	S5	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		8.0	–	9.0	–	8.0	–	9.0	–	
	S6	Y to PCLK ↑ (Inst. 3)		1.0	–	1.5	–	1.0	–	1.5	–	
t_H	H1	D to PCLK ↑		2.0	–	2.5	–	2.0	–	2.5	–	ns
	H2	C/$\overline{D}$ to SCLK ↓		12.0	–	14.0	–	12.0	–	14.0	–	
	H3	SDI to SCLK ↑		1.0	–	1.0	–	1.0	–	1.0	–	
	H4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)		2.0	–	2.5	–	2.0	–	2.5	–	
	H5	SCLK (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–	2.0	–	2.5	–	
	H6	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–	2.0	–	2.5	–	
	H7	Y to PCLK ↑ (Inst. 3)		4.5	–	5.0	–	4.5	–	5.0	–	
t_{PHZ} t_{PLZ}	1Z	$\overline{OE}_Y$ to Y		3.0	10.0	3.0	11.0	3.0	8.0	3.0	9.0	ns
	2Z	SCLK ↑ to D (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	3Z	C/$\overline{D}$ ↑ to D or Y (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	4Z	SCLK ↑ to Y ($\overline{OE}_Y$ = High Inst. 8 & 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	5Z	C/$\overline{D}$ to ↑ to D or Y ($\overline{OE}_Y$ = High Inst. 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
t_{PZH} t_{PZL}	Z1	$\overline{OE}_Y$ to Y		3.0	11.0	3.0	12.0	3.0	9.0	3.0	10.0	ns
	Z2	C/$\overline{D}$ ↓ to D (Inst. 5 & 9)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
	Z3	C/$\overline{D}$ ↓ to Y ($\overline{OE}_Y$ = High Inst. 14)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
t_W	W1	PCLK (High & Low)		7.0	–	8.0	–	7.0	–	8.0	–	ns
	W2	SCLK (High & Low)		25.0	–	25.0	–	25.0	–	25.0	–	
	W3	C/$\overline{D}$ (High)		25.0	–	25.0	–	25.0	–	25.0	–	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Preliminary information only.

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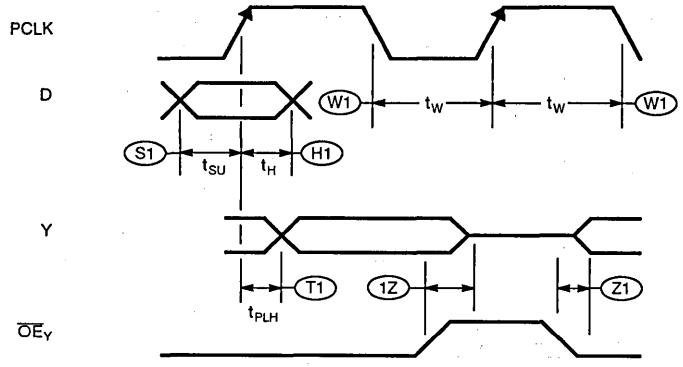
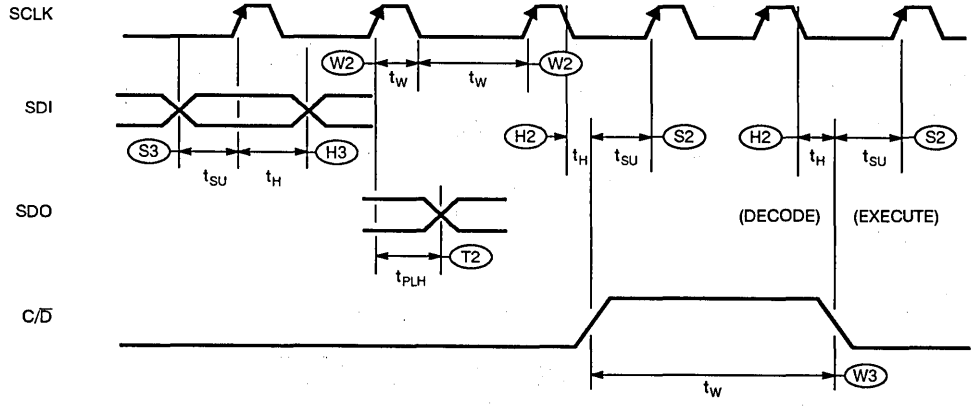
GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS

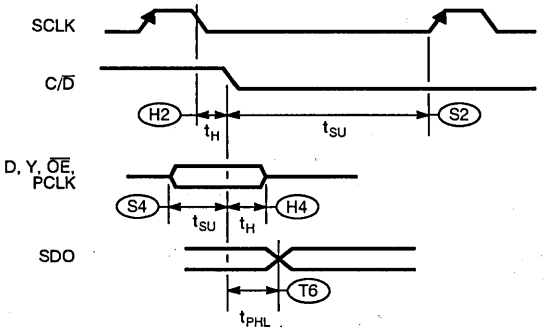


GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS

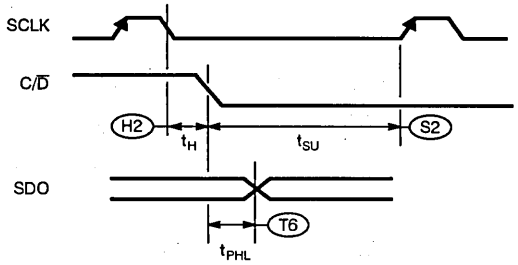


DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

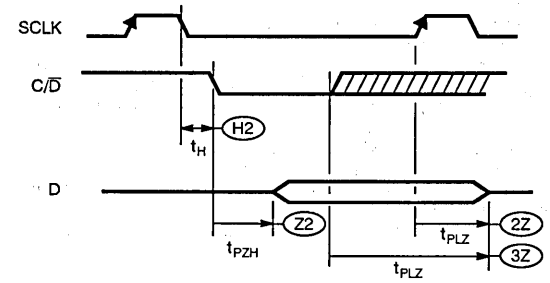
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



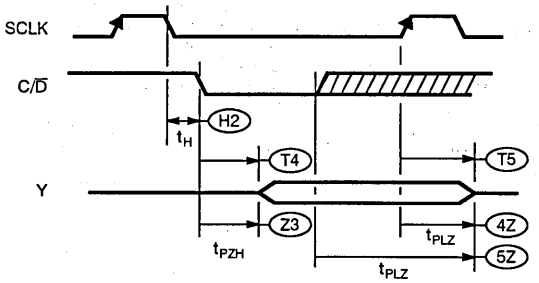
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



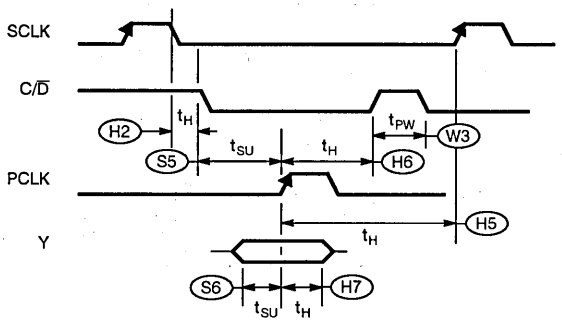
CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



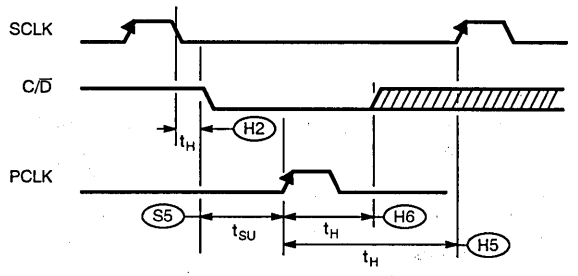
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



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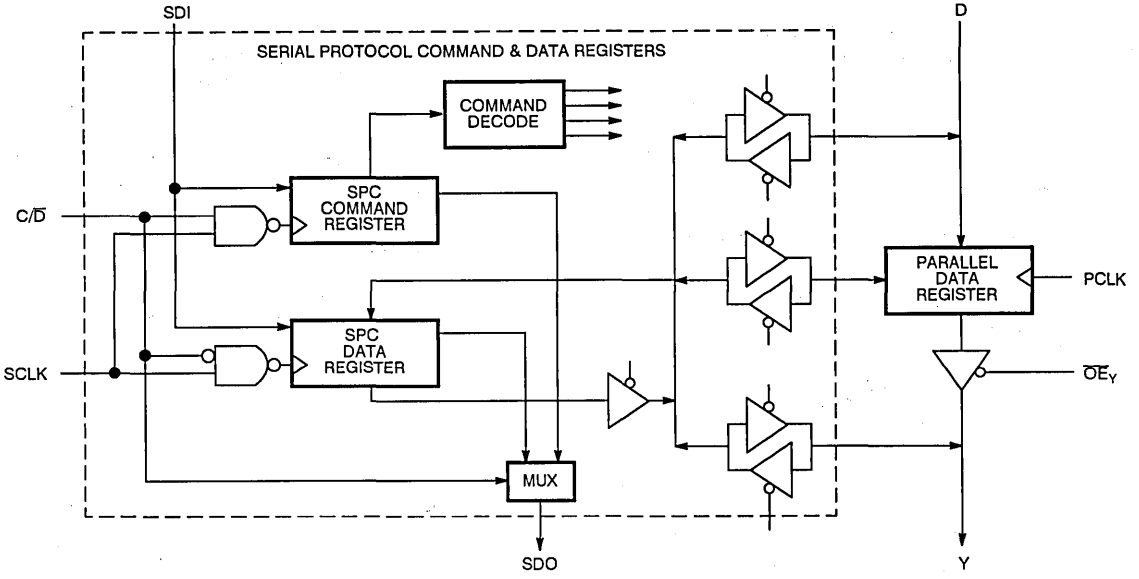
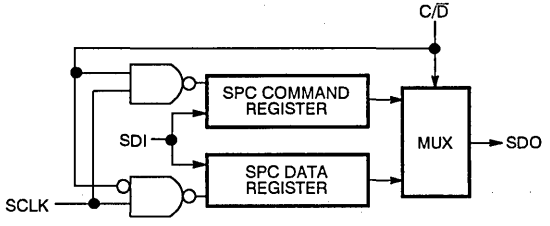
DETAILED FUNCTIONAL BLOCK DIAGRAM



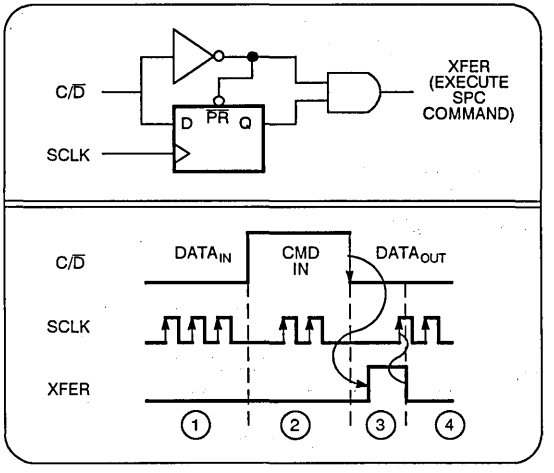
The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. The main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.



SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge.



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

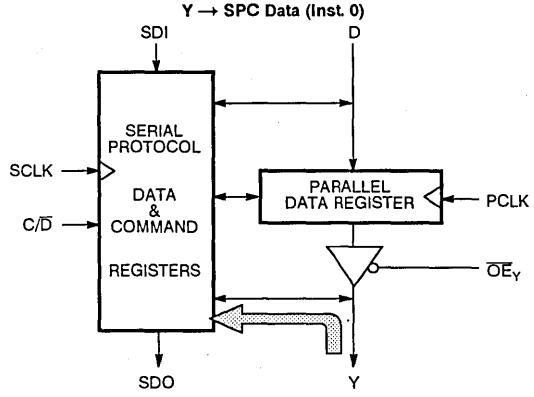
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

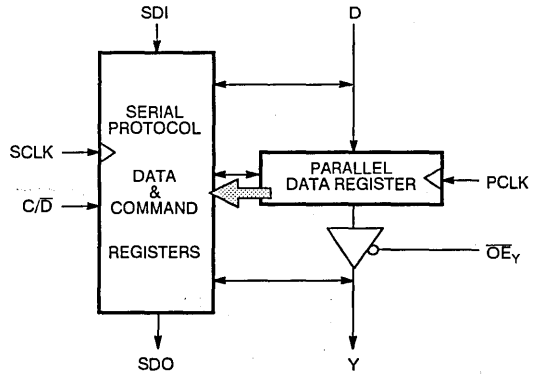
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

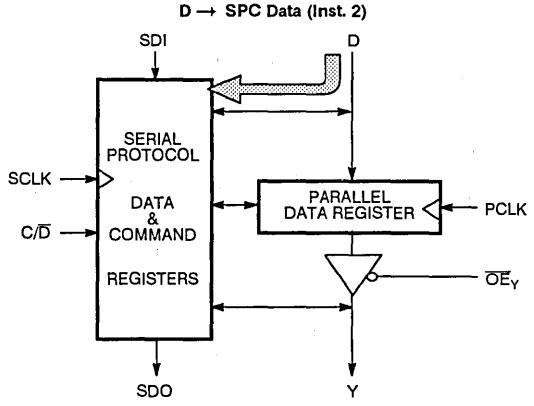
Y → SPC Data (Inst. 0)



Data Register → SPC Data (Inst. 1)



D → SPC Data (Inst. 2)



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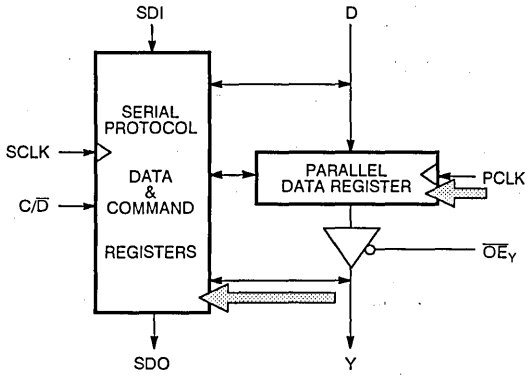
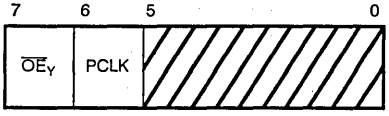
Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

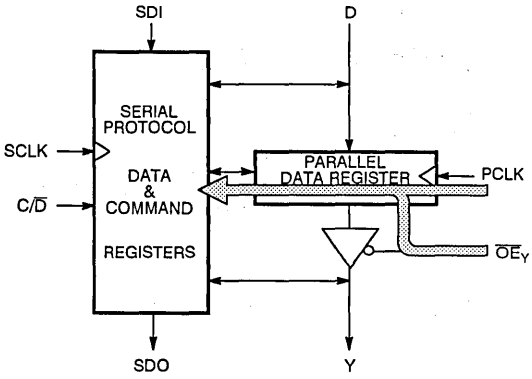
Y → SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

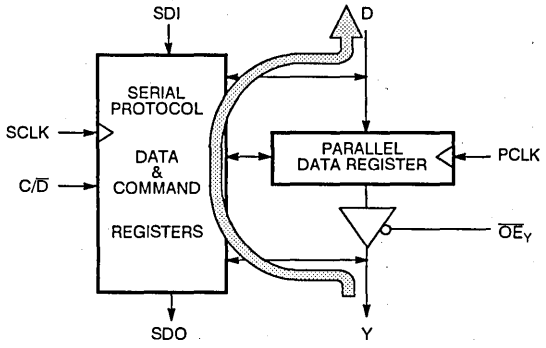


Status → SPC Data (Inst. 4)

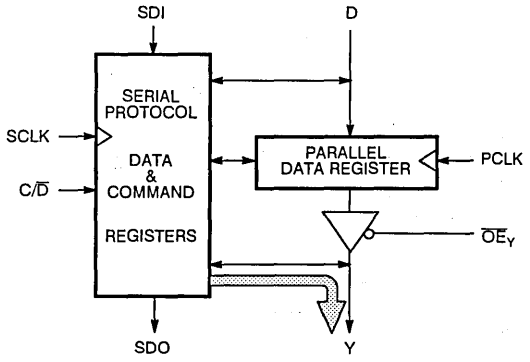


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

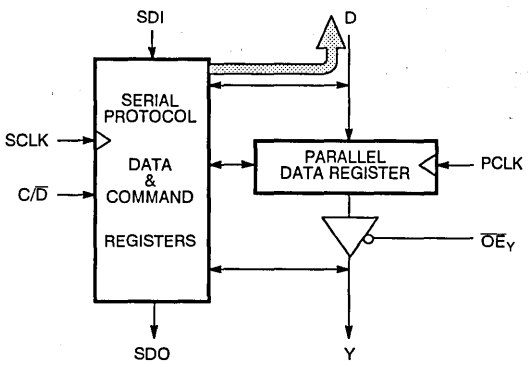


SPC Data → Y (Inst. 8)



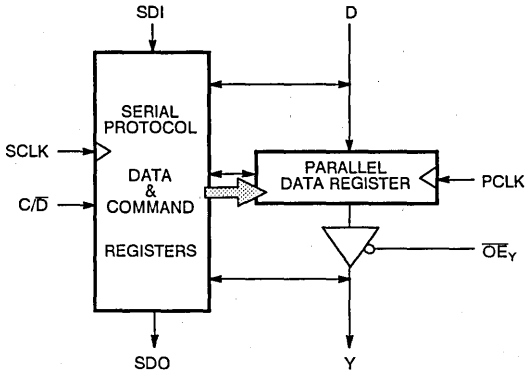
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

SPC Data → D (Inst. 9)



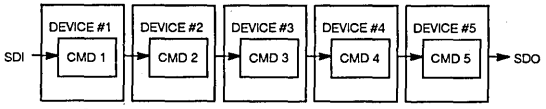
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.

SPC Data → Parallel Data Register (Inst. 10)



Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

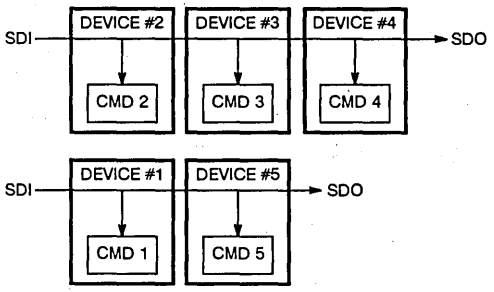
SERIAL MODE



In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

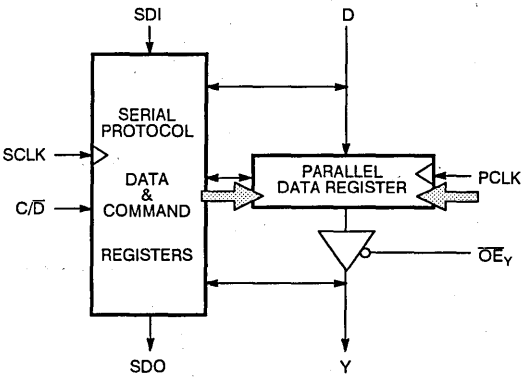
Note: The state of $\overline{OE}_Y$ is a "do not care;" that is, data will be output even if $\overline{OE}_Y$ = High.

STUB MODE

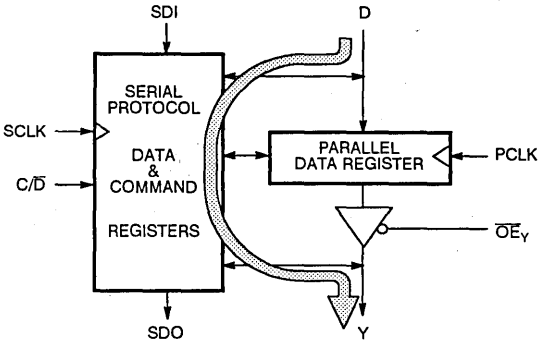


Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again, The operation is terminated by SCLK.

SPC Data → Parallel Data Register Synchronous w/PCLK (Inst. 13)



Connect D to Y (Inst. 14)



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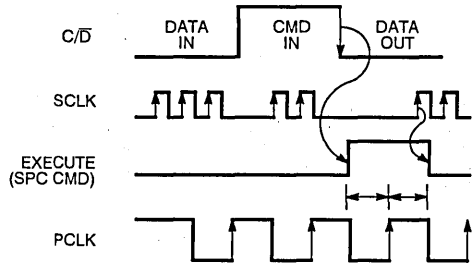
Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



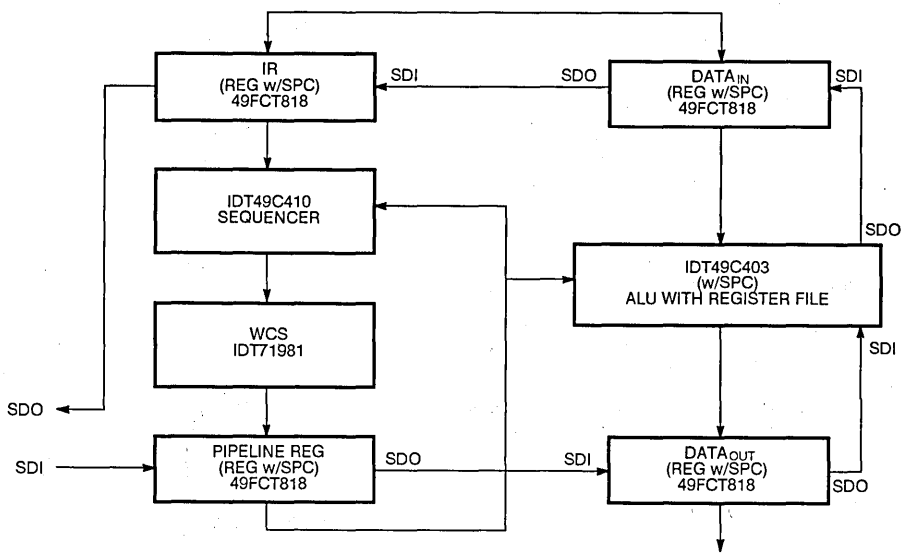
The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

TYPICAL APPLICATION

In the block diagram of the typical application, the SPC data register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostics path. The SPC data register is used for the instruction register going into the IDT49C410, as well as for data registers around the IDT49C403. In this way, the designer may use the SPC data register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which includes an SPC port for diagnostic and break point purposes.

The block diagram of the diagnostics ring shows how devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals, The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

TYPICAL MICROPROGRAM APPLICATION WITH SPC™



As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, it may be necessary to use $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for ATE testing purposes.

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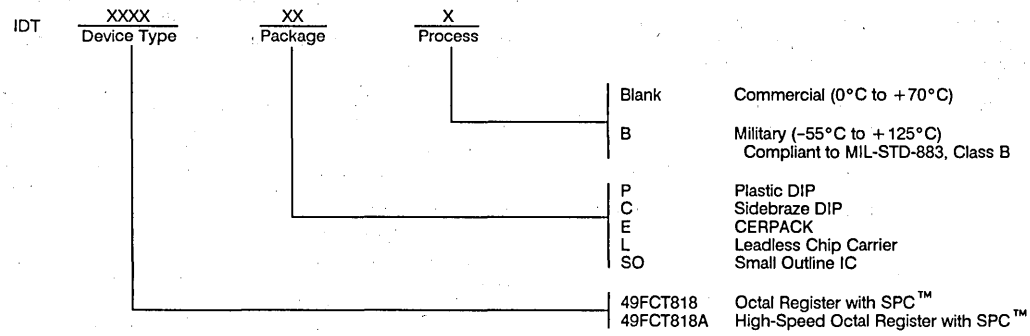
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER

IDT 54/74FCT138
IDT 54/74FCT138A

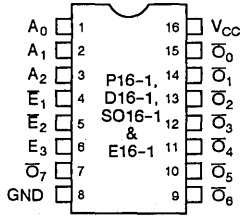
FEATURES:

- IDT54/74FCT138 equivalent to FAST™ speed; **IDT54/74FCT138A 35% faster than FAST™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 1-of-8 decoder with enables
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87654 is listed on this function. Refer to Section 2/page 2-4.

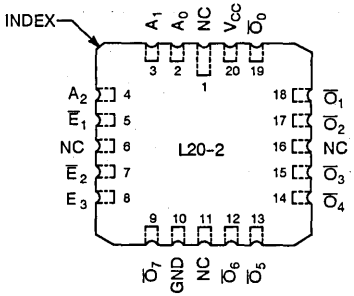
DESCRIPTION:

The IDT54/74FCT138 and IDT54/74FCT138A are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138 and IDT54/74FCT138A accept three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138 and IDT54/74FCT138A feature three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138 or IDT54/74FCT138A devices and one inverter.

PIN CONFIGURATIONS

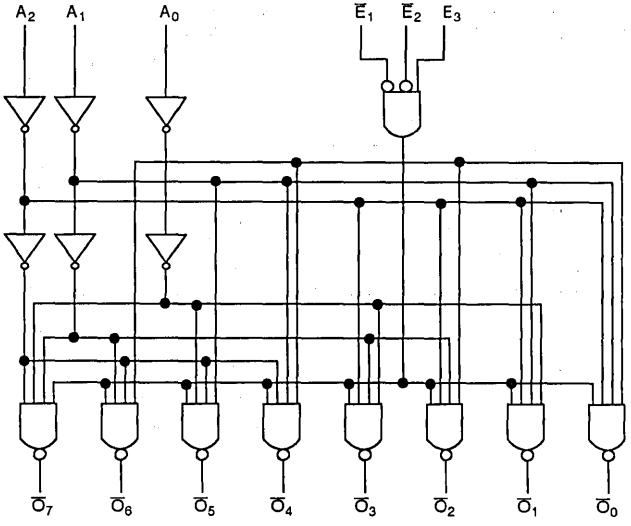


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP. (2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5 (4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5 (4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.5	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	0.38	2.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	0.63	3.3[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0 - A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$ - $\overline{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

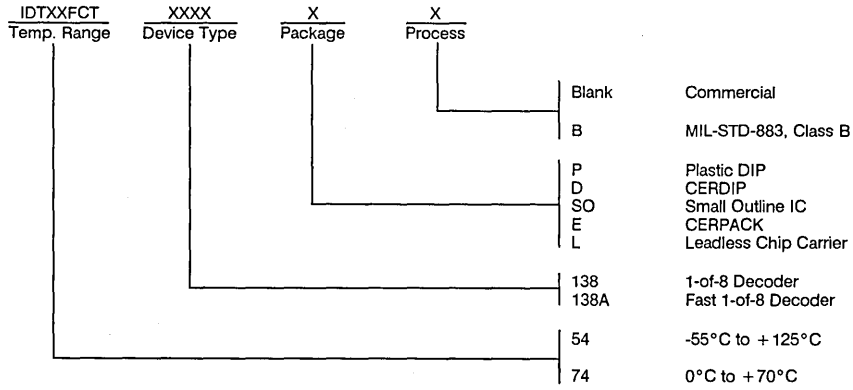
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT138					IDT54/74FCT138A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	7.0	1.5	9.0	1.5	12.0	4.5	1.5	5.8	1.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		6.0	1.5	9.0	1.5	12.5	4.5	1.5	5.9	1.5	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		6.0	1.5	9.0	1.5	12.5	4.5	1.5	5.9	1.5	8.0	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS CARRY LOOKAHEAD GENERATOR

IDT 54/74FCT182
IDT 54/74FCT182A

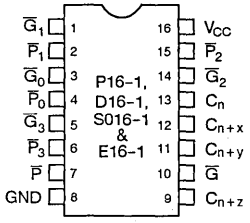
FEATURES:

- IDT54/74FCT182 equivalent to FAST™ speed; **IDT54/74FCT182A 30% faster than FAST™**
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Carry lookahead generator
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

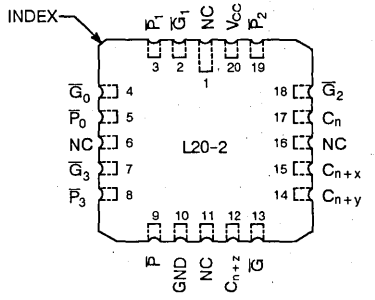
DESCRIPTION:

The IDT54/74FCT182 and IDT54/74FCT182A are high-speed carry lookahead generators built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT182 and IDT54/74FCT182A are carry lookahead generators that accept up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n) and provides anticipated HIGH carries (C_{n+y}, C_{n+z}) across four groups of binary adders. These products also have active LOW Carry Propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

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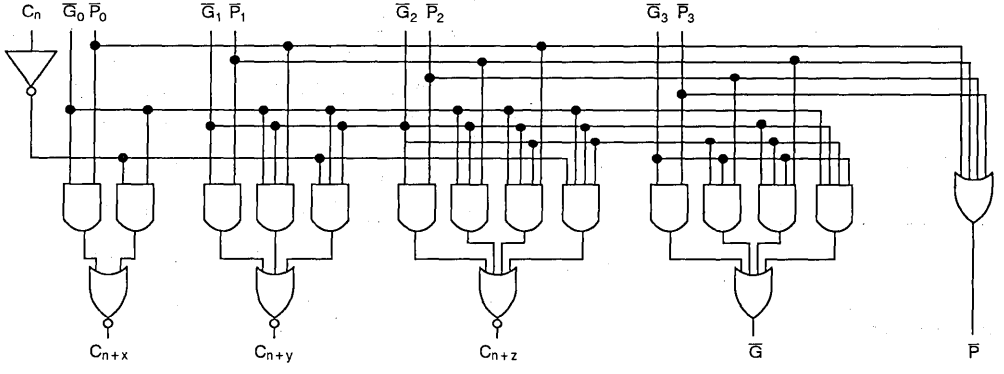
FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[5,6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x} - C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	X	X	L						H			
X	X	X	X	H	H	H					L		
X	X	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	L	X	L	X					H		
X	X	X	X	L	X	X					H		
H	X	X	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	X	H	X				H	
	X		H	H	H	X	H	X				H	
	H		X	X	X	X	X	X				L	
	X		X	X	L	X	L	L				L	
	X		X	X	X	L	X	L				L	
	X		X	X	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

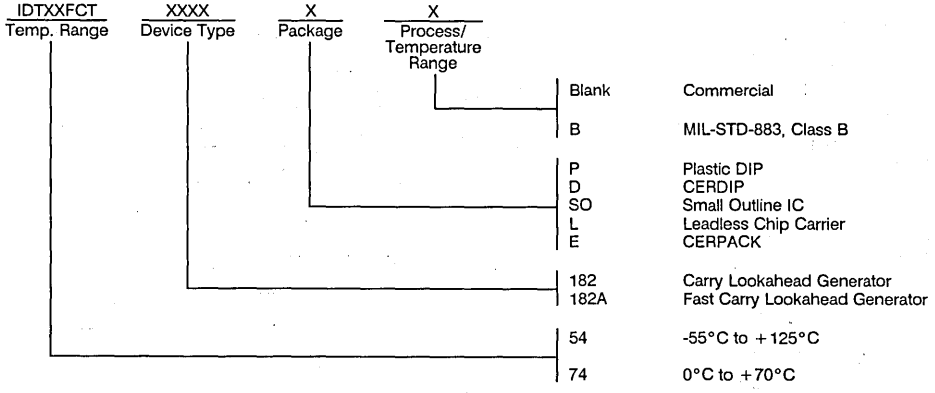
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT182					IDT54/74FCT182A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+y}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	6.0	2.0	10.0	2.0	16.5	4.0	2.0	7.0	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, to C_{n+y}, C_{n+y}, C_{n+z}		6.0	1.5	9.0	1.5	11.5	4.0	1.5	8.5	1.5	9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		6.0	1.5	9.5	1.5	11.5	4.0	1.5	8.5	1.5	9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$ $\overline{P}_3$ to $\overline{G}$		7.0	2.0	11.0	2.0	16.5	4.8	2.0	7.2	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$		7.5	2.0	11.5	2.0	16.5	5.0	2.0	7.6	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$		6.0	1.5	8.5	1.5	12.5	4.0	1.5	6.0	1.5	7.4	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT 54/74FCT240
IDT 54/74FCT240A

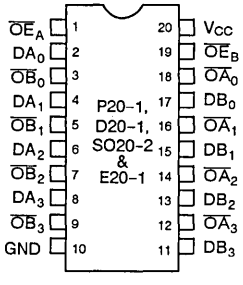
FEATURES:

- IDT54/74FCT240 equivalent to FAST™ speed; **IDT54/74FCT240A 30% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87655 is listed on this function.

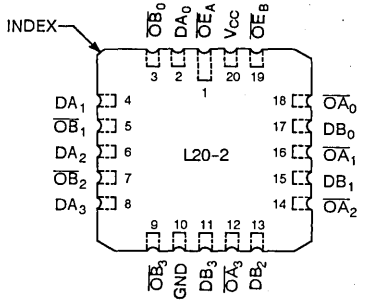
DESCRIPTION:

The IDT54/74FCT240/A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

PIN CONFIGURATIONS

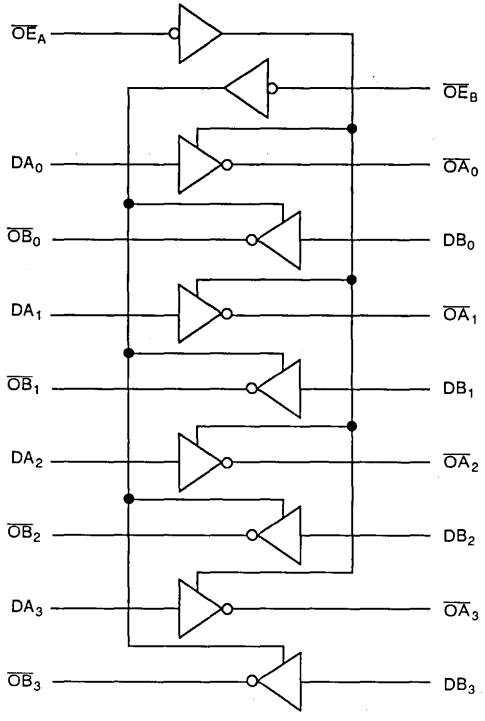


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTES:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS FOR 'FCT240

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
D_{XX}	Inputs
$\overline{O}_{XX}$	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT240					IDT54/74FCT240A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	5.0	1.5	8.0	1.5	9.0	3.5	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	1.5	10.0	1.5	10.5	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	9.5	1.5	12.5	4.3	1.5	5.6	1.5	5.9	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

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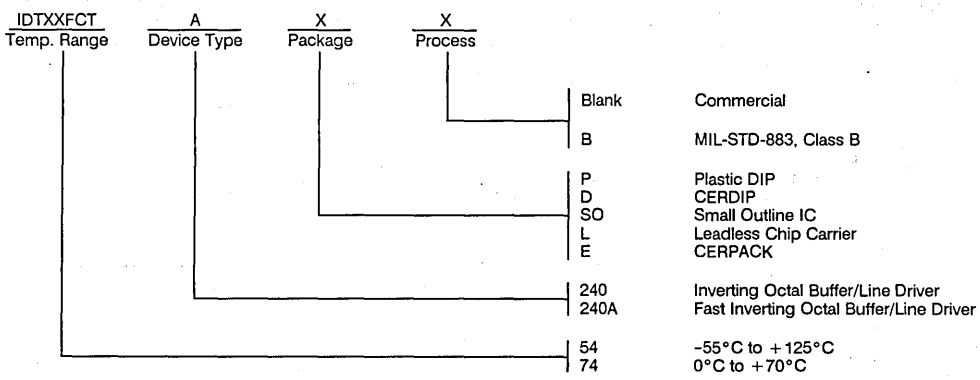
ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT 54/74FCT241/A
IDT 54/74FCT244/A

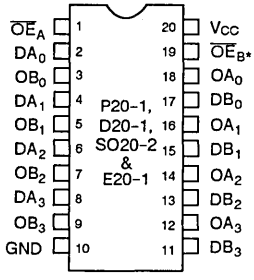
FEATURES:

- IDT54/74FCT241/244 equivalent to FAST™ speed; **IDT54/74FCT241A/244A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (Commercial), 48mA (Military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87630 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

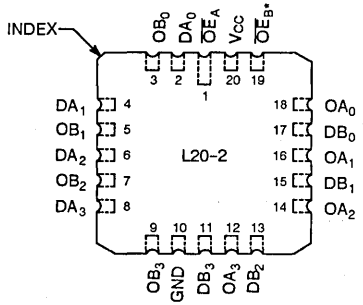
The IDT54/74FCT241/244 and IDT54/74FCT241A/244A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/ receivers which provide improved board density.

PIN CONFIGURATIONS



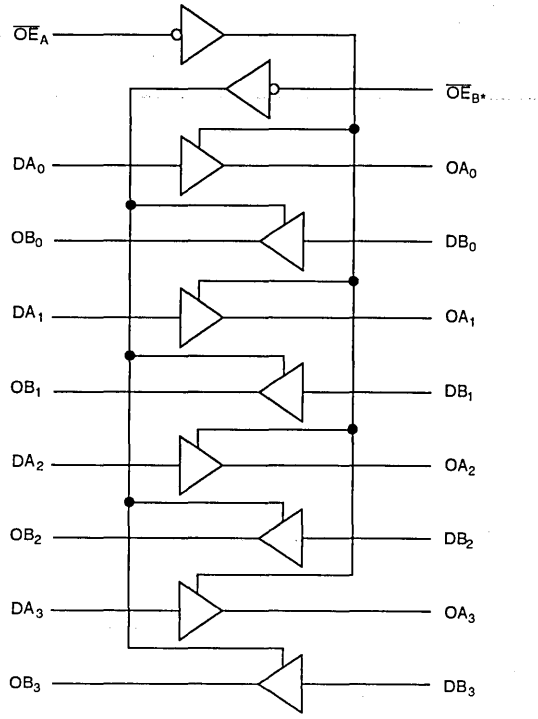
DIP/SOIC/CERPACK TOP VIEW

*$\overline{OE}_B$ for 'FCT241
$\overline{OE}_B$ for 'FCT244



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

DSC-4020/-1

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS FOR 'FCT241

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = OE_B = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = OE_B = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = OE_B = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

POWER SUPPLY CHARACTERISTICS FOR 'FCT244

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$ (1)	3-State Output Enable Input (Active LOW)
D_{xx}	Inputs
O_{xx}	Outputs

NOTE:
1. For 'FCT241 use OE_B, and for 'FCT244 use $\overline{OE}_B$.

TRUTH TABLE FOR 'FCT241

INPUTS			OUTPUT
$\overline{OE}_A$,	OE_B	D	
L	H	L	L
L	H	H	H
H	L	X	Z

TRUTH TABLE FOR 'FCT244

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level X = Don't Care
L = LOW Voltage Level Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FCT241

SYMBOL	PARAMETER	CONDITION (1)	IDT54/74FCT241					IDT54/74FCT241A (4)					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	4.0	1.5	6.5	1.5	7.0	3.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		5.5	1.5	8.0	1.5	8.5	4.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		4.5	1.5	7.0	1.5	7.5	3.0	1.5	5.6	1.5	5.9	ns

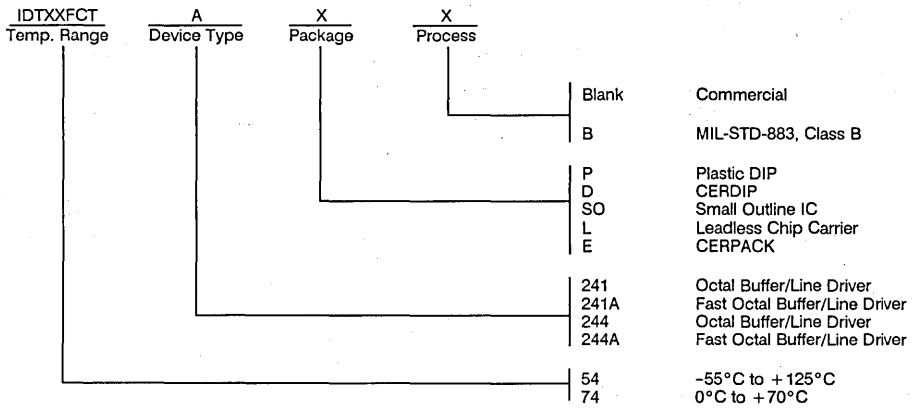
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These numbers are preliminary only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR 'FCT244

SYMBOL	PARAMETER	CONDITION (1)	IDT54/74FCT244					IDT54/74FCT244A					UNIT
			TYP.(3)	COM'L.		MIL.		TYP.(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	4.5	1.5	6.5	1.5	7.0	3.1	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		6.0	1.5	8.0	1.5	8.5	3.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		5.0	1.5	7.0	1.5	7.5	3.3	1.5	5.6	1.5	5.9	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT 54/74FCT245
IDT 54/74FCT245A

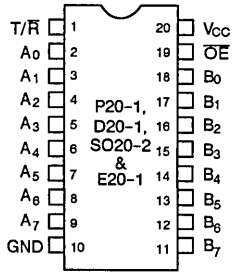
FEATURES:

- IDT54/74FCT245 equivalent to FAST™ speed; **IDT54/74FCT245A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military) for both ports
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87629 is listed on this function. Refer to Section 2/page 2-4.

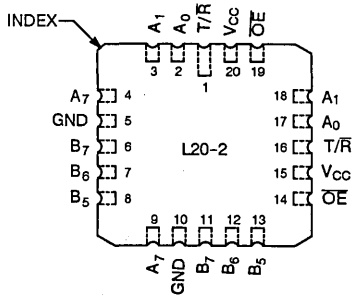
DESCRIPTION:

The IDT54/74FCT245 and IDT54/74FCT245A are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™, a dual metal CMOS technology. These bidirectional buffers have 3-state outputs and are intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS

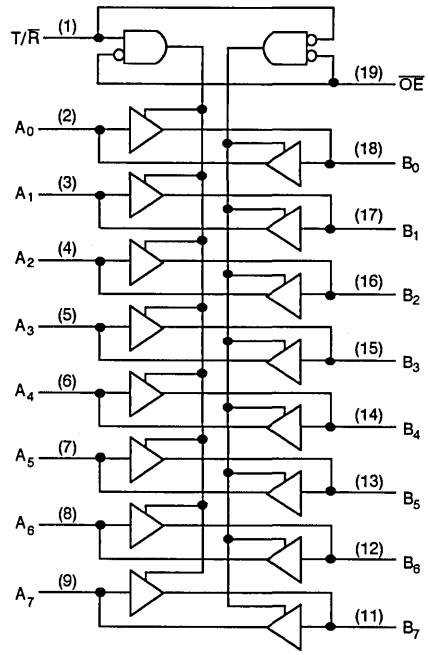


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage (Port A and Port B)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$[6] $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V[6] V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

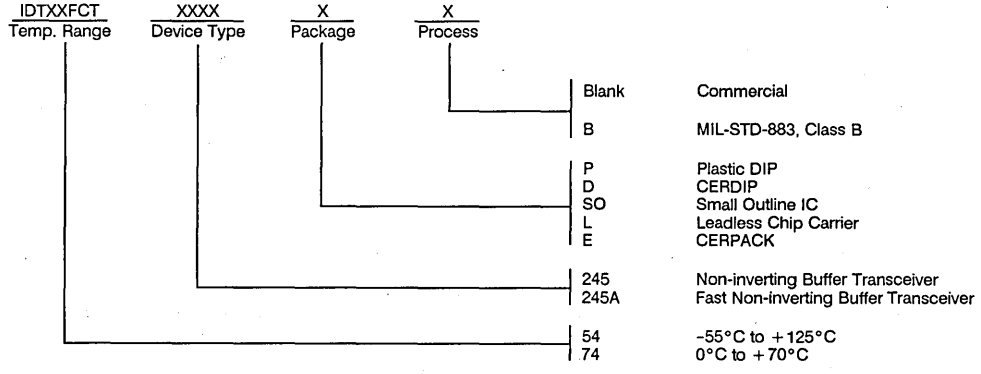
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT245					IDT54/74FCT245A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	5.0	1.5	7.0	1.5	7.5	3.3	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		6.0	1.5	9.5	1.5	10.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		6.0	1.5	7.5	1.5	10.0	4.5	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[4]		6.0	1.5	9.5	1.5	10.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Enable Time T/$\overline{R}$ to A or B[4]		6.0	1.5	7.5	1.5	10.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT 54/74FCT273
IDT 54/74FCT273A

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed; **IDT54/74FCT273A 45% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clear
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87656 is listed on this function. Refer to Section 2/page 2-4.

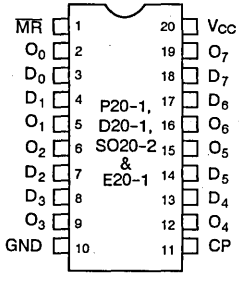
DESCRIPTION:

The IDT54/74FCT273 and IDT54/74FCT273A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273 and IDT54/74FCT273A have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

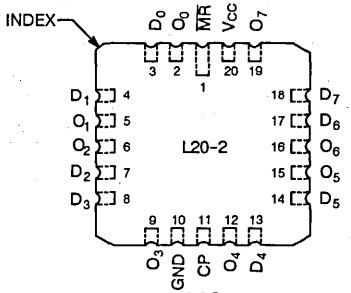
The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS

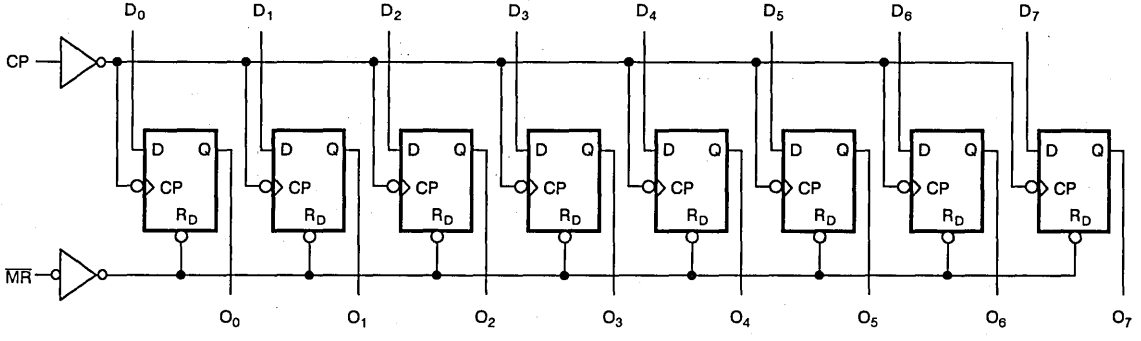


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - .2
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{MR} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$D_0 - D_7$	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$O_0 - O_7$	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

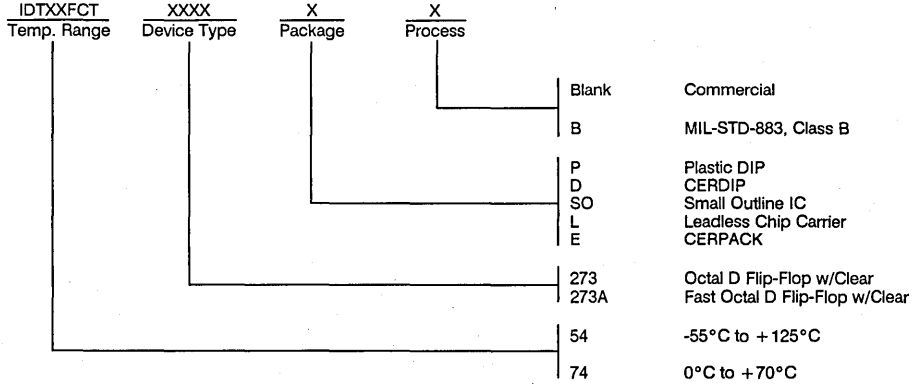
H = HIGH voltage steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady rate
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT273					IDT54/74FCT273A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	C_L = 50pF R_L = 500Ω	7.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		8.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{SU}	Set-up Time HIGH or LOW Data to CP		3.0	3.0	–	3.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW Data to CP		1.0	2.0	–	2.0	–	1.0	1.5	–	1.5	–	ns
t_W	Clock Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	3.0	6.0	–	6.0	–	ns
t_W	$\overline{MR}$ Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	3.0	6.0	–	6.0	–	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		3.0	4.0	–	5.0	–	1.5	2.0	–	2.5	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT 54/74FCT299
IDT 54/74FCT299A

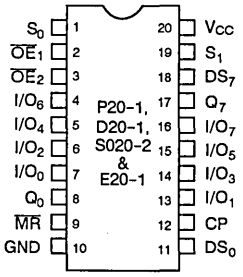
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed; **IDT54/74FCT299A 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to Section 2/page 2-4.

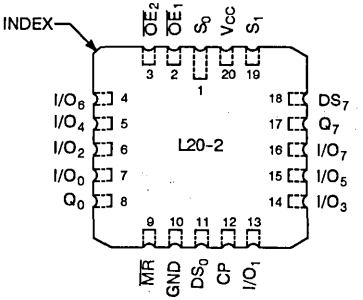
DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible; hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS

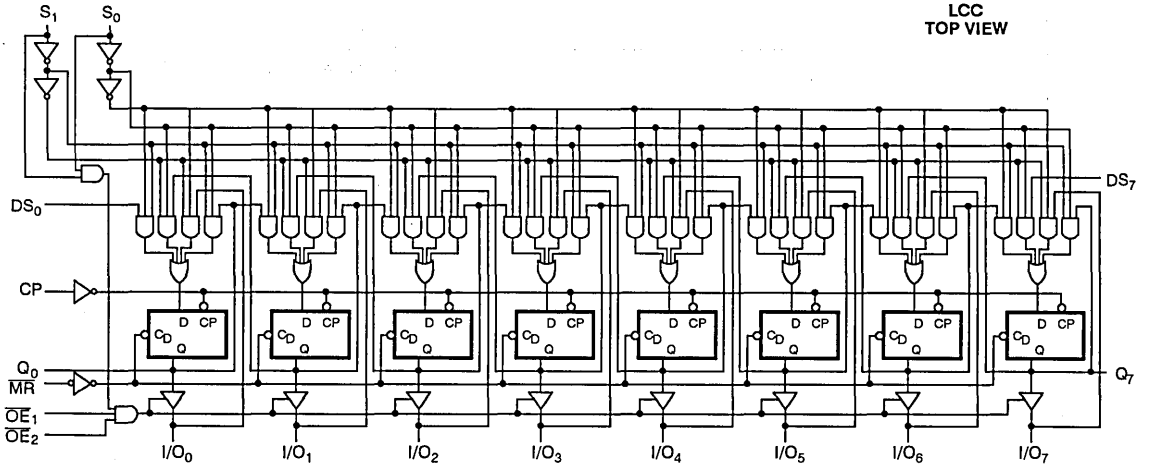


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Currents (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15[4]	
I_{IL}	Input LOW Currents (I/O pins only)		V_I = 0.5V	–	–	-15[4]	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC}= 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_7	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0 - I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset Q_0-Q_7 = LOW
H	H	H	⎍	Parallel Load; I/O $\rightarrow Q_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

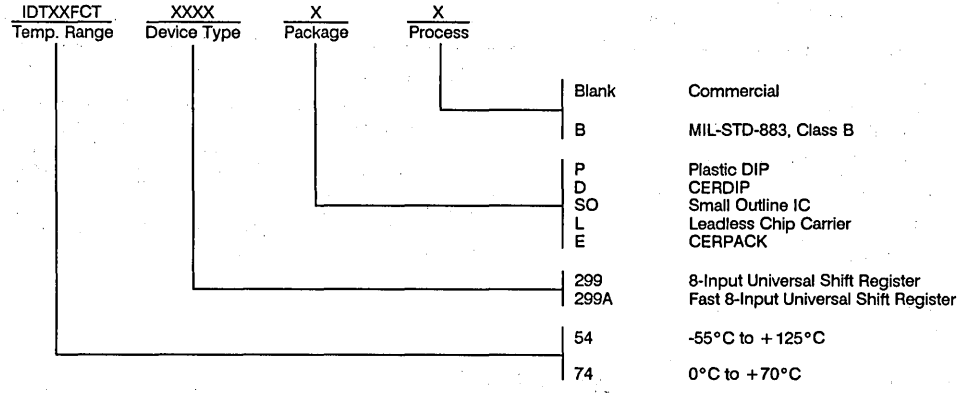
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT299					IDT54/74FCT299A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	7.0	2.0	10.0	2.0	14.0	5.0	2.0	7.2	2.0	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		6.0	2.0	12.0	2.0	12.0	5.0	2.0	7.2	2.0	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		7.0	2.0	10.0	2.0	10.5	5.0	2.0	7.2	2.0	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		7.0	2.0	15.0	2.0	15.0	6.0	2.0	8.7	2.0	11.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n		8.0	1.5	11.0	1.5	15.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n		5.5	1.5	7.0	1.5	9.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		2.0	7.5	–	7.5	–	2.5	3.5	–	4.0	–	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		0	1.0	–	1.0	–	-1.5	1.0	–	1.0	–	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		0.5	5.5	–	5.5	–	2.5	4.0	–	4.5	–	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		7.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

10

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH

IDT 54/74FCT373
IDT 54/74FCT373A

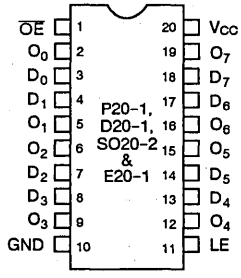
FEATURES:

- IDT54/74FCT373 equivalent to FAST™ speed; **IDT54/74FCT373A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87644 is listed on this function. Refer to Sction 2/page 2-4.

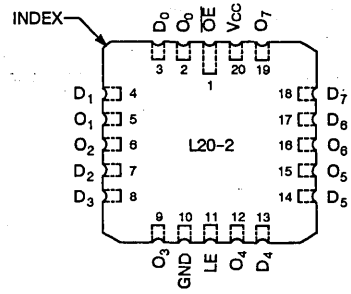
DESCRIPTION:

The IDT54/74FCT373 and IDT54/74FCT373A are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

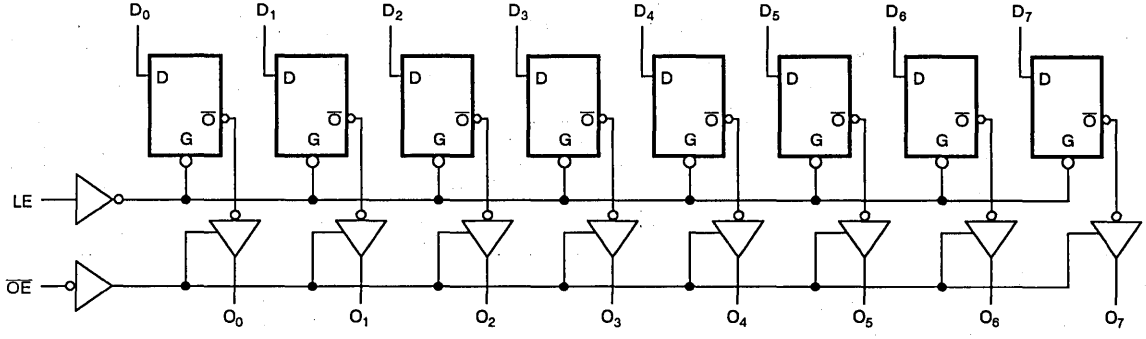


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0 - D_7	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0 - O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

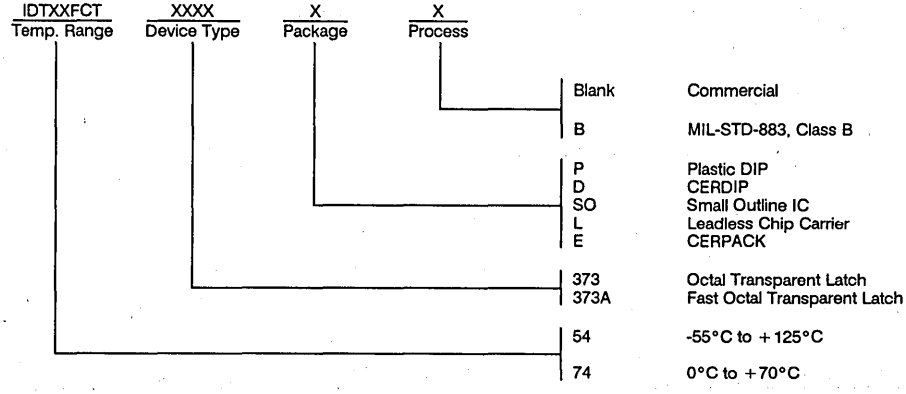
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT373					IDT54/74FCT373A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	5.0	1.5	8.0	1.5	8.5	4.0	1.5	5.2	1.5	5.6	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	1.5	12.0	1.5	13.5	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	7.5	1.5	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	2.0	13.0	2.0	15.0	7.0	2.0	8.5	2.0	9.8	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		1.0	2.0	–	2.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	–	6.0	–	4.0	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTER (3-STATE)

IDT 54/74FCT374
IDT 54/74FCT374A

FEATURES:

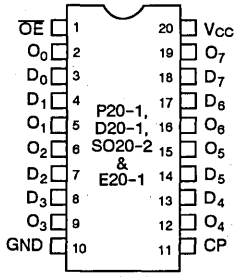
- IDT54/74FCT374 equivalent to FAST™ speed; **IDT54/74FCT374A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Positive, edge-triggered Master/Slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87628 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

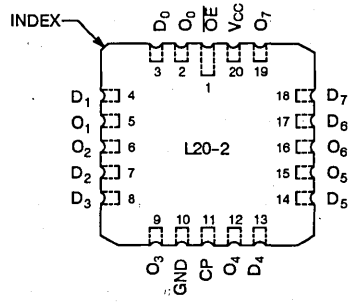
The IDT54/74FCT374 and IDT54/74FCT374A are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

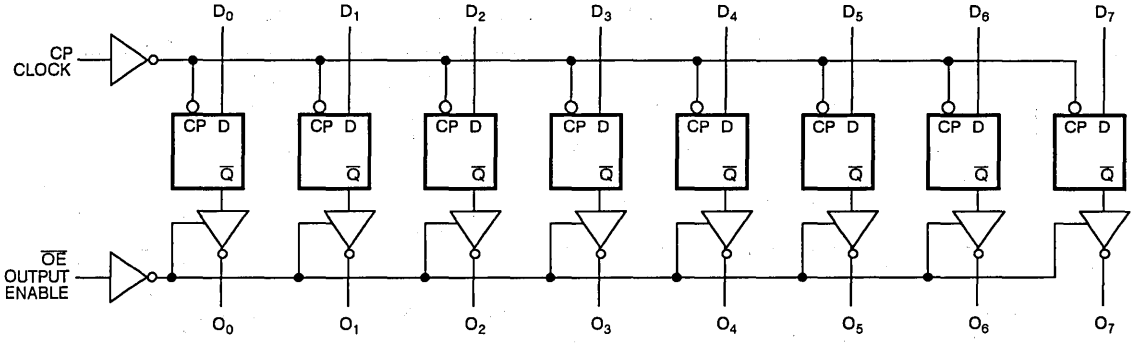


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	$\overline{Q}_I$
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↗	L	L	H
	L	↗	H	H	L
	H	↗	L	Z	H
	H	↗	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↗ = LOW-to-HIGH transition
NO = No Change

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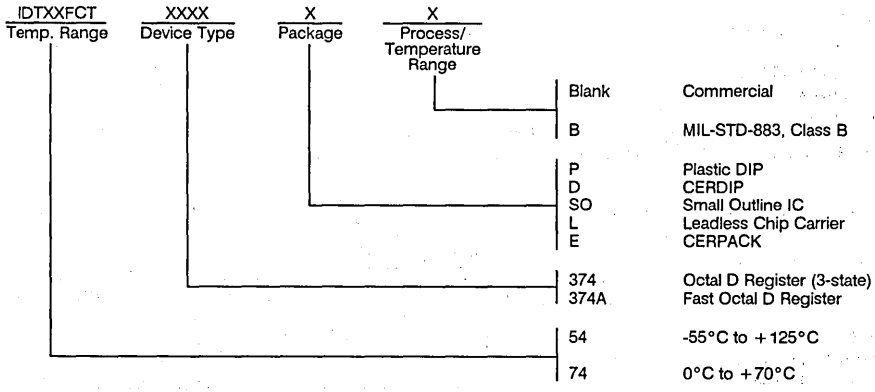
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT374					IDT54/74FCT374A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	C_L = 50pF R_L = 500Ω	6.6	2.0	10.0	2.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	12.5	1.5	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	8.0	1.5	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.0	–	2.5	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		0.5	2.0	–	2.0	–	0.5	1.5	–	1.5	–	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	–	7.0	–	4.0	5.0	–	6.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT 54/74FCT377
IDT 54/74FCT377A

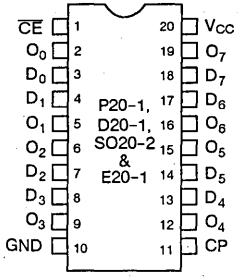
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed; **IDT54/74FCT377A 45% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clock enable
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87627 is pending listing on this function. Refer to Section 2/page 2-4.

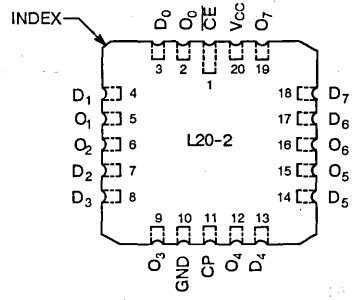
DESCRIPTION:

The IDT54/74FCT377 and IDT54/74FCT377A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AFCT377 and IDT54/74FCT377A have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS

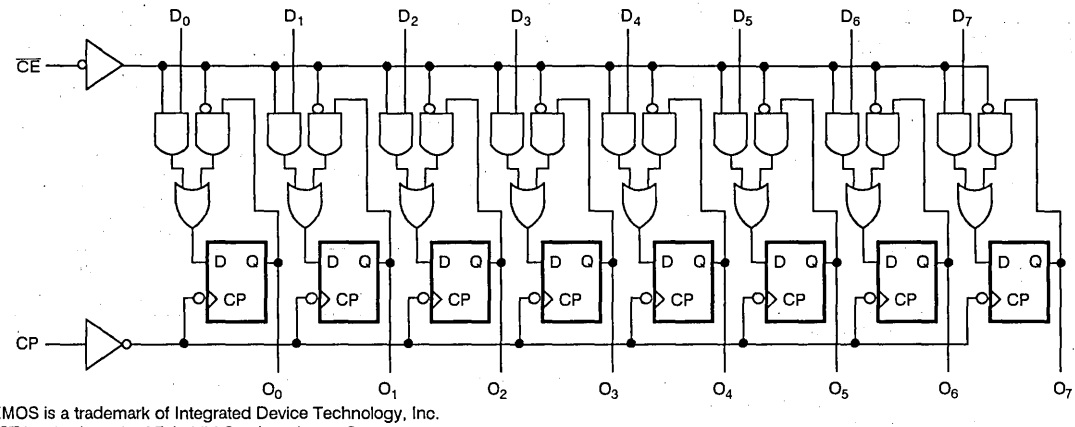


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

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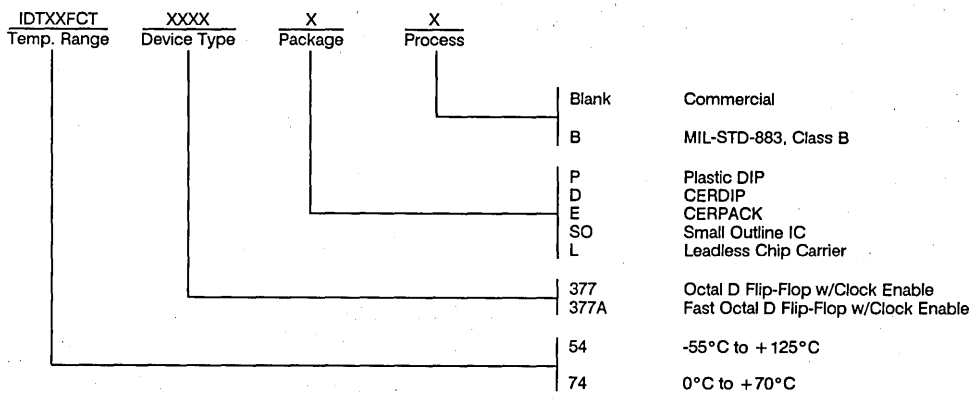
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT377					IDT54/74FCT377A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	7.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		1.0	2.5	–	3.0	–	1.0	2.0	–	2.0	–	ns
t_H	Hold Time HIGH or LOW D_n to CP		1.0	2.0	–	2.5	–	1.0	1.5	–	1.5	–	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{CE}$ to CP		1.5	4.0	–	4.0	–	1.0	3.5	–	3.5	–	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		3.0	1.5	–	1.5	–	1.0	1.5	–	1.5	–	ns
t_W	Clock Pulse Width, LOW		4.0	7.0	–	7.0	–	4.0	6.0	–	7.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT 54/74FCT399
IDT 54/74FCT399A

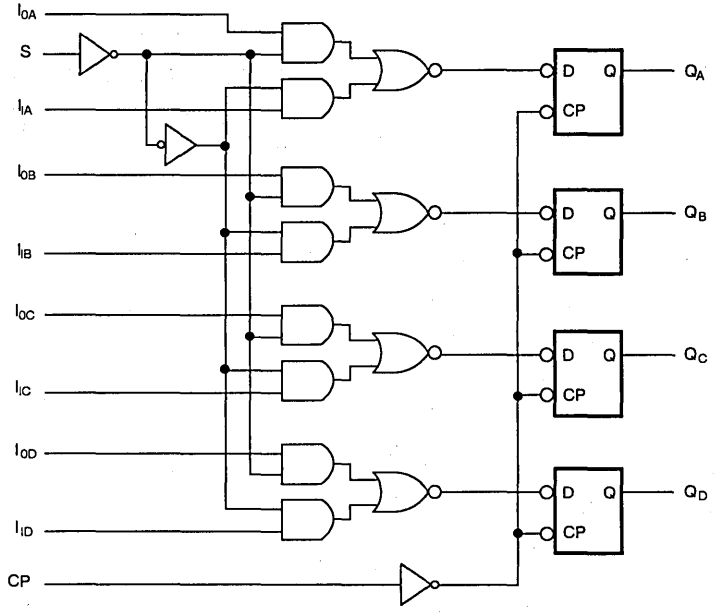
FEATURES:

- IDT54/74FCT399 equivalent to FAST™ speed; **IDT54/74FCT399A 30% faster than FAST™**
- Equivalent to FAST™ pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 16-pin DIP and SOIC, and 20-pin LCC
- Military product compliant to MIL-STD-883, Class B
- Product available in Radiation Tolerant and Enhanced versions

DESCRIPTION:

Both these devices are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM



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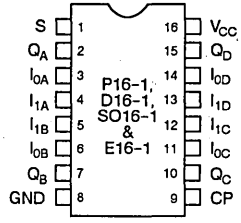
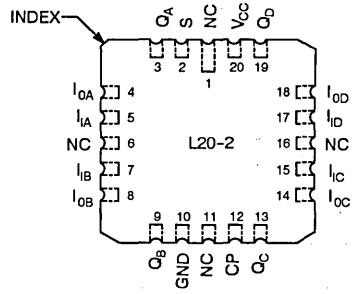
PIN CONFIGURATIONS

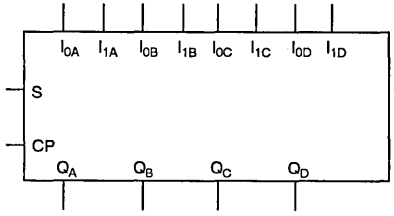


DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I_{0A}-I_{0D}	Data Inputs from Source 0
I_{1A}-I_{1D}	Data Inputs from Source 1
Q_A - Q_D	Register True Outputs

FUNCTIONAL TABLE

INPUTS			OUTPUTS
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
X = Immaterial

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle One Input Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Four Inputs Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.75[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	12.75[5]	

NOTES:

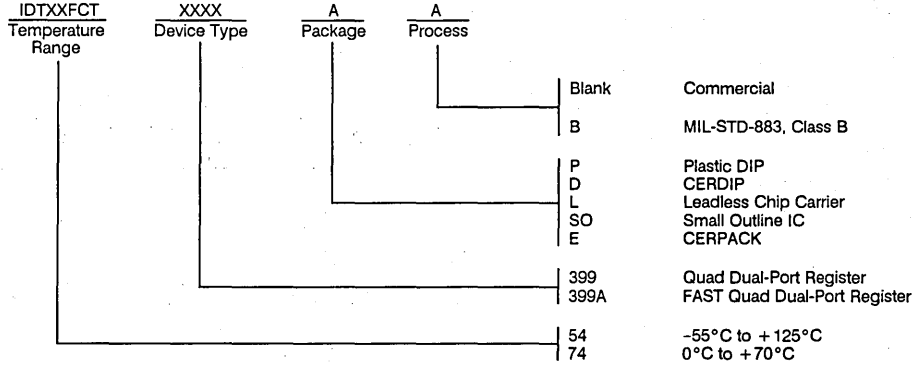
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		(1)	IDT54FCT399					IDT54FCT399A					
			(3)	COM'L.		MIL.		(3)	COM'L.		MIL.		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$	C_L = 50pF R_L = 500Ω	6.8	3.0	10.0	3.0	11.5	4.0	2.5	7.0	2.5	7.5	ns
t_{SU}	Set-Up Time HIGH or LOW I_n to CP		3.0	4.0	–	4.5	–	2.5	3.5	–	4.0	–	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	1.0	–	1.5	–	1.0	1.0	–	1.0	–	ns
t_{SU}	Set-Up Time HIGH or LOW S to CP		8.0	9.0	–	9.5	–	7.0	8.5	–	9.0	–	ns
t_H	Hold Time HIGH or LOW S to CP		0	0	–	0	–	0	0	–	0	–	ns
t_W	CP Pulse Width, HIGH or LOW(4)		4.0	5.0	–	7.0	–	3.5	5.0	–	6.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V and +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/ LINE DRIVER

PRELIMINARY
IDT 54/74FCT540/A
IDT 54/74FCT541/A

FEATURES:

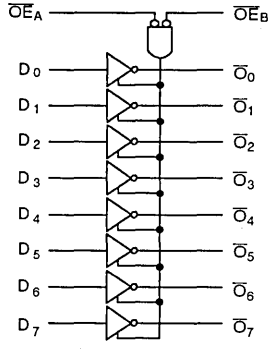
- IDT54/74FCT540/41 equivalent to FAST™ speed; **IDT54/74FCT540A/41A 30% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- Octal buffer/line driver with 3-state output
- Pinout arrangement for flow-through architecture
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- Available in CERDIP, Plastic DIP, LCC and SOIC
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

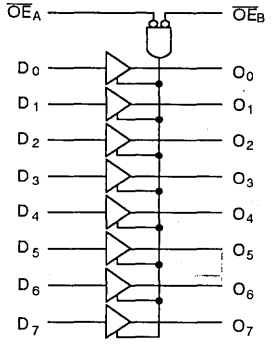
The IDT54/74FCT540/A and IDT54/74FCT541/A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology.

These devices are similar in function to the IDT54/74FCT240 and IDT54/74FCT241, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAM

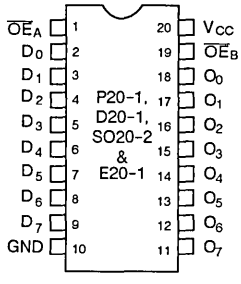


IDT54/74FCT540

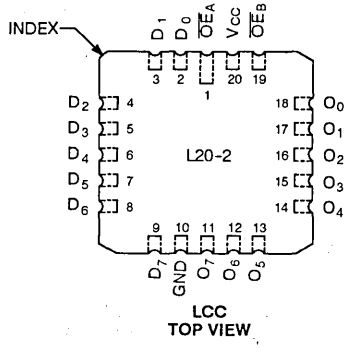


IDT54/74FCT541

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
D_{XX}	Inputs
O_{XX}	Outputs

TRUTH TABLE

INPUTS		OUTPUT	
$\overline{OE}_A$, $\overline{OE}_B$	D	540	541
L	L	H	L
L	H	L	H
H	X	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5[4]	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10[4]	
			V_O = 0.5V	–	–	-10[4]	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B$ = GND Eight Inputs Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

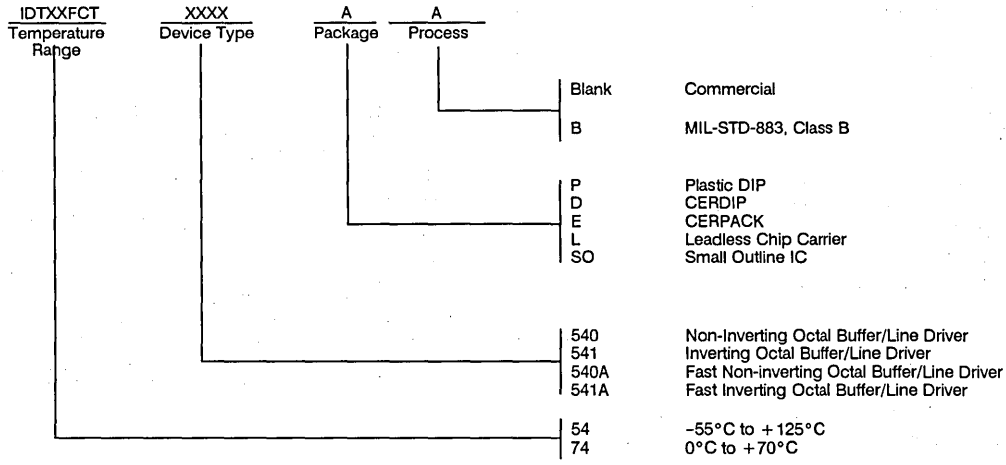
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		[1]	IDT54/74FCT540/541					IDT54/74FCT540A/541A					
				COM'L.		MIL.			COM'L.		MIL.		
			[3]	MIN.[2]	MAX.	MIN.[2]	MAX.	[3]	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n IDT54/74FCT540	C_L = 50pF R_L = 500Ω	5.0	2.0	8.5	2.0	9.5	3.5	2.0	4.8	2.0	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n IDT54/74FCT541		5.0	2.0	8.0	2.0	9.0	3.5	2.0	4.8	2.0	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		7.0	2.0	10.0	2.0	10.5	4.2	2.0	6.2	2.0	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	2.0	9.5	2.0	12.5	4.0	2.0	5.6	2.0	5.9	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



10

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVER

PRELIMINARY
IDT 54/74FCT543
IDT 54/74FCT543A

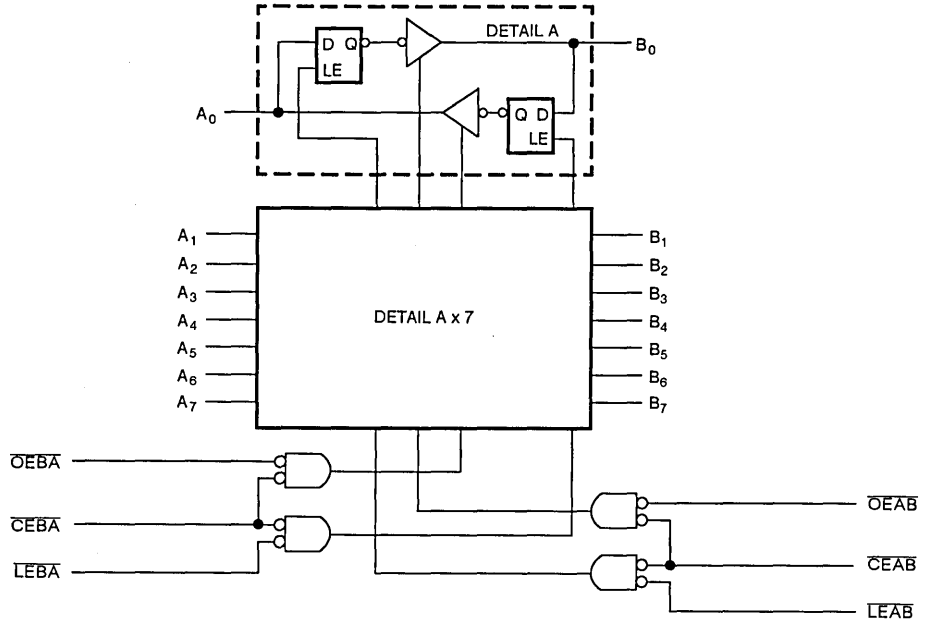
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed; **IDT54/74FCT543A is 25% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT543 and IDT54/74FCT543A are non-inverting octal transceivers built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

FUNCTIONAL BLOCK DIAGRAM



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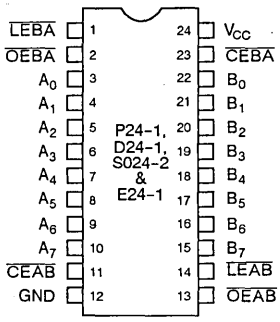
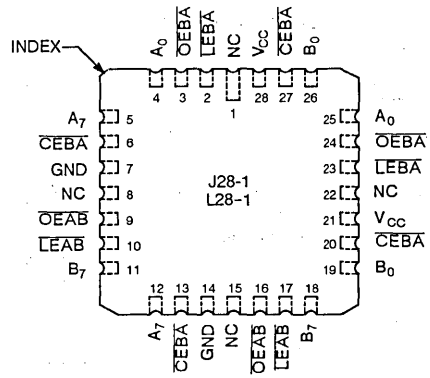
PIN CONFIGURATIONS

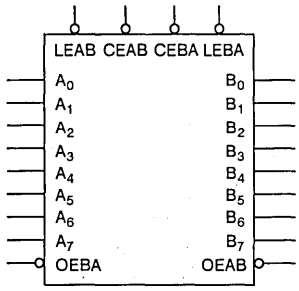


DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



TRUTH TABLE For A-TO-B (Symmetric with B-TO-A)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B_0-B_7
H	X	X	Storing	High Z
X	H	–	Storing	–
X	–	H	–	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

* Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

PIN DESCRIPTIONS

PIN NAMES	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0-A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0-B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Currents (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Currents (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.(5)	–	0.3	0.55	
			I_{OL} = 64mA COM'L.(5)	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{CEAB}$ & $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} f_{CP} = $\overline{LEAB}$ = 10MHz One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} f_{CP} = $\overline{LEAB}$ = 10MHz Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	12.75[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	21.75[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT543					IDT54/74FCT543A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	C_L = 50pF R_L = 500Ω	5.0	2.5	8.5	2.5	10.0	–	2.5	6.5	2.5	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n, $\overline{LEAB}$ to B_n		8.5	2.5	12.5	2.5	14.0	–	2.5	8	2.5	9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		7.0	2.0	12.0	2.0	14.0	–	2	9	2	10	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		5.5	2.0	9.0	2.0	13.0	–	2	7.5	2	8.5	ns
t_{SU}	Set-up Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		–	3.0	–	3.0	–	–	2	–	2	–	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		–	2.0	–	2.0	–	–	2	–	2	–	ns

NOTES:

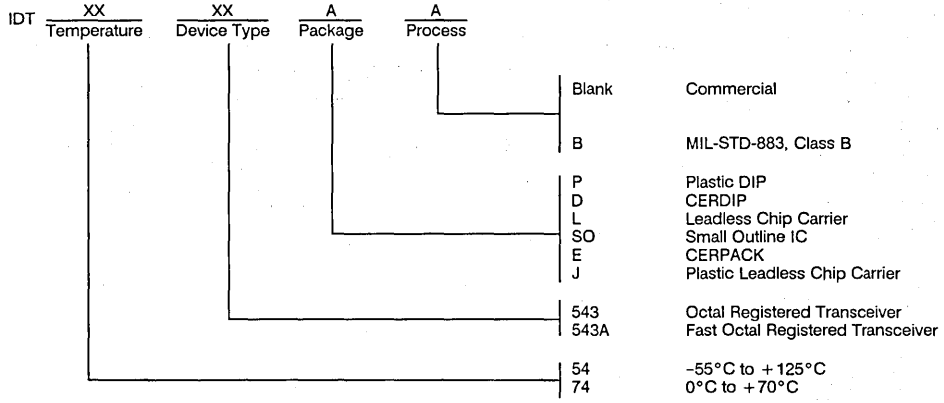
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, it may be necessary to use $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for ATE testing purposes.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT 54/74FCT640
IDT 54/74FCT640A

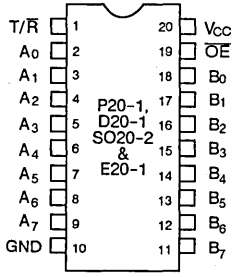
FEATURES:

- IDT54/74FCT640 7.0ns max. data to output;
  IDT54/74FCT640A 5.0ns max. data to output
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA commercial and 48mA military
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Inverting buffer transceiver
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

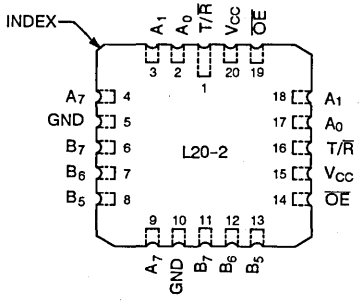
DESCRIPTION:

The IDT54/74FCT640 and IDT54/74FCT640A are 8-bit inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

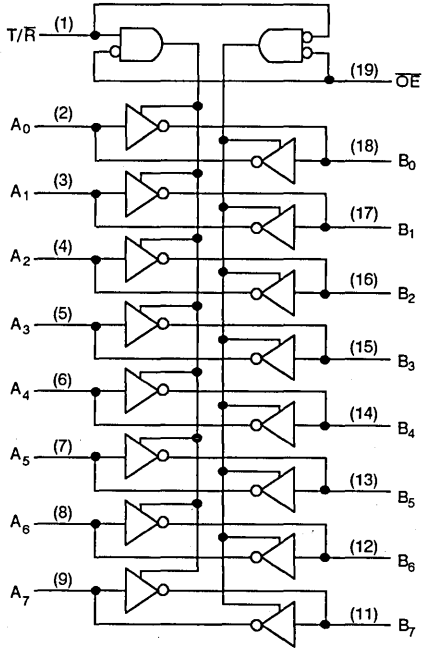


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a registered trademark of Fairchild Semiconductor Co.

DSC-4033/1

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} -0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.4V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.4V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

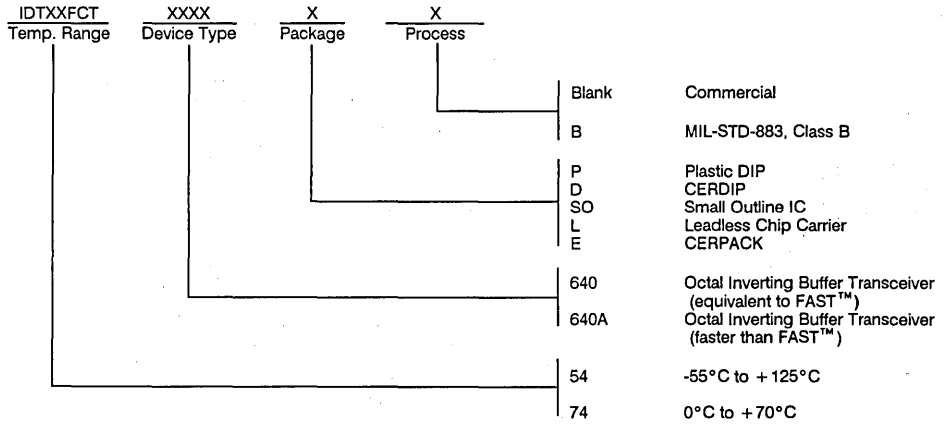
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT640					IDT54/74FCT640A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	2.0	7.0	2.0	8.0	3.5	1.5	5.0	1.5	5.3	ns
t_{PZH} t_{PZL}	Output Enable Time for $\overline{OE}$ and T/$\overline{R}$		11.0	2.0	13.0	2.0	16.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time for $\overline{OE}$ and T/$\overline{R}$		7.0	2.0	10.0	2.0	12.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT 54/74FCT645
IDT 54/74FCT645A

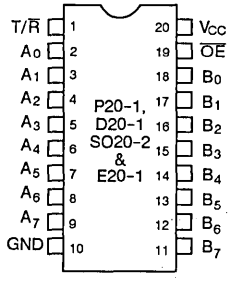
FEATURES:

- IDT54/74FCT645 equivalent to FAST™ speed; **IDT54/74FCT645A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- TTL input and output level compatible
- CMOS output level compatible
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

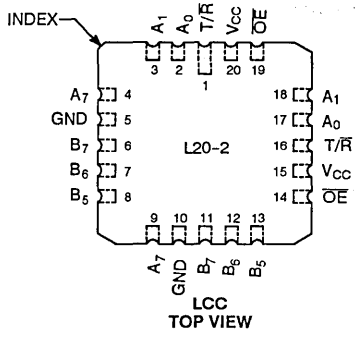
DESCRIPTION:

The IDT54/74FCT645 and IDT54/74FCT645A are 8-bit non-inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS

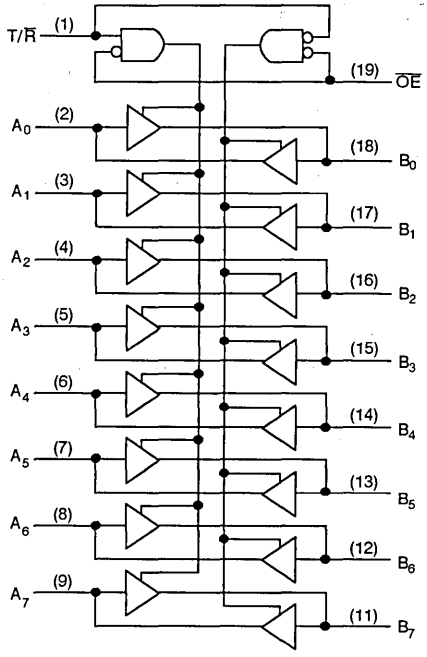


DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_I = 10MHz, 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

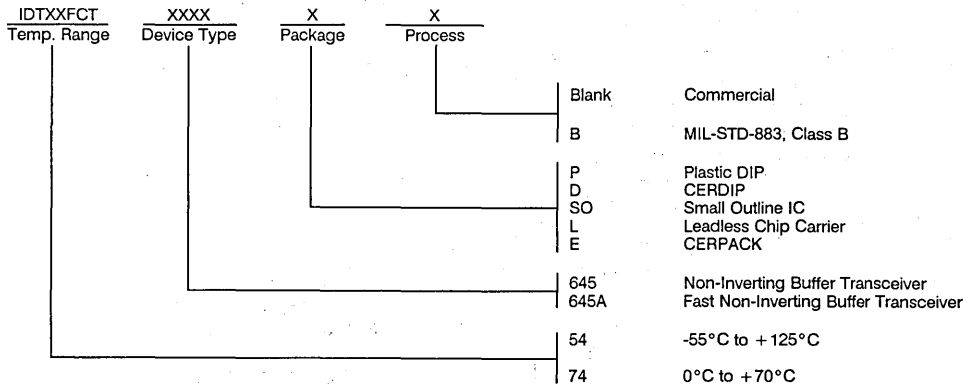
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT645					IDT54/74FCT645A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	1.5	9.5	1.5	11.0	3.3	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		9.0	1.5	11.0	1.5	12.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B		9.0	1.5	11.0	1.5	12.0	4.8	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B[4]		6.0	1.5	12.0	1.5	13.0	4.5	1.5	5.0	1.5	6.0	ns
t_{PHZ} t_{PLZ}	Output Enable Time T/$\overline{R}$ to A or B[4]		6.0	1.5	12.0	1.5	13.0	4.5	1.5	5.0	1.5	6.0	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. This parameter is guaranteed but not tested.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTER

PRELIMINARY
IDT 54/74FCT646/A
IDT 54/74FCT648/A

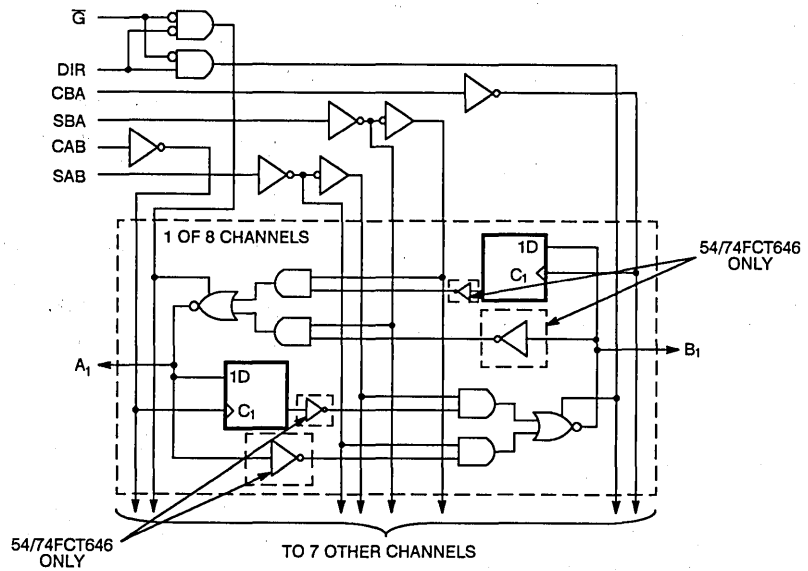
FEATURES:

- IDT54/74FCT646 and IDT54/74FCT648 equivalent to FAST™ speed;
- **IDT54/74FCT646A and IDT54/74FCT648A are 30% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- 3-state outputs
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin, 300 mil CERDIP, plastic DIP, SOIC, CERPACK, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT646/A and IDT54/74FCT648/A consist of a bus transceiver circuit with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (Enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

FUNCTIONAL BLOCK DIAGRAM



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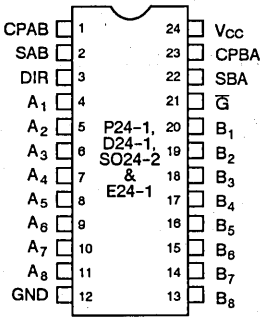
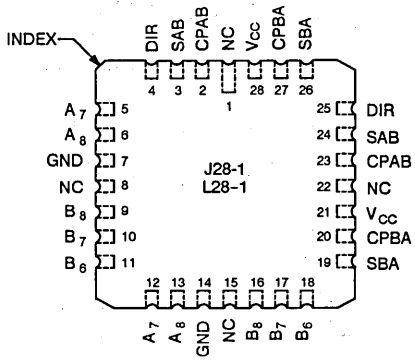
PIN CONFIGURATIONS

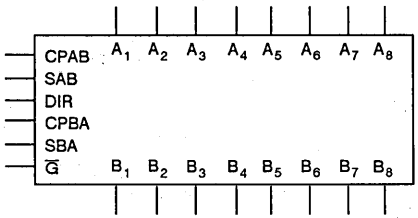


DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
$A_1 - A_8$	Data Register A Inputs Data Register B Outputs
$B_1 - B_8$	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

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FUNCTION TABLE

INPUTS						DATA I/O[1]		OPERATION or FUNCTION	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	$A_1 - A_8$	$B_1 - B_8$	FCT646/A	FCT648/A
H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH
   L = LOW
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.,	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.,	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output High Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.0	–	
			I_{OH} = -15mA COM'L.	2.4	4.0	–	
V_{OL}	Output Low Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These parameters are guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{G}$ = GND DIR = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = GND DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = GND DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	6.75	12.75[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	9.75	21.75[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS[1]	IDT54/74FCT646					IDT54/74FCT646A[4]					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	8.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus & DIR to A or B		9.0	2.0	14.0	2.0	15.0	–	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus & Direction to Bus		9.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		8.0	2.0	9.0	2.0	10.0	–	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	1.5	–	1.5	–	ns
t_{PW}	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	5.0	–	5.0	–	ns

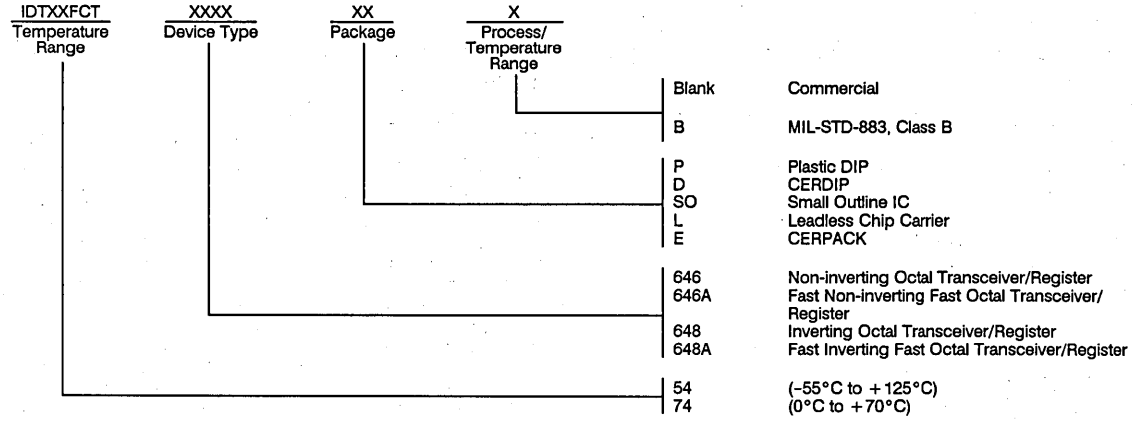
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These are preliminary numbers only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS[1]	IDT54/74FCT648[4]					IDT54/74FCT648A[4]					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	7.0	2.0	8.0	2.0	9.0	–	2.0	5.6	2.0	6.3	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus & DIR to A or B		9.0	2.0	15.0	2.0	18.0	–	2.0	10.5	2.0	12.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus & Direction to Bus		9.0	2.0	9.0	2.0	11.0	–	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		7.0	2.0	9.0	2.0	10.0	–	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	2.0	–	2.0	–	ns
t_H	Hold time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	1.5	–	1.5	–	ns
t_{PW}	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	5.0	–	5.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. These are preliminary numbers only.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTER

PRELIMINARY
IDT 54/74FCT651/A
IDT 54/74FCT652/A

FEATURES:

- IDT54/74FCT651 and IDT54/74FCT652 are equivalent to FAST™ speeds
- **IDT54/74FCT651A and IDT54/74FCT652A 30% faster than FAST™ speeds**
- Bidirectional bus transceiver and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- Choice of true and inverting data transfer
- 3-state outputs
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin 300 mil DIP, SOIC, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

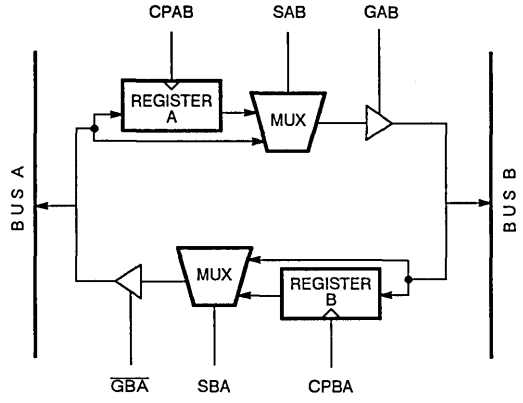
DESCRIPTION:

The IDT54/74FCT651/A and IDT54/74FCT652/A, built in CEMOS™, consist of bus transceiver circuits, D-type flip-flops and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

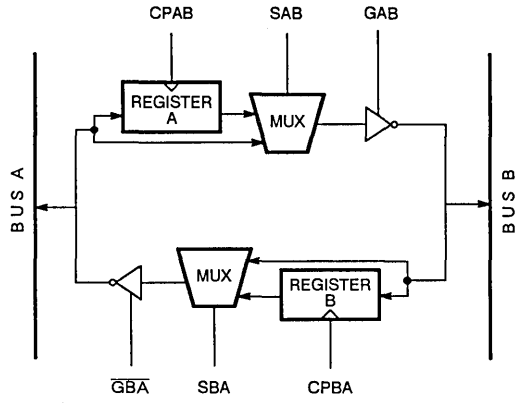
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT652/A (Non-inverting)



IDT54/74FCT651/A (Inverting)



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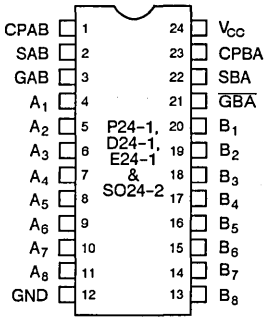
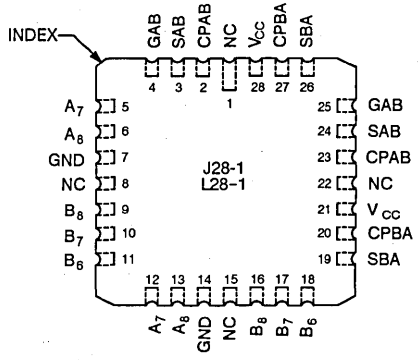
FAST is a trademark of Fairchild Semiconductor Co.

PIN CONFIGURATIONS

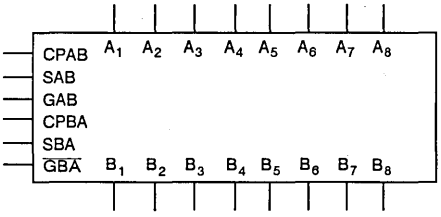


DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
A_1-A_8	Data Register Inputs Data Register A Outputs
B_1-B_8	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
GAB, $\overline{GBA}$	Output Enable Inputs

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 THRU A_8	B_1 THRU B_8	FCT651/A	FCT652/A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.

H = HIGH, L = LOW, X = Don't Care, ↑ LOW-to-HIGH Transition

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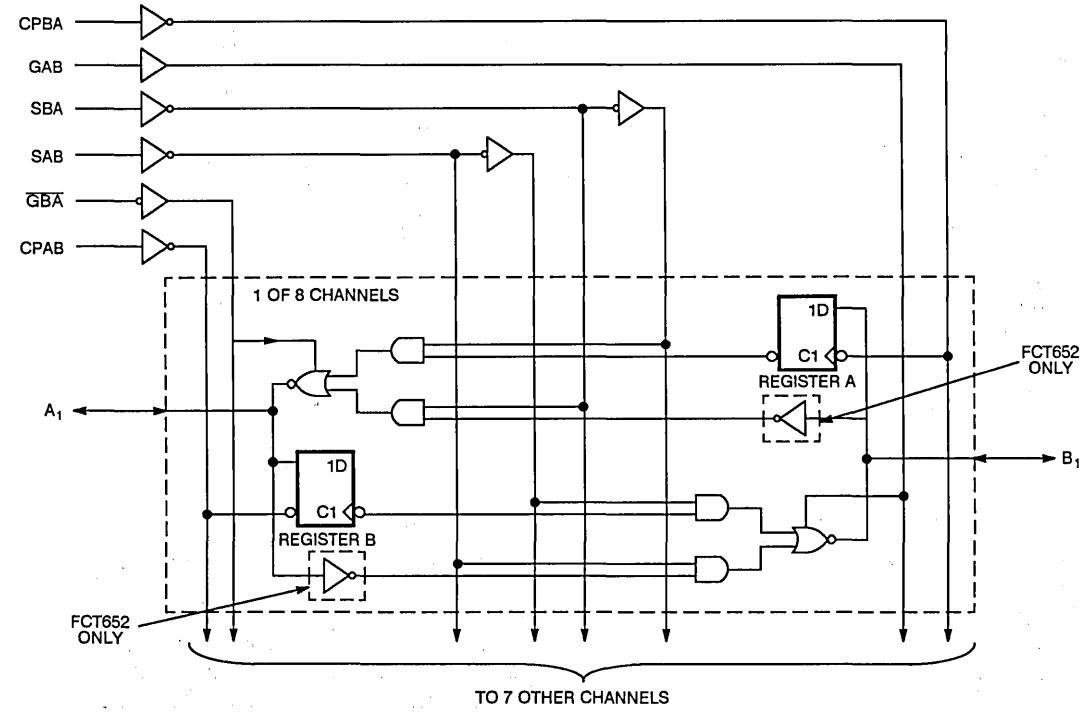
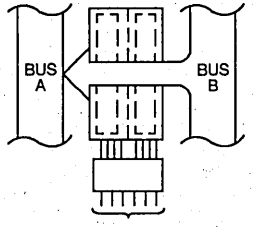
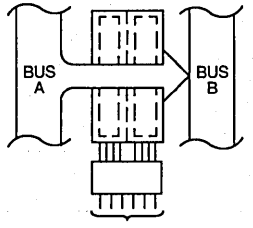
DETAILED BLOCK DIAGRAM





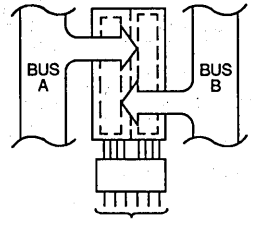
GAB	GBA	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



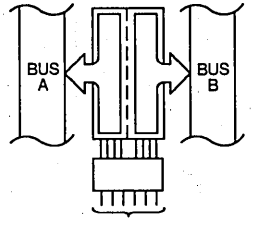
GAB	GBA	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	GBA	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	GBA	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	μA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	μA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 μA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300μA	V_{HC}	V_{CC}	–	
			I_{OH} = −12mA MIL.	2.4	4.3	–	
			I_{OH} = −15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

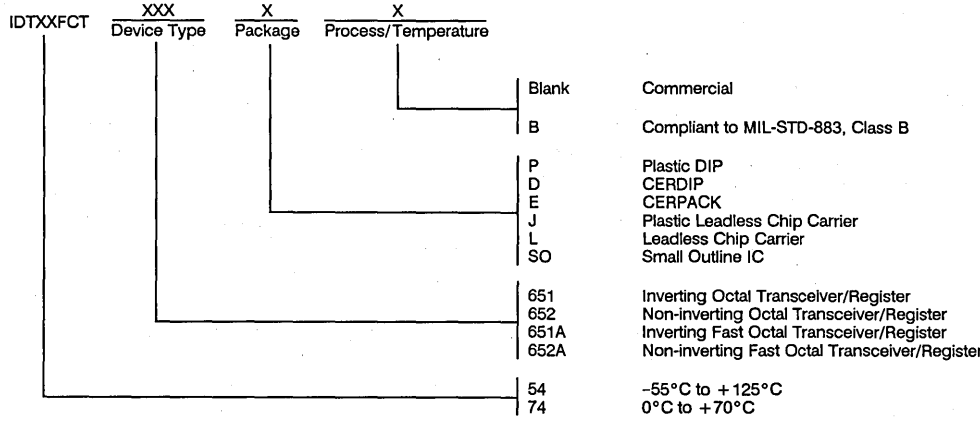
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT651/652					IDT54/74FCT651A/652A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	8.0	2.0	9.0	2.0	10.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		8.0	2.0	9.0	2.0	11.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	–	–	–	–	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	–	–	–	–	ns
t_W	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	–	–	–	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT 54/74FCT821A/B-
IDT 54/74FCT826A/B*

FEATURES:

- Equivalent to AMD's Am29821-26 bipolar registers in pinout/ function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Non-inverting CP-Y t_{PD} = 7.5ns typ.
  - Inverting CP-Y t_{PD} = 7.5ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

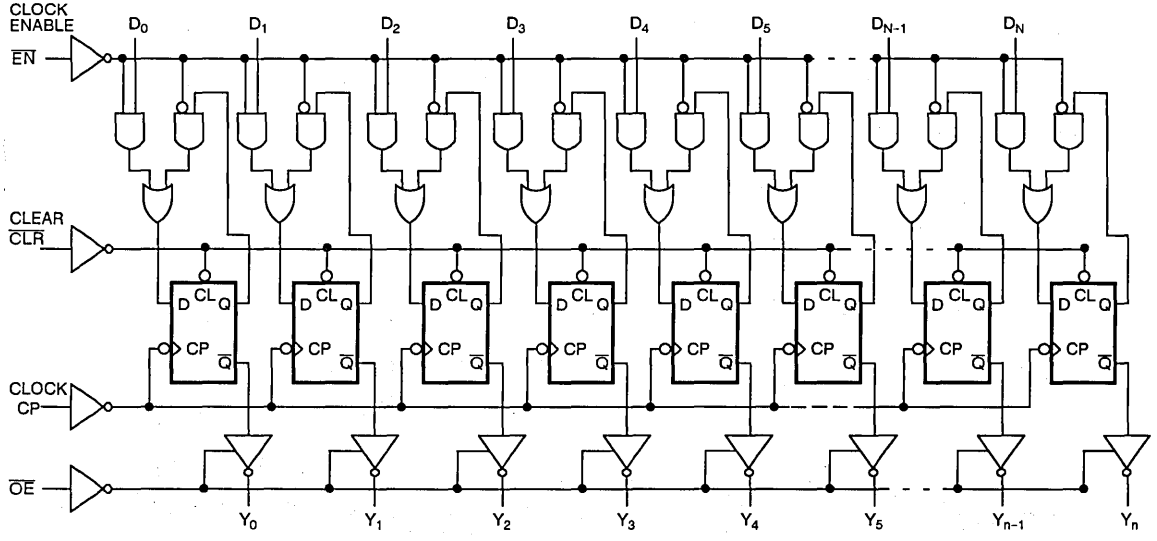
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/ data paths or buses carrying parity. The IDT54/74FCT821 and IDT54/74FCT822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 and IDT54/74FCT826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

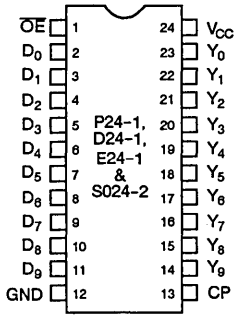
	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT821A/B	54/74FCT823A/B	54/74FCT825A/B
Inverting	54/74FCT822A/B	54/74FCT824A/B	54/74FCT826A/B

CEMOS is a trademark of Integrated Device Technology, Inc.

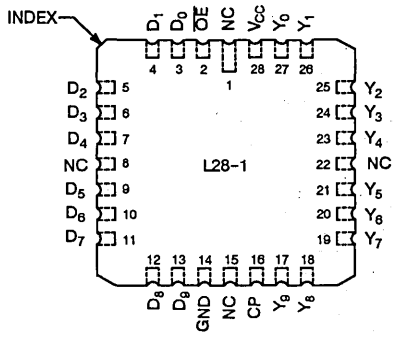
*Advance information only for IDT54/74FCT822 and IDT54/74FCT826.

PIN CONFIGURATIONS

IDT54/74FCT821/IDT54/74FCT822 10-BIT REGISTERS

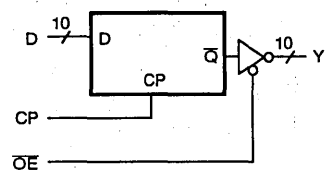


DIP/CERPACK/SOIC
TOP VIEW

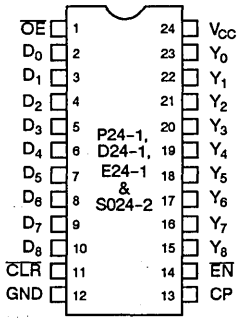


LCC
TOP VIEW

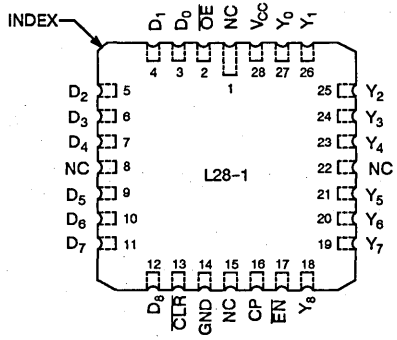
LOGIC SYMBOLS



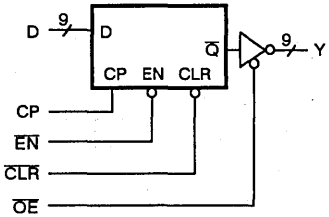
IDT54/74FCT823/IDT54/74FCT824 9-BIT REGISTERS



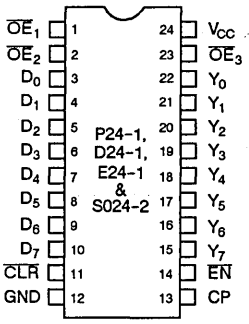
DIP/CERPACK/SOIC
TOP VIEW



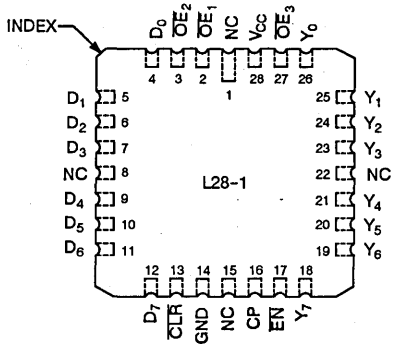
LCC
TOP VIEW



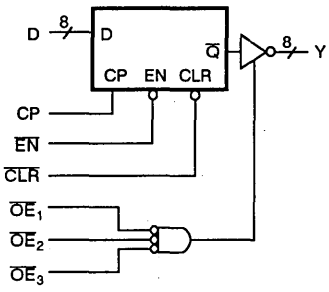
IDT54/74FCT825/IDT54/74FCT826 8-BIT REGISTERS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



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PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both Inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I , $\overline{Y_I}$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

FUNCTION TABLES [1]
IDT54/74FCT821/23/25

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT822/24/26

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	
H	X	L	L	↑	H	Z	High Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

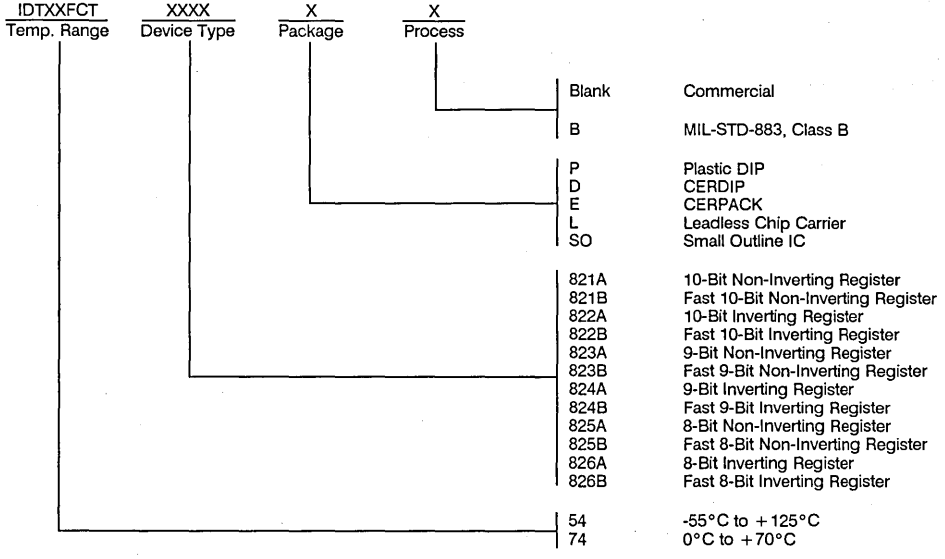
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION		TEST CONDITIONS[1]	IDT54/74FCT821A-26A				IDT54/74FCT821B-26B				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF R_L = 500Ω	–	10	–	11.5	–	7.5	–	8.5	ns
t_{PLH} t_{PHL}			C_L = 300pF[3] R_L = 500Ω	–	20	–	20	–	15	–	16	ns
t_{SU}	Data to CP Set-up Time		C_L = 50pF R_L = 500Ω	4	–	4	–	3	–	3	–	ns
t_H	Data CP Hold Time			2	–	2	–	1.5	–	1.5	–	ns
t_{SU}	Enable ($\overline{EN}$ ↓) to CP Set-up Time			4	–	4	–	3.0	–	3.0	–	ns
t_{SU}	Enable ($\overline{EN}$ ↓) to CP Set-up Time			4	–	4	–	3.0	–	3.0	–	ns
t_H	Enable ($\overline{EN}$) Hold Time			2	–	2	–	0	–	0	–	ns
t_{PHL}	Propagation Delay, Clear to Y_i			–	14	–	15	–	9.0	–	9.5	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ↓) Time			6	–	7	–	6.0	–	6.0	–	ns
t_{PWH}	Clock Pulse Width	HIGH		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}		LOW		7	–	7	–	6.0	–	6.0	–	ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			6	–	7	–	6.0	–	6.0	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 50pF R_L = 500Ω	–	12	–	13	–	8	–	9	ns
t_{PZH} t_{PZL}			C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	15	–	16	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6.5	–	7	ns
t_{PHZ} t_{PLZ}			C_L = 50pF R_L = 500Ω	–	8	–	9	–	7.5	–	8	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT 54/74FCT827A/B
IDT 54/74FCT828A/B*

FEATURES:

- **Faster than AMD's Am29827-28 series**
- Equivalent to AMD's Am29827-28 bipolar buffers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed buffers
  - Non-inverting t_{PD} = 3.5ns typ.
  - Inverting t_{PD} = 4.0ns typ.
- I_{OL} = 48mA (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

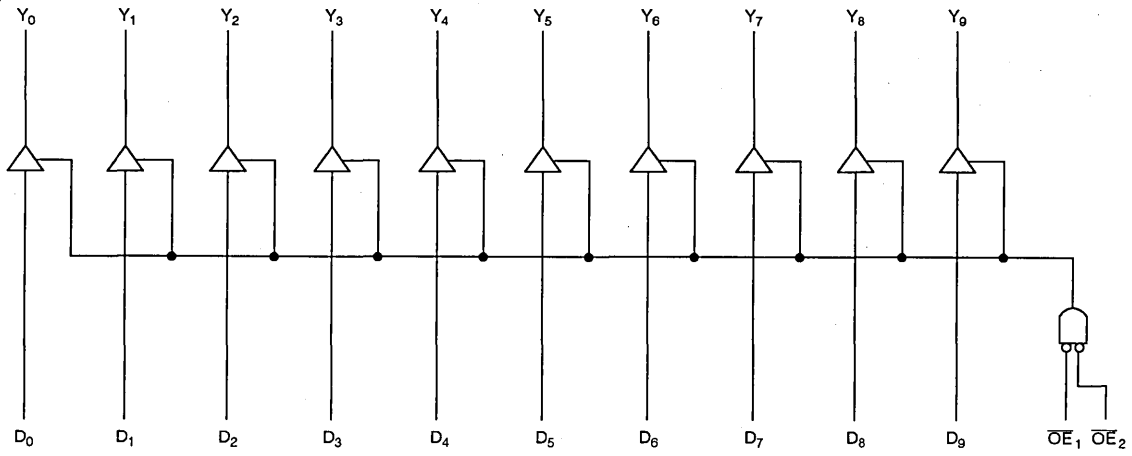
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827A/B and IDT54/74FCT828A/B 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT827A/B–IDT5474FCT828A/B 10-BIT BUFFERS



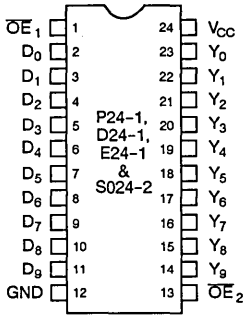
PRODUCT SELECTOR GUIDE

	10-BIT BUFFER
Non-inverting	IDT54/74FCT827A/B
Inverting	IDT54/74FCT828A/B

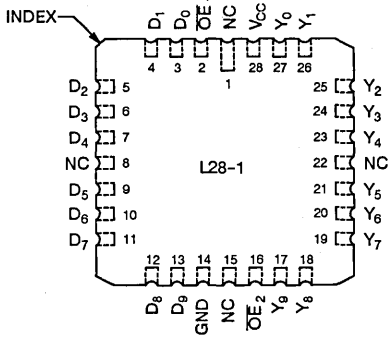
CEMOS is a trademark of Integrated Device Technology, Inc.

*Advance information only for IDT54/74FCT828.

PIN CONFIGURATIONS
IDT54/74FCT827A/B/IDT54/74FCT828A/B

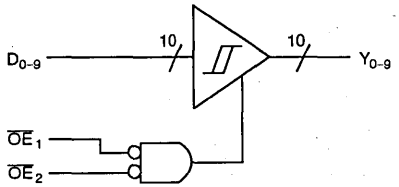


DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

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FUNCTIONAL TABLES
IDT54/74FCT827A/B (NON-INVERTING)(1)

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

IDT54/74FCT828A/B (INVERTING)(1)

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.0	–	
			I_{OH} = -24mA COM'L.	2.4	4.0	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_I = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_I = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_I = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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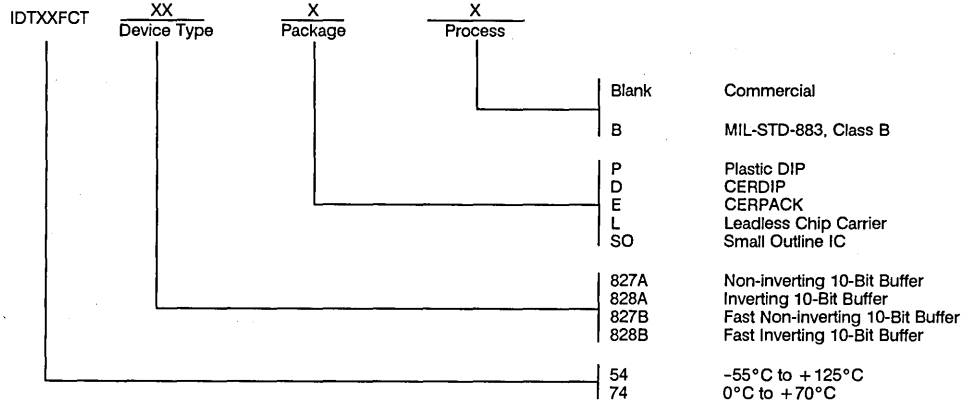
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT827A/28A				IDT54/74FCT827B/28B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from D_I to Y_I IDT54/74FCT827A/B (Non-inverting)	C_L = 50pF R_L = 500Ω	–	8	–	9	–	5.0	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	15	–	17	–	13.0	–	14.0	ns
t_{PLH} t_{PHL}	Propagation Delay from D_I to Y_I IDT54/74FCT828A/B (Inverting)	C_L = 50pF R_L = 500Ω	–	9	–	10	–	5.5	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	14	–	16	–	13.0	–	14.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_I	C_L = 50pF R_L = 500Ω	–	12	–	13	–	8.0	–	9.0	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	15.0	–	16.0	ns
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_I	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6.0	–	7.0	ns
t_{PHZ} t_{PHL}		C_L = 50pF R_L = 500Ω	–	10	–	10	–	7.0	–	8.0	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS PARITY BUS TRANSCEIVER

IDT 54/74FCT833A/B
IDT 54/74FCT834A/B*
IDT 54/74FCT853A/B
IDT 54/74FCT854A/B*

FEATURES:

- Equivalent to AMD's Am29833-34 and Am29853-54 bipolar parity bus transceivers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High speed bidirectional bus transceiver for processor-organized devices
  - Non-inverting propagation delay = 7.0ns max.
  - Inverting propagation delay = 7.0ns max.
- Buffered direction three state control
- Error Flag with open-drain output
- I_{OL} = 48mA (commercial) and 32mA (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Available in Plastic DIP, CERDIP, LCC, PLCC and SOIC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

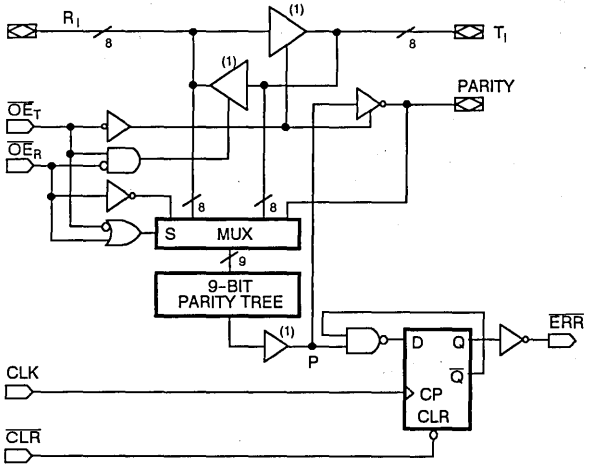
DESCRIPTION:

The IDT54/74FCT833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available: the IDT54/74FCT833/34 register option and the IDT54/74FCT853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

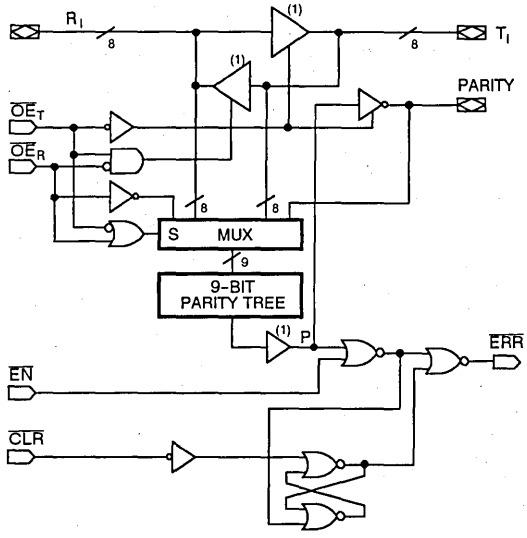
The output enables $\overline{OE_T}$ and $\overline{OE_R}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{OE_R}$ and $\overline{OE_T}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The IDT54/74FCT833 and IDT54/74FCT853 are non-inverting, while the IDT54/74FCT834 and IDT54/74FCT854 present inverting data at the outputs. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT833
(Device Shown Non-inverting)



IDT54/74FCT853
(Device Shown Non-inverting)



NOTE:

1. Non-inverting buffer for IDT54/74FCT833/53, inverting buffer for IDT54/74FCT834/54, note that the inverting device converts the positive logic "R" bus levels to negative levels on "T" bus.

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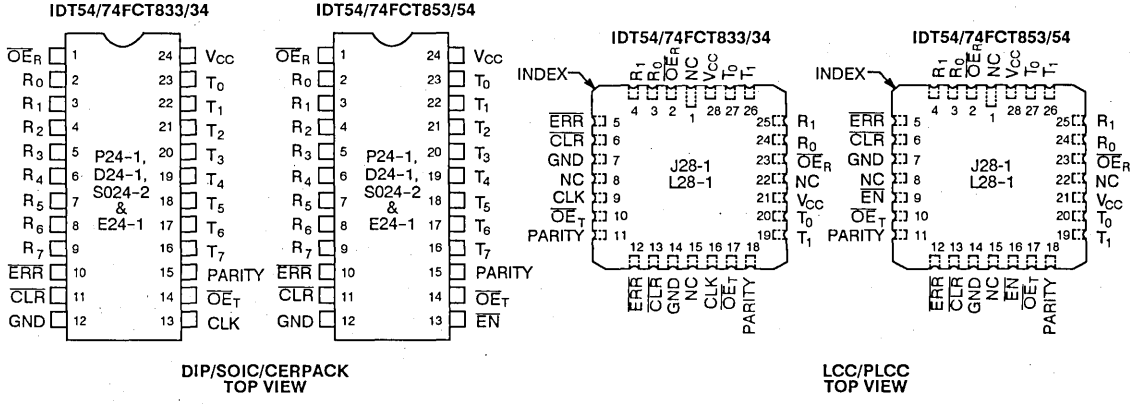
*Advance information only for IDT54/74FCT834 and IDT54/74FCT854.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
IDT54/74FCT833/34			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
IDT54/74FCT853/54			
1	$\overline{OE}_R$	I	RECEIVE enable input.
2-9	R_I	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault latch output.
16-23	T_I	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Enable latch input for fault flag.

ERROR FLAG OUTPUT TRUTH TABLE

IDT54/74FCT833/IDT54/74FCT834 (REGISTER OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
CLR	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	Sample (1's Capture)
H	↑	–	L	L	
H	↑	L	–	L	
L	–	–	–	H	Clear

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

IDT54/74FCT853/IDT54/74FCT854 (LATCH OPTION)

INPUTS		INTERNAL TO DEVICE	OUTPUTS PRE-STATE	OUTPUT	FUNCTION
$\overline{EN}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample (1's Capture)
L	H	–	L	L	
L	H	H	H	H	
H	L	–	–	H	Clear
H	H	–	L	L	Store
H	H	–	H	H	

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.

FUNCTION TABLES

IDT54/74FCT833 NON-INVERTING REGISTER OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	H	
H	H	H	↑	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT834 INVERTING REGISTER OPTION(2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ OF L'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	L	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	L	NA	NA	H	
H	L	H	↑	NA	L (Odd)	H	NA	NA	L	
H	L	H	↑	NA	L (Even)	H	NA	NA	H	
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	↑	L (Odd)	–	Z	Z	Z	L	
H	H	H	↑	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
*Store the Error State of the Last Receive Cycle

Z = High Impedance
NA = Not Applicable
– = Don't Care or Irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:

1. Output state assumes HIGH output pre-state.
2. Note that for the negative levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

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FUNCTION TABLES (CONTINUED)

IDT54/74FCT853 NON-INVERTING LATCH OPTION

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

IDT54/74FCT854 INVERTING LATCH OPTION (2)

INPUTS						OUTPUTS				FUNCTION
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	$\overline{EN}$	R_i (Σ OF H'S)	T_i INCL PARITY (Σ OF H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	*	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	H (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance
NC = No Change

NA = Not Applicable
*Store the Error State of the Last Receive Cycle
– = Don't Care or Irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

NOTES:

1. Output state assumes HIGH output pre-state.
2. Note that for negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1".

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Ouput and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min.	All other outputs V_{IN} = V_{IH} or V_{IL} I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
			$\overline{ERR}$ I_{OL} = 48mA	–	0.3	0.5	
V_H	Input Hysteresis on T_I and R_I	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \leq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_T$ = $\overline{OE}_R$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND $\overline{OE}_R$ = V_{CC} f_i = 2.5MHz One Input Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	1.2	3.4	mA
			V_{IN} = 3.4V V_{IN} = GND	–	1.6	5.4	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLK or $\overline{EN}$) 50% Duty Cycle $\overline{OE}_T$ = GND f_i = 2.5MHz $\overline{OE}_R$ = V_{CC} Eight Inputs Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (FCT)	–	3.8	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER TEMPERATURE RANGE

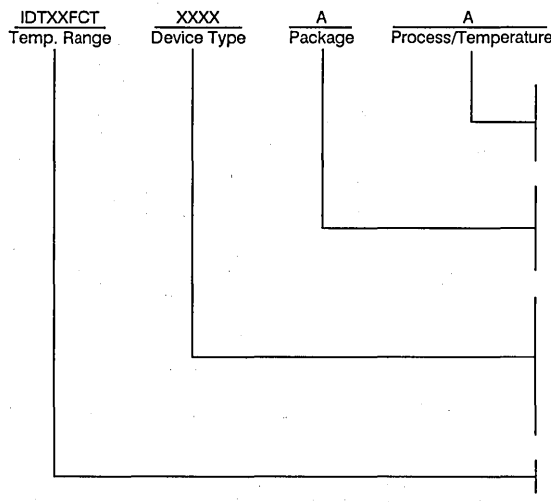
PARAMETERS	DESCRIPTION		TEST CONDITIONS[4]	IDT54/74FCT8XXA[3]				IDT54/74FCT8XXB[3]				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH}	Propagation Delay R_I to $\overline{T}_i$, T_i to R_I		C_L = 50pF	–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PHL}				–	10.0	–	14.0	–	7.0	–	10.0	ns
t_{PLH}			C_L = 300pF[6]	–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PHL}				–	17.5	–	21.5	–	14.5	–	17.5	ns
t_{PLH}	Propagation Delay R_I to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF[6]	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PZH}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_I, $\overline{T}_i$		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZL}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PZH}			C_L = 300pF[6]	–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PZL}				–	19.5	–	23.5	–	16.0	–	18.5	ns
t_{PHZ}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_I, $\overline{T}_i$		C_L = 5pF[6]	–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PLZ}				–	10.7	–	14.7	–	7.2	–	9.8	ns
t_{PHZ}			C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLZ}				–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{SU}	$\overline{T}_i$, PARITY to CLK Set-up Time[1]		C_L = 50pF	12.0	–	16.0	–	8.5	–	11.0	–	ns
t_H	$\overline{T}_i$, PARITY to CLK Hold Time[1]			0	–	0	–	0	–	0	–	ns
t_{SU}	Clear Recovery Time $\overline{CLR}$ to CLK[2]			15.0	–	20.0	–	10.5	–	14.0	–	ns
t_W	Clock Pulse Width[1]	HIGH		7.0	–	9.5	–	5.5	–	7.0	–	ns
		LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_W	Clear Pulse Width	LOW		7.0	–	9.5	–	5.5	–	7.0	–	ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$[1]		C_L = 50pF	–	12.0	–	16.0	–	8.5	–	11.0	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		C_L = 50pF	–	16.0	–	20.0	–	15.0	–	18.0	ns
t_{PLH}	Propagation-Delay T_i, PARITY TO $\overline{ERR}$ (PASS Mode Only) IDT54/74FCT853 and IDT54/74FCT854		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}	Propagation Delay $\overline{OE}_R$ to PARITY		C_L = 50pF	–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PHL}				–	15.0	–	20.0	–	10.5	–	14.0	ns
t_{PLH}			C_L = 300pF[6]	–	22.5	–	27.5	–	18.0	–	21.5	ns
t_{PHL}				–	22.5	–	27.5	–	18.0	–	21.5	ns

NOTES:

1. For IDT54/74FCT853/54, replace CLK with $\overline{EN}$.
2. Not applicable to IDT54/74FCT853/54.
3. XX represents 33, 34, 53 and 54.
4. See test circuit and waveforms.
5. Minimum limits are guaranteed but not tested on Propagation Delays.
6. These parameters are guaranteed but not tested.

10

ORDERING INFORMATION



Blank	Commercial (0°C to +70°C)
B	Military (−55°C to +125°C) Compliant to MIL-STD-883, Class B
P	Plastic DIP
D	Cerdip
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK
833A	Non-inverting Parity Bus Transceiver (Register Option)
833B	Fast non-inverting Parity Bus Transceiver (Register Option)
834A	Inverting Parity Bus Transceiver (Register Option)
834B	Fast inverting Parity Bus Transceiver (Register Option)
853A	Non-inverting Parity Bus Transceiver (Latch Option)
853B	Fast non-inverting Parity Bus Transceiver (Latch Option)
854A	Inverting Parity Bus Transceiver (Latch Option)
854B	Fast inverting Parity Bus Transceiver (Latch Option)
54	−55°C to +125°C
74	0°C to +70°C

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT 54/74FCT841A/B-
IDT 54/74FCT846A/B*
(Replaces 39C841-46)

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  - Non-inverting transparent t_{PD} = 5.5ns typ.
  - Inverting transparent t_{PD} = 6.0ns typ.
- Buffered common latch enable, clear and preset input
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

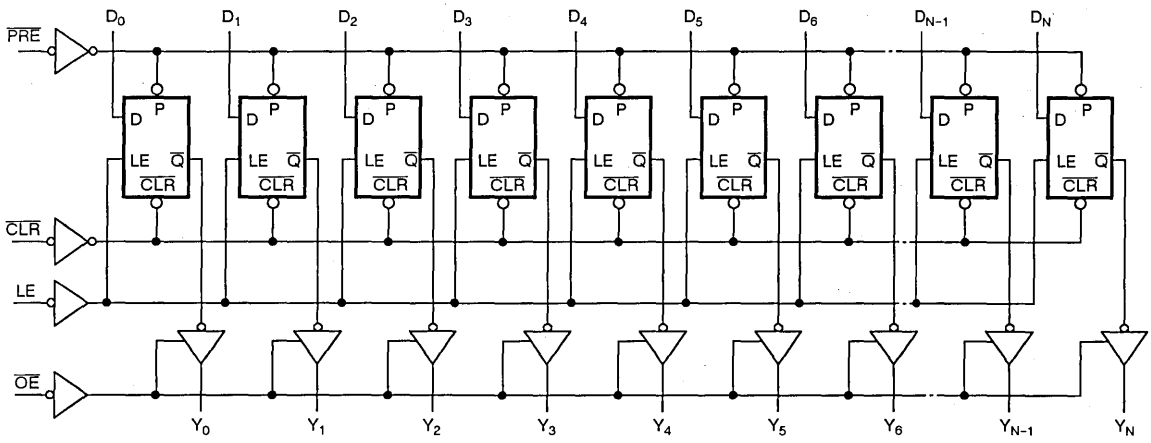
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 and IDT54/74FCT842 are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 and IDT54/74FCT846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

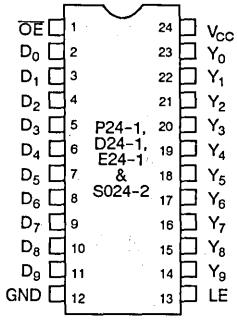
	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT841A/B	54/74FCT843A/B	54/74FCT845A/B
Inverting	54/74FCT842A/B	54/74FCT844A/B	54/74FCT846A/B

CEMOS is a trademark of Integrated Device Technology, Inc.

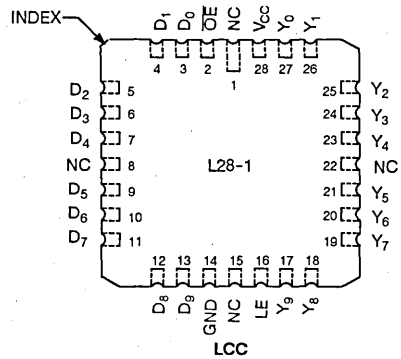
*Advance information only for IDT54/74FCT842 and IDT54/74FCT846.

PIN CONFIGURATIONS

IDT54/74FCT841/IDT54/74FCT842 10-BIT LATCHES

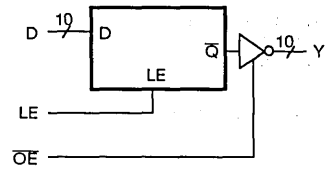


DIP/CERPACK/SOIC
TOP VIEW

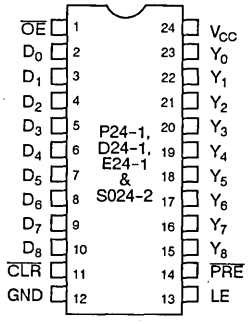


LCC
TOP VIEW

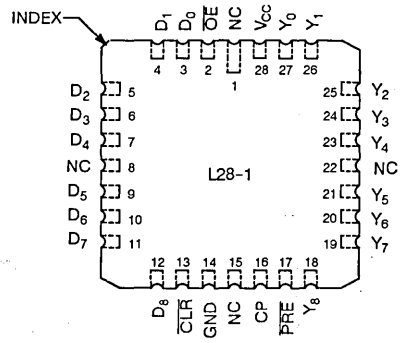
LOGIC SYMBOLS



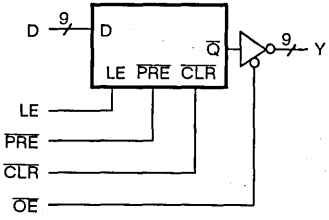
IDT54/74FCT843/IDT54/74FCT844 9-BIT LATCHES



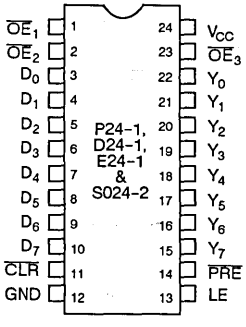
DIP/CERPACK/SOIC
TOP VIEW



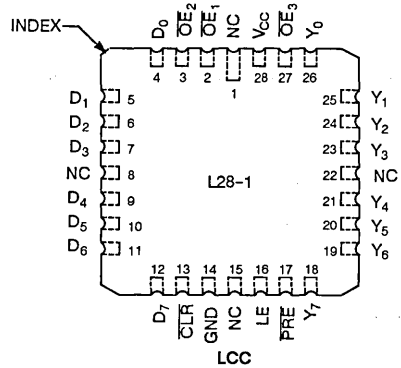
LCC
TOP VIEW



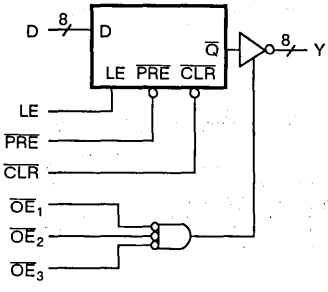
IDT54/74FCT845/IDT54/74FCT846 8-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT841/43/45 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT54/74FCT842/44/46 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES [1]
IDT54/74FCT841/43/45

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLES [1]
IDT54/74FCT842/44/46

INPUTS					INTERNAL	OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

10

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions apply unless otherwise specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	Vcc = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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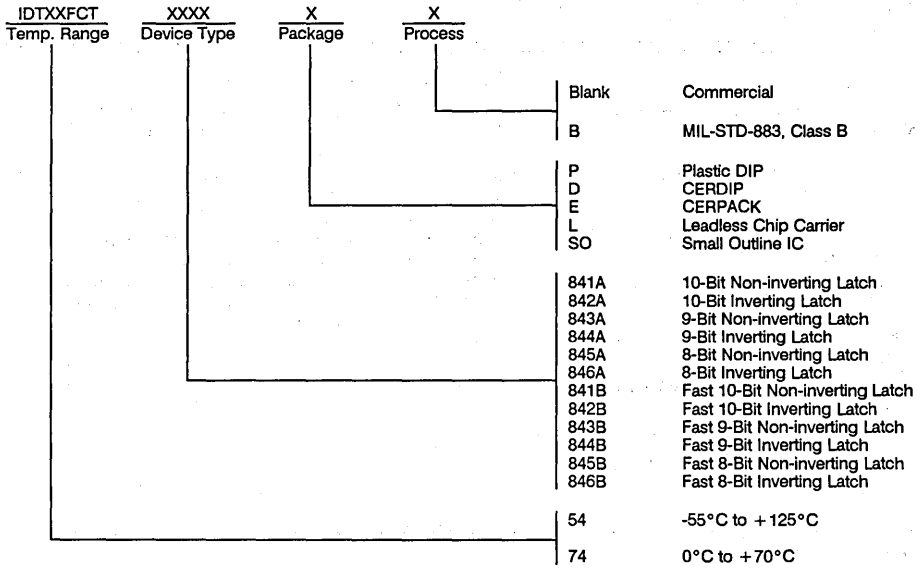
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION		TEST CONDITIONS[1]	IDT54/74FCT841A-46A				IDT54/74FCT841B-46B				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT54/74FCT841, 43, 45) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)		C_L = 50pF R_L = 500Ω	–	9	–	10	–	6.5	–	7.5	ns
t_{PLH} t_{PHL}			C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time		C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time			2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} (IDT54/74FCT842, 44, 46) t_{PHL}	Data (D_I) to Output (Y_I) (LE = HIGH)		C_L = 50pF R_L = 500Ω	–	10	–	12	–	8.0	–	9.0	ns
t_{PLH} t_{PHL}			C_L = 300pF[3] R_L = 500Ω	–	13	–	15	–	13	–	15	ns
t_{SU}	Data to LE Set-up Time		C_L = 50pF R_L = 500Ω	2.5	–	2.5	–	2.5	–	2.5	–	ns
t_H	Data to LE Hold Time			2.5	–	3	–	2.5	–	2.5	–	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_I		C_L = 50pF R_L = 500Ω	–	12	–	13	–	8.0	–	10.5	ns
t_{PLH} t_{PHL}			C_L = 300pF[3] R_L = 500Ω	–	16	–	20	–	15.5	–	18	ns
t_{PLH}	Propagation Delay, Preset to Y_I		C_L = 50pF R_L = 500Ω	–	12	–	14	–	8.0	–	10	ns
t_{SU}	Preset Recovery ($\overline{PRE}$ ↓) Time			–	14	–	17	–	10	–	13	ns
t_{PHL}	Propagation Delay, Clear to Y_I			–	13	–	14	–	10	–	11	ns
t_{SU}	Clear Recovery ($\overline{CLR}$ ↓) Time			–	14	–	17	–	10	–	10	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF R_L = 500Ω	4	–	5	–	4	–	4	–	ns
t_{PWL}	Preset Pulse Width	LOW		5	–	7	–	4	–	4	–	ns
t_{PWL}	Clear Pulse Width	LOW		4	–	5	–	4	–	4	–	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ↓ to Y_I		C_L = 50pF R_L = 500Ω	–	11.5	–	13.0	–	8	–	8.5	ns
t_{PZH} t_{PZL}			C_L = 300pF[3] R_L = 500Ω	–	23	–	25	–	14	–	15	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ↑ to Y_I		C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6	–	6.5	ns
t_{PHZ} t_{PLZ}			C_L = 50pF R_L = 500Ω	–	8	–	10	–	7.0	–	7.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT 54/74FCT861A/B-
IDT 54/74FCT864A/B*
(Replaces 39C861-64)

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed symmetrical bidirectional transceivers
  - Non-inverting t_{PD} = 5.5ns typ.
  - Inverting t_{PD} = 6.0ns typ.
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5μA max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

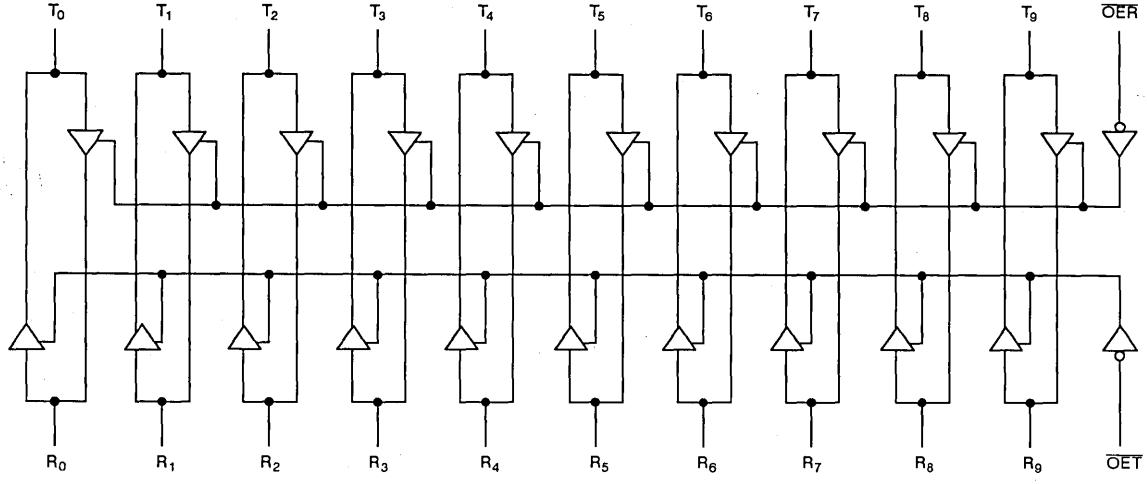
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 Series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863/64 9-bit transceivers have NOR-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT861/IDT54/74FCT862 10-BIT TRANSCEIVERS



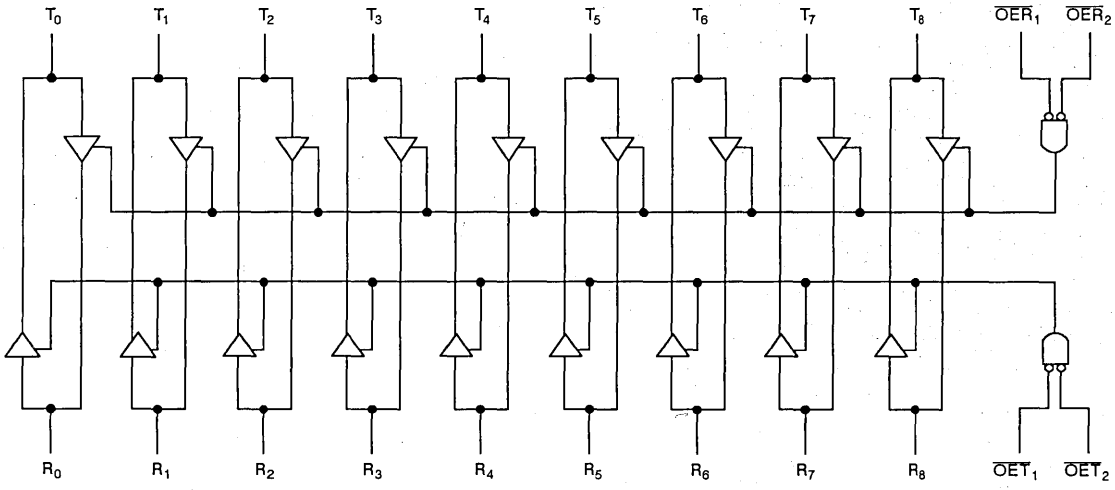
PRODUCT SELECTOR GUIDE

	DEVICE	
	10-BIT	**9-BIT**
Non-inverting	IDT54/74FCT861	IDT54/74FCT863
Inverting	IDT54/74FCT862	IDT54/74FCT864

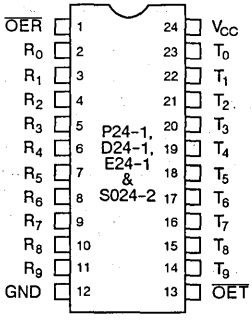
CEMOS is a trademark of Integrated Device Technology, Inc.

*Advance information only for IDT54/74FCT862.

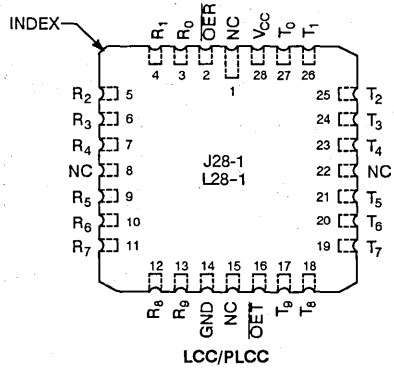
FUNCTIONAL BLOCK DIAGRAM
IDT54/74FCT863/IDT54/74FCT864 9-BIT TRANSCEIVERS



PIN CONFIGURATIONS
IDT54/74FCT861/IDT54/74FCT862 10-BIT TRANSCEIVERS

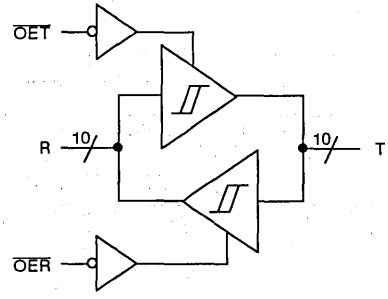


DIP/CERPACK/SOIC
TOP VIEW

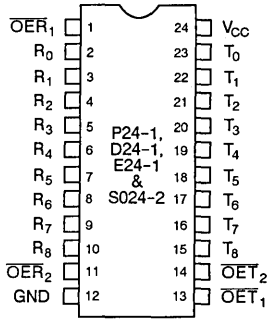


LCC/PLCC
TOP VIEW

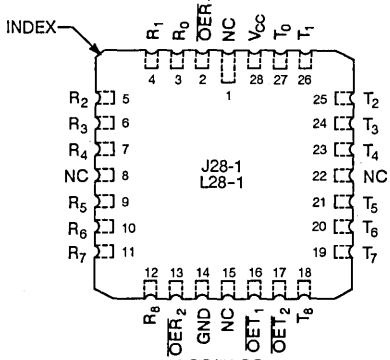
LOGIC SYMBOLS
IDT54/74FCT861



IDT54/74FCT863/IDT54/74FCT864 9-BIT TRANSCEIVERS

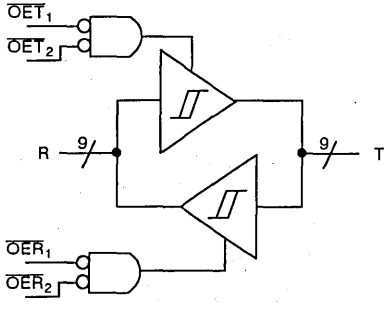


DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

IDT54/74FCT863



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PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT861/62		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$, HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$, HIGH activates the TRANSMIT mode.
R_I	I/O	10-bit RECEIVE input/output.
T_I	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/64		
$\overline{OER}_I$	I	When LOW in conjunction with $\overline{OET}_I$, HIGH activates the RECEIVE mode.
$\overline{OET}_I$	I	When LOW in conjunction with $\overline{OER}_I$, HIGH activates the TRANSMIT mode.
R_I	I/O	9-bit RECEIVE input/output.
T_I	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES[1]
IDT54/74FCT861/63 (Non-inverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable

FUNCTION TABLES[1]
IDT54/74FCT862/64 (Inverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.,	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.,	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-75	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -15mA MIL.	2.4	4.3	–	
			I_{OH} = -24mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on T_I and R_I Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND $T/\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	1.8	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.0	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	–	5.0	14.5[5]	

NOTES:

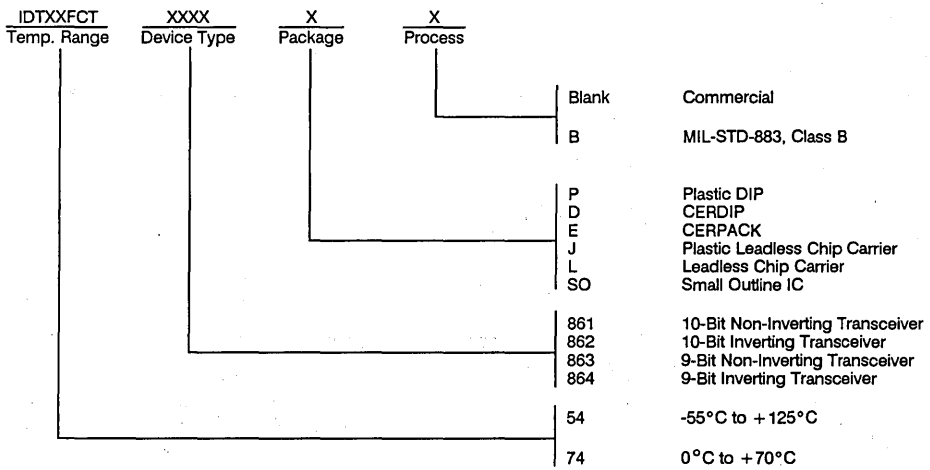
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST CONDITIONS[1]	IDT54/74FCT861A-64A				IDT54/74FCT861B-64B				UNIT
			COM'L.		MIL.		COM'L.		MIL.		
			MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from R_I to T_i or T_i to R_I IDT54/74FCT861/IDT54/74FCT863 (Non-inverting)	C_L = 50pF R_L = 500Ω	–	8	–	9	–	6.0	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	15	–	17	–	13	–	14	ns
t_{PLH} t_{PHL}	Propagation Delay from R_I to T_i or T_i to R_I IDT54/74FCT862/IDT54/74FCT864 (Inverting)	C_L = 50pF R_L = 500Ω	–	7.5	–	9.0	–	5.5	–	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF[3] R_L = 500Ω	–	14	–	16	–	13	–	14	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_I	C_L = 50pF R_L = 500Ω	–	12	–	13	–	8.0	–	9.0	ns
t_{PZH} t_{PZL}		C_L = 300pF[3] R_L = 500Ω	–	20	–	22	–	15	–	16	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_I	C_L = 5pF[3] R_L = 500Ω	–	9	–	10	–	6	–	7	ns
t_{PHZ} t_{PLZ}		C_L = 50pF R_L = 500Ω	–	10	–	10	–	7.0	–	8.0	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT 54AHCT377

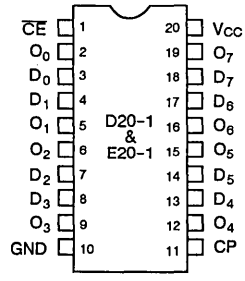
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clock enable
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

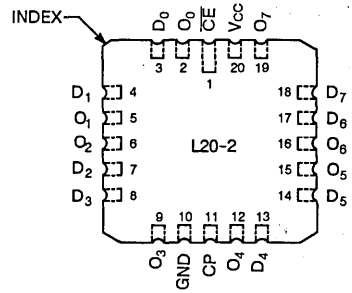
DESCRIPTION:

The IDT54AHCT377 is an octal D flip-flop built using advanced CEMOS™, a dual metal CMOS technology. The IDT54AHCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS

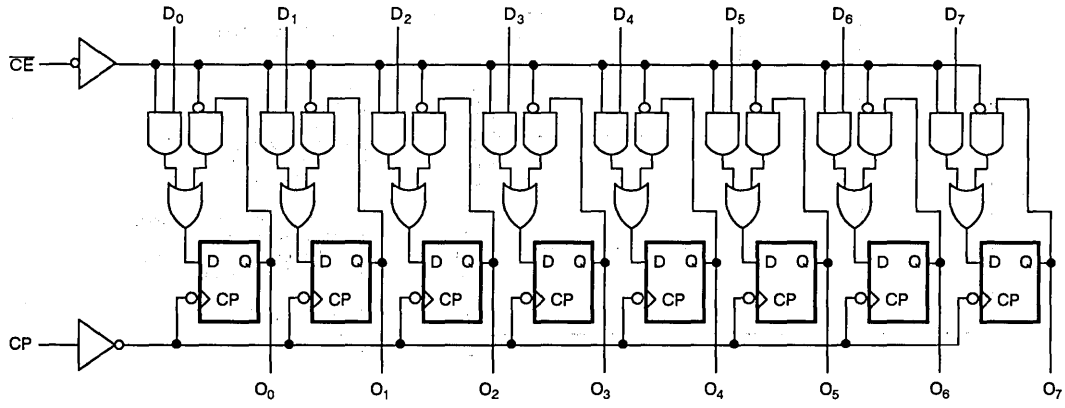


DIP/CERPACK
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5.0	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	mA
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_I = 0$		–	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current [4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_I = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	0.65	3.8	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_I = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ [6] $V_{IN} \leq V_{LC}$ (AHCT)	–	0.63	2.2	
			V_{IN} = 3.4V or [6] V_{IN} = GND	–	2.88	11.2	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	CE	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑ X	h H	X X	No Change No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	TYP.	MIN.[2]	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pF R_L = 500Ω	10.0	2.0	20.0	ns
t_S	Set-up Time HIGH or LOW D_N to CP		5.0	2.0	–	ns
t_H	Hold Time HIGH or LOW D_N to CP		2.0	1.5	–	ns
t_S	Set-up Time HIGH or LOW $\overline{CE}$ to CP		3.0	4.0	–	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		2.0	1.5	–	ns
t_W	Clock Pulse Width, LOW		7.0	7.0	–	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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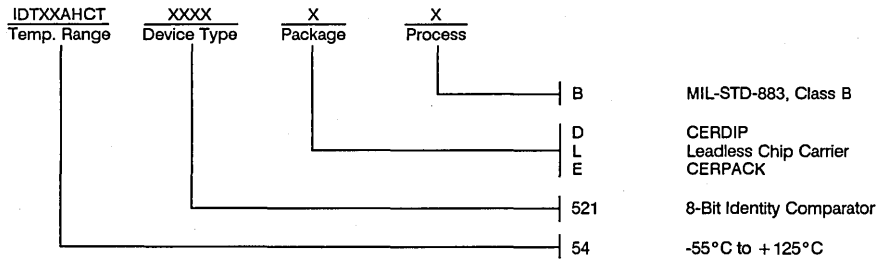
ORDERING INFORMATION



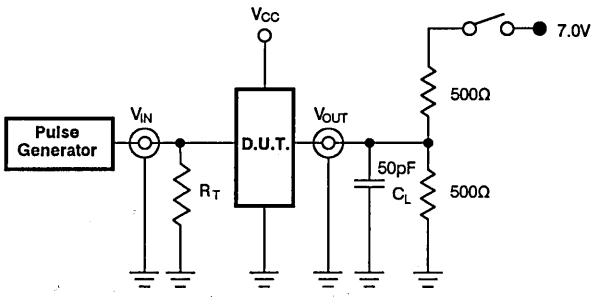
CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1. All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2. Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3. Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4. To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for hardware-induced noise, it may be necessary to use $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for ATE testing purposes.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



SWITCH POSITION

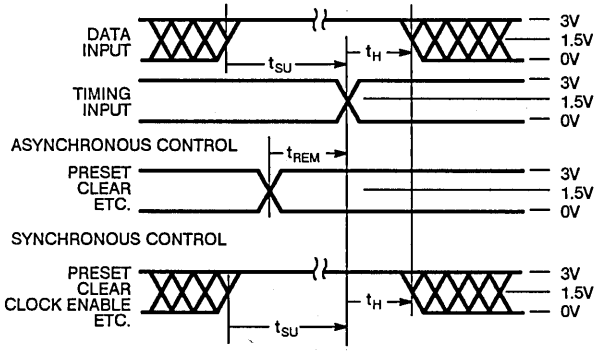
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

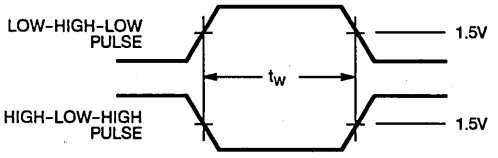
C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

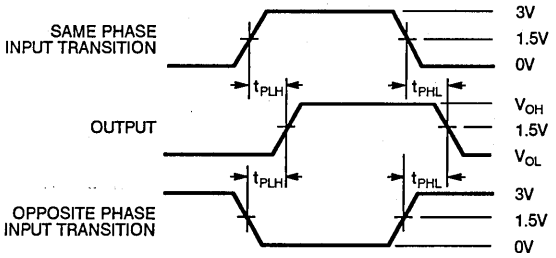
SET-UP, HOLD, AND RELEASE TIMES



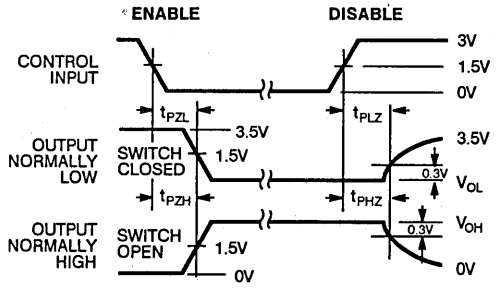
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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DATA CONVERSION INTRODUCTION

The Data Conversion Group is one of the newest members of IDT's product family. Mixing high-speed digital logic with high-performance analog functions opens a number of product opportunities

Video-Speed Analog products are a primary area of concentration for the Data Conversion Group. Integration advances in digital logic have allowed video/graphic resolutions to reach levels approaching broadcast quality in a personal computer. Until now, however, similar advances on the analog side have not been made.

IDT has targeted this area with a family of DACs featuring clock rates in excess of 100MHz (more than 1,000 by 1,000 CRT pixel resolution) and outputs which directly drive the coaxial cable connections to the display. Merging IDT's SRAM technology with analog, it is now possible to integrate all of the functions needed for a high-resolution, RGB graphic output without power-hungry ECL logic.

The recent introduction of a family of PaletteDACs™ has not only boosted integration levels, but performance levels as well. These complete graphics output systems include three 8-bit DACs along with high-speed, dual-ported, palette RAM. The PaletteDACs™ provide the performance for today's standard screen resolution as well as next generation, photo realistic displays.

Many of today's video systems must do extensive computations on the analog signal to enhance, convert and recognize patterns. These computations are done most easily in the digital domain, requiring a high-performance Analog-to-Digital Converter at the front end. IDT's first product offering in this area allows the conversion of video speed analog signals at clock rates exceeding four times the color subcarrier ($\sim$ 14MHz NTSC, $\sim$ 17MHz PAL). Along with the low power consumption, these parts include, a first for the industry, on-chip error detection and correction making it more immune to digital noise and much easier to use.

IDT is dedicated to providing complete CMOS solutions for high-performance system designs. High speed SRAMs, FIFOs, MICROSLICE™ components, Arithmetic Processors, DSP units and FCT fast logic elements form the basis for leading-edge designs. The Data Conversion Group completes this picture with mixed analog and digital chips for front – and back – end interface. Look to IDT for innovative Data Conversion solutions.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT VIDEO DAC MODULE

PRELIMINARY
IDT 75MB38

FEATURES:

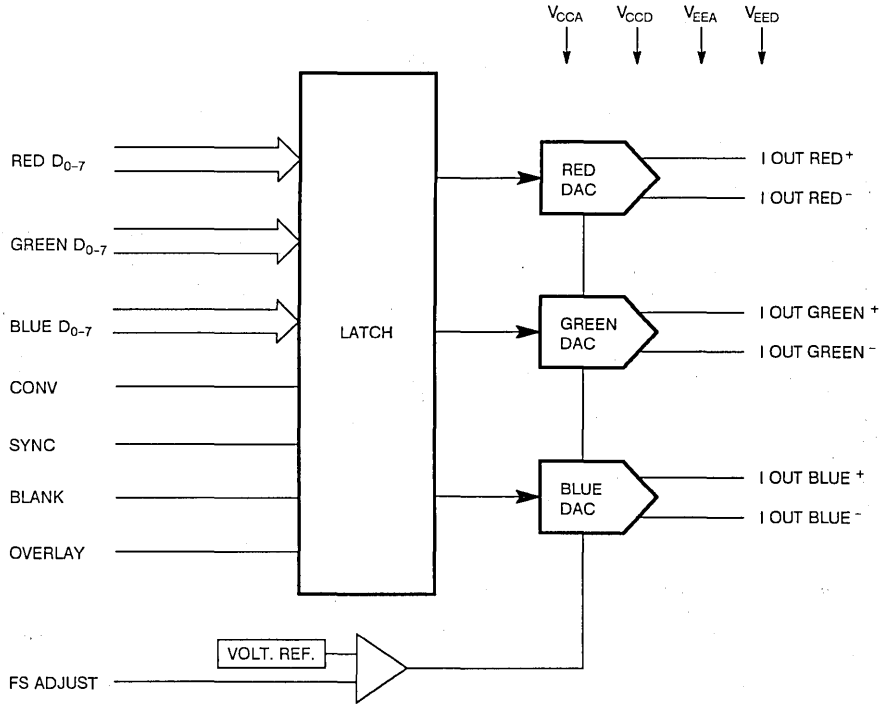
- Graphics Ready
- Pin-compatible with TDC1318 & BT109
- Triple 8-bit DACs, 1/2 LSB linearity
- 70/100/125MHz update rate
- ECL-compatible inputs
- Low power consumption: 1500mW
- On-board voltage reference
- Complementary current outputs
- Registered SYNC, BLANK and OVERLAY inputs
- Surface mount packages on an epoxy laminate substrate

DESCRIPTION:

The IDT75MB38 is a 70/100/125 MegaSample per Second (MSPS), triple 8-bit Digital to Analog Converter capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering or deglitching. All inputs are ECL-compatible and the part runs from a single -5.2V supply.

The IDT75MB38 is built using three IDT75C18 Video DACs in small outline plastic packages, mounted on an epoxy laminate (FR4) substrate. The module fits into a standard 40-pin DIP (600 mil) footprint. Due to IDT's high-performance CEMOS™ process, power consumption is kept under 1500mW.

FUNCTIONAL BLOCK DIAGRAM



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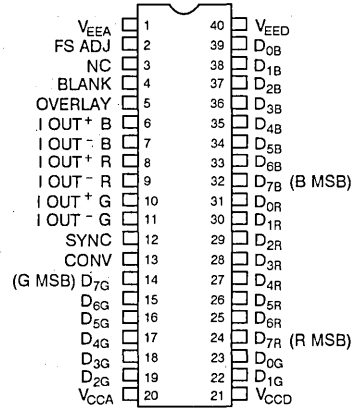
PIN CONFIGURATION



DIP
TOP VIEW

GENERAL INFORMATION

The IDT75MB38 is built using three monolithic Video DACs, a voltage reference and resistor network to control the full-scale output current. All devices are housed in plastic SOIC packages and are mounted on a multilayer FR4 substrate. Conventional through-hole pins are attached for connection to the user's printed circuit board.

The IDT75MB38 provides 24 data input pins (8 each for red, blue and green) which are ECL-compatible. Data are latched on the rising edge of the clock input, CONV. In addition, three control signals are available which ease the interface to RS-343 systems.

The IDT75MB38 outputs three pairs of complementary analog current signals which will directly drive the 75Ω inputs of a color video CRT. The current produced by these outputs is directly proportional to the product of the digital input data and the reference current.

POWER

The IDT75MB38 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. All power and ground pins must be connected and properly decoupled.

REFERENCE

The IDT75MB38 has an on-board voltage reference and associated circuitry which provides a bias voltage for the DAC current switches and sets the full-scale current. Typically, a 1.1K resistor is connected between the FS Adjust pin and V_{CCA} which provides the reference current to the DACs.

DATA INPUTS

The IDT75MB38 has 24 data inputs which are ECL-compatible and have an internal pull-down resistor which forces unconnected pins to their inactive state. Each DAC, red, green and blue, has 8 data inputs which are latched on the rising edge of the clock, CONV. Data must be valid for a set-up time (t_S) before and a hold time (t_H) after this edge to be correctly latched.

SYMBOL	FUNCTION
D_7	MSB
D_6	
D_5	•
D_4	•
D_3	•
D_2	
D_1	
D_0	LSB

CONTROL INPUTS

The IDT75MB38 has three special control inputs, SYNC, BLANK and OVERLAY, which ease the interface in video applications. These inputs are ECL-compatible and have an internal pull-down resistor which forces unconnected pins to their inactive state. The controls, as the data inputs, are latched on the rising edge of clock.

The video controls produce specific output levels for RS-343 compatible synchronization and blanking. Also provided is a 110% white OVERLAY function. SYNC is only active on the IOG output and overrides all other data and control on that output only. BLANK is active on all three DACs, overrides OVERLAY and data, and produces a "blacker than black" level. OVERLAY produces a "whiter than white" level and overrides data on all three DACs.

CLOCK

The clock input, CONV, is a single-ended, ECL-compatible input. On the rising edge of CONV, all data and control inputs are latched provided that they were valid for a set-up time before and a hold time after the edge.

ANALOG OUTPUTS

The IDT75MB38 has three complementary current outputs corresponding to the red, green and blue DACs. These outputs are high-impedance current sinks which can directly drive a doubly terminated 75Ω load to video levels compatible with the RS-343A standard. The output current is proportional to the product of the DAC input data and the reference current set on the internal FS Adj.

VIDEO OUTPUT VALUES[4]

DESCRIPTION	SYNC	BLANK	OVERLAY	DATA	I_{OUT-}[2] mA	V_{OUT-}[3] mV	I_{OUT+}[2] mA	V_{OUT+}[3] mV
110% White	0	0	1	X	0.00	0.00	28.56	-1071
Reference White	0	0	0	FF	1.95	-73	26.61	-998
Reference Black	0	0	0	00	19.41	-728	9.15	-343
Blank	0	1	X	X	20.83	-781	7.73	-290
Sync[1]	1	X	X	X	28.56	-1071	0	0

NOTES:

1. IOG output only. IOR and IOB have no SYNC input.
2. Current is specified as conventional current when flowing into the device.
3. Voltage produced when driving the standard load configuration, 37.5Ω.
4. RS-343A tolerance on all control values assumed.

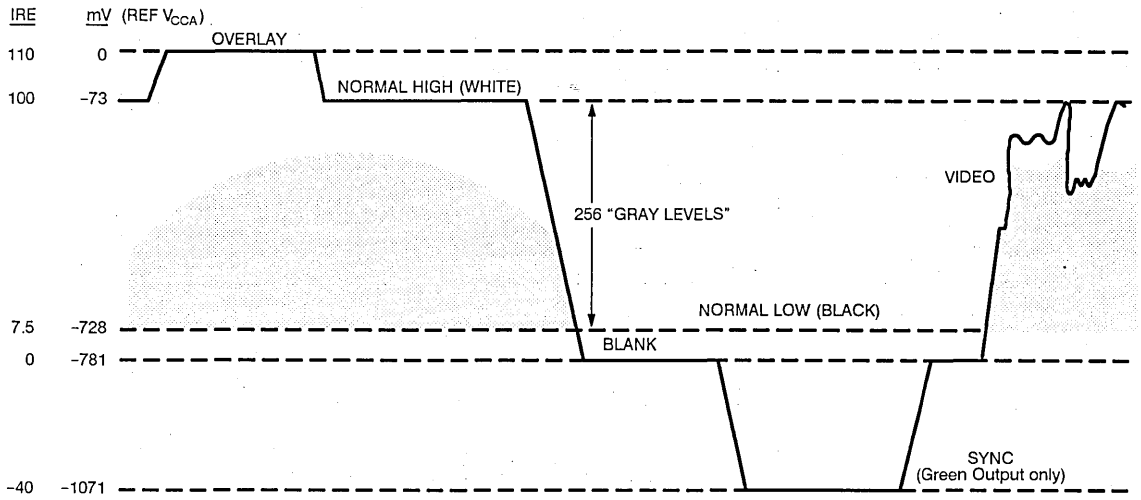


Figure 1. Video Output Waveform for I_{OUT}- and Standard Load Configuration

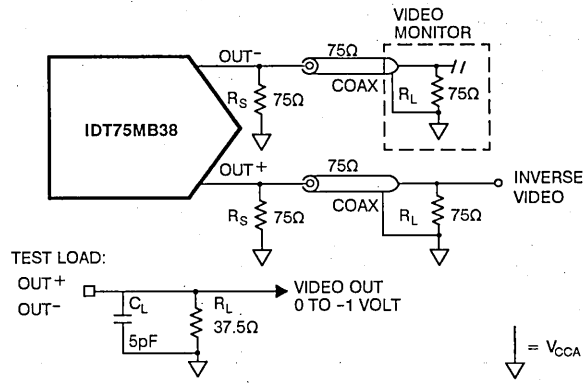


Figure 2. Standard Load Configuration

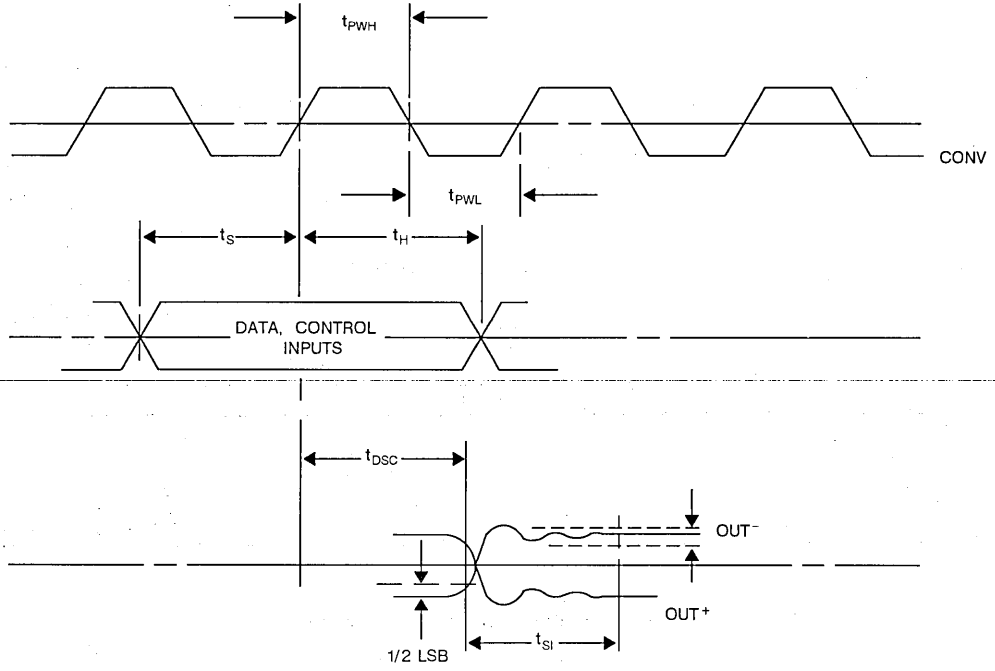


Figure 3. Timing Diagram

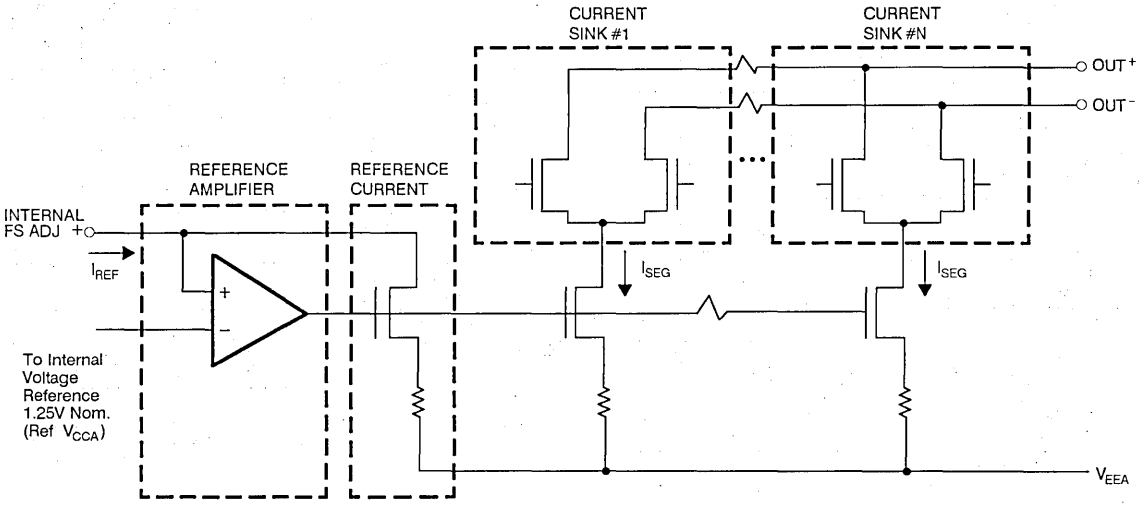


Figure 4. Equivalent Output Circuit

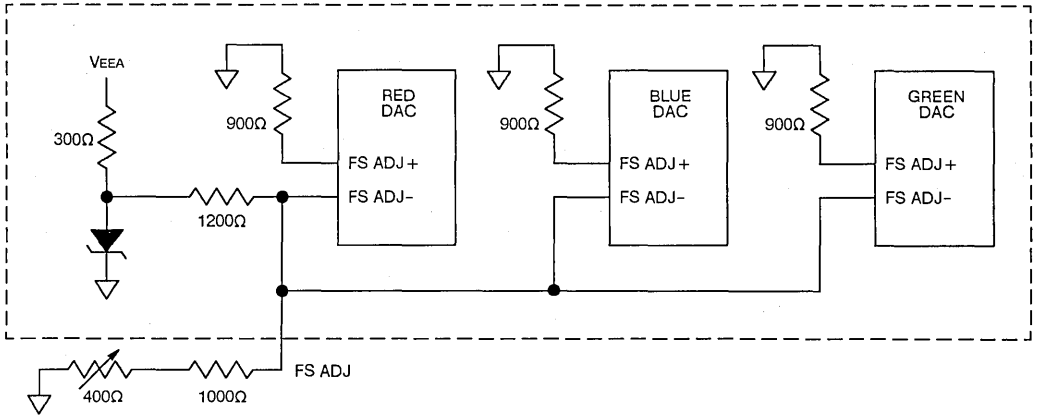


Figure 5. FS ADJ Internal Circuitry

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{EED}	Measured to V_{CCD}	-7.0 to +0.05	V
V_{EEA}	Measured to V_{CCD}	-7.0 to + 0.05	V
A_{GND}	Measured to V_{CCD}	-0.5 to + 0.5	V
INPUT VOLTAGES			
CONV, Data & Controls	Measured to V_{CCD}	V_{EED} to 0.5	V
FS ADj, Applied Voltage(2)	Measured to V_{CCA}	V_{EEA} to 0.5	V
OUTPUT			
Analog Output, Applied Voltage(2)	Measured to V_{CCA}	-2.0 to +0.4	V
Analog Output, Applied Current(3,4)		50	mA
Short Circuit Duration		Unlimited	
TEMPERATURE			
Operating, Ambient	Commercial	0 to +70	°C
Storage	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{EED}	Digital Supply Voltage (REF V_{CCD})	-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (REF V_{CCA})	-4.9	-5.2	-5.5	V
V_{CCA}	Analog Ground Voltage (REF V_{CCD})	-0.1	0	+ 0.1	V
V_{EEA}-V_{EED}	Supply Voltage Differential	-0.1	0	+ 0.1	V
V_{IL}	Input Voltage, Logic LOW	-1.49	–	–	V
V_{IH}	Input Voltage, Logic HIGH	–	–	-1.045	V
R_{REF}	Reference Current, Video Std.	1100	1200	1300	Ω
T_A	Ambient Temperature	0	–	70	°C

NOTE:

1. Minimum and maximum values allowed by +5% variation given in RS-343A and RS-170 after initial gain correction of device.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
I_{EEA+} I_{EED}	Supply Current	$V_{EEA} = V_{EED}$ = Max.,(1)Static	–	–	mA
C_I	Input Capacitance, Data & Controls		–	15	pF
V_{OCP}	Compliance Voltage, +Output		-1.2	+0.1	V
V_{OCN}	Compliance Voltage, -Output		-1.2	+0.1	V
R_O	Equivalent Out R		20	–	kΩ
C_O	Equivalent Out C		–	20	pF
I_{OP}	Max. I, +Output	V_{EEA} = Typ., SYNC = BLANK = 0 OVERLAY = 1	30	–	mA
I_{ON}	Max. I, -Output(2)	V_{EEA} = Typ., SYNC = 1	30	–	mA
I_{IL}	Input Current, Logic LOW, Data & Controls	V_{EED} = Max.: V_I = -1.40V	–	600	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls	V_{EED} = Max.: V_I = -1.00V	–	600	µA
I_{IC}	Input Current, CONV	V_{EED} = Max.: -2.5 < V_I < -0.5	–	150	µA

NOTES:
1. Worst case for all Data and Control States. No termination on I_{OUT+} or I_{OUT-}.
2. Green output only.

AC ELECTRICAL CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MB5038X70 MIN.	IDT7MB5038X70 MAX.	IDT7MB5038X100 MIN.	IDT7MB5038X100 MAX.	IDT7MB5038X125 MIN.	IDT7MB5038X125 MAX.	UNIT
F_S	Max. Conversion Rate	V_{EEA}, V_{EED}, = Min.	–	70	–	100	–	125	MHz
t_{PWL}	CONV LOW Time	V_{EEA}, V_{EED}, = Min.	6	–	5	–	4	–	ns
t_{PWH}	CONV HIGH Time	V_{EEA}, V_{EED}, = Min.	6	–	5	–	4	–	ns
t_S	Set-up Time, Data & Control	V_{EEA}, V_{EED}, = Min.	8	–	6	–	5	–	ns
t_H	Hold Time, Data & Control	V_{EEA}, V_{EED}, = Min.	5	–	1	–	0	–	ns
t_{DSC}	CONV to OUT Delay	V_{EEA}, V_{EED}, = Min.	–	14	–	10	–	8	ns
t_{SI}	Current Setting Time	V_{EEA}, V_{EED}, = Min. 0.2% 0.8% 3.2%	 – – –	 – – –	 – – –	 – – –	 – – –	 – – –	 ns ns ns
t_{RI}	Current Rise Time	10% to 90% of Full Scale	–	3.0	–	2.1	–	1.7	ns

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SYSTEM PERFORMANCE CHARACTERISTICS

Specifications over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
ELI	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
ELD	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
IOF	Output Offset I	V_{EEA}, V_{EED} = Max. SYNC = BLANK = 0 OVERLAY = 1	–	±1.0	µA
EG	Abs. Gain Error	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	±5	%FS
TCG	Gain Error Tempco		–	–	%FS/°C
DP	Differential Phase	F_S = 4 x NTSC	–	1.0	Deg.
DG	Differential Gain	F_S = 4 x NTSC	–	2.0	%
PSRR	Power Supp. Rej. Ratio	V_{EEA}, V_{EED}, I_{REF} = Typ.(1) V_{EEA}, V_{EED}, I_{REF} = Typ.(2)	– –	45 55	dB dB
PSS	Power Supp. Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	120	µV/V
GC	Peak Glitch Charge(3, 4)		–	800	f_C
GI	Peak Glitch Current		–	1.2	mA
GE	Peak Glitch Energy(4)		–	30	pV-Sec
FT	Clock Feedthrough	Data Constant(5)	–	-50	dB
FT	Data Feedthrough	Clock Constant(5)	–	-50	dB
MDD	DAC to DAC Matching	V_{EEA}, V_{EED}, I_{REF} = Typ.		5	%
CT	Crosstalk	V_{EEA}, V_{EED}, I_{REF} = Typ.(5) Source = 3.0 MHz, Full Grey Scale Sine Wave		50	dB

NOTES:

1. 20kHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB reltive to full gray scale.
3. $f_{Coulombs}$ = microamps x nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

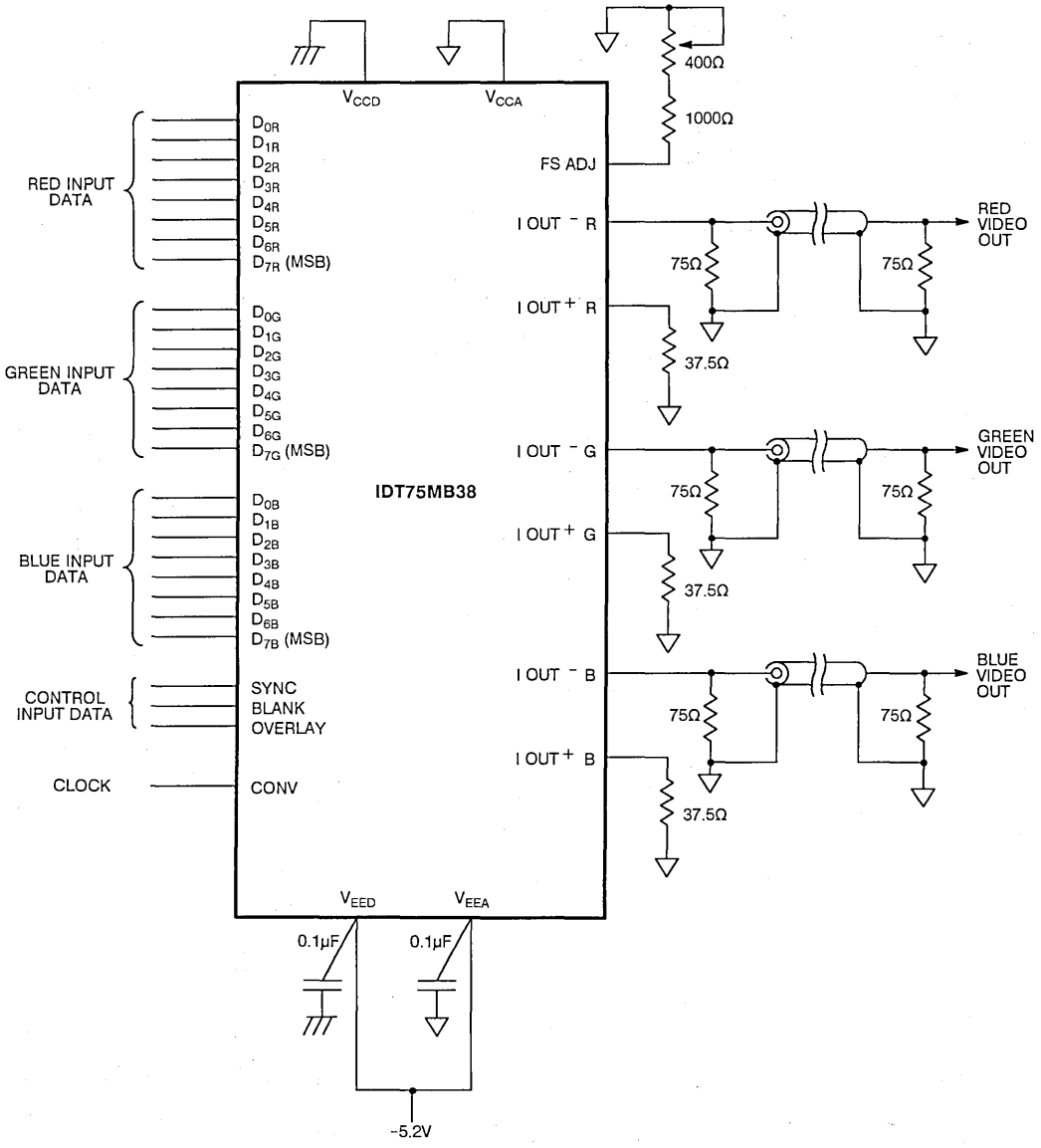

Figure 6. Typical Interface Circuit

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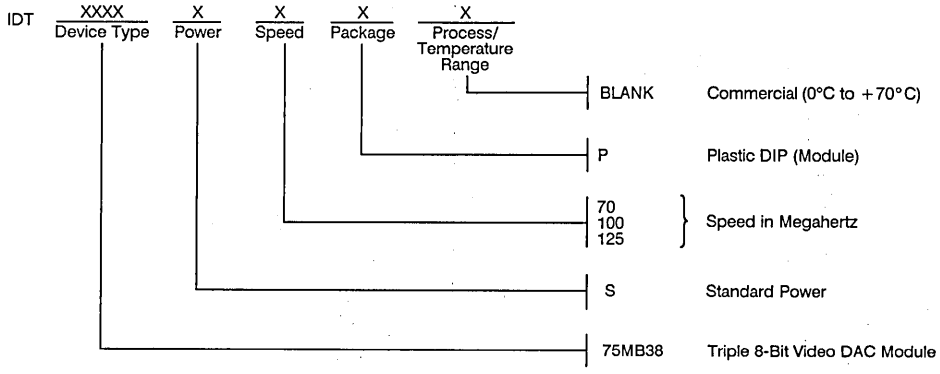
ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT PALETTEDAC™

IDT 75C458

FEATURES:

- 165/135/125/110/80MHz operating speed
- Fixed pipeline delay: 9 clock cycles
- 50ns read access time
- Integral and differential linearity < 1/2LSB
- Triple 8-bit DACs
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- CEMOS™ monolithic construction
- Single 5V power supply
- 84-pin PGA and PLCC packages
- Typical power dissipation: 1000mW
- Pin- and function-compatible with Brooktree BT458
- Military product is compliant to MIL-STD-883, Class B

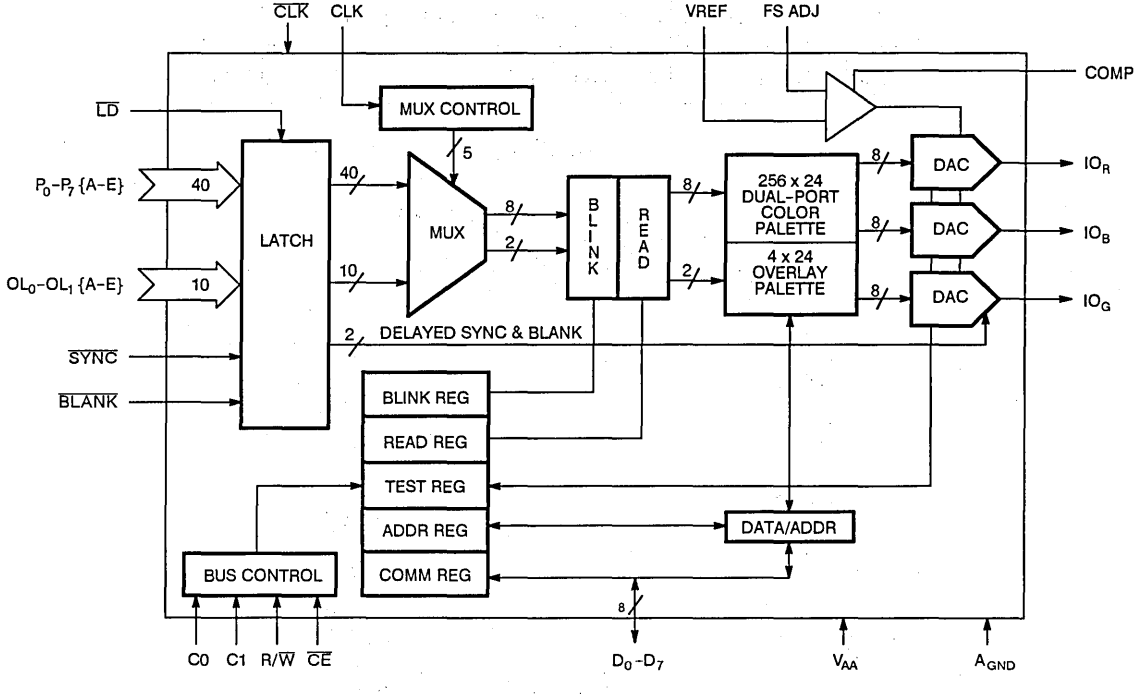
DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

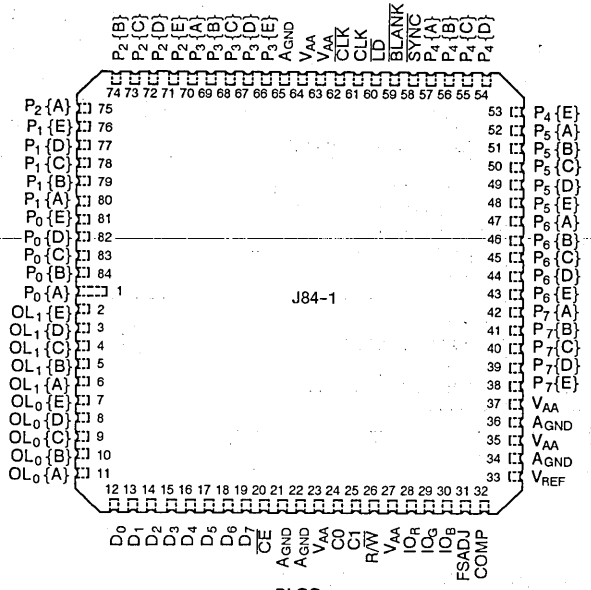


CEMOS and PaletteDAC are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	A_{GND}	V_{AA}	$P_7\{D\}$	$P_7\{B\}$	$P_6\{E\}$	$P_6\{C\}$	$P_6\{B\}$	$P_5\{E\}$	$P_5\{C\}$	$P_5\{B\}$	$P_4\{E\}$
11	IO_B	A_{GND}	V_{AA}	$P_7\{E\}$	$P_7\{C\}$	$P_7\{A\}$	$P_6\{D\}$	$P_6\{A\}$	$P_5\{D\}$	$P_5\{A\}$	$P_4\{C\}$	$P_4\{A\}$
10	IO_G	FSADJ	V_{REF}							$P_4\{D\}$	$P_4\{B\}$	$\overline{SYNC}$
9	V_{AA}	IO_R									$\overline{BLANK}$	$\overline{LD}$
8	C1	R/$\overline{W}$									$\overline{CLK}$	CLK
7	V_{AA}	C0									V_{AA}	V_{AA}
6	A_{GND}	A_{GND}					G84-2				$P_3\{E\}$	A_{GND}
5	$\overline{CE}$	D_7									$P_3\{C\}$	$P_3\{D\}$
4	D_6	D_5									$P_3\{A\}$	$P_3\{B\}$
3	D_4	D_2	D_0	△ ALIGNMENT MARK						$P_2\{A\}$	$P_2\{C\}$	$P_2\{E\}$
2	D_3	D_1	$OL_0\{B\}$	$OL_0\{E\}$	$OL_1\{B\}$	$OL_1\{E\}$	$P_0\{B\}$	$P_0\{D\}$	$P_1\{A\}$	$P_1\{D\}$	$P_1\{E\}$	$P_2\{D\}$
1	$OL_0\{A\}$	$OL_0\{C\}$	$OL_0\{D\}$	$OL_1\{A\}$	$OL_1\{C\}$	$OL_1\{D\}$	$P_0\{A\}$	$P_0\{C\}$	$P_0\{E\}$	$P_1\{B\}$	$P_1\{C\}$	$P_2\{B\}$

PGA
TOP VIEW



PLCC
TOP VIEW

GENERAL INFORMATION:

The IDT75C458 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to an analog RS-343A, high bandwidth output. To decrease the frame buffer memory requirements, the IDT75C458 has a color lookup table (dual-port RAM) included on-chip.The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/W port and one high-speed R/O port and three 8-bit video speed DACs.

MICROPROCESSOR BUS INTERFACE

The IDT75C458 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0 - D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{W}$, and a clock input, $\overline{CE}$. All data and control information are latched on the falling edge of $\overline{CE}$, as shown in Figure 3. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{W}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 addresses with 8 bits of red, blue and green information. Additionally, there are four extra addresses assigned to overlay information, yielding a total memory size of 260 x 24.

Access to the palette entries is, again, through the address register. The desired palette address is loaded into the address register, C0 and C1 are modified to point to the color palette or overlay and the information is read or written. In this case, however, an internal counter is used to access the red, green or blue color information. The first color palette or overlay access reads or writes red. The next access is for green, while the third access is for blue. After the third access, the address register is incremented, allowing the reading or writing of the red information of the next palette address. When writing, red and green information is temporarily stored in registers and, during the blue cycle, all 24 bits are written.

The internal counter is reset by an access to the address or any of the control registers. After setting the address register, it is possible to read or write the entire palette without accessing the address register again. Some care is needed; only continuous reads or writes are allowed and it is not possible to switch between the color palette and overlay.

The color palette RAM and overlay registers are dual-ported which allows simultaneous access from the MPU port (D_0 - D_7) and the pixel port (P_0 - P_7{A-E}). If the pixel port is reading the same palette entry as the MPU is writing, it is possible that the DAC output may be invalid. It is recommended that the palette and overlay entries be updated during the blanking time.

ADDRESS REGISTER DATA	C1	C0	ACCESS
X	0	0	Address Register
$00-$FF	0	1	Color Palette
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

NOTE:
Control input C0 = 1 enables the internal counter which accesses the red, green and blue colors individually and increments the address counter after the blue access. C0 = 0 disables auto-increment of the address register allowing read-modify-write operations.

Table 1. Truth Table for MPU Operations

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C458 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency, CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0 - P_7{A-E} and up to 10 bits of overlay information are input through OL_0 - OL_1{A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C458 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank times are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0 - OL_1) have the same timing as the pixel inputs (P_0 - P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

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Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0 - P_7) and two bits of overlay information (OL_0 - OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. In this way, 8 bits of information can select from a palette of over 16 million with 256 simultaneous displayed colors (plus 3 overlay colors). Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR6	OL_1	OL_0	$P_7 - P_0$	PALETTE ENTRY
1	0	0	$00	Color palette entry $00
1	0	0	$01	Color palette entry $01
	.			.
	.			.
	.			.
1	0	0	$FF	Color palette entry $FF
0	0	0	$xx	Overlay color 0
x	0	1	$xx	Overlay color 1
x	1	0	$xx	Overlay color 2
x	1	1	$xx	Overlay color 3

NOTE:
CR6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

Video Generation, DACs

On every CLK cycle, the selected 24 bits of color information (8 bits each of red, green and blue) from the Color Palette RAM are presented to the three 8-bit D/A converters. The IDT75C458 uses a 5 x 3 segmented approach where the five MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "course" output levels. The remaining three LSBs of input data drive three binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are pipelined to maintained synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Note that the sync information is only available at the IO_G (green) output and that the input data to the DAC sums with the sync current. Table 3 details the output levels associated with $\overline{SYNC}$, $\overline{BLANK}$ and data.

Monitor Interface

The analog outputs of the IDT75C458 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 4.

Description	S	B	DAC data	IO_G(mA)	IO_R, IO_B (mA)
WHITE	1	1	$FF	26.67	19.05
DATA	1	1	data	data+9.05	data+1.44
DATA & SYNC	0	1	data	data+1.44	data+1.44
BLACK	1	1	$0	9.05	1.44
BLACK & SYNC	0	1	$0	1.44	1.44
BLANK	1	0	X	7.62	0
SYNC	0	0	X	0	0

NOTE:
Typical values with full scale IOG=26.67mA. RSET=523Ω, VREF=1.235V. S is $\overline{SYNC}$, B is $\overline{BLANK}$.

Table 3. Video Output Truth Table

IO_R, IO_B		IO_G	
mA	V	mA	V
19.05	0.714	26.67	1.000
•	•	•	•
•	•	•	•
•	•	•	•
1.44	9.954	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

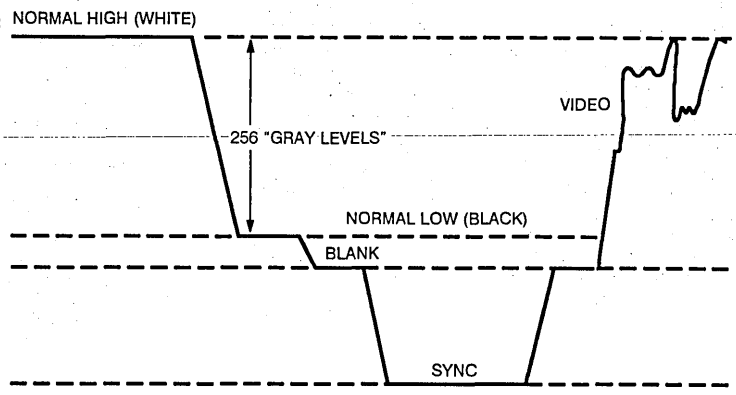


Figure 1. Composite Video Output Waveform

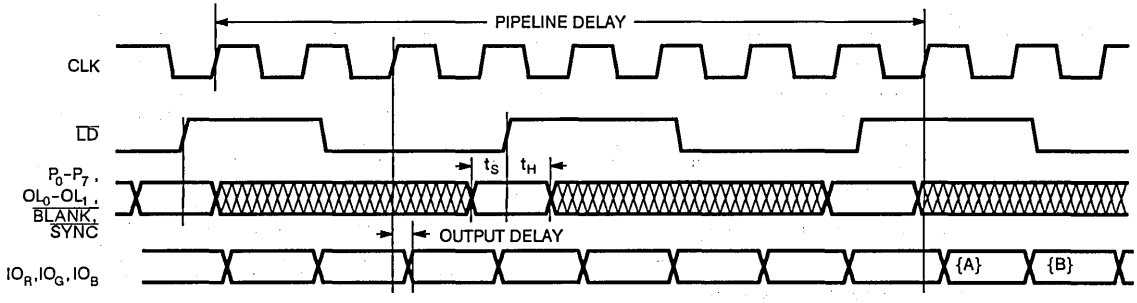


Figure 2. Pixel Timing

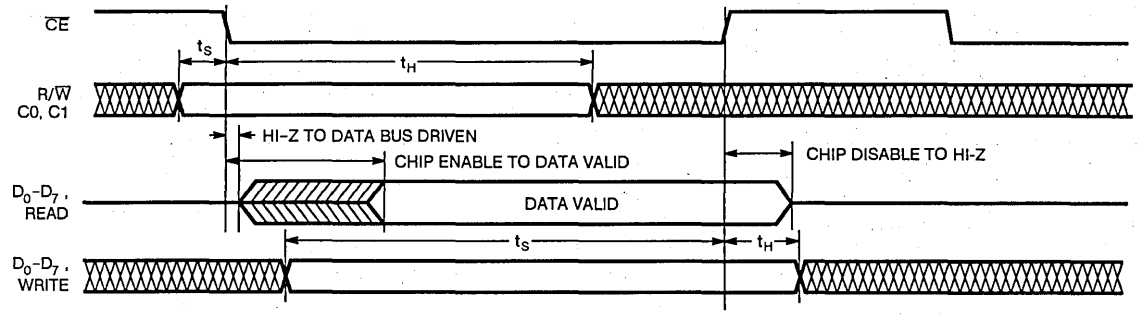


Figure 3. Data Bus Timing

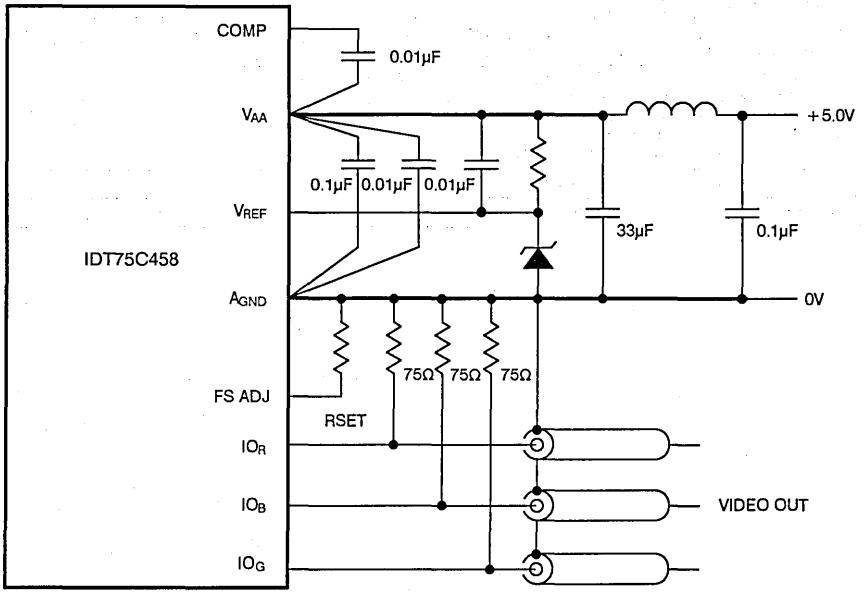


Figure 4. Typical Application

11

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DATA BUS	
$D_0 - D_7$	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on $D_0 - D_7$ is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus $D_0 - D_7$. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, $D_0 - D_7$ are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
PIXEL	
CLK, $\overline{CLK}$	Pixel Clock inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register, bit 7). The pixel data, $P_0 - P_7$ {A-E} and $OL_0 - OL_1$ {A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
$P_0 - P_7$ {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
$OL_0 - OL_1$ {A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as $P_0 - P_7$ and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information $P_0 - P_7$ {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (IO_R, IO_G, IO_B) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the IO_G analog output and overrides no other pixel information. For the correct SYNC level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
ANALOG	
A_{GND}	Analog Ground Power Supply, 0V.
V_{AA}	Analog Power Supply, 5V.
V_{REF}	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS ADJ	Full-Scale Adjust Input. The current flowing from this pin to A_{GND} is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and A_{GND}. The voltage on this pin is approximately equal to V_{REF}. The relationship between the full-scale output current and RSET is: IO_G (mA) = 11.294 x V_{REF} (V)/RSET (KΩ) IO_R, IO_B (mA) = 8.067 x V_{REF} (V)/RSET (KΩ)
IO_G, IO_R, IO_B	Green, Red and Blue DAC current outputs.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.

INTERNAL REGISTERS

Command Register

The Command Register is accessed by reading or writing with the Address Register = $06, C0 = 0 and C1 = 1 (see Table 1). It provides control over multiplexing and blink rate selection. The Command Register may be read or written at any time. CR7 (Command Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0 — OL_0 display enable. This bit is ANDed internally with the data from OL_0 prior to the palette selection. If CR0 is LOW, the internal OL_0 bits are set LOW allowing only overlay colors 0 and 2 to be selected.

CR1 — OL_1 display enable. This bit is ANDed internally with the data from OL_1 prior to the palette selection. If CR1 is LOW, the internal OL_1 bits are set LOW allowing only overlay colors 0 and 1 to be selected.

CR2 — OL_0 blink enable. If this bit is set HIGH, the OL_0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.

CR3 — OL_1 blink enable. If this bit is set HIGH, the OL_1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.

CR4, CR5 — Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.

CR6 — Color Palette RAM enable. This bit specifies whether to use the Color Palette or the Overlay Palette when $OL_0 = OL_1 =$ LOW.

CR7 — Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing, the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = $04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

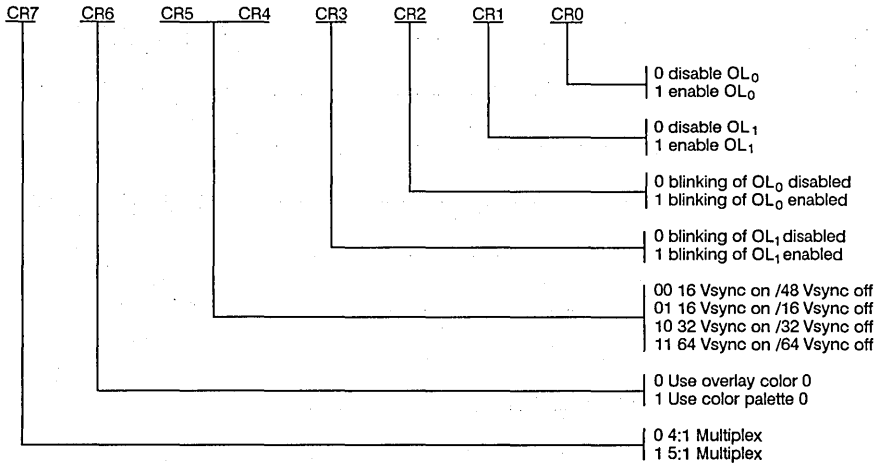
The Blink Mask Register is accessed by reading or writing with the Address Register = $05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P_0 - P_7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D_7 (Data Bus bit 7).

Test Register

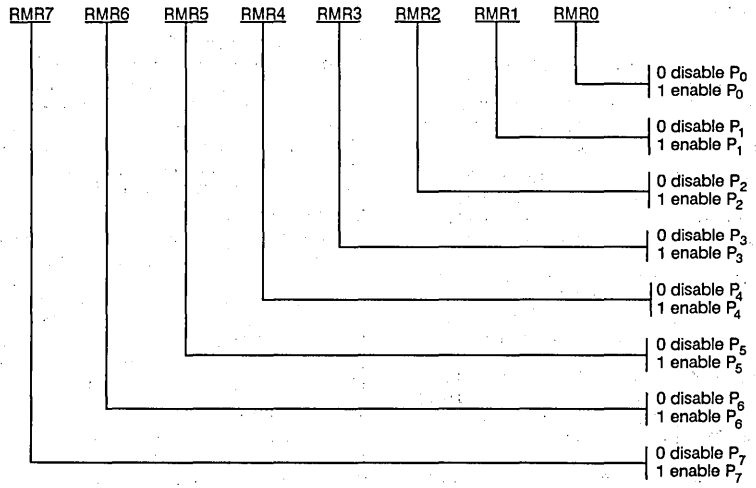
The Test Register is accessed by reading or writing with the Address Register = $07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 24 input bits of the DACs. The register bits are defined below.

TR7-TR4	Read data (one nibble of red, blue or green)
TR3	Upper (LOW) or Lower (HIGH) nibble select
TR2	Blue enable
TR1	Green enable
TR0	Red enable

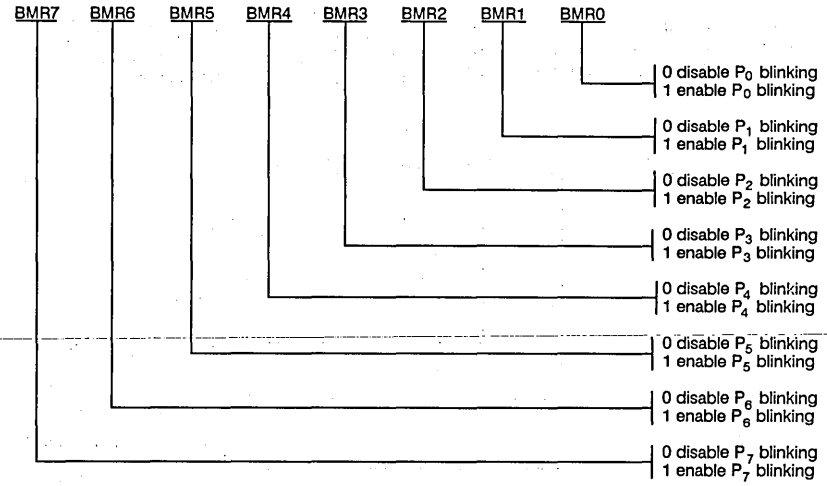
The desired DAC is selected by setting only one color enable bit (D_0 - D_2) HIGH and the upper or lower nibble is selected with D_3. After this write operation, a subsequent read yields the DAC data on D_7 - D_4 and the previously written enable data on D_0 - D_3. For a correct read, pixel and overlay data must remain constant for the entire MPU read cycle. When $\overline{BLANK}$ is asserted, the Test Register information D_7 - D_4 will be forced to zero. TR7 (Test Register bit 7) corresponds to D_7 (Data Bus bit 7).



COMMAND REGISTER DESIGNATIONS



READ MASK REGISTER DESIGNATIONS



BLINK MASK REGISTER DESIGNATIONS

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{AA}	Measured to A_{GND}	-0.5 to +7.0	V
INPUT VOLTAGE			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} +0.5	V
OUTPUT			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} +0.5	V
Applied Current(2,3,4)	Externally forced	-1.0 to +6.0	mA
Short Circuit Duration	Single output High to A_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{AA}	Power Supply	Measured to A_{GND}	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ., Static	–	200	–	mA
V_{IH} (1)	Input Voltage HIGH		2.0	–	V_{AA} +0.5	V
V_{IL} (1)	Input Voltage LOW		A_{GND} -0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} -1.0	–	V_{AA} +0.5	V
V_{CIL}	Clock Input Voltage LOW		A_{GND} -0.5	–	V_{AA} -1.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	µA
I_{IL}	Input Current LOW	V_{IN} = 0.8V	–	–	1	µA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = -800µA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	µA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		IDT75C458-165		IDT75C458-135		IDT75C458-125		IDT75C458-110		IDT75C458-80		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	165	–	135	–	125	–	110	–	80	MHz
F_{LD}	$\overline{LD}$ Clock Frequency	–	41	–	34	–	32	–	28	–	20	MHz
t_{CS}	Control Set-up Time; C0, C1, R/$\overline{W}$	0	–	0	–	0	–	0	–	0	–	ns
t_{CH}	Control Hold Time; C0, C1, R/$\overline{W}$	15	–	15	–	15	–	15	–	15	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	20	–	20	–	25	–	25	–	25	–	ns
t_{CEL}	$\overline{CE}$ LOW Time	30	–	30	–	50	–	50	–	50	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	10	–	10	–	10	–	10	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	30	–	30	–	50	–	50	–	75	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus HI-Z	–	15	–	15	–	15	–	15	–	15	ns
t_{WDS}	Write Data Set-up Time	30	–	30	–	35	–	35	–	50	–	ns
t_{WDH}	Write Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{CLKCY}	Clock Cycle Time	6	–	7.4	–	8	–	9	–	12	–	ns
t_{CLKPL}	Clock Pulse Width LOW	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	24	–	29	–	31	–	35	–	50	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	10	–	12	–	13	–	15	–	20	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	10	–	12	–	13	–	15	–	20	–	ns
t_{PS}	Pixel Data Set-up Time	2	–	3	–	3	–	3	–	4	–	ns
t_{PH}	Pixel Data Hold Time	1	–	2	–	2	–	2	–	2	–	ns
t_{AAD}	Dynamic Supply Current Commercial Temp.	–	450	–	425	–	400	–	380	–	360	mA
t_{AAD}	Dynamic Supply Current Military Temp.	–	500	–	475	–	450	–	430	–	410	mA

ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Res	Resolution			–	8	–	bits
I_{LSB}	LSB Current Size			–	69.1	–	µA
L_I			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
L_D			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
V_{OC}	Output Compliance Voltage			-1.0	–	1.2	V
R_{AOUT}(2)	Output Impedance				50		kΩ
C_{AOUT}(2)	Output Capacitance	f = 1MHz, I_{OUT} = 0mA			8	12	pF
I_{REF}	V_{REF} Input Current				10		µA
E_M	Matching Error (DAC to DAC)			–	2	5	%
PSRR	Power Supply Rejection Ratio			–	50	–	dB
I_W(1)	White Current	Measured to Blank		17.69	19.05	20.40	mA
I_W(1)	White Current	Measured to Black		16.74	17.62	18.50	mA
I_B(1)	Black Current	Measured to Blank		0.95	1.44	1.90	mA
I_{BLANK}	Blank Current IO_R, IO_B			0	5	50	µA
I_{BLANK}(1)	Blank Current IO_G			6.29	7.62	8.96	mA
I_{SYNC}	Sync Current IO_G			0	5	50	µA

NOTE:
1. R_{SET} = 523Ω, V_{REF} = 1.235V
2. This parameter is guaranteed but not tested in production.

ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time <5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time <2ns
Timing reference points at 50% of signal swing

		IDT75C458-165			IDT75C458-135			IDT75C458-125			IDT75C458-110			IDT75C458-80			
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	–	165	–	–	135	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns
t_{VT}	Video Output Transition Time	–	1.5	–	–	1.7	–	–	1.8	–	–	2	–	–	2	–	ns
t_S	Video Output Skew(1)	–	0	<2	–	0	<2	–	0	<2	–	0	<2	–	0	<2	ns
t_{SI}(2)	Video Output Settling Time	–	6	–	–	7	–	–	8	–	–	8	–	–	12	–	ns
FT(2)	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
G_E(2)	Glitch Energy	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
CT(2)	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	9	–	9	9	–	9	9	–	9	9	–	9	9	–	9	clock

NOTE:
1. C_L = 10pF, 10%-90% points
2. This parameter is guaranteed but not tested in production.

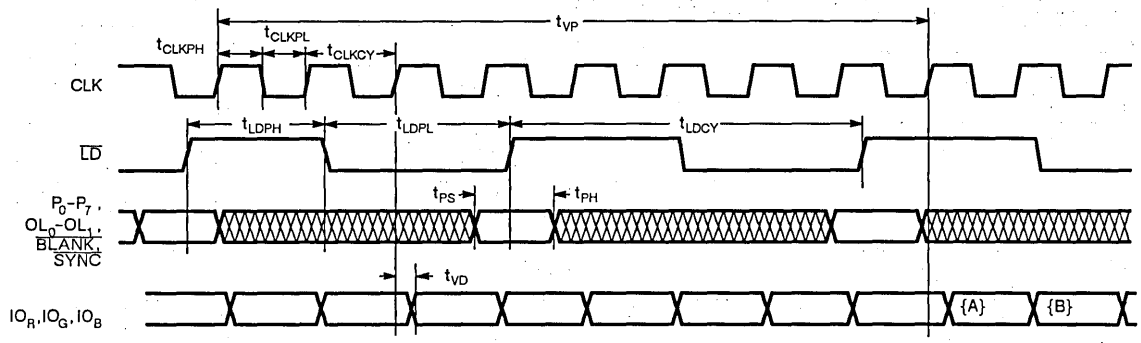


Figure 5. Video I/O Timing Diagram

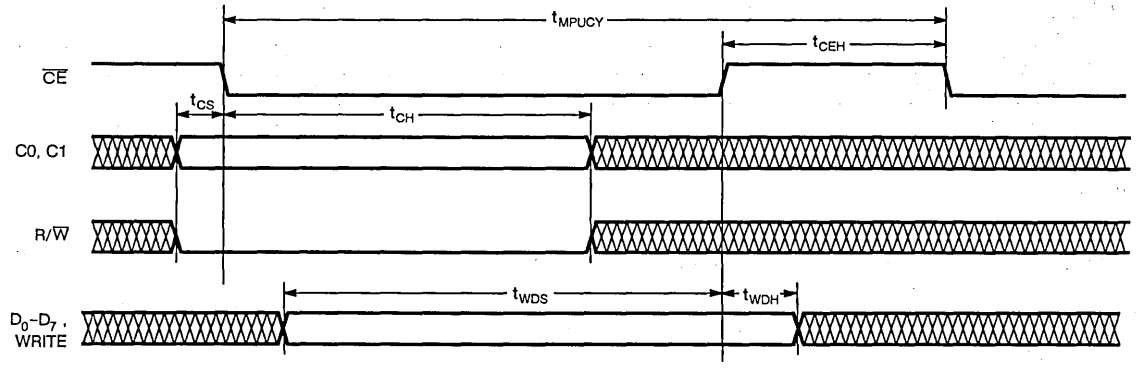


Figure 6. MPU WRITE Timing Diagram

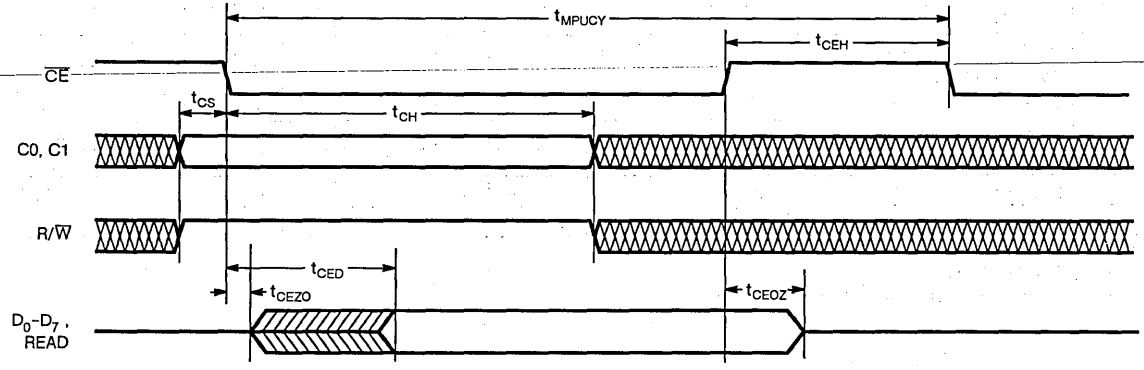
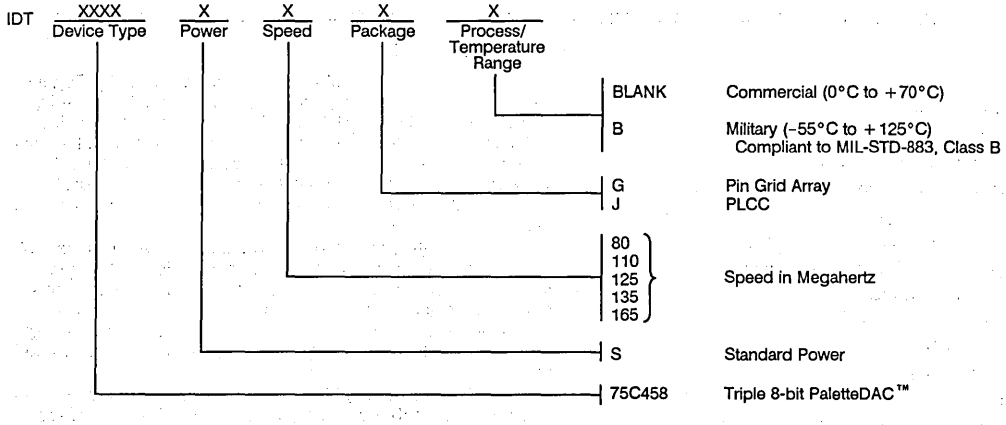


Figure 7. MPU READ Timing Diagram

ORDERING INFORMATION



11

Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT 75C48

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Guaranteed no missing codes
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- Selectable output formats
- TTL-compatible
- Available in 28-pin Plastic DIP, CERDIP and LCC
- Military product is compliant to MIL-STD-883, Class B

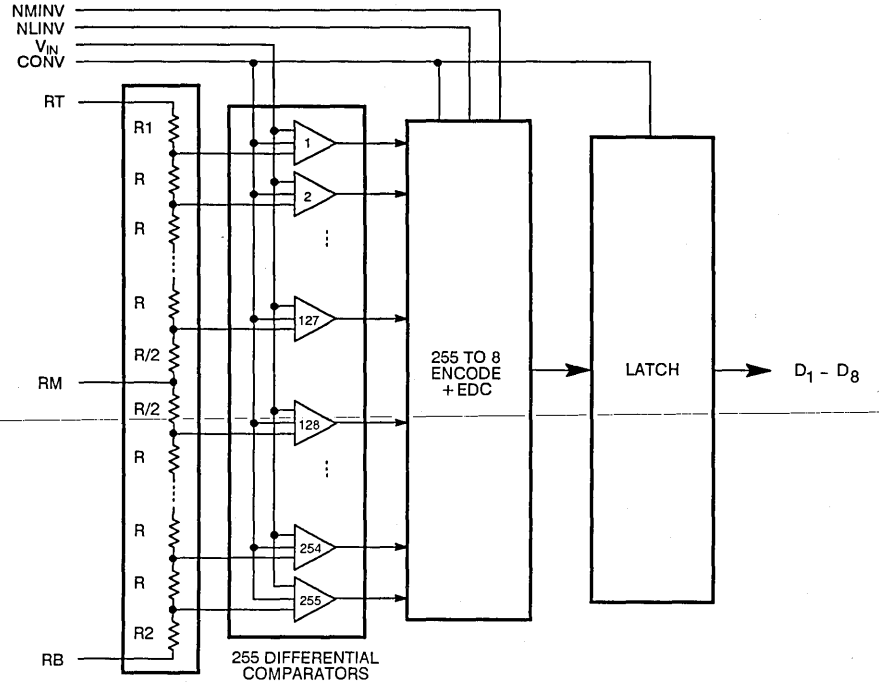
DESCRIPTION:

The IDT75C48 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10 MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption, due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

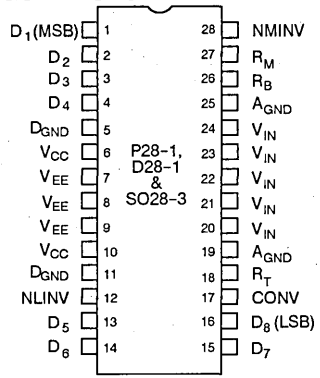
The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

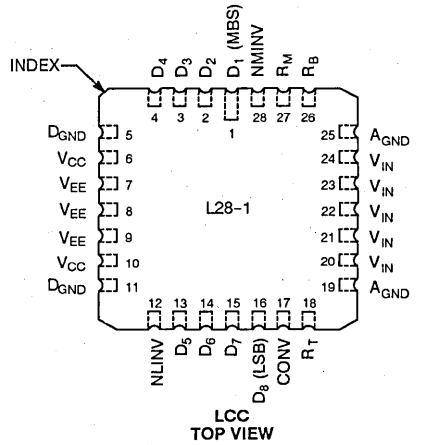


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP & SOIC TOP VIEW



LCC TOP VIEW

GENERAL INFORMATION

The IDT75C48 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 255 reference voltages to produce an N - of - 255 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on," while those with their reference above the input will be "off."

The reference voltage generator consists of a string of precisely matched resistors which generate the 255 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and -2V, respectively.

The encoding logic converts the "Thermometer" code into binary or offset two's complement numbers and can invert either code. Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C48 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = -5.2V and V_{CC} = +5.0V. Two separate grounds are provided, A_{GND} and D_{GND}, the analog and digital grounds. The difference between A_{GND} and D_{GND} must not exceed ±0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C48 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +2.1V to -2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = -2.0V.

The IDT75C48 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 5 shows a circuit which will provide approximately 1/2 LSB adjustment of the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, RT and RB should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommended.

CONTROL

The IDT75C48 provides two function control pins, NMINV and NLINV. These controls are for steady state use and are usually tied to the appropriate voltages. They control the output coding format in either straight binary or offset two's complement. In addition, both formats may be either true or inverted. These pins are active low and perform the functions shown in Figure 1.

CONVERT

The IDT75C48 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV and is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps.

If the maximum CONV pulse width HIGH time (t_{PWH}) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (t_{PWL}) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity,

The digital output data is presented at t_D, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the t_{HO} (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N+2.

ANALOG INPUT

The IDT75C48 uses strobed, auto-zeroing, latching comparators. All five analog input pins must be connected together as close to the package as possible.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal above V_{RT} will yield a full-scale positive output while an input below V_{RB} will cause a full-scale negative output.

11

STEP	RANGE		BINARY		OFFSET TWO'S	
	-2.0000V FS 7.8431mV/STEP	-2.0480V FS 8.000mV/STEP	NMINV=1 NLINV=1	NMINV=0 NLINV=0	NMINV=0 NLINV=1	NMINV=1 NLINV=0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	-0.0078V	-0.0080V	00000001	11111110	10000001	01111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
127	-0.9961V	-1.0160V	01111111	10000000	11111111	00000000
128	-1.0039V	-1.0240V	10000000	01111111	00000000	11111111
129	-1.0118V	-1.0320V	10000001	01111110	00000001	11111110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
254	-1.9921V	-2.0320V	11111110	00000001	01111110	10000001
255	-2.0000V	-2.0400V	11111111	00000000	01111111	10000000

Figure 1. Output Coding

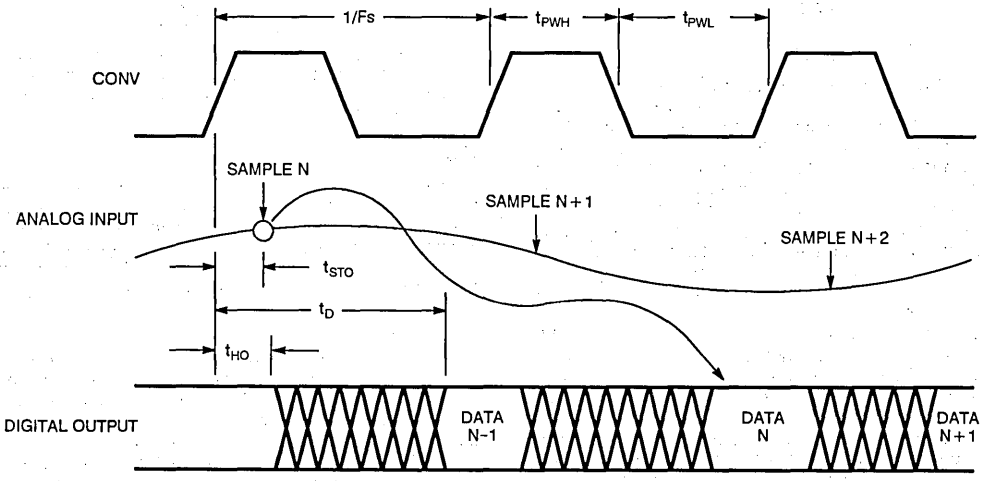


Figure 2. Timing Diagram

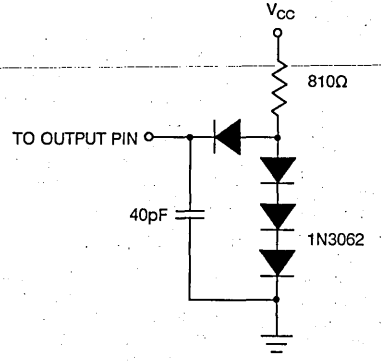


Figure 3. Output Load 1

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{CC}	Measured to D_{GND}	-0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	+0.5 to -7.0	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGE			
CONV, NMINV, NLINV	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
V_{IN} , V_{RT} , V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to V_{RB}	-4.0 to +4.0	V
OUTPUT			
Applied Voltage (2)	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	-3.0 to +6.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
POWER SUPPLY									
V_{CC}	Positive Power Supply		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply		-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})		-0.1	0	+0.1	-0.1	0	+0.1	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static(1)	–	50	70	–	60	80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static(1)	–	-25	-35	–	-25	-35	mA
DIGITAL INPUTS (CONV, NMINV, NLINV)									
V_{IL}	Input Voltage, Logic LOW(4)		-0.5	–	0.8	-0.5	–	0.8	V
V_{IH}	Input Voltage, Logic HIGH(4)		2.0	–	V_{CC} + .1	2.0	–	V_{CC} + .1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5 V	–	–	±10	–	–	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4 V	–	–	±10	–	–	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	–	–	50	–	–	50	µA
C_I	Digital Input Capacitance(4)	T_A = +25°C, F = 1 MHz	–	–	15	–	–	15	pF
DIGITAL OUTPUTS									
I_{OL}	Output Current, Logic LOW		–	–	4.0	–	–	4.0	mA
I_{OH}	Output Current, Logic HIGH		–	–	-2	–	–	-2	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min., I_{OL} = Max.	–	–	0.5	–	–	0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = Max.	2.4	–	–	2.4	–	–	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max.(2)	–	–	-50	–	–	-50	mA
REFERENCE									
V_{RT}	Most Positive Reference Voltage(3)		-0.1	0	+0.1	-0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage(3)		-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT} - V_{RB}$	Reference Voltage Range		1.8	2.0	2.2	1.8	2.0	2.2	V
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	–	5	9	–	6	10	mA
R_{REF}	Reference Resistance (R_T to R_B)	V_{RT}, V_{RB} = Nom.	250	400	–	200	330	–	Ohm
ANALOG INPUT									
V_{IN}	Input Voltage Range		V_{RB}	–	V_{RT}	V_{RB}	–	V_{RT}	V
R_{IN}	Equiv. Input Resistance(4)	V_{RT}, V_{RB} = Nom., V_{IN} = V_{RB}	100	–	–	100	–	–	KOhm
C_{IN}	Equiv. Input Capacitance(4)	V_{RT}, V_{RB} = Nom., V_{IN} = V_{RB}	–	–	50	–	–	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	–	–	10	–	–	10	µA
T_A	Ambient Temperature, Still Air		0	–	70	–	–	–	°C
T_C	Case Temperature		–	–	–	-55	–	+125	°C

NOTES:

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. V_{RT} must be more positive than V_{RB} and the voltage reference must be within the specified range. Although the device is specified and tested with the reference equal to 0V and -2V, the part will operate with V_{RT} up to +2.1V. Likewise, the reference range may vary from 1.2V to 2.6V.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C48 x 20 (20 MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	20	30	–	20	30	–	MSPS
t_{PWL}	CONV, Pulse Width Low[3]		18	–	100,000	18	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH[3]		22	–	20,000	22	–	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	0	–	10	0	–	15	ns
E_{AP}	Aperture Error[4]		–	–	60	–	–	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	–	–	30	–	–	35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	–	–	5	–	–	ns
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = Nom. 1/2 LSB[2]	–	–	0.2	–	–	0.2	%FS
		V_{RT}, V_{RB} = Nom. 3/4 LSB[2]	–	–	0.3	–	–	0.3	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom.	–	–	0.2	–	–	0.2	%FS
CS	Code Size[1]		25	100	175	25	100	175	%Nom
E_{OT}	Offset Error, Top	V_{IN} = midpoint of code 0	–	10	45	–	10	45	mV
E_{OB}	Offset Error, Bottom	V_{IN} = midpoint of code 255	–	-10	-30	–	-10	-30	mV
T_{CO}	Offset Error, Temperature Coefficient[4]	V_{IN} = V_{RB}	–	–	±20	–	–	±20	µV/°C
BW	Bandwidth, Full Power Input		7	12	–	5	10	–	MHz
T_{TR}	Transient Response, Full Scale[4]		–	–	20	–	–	20	nS
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10 MHz Bandwidth							
	Peak Signal/RMS Noise	1.248 MHz Input	54	56	–	53	55	–	dB
		2.438 MHz Input	53	56	–	52	55	–	dB
	RMS Signal/RMS Noise	1.248 MHz Input	45	47	–	44	46	–	dB
		2.438 MHz Input	44	47	–	43	46	–	dB
NPR	Noise Power Ratio	DC to 8 MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20 MSPS Conversion Rate	36.5	39	–	36.5	39	–	dB
DP	Differential Phase Error	F_S = 4 x NTSC	–	.5	1	–	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	–	1	2	–	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. No damage to the part will occur if Max. times are exceeded. See the Convert Section for more information about the Conv Max. time limitations.
4. This parameter is guaranteed but not tested in production.

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AC ELECTRICAL CHARACTERISTICS FOR IDT75C48 x 30 (30 MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	30	40	–	30	40	–	MSPS
t_{PWL}	CONV, Pulse Width Low		14	–	100,000	14	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH		14	–	20,000	14	–	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	0	–	10	0	–	15	ns
E_{AP}	Aperture Error[4]		–	–	60	–	–	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	–	–	25	–	–	28	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	–	–	5	–	–	ns
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = Nom. 3/4 LSB[2]	–	–	0.3	–	–	0.3	%FS
		V_{RT}, V_{RB} = Nom. 1 LSB[2]	–	–	0.4	–	–	0.4	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom.	–	–	0.2	–	–	0.2	%FS
CS	Code Size[1]		25	100	175	25	100	175	%Nom
E_{OT}	Offset Error, Top	V_{IN} = midpoint of code 0	–	10	45	–	10	45	mV
E_{OB}	Offset Error, Bottom	V_{IN} = midpoint of code 255	–	-10	-30	–	-10	-30	mV
T_{CO}	Offset Error, Temperature Coefficient[4]	V_{IN} = V_{RB}	–	–	±20	–	–	±20	µV/°C
BW	Bandwidth, Full Power Input		10	13	–	8	10	–	MHz
T_{TR}	Transient Response, Full Scale[4]		–	–	20	–	–	20	nS
SNR	Signal to Noise Ratio	30 MSPS Conversion Rate, 15 MHz Bandwidth							
	Peak Signal/RMS Noise	5 MHz Input	50	53	–	49	53	–	dB
		10 MHz Input	49	52	–	48	52	–	dB
	RMS Signal/RMS Noise	5 MHz Input	41	44	–	40	44	–	dB
		10 MHz Input	40	43	–	39	43	–	dB
NPR	Noise Power Ratio	DC to 15 MHz White Noise Bandwidth 4 Sigma Loading 5 MHz Slot 30 MSPS Conversion Rate	–	–	–	–	–	–	dB
DP	Differential Phase Error	F_S = 4 x NTSC	–	.5	1	–	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	–	1	2	–	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. No damage to the part will occur if Max. times are exceeded. See the Convert Section for more information about the Conv Max. time limitations.
4. This parameter is guaranteed but not tested in production.

CALIBRATION

The calibration of the IDT75C48 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done by varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to -2V reference range, apply -0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the converter output toggles between the codes of 0 and 1. To adjust the 255th comparator, apply -1.996V (1/2 LSB from -2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 254 and 255.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB} are specified in the AC Electrical Characteristics Table and indicate the degree of adjustment needed.

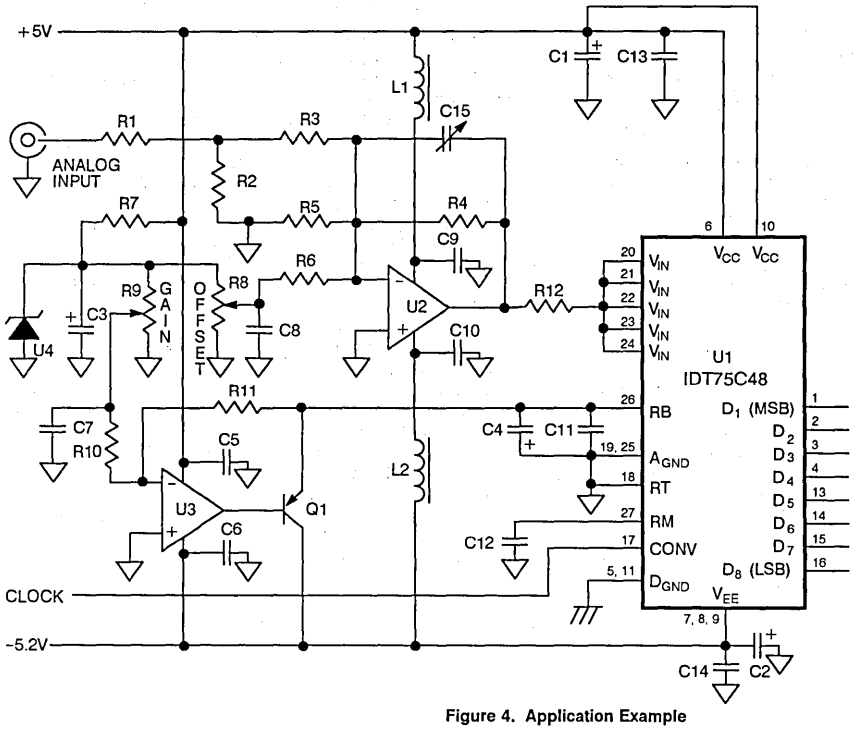
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e., be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, RT, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to RB. This is a preferred method for gain adjustment since it is not in the input signal path. See Figure 4 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 4 shows a typical application example for the IDT75C48. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p-p) to the recommended 2V converter input range. All five V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead length possible. Massive ground planes are recommended. If separate digital and analog ground planes are used, they should be connected together at one point close to the IDT75C48.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10µF
C5-C14	0.1µF
C15	1-6pF Variable
U1	IDT75C48
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 4. Application Example

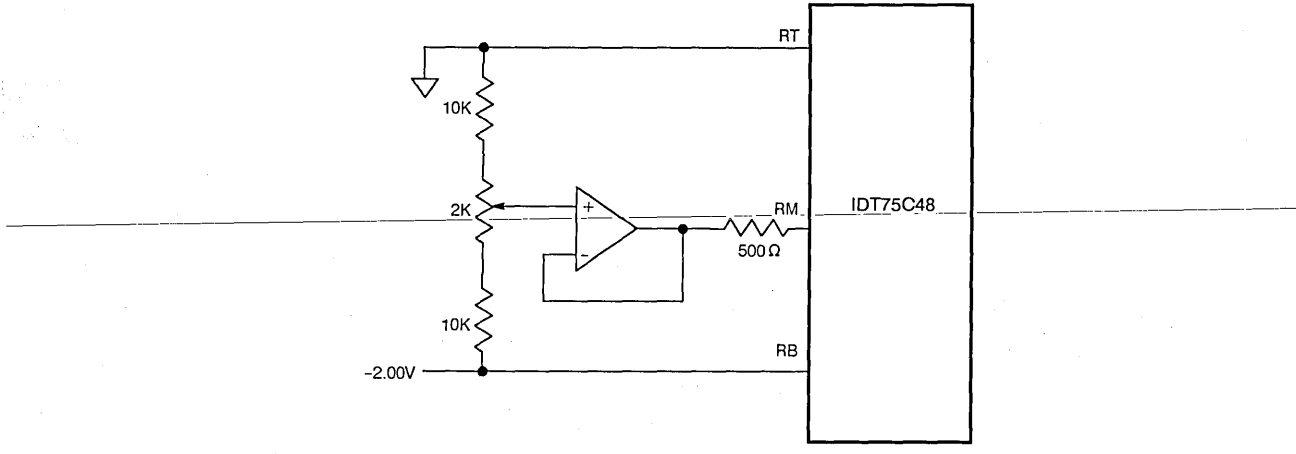
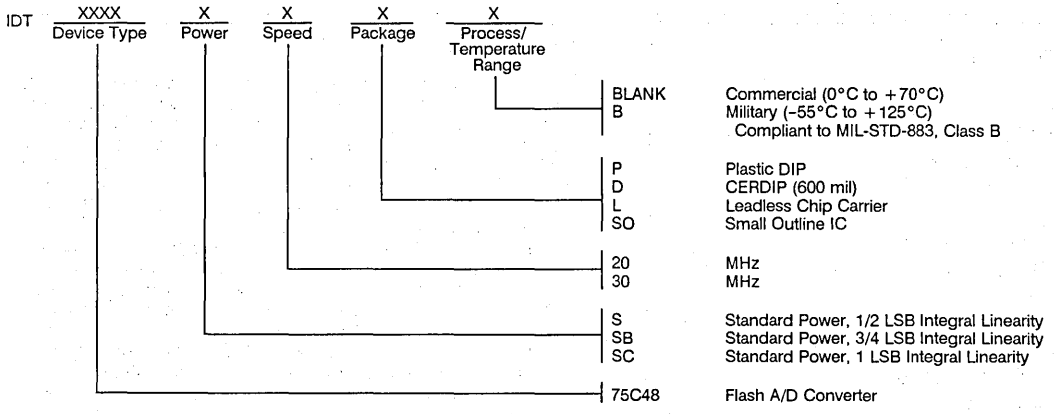


Figure 5. Mid-Point Adjust

ORDERING INFORMATION



11

Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT 75C58

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Overflow Output
- Low power consumption: 500mW
- Guaranteed no missing codes
- Power-Down mode
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Tri-state outputs
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase = 1 Degree
- Differential Gain = 2%
- TTL-compatible
- Available in 28-pin CERDIP and Plastic DIP or LCC
- Military product is compliant to MIL-STD-883, Class B

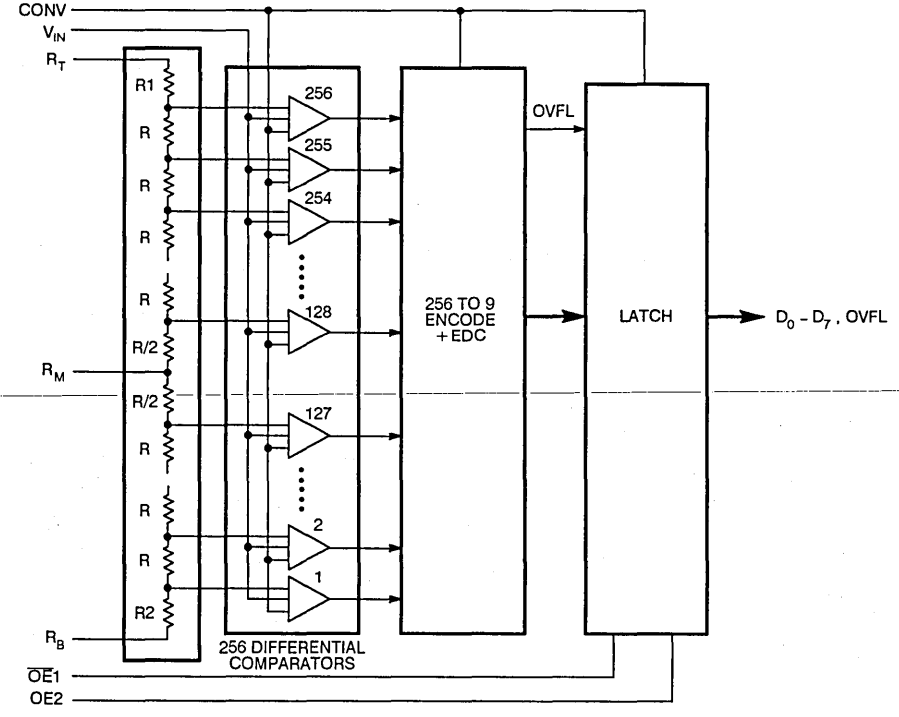
DESCRIPTION:

The IDT75C58 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing virtually eliminates thermal considerations. The IDT75C58 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C58 consists of a reference voltage generator, 256 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. An additional comparator detects an Overflow condition (V_{IN} more positive than Full-Scale + 1LSB) and activates the OVFL output. This output, together with two output enable inputs ($\overline{OE1}$ and OE2), allow the stacking of two IDT75C58s for 9-bit resolution with no external components.

The IDT75C58 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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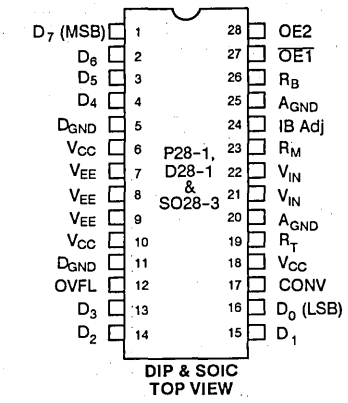
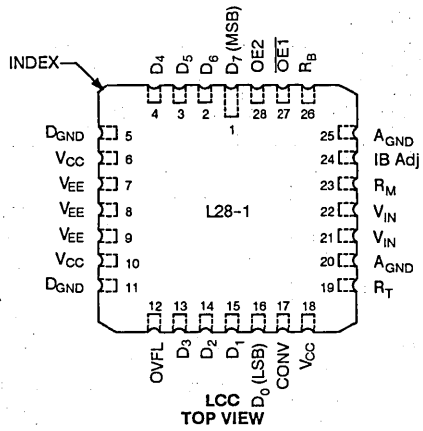
PIN CONFIGURATIONS



DIP & SOIC TOP VIEW



LCC TOP VIEW

GENERAL INFORMATION

The IDT75C58 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 256 reference voltages to produce an N - of - 256 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on" while those with their reference above the input will be "off".

The reference voltage generator consists of a string of precisely matched resistors which generate the 256 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and -2V, respectively.

Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C58 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = -5.0V and V_{CC} = +5.0V. Two separate grounds are provided, A_{GND} and D_{GND}, the analog and digital grounds. The difference between A_{GND} and D_{GND} must not exceed ± 0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C58 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +2.1V to -2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = -2.0V.

The IDT75C58 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 6 shows a circuit which will provide approximately 1/2 LSB adjustment to the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, R_T and R_B should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommended.

CONTROL

Two function control pins, $\overline{OE1}$ and OE2 control the outputs with the function shown in Table 1.

IB Adj

An analog control pin, IB Adj, controls the bias current in the comparators. Normally, this pin is connected to analog ground. To reduce the quiescent current, a "power-down" mode, IB Adj may be connected to V_{EE}. For somewhat better analog performance at higher input frequencies, IB Adj may be connected to a voltage between A_{GND} and V_{CC}.

CONVERT

The IDT75C58 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV. This is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps. If the maximum CONV pulse width HIGH time (t_{PWH}) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (t_{PWL}) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at t_D, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the t_{HO} (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N+2.

11

ANALOG INPUT

The IDT75C58 uses strobed, auto-zeroing, latching comparators. Both analog input pins must be connected together as close to the package as possible. The input signal must remain within the range of V_{CC} to V_{EE} to prevent damage to the device.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal below V_{RB} will yield a full-scale (all outputs low) output while an input above V_{RT} will cause an OVFL output.

STEP	RANGE		OUTPUT	OVFL
	-2.0000V FS 7.8125mV/Step	-2.0480V FS 8.000mV/Step		
256	0.0000V	0.0000V	11111111	1
255	-0.0078V	-0.0080V	11111111	0
254	-0.0156V	-0.0160V	11111110	0
⋮	⋮	⋮	⋮	⋮
129	-0.9961V	-1.0160V	10000000	0
128	-1.0039V	-1.0240V	01111111	0
127	-1.0118V	-1.0320V	01111110	0
⋮	⋮	⋮	⋮	⋮
001	-1.9921V	-2.040V	00000001	0
000	-2.0000V	-2.048V	00000000	0

Figure 1. Output Coding

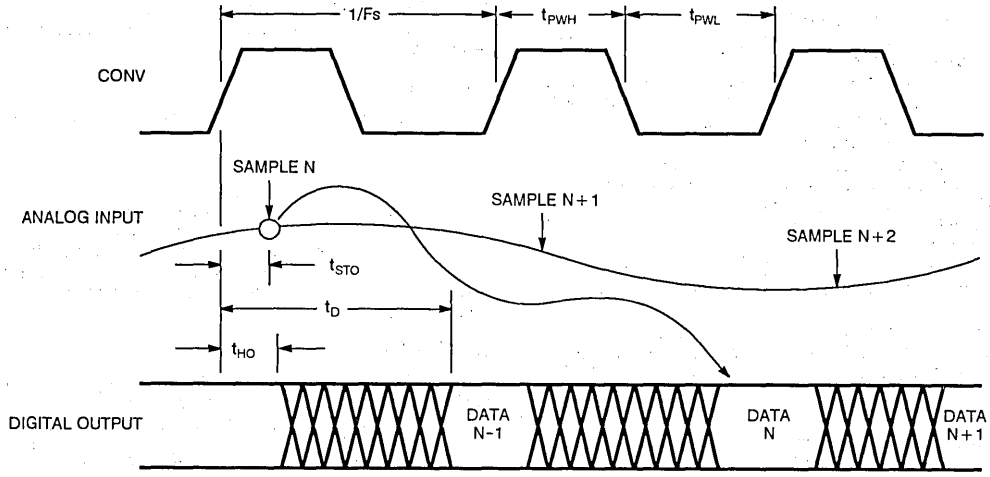


Figure 2. Timing Diagram

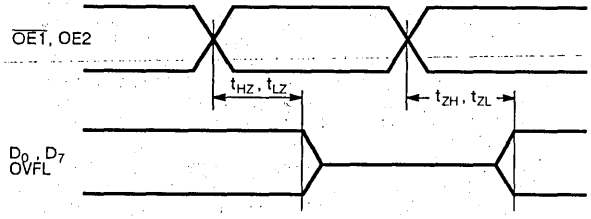


Figure 3. Output, Enable/Disable Timing

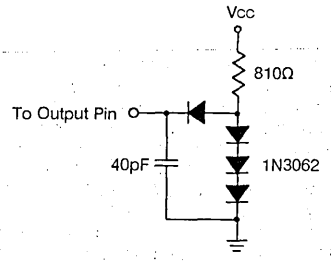


Figure 4. Output Load 1

$\overline{OE1}$	OE2	D_0 - D_7	OVFL
0	1	Valid	Valid
1	1	High Z	Valid
X	0	High Z	High Z

Table 1. Function Control

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{CC}	Measured to D_{GND}	-0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	-0.5 to -7.0	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGE			
CONV, $\overline{OE1}$, OE2	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
V_{IN} ,V_{RT},V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to V_{RB}	-4.0 to +4.0	V
OUTPUT			
Applied Voltage (2)	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	-3.0 to +6.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

11

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
POWER SUPPLY									
V_{CC}	Positive Power Supply		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply		-4.75	-5.2	-5.5	-4.5	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})		-0.1	0	+0.1	-0.1	0	+0.1	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static(1)	–	50	70	–	60	80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static(1)	–	-15	-25	–	-15	-25	mA
DIGITAL INPUTS (CONV, NMINV, NLINV)									
V_{IL}	Input Voltage, Logic LOW(4)		-0.5	–	0.8	-0.5	–	0.8	V
V_{IH}	Input Voltage, Logic HIGH(4)		2.0	–	V_{CC} + .1	2.0	–	V_{CC} + .1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5 V	–	–	±10	–	–	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4 V	–	–	±10	–	–	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	–	–	50	–	–	50	µA
C_I	Digital Input Capacitance(4)	T_A = +25°C, F = 1 MHz	–	–	15	–	–	15	pF
DIGITAL OUTPUTS									
I_{OL}	Output Current, Logic LOW	V_{CC} = Min., V_O = 0.4 V	–	–	4.0	–	–	4.0	mA
I_{OH}	Output Current, Logic HIGH	V_{CC} = Min., V_O = 2.4 V	–	–	-2	–	–	-2	mA
I_{OZ}	Output High Z Current(4)	V_{CC} = Max.	–	5	–	–	5	–	µA
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH}= Max.	2.4	–	–	2.4	–	–	V
V_{OL}	Output Voltage, Logic Low	V_{CC} = Min., I_{OL} = Max.	–	–	0.5	–	–	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max.(2)	–	–	-50	–	–	-50	mA
REFERENCE									
V_{RT}	Most Positive Reference Voltage(3)		-0.1	0	+0.1	-0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage(3)		-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT} - V_{RB}$	Reference Voltage Range		1.8	2.0	2.2	1.8	2.0	2.2	V
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	–	5	9	–	6	10	mA
R_{REF}	Reference Resistance (R_T to R_B)	V_{RT}, V_{RB} = Nom.	250	400	–	220	330	–	Ohm
ANALOG INPUT									
V_{IN}	Input Voltage Range		V_{RB}	–	V_{RT}	V_{RB}	–	V_{RT}	V
R_{IN}	Equiv. Input Resistance(4)	V_{RT}, V_{RB} = Nom., V_{IN} = V_{RB}	100	–	–	100	–	–	KOhm
C_{IN}	Equiv. Input Capacitance(4)	V_{RT}, V_{RB} = Nom., V_{IN} = V_{RB}	–	–	50	–	–	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	–	–	10	–	–	10	µA
T_A	Ambient Temperature, Still Air		0	–	70	–	–	–	°C
T_C	Case Temperature		–	–	–	-55	–	+125	°C

NOTES:

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. V_{RT} must be more positive than V_{RB} and the voltage reference must be within the specified range. Although the device is specified and tested with the reference equal to 0V and -2V, the part will operate with V_{RT} up to +2.1V. Likewise, the reference range may vary from 1.2V to 2.6V.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C58 x 20 (20 MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	20	30	–	20	30	–	MSPS
t_{PWL}	CONV, Pulse Width Low(4)		18	–	100,000	18	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH(4)		22	–	20,000	22	–	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	0	–	10	0	–	15	ns
E_{AP}	Aperture Error(5)		–	–	60	–	–	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	–	–	30	–	–	35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	–	–	5	–	–	ns
t_{HZ}	Output Disable Time from High(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	10	–	5	10	ns
t_{LZ}	Output Disable Time from Low(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	10	–	5	10	ns
t_{ZH}	Output Enable Time to High(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	18	–	12	–	ns
t_{ZL}	Output Enable Time to Low(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	18	–	12	18	ns
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = Nom. 1/2 LSB(2)	–	–	0.2	–	–	0.2	%FS
		V_{RT}, V_{RB} = Nom. 3/4 LSB(2)	–	–	0.3	–	–	0.3	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom.	–	–	0.2	–	–	0.2	%FS
CS	Code Size(1)		25	100	175	25	100	175	%Nom
E_{OT}	Offset Error, Top	V_{IN} = midpoint code 255	–	10	20	–	10	20	mV
E_{OB}	Offset Error, Bottom	V_{IN} = midpoint code 0	–	-10	-20	–	-10	-20	mV
E_{OO}	Offset Error, OVFL(3)	V_{IN} = V_{RT}	-6	0	6	-6	0	6	mV
T_{CO}	Offset Error, Temperature Coefficient(5)	V_{IN} = V_{RB}	–	–	±20	–	–	±20	µV/°C
BW	Bandwidth, Full Power Input		7	12	–	5	10	–	MHz
T_{TR}	Transient Response, Full Scale(5)		–	–	20	–	–	20	nS
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10 MHz Bandwidth							
	Peak Signal/RMS Noise	1.248 MHz Input	54	56	–	53	55	–	dB
		2.438 MHz Input	53	56	–	52	55	–	dB
	RMS Signal/RMS Noise	1.248 MHz Input	45	47	–	44	46	–	dB
		2.438 MHz Input	44	47	–	43	46	–	dB
NPR	Noise Power Ratio	DC to 10 MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20 MSPS Conversion Rate	36.5	39	–	36.5	39	–	dB
DP	Differential Phase Error	F_S = 4 x NTSC	–	.5	1	–	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	–	1	2	–	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. A 0mV offset means 1 LSB above the 255th code threshold.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

11

AC ELECTRICAL CHARACTERISTICS FOR IDT75C58 x 30 (30 MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE						UNIT
			COMMERCIAL			MILITARY			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	30	40	–	30	40	–	MSPS
t_{PWL}	CONV, Pulse Width Low(4)		14	–	100,000	14	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH(4)		14	–	20,000	14	–	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	0	–	10	0	–	15	ns
E_{AP}	Aperture Error(5)		–	–	60	–	–	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	–	–	25	–	–	28	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	–	–	5	–	–	ns
t_{HZ}	Output Disable Time from High(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	–	–	5	–	ns
t_{LZ}	Output Disable Time from Low(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	–	–	5	–	ns
t_{ZH}	Output Enable Time to High(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	–	–	12	–	ns
t_{ZL}	Output Enable Time to Low(5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	–	–	12	–	ns
E_{LI}	Linearity Error, Integral	V_{RT}, V_{RB} = Nom. 3/4 LSB(2)	–	–	0.3	–	–	0.3	%FS
		V_{RT}, V_{RB} = Nom. 1 LSB (2)	–	–	0.4	–	–	0.4	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom.	–	–	0.2	–	–	0.2	%FS
CS	Code Size(1)		25	100	175	25	100	175	%Nom
E_{OT}	Offset Error, Top	V_{IN} = midpoint code 255	–	10	45	–	45	20	mV
E_{OB}	Offset Error, Bottom	V_{IN} = midpoint code 0	–	-10	-30	–	-30	-20	mV
E_{OO}	Offset Error, OVFL(3)	V_{IN} = V_{RT}	-6	0	6	-6	0	6	mV
T_{CO}	Offset Error, Temperature Coefficient(5)	V_{IN} = V_{RB}	–	–	±20	–	–	±20	µV/°C
BW	Bandwidth, Full Power Input		10	13	–	8	10	–	MHz
T_{TR}	Transient Response, Full Scale(5)		–	–	20	–	–	20	nS
SNR	Signal to Noise Ratio	30 MSPS Conversion Rate, 15 MHz Bandwidth							
	Peak Signal/RMS Noise	5 MHz Input	50	53	–	49	53	–	dB
		10 MHz Input	49	52	–	48	52	–	dB
	RMS Signal/RMS Noise	5 MHz Input	41	44	–	40	44	–	dB
		10 MHz Input	40	43	–	39	43	–	dB
NPR	Noise Power Ratio	DC to 15 MHz White Noise Bandwidth 4 Sigma Loading 5 MHz Slot 30 MSPS Conversion Rate	–	–	–	–	–	–	dB
DP	Differential Phase Error	F_S = 4 x NTSC	–	.5	1	–	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	–	1	2	–	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. A 0mV offset means 1 LSB above the 255th code threshold.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

CALIBRATION

The calibration of the IDT75C58 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done by varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to -2V reference range, apply -0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the OVFL output toggles between 0 and 1. To adjust the first comparator, apply -1.996V (1/2 LSB from -2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 0 and 1.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on-chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB}, are specified in the AC Electrical Characteristics and indicate the degree of adjustment needed.

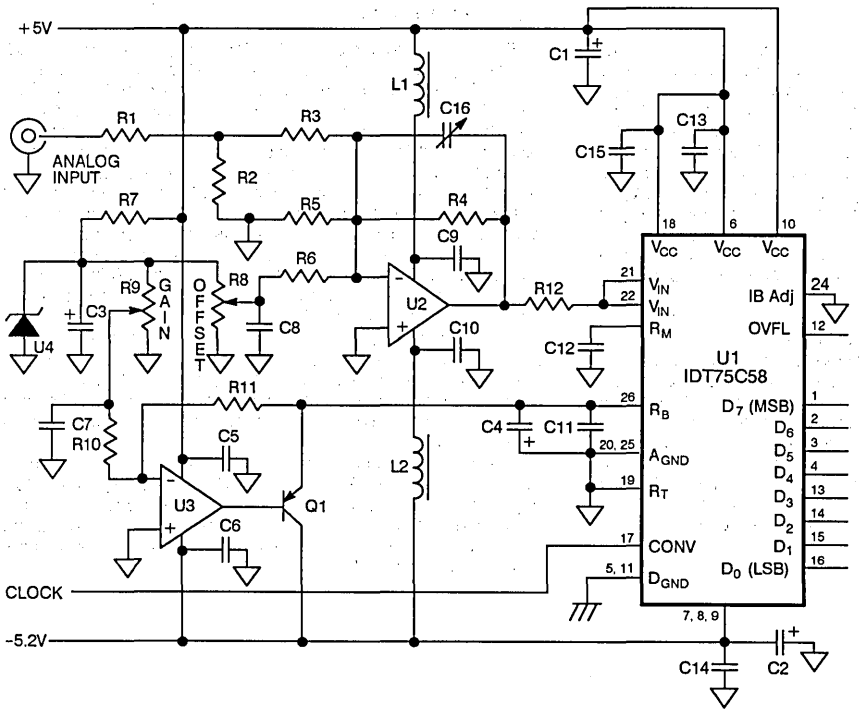
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e. be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, R_T, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error which can be compensated for by varying the voltage applied to R_B. This is a preferred method for gain adjustment since it is not in the input signal path. See Figure 5 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 5 shows a typical application example for the IDT75C58. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p-p) to the recommended 2V converter input range. Both V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead length possible. Massive ground planes are recommended. If separate digital and ground planes are used, they should be connected together at one point close to the IDT75C58.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10µF
C5-C15	0.1µF
C16	1-6pF Variable
U1	IDT75C58
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 5. Application Example

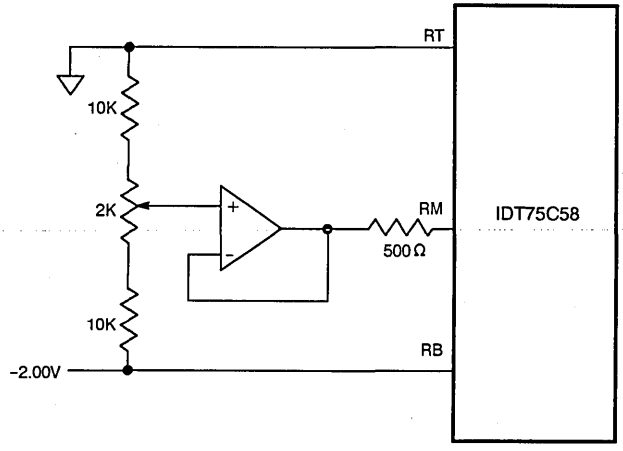


Figure 6. Mid-Point Adjust

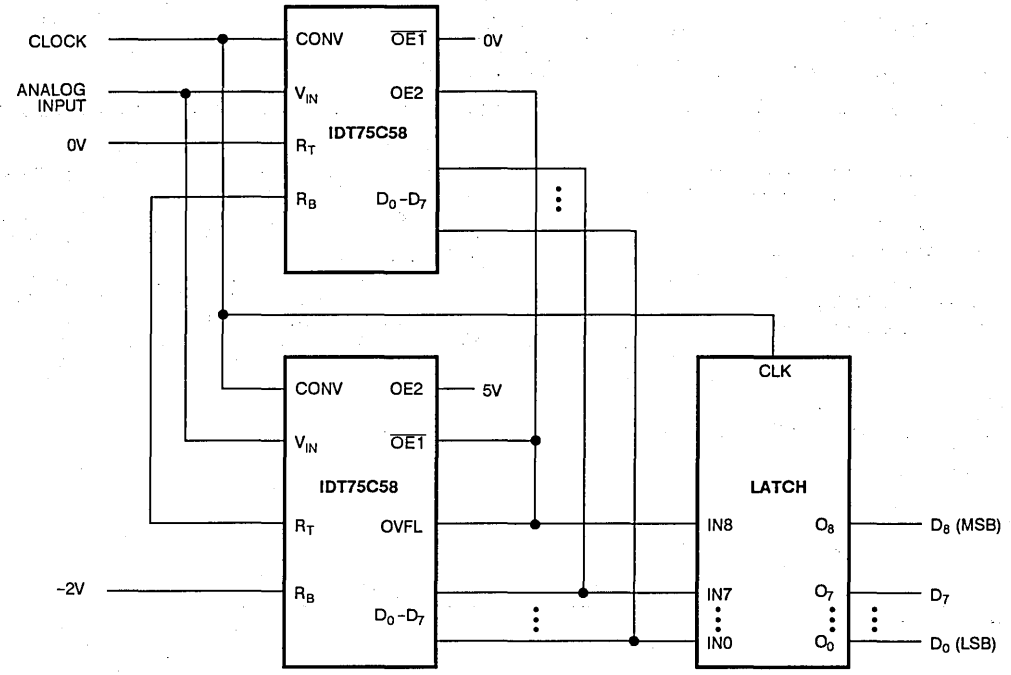
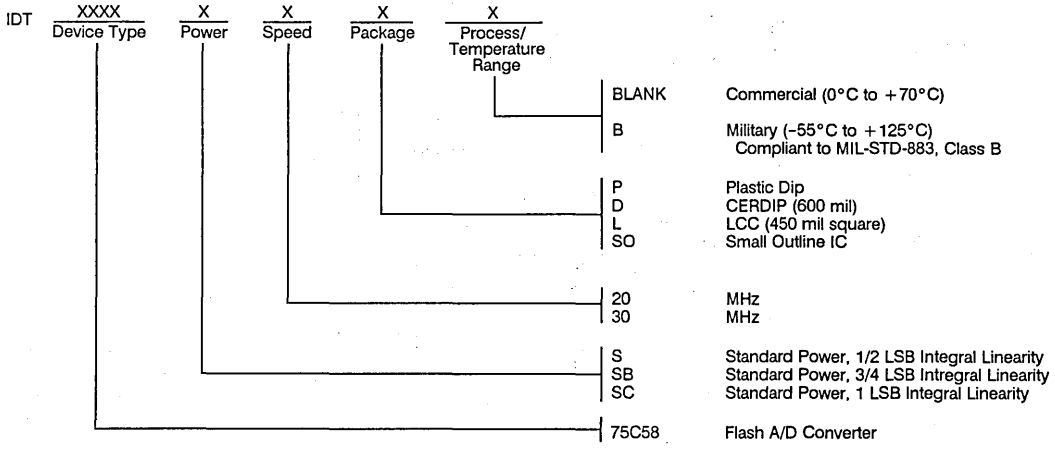


Figure 7. Simplified 9-Bit Application

ORDERING INFORMATION



Integrated Device Technology, Inc.

COMPLETE FLASH ADC DIGITIZING SYSTEM MODULE

PRELIMINARY
IDT 75MB58

FEATURES:

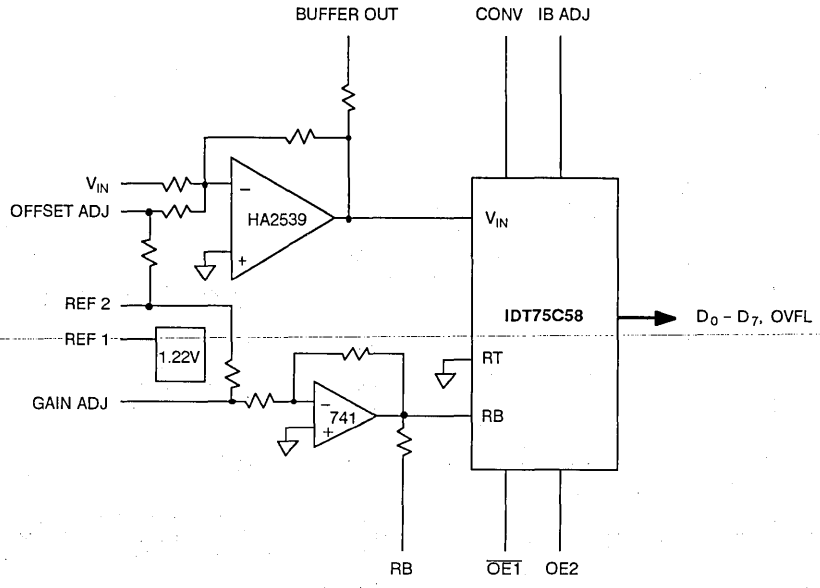
- Complete Analog to Digital Converter System
- No External Buffer Amplifier or S/H Required
- 20MHz Sampling Rate
- 10MHz Full Power Analog Input Bandwidth
- Pin Strappable Unipolar or Bipolar Input Ranges
- External Offset and Gain Adjust
- TTL Compatible, Three State Outputs
- Overflow Output Flag
- ±5V Power Supply Operation
- 1000mW Maximum Power Dissipation
- 24-pin, 600 mil Wide Plastic Module Construction

DESCRIPTION:

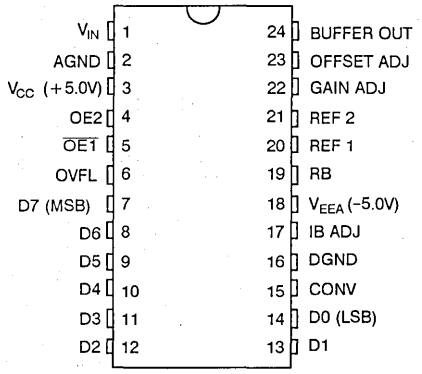
The IDT75MB58 is a complete, 20MSPS (Mega Samples per Second) Analog to Digital Converter subsystem. This module combines all of the components needed to digitize video speed analog signals (10MHz full-scale analog input bandwidth) into 8-bit digital words.

The IDT75MB58 module consists of a buffer amplifier, reference voltage generator and a 20MSPS Flash ADC all housed in surface-mount packages mounted on an FR4 plastic substrate. Combining all analog functions with the Flash ADC significantly reduces board space requirements as well as design costs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



24-PIN DIP
(TOP VIEW)

DESCRIPTION

The IDT75MB58 is a complete, 20MSPS (Mega Samples per Second) Analog to Digital Converter subsystem. This module combines all of the components needed to digitize video speed analog signals (10MHz full-scale analog input bandwidth) into 8-bit digital words.

The IDT75MB58 module consists of a buffer amplifier, reference voltage generator and a 20MSPS Flash ADC all housed in surface-mount packages mounted on an FR4 plastic substrate. Combining all analog functions with the Flash ADC significantly reduces board space requirements as well as design costs.

GENERAL INFORMATION

The IDT75MB58 consists of three functional blocks: The input buffer amplifier, the reference voltage generator and the Flash Analog to Digital Converter.

For more information about the Flash ADC and the input buffer amplifier, refer to the IDT75C58 and Harris HA2539 data sheets.

THEORY OF OPERATION

The input buffer amplifier has been designed to provide flat response up to ~10 MHz full scale frequency. The input impedance is set at ~1K Ohms with an input range of 0V to +1V. The output of the amplifier is available, through a 500Ω isolation resistor, as a test point or for application circuits.

An internal 1.22V bandgap voltage reference is available to derive the -2.00V for the Flash ADC's reference bottom (R_B) input. The actual voltage input to the R_B generator may be supplied externally to REF2, pin 21, but is usually strapped to the internal reference REF1, Pin 20.

The conversion range of the IDT75MB58 is set by the voltages applied to the top and bottom of the reference resistor ladder of the Flash ADC, R_T and R_B. R_T is internally connected to analog ground setting the top of the conversion range. R_B is connected to the reference generator as described above. The gain of the module is adjusted by varying V_{RB}.

A conversion is initiated on every rising edge of CLK. At this time a sample is taken of the buffered analog input signal. The 255 comparator outputs are latched and converted to binary code on the falling edge of CLK. Output data is presented, after a delay time, on the next rising edge of CLK. The easiest way to register the output data is on the third rising edge of CLK. The chip specifications guarantee a hold time for easy interface to an external register.

POWER

The IDT75C58 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = -5.0V and V_{CC} = +5.0V. Two separate ground pins are provided, AGND and DGND, however, they are internally connected. It is recommended that a one ground system be maintained and both AGND and DGND be connected together under the device. If a two ground system is used, the analog ground should be connected to AGND and the digital ground to DGND.

REFERENCE

The IDT75MB58 contains all circuitry needed to generate the negative reference voltage for the Flash ADC. A bandgap reference voltage, 1.22V, is available on REF1, pin 20. This voltage is usually strapped to the reference voltage generator input REF2, pin 21. The actual voltage applied to the Flash ADC is available on RB, pin 19, isolated by a 500Ω resistance and is typically -2.00V.

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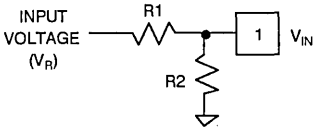
ANALOG INPUT

The analog input of the IDT75MB58 drives a buffer amplifier, configured with a gain of -2, which drives the Flash ADC. Typically, the analog input can accept either a unipolar 0 to +1V or bipolar ±0.5V input range. Other input ranges may be accommodated by attenuating the input signal as shown below. The equations to determine R1 and R2 are:



Input Attenuator

$$R2 = \frac{1}{\frac{V_R}{Z_{IN}} - \frac{1}{1000}}$$

$$R1 = ZIN - \frac{1000\ R2}{R2 + 1000}$$

Where V_R is the desired input voltage range, Z_{IN} is the desired input impedance and 1000±1% is the constant input resistance of the module.

Bipolar operation is obtained by leaving OFFSET ADJ, pin 23 open. Conversely, unipolar operation is possible with pin 23 connected to AGND. The OFFSET ADJ pin is also used to set the accuracy of the system. Please refer to the calibration section for more details.

The actual voltage applied to the Flash ADC is made available at BUFFER OUT, pin 24, through a 500Ω isolation resistor.

CONTROL

Two function control pins, $\overline{OE1}$ and OE2 control the outputs with the function shown in Table 1. These inputs determine the HI-Z status of the data outputs and OVFL.

IB ADJ

An analog control IB Adj, pin 17, controls the bias current in the comparators. Normally, this pin is connected to analog ground. To reduce the quiescent current, a "power-down" mode, IB ADJ may be connected to V_{EE}. For somewhat better analog performance at higher input frequencies, IB ADJ may be connected to a voltage between AGND and V_{CC}.

CONVERT

The IDT75MB58 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV. This is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short term uncertainty or jitter is less than 60ps. If the maximum CONV pulse width HIGH time (t_{PWH}) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (t_{PWL}) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at t_D, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the t_{HO} (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for sample N is acquired while the converter is taking sample N + 2.

CALIBRATION

The IDT75MB58 provides controls for adjusting the gain and offset of the system. OFFSET ADJ, pin 23, varies the DC level of the input buffer amplifier. When this pin is left open, a -0.5V offset is introduced into the buffer amplifier allowing a ±0.5V bipolar input signal to correctly drive the Flash ADC (translating the signal to a 0V to -2V range). When the OFFSET ADJ pin is connected to AGND, no offset is introduced, accomodating a 0V to 1V unipolar input signal. The OFFSET ADJ pin can also be used to adjust the DC accuracy of the Flash Modules. Two methods for trimming unipolar offset are shown in Figure 1. The simpler method, shown in Fig. 1a), depends on the absolute resistor stability over temperature. A more elegant approach, shown in b) reduces self-heating and dissipates less power.

Offset trim for Bipolar input signals is simpler and is shown in Fig. 2. The range of adjustment is ± 75mV or approximately 19LSB.

GAIN ADJ, pin 22, varies the voltage applied to the reference resistor ladder of the Flash ADC, effectively varying the gain of the system. Note that larger gain decreases may be obtained by padding the analog input. A typical circuit for gain adjustment is shown in Figure 3 while a more stable circuit is shown in Figure 4.

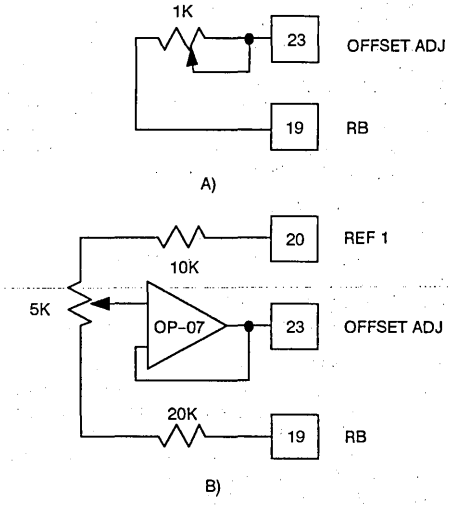


Figure 1. Unipolar Offset Adjust Circuit

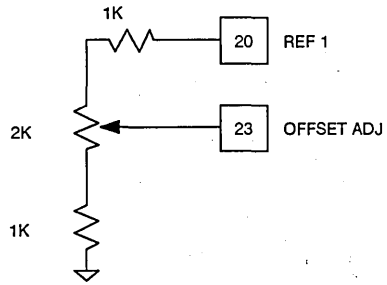


Figure 2. Bipolar Offset Adjust Circuit

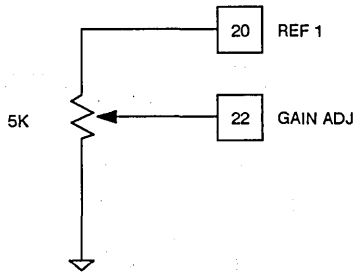


Figure 3. Gain Adjust Circuit

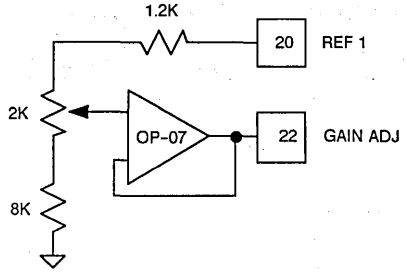


Figure 4. Gain Adjust Circuit (±10%)

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STEP	RANGE		OUTPUT	OVFL
CODE CENTERS	BIPOLAR ±0.5V FS 3.90mV/Step	UNIPOLAR 0 TO +1V FS 3.90mV/Step		
256	-0.5000V	0.0000V	11111111	1
255	-0.4961V	0.0039V	11111111	0
254	-0.4922V	0.0078V	11111110	0
129	-0.0039V	0.4961V	10000000	0
128	0.0000V	0.5000V	01111111	0
127	0.0039V	0.5039V	01111110	0
001	0.4961V	0.9961V	00000001	0
000	0.5000V	1.0000V	00000000	0

Figure 5. Output Coding

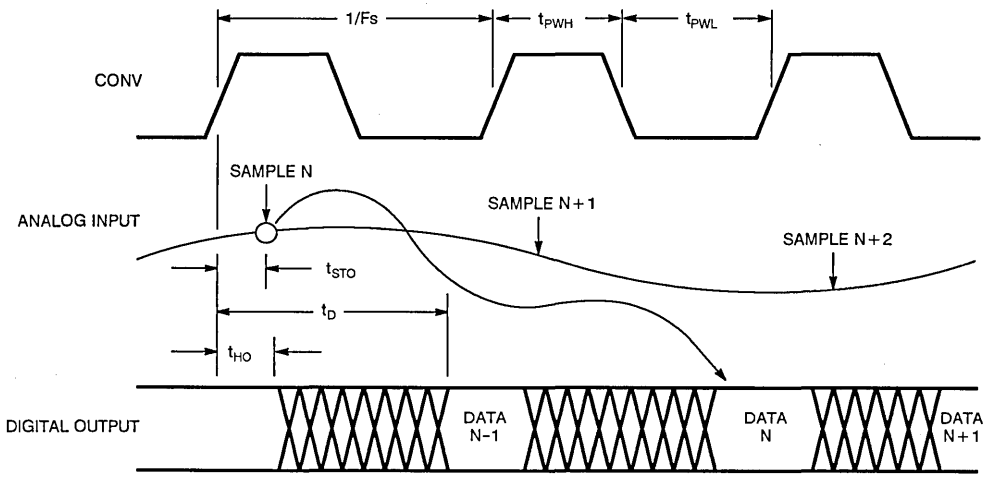

Figure 6. Timing Diagram

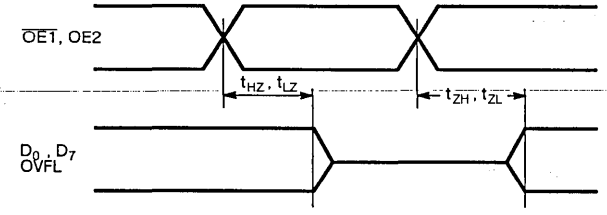

Figure 7. Output, Enable/Disable Timing

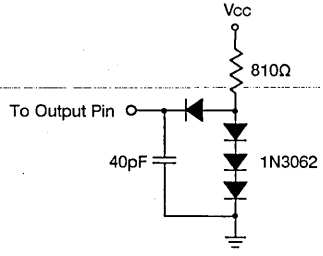

Figure 8. Output Load 1

$\overline{OE1}$	OE2	D_0 - D_7	OVFL
0	1	Valid	Valid
1	1	High Z	Valid
X	0	High Z	High Z

Table 1. Function Control

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLY			
V_{CC}	Measured to A_{GND}	-0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	+0.5 to -7.0	V
INPUT VOLTAGE			
CONV, $\overline{OE1}$, OE2	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
V_{IN} , REF2	Measured to A_{GND}	V_{CC} to V_{EE}	V
OUTPUT			
Applied Voltage (2)	Measured to D_{GND}	-0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	-3.0 to +6.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
TEMPERATURE			
Operating, Ambient	Commercial	0 to +70	°C
Storage	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL MIN.	NOM.	MAX.	UNIT
POWER SUPPLY						
V_{CC}	Positive Power Supply		4.75	5.0	5.25	V
V_{EE}	Negative Power Supply		-4.75	-5.0	-5.5	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static (1)	–	–	110	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static (1)	–	–	-70	mA
DIGITAL INPUTS (CONV, $\overline{OE1}$, OE2)						
V_{IL}	Input Voltage, Logic LOW (3)		-0.5	–	0.8	V
V_{IH}	Input Voltage, Logic HIGH (3)		2.0	–	V_{CC}+.1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5 V	–	–	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4 V	–	–	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	–	–	50	µA
C_I	Digital Input Capacitance (3)	T_A = +25°C, F = 1 MHz	–	–	15	pF
DIGITAL OUTPUTS						
I_{OL}	Output Current, Logic LOW	V_{CC} = Min., V_O = 0.4 V	–	–	4.0	mA
I_{OH}	Output Current, Logic HIGH	V_{CC} = Min., V_O = 2.4 V	–	–	-2	mA
I_{OZ}	Output High Z Current (3)	V_{CC} = Max.	–	5	–	µA
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = Max.	2.4	–	–	V
V_{OL}	Output Voltage, Logic Low	V_{CC} = Min., I_{OL} = Max.	–	–	0.5	V
REFERENCE						
V_{REF1}	Internal Reference Voltage		1.22	1.235	1.25	V
I_{REF1}	Reference Source Current		–	–	2.0	mA
V_{RB}	RB Voltage Range		-1.8	-2.0	-2.2	V
ANALOG INPUT						
V_{IN}	Input Voltage Range	OFFSET ADJ Pin Open	-0.5		+0.5	V
R_{IN}	Input Resistance (3)		985	1000	1015	KOhm
C_{IN}	Input Capacitance (3)	V_{RT}, V_{RB} = Nom., V_{IN} = V_{RB}			5	pF
T_A	Ambient Temperature, Still Air		0	–	70	°C

NOTES:

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS

Specifications over the DC Electrical range unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	TEMPERATURE RANGE COMMERCIAL			UNIT
			MIN.	TYP.	MAX.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	20	30	–	MSPS
t_{PWL}	CONV, Pulse Width Low (4)		18	–	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH (4)		22	–	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	-5	–	15	ns
E_{AP}	Aperture Error (5)		–	–	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	–	–	30	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	–	–	ns
t_{HZ}	Output Disable Time from High (5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	10	
t_{LZ}	Output Disable Time from Low (5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	5	10	ns
t_{ZH}	Output Enable Time to High (5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	18	ns
t_{ZL}	Output Enable Time to Low (5)	V_{CC} = Min., V_{EE} = Min., Load 1	–	12	18	ns
E_{LI}	Linearity Error, Integral	V_{RB} = Nom.	–	0.2	–	%FS
E_{LD}	Linearity Error, Differential	V_{RB} = Nom.	–	0.2		%FS
CS	Code Size (1)		25	100	175	%Nom
E_{OSB}	Offset Error, Bipolar, Unadjusted		-75	–	+75	mV
E_{OSU}	Offset Error, Unipolar, Unadjusted		-60	–	+60	mV
E_{OO}	Offset Error, OVFL (3)	V_{IN} = V_{RT}	-6	0	6	mV
BW	Bandwidth, Full Power Input		10	12	–	MHz
E_G	Gain Error, Unadjusted		-8	–	+8	%FS
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10 MHz Bandwidth				
	RMS Signal/RMS Noise	2.5 MHz Input 5 MHz Input	44 43	47 47	– –	dB dB
NPR	Noise Power Ratio	DC to 10 MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20 MSPS Conversion Rate	36.5	39	–	dB
DP	Differential Phase Error	F_S = 4 x NTSC	–	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	–	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. A 0mV offset means 1 LSB above the 255th code threshold.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

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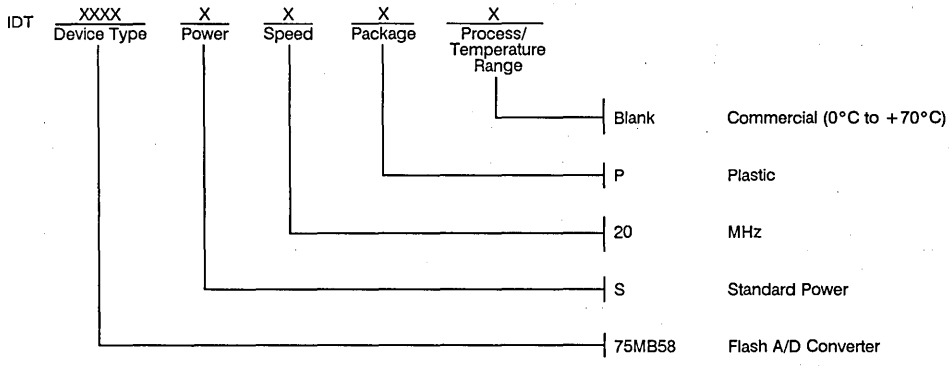
ORDERING INFORMATION



INTRODUCTION TO THE ECL PRODUCTS GROUP

The ECL Product Group is one of the newest product groups to be created at Integrated Device Technology, Inc. The charter of the group is to develop a leadership BiCMOS technology, create ECL-compatible products which drive and showcase that technology, and understand the needs of ECL users with the aim of creating products which more completely provide systems solutions.

The products offered by the ECL Products Group provide the designer of high-speed emitter-coupled logic (ECL) systems with a lower-power alternative to older bipolar ECL technologies. IDT BiCMOS ECL memory products allow the designer to achieve performance levels close to bipolar equivalents, yet with less engineering time and resources devoted to heat dissipation and thermal design. These products are ideal for cache, control-store, or main memory applications in mini-supercomputer and high-end workstation, or pattern generation and data capture in test equipment.

This revolution in performance-density is achieved by IDT through the development of a technology which combines high-speed CMOS with limited use of bipolar structures. Called BiCEMOS™, the technology provides greater performance in memory components by speeding up word-line drivers, sense amplifiers, and input-output buffers. Bipolar structures on-chip also allow the option of ECL-compatible interfaces.

To build components with ECL interfaces in the past required 100% bipolar circuit designs. Full bipolar designs were limited in density, however, by the high power dissipation of the chip: the level of integration available to the designer of ECL systems has thus been necessarily low when compared to CMOS. But in the past, designers looking for performance sacrificed density and solved power dissipation engineering problems in order to use bipolar ECL components. Today, BiCMOS provides the high-density and low cost of CMOS to ECL designers.

Integrated Device Technology has begun its family of BiCMOS ECL components with the most density-intensive elements: memory. Because memories benefit in speed from bipolar word-line drivers as mentioned above, larger (longer word-line) memories benefit most from BiCMOS. Thus, IDT has begun building BiCMOS ECL SRAMs at the 64K-bit density, and will offer products with ever greater levels of integration. These density enhancements will include 256K-bit memories and beyond, as well as memories including on-chip logic to improve their use in computer architectures.

The speed of memories, measured as access time, is also improved with the development of BiCMOS. Bipolar structures speed up internal elements of already fast CMOS memories. Because it is based on, and integrated into, standard IDT CMOS, BiCMOS will directly receive the benefits of enhancements made in future CMOS technology generations. Speed improvements will be achieved for both BiCMOS TTL and BiCMOS ECL memories, but the ECL output buffer is a clear speed leader over TTL, implying that ECL memories will in general out-perform TTL. In a system, ECL logic elements out-perform TTL by as much as a factor of three; IDT feels that ECL will win renewed interest as an interconnect standard for high-performance systems now that BiCMOS allows CMOS densities at ECL speeds.

Military applications will also benefit from BiCMOS ECL components. The low-power dissipation of BiCMOS allows ECL SRAMs to be offered as fuly MIL-STD-883 compliant over the full -55°C to +125°C temperature range. The high density and low power will be ideal for high data rate applications such as RADAR, satellite communication, and graphics.

The lower power dissipation of BiCMOS ECL components makes the job of designing with ECL much easier than with bipolar ECL. System reliability goals are much easier to achieve because these components create less heat in a system. Heat dissipation techniques needed for system cooling benefit from a better starting point, reducing the amount of time and resources needed to prove a design. Power supply requirements are of course reduced. New packaging options are realized, such as plastic DIP and surface-mount packages.

Integrated Device Technology believes that BiCMOS will be a major technology for the coming years, and is dedicated to be the leader. To do this we have created memory products to drive the technology down the learning curve to provide our customers cost-effective high-performance. We offer standard and leadership ECL products implemented in high-performance BiCMOS. We intend to work closely with our customers to create new standard products which bring more of the advantages of BiCMOS speed, integration, and lower power to ECL systems.

BiCEMOS is a trademark of Integrated Device Technology, Inc.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT 10490

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 420mW (typ.)
- Fully compatible with 10K logic level
- Address access time: 8/10/12/15/20ns (max.)
- Write pulse width: 6ns (min.)
- Separate data input and output
- JEDEC standard high-density 22-pin CERDIP

DESCRIPTION:

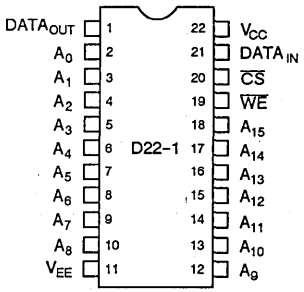
The IDT10490 is a 10K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1.

The IDT10490 is available with address access times as fast as 8ns with a typical power consumption of only 420mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

Designed for very high-speed applications, the IDT10490 is fully compatible with standard ECL 10K logic levels and offers extremely fast access times. The address access time of 8ns and write pulse width of 6ns assure that operations of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

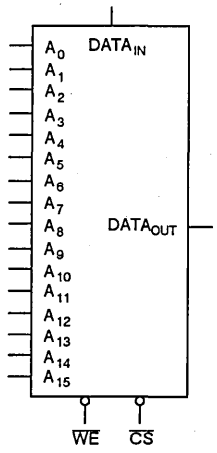
The IDT10490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

PIN CONFIGURATIONS

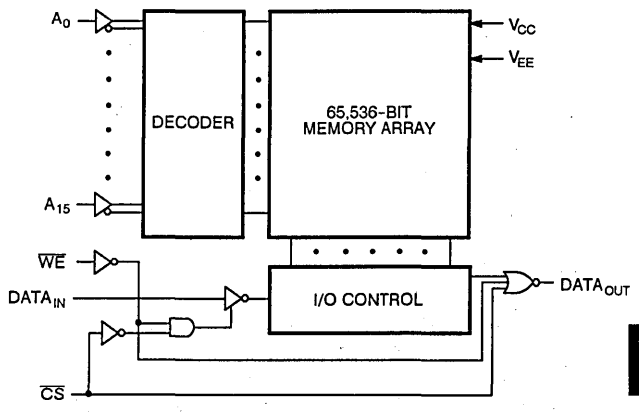


DIP
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +75	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H = High, L = Low, X = Don't Care

DC ELECTRICAL CHARACTERISTICS

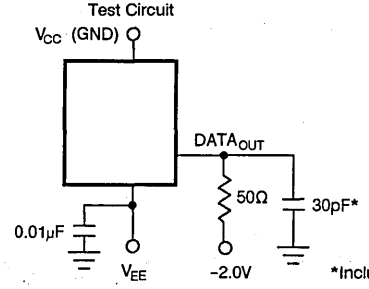
(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-855	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-140	-80	–	mA	

NOTE:

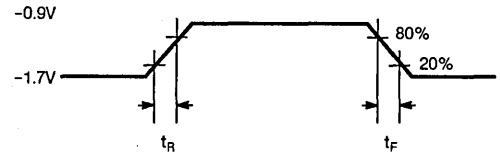
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE

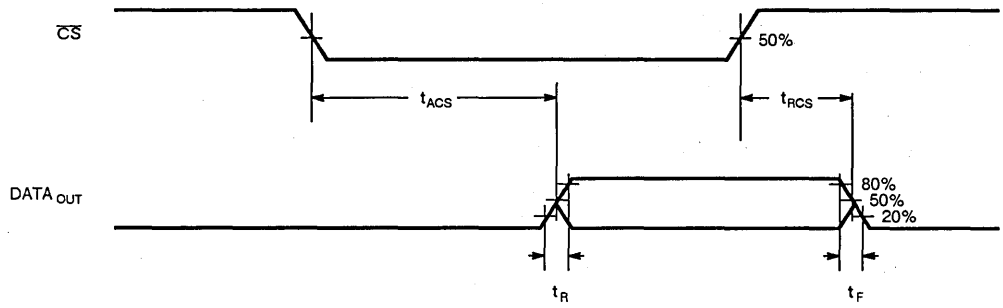


t_R = t_F = 2.0ns typ.

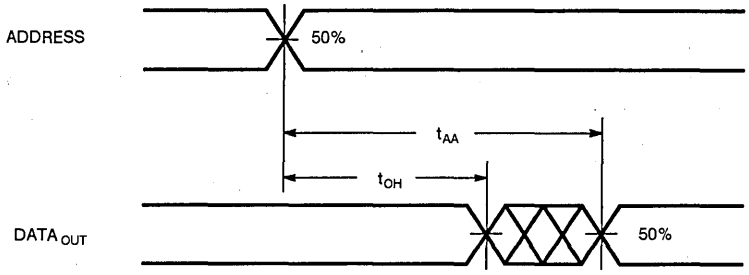
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10490S8 MIN.	IDT10490S8 MAX.	IDT10490S10 MIN.	IDT10490S10 MAX.	IDT10490S12 MIN.	IDT10490S12 MAX.	IDT10490S15 MIN.	IDT10490S15 MAX.	IDT10490S20 MIN.	IDT10490S20 MAX.	UNIT
READ CYCLE													
t_{ACS}	Chip Select Access Time	–	–		–	5	–	5	–	10	–	10	ns
t_{RCS}	Chip Select Recovery Time	–	–		–	5	–	5	–	10	–	10	ns
t_{AA}	Address Access Time	–	–	8	–	10	–	12	–	15	–	20	ns
t_{OH}	Data Hold from Address Change	–	3	–	3.5	–	3.5	–	3.5	–	3.5	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT10490 MIN.	IDT10490 TYP.	IDT10490 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

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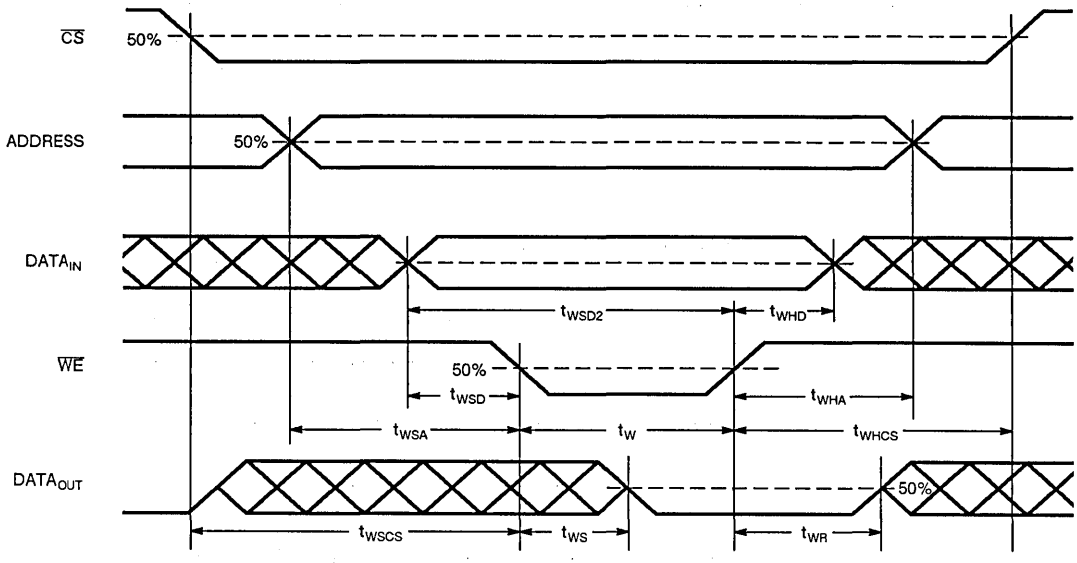
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10490S8 MIN.	IDT10490S8 MAX.	IDT10490S10 MIN.	IDT10490S10 MAX.	IDT10490S12 MIN.	IDT10490S12 MAX.	IDT10490S15 MIN.	IDT10490S15 MAX.	IDT10490S20 MIN.	IDT10490S20 MAX.	UNIT
WRITE CYCLE													
t_W	Write Pulse Width	t_{WSA} = minimum	6	–	8	–	10	–	10	–	15	–	ns
t_{WSD}	Data Set-up Time	–	0	–	0	–	0	–	2	–	3	–	ns
t_{WSD2}(1)	Data Set-up to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	7	–	ns
t_{WHD}	Data Hold Time	–	2	–	2	–	2	–	3	–	4	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum		–	0	–	0	–	2	–	3	–	ns
t_{WHA}	Address Hold Time	–		–	2	–	2	–	3	–	4	–	ns
t_{WSCS}	Chip Select Set-up Time	–		–	0	–	0	–	2	–	3	–	ns
t_{WHCS}	Chip Select Hold Time	–		–	2	–	2	–	3	–	4	–	ns
t_{WS}	Write Disable Time	–		–	–	5	–	5	–	10	–	10	ns
t_{WR}(2)	Write Recovery Time	–		–	–	12	–	14	–	18	–	23	ns

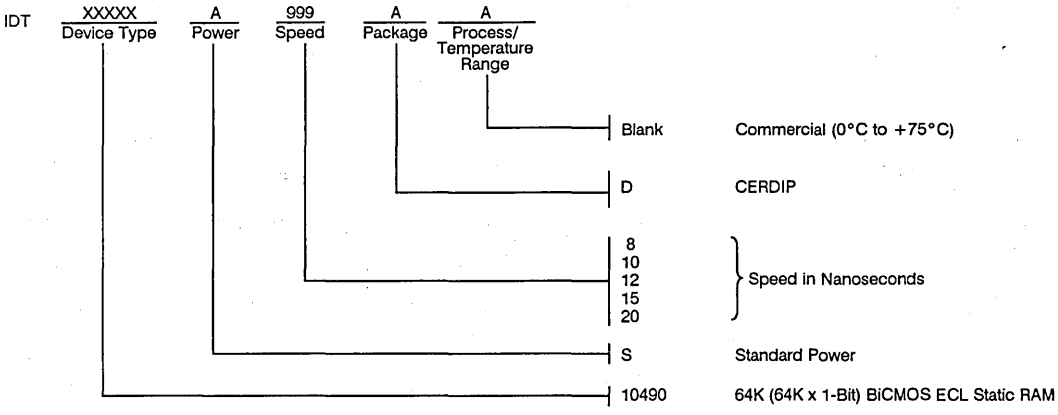
NOTES:

1. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. $t_{WR} = t_{WHA} + t_{AA}$ and thus can include a full access time if addresses change while Chip Select is still low.

TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT) MIL-STD-883 COMPLIANT

PRELIMINARY
IDT 10490M

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 420mW (typ.)
- Fully compatible with 10K logic level
- Address access time: 15/20ns (max.)
- Write pulse width: 10ns (min.)
- Separate data input and output
- JEDEC standard high-density 22-pin CERDIP
- Mil-STD-883 Compliant
- Operation over the full temperature range -55°C to + 125°C

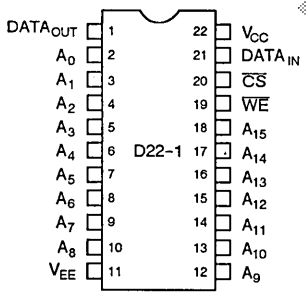
DESCRIPTION:

The IDT10490 is a 10K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1. It is manufactured, assembled, and tested by Integrated Device Technology, Inc. in full compliance with MIL-STD-883, and operates over the full temperature range of -55°C to + 125°C.

The IDT10490 is available with address access times as fast as 15ns with a typical power consumption of only 420mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to achieve a high-performance ECL system with dramatically lower power dissipation than bipolar equivalents, reducing power supply and cooling requirements.

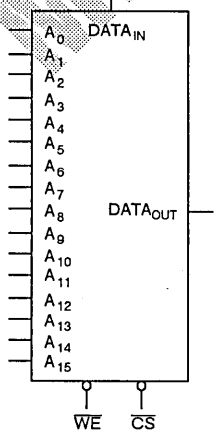
Designed for very high-speed applications, the IDT10490 is fully compatible with standard ECL 10K logic levels and offers extremely fast access times. Applications include cache, control store, buffer, and main memory uses. The high density allows fewer address-decode delays, providing better system speed over smaller ECL memories.

PIN CONFIGURATIONS

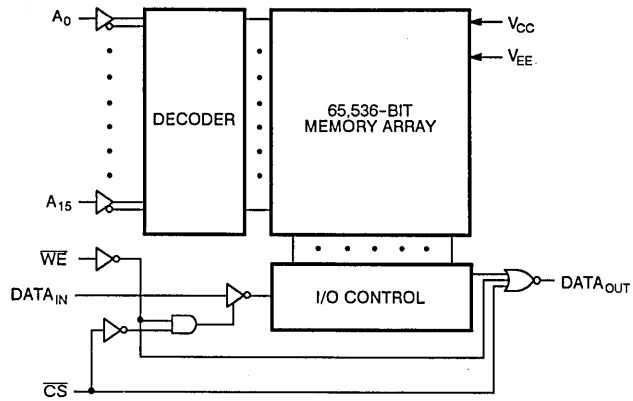


DIP
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H = High, L = Low, X = Don't Care

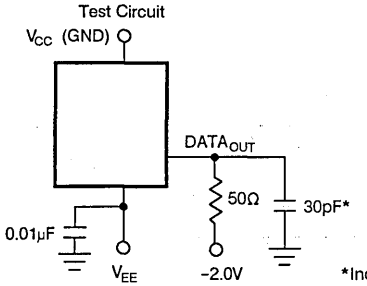
DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = -55 to +125°C for DIP, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1070 -960 -860	-855	-860 -810 -600	mV	-55°C 25°C +125°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1900 -1850 -1800	–	-1690 -1650 -1570	mV	-55°C 25°C +125°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1090 -980 -830	–	–	mV	-55°C 25°C +125°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1670 -1630 -1550	mV	-55°C 25°C +125°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1213 -1105 -1005	–	-860 -810 -600	mV	-55°C 25°C +125°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1900 -1850 -1800	–	-1515 -1475 -1395	mV	-55°C 25°C +125°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-140	-80	–	mA	

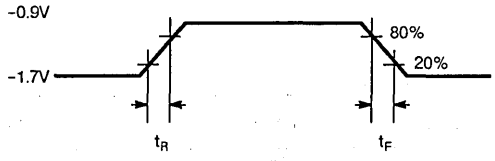
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE



t_R = t_F = 2.0ns typ.

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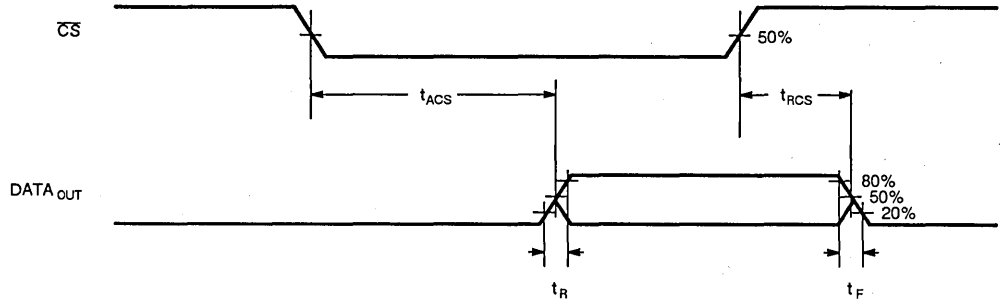
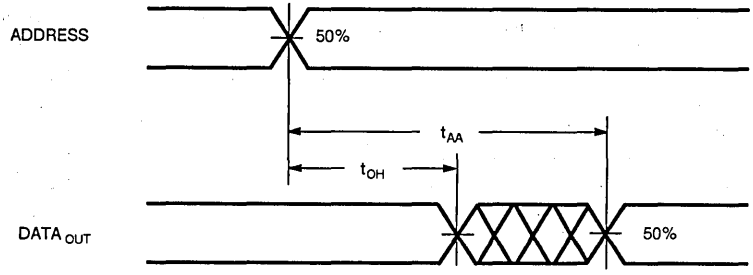
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = -55 to +125°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10490S15 MIN.	IDT10490S15 MAX.	IDT10490S20 MIN.	IDT10490S20 MAX.	UNIT
READ CYCLE							
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{AA}	Address Access Time	–	–	15	–	20	ns
t_{OH}	Data Hold from Address Change	–	3.5	–	3.5	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT10490 MIN.	IDT10490 TYP.	IDT10490 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

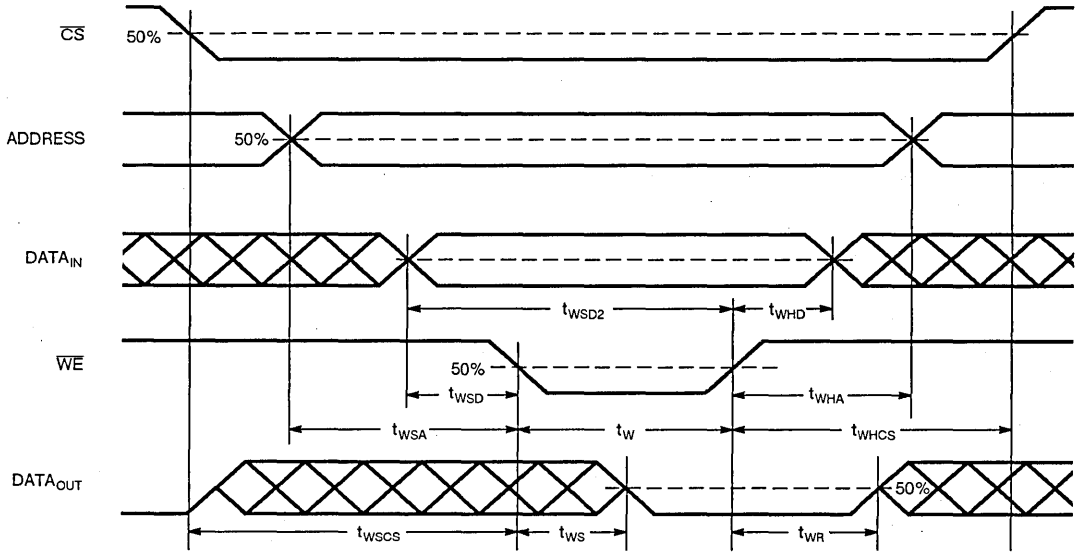
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = -55 to +125°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10490S15 MIN.	IDT10490S15 MAX.	IDT10490S20 MIN.	IDT10490S20 MAX.	UNIT
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	13	–	ns
t_{WSD}	Data Set-up Time	–	2	–	3	–	ns
t_{WSD2}	Data Set-up to $\overline{WE}$ high	–	5	–	7	–	ns
t_{WHD}	Data Hold Time	t_W = minimum	3	–	4	–	ns
t_{WSA}	Address Set-up Time		2	–	3	–	ns
t_{WHA}	Address Hold Time	–	3	–	4	–	ns
t_{WSCS}	Chip Select Set-up Time	–	2	–	3	–	ns
t_{WHCS}	Chip Select Hold Time	–	3	–	4	–	ns
t_{WS}	Write Disable Time	–	–	10	–	10	ns
t_{WR}(1)	Write Recovery Time	–	–	18	–	23	ns

NOTE:

1. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. t_{WR} is defined as the time to reflect newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.

TIMING WAVEFORM OF WRITE CYCLE



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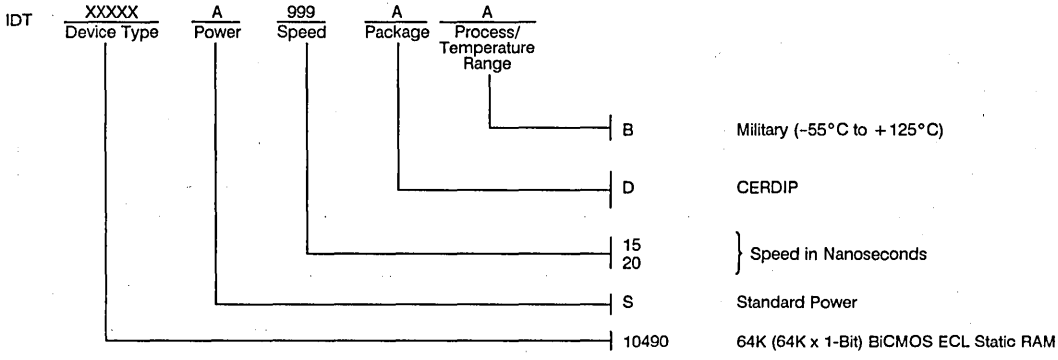
ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT)

PRELIMINARY
IDT 100490

FEATURES:

- 65,536-words x 1-bit organization
- Low power dissipation: 320mW (typ.)
- Fully compatible with 100K logic level
- Address access time: 8/10/12/15/20ns (max.)
- Write pulse width: 6ns (min.)
- Separate data input and output
- JEDEC standard high-density 22-pin plastic DIP and CERDIP and 24-pin Small Outline J-Bend IC

DESCRIPTION:

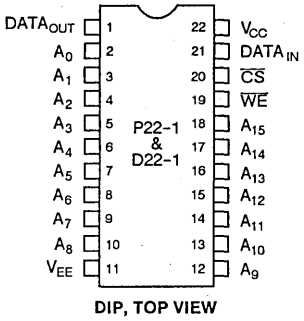
The IDT100490 is a 100K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 64K x 1.

The IDT100490 is available with address access times as fast as 8ns with a typical power consumption of only 320mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

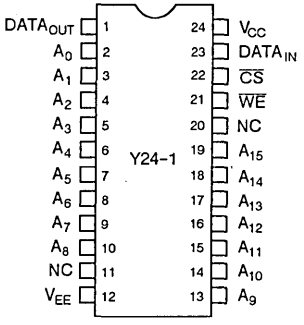
Designed for very high-speed applications, the IDT100490 is fully compatible with standard ECL 100K logic levels and offers extremely fast access times. The address access time of 8ns and write pulse width of 6ns assure that operations of this BiCEMOS part will be as fast as those available with less dense parts requiring external address decoding.

The IDT100490 is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

PIN CONFIGURATIONS

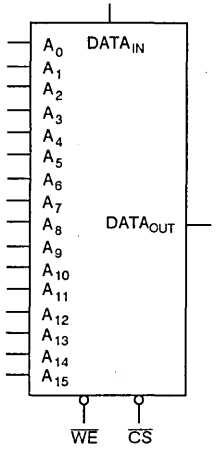


DIP, TOP VIEW

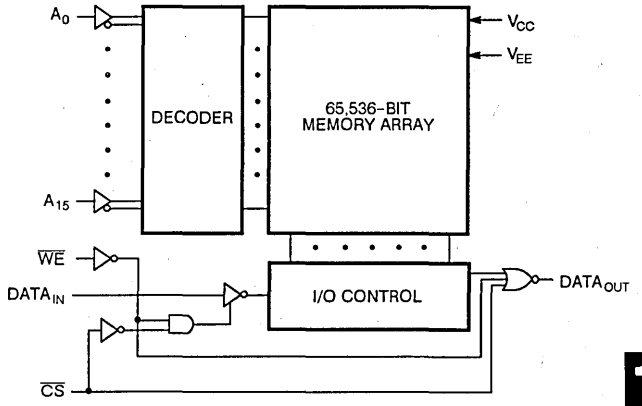


SOJ, TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Hermetic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H = High, L = Low, X = Don't Care

DC ELECTRICAL CHARACTERISTICS

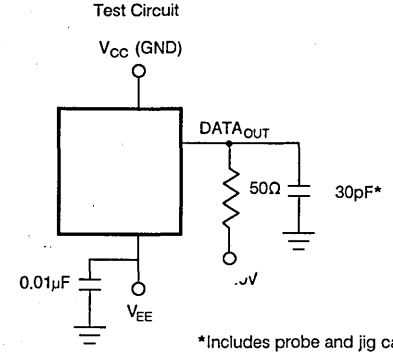
(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	–	
I_{EE}	Supply Current	All inputs and outputs open		-120	-70	–	mA

NOTE:

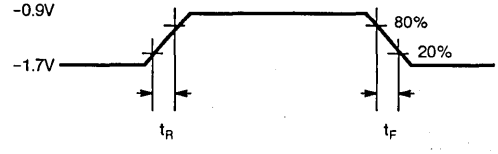
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE

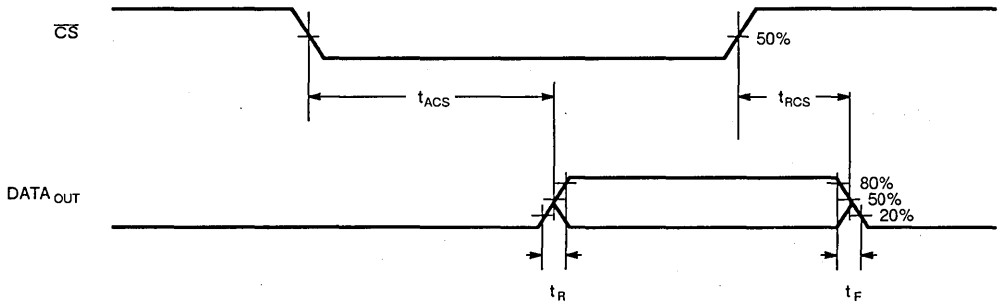


t_R = t_F = 2.0ns typ.

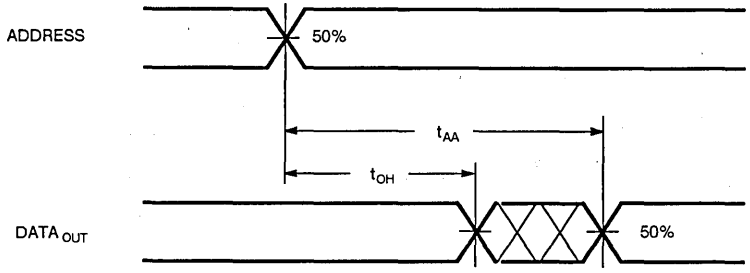
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100490S8 MIN.	IDT100490S8 MAX.	IDT100490S10 MIN.	IDT100490S10 MAX.	IDT100490S12 MIN.	IDT100490S12 MAX.	IDT100490S15 MIN.	IDT100490S15 MAX.	IDT100490S20 MIN.	IDT100490S20 MAX.	UNIT
READ CYCLE													
t_{ACS}	Chip Select Access Time	–	–		–	5	–	5	–	10	–	10	ns
t_{RCS}	Chip Select Recovery Time	–	–		–	5	–	5	–	10	–	10	ns
t_{AA}	Address Access Time	–	–	8	–	10	–	12	–	15	–	20	ns
t_{OH}	Data Hold from Address Change	–	3.0	–	3.5	–	3.5	–	3.5	–	3.5	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT100490 MIN.	IDT100490 TYP.	IDT100490 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

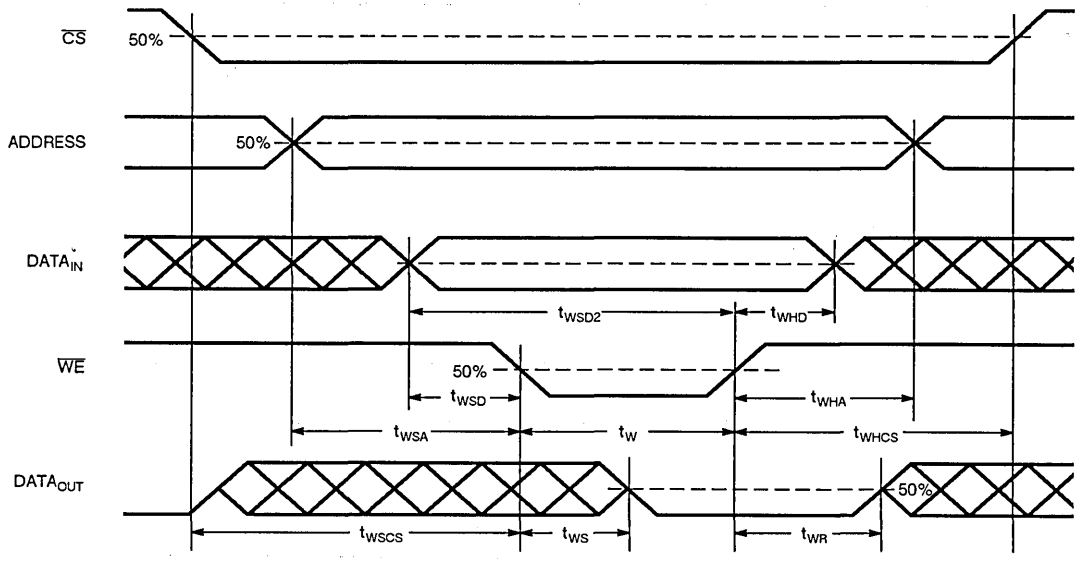
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100490S8 MIN.	IDT100490S8 MAX.	IDT100490S10 MIN.	IDT100490S10 MAX.	IDT100490S12 MIN.	IDT100490S12 MAX.	IDT100490S15 MIN.	IDT100490S15 MAX.	IDT100490S20 MIN.	IDT100490S20 MAX.	UNIT
WRITE CYCLE													
t_W	Write Pulse Width	t_{WSA} = minimum	6	–	8	–	10	–	10	–	15	–	ns
t_{WSD}(1)	Data Set-up Time	–	0	–	0	–	0	–	2	–	3	–	ns
t_{WSD2}	Data Set-up to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	7	–	ns
t_{WHD}	Data Hold Time	–	2	–	2	–	2	–	3	–	4	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum		–	0	–	0	–	2	–	3	–	ns
t_{WHA}	Address Hold Time	–		–	2	–	2	–	3	–	4	–	ns
t_{WSCS}	Chip Select Set-up Time	–		–	0	–	0	–	2	–	3	–	ns
t_{WHCS}	Chip Select Hold Time	–		–	2	–	2	–	3	–	4	–	ns
t_{WS}	Write Disable Time	–		–	–	5	–	5	–	10	–	10	ns
t_{WR}(2)	Write Recovery Time	–		–	–	12	–	14	–	18	–	23	ns

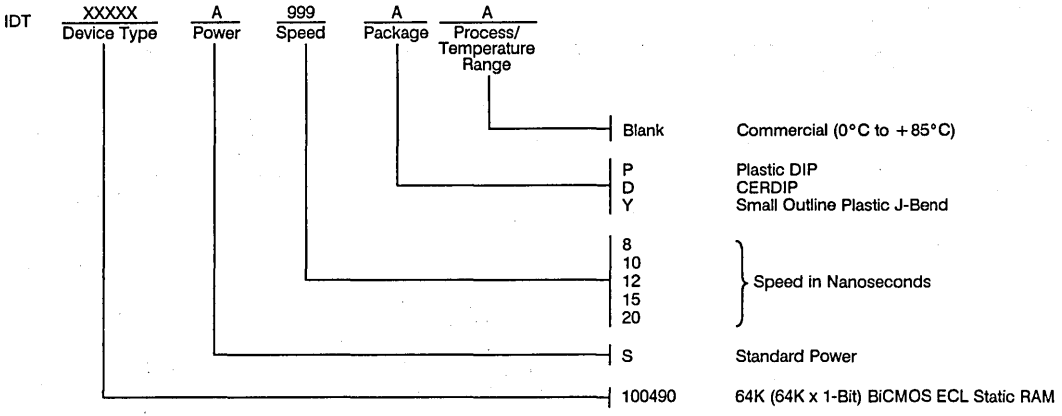
NOTE:

1. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. $t_{WR} = t_{WHA} + t_{AA}$ and thus can include a full access time if addresses change while Chip Select is still low.

TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION



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Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT)

PRELIMINARY
IDT 10494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 8/10/15 ns (max.)
- Low power dissipation: 600mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

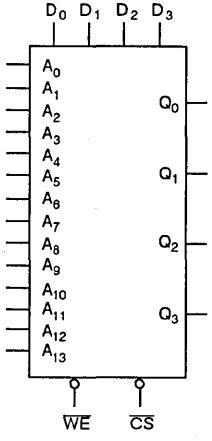
The IDT10494 is a 65,536-bit high-speed BiCEMOS™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL-10K levels.

Available with address access times as fast as 8ns, this device exhibits a typical power consumption of only 600mW. It offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

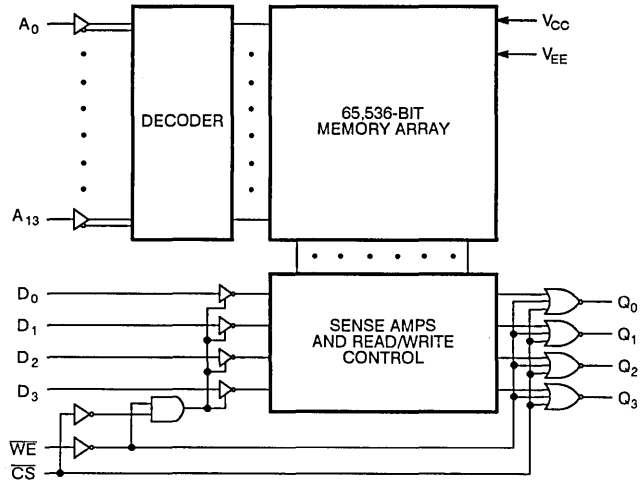
Designed for very high-speed applications, the IDT10494 offers open emitter outputs and separate data input and output, as well as extremely fast access times. The address access time of 8ns assures that operation of this BiCEMOS part will be as fast as with less dense parts requiring external address decoding.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +75	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H = High, L = Low, X = Don't Care

DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2m/sec)

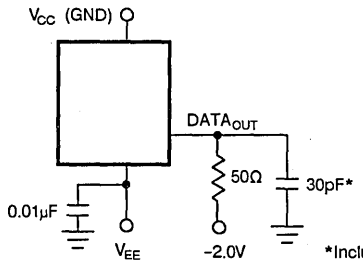
SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-855	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-160	-110	–	mA	

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

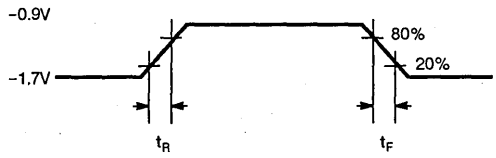
LOAD CONDITION

Test Circuit



*Includes probe and jig capacitance.

INPUT PULSE



t_R = t_F = 2.0ns typ.

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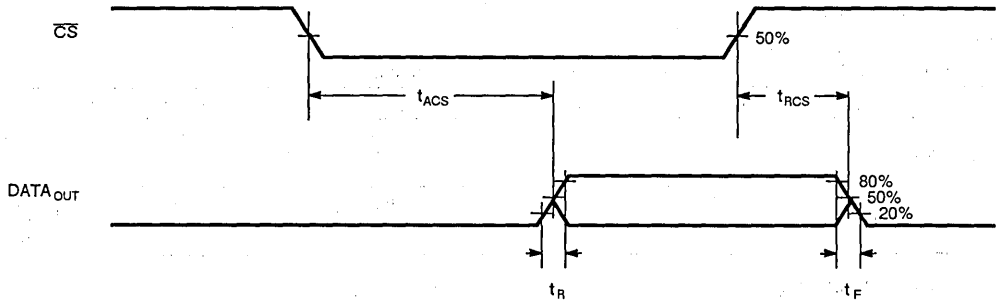
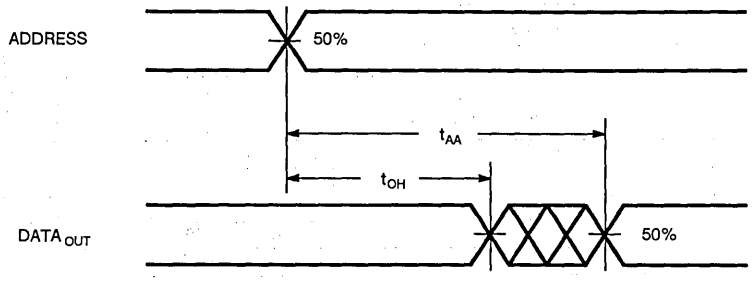
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10494S8 MIN.	IDT10494S8 MAX.	IDT10494S10 MIN.	IDT10494S10 MAX.	IDT10494S15 MIN.	IDT10494S15 MAX.	UNIT
READ CYCLE									
t_{ACS}	Chip Select Access Time	–			–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–			–	5	–	5	ns
t_{AA}	Address Access Time	–		8	–	10	–	12	ns
t_{OH}	Data Hold from Address Change	–	3	–	3.5	–	3.5	–	ns

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT10494 MIN.	IDT10494 TYP.	IDT10494 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

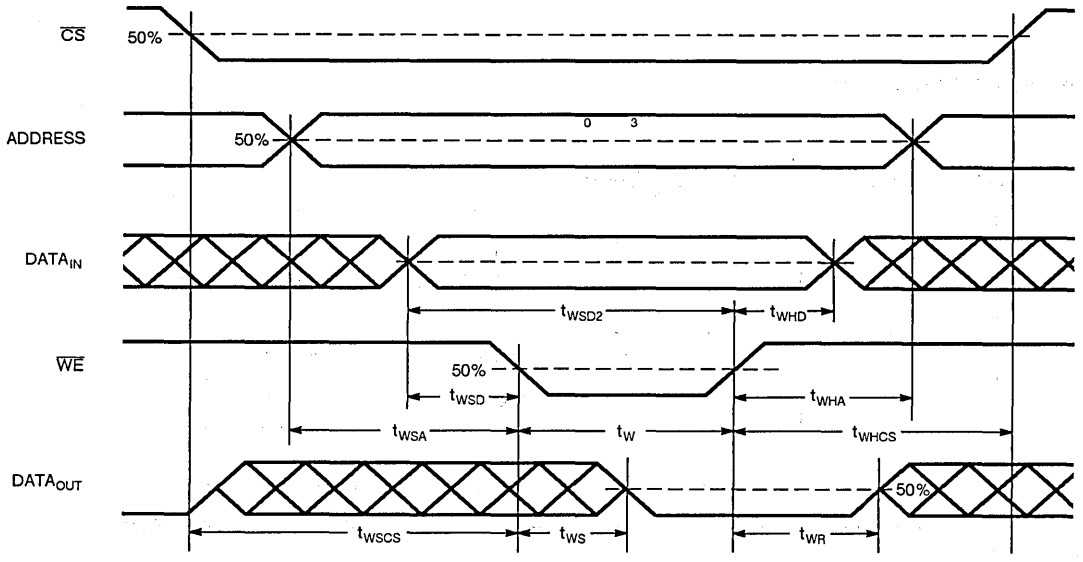
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10494S8 MIN.	IDT10494S8 MAX.	IDT10494S10 MIN.	IDT10494S10 MAX.	IDT10494S15 MIN.	IDT10494S15 MAX.	UNIT
WRITE CYCLE									
t_W	Write Pulse Width	t_{WSA} = minimum	6	–	8	–	10	–	ns
t_{WSD}	Data Set-up Time	–	0	–	0	–	2	–	ns
t_{WSD2}(1)	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	ns
t_{WHD}	Data Hold Time	–	2	–	2	–	3	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum		–	0	–	2	–	ns
t_{WHA}	Address Hold Time	–		–	2	–	3	–	ns
t_{WSCS}	Chip Select Set-up Time	–		–	0	–	2	–	ns
t_{WHCS}	Chip Select Hold Time	–		–	2	–	3	–	ns
t_{WS}	Write Disable Time	–		–	–	5	–	5	ns
t_{WR}(1)	Write Recovery Time	–		–	–	5	–	5	ns

NOTES:

1. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. t_{WR} is defined as the time to reflect the newly written data on the Data Outputs (Q to Q) when no new Address transition occurs.

TIMING WAVEFORM OF WRITE CYCLE



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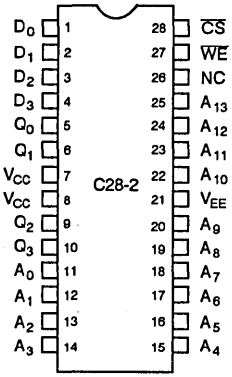
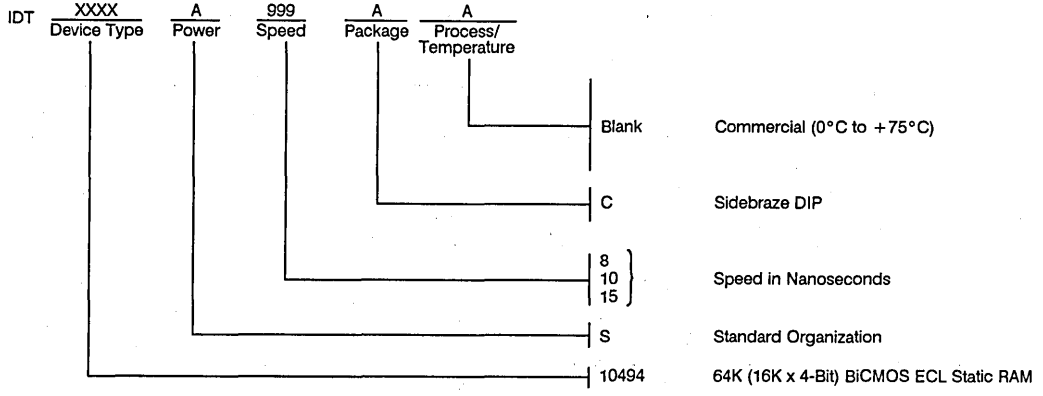
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) MIL-STD-883 COMPLIANT

ADVANCE INFORMATION
IDT 10494M

FEATURES:

- 16,384-word x 4-bit organization
- Low power dissipation: 600mW (typ.)
- Fully compatible with ECL—10K logic levels
- Address access time: 15/20ns (max.)
- Write pulse width: 10ns (min.)
- Open emitter output for ease of memory expansion
- Separate data input and output
- JEDEC standard 28-pin DIP
- MIL-STD-883 compliant
- Operation over the full temperature range -55°C to +125°C

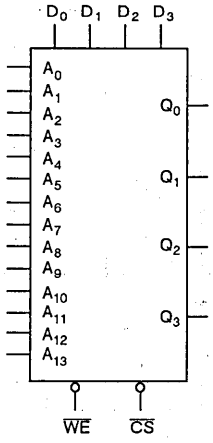
DESCRIPTION:

The IDT10494 is a 10K compatible 65,536-bit high-speed BiCEMOS™ ECL static RAM organized as 16K x 4. It is manufactured, assembled, and tested by Integrated Device Technology, Inc. in full compliance with MIL-STD-883, and operates over the full temperature range of -55°C to +125°C.

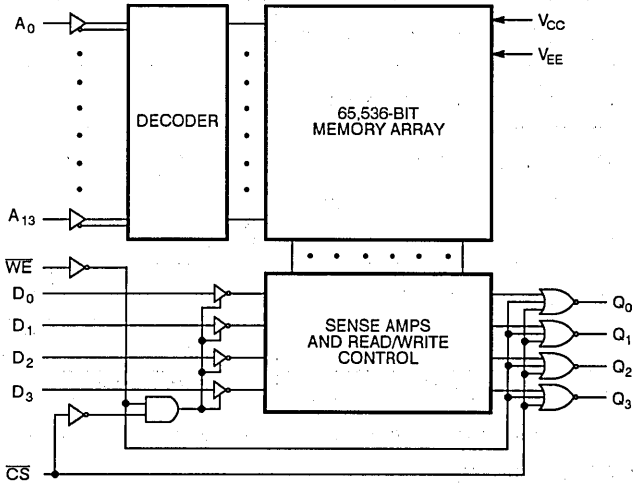
The IDT10494 is available with address access times as fast as 15ns with a typical power consumption of only 600mW. This product offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to achieve a high-performance ECL system with dramatically lower power dissipation than bipolar equivalents, reducing power supply and cooling requirements.

Designed for very high-speed applications, the IDT10494 is fully compatible with standard ECL-10K logic levels and offers extremely fast access times. Applications include cache, control store, buffer, and main memory uses. The high density allows fewer address-decode delays, providing better system speed over smaller ECL memories.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	–	6	pF
C_{OUT}	Output Capacitance	–	6	pF

TRUTH TABLE (1)

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H = High, L = Low, X = Don't Care

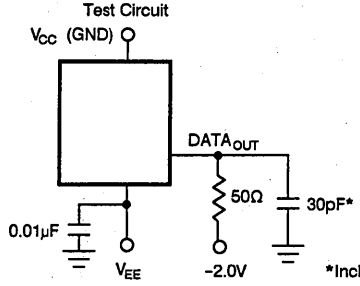
DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = -55 to +125°C for DIP, air flow exceeding 2m/sec)

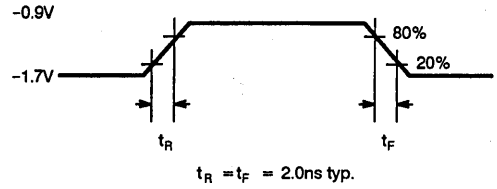
SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.(1)	MAX. (A)	UNIT	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1070 -960 -860	-855	-860 -810 -600	mV	-55°C 25°C +125°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1900 -1850 -1800	–	-1690 -1650 -1570	mV	-55°C 25°C +125°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1090 -980 -830	–	–	mV	-55°C 25°C +125°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1670 -1630 -1550	mV	-55°C 25°C +125°C
V_{iH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1215 -1105 -1005	–	-860 -810 -600	mV	-55°C 25°C +125°C
V_{iL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1900 -1850 -1800	–	-1515 -1475 -1395	mV	-55°C 25°C +125°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-160	-110	–	mA	

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

LOAD CONDITION



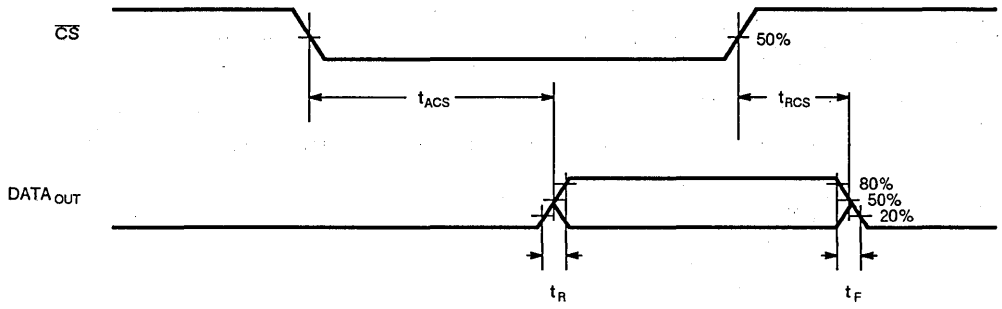
INPUT PULSE



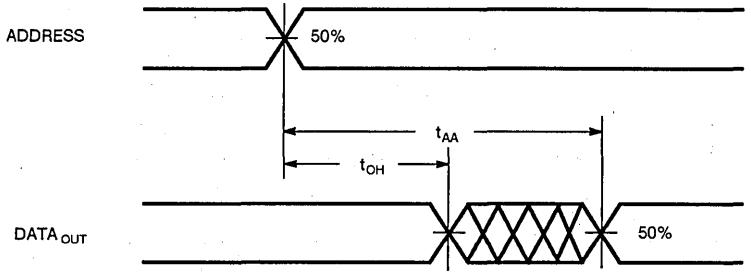
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = -55 to +125°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10494S15 MIN.	IDT10494S15 MAX.	IDT10494S20 MIN.	IDT10494S20 MAX.	UNIT
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{AA}	Address Access Time	–	–	15	–	20	ns
t_{OH}	Data Hold from Address Change	–	TBD	–	TBD	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT10494 MIN.	IDT10494 TYP.	IDT10494 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

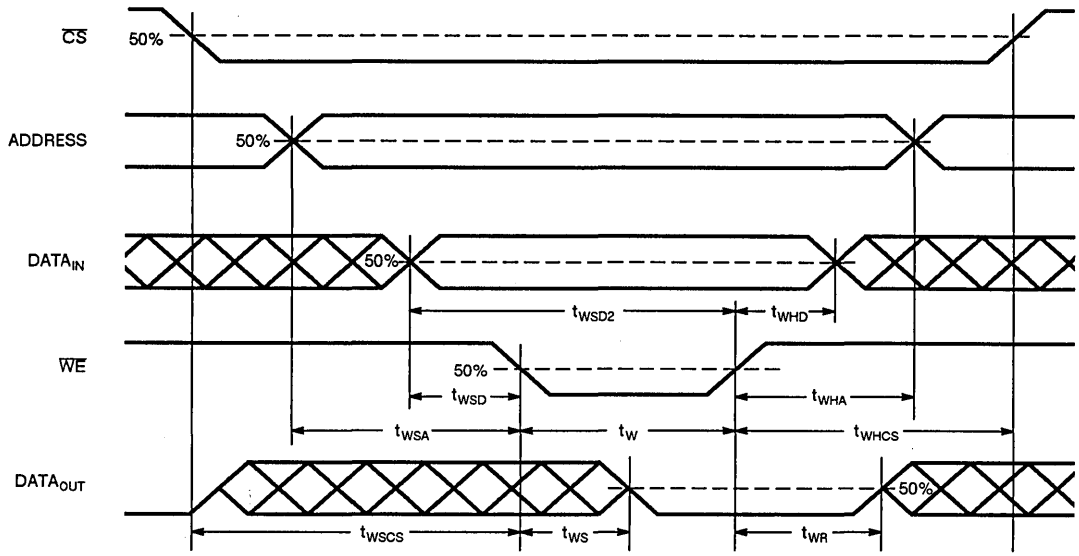
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ±5%, T_A = -55 to +125°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10494S15 MIN.	IDT10494S15 MAX.	IDT10494S20 MIN.	IDT10494S20 MAX.	UNIT
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	13	–	ns
t_{WSD}	Data Set-up Time	–	2	–	3	–	ns
t_{WSD2}	Data Set-up to $\overline{WE}$ high	–	TBD	–	TBD	–	ns
t_{WHD}	Data Hold Time	t_W = minimum	3	–	4	–	ns
t_{WSA}	Address Set-up Time		2	–	3	–	ns
t_{WHA}	Address Hold Time	–	3	–	4	–	ns
t_{WSCS}	Chip Select Set-up Time	–	2	–	3	–	ns
t_{WHCS}	Chip Select Hold Time	–	3	–	4	–	ns
t_{WS}	Write Disable Time	–	–	5	–	5	ns
t_{WR}(1)	Write Recovery Time	–	–	5	–	5	ns

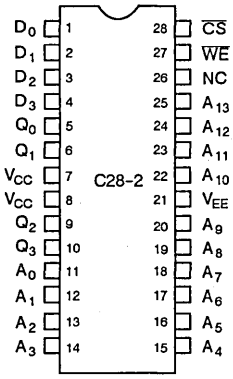
NOTE:

1. t_{WSD} is specified with respet to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. t_{WR} is defined as the time to reflect newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.

TIMING WAVEFORM OF WRITE CYCLE



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

ORDERING INFORMATION

IDT — XXXXX (Device Type) — A (Power) — 999 (Speed) — A (Package) — A (Process/Temperature Range)

B	Military -55°C to +125°C
C	Sidebraze DIP
15 20	Speed in Nanoseconds
S	Standard Power
10494	64K (16K x 4-Bit) BiCMOS ECL Static RAM

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Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT)

PRELIMINARY
IDT 100494

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 8/10/15ns (max.)
- Low power dissipation: 500mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

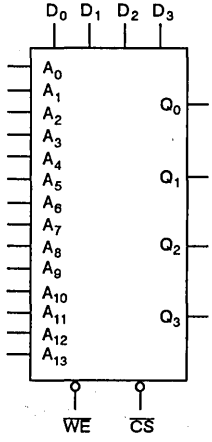
The IDT100494 is a 65,536-bit high-speed BiCEMOS™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL–100K levels

Available with address access times as fast as 8ns, this device exhibits a typical power consumption of only 600mW. It offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

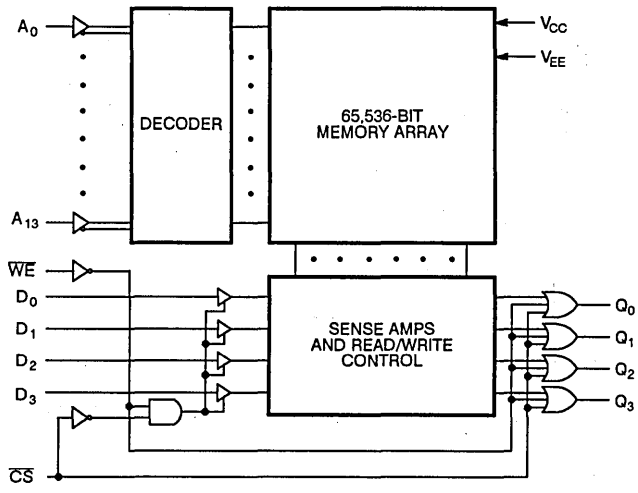
Designed for very high-speed applications, the IDT100494 offers open emitter outputs and seperate data input and output, as well as extremely fast access times. The address access time of 8ns assures that operation of this BiCEMOS part will be as fast as with less dense parts requiring external address decoding.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Hermetic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	DIP		SOJ	
		TYP.	MAX.	TYP.	MAX.
C_{IN}	Input Capacitance	6	–	TBD	–
C_{OUT}	Output Capacitance	6	–	TBD	–

TRUTH TABLE (1)

$\overline{CS}$	$\overline{WE}$	$DATA_{OUT}$	FUNCTION
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:

1. H = High, L = Low, X = Don't Care

DC ELECTRICAL CHARACTERISTICS

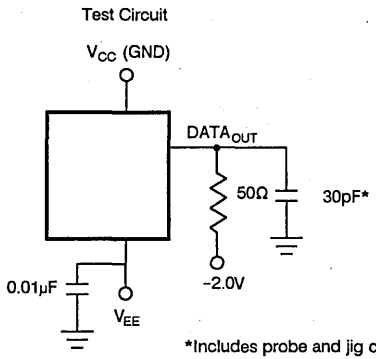
(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.(1)	MAX. (A)	UNIT
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	–	
I_{EE}	Supply Current	All inputs and outputs open		-140	-110	–	mA

NOTE:

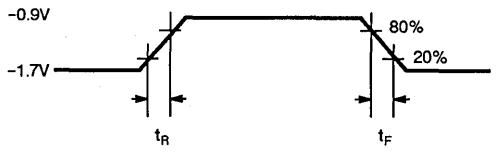
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE



t_R = t_F = 2.0ns typ.

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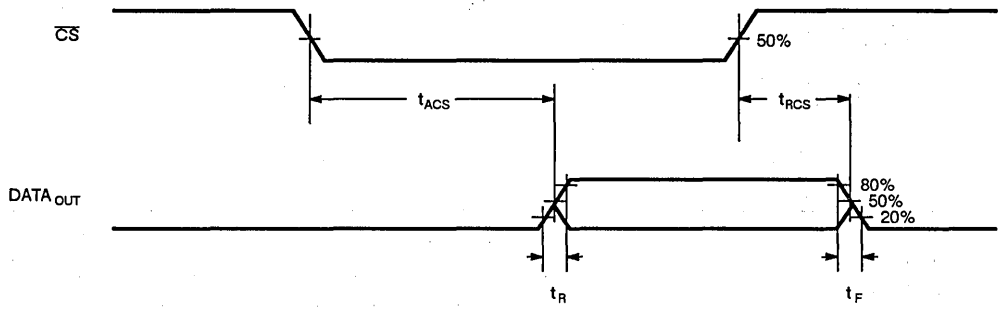
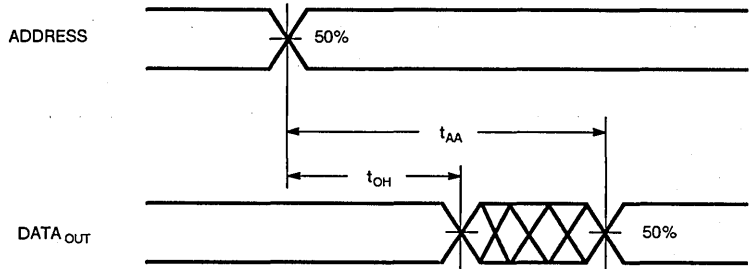
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100494S8	IDT100494S10 MIN.	IDT100494S10 MAX.	IDT100494S15 MIN.	IDT100494S15 MAX.	UNIT
READ CYCLE								
t_{ACS}	Chip Select Access Time	–	3	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	–	5	–	5	ns
t_{AA}	Address Access Time	–	8	–	10	–	15	ns
t_{OH}	Data Hold from Address Change	–	3 –	3.5	–	3.5	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1



TIMING WAVEFORM OF READ CYCLE NO. 2



RISE/FALL TIME

SYMBOL	PARAMETER	TEST CONDITION	IDT100494 MIN.	IDT100494 TYP.	IDT100494 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

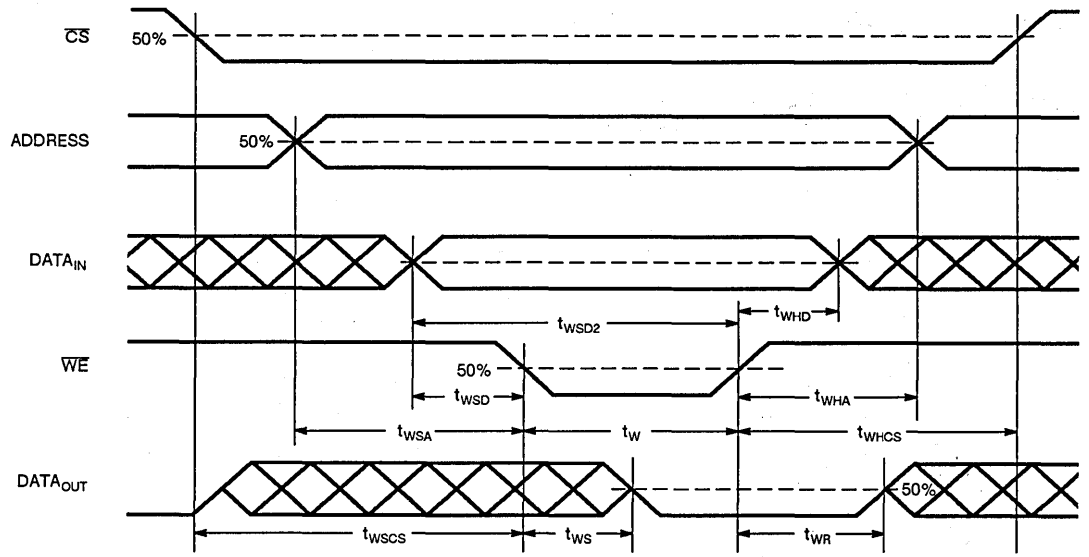
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ±5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT100494S8	IDT100494S10 MIN.	IDT100494S10 MAX.	IDT100494S15 MIN.	IDT100494S15 MAX.	UNIT
WRITE CYCLE								
t_W	Write Pulse Width	t_{WSA} = minimum	6	8	–	10	–	ns
t_{WSD}	Data Set-up Time	–	0	0	–	2	–	ns
t_{WSD2}(1)	Data Set-up to $\overline{WE}$ High	–	5	5	–	5	–	ns
t_{WHD}	Data Hold Time	t_W = minimum	2	2	–	3	–	ns
t_{WSA}	Address Set-up Time			0	–	2	–	ns
t_{WHA}	Address Hold Time	–		2	–	3	–	ns
t_{WSCS}	Chip Select Set-up Time	–		0	–	2	–	ns
t_{WHCS}	Chip Select Hold Time	–		2	–	3	–	ns
t_{WS}	Write Disable Time	–		–	5	–	5	ns
t_{WR}(2)	Write Recovery Time	–		–	5	–	5	ns

NOTE:

1. t_{WSD} is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires t_{WSD2} with respect to rising edge of $\overline{WE}$.
2. t_{WR} is defined as the time to reflect newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.

TIMING WAVEFORM OF WRITE CYCLE



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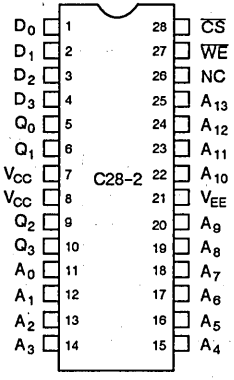
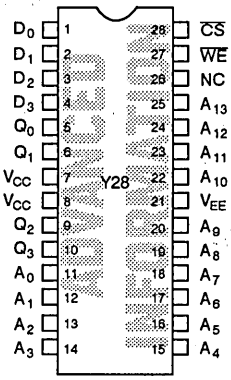
PIN CONFIGURATION

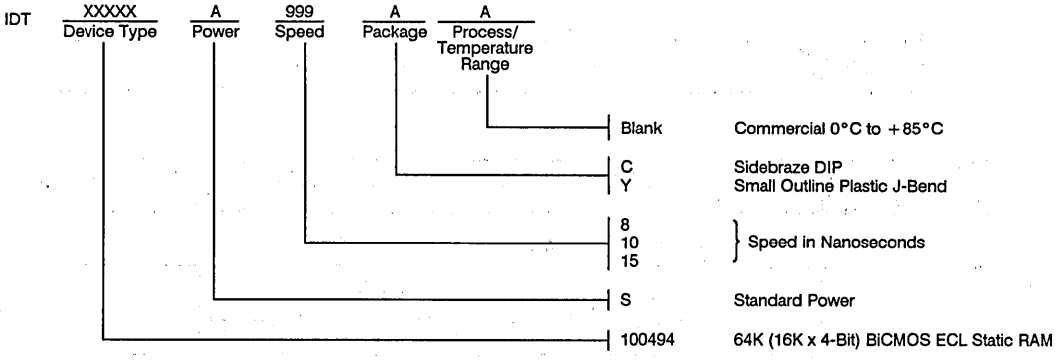


DIP
TOP VIEW
(400mil)



SOJ
TOP VIEW
(350mil)

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT 10496LL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with latches on inputs and outputs
- Cycle time 13/15ns
- Address access time: 10/12ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

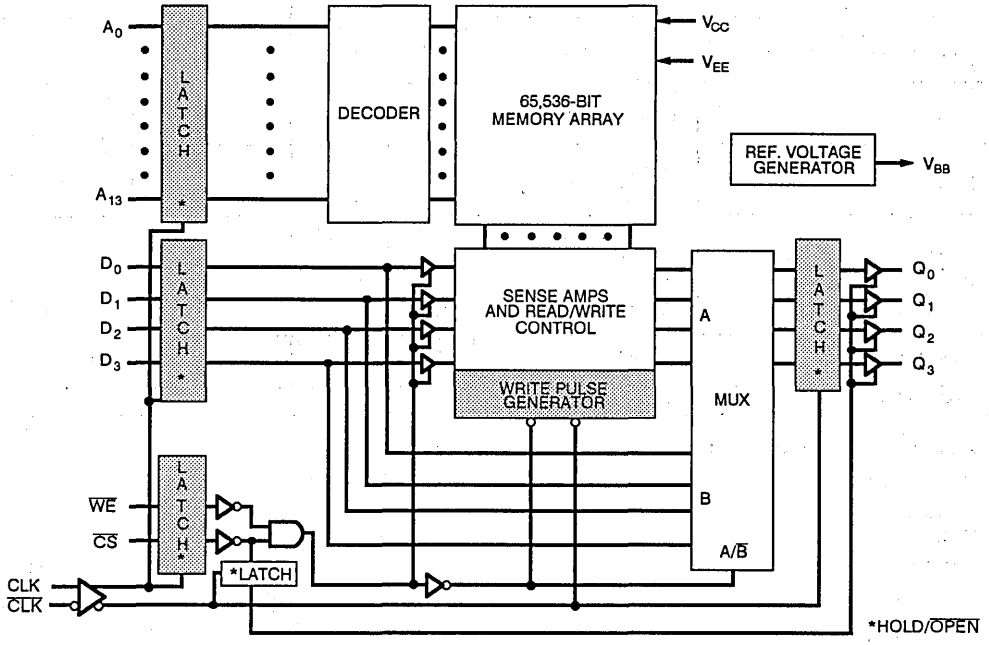
DESCRIPTION:

The IDT10496LL is a 65,536-bit high-speed BiCEMOS™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL 10K levels. This device has on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, the IDT10496LL allows cycle times as fast as 15ns.

The IDT10496LL is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. It offers the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +75	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance except CLK	4	–	pF
C_{IN}	Input Capacitance CLK	6	–	pF
C_{OUT}	I/O Capacitance	6	–	pF

TRUTH TABLE (1)

$\overline{CS}$	$\overline{WE}$	CLK	$DATA_{OUT}$(2)	FUNCTION
H	X	⌐⌙	L	Deselected
L	H	⌐⌙	RAM Data	Read
L	L	⌐⌙	WRITE Data	Write

NOTES:

1. H = High, L = Low, X = Don't Care
2. $DATA_{OUT}$ changes when CLK returns high.

DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2m/sec)

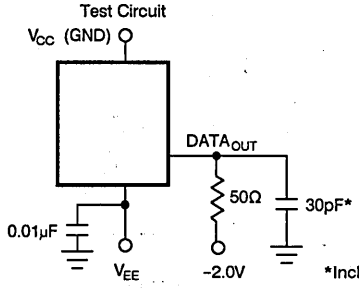
SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.(1)	MAX. (A)	UNIT	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-855	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-200	-150	–	mA	

NOTE:

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

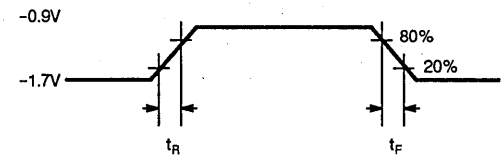
LOAD CONDITION

Test Circuit



*Includes probe and jig capacitance.

INPUT PULSE



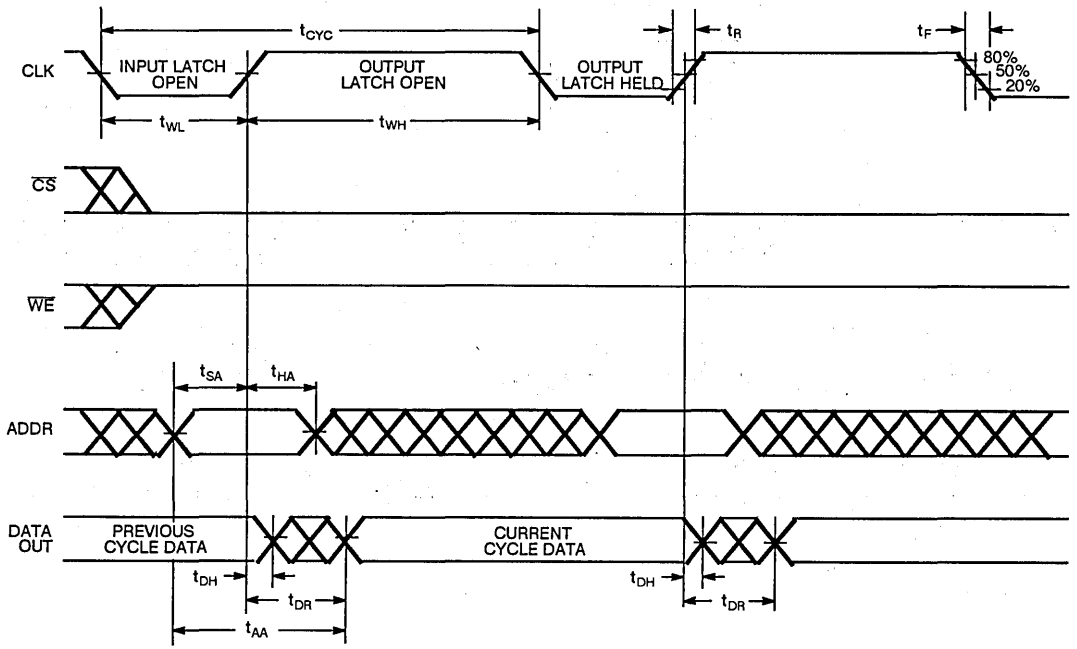
t_R = t_F = 2.0ns typ.

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496LL13 MIN.	IDT10496LL13 MAX.	IDT10496LL15 MIN.	IDT10496LL15 MAX.	UNIT
READ CYCLE GATED BY ADDRESS[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{AA}[3]	Address Access Time	–	–	10	–	12	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by address when $t_{SA} < t_{WL}$ so that the access begins at the setting of the address.
3. Access time is the larger of t_{AA} or $t_{SA} + t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SA} > t_{AA}$ (max) $- t_{DR}$ (max).

READ CYCLE GATED BY ADDRESS



RISE/FALL TIME

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496 MIN.	IDT10496 TYP.	IDT10496 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

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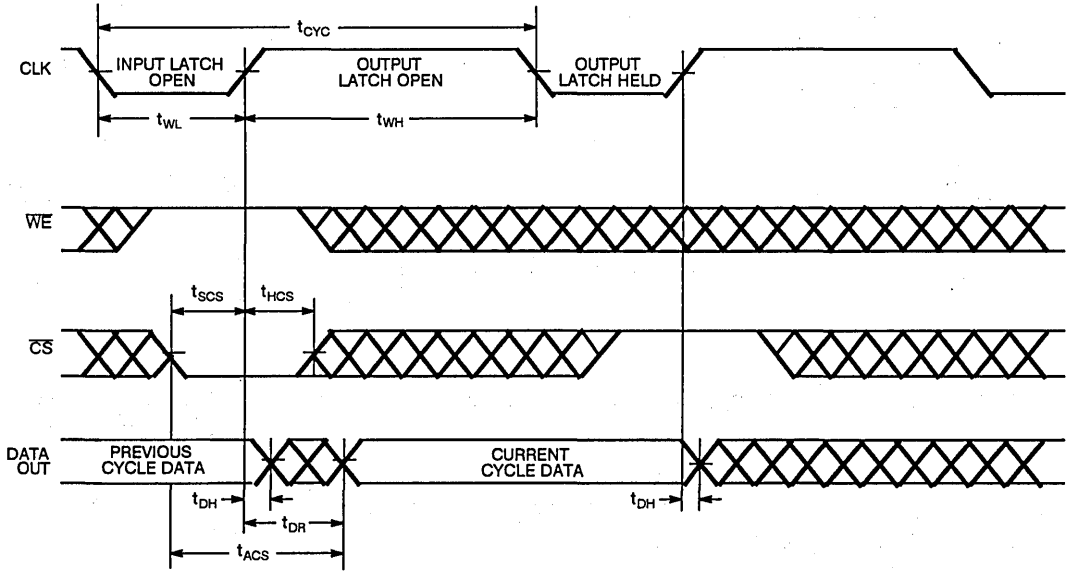
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496LL13 MIN.	IDT10496LL13 MAX.	IDT10496LL15 MIN.	IDT10496LL15 MAX.	UNIT
READ CYCLE GATED BY CHIP SELECT[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACS}[3]	Chip Select Access Time	–	–	5	–	5	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SCS}	Setup Time for Chip Select	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Chip Select when $t_{SCS} < t_{WL}$ so that the access begins as the falling edge of Chip Select.
3. Access time is the larger of t_{ACS} or $t_{SCS} + t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SCS} > t_{ACS}$ (max) $- t_{DR}$ (max).

READ CYCLE GATED BY CHIP SELECT

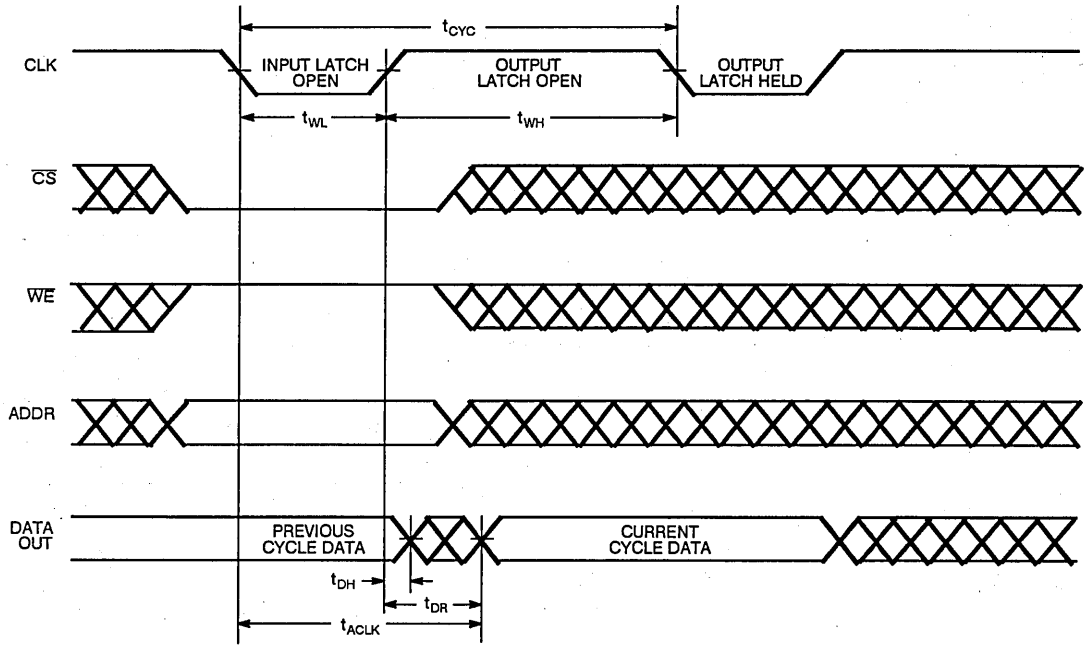


AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496LL13 MIN.	IDT10496LL13 MAX.	IDT10496LL15 MIN.	IDT10496LL15 MAX.	UNIT
READ CYCLE GATED BY CLOCK[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACLK}[3]	Clocked Access Time	–	–	10	–	12	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Clock when $t_{SA} < t_{WL}$ so that the access begins as the falling edge of Clock.
3. Access time is the larger of t_{ACLK} or $t_{WL} + t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{WL} > t_{ACLK} - t_{DR}$ (max).

READ CYCLE GATED BY CLOCK



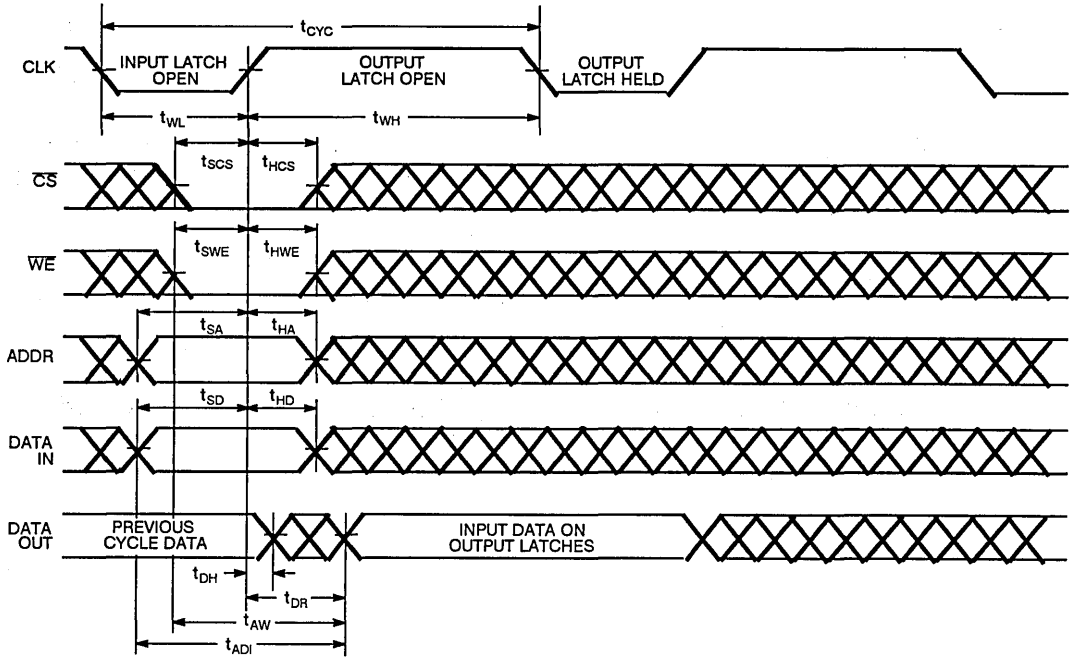
12

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496LL13 MIN.	IDT10496LL13 MAX.	IDT10496LL15 MIN.	IDT10496LL15 MAX.	UNIT
WRITE CYCLE[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{AW}[3]	Write Access Time	–	–	5	–	5	ns
t_{ADI}[4]	Write Data Access Time	–	–	5	–	5	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SCS}	Set-up Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Set-up Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{SD}	Set-up Time for Data In	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns

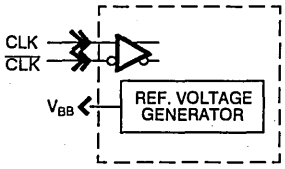
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Data Hold t_{DH} and Data Ready t_{DR} are the same as for Read Cycle.
3. Access time is the larger of t_{AW} or $t_{SWE} + t_{DR}$.
4. Access time is the larger of t_{ADI} or $t_{SD} + t_{DR}$.
5. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SD} > t_{ADI}$ (max) - t_{DR} (max) and $t_{SWE} > t_{AW}$ (max) - t_{DR} (max).

WRITE CYCLE

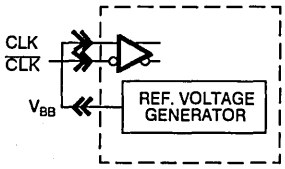


CLOCK INPUT

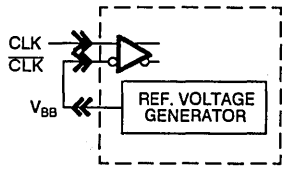
The clock input circuit in the IDT10496LL has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better rejection of common-mode noise and is obtained by driving both true and complement CLK lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising edge-active, as shown in Figures (b) and (c), respectively.



(a) Differential Mode

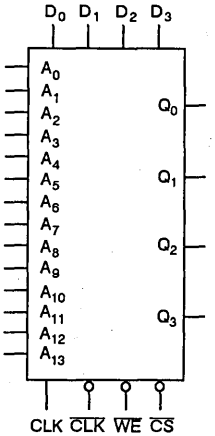


(b) Falling-Edge-Active Single-Ended Mode

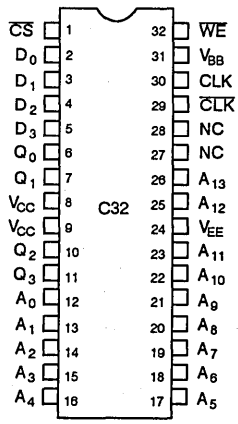


(c) Rising-Edge-Active Single-Ended Mode

LOGIC SYMBOL



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT 100496LL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with latches on inputs and outputs
- Cycle time 13/15ns
- Address access time: 10/12ns (max.)
- Low power dissipation: 700mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

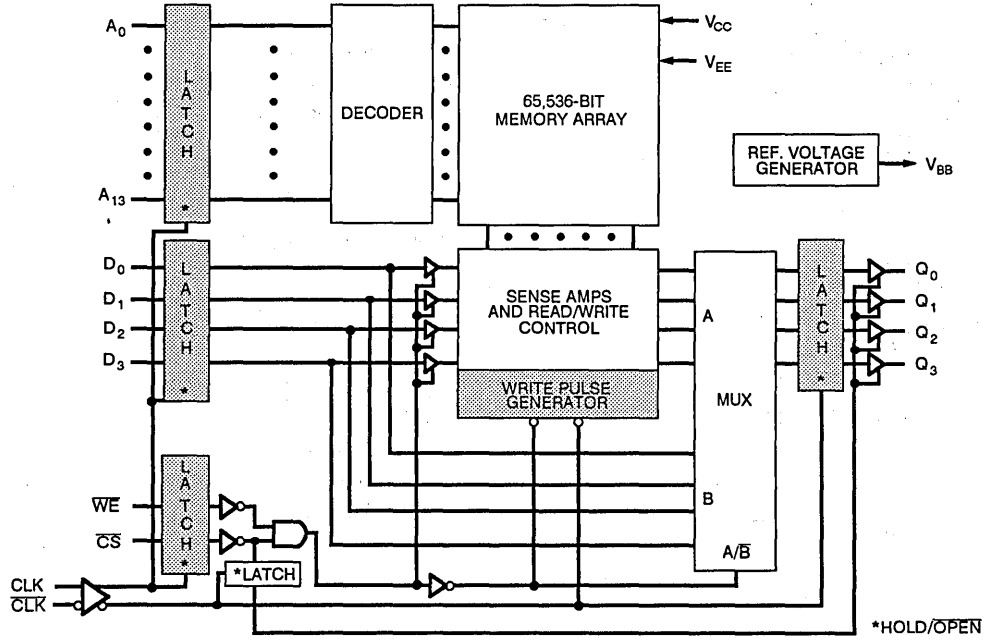
DESCRIPTION:

The IDT100496LL is a 65,536-bit high-speed BiCEMOS ™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL-100K levels. This device has on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, the IDT100496LL allows cycle times as fast as 15ns.

The IDT100496LL is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. It offers the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance except CLK	4	–	pF
C_{IN}	Input Capacitance CLK	6	–	pF
C_{OUT}	I/O Capacitance	6	–	pF

TRUTH TABLE [1]

$\overline{CS}$	$\overline{WE}$	CLK	$DATA_{OUT}$[2]	FUNCTION
H	X	⌐¬	L	Deselected
L	H	⌐¬	RAM Data	Read
L	L	⌐¬	WRITE Data	Write

NOTES:

1. H = High, L = Low, X = Don't Care
2. $DATA_{OUT}$ changes when CLK returns high.

DC ELECTRICAL CHARACTERISTICS

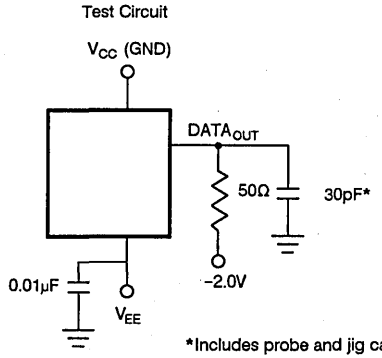
(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.[1]	MAX. (A)	UNIT
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	–	
I_{EE}	Supply Current	All inputs and outputs open		-180	-110	–	mA

NOTE:

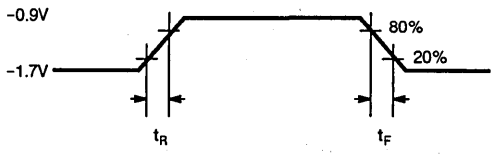
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE



t_R = t_F = 2.0ns typ.

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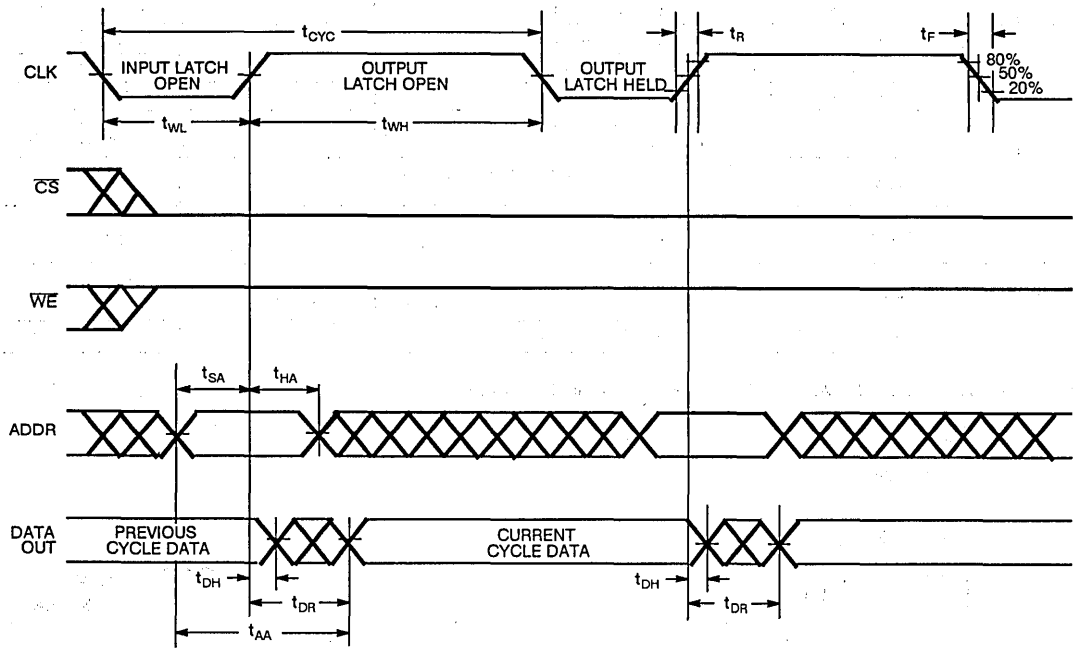
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496LL13 MIN.	IDT100496LL13 MAX.	IDT100496LL15 MIN.	IDT100496LL15 MAX.	UNIT
READ CYCLE GATED BY ADDRESS[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{AA}[3]	Address Access Time	–	–	10	–	12	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SA}	Setup Time for Address	–	1	–	1	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when $t_{SA} < t_{WL}$ so that the access begins at the setting of Address.
3. Access time is the larger of t_{AA} or $t_{AS} + t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SA} > t_{AA}$ (max) – t_{DR} (max).

READ CYCLE GATED BY ADDRESS



RISE/FALL TIME

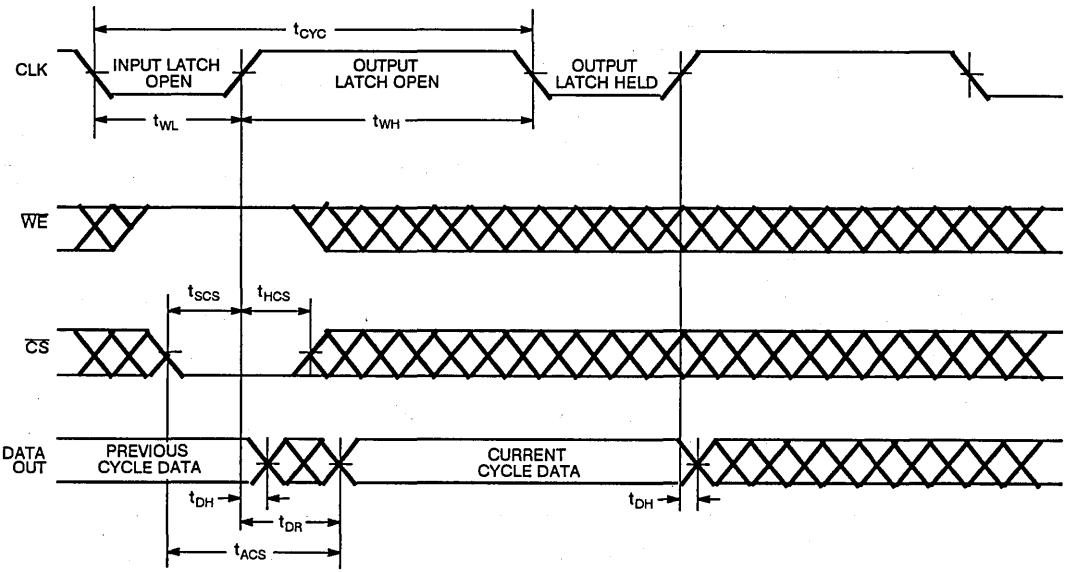
SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496 MIN.	IDT100496 TYP.	IDT100496 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496LL13 MIN.	IDT100496LL13 MAX.	IDT100496LL15 MIN.	IDT100496LL15 MAX.	UNIT
READ CYCLE GATED BY CHIP SELECT[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACS}[3]	Chip Select Access Time	–	–	5	–	5	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SCS}	Setup Time for Chip Select	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when $t_{SCS} < t_{WL}$ so that the access begins at the falling edge of Chip Select.
3. Access time is the larger of t_{ACS} or $t_{SCS}+t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SCS} > t_{ACS}$ (max) - t_{DR} (max).

READ CYCLE GATED BY CHIP SELECT



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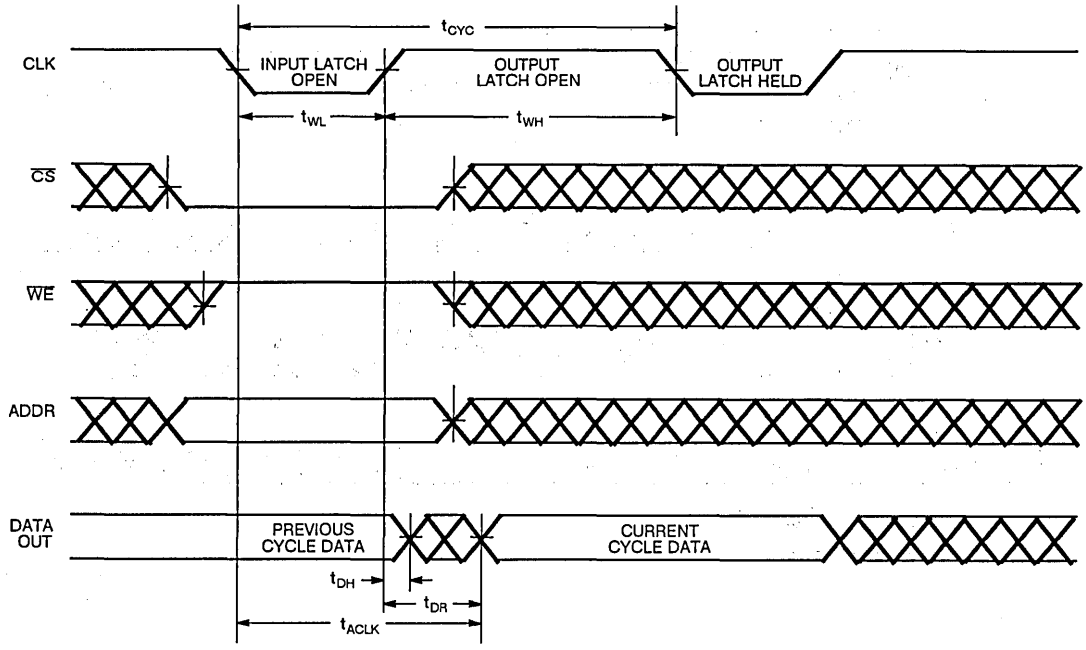
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496LL13 MIN.	IDT100496LL13 MAX.	IDT100496LL15 MIN.	IDT100496LL15 MAX.	UNIT
READ CYCLE GATED BY CLOCK[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACLK}[3]	Clocked Access Time	–	–	10	–	12	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{DH}	Data Out Hold from Clock High	–	0	–	0	–	ns
t_{DR}[3, 4]	Data Out Ready from Clock High	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when $t_{SA} < t_{WL}$ so that the access begins at the falling edge of Clock.
3. Access time is the larger of t_{ACLK} or $t_{WL} + t_{DR}$.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{WL} > t_{ACLK}$(max) – t_{DR} (max).

READ CYCLE GATED BY CLOCK

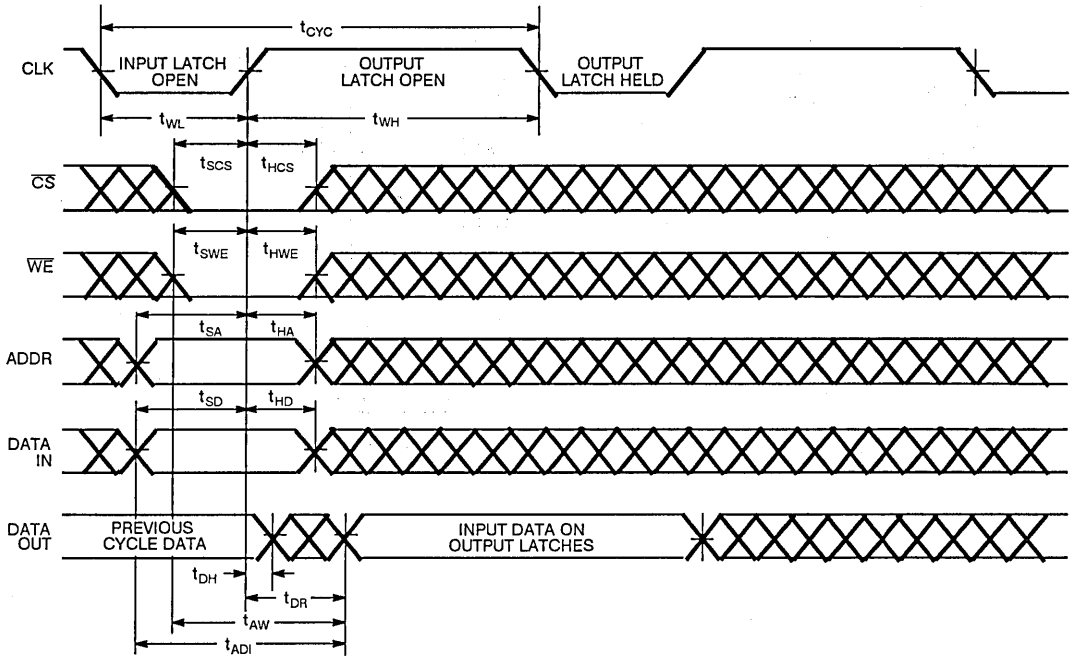


AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496LL13 MIN.	IDT100496LL13 MAX.	IDT100496LL15 MIN.	IDT100496LL15 MAX.	UNIT
WRITE CYCLE[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{AW}[3]	Write Access Time	–	–	5	–	5	ns
t_{ADI}[4]	Write Data Access Time	–	–	5	–	5	ns
t_{WL}	Clock Low Pulse Width	–	3	–	3	–	ns
t_{WH}	Clock High Pulse Width	–	10	–	12	–	ns
t_{SCS}	Set-up Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Set-up Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{SD}	Set-up Time for Data In	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Data Hold t_{DH} and Data Ready t_{DR} are the same as for Read Cycle.
3. Access time is the larger of t_{AW} or $t_{SWE} + t_{DR}$.
4. Access time is the larger of t_{ADI} or $t_{SD} + t_{DR}$.
5. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{SD} > t_{ADI}$ (max) – t_{DR}(max) and $t_{SWE} > t_{AW}$(max) – t_{DR} (max).

WRITE CYCLE



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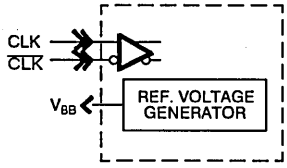
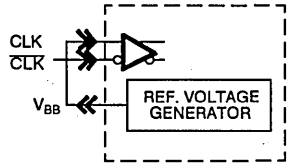
CLOCK INPUT

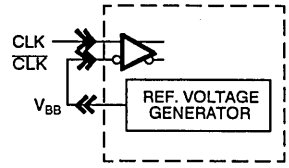
The clock input circuit in the IDT100496LL has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better rejection of common-mode noise and is obtained by driving both true and complement CLK lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising edge-active, as shown in Figures (b) and (c), respectively.



(a) Differential Mode

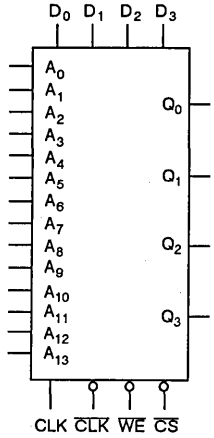


(b) Falling-Edge-Active Single-Ended Mode

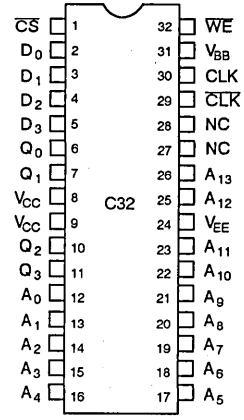


(c) Rising-Edge-Active Single-Ended Mode

LOGIC SYMBOL



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY INFORMATION IDT 10496RL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Cycle time 13/15ns
- Address access time: 10/12ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

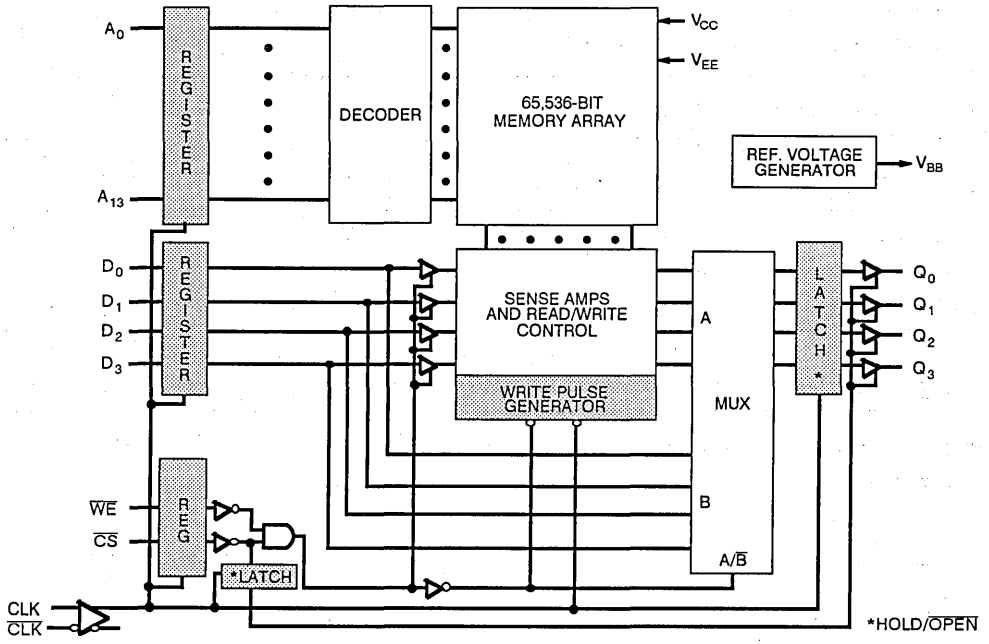
DESCRIPTION:

The IDT10496RL is a 65,536-bit high-speed BiCEMOS ™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL 10K levels. This device has on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, the IDT10496RL allows cycle times as fast as 15ns.

The IDT10496RL is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. It offers the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +75	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance except CLK	4	–	pF
C_{IN}	Input Capacitance CLK	6	–	pF
C_{OUT}	I/O Capacitance	6	–	pF

TRUTH TABLE (1)

$\overline{CS}$	$\overline{WE}$	CLK	$DATA_{OUT}$(2)	FUNCTION
H	X	↓	L	Deselected
L	H	↓	RAM Data	Read
L	L	↓	WRITE Data	Write

NOTES:

1. H = High, L = Low, X = Don't Care
2. $DATA_{OUT}$ changes when CLK returns high.

DC ELECTRICAL CHARACTERISTICS

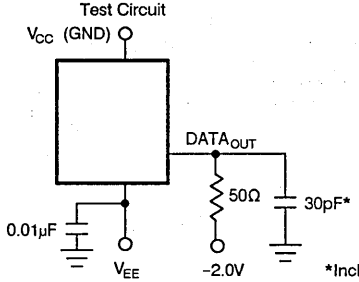
(V_{EE} = -5.2V, RL = 50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.(1)	MAX. (A)	UNIT	T_A/T_C
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-855	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	
			Others	–	–	110		
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	
			Others	-50	–	90		
I_{EE}	Supply Current	All inputs and outputs open		-200	-150	–	mA	

NOTE:

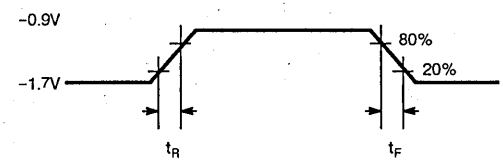
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE



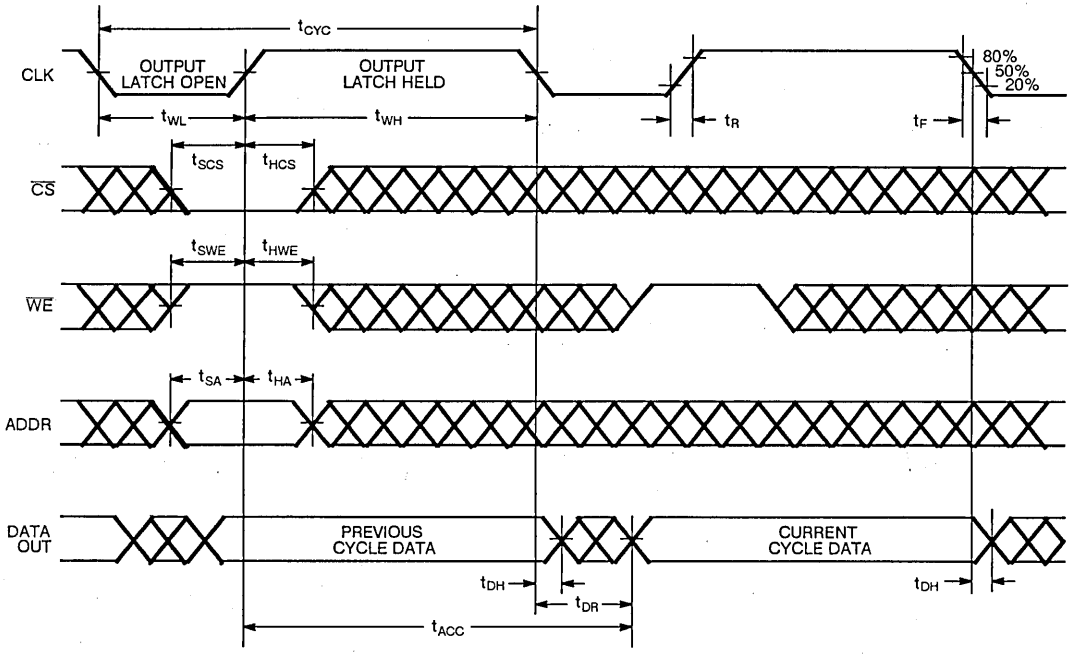
t_R = t_F = 2.0ns typ.

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496RL13 MIN.	IDT10496RL13 MAX.	IDT10496RL15 MIN.	IDT10496RL15 MAX.	UNIT
READ CYCLE[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACC}[3]	Access Time from Clock High	–	–	10	–	10	ns
t_{WL}	Clock Low Pulse Width	–	5	–	5	–	ns
t_{WH}	Clock High Pulse Width	–	7.5	–	7.5	–	ns
t_{SCS}	Setup Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Setup Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Setup Time for Address	–	1	–	1	–	ns
t_{SD}	Setup Time for Data in	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data in	–	2	–	2	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}	Data Ready from Clock Low	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of t_{ACC} or $t_{WH} + t_{DR}$.

READ CYCLE



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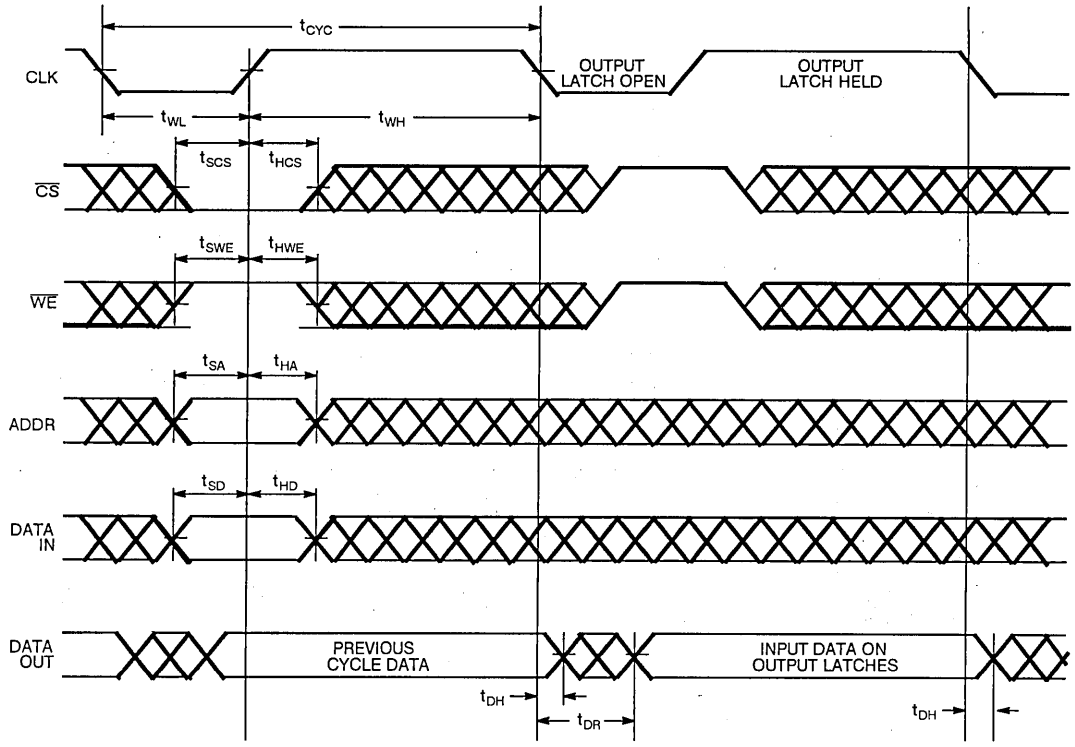
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT10496RL13 MIN.	IDT10496RL13 MAX.	IDT10496RL15 MIN.	IDT10496RL15 MAX.	UNIT
WRITE CYCLE							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{WL}	Clock Low Pulse Width	–	5	–	5	–	ns
t_{WH}	Clock High Pulse Width	–	7.5	–	7.5	–	ns
t_{SCS}	Set-up Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Set-up Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{SD}	Set-up Time for Data In	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

WRITE CYCLE

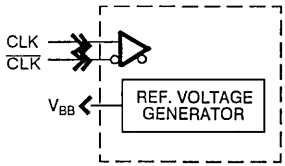


RISE/FALL TIME

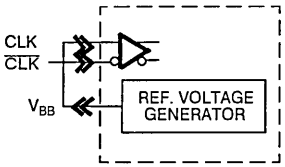
SYMBOL	PARAMETER	TEST CONDITION	IDT10496RL MIN.	IDT10496RL TYP.	IDT10496RL MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

CLOCK INPUT

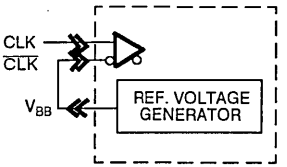
The clock input circuit in the IDT10496RL has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better rejection of common-mode noise and is obtained by driving both true and complement CLK lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising edge-active, as shown in Figures (b) and (c), respectively.



(a) Differential Mode

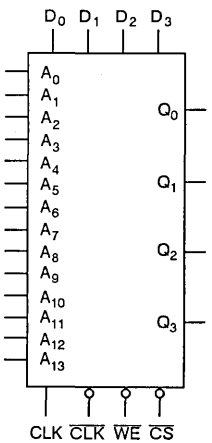


(b) Falling-Edge-Active Single-Ended Mode

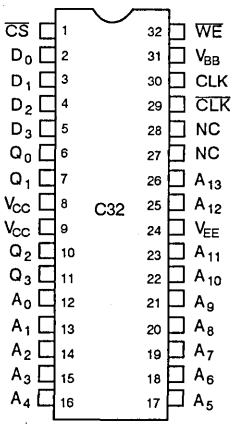


(c) Rising-Edge-Active Single-Ended Mode

LOGIC SYMBOL



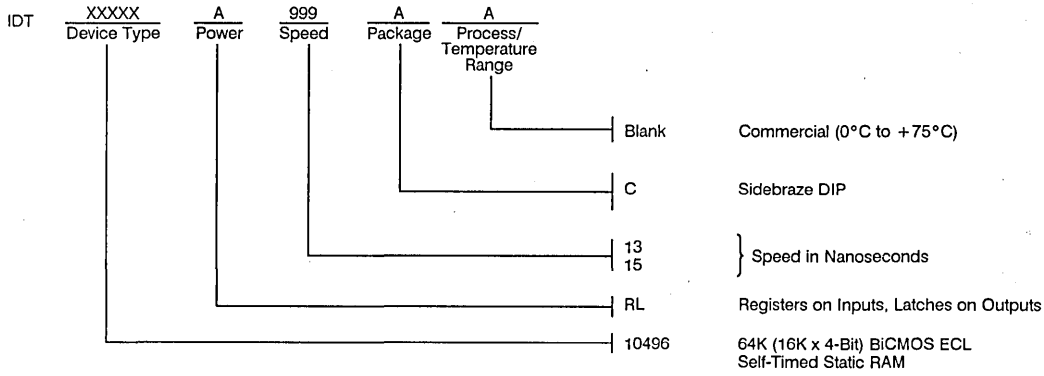
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY INFORMATION IDT 100496RL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Cycle time 13/15ns
- Address access time: 10/12ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

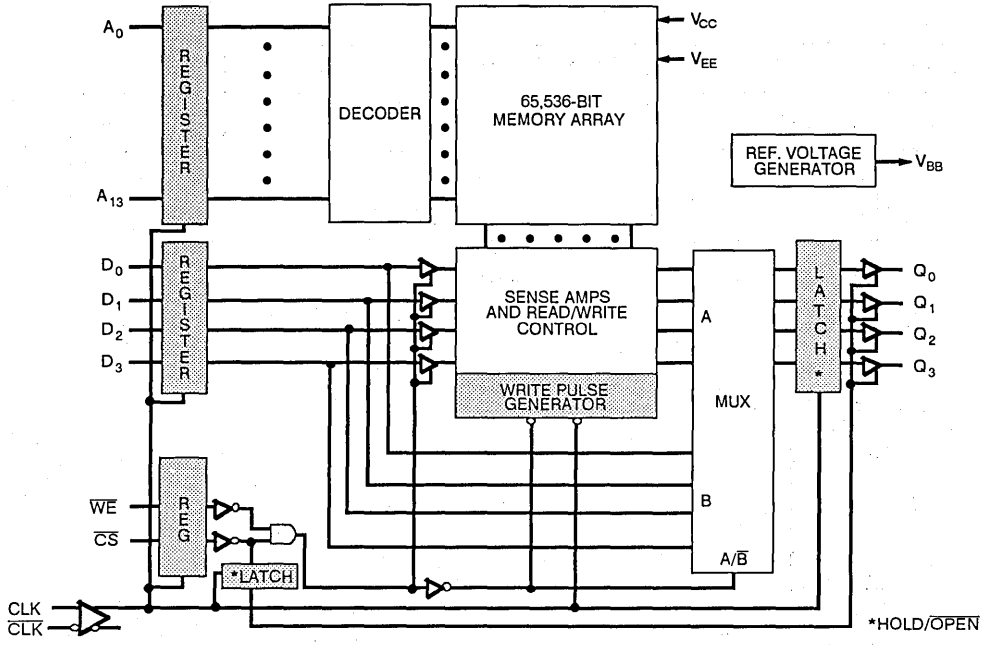
DESCRIPTION:

The IDT100496RL is a 65,536-bit high-speed BiCEMOS™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL-100K levels. This device has on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, the IDT100496RL allows cycle times as fast as 15ns.

The IDT100496RL is fabricated using IDT's high-performance, high-reliability BiCEMOS technology. It offers the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	+0.5 to -7.0	V
T_A	Operating Temperature	0 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (Output High)	-50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance except CLK	4	–	pF
C_{IN}	Input Capacitance CLK	6	–	pF
C_{OUT}	I/O Capacitance	6	–	pF

TRUTH TABLE (1)

$\overline{CS}$	$\overline{WE}$	CLK	$DATA_{OUT}$(2)	FUNCTION
H	X	↓	L	Deselected
L	H	↓	RAM Data	Read
L	L	↓	WRITE Data	Write

NOTES:

1. H = High, L = Low, X = Don't Care
2. $DATA_{OUT}$ changes when CLK returns high.

DC ELECTRICAL CHARACTERISTICS

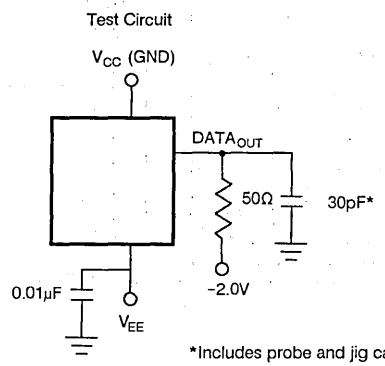
(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN. (B)	TYP.(1)	MAX. (A)	UNIT
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage High/Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	–	
I_{EE}	Supply Current	All inputs and outputs open		-180	-150	–	mA

NOTE:

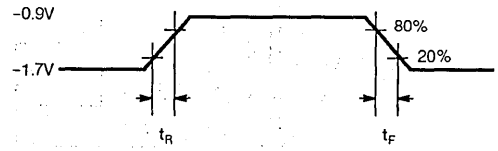
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

LOAD CONDITION



*Includes probe and jig capacitance.

INPUT PULSE



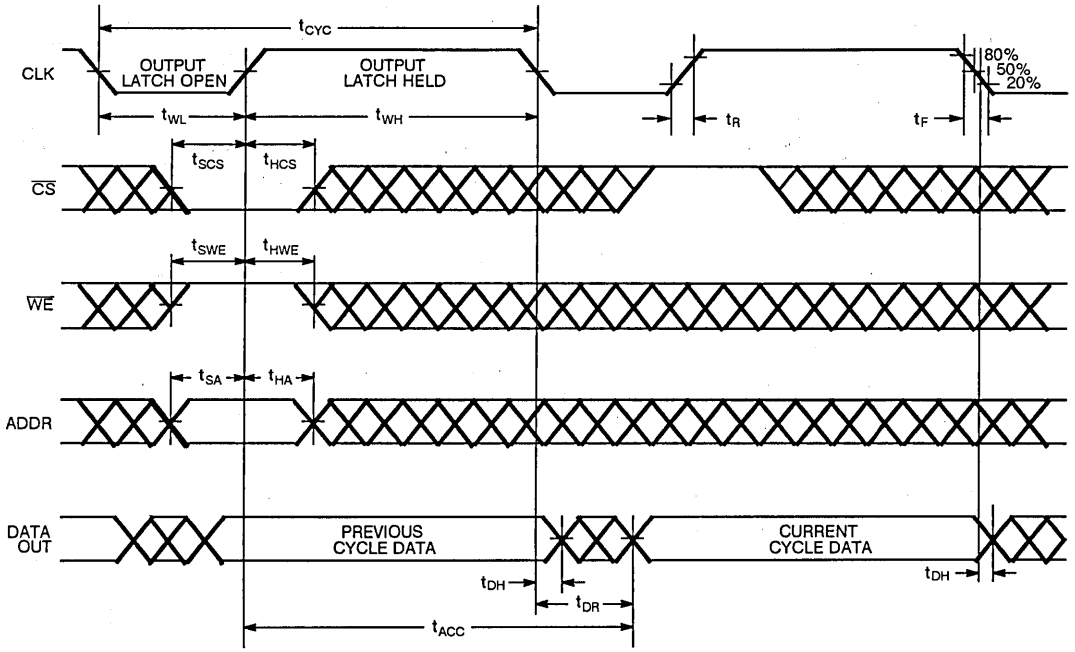
t_R = t_F = 2.0ns typ.

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496RL13 MIN.	IDT100496RL13 MAX.	IDT100496RL15 MIN.	IDT100496RL15 MAX.	UNIT
READ CYCLE GATED BY ADDRESS[2]							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{ACC}[3]	Access Time from Clock High	–	–	10	–	12	ns
t_{WL}	Clock Low Pulse Width	–	5	–	5	–	ns
t_{WH}	Clock High Pulse Width	–	7.5	–	7.5	–	ns
t_{SCS}	Set-up Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Set-up Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{SD}	Set-up Time for Data In	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns
t_{DH}	Data Hold from Clock Low	–	0	–	0	–	ns
t_{DR}[3]	Data Ready from Clock Low	–	0	4	0	4	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Set-up and Hold Times are the same as for Write Cycle.
3. Access time is the larger of t_{ACC} or $t_{WH} + t_{DH}$.

READ CYCLE



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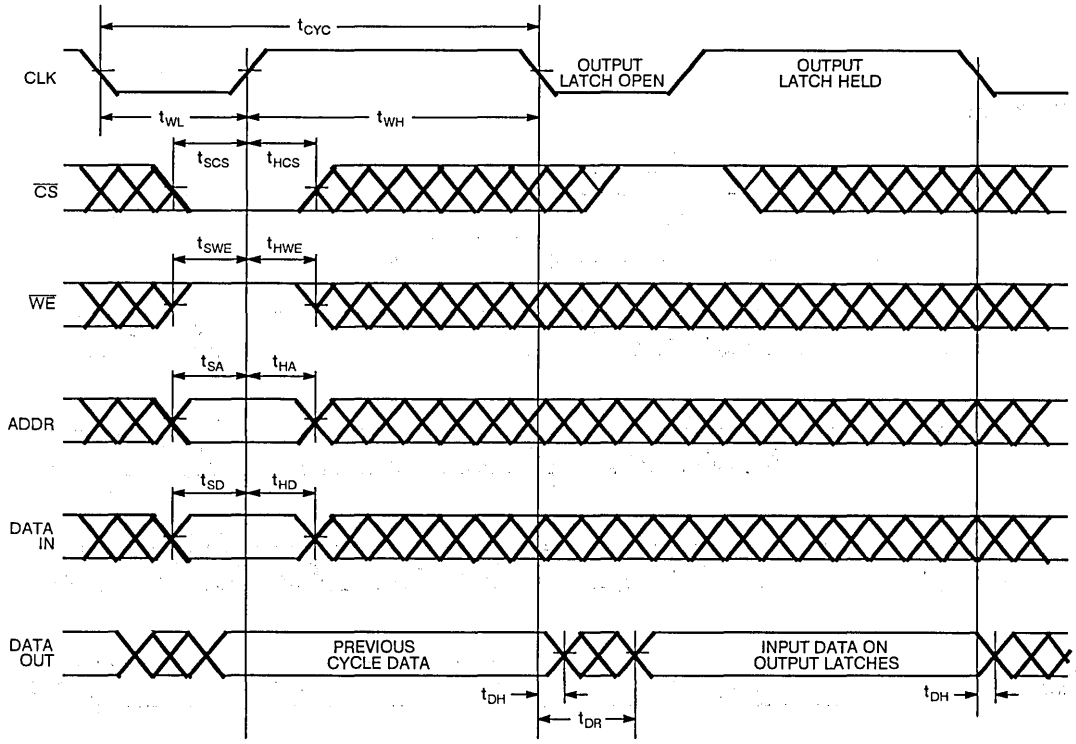
AC ELECTRICAL CHARACTERISTICS (V_{EE} = -4.5V ± 5%, T_A = 0 to +85°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER[1]	TEST CONDITION	IDT100496RL13 MIN.	IDT100496RL13 MAX.	IDT100496RL15 MIN.	IDT100496RL15 MAX.	UNIT
WRITE CYCLE							
t_{CYC}	Cycle Time	–	13	–	15	–	ns
t_{WL}	Clock Low Pulse Width	–	5	–	5	–	ns
t_{WH}	Clock High Pulse Width	–	7.5	–	7.5	–	ns
t_{SCS}	Set-up Time for Chip Select	–	1	–	1	–	ns
t_{SWE}	Set-up Time for Write Enable	–	1	–	1	–	ns
t_{SA}	Set-up Time for Address	–	1	–	1	–	ns
t_{SD}	Set-up Time for Data In	–	1	–	1	–	ns
t_{HCS}	Hold Time for Chip Select	–	2	–	2	–	ns
t_{HWE}	Hold Time for Write Enable	–	2	–	2	–	ns
t_{HA}	Hold Time for Address	–	2	–	2	–	ns
t_{HD}	Hold Time for Data In	–	2	–	2	–	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

WRITE CYCLE

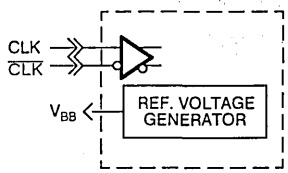


RISE/FALL TIME

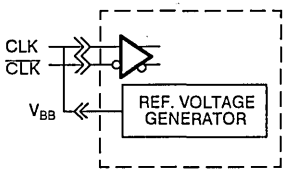
SYMBOL	PARAMETER	TEST CONDITION	IDT100496RL MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

CLOCK INPUT

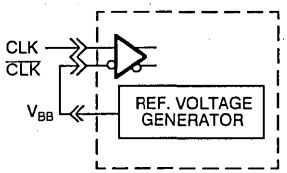
The clock input circuit in the IDT100496RL has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better rejection of common-mode noise and is obtained by driving both true and complement CLK lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising edge-active, as shown in Figures (b) and (c), respectively.



(a) Differential Mode

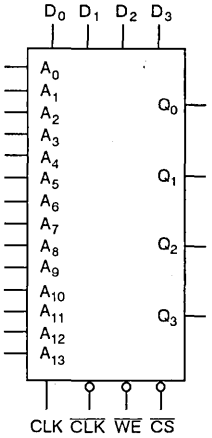


(b) Falling-Edge-Active Single-Ended Mode

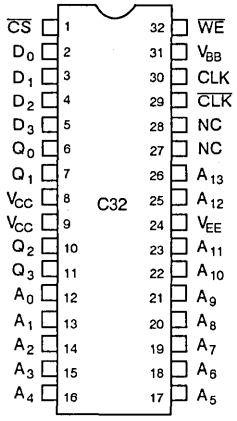


(c) Rising-Edge-Active Single-Ended Mode

LOGIC SYMBOL



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

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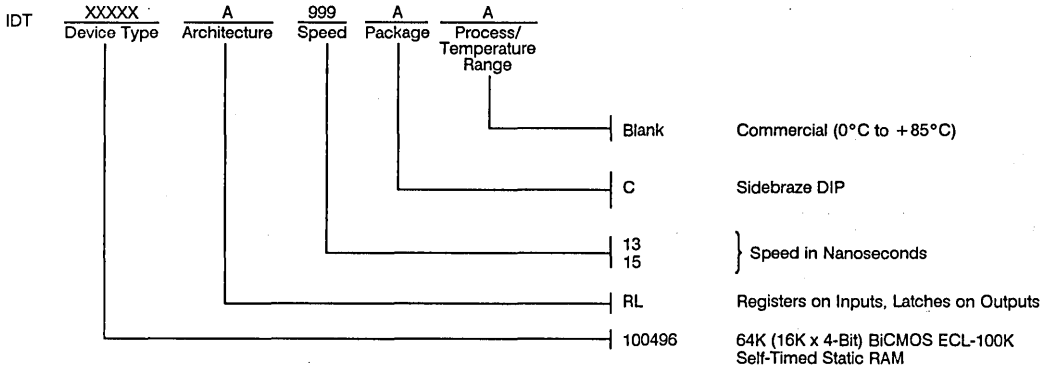
ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) WITH SYNCHRONOUS WRITE

ADVANCE INFORMATION
IDT 10497
IDT 100497

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 12/15ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Internal Circuitry Allows Synchronous Write Operation
- Tight Input Data Set-Up and Hold Timing
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

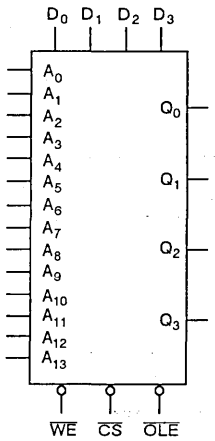
The IDT10497 and IDT100497 are 65,536-bit high-speed BiCEMOS™ ECL static random access memory organized as 16K x 4, with inputs and outputs fully compatible with ECL 10K levels and ECL 100K, respectively.

Available with address access times as fast as 12ns, these devices exhibit a typical power consumption of only 800mW. They offer the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

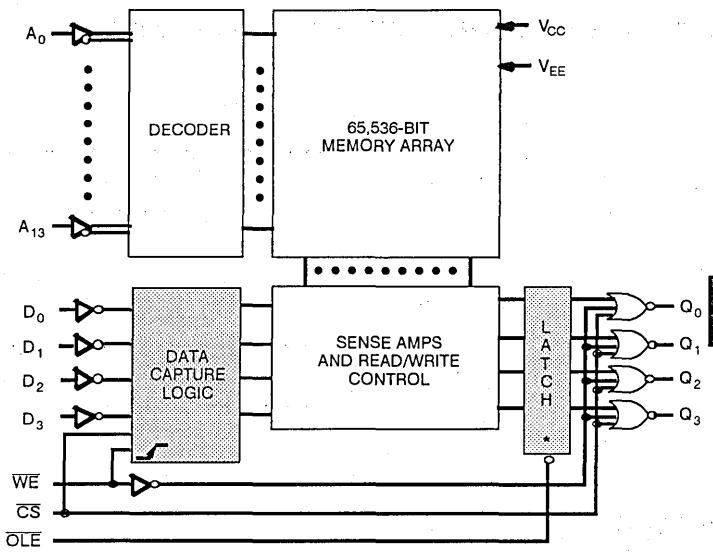
Designed for synchronous applications, the IDT10497 and IDT100497 include Data Capture Logic which allows very tight specifications for Input Data Set-Up and Hold with respect to the trailing edge of $\overline{WE}$. This allows relaxed timing or a pipeline stage in the datapath. An output latch with enable allows control of output hold time. Note that when OLE is tied low, the IDT10497 functions exactly as an IDT10494 asynchronous SRAM.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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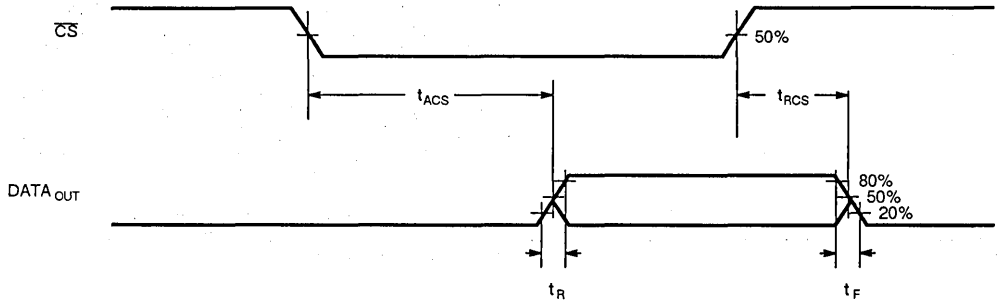
BiCEMOS is a trademark of Integrated Device Technology, Inc.

AC ELECTRICAL CHARACTERISTICS

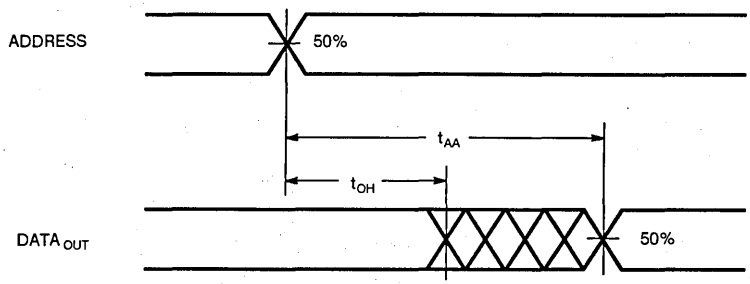
SYMBOL	PARAMETER	TEST CONDITION	IDT10497S12 IDT100497S12 MIN.	IDT10497S12 IDT100497S12 MAX.	IDT10497S15 IDT100497S15 MIN.	IDT10497S15 IDT100497S15 MAX.	UNIT
READ CYCLE, ASYNCHRONOUS MODE[1]							
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{AA}	Address Access Time	–	–	12	–	15	ns
t_{OH}	Data Hold from Address Change	–	TBD	–	TBD	–	ns

NOTE:
1. Asynchronous mode when Output Latch Enable ($\overline{OLE}$) is held low.

ASYNCHRONOUS[1] READ CYCLE GATED BY CHIP SELECT



ASYNCHRONOUS[1] READ CYCLE GATED BY ADDRESS



RISE/FALL TIME

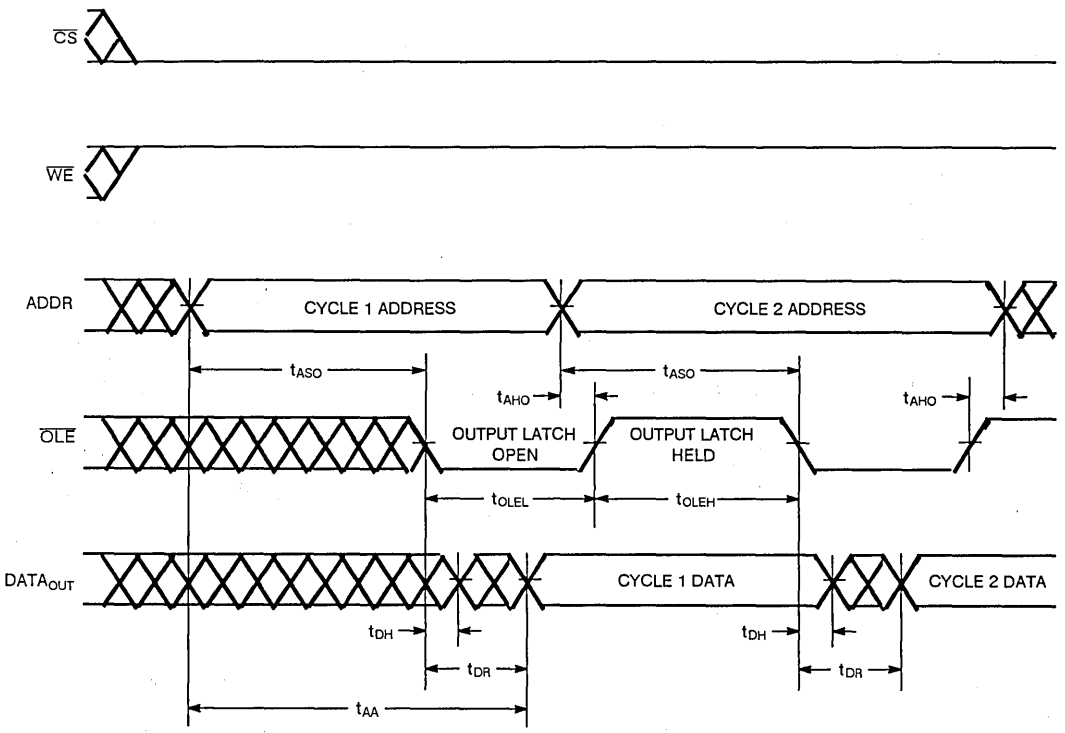
SYMBOL	PARAMETER	TEST CONDITION	IDT10497 IDT100497 MIN.	IDT10497 IDT100497 TYP.	IDT10497 IDT100497 MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10497S12 IDT100497S12 MIN.	MAX.	IDT10497S15 IDT100497S15 MIN.	MAX.	UNIT
SYNCHRONOUS READ CYCLE GATED BY ADDRESS							
t_{AA}(2)	Address Access Time	–	–	12	–	15	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{OLEH}(3)	Latch Enable High Pulse Width	–	6	–	7.5	–	ns
t_{ASO}(3)	Address Set-up to $\overline{OLE}$ Low	–	9	–	12	–	ns
t_{AHO}(3)	Address Hold to $\overline{OLE}$ High	–	-3	–	-3	–	ns
t_{DH}	Data Out Hold from $\overline{OLE}$ Low	–	0	–	0	–	ns
t_{DR}(2)	Data Out Ready from $\overline{OLE}$ Low	–	0	3	0	3	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of t_{AA} or t_{ASO} + t_{DR}.
3. t_{ASO} must equal t_{OLEH} -t_{AHO}.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{ASO} > t_{AA}$ (max) and $t_{CSO} > t_{ACS}$ (max) and $t_{WSA} + t_W + t_{WR} > t_{AA}$ (max).

SYNCHRONOUS READ CYCLE GATED BY ADDRESS

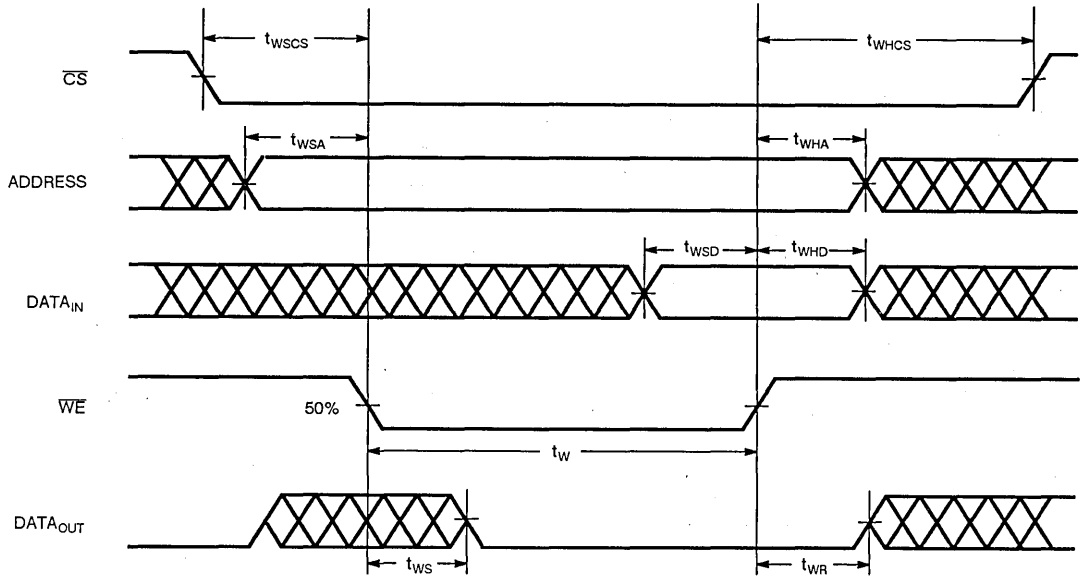


AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	IDT10497S12 IDT100497S12 MIN.	MAX.	IDT10497S15 IDT100497S15 MIN.	MAX.	UNIT
ASYNCHRONOUS[1] WRITE CYCLE							
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	12	–	ns
t_{WSD}	Data Set-up Time	–	1	–	2	–	ns
t_{WHD}	Data Hold Time	–	2	–	3	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum	1	–	2	–	ns
t_{WHA}	Address Hold Time	–	2	–	3	–	ns
t_{WSCS}	Chip Select Set-up Time	–	0	–	0	–	ns
t_{WHCS}	Chip Select Hold Time	–	2	–	3	–	ns
t_{WS}	Write Disable Time	–	–	5	–	5	ns
t_{WR}[2]	Write Recovery Time	–	–	5	–	5	ns

NOTES:
1. Asynchronous mode when Output Latch Enable ($\overline{OLE}$) is held low.
2. t_{WR} is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.

ASYNCHRONOUS WRITE CYCLE

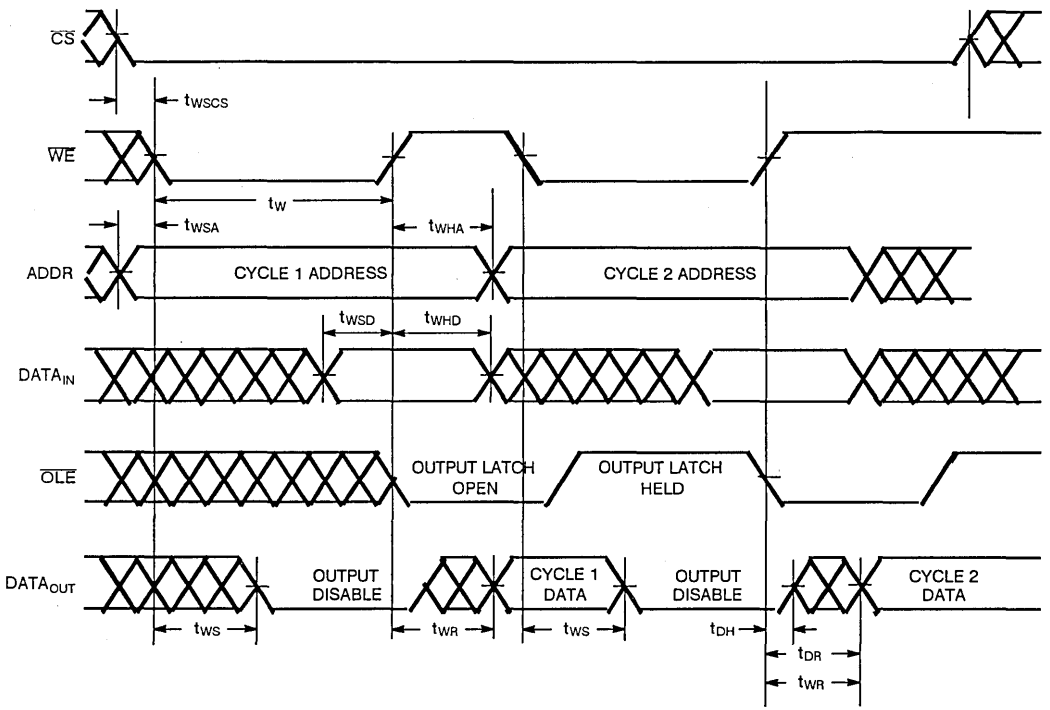


AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10497S12 IDT100497S12 MIN.	MAX.	IDT10497S15 IDT100497S15 MIN.	MAX.	UNIT
SYNCHRONOUS WRITE CYCLE							
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	12	–	ns
t_{WSD}	Data Set-up Time	–	1	–	2	–	ns
t_{WHD}	Data Hold Time	–	2	–	3	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum	1	–	2	–	ns
t_{WHA}	Address Hold Time	–	2	–	3	–	ns
t_{WSCS}	Chip Select Set-up Time	–	0	–	0	–	ns
t_{WHCS}	Chip Select Hold Time	–	2	–	3	–	ns
t_{WS}	Write Disable Time	–	–	5	–	5	ns
t_{WR}(1)	Write Recovery Time	–	–	5	–	5	ns
t_{DH}	Data Out Hold from $\overline{OLE}$ Low	–	0	–	0	–	ns
t_{DR}(2)	Data Out Ready from $\overline{OLE}$ Low	–	0	3	0	3	ns

NOTE:
1. t_{WR} is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.
2. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{ASO} > t_{AA}$ (max) and $t_{CSO} > t_{ACS}$(max) and $t_{WSA} + t_W + t_{WR} > t_{AA}$ (max).

SYNCHRONOUS WRITE CYCLE



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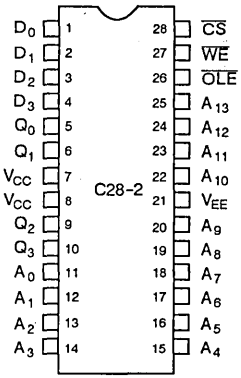
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) WITH CONDITIONAL WRITE

ADVANCE INFORMATION
IDT 10498
IDT 100498

FEATURES:

- 16,384-words x 4-bit organization
- Address access time: 12/15ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Internal Circuitry Allows Conditional Write Operation
- Tight Input Data Set-Up and Hold Timing
- $\overline{CE}$ allows very late termination of Write function
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

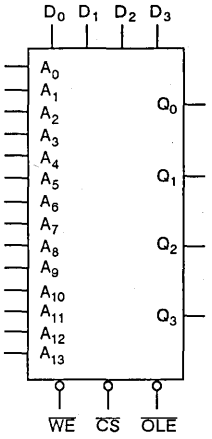
The IDT10498 and IDT100498 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K, respectively.

Available with address access times as fast as 12ns, these devices exhibit a typical power consumption of only 800mW. They offer the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

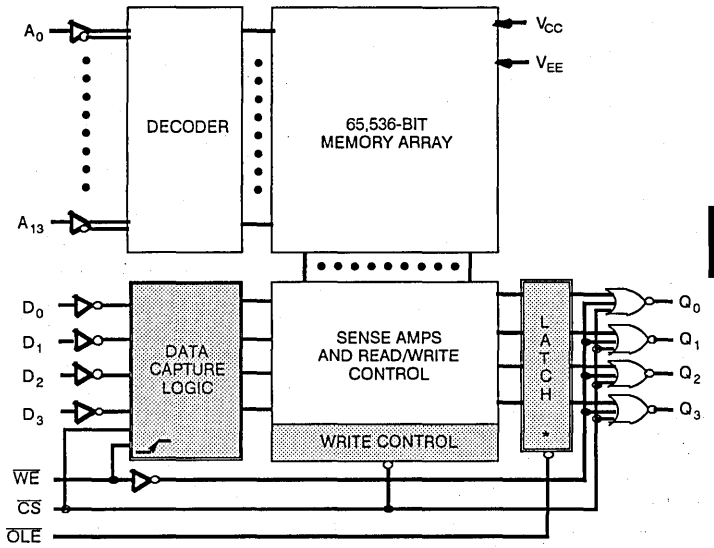
Designed for cache applications, the IDT10498 and IDT100498 include Data Capture Logic which allows very tight specifications for Input Data Set-Up and Hold with respect to the trailing edge of $\overline{WE}$. This allows relaxed timing or a pipeline stage in the datapath. An output latch with enable allows control of output hold time. Note that when $\overline{OLE}$ is tied low, the device functions exactly as an IDT10494 asynchronous SRAM. Additionally, the IDT10498 and IDT100498 incorporate logic to terminate the Write Operation very late in the cycle by removing $\overline{CE}$, providing more time for cache—hit decision logic.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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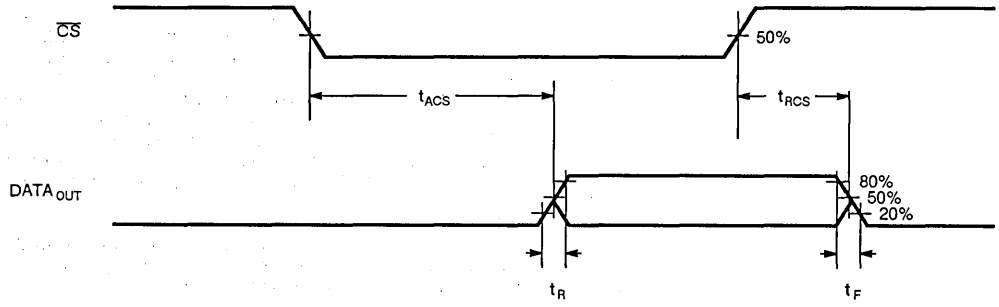
AC ELECTRICAL CHARACTERISTICS

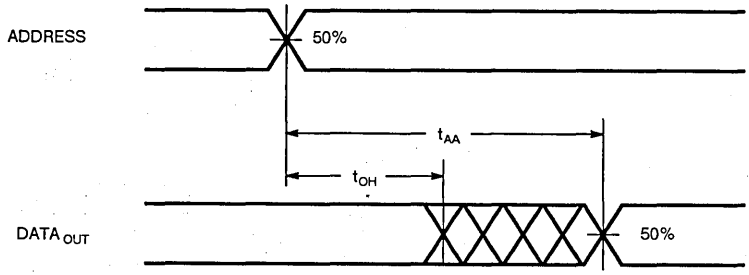
SYMBOL	PARAMETER	TEST CONDITION	IDT10498S12 IDT100498S12 MIN.		IDT10498S15 IDT100498S15 MIN.		UNIT
				MAX.		MAX.	
READ CYCLE, ASYNCHRONOUS MODE [1]							
t_{ACS}	Chip Select Access Time	–	–	5	–	5	ns
t_{RCS}	Chip Select Recovery Time	–	–	5	–	5	ns
t_{AA}	Address Access Time	–	–	12	–	15	ns
t_{OH}	Data Hold from Address change	–	TBD	–	TBD	–	ns

NOTE:
1. Asynchronous mode when Output Latch Enable ($\overline{OLE}$) is held low.

ASYNCHRONOUS[1] READ CYCLE GATED BY CHIP SELECT



ASYNCHRONOUS[1] READ CYCLE GATED BY ADDRESS



RISE/FALL TIME

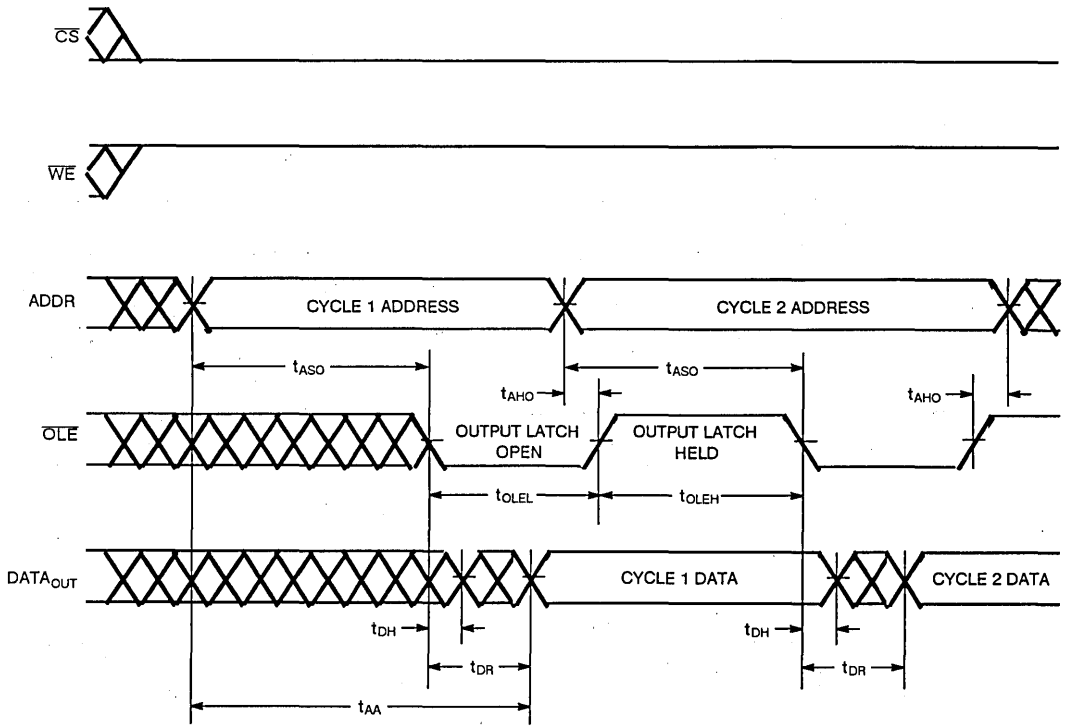
SYMBOL	PARAMETER	TEST CONDITION	IDT10498 IDT100498 MIN.	TYP.	MAX.	UNIT
t_R	Output Rise Time	–	–	2	–	ns
t_F	Output Fall Time	–	–	2	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER [1]	TEST CONDITION	IDT10498S12 IDT100498S12 MIN.	IDT10498S12 IDT100498S12 MAX.	IDT10498S15 IDT100498S15 MIN.	IDT10498S15 IDT100498S15 MAX.	UNIT
SYNCHRONOUS READ CYCLE GATED BY ADDRESS							
t_{AA}[2]	Address Access Time	–	–	12	–	15	ns
t_{OLEL}	Latch Enable Low Pulse Width	–	5	–	5	–	ns
t_{OLEH}[3]	Latch Enable High Pulse Width	–	6	–	7.5	–	ns
t_{ASO}[3]	Address Set-up to $\overline{OLE}$ Low	–	9	–	12	–	ns
t_{AHO}[3]	Address Hold to $\overline{OLE}$ High	–	-3	–	-3	–	ns
t_{DH}	Data Out Hold from $\overline{OLE}$ Low	–	0	–	0	–	ns
t_{DR}[2, 4]	Data Out Ready from $\overline{OLE}$ Low	–	0	3	0	3	ns

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of t_{AA} or t_{ASO} + t_{DR}.
3. t_{ASO} must equal t_{OLEH} -t_{AHO}.
4. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when t_{ASO} > t_{AA} (max) and t_{WSCS} > t_{ACS} (max) and rising edge of $\overline{WE}$ preceeds falling edge of $\overline{OE}$ such that t_{WR} (max) preceeds t_{DR} (max).

SYNCHRONOUS READ CYCLE GATED BY ADDRESS



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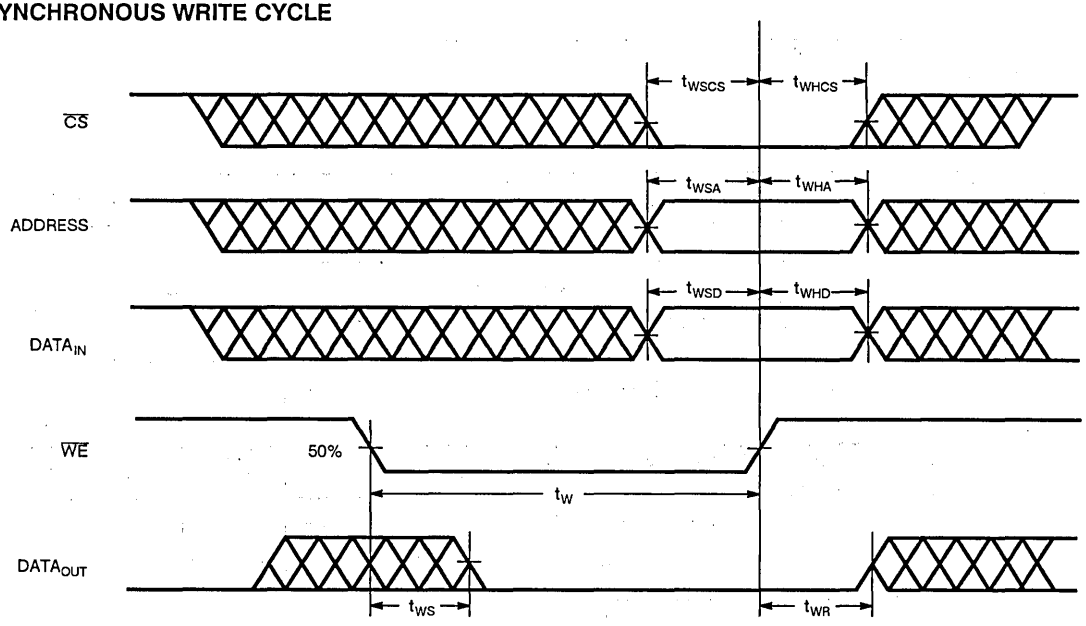
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	IDT10498S12 IDT100498S12 MIN.	MAX.	IDT10498S15 IDT100498S15 MIN.	MAX.	UNIT
ASYNCHRONOUS[1] WRITE CYCLE							
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	12	–	ns
t_{WSD}	Data Set-up Time	–	1	–	2	–	ns
t_{WHD}	Data Hold Time	–	2	–	3	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum	1	–	2	–	ns
t_{WHA}	Address Hold Time	–	2	–	3	–	ns
t_{WSCS}	Chip Select Set-up Time	–	1	–	2	–	ns
t_{WHCS}	Chip Select Hold Time	–	2	–	3	–	ns
t_{WS}	Write Disable Time	–	–	5	–	5	ns
t_{WR}[2]	Write Recovery Time	–	–	5	–	5	ns

NOTES:
1. Asynchronous mode when Output Latch Enable ($\overline{OLE}$) is held low.
2. t_{WR} is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.

ASYNCHRONOUS WRITE CYCLE

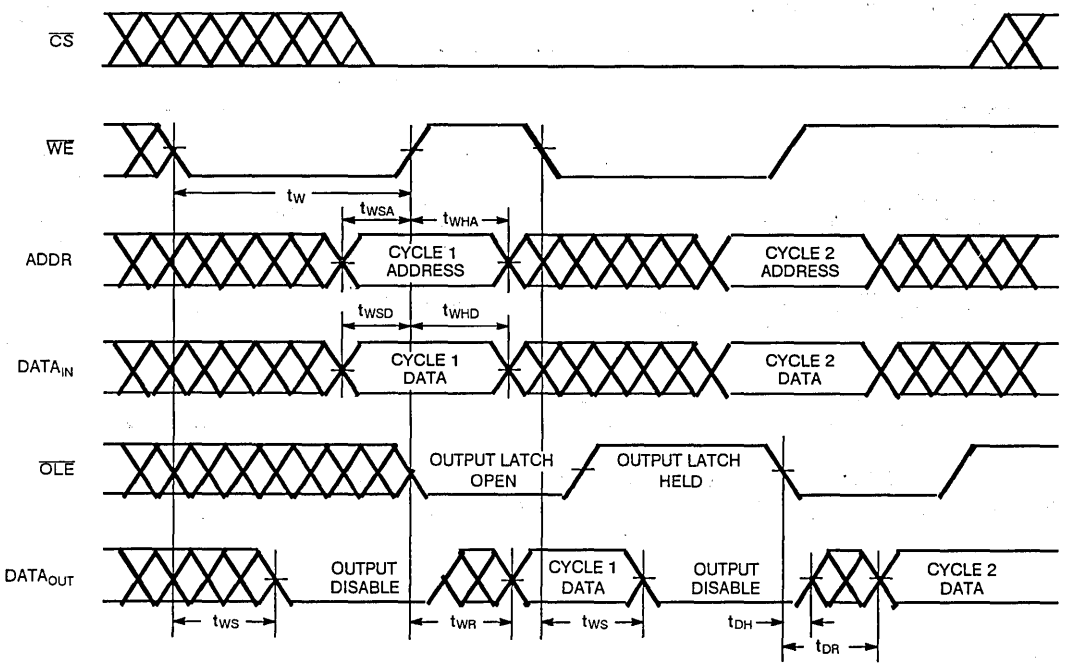


AC ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2V ± 5%, T_A = 0 to +75°C, air flow exceeding 2m/sec)

SYMBOL	PARAMETER	TEST CONDITION	IDT10498S12 IDT100498S12 MIN.	MAX.	IDT10498S15 IDT100498S15 MIN.	MAX.	UNIT
SYNCHRONOUS WRITE CYCLE							
t_W	Write Pulse Width	t_{WSA} = minimum	10	–	12	–	ns
t_{WSD}	Data Set-up Time	–	1	–	2	–	ns
t_{WHD}	Data Hold Time	–	2	–	3	–	ns
t_{WSA}	Address Set-up Time	t_W = minimum	1	–	2	–	ns
t_{WHA}	Address Hold Time	–	2	–	3	–	ns
t_{WS}	Write Disable Time	–	–	5	–	5	ns
t_{WR}(1)	Write Recovery Time	–	–	5	–	5	ns
t_{DH}	Data Out Hold from $\overline{OLE}$ Low	–	0	–	0	–	ns
t_{DR}(2)	Data Out Ready from $\overline{OLE}$ Low	–	0	3	0	3	ns

NOTES:
1. t_{ASO} is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address transition occurs.
2. t_{DR} (max) is specified when all other gating conditions have been satisfied, specifically when $t_{ASO} > t_{AA}$ (max) and $t_{WSCS} > t_{ACS}$ (max) and rising edge of $\overline{WE}$ preceeds falling edge of $\overline{OE}$ such that t_{WR} (max.) preceeds t_{DR} (max).

SYNCHRONOUS WRITE CYCLE

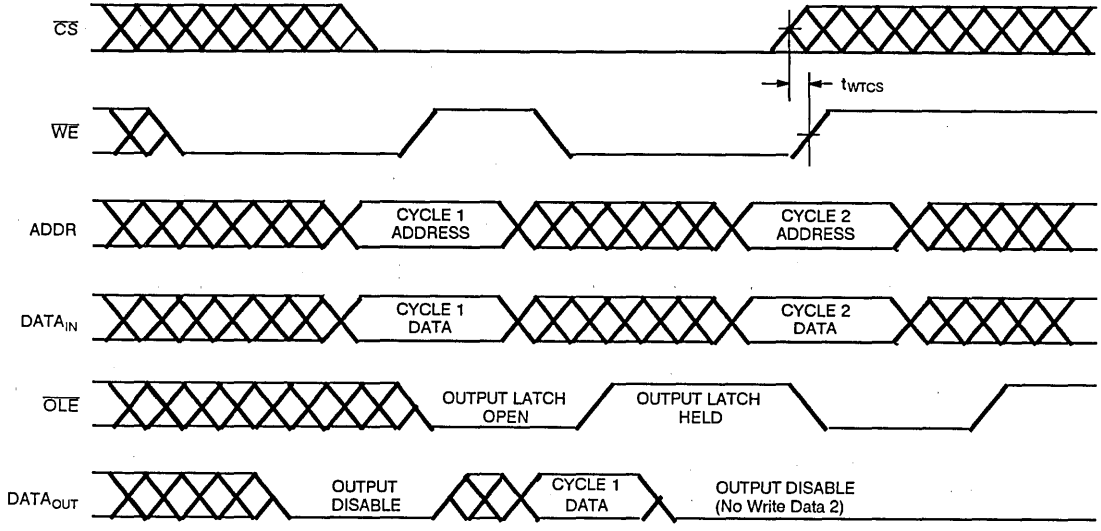


AC ELECTRICAL CHARACTERISTICS

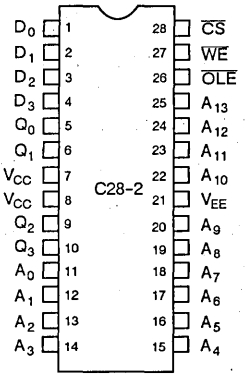
SYMBOL	PARAMETER	TEST CONDITION	IDT10498S12 IDT100498S12 MIN.	MAX.	IDT10498S15 IDT100498S15 MIN.	MAX.	UNIT
SYNCHRONOUS WRITE CYCLE, TERMINATED WRITE							
t_{WTCS}	$\overline{CS}$ Set-up, Terminated Write	–	2	–	2	–	ns

NOTE:
1. The Write Cycle is terminated, and no data written to the memory, when $\overline{CS}$ is unasserted t_{WTCS} before the rising edge of $\overline{WE}$.

SYNCHRONOUS WRITE CYCLE, TERMINATED WRITE



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT)

ADVANCE INFORMATION
IDT 10504
IDT 100504

FEATURES:

- 65,536-words x 4-bit organization
- Address access time: 12/15ns (max.)
- Low power dissipation: 600mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages
- Military version fully compliant to MIL-STD-883, class B.

DESCRIPTION:

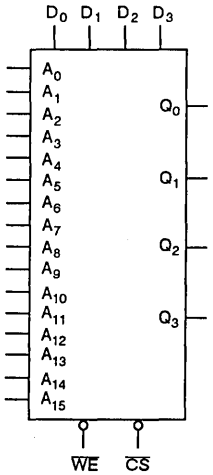
The IDT10504 and IDT100504 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K levels, respectively.

Available with address access times as fast as 12ns, this device exhibits a typical power consumption of only 600mW. It offers the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

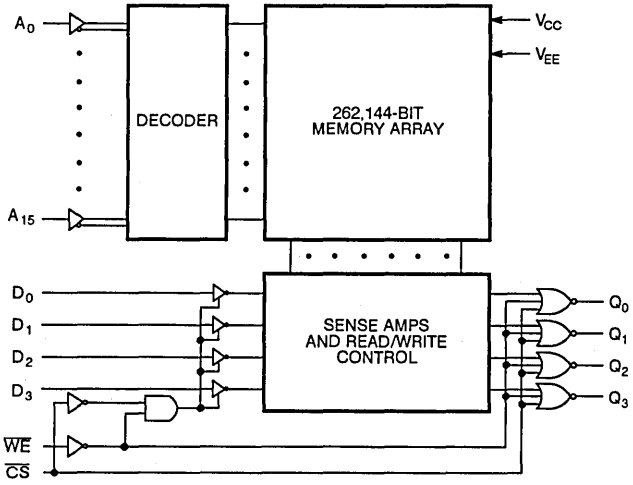
Designed for very high-speed applications, the IDT10504 and IDT100504 offer open emitter outputs and separate data input and output, as well as extremely fast access times. The address access time of 12ns assures that operation of this BiCEMOS part will be as fast as with less dense parts requiring external address decoding.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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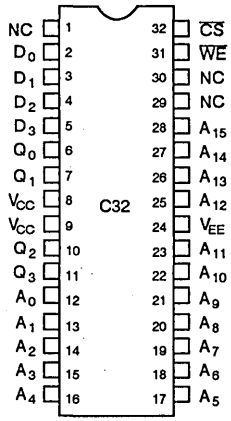
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 256K (64K x 4-BIT)

ADVANCE INFORMATION
IDT 10506LL
IDT 100506LL

FEATURES:

- 65,536-words x 4-bit organization
- Self-Timed, with latches on inputs and outputs
- Cycle time 15/18 ns
- Address access time: 12/15 ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

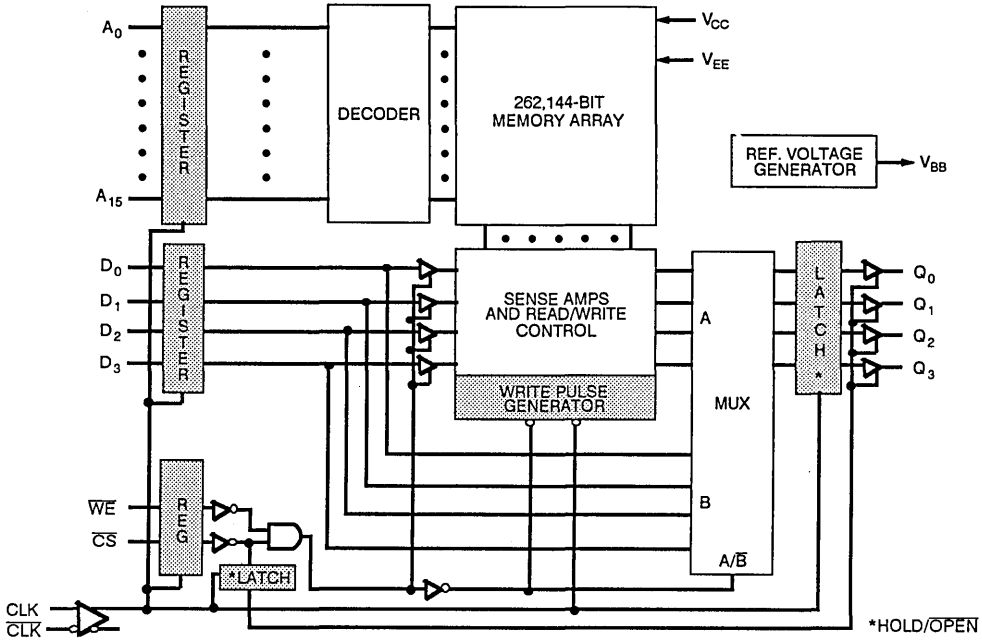
DESCRIPTION:

The IDT10506LL and IDT100506LL are 262,144-bit high-speed BiCEMOS™ ECL static random access memory organized as 64K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K levels, respectively. These devices have on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, these devices allow cycle times as fast as 15ns.

The IDT10506LL and IDT100506LL are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. They offer the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BiCEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM



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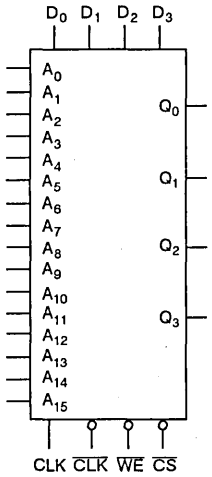
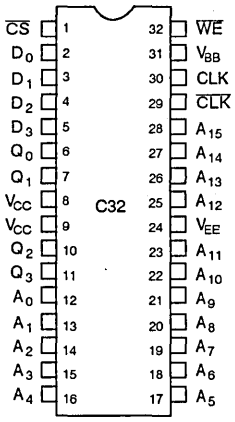
LOGIC SYMBOL



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL SELF-TIMED STATIC RAM 256K (64K x 4-BIT)

ADVANCE INFORMATION
IDT 10506RL
IDT 100506RL

FEATURES:

- 65,536-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Cycle time 15/18 ns
- Address access time: 12/15 ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

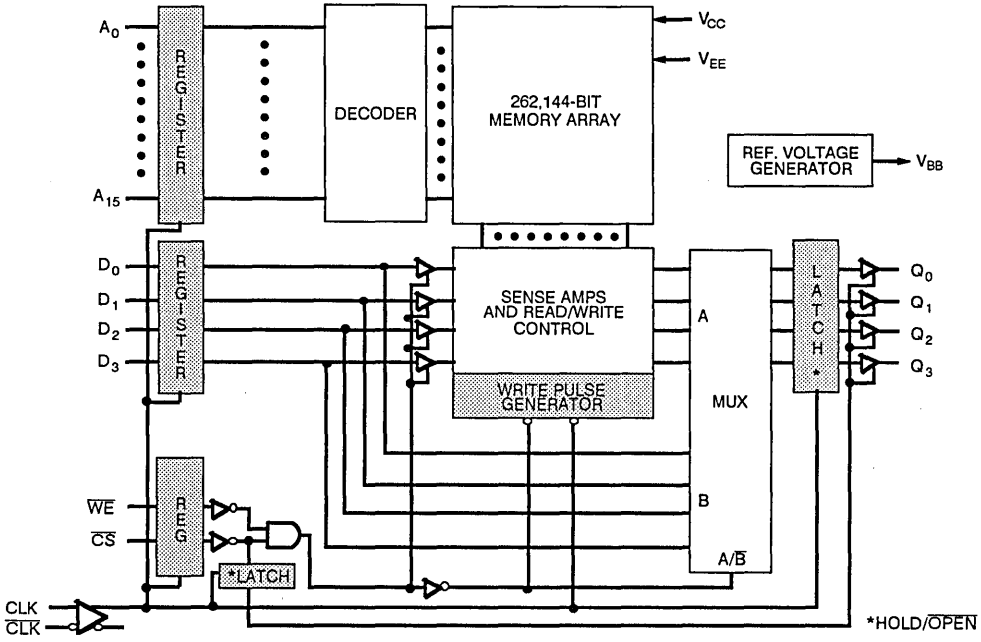
DESCRIPTION:

The IDT10506RL and IDT100506 are 262,144-bit high-speed BiCEMOS™ ECL static random access memory organized as 64K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K levels, respectively. These devices have on-board self-timed circuitry to relax control timing, providing easier design and improved system level cycle times.

Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs by removing the need to control any write pulse width, and relaxes timing of write enable ($\overline{WE}$). Combined with address access times as fast as 12ns, these devices allow cycle times as fast as 15ns.

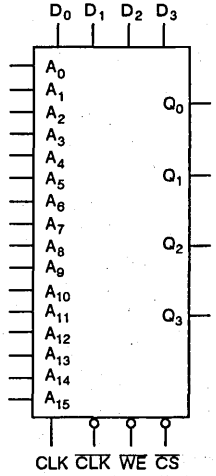
The IDT10506RL and IDT100506 are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. They offer the advantage of low-power operation without sacrificing speed by integrating a dense, high-speed CMOS static RAM and logic with internal level conversion. Power supply and cooling requirements are reduced, while the fast access time assures that operation of BICEMOS parts will be as fast as with less dense parts requiring external address decoding.

FUNCTIONAL BLOCK DIAGRAM

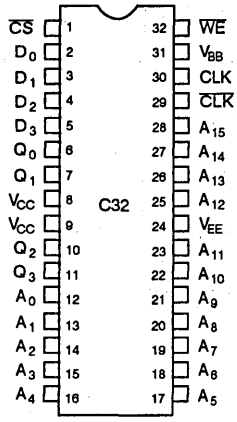


BiCEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL



PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) WITH SYNCHRONOUS WRITE

ADVANCE INFORMATION
IDT 10507
IDT 100507

FEATURES:

- 65,535-words x 4-bit organization
- Address access time: 12/15 ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Internal Circuitry Allows Synchronous Write Operation
- Tight Input Data Set-Up and Hold Timing
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

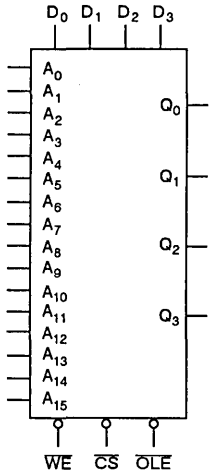
The IDT10507 and IDT100507 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K, respectively.

Available with address access times as fast as 12ns, these devices exhibit a typical power consumption of only 800mW. They offer the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

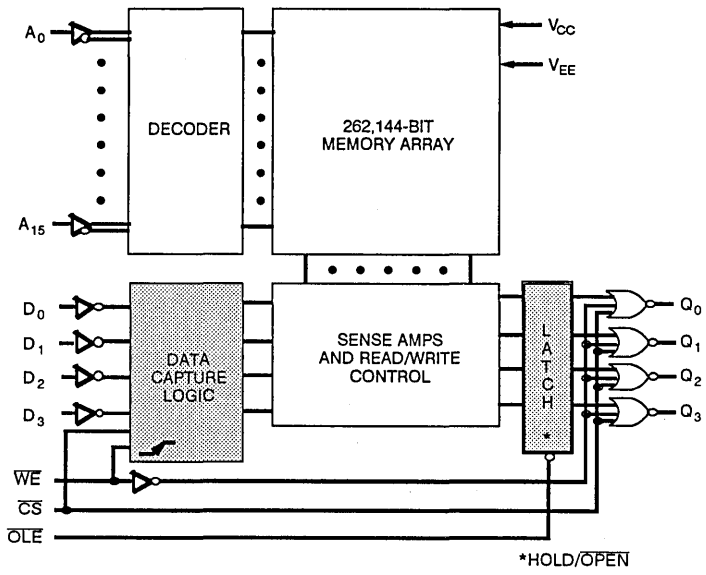
Designed for synchronous applications, the IDT10507 and IDT100507 include Data Capture Logic which allows very tight specifications for Input Data Set-Up and Hold with respect to the trailing edge of $\overline{WE}$. This allows relaxed timing or a pipeline stage in the datapath. An output latch with enable allows control of output hold time. Note that when $\overline{OLE}$ is tied low, the IDT10507 functions exactly as an IDT10504 assynchronous SRAM.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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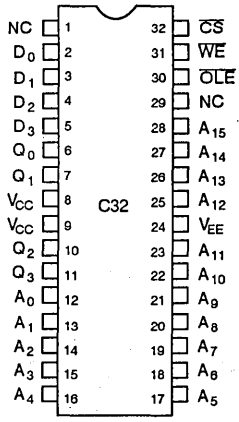
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) WITH CONDITIONAL WRITE

ADVANCE INFORMATION
IDT 10508
IDT 100508

FEATURES:

- 65,535-words x 4-bit organization
- Address access time: 12/15ns (max.)
- Low power dissipation: 800mW (typ.)
- Fully compatible with ECL logic levels
- Internal Circuitry Allows Synchronous Write Operation
- Tight Input Data Set-Up and Hold Timing
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

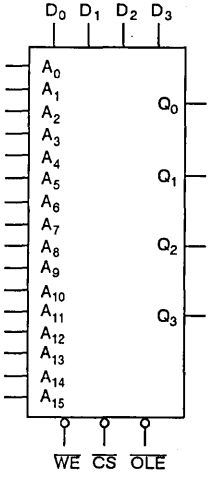
The IDT10508 and IDT100508 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 4, with inputs and outputs fully compatible with ECL-10K and ECL-100K, respectively.

Available with address access times as fast as 12ns, these devices exhibit a typical power consumption of only 800mW. They offer the advantages of low-power operation, without sacrificing speed, by integrating a dense high-speed CMOS static RAM with internal level conversion. This allows the designer to reduce package count in an ECL system without increasing either power dissipation or access time.

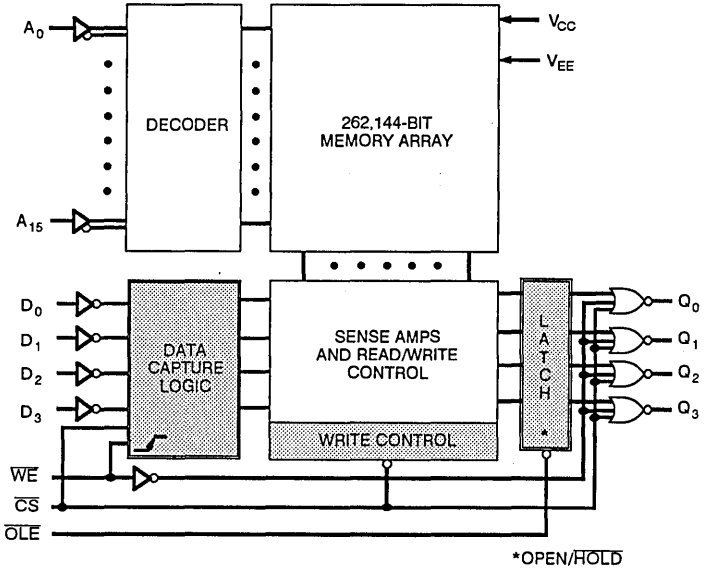
Designed for cache applications, the IDT10508 and IDT100508 include Data Capture Logic which allows very tight specifications for Input Data Set-Up and Hold with respect to the trailing edge of $\overline{WE}$. This allows relaxed timing or a pipeline stage in the datapath. An output latch with enable allows control of output hold time. Note that when $\overline{OLE}$ is tied low, the IDT10507 functions exactly as an IDT10504 asynchronous SRAM. The devices also incorporate logic to terminate the Write Operation very late in the cycle by removing $\overline{CE}$, providing more time for cache-hit decision logic.

The devices are fabricated using IDT's high-performance, high-reliability BiCEMOS technology. Operating power dissipation is extremely low compared with most ECL-compatible bipolar devices, lowering power supply and cooling requirements.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



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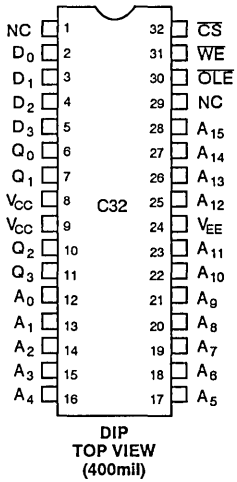
PIN CONFIGURATION



DIP
TOP VIEW
(400mil)

12

SUBSYSTEM PRODUCTS INTRODUCTION

A unique combination of resources and experience sets the Subsystems Division apart from its competitors. IDT's advanced technology, multiple manufacturing plants and the backing of sister divisions allow us to offer a diverse range of module products quickly and cost-effectively. In addition, our capabilities are flexible enough to include standard and custom modules, as well as a complete, self-contained, U.S.-based military device assembly and module operation.

IDT's subsystems provide a modular approach which allows designers to meet several important criteria needed in a modern electronics system. These features include:

- High Performance
- High Reliability
- High Density
- Low Power
- Quick Design Time
- Ease of Manufacture
- Competitive Cost

High-performance CMOS products in surface mounted packages are combined with thermally matched substrates to produce very dense and highly reliable modules. Conventional pins are then attached to these modules so that they can be plugged into a circuit board in a conventional through-hole manner.

This process allows production of a Megabit static RAM in a standard size dual in-line package several years before the available technology can produce a comparable monolithic device. In addition, an application specific product can be manufactured that could not be easily or cost-effectively produced as a monolithic device. These ASIC products can include error detection, parity, address latching or buffering and wide words (x16 and x32).

Complete memory systems, such as megabyte-size high-speed caches or writable control stores, can also be produced on a single plug-in module. Systems can now be designed with the major memory portions supplied as a single fully-tested high density component. This approach gives customers access to surface mount technology without the need to invest in special design, manufacturing and testing facilities.

TABLE OF CONTENTS

TABLE OF CONTENTS (CON'T.)

Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM MODULE

IDT 7M624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 4.8W (typ. in 64K x 16 organization)
  - Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin-compatible with IDT7M656 (256K RAM module)
- Single 5V(±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

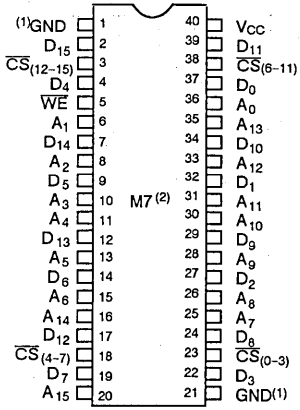
The IDT7M624 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 12.3W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 5.7W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

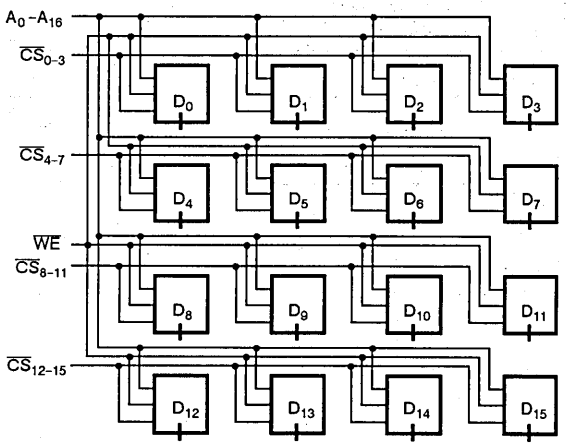


DIP
TOP VIEW

PIN NAMES

A_{0-16}	Address
D_{0-15}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. Both GND pins need to be grounded for proper operation.
2. For module dimensions, please refer to module drawing M7 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M624S MIN.	TYP.(1)	MAX.(3)	MAX.(4)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} =5.5V, V_{IN} = GND to V_{CC}	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}_{XX}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f=f_{MAX}	–	960	1950	2240	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	–	720	1380	1640	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	–	600	1100	1340	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{IH} (TTL Level), V_{CC} =5.5V, Output Open	–	480	820	1040	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V (CMOS Level)	–	0.32	320(2)	320	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	–	–	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	–	–	–	V

NOTES:

1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} max. at commercial temperature = 240mA.
3. t_{AA} = 30, 35, 45, 55, 65ns
4. t_{AA} = 25ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

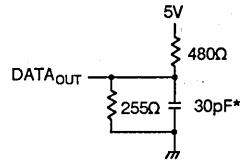


Figure 1. Output Load

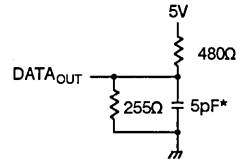


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to 70°C)

SYMBOL	PARAMETER	7M624S25 COM'L. ONLY MIN.	7M624S25 COM'L. ONLY MAX.	7M624S30 COM'L. ONLY MIN.	7M624S30 COM'L. ONLY MAX.	7M624S35 MIN.	7M624S35 MAX.	7M624S45 MIN.	7M624S45 MAX.	7M624S55 MIN.	7M624S55 MAX.	7M624S65 MIN.	7M624S65 MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	–	20	–	25	–	30	–	30	–	30	–	30	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Selection to Power Down Time	–	25	–	30	–	35	–	35	–	35	–	35	ns

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to 70°C)

SYMBOL	PARAMETER	7M624S25 COM'L. ONLY MIN.	7M624S25 COM'L. ONLY MAX.	7M624S30 COM'L. ONLY MIN.	7M624S30 COM'L. ONLY MAX.	7M624S35 MIN.	7M624S35 MAX.	7M624S45 MIN.	7M624S45 MAX.	7M624S55 MIN.	7M624S55 MAX.	7M624S65 MIN.	7M624S65 MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{CW}	Chip Selection to End of Write	22	–	25	–	30	–	40	–	50	–	55	–	ns
t_{AW}	Address Valid to End of Write	22	–	25	–	30	–	40	–	50	–	55	–	ns
t_{AS}	Address Set-up Time	2	–	3	–	5	–	5	–	5	–	10	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	20	–	25	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z	0	20	0	25	0	25	0	30	0	30	0	35	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

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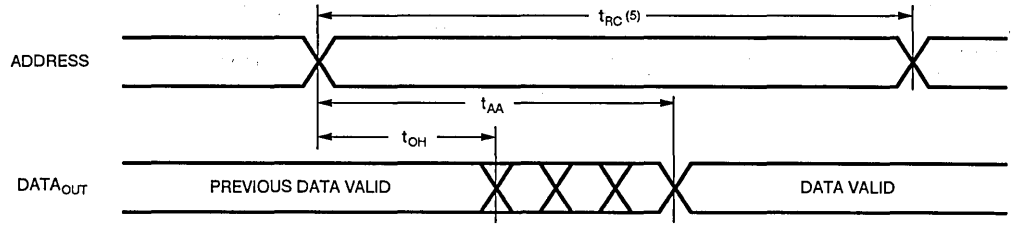
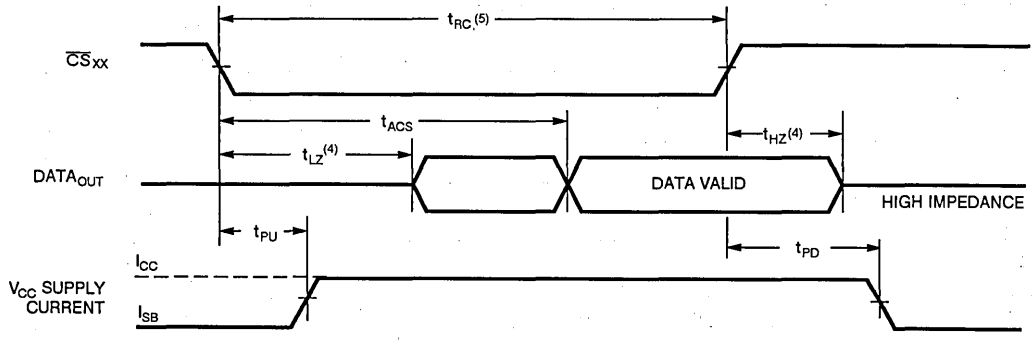
TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



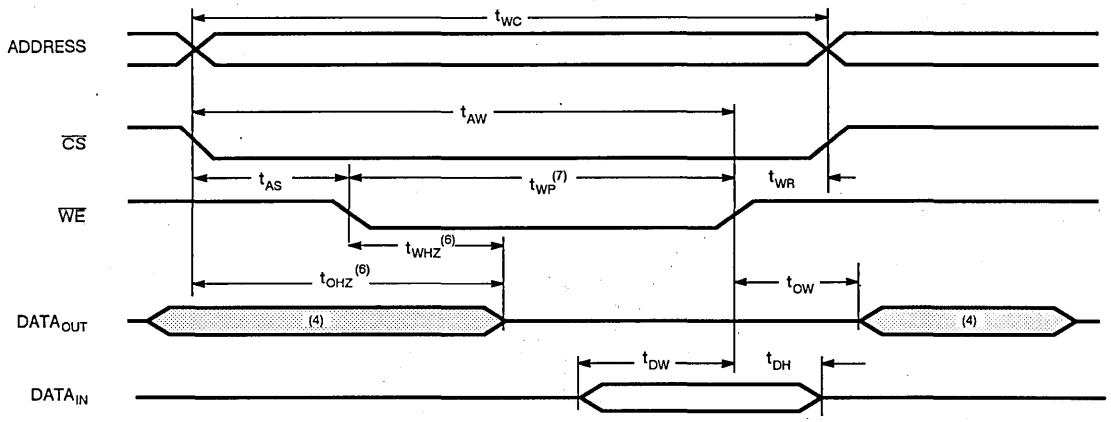
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



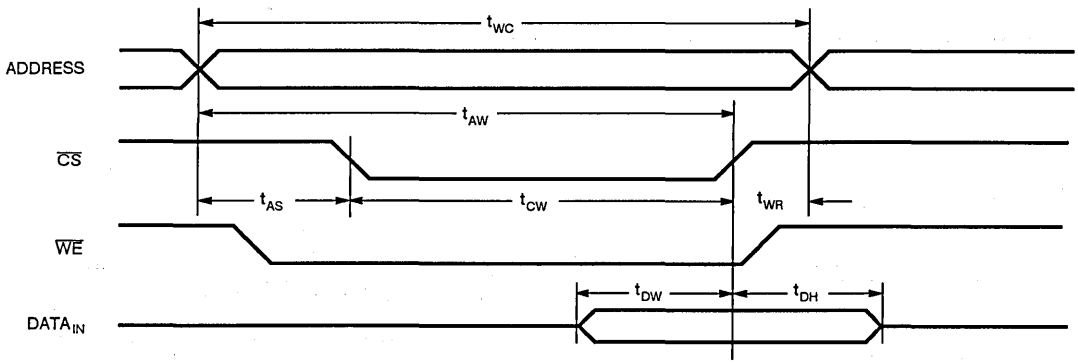
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



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NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

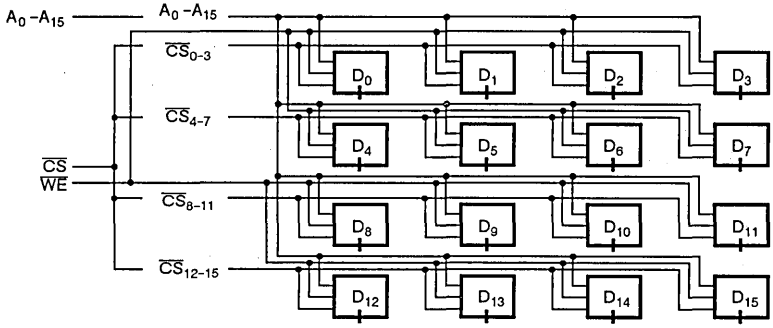
MODE	$\overline{CS}_{XX}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	130	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

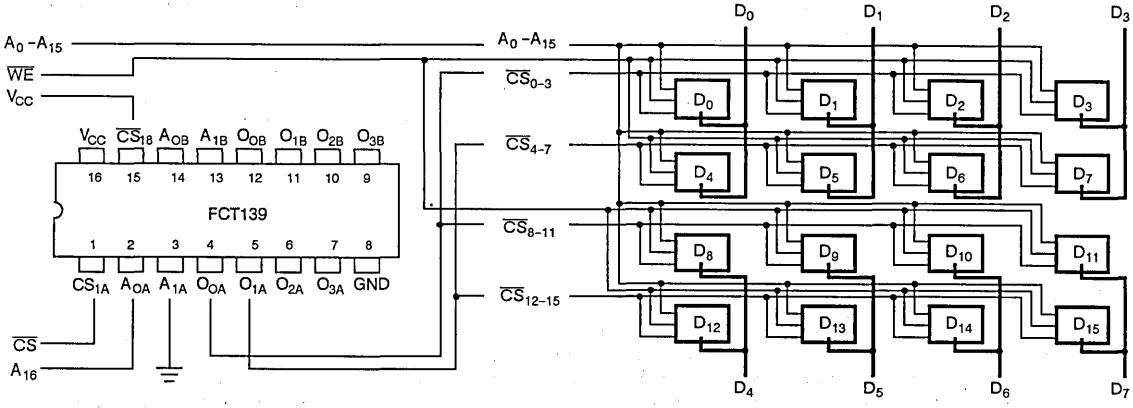
NOTE:
1. This parameter is sampled and not 100% tested.

IDT7M624
64K x 16 CONFIGURATION



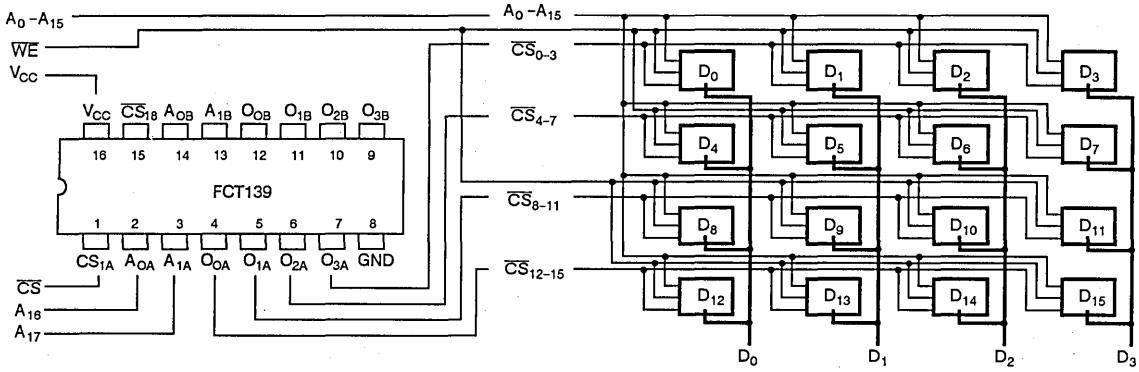
NOTE:
All chip selects tied together since, in a by 16 configuration, all chips are either on or off.

IDT7M624
128K x 8 CONFIGURATION



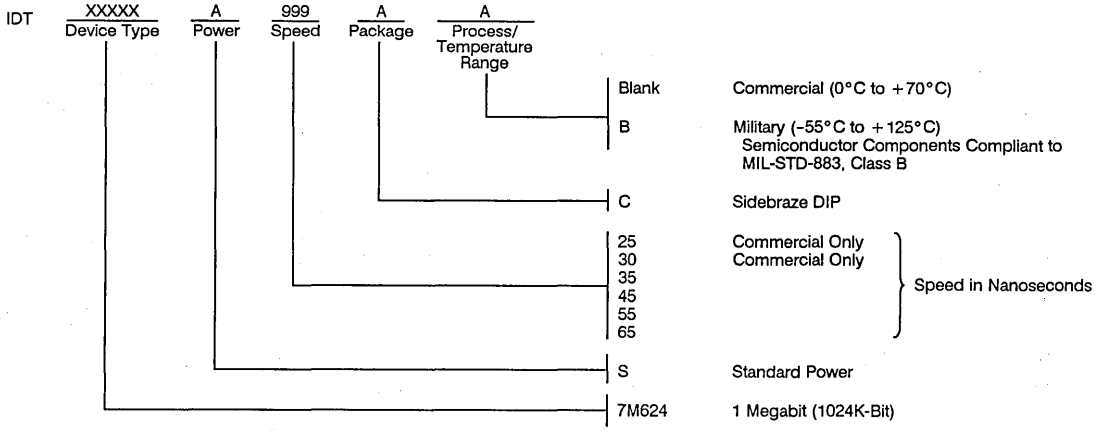
NOTE:
The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

IDT7M624
256K x 4 CONFIGURATION



NOTE:
Each chip is now controlled by the two higher order address pins A_{16} and A_{17}.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

256K CMOS STATIC RAM MODULE

IDT 7M656L

FEATURES:

- High-density 256K-bit CMOS static RAM module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  - Military: 20ns
  - Commercial: 15ns
- Low power consumption
  - Active: 3.2mW (typ.) (in 16K x 16 organization)
  - Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s high-performance 16K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Module available with semiconductor components compliant to MIL-STD-883, Class B.

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

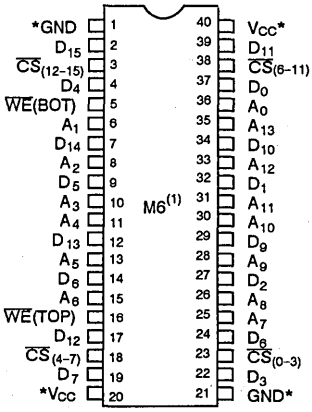
The IDT7M656 is available with access times as fast as 15ns commercial and 20ns military temperature range, with maximum operating power consumption of only 7.9W (significantly less if organized 32Kx8 or 64Kx4). The RAM module also offers a maximum standby power mode of 3.0W and a maximum full standby mode of 176mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167s in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

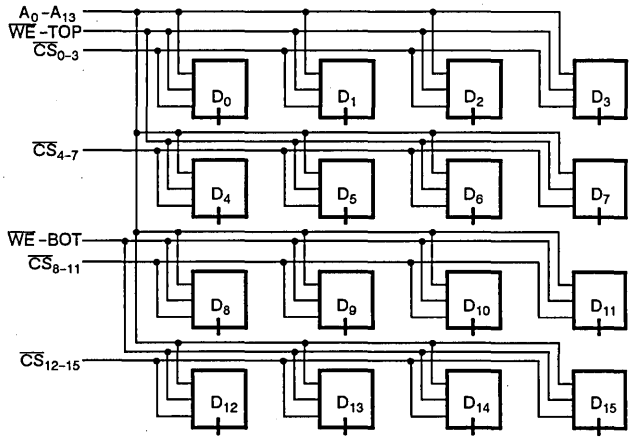
PIN CONFIGURATION



DIP
TOP VIEW

1. For module dimensions, please refer to module drawing M6 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{xx}	Addresses	D_{xx}	$DATA_{IN/OUT}$
$\overline{CS}_{xx}$	Chip Selects	V_{CC}	Power
$\overline{WE}_{xx}$	Write Enable	GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC}= 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M656L MIN.	TYP.(1)	MAX.(3)	MAX.(4)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} =5.5V, V_{IN} = 0V to V_{CC}	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	–	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f_{MAX}	–	640	1280	1920	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f_{MAX}	–	420	840	1360	mA
I_{CCX4}	Operating Current in X4 Mode	$\overline{CS}_{xx}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f_{MAX}	–	310	620	1080	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{xx}$ ≥ V_{CC} (TTL Level), V_{CC} =5.5V, Output Open	–	200	400	800	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{xx}$ ≥ V_{CC} -0.2V (CMOS Level V_{IN} ≥ V_{CC} -0.2V or <0.2V	–	0.032	15(2)	160	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	–	2.4	V

NOTES:

1. V_{CC} = 5V, T_A=+25°C
2. I_{SB1} max. at commercial temperature = 5.0mA
3. t_{AA} = 25, 35, 55, 65ns
4. t_{AA} = 15, 20ns

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	200	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	60	pF

NOTE:

1. This parameter is determined by device characterization, but is not 100% tested.
2. For each output, 16K x 16 mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

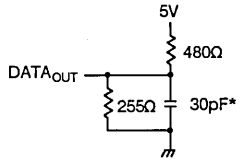


Figure 1. Output Load

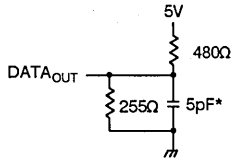


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

* Including scope and jig.

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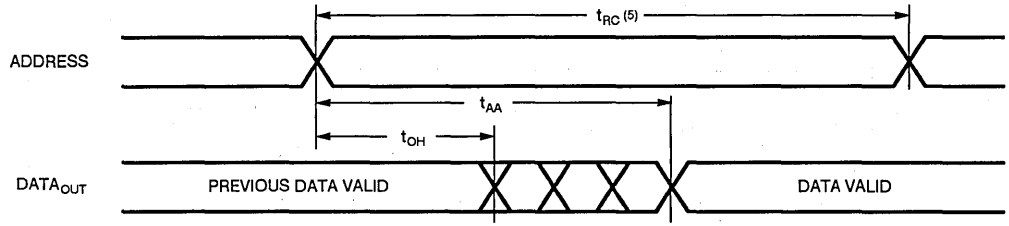
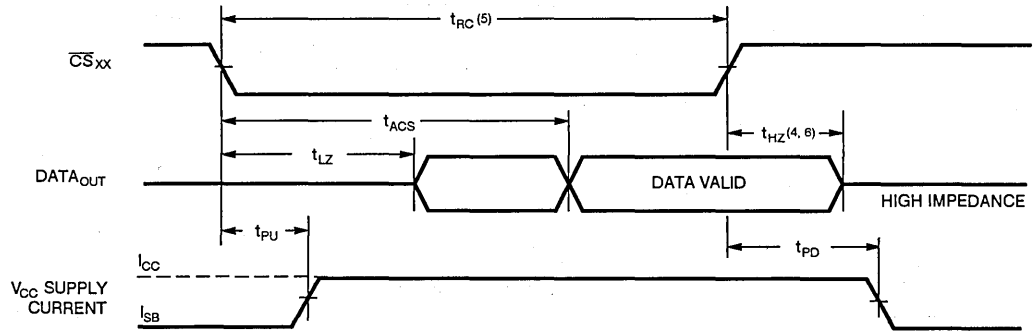
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7M656L15 (COM'L. ONLY)		IDT7M656L20		IDT7M656L25		IDT7M656L35		IDT7M656L55		IDT7M656L65		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselect to Output in High Z	–	10	–	15	–	15	–	20	–	40	–	40	ns
t_{PU}	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time	–	15	–	20	–	25	–	35	–	55	–	65	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	55	–	65	–	ns
t_{CW}	Chip Select to End of Write	15	–	20	–	20	–	30	–	45	–	55	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	25	–	35	–	45	–	55	–	ns
t_{AS}	Address Set-up Time	2	–	2	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	13	–	17	–	20	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	13	–	15	–	15	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{IY}	Write Enable to Output in HIGH Z	–	10	–	10	–	10	–	15	–	40	–	40	ns
t_{WY}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



NOTES:

1. $\overline{WE}_{XX}$ is High for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

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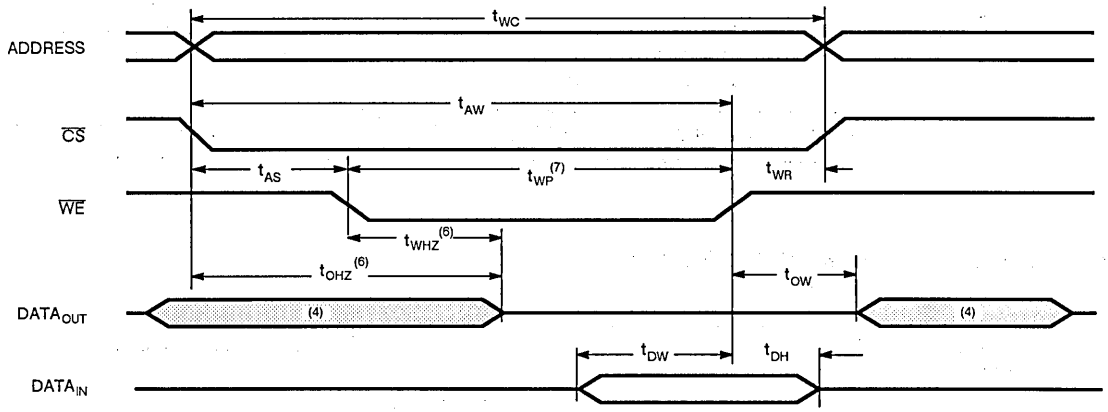
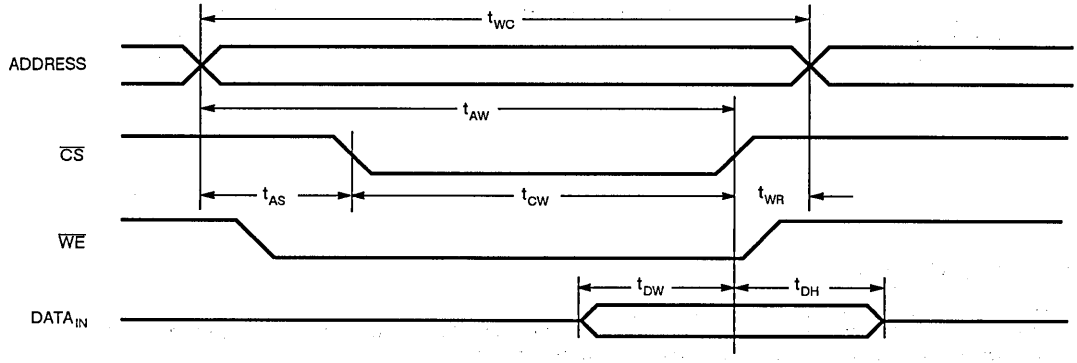
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

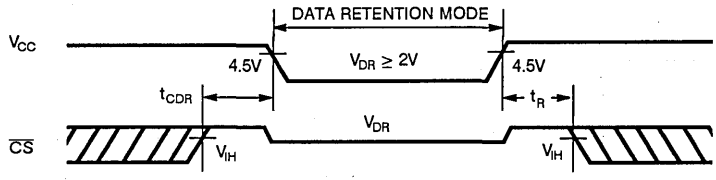
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS (V_{CC}= 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX. COM'L.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS}_{xx} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	2.0	–	–	–	V
I_{CCDR}	Data Retention Current		– –	.01(2) .02(3)	2.0(2) 3.0(3)	6.0 9.0	mA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	–	–	ns
t_R	Operation Recovery Time		t_{RC}(4)	–	–	–	ns

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM



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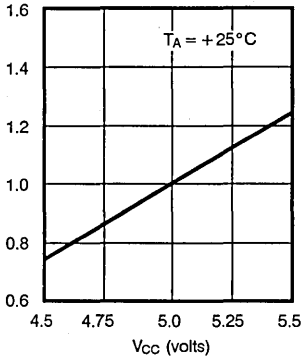
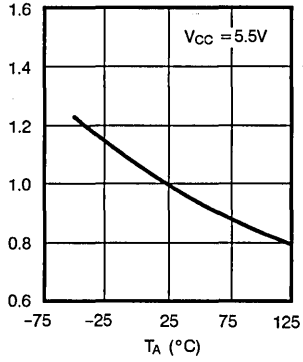
NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

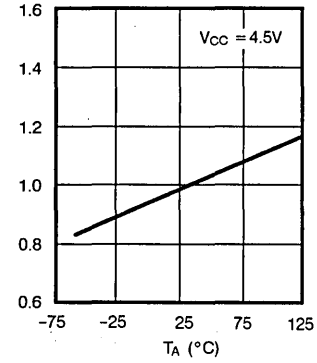
Supply Current vs. Voltage



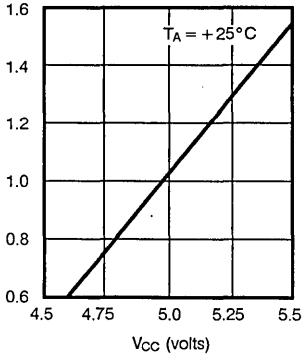
Supply Current vs. Ambient Temperature



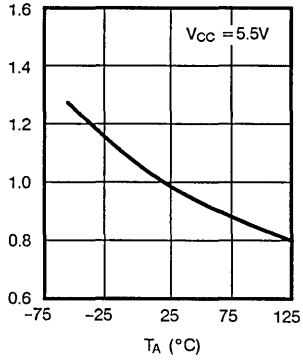
Address Access Time vs. Ambient Temperature



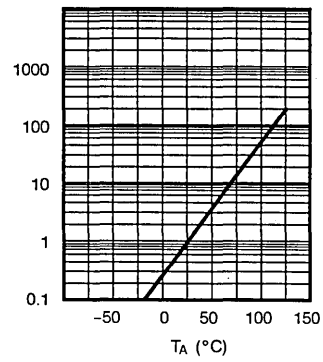
Stand-by-Power Supply Current vs. Voltage



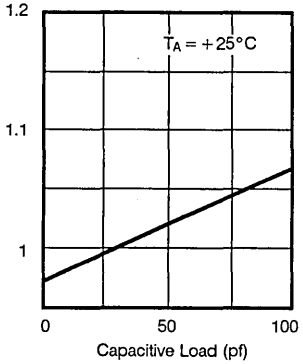
Stand-by-Power Supply Current vs. Ambient Temperature



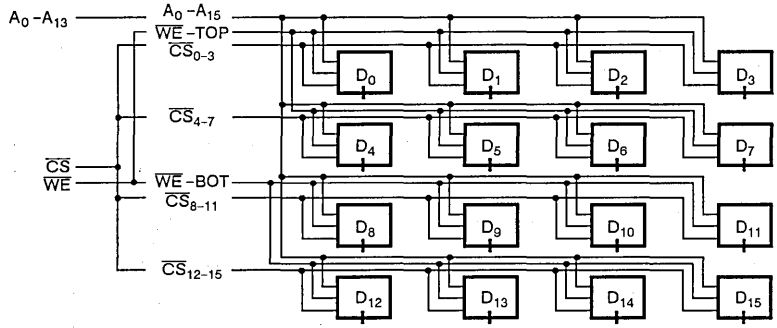
Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load

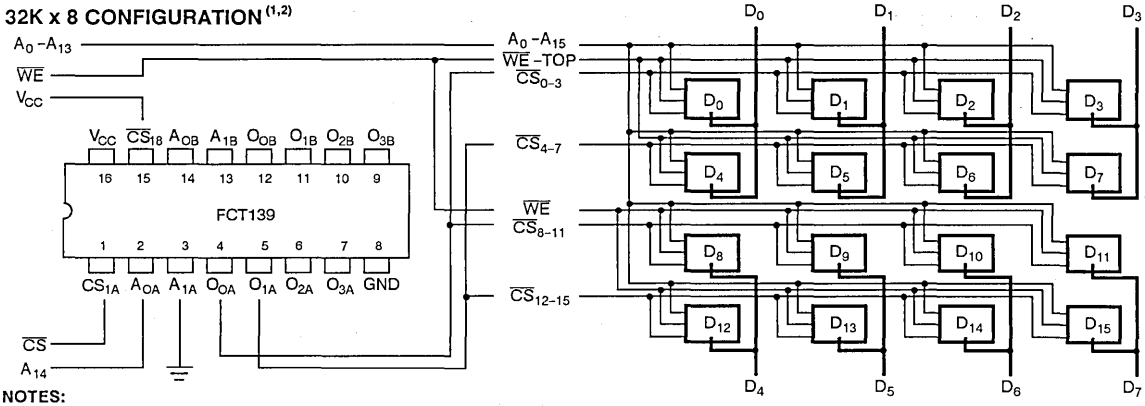


IDT7M656
16K x 16 CONFIGURATION[1,2]



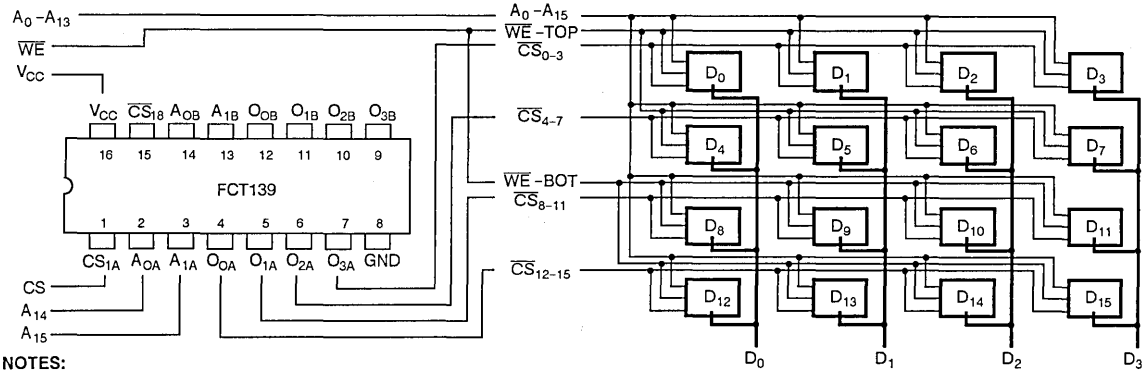
NOTES:
1. All chip selects tied together since, in a by-16 configuration, all chips are either on or off.
2. The two write enables are tied together allowing control of the write enable for entire memory at one time (necessary) in a by-16 organization since all chips are either writing or reading at any given time.

32K x 8 CONFIGURATION[1,2]



NOTES:
1. All chip selects tied together in groups of two. The decoder uses the new higher order address pin (A_{14}) to determine which of the two banks of memory are disabled.
2. The two write enables are tied together for ease of layout. They could be controlled by the decoder similar to the chip selects but would save only a minimal amount of power and add complexity to the layout.

64K x 4 CONFIGURATION[1,2]



NOTES:
1. Each chip select is now controlled by the two higher order address pins A $_{14}$(necessary in 64K deep memory).
2. Again the two write enables are tied together for ease of layout (the megabit part will only have one write enable pin).

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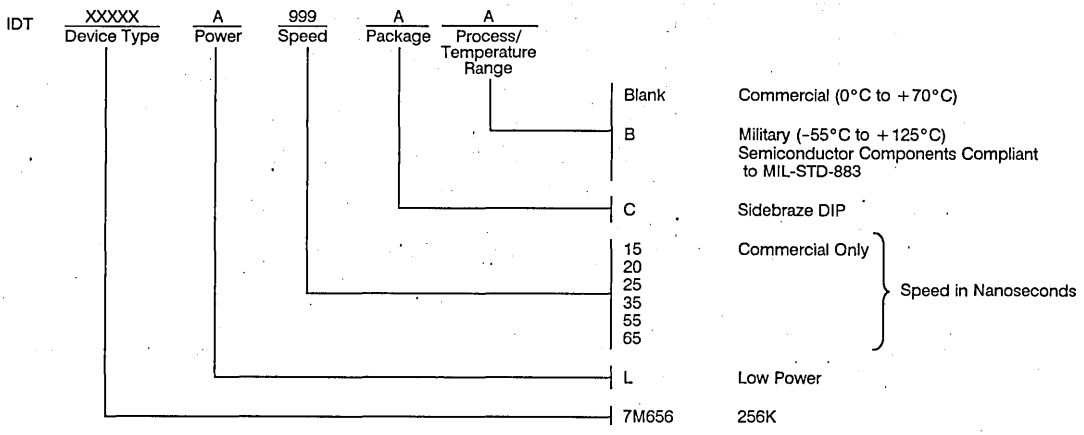
ORDERING INFORMATION



Integrated Device Technology, Inc.

512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

IDT 7M812
IDT 7M912

FEATURES:

- High-density 512K-bit CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 2.4W (typ. in 64K x 8 organization)
  - Standby: 240µW (typ. in 64K x 8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64K x 1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

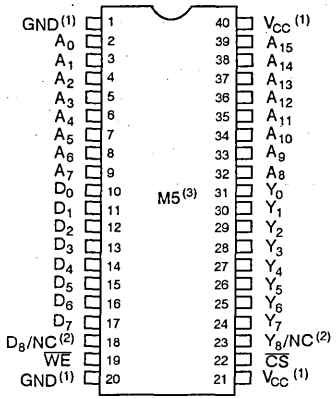
The IDT7M812/IDT7M912 are available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 6.9W (IDT7M912, 64K x 9 option). The module also offers a standby power mode of less than 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing access and cycles times for ease of use.

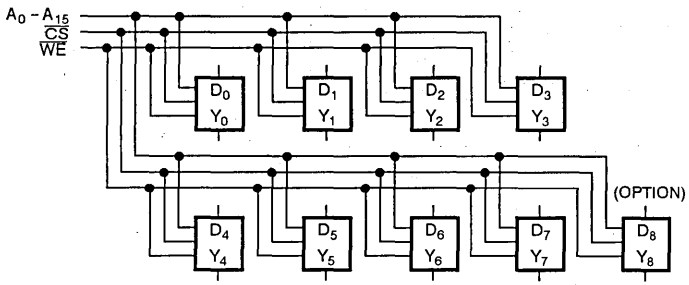
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address
D_0-D_8	Data Input
Y_0-Y_8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64K x 9 (IDT7M912) option and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.
3. For module dimensions, please refer to module drawing M5 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M912 MIN.	IDT7M912 TYP.	IDT7M912 MAX.(3)	IDT7M912 MAX.(4)	IDT7M812 MIN.	IDT7M812 TYP.	IDT7M812 MAX.(3)	IDT7M812 MAX.(4)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V; V_{IN} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open Min. Duty Cycle = 100%	–	540	1080	1260	–	480	960	1120	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% Output Open	–	540	1080	1530	–	480	960	1360	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ Min. Duty Cycle = 100%	–	270	450	585	–	240	400	520	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or ≤ 0.2V	–	0.2	180(2)	225	–	0.05	160(2)	200	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	–	–	0.5	0.5	–	–	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	2.4	–	–	–	V

NOTES:

1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} (max.) of IDT7M812/912 at commercial temperature = 80mA/90mA.
3. t_{AA} = 30, 35, 45, 55ns
4. t_{AA} = 25ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

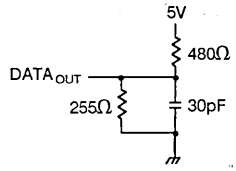


Figure 1. Output Load

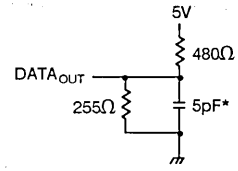


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

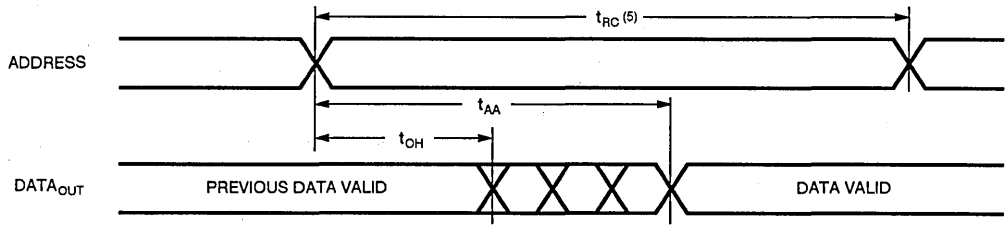
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

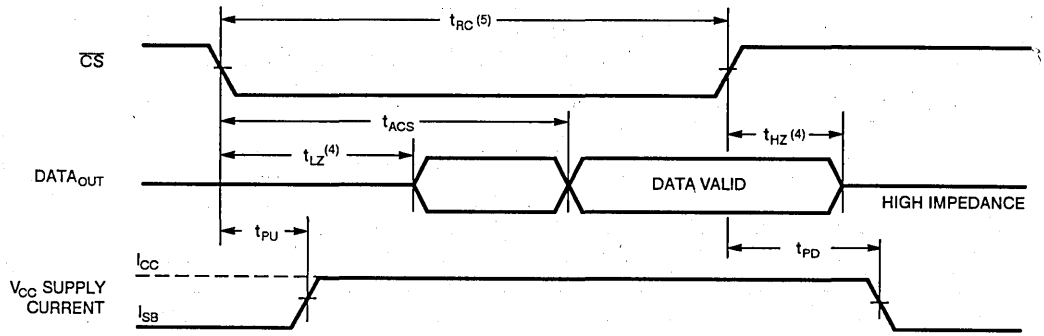
SYMBOL	PARAMETER	7M912S25 7M812S25 COM'L. ONLY		7M912S30 7M812S30 COM'L. ONLY		7M912S35 7M812S35		7M912S45 7M812S45		7M912S55 7M812S55		7M912S65 7M812S65		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Selection to Power Down Time	–	25	–	30	–	35	–	35	–	35	–	35	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{CW}	Chip Selection to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AW}	Address Valid to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AS}	Address Set-up Time	3	–	3	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	25	–	30	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	20	–	25	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z	0	20	0	25	0	25	0	30	0	30	0	35	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

13

TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



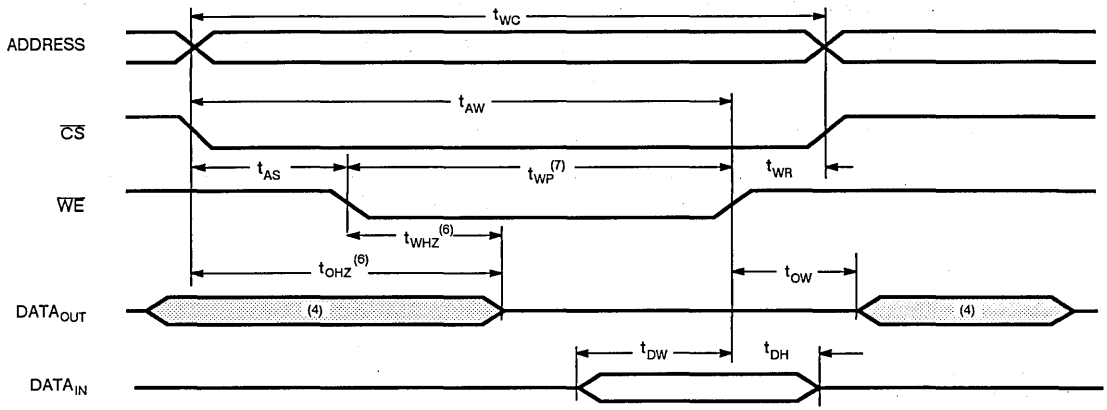
TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



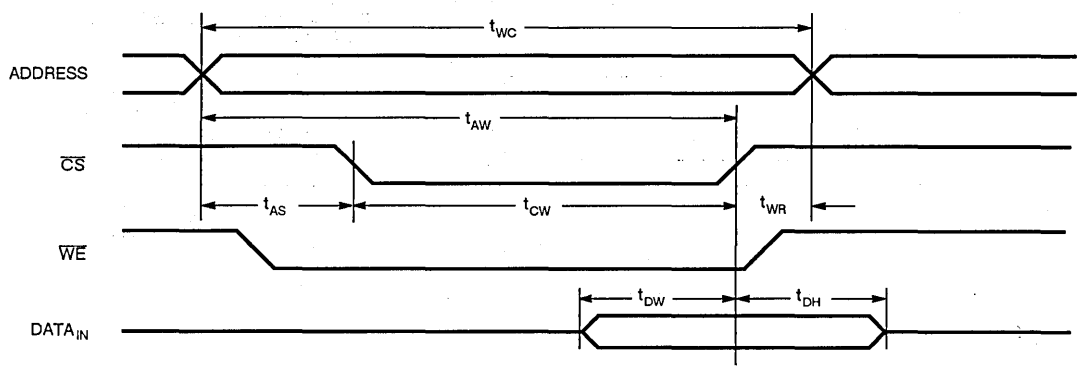
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

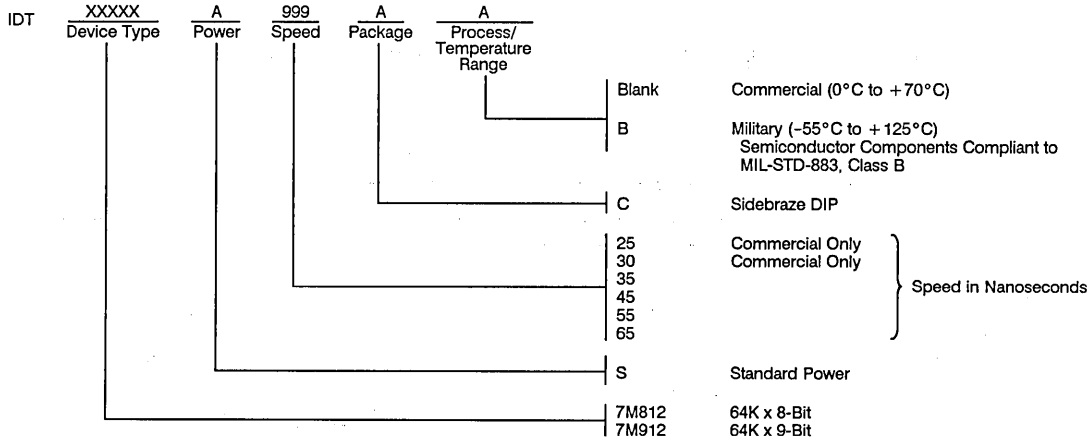
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

4 MEGABIT (256K x 16) CMOS STATIC RAM MODULE

PRELIMINARY
IDT 7M4016

FEATURES:

- High-density 4 megabit (256K x 16) CMOS static RAM module
- Low power consumption
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 48-pin, 900 mil wide ceramic sidebraze DIP
- 4X the density of the IDT7M624 (1024K RAM module) in the same size package
- Multiple GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

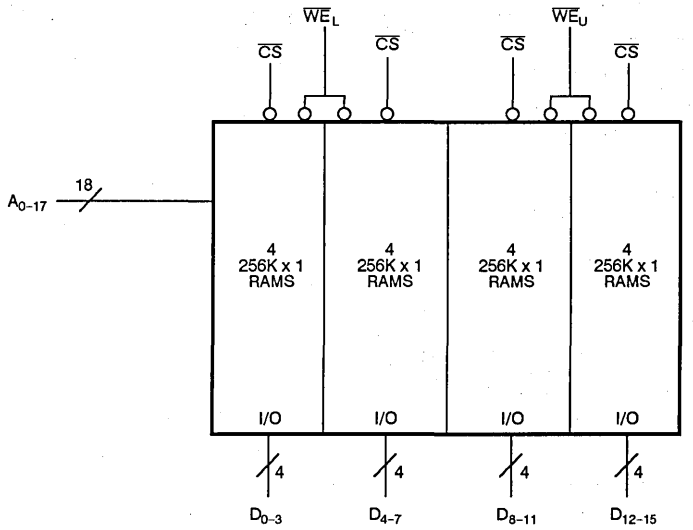
The IDT7M4016 is a 4-megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen (256K x 1) static RAMs in leadless chip carriers. The IDT7M4016 is an upgrade from the IDT7M624 (1024K RAM module) offering four times the memory density in the same size package. Making four chip select lines available (one for each group of four RAMs) allows the user to configure the memory into a 256K x 16, 512K x 8 or 1024K x 4 organization.

The IDT7M4016 is packaged in a 48-pin, 900 mil wide sidebraze DIP to take advantage of the compact leadless chip carriers. This enables four megabits of static RAM memory to be placed in less than 2.2 square inches of board space.

All inputs and outputs of the IDT7M4016 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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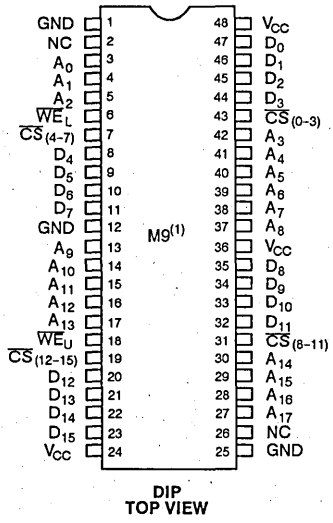
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M9 in the packaging section.

PIN NAMES

V_{CC}	Power
GND	Ground
A_{0-17}	Addresses
D_{0-15}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}_L$	Write Enable (Lower Byte)
$\overline{WE}_U$	Write Enable (Upper Byte)

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

Note:

1. V_{IL} = -3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ±10%
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = MAX, V_{IN} = GND to V_{CC}	–	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = MAX, V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = MAX, $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	V_{CC}= MIN, I_{OL}= 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC}= MIN, I_{OH}= -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

			IDT7M4016 (1) MAX.		IDT7M4016 (2) MAX.		
SYMBOL	PARAMETER	TEST CONDITIONS	COM'L.	MIL.	COM'L.	MIL.	UNIT
I_{CC1}	Operating Current	f = 0; $\overline{CS} \leq V_{IL}$, V_{CC} = MAX; Output Open	1760	–	1600	1760	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = MAX; $\overline{CS} \leq V_{IL}$; f = f_{MAX} Output Open	2560	–	2400	2560	mA
I_{SB}	Standby Current Supply	$\overline{CS} \leq V_{IL}$	560	–	560	560	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2 or $\leq$ 0.2V	480	–	480	480	mA

Notes:
1. 25ns
2. 35, 45, 55, 70ns

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	7M4016S25 (COM'L. ONLY) MIN.	MAX.	7M4016S35 MIN.	MAX.	7M4016S45 MIN.	MAX.	7M4016S55 MIN.	MAX.	7M4016S70 (MIL. ONLY) MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	–	13	–	20	–	25		25		30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	25	–	35	–	45	–	55	–	70	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	35	–	45	–	55	–	70	–	ns
t_{CW}	Chip Selection to End of Write	25	–	35	–	45	–	55	–	65	–	ns
t_{AW}	Address Valid to End of Write	25	–	35	–	45	–	55	–	65	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	25	–	35	–	45	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}(1)	Write Enabled to Output in High Z	–	13	–	20	–	25	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	12	–	15	–	20	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}(1)	Output Active From End of Write	5	–	5	–	5	–	5	–	5	–	ns

Notes:
1. This parameter guaranteed but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

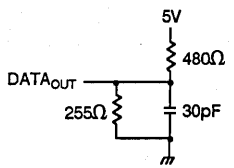


Figure 1. Output Load

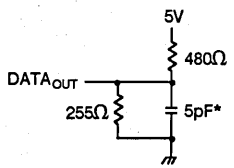


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

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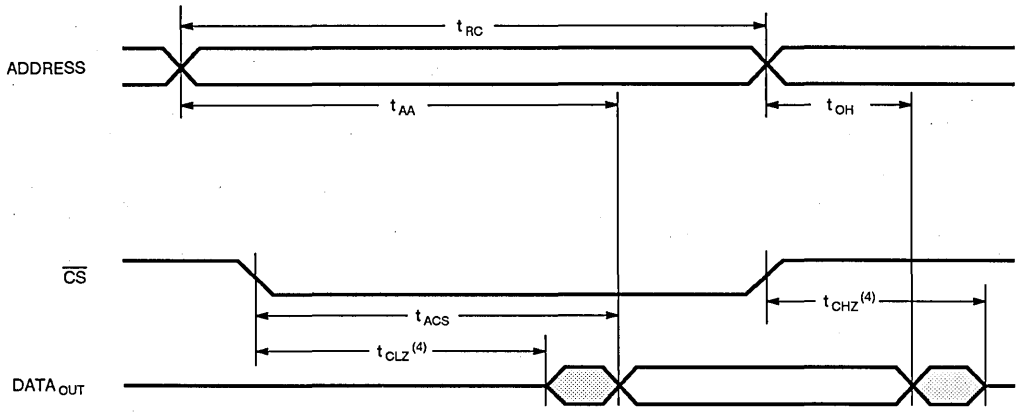
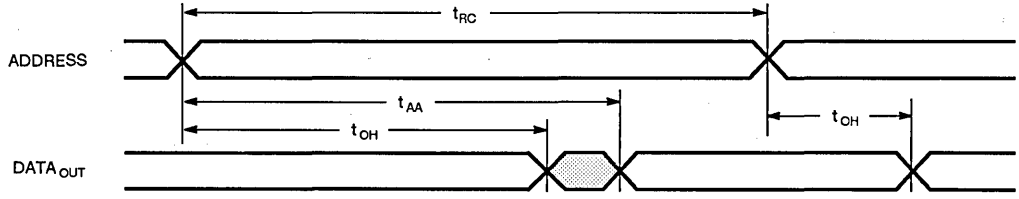
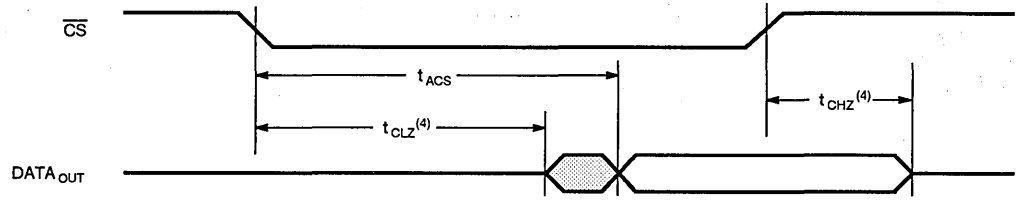
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2]



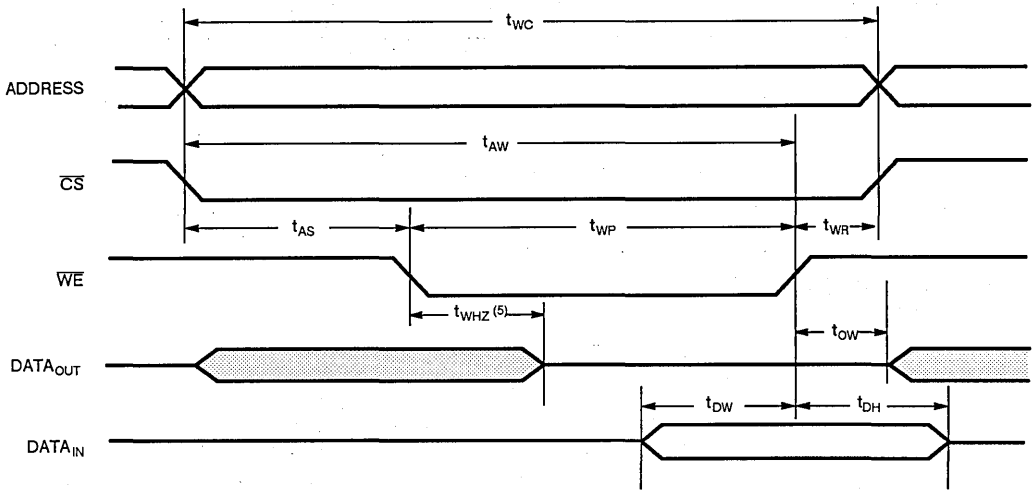
TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3]



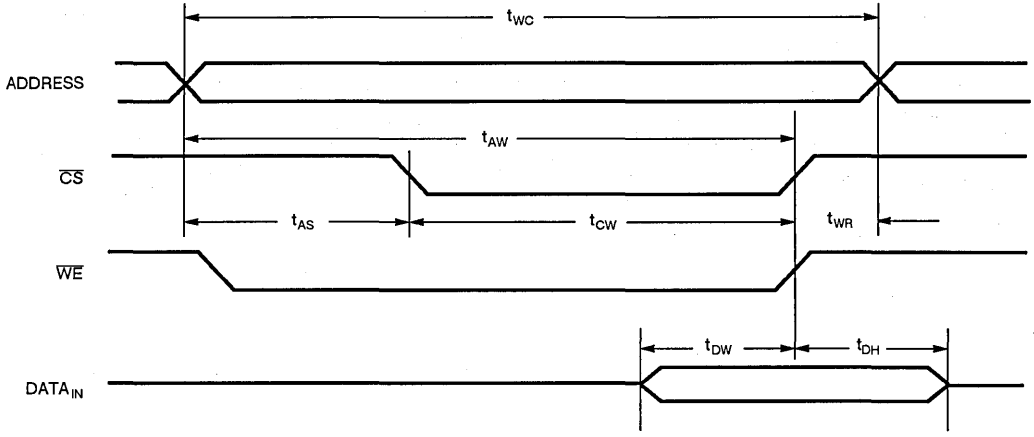
NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 [1, 2, 3]
($\overline{WE}$ CONTROLLED TIMING)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 [1, 2, 3, 4]
($\overline{CS}$ CONTROLLED TIMING)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TRUTH TABLE

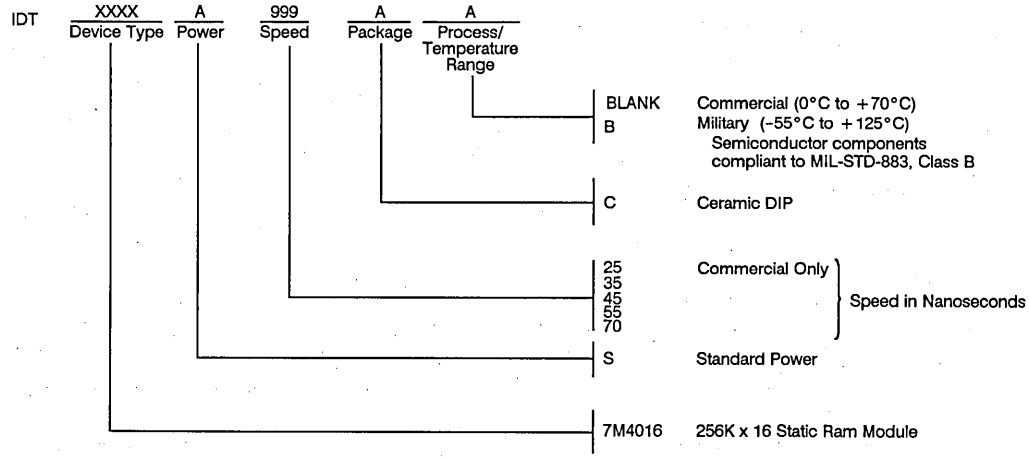
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High-Z	Active

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = OV	30	pF
$C_{IN(A)}$	Input Capacitance Address and Control	$V_{(IN)}$ = OV	200	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = OV	30	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

2 MEGABIT (64K x 32) CMOS STATIC RAM MODULE

IDT 7M4017

FEATURES:

- High-density 2 megabit (64K x 32) CMOS static RAM module
- Fast access times
  - Military: 50ns (max.)
  - Commercial: 40ns (max.)
- Individual byte selects
- Upper and lower word write enables
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Available in 60-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M4017 is a 2 megabit (64K x 32) high-speed static RAM module constructed on a co-fired ceramic substrate using eight IDT71256 32K x 8 static RAMs in leadless chip carriers. On-board decoders use A_{15} to select the upper or lower bank of RAMs. Four chip selects control individual byte selection. Extremely fast speeds can be achieved due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

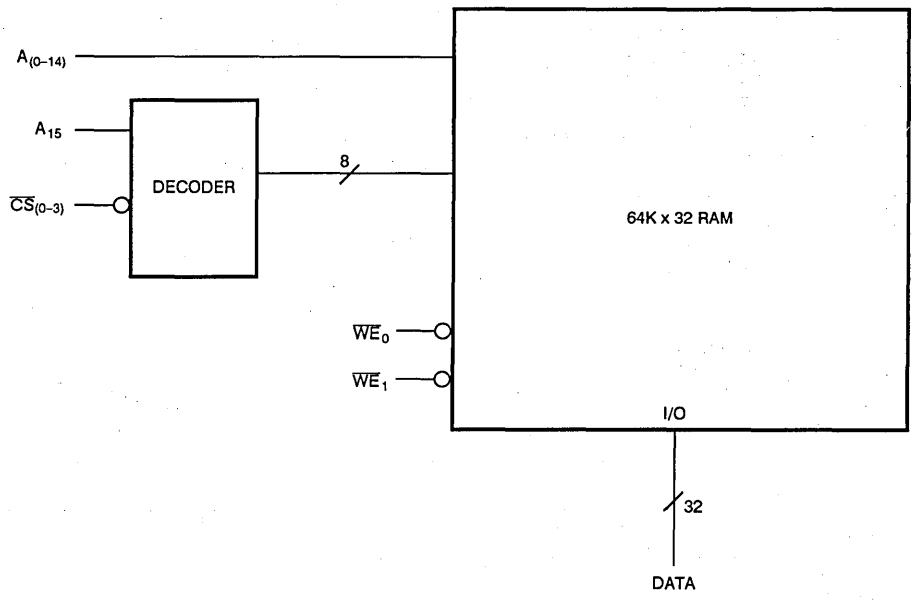
The IDT7M4017 is offered in a 60-pin, 600 mil center sidebraze DIP which enables two megabits of memory to be placed in less than 1.9 square inches of board space.

The IDT7M4017 is available with fast access times over the commercial and military temperature ranges, with minimal power consumption. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode.

All inputs and outputs of the IDT7M4017 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

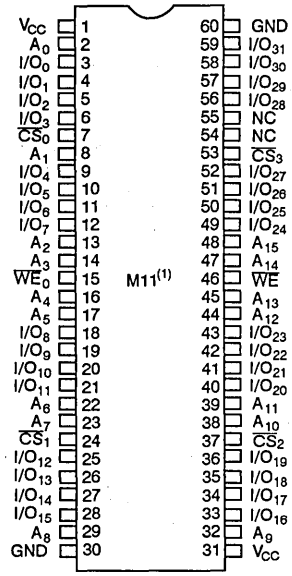
All IDT military module semiconductor components are manufactured in compliance with MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



NOTE:
1. For module dimensions, please refer to module drawing M11 in the packaging section.

PIN NAMES

$A_0 - A_{15}$	Addresses
I/O_{0-31}	Data Inputs/Outputs
$\overline{CS}_0$	Chip Select for I/O_{0-7}
$\overline{CS}_1$	Chip Select for I/O_{8-15}
$\overline{CS}_2$	Chip Select for I/O_{16-23}
$\overline{CS}_3$	Chip Select for I/O_{24-31}
$\overline{WE}_0$	Write Enable for I/O_{0-15}
$\overline{WE}_1$	Write Enable for I/O_{16-31}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT7M4017 MAX. COM'L.	IDT7M4017 MAX. MIL.	UNIT
I_{CC1}	Operating Current	F = 0, $\overline{CS} \leq V_{IL}$ V_{CC} = Max.; Output Open	460	500	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS} \leq V_{IL}$; F = F_{MAX} Output Open	750	790	mA
I_{SB}	Standby Supply Current	$\overline{CS} \leq V_{IL}$	180	180	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	135	175	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT4017S40 (COM'L. ONLY) MIN.	MAX.	IDT7M4017S45 (COM'L. ONLY) MIN.	MAX.	IDT7M4017S50 MIN.	MAX.	IDT7M4017S60 MIN.	MAX.	IDT7M4017S70 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{AA}	Address Access Time	–	40	–	45	–	50	–	60	–	70	ns
t_{ACS}	Chip Select Access Time	–	40	–	45	–	50	–	60	–	70	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	–	15	–	20	–	20	–	25	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	45	–	50	–	60	–	70	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	–	45	–	50	–	60	–	70	–	ns
t_{CW}	Chip Selection to End of Write	35	–	40	–	45	–	55	–	60	–	ns
t_{AW}	Address Valid to End of Write	35	–	40	–	45	–	55	–	60	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	35	–	45	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	15	–	20	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	3	–	3	–	3	–	3	–	3	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter is guaranteed but not tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

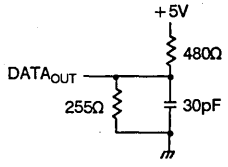


Figure 1. Output Load

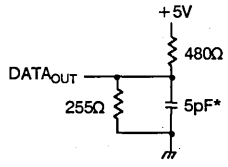


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

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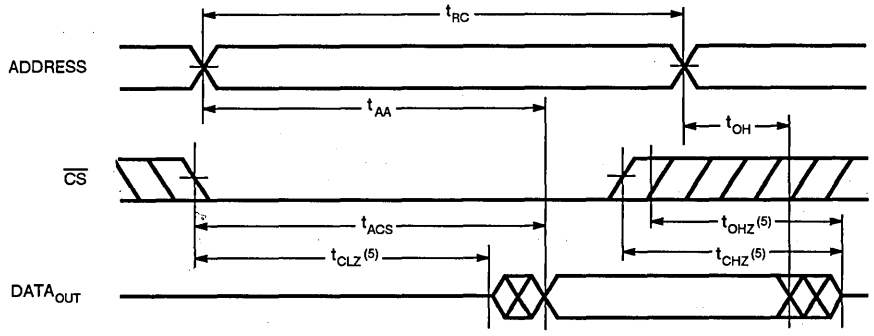
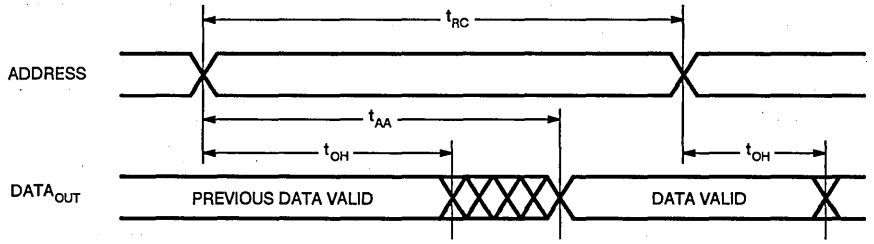
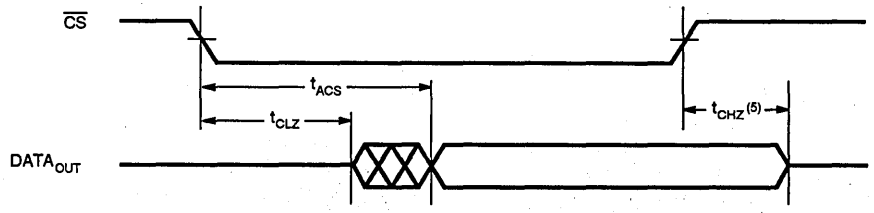
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



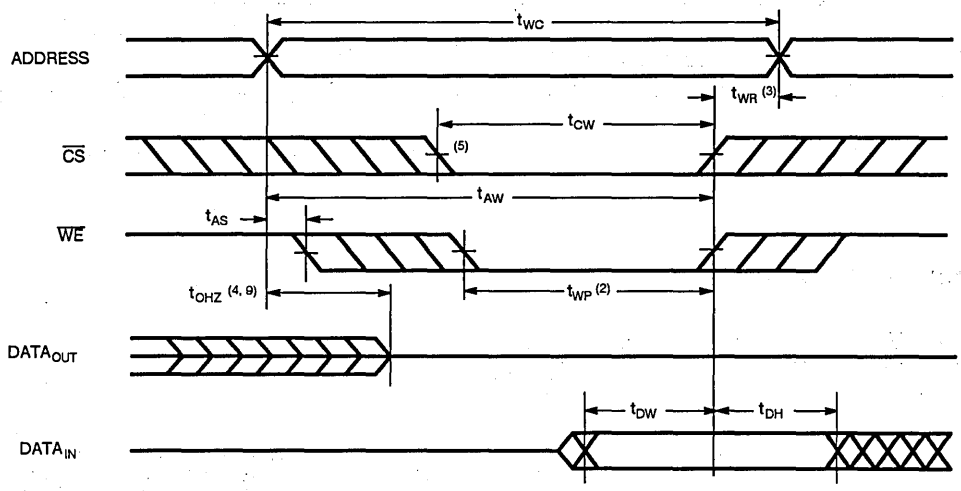
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



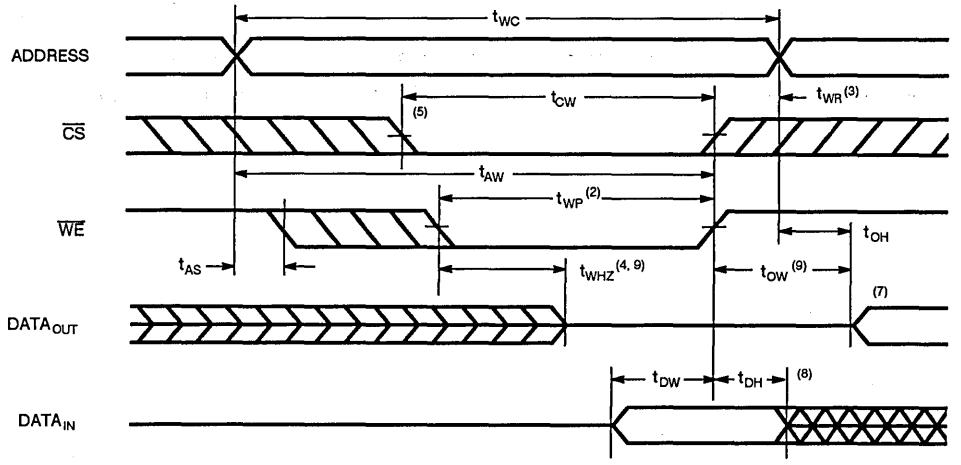
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



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NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

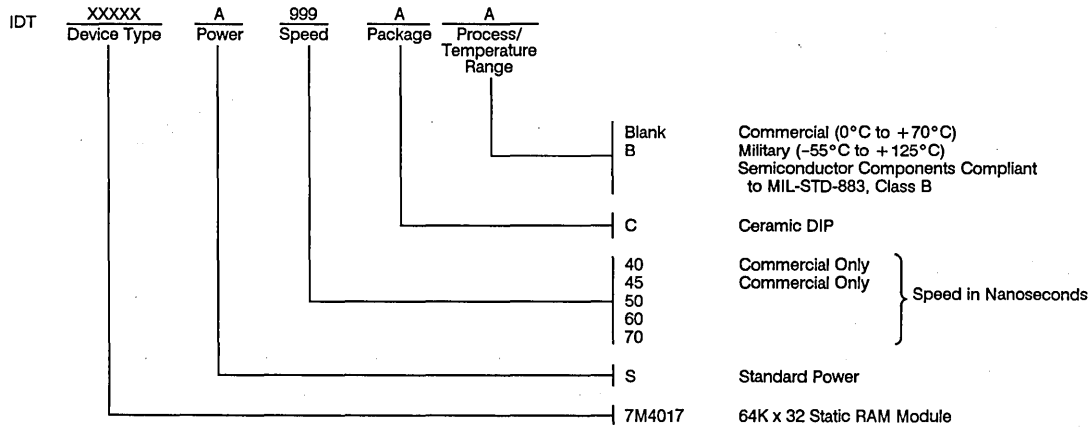
MODE	$\overline{CS}_X$	$\overline{WE}_X$	OUTPUT	POWER
Standby	L	X	X	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN\ (D)}$	Input Capacitance (Data)	V_{IN} = 0V	30	pF
$C_{IN\ (A)}$	Input Capacitance Address and Control	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	30	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

DUAL MULTIPLEXED 16K x 20 SYNCHRONOUS STATIC RAM MODULE

IDT 7M6001

FEATURES:

- Dual 16K x 20 synchronous RAM
- Edge triggered data input and data output registers
- Edge triggered data address registers
- Two address register sources individually selectable
- Separate chip select and write enables to each memory array
- Individual clock lines to each register
- Dual high-performance 16K x 20 memories
- Unique ping-pong operation capability
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in compact 92-pin ceramic sidebraze QIP (quad in-line) package
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

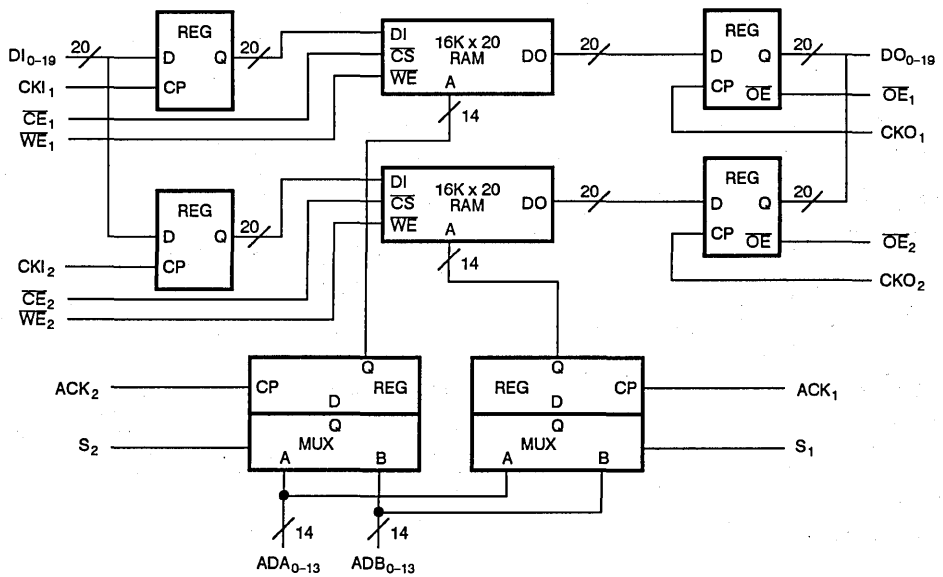
The IDT7M6001 is a dual multiplexed 16K x 20 synchronous RAM module. It utilizes ten IDT71981 high-speed synchronous memories, along with the appropriate input data, output data and address registers. The device features the ability to be used in a ping-pong mode. That is, data can be loaded into one memory array at one address and be read from the other memory array at a different address. This allows systems to be built that can perform fast Fourier Transforms in either a decimation-in-time or a decimation-in-frequency configuration. Data read from Memory 1 can be synchronously loaded into its output register, while data can be written into a different location in Memory 2. Similarly, data can be read from Memory 1 and Memory 2 in parallel from two different addresses and can be written into Memory 1 and Memory 2 at unique addresses. Registers at the data input and data output provide fully synchronous pipelined operation. The two memory systems are 20 bits wide and have multiplexed data input and data output bits from the module data pins. By taking advantage of the speed of the registers, data on the pins can run at a speed twice that of the memory. That is, both output registers can be read or both input registers can be loaded in a single memory cycle.

Two address sources are available to each address register to the RAM. Address Source A or Address Source B may be selected to load the edge triggered register for the 16K x 20-bit memory. The IDT54/74FCT399 is used for the two input multiplexer and address registers for each 16K x 20 memory. All inputs and outputs of the IDT7M6001 are TTL-compatible and operate from a single 5V supply.

The IDT7M6001 is offered as a compact 92-pin quad in-line (QIP) ceramic module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies only 4.2 square inches of board space.

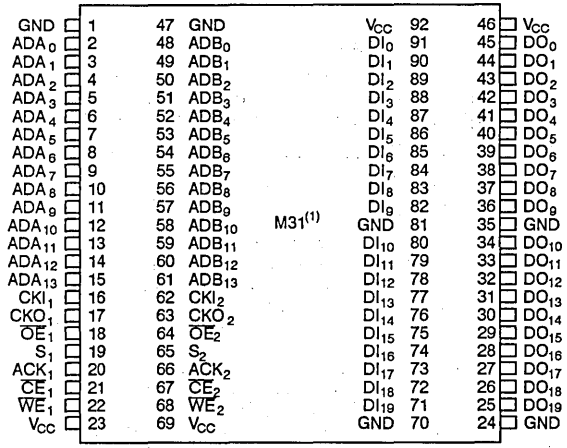
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M31 in the packaging section.

PIN NAMES

$\overline{OE}_1$-$\overline{OE}_2$	Data Out Register Output Enable
ADA_0-ADA_{13}	A Address Inputs
ADB_0-ADB_{13}	B Address Inputs
DI_0-DI_{19}	Data Inputs
DO_0-DO_{19}	Data Outputs
CKI_1-CKI_2	Data In Register Clock Input (Active Rising Edge)
ACK_1-ACK_2	Address Clock Input (Active Rising Edge)
S_1-S_2	Address MUX Select Input
$\overline{WE}_1$-$\overline{WE}_2$	Write Enable
$\overline{CE}_1$-$\overline{CE}_2$	RAM Select
CKO_1-CKO_2	Data Out Register Clock Input (Active Rising Edge)

FUNCTIONAL TABLE FOR ADDR MUX

INPUTS			OUTPUTS
$S_{1,2}$	S_A	S_B	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition of ACK1, 2
l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition of ACK1, 2
X = Immaterial

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	25	µA
$\|I_{LI}\|$	Input Leakage (Data & Address)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 10%

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT7M6001 MAX. COM'L.	IDT7M6001 MAX. MIL.	UNIT
I_{CC1}	Operating Current	f = 0, $\overline{CS}x \geq V_{IL}$, V_{CC} = Max.; Output Open	1000	1150	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}x \geq V_{IL}$; f = f_{MAX} Output Open	1910	2035	mA
I_{SB}	Standby Supply Current	$\overline{CS} \leq V_{IL}$	870	920	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}x \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	440	490	mA

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AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	7M6001S40		7M6001S45		7M6001S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{RC}	Read Cycle Time	40	–	45	–	55	–	ns
t_{CKO-DO}	CKOx to Output Valid	–	12	–	12	–	12	ns
t_S	Address Set-up Time	5	–	5	–	5	–	ns
t_H	Address Hold Time	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	15	–	15	ns
t_{CP}	CKOx, ACKx Pulse Width	10	–	10	–	10	–	ns
t_{CS-CKO}	Chip Select-1, 2 to CKOx	30	–	35	–	45	–	ns
t_{OHZ} (1)	Output disable to Output in High Z	18	–	18	–	18	–	ns
t_{SU}	S to ACK set up time	10	–	10	–	10	–	ns
t_{SH}	S to ACK to hold time	0	–	0	–	0	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	40	–	45	–	55	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	40	–	45	–	55	–	ns
t_S	Address, Din Set-up Time	5	–	5	–	5	–	ns
t_H	Address, Din hold Time	5	–	5	–	5	–	ns
t_{ACK-WE}	ACKx to Write Enable	12	–	12	–	12	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	35	–	ns
t_{CP}	CKIx, ACK Pulse Width	10	–	10	–	10	–	ns
t_{CW}	Chip Select to End of Write	25	–	30	–	35	–	ns
t_{ACKW}	ACK to End of Write	37	–	42	–	47	–	ns
t_{CKIW}	CKIx to End of Write	27	–	29	–	32	–	ns
t_{SU}	S to ACK set up time	10	–	10	–	10	–	ns
t_{SH}	S to ACK hold time	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

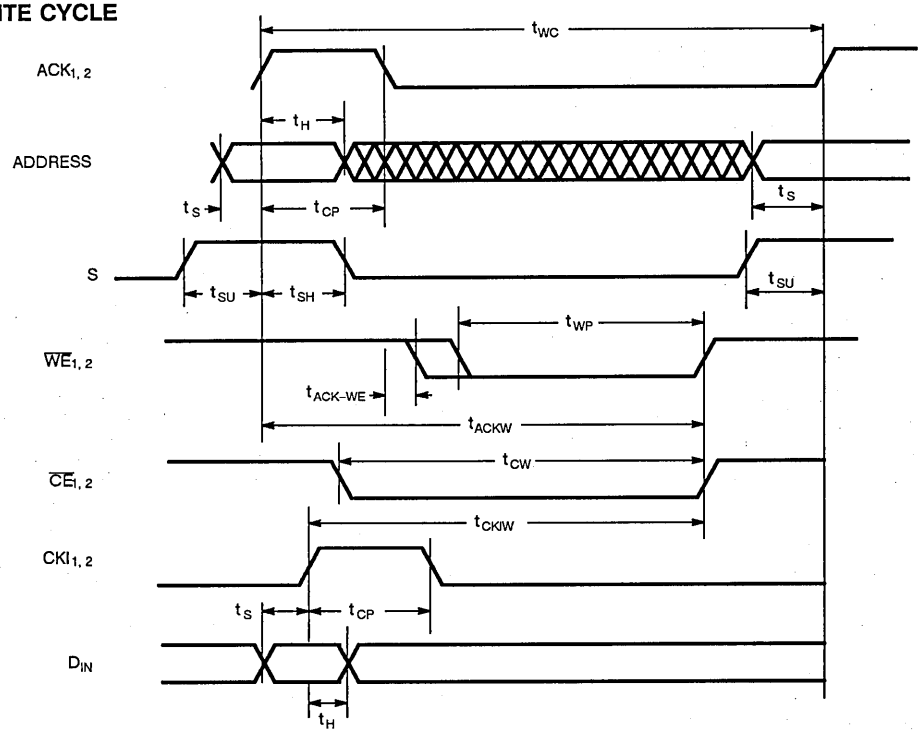
SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
$C_{IN(D)}$	Input Capacitance Din and Address	V_{IN} = 0V	40	pF
$C_{IN(C)}$	Input Capacitance Control	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

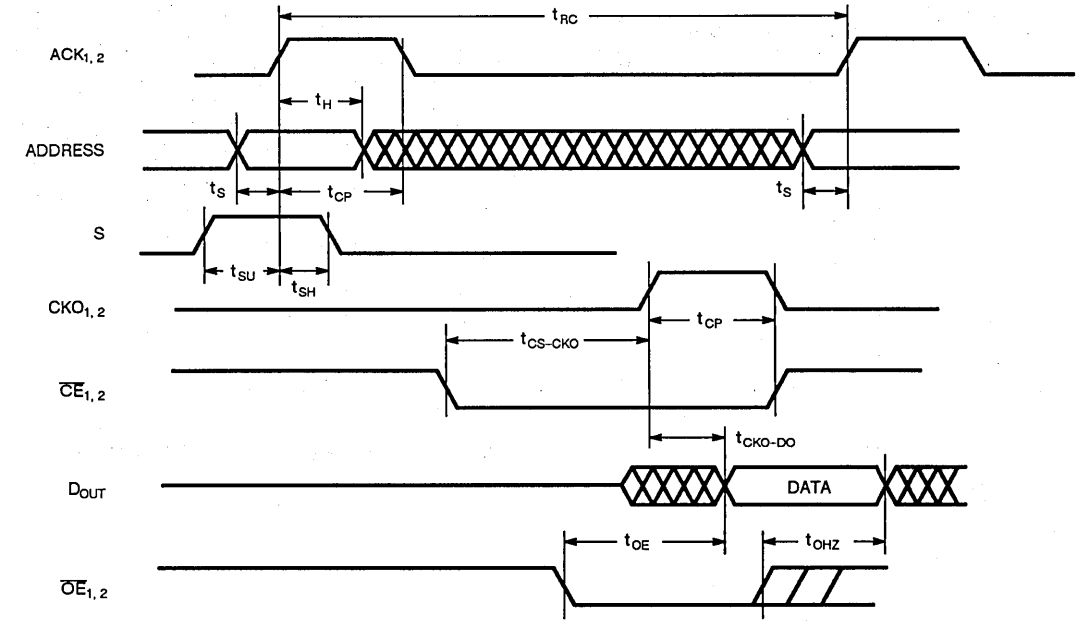
TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	CKO	CKI	POWER
Standby	H	X	X	X	X	Standby
Read	L	L	H	↑	X	Active
Write	L	X	L	X	↑	Active

WRITE CYCLE



READ CYCLE



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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

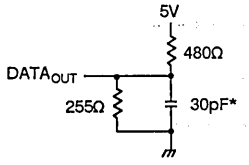


Figure 1. Output Load

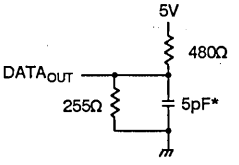
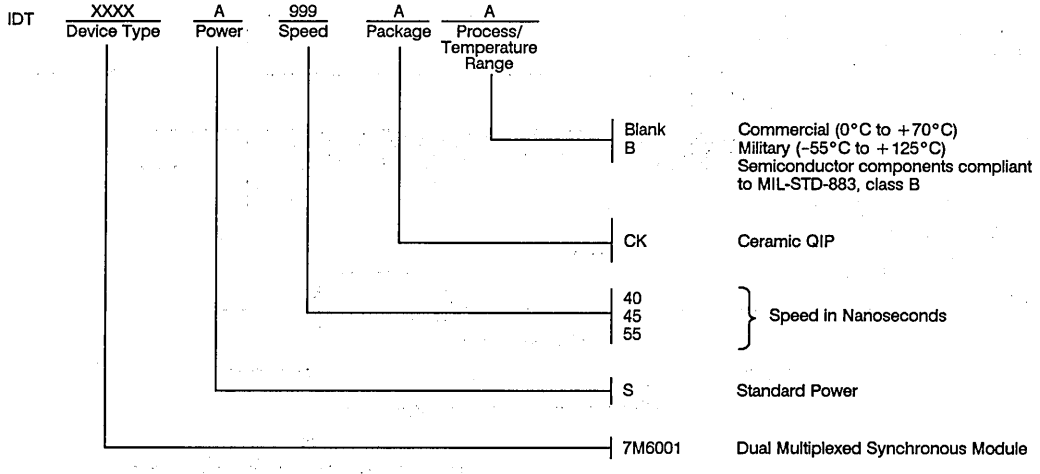


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, and t_{WHZ})

* Including scope and jig.

ORDERING INFORMATION



Integrated Device Technology, Inc.

16K x 32 WRITABLE CONTROL STORE STATIC RAM MODULE

IDT 7M6032

FEATURES:

- 16K x 32 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- 4 byte/wide output enables
- Separate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact 64-pin ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components manufactured in compliance to MIL-STD-883, Class B

DESCRIPTION:

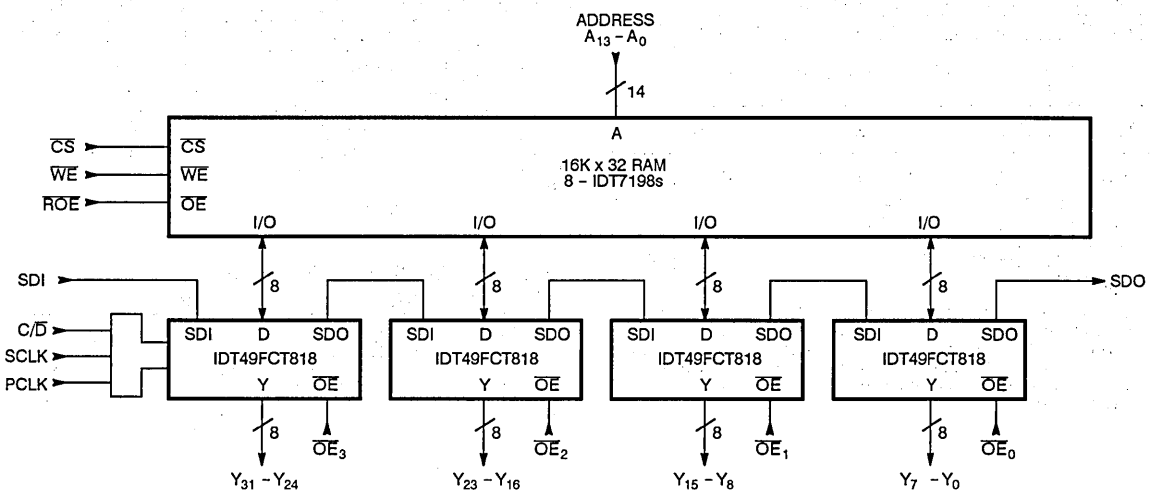
The IDT7M6032 is a 16K x 32-bit Writable Control Store (WCS) RAM and pipeline register. It features eight IDT7198 16K x 4 high-performance static RAMs and four IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 16K x 32 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. The address lines, chip select, write enable and output enable of the RAMs are all bused together to form one large 16K x 32 memory. Each eight Data I/Os of the RAM are connected to the D inputs of an IDT49FCT818. The device has the serial data-in and serial data-output bits connected to form a 32-bit Serial Protocol Channel register. The module features four separate output enables, one for each of the IDT49FCT818 registers. Thus, the Y outputs from the IDT49FCT818 registers may be enabled or put into the high-impedance state on individual 8-bit boundaries. The Command/Data (C/$\overline{D}$), Serial Shift Clock (SCLK) and Parallel Clock (PCLK) are all bus organized across the four IDT49FCT818 registers. The thirty-two register output bits, eight from each device, are separately brought out to form a 32-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 32-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel is performed using the IDT49FCT818. That is, the data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7M6032 is offered in a compact 64-pin 600 mil wide ceramic dual in-line module. It is constructed using ceramic LCC components on a multilayer co-fired ceramic substrate and occupies less than 2 square inches of board space.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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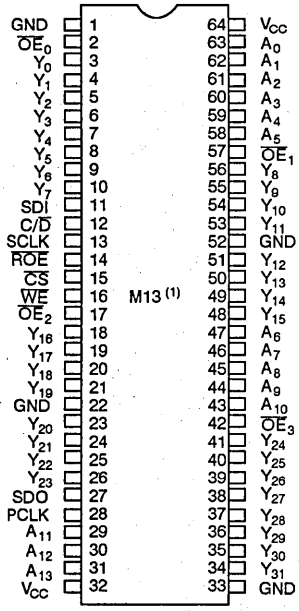
PIN CONFIGURATION



NOTE:
1. For module dimensions, please refer to module drawing M13 in the packaging section.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	H	X	High Z	Standby
Standby	H	L	X	D_{OUT}	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	SPC(1)	L	SPC(1)	Active

NOTE:
1. See SPC Commands for proper execution of write cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
$C_{IN(D)}$	Input Capacitance	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance Address and Control	V_{IN} = 0V	60	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. This parameter is sampled and not 100% tested.

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
Y_{0-31}	O	Parallel Data Register Output Pins (Y_0 = LSB, Y_{31} = MSB)
$\overline{OE}_Y$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 & 14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations
$\overline{CS}$	I	RAM Chip Select
$\overline{WE}$	I	RAM Write Enable
A_{0-13}	I	Address Bus Pins
$\overline{ROE}$	I	Internal RAM Output Enable for D bus

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DC ELECTRICAL CHARACTERISTICS

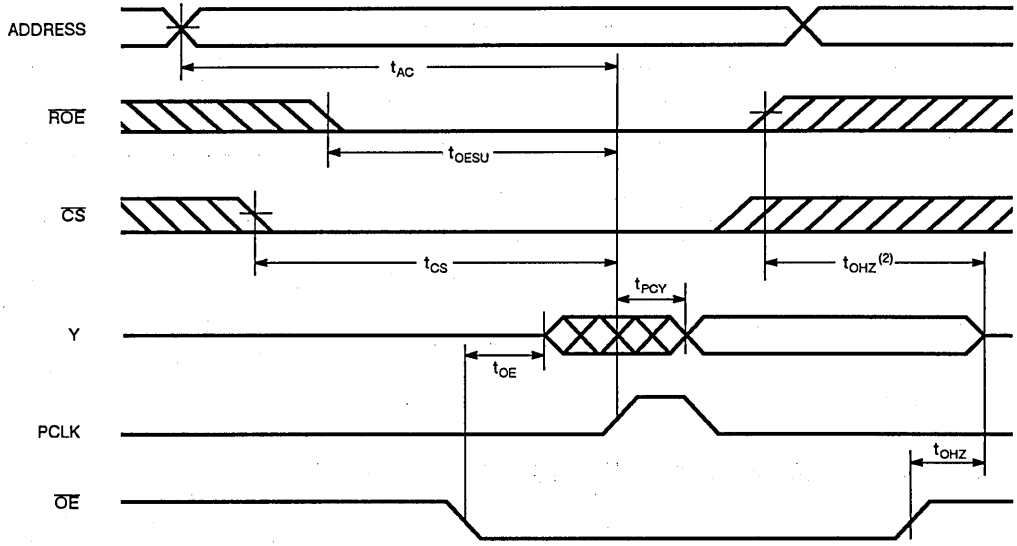
SYMBOL	PARAMETER	TEST CONDITIONS	25ns		30ns		35ns		45ns		55ns	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
$\|I_{LI}\|$	Input Leakage Data Bus µA	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	20	–	20	–	20	–	20	–	20
$\|I_{LO}\|$	Output Leakage µA	V_{CC} = Max, $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	20	–	20	–	20	–	20	–	20
I_{CC1}	Operating Current mA	f = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max; Output Open	–	900	–	800	–	800	–	800	–	800
I_{CC2}	Dynamic Operating Current mA	V_{CC} = Max; CS = V_{IL}; F = F_{MAX} Output Open	–	1200	–	1150	–	1050	–	1050	–	1050
I_{SB}	Standby Supply Current mA	$\overline{CS}$ = V_{IL}	–	450	–	450	–	450	–	450	–	450
I_{SB1}	Full Standby mA Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or < 0.2V	–	125	–	125	–	125	–	125	–	125
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -15mA	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 32mA	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	25ns		30ns		35ns		45ns		55ns	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
READ CYCLE											
t_{AC}	Address Valid to PCLK	25	–	30	–	35	–	45	–	55	–
t_{CS}	$\overline{CS}$ Valid to PCLK	25	–	30	–	35	–	45	–	55	–
t_{OESU}	$\overline{ROE}$ Valid to PCLK Set Up	15	–	20	–	25	–	30	–	35	–
t_{PCY}	PCLK to Output Valid	–	13	–	13	–	16	–	16	–	16
t_{OE}	$\overline{OE}$ Valid to Output Valid	2	13	2	13	2	16	2	16	2	16
t_{OHZ}(1)	$\overline{OE}$ Negated to Output in High Z	2	12	2	12	2	12	2	12	2	12
WRITE CYCLE											
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	45	–
t_{CW}	$\overline{CS}$ Valid to End of Write	20	–	25	–	30	–	35	–	45	–
t_{WP}	Write Enable Pulse Width	18	–	23	–	28	–	30	–	40	–
t_{WCD}	Cont/Dat to End of Write	22	–	25	–	28	–	30	–	35	–
t_{AS}	Address Setup Time	2	–	2	–	2	–	2	–	2	–

NOTE:
1. Guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Transition is measured ±200mV from steady state.

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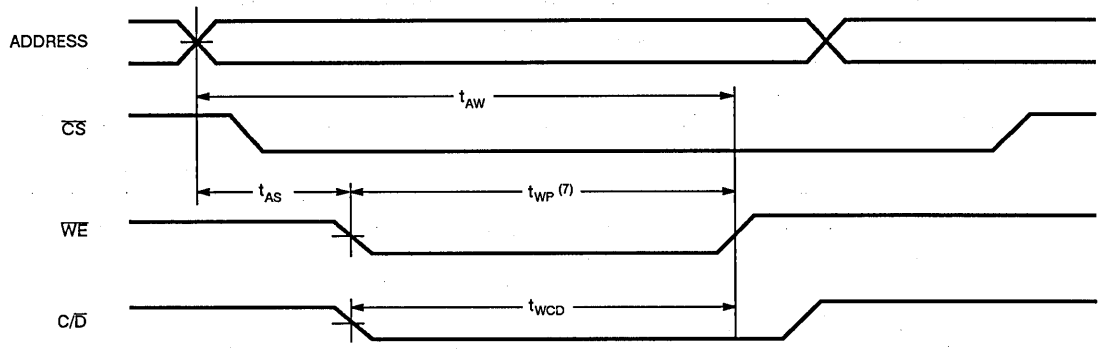
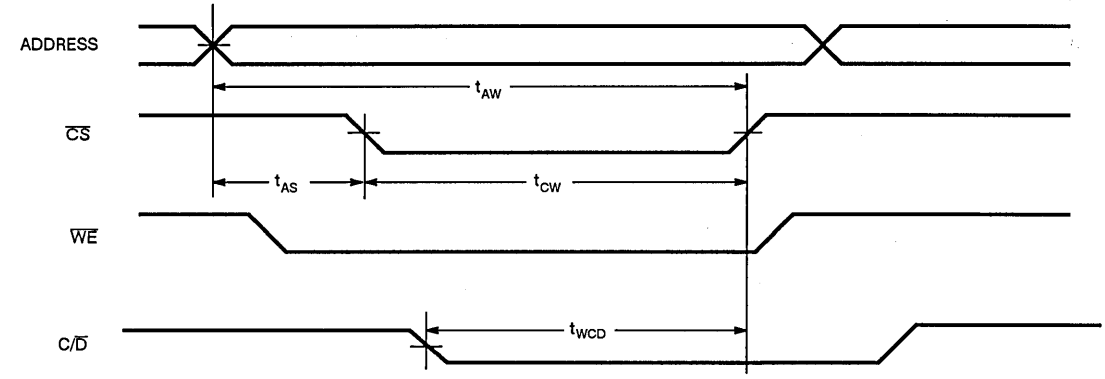
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 5]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 4, 5]



NOTES:

1. $\overline{WE}$, $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. $\overline{ROE}$ = V_{IH}

AC ELECTRICAL CHARACTERISTICS

SPC TIMING

SYMBOL		PARAMETER	25ns		30ns		35ns		45ns		55ns		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	T2	SCLK High to SDO	–	15	–	15	–	22	–	22	–	22	ns
	T3	SDI to SDO (Stub Mode)	–	45	–	45	–	45	–	45	–	45	ns
	T4	C/$\overline{D}$ Low to Y	–	15	–	15	–	20	–	20	–	20	ns
	T5	SCLK High to Y	–	15	–	15	–	25	–	25	–	25	ns
	T6	C/$\overline{D}$ Low to SDO	–	15	–	15	–	25	–	25	–	25	ns
t_{SU}	S2	C/$\overline{D}$ to SCLK High	15	–	15	–	15	–	15	–	15	–	ns
	S3	SDI to SCLK High	8	–	8	–	8	–	8	–	8	–	ns
	S4	Y or D to C/$\overline{D}$ Low	5	–	5	–	5	–	5	–	5	–	ns
	S5	C/$\overline{D}$ to PCLK High	12	–	12	–	12	–	12	–	12	–	ns
t_H	S6	Y to PCLK High	5	–	5	–	5	–	5	–	5	–	ns
	H2	C/$\overline{D}$ from SCLK Low	12	–	12	–	12	–	12	–	12	–	ns
	H3	SDI from SCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H4	Y or D from C/$\overline{D}$ Low	2	–	2	–	2	–	2	–	2	–	ns
	H5	SCLK High from PCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H6	C/$\overline{D}$ from PCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H7	Y from PCLK High	3	–	3	–	3	–	3	–	3	–	ns
t_{HZ}(1, 2)	2z, 4z	SCLK High to D or Y High Z	–	15	–	15	–	20	–	20	–	20	ns
t_{LZ}(1, 2)	3z,5z	C/$\overline{D}$ High to D or Y High Z	–	15	–	15	–	20	–	20	–	20	ns
t_{ZHL}(1, 2)	Z2, Z3	C/$\overline{D}$ Low to D or Y Valid 22, 23	–	15	–	15	–	20	–	20	–	20	ns
t_W	W1	PCLK (High & Low)	10	–	10	–	15	–	15	–	15	–	ns
	W2	SCLK (High & Low)	30	–	30	–	35	–	35	–	35	–	ns
	W3	C/$\overline{D}$ High	30	–	30	–	35	–	35	–	35	–	ns

NOTE:
1. Guaranteed but not tested.
2. OE = V_{IH}

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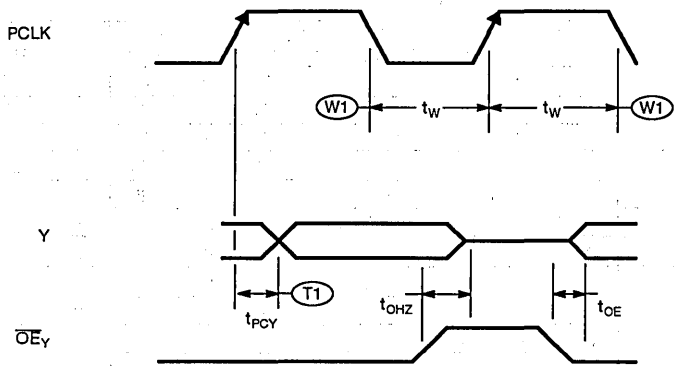
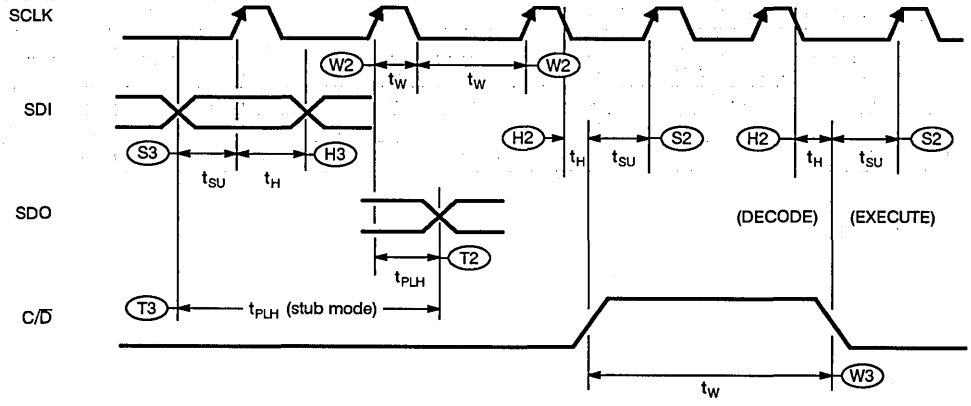
GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS

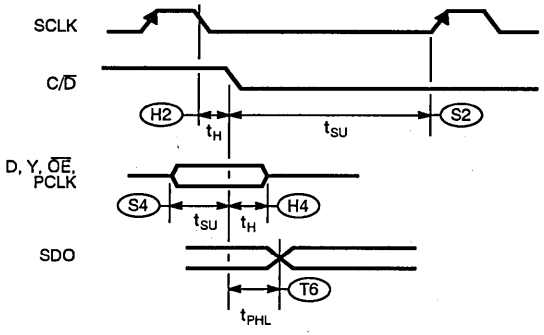


GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS

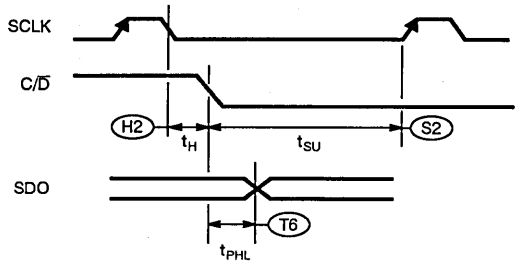


DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

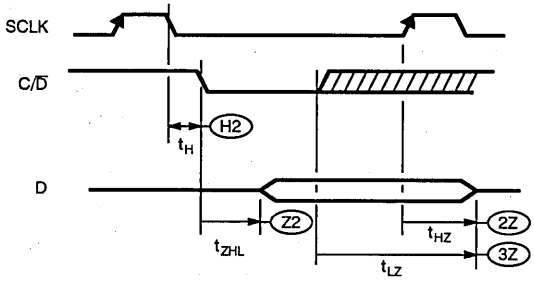
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



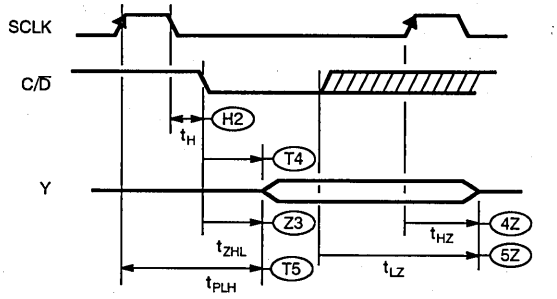
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



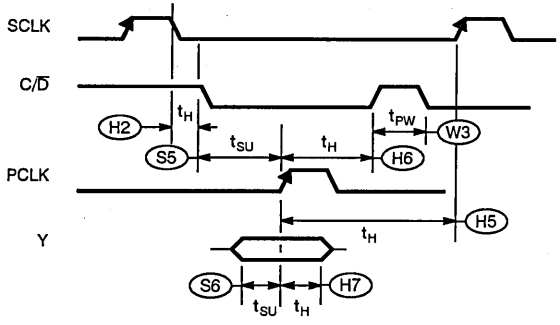
CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



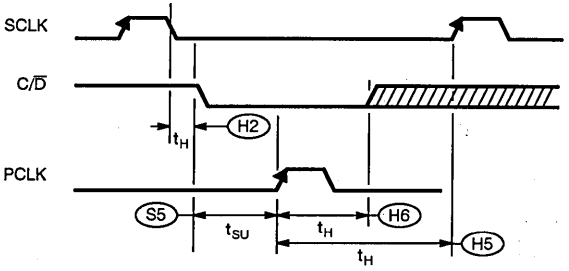
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



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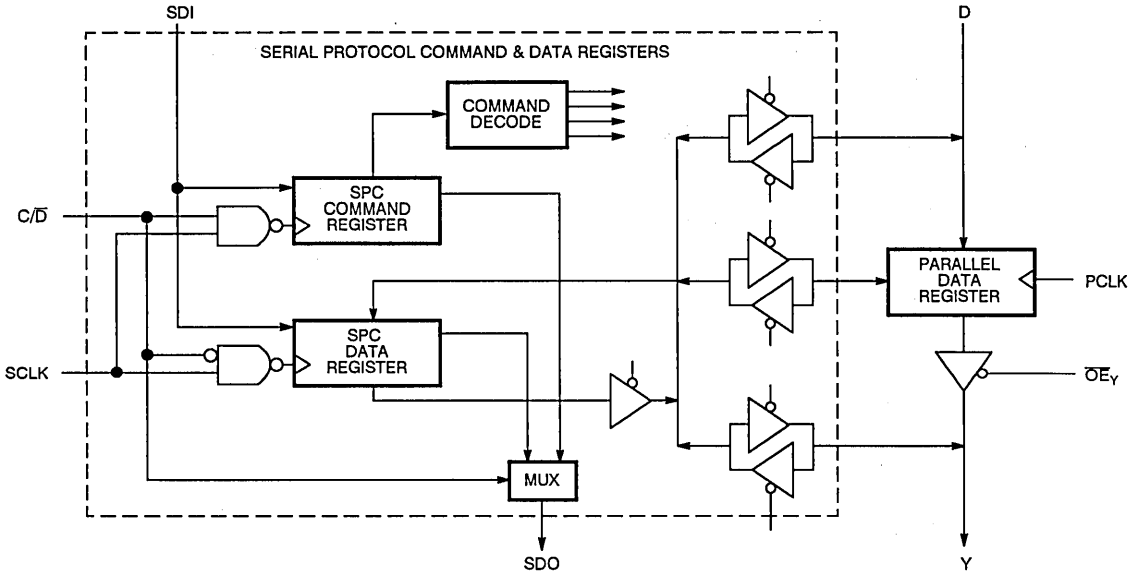
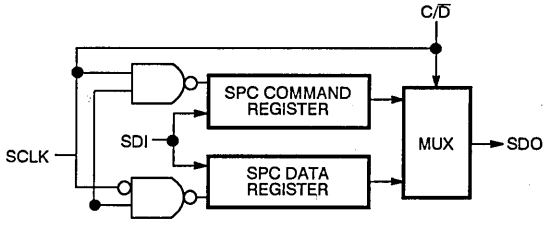
DETAILED FUNCTIONAL BLOCK DIAGRAM



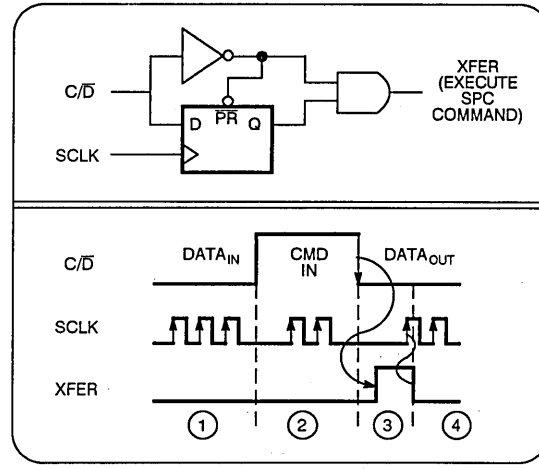
The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. The main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.



SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge.



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

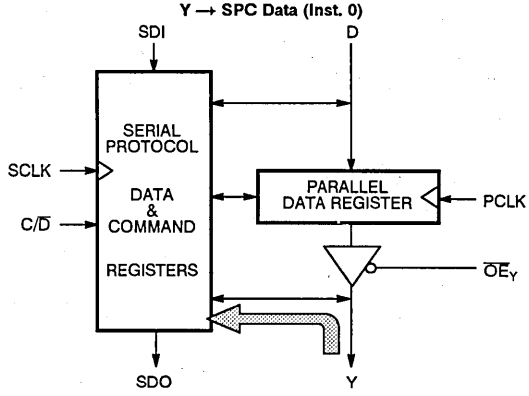
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

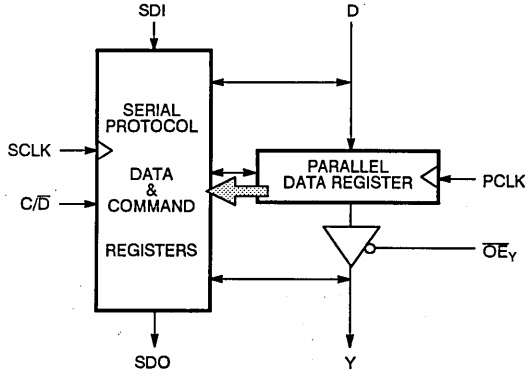
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

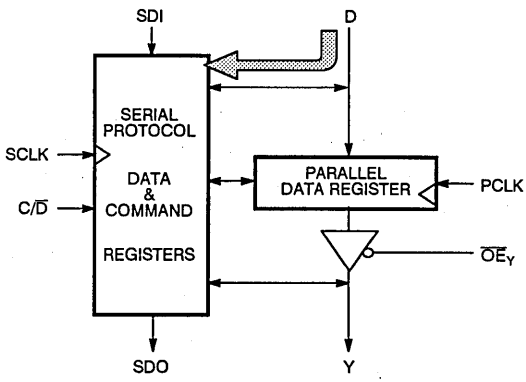
Y → SPC Data (Inst. 0)



Data Register → SPC Data (Inst. 1)



D → SPC Data (Inst. 2)



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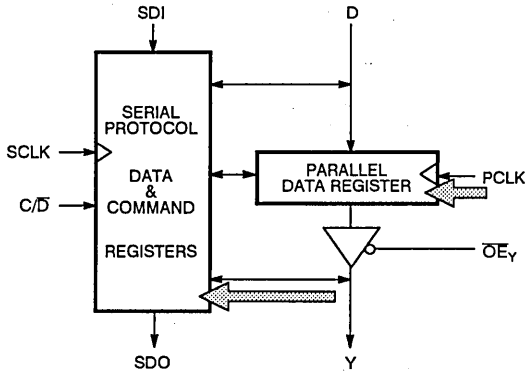
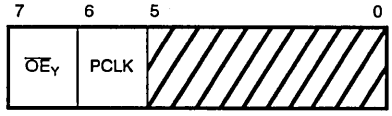
Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

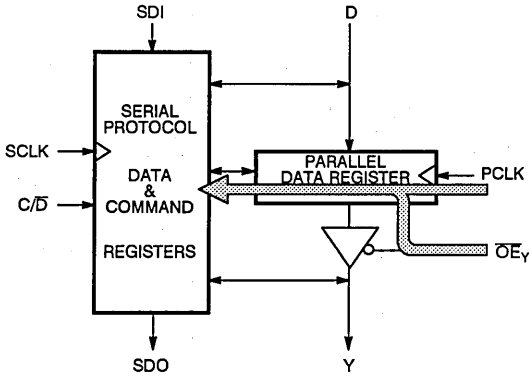
Y → SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

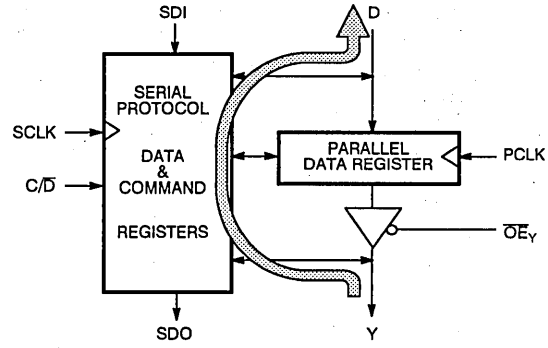


Status → SPC Data (Inst. 4)

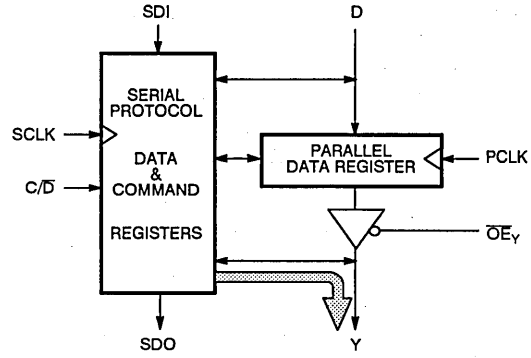


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

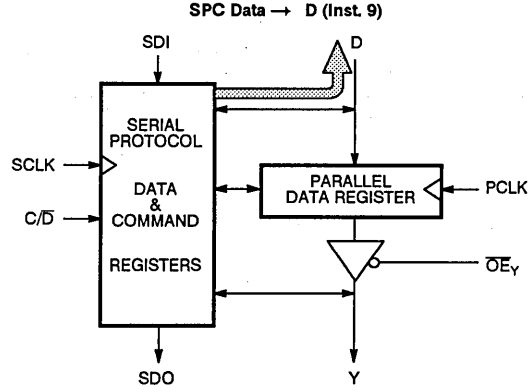


SPC Data → Y (Inst. 8)



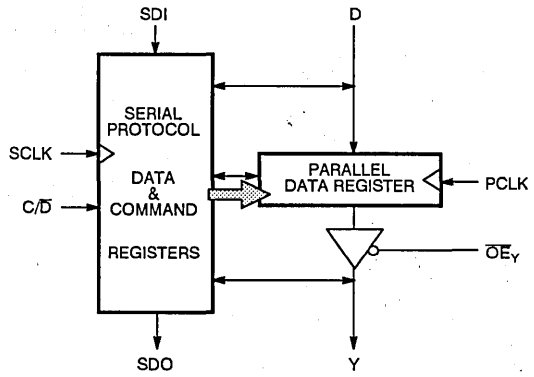
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

SPC Data → D (Inst. 9)



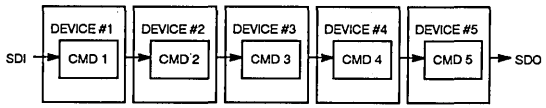
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.

SPC Data → Parallel Data Register (Inst. 10)



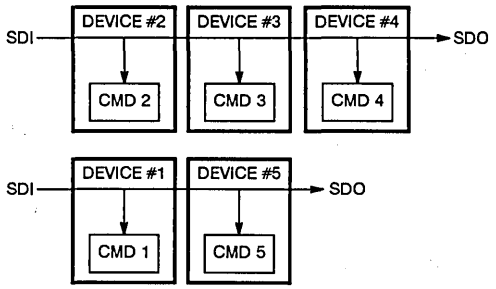
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



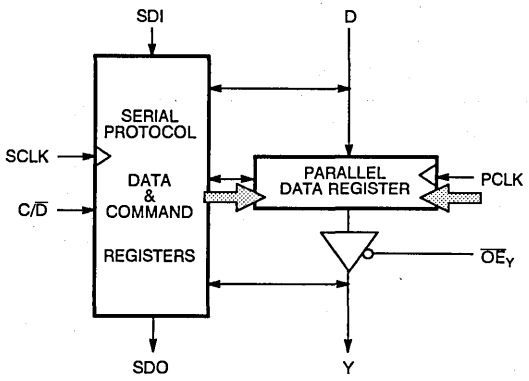
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

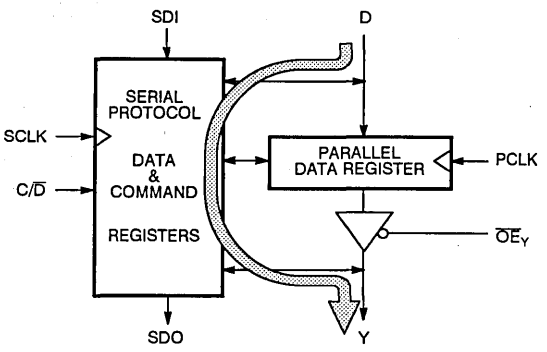


Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.

SPC Data → Parallel Data Register Synchronous w/PCLK (Inst. 13)

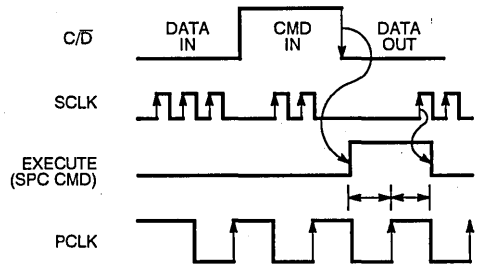


Connect D to Y (Inst. 14)



13

Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

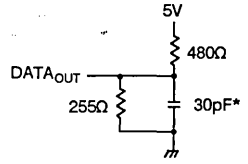


Figure 1. Output Load

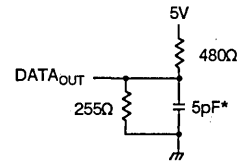
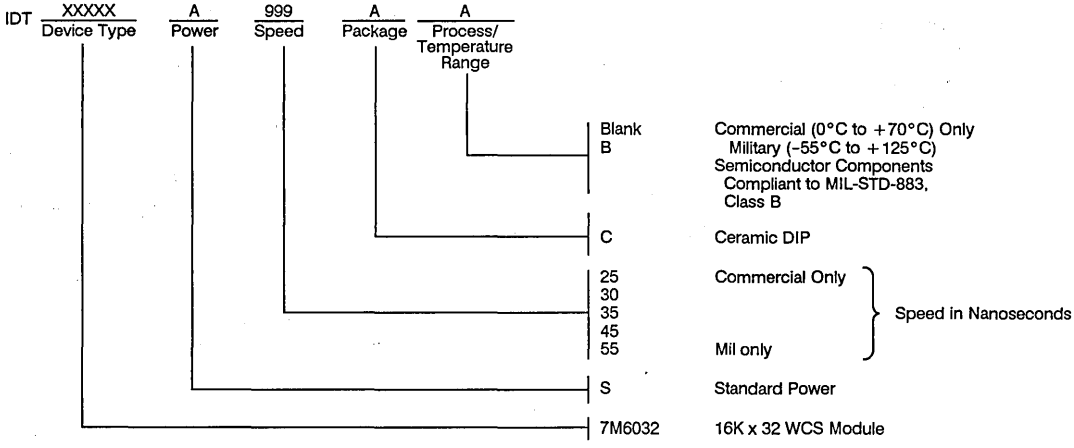


Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig.

ORDERING INFORMATION



Integrated Device Technology, Inc.

4K x 80 WRITABLE CONTROL STORE STATIC RAM MODULE WITH ON-BOARD SEQUENCER

PRELIMINARY
IDT 7M6052

FEATURES:

- Serial Protocol Channel (SPC™) reading, writing and interrogation
- Separate chip select, write enable and output enable memory controls
- High fanout pipeline register
- Fully width-expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact 128-pin ceramic QIP (quad in-line package)
- Single 5V (+/- 10%) power supply
- Inputs and outputs directly TTL-compatible
- Military modules available with semiconductor components manufactured in compliance to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M6052 is a 4K x 80 Writable Control Store with on-board sequencer, on a multilayer co-fired ceramic substrate, using five IDT71502 (4K x 16 registered RAMs), an IDT39C10 (12-bit sequencer) and an IDT54/74FCT521 (8-bit comparator) for parity verification. The IDT7M6052 is offered in a 128-pin, 600 mil wide quad in-line package (QIP).

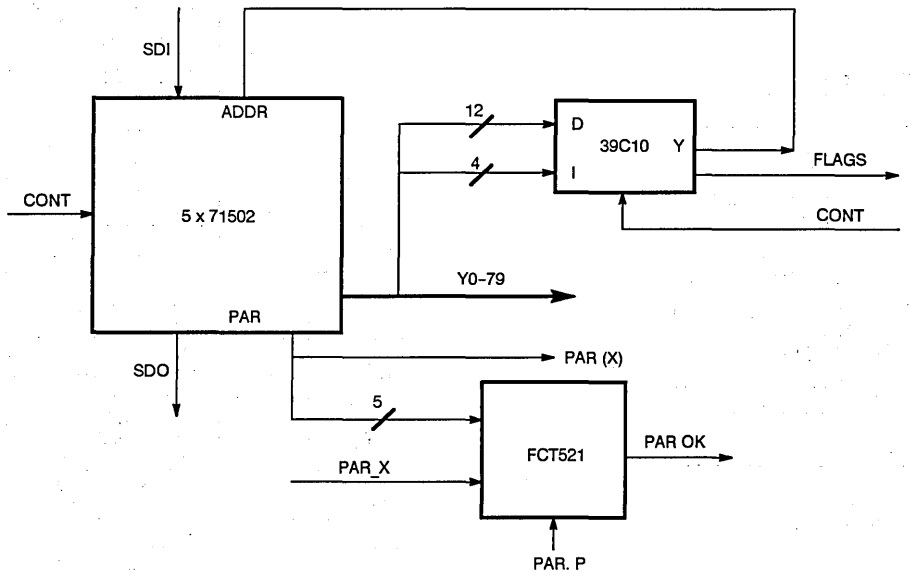
In normal operation (Read Mode), the D(0:11) inputs of the sequencer are driven by the Y(0:11) outputs of the first RAM and the I(0:3) inputs are driven by the Y(16:19) outputs of the second RAM. Since each of the RAMs have their own external output enabled, either or both of these fields can be overridden from an external source, i.e. by negating $\overline{OE}$ (0-15). Y(0:15) is placed in the Hi-Z mode, allowing the D(0:11) inputs to the sequencer to be driven from an external source (similarly for Y(16:32), which includes the I(0:3) field). The output from the sequencer drives the addresses of all of the RAMs. All the control, clocks and flags of the sequencer are connected directly to module pins for external control. (For additional details on how the sequencer operates, please refer to the IDT39C10 data sheet.) All controls and clocks, except for output enables, parity and the serial data path, are bussed to all RAMs and connected to module pins for external control. The serial data path is daisy chained through the five RAMs to give an 80-bit SPC configuration. (For additional information on the RAM operation, please refer to the IDT71502 data sheet).

The WCS can be loaded using either the serial data path and the SPC controls, or in parallel from the Y(0:79) pins, again using the SPC controls. The address for the RAMs will either be from the internal counter in each RAM for loading sequential locations, or by external control of the sequencer.

The parity output from each RAM is connected to a module pin and also to an input of the on-board comparator. The five RAM parities, together with 3 additional parity inputs (PAR_A to PAR_C), are compared to PAR_P (tied to all 8 inputs of the other side of the comparator) to generate $\overline{PAR\_OK}$.

The semiconductor components used on all IDT milatary modules are maufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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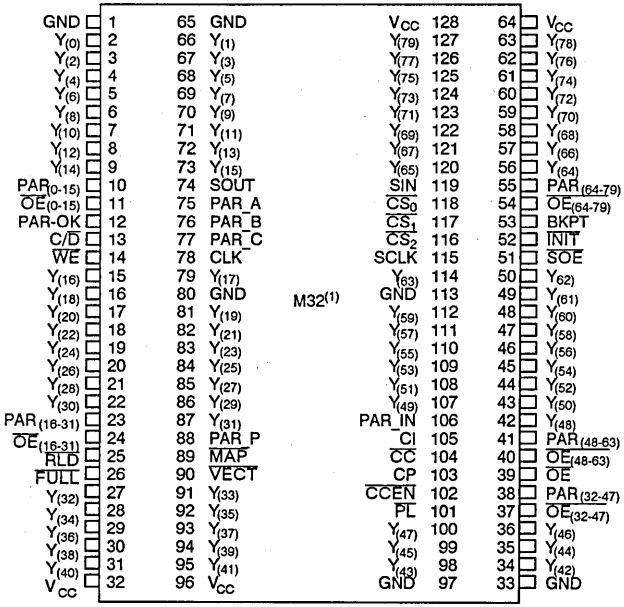
PINOUT CONFIGURATION



QIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M32 in the packaging section.

PIN DESCRIPTIONS

NAME	FUNCTION
$\overline{CS}_{0-2}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{SOE}$	Synchronous Output Enable
CLK	Clock (to register)
$\overline{INIT}$	Initialize
BKPT	Breakpoint Detect
PAR_{0-79}	Parity
S_{IN}	SPC Serial $DATA_{IN}$ (1)
S_{OUT}	SPC Serial $DATA_{OUT}$ (1)
SCLK	SPC Clock (1)
$C/\overline{D}$	SPC Command/$\overline{Data}$ (1)
GND	Ground
V_{CC}	Power

NOTE:

1. The Serial Protocol Channel (SPC) is discussed at length in IDT Application Note 16.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$\overline{OE}$	I	Tristates internal address bus for 71502s.
$\overline{CC}$	I	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$ (0-79)	I	Three-state control of Y_i outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
Y_i	O	Address to microprogram memory. Y_0 is LSB, Y_{79} is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.
PAR_OK	O	5 RAM parity bits, together with 3 parity inputs are compared to generate PAR_OK.
PAR_P	I	Generated from all 8 inputs from the other side of the comparator.
PAR IN	I	Parity input
PAR (A-C)	I	Parity inputs combined with the on board parity with the 71502 to generate parity across 8 bits for parity O.K.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN\ (D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN\ (A)}$	Input Capacitance (Control)	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	15	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 10%

SYMBOL	PARAMETERS	TEST CONDITIONS		MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	COM'L.	–	20	µA
			MIL.		50	
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	COM'L.	–	5	µA
			MIL.		10	
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	COM'L.	–	5	µA
			MIL.		10	
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA		–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA		2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	7M6052S25 COM'L. ONLY	7M6052S35 COM'L.	7M6052S35 MIL.	7M6052S45 COM'L.	7M6052S45 MIL.	7M6052S55 COM'L.	7M6052S55 MIL.	UNIT
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	850	825	925	825	925	825	925	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL} f = f_{MAX}, Output Open	1350	1300	1400	1225	1300	1175	1250	mA

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AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%

READ CYCLE
SET UP AND HOLD TIMES W.R.T. CLK (NOTE 1)

SYMBOL	PARAMETER	7M6052S25		7M6052S35		7M6052S45		7M6052S55		UNITS
		tS	tH	tS	tH	tS	tH	tS	tH	
t_{AS}, t_{AH}	Address A(0:11)	25	0	35	0	45	0	55	0	ns
t_{CS}	Chip Sel $\overline{CS}$	10	–	12	–	15	–	20	–	ns
t_S	Sync OE SOE	10	–	12	–	15	–	20	–	ns

SYMBOL	PARAMETER		MAX.		MAX.		MAX.		MAX.	UNIT
t_{PD}	Prop Delay CLK to Y(0:9)		12		15		20		25	ns

SET UP AND HOLD TIMES W.R.T. CP (NOTE 2)
(For All Speed Grades)

PARAMETER	tS	tH	UNITS
Data D(0:11) to REG/CNT	6	0	ns
Data D(0:11) to PROG CNT	13	0	ns
Instruction I(0:3)	23	0	ns
Test Flag $\overline{CC}$	15	0	ns
Test Flag EN $\overline{CLEN}$	15	0	ns
Carry in CI	6	0	ns
Reload RLD	11	0	ns

COMBINATION DELAYS

(For All Speeds)	MAX.	UNITS
D(0:11) to A(0:11)	12	ns
I(0:3) to A(0:11)	20	ns
I(0:3) to source con7	12	ns
$\overline{CC}$ to A(0:11)	16	ns
$\overline{CCEN}$ to A(0:11)	16	ns
CP to A(0:11)	28	ns
CP to $\overline{FULL}$	22	ns
$\overline{OE}$ to A(0:11)	10	ns

READ CONTROL

SYMBOL	PARAMETER	7M6052S25		7M6052S35		7M6052S45		7M6052S55		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{OE}	ASYNC	–	14	–	17	–	25	–	30	ns
t_{OZ}	ASYNC	–	14	–	17	–	25	–	30	ns
t_{SOE}	SYNC	–	17	–	22	–	30	–	35	ns
t_{SOE}	SYNC	–	17	–	22	–	30	–	35	ns
t_{PAR}	Individual Parity	–	30	–	35	–	45	–	55	ns
t_{PAR-}	OK	–	40	–	45	–	55	–	65	ns

SYMBOL	PARAMETER	7M6052S25		7M6052S35		7M6052S45		7M6052S55		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{IW}	INIT Pulse Width	35	–	40	–	50	–	60	–	ns
t_{IR}	INIT REC TIME	35	–	40	–	50	–	60	–	ns
t_{INIT}	INIT REC to Y(0;79)	–	50	–	55	–	70	–	85	ns

CLOCKS

PARAMETER	7M6052S25		7M6052S35		7M6052S45		7M6052S55		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLK High Min	15	–	15	–	20	–	25	–	ns
CLK Low Min	15	–	15	–	20	–	25	–	ns
CP High Min	20	–	20	–	20	–	20	–	ns
CP Low Min	20	–	20	–	20	–	20	–	ns

WRITE CYCLE

SYMBOL	PARAMETER	7M6052S25		7M6052S35		7M6052S45		7M6052S55		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write CYC Time	40	–	50	–	65	–	80	–	ns
t_{WAS}	Address SU	2	–	2	–	5	–	5	–	ns
t_{W}	Write Pulse Width	25	–	30	–	50	–	60	–	ns
t_{DW}	Data to End of Write	17	–	20	–	25	–	30	–	ns
t_{WDH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WCW}	CS to End of Write	25	–	30	–	50	–	60	–	ns
t_{WR}	Write Recovery	5	–	5	–	5	–	5	–	ns
t_{AW}	Addr Valid to End of Write	30	–	35	–	55	–	65	–	ns

SPC ALL SPEEDS

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{SCLK}	SCLK Period	100	–	ns
t_{SCW}	SCLK Pulse Width	45	–	ns
t_{SDS}	Serial Data Set-up Time	20	–	ns
t_{SDH}	Serial Data Hold Time	5	–	ns
t_{SCD}	Clock to Serial Data Output Delay	–	35	ns
t_{SPD}	Serial Data-In-to-Out Delay, Stub Mode	–	120	ns
t_{CMLH}	Command/Data Set-up Time, Low-to-High[2]	20	–	ns
t_{CMHC}	Command/Set-Up Time, High-to-Low (Execution Time)[2]	40	–	ns
t_{CMH}	Command/Data Hold Time[2]	20	–	ns

NOTES:
1. Since A(0:11) are being driven by the O/P of the 39C10 the delays from the sequencer must be added to the A(0:11) set time.
2. D(0:11) and I(0:3) are being driven by the O/P of two 71502s, Y(0:11) and Y(16:19), therefore the delay of CLK to Y(0:79) must be added to the set up time for the approximate parameters.

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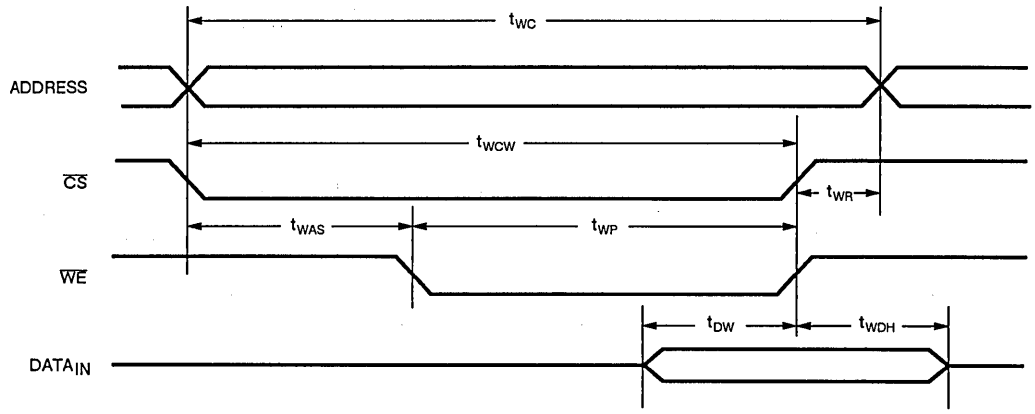
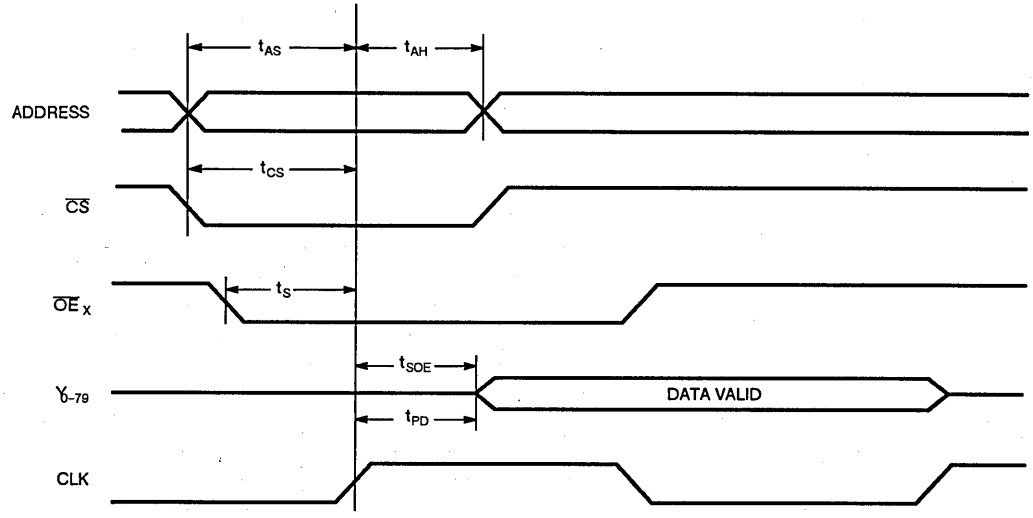
TIMING WAVEFORM OF WRITE CYCLE [1]



NOTE:
1. A write occurs during the overlap of both $\overline{CS}$ and $\overline{WE}$ low.

TIMING WAVEFORM OF READ CYCLE



The following descriptions are supplemental. Selected portions of the 39C10 and the 71502 data sheets are attached for further understanding of the 7M6052.

IDT39C10 PRODUCT DESCRIPTION

The IDT39C10s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 4K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of twelve D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control (RLD) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT39C10s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 12-bit incrementer followed by a 12-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are twelve D-inputs on the IDT39C10s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 12-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT39C10s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT39C10s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT39C10s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{\text{FULL}}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of zero. Similary, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT39C10s' internal 12-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 12-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, Instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT39C10s provide a 12-bit address at the Y outputs that are under control of the $\overline{\text{OE}}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT39C10s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

IDT39C10 OPERATION

The IDT39C10s are CMOS pin-compatible implementations of the Am2910 & 2910A microprogram sequencers. The IDT39C10's microprogram is functionally identical except that it provides a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{\text{PL}}$, $\overline{\text{MAP}}$, $\overline{\text{VECT}}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs only one of the three outputs ($\overline{\text{PL}}$, $\overline{\text{MAP}}$, $\overline{\text{VECT}}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{\text{CC}}$ and $\overline{\text{CCEN}}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{\text{RLD}}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{\text{RLD}}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{\text{OE}}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT39C10s is a last-in/first-out memory that is 12-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change

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the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more pushes than pops have occurred since the stack was last empty. When this happens, the Full Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT39C10 INSTRUCTION SET

This data sheet contains a block diagram of the IDT39C10 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word ($I_3 - I_0$). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 4K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT39C10s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT39C10s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT39C10s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT39C10 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 – CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 – CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source, except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 – CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test

is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 – REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 – REPEAT PIPELINE COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 – CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 – CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT39C10s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs,the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 – LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 – TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 – CONTINUE (CONT)

Continue is a simple instruction where the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 – THREE WAY BRANCH (TWB)

The Three-Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT39C10's flow diagram and is also described in full detail in the IDT39C10's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT39C10s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT39C10 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

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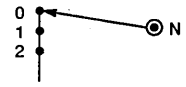
IDT39C10 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

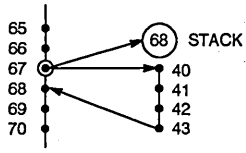
NC = No Change; DEC = Decrement

FIGURE 1. IDT39C10B FLOW DIAGRAMS

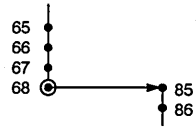
0 Jump Zero (JZ)



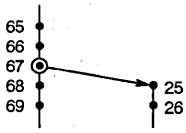
1 Cond JSB PL (CJS)



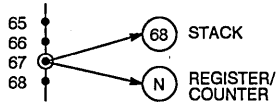
2 Jump Map (JMAP)



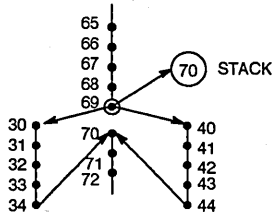
3 Cond Jump PL (CJP)



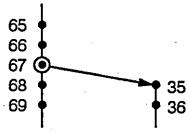
4 Push/Cond LD CNTR (PUSH)



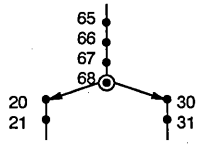
5 Cond JSB R/PL (JSRP)



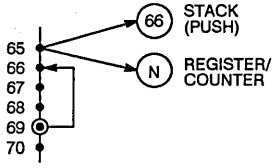
6 Cond Jump Vector (CJV)



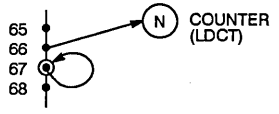
7 Cond JUMP R/PL (JRP)



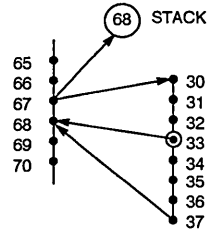
8 Repeat Loop, CNTR ≠ 0 (RFCT)



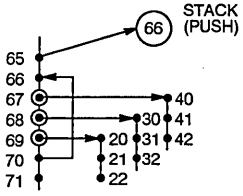
9 Repeat PL, CNTR ≠ 0 (RPCT)



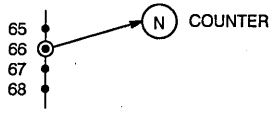
10 Cond Return (CRTN)



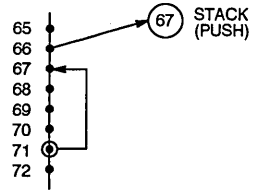
11 Cond Jump PL & POP (CJPP)



12 LD CNTR & Continue (LDCT)

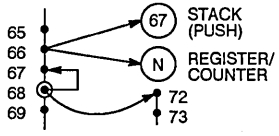


13 Test End Loop (LOOP)



14 Continue (CONT)

15 Three-Way Branch (TWB)



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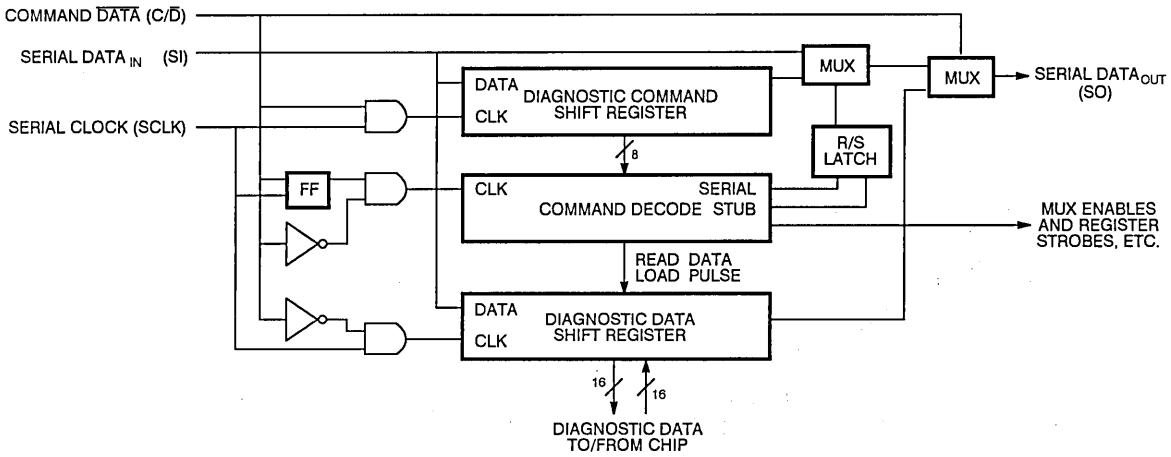
IDT39C10 INSTRUCTIONS

I_3- I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	CLEAR	0	CLEAR	HOLD	$\overline{PL}$
1	CJS	Cond JSB PL	X	PC	HOLD	D	PUSH	HOLD	$\overline{PL}$
2	JMAP	Jump Map	X	D	HOLD	D	HOLD	HOLD	$\overline{MAP}$
3	CJP	Cond Jump PL	X	PC	HOLD	D	HOLD	HOLD	$\overline{PL}$
4	PUSH	PUSH/Cond Ld Cntr	X	PC	PUSH	PC	PUSH	Note 1	$\overline{PL}$
5	JSRP	Cond JSB R/PL	X	R	PUSH	D	PUSH	HOLD	$\overline{PL}$
6	CJV	Cond Jump Vector	X	PC	HOLD	D	HOLD	HOLD	$\overline{VECT}$
7	JRP	Cond Jump R/PL	X	R	HOLD	F	HOLD	DEC	$\overline{PL}$
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	$\overline{PL}$
			= 0	PC	POP	PC	POP	HOLD	$\overline{PL}$
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	$\overline{PL}$
			= 0	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
10	CRTN	Cond RTN	X	PC	HOLD	F	POP	HOLD	$\overline{PL}$
11	CJPP	Cond Jump PL & POP	X	PC	HOLD	D	POP	HOLD	$\overline{PL}$
12	LDCT	LD Contr & Continue	X	PC	HOLD	PC	HOLD	LOAD	$\overline{PL}$
13	LOOP	Test End Loop	X	F	HOLD	PC	POP	HOLD	$\overline{PL}$
14	CONT	Continue	X	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
15	TWB	Three-Way Branch	≠ 0	F	HOLD	PC	POP	DEC	$\overline{PL}$
			= 0	D	POP	PC	POP	HOLD	$\overline{PL}$

NOTE:
1. If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

IDT71502 DESCRIPTION
SPC FUNCTIONAL BLOCK DIAGRAM



SPC COMMAND FORMAT

7 — 4	3 — 0
SPC Command Code 4 bits	SPC Register Code 4 bits

SPC COMMAND CODES

COMMAND CODE	READ/WRITE FUNCTION	ACTION	NOTES
0	Read	Read Register	Uses Register Select Field
1	Write	Write Register	Uses Register Select Field
2	Read	Read Register and Increment Initialize Counter	Serial RAM Read
3	Write	Write and Increment Initialize Counter	Serial RAM Write
4-C	–	Reserved (No-Op)	–
D	Write	Stub Diagnostic	Broadcast Commands
E	Write	Serial Diagnostic	Serial Commands
F	–	No-Op	Guaranteed No-Op

SPC REGISTER CODES

REGISTER CODE	READ/WRITE FUNCTION	REGISTER	NOTES
0	R/W	Initialize Counter	–
1	R/W	RAM Output	–
2	R/W	Pipeline Register	–
3	R/W	Break Mask Register	–
4	R/W	Break Data Register	–
5	R/W	Set-up + Status Register	Break Multiplexer, Trace Mode, etc.
6	Rd Only	Y_{15} -Y_0 (Data Pins)	Data Pins of Chip
7	Rd Only	RAM Address	Address Going into RAM
8-F	–	Reserved (unused)	–

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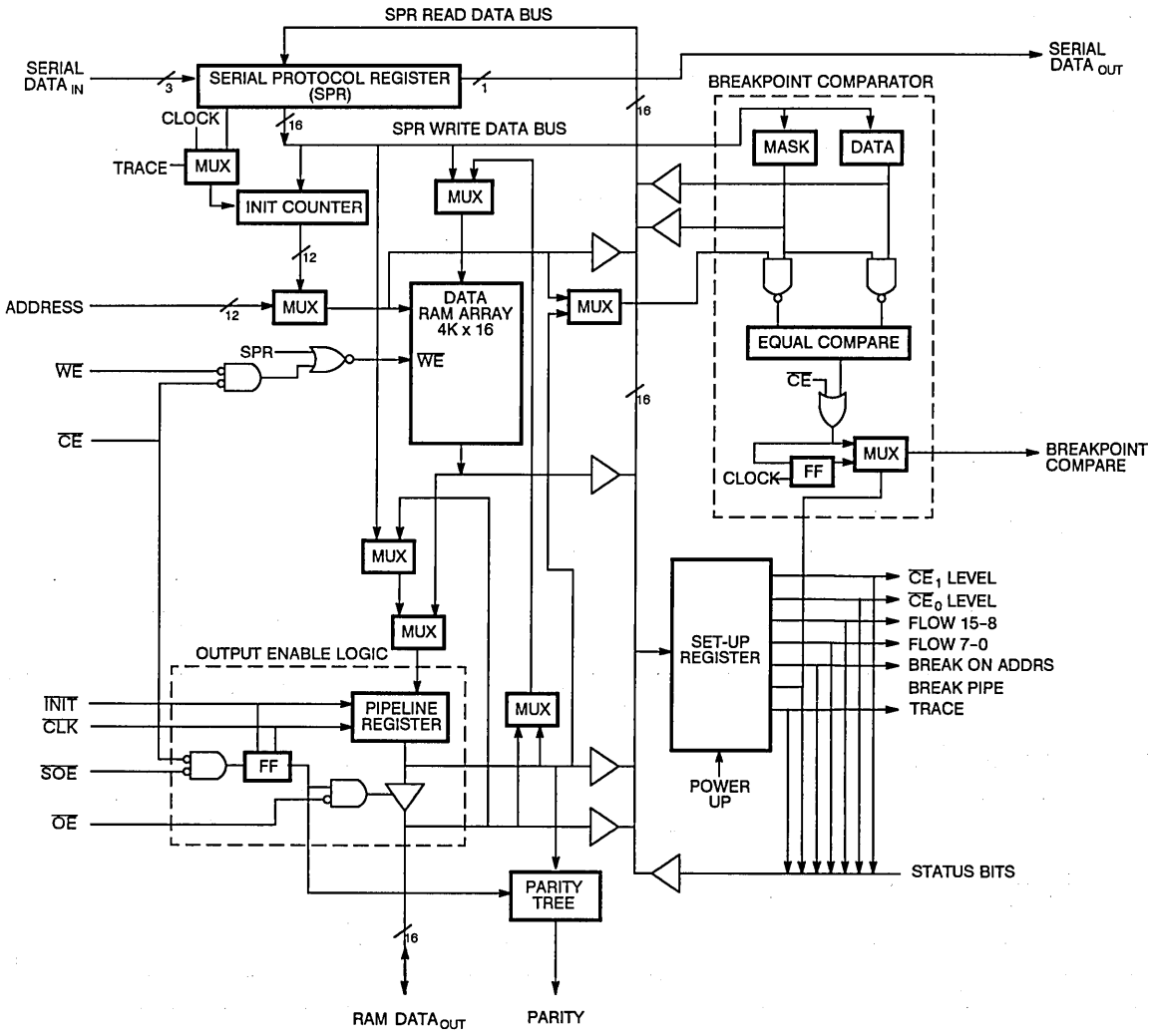
REGISTERED RAM DATA FLOW BLOCK DIAGRAM



SET-UP REGISTER FORMAT

BIT	NAME	TYPE [1]	FUNCTION	POWER-UP VALUE
15	$\overline{CE}$	RO	Chip Enable State: NOR of All Chip Enable Pins	0
14	$\overline{SOE}$ FF	RO	$\overline{SOE}$ FF State: 1 = Output Enabled, 0 = Output Disabled	0
13	$\overline{SOE}$ Pin	RO	$\overline{SOE}$ Pin State: 1 = High, 0 = Low	0
12	$\overline{OE}$ Pin	RO	$\overline{OE}$ Pin State: 1 = High, 0 = Low	0
11	$\overline{WE}$ Pin	RO	$\overline{WE}$ Pin State: 1 = High, 0 = Low	0
10	$\overline{INIT}$ Pin	RO	$\overline{INIT}$ Pin State: 1 = High, 0 = Low	0
9	BP Compare	RO	Breakpoint Comparator Output: 1 = Compare Valid	0
8	BP Pin	RO	BP Pin State: 1 = High, 0 = Low	0
7	$\overline{CS}_1$ Level	R/W	0 = $\overline{CS}_1$ is Low Active; 1 = CS_1 is High Active	0
6	$\overline{CS}_0$ Level	R/W	0 = $\overline{CS}_0$ is Low Active; 1 = CS_0 is High Active	0
5	Non-Reg High	R/W	Set Pipeline Register Bits 15-8 to Flow-Through Mode	0
4	Non-Reg Low	R/W	Set Pipeline Register Bits 7-0 to Flow-Through Mode	0
3	–	–	(Unused)	0
2	BC Address	R/W	0 = Breakpoint on Pipeline Register Output, 1 = Breakpoint on RAM Address Inputs	0
1	BC Pipelined	R/W	Set Breakpoint Output MUX for Pipeline FF Output	0
0	Trace Mode	R/W	Set for Trace Mode: Y_{15-0} to Pipeline Register, Pipeline Register to RAM, Initialize Counter as Address, Write with Clock Pulse	0

NOTE:
1. RO means Read Only. R/W means Read/Write.

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IDT71502 GENERAL DESCRIPTION

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and read-back of the RAM data. A RAM address counter is also provided to speed up RAM load and read-back. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 Registered RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize register as the address counter. The Trace mode, in combination with the breakpoint comparator, allows the IDT71502 Registered RAM to be used as a one-chip logic analyzer.

RAM Operation

After power up, and in its typical operating mode, the IDT71502 Registered RAM is set for pipelined read and direct (non-pipelined) write. Data may be directly written into the RAM by driving the address and data inputs and strobing the Write Enable input. Data is read from the RAM by driving the address lines and clocking the pipeline register.

The RAM may also be read and written by the Serial Protocol Channel (SPC). This is the typical path for loading the RAM after power up.

Serial Protocol Channel

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. A block diagram of the command decode logic is shown for reference. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (NOTE: The data to the SPC is shifted in LSB first.)

The SPC is connected to the outside world through four wires. These wires consist of serial data in and out, a shift clock and a command/$\overline{\text{data}}$ line. When the command/$\overline{\text{data}}$ line is high, commands are shifted from the serial data in to the command register by the clock. When the command/$\overline{\text{data}}$ line is low, data is shifted into the data shift register by the clock. When the command/data line transitions from high (command) to low (data), a clock pulse is generated internally to the command decode logic. This pulse lasts from the beginning of the high-to-low transition to the next serial clock pulse and is used to execute the command in the command register.

Two of the defined commands are Serial and Stub. These commands control a latch which determines the source of the serial data out in the command mode. The Serial command causes the data output to be taken from the last stage of the command shift register. This is the normal operating mode, where all the shift registers in a system are connected into one long shift register. The SPC logic in the IDT71502 is automatically set to the Serial mode by power up. The Stub command sets the latch and causes the serial output data to be taken from the serial input. In this mode, the serial data is passed directly from one chip to the next so that all command registers have the same data at their serial inputs. This allows a broadcast mode where all command registers in a system can be loaded with the same command at the same time.

RAM Load/Readback Logic

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

A detailed block diagram of the IDT71502 Registered RAM, showing the various internal registers and the load and readback paths, is shown in the Registered RAM Data Flow Block Diagram. In addition to the logic shown in the Functional Block Diagram on the first page of the data sheet, there is an Initialize Counter for loading and initializing the RAM, Break Data and Mask registers for the Breakpoint Comparator and multiplexers at the input to the Pipeline register for allowing data from the data I/O pins to be clocked into the Pipeline register in the Trace mode before being written into the RAM. The data flow block diagram also shows the various multiplexers for routing data for breakpoint and readback use.

Initialize Counter

The Initialize Counter provides the initial address to the RAM after reset of the part. A pulse applied to the Initialize pin causes the Initialize Counter to be gated to the RAM address and the RAM data to be preset into the pipeline register. This provides an initial value in the pipeline register before the first clock pulse arrives. The Initialize Counter can be reset to zero at power up of the chip and can be loaded with a value other than zero by the SPC. Once loaded with a value by the SPC, this value is used in further chip reset operations.

Set-up Register

The Set-up Register is a 16-bit register used to set the chip operating mode and to read back chip operating status conditions. A command word written into the Set-up Register sets 7 latches which control the chip operating conditions. Reading the Set-up Register provides the current status of these 7 latches and various other signals on the chip. At power up, the 7 latches are cleared to zero and the Initialize counter is cleared to zero. The format of the Set-up Register is shown in the Set-up Register Format table.

The Set-up Register has 7 latches which determine the operating mode of the chip. These are $\overline{\text{CS}}_1$, $\overline{\text{CS}}_0$, Non-Reg High, Non-Reg Low, BC RAM, Break Pipe and Trace. The $\overline{\text{CS}}_1$ and $\overline{\text{CS}}_0$ bits determine the polarity of the $\overline{\text{CS}}_1$ and $\overline{\text{CS}}_0$ chip enables. The Non-Reg High and Low bits set the upper and lower bytes of the Pipeline Register to a flow-through mode, respectively. The BC RAM bit determines the source of the data for breakpoint comparison, either the Pipeline Register or the RAM address. The Break Pipe latch switches the breakpoint pin multiplexer from the comparator to the buffer flip-flop. The trace latch sets the chip into the Trace mode.

Power Up State

Power up is defined as taking V_{CC} from below 1.0 volts to 5.0 volts nominal. This generates power up reset, an internal signal which resets several registers on the chip. After power up, the IDT71502 is in the following state:

- Set-up Register cleared to zero
- Initialize Counter cleared to zero
- Breakpoint Mask Register cleared to equal (Breakpoint output high)
- $\overline{SOE}$ Flip-Flop cleared to outputs off

Note that taking V_{CC} from 5.0 volts to 2.0 volts and back to 5.0 volts will not cause power up reset.

Set-up Register: Programmable Chip Enable

The chip enable function is programmable by bits in the Set-up Register. The logic for this is shown in Figure 1. The bits in the Set-up Register define the active state of each chip enable: high or low. This allows up to four RAMs to be cascaded in depth with no external decoders required (16K x 16 bits of RAM).

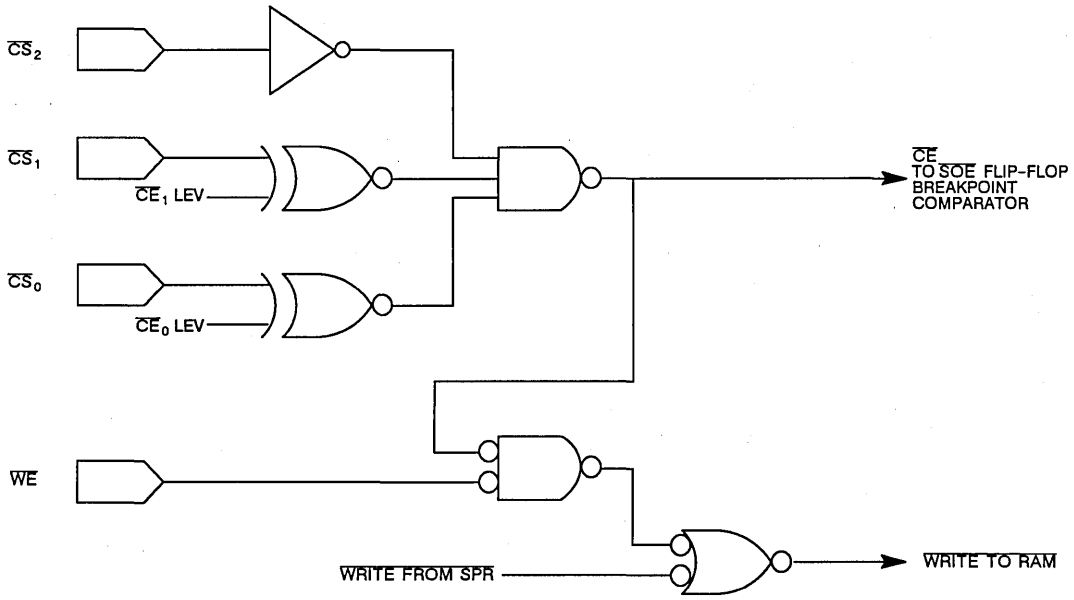

Figure 1. Chip Enable Logic Block Diagram

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Set-up Register: Non-Registered Outputs

Two bits of the Set-up Register, Non-Reg Hi and Non-Reg Lo, can be set to cause the Pipeline Register bits 15-9 and 7-0, respectively, to be set to the flow-through mode. In the flow-through mode, both latches of the register are open and the register acts like a simple buffer with its output following its input. This allows the user to have some non-registered bits in microcode applications. The output circuit consisting of the Pipeline Register, the Synchronous Output Enable ($\overline{SOE}$), and the Output Enable ($\overline{OE}$), has some special logic to support this mode, as shown in Figure 2. Also, activating the Initialize pin causes the Pipeline Register to be put in the flow-through mode. Figure 2 shows the Pipeline Register as two latches operated in the MASTER/SLAVE configuration. The clock input will cause the latch pair to work as a register. If the Initialize pin is activated, both registers will be placed in the flow-through mode by the OR gates. Also, if either Non-Reg bit is set, its corresponding 8-bit portion of the register will be placed in the flow-through mode.

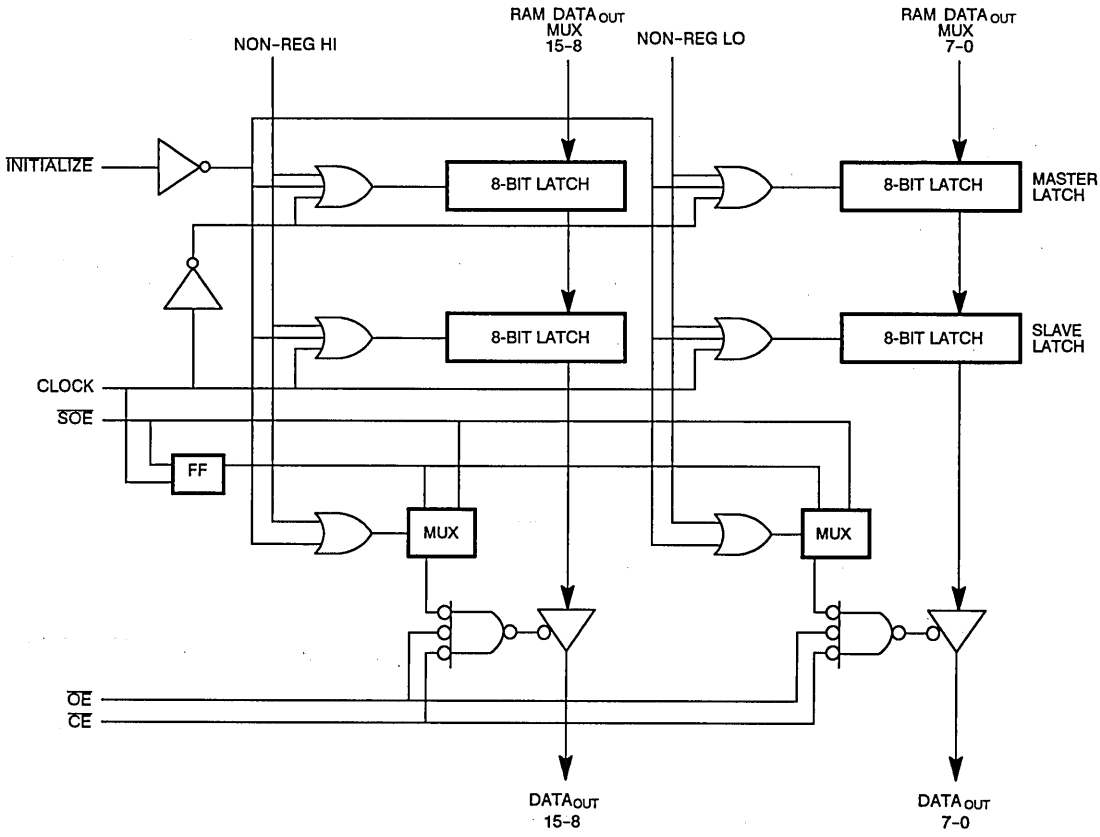

Figure 2. Output Logic Block Diagram

When in the flow-through mode, the output enable flip-flop for that half must also be in the flow-through mode for external chip expansion to work properly. A non-registered RAM bit must be enabled by a non-registered output enable, while a registered bit must be enabled by a synchronous output enable. This is done by using the non-registered bit to control a multiplexer which selects between the $\overline{SOE}$ flip-flop input and output as the source of the output enable.

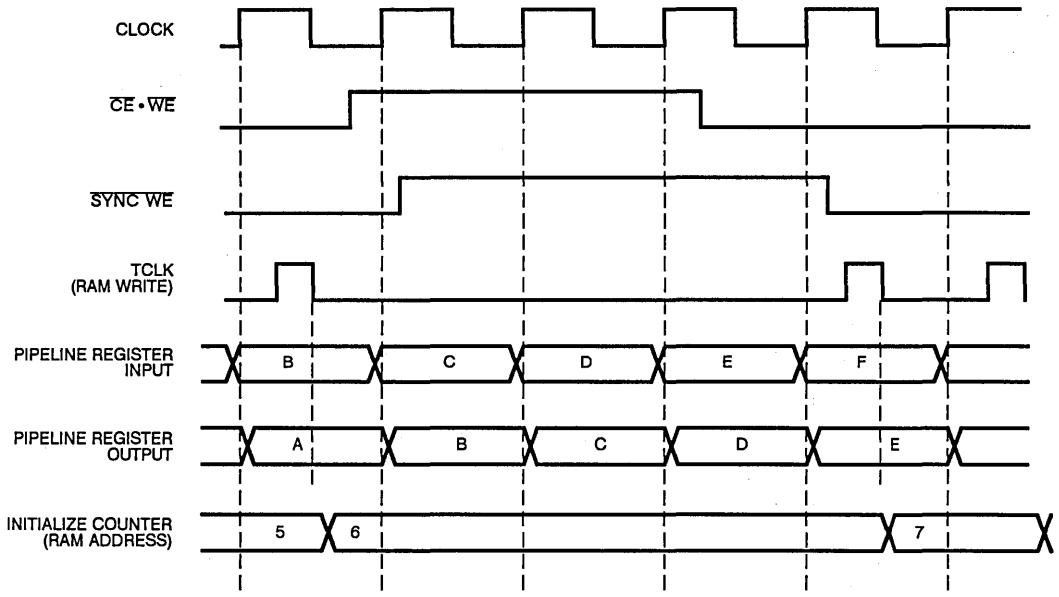

Figure 4. Trace Mode Sequence Timing Diagram

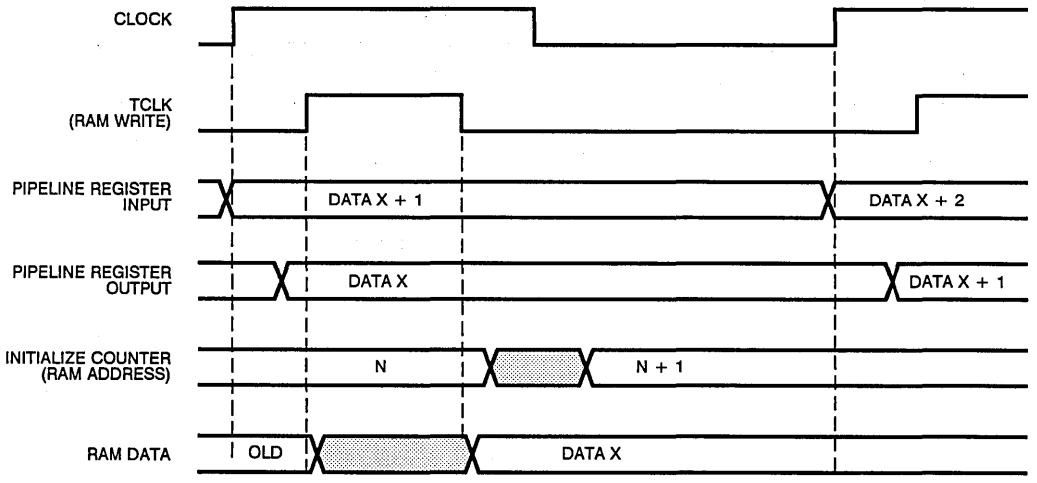

Figure 5. Trace Mode Clock Timing Diagram

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Parity Output

The Parity Output pin is generated from a 16-bit parity tree, as shown in the Parity Tree Logic Block Diagram (Figure 6). Even parity is used. Parity is generated on the contents of the Pipeline Register. The parity output driver is three-state and is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the parity output.

The Parity Output always reflects the parity of the registered value. Additional flip-flops and multiplexers are included in the parity tree to cover the case of non-registered outputs. If one or both bytes of the Pipeline Register are set to the Non-Registered mode, a flip-flop pipeline delay is added to the corresponding byte parity chain to make the result of that byte parity calculation the same as if the Pipeline Register was not in the Non-Pipelined mode.

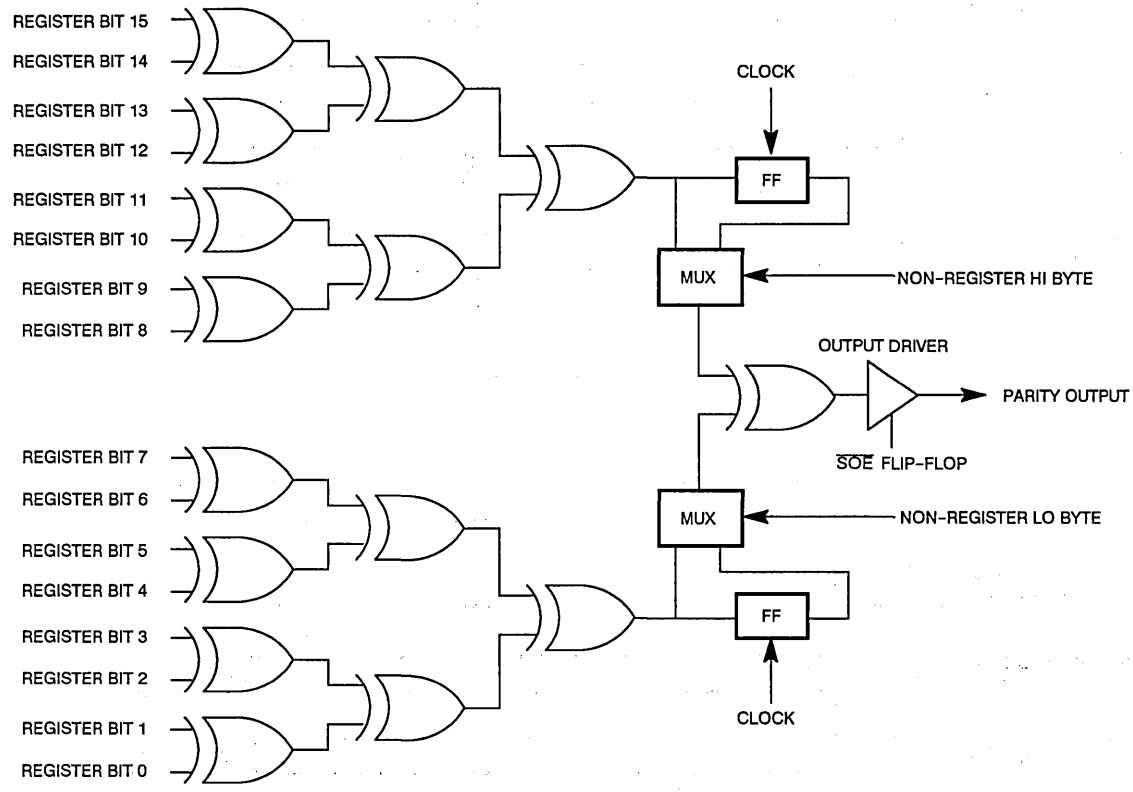
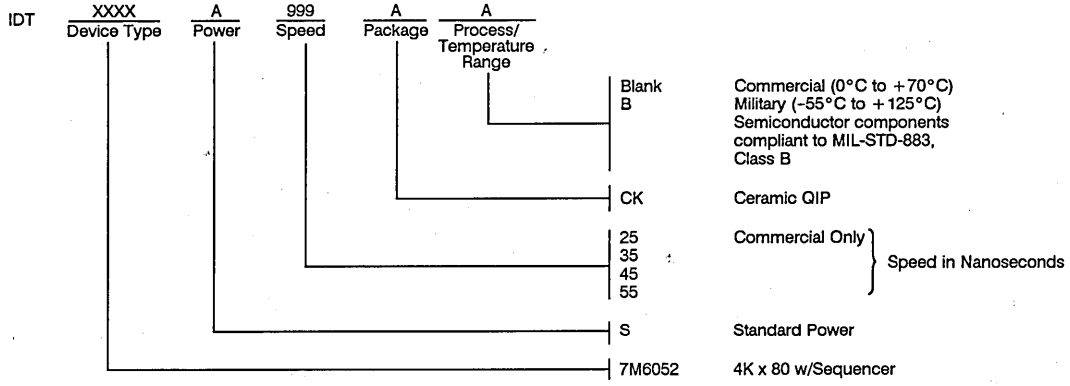


Figure 6. Parity Tree Logic Block Diagram

ORDERING INFORMATION



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Integrated Device Technology, Inc.

8K x 36 FIFO MODULE

IDT 7MB2001S

FEATURES:

- First-In/First-Out memory module
- Asynchronous and simultaneous read and write
- Configurable as 8K x 36 or 16K x 18 unidirectional or 8K x 18 bidirectional FIFO
- Multiple status flags: Full, Empty
- Ultra-high-speed: 40ns access time
- Fully expandable by both word depth and/or bit width
- Dual-port zero fall-through time architecture
- Available in high-density 108-pin quad in-line FR-4 package

DESCRIPTION:

The IDT7MB2001 is a FIFO module that consists of eight IDT72041s (4K x 9). The IDT72041 is a dual-ported memory that utilizes a special first-in/first-out algorithm that loads and empties data on a first-in/first-out basis.

The IDT7MB2001 is user-configurable in three modes:

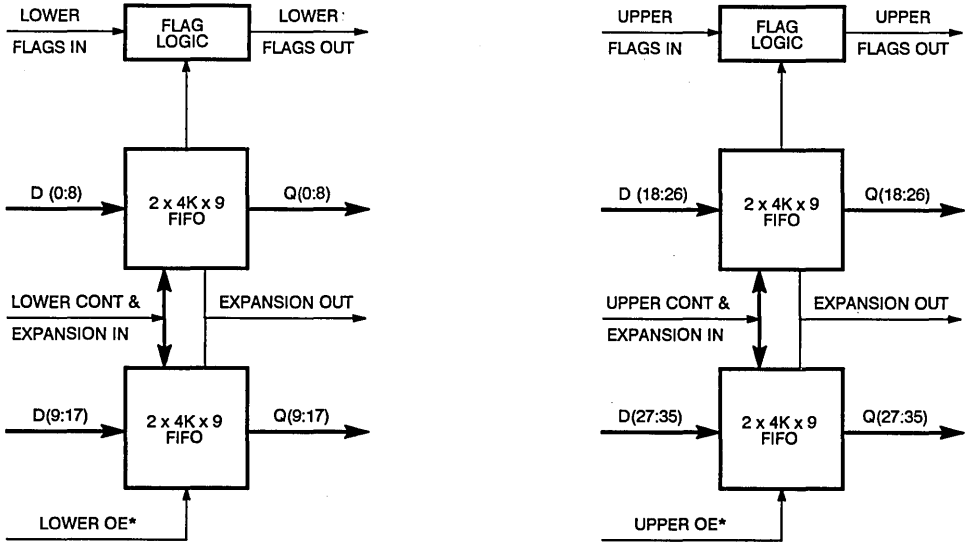
- An 8K x 36 unidirectional FIFO, or
- A 16K x 18 unidirectional FIFO, or
- An 8K x 18 bidirectional FIFO.

In all three modes, the module offers two flags, Full and Empty, to prevent data overflow and underflow. Expansion logic of the IDT72041s allows wider and/or deeper FIFOs to be created using multiple devices without external logic.

The module also allows asynchronous and simultaneous read and write operations. The dual-port RAM array allows zero fall-through time and a ninth bit is provided for every byte to store parity.

Access time is as fast as 40ns. The module is offered in a high-density 108-pin quad in-line package.

FUNCTIONAL BLOCK DIAGRAM



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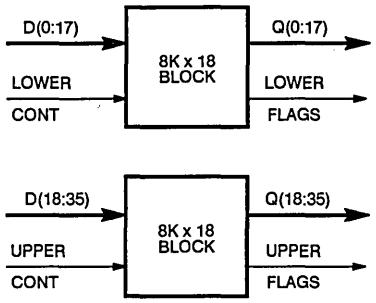
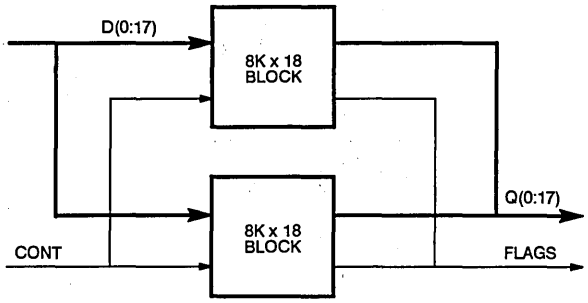
FUNCTIONAL BLOCK DIAGRAM (Continued)

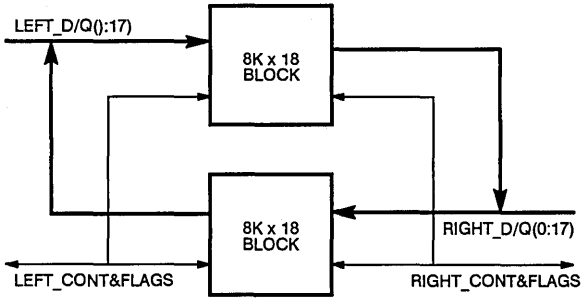
8K x 36



16K x 18



8K x 18 BIFIFO



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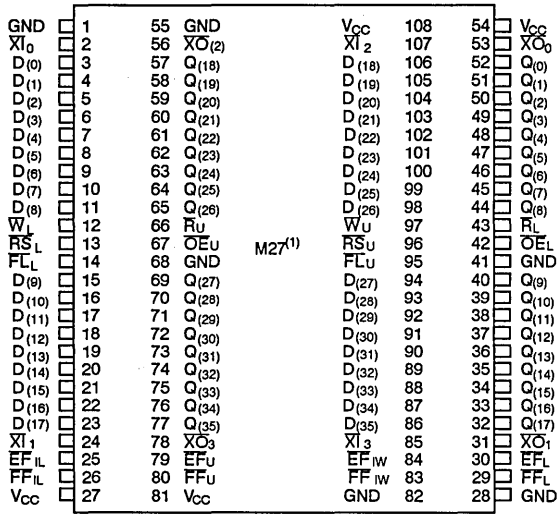
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M27 in the packaging section.

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	X	0	Location Zero	Location Zero	0	1
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X

NOTE:

1. Pointer will increment if flag is high.

TABLE II – RESET AND FIRST LOAD TRUTH TABLE

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device for depth expansion.
   $\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D0-D8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array, $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be high during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	When WRITE is low, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{FF}$ must be high. When the FIFO is full ($\overline{FF}$-low), the internal WRITE operation is blocked.
$\overline{R}$	READ	I	When READ is low, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{EF}$ must be high. When FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked and Q0-Q8 are in a high impedance condition.
$\overline{FL}$	First Load	I	In the depth expansion configuration, $\overline{FL}$-low indicates the first activated device.
XI	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three-state buffers inhibit data flow.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{XO}$	Expansion Out	O	In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q0 - Q8	Outputs	O	Data outputs for 9-bit wide data.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} (1)	Input High Voltage Commercial	2.0	–	–	V
V_{IL} (1)	Input Low Voltage Commercial	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	COMMERCIAL MIN.	COMMERCIAL TYP.	COMMERCIAL MAX.	UNIT
I_{IL} (1)	Input Leakage Current (Any Input)	-5	–	5	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	–	–	0.4	V
I_{CC1} (3)	Average V_{CC} Power Supply Current	–	600	960	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	64	96	mA
I_{CC3} (3)	Power Down Current (All Input = V_{CC} = -0.2V)	–	–	64	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $R \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS [1]

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7MB2001S40		7MB2001S50		7MB2001S60		7MB2001S70		7MB2001S85		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	50	–	65	–	75	–	85	–	105	–	ns
t_A	Address Access Time	–	40	–	50	–	60	–	70	–	85	ns
t_{RR}	Read Recovery Time	10	–	15	–	15	–	15	–	20	–	ns
t_{RPW}[2]	Read Pulse Width	40	–	50	–	60	–	70	–	85	–	ns
t_{OE}	Output Enable to O/P Valid	–	20	–	25	–	30	–	30	–	30	ns
t_{OLZ}[3]	Output Enable to O/P in Low Z	0	–	0	–	0	–	0	–	0	–	ns
t_{OHZ}[3]	Output Disable to O/P in High Z	–	20	–	25	–	30	–	30	–	30	ns
t_{WC}	Write Cycle Time	50	–	65	–	75	–	85	–	105	–	ns
t_{WPW}[2]	Write Pulse Width	40	–	50	–	60	–	70	–	85	–	ns
t_{WR}	Write Recovery Time	10	–	15	–	15	–	15	–	20	–	ns
t_{DS}	Data Set-up Time	20	–	30	–	30	–	30	–	40	–	ns
t_{DH}	Data Hold Time	0	–	5	–	5	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	50	–	65	–	75	–	85	–	105	–	ns
t_{RS}[2]	Reset Pulse Width	40	–	50	–	60	–	70	–	85	–	ns
t_{RSR}	Reset Recovery Time	10	–	15	–	15	–	15	–	20	–	ns
t_{RSF}	Reset to Empty Flag Low, Full Flag High	–	50	–	65	–	75	–	85	–	105	ns
t_{REF}	Read Low to Empty Flag Low	–	40	–	50	–	60	–	70	–	85	ns
t_{RFF}	Read High to Full Flag High	–	40	–	50	–	60	–	70	–	85	ns
t_{WEF}	Write High to Empty Flag High	–	40	–	50	–	60	–	70	–	85	ns
t_{WFF}	Write Low to Full Flag Low	–	40	–	50	–	60	–	70	–	85	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

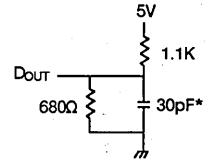

Figure 1. Output Load

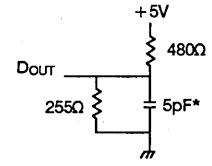

Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

*Includes jig and scope capacitances.

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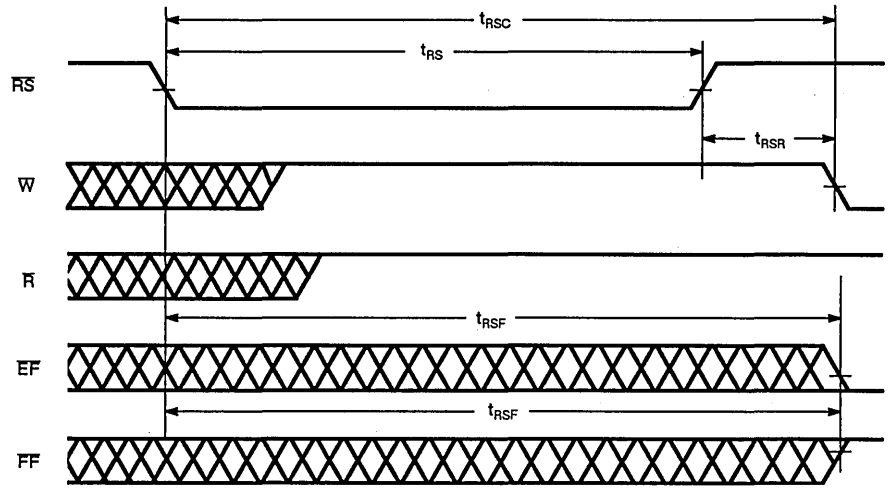

NOTES:
1. $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 3. Reset

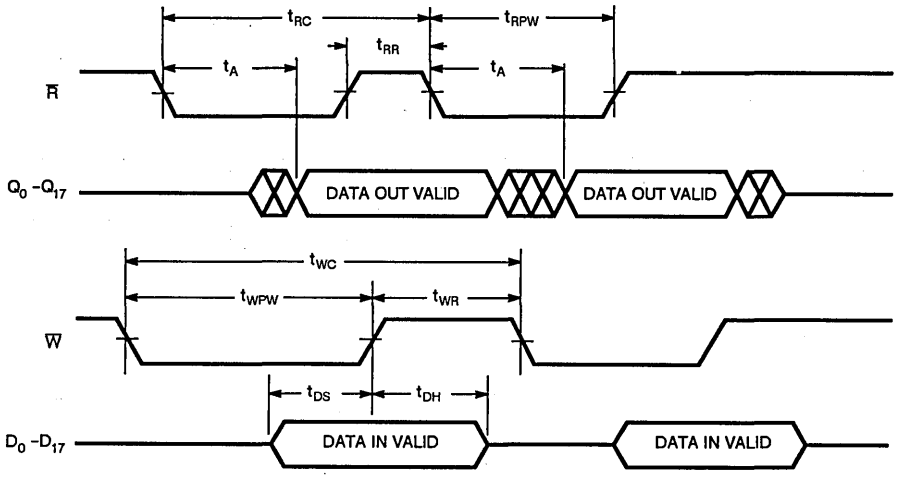

Figure 4. Asynchronous Write and Read Operation

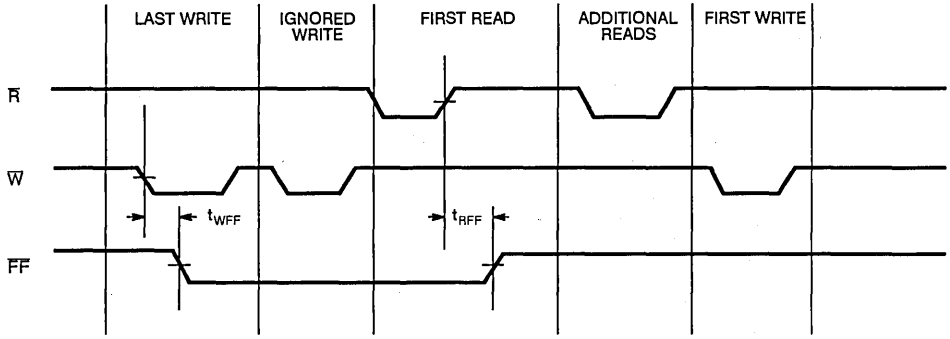

Figure 5. Full Flag From Last Write to First Read

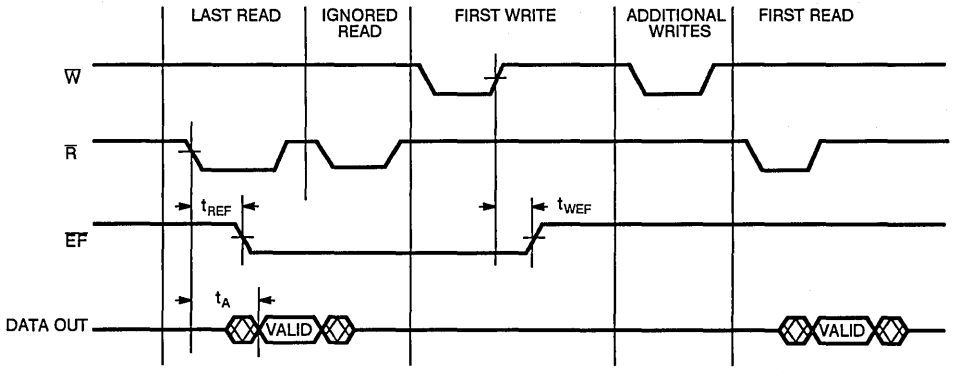

Figure 6. Empty Flag From Last Read to First Write

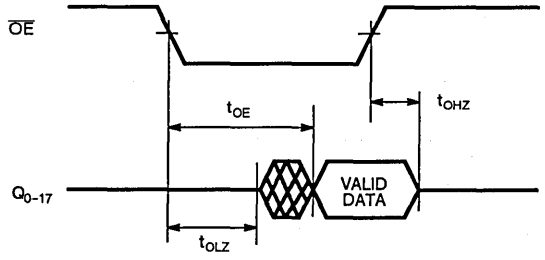

Figure 7. Output Enable Timings

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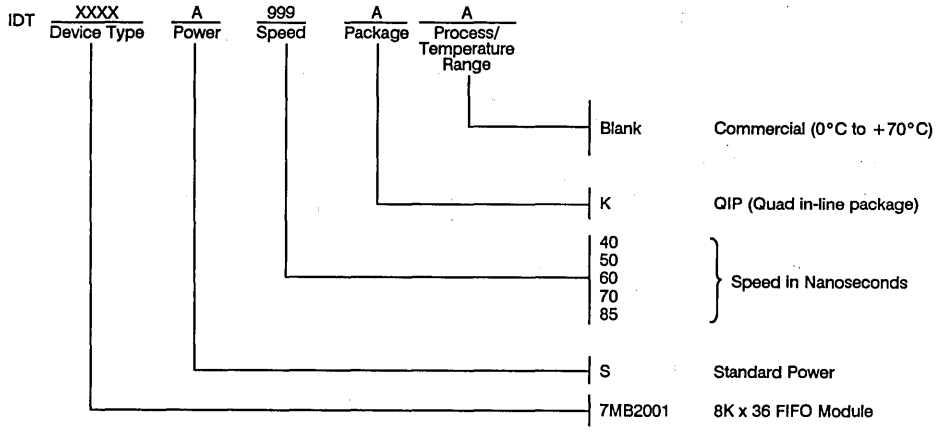
ORDERING INFORMATION



Integrated Device Technology, Inc.

36 TO 9 BIFIFO

IDT 7MB2002

FEATURES:

- First-in/First-out memory module
- Asynchronous and simultaneous read and write
- 36-bit data bus on one side; 9-bit data bus on other side
- All logic required for conversion between 36 and 9-bit buses included on board
- 4K x 36-bit to 16K x 9-bit deep
- Selectable LSB or MSB first on 9-bit side
- Bidirectional
- Latching transceiver for LS 8 bits between the two buses
- Total cycle time 45ns

DESCRIPTION:

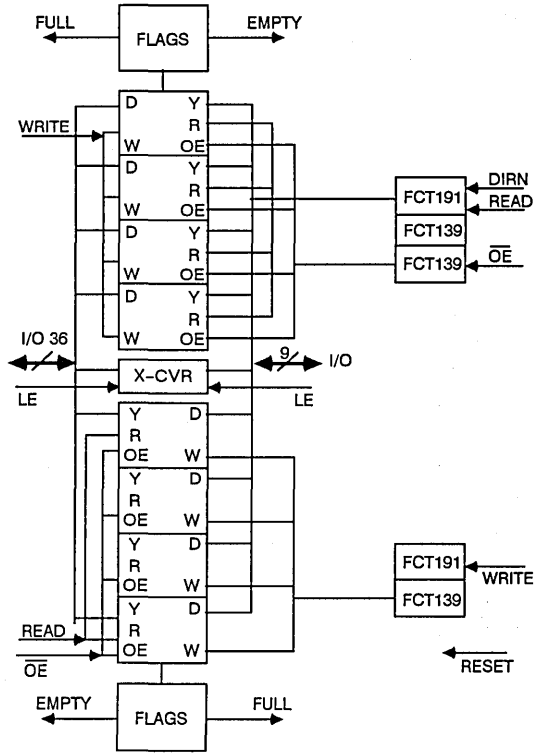
This module is a FIFO that has up to 8 IDT72041s (4K x 9) on board. The module is bidirectional with 4K x 36 transforming to 16K x 9 on one side and back to 4K x 36 on the other side. All logic necessary to control the conversion between 36 and 9 bits is included on the module.

On the 9-bit side, there is a DIRN pin which determines whether the 36 bits of data is presented to the 9-bit side's most significant byte first or least significant byte first and, conversely, whether the 9-bit side data is being entered MSB or LSB first.

Included on-board is an 8-bit transceiver with separate latch enables for each side to allow the passing of status between the buses.

The module is packaged on a 92 pin FR-4 substrate occupying less than 4 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION

GND	1	37	GND	V_{CC}	72	36	V_{CC}
I/OL_0	2	38	$\overline{OELR}$	$\overline{OERL}$	71	35	I/OR_8
I/OL_1	3	39	$\overline{LELR}$	$\overline{LERL}$	70	34	I/OR_7
I/OL_2	4	40	I/OL_3	I/OR_5	69	33	I/OR_6
I/OL_4	5	41	I/OL_5	I/OR_3	68	32	I/OR_4
I/OL_6	6	42	I/OL_7	GND	67	31	I/OR_2
I/OL_8	7	43	I/OL_9	I/OR_0	66	30	I/OR_1
I/OL_{10}	8	44	I/OL_{11}	I/OL_{35}	65	29	RESET
$\overline{FULL}_L$	9	45	$\overline{FULL}_R$ M25(1)	I/OL_{33}	64	28	I/OL_{34}
$\overline{EMPTY}_L$	10	46	$\overline{EMPTY}_R$	I/OL_{31}	63	27	I/OL_{32}
$\overline{WRITE}_L$	11	47	DIRN	I/OL_{30}	62	26	$\overline{WRITE}_R$
$\overline{READ}_L$	12	48	GND	GND	61	25	$\overline{READ}_R$
$\overline{OE}_L$	13	49	I/OL_{12}	I/OL_{29}	60	24	$\overline{OE}_R$
I/OL_{13}	14	50	I/OL_{14}	I/OL_{27}	59	23	I/OL_{28}
I/OL_{15}	15	51	I/OL_{16}	I/OL_{25}	58	22	I/OL_{26}
I/OL_{17}	16	52	I/OL_{18}	I/OL_{23}	57	21	I/OL_{24}
I/OL_{19}	17	53	I/OL_{20}	I/OL_{21}	56	20	I/OL_{22}
V_{CC}	18	54	V_{CC}	GND	55	19	GND

NOTE:

1. For module dimensions, please refer to module drawing M25 in the packaging section.

PIN DESCRIPTIONS

SIGNAL NAME	DESCRIPTION
V_{CC}	Power
GND	Ground
I/OL	36 bit I/O bus
I/OR	9 bit I/O bus
FULL	FIFO Full Flag
EMPTY	FIFO Empty Flag
WRITE	Write Enable
READ	Read Enable
$\overline{OE}$	Output Enable
OELR	Transceiver Output Enable (L - R)
OERL	Transceiver Output Enable (R - L)
LELR	Transceiver Latch Enable (L - R)
LERL	Transceiver Latch Enable (R - L)
DIRN	LSB/MSB Selection on 9 bit side
RESET	System Reset

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to 7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	50V ±10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Commercial Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} (1)	Input High Voltage Commercial	2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
$I_{L1\ LEFT}$	Leakage Current Left		-10	10	µA
$I_{L1\ RIGHT}$	Leakage Current Right		-40	40	µA
I_{CC1}	Ave. V_{CC} Supply Current		–	680(1)	mA
I_{CC2}	Ave. Standby Current		–	130	mA
I_{CC3}	Power Down Current		–	90	mA
V_{OH}	Output High Voltage	I_{OH} = -2mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = -8mA	–	0.4	V

NOTE:
1. I_{CC1} = 780mA at 45ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	pF

NOTE:
1. This parameter is sampled and not 100% tested.

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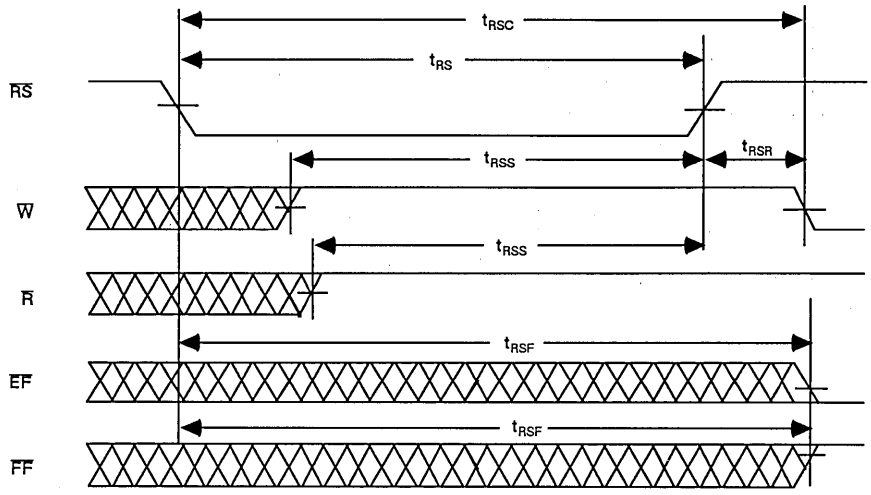
AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7MB2002S45		7MB2002S60		7MB2002S75		7MB2002S90		7MB2002S130		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
f_s	Frequency Shift	–	18	–	13	–	11	–	9	–	7	MHz
t_{RC}	Read Cycle Time	55	–	75	–	90	–	110	–	150	–	ns
t_A	Access Time	–	45	–	60	–	75	–	90	–	130	ns
t_{RR}	Read Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width	45	–	60	–	75	–	90	–	130	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	ns
t_{REF}	Read Low to Empty Flag Low	–	45	–	60	–	75	–	75	–	75	ns
t_{RFF}	Read High to Full Flag High	–	45	–	60	–	75	–	75	–	75	ns
t_{RLZ}	Read Low to Data Low Z	5	–	10	–	10	–	10	–	10	–	ns
t_{RHZ}	Read High to Data High Z	–	30	–	40	–	40	–	40	–	40	ns
WRITE TIMING												
t_{WC}	Write Cycle Time	55	–	75	–	90	–	110	–	150	–	ns
t_{WPW}	Write Pulse Width	45	–	60	–	75	–	90	–	130	–	ns
t_{WR}	Write Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	20	–	32	–	32	–	42	–	42	–	ns
t_{DH}	Data Hold Time	0	–	5	–	10	–	10	–	10	–	ns
t_{WEF}	Write High to Empty Flag High	–	45	–	60	–	75	–	75	–	75	ns
t_{WFF}	Write Low to Fall Flag Low	–	45	–	60	–	75	–	75	–	75	ns
RESET TIMING												
t_{RSC}	Reset Cycle Time	50	–	70	–	85	–	105	–	145	–	ns
t_{RS}	Reset Pulse Width	40	–	55	–	70	–	85	–	125	–	ns
t_{RSS}	Reset Set-up Time	40	–	55	–	70	–	85	–	125	–	ns
t_{RSR}	Reset Recovery Time	10	–	15	–	15	–	20	–	20	–	ns
t_{OHZ}	$\overline{OE}$ High to Data High Z	–	23	–	31	–	40	–	40	–	40	ns
t_{OLZ}	$\overline{OE}$ Low to Data Low Z	–	23	–	31	–	40	–	40	–	40	ns
t_{OE}	$\overline{OE}$ Low to Valid Data	–	26	–	36	–	50	–	50	–	50	ns
t_{RSF}	Reset Empty/Full Flag	–	55	–	75	–	90	–	110	–	150	ns



NOTES:
1. $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_H around the rising edge of $\overline{RS}$.

Figure 1. Reset

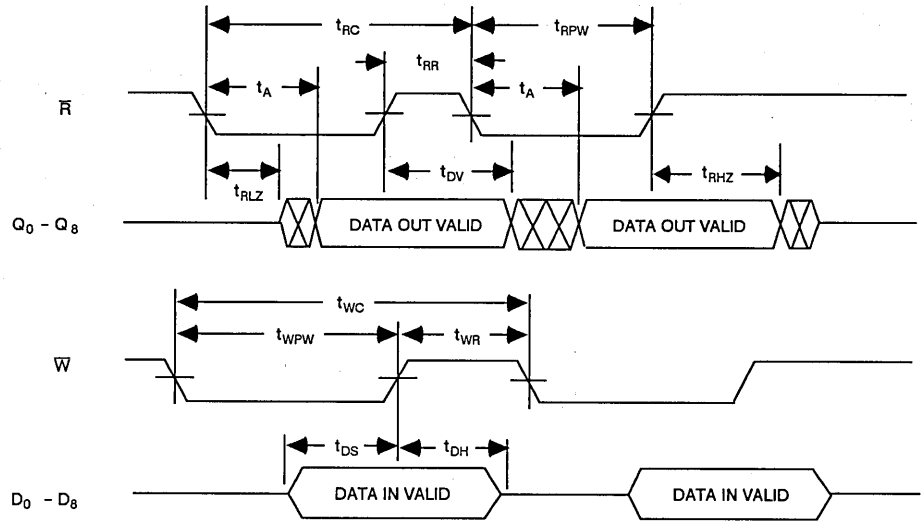


Figure 2. Asynchronous Write and Read Operation

13

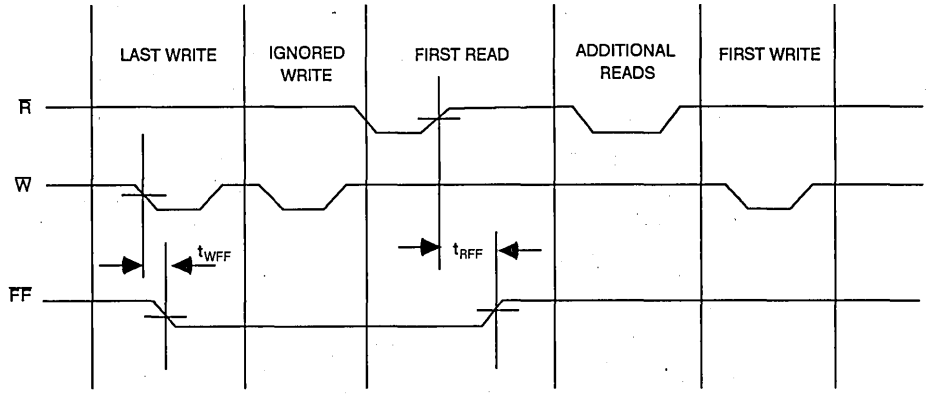


Figure 3. Full Flag from Last Write to First Read

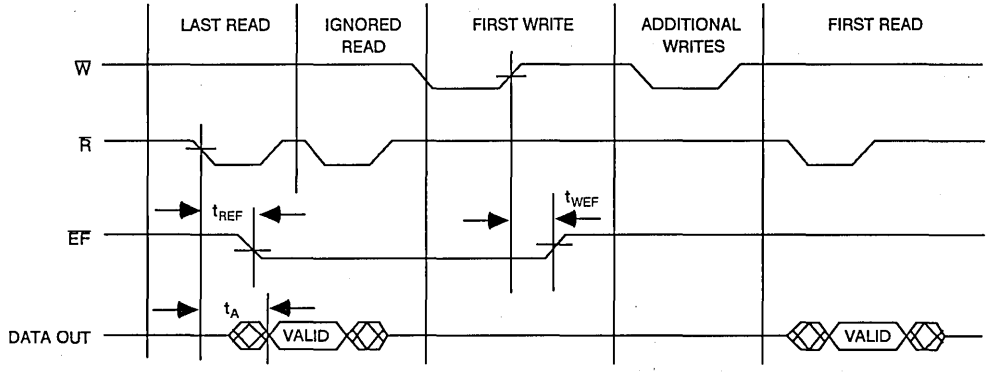


Figure 4. Empty Flag from Last Read to First Write

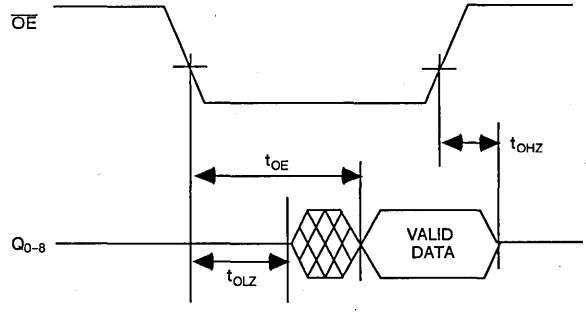


Figure 5. Output Enable Timing

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

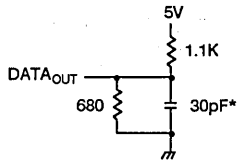


Figure 1. Output Load

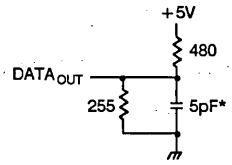
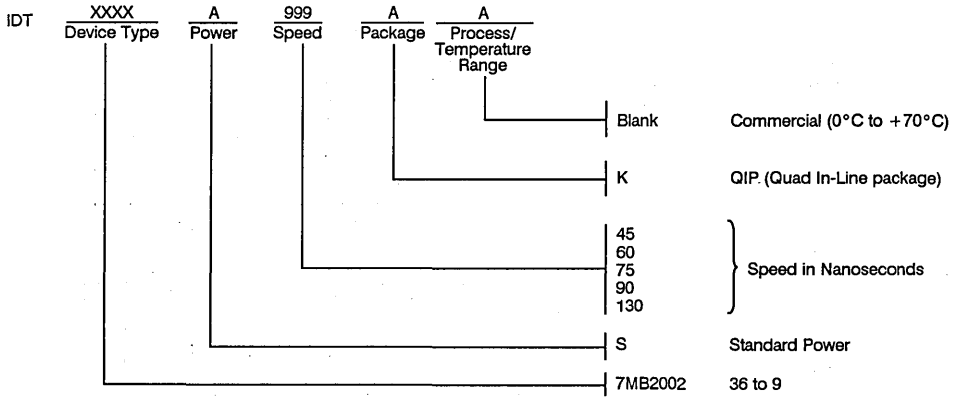


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

* Includes jig and scope capacitances.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

2 (16K x 16) CMOS STATIC RAM FR-4 DIP MODULE

IDT 7MB4009

FEATURES:

- High Density 512K 2(16K x 16) Static RAM Module
- Cost effective surface mount components mounted on an epoxy laminate (FR-4) substrate
- Packaged in a 44 pin 600 mil wide DIP
- 20ns access time
- Common data and address pins for both banks of RAM resulting in increased density
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL compatible

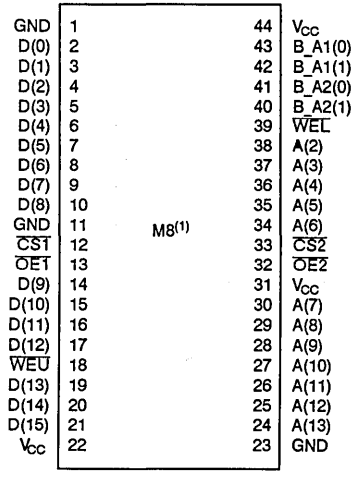
DESCRIPTION:

The IDT7MB4009 is a 512K 2(16K x 16) high-speed static RAM module constructed on an epoxy laminate surface using 8 IDT7198 16K x 4 static RAMs packaged in surface mount packages. Extremely fast speeds can be obtained by using RAMs fabricated in IDT's high performance, high reliability CEMOS™ technology.

The IDT7MB4009 is organized as 2 separate banks of 16K x 16 RAM with common address and data pins to minimize the module size. The IDT7MB4009 is packaged in a 44pin 600 mil wide DIP, packing 512K of fast memory in 1.8 square inches.

The IDT7MB4009 is available with access time as fast as 20ns, with maximum power consumption of 4.2W.

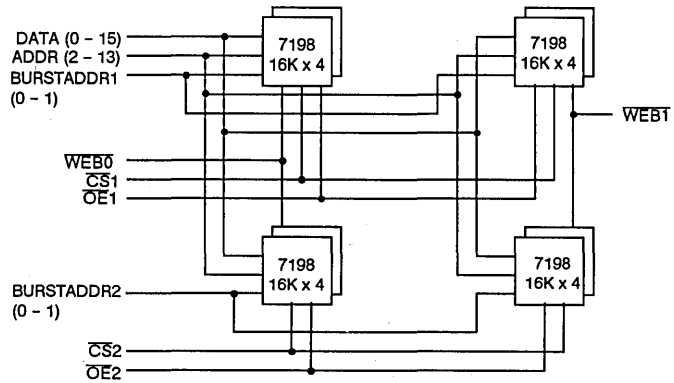
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M8 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A (2-13)	Addresses
BA1 (0-1)	Burst address, Bank 1
BA2 (0-1)	Burst address, Bank 2
D (0-15)	Data Inputs/Outputs
$\overline{WEU}$	Write Enable, Upper
$\overline{WEL}$	Write Enable, Lower
$\overline{CS}$1, 2	Chip Select
$\overline{OE}$1, 2	Output Enable
GND	Ground
V_{CC}	Power Supply

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL MAX.	UNIT
I_L	Input Leakage Current (Address & Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	40	µA
I_{LI}	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	10	µA
I_{LO}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OL} = -4mA	2.4	–	V
I_{CC1}	Operating Current	F = O, $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	–	620	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	–	760	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IH}	–	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	–	120	mA

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7MB4009S20P MIN.	7MB4009S20P MAX.	7MB4009S25P MIN.	7MB4009S25P MAX.	7MB4009S35P MIN.	7MB4009S35P MAX.	7MB4009S45P MIN.	7MB4009S45P MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	20	–	25	–	–	–	–	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	–	–	–	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	–	–	–	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	15	–	20	–	25	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	10	–	12	–	15	–	15	ns
t_{OHZ} (1)	Output Disable to Output in High Z	–	10	–	15	–	15	–	15	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	20	–	25	–	35	–	45	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	18	–	20	–	30	–	40	–	ns
t_{CW}	Chip Select to End of Write	18	–	20	–	30	–	40	–	ns
t_{AW}	Address Valid to End of Write	18	–	21	–	32	–	42	–	ns
t_{AS}	Address Set Up Time	0	–	1	–	2	–	2	–	ns
t_{WP}	Write Pulse Width	17	–	20	–	25	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z	–	7	–	8	–	10	–	15	ns
t_{DW}	Data to Write Time Overlap	–	10	14	–	16	–	20	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

NOTE:

1. This parameter guaranteed, but not tested

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

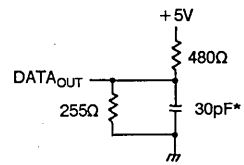


Figure 1. Output Load

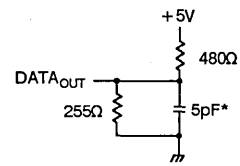
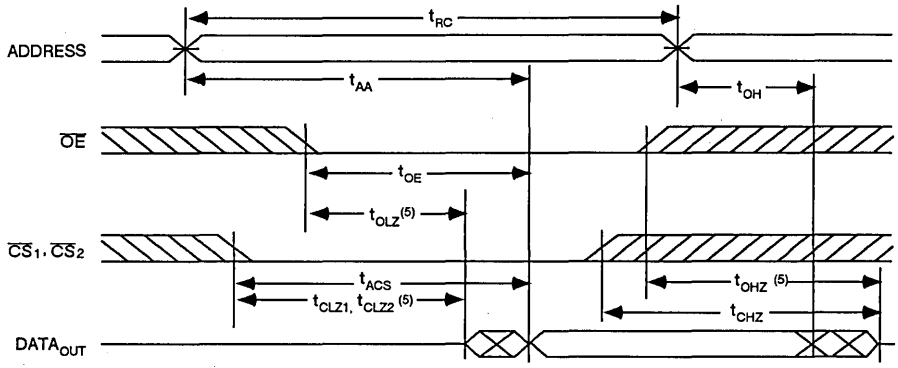


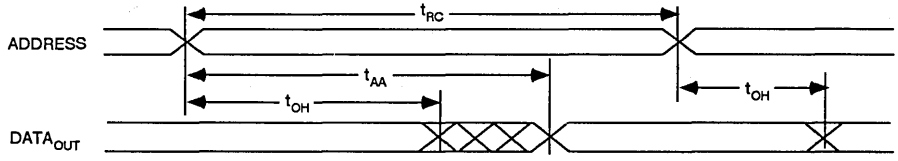
Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

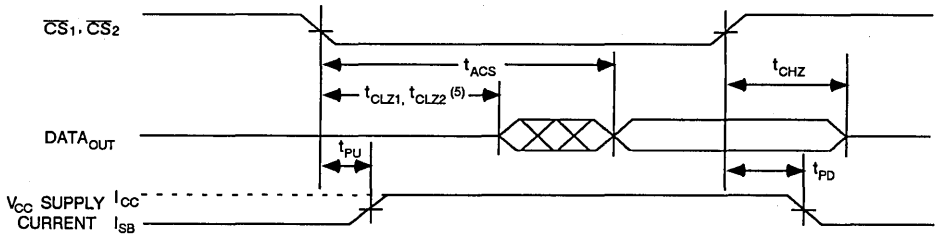
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

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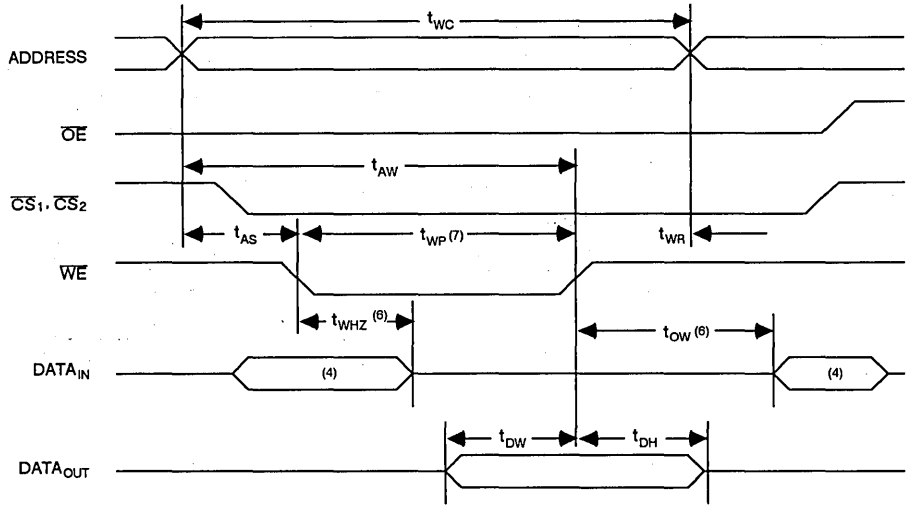
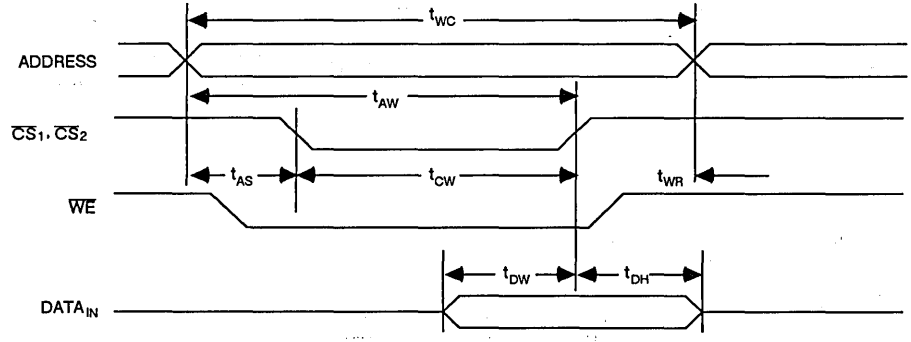
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5, 8]



NOTES:

1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a low $\overline{CS_2}$, and a low $\overline{WE}$.
3. t_{WP} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a WE controlled write cycle, the write pulse width must be the greater of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE} = V_{IH}$.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

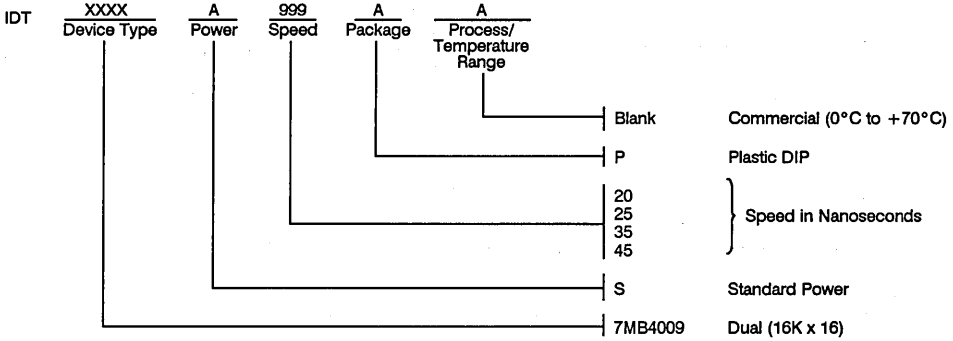
SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$C_{IN\ ADDR}$	Input Capacitance	V_{IN} = 0V	–	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTES:
1. This parameter is measured at characterization but not tested.
2 $C_{IN\ DATA}$ = 20pF.

TRUTH TABLE

MODE	$\overline{CST}$	$\overline{CS2}$	$\overline{OE1}$	$\overline{OE2}$	$\overline{UEB0}$	$\overline{UEB1}$	OUTPUT	POWER
Standby	H	H	X	X	X	X	High Z	Standby
Read	L	H	L	X	H	H	D_{OUT} BA (1)	Active
Read	L	H	H	X	H	H	High Z	Active
Read	H	L	X	L	H	H	D_{OUT} BA (2)	Active
Read	H	L	X	H	H	H	High Z	Active
Write	L	H	X	X	L	H	D_{IN} BA (1) D (0-7)	Active
Write	L	H	X	X	H	L	D_{IN} BA (1) D (8-15)	Active
Write	H	L	X	X	L	H	D_{IN} BA (2) D (0-7)	Active
Write	H	L	X	X	H	L	D_{IN} BA (2) D (8-15)	Active
Write	L	H	X	X	L	L	D_{IN} BA (1) D (0-15)	Active
Write	H	L	X	X	L	L	D_{IN} BA (2) D (0-15)	Active

ORDERING INFORMATION



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Integrated Device Technology, Inc.

128K x 16 SHARED PORT RAM

PRELIMINARY
IDT 7MB6036

FEATURES:

- Fully asynchronous operation from either port
- Versatile control for write: separate write control for lower and upper byte for each port
- On-board port arbitration and multiplexing logic by custom FCT chip set
- Master/Slave control for expanding width
- $\overline{BUSY}$ output flag

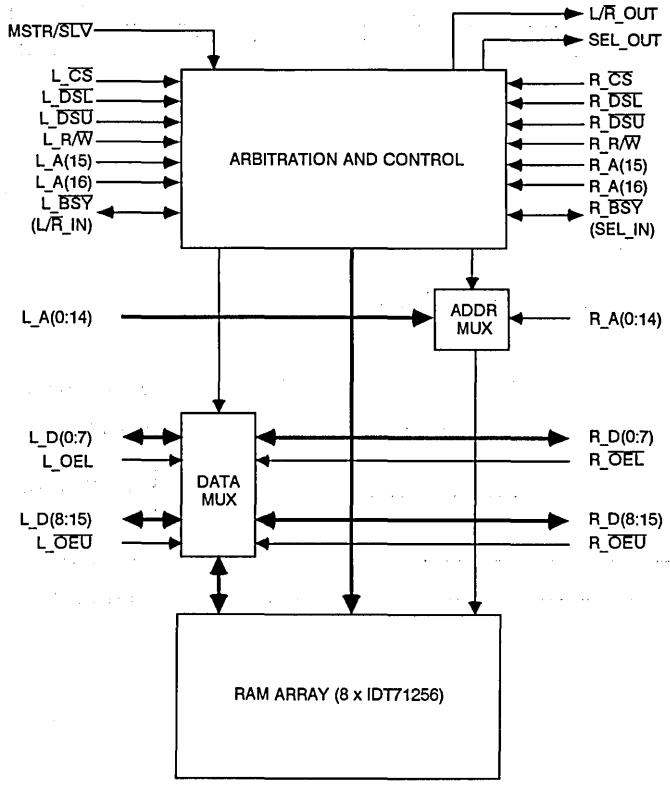
DESCRIPTION:

The Shared Port RAM provides two ports with separate control, address and Data I/O pins that permit independent access for reads or writes to any location in the 128 K x 16 memory array. The Master/Slave input allows the module to be used as a master with one or more slaves.

ARBITRATION:

In the Master Mode, the Shared Port RAM arbitrates asynchronously between the left and right ports on the leading edge of the left and right $\overline{CS}$ inputs. The first to arrive is granted exclusive access to the RAM array for as long as its $\overline{CS}$ is asserted. If both ports attempt simultaneous access, the losing port will have its $\overline{BUSY}$ asserted until the winning port completes it access, at which time the second port will be granted access to the RAM array.

FUNCTIONAL BLOCK DIAGRAM



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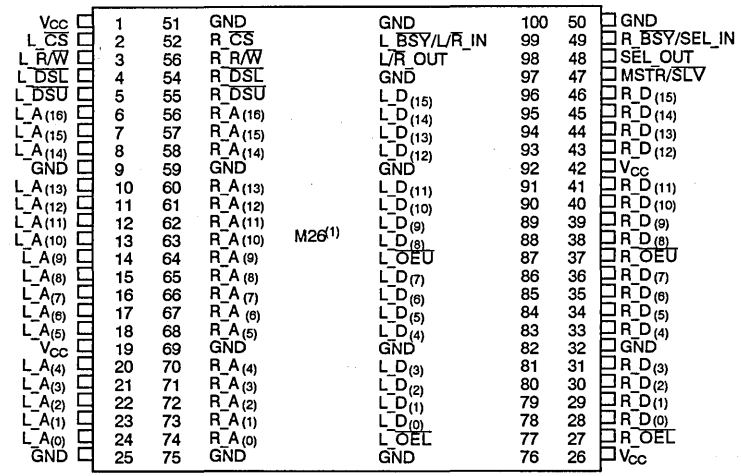
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M26 in the packaging section.

PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
Vcc	Power
GND	Ground
L_A(0:16)	Left Port Address
L_D(0:15)	Left Port Data
R_A(0:16)	Right Port Address
R_D(0:15)	Right Port Data
R/$\overline{W}$	Read/Write Control
$\overline{CS}$	Active low Chip Select
$\overline{DSL}$	Data Strobe for lower byte
$\overline{DSU}$	Data Strobe for upper byte
$\overline{OEL}$	Output Enable for lower byte
$\overline{OEU}$	Output Enable for upper byte
L_$\overline{BSY}$/L/$\overline{R}$_IN	Left Busy Output (Master)/Left and Right Port Select In (Slave)
R_$\overline{BSY}$/SEL_IN	Right Busy Output (Master)/RAM Select In (Slave)
L/$\overline{R}$_OUT	Left and Right Port Select Out (Master)
SEL_OUT	RAM Select Out (Master)
MSTR/$\overline{SLV}$	Master/Slave signal for cascading master w/one or more slaves

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AC ELECTRICAL CHARACTERISTICS

Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MB6036S70		IDT7MB6036S85		IDT7MB6036S100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
NO CONTENTION READ								
t_{RC}	Read Cycle Time	70		85		100		ns
t_{AA}	Address Access Time		70		85		100	ns
t_{ACS}	Chip Select Access Time		70		85		100	ns
t_{OE}	Output Enable To Data Valid		15		15		15	ns
t_{OH}	O/P Hold From Address Change	5		5		5		ns
t_{OLZ}	O/P to Low-z		15		15		15	ns
t_{OHZ}	O/P to Hi-z		15		15		15	ns
NO CONTENTION WRITE								
t_{WC}	Write Cycle Time	70		85		100		ns
t_{AW}	Addr Valid To End Of Write	60		75		90		ns
t_{CW}	$\overline{CS}$ to End Of Write	60		75		90		ns
t_{AS}	Address Set Up Time	0		0		0		ns
t_{CDS}	$\overline{CS}$ to Data Strobe	20		25		25		ns
t_{DS}	Data Strobe Width	35		50		60		ns
t_{WR}	Write Recovery Time	5		5		5		ns
t_{DW}	Data Valid to End of Write	30		45		50		ns
t_{DH}	Data Hold From End of Write	5		10		10		ns
CONTENTION READ								
t_{CB}	$\overline{CS}$ to $\overline{BUSY}$		15		20		20	ns
t_{BD}	$\overline{Busy}$ Negate to Data Valid		70		85		100	ns
CONTENTION WRITE								
t_{CB}	$\overline{CS}$ to Busy		15		20		20	ns
t_{BDS}	$\overline{BUSY}$ Negate to Data Strobe	10		15		15		ns
SLAVE TIMING								
t_{LR}	$\overline{CS}$ to L/$\overline{R}$ Output		15		20		20	ns
t_{SEL}	$\overline{CS}$ to Select Output		15		20		20	ns
t_{APS}	Arbitration Priority Set-up Time	5		5		5		ns

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
I_{LI}	Input Leakage Current	-15	15	µA
I_{LO}	Output Leakage Current	-15	15	µA
I_{CC1}	Operating Power Supply Current		300	mA
I_{CC2}	Dynamic Operating Current		420	mA
I_{SB}	Standby Power Supply Current		150	mA
V_{OH}	Output High Voltage (I_{OH} = 8mA)	2.4		V
V_{OL}	Output Low Voltage (I_{OH} = 16mA)		0.4	V

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.5V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

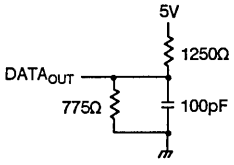

Figure 1. Output Load

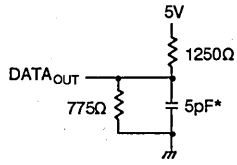

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

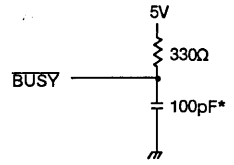

Figure 3. $\overline{BUSY}$ Output Load

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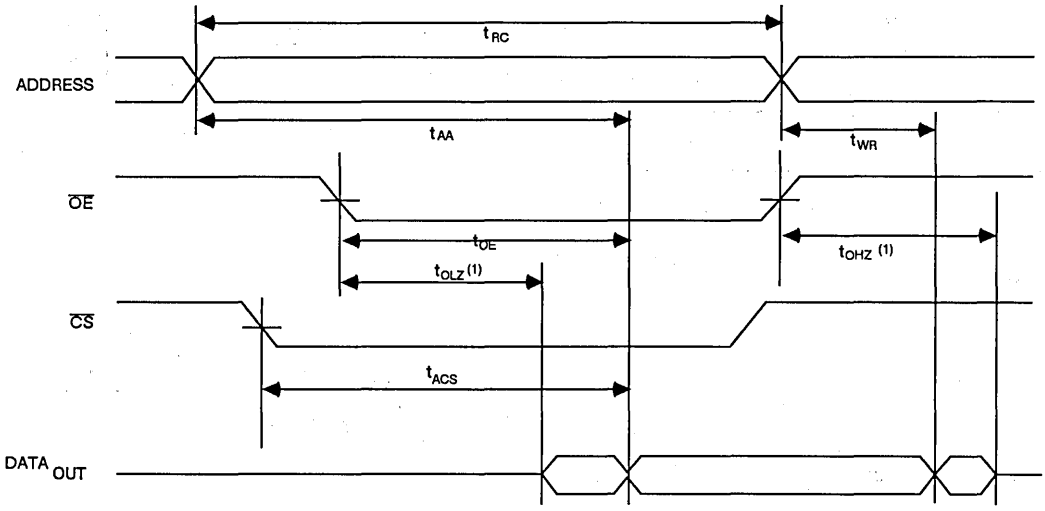
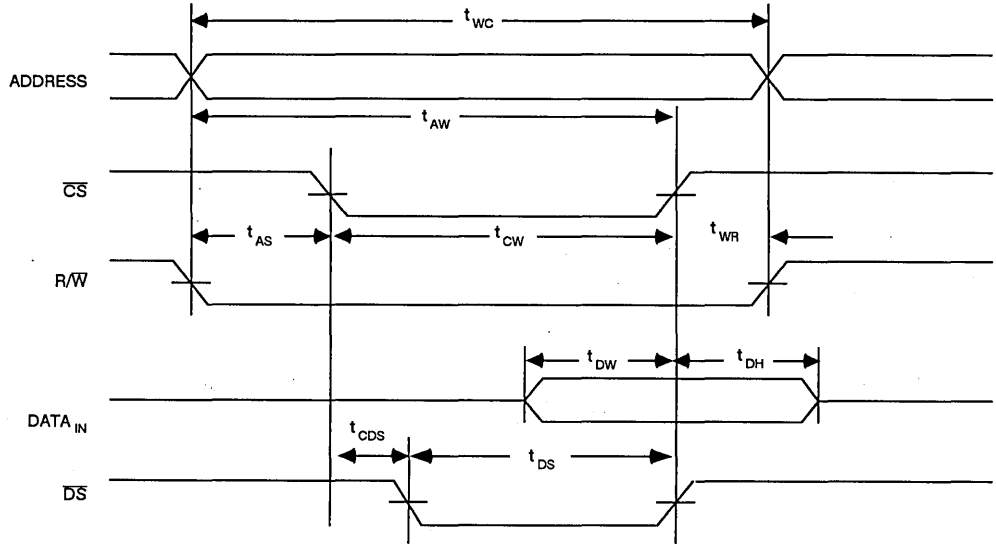
TIMING WAVEFORM OF READ CYCLE



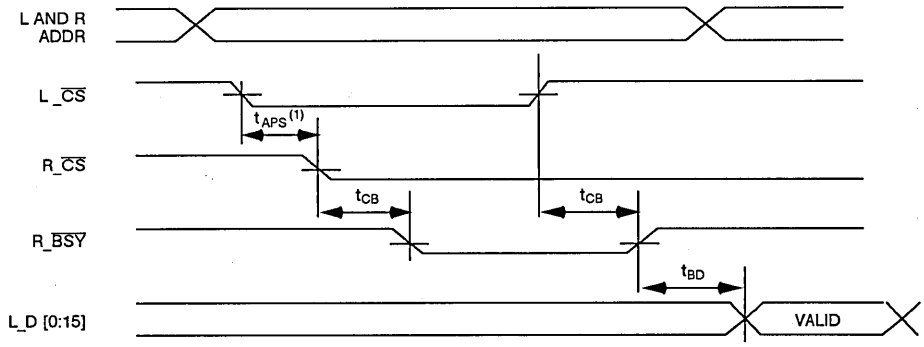
NOTE:
1. Transition is measured ± 200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF CONTENTION READ, $\overline{CS}$ ARBITRATION

L_$\overline{CS}$ VALID FIRST:

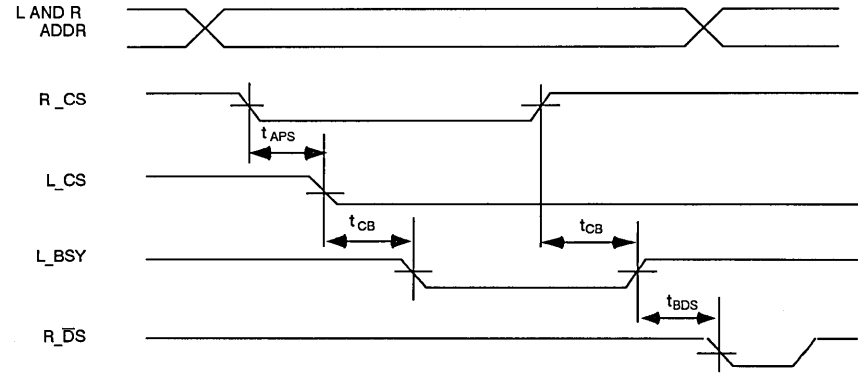


NOTE:

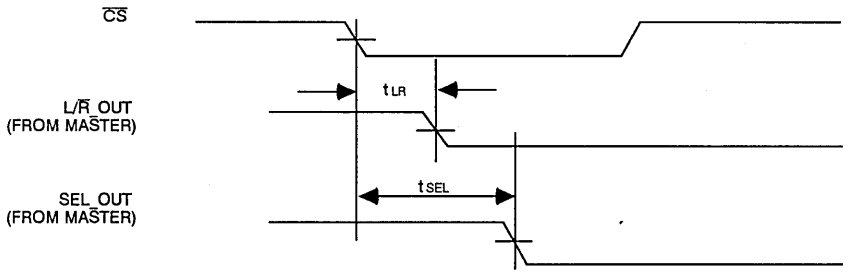
1. t_{APS} is only necessary to guarantee left side access. Within this set-up time, one side or the other will gain access, but neither will have priority.

TIMING WAVEFORM OF CONTENTION WRITE

R_$\overline{CS}$ VALID FIRST:



TIMING WAVEFORM OF SLAVE



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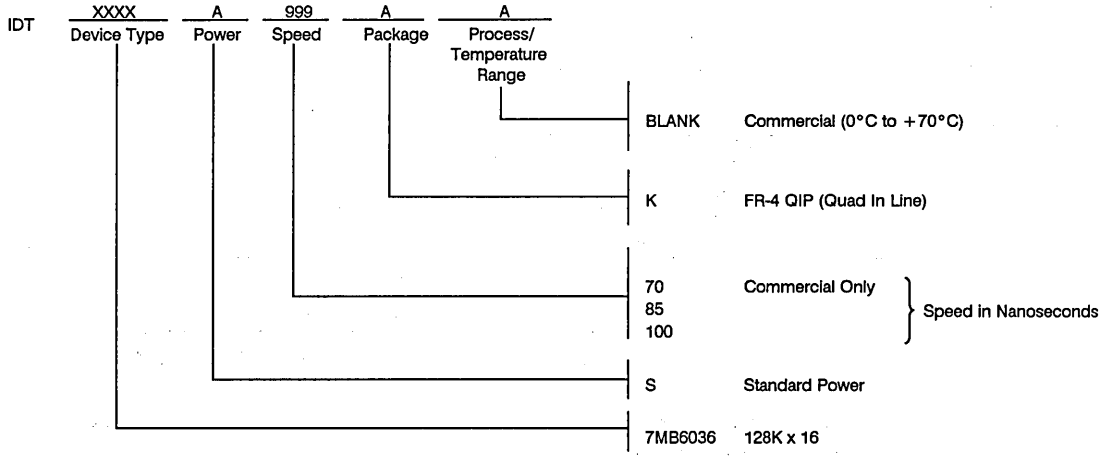
ORDERING INFORMATION



Integrated Device Technology, Inc.

DUAL(16K x 60) DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

IDT 7MB6039

FEATURES:

- High-speed CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache (dual 16K x 60)
- Operating frequencies to support 12 MHz, 16.7MHz, 20MHz and 25MHz CPUs
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL-compatible I/Os
- Single 5V (±10%) power supply

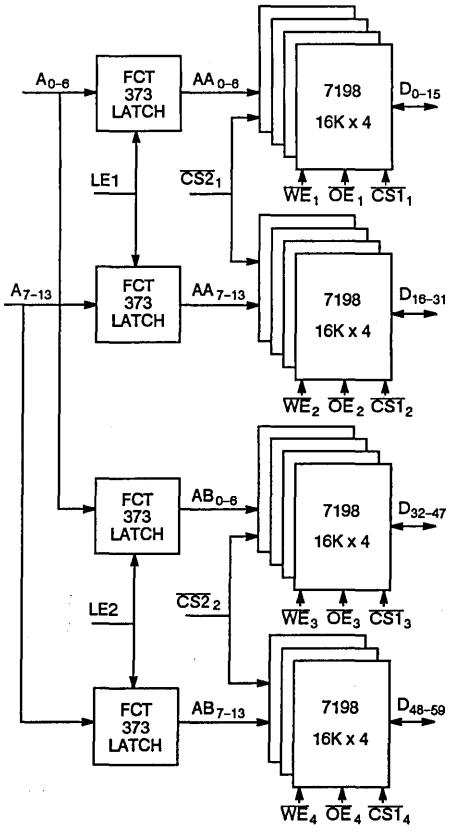
DESCRIPTION:

The IDT7MB6039 is a 240K byte high-speed CMOS static RAM consructed on a multilayer epoxy substrate (FR-4), using 30 IDT7198 (16K x 4) RAMs and 8 IDT74FCT373 latches.

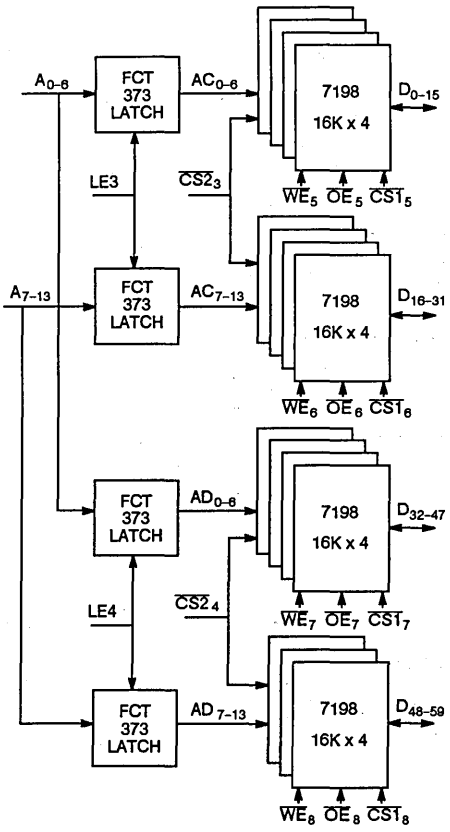
The construction and specifications of this module have been optimized to support its use as a complete 16K deep INSTRUCTION and DATA cache for the IDT79R3000.

The iDT7MB6039 is organized as two seperate banks of 16K X 60, with the IDT74FCT373s being used as ADDRESS latches. The two banks of RAM with thier associated ADDRESS latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Also, each bank has two sets of ADDRESS latches to reduce the capacitance loading on the outputs of the latches and thereby enhance performance.

DATA CACHE



INSTRUCTION CACHE



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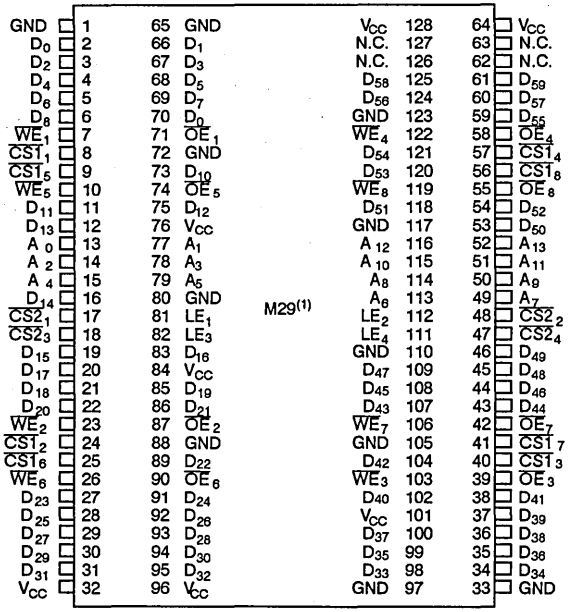
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M29 in the packaging section.

PIN NAMES

D_0 - D_{59}	Data I/Os
A_0 - A_{13}	Address Inputs
LE_1 - LE_4	Latch Enables
$\overline{CS1}_1$ - $\overline{CS1}_8$	RAM Selects
$\overline{CS2}_1$ - $\overline{CS2}_4$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enables
GND	Ground
V_{CC}	Power Supply
N.C.	No Connection

NOTES:

1. All GND pins must be grounded for proper operation.
2. All V_{CC} pins must be connected to +5V for proper operation.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

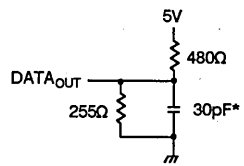


Figure 1. Output Load

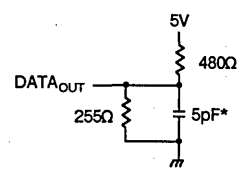


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

* Including scope and jig.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	12 MHz		16.7 MHz		20 MHz		25 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	-20	20	-20	20	-20	20	-20	-20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	10	-10	10	-10	10	-10	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open		3000		3000		3000		3600	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX} Output Open		3750		3750		4050		4500	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V, $V_{IN} > V_{CC}$ -0.2V or < 0.2V		450		450		450		600	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ = V_{IH}	1500			1500		1650		1800	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA		0.4		0.4		0.4		0.4	V

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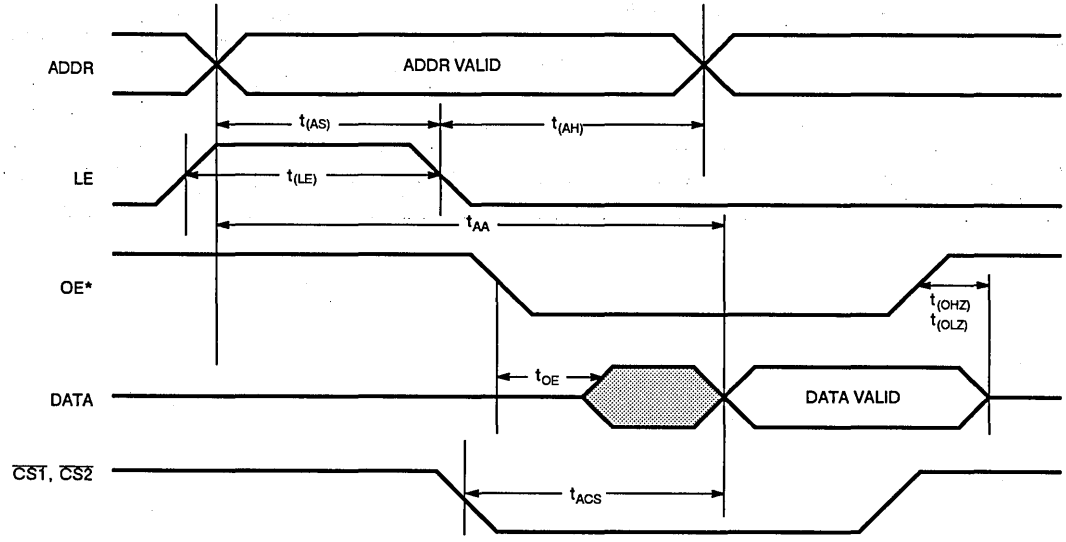
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	12 MHz		16.6 MHz		20 MHz		25 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
t_{LE}	Latch Enable Width	8	–	6	–	6	–	6	–	ns
t_{AS}	Address Setup Time to LE	4	–	2	–	2	–	2	–	ns
t_{AH}	Address Hold Time from LE	3	–	1.5	–	1.5	–	1.5	–	ns
t_{AA}(2)	Address Access Time	–	45	–	35	–	30	–	25	ns
t_{ACS}	Chip Select Time	–	40	–	30	–	25	–	20	ns
t_{OE}	Output Enable Time	–	22	–	17	–	13	–	10	ns
t_{OHZ}(1)	Output Diasable to Output in High Z	2	16	2	14	2	10	2	8	ns
t_{OLZ}(1)	Output Diasable to Output in Low Z	5	–	5	–	5	–	5	–	ns

NOTES:
1. Guaranteed but not tested.
2. LE tested.

TIMING WAVEFORM OF READ CYCLE

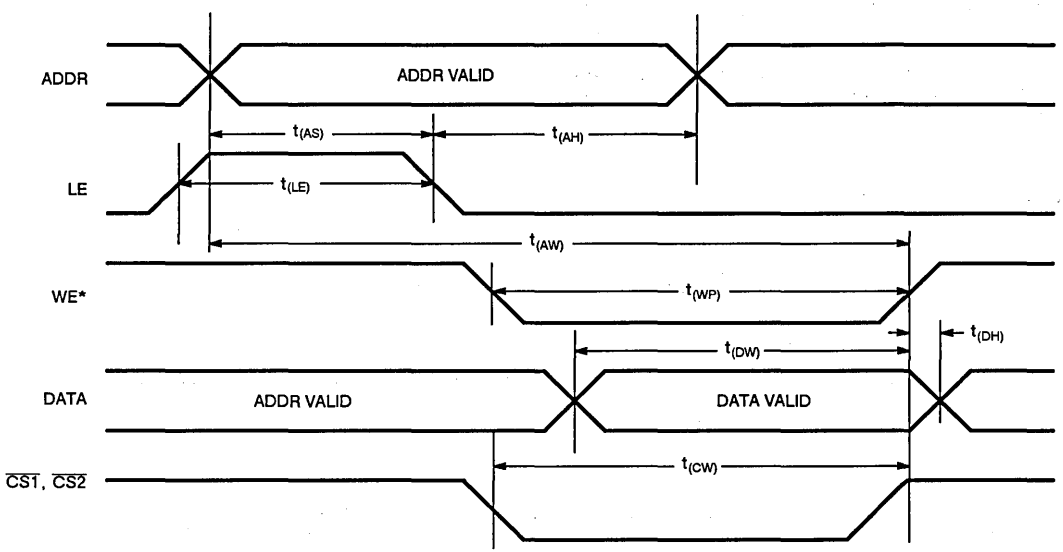


AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	12 MHz		16.6 MHz		20 MHz		25 MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE										
t_{LE}	Latch Enable Width	8	–	6	–	6	–	6	–	ns
t_{AS}	Address Setup Time to LE	4	–	2	–	2	–	2	–	ns
t_{AH}	Address Hold Time from LE	3	–	1.5	–	1.5	–	1.5	–	ns
t_{AW} (2)	Address Valid to End of Write	40	–	30	–	25	–	23	–	ns
t_{CW}	Chip Select to End of Write	35	–	25	–	20	–	18	–	ns
t_{WP}	Write Pulse Width	30	–	25	–	20	–	17	–	ns
t_{DW}	Data Valid to End of Write	20	–	13	–	13	–	11	–	ns
t_{DH}	Data Hold Time	0	7	0	7	0	7	0	7	ns

NOTES:
1. Guaranteed but not tested.
2. LE asserted.

TIMING WAVEFORM OF WRITE CYCLE



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TRUTH TABLE

MODE	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	D_{OUT}	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	18	pF

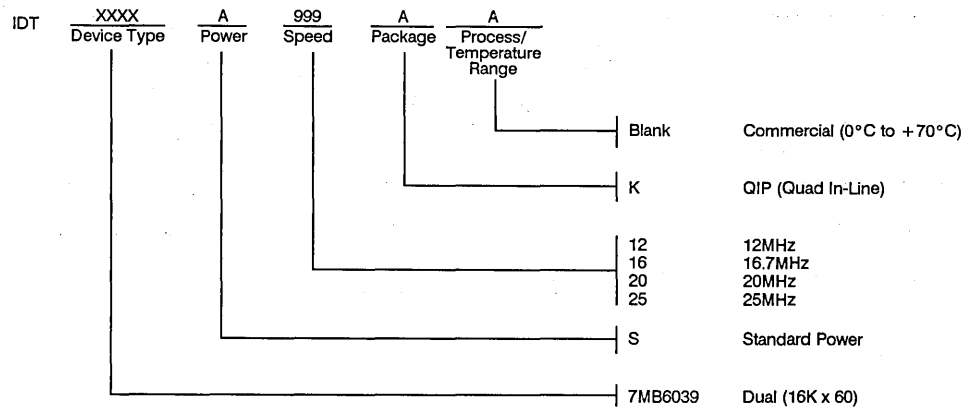
NOTE:
1. This parameter is sampled and not 100% tested.

FULLY ASSEMBLED MODULE SCREENING FLOW[1]

SCREEN	TEST METHOD	LEVEL
Final Electrical Tests		
Static (DC)	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes	100%
Functional	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	IDT Specification	100%

NOTE:
1. Screening of the fully assembled module is performed per the table to assure package integrity and mechanical reliability. Finally, 100% electrical tests are performed.

ORDERING INFORMATION



Integrated Device Technology, Inc.

DUAL(16K x 64) DATA/ INSTRUCTION CACHE MODULE FOR GENERAL CPUs

IDT 7MB6040

FEATURES:

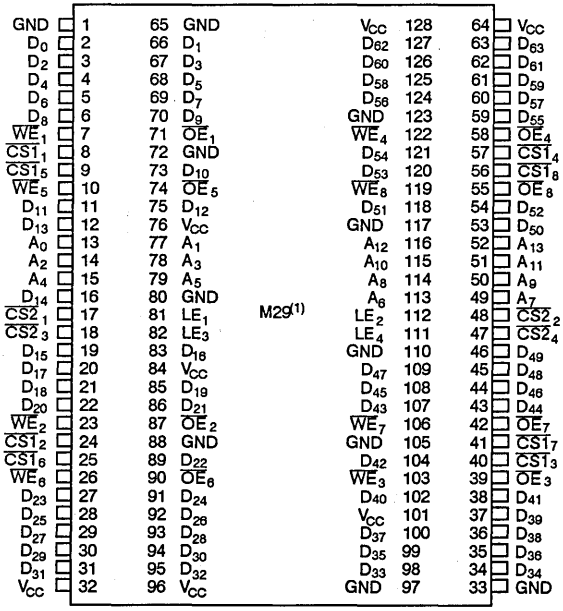
- High-speed CMOS static RAM module constructed to support general purpose CPUs as a complete data and instruction cache (dual 16K x 64)
- Operating frequencies to support 12MHz,16.7MHz, 20MHz and 25MHz
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL-compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

The IDT7MB6040 is a 256K-byte high-speed CMOS static RAM constructed on a multilayer epoxy substrate (FR-4), using 30 IDT7189 (16K x 4) RAMs and 8 IDT74FCT373 latches.

The IDT7MB6040 is organized as two separate banks of 16K x 64 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches and, thereby, enhance performance.

PIN CONFIGURATION



QIP
TOP VIEW

PIN NAMES

$D_0 - D_{63}$	Data I/Os
$A_0 - A_{13}$	Address Inputs
$LE_1 - LE_4$	Latch Enables
$\overline{CS1}_1 - \overline{CS1}_8$	RAM Selects
$\overline{CS2}_1 - \overline{CS2}_4$	RAM Selects
$WE_1 - WE_8$	Write Enables
$OE_1 - OE_8$	Output Enables
GND	Ground
V_{CC}	Power Supply

NOTE:

1. For module dimensions, please refer to module drawing M29 in the packaging section.

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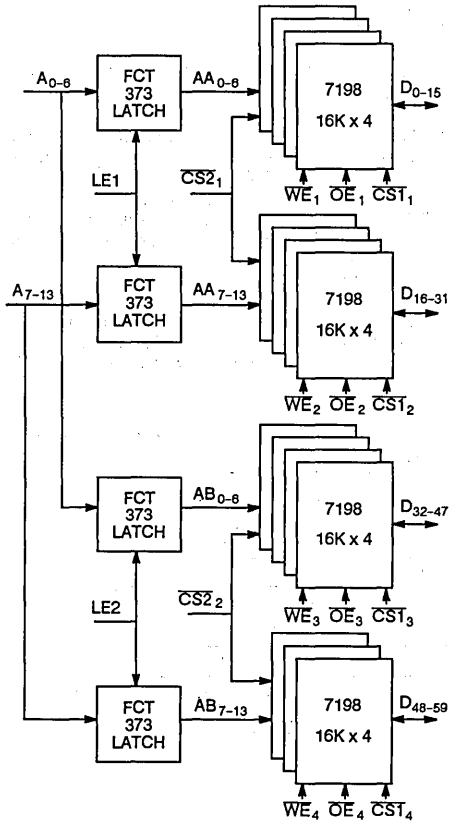
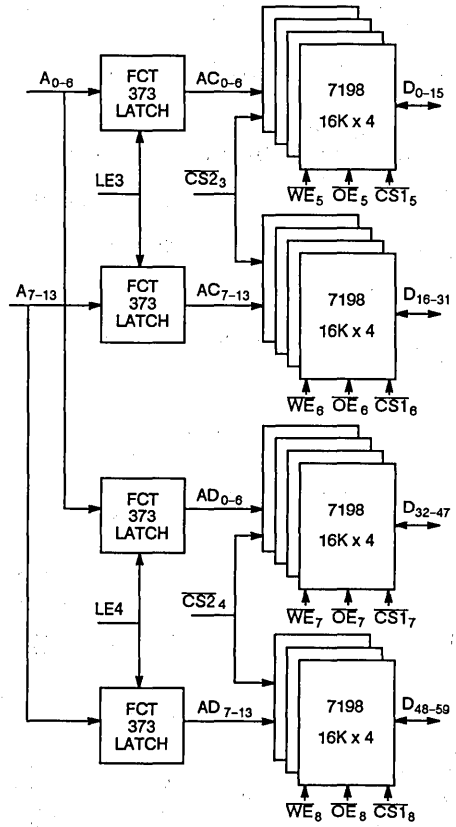
DATA CACHE



INSTRUCTION CACHE



AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

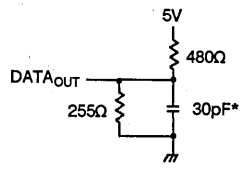


Figure 1. Output Load

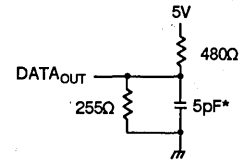


Figure 2. Output Load (for t_{OLZ}, t_{OHZ})

* Including scope and jig.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	12 MHz		16.7 MHz		20 MHz		25 MHz		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	-20	20	-20	20	-20	20	-20	-20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-10	10	-10	10	-10	10	-10	10	µA
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open		3000		3000		3000		3600	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX} Output Open		3750		3750		4050		4500	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V, $V_{IN} > V_{CC}$ -0.2V or < 0.2V		450		450		450		600	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ = V_{IH}	1500			1500		1650		1800	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA		0.4		0.4		0.4		0.4	V

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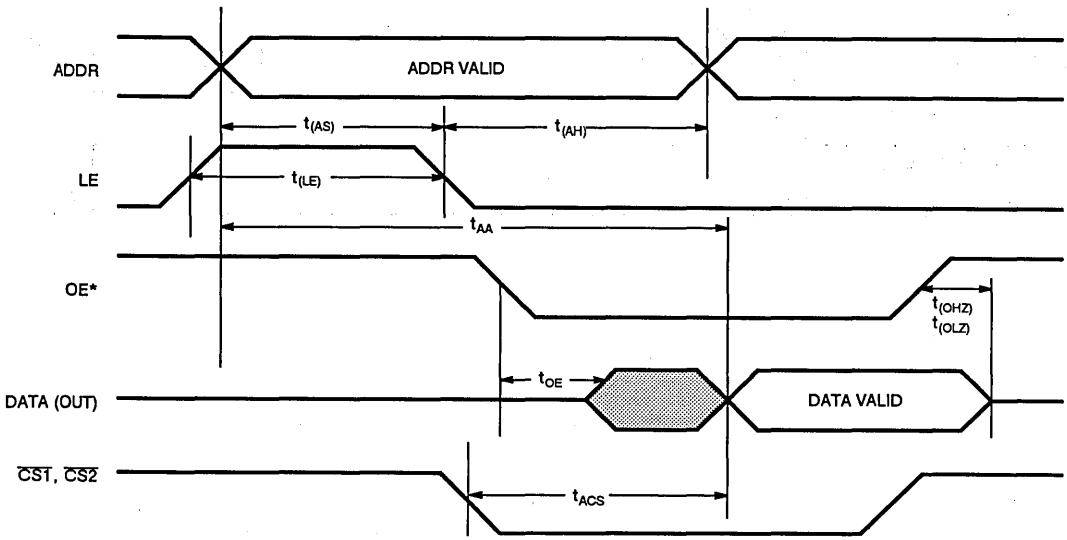
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	12 MHz MIN.	12 MHz MAX.	16.6 MHz MIN.	16.6 MHz MAX.	20 MHz MIN.	20 MHz MAX.	25 MHz MIN.	25 MHz MAX.	UNIT
READ CYCLE										
t_{LE}	Latch Enable Width	8	–	6	–	6	–	6	–	ns
t_{AS}	Address Setup Time to Le	4	–	2	–	2	–	2	–	ns
t_{AH}	Address Hold Time from Le	3	–	1.5	–	1.5	–	1.5	–	ns
t_{AA}(2)	Address Access Time	–	45	–	35	–	30	–	24	ns
t_{ACS}	Chip Select Time	–	40	–	30	–	25	–	20	ns
t_{OE}	Output Enable Time	–	22	–	17	–	13	–	10	ns
t_{OHZ}(1)	Output Diasable to Output in High Z	2	16	2	14	2	10	2	8	ns
t_{OLZ}(1)	Output Diasable to Output in Low Z	5	–	5	–	5	–	5	–	ns

NOTES:
1. Guaranteed but not tested.
2. LE tested.

TIMING WAVEFORM OF READ CYCLE

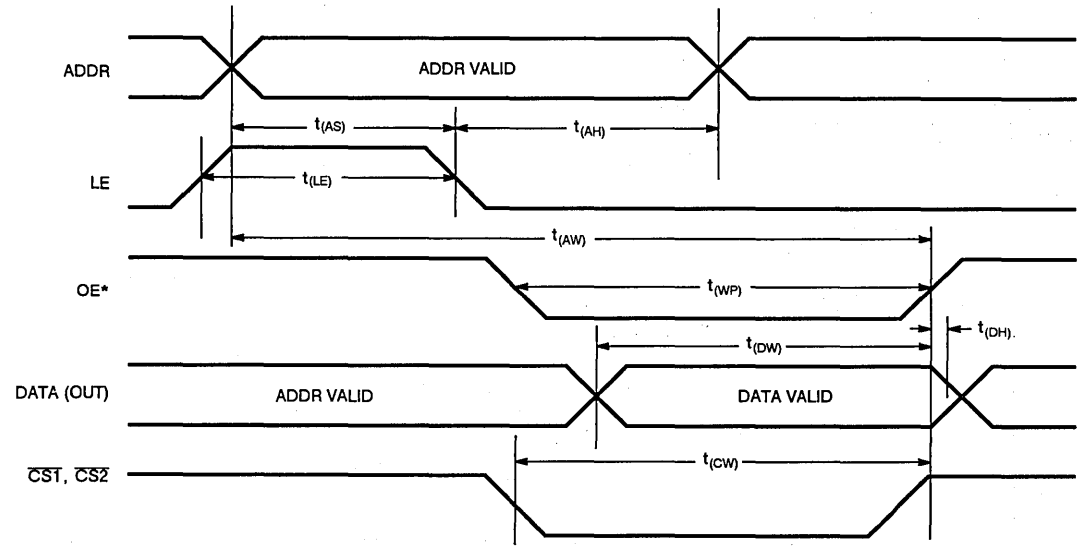


AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	12 MHz MIN.	12 MHz MAX.	16.6 MHz MIN.	16.6 MHz MAX.	20 MHz MIN.	20 MHz MAX.	25 MHz MIN.	25 MHz MAX.	UNIT
WRITE CYCLE										
t_{LE}	Latch Enable Width	8	–	6	–	6	–	6	–	ns
t_{AS}	Address Setup Time to LE	4	–	2	–	2	–	2	–	ns
t_{AH}	Address Hold Time from LE	3	–	1.5	–	1.5	–	1.5	–	ns
t_{AW} (2)	Address Valid to End of Write	40	–	30	–	25	–	22	–	ns
t_{CW}	Chip Select to End of Write	35	–	25	–	20	–	17	–	ns
t_{WP}	Write Pulse Width	30	–	25	–	20	–	17	–	ns
t_{DW}	Data Valid to End of Write	20	–	13	–	13	–	10	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns

NOTES:
1. Guaranteed but not tested.
2. LE asserted.

TIMING WAVEFORM OF WRITE CYCLE



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TRUTH TABLE

MODE	$\overline{CS1}$	$\overline{CS2}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	D_{OUT}	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	18	pF

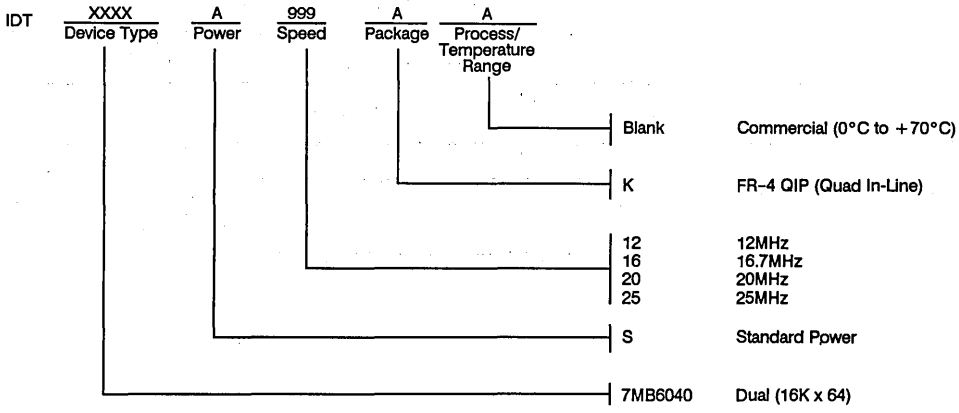
NOTE:
1. This parameter is sampled and not 100% tested.

FULLY ASSEMBLED MODULE SCREENING FLOW[1]

SCREEN	TEST METHOD	LEVEL
Final Electrical Tests		
Static (DC)	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes	100%
Functional	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a) @ 25°C and Power Supply Extremes	100%
	b) @ Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	IDT Specification	100%

NOTE:
1. Screening of the fully assembled module is performed per the table to assure package integrity and mechanical reliability. Finally, 100% electrical tests are performed.

ORDERING INFORMATION



Integrated Device Technology, Inc.

8K x 112 WRITABLE CONTROL STORE STATIC RAM MODULE

IDT 7MB6042

FEATURES:

- 8K x 112 high-performance Writable Control Store (WCS)
- Serial Protocol Channel (SPC™)—reading, writing and interrogation
- High fanout pipeline register
- Width expandable
- Designed for high-speed writable control store applications
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Compact quad in-line module
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

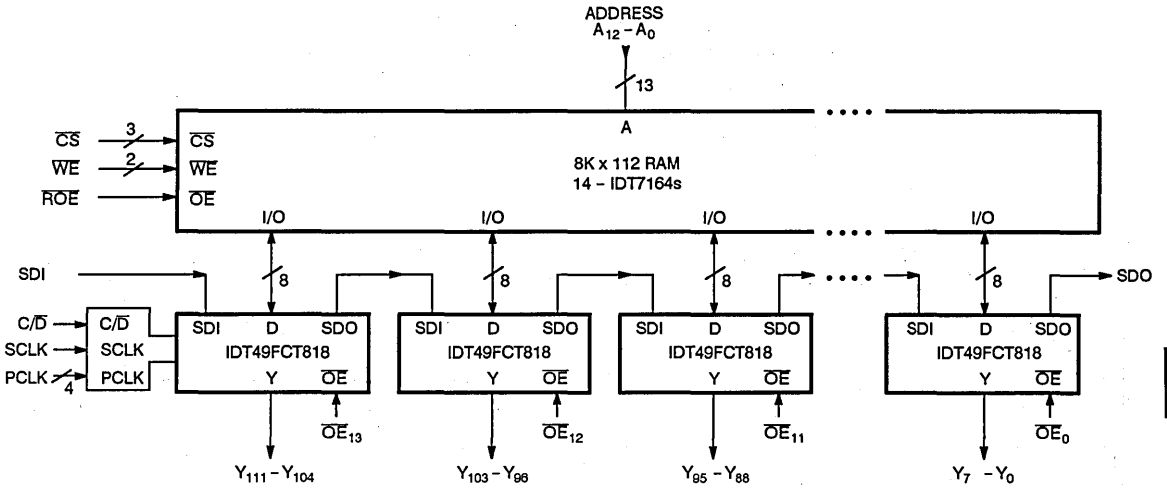
DESCRIPTION:

The IDT7MB6042 is an 8K x 112-bit Writable Control Store (WCS) RAM and pipeline register. It features fourteen 8K x 8 IDT7164 high-performance static RAMs and fourteen IDT49FCT818 Serial Protocol Channel (SPC) registers. These devices are arranged to form the 8K x 112 Writable Control Store RAM with Serial Protocol Channel for loading of the memory. Each eight outputs of the RAM are connected to the D inputs of an IDT49FCT818 in the normal fashion. The device has the serial data-in and serial data-output bits connected to form a 112-bit Serial Protocol Channel register. The command/data (C/$\overline{D}$) and Serial Shift Clock (SCLK) are all bus organized across the fourteen IDT49FCT818 registers. The 112 register output bits, 8 from each device, are separately brought out to form a 112-bit wide pipeline register on the Writable Control Store.

In normal operation, data from the 112-bit wide memory is loaded into the IDT49FCT818 registers on the low-to-high transition of PCLK. Reading and writing of the memory by means of the Serial Protocol Channel are performed using the protocol of the IDT49FCT818. (For details of this operation, please refer to the IDT49FCT818 data sheet.) The data to be loaded can be shifted in the serial data input by using the SCLK and a load command executed by shifting the proper command word in the serial data input when the C/$\overline{D}$ line is in the command mode. This command will then be executed by manipulating the C/$\overline{D}$ line and SCLK line in the desired fashion. Data is then written into the RAM by bringing the write enable line on the RAM memory from the high state to the low state and back to the high state.

The IDT7MB6042 is offered as a compact, cost-effective FR-4 quad in-line module and occupies less than 9 square inches of board space.

FUNCTIONAL BLOCK DIAGRAM



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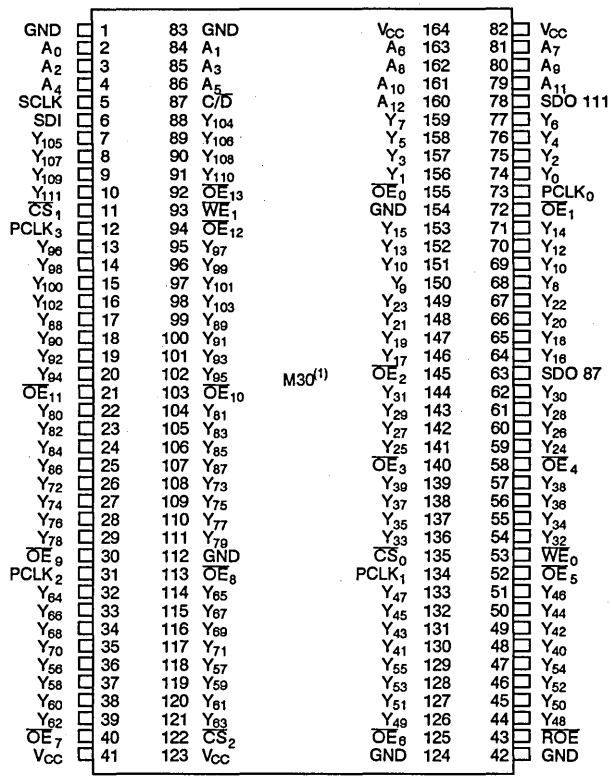
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M30 in the packaging section.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMM.	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	H	X	High Z	Standby
Standby	H	L	X	D_{OUT}	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	SPC(1)	L	SPC(1)	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
$C_{IN(D)}$	Input Capacitance Data	V_{IN} = 0V	10	pF
$C_{IN(A)}$	Input Capacitance Address and Control	V_{IN} = 0V	120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. This parameter is sampled and not 100% tested.

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
A_{0-12}	I	Address Bus Pins (A_0 = LSB, A_{12} = MSB)
Y_{0-111}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_{111} = MSB)
$\overline{OE}_Y$	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 & 14)
SDI	I	Serial Data In for SPC Operation. Data and command shifts in the Least Significant Bit first
SDO	O	Serial Data Out for SPC Operation. Data and command shifts out the Least Significant Bit first
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations
$\overline{CS}$	I	Internal RAM Chip Select
$\overline{WE}$	I	Internal RAM Write Enable
$\overline{ROE}$	I	Internal RAM Output Enable

NOTE:
1. See SPC commands for proper execution of write cycle.

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	100	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	15	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	15	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 32mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15mA	2.4	–	V
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open	–	1500	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	–	2380	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IL}	–	560	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V	–	280	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	30ns MIN.	30ns MAX.	35ns MIN.	35ns MAX.	40ns MIN.	40ns MAX.	50ns MIN.	50ns MAX.	60ns MIN.	60ns MAX.	UNIT
READ CYCLE												
t_{AC}	Address Valid to PCLK Set Up	30	–	35	–	40	–	50	–	60	–	ns
t_{CS}	$\overline{CS}$ Valid to PCLK Set Up	30	–	35	–	40	–	50	–	60	–	ns
t_{OESU}	$\overline{ROE}$ Valid to PCLK Set Up	17	–	20	–	25	–	30	–	35	–	ns
t_{PCY}	PCLK to Output Valid	–	10	–	12	–	15	–	15	–	15	ns
t_{OE}	$\overline{OE}$ Asserted to Output Valid	–	10	–	12	–	15	–	15	–	15	ns
t_{OHZ}	$\overline{OE}$ Negated to Output In High Z	–	10	–	12	–	15	–	15	–	15	ns
WRITE CYCLE												
t_{AW}	Address Valid to End of Write	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Address Valid to End of Write	25	–	30	–	35	–	45	–	55	–	ns
t_{WP}	Write Enable Pulse Width	23	–	28	–	33	–	43	–	53	–	ns
t_{WCD}	Cont/Dat to End of Write	23	–	28	–	30	–	35	–	40	–	ns
t_{AS}	Address Setup Time	0	–	0	–	2	–	2	–	2	–	ns

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SPC TIMING

SYMBOL		PARAMETER	30ns		35ns		40ns		50ns		60ns		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	T_2	SCLK High to SDO	–	15	–	15	–	22	–	22	–	22	ns
	T_3	SDI to SDO (Stub Mode)	–	210	–	210	–	310	–	310	–	310	ns
	T_4	C/$\overline{D}$ Low to Y	–	15	–	15	–	20	–	20	–	20	ns
	T_5	SCLK High to Y	–	15	–	15	–	25	–	25	–	25	ns
	T_6	C/$\overline{D}$ Low to SDO	–	15	–	15	–	25	–	25	–	25	ns
t_{SU}	S_2	C/$\overline{D}$ to SCLK High	15	–	15	–	15	–	15	–	15	–	ns
	S_3	SDI to SCLK High	8	–	8	–	8	–	8	–	8	–	ns
	S_4	Y or D to C/$\overline{D}$ Low	5	–	5	–	5	–	5	–	5	–	ns
	S_5	C/$\overline{D}$ to PCLK High	12	–	12	–	12	–	12	–	12	–	ns
t_H	S_6	Y to PCLK High	5	–	5	–	5	–	5	–	5	–	ns
	H_2	C/$\overline{D}$ from SCLK Low	12	–	12	–	12	–	12	–	12	–	ns
	H_3	SDI from SCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H_4	Y or D to C/$\overline{D}$ Low	2	–	2	–	2	–	2	–	2	–	ns
	H_5	SCLK High to PCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H_6	C/$\overline{D}$ from PCLK High	2	–	2	–	2	–	2	–	2	–	ns
	H_7	Y from PCLK High	3	–	3	–	3	–	3	–	3	–	ns
t_{HZ}[1,2]	2z, 4z	SCLK High to D or Y High Z	–	15	–	15	–	20	–	20	–	20	ns
t_{LZ}[1,2]	3z, 5z	C/$\overline{D}$ High to D or Y High Z	–	15	–	15	–	20	–	20	–	20	ns
t_{ZHL}[1,2]	Z2,Z3	C/$\overline{D}$ Low to D or Y Valid	–	15	–	15	–	20	–	20	–	20	ns
t_W	W_1	PCLK (High & Low)	10	–	10	–	15	–	15	–	15	–	ns
	W_2	SCLK (High & Low)	30	–	30	–	35	–	35	–	35	–	ns
	W_3	C/$\overline{D}$ High	30	–	30	–	35	–	35	–	35	–	ns

NOTES:
1. Guaranteed but not tested.
2. $\overline{OE}$ = V_{IH}

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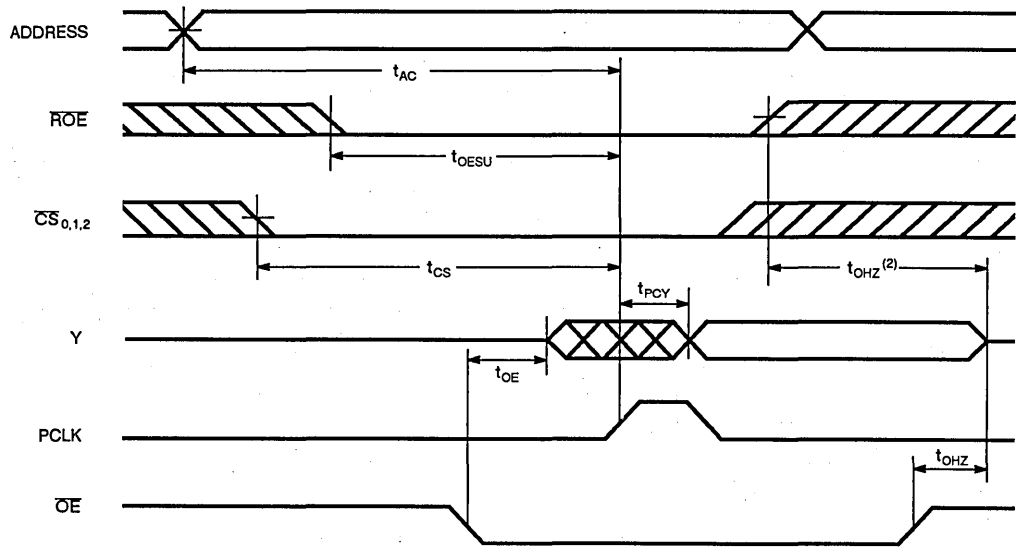
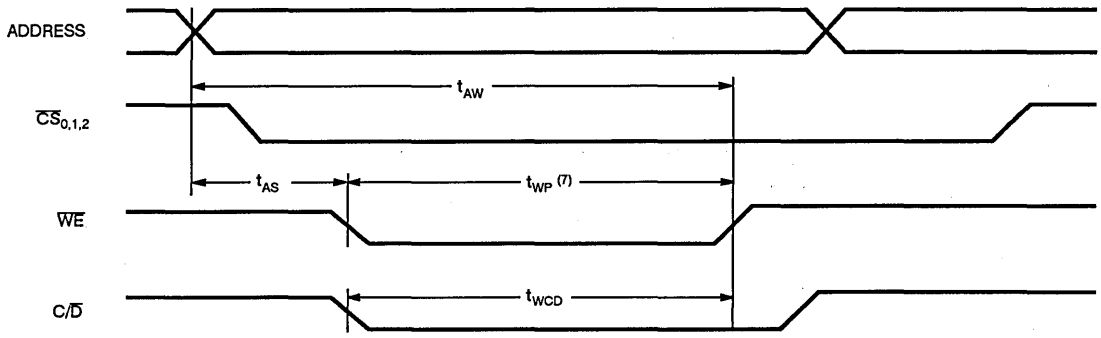
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)

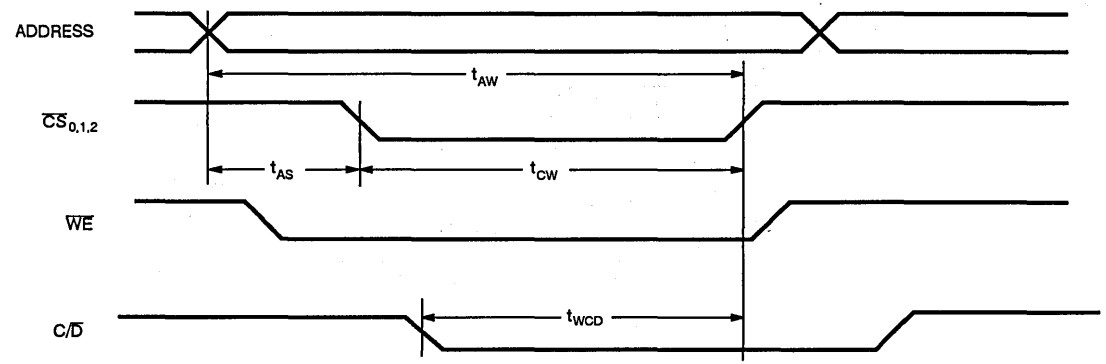


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 5]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 4, 5]



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. $\overline{ROE}$ = V_{IH}

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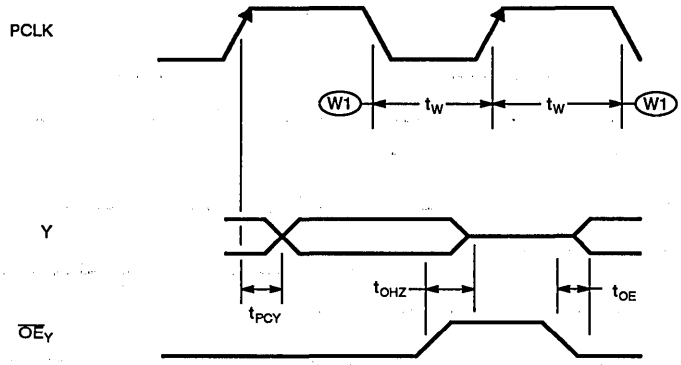
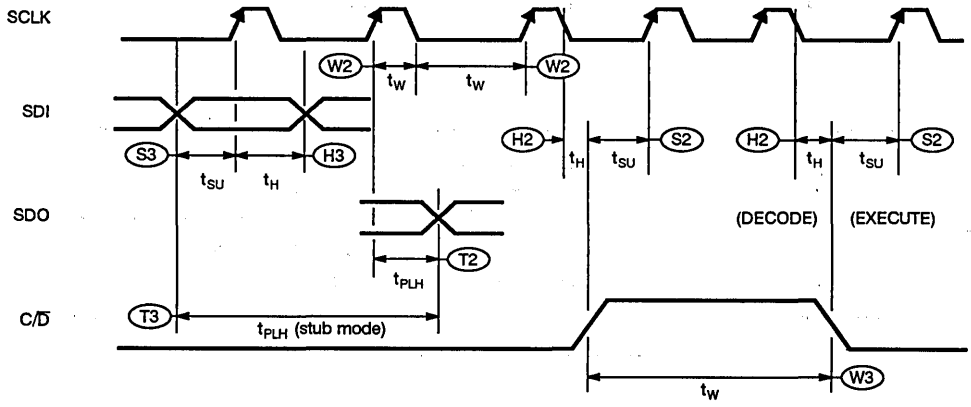
GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS

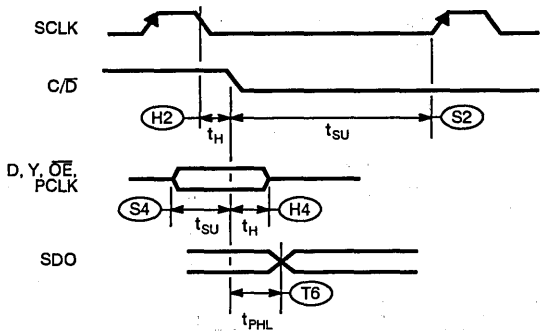


GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS

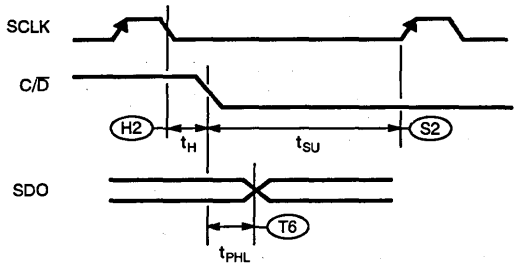


DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

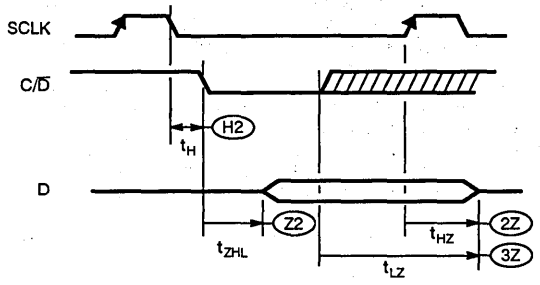
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



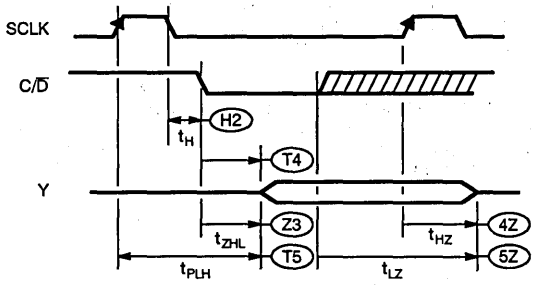
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



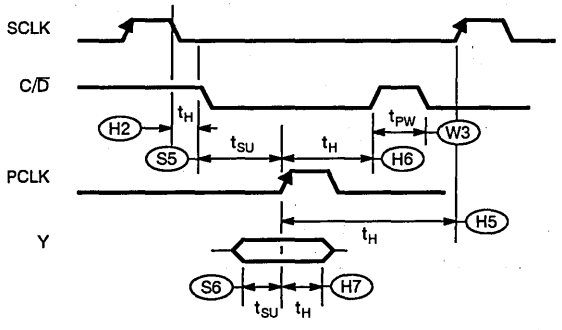
CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



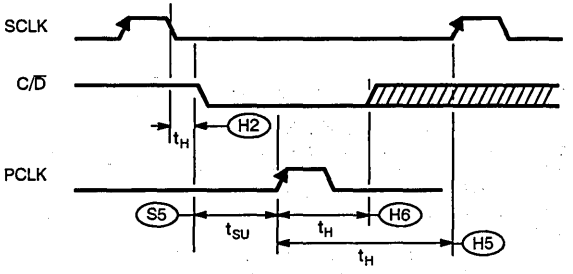
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



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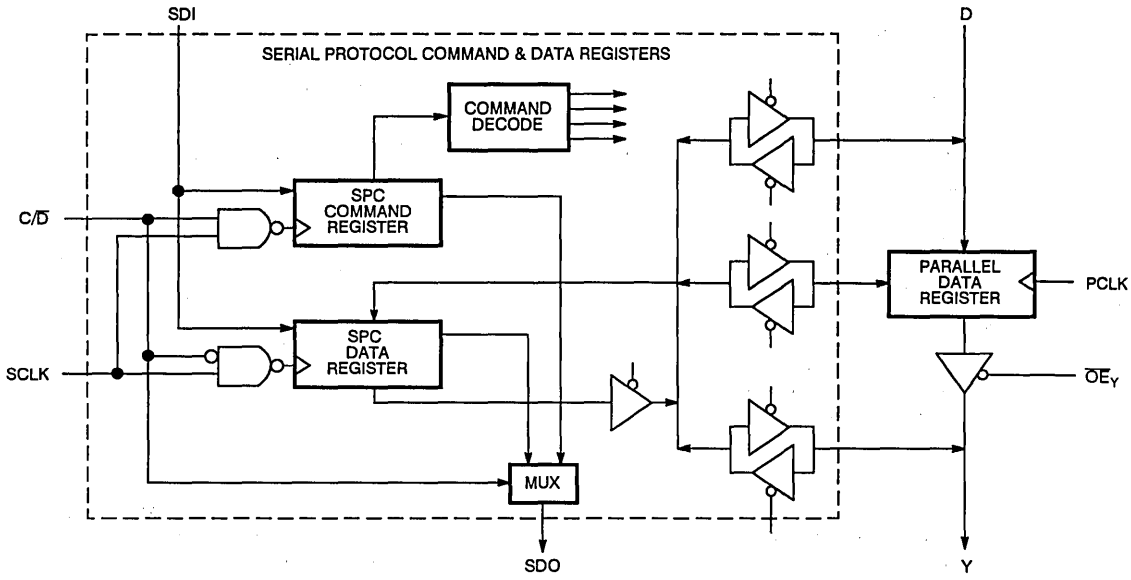
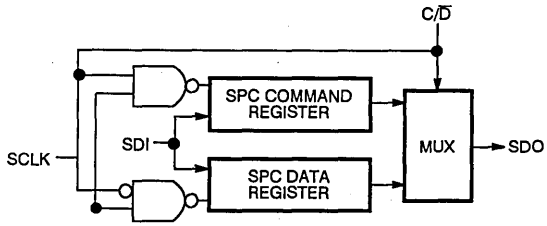
DETAILED FUNCTIONAL BLOCK DIAGRAM



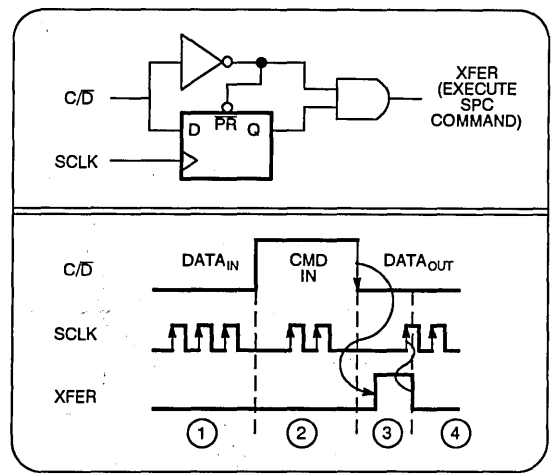
The detailed block diagram consists of two main elements: the parallel data register and the SPC data/command registers. The main data path is from the D inputs down to the data register and through to the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.



SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel—one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge.



SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may then be transitioned from low-to-high. SPC commands and data can be shifted anytime, without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow the PCLK to run. In these operations, the high-to-low transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next low-to-high transition of the PCLK.

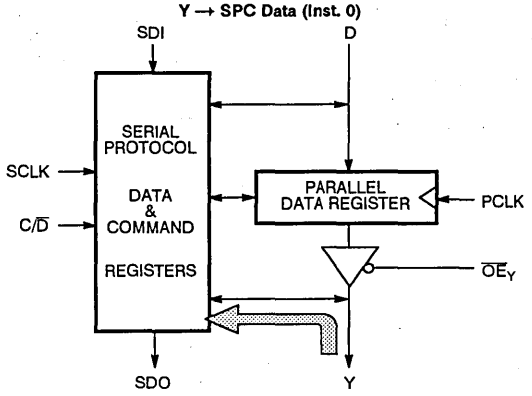
SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

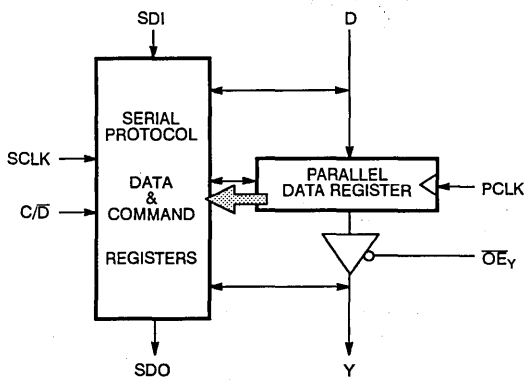
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}$ is overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

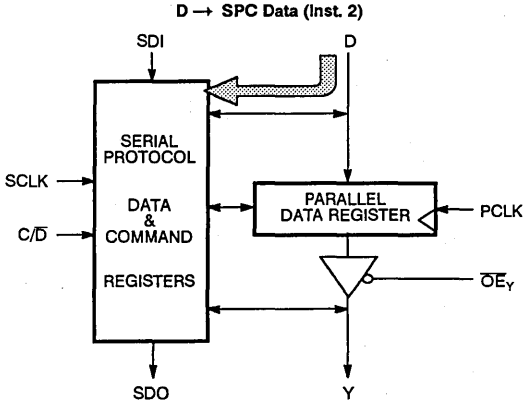
Y → SPC Data (Inst. 0)



Data Register → SPC Data (Inst. 1)



D → SPC Data (Inst. 2)



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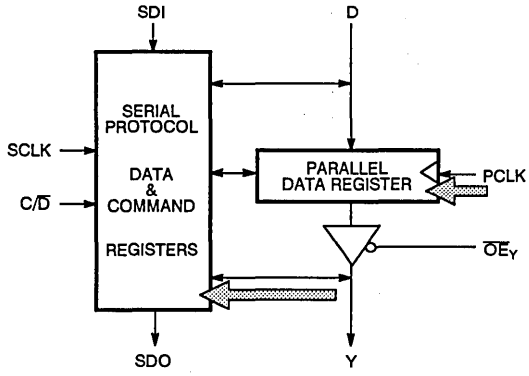
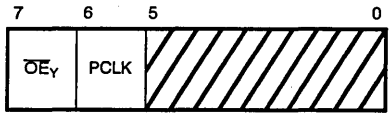
Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the SPC data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ low-high-low after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

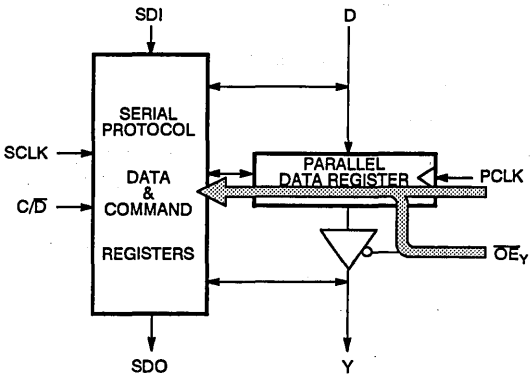
Y → SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

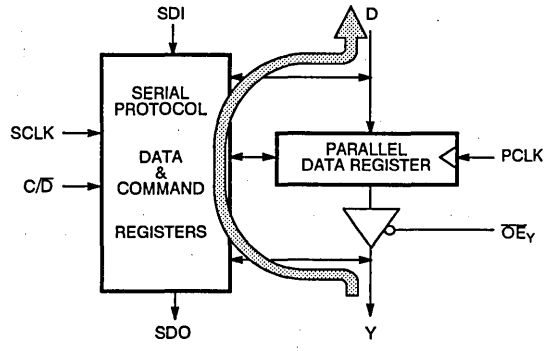


Status → SPC Data (Inst. 4)

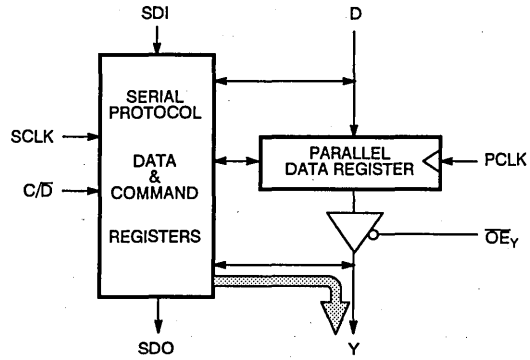


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

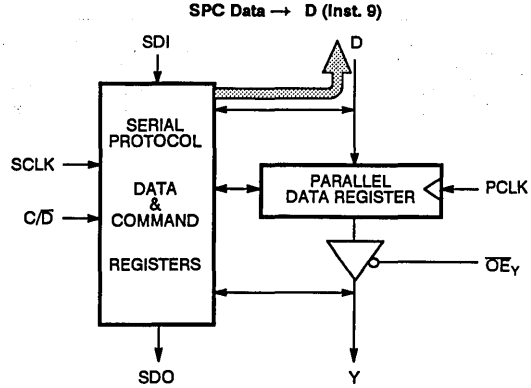


SPC Data → Y (Inst. 8)



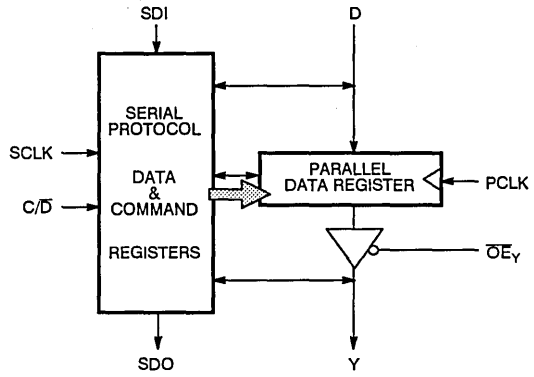
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

SPC Data → D (Inst. 9)



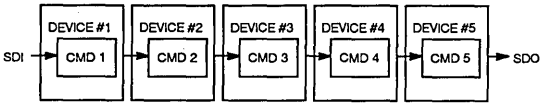
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going high-to-low and SCLK going low-to-high.

SPC Data → Parallel Data Register (Inst. 10)



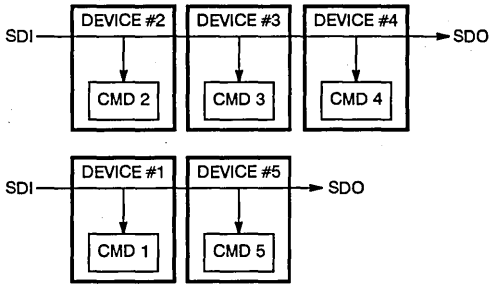
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



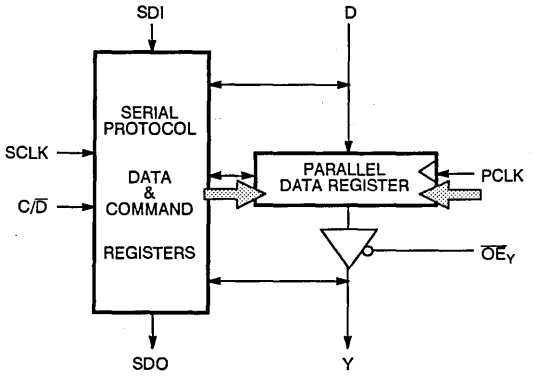
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

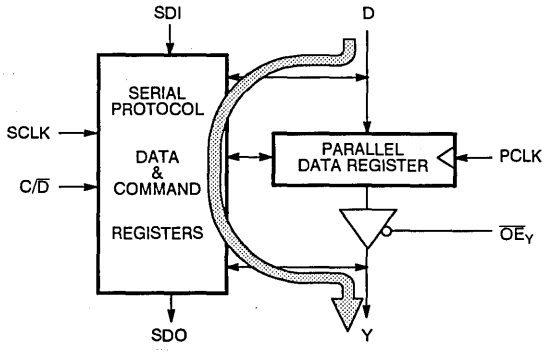


Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.

SPC Data → Parallel Data Register Synchronous w/PCLK (Inst. 13)

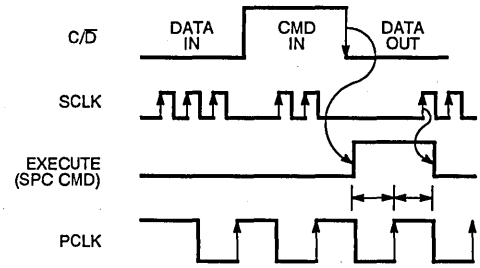


Connect D to Y (Inst. 14)



13

Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the high-to-low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC data register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line high. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

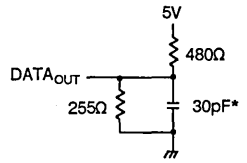


Figure 1. Output Load

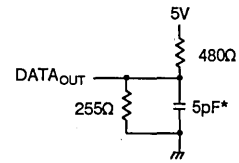
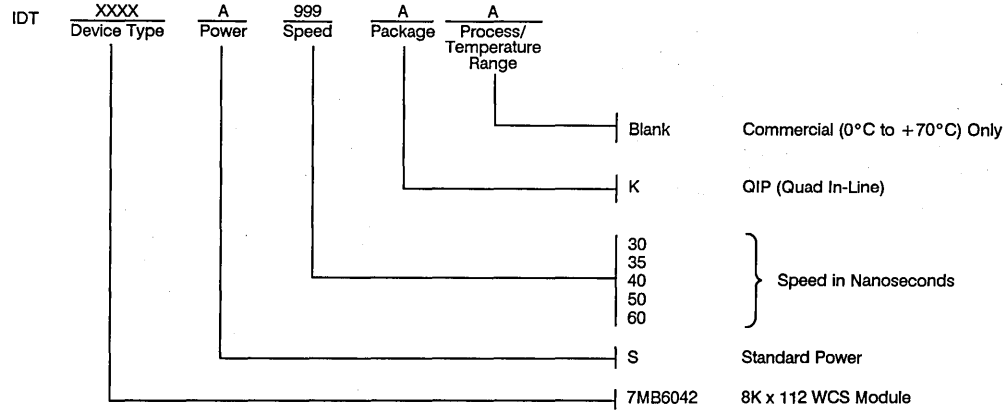


Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig.

ORDERING INFORMATION



Integrated Device Technology, Inc.

DUAL (8K x 64) DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

ADVANCE INFORMATION
IDT 7MB6043

FEATURES:

- High-speed CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache (dual 8K x 64)
- Operating frequencies to support 12MHz, 16.7MHz and 20MHz IDT79R3000
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (±10%) power supply

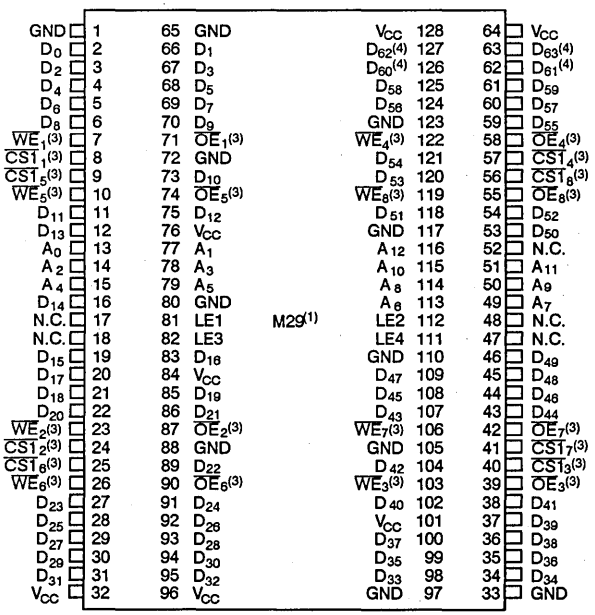
DESCRIPTION:

The IDT7MB6043 is a 128K-byte high-speed CMOS static RAM constructed on a multilayer epoxy substrate (FR-4), using 16 IDT7164 (8K x 8) RAMs and 8 IDT74FCT373 latches.

The construction and specifications of this module have been optimized to support its use as a complete 8K deep Instruction and Data cache for the IDT79R3000.

The IDT7MB6043 is organized as two separate banks of 8K x 64 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 13-bit ADDRESS bus and a common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches and, thereby, enhance performance.

PIN CONFIGURATION



QIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M29 in the packaging section.

PIN NAMES

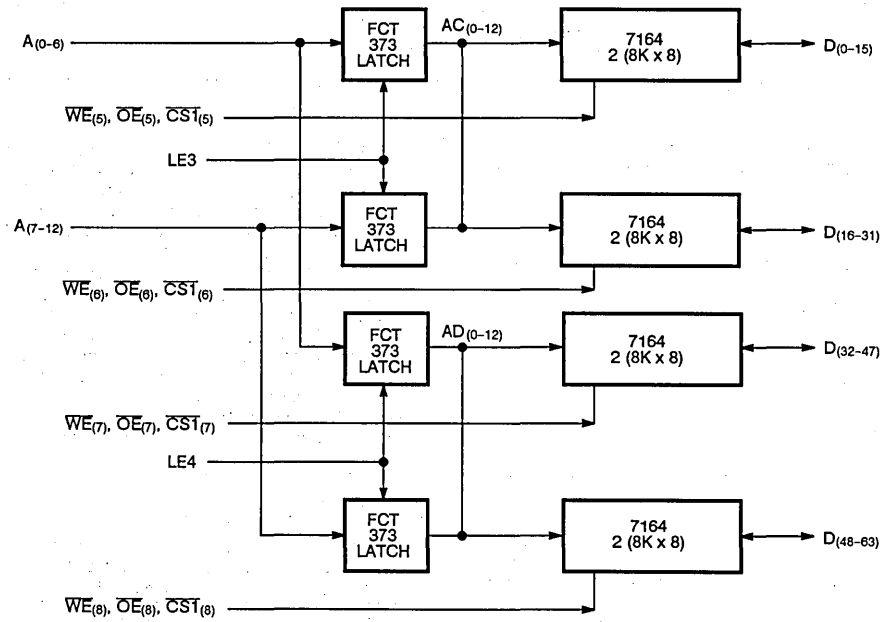
D_0 – D_{59}	Data I/Os
A_0 – A_{11}	Address Inputs
LE1 – LE4	Latch Enables
$\overline{CST}_1$(3) – $\overline{CST}_8$(3)	RAM Selects
$\overline{WE}_1$(3) – $\overline{WE}_8$(3)	Write Enables
$\overline{OE}_1$(3) – $\overline{OE}_8$(3)	Output Enables
GND	Ground
V_{CC}	Power Supply
N.C.	No Connection

NOTES:

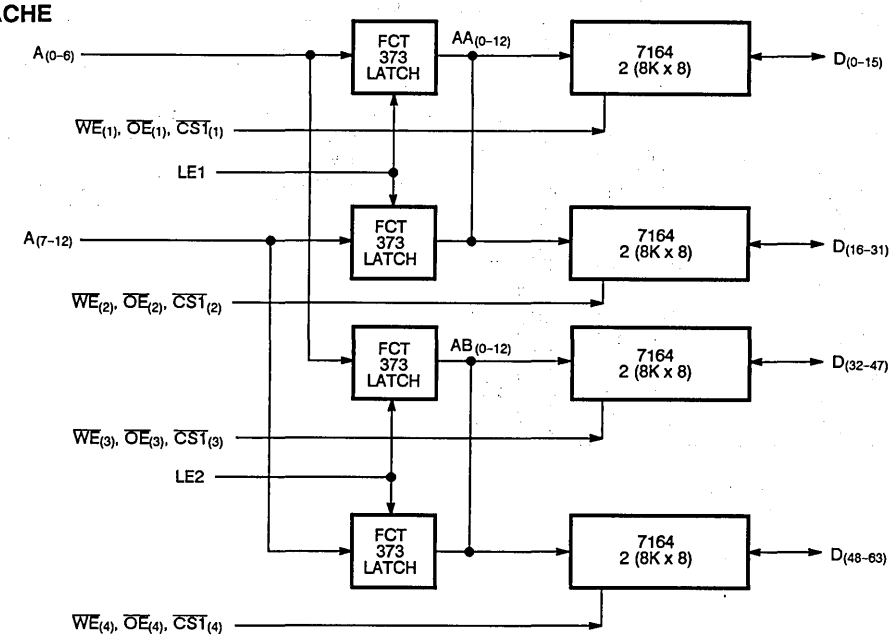
1. All GND pins must be grounded for proper operation.
2. All V_{CC} pins must be connected to +5V for proper operation.
3. Active Low Signal.
4. These pins must be connected to GND or V_{CC} through a resistor for proper operation in the IDT79R3000 application.

13

INSTRUCTION CACHE



DATA CACHE



Integrated Device Technology, Inc.

DUAL (4K X 64) DATA/ INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU

ADVANCE INFORMATION
IDT 7MB6044

FEATURES:

- High-speed CMOS static RAM module constructed to support the IDT79R3000 RISC CPU as a complete data and instruction cache (dual 4K x 64)
- Operating frequencies to support 12MHz, 16.7MHz and 20MHz IDT79R3000
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- On-board address latches for direct interface to the IDT79R3000 CPU
- TTL compatible I/Os
- Single 5V (±10%) power supply

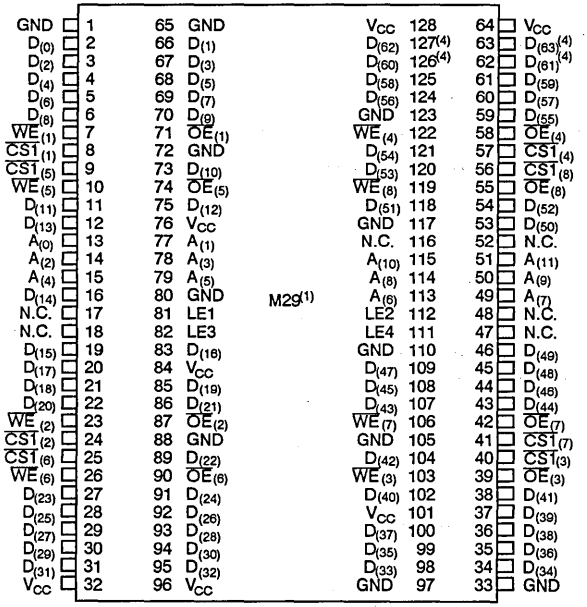
DESCRIPTION:

The IDT7MB6044 is a 64K-byte high-speed CMOS static RAM constructed on a multilayer epoxy substrate (FR-4), using 8 IDT71586 (4K x 16) Latched RAMs.

The construction and specifications of this module have been optimized to support its use as a complete 4K deep Instruction and Data cache for the IDT79R3000.

The IDT7MB6044 is organized as two separate banks of 4K x 64 with the IDT71586s being used as address latched RAMs. The two banks of RAM with their associated address latches share a common 12-bit ADDRESS bus and a common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM.

PIN CONFIGURATION



QIP
TOP VIEW

NOTE:

1. For module dimensions, please refer to module drawing M29 in the packaging section.

PIN NAMES

D_0 - D_{59}	Data I/Os
A_0 - A_{11}	Address Inputs
LE1 - LE4	Latch Enables
$\overline{CS1}_1$ - $\overline{CS1}_8$	RAM Selects
$\overline{WE}_1$ - $\overline{WE}_8$	Write Enables
$\overline{OE}_1$ - $\overline{OE}_8$	Output Enables
GND	Ground
V_{CC}	Power Supply
NC	No Connection

NOTES:

1. All GND pins must be grounded for proper operation.
2. All V_{CC} pins must be connected to +5V for proper operation.
3. These pins must be connected to GND or V_{CC} through a resistor for proper operation of the IDT79R3000 application.

13

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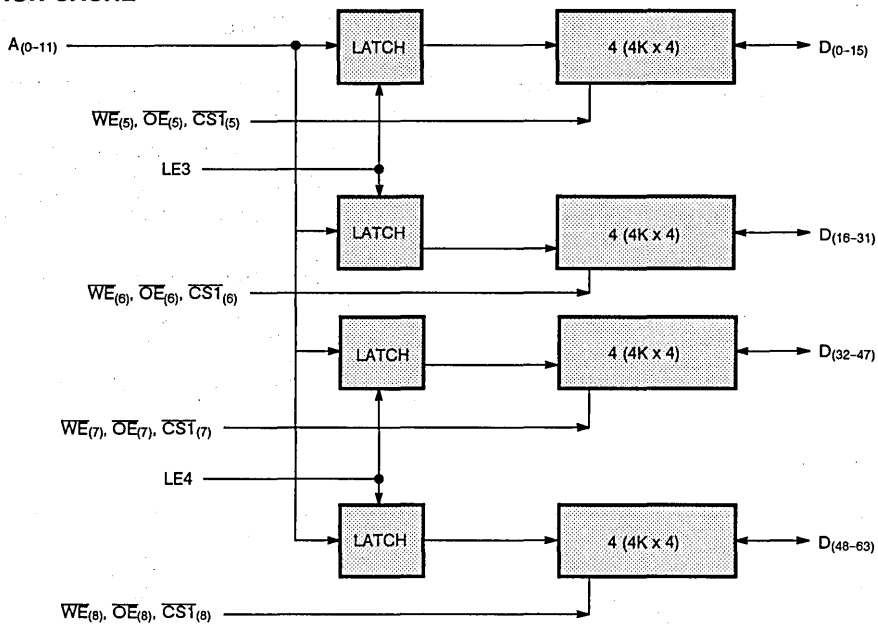
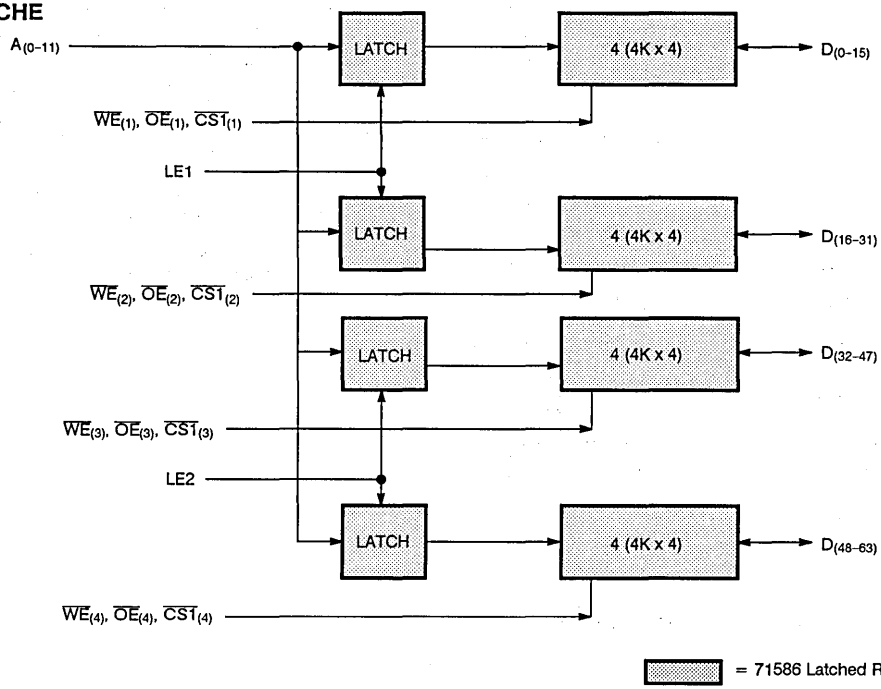
DSC-7031/-

INSTRUCTION CACHE



DATA CACHE



Integrated Device Technology, Inc.

DUAL(16K x 60) DATA/ INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

ADVANCE INFORMATION
IDT 7MB6049

FEATURES:

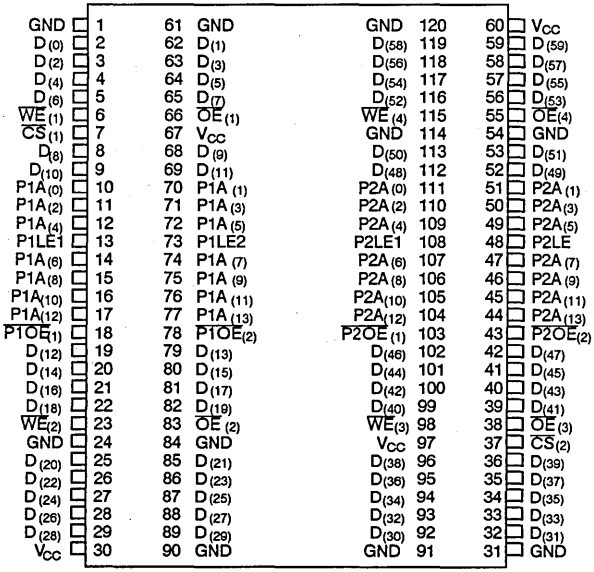
- High-speed CMOS static RAM module constructed to support the IDT79R3000 CPU in a multi-processor system as a complete data and instruction cache (dual 16K x 60)
- Additional data address invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz and 25MHz IDT79R3000
- Available in a high-density, low profile 120-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

The IDT7MB6049 is a 256K-byte high-speed CMOS static RAM constructed on a multilayer epoxy substrate (FR-4), using 28 IDT7198 (16K x 4) RAMs and 18 IDT74FCT373 latches.

The IDT7MB6049 supports use in a multi-processor system by providing data and instruction address invalidation latches on-board. The IDT7MB6049 is organized as two separate banks of 16K x 60 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches and, thereby, enhance performance.

PIN CONFIGURATION



QIP
TOP VIEW

PIN NAMES

$D_0 - D_{59}$	Data I/Os
$P1A_{(0)} - P1A_{(13)}$	Address Inputs
$P2A_0 - P2A_{13}$	Invalidate Address
P1LE1	Data Address Latch Enable
P1LE2	Instruction Address Latch Enable
$\overline{P1OE}_1$	Data Address Enable
$\overline{P1OE}_2$	Instruction Address Enable
$\overline{P2OE}_1$	Invalidate Data Address Enable
$\overline{P2OE}_2$	Invalidate Instruction Address Enable
$P2LE_1$	Invalidate Data Address Latch Enable
$P2LE_2$	Invalidate Instruction Address Latch Enable
$\overline{CS}_1 - \overline{CS}_2$	RAM Selects
$\overline{WE}_1^{(3)} - \overline{WE}_8^{(3)}$	Write Enables
$\overline{OE}_1^{(3)} - \overline{OE}_8^{(3)}$	Output Enables
GND	Ground
V_{CC}	Power Supply

NOTES:
1. All GND pins must be grounded for proper operation.
2. All V_{CC} pins must be connected to +5V for proper operation.
3. Active Low Signal.

13

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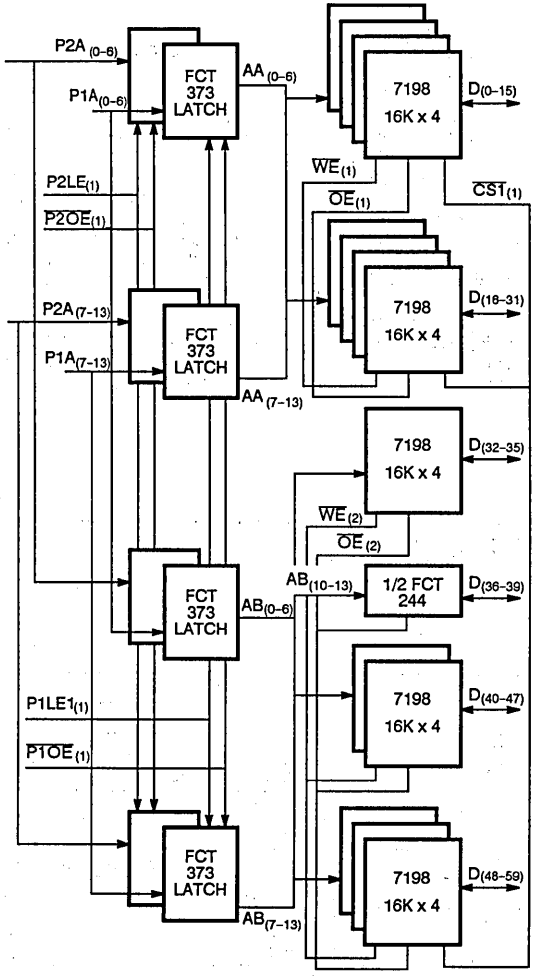
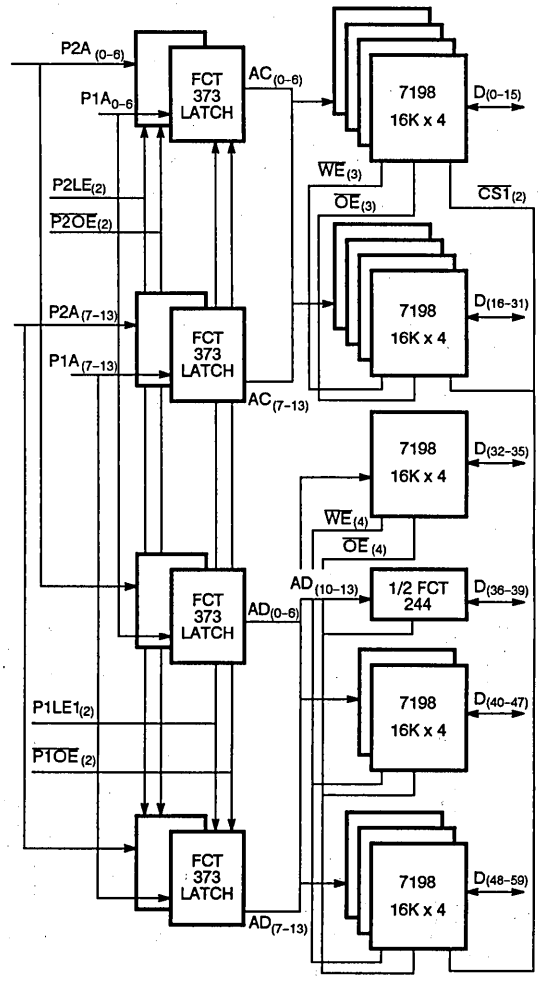
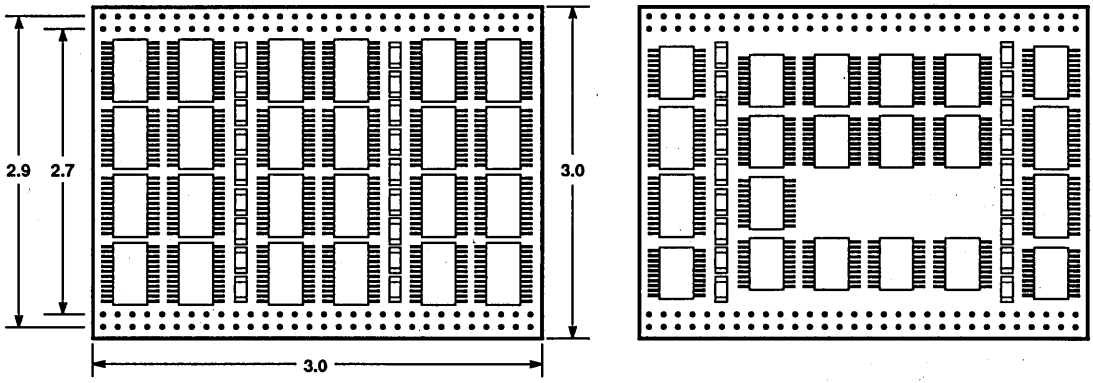
DATA CACHE



INSTRUCTION CACHE



PACKAGE DIMENSIONS
120-PIN QIP



13

Integrated Device Technology, Inc.

DUAL(8K x 64) DATA/ INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

ADVANCE INFORMATION
IDT 7MB6051

FEATURES:

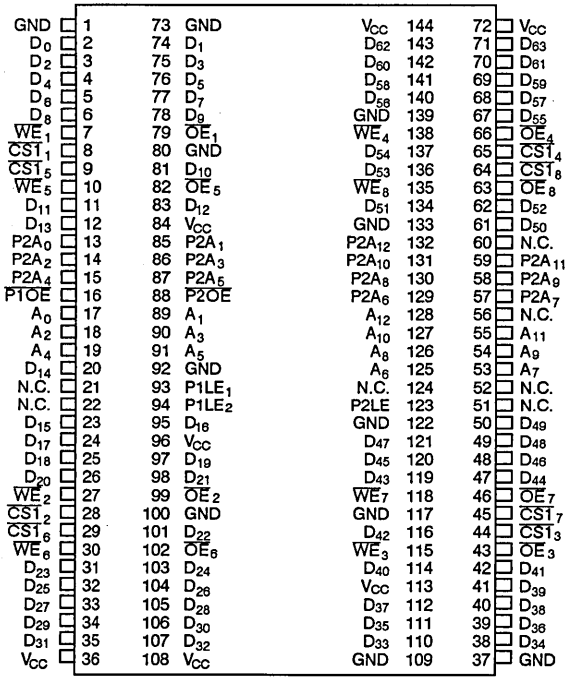
- High-speed CMOS static RAM module constructed to support the IDT79R3000 RISC CPU in a multi-processor system as a complete data and instruction cache (Dual 8K x 64)
- Additional data address invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12 MHz, 16.7 MHz and 20 MHz IDT79R3000
- Available in a high-density, low profile 144-pin QIP (quad in-line package)
- Surface mounted SOIC components on a multilayer epoxy substrate
- Multiple ground pins for maximum noise immunity
- TTL-compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

IDT7MB6051 is a 128K-byte high-speed CMOS static RAM constructed on a multilayer epoxy substrate (FR-4), using 16 IDT7164 (8K x 8) RAMs and 8 IDT4FCT373 latches.

The IDT7MB6051 supports use in a multi-processor system by providing data address invalidation latches on-board. The IDT7MB6051 is organized as two separate banks of 16K x 64 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches and, thereby, enhance performance.

PIN CONFIGURATION



QIP
TOP VIEW

PIN NAMES

$D_0 - D_{59}$	Data I/Os
$A_0 - A_{13}$	Address Inputs
$P2A_0 - P2A_{13}$	Invalidate Address
P1LE1	Data Address Latch Enable
P1LE2	Instruction Address Latch Enable
$\overline{P1OE}$	Data Address Enable
$\overline{P2OE}$	Invalidate Address Enable
P2LE	Invalidate Address Latch Enable
$\overline{CS1}_1 - \overline{CS1}_8$	RAM Selects
$\overline{CS2}_1 - \overline{CS2}_4$	RAM Selects
$WE_1 - WE_8$	Write Enables
$OE_1 - OE_8$	Output Enables
GND	Ground
V_{CC}	Power Supply
NC	No Connection

NOTES:
1. All GND pins must be grounded for proper operation.
2. All V_{CC} pins must be connected to +5V for proper operation.

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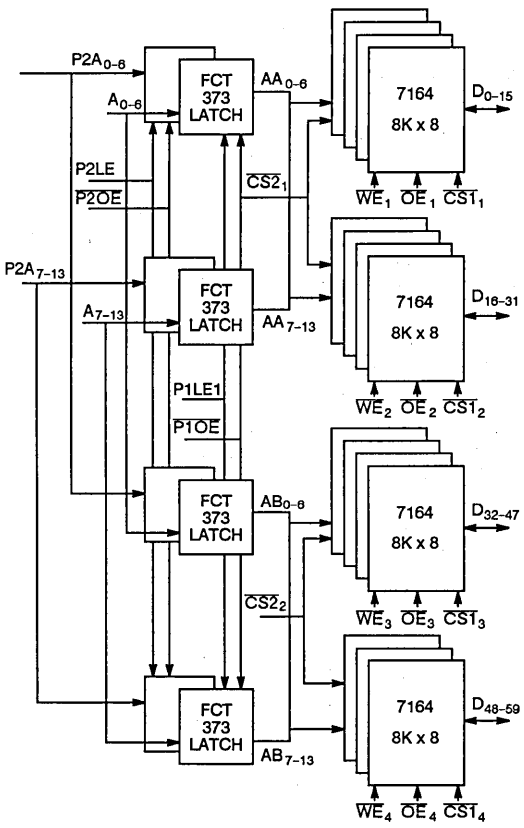
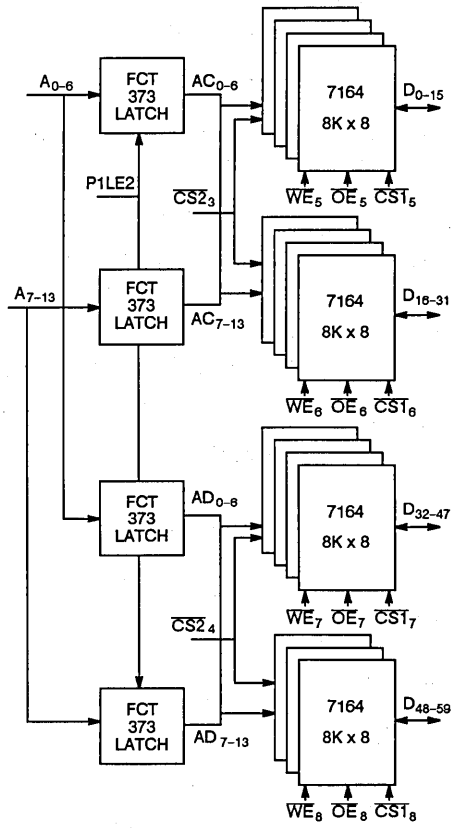
DSC-7045/-

DATA CACHE



INSTRUCTION CACHE



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Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM SIP MODULE

IDT 7MC156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 28-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187s high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

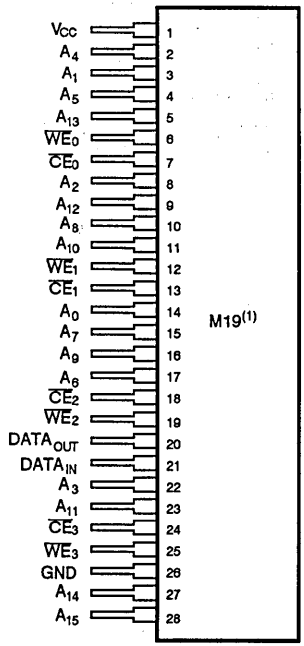
The IDT7MC156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on a co-fired ceramic substrate using four IDT7187 64K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC156 is offered in a 28-pin ceramic SIP (single in-line package). At only 350 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing greater than three IDT7MC156 modules to be stacked per inch of board space.

The IDT7MC156 is available with maximum access times as fast as 25ns and maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

All inputs and outputs of the IDT7MC156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION



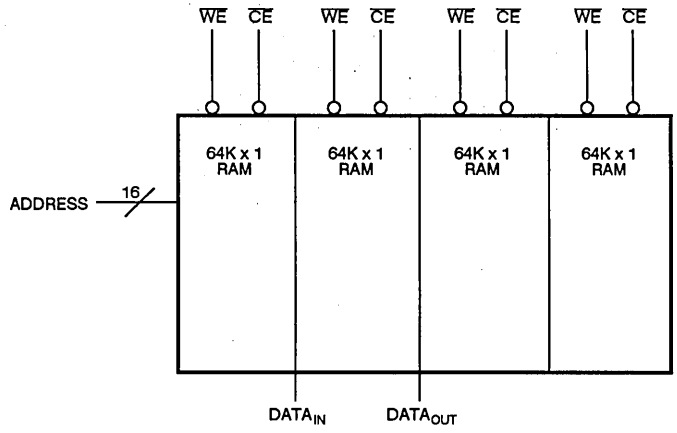
SIP
SIDE VIEW

NOTE:

1. For module dimensions, please refer to module drawing M19 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC156 MIN.	TYP.(1)	MAX.(2)	MAX.(3)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	110	225	300	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	120	245	330	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{IN} ≥ V_{HC} or V_{LC} V_{CS} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C
2. t_{AA} = 35, 45, 45, 55ns
3. t_{AA} = 25, 30ns

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

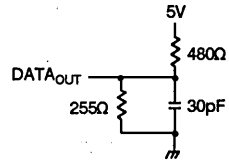


Figure 1. Output Load

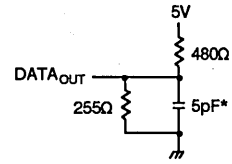


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MC156S25 MIN.	IDT7MC156S25 MAX.	IDT7MC156S30 MIN.	IDT7MC156S30 MAX.	IDT7MC156S35 MIN.	IDT7MC156S35 MAX.	IDT7MC156S45 MIN.	IDT7MC156S45 MAX.	IDT7MC156S55 MIN.	IDT7MC156S55 MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ [1]	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} [1]	Chip Select to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} [1]	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} [1]	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns

NOTE:
1. This parameter guaranteed but not tested.

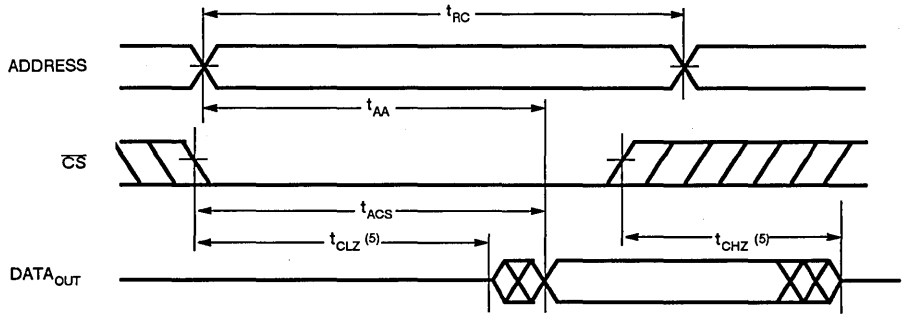
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

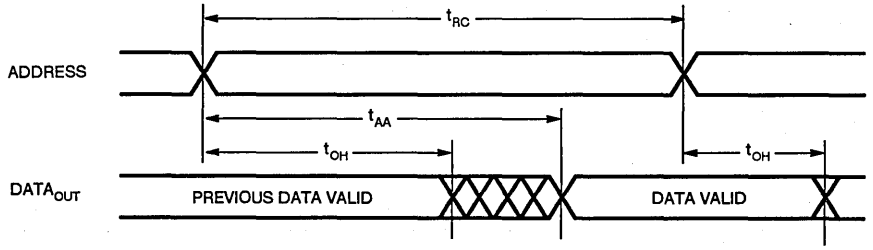
SYMBOL	PARAMETER	IDT7MC156S25 MIN.	IDT7MC156S25 MAX.	IDT7MC156S30 MIN.	IDT7MC156S30 MAX.	IDT7MC156S35 MIN.	IDT7MC156S35 MAX.	IDT7MC156S45 MIN.	IDT7MC156S45 MAX.	IDT7MC156S55 MIN.	IDT7MC156S55 MAX.	UNIT
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} [1]	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} [1]	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

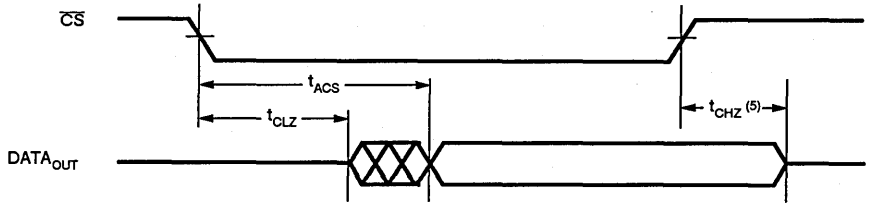
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

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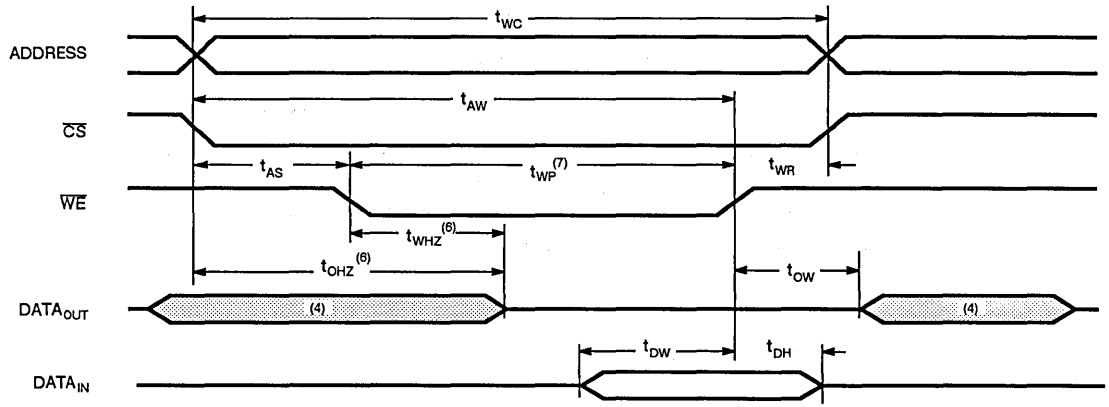
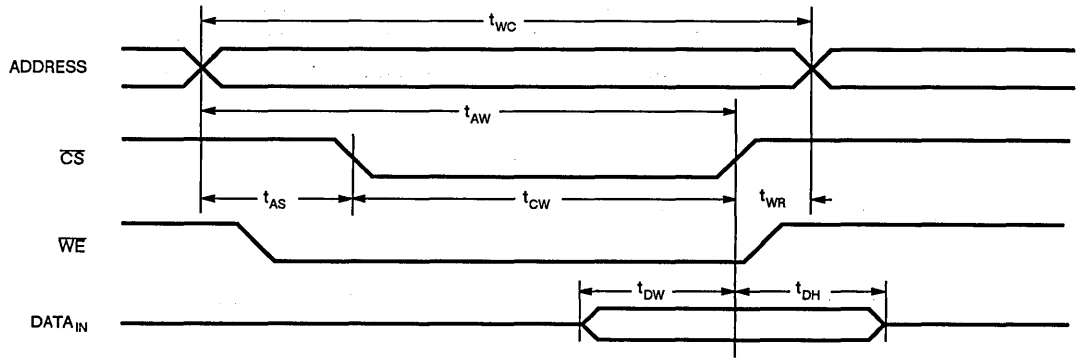
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

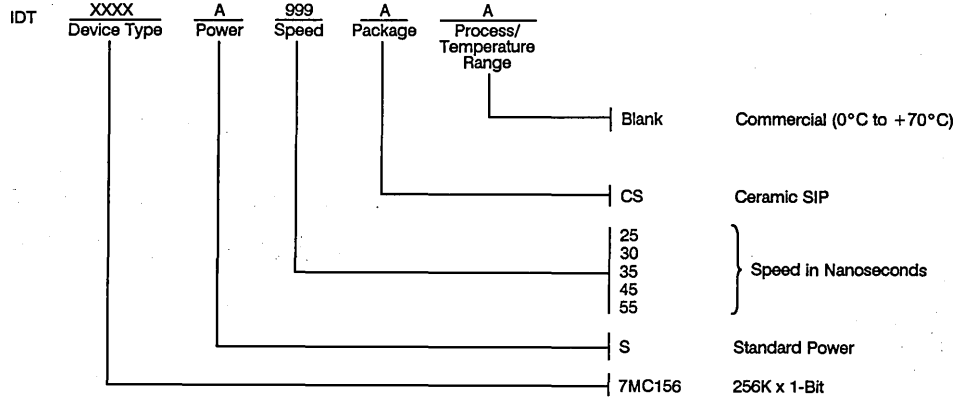
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

1 MEGABIT (1024K x 1-BIT) CMOS STATIC RAM SIP MODULE

PRELIMINARY
IDT 7MC4001

FEATURES:

- High-density 1 megabit (1024K x 1) CMOS static RAM module
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 35ns (max.)
- Separate I/O lines
- Low power consumption
  - Dynamic: 1.35W (max.)
  - Full standby: 330mW (max.)
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

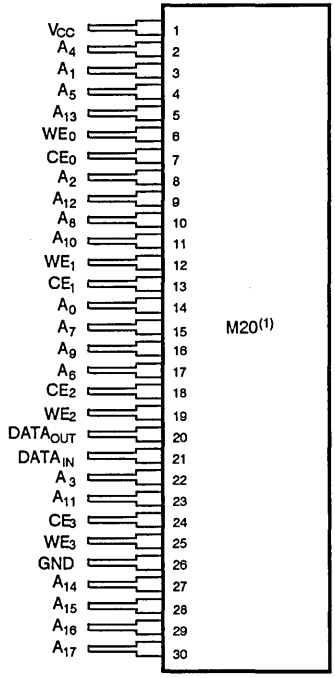
The IDT7MC4001 is a 1 megabit (1024K x 1-bit) high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four IDT71257 256K x 1 static RAMs in surface mount packages.

The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (single in-line package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing five IDT7MC4001 modules to be stacked per inch of board space.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access times for ease of use.

PIN CONFIGURATION

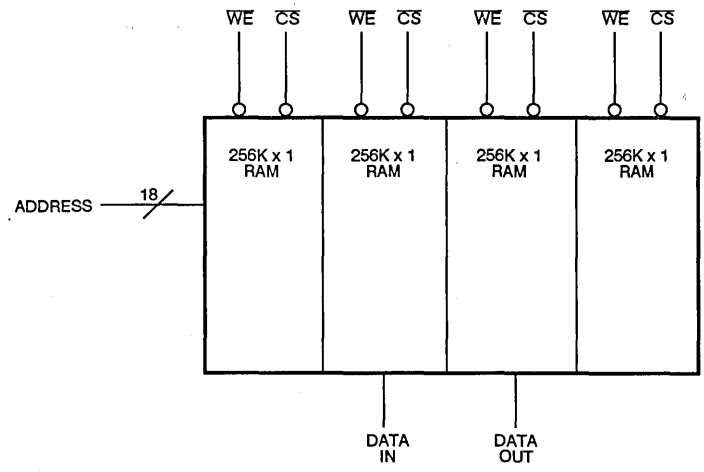


SIP
SIDE VIEW

NOTE:

1. For module dimensions, please refer to module drawing M20 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-17}	Address
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4001 MIN.	IDT7MC4001 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	50	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	225	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	245	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., Output Open	–	180	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	–	60	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	V

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

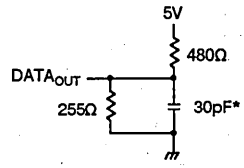


Figure 1. Output Load

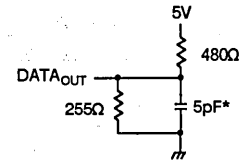


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
READ CYCLE								
t_{RC}	Read Cycle Time	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	10	–	10	–	10	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	25	–	35	–	45	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	35	–	45	–	55	ns

NOTE:
1. This parameter guaranteed but not tested.

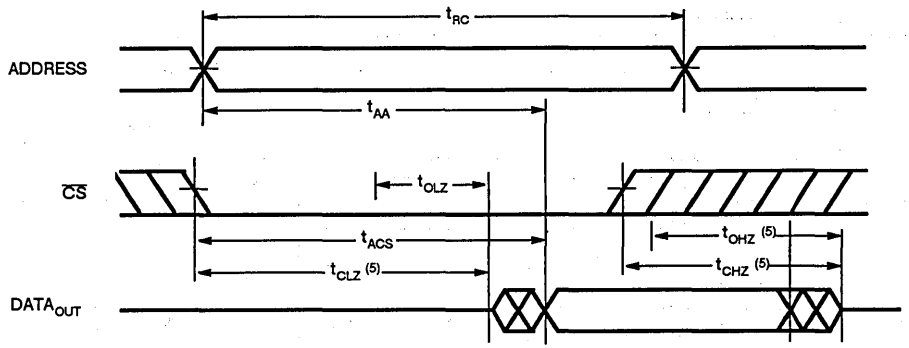
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

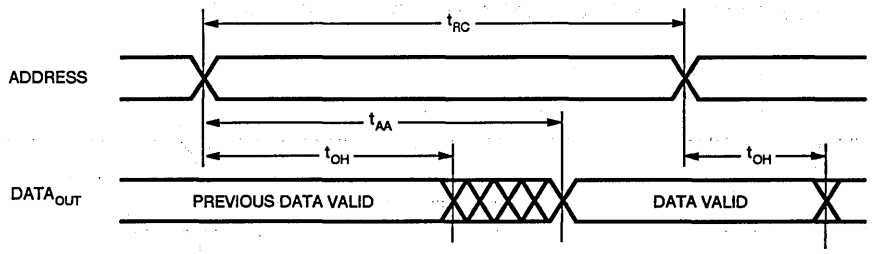
SYMBOL	PARAMETER	IDT7MC4001S35 MIN.	MAX.	IDT7MC4001S45 MIN.	MAX.	IDT7MC4001S55 MIN.	MAX.	UNIT
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	25	–	30	–	40	ns
t_{DW}	Data Valid to End of Write	20	–	25	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

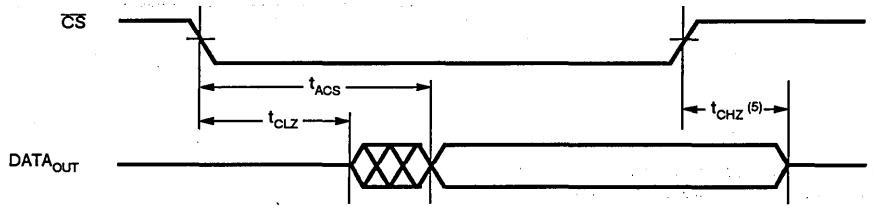
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)

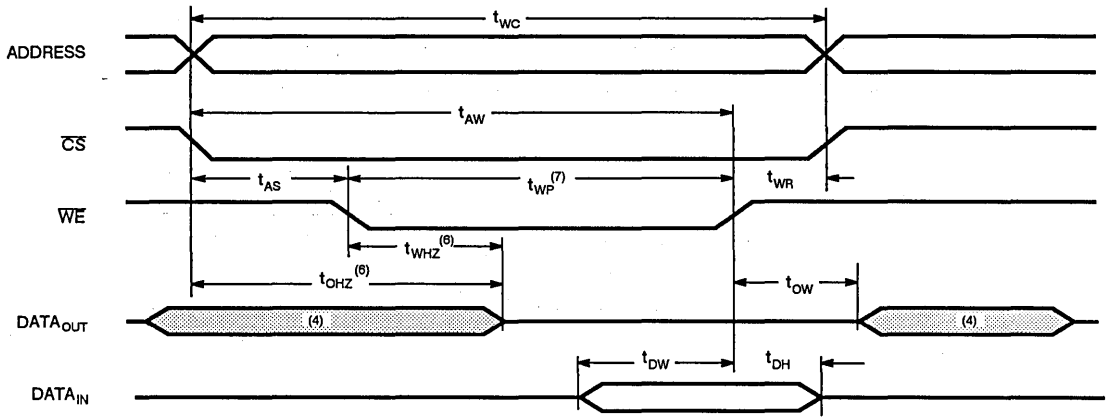


TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)

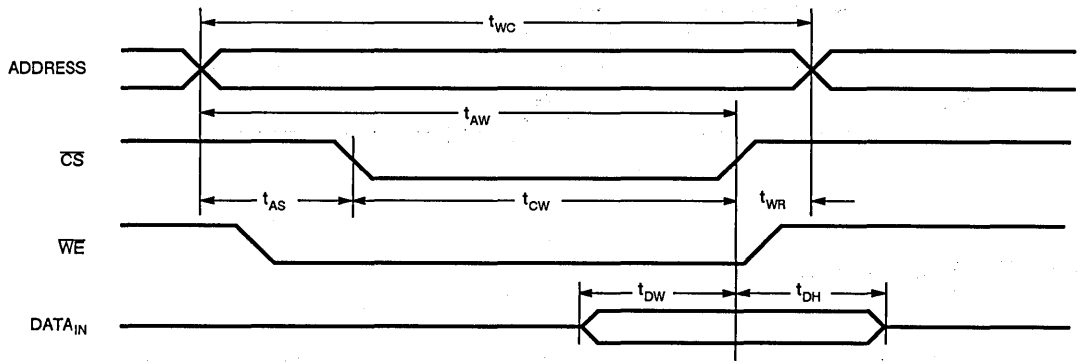


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

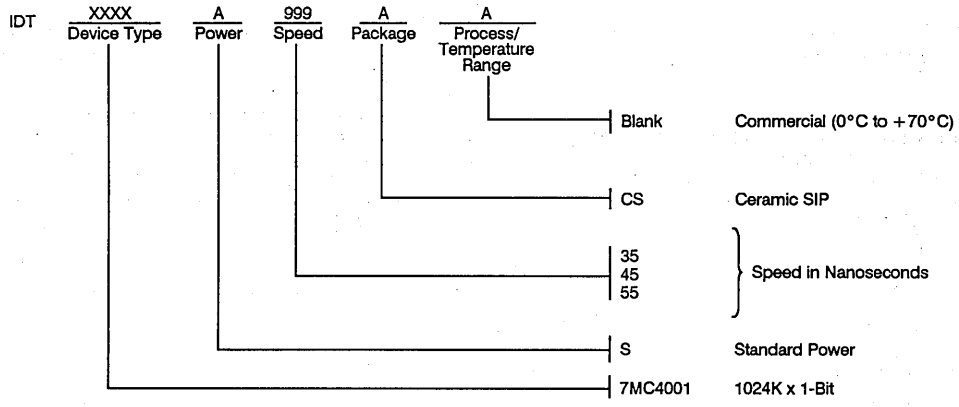
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

256K (16K x 16) CMOS STATIC RAM DUAL SIP MODULE

IDT 7MC4005

FEATURES:

- High-density 16-bit word 256K (16K x 16) static RAM module
- Low profile 36-pin sidebraze ceramic DSIP (dual single-in-line package)
- Fast access time: 20ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%)
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

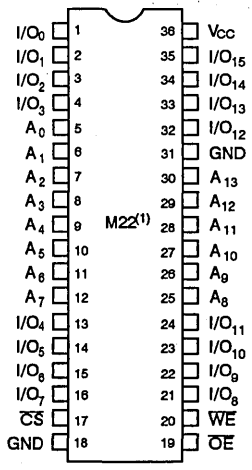
The IDT7MC4005 is a 16-bit wide 256K (16K x 16) static RAM module constructed on a co-fired ceramic substrate using four IDT7198 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology. The IDT7MC4005 is available with access times as fast as 20ns, with minimal power consumption.

The IDT7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4005 is packaged in a 36-pin ceramic DSIP (dual single-in-line package). The dual row configuration allows 36 pins to be placed on a package 1.8 inches long and .27 inches wide. At only .500 inches high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved, allowing four IDT7MC4005 modules to be stacked per 1.2 inches of board space.

All inputs and outputs of the IDT7MC4005 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

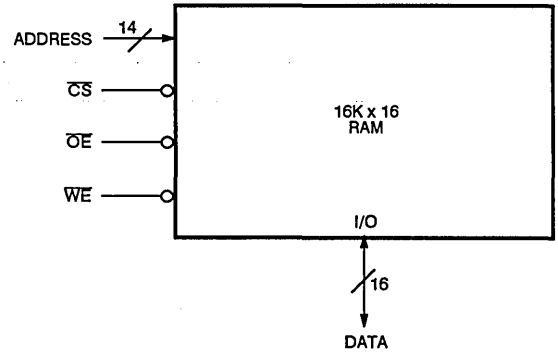
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M22 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O_{0-15}	Data Inputs/Outputs
A_{0-13}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN.	MILITARY MAX.	COMMERCIAL MIN.	COMMERCIAL MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	40	–	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4005 20ns COM'L.	IDT7MC4005 20ns MIL.	IDT7MC4005 25ns COM'L.	IDT7MC4005 25ns MIL.	IDT7MC4005 30, 35, 45, 55ns COM'L.	IDT7MC4005 30, 35, 45, 55ns MIL.	UNIT
I_{CC1}	Operating Current	F = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	480	–	480	500	400	440	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	600	–	600	620	500	560	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IL}	240	–	240	240	200	220	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or <0.2V	80	–	80	80	60	80	mA

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7MC4005S20 (COM'L)		7MC4005S25		7MC4005S30		7MC4005S35		7MC4005S45		7MC4005S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	15	–	20	–	20	–	25	–	35	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	–	8	–	10	–	13	–	15	–	15	–	20	ns
t_{OHZ}(1)	Output Disable to Output In High Z	–	8	–	15	–	15	–	15	–	15	–	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	17	–	20	–	25	–	30	–	40	–	50	–	ns
t_{CW}	Chip Selection to End of Write	17	–	20	–	25	–	25	–	35	–	50	–	ns
t_{AW}	Address Valid to End of Write	17	–	20	–	25	–	27	–	37	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	2	–	2	–	2	–	ns
t_{WP}	Write Pulse Width	17	–	20	–	25	–	25	–	35	–	48	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	7	–	7	–	10	–	10	–	15	–	25	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	15	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

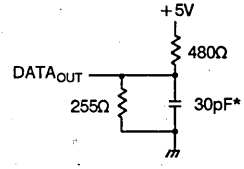


Figure 1. Output Load

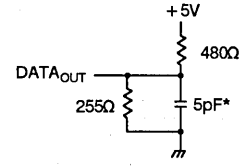
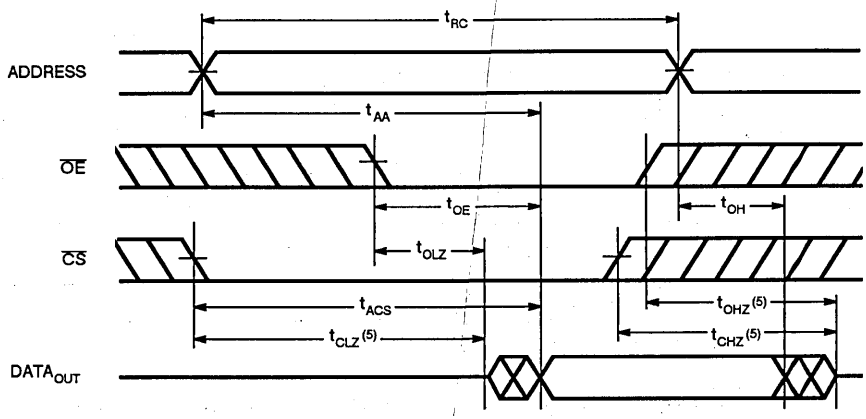


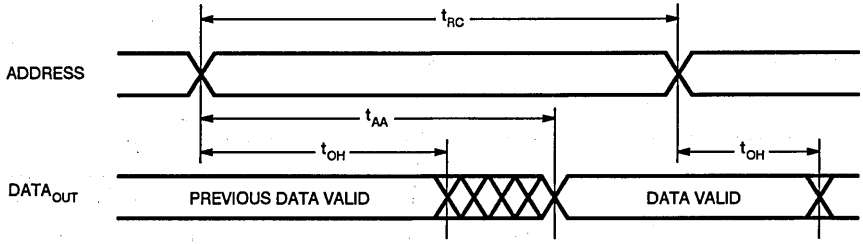
Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

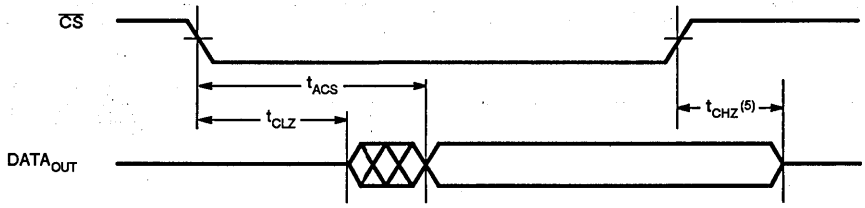
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



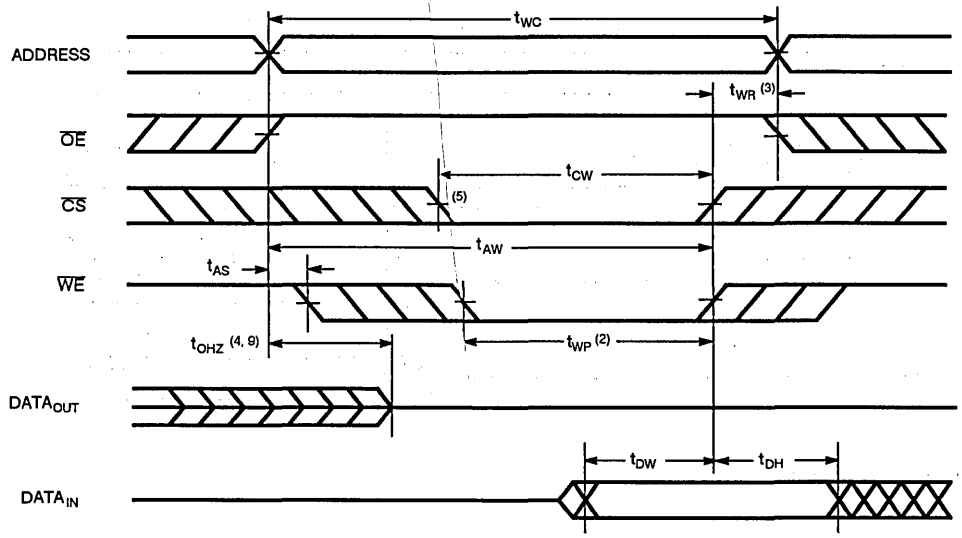
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



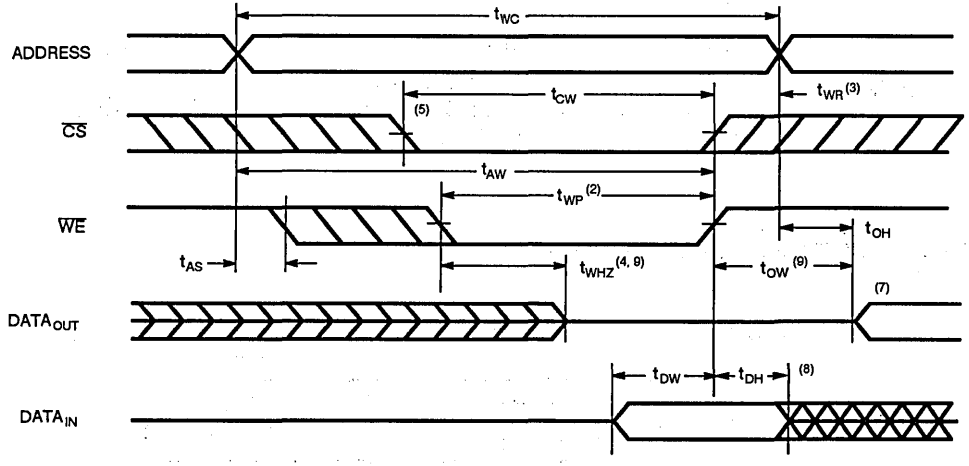
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WP} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active
Read	L	H	H	High Z	Active

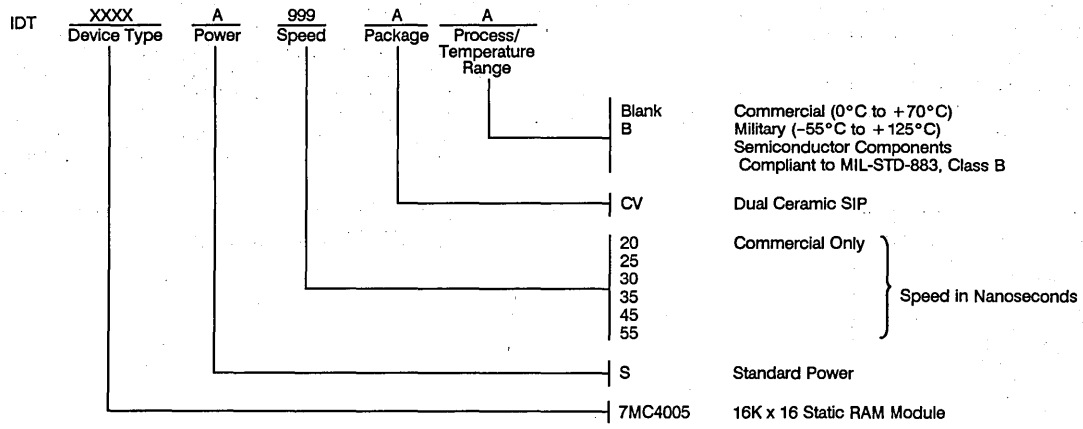
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN\ (D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN\ (A)}$	Input Capacitance Address and Control	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:

1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

64K x 6 CMOS STATIC RAM CERAMIC SIP MODULE WITH SEPARATE DATA I/O

IDT 7MC4018

FEATURES:

- High-density 64K x 6 CMOS static RAM module
- Separate data inputs and outputs
- Configurable as 64K x 18 using 3 modules
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 40-pin ceramic SIP (single in-line package) for maximum space saving
- Fast access times: 20ns (max.) over commercial temperature
- Low power consumption
- Utilizes IDT7187s, high-performance 64K static RAMs, produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7MC4018 is a 64K x 6-bit high-speed static RAM module constructed on a co-fired ceramic substrate using six IDT7187 64K x 1 static RAMs in surface mount packages.

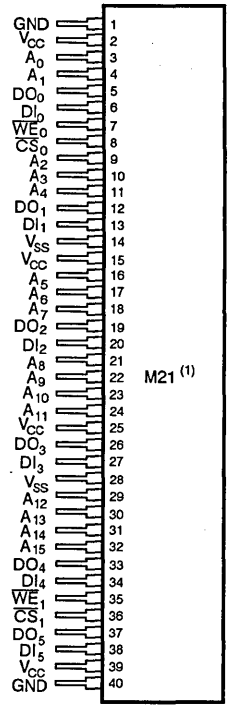
The 7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4018 is offered in a 40-pin ceramic SIP (single in-line package). At only 360 mils high, this low profile package is ideal for systems with minimal board spacing. Surface mount SIP technology also yields very high packing density, allowing five IDT7MC4018 modules to be stacked per inch of board space.

The IDT7MC4018 is available with maximum access times as fast as 20ns. Separate data inputs and outputs are supplied for high-performance systems. Three modules can be configured to yield 64K x 18, which is ideal for 16-bit systems with 2 parity bits.

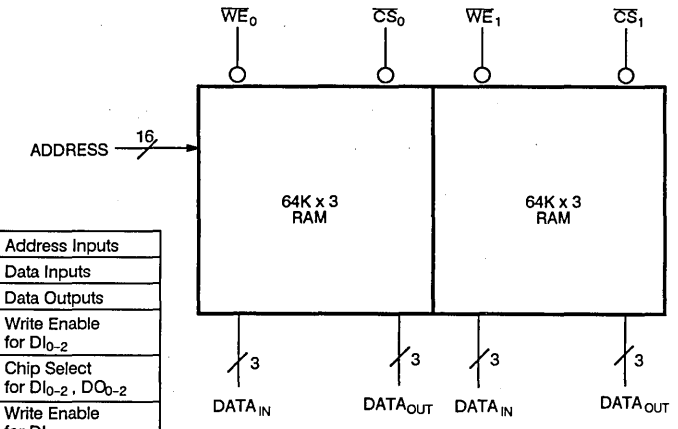
All inputs and outputs of the IDT7MC4018 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal chip select and access times for ease of use.

All IDT military module components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{15}$	Address Inputs
$DI_0 - DI_5$	Data Inputs
$DO_0 - DO_5$	Data Outputs
$\overline{WE}_0$	Write Enable for DI_{0-2}
$\overline{CS}_0$	Chip Select for DI_{0-2}, DO_{0-2}
$\overline{WE}_1$	Write Enable for DI_{3-5}
$\overline{CS}_1$	Chip Select for DI_{3-5}, DO_{3-5}
V_{CC}	Supply Voltage
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M21 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	30	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	30	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT7MC4018				UNIT
			MAX.(1)		MAX.(2)		
			COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Current	F = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	720	–	540	630	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; F = F_{MAX} Output Open	900	–	660	720	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IL}	360	–	270	300	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or < 0.2V	120	–	90	120	mA

NOTES:

1. 20, 25ns
2. 30, 35, 45, 55ns

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AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	7MC4018S20 COM'L. ONLY		7MC4018S25 COM'L. ONLY		7MC4018S30		7MC4018S35		7MC4018S45		7MC4018S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	35	–	45	–	55	–	ns
t_{CHZ} (1)	Chip Deselect to Output In High Z	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{WC}	Write Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	20	–	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	20	–	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

NOTE:

1. This parameter guaranteed but not tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

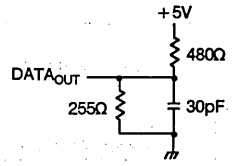


Figure 1. Output Load

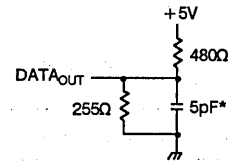
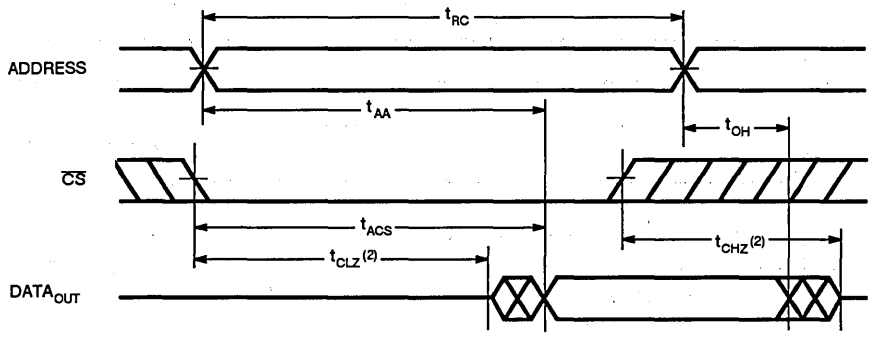


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

TIMING WAVEFORM OF READ CYCLE (1)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Transition is measured ± 200mV from steady state. This parameter is sampled and not 100% tested.

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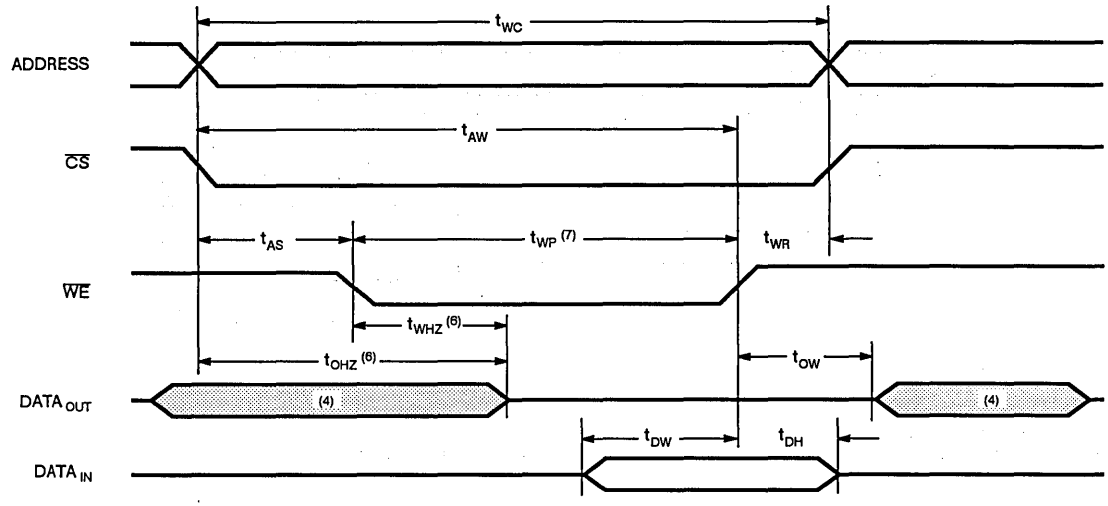
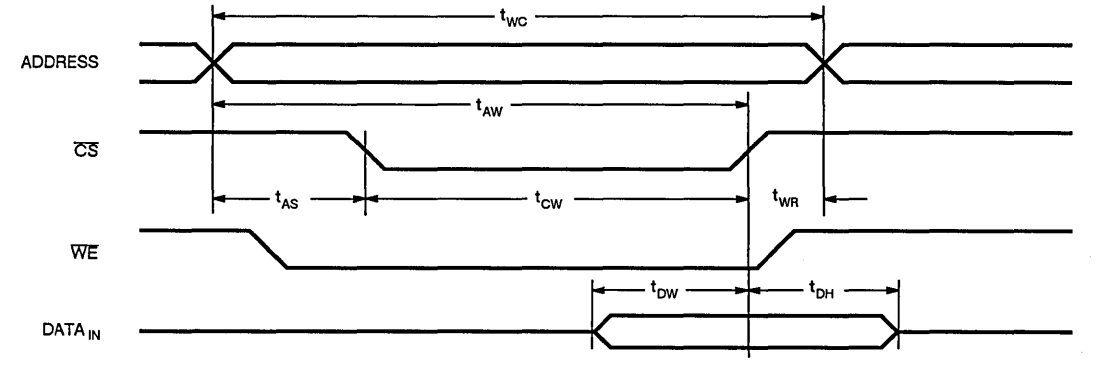
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TRUTH TABLE

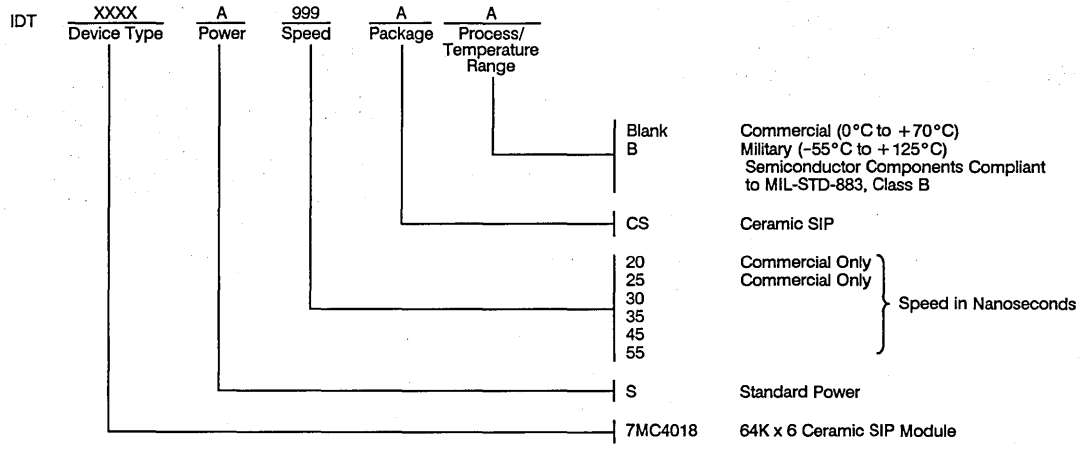
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN\ (D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN\ (A)}$	Input Capacitance Address and Control	V_{IN} = 0V	60	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



13

Integrated Device Technology, Inc.

512K (16K x 32) CMOS STATIC RAM DUAL CERAMIC SIP MODULE

IDT 7MC4032

FEATURES:

- High-density 32-bit word 512K (16K x 32) static RAM module
- Available in low profile 88-pin sidebraze dual ceramic SIP (dual single in-line package)
- Separate I/O
- Fast access time: 20ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- High impedance outputs during write mode
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

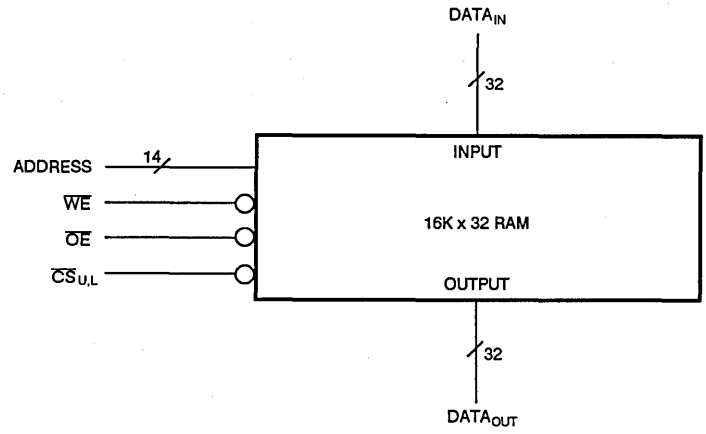
The IDT7MC4032 is a 32-bit wide 512K (16K x 32) static RAM module with separate I/O constructed on a co-fired ceramic substrate using eight IDT71982 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The IDT7MC4032 is available with access time as fast as 20ns, with minimal power consumption.

The 7MC family of ceramic SIPs offers the optimum is packing density and profile height. The IDT7MC4032 is packaged in a 88-pin dual ceramic SIP. The dual row configuration allows 88 pins to be placed on a package less than 4.5 inches long and .27 inches wide. At only 520 mils high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved allowing four IDT7MC4032 modules to be stacked per inch of board space.

All inputs and outputs of the IDT7MC4032 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

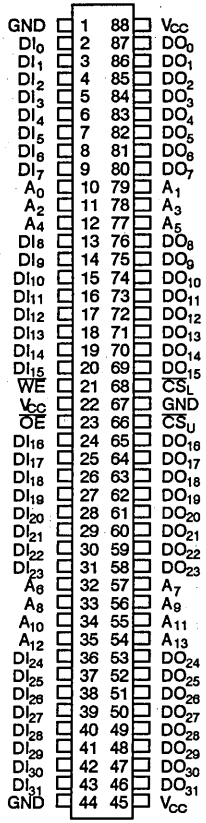
All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION [1]



PIN NAMES

A_{0-13}	Addresses
DI_{0-31}	Data Input
DO_{0-31}	Data Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}_L$	Chip Select (Lower)
$\overline{CS}_U$	Chip Select (Upper)
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M23 in the packaging section.

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4032 20ns MAX. COM'L.	IDT7MC4032 20ns MAX. MIL.	IDT7MC4032 25ns MAX. COM'L.	IDT7MC4032 25ns MAX. MIL.	IDT7MC4032 30, 40, 50, 70ns MAX. COM'L.	IDT7MC4032 30, 40, 50, 70ns MAX. MIL.	UNIT
I_{CC1}	Operating Current	F = 0, $\overline{CS}$ = V_{IL} V_{CC} = MAX; Output Open	960	–	960	1000	800	800	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = MAX; $\overline{CS}$ = V_{IL}; F = F_{MAX} Output Open	1200	–	1200	1200	1000	1120	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IL}	480	–	480	480	400	440	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or <0.2V	160	–	160	160	120	160	mA

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	7MC4032S20 COM'L. ONLY MIN.	MAX.	7MC4032S25 MIN.	MAX.	7MC4032S30 MIN.	MAX.	7MC4032S40 MIN.	MAX.	7MC4032S50 MIN.	MAX.	7MC4032S70 MIL. ONLY MIN.	MAX	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	30	–	40	–	50	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	–	40	–	50	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30	–	40	–	50	–	70	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	15	–	20	–	22	–	30	–	45	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	8	–	10	–	13	–	17	–	18	–	25	ns
t_{OHZ} (1)	Output Disable to Output in High Z	–	8	–	15	–	17	–	17	–	18	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	20	–	25	–	30	–	40	–	50	–	70	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	17	–	20	–	25	–	35	–	45	–	65	–	ns
t_{CW}	Chip Selection to End of Write	17	–	20	–	25	–	28	–	38	–	62	–	ns
t_{AW}	Address Valid to End of Write	17	–	20	–	25	–	30	–	40	–	65	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	2	–	2	–	3	–	ns
t_{WP}	Write Pulse Width	17	–	20	–	25	–	28	–	38	–	62	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	7	–	7	–	10	–	12	–	17	–	30	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	15	–	17	–	23	–	30	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTE:

1. This parameter guaranteed but not tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

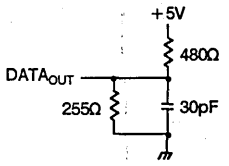

Figure 1. Output Load

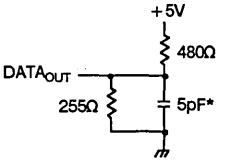

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

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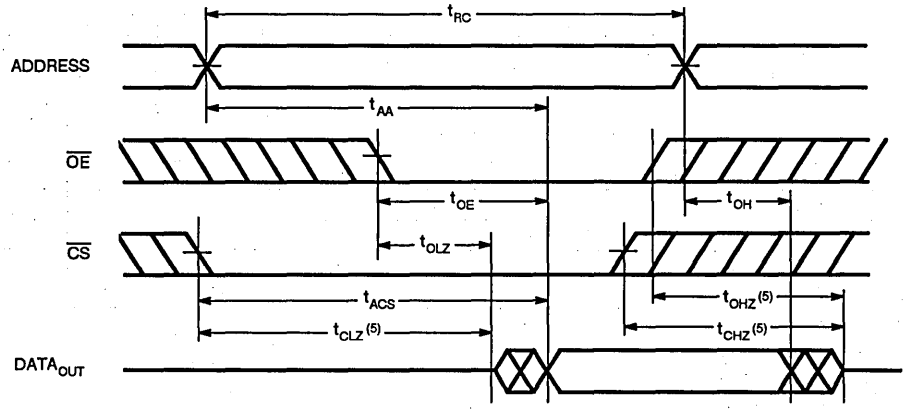
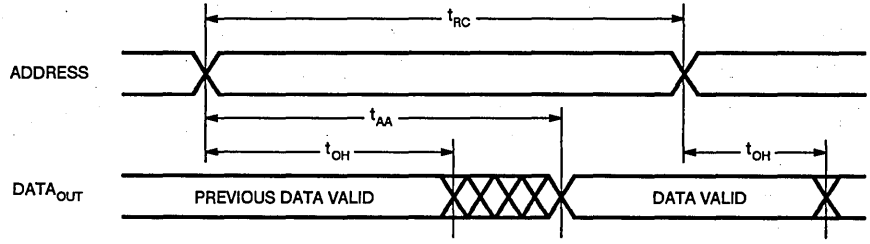
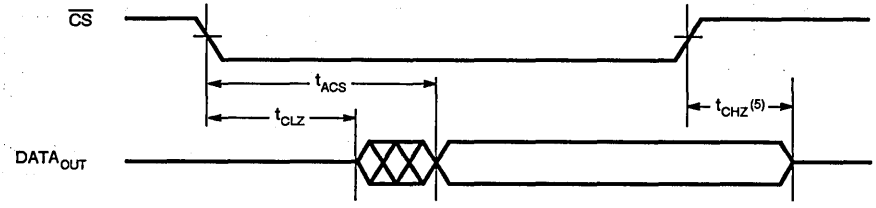
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



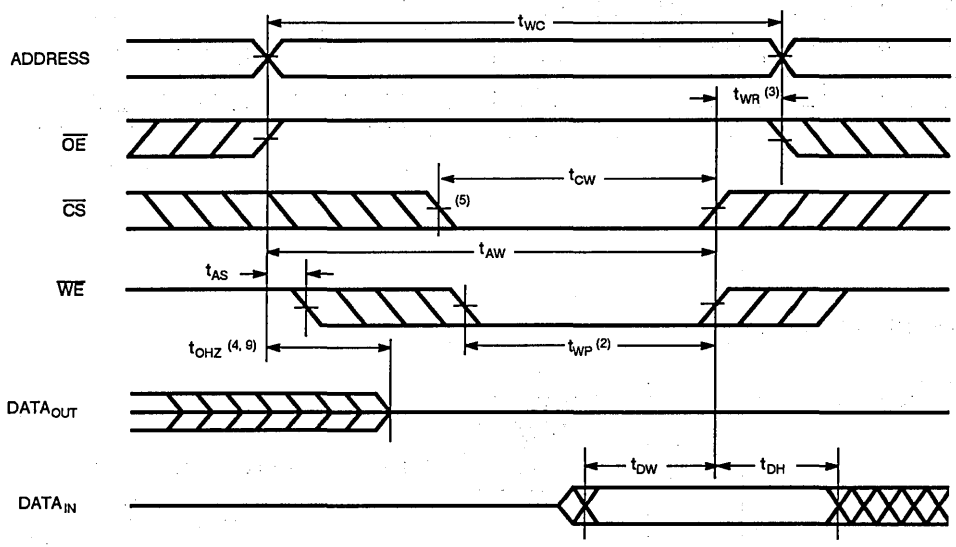
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



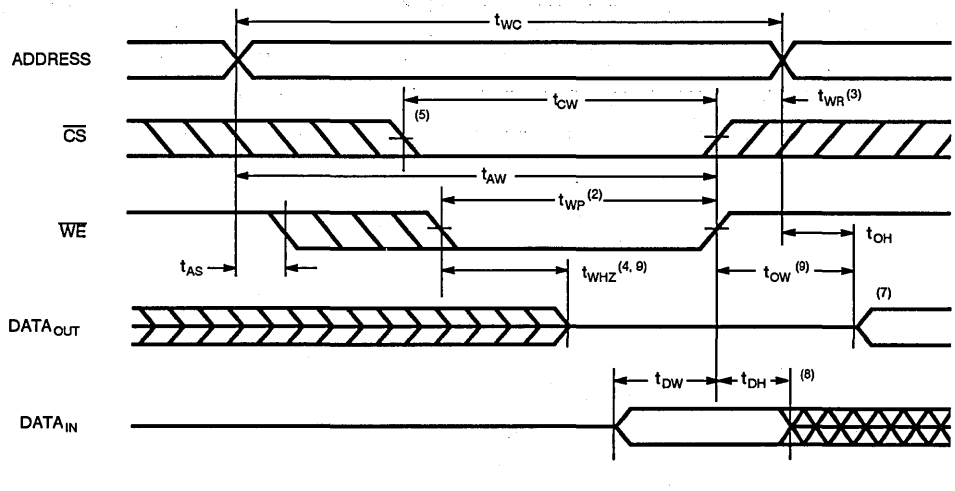
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

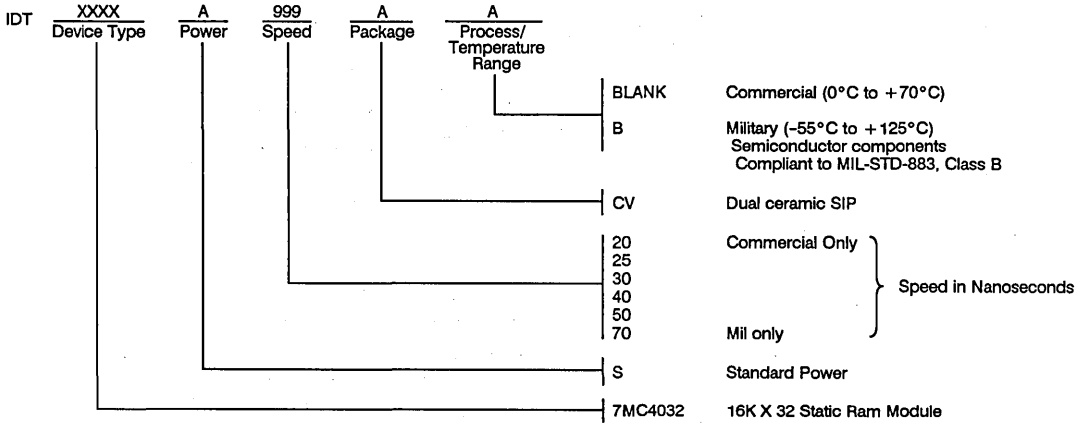
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active
Read	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}(D)	Input Capacitance	V_{IN} = 0V	15	pF
C_{IN}(A)	Output Capacitance Address and Control	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K (256K x 1-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT 7MP156

FEATURES:

- High-density 256K (256K x 1) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - Dynamic: less than 600mW (typ.)
  - Full standby: less than 30mW (typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION

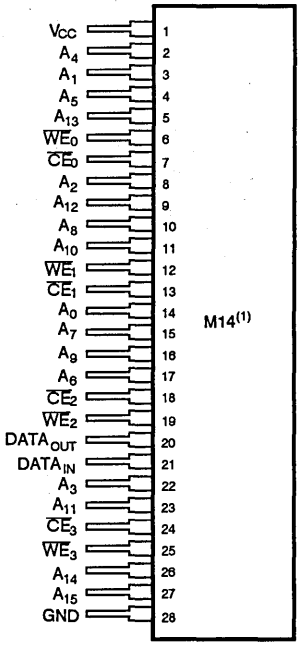
The IDT7MP156 is a 256K (256K x 1-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology.

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP156 is offered in a 28-pin SIP (single in-line package). The IDT7MP156 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP156 is available with maximum access times as fast as 25ns with maximum power consumption of 1.8 watts. The module also offers a full standby mode of 440mW (max.).

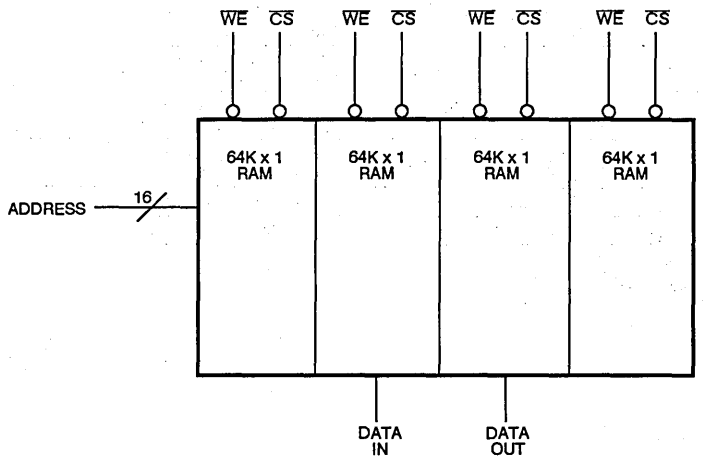
All inputs and outputs of the IDT7MP156 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Lines
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}_{0-3}$	Chip Enable
$\overline{WE}_{0-3}$	Write Enable
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, plese refer to module drawing M14 in the packaging section.

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP156 MIN.	TYP.(1)	MAX.(2)	MAX.(3)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0	–	110	225	300	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}	–	120	245	330	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max., Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	CS ≥ V_{HC}, V_{IN} ≥ V_{HC} or V_{LC} V_{CS} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C
2. t_{AA} = 35, 45, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

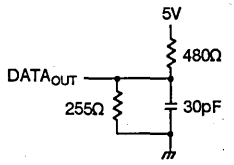


Figure 1. Output Load

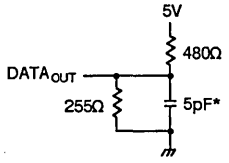


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to 70°C)

SYMBOL	PARAMETER	IDT7MP156S25 MIN.	MAX.	IDT7MP156S30 MIN.	MAX.	IDT7MP156S35 MIN.	MAX.	IDT7MP156S45 MIN.	MAX.	IDT7MP156S55 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

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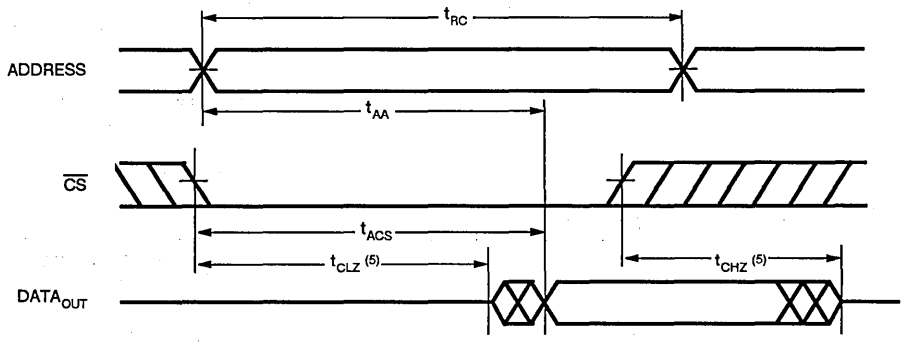
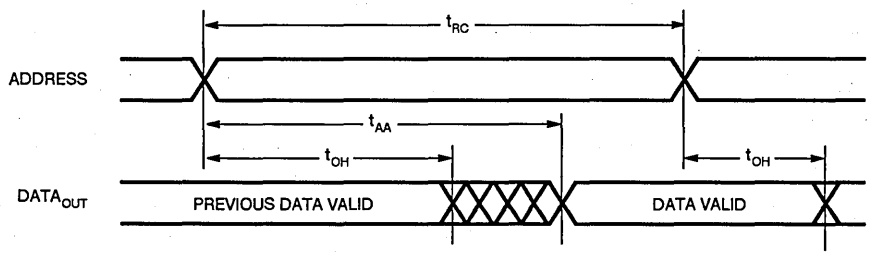
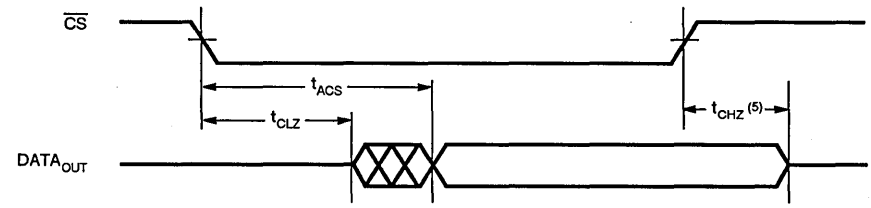
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



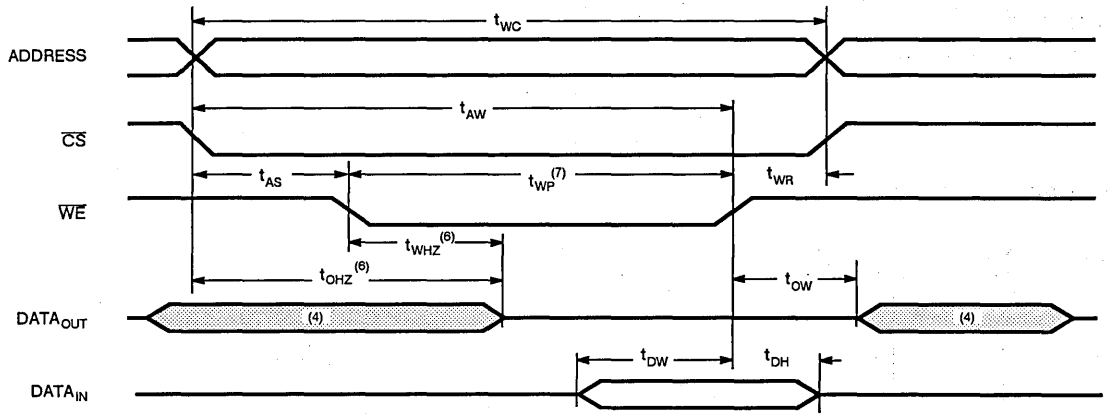
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



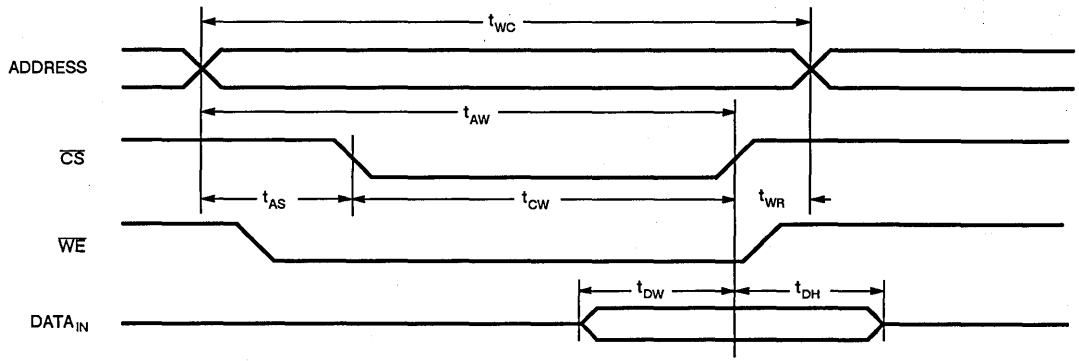
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



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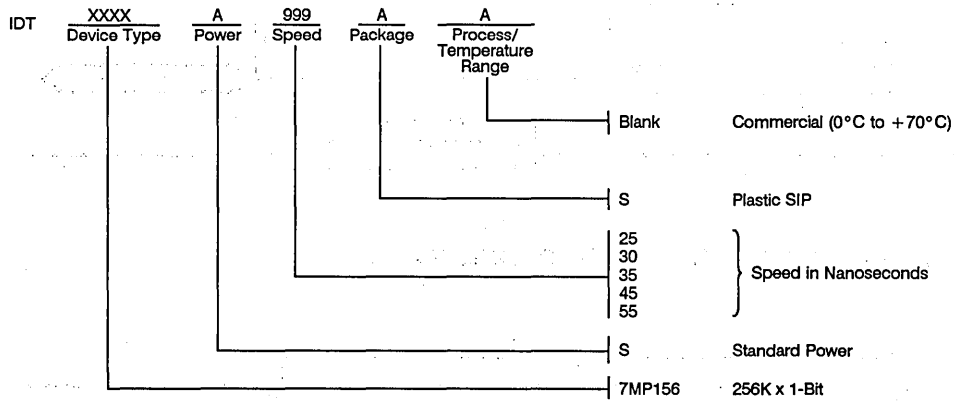
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K (64K x 4-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT 7MP456

FEATURES:

- High-density 256K (64K x 4) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - —Dynamic: less than 1.2W (typ.)
  - —Full standby: less than 30 mW(typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

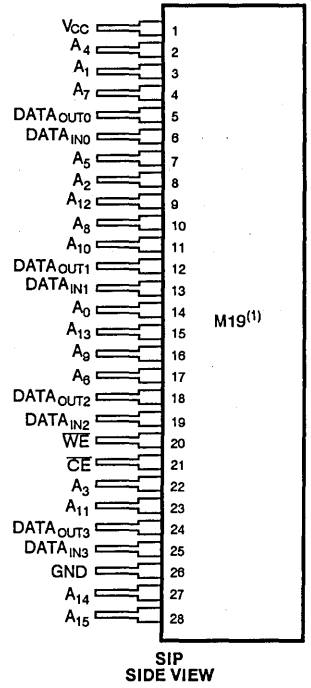
The IDT7MP456 is a 256K (64K x 4-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology .

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP456 is offered in a 28-pin SIP. The IDT7MP456 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP456 is available with maximum access times as fast as 25ns, with maximum power consumption of 3.3 watts. The module also offers a full standby mode of 440mW(max.).

All inputs and outputs of the IDTMP456 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION

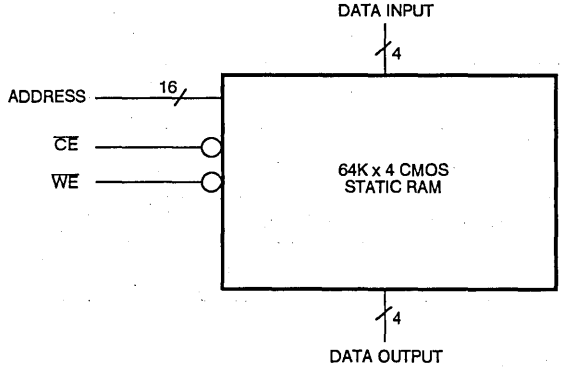


SIP
SIDE VIEW

NOTE:

1. For module dimensions, please refer to module drawing M19 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{15}	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
D_{IN0} – D_{IN3}	Data Input
D_{OUT0} – D_{OUT3}	Data Output
V_{CC}	Power
GND	Ground

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DSC-7007/1

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC}= 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP456 MIN.	TYP.(1)	MAX.(2)	MAX.(3)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open F = 0	–	180	360	480	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	240	440	600	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max. Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, t_{AA} = 25°C
2. t_{AA} = 35, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

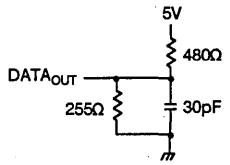

Figure 1. Output Load

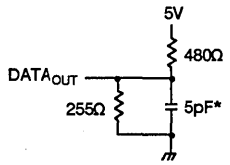

Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP456S25 MIN.	MAX.	IDT7MP456S30 MIN.	MAX.	IDT7MP456S35 MIN.	MAX.	IDT7MP456S45 MIN.	MAX.	IDT7MP456S55 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:

1. This parameter guaranteed but not tested.

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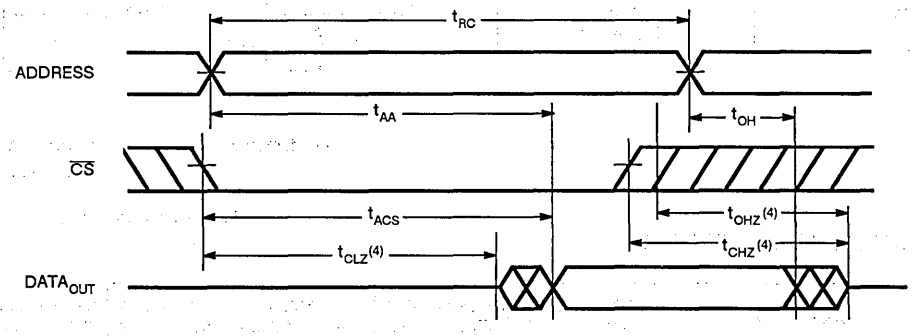
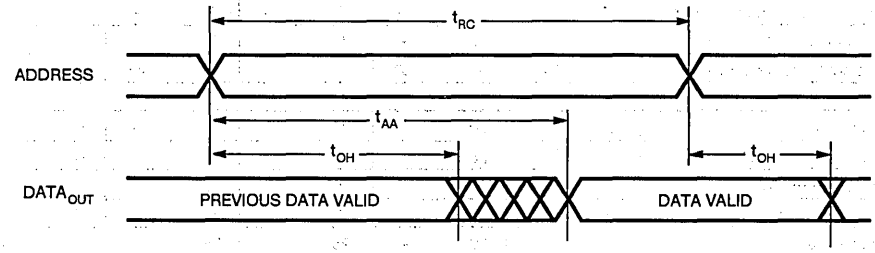
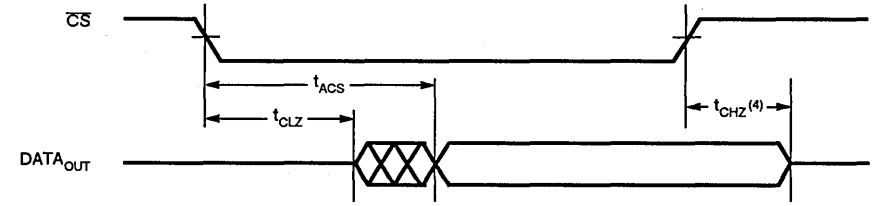
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



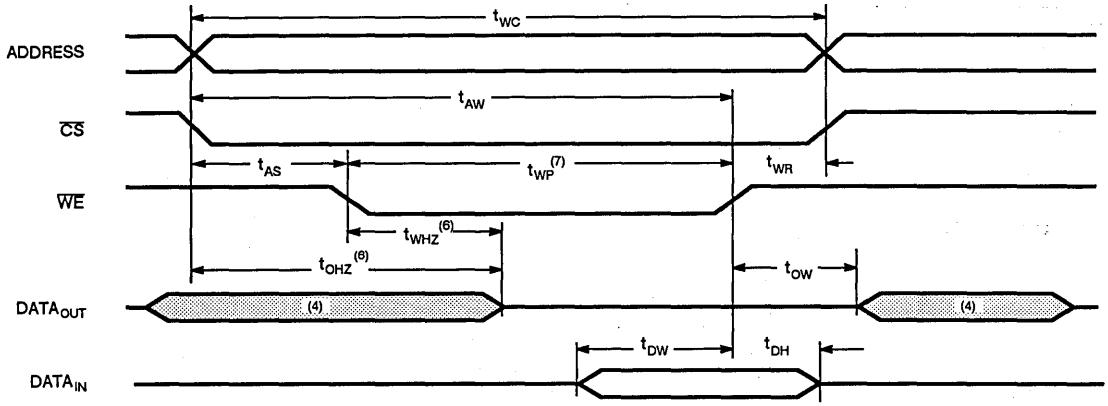
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3)



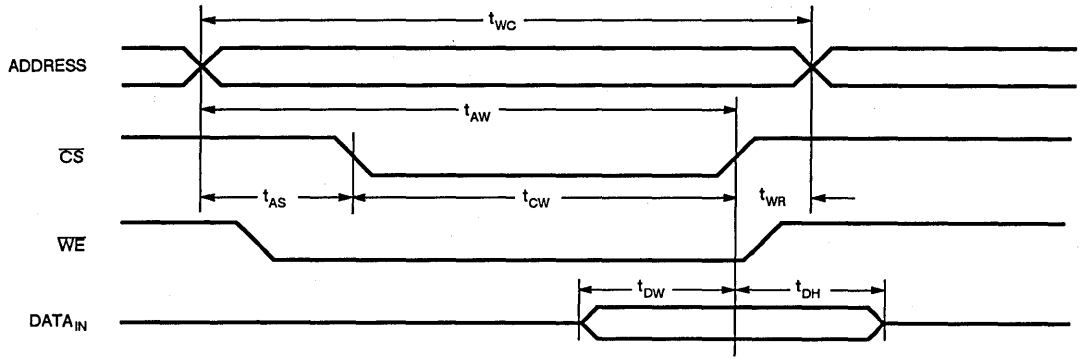
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} .
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

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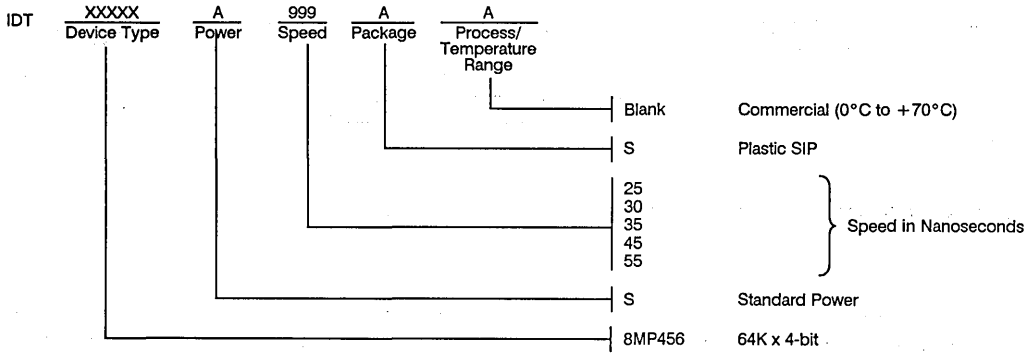
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

4 MEGABIT (512K x 8-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT 7MP4008L

FEATURES:

- High-density 4096K (512K x 8) CMOS static RAM module
- Access time
  - 70ns (max.)
- Low power consumption
  - Dynamic: less than 910mW (max.)
  - Full standby: less than 430mW (max.)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in a 36-pin SIP (single in-line package) for maximum space-saving
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

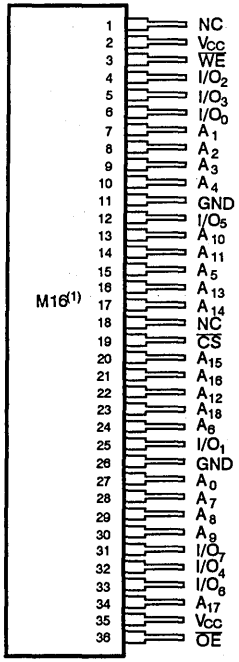
The IDT7MP4008L is a 4096K (512K x 8-bit) high-speed static RAM module constructed on an epoxy laminate surface using sixteen 32K x 8 static RAMs in plastic surface mount packages.

The IDT7MP4008L is available with maximum access times as fast as 70ns, with maximum operating power consumption of 910mW. The module also offers a full standby mode of 430mW (max.).

The IDT7MP4008L is offered in a 36-pin SIP (single in-line package). Surface mount SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP4008L can be stacked on 300 mil centers, yielding greater than 12 Megabits of memory per inch of board space.

All inputs and outputs of the IDT7MP4008L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

PIN CONFIGURATION

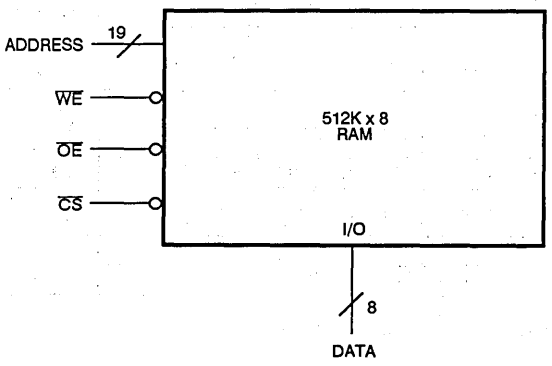


SIP
SIDE VIEW

NOTE:

1. For module dimensions, please refer to moudle drawing M16 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-18}	Addresses
I/O_{0-7}	Data Input/Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Power
GND	Ground
NC	No Connect

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	0.3V	–	0.8	V

NOTE:

1. V_{IL} (min.) = -2.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP4008L MIN.	IDT7MP4008L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	40	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = 0	–	90	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	165	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}	–	78	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ > V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	–	78	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA, V_{CC} = Min.	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1mA, V_{CC} = Min.	2.4	—	V

NOTE:

1. $|I_{LI}|$ for A_{15} – A_{18} and $\overline{MS}$ is 400 µA max.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

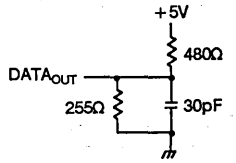

Figure 1. Output Load

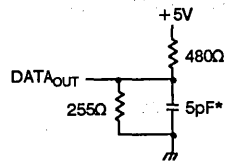

Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETERS	7MP4008L70 MIN.	7MP4008L70 MAX.	7MP4008L85 MIN.	7MP4008L85 MAX.	7MP4008L100 MIN.	7MP4008L100 MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Time	70	–	85	–	100	–	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	ns
t_{ACS}	Chip Select Access Time	–	70	–	85	–	100	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	10	–	10	–	10	–	ns
t_{OE}	Output Enable to Output Valid	–	40	–	50	–	60	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	–	40	–	40	–	50	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	30	–	35	–	40	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	70	–	85	–	100	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	70	–	85	–	100	–	ns
t_{CW}	Chip Selection to End of Write	65	–	75	–	90	–	ns
t_{AW}	Address Valid to End of Write	65	–	75	–	90	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns
t_{WR}	Write Recovery Time	5	–	10	–	10	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	30	–	35	–	40	ns
t_{DW}	Data Valid to End of Write	30	–	35	–	45	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	ns

NOTE:

1. This parameter is guaranteed but not tested.

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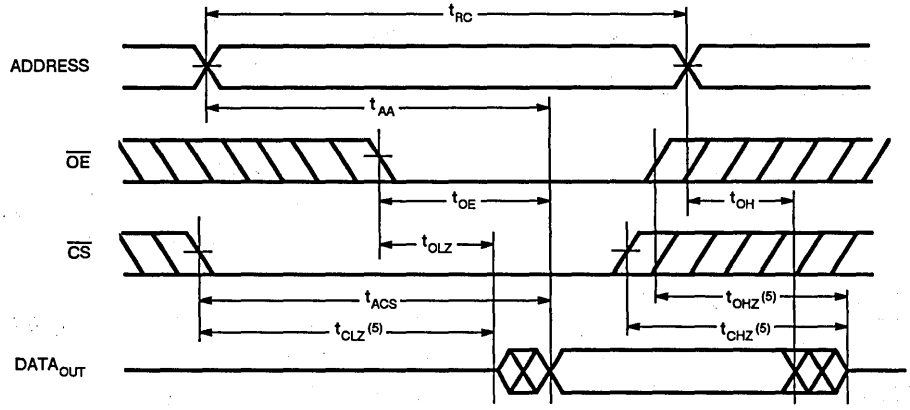
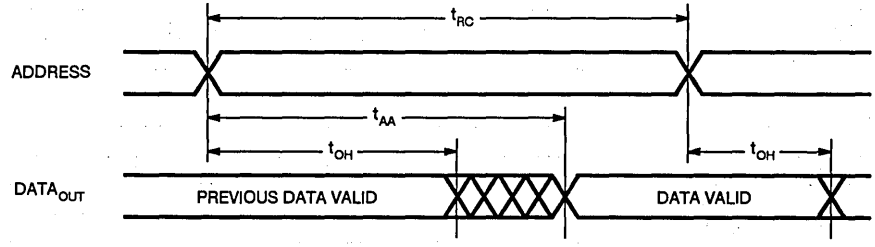
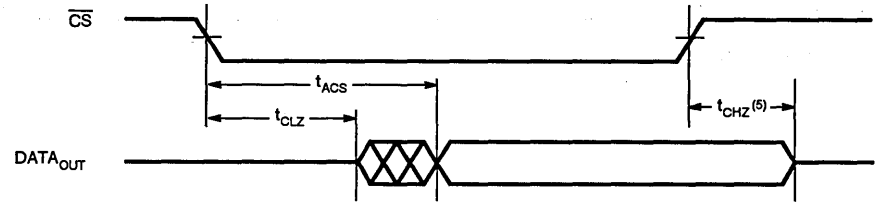
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



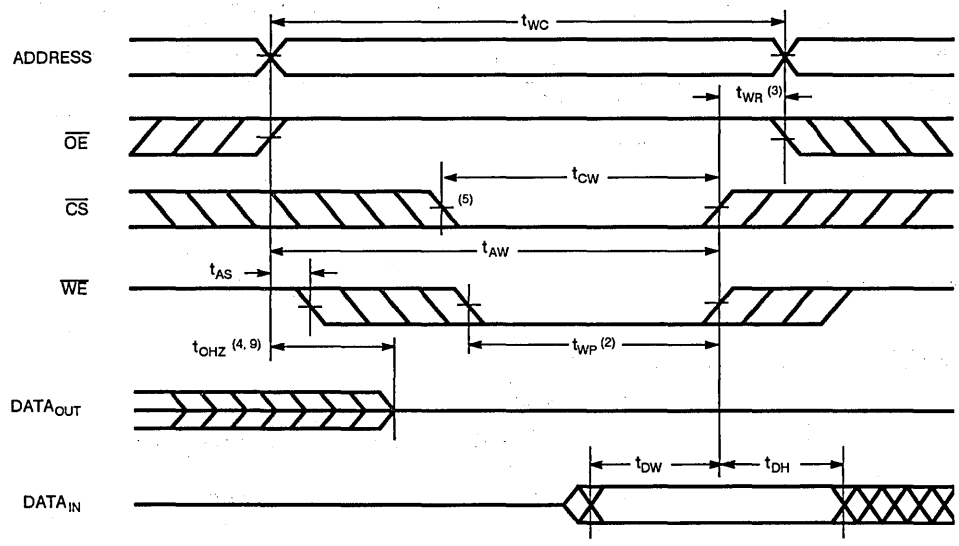
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



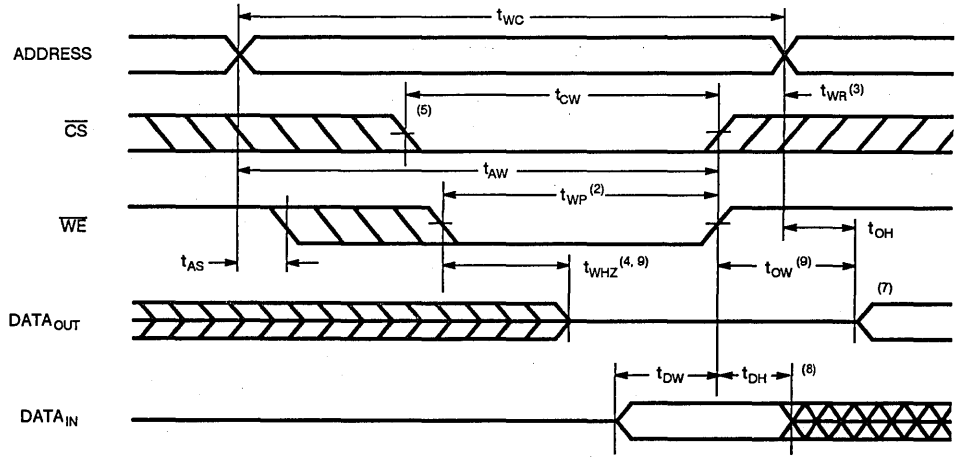
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

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TRUTH TABLE

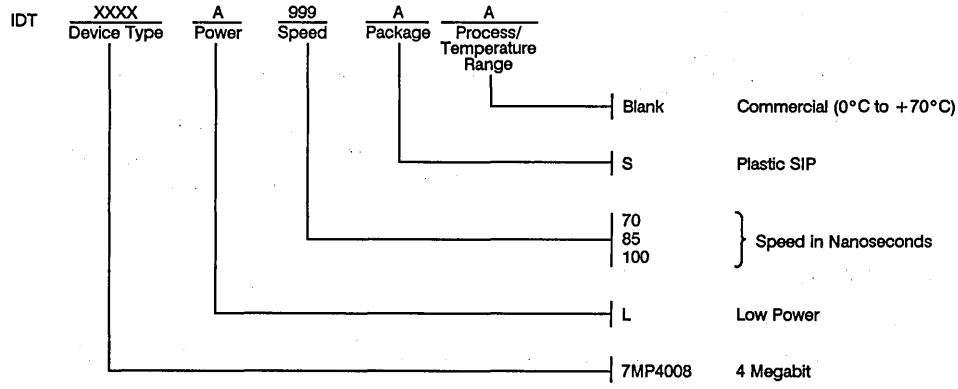
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	36	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	128	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



Integrated Device Technology, Inc.

512K (64K x 8) SYNCHRONOUS STATIC RAM PLASTIC SIP MODULE

IDT 7MP6025

FEATURES:

- 64K x 8 fully synchronous memory
- High-speed—20MHz read cycle time
- 16-bit synchronous address input
- 8-bit synchronous data input
- Synchronous chip select and write enable
- Separate clock enable for each register
- Low standby power
- Onboard decoupling capacitors
- Available in 43-pin SIP (single in-line package) configuration
- 2 Ground and 2 V_{CC} pins

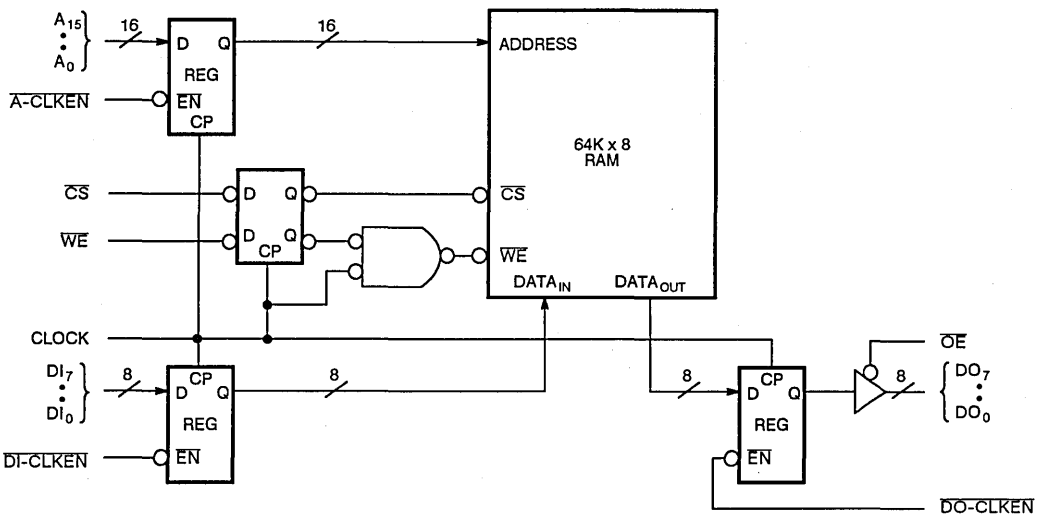
DESCRIPTION:

The IDT7MP6025 is a 64K x 8 synchronous RAM with edge triggered registers on the address lines, data-in bus, data-out bus, chip select and write enable. The edge triggered register of the 16 address lines features an independent clock enable that allows the address register to be selectively loaded. The address register will be loaded on the low-to-high transition of the clock when the clock enable line is low and will hold its current contents on the low-to-high transition of the clock when the clock enable is high. Similarly, the 8-bit data-in register will be loaded with new data on the low-to-high transition of the clock when the data-in clock enable is low and will hold its contents when the data-in clock enable is high. The data-out register will receive new data from the 64K x 8 RAM when the clock enable line is low and will hold its data when the clock enable line is high at the low-to-high transition of the clock. All clock enables, as well as address and data inputs, must meet the appropriate set-up and hold times with respect to the clock.

The eight data output bits are enabled when the output enable is low and are in the high-impedance state when the output enable is high. The chip select and write enable signals are also registered in D flip-flops. These two flip-flops are loaded with new data on each low-to-high transition of the clock. The chip select is passed directly from the Q output of the D-type flip-flop to the 64K x 8 RAM. The write enable signal is gated with the clock signal to generate a delayed write enable pulse. In essence, this gives the output of the address register time to settle and internally select the appropriate byte of RAM before the write enable goes low to write new data into the RAM. Thus, the low-to-high transition of the clock causes the chip select and write enable flip-flops to be loaded with new data and immediately deselects a previous write by means of the clock going high. The data lines to the RAM and the address lines to the RAM may indeed change to new values based on the low-to-high transition of the clock. When the clock goes from high-to-low, if the chip select is low and the write enable is low, a write cycle is begun and the data at the RAM data inputs will be written into the selected address. If the write enable is high or the chip enable is high, data will not be written into the memory.

One of the features of this configuration of memory that has registers on all of the address lines, data input lines and data output lines as well as the control lines, is to provide the highest possible clock rate in the system. All that is necessary is that the data, address, chip select, write enable and clock enables signals meet the required set-up and hold time with respect to the clock. In this manner, fully asynchronous operation is achieved. The IDT7MP6025 is offered as a compact, cost-effective 43-pin plastic SIP module.

FUNCTIONAL BLOCK DIAGRAM



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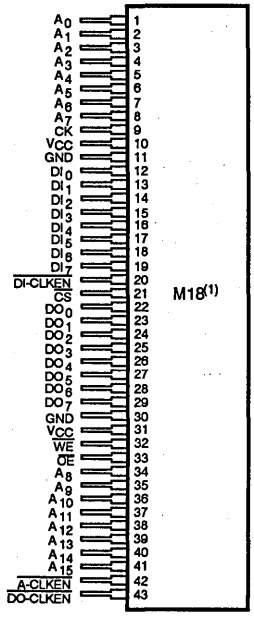
PIN CONFIGURATION



SIP
SIDE VIEW

NOTE:

1. For module dimension, please refer to module drawing M18 in the packaging section.

PIN NAMES

A_{0-15}	Addresses
CK	Clock
DI_{0-7}	Data Input
DO_{0-7}	Data Output
$\overline{DI\text{-}CLKEN}$	Data Input Clock Enable
$\overline{A\text{-}CLKEN}$	Address Clock Enable
$\overline{DO\text{-}CLKEN}$	Data Output Clock Enable
V_{CC}	Power
GND	Ground
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	COMMERCIAL	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{OUT}, V_{OUT} = GND to V_{CC}	–	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	MAX.	UNIT
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max.; Output Open	725	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}.; f = $f_{MAX.}$ Output Open	950	mA
I_{SB1}	Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or < 0.2V	125	mA

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE:

1. This parameter is sampled and not 100% tested.

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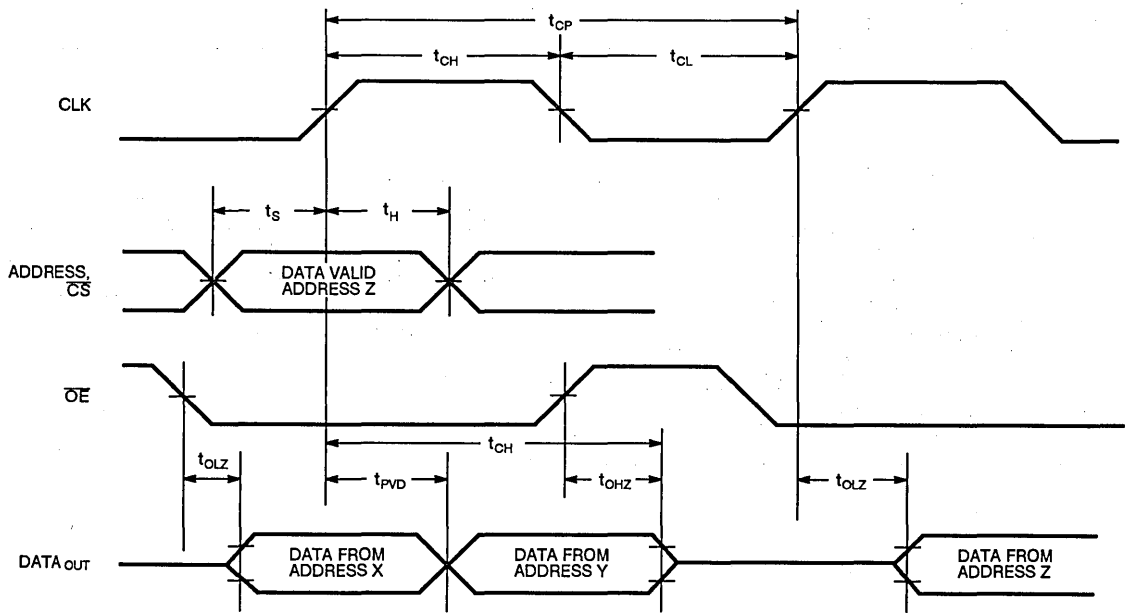
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%

SYMBOL	PARAMETER	7MP6025S35		7MP6025S45		7MP6025S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t_{CP}	Read Cycle Time	35	–	45	–	55	–	ns
t_{CH}	Clock High Time	10	–	10	–	10	–	ns
t_{CL}	Clock Low Time	10	–	10	–	10	–	ns
t_S	Address, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Set Up Time	4	–	5	–	5	–	ns
t_H	Address, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Hold Time	4	–	6	–	6	–	ns
t_{OLZ} (1)	Output Low Z Time	–	10	–	15	–	15	ns
t_{OHZ} (1)	Output High Z Time	–	8	–	11	–	11	ns
t_{PVD}	Prop Delay to Valid Data Out	–	10	–	15	–	15	ns
WRITE CYCLE								
t_{CP}	Write Cycle Time	35	–	45	–	55	–	ns
t_{CH}	Clock High Time	10	–	10	–	10	–	ns
t_{CL}	Clock Low Time	23	–	30	–	37	–	ns
t_S	Data, Addr, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Set Up Time	4	–	5	–	5	–	ns
t_H	Data, Addr, $\overline{WE}$, $\overline{CS}$, $\overline{CE}$ Hold Time	4	–	6	–	6	–	ns

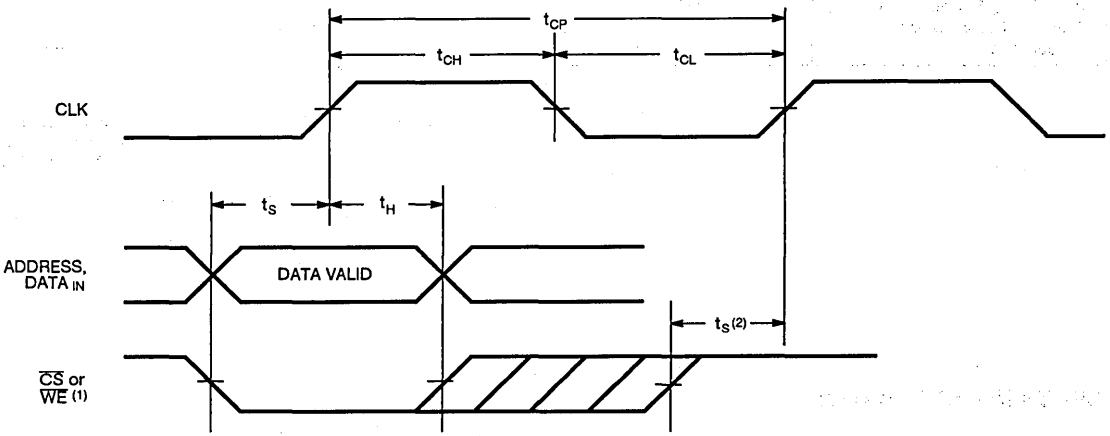
NOTE:
1. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE (1)



NOTE:
1. The device must be selected by a $\overline{CS}$ level for the conditions above to take place.

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. Either $\overline{CS}$ or $\overline{WE}$ can be used to trigger a write cycle, provided that the other signal is low at the same time.
2. When a write is terminated, either $\overline{CS}$ or $\overline{WE}$ must become high at least one t_S before the next rising edge of CLK.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	CK	$\overline{DO}$-CLKEN	$\overline{DI}$-CLKEN	$\overline{A}$-CLKEN	$\overline{WE}$	OUTPUT	POWER
Standby	H	H	↑	H	H	H	X	High Z	Standby
Read	L	L	↑	L	X	L	H	Low Z	Active
Read	L	H	↑	L	X	L	H	High Z	Active
Write	L	H	↑	H	L	L	L	High Z	Active

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

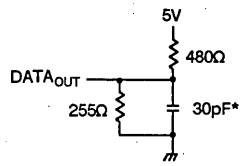


Figure 1. Output Load

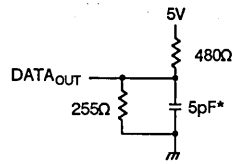
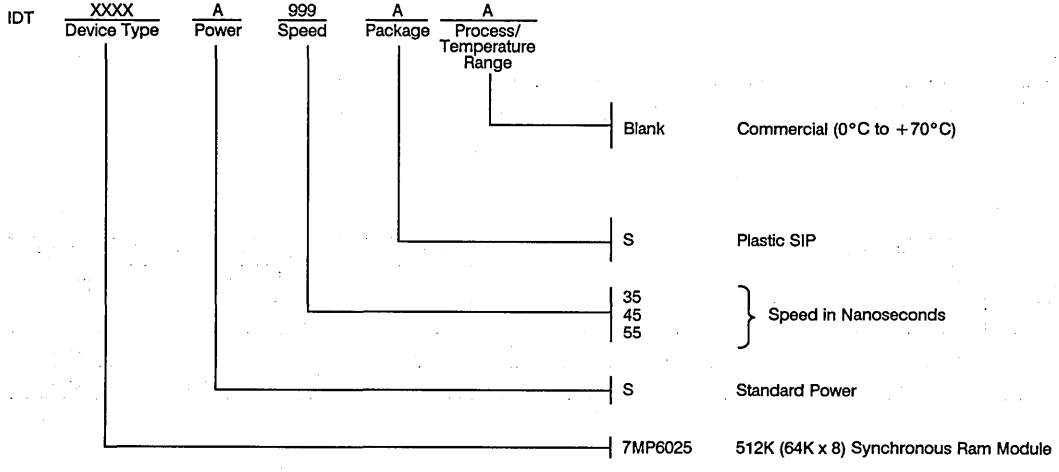


Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW})

* Including scope and jig.

ORDERING INFORMATION



Integrated Device Technology, Inc.

256K (16K x 16-BIT) & 128K (8K x 16-BIT) CMOS STATIC RAM PLASTIC SIP MODULES

IDT 8MP656S
IDT 8MP628S

FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656S) with 8K x 16 option (IDT8MP628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  - Flexibility in application
- Fast access times
  - 40ns (max.)
- Low power consumption
  - Active: less than 825mW (typ. in 16K x 16 organization)
  - Standby: less than 20mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in an SIP (single in-line) package for maximum space-savings
- Utilizes IDT7164s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8MP656S/IDT8MP628S are 256K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656S) or two IDT7164 static RAMs (IDT8MP628S) in plastic surface mount packages.

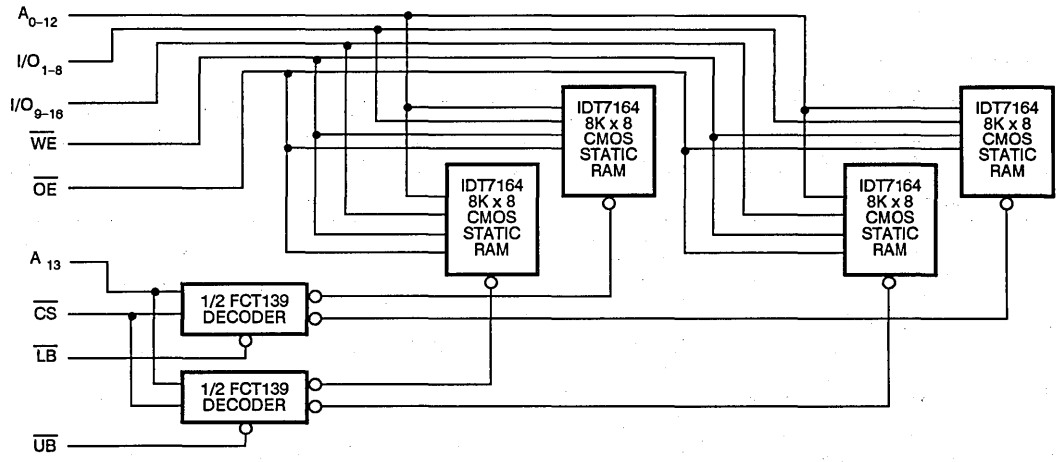
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP628S 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656S/IDT8MP628S are available with maximum operating power consumption of only 1.8W (IDT8MP656S 16K x 16 option). The modules also offer a full standby mode of 330mW (max.).

The IDT8MP656S/IDT8MP628S are offered in a 40-pin plastic SIP. For the JEDEC standard 40-pin DIP, refer to the IDT8M656S/IDT8M628S.

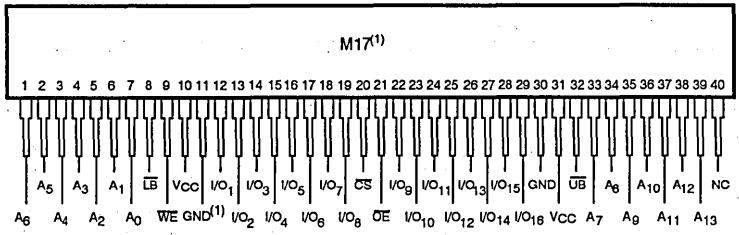
All inputs and outputs of the IDT8MP656S/IDT8MP628S are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



SIP
FRONT VIEW

NOTE:
1. For module dimensions, please refer to module drawing M17 in the packaging section.

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. On IDT8MP628S, 128K (8K x 16-Bit) option, A_{13}(Pin 39) is required external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 (1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8MP656S MIN.	IDT8MP656S TYP.	IDT8MP656S MAX.	IDT8MP628S MIN.	IDT8MP628S TYP.	IDT8MP628S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	–	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	–	–	15	µA
I_{CCX16}	Operating Current In X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	165	330	–	150	300	mA
I_{CCX8}	Operating Current In X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	100	200	–	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or UB ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	–	4	60	–	2	30	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	2.4	–	–	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

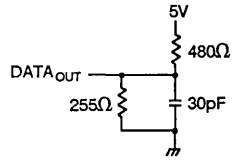


Figure 1. Output Load

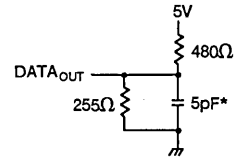


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETERS	IDT8MP656S40 IDT8MP628S40 MIN.	MAX.	IDT8MP656S50 IDT8MP628S50 MIN.	MAX.	IDT8MP656S70 IDT8MP628S70 MIN.	MAX.	IDT8MP656S85 IDT8MP628S85 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	40	–	50	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	40	–	50	–	70	–	85	ns
t_{ACS}	Chip Select Access Time	–	40	–	50	–	70	–	85	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	25	–	30	–	40	–	50	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	15	–	20	–	30	–	35	ns
t_{OHZ} (1)	Output Disable to Output in High Z	–	15	–	20	–	30	–	35	ns
t	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	40	–	50	–	70	–	85	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	40	–	50	–	70	–	85	–	ns
t_{CW}	Chip Selection to End of Write	5	–	45	–	65	–	75	–	ns
t_{AW}	Address Valid to End of Write	35	–	45	–	65	–	75	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	30	–	40	–	55	–	65	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	10	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	15	–	20	–	25	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

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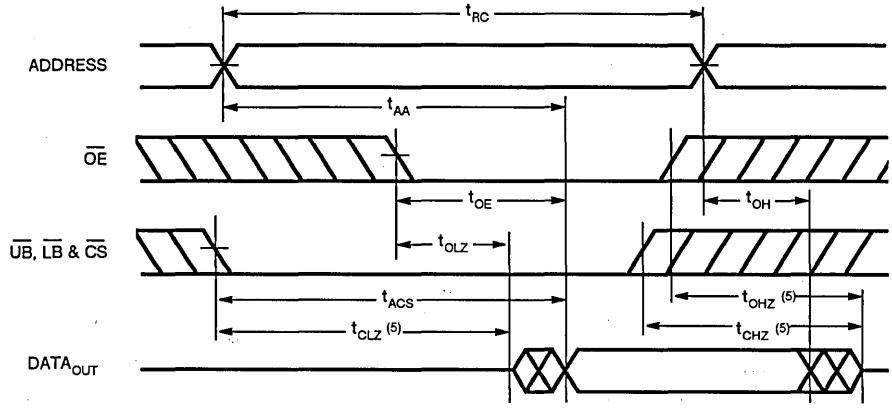
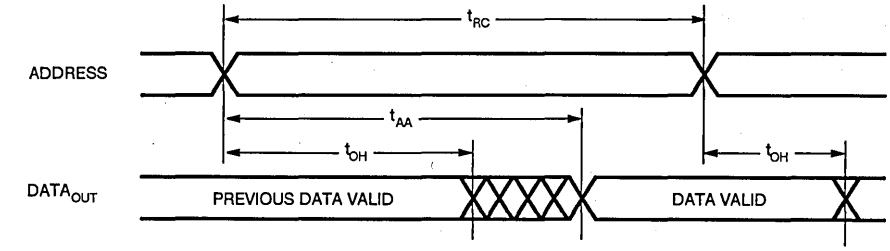
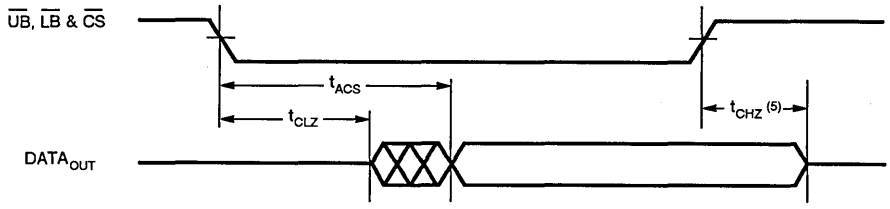
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



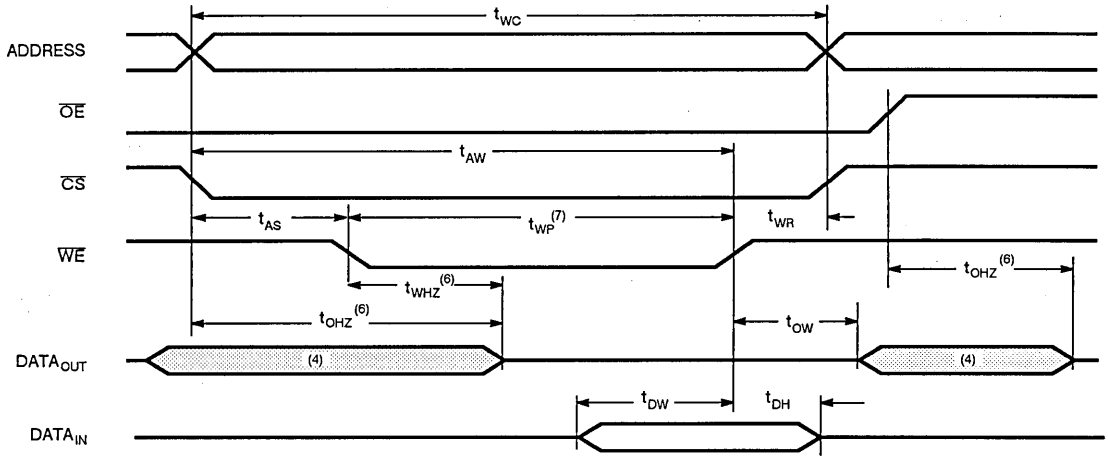
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



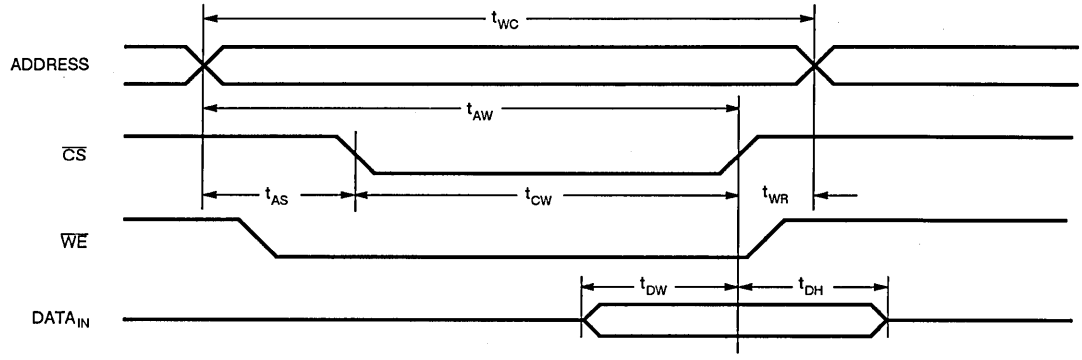
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



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NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse (t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

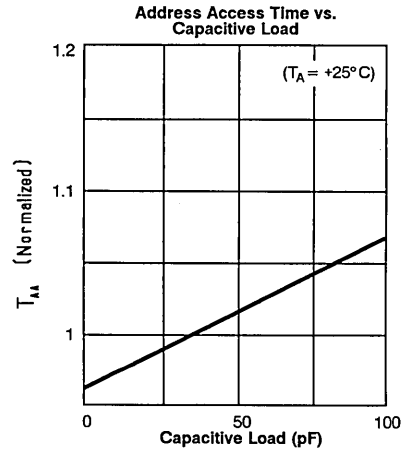
TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.



ORDERING INFORMATION

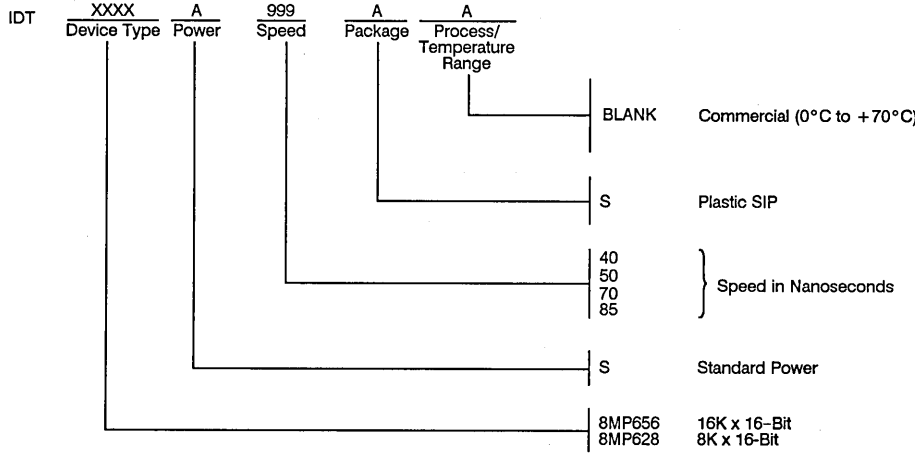


TABLE OF CONTENTS

Integrated Device Technology, Inc.

EXPAND YOUR IDT49C403

TECHNICAL NOTE TN-14

By Michael J. Miller

INTRODUCTION

One of the key features of the IDT49C403 that distinguishes it from other registered ALUs, such as the IDT49C402, is its 3-bus architecture which allows for flexibility expanding its function. This technote shows how the ALU can be expanded in an example employing a very high speed fixed point multiplier. The technote goes on to further demonstrate the flexibility of the IDT49C403 in an example expanding the register file using a 2K by 16 Dual Port RAM.

EXPANDING THE ALU

The IDT49C403 (Figure 1) is comprised of a 3-Port register file tightly coupled with an ALU. There are 3 data buses which go on and off this device – DA, DB, and Y. These are 16 bit buses and are bidirectional, each with its own output enable control, $\overline{OEA}$, $\overline{OEB}$, and $\overline{OEY}$ respectively. The onboard 64 location by 16 register file is capable of outputting two 16-bit words simultaneously, the contents of which are selected by the address buses A and B. Data is written back into the register file via the Y bus to the location identified by the B address bus. The Y bus is also connected to the output of the ALU.

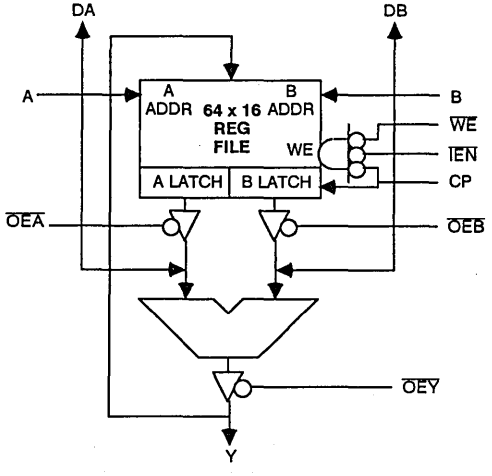


Figure 1. The IDT49C403 16-Bit Registered ALU

The flow of data in and out of the register file is controlled primarily by the system clock (CP). The output of the register file is put into two latches which hold the data constant through the write cycle. When the clock CP is HIGH, the register file is in the Read mode and the latches are transparent. When the clock is LOW the register file enters into a Write mode and the latches are closed, thus holding the data previously fetched during the Read portion of the cycle. Data is written when CP is LOW, the instruction enable $\overline{IEN}$ is LOW and the write enable $\overline{WE}$ is LOW.

The data from the latches travels through output buffers and onto the DA and DB buses as well as into the ALU. When $\overline{OEA}$ or $\overline{OEB}$ are LOW, data is supplied from the register file to the DA or DB bus and to the ALU. When either of these control lines are HIGH the respective data bus becomes an input and data can be fed from an external source into the ALU. The Y bus is the output bus of the ALU. When $\overline{OEY}$ is low the data present on the Y bus comes from the ALU. When $\overline{OEY}$ is high data can be brought onto the chip through the Y bus and written into the RAM.

The IDT7217 (Figure 2) is a fixed point multiplier capable of providing a 16 x 16-bit multiply in 20ns. It too is organized with 3 data buses going on and off the chip. The X and Y buses are the input into the multiplier chip. Data coming in on these buses is captured in the X register and Y register on every rising edge of CP. The two enable signals $\overline{ENX}$ and $\overline{ENY}$ are used as clock enables for the X and Y register respectively and control which given cycle new data will be loaded. On every cycle the output of the X and Y registers are multiplied together, the result being a 32-bit binary number which is clocked into the MSP and LSP register on the rising edge of CP. Again, the enable signal ENP is used to control which cycle will load these two registers. Two paths are provided for bringing data off the chip. The LS P register contents may be read back out onto the Y bus through a buffer controlled by $\overline{OEL}$. When $\overline{OEL}$ is low the Y pins become output pins. The other path is through a multiplexer which selects the contents of the MSP or LSP registers. The multiplexer is controlled by MSPSEL. $\overline{OEP}$ is the control line which controls when the P Port will be driven with the data selected by the multiplexer at the output of MSP and LSP.

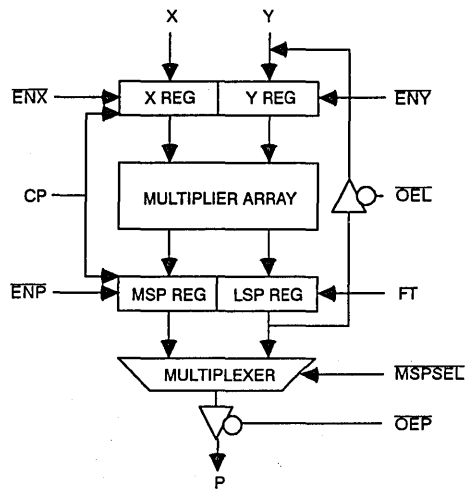


Figure 2. Block Diagram of IDT7217 16 x 16 Multiplier

The functionality of the IDT49C403 can be expanded by connecting an IDT7217 in parallel with the ALU on the IDT49C403. This is accomplished by connecting the X bus to the DA bus and the Y bus to the DB bus, thus providing a path to take data out of the

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register file on the IDT49C403 and place it into the X and Y registers on the IDT7217 (Figure 3a). On the following clock edge the results are put into the MSP and LSP registers of the IDT7217 at which point the data can be read out on the P bus which is connected to the Y bus. The Y bus then is used to write data back into the register file as shown in Figure 3b. Therefore operands go out on the DA and DB bus and results come back on the Y bus.

The FT control input on the IDT7217 can be used to make the MSP and LSP registers transparent. In this way the multiplier would have only one pipeline delay thus allowing the actual multiply and register file update to happen in one cycle.

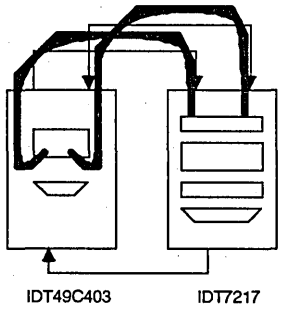

Figure 3a.

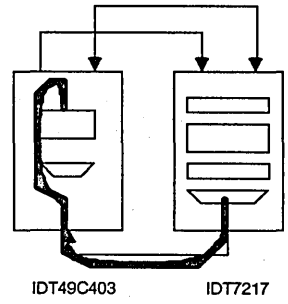

Figure 3b.

Figure 3. Data Flow Between the IDT49C403 and IDT7217

An alternate path for bringing results into the IDT49C403 is using the Y bus of the IDT7217 as shown in Figure 4. By lowering $\overline{OEL}$ the Y bus becomes an output. Correspondingly the $\overline{OEB}$ signal on the IDT49C403 must be brought HIGH. The data then can be brought back on the DB bus, passed through the ALU, possibly added with an accumulation value in the register file, and written back into the accumulation register in the register file.

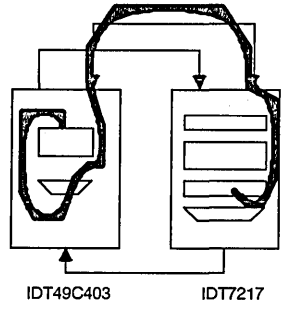

Figure 4. Alternate Data Flow From the IDT7217 to the IDT49C403

EXPANDING THE REGISTER FILE

Three buses on the IDT49C403 also make it convenient for expanding the register file. In the previous discussion we explored how data has been taken out of the register file via the DA and DB buses. In this section we explore how data can be brought from external memory on the DA and DB buses, pass through the ALU and the result brought out on the Y bus is written back into the external memory or register file.

The IDT7133, (2K x 16 Dual Port RAM) is an ideal selection with respect to register file expansion. It is comprised of two address buses and two data buses which can be operated at the same time in both the read or the write modes. In the first example shown in Figure 5, the Dual Port RAM is configured in such a way that in one half of the cycle (CP HIGH) two operands may be read out of the Dual Port RAM and passed through transparent latches. When the clock goes LOW, the latches are then closed providing continuous data to the ALU. The result may be brought out on the Y bus which is then enabled back onto the B port data bus. At this point the Dual Port RAM could be put into the write mode on the B side, thus turning the B data bus around and writing the results back in. Also, the A side at this point could be turned around and new data could be brought in from the outside host system and written into the Dual Port RAM. The advantage of this configuration is that two operands can be fetched simultaneously from the Dual Port RAM at the beginning of the cycle and on the last part of the cycle two values can be written back into the Dual Port RAM, one being the result from the ALU and one being from the host system.

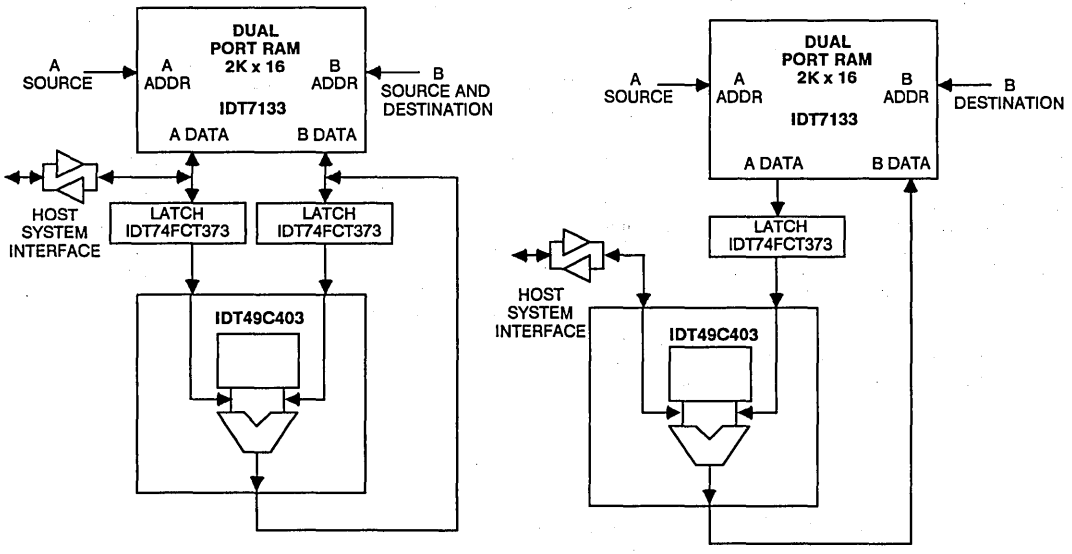

Figure 5. Expanding the IDT49C403 Register File with Dual Port RAM

In the second design example shown in Figure 5, the Dual Port RAM provides one operand while the host system might be providing the other operand. The host system may be buffered through some memory device like another Dual Port RAM or a FIFO. The result of the IDT49C403 could be written back into the Dual Port RAM on the B port. Thus the A port would be dedicated to only reading operands and the B port would be dedicated only to writing the results. This architecture can run much faster because the data buses are not constantly being switched from input to output.

CONCLUSION

Because of the 3-bus architecture, the IDT49C403 allows for easy expansion of the chip register file as well as expanding the ALU. These three buses not only add flexibility, but they also increase the bandwidth going on and off the ALU. While the IDT49C402 may operate at a slightly faster cycle time, the IDT49C403 has fifty percent more bandwidth capability in its third data bus, thus making it an ideal choice in certain applications.

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PROGRAMMABLE LENGTH SHIFT REGISTERS USING RAMs AND COUNTERS

TECHNICAL NOTE TN-16

By David C. Wyland

Programmable length shift registers can be made using counters and RAMs. These shift registers can be quite long and reprogrammed during use if desired.

A block diagram of a programmable length shift register made from a RAM and counter is shown in Figure 1. This shift register can be from one to 16,384 words long by four bits per word. It can shift at clock cycle times down to 38ns for 15ns RAMs and FCT161A counters.

The RAM and counter configuration provide a circular buffer. The counter size (in total counts) sets the size of the circular buffer. The counter points to the next location for storing data in this buffer. Before storing new data at this location, the old data is read out and latched. As the counter walks around the ring, the old data is continuously read out and new data written in.

The programmable length is provided by the counter. In the case shown, the counter counts from zero and increments up to the compare value which is the shift register effective length minus 1. The 521 comparator output is active at this maximum count and causes the counter to be parallel loaded with zero, effectively resetting the counter.

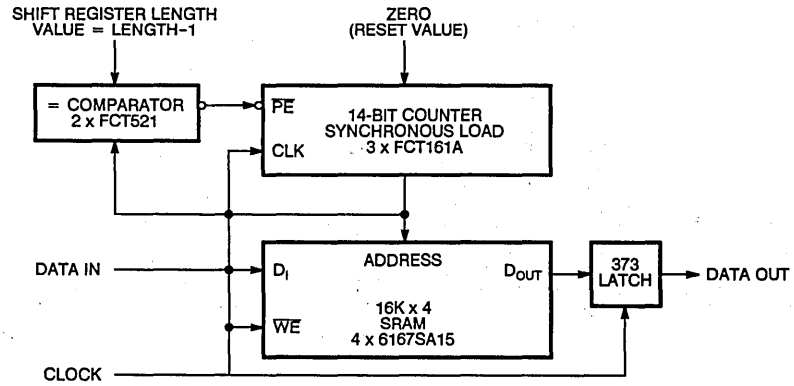

Figure 1. Variable Length RAM Based Shift Register Block Diagram

Timing for this shift register is shown in Figure 2. Data is read out from the RAM during the first half of the clock cycle and latched in the 373 during the second half. Data is written into the RAM in the second half, and the counter is incremented at the end of the cycle. Clock cycle time calculations are shown in Table 1.

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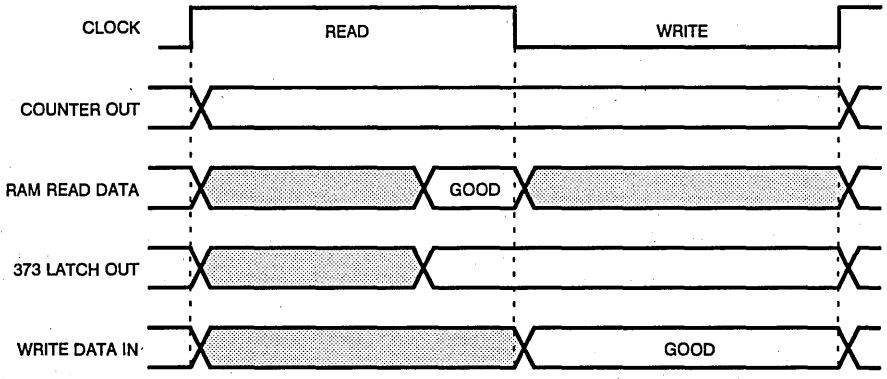

Figure 2. Variable Length RAM Based Shift Register Timing Diagram

Table 1. Clock Cycle Time Calculations

Counter settling time: FCT161A	7.2ns
RAM access time: IDT6167SA15	15.0
Latch setup time: FCT373A	2.0
Clock high time, minimum	24.2ns
Clock low time = RAM write time: IDT6167SA15	13.0
Total	37.2ns

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Integrated Device Technology, Inc.

USING THE IDT7MB6049 CACHE MODULE

TECHNICAL NOTE TN-18

By Kelly Maas

The IDT7MB6049 is a complete cache module for the R3000 RISC processor and is designed for both single- and multi-processor systems. It has two banks of SRAM, each configured as 16K x 60, and each with address latches. One bank is used to cache data, and the other is used to cache instructions. They share a data bus, allowing one bank to be accessed at a time.

Use in multi-processor systems is facilitated by a second address bus and an additional set of latches for that bus. This bus is used in multi-processor applications to latch an address from a source other than the R3000. This allows the system to invalidate entries in the data cache in conjunction with the R3000. This is done in order to maintain cache coherency. The second address latch for the instruction cache is included in the module for symmetry, although normally no invalidations are done to the instruction cache. Only data cache invalidation is described below. Instruction cache invalidation would require cache swapping.

When the system wants to invalidate an entry in the data cache, it forces the R3000 into an MP Stall by asserting CpCond(3). During the one clock cycle that it takes for the processor to enter the MP Stall, it is the responsibility of the system to disable the output of the latch which supplies the processor's address to the data cache, and enable the output of the latch which supplies the invalidate address. The module pins P1OE*(1) and P2OE*(1) are used for this purpose. It is important that they should never be activated simultaneously since the outputs of the latches are tied together. The same applies to P1OE*(2) and P2OE*(2) for the instruction cache. Both address latches of the data cache are normally clocked by the same DClk signal from the R3000 through the P1LE(1) and P2LE(1) pins of the 7MB6049.

Once the processor is in MP Stall, it strobes DRd* while CpCond(2) is unasserted, allowing the system to read the contents of the cache. The actual invalidation of data cache entries begins when the system asserts CpCond(2) and provides the appropriate invalidate address. CpCond(2) causes the R3000 to output an invalid bit and strobe DWr*. Multiple invalidations are performed by keeping CpCond(2) and (3) asserted, and changing the invalidate address. Note that the invalidate address timing must be consistent the processor timing. One suggestion is that the invalidate address input of the module be driven by a register that is clocked by SysOut.

The IDT7MB6049 has two chip select (CS*) signals. Both of these should be grounded if the cache is not depth expanded. The four output enable (OE*) and four write enable (WE*) signals are split evenly between the data and instruction caches: (1-2) control the data cache, and (3-4) control the instruction cache.

OE*(1-2) of the 7MB6049 connect to DRd1* and DRd2* on the R3000. DRd1* and DRd2* are identical, and the load should be distributed evenly between them. Likewise, OE*(3-4) connect to IRd1* and IRd2*. WE*(1-2) connect to DWr1* and DWr2*, and WE*(3-4) connect to DWr1* and DWr2*.

The convention of the pin naming of the 7MB6049 is that P1 refers to the address from the R3000, and that P2 refers to the (invalidate) address from the system. Likewise, (1) refers to the data cache and (2) refers to the instruction cache. As shown in Figure 2, P1LE*(1) and P2LE*(1) are typically connected together to DClk since they latch addresses into the two data cache latches. P1LE*(2) and P2LE*(2) likewise connect together to IClk, although P2LE*(2) is not used if instruction cache invalidation is not performed.

Similarly, P1OE*(1) and P1OE*(2) are typically connected together so that the outputs of the two R3000 address latches are enabled and disabled together, while P2OE*(1) and P2OE*(2) can together control the output of the invalidate address latches. P2OE*(2) may be pulled continuously high if the instruction invalidate address latch is unused.

The 60 data I/O pins of the module are labeled D(0) to D(59). Although the ordering of the data and address pins of a RAM is normally arbitrary and can be ignored, that is not the case with the 7MB6049. Because of steps taken to reduce the chip count and power consumption of the module, Tag(12)-Tag(15) of the R3000 *must* connect to D(36)-D(39) on the 7MB6049, and AdrLo(12)-AdrLo(15) of the R3000 *must* connect to P1A(10)-P1A(13) on the 7MB6049. The order in which the other I/O pins are connected is not critical. Table 1 shows recommended I/O pin connections between the R3000 and the 7MB6049.

R3000 Signals		IDT7MB6049 Signals
data	Data(0) - Data(31)	D(0) - D(31)
data parity	DataP(0) - DataP(3)	D(32) - D(35)
tag	Tag(12) - Tag(31)	D(36) - D(55)
tag parity	TagP(0) - TagP(2)	D(56) - D(58)
tag valid	TagV	D(59)

Table 1. Connection of Data and Tag Buses

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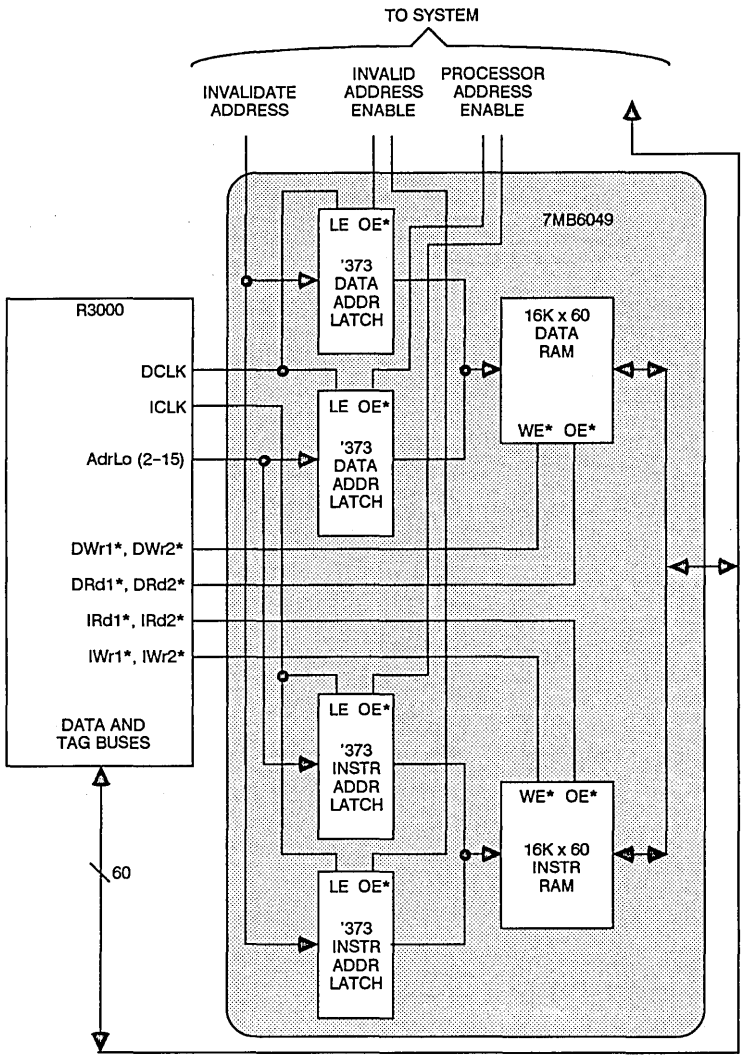

Figure 1. Block Diagram of the 7MB6049

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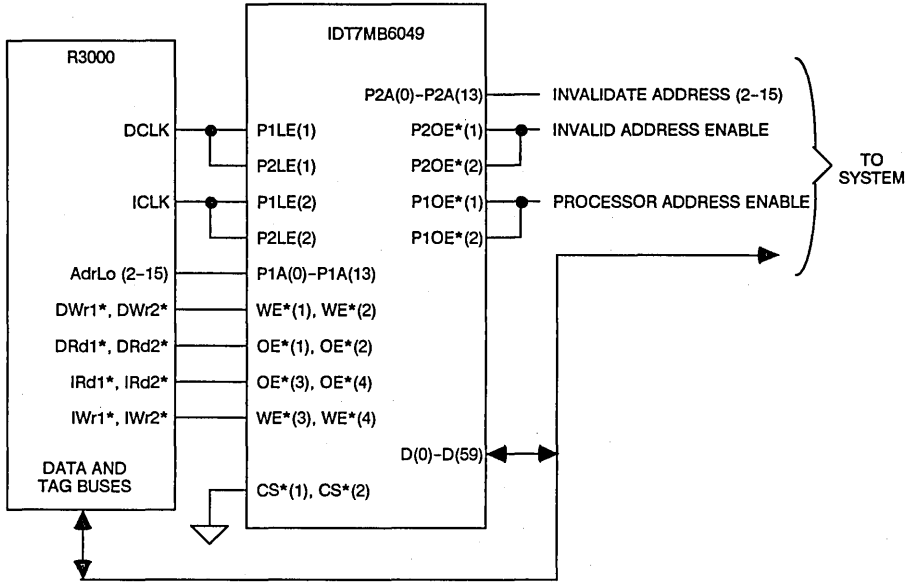

Figure 2. Pin Connections of the 7MB6049

Integrated Device Technology, Inc.

RISC AND THE MEMORY HIERARCHY

APPLICATION NOTE AN-19

By Michael J. Miller

The goal of every computer architecture is to decrease the time it takes to execute a task. With RISC the goal is no different, but the way this is achieved is different than previous architectures such as CISC. To achieve this desired goal, many aspects of CPU design must be addressed. One of the techniques used in RISC to achieve a faster execution rate is to implement a reduced instruction set to gain shorter clock cycles. However it is not sufficient to just speed up the cycle time of the processor. One must pay attention to how to best feed the streamlined processor. In other words, the architect needs to solve the problem of how to support the increased instruction and data bandwidth required by the CPU. Beyond speeding up the datapath, the architect must also address issues such as how to achieve efficient exception handling, fast context switching, memory management and fast Floating Point operation. For further performance,the architect must also address how to tie together multiple copies of this architecture to achieve ever increasing power. This application note will concentrate on how these issues are addressed by the IDT79R3000.

The Performance Equation

The measurement of performance is the time it takes to complete a task, (which is a product of the number of instructions to be executed for the task, the number of cycles per each instruction and cycle time (Figure 1.)) The architects of some of the most recent generation of CPUs (CISC) have spent most of their time addressing the number of instructions per task. By increasing the complexity of the instruction set, the number of instructions to execute the task was decreased. However, each term of the basic performance equation is not independent from the others. In increasing the complexity of the instructions, the number of cycles to execute the instructions increased. The RISC philosophy is to roll-back the complexity of the instructions and reduce the cycles per instruction. This reapportions the resources of the silicon to execute more instructions in parallel as well as include structures to control cache and memory management.

$$\frac{\text{TIME}}{\text{TASK}} = \frac{\text{INSTRUCTIONS}}{\text{TASK}} \times \frac{\text{CYCLES}}{\text{INSTRUCTION}} \times \frac{\text{TIME}}{\text{CYCLE}}$$

Figure 1. Performance Equation

The first term of the performance equation is the number of instructions per task. Whether it be RISC or CISC, the number of instructions to be executed can be minimized by optimizing compilers that have come into their own in the last 6 years. RISC strives to take advantage of these optimizing compilers by including simple register to register instructions which can be utilized more efficiently by the compiler. Additionally, it takes less time to operate on data already in the register than it does to go external to the CPU. The RISC philosophy is to include a large number of registers on the CPU chip and to require the compiler to make efficient use of the registers through effective allocation. Register allocation is an operation that allows optimizing compilers to achieve some of the biggest gains in performance.

In choosing those instructions to be included in the architecture, the designers of RISC analyzed the typical programs executed on the CPU. It was found that about 90% of all instructions executed in a task were simple loads and stores, ALU operations and branches. If the architects could speed up these instructions, they could make a significant performance gain. The other 10% of instructions were more complex operations. Previous generations of CPUs used more of the silicon for this 10% than they used for the 90% of simple operations. It was found that few architectural additions could be made to speed up this 10% of the instruction space without slowing the execution of the other 90% of the instructions. Therefore, RISC design focuses in the area that promises the biggest gain, i.e. the simpler instructions.

Once the architects isolated the key instructions to speed up, they could minimize the cycles that it took to execute those instructions. Pipelining was employed so that on every clock cycle a new instruction could be started before the previous one completed. Although the goal of RISC is to execute one instruction on every clock cycle, not all instructions can be completed on one clock cycle. Some instructions have a latency effect. These instructions typically are branches, loads and stores. Therefore, the task is to remove the latency as much as possible in these instructions to achieve the single-cycle execution goal. These latencies are mainly caused by the external memory pipelines for loads and branches. When branching, the way the test conditions are determined has the most affect on the latency. Fast RISC CPUs therefore, only compare operands for equality or against zero to eliminate carry/propagate chains in ALUs. This solution simplifies the architecture for increased speed without compromising the power.

The third part of the equation is to maximize the clock speed. This is done through improving the process technology that is used to implement the architecture, (such as bipolar, NMOS or CMOS), as well as the implementation of the architecture in it's logical form. As the internal delays are decreased and clock cycles shortened, the impact of external paths becomes greater. With RISC, the critical path external to the CPU is through the memory. To speed up the memory access for systems with big main memories implemented in DRAM, caches have been employed. The access time of the cache is determined by the organization and the implementation of the tag checking. Therefore, caches are integral to supporting the increased clock speed of RISC in big systems, but the caches alone cannot keep the CPU supplied.

The Memory Hierarchy

Programs and data are stored in DRAMs and secondary storage devices like hard disks which have slow access times in comparison with a cycle time of the ALU. The total RISC system implementation utilizes a memory hierarchy where each level of the hierarchy is, in effect, a cache for the next level down. The top of the hierarchy is a very small fast cache (register file) while the bottom level (main memory) is slow and very large. As an example, to support 20 MIPS operation, the CPU needs at least 200 Mbytes/sec of instruction and data bandwidth while main memory typically only supports 28 Mbytes/sec (see Figure 2). Previous CPUs, like the 68020, only required 15 Mbytes/sec to support 1.5 MIPS of performance.

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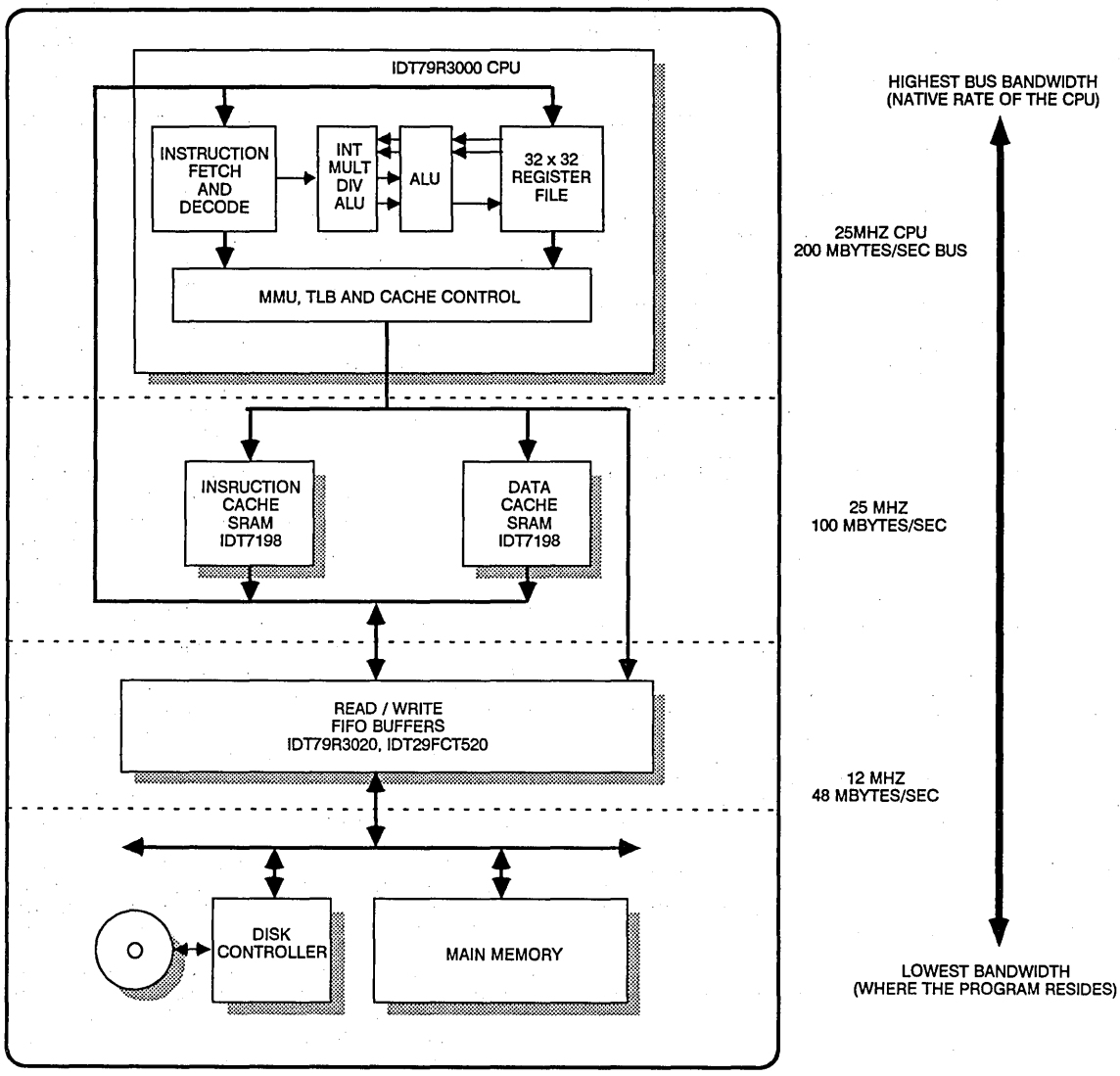

Figure 2. The Memory Hierarchy

The first level of the hierarchy is the register file that keeps the ALU fed with data. The management of the register file is performed at compile time. Without optimizing compilers, the total power of RISC cannot be realized.

The second level of the hierarchy is the instruction and data caches. Because RISC CPUs require a new instruction every clock cycle, the access time of the cache SRAM is the pacing delay in a RISC CPU's cycle time. To further increase the bandwidth into the RISC CPU, a separate cache for data is used.

The third level hierarchy is the main memory consisting of cache hard disks. Today's RISC CPUs employ on-chip a memory management unit (MMU) to manage the swapping of program segments between main memory and the disk. The Translation Lookaside Buffer (TLB) is a key element in the MMU that translates the logical addresses to the physical address of the programs stored in main memory. The TLB is a look-up table of addresses. Since circuitry to implement TLBs is costly in silicon area, TLBs are kept small and function as another cache for a large master look-up table kept in main memory.

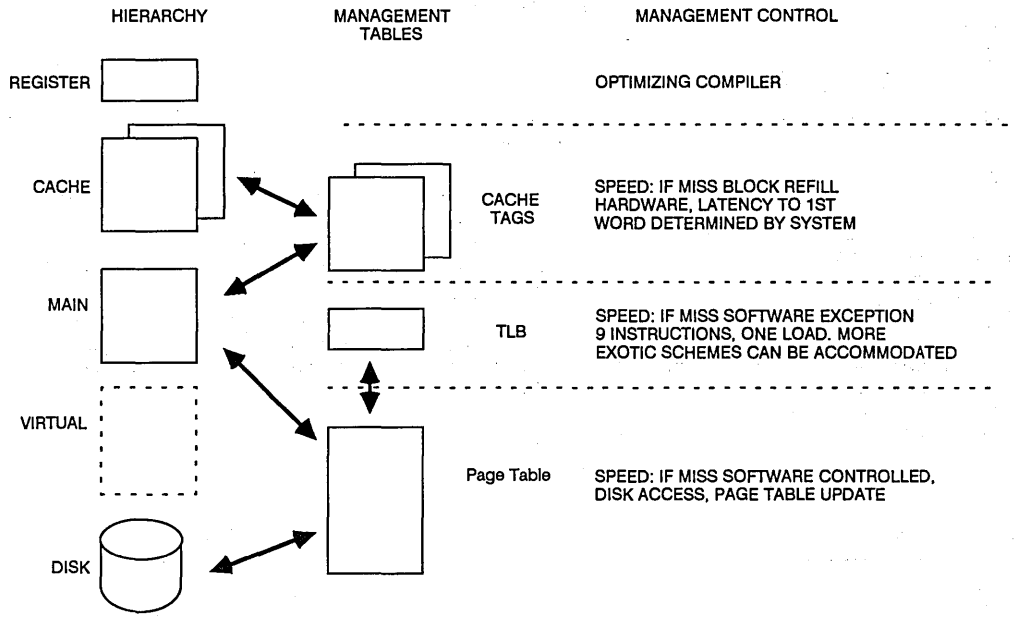

Figure 3. Managing the Memory Hierarchy

More than a Data Path

Therefore, RISC CPUs need not only a datapath, but also a memory hierarchy that must be managed by the CPU and software in order to operate efficiently. All levels of the hierarchy are used to feed the insatiable appetite of the instruction and data path of today's RISC CPUs. Since the reduced instruction set is only one aspect of the RISC CPU technique, perhaps a more appropriate name would be Bandwidth Increased Streamlined Computer (BISC). This new term could be used at the 'risc' of adding more letters to todays' already full bowl of alphabet soup!

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Integrated Device Technology, Inc.

STATIC RAM TIMING

APPLICATION NOTE AN-20

By Mammad A. Safai

INTRODUCTION

This application note is about timing parameters involved in the use of static RAMs. The application note describes these parameters, their individual meanings and their uses.

Optimum performance can be accomplished by understanding the timing of the memory element. A system which is designed using this knowledge will be fast and will not consume a lot of power.

The timing parameters are actually the reflection of the internals of the static RAMs. These internals will be discussed and the relationship between the timing at the cell level and the timing at the component level will become clear.

The timing parameters are divided into two groups: those that are involved with common I/O parts and those that are involved with the separate I/O parts.

In order to show the different aspects of the timing problem in static RAMs, two IDT 16K static RAMs will be used as examples.

The RAM Cell

In order to better represent the different timing parameters involved in read or write operations in static RAMs, we will start with the basic memory cell. The basic memory cell of Integrated Device Technology is the four transistor cell (4T Cell shown in Figure 1).

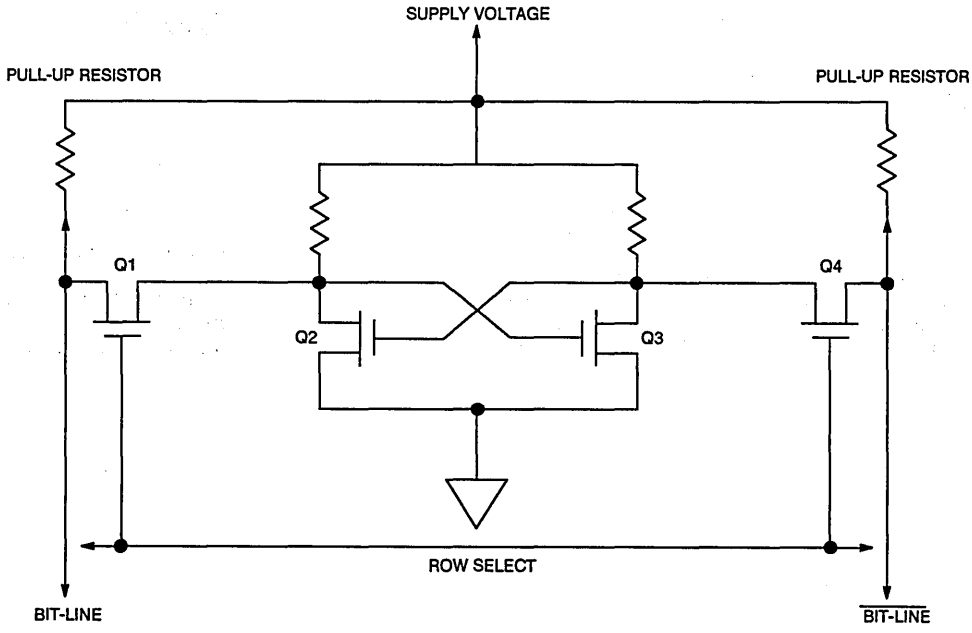

Figure 1. Four Transistor Cell

In the four transistor cell of Figure 1, transistors Q2 and Q3 constitute a latch. When Q2 is on, it keeps Q3 off, and when Q3 is on, it keeps Q2 off. A zero (0) bit is accomplished by Q2 on and Q3 off. A one (1) bit is accomplished by Q3 on and Q2 off.

WRITING INTO THE CELL

To write a one (1) into the cell, Row Select becomes active. Transistors Q1 and Q4 turn on. Bit-Line is forced high and $\overline{\text{Bit-Line}}$ is forced low. Transistor Q2 will turn off and transistor Q3 will turn on. Therefore, the contents of the latch becomes a "1".

READING FROM THE CELL

To read the contents of the cell, Row Select becomes active. Transistors Q1 and Q4 turn on. The state of the drains of transistors Q2 and Q3 becomes available on Bit-Line and $\overline{\text{Bit-Line}}$. One of the two Bit-Lines will be pulled down through Q1Q2 or Q3Q4. If Bit-Line is high and $\overline{\text{Bit-Line}}$ is low, the contents of the latch is a "1".

RAM

A RAM is a RAM cell together with some logic interface for read or write operations. Figure 2 shows a one-bit RAM with some logic interface in order to operate it.

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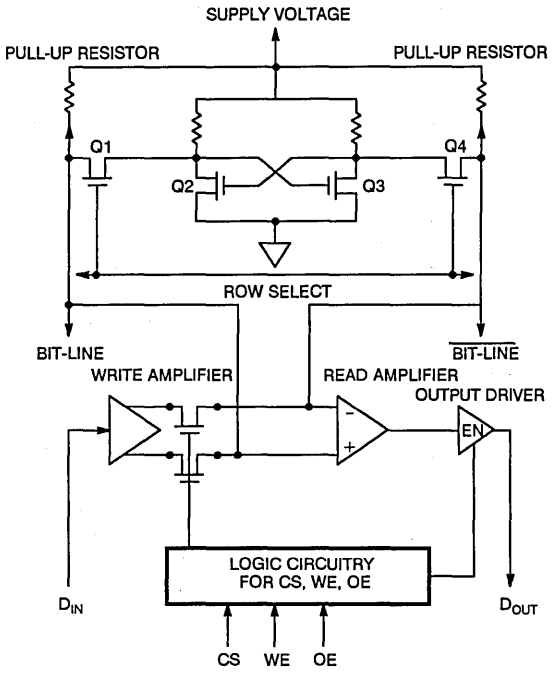

Figure 2. One-Bit RAM

WRITING TO THE ONE-BIT RAM

The writing operations of the one-bit RAM are performed in the following order:

- Force Bit-Line high and $\overline{\text{Bit-Line}}$ low (to write a "1")
- Row Select goes high to select the cell to be written
- Q1 and Q4 turn on
- Q2's drain is pulled high towards the supply
- Q3's drain is pulled down to ground level
- Q2's gate will be low, therefore Q2 is OFF
- Q3's gate will be high, therefore Q3 is ON

As shown in Figure 2, in order to write, the control logic has to enable the differential write amplifier that is placed in the path of D_{IN}. When a data bit has to be written into the latch, D_{IN} is put through that differential amplifier which will charge up one of the bit lines and will charge down the other. The Row Select line has already selected the appropriate latch, and finally, the data is written into the cell.

READING FROM THE ONE-BIT RAM

The reading operations of the one-bit RAM are performed in the following order:

- Row Select becomes active
- Q1 and Q4 turn on
- Bit-Line will charge to the value of the drain of Q2
- $\overline{\text{Bit-Line}}$ will charge to the value of the drain of Q3
- Read amplifier will evaluate the two Bit-Lines and will output the logic value corresponding to the content of the latch.

While reading from the latch, Row Select selects the appropriate latch. The control logic will enable the appropriate sense amplifier. The sense amplifier will sense the bit lines and output a value that will represent the content of the latch in question.

In Figure 2, the read amplifier is a differential amplifier that senses which bit line is being pulled low. Both bit lines start high and are pulled low by Q1Q2 or by Q3Q4. By sensing the movement of the bit line being pulled low, the time spent to determine the content of the latch is reduced.

A 2 x 2 RAM ARRAY

Before showing the general picture, let us examine the inner connections of four cells arranged as a 2-word-by-2-bit RAM. Figure 3 shows the configuration of this memory array. This array could be extended in both directions.

A0 selects the particular row that interest the user. If A0 is low, RS0 becomes active, and if it is high, RS1 becomes active. A1 selects the particular column that interest the user. If A1 is low, CS0 becomes active, and if it is high, CS1 becomes active.

In the manner described above, if the user would like to access the latch placed on the top left part of the Figure 3A, A1A0 = 00.

Latch (0,0) --> A1A0 = 00
Latch (1,0) --> A1A0 = 10
Latch (0,1) --> A1A0 = 01
Latch (1,1) --> A1A0 = 11

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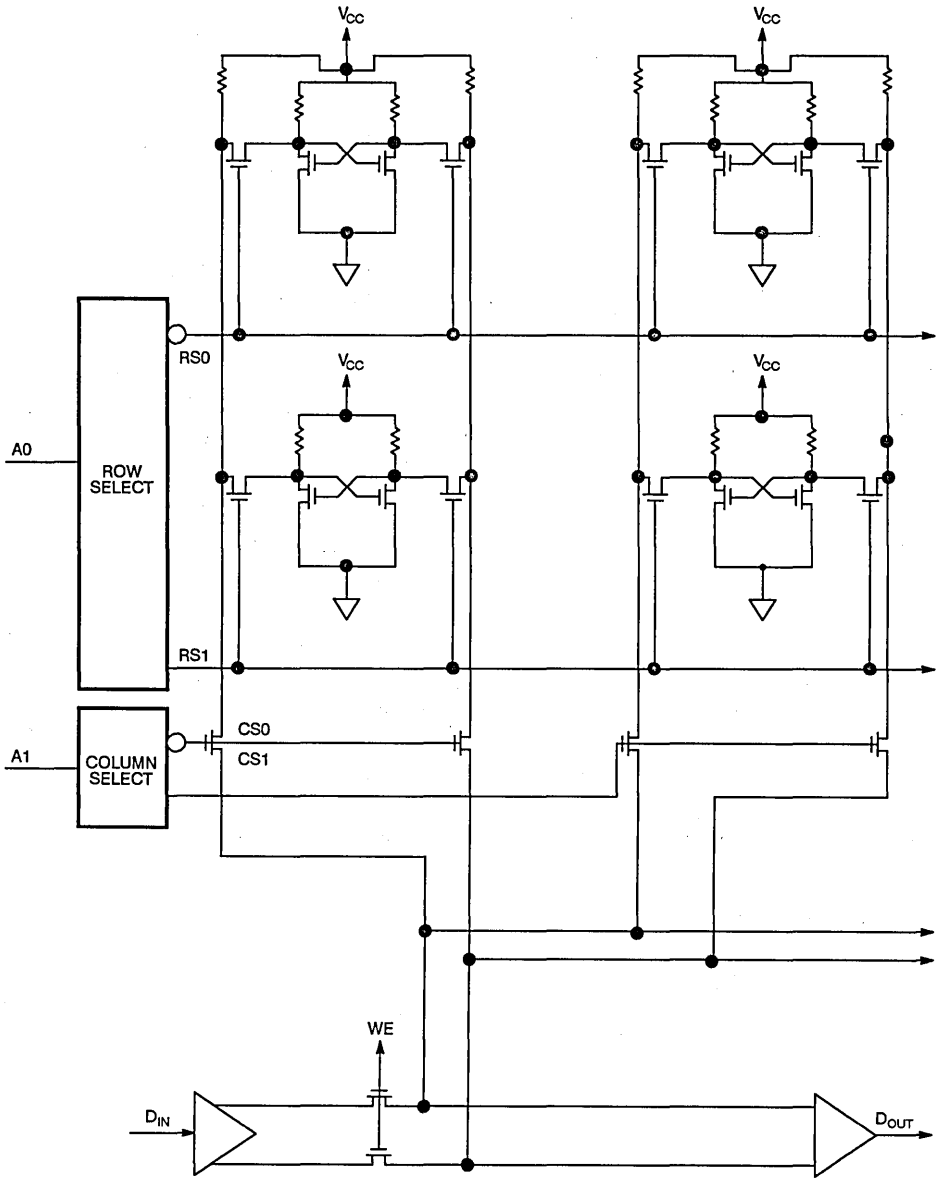

Figure 3. A 2 x 2 Array

A REAL PART

Before going into detail about the different aspects and trade-offs of the various approaches of reading or writing, let us take a look at Figure 4 which represents an actual part. This part has 16K of memory and is arranged in a 16K x 1-bit manner (IDT6167). It is similar to the array shown in Figure 3 but has been expanded from 2 x 2 to 128 x 128.

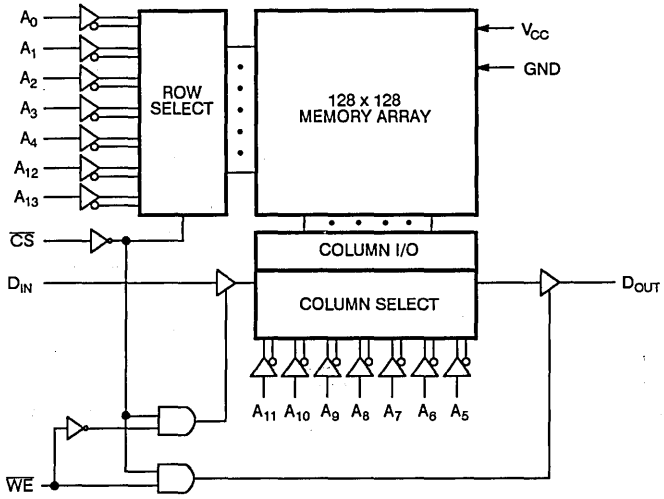

Figure 4. Functional Block Diagram of IDT6167 16K x-Bit

The selection of a particular row is done using address lines A0---A4, A12 and A13. The selection of a particular column is done using address lines A5---A11. The chip select line ($\overline{CS}$), enables the row select logic and the write/read signal. Data In and Data Out paths are controlled by $\overline{CS}$ and the $\overline{WE}$ signal. If $\overline{CS}$ and $\overline{WE}$ are active, the path for Data In becomes valid. If $\overline{CS}$ is active and $\overline{WE}$ high, the path for Data Out becomes active. If $\overline{CS}$ is not active, both paths are turned off.

WRITING METHODS: WE vs. CS CONTROLLED WRITE

There are also two different ways for executing a write, i.e. the $\overline{WE}$-controlled or the $\overline{CS}$-controlled write. For the $\overline{WE}$-controlled write, the basic steps that one should consider are:

- Bring the address bits to the address pins
- Wait for the address pins to settle
- Select the chip
- Strobe the Write Enable pin: This will turn on the write amplifier switches
- Bring the data bits to the data pins
- Terminate the strobe
- Keep the data bits stable for a while

Chip Select controlled write uses a slightly different set of steps :

- Bring the Write Enable low (enabled)
- Bring the address bits to the address pins of the IC
- Wait for the address pins to settle
- Strobe the Chip Select: This will turn on the bit and row select switches
- Bring the data bits to the IC data pins
- Terminate the strobe
- Keep the data bits stable for a while

READING FROM THE RAM ARRAY

During a read operation, the $\overline{WE}$ signal is high, disabling the write amplifiers and enabling the output drivers. In Figure 4, since the part is a by one (x1) part, there is only one output driver and one write amplifier.

Once the sense amplifier is active, the address lines (using the row and column select logic) enable a particular memory cell. The state of the cell is sensed by the sense amplifier (read amplifier) which in turn will output the corresponding logic level.

The user has to wait a certain amount of time for the read amplifier to sense the value of the latch. This amount of time will correspond to the access time of the device.

Here are some steps representing a read operation:

- Select the device ($\overline{CS}$ low)
- Enable the read amplifier or sense amplifier ($\overline{WE}$ high): This will actually turn on the driver at the output of the sense amplifier (see Figure 2)
- Wait for the access time
- Read the data bit out of the data bus

COMMON I/O AND SEPARATE I/O

What we have discussed is called a **Separate I/O** part. Separate I/O means that you have separate input and output paths. As far as the user is concerned, it means that, at the device level, the part has different pins for the Data In and Data Out bits.

A 2 x 2 COMMON I/O RAM ARRAY

There are also other memory parts that are called **Common I/O** RAMs. A common I/O part has only one path for the data bits and

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this path is bidirectional. At the cell level in a common I/O part, the D_{IN} line is connected directly to the D_{OUT} line. Figure 5 illustrates the idea of a common I/O part at the cell level. It represents a 2 x 2 common I/O array of RAM.

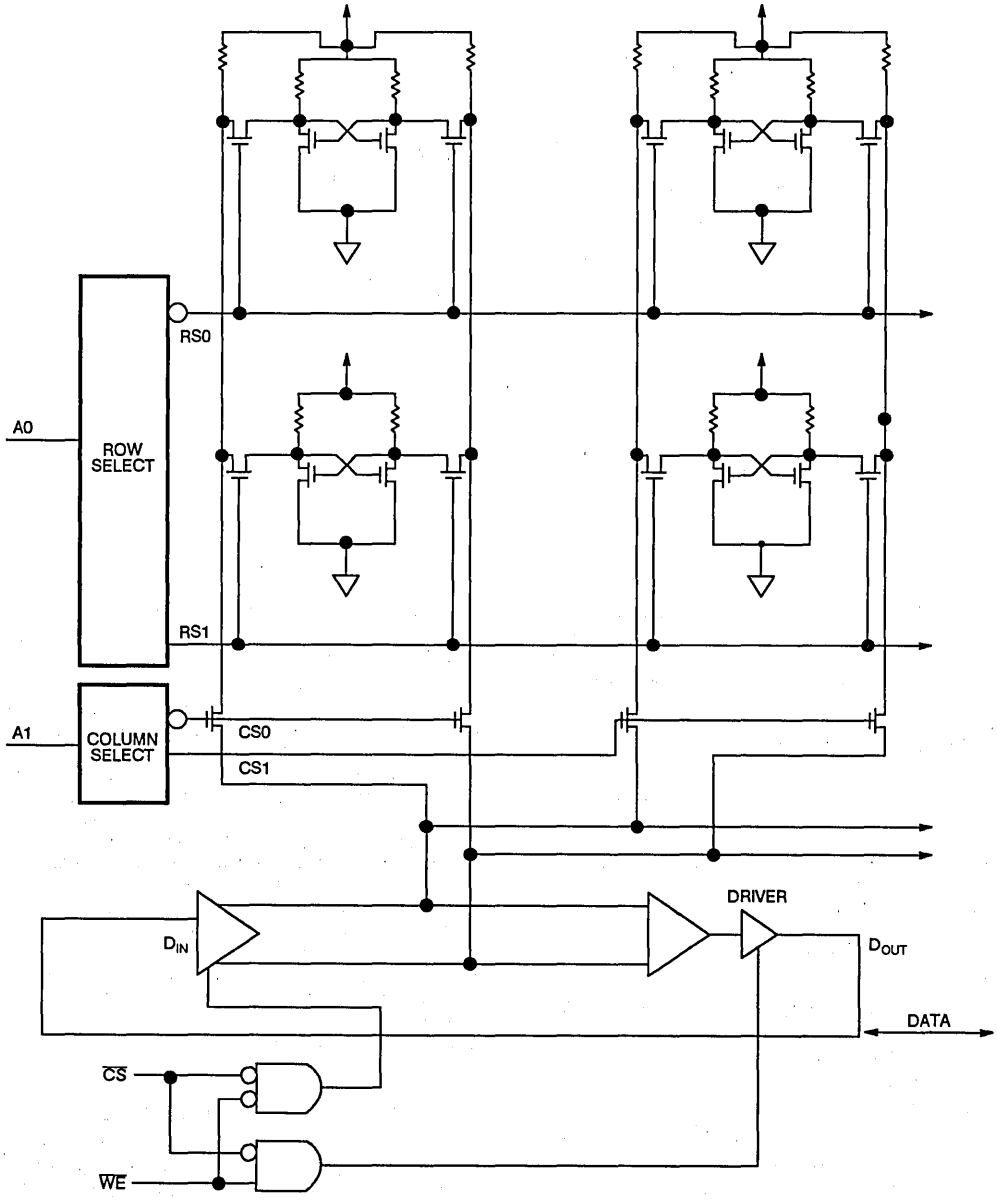

Figure 5. A 2 x 2 Common I/O ARRAY

If the user decides to execute a write on a common I/O part, there will be one extra step to take compared to our previous set of steps illustrated for a separate I/O part. This extra step is just turning off the output driver, enabling the input differential amplifier and finally executing a write into the array.

A REAL COMMON I/O PART

Let us now take a look at another actual part from Integrated Device Technology. Figure 6 shows the functional block diagram of a 4K x 4-bit memory device, the IDT6168.

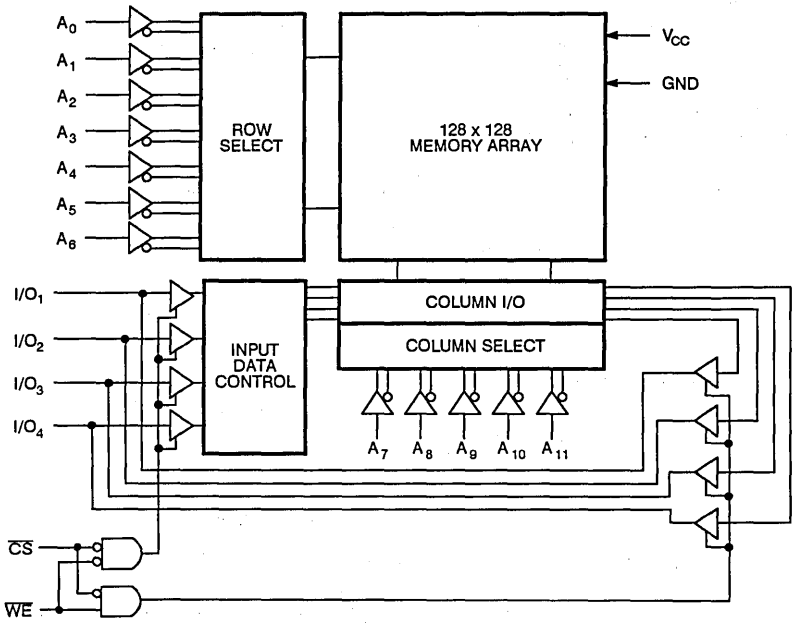

Figure 6. Functional Block Diagram of 4K x 4-Bit Common I/O Memory

In order to understand the different timing parameters involved in the read/write operation of the memory elements in general, let us examine Figure 6 in more detail.

WRITING METHODS: WE vs. CS CONTROLLED WRITE

Writing is achieved using two different techniques. Similar to the previous section, a write can be achieved by either strobing the chip select or strobing the write pulse. Here is the sequence to follow if the WE (Write Pulse) controlled write is used:

- Bring the address bits to the IC address pins
- Select the IC by enabling Chip Select
- Wait for the address pins to settle
- Start the Write Pulse: This will turn off the output drivers and enable the input differential amplifier
- Bring the data bits to the IC data pins
- Turn off the write pulse
- Keep the data bits stable for a while after the Write pulse: This is required hold time for the cells to settle

The other way of writing is the Chip Select controlled write. The steps that follow are very similar to the steps taken for the separate I/O part. Here is the sequence:

- Bring the address bits to the IC address pins
- Wait for the address pins to settle
- Keep the Write Enable pin low: This will keep the output drivers off and allows the input differential amplifier to get enabled as soon as the CS goes low
- Bring the data bits to the IC data pins
- Strobe the Chip Select: This will enable the input differential amplifier for writing
- Bring the Chip signal high again: This will disable the input differential amplifier
- Keep the data bus stable for a while after the Chip Select pulse goes high: This is the required hold time for the cells to settle

READING FROM THE COMMON I/O ARRAY

Again, reading the common I/O part is not very different from reading the separate I/O part. If the user decides to continuously read an entire block sequentially, the Chip Select signal should be kept low and the Write Enable signal high. In this way, the output drivers are enabled and the concerned memory cells are selected. The steps to follow are described below:

- Bring the address bits to the pins of the IC
- Select the IC by bringing the CS signal low
- Turn the outputs on by bringing the WE signal high: This step and the two above can be executed together

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- Wait for a while for:
  The concerned cells to be selected
  The output drivers to be enabled (t_{LZ})
  The data bits to be valid (t_{ACS})
- Read the Data Out of the IC after the above wait

Data will be available after T_{AA} (address access time) from the last time the address changed or after t_{ACS} (chip select access time) from the time $\overline{CS}$ became active, whichever is longer.

WHAT DID WE TALK ABOUT SO FAR?

We have talked about latches and how they work. We have described the structure of an array and then shown that there are two different sorts of array. We have shown that the difference is not a big one (Separate I/O vs. Common I/O) and that the parts are not only similar in their base structure, but also similar in the way they work.

Then the description of the necessary steps to take for a write or a read operation was given. In order to finalize the idea about memory parts, and before going into further detail about the timing parameters and what they mean, Figure 7 shows a general block diagram representing a memory part.

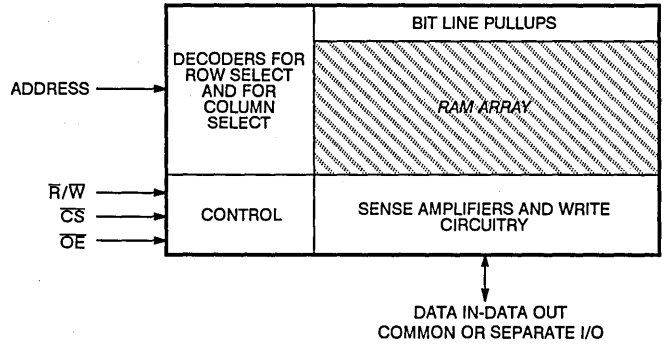

Figure 7. Block Diagram for a Static RAM Memory Device

TIMING

At this point let us divide the timing parameters into two different categories: those involved with common I/O and those involved with separate I/O. To have a better understanding of these parameters, let us take a look at various timing diagrams taken from actual devices that Integrated Device Technology produces.

WRITING TO SEPARATE I/O SRAM

To start, let us take a look at the 16K x 1-bit part (separate I/O), the IDT6167. As the reader remembers, there are two ways of accomplishing a write. Figure 8 illustrates the Write Enabled controlled write for the mentioned memory IC.

WRITE ENABLED CONTROLLED WRITE

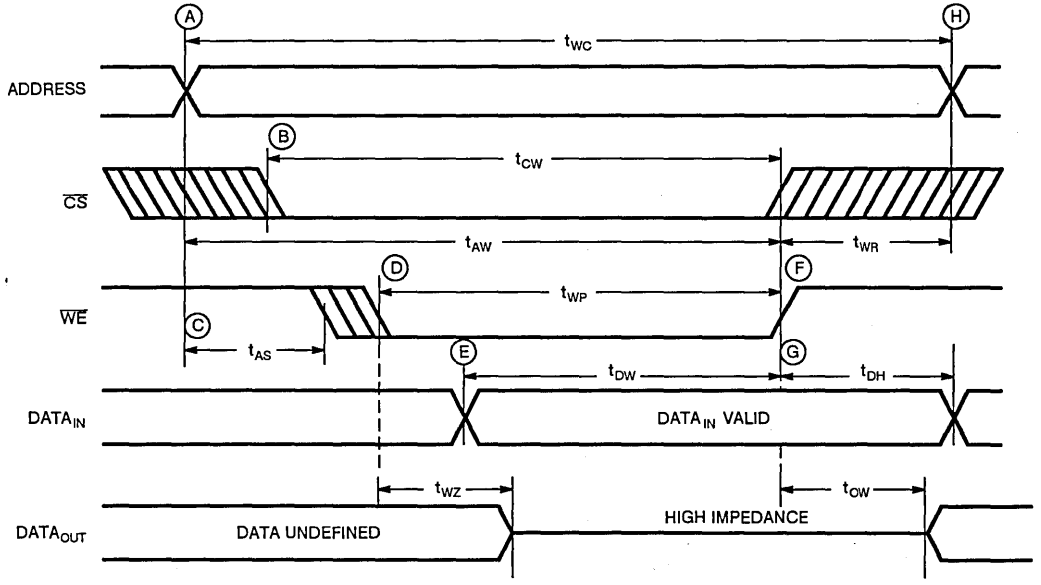

Figure 8. Timing Diagram for WE Controlled Write, IDT6167

Figure 8 shows the timing for Write Enabled controlled write and the steps described below relate to that Figure:

- Bring the address bits at the IC address pins. (At this point the user should keep the address bits stable throughout the write operation.) The Write Cycle time is t_{WC} during which the address must remain constant.
- Select the chip. At this point the chip is selected and t_{CW} is the chip select to end of write ($\overline{WE}$ signal) time. This is the minimum amount of time that the IC has to remain in a selected mode.
- Wait a while for the address pins to settle. The address set-up time is t_{AS}. During that particular time the user is giving the memory some time for the concerned cells to be selected with the row and column select logic.
- Strobe the Write Enable pin. This will enable the write differential amplifiers (since CS is active already). The write pulse width is t_{WP}. This is the minimum amount of time necessary for the $\overline{WE}$ signal to be active in order to give enough time for the cells to change state.
- Bring the data bits to the IC data pins. The data bits should be stable by the cells for at least t_{DW}, which is the data valid to end of write time. The set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point, the $\overline{WE}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the hold time for the latches of the IC, t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state while the write switches turn off.
- This is the end of the cycle. At this point, the user can make an address transition for the next operation **but remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** If the $\overline{CS}$ or the $\overline{WE}$ signals are not held high during an address transition, the address decoders can glitch when addresses change, and therefore, cause random cells to be written:

Figure 9 shows the timing for chip select controlled write and the steps described below relate to this Figure:

- Keep the Write Enable low (enabled). During a Chip Select controlled write, the Write Enable signal is low during the the Chip Select pulse. It should be active for at least the minimum. The write pulse width is t_{WP}.
- Bring the Address bits at the IC address pins.The user must keep the address bits stable throughout the write operation. The Write Cycle time is t_{WC} during which the address must remain constant.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected by the row and column select logic.
- Strobe the Chip Select. This will turn on the bit and row select switches and will bring the cells to a situation where they are ready to be written into. t_{CW} is the chip select to end of write time. This is the minimum width of the CS strobe.
- Bring the data bits at the IC data pins. The Data bits should be stable at the cells for at least t_{DW}, which is the data valid to end of write time. The set-up time t_{DW} is for the latches of the IC.
- Terminate the strobe. At this point the $\overline{CS}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. t_{DH} is the data hold time. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state while the select lines turn off.
- This the end of the cycle. At this point the user can make an address transition for the next operation **but remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** If the $\overline{CS}$ or the $\overline{WE}$ signals are not held high during an address transition, the address decoders can glitch when addresses change and, therefore, cause random cells to be written.

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CHIP SELECT CONTROLLED WRITE

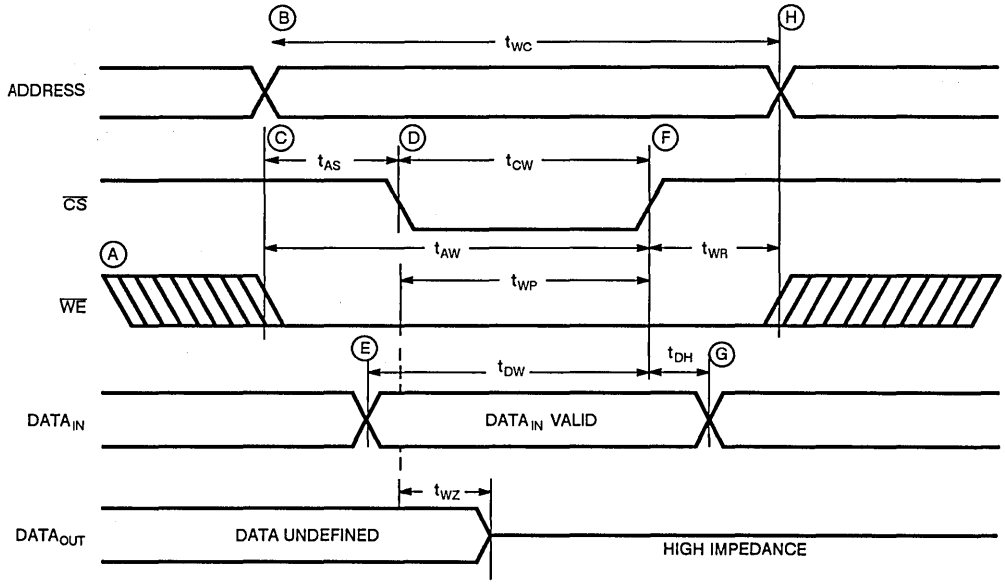

Figure 9. Timing Diagram for CE Controlled Write, IDT6167

TIMING FOR CONTINUOUS READ

Let us now take a look at the timing for a read cycle. Let us assume that the user wants to constantly read the IC. The $\overline{WE}$ signal is high and the $\overline{CS}$ signal is low, continuously. The timing that will apply is shown in Figure 10.

TIMING WAVEFORM OF READ CYCLE NO. 1

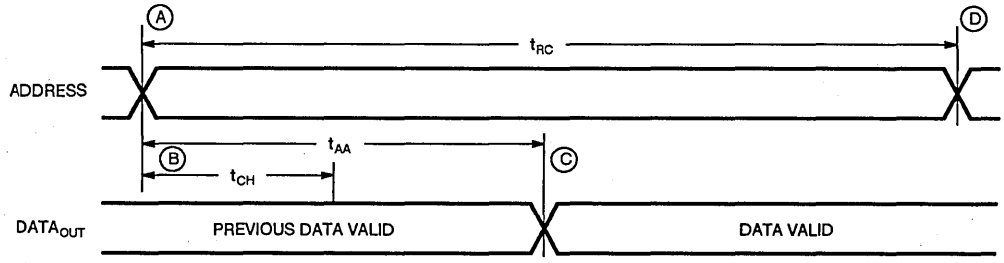

Figure 10. Timing Waveform for Read Cycle No.1

During this read cycle, the Write Enable ($\overline{WE}$) is high (therefore disabled) and the Chip Select line is low ($\overline{CS}$, therefore enabled). The output drivers are turned on while the chip is selected, putting the IC in a constant read mode. The amount of time that the previous data will still be valid after an address transition has occurred is t_{OH}. Finally, after T_{AA} has passed since the address transition, the valid data bits are available. Since T_{AA}-t_{OH} is changing, data from the IC is not valid during this time.

Let us go through Figure 10 step by step:

- Bring the address bits to the IC address pins. The read cycle time parameter during which the address must remain constant is t_{RC} .
- At this point the previous data is still valid on the bus. This data is going to stay valid for t_{OH}, which is the output hold from address change time.
- At this point the valid data will appear at the pins. T_{AA} is the IC access time and is the amount of time that has to pass since the address transition for the valid data to appear at the pins.

- At this point the IC is ready for a new address.

TIMING FOR CS CONTROLLED READ

Figure 11 shows the timing of a chip select continuous read operation.

TIMING WAVEFORM OF READ CYCLE NO. 2

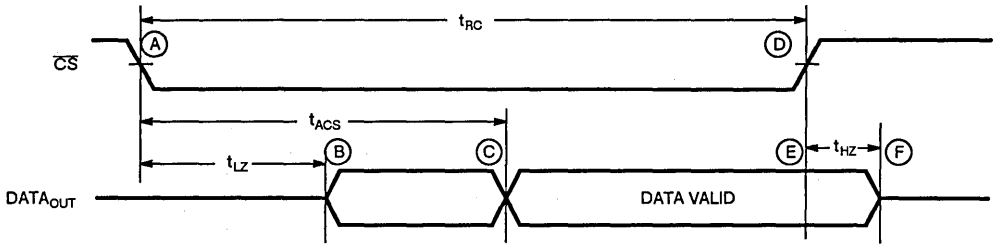

Figure 11. Timing Waveform for Read Cycle No.2

In Figure 11, it is assumed that the $\overline{WE}$ signal is high and that the address transition has occurred and the address is valid prior to the $\overline{CS}$ transition to a low state:

- The $\overline{CS}$ signal makes a high-to-low transition, therefore becoming active. t_{RC} is the read cycle time and represents the amount of time that this signal has to stay active.
- The Chip Select to Output in low Impedance state is t_{LZ}. This shows that t_{LZ} time after the $\overline{CS}$ high-to-low transition the output drivers will be on.
- The Chip Select access time is t_{ACS} . This shows the amount of wait necessary after the high-to-low transition of the $\overline{CS}$ signal before the valid data will appear at the output pins.
- Terminate the strobe. This will start turning off the output drivers. At this point the $\overline{CS}$ signal will become inactive.
- From this point on, the output drivers are turning off and the valid data will be present for only t_{HZ} time after this point. t_{HZ} is the Chip Deselect to output in high impedance time parameter.

WRITING TO COMMON I/O SRAM

Let us take a look at the 4K x 4-bit part (Common I/O), the IDT6168. Figure 12 illustrates the Write Enabled controlled write for the common I/O RAM.

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WRITE CYCLE NO. 1

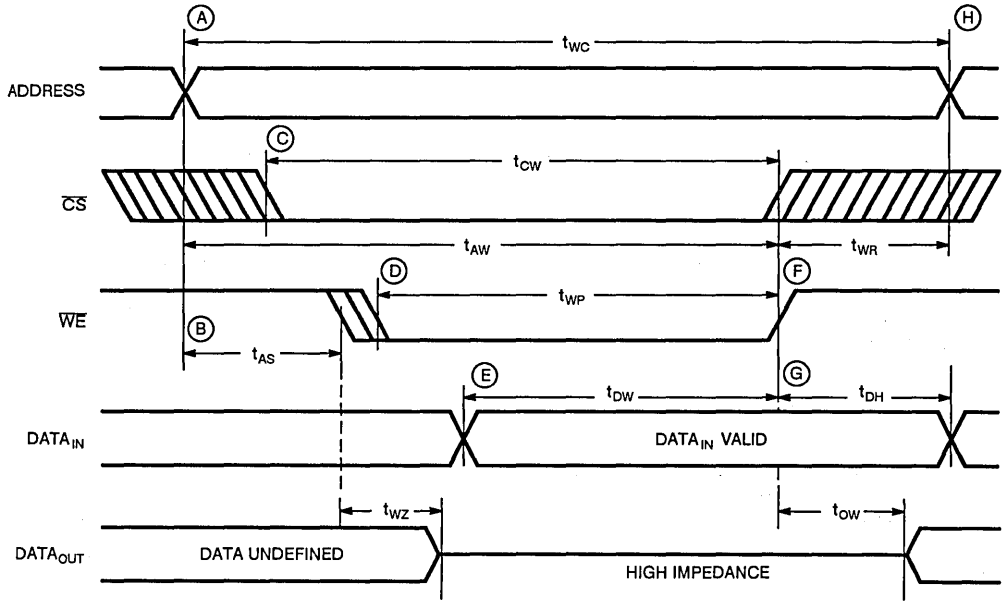

Figure 12. Timing Diagram for WE Controlled Write, IDT6168

TIMING FOR WE CONTROLLED WRITE

The steps described below relate to Figure 12:

- Bring the address bits to the IC address pins. At this point, the user must keep the address bits stable throughout the write operation. The Write Cycle time during which the address must remain constant is t_{WC}.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected with the row and column select logic.
- Select the chip by enabling Chip Select. At this point the chip is selected and T_{CW} is the chip select to end of write ($\overline{WE}$ signal) time. This is the minimum amount of time the IC has to remain selected.
- Strobe the Write Enable pin. This will enable the write differential amplifiers (since CS is active already). The minimum write pulse width is t_{WP}. This is part of the amount of time necessary for the $\overline{WE}$ signal to be active in order to give enough time to the cells to change state. On the data out graph in Figure 12 (bottom), the user should notice that at this time, the output drivers start to turn off and, in t_{WZ} time, they will be completely in the high impedance state.
- Bring the data bits to the IC data pins. The data bits should be "seen" by the cells for at least t_{DW}, which is the data valid to end of write time. The Set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point the $\overline{WE}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. The data hold time is t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state.
- This is the end of the cycle. At this point, the user can make an address transition for the next operation. **Remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** By keeping them inactive, the user is preventing the row and column select logic to expose the cells to the address bus while it is in transition.

WRITE CYCLE NO. 2

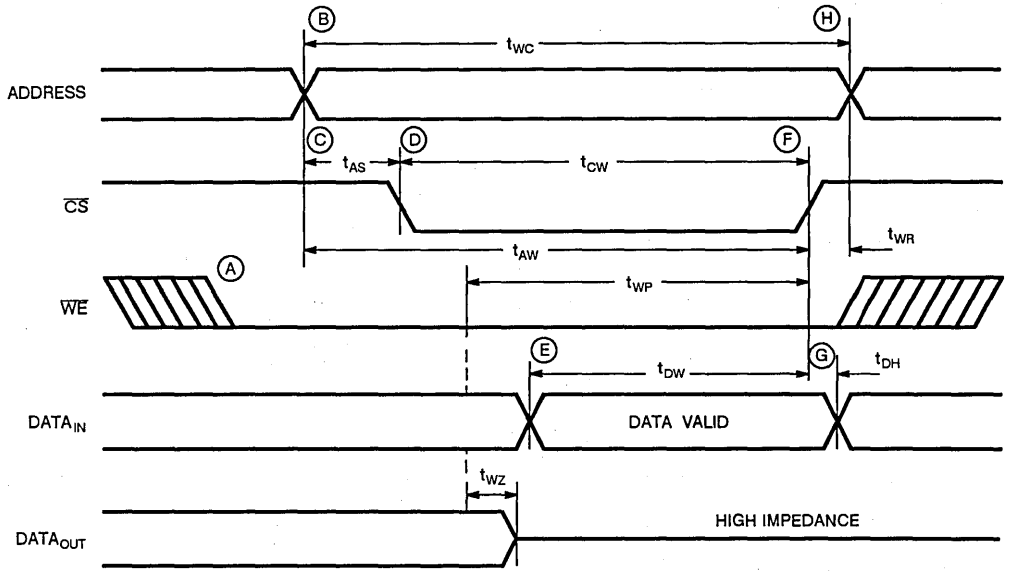

Figure 13. Timing Diagram for CS Controlled Write, IDT6168

TIMING FOR CS CONTROLLED WRITE

The steps described below refer to Figure 13.

- Keep the Write Enable low (enabled). During a Chip Select controlled write, the Write Enable signal is supposed to be active for at least the write pulse width amount of time. The time that the WE signal is enabled should correspond to the time where the IC is selected for at least the width of the write pulse. From the moment that $\overline{WE}$ becomes active, t_{WZ} is the amount of time after which the output drivers are turned off and reach high impedance state.
- Bring the address bits to the IC address pins. The user should keep the address bits stable throughout the write operation. The Write Cycle time is t_{WC} during which the address must remain constant.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected with the row and column select logic.
- Strobe the Chip Select. This will turn on the bit and row select switches and bring the cells to a situation where they are ready to be written into. The chip select to end of write time is t_{CW}. This is the minimum width of the CS strobe.
- Bring the data bits to the IC data pins. The Data bits should be "seen" by the cells for at least t_{DW}, which is the data valid to end of write time. The Set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point, the $\overline{CS}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. The data hold time is t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state.
- This the end of the cycle. At this point the user can make an address transition for the next operation. **Remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** By keeping them inactive, the user is preventing the row and column select logic to expose the cells to the address bus while it is in transition.

SOME POINTS TO NOTICE IN COMMON I/O SRAMs

1. $\overline{WE}$ vs. $\overline{CS}$ Controlled Write on Common I/O SRAMs

One more detail about common I/O is that it is possible to improve the speed of operation of the system by intelligently choosing what signal will be strobed during a write:

if the user decides to strobe the WE signal, he would have to wait for at least:

– $T_{WZ} + T_{DW}$ (Write Enable to output in high Z+ data valid to end of write)

if the user decides to strobe the CS signal, he would have to wait only for:

– T_{WP} (Write Pulse width)

– And generally ------->$T_{WZ} + T_{DW} \geq T_{WP}$

2. WE Controlled Write

An additional timing requirement is to wait for the drivers to turn off at the beginning of the write.

3. CS Controlled Write

In a Chip Select controlled write, the designer does not have to wait for the drivers to turn off.

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TIMING FOR CONTINUOUS READ

Let us now take a look at the read cycles of a common I/O device. Again, they are not really different from the separate I/O case. Figure 14 shows the read cycle for continuous enabled write.

In this cycle, it is assumed that the IC is continuously selected and that the addresses are changing at a certain rate. The data is being read after an appropriate wait after each address transition.

TIMING WAVEFORM OF READ CYCLE NO. 1

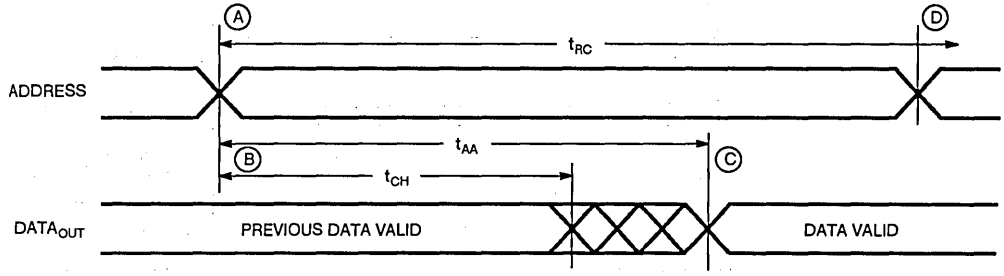

Figure 14. Timing Waveform for Read Cycle No. 1

In a continuously enabled read cycle, $\overline{CS}$ is active, therefore the IC is selected and $\overline{WE}$ signal is high—putting the IC in the read "mode" by turning off the output drivers. Let us examine Figure 14 step by step:

- Bring the address bits to the IC address pins. The read cycle time is t_{RC} parameter during which the address remains constant.
- At this point the previous data is still valid on the bus. This data is going to stay valid for t_{OH}, which is the output hold from address change time.
- At this point the valid data will appear at the pins. T_{AA} is the IC access time and is the amount of time that has to pass since the address transition for the valid data to appear at the pins.
- At this point the IC is ready for a new address.

TIMING FOR CS CONTROLLED READ

Let us now take a look at Figure 15, which shows the timing of a single read operation.

TIMING WAVEFORM OF READ CYCLE NO. 2

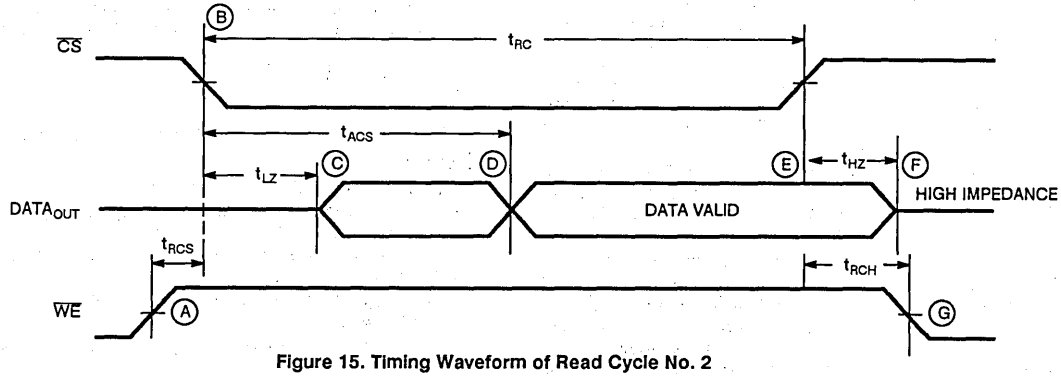

Figure 15. Timing Waveform of Read Cycle No. 2

- $\overline{WE}$ goes high, putting the IC in a read "mode". The read command set-up time is t_{RCS}. At this point the IC is ready to turn on the output drivers as soon as the $\overline{CS}$ (Chip Select) signal becomes active.
- The $\overline{CS}$ signal makes a high-to-low transition, therefore becoming active. The read cycle time is t_{RC} and represents the amount of time that this signal has to stay active.
- The Chip Select to Output in low impedance state is t_{LZ}. This shows that t_{LZ} time after the $\overline{CS}$ high-to-low transition, the output drivers will be on.
- The Chip Select access time is t_{ACS}. This shows the amount of wait necessary after the high-to-low transition of the $\overline{CS}$ signal before the valid data will appear at the output pins.

- Terminate the strobe. This will start turning off the output drivers. At this point the $\overline{CS}$ signal will become inactive. The valid data will be present for only t_{HZ} time, the Chip Deselect to Output in High Impedance time is t_{HZ} parameter.
- From this point on, the output drivers are turned off.

CONCLUSION

To get a better understanding of the timing for read or write operations, this application note went through an overview covering a range of subjects.

To start, a RAM cell and its operation was presented. Then, the way of achieving an array of RAM by interconnecting the different RAM cells was shown.

There are two different sorts of RAMs: Separate I/O and Common I/O. The application note went through a complete explanation of read and write operations for these different types with concrete examples.

There are two different ways of writing into the memory: Chip Select controlled Write and Write Enabled controlled write.

While writing to a common I/O device, it is generally faster to use the Chip Select controlled write.

The use of all RAMs is very similar and generally, if the guidelines of this paper are followed, the operations will be accomplished successfully.

Integrated Device Technology, Inc.

PERFORMANCE ADVANTAGES WITH IDT's FLAGGED FIFOS

APPLICATION NOTE AN-22

By Danh Le Ngoc

INTRODUCTION

The most common application for the FIFO is an elastic data buffer between two synchronous or asynchronous systems for the purpose of passing data.

Because data is produced and accepted at different rates, it is important to monitor the boundary conditions (FULL or EMPTY) of the data buffer. Failure to act on the boundary conditions will result in data overflow or underflow. The current FIFO generation, such as IDT7201/02/03/04, signals the empty, half-full and full condition by asserting the $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$, respectively. The empty and full flags are also fed back internally and inhibit further Read and Write operations until the FIFO is no longer empty or full.

The increasing use of high-speed CMOS, coupled with the introduction of the 32-bit CPU, has created the demand for a faster and smarter generation of FIFOs. New Flagged FIFOs offer the basic features of IDT's industry standard FIFOs (IDT7201/02/03/04) while providing two new flags: ALMOST-EMPTY and ALMOST-FULL. These flags can be used as early warning flags in critical real-time applications such as data acquisition, high-speed data link and pipeline Digital Signal Processing applications. In the multi-tasking environment, the ALMOST-EMPTY and ALMOST-FULL can also be used to set the interrupt request in advance, so that the CPU has sufficient time to perform the task switch without loss of data due to the task switch latency. Other advantages of these Flagged FIFOs are an increase in memory utilization and the Three-State Control, $\overline{OE}$, for the outputs (Q0-8). The use of independent Three-State Control simplifies the interface with bus and I/O channels and improves timing in read and write cycles. Figure 1 is a block diagram of the new Flagged FIFOs: IDT72021/31/41.

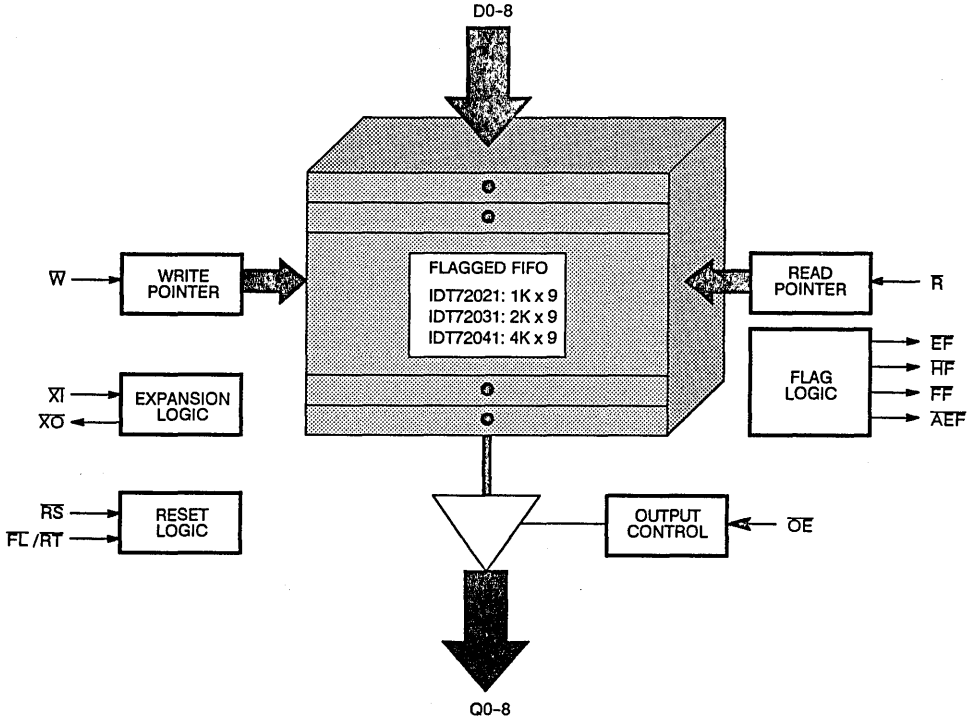

Figure 1. Simplified Block Diagram for Flagged FIFOs

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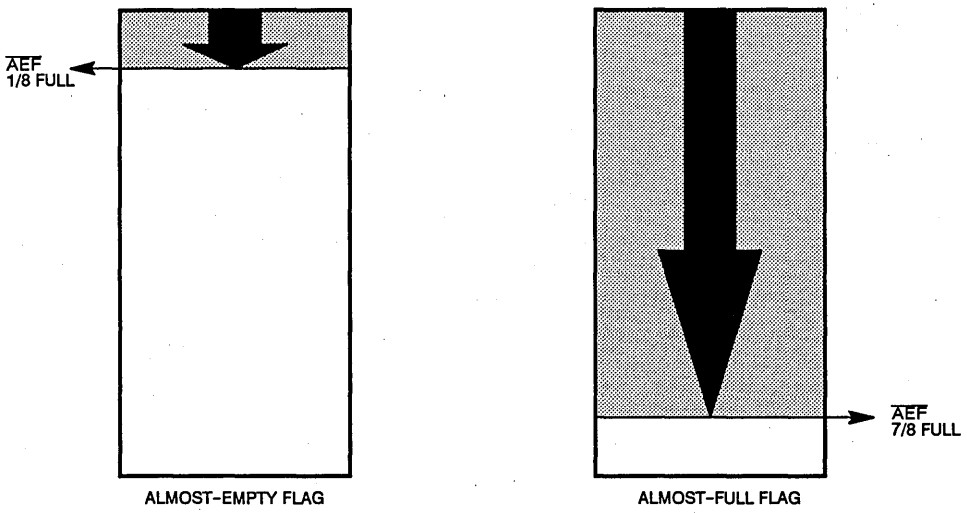

Figure 2. Almost-Empty and Almost-Full Flags on the IDT72021/31/41

APPLICATIONS USING THE FLAGGED FIFOS

Typical applications using the new features of the Flagged FIFOs are demonstrated below.

- **ALMOST-EMPTY AND ALMOST-FULL FLAG AS EARLY WARNING FLAGS IN REAL-TIME DIGITAL SIGNAL PROCESSING APPLICATIONS**

  Figure 3 is a simplified block diagram of a real-time spectrum analyzer featuring A/D channels, input buffer, FFT processor, display processor, output buffer and CRT. In operation, the DSP engine processes on the previous frame of data at the 50 MHz rate, while the A/D channel samples the analog signal at the comparatively slow rate of 20 MSPS. This data rate mismatch requires the use of a FIFO to act as an elastic data buffer. To prevent data overflow, the ALMOST-FULL flag is used as an early warning to the DSP controller. With this signal, the DSP engine has sufficient time to empty the input buffer (FIFO) into the buffer at its own high-speed data rate. Meanwhile, the A/D channel continues to refill the input buffer from other side at its much slow rate. At the other end of the system, a second FIFO acts as an output buffer between the high-speed display processor and slow CRT. In this case the ALMOST-EMPTY FLAG is used as an early warning so that the display processor can begin filling the buffer with the next image.

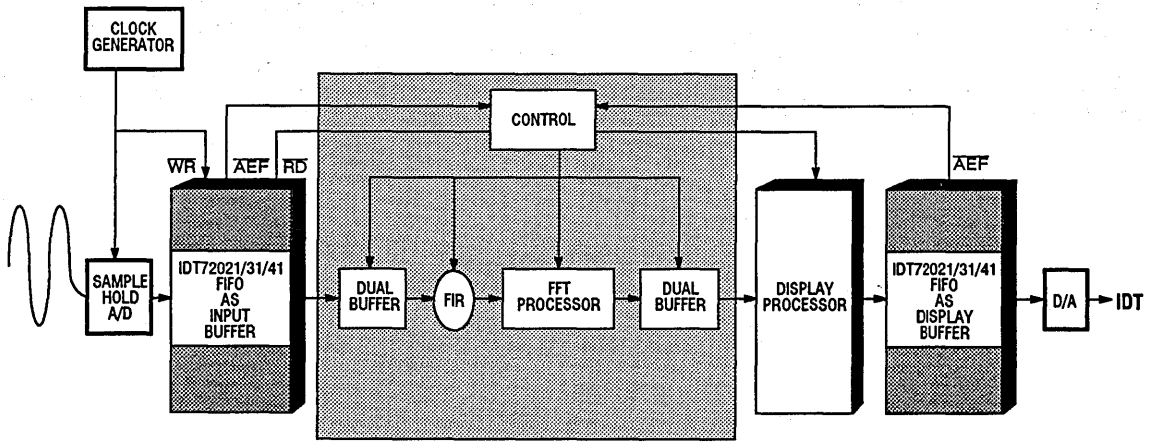

Figure 3. Simplified Block Diagram for a Real-Time Spectrum Analyzer

- **MAXIMUM UTILIZATION OF MEMORY WITH THE ALMOST-FULL AND ALMOST-EMPTY FLAGS IN HARD DISK DRIVE APPLICATIONS**

  Because of the high data rates used in the hard disk drive protocols, SMD, SCSI and IPI or the standard data communication protocols (Ethernet, Supernet and Fiber-optics which can go up to 100 Mbits per second), even the newer and faster microprocessors will struggle to keep up with the speed of I/O channels. For this reason, data buffering is always considered in any high-speed I/O transfer. The design in Figure 4 shows the data buffer for a high-speed hard disk application. In such CPU-to-I/O controller applications, FIFOs are often used to construct the data buffer. Normally two sets of FIFOs are arranged in the back-to-back manner, where one set acts as a transmit buffer and the other as the receiver buffer. In this arrangement, the CPU dumps data in the transmit FIFO until the FIFO is 7/8 full. At this point, the FIFO sets the Almost-Full Flag, initiating the data transfer to the I/O channel at its higher speed rate. In similar fashion, the high-speed I/O channel dumps data into the receiver FIFO until it is almost full. In this case, the Almost-Full Flag triggers an interrupt request to the host processor or DMA request to the DMA controller. If the request goes to the DMA controller, the DMA channel can transfer the entire block of data into the system memory in one burst. Figure 4 illustrates a host interface between a 32-bit microcomputer system based on an Intel 80386 and a Disk Drive.

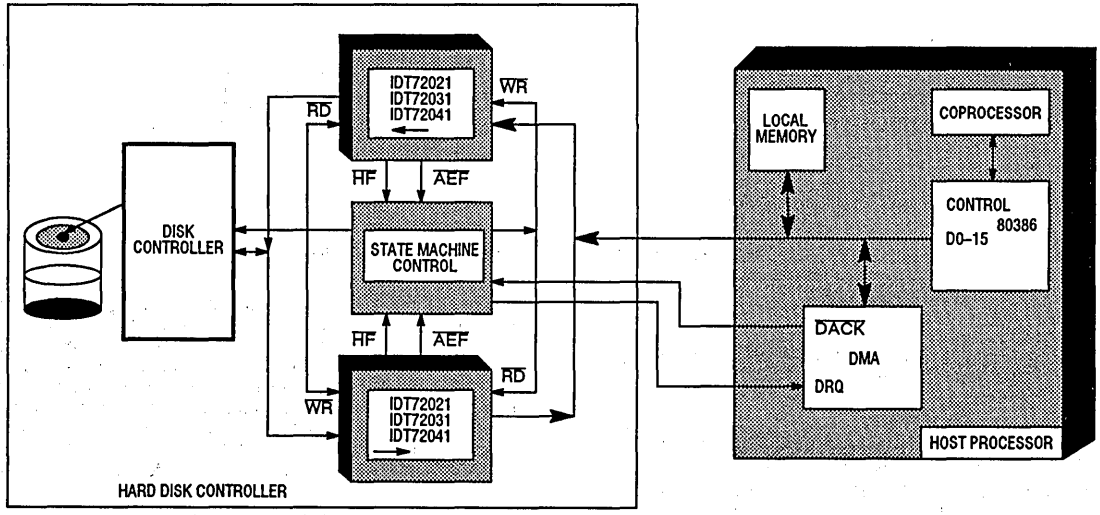

Figure 4. Block Diagram of a Disk Drive Controller

- **ASYNCHRONOUS THREE-STATE CONTROL**

  Another common use for FIFOs is as a data buffer between a microcomputer and high-speed I/O bus for the purpose of passing data back and forth. The figures on the next page illustrate two examples of the interface between a 32-bit processor and the I/O channel of the IBM PC AT, one using FIFOS without three-state control and the other using FIFOs with their three-state control. As Table 1 indicates, using the new Flagged FIFOs with their three-state control pin produces faster read and write cycles. An additional advantage is the ability to repeat a reading from the same FIFO location without advancing the read pointer.

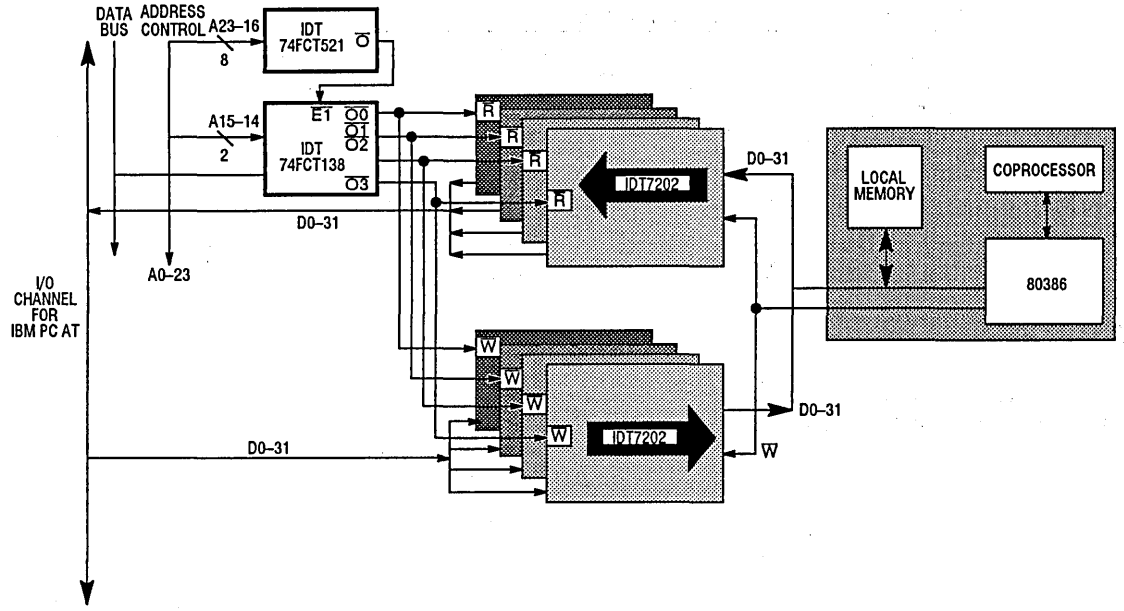

Figure 5. IDT7202 FIFOs Without Three-State Control as a Data Buffer Between IBM AT and an Accelerator Board

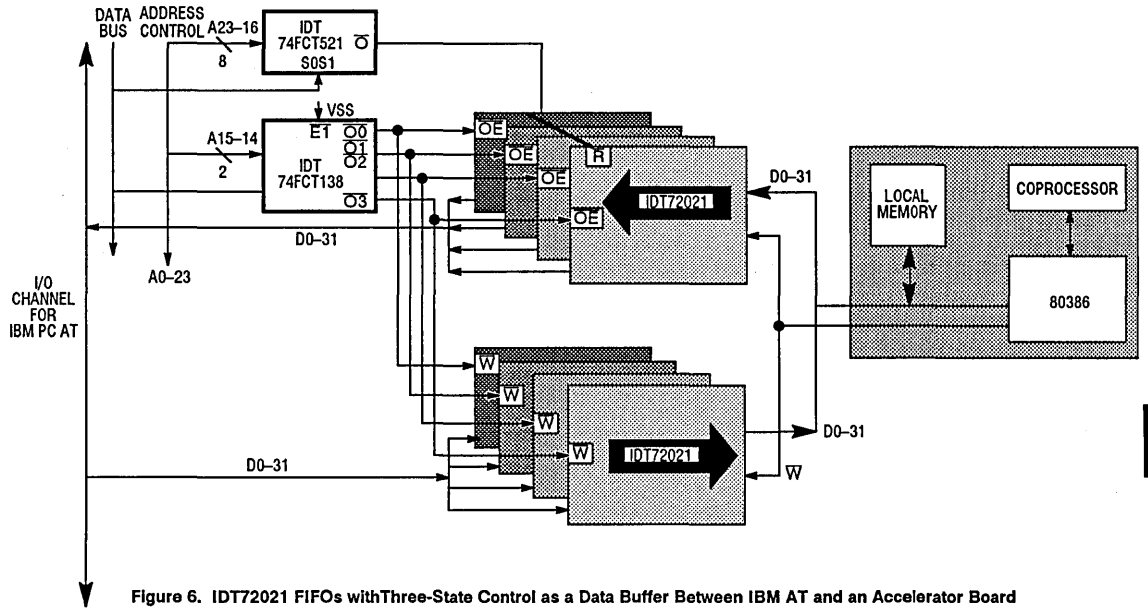

Figure 6. IDT72021 FIFOs withThree-State Control as a Data Buffer Between IBM AT and an Accelerator Board

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Table 1. Read and Write Cycle with IDT7202/021

DELAYS PATHS	WITHOUT THREE-STATE CONTROL	WITHOUT THREE-STATE CONTROL
IDT74FCT521A: TPLH	7.2ns	0.0ns*
IDT74FCT138A: TPLH	9.0ns	9.0ns
IDT7402/021: TRC	35.0ns	35.0ns
TOTAL	**50.2ns**	**44.0ns**

*Although this propagation delay is specified at 7.2ns, it occurs in parallel with the slower 9.0ns propagation delay of the IDT74FCT138A and is not additive as is the case in the "without three-state control" application.

CONCLUSION

As the need for high-speed data computation increases, the FIFO must also become faster and smarter. The next generation of FIFO, as exemplified by the IDT72021/31/41, meets that challenge.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE FIXED-POINT FAST FOURIER TRANSFORM PROCESSOR

APPLICATION NOTE AN-23

By Julie Lin and Danh Le Ngoc

Some digital signal processing applications involve large amounts of data requiring very fast, real-time processing. In these cases, convolution in the time domain is too time consuming and is usually replaced by the frequency domain multiplication. The use of an FFT processor in a pipelined architecture meets the high-speed computation requirements for this class of applications. Typical application areas include:

- Digital Image Processing—Image compression, used for communication and storage, can be done in the Fourier transform domain. FFT processing has been successfully applied to image deblurring for motion blur and optical aberrations. Reconstruction from projections requires two-dimensional FFT processing.
- Radar Signal Processing—Doppler frequency determination for ambiguities is done in the frequency domain. Implementation of the critical digital match filter requires a high-speed FFT processor. When the detection processor encounters a large number of targets or clutter, a special kind of postprocessor is required, which is implemented with a small, fast FFT system. The moving target indication in air traffic control uses a bank of FFT-implemented bandpass filters. The sophisticated computation of signal compression used for synthetic aperture radar also needs the power of FFT processing.
- Sonar Signal Processing—In active sonar systems, the user transmits the acoustic energy. The energy is observed after it has propagated through the water and is reflected by a target. Uses include target detection, communications, navigation, mapping and charting. The signal processing methods used in active sonar signal processing have much in common with radar. As such, the detector processors are also implemented with FFT-based algorithms for building match filters and detecting ambiguities. With passive sonar systems, one listens to signals that are radiated by various sources of acoustic energy in the ocean. Some of these sources are natural, arising from wind, earthquakes, and marine life. The signals of most interest are man-made by shipping and military vessels. The most important use of passive sonar is in surveillance systems. Spectral analysis and array processing are the main signal processing elements of a passive sonar system and both are prime candidates for FFT processing.

The fixed point implementation of an FFT processor can be used to meet the very high performance requirements of some special-purpose systems, where the dynamic range has been carefully studied to prevent overflow problems. The IDT7317 (multiplier) and IDT7384 (ALU) are new building blocks with architectures optimized for fast pipeline digital signal processing (DSP) applications. With IDT's high-performance submicron CEMOS technology, both chips have low power consumption and very fast (20ns) clock cycle time.These two powerful ICs make it very easy to implement a high-speed FFT processor. This application note gives a brief introduction to the IDT7317 and the IDT7384, after which the general architecture of the FFT processor is described. Within the processor are several basic function blocks: control unit, butterfly unit, address generator, input and output buffers, and the coefficient look-up tables. Further explorations detail the design of the control and butterfly units. We also consider the data addressing problem. The performance for 1024-point complex FFT is discussed. Appendix A contains the description of DFT and FFT algorithm.

FEATURES OF THE IDT7317 AND IDT7384

The IDT7317 is a fixed point 16-bit x 16-bit parallel multiplier with a 32-bit output. Multiplier operations include unsigned, two's complement and mixed-mode multiplications for both integer and fractional numbers. A functional block diagram for the IDT7317 is shown in Figure 1. It features a flexible output scaling shifter and pipeline or flow-through operational modes. Figure 2 is the functional block diagram of the IDT7384 16-bit ALU, which can be cascaded to form a 32-bit ALU. In addition to 32 basic ALU functions, an on-chip funnel shifter performs flexible scaling functions. On-chip merge capability is also provided. Input data on A0-15 and B0-15 can be fetched directly by the ALU or shifter in the flow-through mode or stored in the pipeline registers. Data path B has a single register, but Data path A can be optimized to match pipelined DSP systems with depths to 4 levels. The ALU or shifter result is fed into one of three output registers and can then go into either the internal feedback path for accumulation or through final stage manipulations. Available manipulations include shifting, rounding, bit-reversing, and flow-through. The output shifter is used for scaling. Rounding can be done on either bit 14 or bit 15 of the Least Significant Slice. The bit-reversing scheme is particularly suited for FFT processing on data lengths of 1K, 4K, 16K, and 64K. Both the IDT7317 and the IDT7384 are housed in 84-pin packages.

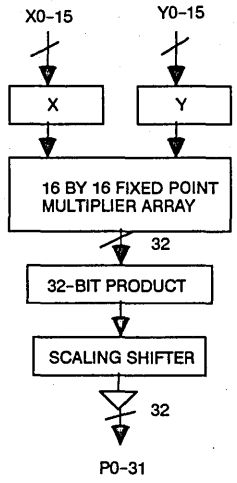

Figure 1. Functional Block Diagram of the IDT7317

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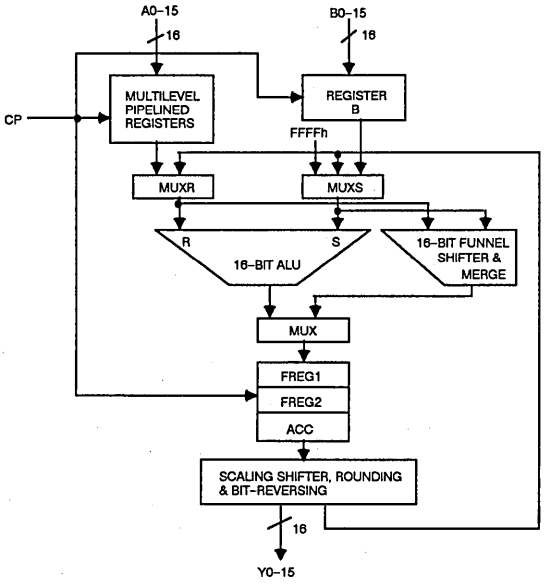

Figure 2. Functional Block Diagram of the IDT7384

GENERAL ARCHITECTURE

As shown in the block diagram of Figure 3, the FFT processor is composed of six basic blocks. The control unit contains the horizontally micro-coded program, which controls all the other blocks in parallel. Initially, a macro-instruction is fetched from the host processor. The opcode is then decoded and used as the jump-address to the microprogram. By executing a sequence of micro-instructions, the microprogram emulates this macro-instruction. All internal tasks, such as address generation, input-buffer access, table look-up, butterfly execution, and writing the result to the output-buffer, are controlled by these micro-instructions. All of these tasks are executed in a pipelined manner.

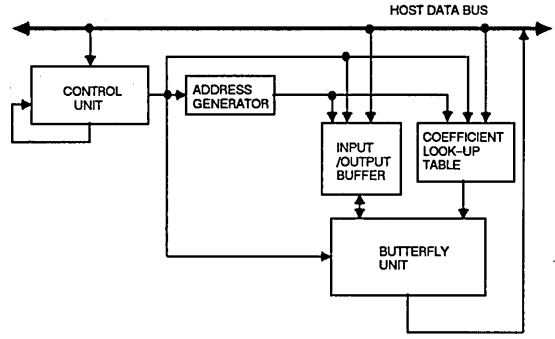

Figure 3. The Basic Block Diagram of an FFT Processor

CONTROL UNIT

The control unit coordinates the entire FFT engine. It consists of a high-speed 12-bit sequencer, IDT71502 Registered RAMs for microcode storage, and a multiplexer for condition code selection (Figure 4). The IDT71502 is a registered RAM with a high-speed pipeline register at the output and serial load and read capability using the IDT Serial Protocol Channel (SPC). FFT microprograms can be loaded through the SPC and executed in real time. An octal register (IDT49FCT818A) is inserted between the sequencer and the writable control store (WCS) to provide pipelining. Table 1 summarizes the control unit's worst case propagation delay time if the multiplexer is implemented with a 74F151 and the sequencer with an IDT39C10. It is clear that the propagation delay from register to WCS dominates the timing consideration of the whole control unit. 45ns is the clock cycle requirement of the control unit.

Table 1. The Worst Case Propagation Delay Time Within the Control Unit

• Condition Multiplexer 74F151	9ns
• Sequencer IDT39C10	16ns
• Input set up time of IDT49FCT818A	2.5ns
• Total	27.5ns
• Propagation delay of IDT49FCT818A	10ns
• WCS IDT71502	35ns
• Total	45ns

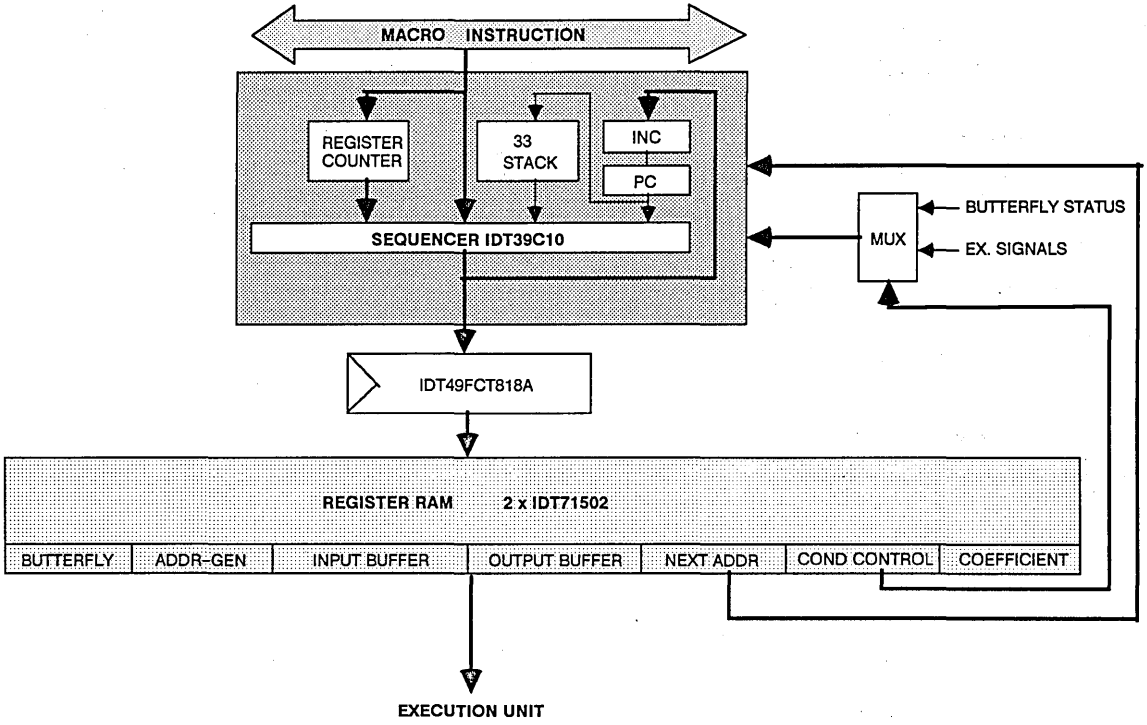

Figure 4. Block Diagram of the Control Unit

BUTTERFLY UNIT

As discussed in Appendix A, the butterfly units execute the heart of the FFT computation, consisting of four multiplications, three additions and three subtractions. The signal flow graph of the butterfly computation is shown in Figure 5a, where the input variables are denoted as *C* and *D* and the output variables as *G* and *H*.

With the twiddle factor represented as $W^k = e^{j\theta} = \cos\theta + j\sin\theta$, the relationship between butterfly input and output is redrawn in Figure 5b to separate the real and imaginary parts of complex numbers.

Because the butterfly computation is highly repetitive, implementation of the FFT algorithm lends itself to a pipelined structure. This section presents four different implementations of the butterfly unit, using the IDT7317 multiplier and IDT7384 ALU. Their designation—six-cycle, four-cycle, three-cycle, and single-cycle—reflect the clocked cycle time that each needs to complete an entire butterfly computation.

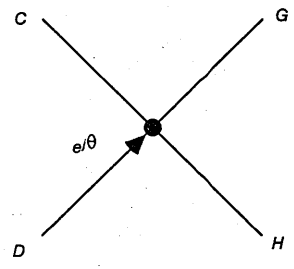

Figure 5a. The Signal Flow Graph of a Butterfly With One Complex Multiplication and Two Complex Additions

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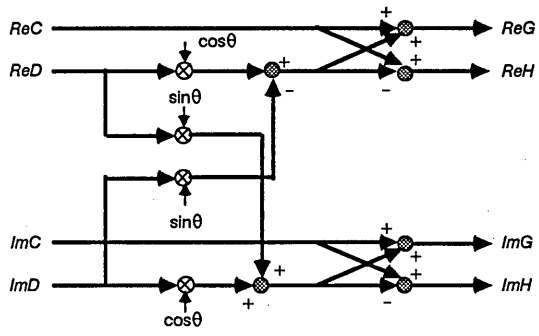

$$G = C + e^{j\theta} \bullet D$$
$$H = C - e^{j\theta} \bullet D$$

$$ReG = ReC + (ReD \bullet \cos\theta - ImD \bullet \sin\theta)$$
$$ReH = ReC - (ReD \bullet \cos\theta - ImD \bullet \sin\theta)$$
$$ImG = ImC + (ImD \bullet \cos\theta + ReD \bullet \sin\theta)$$
$$ImH = ImC - (ImD \bullet \cos\theta + ReD \bullet \sin\theta)$$

Figure 5b. The Signal Flow Graph of a Butterfly With Four Real Multiplications and Six Real Additions

The six-cycle butterfly unit needs only one IDT7317 and two cascaded IDT7384s, which form a 32-bit ALU (Figure 6). The addition of two consecutive results from the IDT7317 is accomplished by using the B register of the IDT7384's input path B. In addition, the three output registers can be used to hold temporary data which is fed back to the ALU as input for the next two addition cycles. Thus, the ALU performs the six additions in six continuous cycles. The pipeline is kept full as each succeeding butterfly computation is performed. Figure 7 shows the timing diagram of a complete six-cycle butterfly, where *ReG* and *ReH* outputs are at clock 5 and clock 6, *ImG* and *ImH* outputs are at clock 8 and clock 9.

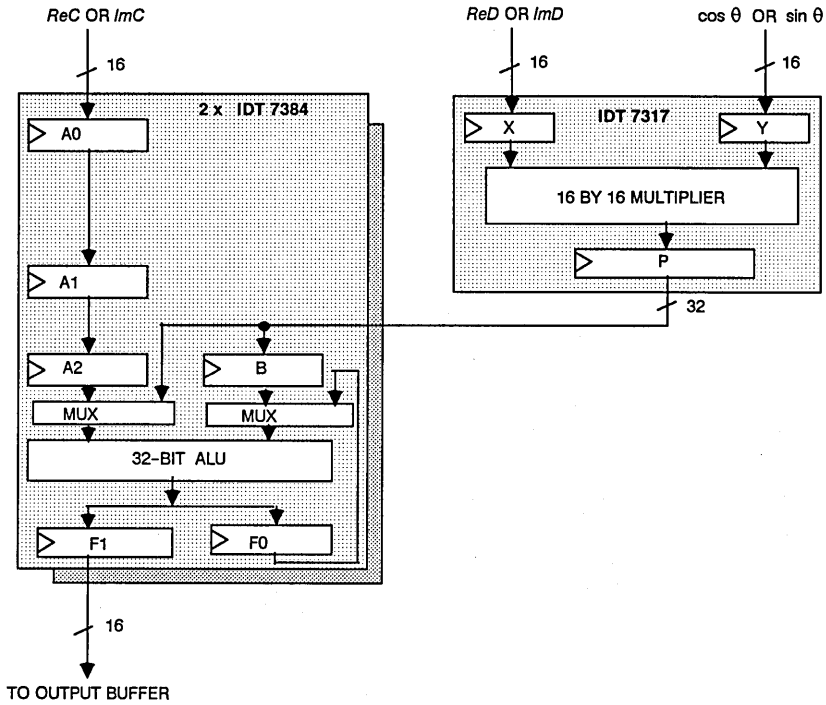

Figure 6. Six-Cycle Butterfly

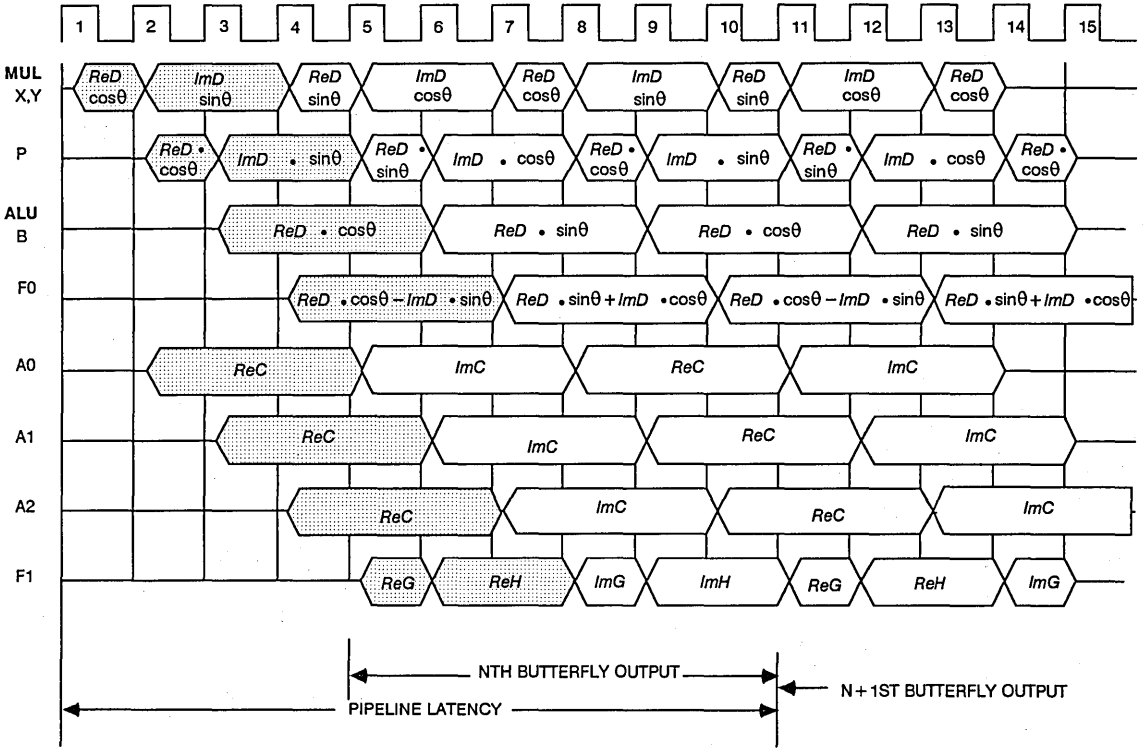

Figure 7. The Timing Diagram of Six-Cycle Butterfly

The four-cycle butterfly has one multiplier and two 32-bit ALUs (Figure 8). One of the ALUs handles the operations for *ReG* and *ReH*. The other one takes care of *ImG* and *ImH*. The timing diagram in Figure 9 shows that four clock cycles are required at the beginning to fill the pipeline. Starting from clock 5, we get the results of *ReG* and *ReH* from one ALU output. The results of *ImG* and *ImH* from the other ALU are at clock 7 and clock 8. At clock 9 we will expect the result of *ReG* from the next butterfly computation.

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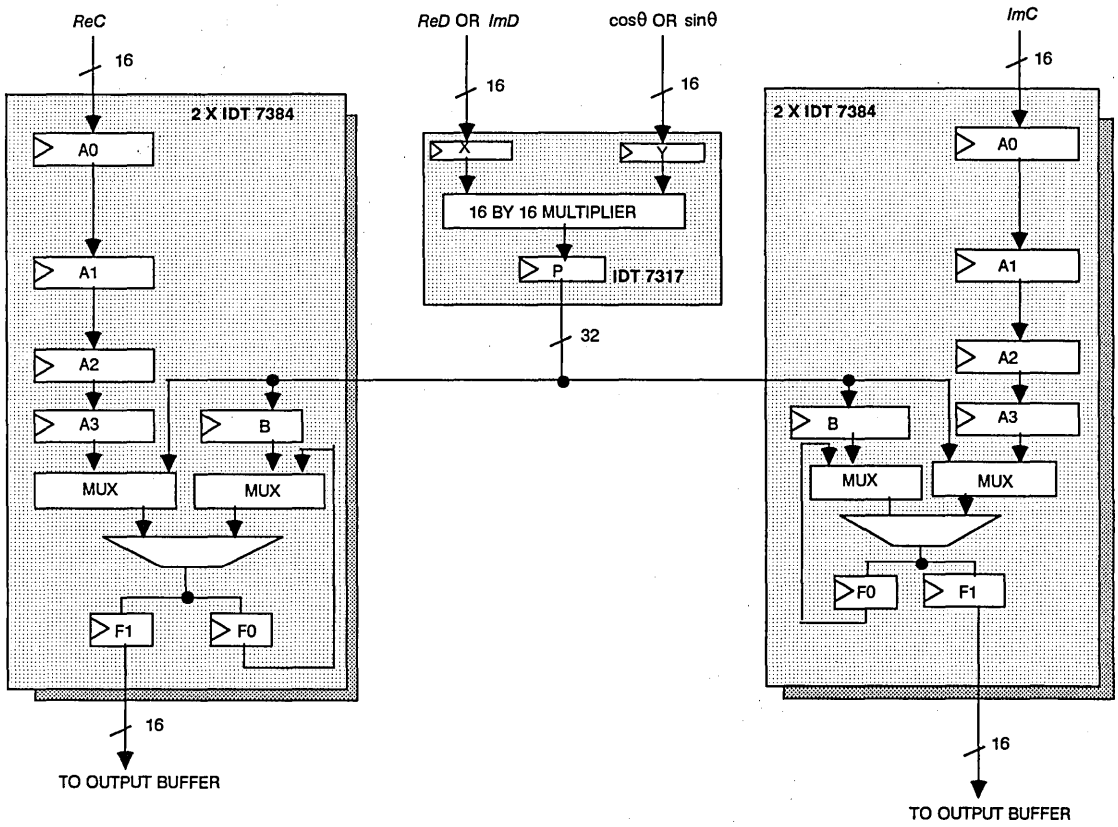

Figure 8. Four-Cycle Butterfly

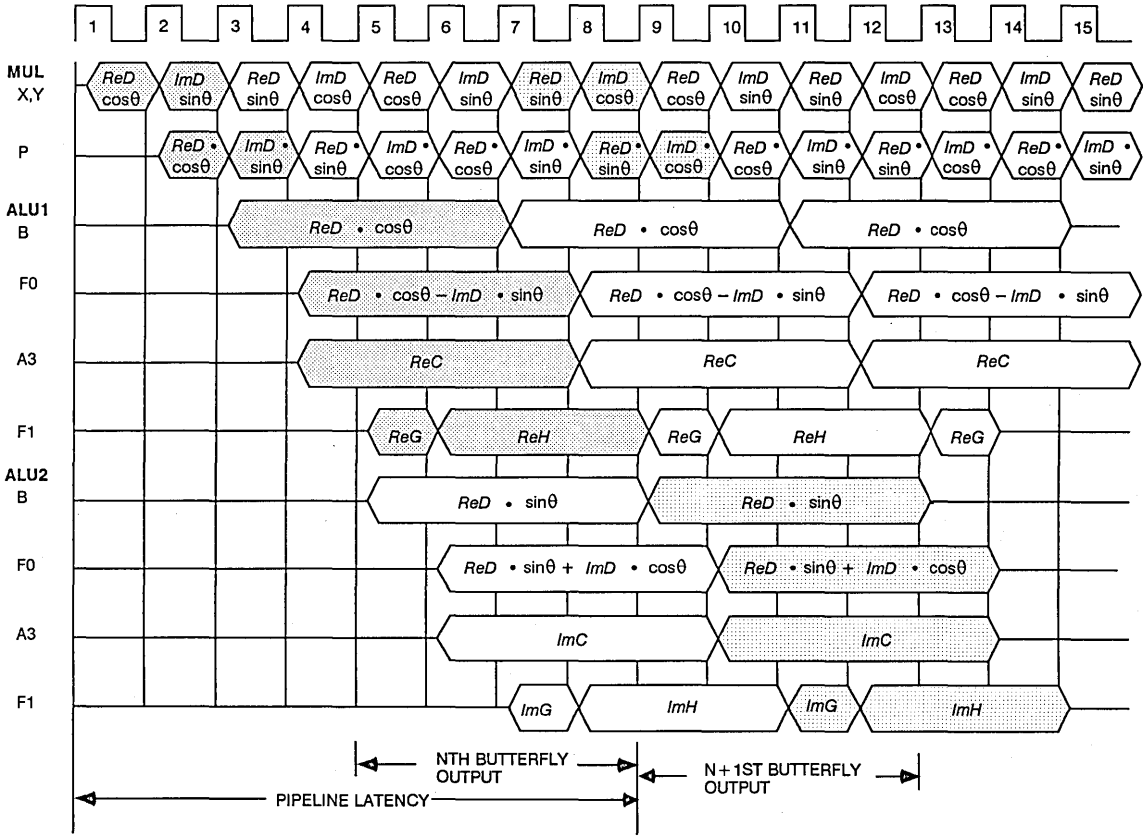

Figure 9. The Timing Diagram of Four-Cycle Butterfly

The three-cycle butterfly requires the addition of one more multiplier (Figure 10). One multiplier and one ALU form one independent data path, one for *ReG* and *ReH*, the other for *ImG* and *ImH*. These two data paths proceed in parallel (Figure 11). Therefore, the results of *ReG* and *ReH* from different ALUs come out at the same time—at clock 5. At clock 6 we get the results of *ReH* and *ImH*. However, *ReG* and *ImG* from next butterfly should wait for one more cycle because the ALUs are dedicated to the previous stage operations, i.e. *ReD* $\cos\theta$ - *ImD* $\sin\theta$ and *ReD* $\sin\theta$ + *ImD* $\cos\theta$. It is clear that the three-cycle is formed because of this waiting cycle.

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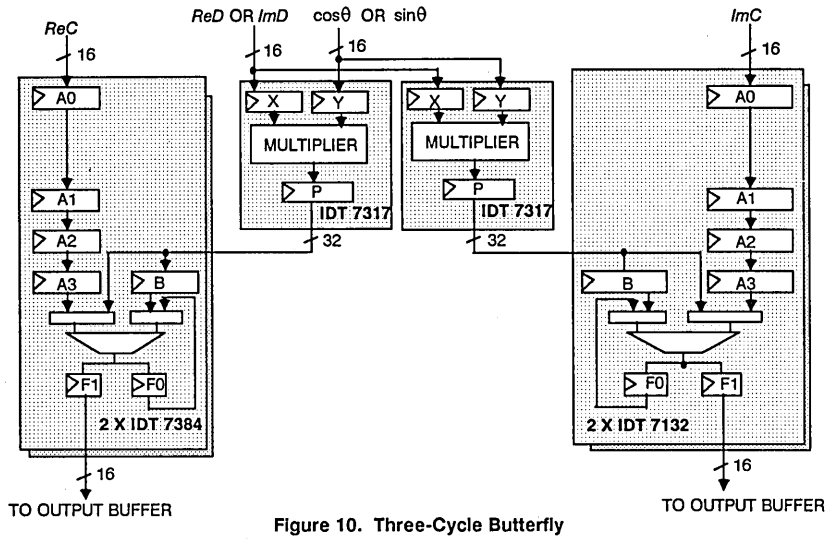

Figure 10. Three-Cycle Butterfly

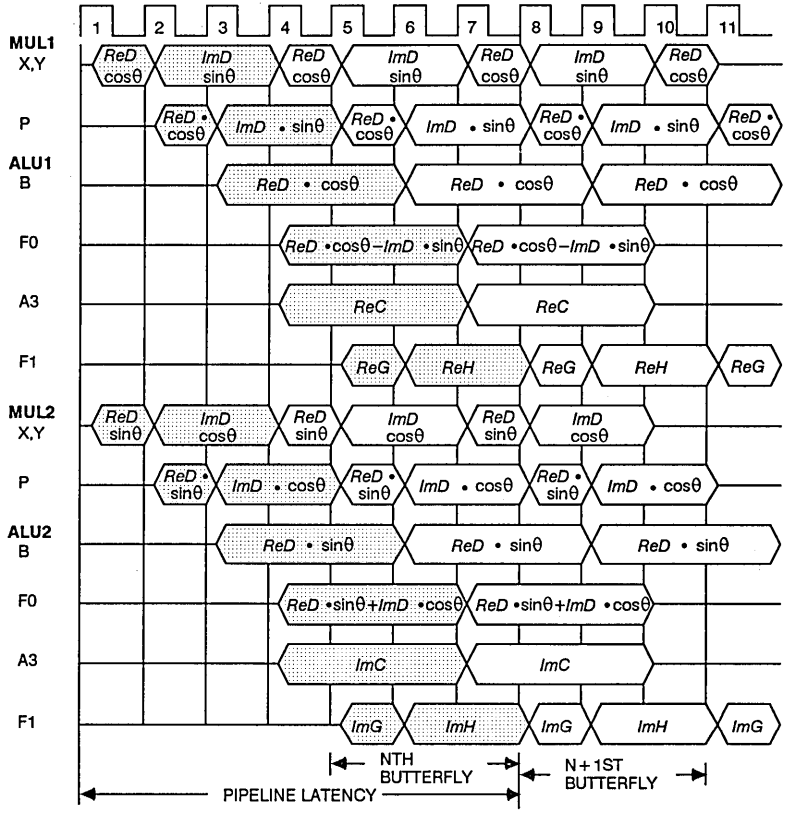

Figure 11. The Timing Diagram of Three-Cycle Butterfly

The high-speed single-cycle butterfly is achieved by assigning a hardware element to each operation, i.e. four multipliers and six ALUs for one butterfly unit (Figure 12). The pipeline is now filled in just two cycles and generates outputs *ReG*, *ReH*, *ImG*, and *ImH* in every clock cycle thereafter (Figure 13). Since two IDT7384s are cascaded to perform 32-bit operations, 40ns is required to finish one addition or subtraction.

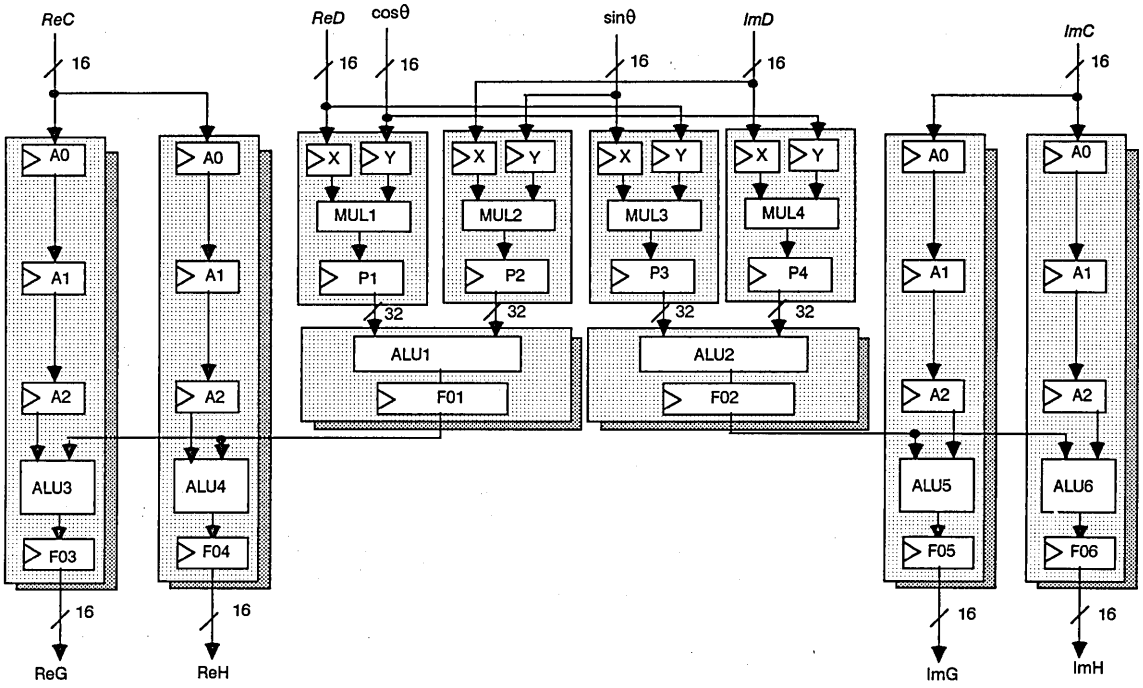

Figure 12. Single-Cycle Butterfly

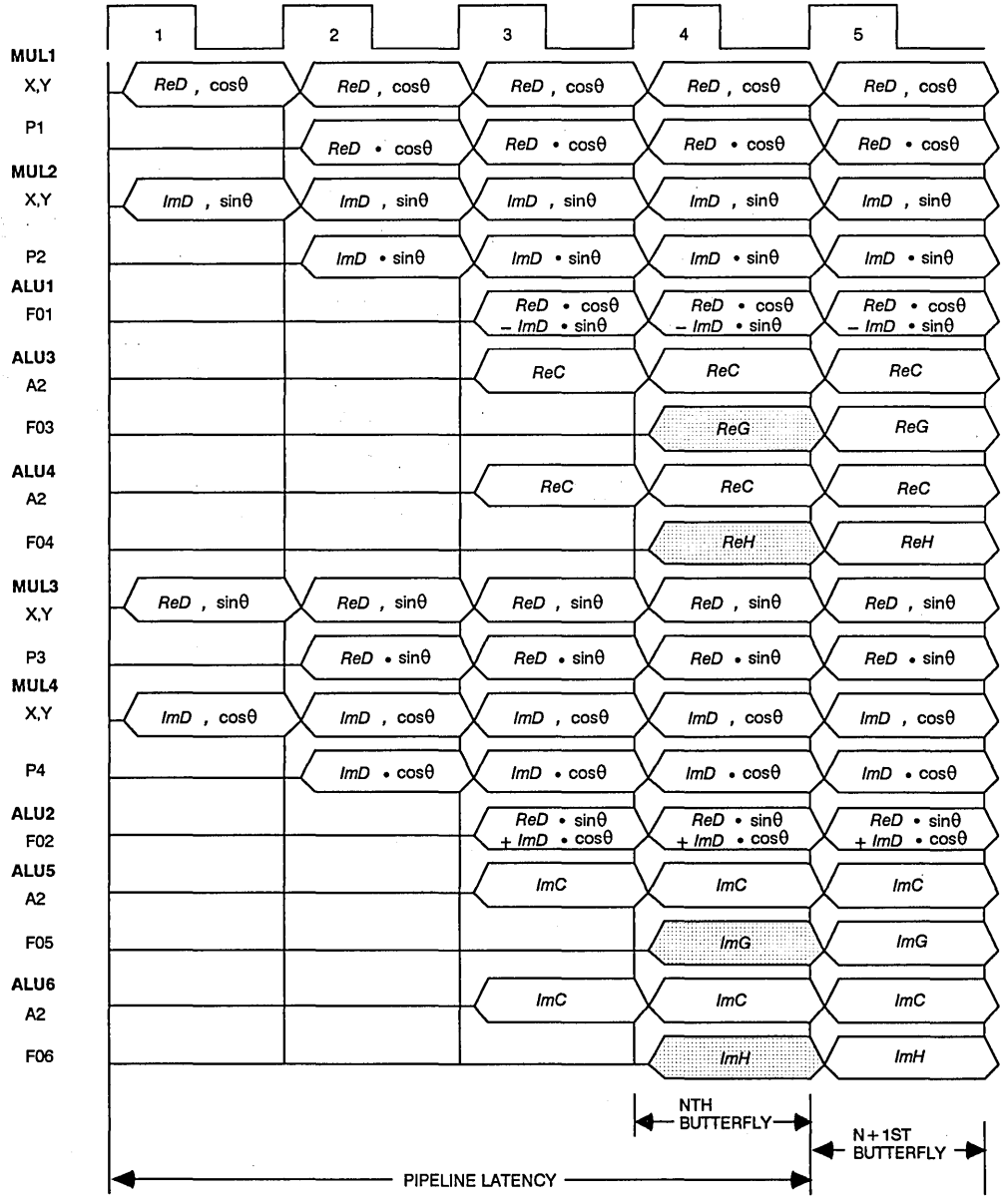

Figure 13. The Timing Diagram of Single-Cycle Butterfly

ADDRESSING AND MEMORY DESIGN

Since the butterfly output rate can be as fast as 40ns, the memory access time should match this speed. The two IDT71502 registered RAMs were selected to implement the SINE and COSINE look-up tables based on their speed (35ns). Furthermore, the on-chip Serial Protocol Channel (SPC) allows user to load WCS and look-up tables simultaneously with the same serial input set-up. Both in-place and not-in-place computations require "bit-reversed" addressing in the input sequence for correctly ordered output results. This is easily accomplished with the special "bit-reversing" feature of the IDT7384, for data lengths of 1K,4K,16K, or 64K. Hence, the IDT7384 is used as the address generator.

In the in-place computation, the butterfly outputs are stored back into the same storage locations (Figure 20). The drawback of this method is the complicated addressing scheme, because the addresses of the memory locations for each butterfly computation vary from stage to stage. Figure 14 shows the memory organization for the in-place computation.

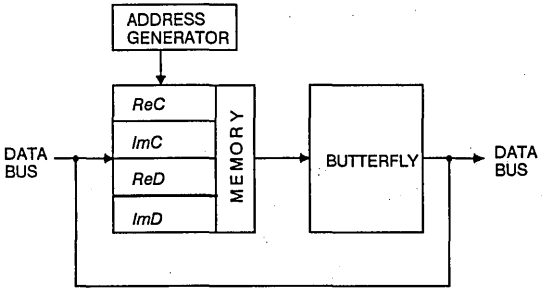

Figure 14. Memory Allocation For the In-Place Computation

As the not-in-place computation of Figure 22 (in Appendix A) shows, the outputs of the butterfly are not put back where they came from. Since the butterfly span for input and output is kept constant from stage to stage, a simple and constant addressing method can be used to select data for each butterfly in all stages. The block diagram in Figure 15 illustrates the memory implementation for the not-in-place algorithm. However, the butterfly outputs stored in *ReG*, *ImG*, *ReH*, and *ImH* are not in one-to-one correspondence with the next stage input storage *ReC*, *ImC*, *ReD*, and *ImD*. Eight dual-port RAMs are used for input and output buffers—four for input and four for output. So, the output results can be put back to the proper input buffers once they are generated. This kind of data shuffling operation has to be done before the next-stage butterfly computation starts. The memory implementation with dual-port RAMs and pipeline structure make this requirement feasible. The pipeline for butterfly computation from one stage to another stage will not be interrupted.

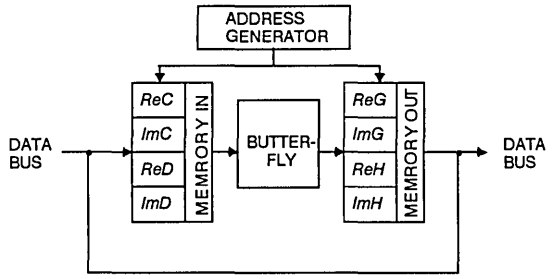

Figure 15. Memory Allocation For the Not-In-Place Computation

If we use the dual-port RAM IDT7132 and IDT7142 as the input/output buffers, the memory delay time for one butterfly computation is calculated in Table 2.

Table 2. Memory Delay Time For One Butterfly Computation

• Output delay to the clock on IDT7384	18ns
• T_{WC} or T_{RC} of the IDT7132/42	35ns
• Input setup time for IDT7317/7384	5ns
• Total	58ns

CONCLUSION AND PERFORMANCE

This application note has introduced a high-speed CMOS FFT solution for a class of DSP applications that require very high-speed processing, such as imaging processing, radar and sonar signal processing. Fast (20ns) IDT7317 multipliers and IDT7384 ALUs are used to build the butterfly unit. The IDT7384 is also used for address generation. The SINE and COSINE look-up tables use the IDT71502 registered RAM. Input and output buffers are made up of IDT7132/42 dual-port RAMs. The control unit consists of an IDT39C10 sequencer and an IDT71502-based WCS. Figure 16 illustrates the complete hardware implementation for the high-speed fixed-point FFT processor.

Three factors affect the pipelined system performance: the signal delay time of the control unit (45ns), the memory delay time of the input register (58ns), and the butterfly computation time, which is 40ns for a single-cycle butterfly implementation. Since the memory access delay path is the longest, the 58ns delay time determines the pipeline clock for the whole system.

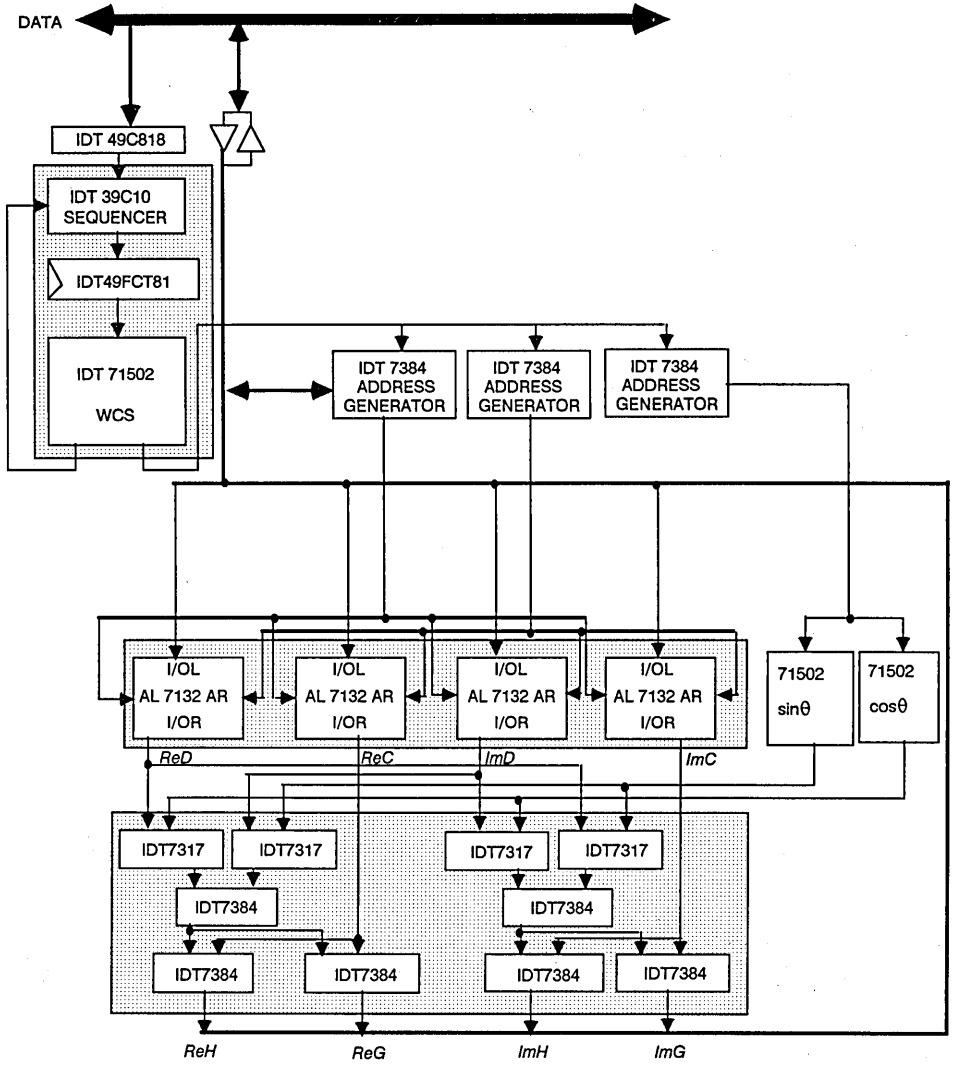

Figure 16. A Fixed-point FFT Processor With Single-Cycle Butterfly and In-Place Design Where Control Lines Are Not Shown

However, for a single-cycle butterfly, this critical memory delay can be reduced by replacing the 35ns IDT7132/42 dual-port RAMs with a pair of fast IDT71682 static RAMs (20ns) arranged in the ping-pong structure shown in Figure 17. In this approach, the butterfly unit reads data from the first RAM, and writes output data to the second RAM. Once a single stage FFT operation is done, then, by changing the state of the WE* input, the butterfly unit reads data from the second RAM and writes output data to the first RAM. In this fashion, one RAM is always in the read mode and the other is in the write mode.

The memory delay time now becomes 43ns, which moves the bottleneck to the control unit (45ns delay). Thus, the system clock cycle time for a single-cycle butterfly becomes 45ns. The system processing time for a 1024-point complex FFT, where 5120 butterfly computations must be made, will be 5120 X 45ns = 230μs.

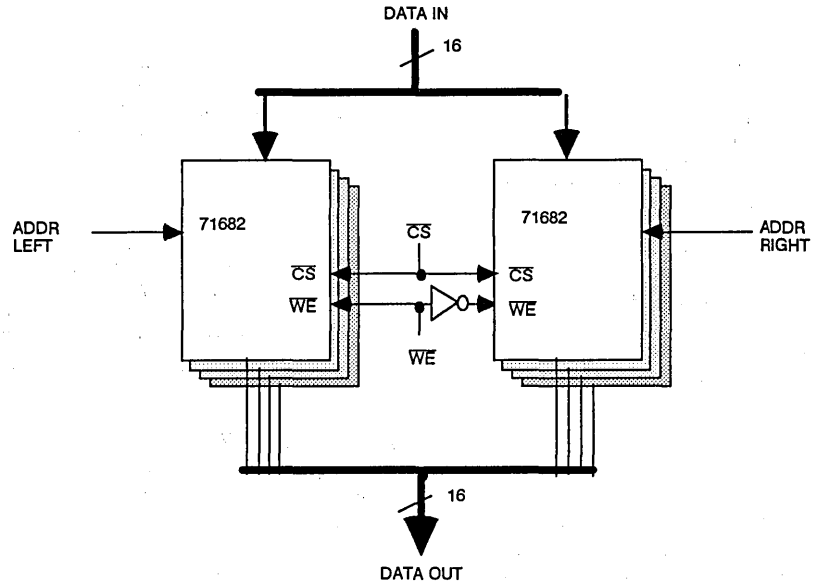

Figure 17. The Ping-Pong RAM Used to Replace Dual-Port RAM of Figure 16

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APPENDIX A

FOURIER TRANSFORM AND DFT

In general, transforms are used to simplify certain types of problems by moving them into a different domain in which analysis is much easier. Specifically, the Fourier transform is used to determine the frequency components of a time series by transferring the time domain signal into the frequency domain. In essence, the Fourier transform decomposes the signal into the sum of sinusoids of different frequencies. The result can be plotted as amplitude or phase angle versus frequency. An inverse transform converts the frequency analysis back to the time domain. Mathematically, the relationship is based on the pair of equations:

$$X(f) = \int_{-\infty}^{\infty} x(t) e^{-j2\pi ft}\, dt$$

$$x(t) = \int_{-\infty}^{\infty} X(f) e^{-j2\pi ft}\, df$$

where $x(t)$ is the signal to be decomposed into a sum of sinusoids and $X(f)$ is the Fourier transform of $x(t)$. Inherent properties of the Fourier transform help solve problems easily in the frequency domain. For example, time domain convolution is equivalent to frequency domain multiplication.

If the signal $x(t)$ is sampled at equally spaced intervals of Δ t to produce a discrete sequence $x_n = x(n\Delta t)$ for $-\infty < n < \infty$, then the Fourier transform may be written as:

$$X'(f) = \Delta t \sum_{n=-\infty}^{\infty} x_n e^{-j2\pi fn\Delta t}$$

$X'(f)$ will be identical in value to the transform $X(f)$ over the interval $-1/(2\Delta t) \leq f \leq 1/(2\Delta t)$ Hz, as long as $x(t)$ is band limited and all frequency components are in this interval.

If (a), the data sequence is only available from a finite time window over $n = 0$ to $n = N-1$, and (b), a discrete-value transform is constructed for N values by taking samples at the frequencies $f = m\Delta f$ for $m = 0,1,...,N-1$ where $\Delta f = 1/N\Delta t$, then one can develop the discrete Fourier transform (DFT) as:

$$X_m = \Delta t \sum_{n=0}^{N-1} x_n e^{-j2\pi mn/N} \text{ for } m = 0,...,N-1$$

For simplicity, the Δt sampling period, which is a constant, is factored out of the equation above to form the conventional DFT pair:

$$X_m = \sum_{n=0}^{N-1} x_n e^{-j2\pi mn/N}$$

$$x_n = \frac{1}{N} \sum_{m=0}^{N-1} X_m e^{j2\pi mn/N}$$

The DFT pair are both cyclic with period N. Thus by using the DFT, we have forced a periodic extension to both the discrete data and the discrete transform values, even though the original continuous signal may not be periodic. Based on a finite data set, the discrete Fourier transform, X_m, is a distorted version of the Fourier transform, $X'(f)$, which is based on an infinite data set. In the time domain, the finite data set $\{x_n, n = 0,...,N-1\}$ is equivalent to the multiplication of an infinite data set $\{x(n), n = -\infty,...,\infty\}$ and a rectangular window $\{y(n) = 1, n = 0,...,N-1\}$. Therefore, the discrete Fourier transform X_m of a finite data set will be the convolution of $X'(f)$ and the Fourier transform of a rectangular window. This leads to "leakage" in the frequency domain, i.e., energy in the main lobe of a frequency response "leaks" into the sidelobes, obscuring and distorting the frequency response. Also, the frequency resolution of the DFT is limited by the length of the data sequence. However, resolution can be improved by simply increasing the number of data points and the distortion can be minimized by skillful selection of tapered windows.

Despite the limitation imposed by the frequency resolution and the distortion effect, the DFT has gained popularity in DSP implementations by adopting the fast Fourier transform (FFT), a high-speed algorithm noted for its computational efficiency.

FFT ALGORITHM

For convenience in notation, the DFT equations are generally written in terms of W_N, defined as:

$$W_N = e^{-j2\pi/N}$$

Thus, the DFT pair are expressed as:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn} \qquad \text{(Forward Transform)}$$

$$X(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) W_N^{-kn} \qquad \text{(Inverse Transform)}$$

It is clear that for each value of k, the direct computation of $X(k)$ requires N complex multiplications and $(N-1)$ complex additions, i.e., $4N$ real multiplications and $(4N-2)$ real additions. Since $X(k)$ must be computed for N different values of k, the direct computation of the DFT of a sequence $x(n)$ requires N^2 complex multiplications and $N(N-1)$ complex additions. For large values of N, the number of arithmetic operations becomes very large. For this reason, the FFT algorithm is employed to reduce the number of multiplications and additions by exploiting the symmetric and periodic properties of W_N^{kn}. The fundamental principle is to decompose the DFT computation of a sequence of length N into successively smaller DFTs. Decimation-in-time (DIT) and decimation-in-frequency (DIF) are two different schemes used to implement this decomposition. Compared with direct computation on DFT equations, a dramatic increase in efficiency can be achieved by limiting the number of data points, N, to an integer power of 2, i.e., $N = 2^U$. Thus, it is called a "Radix-2" FFT algorithm.

The DIT algorithm is based on decomposing the time domain sequence $x(n)$ into smaller sequences. Since N is an even integer, we can compute $X(k)$ by separating $x(n)$ into two $N/2$ -point sequences which consist of an even-numbered part and an odd-numbered part.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}$$

$$= \sum_{r=0}^{N/2-1} x(2r) W_{N/2}^{rk} + W_N^k \sum_{r=0}^{N/2-1} x(2r+1) W_{N/2}^{rk}$$

$$= G(k) + W_N^k H(k)$$

It is recognized that $G(k)$ and $H(k)$ are the $N/2$-point DFTs of the even-numbered and odd-numbered $x(n)$ points, respectively. Using the property

$$W_N^{N/2+k} = W_N^{N/2} W_N^k = -W_N^k$$

we can define butterfly computation as in Figure 18 to compute $X(k)$ and $X(N/2+k)$ using one complex multiplication, i.e., the multiplication of $H(k)$ and the twiddle factor W_N^k.

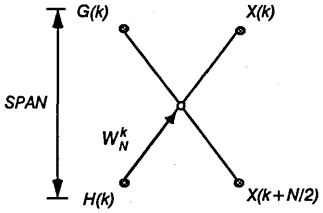

Figure 18. The Notation of a DIT Butterfly Computation

Then, the DIT decomposition of an N-point DFT into two $N/2$-point DFT can be plotted as the flow graph in Figure 19, with $N=8$. Since $N/2$ is still an even number, $N/2$-point DFT $G(k)$ and $H(k)$ can be decomposed into two $N/4$-point DFTs as:

$$G(k) = \sum_{r=0}^{N/2-1} x(2r) W_{N/2}^{rk}$$

$$= \sum_{l=0}^{N/4-1} x(2(2l)) W_{N/4}^{lK} + W_N^{2k} \sum_{l=0}^{N/4-1} x(2(2l+1)) W_{N/4}^{lk}$$

$$H(k) = \sum_{r=0}^{N/2-1} x(2r+1) W_{N/2}^{rk}$$

$$= \sum_{l=0}^{N/4-1} x((2\cdot 2l)+1) W_{N/4}^{lK}$$

$$+ W_N^{2k} \sum_{l=0}^{N/4-1} x((2\cdot(2l+1)+1) W_{N/4}^{lK}$$

As the decomposition process continues, the number of data points for each DFT computation is reduced by half at each stage, until you reach a 2-point DFT. The complete FFT flow graph for computation of the N-point DFT is shown in Figure 20. The whole algorithm requires υ stages of computation, where $\upsilon = \log_2 N$. There are $N/2$ butterfly computations in each stage, which means only $(N/2)(\log_2 N)$ complex multiplications and $N(\log_2 N)$ complex additions. Table 3 shows the comparison between N^2 and $(N/2)(\log_2 N)$ for various values of N from 2 to 2048. It proves that the FFT approach offers a really substantial computational saving.

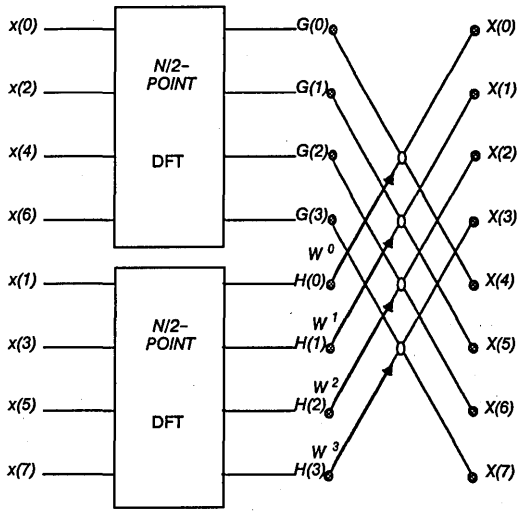

Figure 19. The DIT Decomposition of N-Point DFT Into Two N/2-Point DFTs

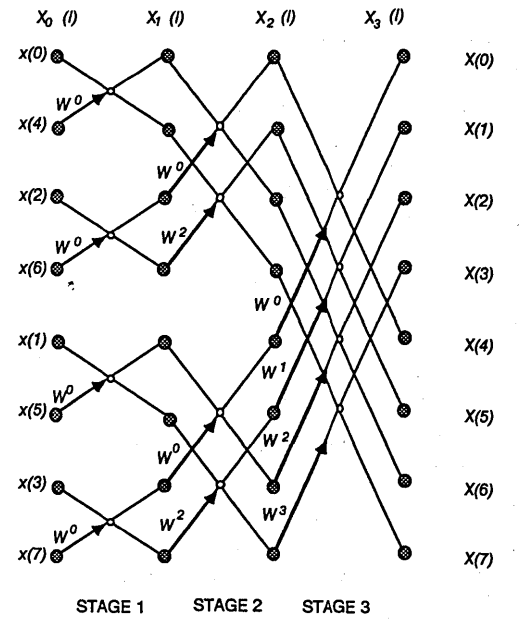

Figure 20. Complete DIT Decomposition of N-Point DFT With N=8

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Table 3. Comparison of N^2 and $(N/2)(\log_2 N)$

N	N^2	$(N/2)(\log_2 N)$	$N^2/(N/2)(\log_2 N)$
2	4	1	4.0
4	16	4	4.0
8	64	12	5.4
16	256	32	8.0
32	1024	80	12.8
64	4096	192	21.4
128	16384	448	36.6
256	65536	512	64.0
512	262144	2304	113.8
1024	1048576	5120	204.8
2048	4194304	11264	372.4

Denote the sequence of complex numbers resulting from the m -th stage as $X_m(l)$, where $l=0,1,...,N-1$, and $m=0,1,2,3$. We can think of $X_m(l)$ as the input array and $X_{m+1}(l)$ as the output array for the $(m+1)$st stage of computations. It is clear from Figure 20 that only N registers are needed to implement the complete computation if $X_{m+1}(p)$ and $X_{m+1}(q)$ are stored in the same registers as $X_m(p)$ and $x_m(q)$, where p, q represent the data positions of a butterfly pair. The advantage of this kind of computation, called "in-place" computation, is that the results are saved in the original storage locations. For the computation to be done in place, the input data must be stored in a nonsequential order, called "bit-reversed" order. For the 8-point flow graph, three binary digits are required to index the data. Since $X_0(l)$ is the input data of the first stage, we can write the indices l,n in binary form to relate $X_0(l)$ and $x(n)$ as in Table 4.

Table 4. The Natural-Order Index and the Bit-Reversed Index

INDEX l	BINARY FORM	BIT-REVERSE BINARY FORM	BIT-REVERSED INDEX n
0	000	000	0
1	001	100	4
2	010	010	2
3	011	110	6
4	100	001	1
5	101	101	5
6	110	011	3
7	111	111	7

Conclusively, if $(n_2n_1n_0)$ is the binary representation of the index of the sequence $x(n)$, $x(n_2n_1n_0)$ is stored in the position of X_0 $(n_0n_1n_2)$. That is, in order to determine the position of $x(n_2n_1n_0)$ in the input sequence, we must reverse the order of the bits of index n. Bit-reversed order is the natural result of the decomposition of the input sequence. The separation of the even-numbered data and odd-numbered data can be carried out by examining the least significant bit (n_0) of the index n—"0" corresponds to an even-numbered index, "1" to an odd-numbered index. Next, subsequences are sorted into their even and odd parts by examining the second least significant bit of the index. This process is repeated until N subsequences of length l are obtained. This sorting into even and odd numbered subsequences is depicted by the tree diagram of Figure 21. Figure 22 shows a "not-in-place" computation of the DIT algorithm, wherein, by a rearrangement of Figure 20, each stage has the same geometry, thereby permitting sequential data accessing and storage. Note that the input data is also "bit-reversed".

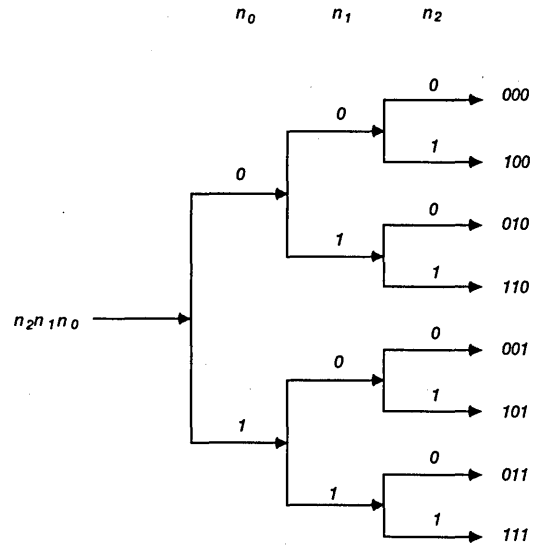

Figure 21. Tree Diagram Depicting Bit-Reversed Sorting

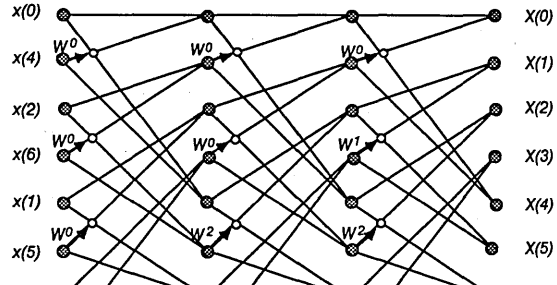

Figure 22. Not-In-Place Computation of the DIT Algorithm

By dividing the output sequence $X(k)$ into smaller sub-sequences, we can derive the DIF algorithm. For N a power of 2, we divide the input sequence $x(n)$ into the first half and the last half of the points so that:

$$X(k)=\sum_{n=0}^{N/2-1}x(n)W_N^{nk}+\sum_{n=N/2}^{N-1}x(n)W_N^{nk}$$

$$=\sum_{n=0}^{N/2-1}x(n)W_N^{nk}+W_N^{(N/2)k}\sum_{n=0}^{N/2-1}x(n+N/2)W_N^{nk}$$

$$=\sum_{n=0}^{N/2-1}(x(n)+(-1)^k x(n+N/2))W_N^{nk}$$

$$X(2r)=\sum_{n=0}^{N/2-1}x(n)+x(n+N/2))W_N^{2rn}$$

$$=\sum_{n=0}^{N/2-1}g(n)W_{N/2}^{rn}$$

$$X(2r+1)=\sum_{n=0}^{N/2-1}x(n)-x(n+N/2))W_N^n W_N^{2rn}$$

$$=\sum_{n=0}^{N/2-1}(h(n)W_N^n)\cdot W_{N/2}^{rn}$$

The N-point DFT is decomposed into two $N/2$-point DFTs $X(2r)$ and $X(2r+1)$ at the output stage as shown in Figure 23.

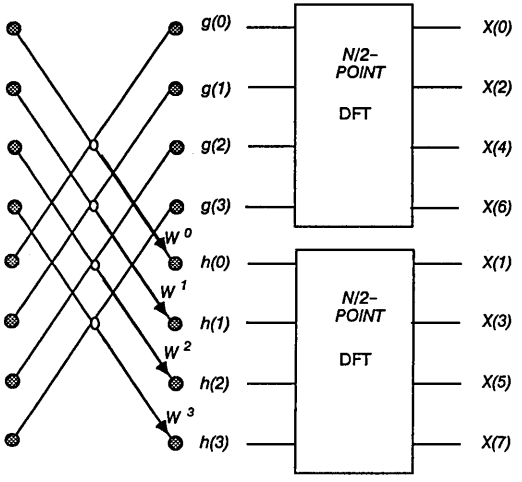

Figure 23. The DIF Decomposition of N-point DFT Into Two N/2-Point DFTs

Similar to the decimation-in-time algorithm, $N/2$-point DFT $X(2r)$ can be decomposed into two $N/4$-point DFTs as:

$$X(2(2l))=\sum_{n=0}^{N/4-1}g(n)W_{N/2}^{2ln}+\sum_{n=N/4}^{N/2-1}g(n)W_{N/2}^{2ln}$$

$$=\sum_{n=0}^{N/4-1}(g(n)+g(n+N/4))W_{N/4}^{ln}$$

$$X(2(2l+))=\sum_{n=0}^{N/4-1}g(n)W_{N/2}^{(2l+1)n}+\sum_{n=N/4}^{N/2-1}g(n)W_{N/2}^{(2l+1)n}$$

$$=\sum_{n=0}^{N/4-1}((g(n)-g(n+N/4))W_N^{2n})W_{N/4}^{ln}$$

We follow the same decomposition process until a 2-point DFT is achieved. The complete flow graph of this FFT algorithm can be plotted as in Figure 24, with the butterfly configuration in Figure 25. It is easy to see from Figure 20 and Figure 24, that the number of arithmetic operations is the same for both DIT and DIF algorithms. However, the output sequence of DIF is in the "bit-reversed" order. The not-in-place computation of Figure 24 also exists, which is shown in Figure 26.

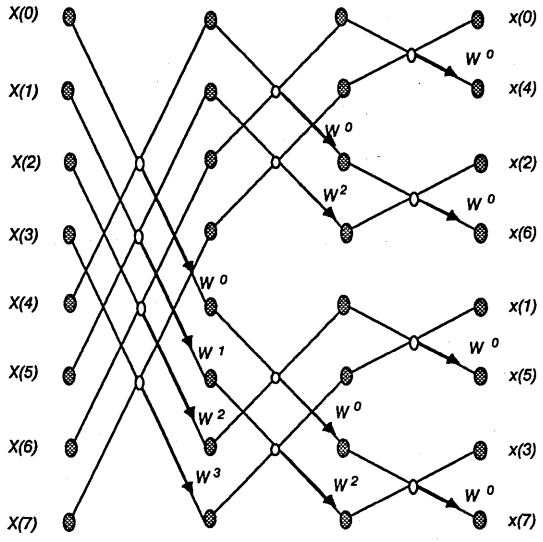

Figure 24. Complete DIF Decomposition of N-Point DFT With N = 8

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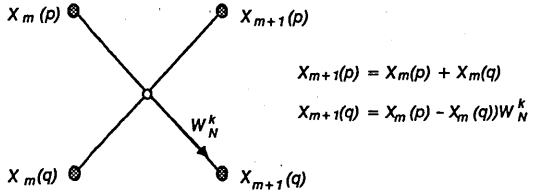

Figure 25. The Notation of a DIF butterfly Computation

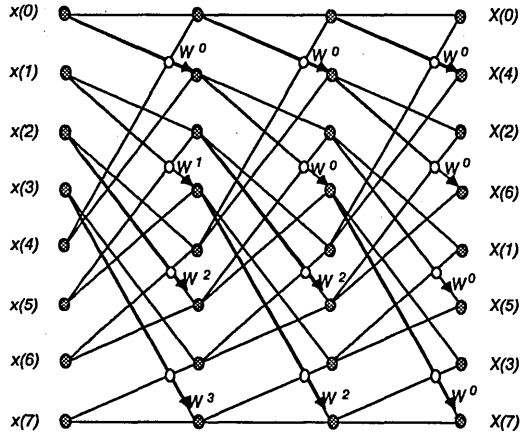

Figure 26. Not-In-Place Computation of the DIF Algorithm

There is an interesting relationship existed between the butterfly configurations of DIT and DIF. The corresponding equations for the DIT butterfly as in Figure 18 are

$$X_{m+1}(p) = X_m(p) + W_N^k X_m(q)$$
$$X_{m+1}(q) = X_m(p) - W_N^k (X)_m(q)$$

where $X_{m+1}(p)$ and $X_{m+1}(q)$ replace $G(k)$ and $H(k)$, $X_m(p)$ and $X_m(q)$ replace $X(k)$ and $X(N/2+k)$. We can solve X_m in terms of X_{m+1} by inverting the computations of the above equations.

$$X_m(p) = \frac{1}{2}(X_{m+1}(p) + X_{m+1}(q))$$
$$X_m(q) = \frac{1}{2}(X_{m+1}(p) - X_{m+1}(q))W_N^{-k}$$

When compared to the butterfly of Figure 25, it can be seen that the reverse of the DIT butterfly is just the DIF butterfly with the added factor *1/2* and an inverted twiddle factor, W_N^{-k}. This implies that the reversed computation of the DIT algorithm (inverse FFT) has the same structure as the forward DIF algorithm. The flow graph of this reversed process is given in Figure 27. Similarly, the inverse FFT structure of the DIF algorithm will be the same as that of the forward DIT algorithm.

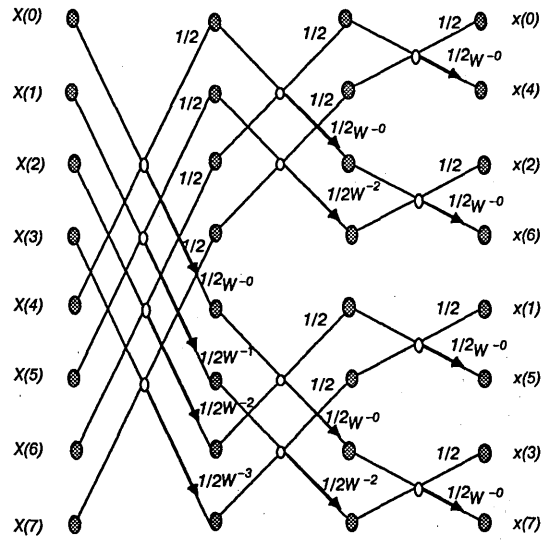

Figure 27. The Inverse FFT of DIT Structure Appears To Be a DIF Structure

Integrated Device Technology, Inc.

DESIGNING WITH THE IDT49C460 AND IDT39C60 ERROR DETECTION AND CORRECTION UNITS

APPLICATION NOTE AN-24

By Robert Stodieck

INTRODUCTION

The Error Detection and Correction (EDC) chip itself is one element of an EDC system. How it is connected to the surrounding system and controlled is left to the system designer. Because there are so many design variations possible, it is important for the designer to develop a clear idea of the target design before beginning the design process. Basic design approaches and perturbations are enumerated in this application note.

The details of the EDC control logic depend on the configuration of the EDC system, EDC bus topology, the nature of the CPU or system bus involved and the nature of diagnostic hardware used. The data bus topology is highly dependent on the individual target system.

This applications note approaches the bus topology issue first. The advantages and disadvantages of using EDC word widths that are different from the system bus are discussed. The next topic to be covered is the use of EDC in a system with a cache. Then the operational configuration of the EDC system is discussed. This implies answering questions about how the EDC unit handles errors in a particular system is discussed. How an operating system deals with the EDC function is discussed, followed by a practical discussion of some non obvious hardware topics. The final topic is memory system diagnostics and verification. An appendix includes tables and software that are useful in debugging and in writing diagnostic software for an EDC board.

Data Bus Topology

Most contemporary CPUs execute write operations of a byte or other sub-word width types. These cause special problems for all EDC units since EDC transactions with the memory are carried out on whole width EDC words. To facilitate partial word write operations with the IDT39C60 or IDT49C460 type EDC units, a set of tri-state transceivers are normally required between the system bus and the EDC unit. These buffers are required to prevent bus contention between the CPU or system bus drivers and the EDC units data outputs during partial word write operations. Figure 3 shows a bus arrangement appropriate for large DRAM arrays. The need for isolation of the EDC data bus and the system bus is shown by examining the data paths, shown with white arrows. These are used by the final write operation of a partial-word write cycle. In this case, only data bits 0-7 are being written from the processor to memory. If the processor or system bus drivers can be tri-stated on byte boundaries then this set of buffers could be removed, but this is not a common situation.

Depending on the memory size, additional buffering may be required between the EDC and the memory bus proper. The buffer configuration must be determined before beginning the EDC and memory controller design.

An appropriate general purpose bus topology is shown in Figure 1. It is common for one or the other sets of bi-directional buffers to be a latched type such as an IDT74FCT646 instead of the IDT74FCT245 shown. A family of waveforms appropriate for the bus format shown in Figure 1 is shown in Figure 2. The waveform diagrams do not include precise timing considerations which are left to the designer.

In any given system, any of the buffers separating the EDC from the memory IC's may be eliminated if bus capacitance and speed considerations allow.

EDC Bus Width vs. System Bus Width

The width of the EDC bus and the System Bus are normally matched. However, there are valid reasons for making the EDC bus both wider or narrower than the system bus.

Wide EDC words are significantly more efficient than narrower EDC word widths in terms of the amount of check-bit memory used for a given amount of data memory. The amount of check-bit memory required for 64 data bits is 8 bits if the 64 data bits are organized as one word and 14 bits if it is handled as two 32-bit words. Twenty-four bits of check-bit memory would required for 64 data bits organized as four 16-bit EDC data words.

For the purposes of speed, it would be ideal to have 8-bit EDC words for systems that do byte write operations. This would make it unnecessary to ever have to read a memory location prior to writing a partial word on these systems. Unfortunately, eight-bit EDC words are grossly inefficient in terms of check-bit memory usage. Therefore, the EDC word widths are normally 16-bits or more.

Since the EDC word widths must generally be 16-bits or more for check-bit memory efficiency, and since general-purpose computers generally use byte or partial-word-write operations, general-purpose computers force the EDC unit to be able to process partial EDC word-width write operations. Partial word-width write operations require the EDC subsystem to execute a read-modify-write type memory cycle. Thus, the EDC controller must take over control of the memory system and execute a read before completing a partial word write. For some applications, where EDC is in use, it may be desirable to speed up processing by prohibiting partial word operations either at the hardware level or software level. Speed critical sections of code should be executed without partial-word write operations.

The read-modify-write EDC cycle executed during a partial-word write is identical to the EDC correction cycle executed during a read cycle when an error has occurred. The read-modify-write EDC cycle should not be confused with the read-modify write cycle executed by some CPU's.

Verification of a memory system using an EDC word wider than the system word is complicated by the fact that all memory write cycles become read-modify-write cycles i.e. partial-word-write EDC cycles. Careful consideration of diagnostic procedures needs to be made during the design to avoid unnecessarily complex debugging procedures.

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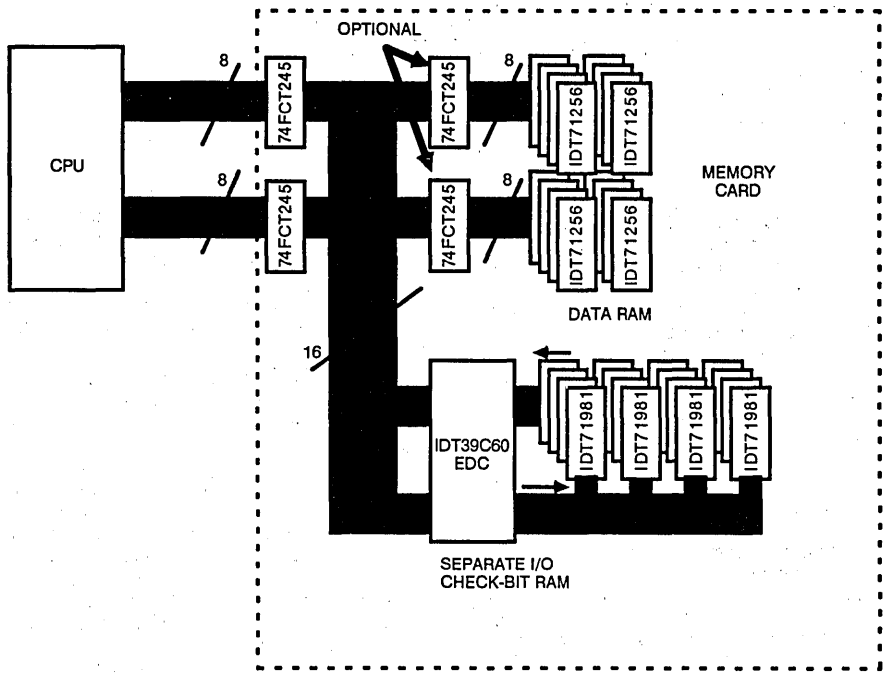

Figure 1. A general purpose 16-bit EDC data bus topology. Corresponding timing waveforms are shown in Figure 2. IDT74FCT245 buffers separate the EDC data bus from the CPU and the main memory. Separate-I/O RAMs are used in the check-bit memory.

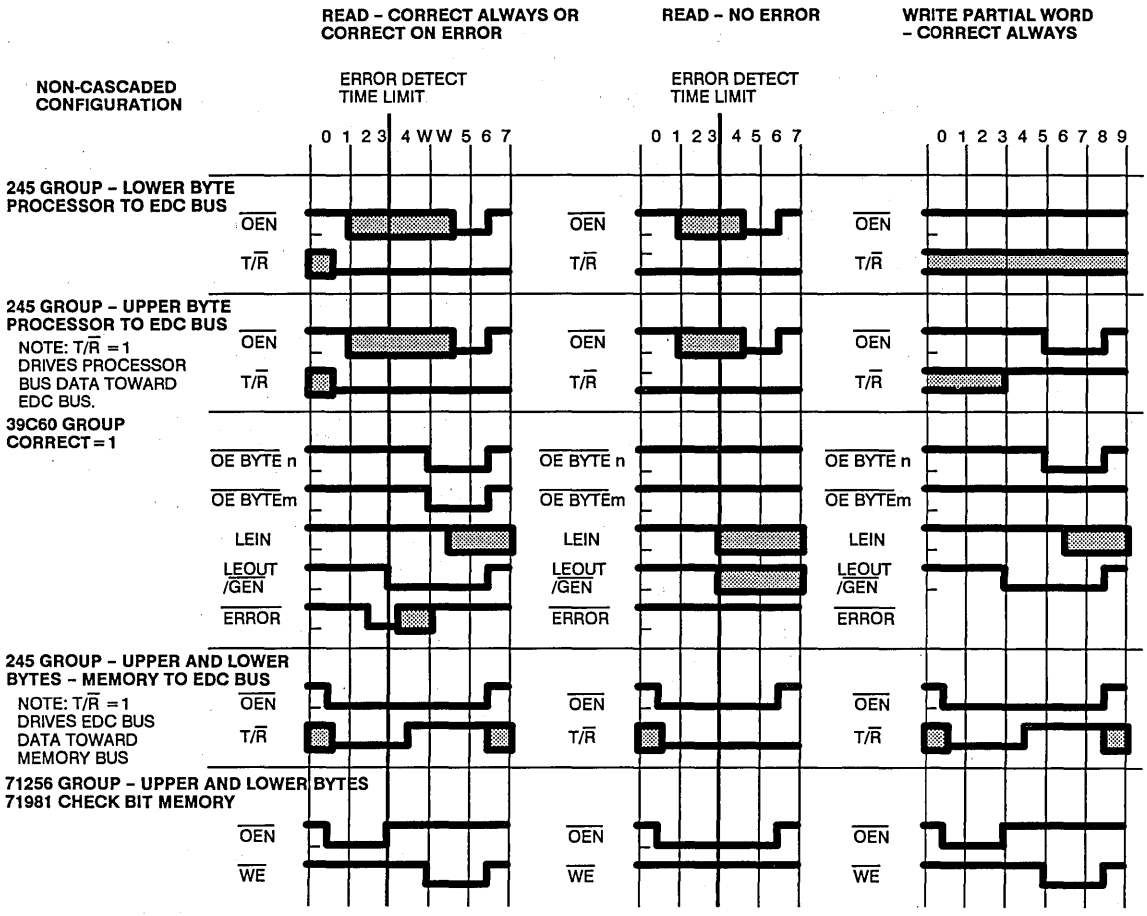

Figure 2. A sample family of timing waveforms for an EDC system. The target system is based on IDT71256 static RAMs for main memory with IDT71981 separate I/O RAMs for checkbit memory. (See Figure 1.) The partial word write case illustrates a low order byte write.

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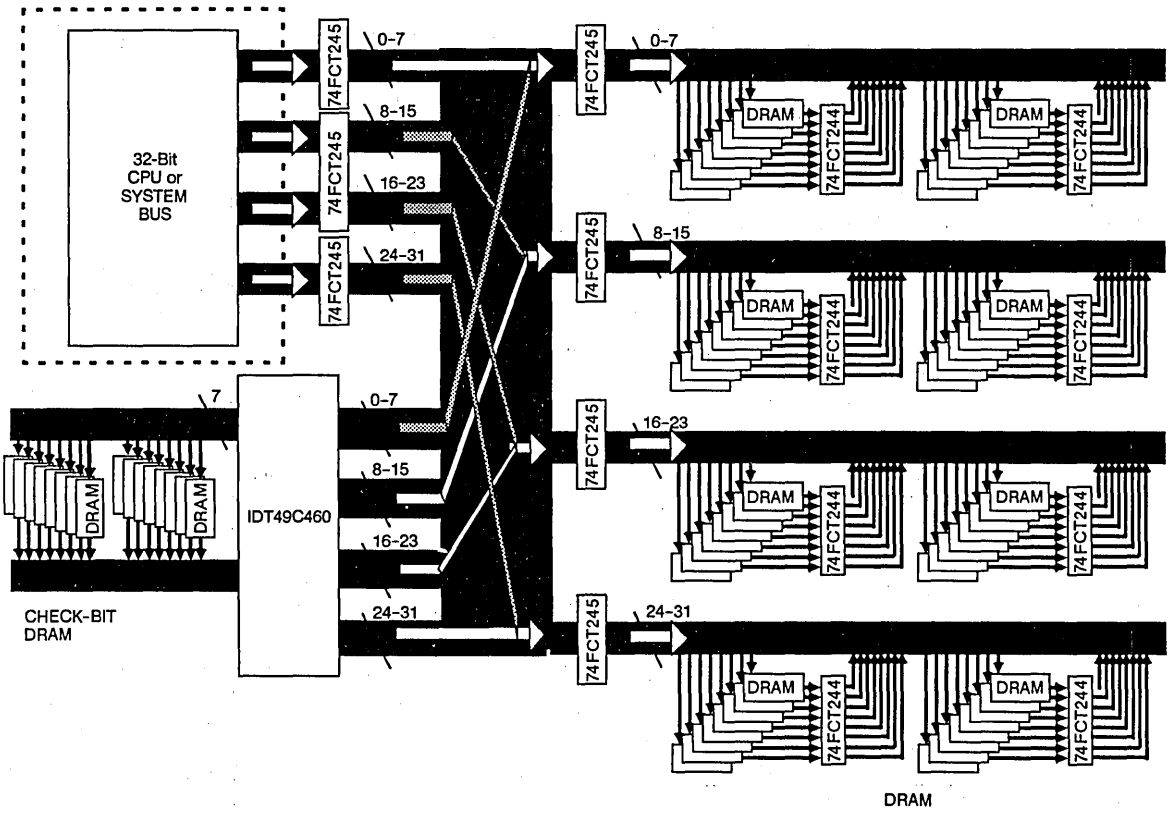

Figure 3. A general purpose 32-bit EDC bus topology for 1 bit wide DRAMS. The white arrows indicate the data flow paths used on the final write phase of a partial word write cycle. Data bits 0-7 are being written into memory from the processor.

EDC in Systems Using Cache

In systems using cache memory, it may be desirable to place the EDC function between the cache and main memory, as opposed to locating the EDC function between the processing elements and cache. Parity can be used as a single-bit error detection scheme between the CPU and cache. RISC architectures tend to require more memory accesses per unit time that complex-instruction-set processors. This makes the use of cache memory more important in the RISC system. An appropriate bus topology for a RISC type processor with cache memory is shown in Figure 4.

Use of a cache memory also affords the possibility of using a different error correcting philosophy. If the EDC function is located between the cache and main memory, then it may be allowable for data reads to be corrected and sent on to the cache, but not to be immediately written back to main memory, after an error has been discovered. In this approach, corrected memory words are updated in the normal write-back processes of the cache memory.

Instruction reads must be thought of differently than data reads since instructions are normally not written back to memory from the cache. However, it may be possible to not write a corrected instruction word back to memory after detection, since the instruction is usually backed up on a different media. In most systems there is no way for the EDC to know whether it is operating on instructions or data, so a correction philosophy must be selected that can be applied to both instruction and data words.

Diagnostic Hardware

A syndrome latch for capturing syndrome values after errors and transferring them to the system data bus is always recommended. Providing a check-bit memory read-back ability allows direct verification of the gross functionality of the check-bit memory 'on board'. This greatly facilitates check-bit memory verification. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory, or a second latch may be provided to allow this.

Ideally, diagnostic hardware includes address latches to capture the address of an error. However, this may not be practical in any particular application. It may be sufficient to identify the individual RAM in which an error has occurred.

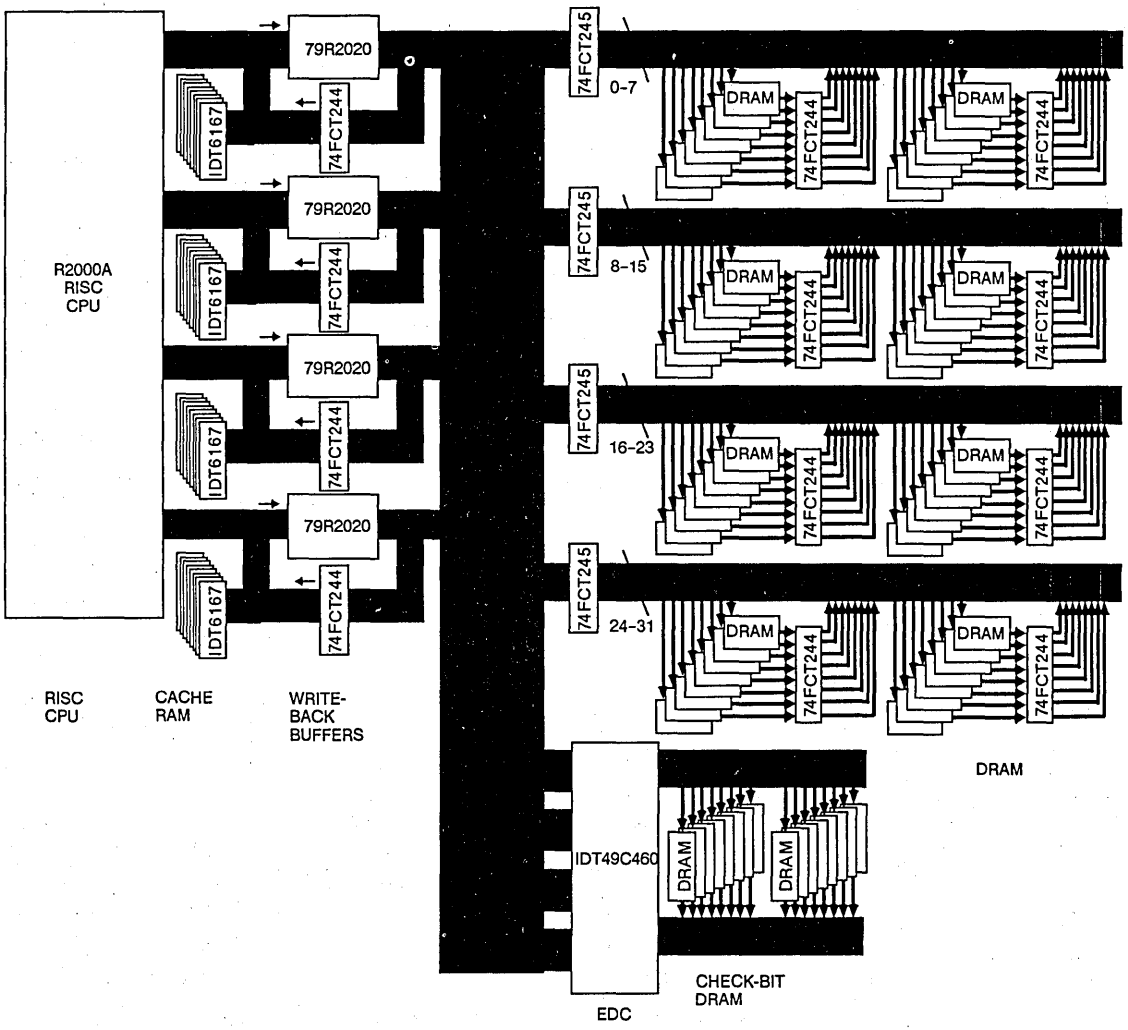

Figure 4. An EDC bus arrangement appropriate for a CPU with caches such as the IDT R3000 or IDT R2000 RISC processor.

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OVERVIEW OF EDC OPERATIONAL MODES

Bus Watch vs. Correct Always for the Memory Read Cycle

In a bus-watch system, errors are only corrected after they have been detected by the EDC chip. Data is corrected and written back to memory to scrub errors, only after an error has been detected. In theory, the EDC chip only "watches" the bus normally, and does not slow memory read cycles with correction delays unless an error has been detected. Since errors during read operations are normally very rare, read cycle bus-watch systems are normally faster than correct-always systems.

In correct-always systems, data read by the system is always corrected. The EDC control logic is simpler to design and implement because there is only one type of read cycle. Memory cycle timing in correct-always systems can be completely deterministic and thus such systems may lend themselves more effectively to real-time applications.

Bus Watch vs. Correct Always for the Partial Word Write Cycle

A write operation that is of a width less than the EDC word width forces the EDC subsystem to execute a read cycle prior to actually writing to memory. This is required to provide the EDC unit with the whole data word to be written into memory for the purpose of check-bit generation. No time is saved by not correcting the data read from memory prior to the subsequent write operation. The partial-word-write operation is virtually identical to a read cycle in correct-always mode or a read cycle with an error detected. Consequently, a partial word write is usually done in a "correct always" mode.

Operating System Involvement

In systems capable of doing partial-word-write operations, it is necessary to initialize the memory on power up. This can be done in hardware but it is usually done by the operating system. Initialization implies writing every memory location with an arbitrarily chosen constant and thereby writing the check-bit memory with the correct corresponding check-bits. The need to initialize memory results from the nature of the read-modify-write EDC cycle required by the event of a partial-word-write operation. If the memory has not been initialized, the read cycle will normally result in an error indication and an attempt to 'correct' a bit in the data field before writing back to memory. This tends to introduce errors into previously written data bytes or sub-words.

It is possible to design a state machine EDC controller that corrects all single bit errors in a fashion transparent to the CPU. This is not always desirable since it masks hard single-bit errors that indicate hardware problems. In any case, the operating system must become involved in the event of multiple errors if only to issue an appropriate error message to the system operator.

It is desirable to log single bit errors and as much information about the error as is practical. Relevant data ideally includes the syndrome bits to identify the bit location in the word, and the physical address of the error. For complete EDC transparency, such as that desired for real time systems, error logging must be eliminated or accommodated entirely in hardware. For non real-time systems, interrupting the CPU after an error occurrence is the conventional way to log error data. Syndrome data is collected, and any other error information the system hardware retains is retrieved.

Non-obvious Hardware Topics

In a 32-bit system with a bi-directional check-bit bus or in 64-bit cascaded mode, the check-bit input-output and syndrome functions are time-multiplexed onto the same bus. If the EDC unit is in the correction mode, the input latches are open, and the OESC pins are low, the bus will tend to oscillate. This combination of control inputs would not be appropriate for normal operation but might occur in an idle period between memory cycles unless the designer specifically designs this condition out. The oscillation occurs in this condition because the EDC units are attempting to output syndrome bits based on the data and 'check-bit' inputs. However, the syndrome outputs in this state are being fed back to the check-bit inputs. The result is an oscillation on the check-bit/ syndrome bus.

It is an important and sometimes overlooked fact that it is not acceptable to allow inputs on most CMOS parts to 'float'. The result of doing this is increased power consumption, on chip noise and sometimes outright oscillation which can lead to latch-up. The check-bit inputs and the data bus of an EDC unit should not be allowed to float when not being used. In low power systems in particular, all inputs not in use must be brought to logic highs or lows when not in use. This may imply not tri-stating some buffers that would otherwise be tri-stated when not actively driving, or actually including pull-up or pull-down resistors on a bus to bias it when it is not actively being driven.

Basic EDC Unit Operation

Basic 32-bit 49C460 EDC operation with timing diagrams is illustrated in Figures 5, 6 and 7. These timing diagrams are also appropriate for a 16-bit IDT39C60 system. In the IDT39C60, the LEout and the Generate functions have separate pins. In the IDT49C460, they are both controlled by one pin. It is usually convenient when using the IDT39C60 to wire the two pins together.

In the non-expanded case, with either EDC unit, use of the input latch may be convenient but is not logically dictated (i.e. the LEin pin may be tied high). Also, the correct pin may be simply left asserted in normal operation. The "detect" mode is usually only used as a diagnostic aid, which allows the data correction function to be shut off while still generating an error signal based on the input data.

Diagnostic Modes

Since the EDC function introduces a complicating layer between the system bus and the memory, diagnostic modes are provided for the EDC to provide testability for the entire memory subsystem. In memory systems where the EDC word is wider that the system bus memory, verification is complicated by the fact that all writes are partial word writes. Good diagnostic design requires forethought.

The EDC unit's internal diagnostic latches have two distinct and unrelated data fields. The check-bit data field is used to provide check data to be substituted for normal check-bits in the diagnostic modes. These will be written to memory in diagnostic generate mode, or substituted for check-bits read from memory in diagnostic-detect or correct mode. The second field in the diagnostic latch is the control field. The control field is ignored except when the part is placed in the internal control mode.

The control byte is used to control the operating features of the part when the part has been placed in internal control mode. Each bit in the control field corresponds to a pin on the part and overrides the logic sense of that pin when the part is in the internal control mode. For example, we could place the part into the correct mode by setting the correct pin on the EDC unit to a logic high, or we could put the part into the internal control mode and set the correct bit in the diagnostic latch to '1'. Thus there are always two ways to achieve any mode of operation. For example, the diagnostic modes may be entered by setting the external diagnostic inputs appropriately, or entering the internal control mode and setting the diagnostic latch bits appropriately. The internal control mode is provided as a convenience and is useful for controlling operating modes during diagnostic testing and software initialization. Conceptually, it is important to realize that anything that can be done in this mode can be done with external logic as well.

Memory System Verification Strategies

When a new design is being verified, it is critical to isolate different problem factors; this is one function of the EDC diagnostics.

To prove the function of the primary memory array, the EDC unit is placed in the pass-through mode so that it does not interact with the data stream. Once the primary memory array has been verified as functional, the check-bit memory must be verified. The diagnostic generate mode is used to write known data into the check-bit memory. Reading the check-bit memory directly through the EDC is not possible, so gross functional testing must be done via an external latch or with a logic analyzer. Using an external latch greatly facilitates check-bit memory verification.

Collecting syndrome data from error events requires that an external latch be included in the design to capture the syndrome data after an error has occurred. It should be possible to clear this latch after reading its contents from the system bus. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns.

SUMMARY

The error detection and correction unit is located in the critical path between a CPU and the memory. The operational configuration of the EDC intimately affects the speed of the final system. Due to the wide variation between computer architectures that EDC is desirable for, the EDC unit is necessarily a generalized IC. Thus, designing an EDC system is not a straightforward process. The object of this applications note has been to illuminate some of the topics that any designer will encounter in the process of designing an EDC system.

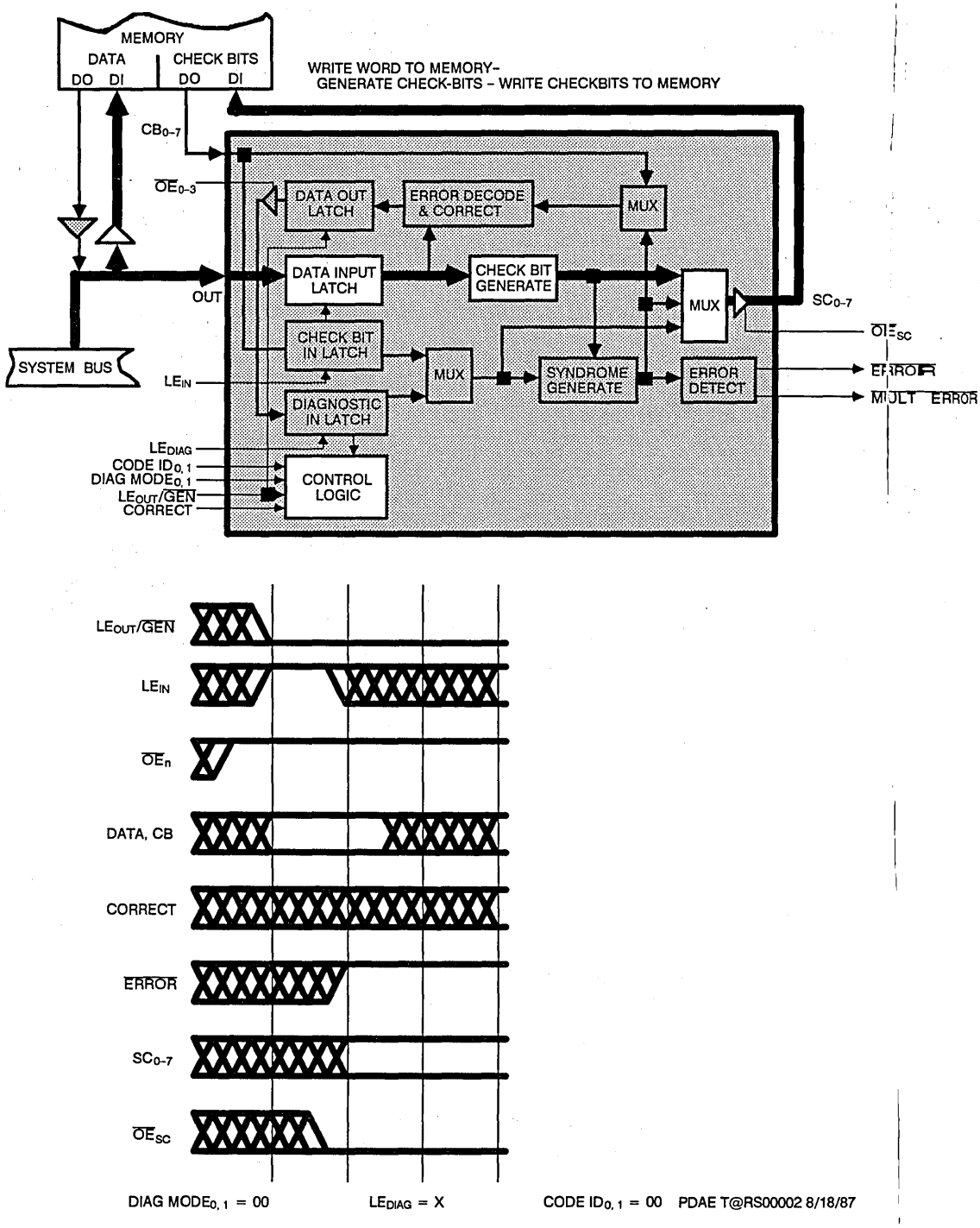

Figure 5. 32-bit full-word-width write operation (generate mode).

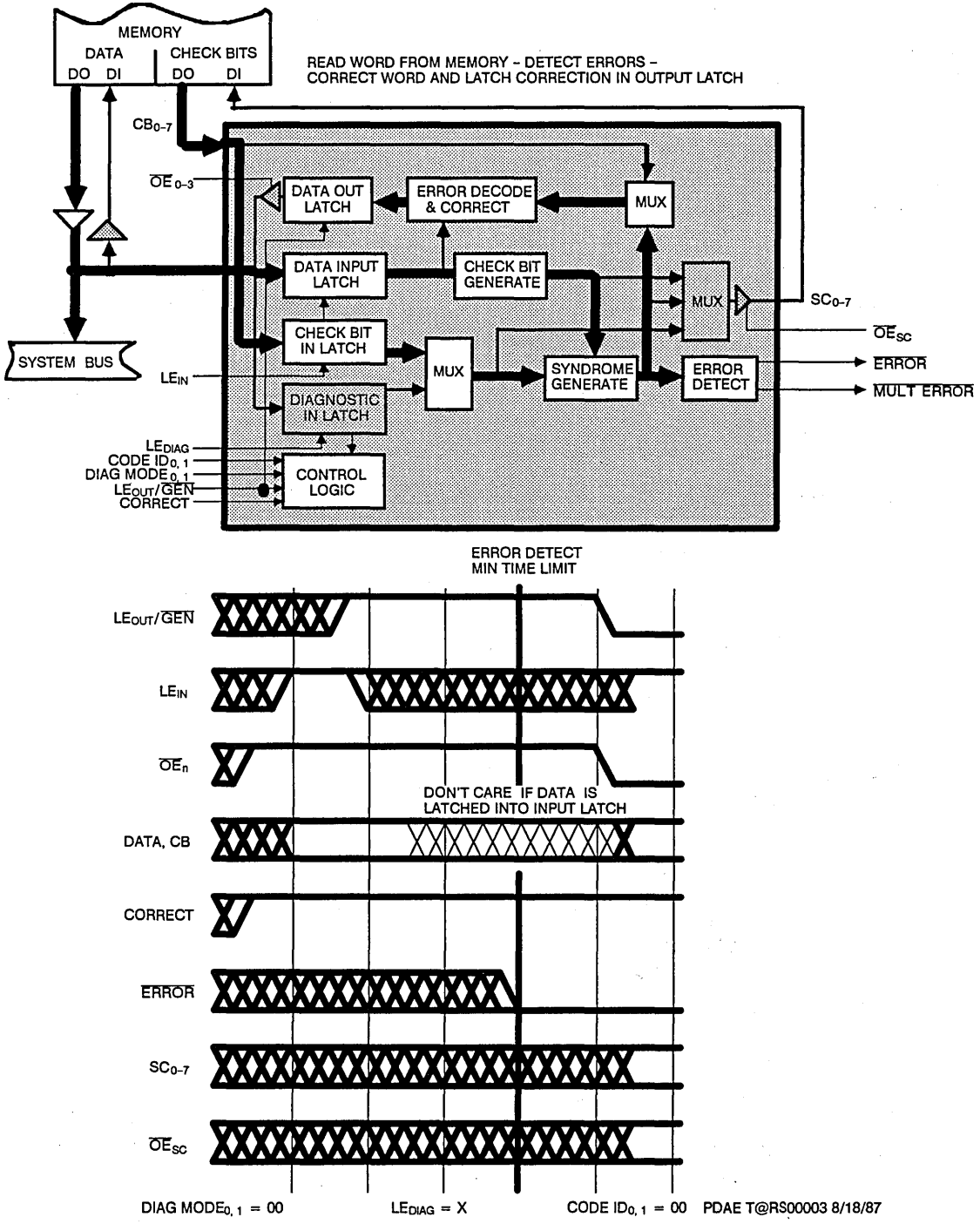

Figure 6. Memory read and error detect. Identical for read operations and the first phase of a partial-word-write operation (correct mode).

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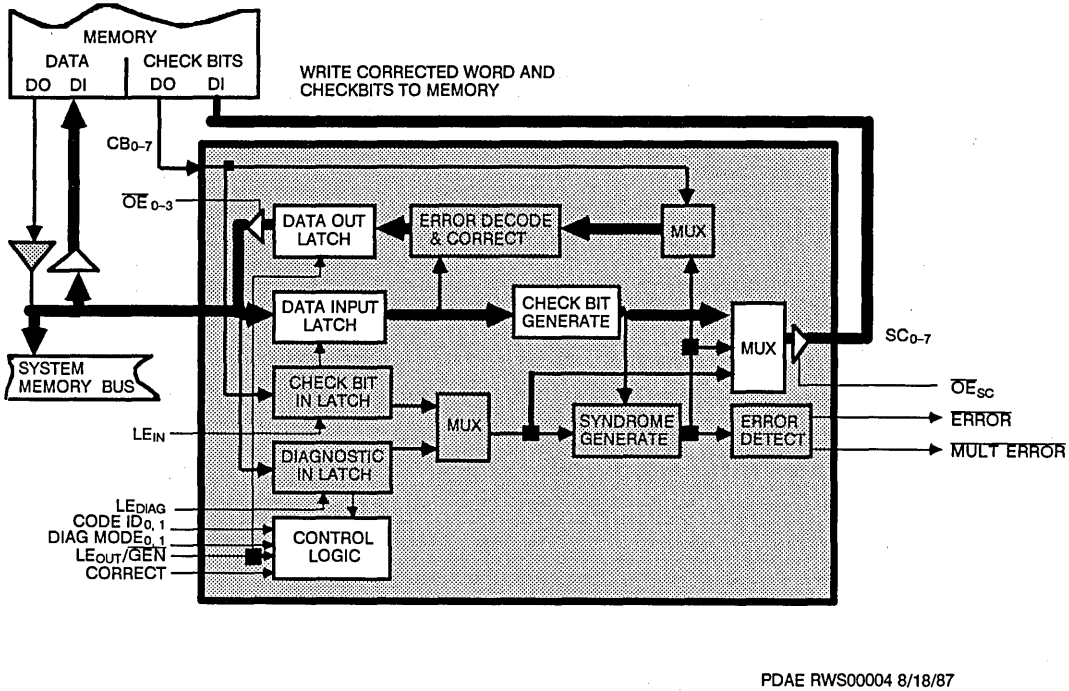

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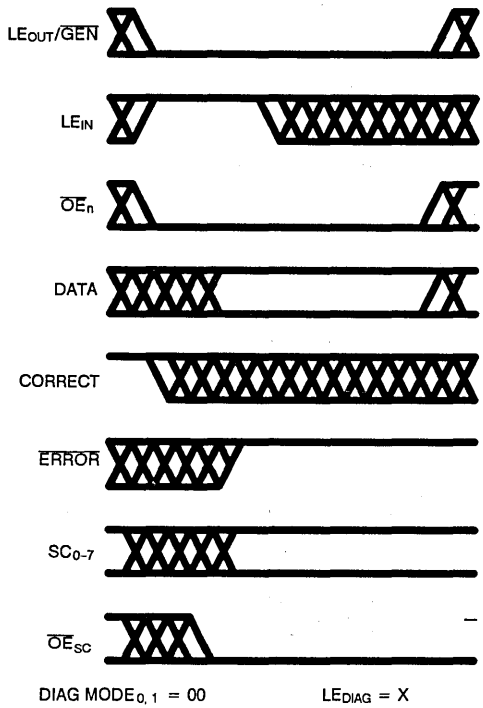

Figure 7. Memory correct and check-bit regenerate. Identical for the second phase of a read operation in which an error has occurred, and for a partial-word-write operation except for the state of the individual byte output enables.

Appendix

ERROR				HEX	0	1	2	3	4	5	6	7
DECIMAL				S6	0	0	0	0	1	1	1	1
SYNDROME				S5	0	0	1	1	0	0	1	1
HEX				S4	0	1	0	1	0	1	0	1
	S3	S2	S1	S0								
0	0	0	0	0	NE	C4	C5	T	C6	T	T	30
DECIMAL EQUIVALENT>>					0	16	32	48	64	80	96	112
1	0	0	0	1	C0	T	T	14	T	M	M	T
					1	17	33	49	65	81	97	113
2	0	0	1	0	C1	T	T	M	T	2	24	T
					2	18	34	50	66	82	98	114
3	0	0	1	1	T	18	8	T	M	T	T	M
					3	19	35	51	67	83	99	115
4	0	1	0	0	C2	T	T	15	T	3	25	T
					4	20	36	52	68	84	100	116
5	0	1	0	1	T	19	9	T	M	T	T	31
					5	21	37	53	69	85	101	117
6	0	1	1	0	T	20	10	T	M	T	T	M
					6	22	38	54	70	86	102	118
7	0	1	1	1	M	T	T	M	T	4	26	T
					7	23	39	55	71	87	103	119
8	1	0	0	0	C3	T	T	M	T	5	27	T
					8	24	40	56	72	88	104	120
9	1	0	0	1	T	21	11	T	M	T	T	M
					9	25	41	57	73	89	105	121
A	1	0	1	0	T	22	12	T	1	T	T	M
					10	26	42	58	74	90	106	122
B	1	0	1	1	17	T	T	M	T	6	28	T
					11	27	43	59	75	91	107	123
C	1	1	0	0	T	23	13	T	M	T	T	M
					12	28	44	60	76	92	108	124
D	1	1	0	1	M	T	T	M	T	7	29	T
					13	29	45	61	77	93	10	125
E	1	1	1	0	16	T	T	M	T	M	M	T
					14	30	46	62	78	94	110	126
F	1	1	1	1	T	M	M	T	0	T	T	M
					15	31	47	63	79	95	111	127

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

Table 1. 32-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

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ERROR				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	NE	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
					0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
					1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
					2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
					3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
					4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
					5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
					6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
					7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
					8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
					9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
					10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
					11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
					12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
					13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
					14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T
					15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

Table 2. 64-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

CB	DATA	CB	DATA	CB	DATA	CB	DATA
0	28	20	127	40	E	60	101
1	1000F	21	10100	41	10029	61	10126
2	10000	22	1010F	42	10026	62	10129
3	27	23	128	43	1	63	10E
4	1000C	24	10103	44	1002A	64	10125
5	2B	25	124	45	D	65	102
6	24	26	12B	46	2	66	10D
7	10003	27	1010C	47	10025	67	1012A
8	10024	28	1012B	48	10002	68	1010D
9	3	29	10C	49	25	69	12A
A	C	2A	103	4A	2A	6A	125
B	1002B	2B	10124	4B	1000D	6B	10102
C	0	2C	10F	4C	26	6C	129
D	10027	2D	10128	4D	10001	6D	1010E
E	10028	2E	10127	4E	1000E	6E	10101
F	F	2F	100	4F	29	6F	126
10	10022	30	1012D	50	10004	70	1010B
11	5	31	10A	51	23	71	12C
12	A	32	105	52	2C	72	123
13	1002D	33	10122	53	1000B	73	10104
14	6	34	109	54	20	74	12F
15	10021	35	1012E	55	10007	75	10108
16	1002E	36	10121	56	10008	76	10107
17	9	37	106	57	2F	77	120
18	2E	38	121	58	8	78	107
19	10009	39	10106	59	1002F	79	10120
1A	10006	3A	10109	5A	10020	7A	1012F
1B	21	3B	12E	5B	7	7B	108
1C	1000A	3C	10105	5C	1002C	7C	10123
1D	2D	3D	122	5D	B	7D	104
1E	22	3E	12D	5E	4	7E	10B
1F	10005	3F	1010A	5F	10023	7F	1012C

Table 3. Minimal 32-bit check-bit to data tables for diagnostic use. One data value is listed to generate every possible check-bit pattern.

DATA	CB	DATA	CB	DATA	CB	DATA	CB
0	C	100	2F	10000	2	10100	21
1	43	101	60	10001	4D	10101	6E
2	46	102	65	10002	48	10102	6B
3	9	103	2A	10003	7	10103	24
4	5E	104	7D	10004	50	10104	73
5	11	105	32	10005	1F	10105	3C
6	14	106	37	10006	1A	10106	39
7	5B	107	78	10007	55	10107	76
8	58	108	7B	10008	56	10108	75
9	17	109	34	10009	19	10109	3A
A	12	10A	31	1000A	1C	1010A	3F
B	5D	10B	7E	1000B	53	1010B	70
C	A	10C	29	1000C	4	1010C	27
D	45	10D	66	1000D	4B	1010D	68
E	40	10E	63	1000E	4E	1010E	6D
F	F	10F	2C	1000F	1	1010F	1F
20	54	120	77	10020	5A	10120	79
21	1B	121	38	10021	15	10121	36
22	1E	122	3D	10022	10	10122	33
23	51	123	72	10023	5F	10123	7C
24	6	124	25	10024	8	10124	2B
25	49	125	6A	10025	47	10125	64
26	4C	126	6F	10026	42	10126	61
27	3	127	20	10027	D	10127	2E
28	0	128	23	10028	E	10128	2D
29	4F	129	6C	10029	41	10129	62
2A	4A	12A	69	1002A	44	1012A	67
2B	5	12B	26	1002B	B	1012B	28
2C	52	12C	71	1002C	5C	1012C	7F
2D	1D	12D	3E	1002D	13	1012D	30
2E	18	12E	3B	1002E	16	1012E	35
2F	57	12F	74	1002F	59	1012F	7A

Table 4. Minimal 32-bit data to check-bit tables for diagnostic use. At least one data value is listed for every possible check-bit pattern. This table is identical to Table 3 except in sequence of presentation.

Integrated Device Technology, Inc.

THE KEY ADVANTAGES OF MULTI-PORT STATIC RAM

PRELIMINARY APPLICATION NOTE AN-25

By Robert Stodieck

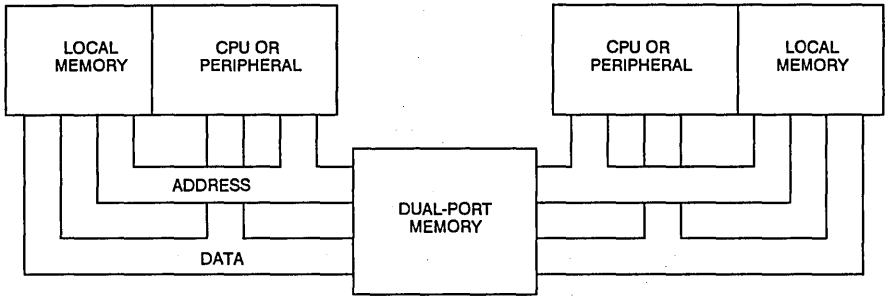

Figure 1. Dual-Port Memory With Separate Busses.

MULTI-PORT STATIC RAM MEMORY

The popularity of multi-port RAM has increased as designers have become more sophisticated about the inherent advantages of multi-ports as a communications devices. Multi-port memory can be far faster than alternate approaches to memory based communication, as well as being simpler to implement. Of the available RAM based communications links, dual-port RAM is the least likely to limit the data processing algorithms that the link is intended to facilitate.

THE HIERARCHY OF MEMORY BASED COMMUNICATIONS TECHNIQUES

Direct memory access (DMA) generally refers to a method of sharing common memory on a single common bus (fig 2). This requires that only one device at a time use the bus. This is a more efficient approach than having the CPU be responsible for all data transfers on a bus, since that usually requires multiple transfers on the bus for any data item moved (i.e. peripheral to CPU then CPU to memory). If the fraction of time spent in accessing peripherals is not large then this conventional DMA approach may be economical. The conventional DMA approach becomes limiting, as the fraction of time that each device needs to spend on a bus increases. This approach to DMA is completely inappropriate for implementing multi-processor schemes where, ideally, all the processors use a memory bus all the time.

Another approach to memory based communication is that of sharing a RAM in a time multiplexed fashion (fig 2). Time-sliced or ping-pong shared RAM can be more efficient than conventional DMA since it provides for independent busses and local memory. Even so, data transfer through a shared RAM interface, as we shall see, is inherently slower and less flexible than a multi-port RAM interface. The additional hardware associated with implementing a real-world shared RAM detracts significantly from the operating speed as well as being more complex and difficult to design.

DUAL-PORT TRANSFER SPEED ADVANTAGE OVER TIME-SHARED RAM

We will use a hypothetical, but realistic, case to examine the advantages of dual-ported memory over time shared RAM. Radar digital signal processing systems frequently use multi-port RAMs to act as a "rate-buffer". The multi-port is located between the analog-to-digital convertors, which must sample the incoming signals at a constant high rate, and the signal processing elements. The signal processors, in general, must access data from the incoming stream in a non-sequential way and this makes a hardware FIFO inappropriate for this task of rate buffering.

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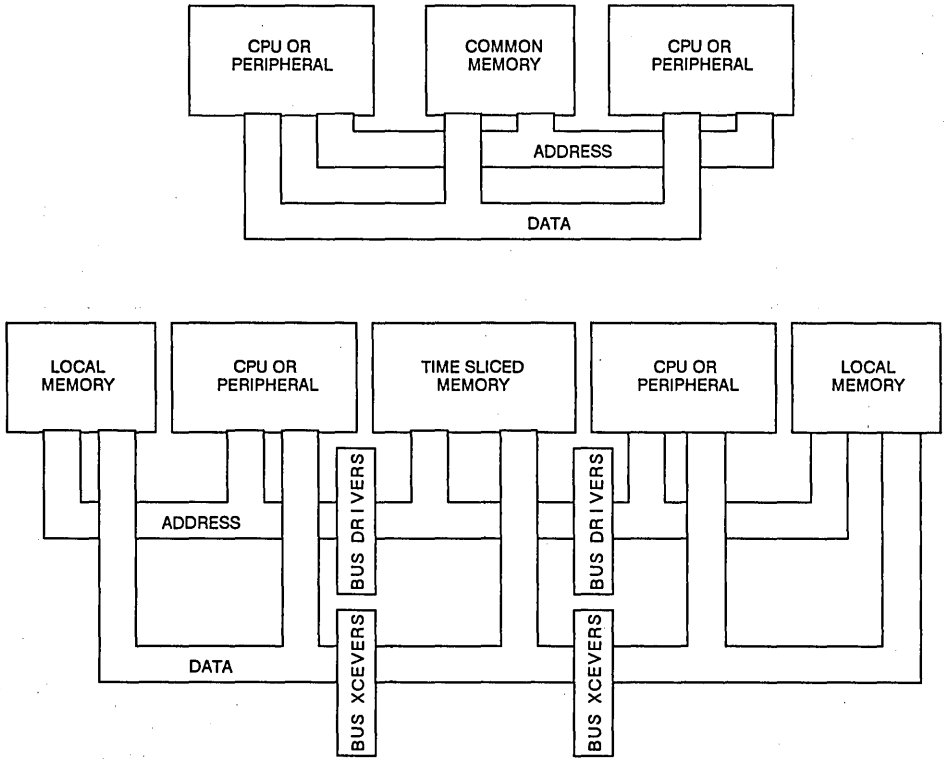

Figure 2. Two Members of a Hierarchy of Memory Based Communications. Common Memory With a Common Bus, Shared RAM with Separate Busses.

Assume that the minimum write access time on the side of the A/D convertor is 35ns and the read access time is 35ns on the signal processor side. The signal processor works on one data set of N words then switches to another. The signal processors accesses are random within a data set. The A/D convertor outputs data continuously in a word-serial stream that wraps around when it reaches the end of the RAM. The two sides never need to simultaneously access the same location.

A dual-port memory handles this communications task painlessly. To better see what the dual-port advantages are we will look at two possible alternatives. A time-sliced single RAM, and a ping-pong multiple RAM arrangement. Both approaches involve more hardware, more design-in time, and create more severe timing constraints than a multi-port memory. Both, we will see, limit the generality of the algorithms that may executed.

In order to begin to meet the basic timing requirements of our radar DSP system, the RAM in a time-sliced RAM system must have an access time at least half that of the equivalent dual-port. This is due to the fact that the RAM must do two accesses in the same time as the dual-port. The buffers required for address and data bus isolation in a real design, will have basic prop-delays of about 6.5ns. For the read path this would add 6.5 + 6.5 ns to the read cycle time. Thus before considering signal skews the basic RAM access times required would be less than 35/2-6.5ns-6.5ns or 4.5ns versus 35ns for a dual-port RAM.

SYNCHRONIZATION AND ALGORITHMIC CONSTRAINTS OF THE TIME-SLICED RAM

The time-sliced example shows us that the dual-port has more than twice the effective data communications bandwidth of a real-world time sliced RAM arrangement for any given RAM speed grade. The time-sliced arrangement also places serious constraints on the algorithms that can be run. To match the transfer rate of the dual-port, the reads and writes in the time-sliced RAM must now be interlaced one to one and thus must occur at the same rate. If reads cannot be cleanly interlaced with writes then the transfer rate may become grossly slower.

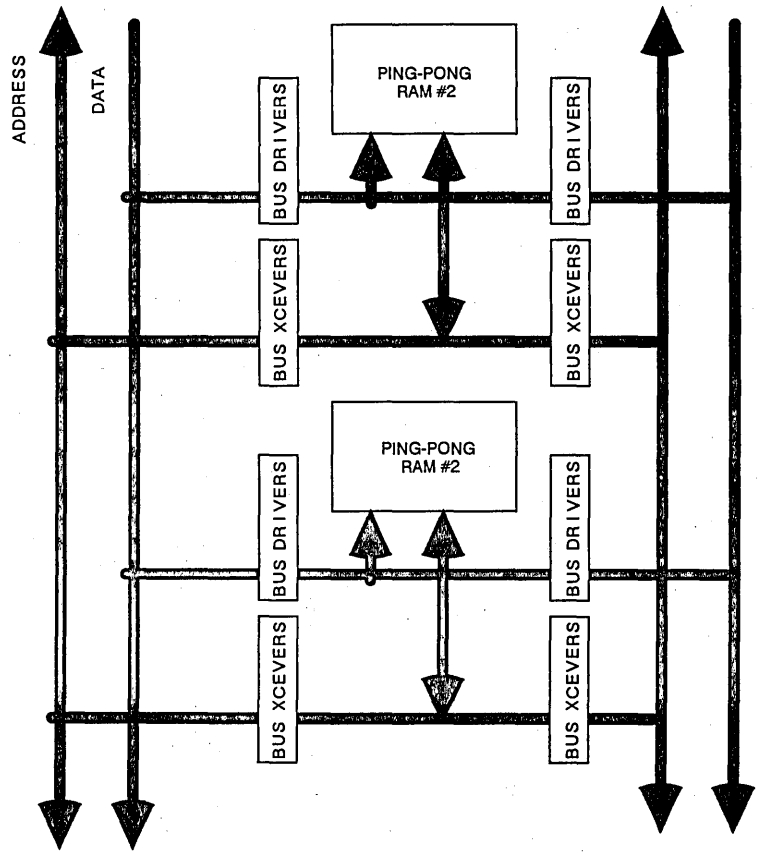

Figure 3. A RAM Ping-Pong RAM. This Arrangement Can be Expanded Indefinitely to Provide Any Number of Independent Sets.

DUAL-PORT RAM TRANSFER SPEED ADVANTAGES OVER THE PING-PONG RAM APPROACH

In order to begin to meet the basic timing requirements of our radar DSP system, the RAM in a ping-pong system (figure 3) must also have an access time that is less than that of the equivalent dual-port. Again in a real-world design, the buffers required for address and data bus isolation will have basic prop-delays of about 6.5ns best case. For the read path this would add 6.5ns + 6.5ns to the read access time. The basic RAM access times required would be less than 35 -6.5 ns-6.5 ns or 22ns.

SYNCHRONIZATION AND ALGORITHMIC CONSTRAINTS OF THE PING-PONG APPROACH

The same kinds of algorithmic constraints are introduced by a ping-pong schemes, but they are less severe than the time-sliced single RAM. In a ping-pong scheme, two or more RAMs are used. In the signal processing scheme, blocks of data are written alternately to one RAM and then the other. Simultaneous accesses are now allowed if they are to different physical RAMs. A two RAM ping-pong scheme could serve the RADAR signal processing example relatively well, if it can operate on only two data sets alternately. One RAM can be accessed at rates appropriate for the A to D convertor, and the other RAM can be accessed at rates appropriate for the signal processor.

If there are more than two datasets involved in the algorithm, we again have a potential scheduling conflict. One way to conquer this problem is to add yet more independent RAMs, One allocated to each dataset or block required by the overall machine algorithm. Each time we add an additional RAM, the algorithmic flexibility of the ping-pong communications link improves, until it approaches that of dual port RAM.

At this point it becomes apparent that we have created a spectrum of memory based communications devices. We can identify the members of this spectrum by the number of fully independent RAM blocks we can access. For example, a two RAM ping-pong arrangement, a three RAM ping-pong arrangement. By this numbering scheme a 1K dual-port is an order one-thousand device. It has one-thousand one word data sets 999 of which can be freely accessed at any time from one side. The order three pin-pong device has three multi-word data sets two of which can be freely accessed at any time from one side. The order two ping-pong device has two multi-word data sets one of which can be freely accessed at any time from one side. The time sliced RAM is an order 1 device and cannot allow any simultaneous accesses.

In this discussion we have ignored the size of the individual RAMs, and in fact there are no advantages to using large individual RAMs in a ping-pong arrangement as long as the total number of words available remains the same. In a ping-pong arrangement the physical RAM sizes determine the maximum data block size. This, again, reduces the number of algorithms that can be run without conflicts. In a dual-port, the data block size is a software variable. It is possible to define any number of arbitrarily sized data blocks for transfer in either direction. In general, hardware synchronization per se is not required, only data block synchronization.

DATA BLOCK SYNCHRONIZATION AND DATA COHERENCY IN TIME OR CONTEXT

A dual-port video interface is an example of a system where strict data-coherency in time is not required. It is usually not critical that a pixel be updated at a precise instant in time. An update can be made on one scan or the next if there is a timing conflict. However, data corruption in the RAM must be avoided.

The video example is a special case. In most data processing environments, however, all data written to memory has to be read again with perfect fidelity both in data content and in coherency in time or context. A reading device must know not only what data was written but it must also know its exact context or meaning. In any common memory system it is possible for data to be changed in a location with out 'informing' all of the devices using the data. So a mechanism must exist for updating the context of data for all devices using data from shared locations.

The passing of context or time information is usually done by semaphores or interrupts. This information synchronizes data-block transfers and, consequently, prevents simultaneous accesses to any location. Data writes and reads may be asynchronous from each other in timing of individual accesses, but the reading of a block of data does not begin until a block of data has been written and its context is known.

The importance of observing that data-coherencyin-time has to be guaranteed in software, in a particular system, is that it often eases the hardware design. For example, "busy" arbitration logic can be used to prevent simultaneous accesses to a single location. Busy logic might appear to be an essential feature of dual-port RAM systems. However, an active busy signal coming on a dual-port usually indicates that something has gone wrong in software or hardware. In any system where strict data coherency-in-time or context is required, i.e. the transfer is block-synchronous, simultaneous accesses to one physical location cannot be allowed because the outcome is not deterministic. (Simultaneous write-read access to one address can be allowed in synchronous systems if timing is done correctly).

TRANSFER ALGORITHMS

Having established that in general purpose computing environments data is normally passed in a block synchronous fashion it is useful to classify some common block transfer algorithms.

1. First-in-first-out (FIFO) buffer Word serial entry, word serial output in the same sequence.
2. Last-in-first-out (LIFO) buffer or stack Word serial entry, word serial output in reverse sequence.
3. Random input, random output buffers
4. Word Serial input/output, random output/input

Any of these algorithms can be run with any of the common memory schemes discussed. The dual-port solution will generally be faster, easier to implement, and much less confining in utilization.

As a simple illustration of dual-port flexibility, consider the fact that a FIFO algorithm could be executed with a hardware FIFO. Using a dual-port RAM, instead, would allow any number of FIFO algorithms to run simultaneously in both directions, along with other types of transfers.

SUMMARY

Single-chip dual-port memory offers greater data transfer rates, easier hardware design, and greater flexibility of application than any competing approach. It facilitates rate-buffering between hardware devices and allows bidirectional transfer. It's intrinsically separate address and data busses make it far faster than conventional approaches to DMA for peripheral-to-CPU data transfer. The application of dual-ported static RAM has seen rapid growth as multiple sources have become available, assuring that multi-ported static RAM will become a mainstream product.

Integrated Device Technology, Inc.

INTERRUPT LATENCY AND HANDLING IN THE IDT79R3000

APPLICATION NOTE AN-26

By Satyanarayana Simha

INTRODUCTION

The exception processing capability of the IDT79R3000 is provided to assure an orderly transfer of control from an executing program to the supervisor program. Exceptions may be broadly divided into two categories: those caused by an instruction, including an unusual condition arising during its execution, and those caused by external events such as interrupts. When an IDT79R3000 detects an exception, the normal sequence of instruction is suspended; the processor exits User mode and is forced to the Kernel mode where it can respond to the abnormal or asynchronous event. This paper presents an overall view of the types of exceptions in the R3000 and the exception handling registers. It then describes one specific exception, namely interrupts, the latency associated with it and gives an example of code on how to handle an interrupt event.

EXCEPTION PROCESSING

The R3000's exception handling system efficiently handles machine exceptions, including Translation Lookaside Buffer (TLB) misses, arithmetic overflows, I/O interrupts, system calls, breakpoints, reset, and coprocessor unusable conditions. All of these events interrupt the normal execution flow. The R3000 aborts the instruction causing the exception and also aborts all those following in the exception pipeline which have already begun execution. The R3000 then performs a direct jump into a designated exception handler routine.

When an exception occurs, the R3000 loads the EPC (Exception Program Counter) with an appropriate restart location where execution may resume after the exception has been serviced. The restart location in the EPC is the address of the instruction causing the exception. If the exception occurred in a branch delay slot, the EPC contains the address of the branch instruction immediately preceding the delay slot.

EXCEPTION HANDLING REGISTERS

The system coprocessor (CP0) registers contain information pertinent to exception processing. Software can examine these registers during exception processing to determine such things as the cause of an exception, and the state of the CPU at the time of an exception. There are six registers handling exception processing (shown in Figure 1). These are the *Cause* register, the *EPC* register, the *Status* register, the *BadVAddr* register, the *Context* register, and the *Prid* register. A brief description of each follows.

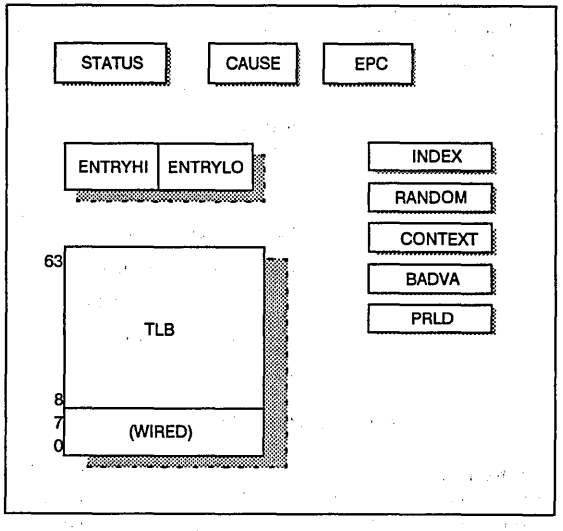

Figure 1. The Exception Handling Registers

The Cause Register:

The contents of this register describe the last exception. A 4-bit exception code indicates the cause. The remaining fields contain detailed information specific to certain exceptions. All bits in this register with the exception of the Sw bits are read-only. The Sw bits can be written into in order to set or reset software interrupts. See Figure 2.

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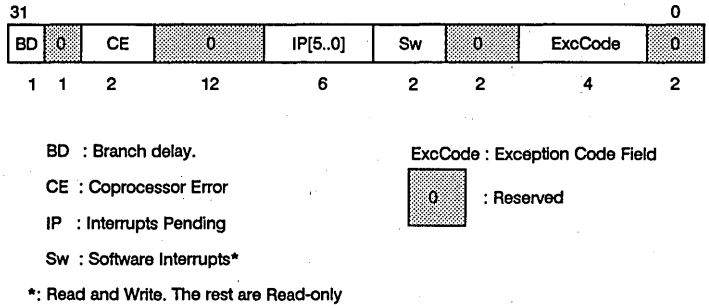


Figure 2. The Cause Register

The EPC (Exception Program Counter) Register:

The 32-bit register contains the address where processing can resume after an exception has been serviced. This register contains the virtual address of the instruction that caused the exception. When the virtual address of the instruction resides in a branch delay slot, the EPC contains the virtual address of the instruction immediately preceding—which is the Branch or Jump instructions.

Bad VAddr Register:

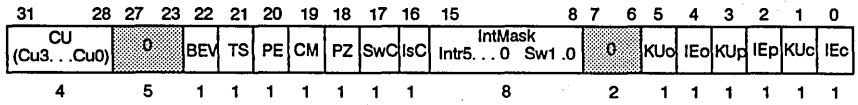
The Bad VAddr register saves the entire bad virtual address for any addressing exception.

Context Register:

The Context register duplicates some of the information in the BadVAddr register, but provides the information in a form that may be more useful for a software TLB exception handler.

The Status Register:

This register contains all the major status bits. Any exception puts the system in Kernel mode. All bits in the status register, with the exception of the TS (TLB shutdown) bit are readable and writeable; the TS bit is read-only. Figure 3 shows the functionality of the various bits in the status register.



CU : Coprocessor Usability
BEV : Bootstrap Exception vector
TS : TLB shutdown
PE : Parity Error
CM : Cache Miss
PZ : Parity Zero
SwC : Swap Caches
IsC : Isolate Cache
IntMask : Interrupt Mask
KUo : Kernel/User mode, old
IEo : Interrupt enable, old
KUp : Kernel/User mode, previous
IEp : Interrupt enable, previous
KUc : Kernel/User mode, current
IEc : Interrupt enable, current
O : Reserved

Figure 3. The Status Register

Processor Revision Identifier Register:

This 32-bit register contains information that identifies the implementation and revision level of the Processor and System Control Co-Processor.

EXCEPTION VECTOR LOCATIONS

The R3000 uses three different addresses for exception vectors:

- The RESET exception vector is at address *0xbfc00000*
- The UTLB Miss exception vector at address *0x80000000*
- The General exception vector for all other exceptions at address *0x80000080*

LATENCY FOR EXCEPTION PROCESSING

Different types of exceptions can occur in different stages of the pipeline. The exception handling routine itself occurs after a one cycle latency. The R3000 has a five stage pipeline that consists of instruction fetch, instruction decode, ALU operation, cache fetch, and the write-back stage. Table 1 shows in the last column the number of instructions in the pipeline that need to be flushed on an exception. Address error, for example, can have a maximum latency of four if it occurs on a memory operation cycle. This is because four instructions in the pipeline stage have to be flushed.

Error	Pipeline stage	Pipeline stages to be flushed
Illegal Instruction	Instruction Decode	2
Address Error	Memory Operation	4
Interrupts	Instruction Fetch	3
Overflow	ALU Operation	3
TLB Miss	Instruction Decode	2

Table 1. Latency in the R3000 on an exception

Figure 4 shows the pipeline stages in the R3000. The different stages are I:Instruction fetch; R:Read Decode; A:ALU operation; M:Memory operation; and W:Write-Back. When there is an exception on an instruction fetch cycle, the exception routine starts executing one clock cycle later as shown.

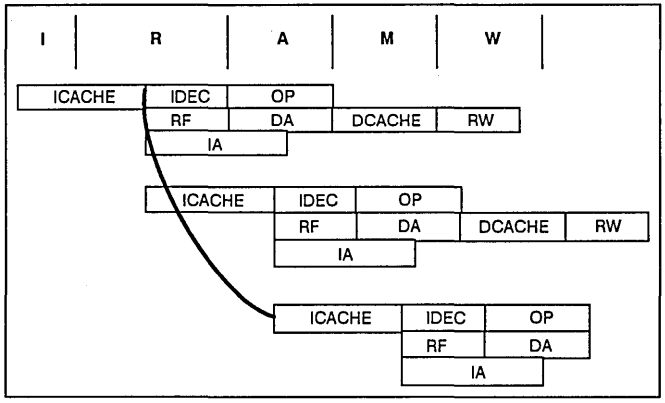


Figure 4. Pipeline Stages in the R3000

INTERRUPTS IN THE IDT79R3000

The R3000 processor has six general purpose hardware interrupts and two software generated interrupts. The hardware interrupts are sampled during phase 2 of all run and fixup clock cycles. This is shown in Figure 5. t_{DS} is the data setup time, t_{HLD} is the data hold time and t_{SMP} is the phase delay between the Clk2xSmp input and the Clk2xPhi input. These two clock inputs are part of the four phase clock inputs given to the processor and are useful for selecting the proper static RAM parts for interface considerations. The interrupts are level-sensitive. They continue to be sampled during phase 2 of the clock cycle after an interrupt exception has occurred. The interrupts are not latched within the processor when an interrupt exception occurs. Since the interrupts are not sampled during stall cycles, BusErr* can be asserted and used for exception processing. This is useful in cases where there is a need to abort from a stall mode.

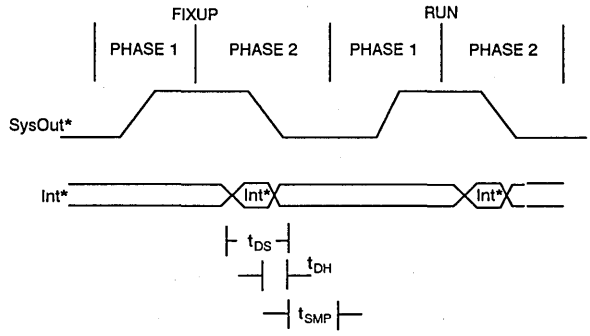


Figure 5. Interrupt Timing Diagram

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Each of the eight interrupts can be individually masked by clearing the corresponding bit in the IntMask field of the Status Register. All eight of the interrupts can be masked at once by clearing the IEc bit in the Status Register.

INTERRUPT HANDLING

The R3000 branches to the general exception vector at address 0x80000080 for the exception. The R3000 sets the Int code in the Cause Register's ExcCode field. The IP field in the Cause register shows which of the six hardware interrupts are pending and the SW field in the Cause register shows which of the two software interrupts are pending. Multiple interrupts can be pending at one time.

When the interrupt occurs, the KUp, IEp, KUc and IEc bits of the Status register are saved in the KUo, IEo, KUp, IEp bit field in the Status register. The current kernel status bit KUc and the interrupt bit IEc are cleared. See Figure 6. This masks all the interrupts.

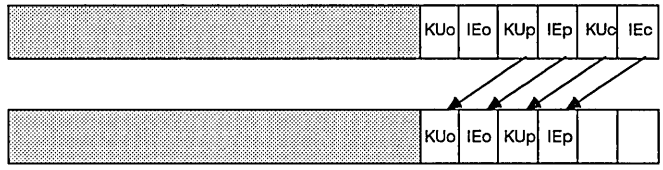

Figure 6. Kernel Status and Interrupt Status Are Saved on Interrupts

INTERRUPT SERVICING

In case of an hardware interrupt, the interrupt must be cleared by deasserting the interrupt line. This has to be done by alleviating the conditions that caused the interrupt. Software interrupts have to be cleared by setting the corresponding bits (SW1:0) in the Cause register to zero. A flow chart of a general exception routine handler is shown in Figure 7.

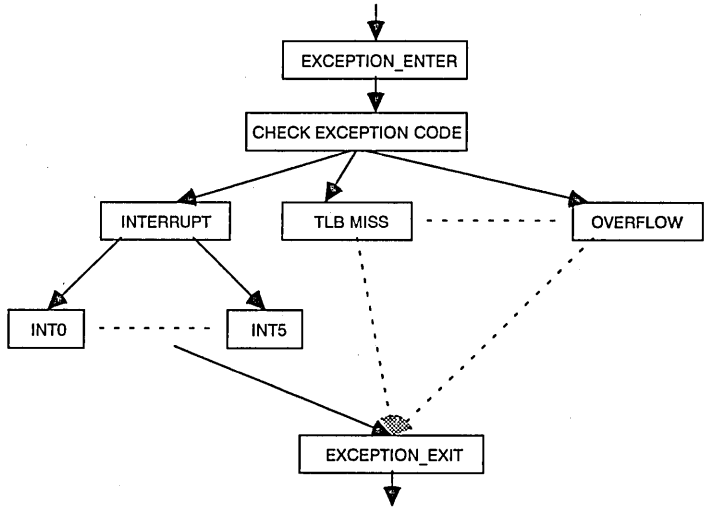

Figure 7. Flow Chart for Exception Handling

An example piece of code is given below in Figure 8. It illustrates a simple service routine that the processor branches to on detecting an interrupt. The actual interrupt handling code itself will depend on the user's application and, therefore, is not given. (an and sn are registers in the R3000.)

As soon as the branch to the address is taken on an interrupt, the exception program counter is saved. Line 2 indicates the reading of the cause register to determine the exception (in this case an interrupt). The status register is saved to be restored after processing the exception. A lookup table contains the addresses of all the different exception processing routines. A jump is taken to the appropriate exception routine.

```
1.      mfc0    a0,EPC          ;save exception PC
2.      mfc0    a3,C0_CAUSE     ;get CAUSE register
3.      mfc0    s0,C0_STATUS    ;save status register
```

```
4.          and     a1,a3,CAUSE_EXC_MASK   ;get entry to
                    index into look up table
5.          lw      a2,causevec(a1)        ;register a2 with address
                                           in look up table
6.          j       a2                     ;jump to service routine
            —                              (line 7)
7. intr:    and     a4,a0,INT_CAUSE        ;load interrupt level in
                                           register
8.          lw      t1,int_level(a4)       ; index into interrupt level
                                           'n' routine.
            —                              ;go to interrupt routine for
            —                              level 'n'
9.          j       t1                     ;return from interrupt
                                           routine
10.         mtc0    a0,EPC
11.         mtc0    s0,C0_STATUS           ;restore status register to
                                           previous value
12.         rfe                            ;restore status and
                                           interrupts prior to
                                           exception exit
```

Figure 8: Interrupt Service Routine Example

Figure 9 illustrates a simplistic block diagram of an R3000 board with the interrupt lines connected to a PAL device. The PAL logic is designed to affect the R3000 run-time behavior and it defines the state of the interrupt lines during Reset. Accordingly, the R3000 can be initialized to work as a big-endian or a little-endian processor, its block refill rate can be varied, etc.

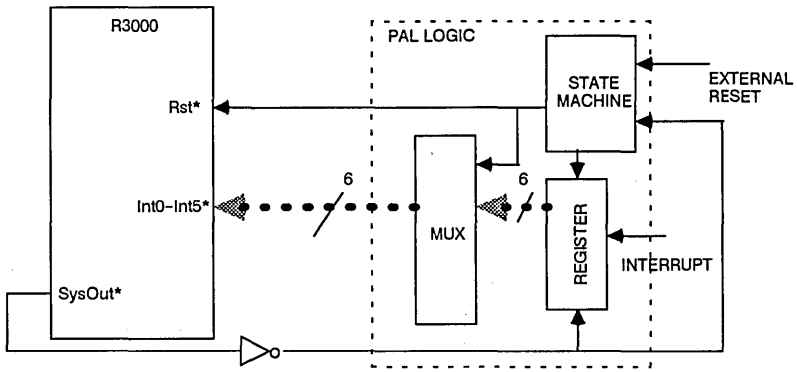

Figure 9: Block Diagram of Interrupt Controller on Reset

CONCLUSION

The IDT79R3000 provides both flexible and fast exception handling capability. Once an exception occurs, the first instruction of the exception handler routine is fetched on the very next clock cycle, providing minimal latency. Management of the processor and system state is left to the exception handling software, allowing the system designer to determine what must be done to respond to a given exception and thus minimizing the amount of processor overhead required to handle exceptions. Even the prioritization of the external interrupts is under software control, providing the system designer with maximum flexibility in the target system*.

*Note: Chapter 5 of the "MIPS RISC Architecture" Book, available from IDT, contains further detail on exception processing of the 79R3000.

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Integrated Device Technology, Inc.

CACHE DESIGN CONSIDERATIONS USING THE IDT 79R3000

APPLICATION NOTE AN-27

By Satyanarayana Simha

INTRODUCTION

The reduced instruction set computer (RISC), the IDT79R3000, has allowed for simplicity in hardware and synergy between architecture and compilers. To further increase the throughput of a computer system, direct-mapped cache memory is implemented on systems using the R3000. The availability of a wide variety of high-speed static RAMs from IDT gives the designer the flexibility of selecting the proper part for his application. It is necessary, however, to know the critical timing parameters governing the design of a cache subsystem. This article is divided into three parts. The first part shows a general cache system with a description of the clock inputs. The second section details the equations used to calculate the critical parameters. It is followed by an example of an IDT7198 static RAM used as a cache RAM for the R3000.

CACHE DESIGN

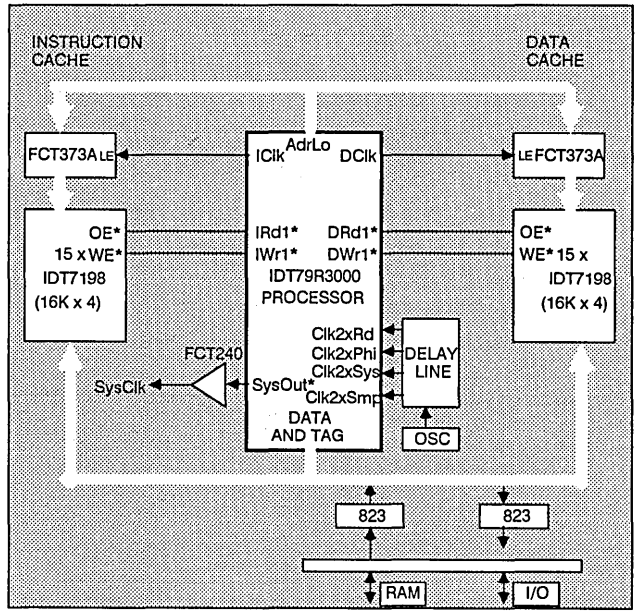

Figure 1. 64KB Instruction/Data Cache Configuration

A simplistic block diagram implementation of a 64KB separate instruction cache and data cache is shown in Figure 1. The design of a cache subsystem such as the one above depends on the four input clocks to the R3000 processor. These clock inputs are twice the frequency of the output clock i.e., SysOut. By adjusting the timings of these clocks, the designer can accommodate a wide variety of static RAMs by properly considering specific parameters such as set-up and hold times. The clocks themselves can be adjusted using tap settings on a delay line or by using delay logic. The clock inputs are described below.

1) Clk2xSyS: Determines the position of SysOut with respect to the data, tag, and address buses. It is positioned so that devices in the cache/bus interface clocked by SysOut meet the set-up and hold time requirements.
2) Clk2xSmp: Is used by the R3000 to capture external data onto data bus and control inputs.
3) Clk2xRd: Is used to delay the enable of data bus drivers.
4) Clk2xPhi: Is used to determine all R3000 outputs i.e., data, address, and tag buses.

Figure 2 shows the timing relationships between the four clocks. All the timing equations for cache design depend on the phase relationship between these clocks. T_{smp} is the Clk2xSmp to Clk2xPhi delay, T_{rd} is the Clk2xRd to Clk2xPhi delay, and T_{sys} is the Clk2xSys to Clk2xPhi delay.

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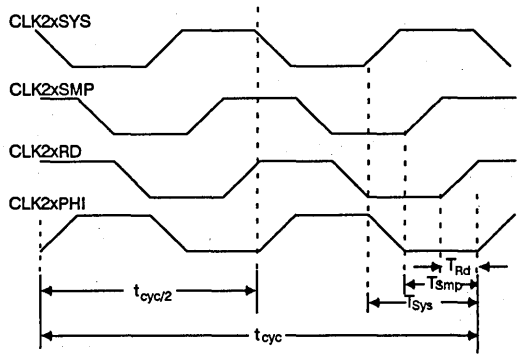

Figure 2. Timing Relationships Between the Four 2x Clock Inputs

In the cache implementation scheme, instruction references begin their reference during phase 2 and transfer data during the following phase 1. Data references begin during phase 1 and transfer data during phase 2. Thus, data and instruction references can take place in different phases of the same clock cycle. See Figures 3a and 3b. This is an important factor to consider in order to prevent contention between instruction and data caches.

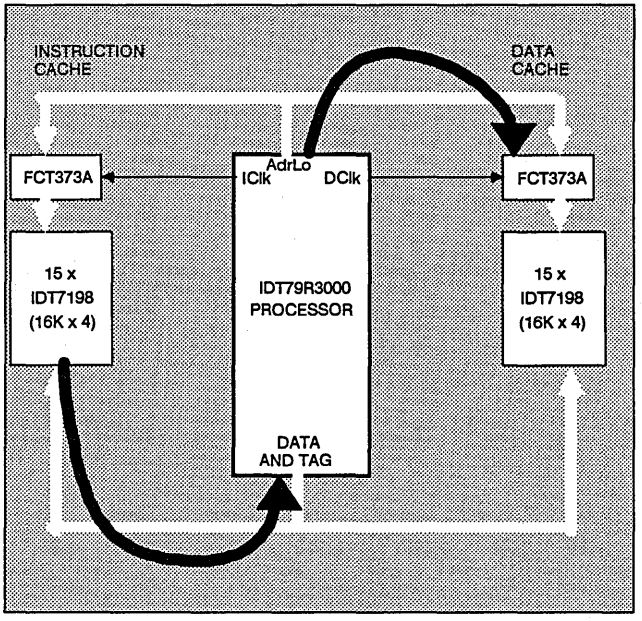

Figure 3a. Data and Instruction Caches During Phase 1

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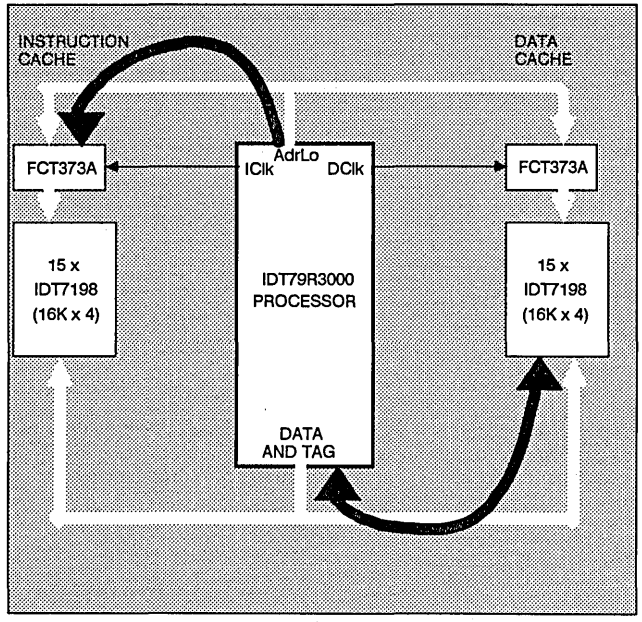

Figure 3b. Data and Instruction Caches During Phase 2

Specific factors such as access time, set-up time, hold time, enable and disable times, and the deration factor are key in choosing the proper static RAM and in setting the phase delays in the clocks. The next section discusses the timing equations needed for selecting a static RAM for cache design.

Equations Governing the Critical Parameters in RAM Selection:

Figure 4 shows the timing of the relevant signals for a 25MHz (40ns) R3000. The numbers represent the equations that are critical in determining the selection of the static RAMs. The timing is given for the worst case condition i.e., a STORE followed by a LOAD. An explanation of the equations is given below.

Internal Sample to Phi: This timing parameter requirement guarantees that the processor internal sample to Phi is met.

$t_{smp} \geq 5ns$ ---------- (1)

Address Access to Data Sample: This timing parameter requirement guarantees that the cache RAMs have sufficient access time. This calculation assumes that the address delay through the FCT373 is limited by its propagation delay.

$RAM^{d}_{AA} \leq t_{cyc} - t_{smp} - AdrLo^{d*} - 373_{PD} - t_{os}$ --- (2)

Cache Enable to Sample: This timing parameter requirement guarantees that the cache RAMs are enabled soon enough to meet the processor's input set-up specification.

$RAM_{OE}{}^{d} \leq T_{cyc/2} - t_{smp-rd} - Rd^{d} - t_{os}$ ------- (3)

Minimum Read Pulse Width: This timing parameter requirement guarantees that the read pulse generated by the processor is at least as long as the cache RAM output enable time.

$RAM^{d}_{OE} \leq t_{cyc/2} - t_{sys-rd}$ ---------- (4)

Read Write I-Cache Data Bus Contention: This timing parameter requirement guarantees that no contention will occur between the instruction cache and the processor on a store.

$RAM_{HZ} \leq t_{sys} - Rd^{d} + D_{en}$ ----- (5)

Processor Data Set-up to End of Write: This timing parameter requirement guarantees that the cache RAMs have adequate data set-up time when being written into by the processor.

$RAM_{SD} \leq t_{cyc/2} - t_{smp} - DVal^{d} + Wr^{d}$----- (6)

Data Hold from End of Write: This timing parameter requirement guarantees that the data hold from end of write specification of the cache RAMs is met when either the processor or the read buffer is writing to the RAMs.

$RAM_{HD} - RAM_{LZ} \leq t_{smp-rd}$ -------- (7)

Data Set-Up to SysClk: This timing parameter requirement guarantees that the set-up time into an external register is met on a processor store.

$SetUp_{sys} \leq t_{cyc/2} - t_{sys} - (DVal^{d} + - Sys^{d} - 240_{PD})$-- (8)

Data Hold from SysClk: This guarantees that the hold time specification of an external register is met on a processor store. The data holds on the bus until a subsequent read drives new data.

$Hold_{sys} \leq t_{sys-rd} - Sys^{d} - 240_{PD} + RAM_{LZ} + Rd^{d}$ - (9)

Equations 1 to 9 are sufficient for the purpose of selecting the proper RAMs for use as cache memory. To illustrate the point further, an IDT RAM device, the IDT7198 (16K x 4), is chosen as an example.

*d: Deration due to additional load. 1ns per 25pF.

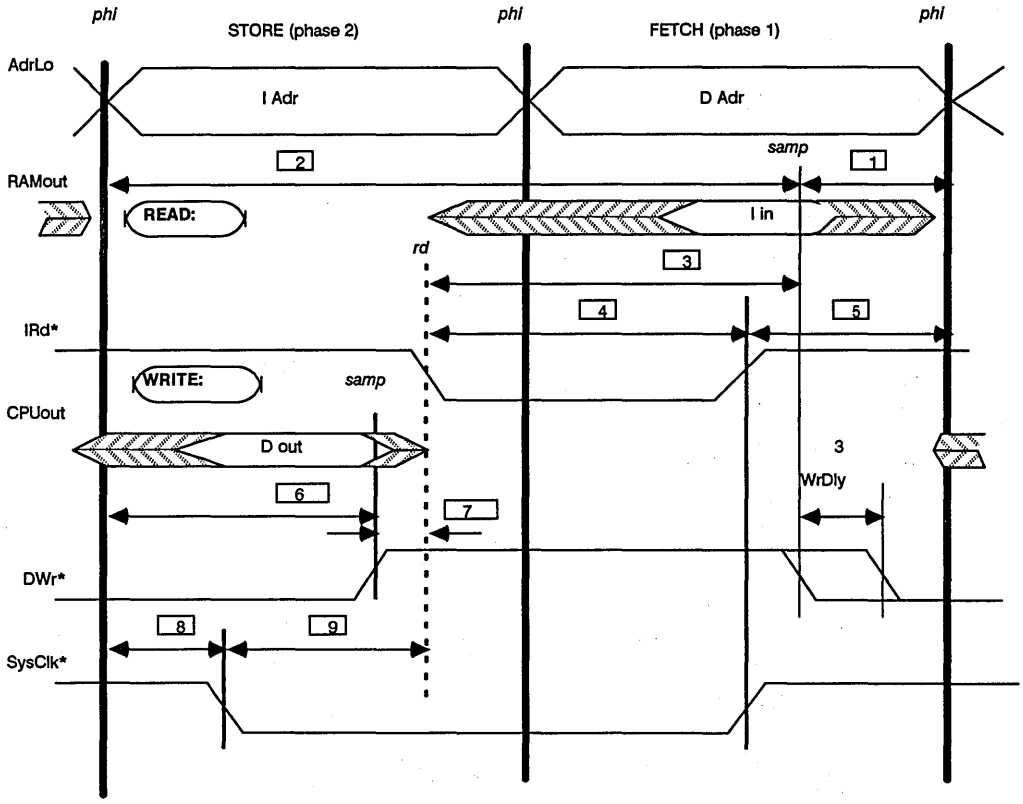

Figure 4. IDTR3000 40ns (25MHz) Cycle Timing

CALCULATION OF TIMING PARAMETERS

An example of a cache subsystem design using an IDT7198 i.e., a 16 K x 4 static RAM follows. All the numbers used in the calculations have been taken from the IDT Data Book[1] and the R3000 Interface Manual. The numbers are presented in Figure 6. The deration factor has been taken into account for DIPs. Surface mount would decrease the deration factor.

The following factors have been taken into account for calculating the deration factor[2].

1) The SSI logic and cache RAM propagation delays are derated by 1ns per 25pF of additional load.
2) Cache RAM input capacitance is 5pF.
3) Cache RAM output capacitance is 7pF.
4) Trace capacitance is estimated at 2pF per inch.
5) Data and trace tag buses are 6 inches.
6) Address buses are 2 x 5 inches.
7) SysOut loading is 50pF.
8) Test value of 30pF to be subtracted.

Deration Calculations:

Address Capacitance: 12 x 2pF = 24pF; (factors 4,5, and 6) 5 Devices = 5 x 10pF = 50pF; Test value = -30pF; Total capacitance = 45pF; At 1ns per 25pF, total deration of address bus = 2ns.

Data Bus Deration: Is approximately the same i.e., 2ns. Read control capacitance for IDT7198 will be about 10 inches of trace and 8 devices at 7pF each. Therefore, Read control deration = (76-30)pF/25pF/ns = 2ns.

In Figure 5, the circled numbers are the equations previously described. The number in parentheses is the allowable worst case timing. The adjacent number is the total time taken using the IDT7198. The numbers for the IDT7198 with the R3000 running at different frequencies and the FCT373A are shown in Table 1 and Table 2 respectively.

The first value for each parameter in Table 1 shows the maximum allowable worst case rating and the second value shows the timing using the IDT7198 RAM.

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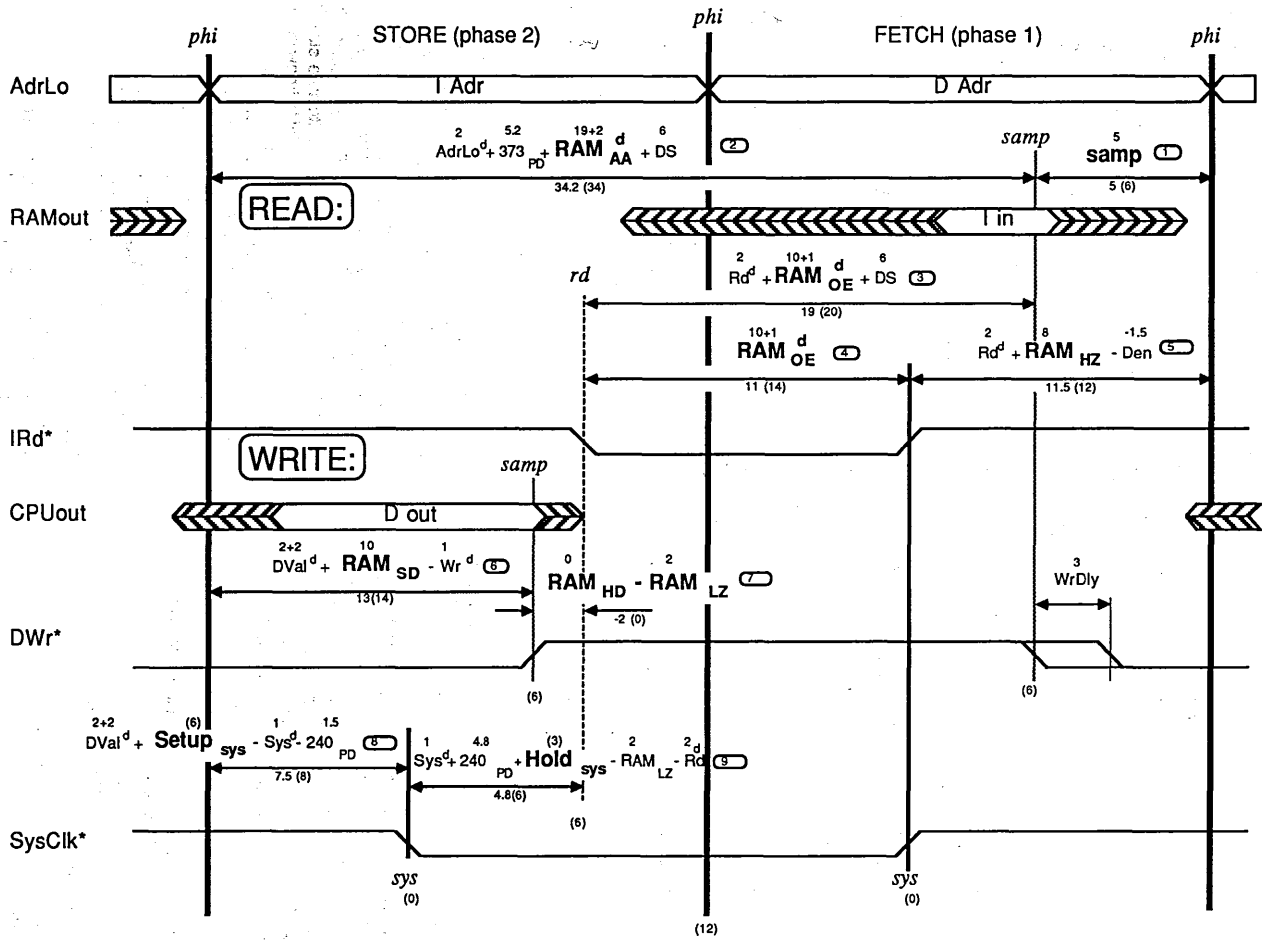

Figure 5: IDT79R3000 40 ns cycle timing using an IDT 7198 SRAM.

Parameter	Load (pF)	Symbol	R3000 Clock Frequencies					
			Min. (ns)	16MHz Max. (ns)	Min. (ns)	20MHz Max. (ns)	Min. (ns)	25MHz Max. (ns)
Address to Data Valid	30	t_{AA}		31		25		19
				29		25		19
Output enable to Data Valid	30	t_{DOE}		17		13		10
				15		13		10
Output Disable time		t_{HZ}		14		12	2	8
				12		10		7
Output Enable Time		t_{LZ}	2		2		2	
			5		5		5	
Address SetUp to End of Write		t_{AW}	43		36		27	
			20		20		13	
Data SetUp to End of Write		t_{DS}	14		13		11	
			13		13		8	
Write Pulse Width		t_{PWE}	55		47		37	
			20		20		13	
Data Hold from End of Write		t_{HD}	0		0		0	
			0		0		0	
Address Hold from End of Write		t_{HA}	0		0		0	
			0		0		0	

Table 1. Cache RAM Parameters. RAM Specifications vs. IDT7198 Specifications.

Parameter	Load (Units)	Symbol	Min. (ns)	Max. (ns)
FCT373A Propagation Delay	50	$t_{373\ PD}$		5.2
FCT373A Latch Enable Delay	50	$t_{373\ LE}$	2	8.5
FCT373A Latch Enable Hold	50	$t_{373\ Hld}$	1.8	
FCT240A Prop Delay	50	$t_{240\ PD}$	1.5	4.8

Table 2. Parameters for Latches and Buffers

Figure 6 shows a block diagram of tap settings on a delay line for the four clock input signals. By varying the phase delay between these signals, the designer can select the proper static RAMs for cache memories and the operating frequency of the R3000. Table 3 shows suggested tap settings on the delay line for the R3000 running at different frequencies.

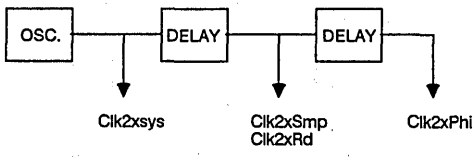

Figure 6. Tap Settings for the Clock Inputs

Parameter	16.67MHz	20MHz	25MHz
Clk2xSys	0	0	0
Clk2xRd	6	6	6
Clk2xSmp	6	6	6
Clk2xPhi	16	14	12

Table 3. Delay Line Setting Summarization

The designer can use a DDU-7F-20* chip for the delay line. The clock is the input to the device and the outputs at various points can be chosen with the appropriate phase delays.

CONCLUSION

The IDT R3000 RISC processor allows an efficient cache system to be implemented with standard architecture static RAMs. To design a cache subsystem, it is essential to know only the critical equations mentioned above and their relation to the four input clocks. The tap settings provide further control of the cache subsystem design for different operating frequencies of the R3000.

REFERENCES

1. IDT Data Book, pp 4-74 -- 4-83, pp 10-72 -- 10-75.
2. MIPS R3000 Processor Interface Manual, pp 105.

*d: deration due to additional load. 1 ns per 25 pF.

*Available from Data Delay Devices (201) 772-1106

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Integrated Device Technology, Inc.

USING THE IDT79R3000 IN A MULTIPROCESSOR ORGANIZATION

APPLICATION NOTE AN-28

By Roy M. Johnson

INTRODUCTION

High performance systems, such as shared memory multiprocessor architectures, can be built using IDT79R3000 RISC processors. The IDT79R3000 incorporates special features that provide support for multiprocessor environments. This applications note discusses the features of shared memory multiprocessor architectures with local caches, examines the critical issue of cache coherency, and demonstrates how the features of the IDT79R3000 facilitate its use in a shared memory multiprocessor system.

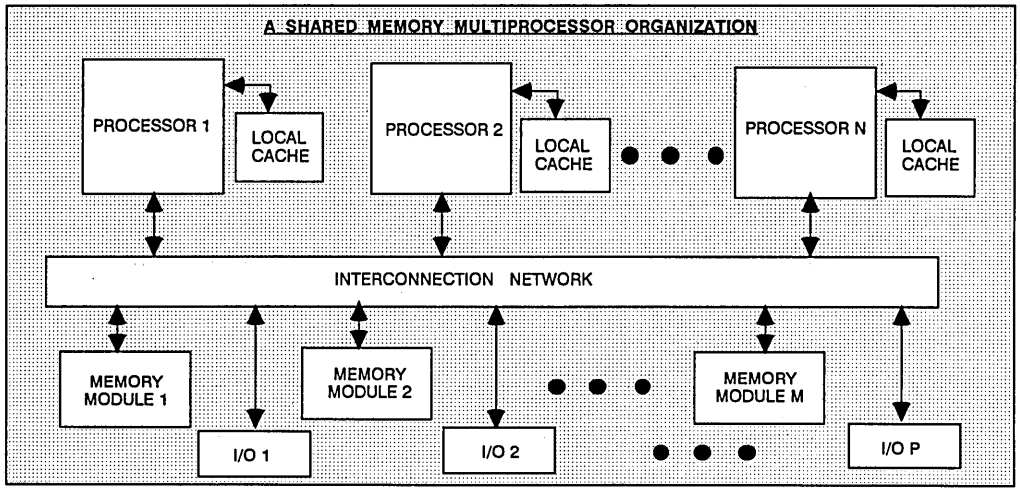

Figure 1. Block Diagram of a Shared Memory Multiprocessor System

SHARED MEMORY MULTIPROCESSOR SYSTEMS

A simplified block diagram of a shared memory multiprocessor with local caches is shown in Figure 1. This model of a multiprocessor system is defined to be tightly coupled and the N processors are connected to M memory modules and P I/O devices via an interconnection network. All the processors have a local cache memory, share the same global address space and communicate via shared memory. The interconnection network ensures complete connectivity between the processors and memory modules and can be implemented as a simple shared bus, multi-stage delta network or a more complex cross-bar switch. The global shared address space is assumed to be interleaved amongst the memory modules in order to minimize memory access conflicts. Note that the need for a interconnection network can be obviated by using a multi-port memory [1]. Examples of commercial machines employing a shared memory multiprocessor configuration using the R2000/3000 RISC processor include the Titan Graphics Supercomputer from Ardent Computers [2] and the 4D-MP Graphics Superworkstation from Silicon Graphics [3].

CACHE COHERENCY

The presence of local caches in a shared memory multiprocessor system introduces the issue of cache coherency that may result in data inconsistencies. This problem arises because several copies of the same data may exist in local caches of different processors at the same time. If one of the processors modifies (writes) the value of its copy of the data, then the other processors will have the stale or incorrect copy of the modified data in their local caches. This is a potential problem created by asynchronous parallel algorithms that do not have explicit synchronization. Data inconsistencies may also arise in multiprogrammed multiprocessor systems whereby a suspended process may migrate to another processor and the most recently updated data of the process might still be in the original processor's local cache. When the process is run on the new processor, there is a possibility that stale data is used if the local cache was not previously flushed. This assumes that the process did run previously on this processor. It is clear that if data consistency is to be ensured in a multiprocessor system, cache coherency must be maintained.

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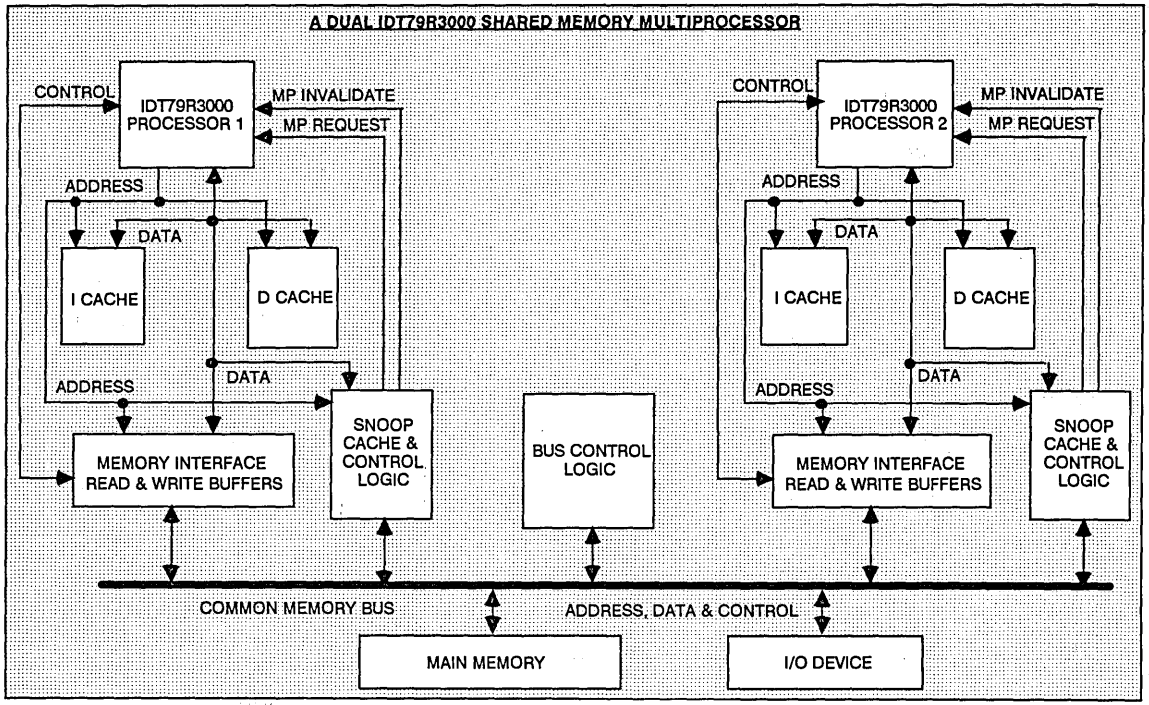

Figure 2. Block Diagram of a Dual IDT79R3000 Shared Memory Multiprocessor

A static approach to maintain cache coherency is to make all writeable data that is shared, non-cacheable. This method ensures data consistency, but at the price of decreased performance and with increased main memory conflicts. A dynamic approach to maintain cache coherency is to allow multiple copies of shared writeable data to exist and rely on a *cache coherence protocol* between the processors to ensure cache consistency. Several cache coherence protocols have been proposed and implemented using both hardware [4] and software support [5]. The type of protocol used depends primarily on interconnection network and the number of processors in the system.

A DUAL IDT79R3000 SHARED MEMORY MULTIPROCESSOR

A simplified block diagram of a dual IDT79R3000 shared memory multiprocessor is shown in Figure 2. A simple shared bus configuration was chosen for clarity. The two processors are connected to the main memory and an I/O device via a common bus. Access to the shared bus is arbitrated by the bus control logic. Each processor has an instruction and data cache and write-through cache update policy is assumed, i.e. all writes to the cache are also immediately transmitted directly to main memory. Note that a write-back cache update policy, (writes done only to the cache and main memory is updated when the cache line is replaced) would generate less memory traffic [10]. This is usually implemented when there are more than two processors in the system. Read and write buffers are included to provide a convenient asynchronous interface to the main memory. The snoop cache and control logic is used to implement a dynamic cache coherency check mechanism. For clarity, a very simple cache coherence protocol is chosen for the dual IDT79R3000 multiprocessor system and is described in detail below (more sophisticated and efficient schemes are described in [4], [5], [6], [7] & [8]).

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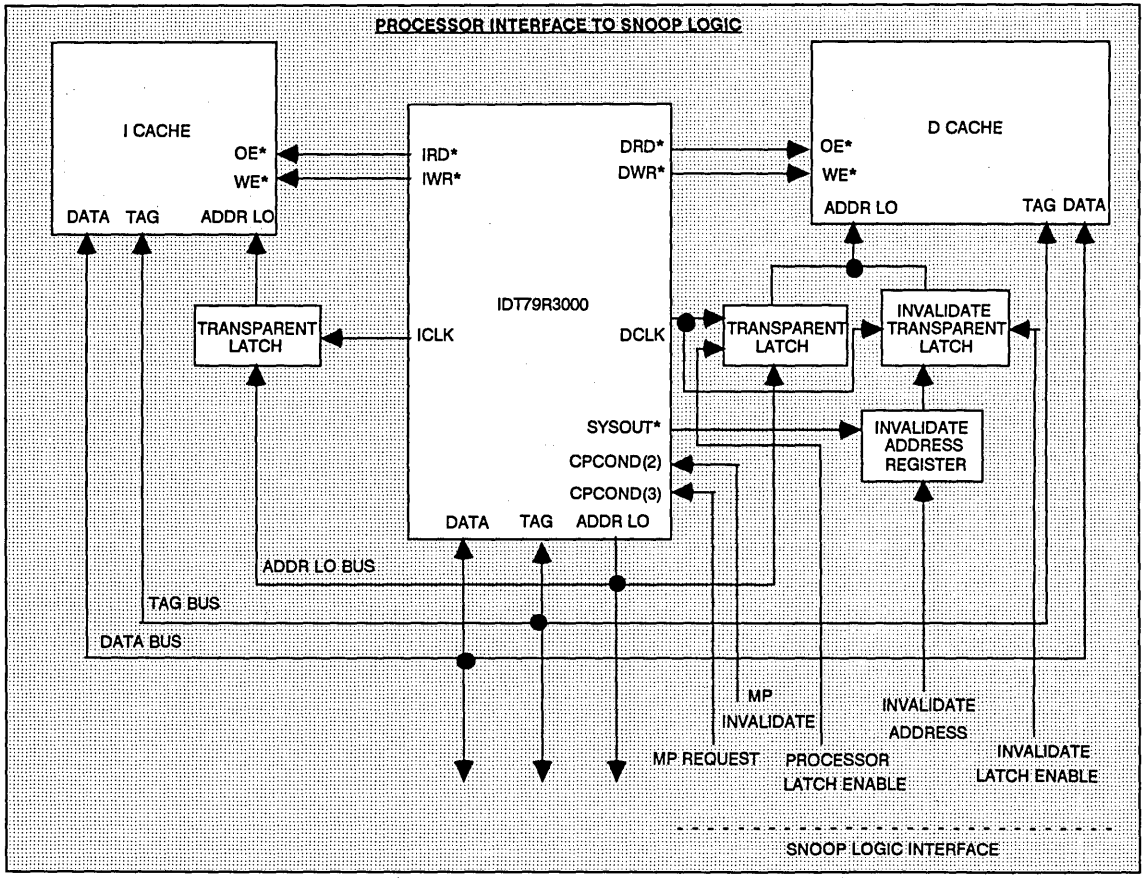

Figure 3. Processor Interface to the Snoop Control Logic

CACHE COHERENCE PROTOCOL

Each snoop cache maintains a directory of the current entries in the local data cache, (i. e. it contains the tags of all the current entries in the local data cache). Its primary function is to monitor the external memory bus for an address match. In addition, the snoop cache maintains state information for each data cache line. A cache (tag) line can be in one of three states: private, shared or invalid. Data that is exclusive to the processor is marked private, data that is common to the processors is marked shared and data that is inconsistent is marked invalid. The snoop cache is updated concurrently with the data cache. Whenever processor 1 modifies or writes a line that is marked shared in its local cache, its snoop control logic signals processor 2 that a write to a shared line has occurred. The snoop control logic of processor 2 then interrogates its snoop cache to determine whether a copy of the modified data is present in the local data cache. If a copy is present, it is invalidated using the *MP request* and *MP invalidate* signals as shown in the Figure 2 and the tag line in the snoop cache of processor 2 is marked invalid. The snoop control logic of processor 2 sends an acknowledge signal to processor 1 which then proceeds to complete its write operation to the shared location, i.e. writes into the data cache as well as into the write buffer. It must be noted that the data value in the write buffer must be retired to the main memory before the write operation can be completed. This prevents possible data inconsistencies that may arise by processor 2 trying to read that particular main memory location before it is updated. This cache coherence protocol is also known as *cross-interrogation*. Note that this protocol is applicable only to cache lines that are marked shared, while writes to cache lines marked private are performed at the processor speed. In the event of simultaneous writes to the same shared cache line by both the processors, only one of the processors will successfully acquire the external bus (determined by the bus arbitration logic) to issue a cross-interrogation signal to the other processor. The write operation of the processor that did not acquire the external bus will result in a write miss. Figure 3 shows a typical processor interface to the snoop cache and control logic in more detail, and is also described below.

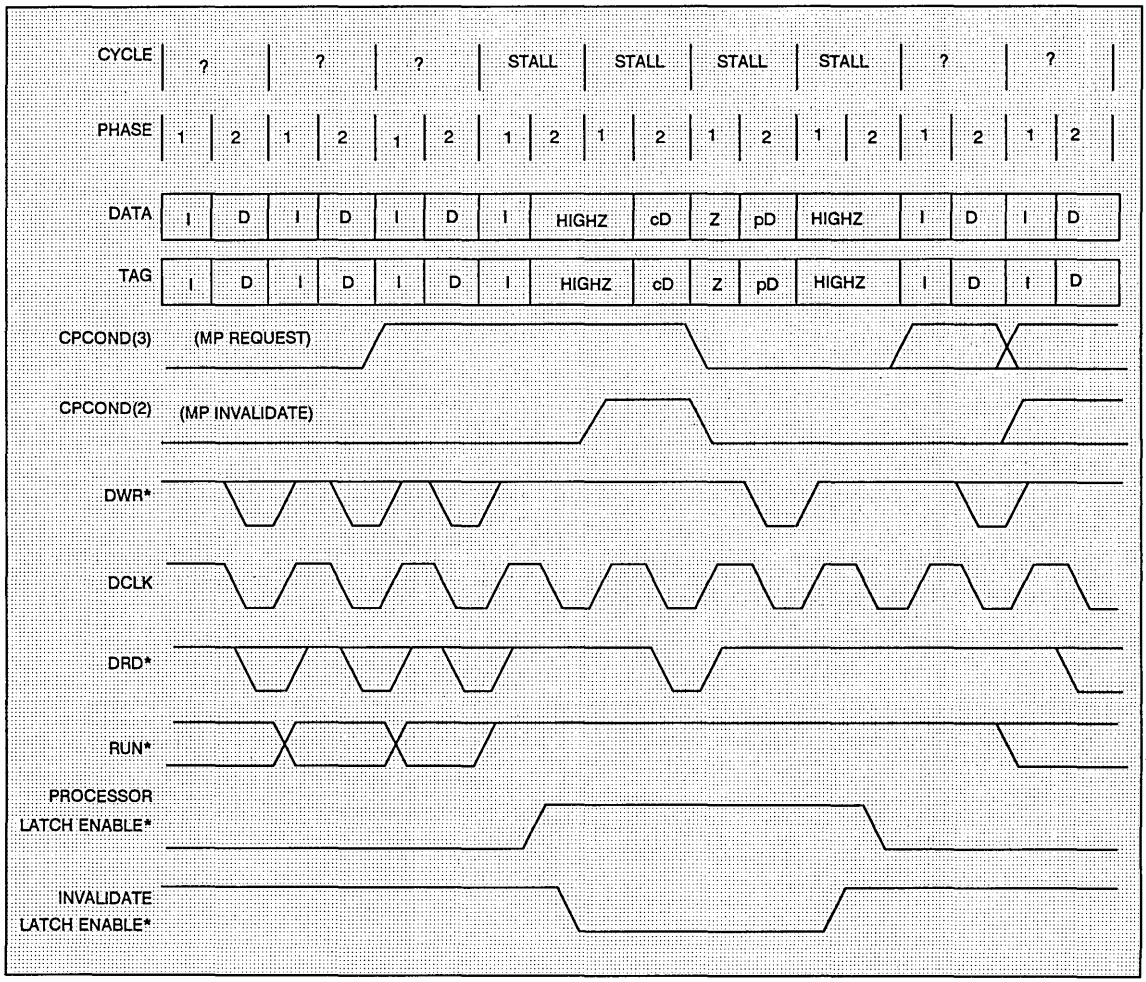

Figure 4. Cache Invalidation Timing Diagram

DYNAMIC CACHE COHERENCY CHECK MECHANISM

The signals at the snoop logic - processor interface include the *MP request*, *MP invalidate*, *processor latch enable*, *invalidate latch enable* and the *invalidate address* (address of the cache location to be invalidated). The snoop logic receives a cross-interrogation signal from the other processor when a write is performed to a shared cache line. It then searches its tags for an address match. If a match occurs, the address is captured in the invalidate address register which is clocked by *SysOut**, as shown in the Figure 3. The *CpCond(3)* input (*MP request* signal) of the IDT79R3000 is then asserted, causing the 79R3000 to enter into a MP stall. As there is no cache activity on the first cycle of an MP stall, the *processor latch enable* signal is deasserted and the *invalidate latch enable* is asserted in order to present the invalidate address to the data cache. After the first stall cycle, the CPU will issue DRd* pulses during every phase 2 and DClk (connected to the transparent latches) during every phase 1, this lasts until the end of the stall or until one cycle after the assertion of CpCond(2). This permits the snoop logic to read the data cache (Data and Tag values can be sampled by the falling edge of SysOut*) in order to determine whether an invalidation is to be performed. If the cache location is to be invalidated, the *MP invalidate* signal (connected to the CpCond(2) input of the 79R3000) is asserted. Invalidation occurs by the assertion of Dwr* during phase 2 of the stall cycle with an arbitrary invalid tag and arbitrary data value driven onto the Tag and Data buses. If CpCond(2) is deasserted while CpCond(3) is still asserted, the processor will return to issuing DRd* pulses to enable data cache reads. The cycle after CpCond(3) is deasserted contains no cache activity. This cycle is used to re-enable the processor's transparent latch and disable the invalidate transparent latch. A detailed timing diagram of a snapshot of the

cache invalidation process is shown in Figure 4. This is a modified version of the timing diagram shown in [11]. Note that Figure 4 shows the minimal timing required. CpCond(2) is asserted two cycles after CpCond(3) is asserted and before the first Drd*. This implies that the data location is invalidated irrespective of the value being read. The symbol "cD" denotes that the cache drives the data and tag buses when CpCond(3) is asserted. The symbol "pD" denotes that the processor drives the data and tag buses when CpCond(2) is asserted. The snoop control logic, at this stage, must mark the tag line in its snoop cache as invalid and send an acknowledge signal to the other processor. This indicates that the cache invalidation is complete. If desired, more sophisticated and efficient invalidation schemes, such as techniques for block invalidation, could be implemented.

SECONDARY CACHE SCHEME

The cache-main memory interface described above could be made more efficient by using a system of multi-level caches [9], [12], to provide additional memory bandwidth. For instance, a secondary cache that is four times the size of the first level or primary cache could be implemented. The secondary cache is a superset of the primary cache and also includes state information to maintain cache coherency. The cache update policy is typically write-through, from the primary to the secondary cache and write-back from the secondary cache to main memory. Since the primary cache is always a subset of the secondary cache, consistent data is guaranteed. This type of multi-level cache organization is implemented in the 4D-MP Graphics Superworkstation [3] made by Silicon Graphics.

CONCLUSION

Maintaining cache coherency is vital in shared memory multiprocessors. The implementation of the cache- main memory interface and the cache coherency protocol are critical issues. The IDT79R3000 RISC processor provides features that facilitate the implementation of cache coherence check mechanisms with minimum hardware and is well suited to be used in a shared memory multiprocessor environment.

REFERENCES

[1] K. Hwang & F. A. Briggs, *Computer Architecture and Parallel Processing*, McGraw-Hill, 1984, pp 459 - 525.

[2] T. Diede et al, "The Titan Graphics Supercomputer Architecture", *IEEE Computer*, Sept. 1988, pp 13 - 30.

[3] F. Baskett, T. Jermoluk & D. Solomon, "The 4D-MP Graphics Superworkstation: Computing + Graphics = 40 MIPS + 40 MFLOPS and 100,000 Lighted Polygons per second", Digest of Papers, COMPCON, Spring
1988, 33'rd IEEE Computer Society Int. Conference, pp 468 - 471.

[4] J. Archibald & J. Baer, "Cache Coherence Protocols: Evaluation Using a Multiprocessor Simulation Model", *ACM Transactions on Computer Systems*, Vol. 4, No. 4, Nov. 1986, pp 273 - 298.

[5] A. J. Smith, " CPU Cache Consistency with Software Support and Using "One Time Identifiers" ", Technical Report 86/290, EECS Department, University of California, Berkeley, California 94720.

[6] M. Papamarcos & J. Patel, "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories", Proc. 11'th Annual Int. Symp. on Comp. Arch., June 1984, pp 348 - 354.

[7] L. Rudolph & Z. Segall, "Dynamic Decentralized Cache Schemes for MIMD Parallel Architectures", Proc. 11'th Annual Int. Symp. on Comp. Arch., June 1984, pp 340 - 347.

[8] P. Sweazey & A. J. Smith, "A Class of Compatible Cache Consistency Protocols and their Support by the IEEE Futurebus", Proc. 13'th Annual Int. Symp. on Comp. Arch., June 1986, pp 414 - 423.

[9] A. J. Smith, "Design of CPU Cache Memories", Proceedings, IEEE TENCON, Korea, Aug. 1987, pp 1 -10.

[10] A. J. Smith, "Cache Memories", ACM Computing Surveys, Vol. 14, No. 3, Sept 1982, pp 474 - 530.

[11] Multi-processor Interface, MIPS R3000 Processor Interface, MIPS Computer Systems, May 23 1988, pp 59-61.

[12] S. Przybylski, M. Horowitz & J. Hennessey, "Performance Tradeoffs in Cache Design", Proc., 15th Annual Int. Symp. on Comp. Arch., June 1988, pp 1 - 18.

Integrated Device Technology, Inc.

THE COMPLETE HIGH PERFORMANCE CACHE SYSTEM FOR THE 80386 MICROPROCESSOR

APPLICATION NOTE AN-30

By Mammad A. Safai

INTRODUCTION

The design of microprocessor systems, today, requires an extensive knowledge of the principles of cache controller and cache memory design—for it is the cache that enables the microprocessor to achieve its maximum throughput. For example, the Intel 25MHz 80386 (using main memory DRAMs with a cycle time of 250ns), without a cache, is rated at 2 MIPs (peak). However, with a well designed cache, the system performance can reach 12.5 MIPs (peak). Similarly, for the Motorola 68030, the performance can be increased from 2 MIPs to 10 MIPs (again with 250ns DRAMs as the main memory element).

Besides increasing the throughput of a microprocessor system, the inclusion of a cache decreases the system bus traffic, making it an ideal element for use in the design of multiprocessing and multi-master based systems. A well designed cache for coherent multiprocessing and multi-master systems.

Central to a cache design, is the coherency architecture employed. This application note discusses the design of a unique cache controller which uses two cache tags to achieve coherency. This dual cache tag design for the 80386 microprocessor offers greater speed than the more common time multiplexed cache tag design in addition to simplifying the system bus interface and timing requirements.

CACHE DEFINITION AND OPERATION

A cache may be defined as a high speed memory element that serves as a high speed memory buffer between slower main memory and the microprocessor. The design of the cache is such that it has an effective cycle time that is less than the cycle time of main memory. This, of course, is because the design of the cache dictates that the data or code needed most often is usually in the cache memory.

The cache memory can not be too large in size because of cost and board space considerations. The main memory will therefore be divided into pages equal in size to the cache memory size. The size of a page will depend on the total size of the cache and the degree of associativity of the cache implementation.

The general operation of a cache based system can be understood by examining its interaction with the microprocessor and main memory during program execution. When a microprocessor issues a read instruction, the microprocessor's address's page field is compared against the page address stored in the cache tag. If the cache tag page address matches the microprocessor address's page field, a hit occurs, and the microprocessor reads the associated data from the data cache SRAM. On the other hand, if the microprocessor page address is not in the cache tag a cache miss occurs. In the latter case, the microprocessor will retrieve the data from main memory and update the cache memory and cache tag with the required main memory address and data i.e. a cache read miss cycle.

CACHE ARCHITECTURE OVERVIEW

A cache system consists of a cache memory which may be divided into two parts; the dictionary or cache tag (a cache tag SRAM) and the cache memory (a data SRAM). The cache tag stores the main memory page addresses of the data that is stored in the cache memory. Besides the cache tag and cache memory, a complete cache system for a microprocessor incorporates; a cache controller to instigate and respond to local and system bus states; system and local bus control logic to interface to external system bus masters and the local microprocessor; coherency logic to assure system coherency in multi-master based systems. Faster caches include a write buffer to allow for zero wait state posted writes.

CACHE TIMING PARAMETERS

When designing a cache system using cache tag and data cache SRAMs, you have to consider the cycle time of the microprocessor used, the match time of the cache tag and the access time of the data cache SRAM. For the Intel 80386 (25MHz version), the cycle time is **40ns**. This allows nearly **80ns** for the cache tag address to be compared against the microprocessor address and the data cache SRAM to be accessed (a minimum of two cycles are required for the read instruction). IDT's cache tag SRAMs and data cache SRAMs can be used to meet the timing requirements of most microprocessors. The IDT7174 8K x 8 cache Tag SRAM features a match time of **20ns** (maximum) while IDT's 7164 8K x 8 has a cycle time of **20ns** (maximum). When both the cache memory and cache tag are accessed simultaneously, valid data can be placed onto the microprocessor address bus in nearly **20ns** (address to match time of the cache tag (20ns) is equal to the access time of the cache memory (20ns) in the above). Here, the controller will start the cycle as if the data is in the cache memory, if later during the cycle it was determined that the data is missing from the cache, the controller will float the I/Os of the cache memory and accesses the main memory.

EFFECTIVE CYCLE TIME

The effective cycle time of a microprocessor based system is the average amount of time that is required to access memory. For a system without a cache, the effective cycle time is equal to the cycle time of main memory (today's 1Mbit DRAMs feature cycle times between 100 and 400ns). However, for a microprocessor system based on a cache, the effective cycle time is a function of the cycle time of main memory, the cycle time of the cache and the hit ratio of the cache, i.e. :

$$t_{eff} = ht_{cache} + (1-h)\, t_{main}$$

where

t_{eff}	=	Effective Cycle Time
h	=	Hit Ratio
1-h	=	Miss Ratio
t_{main}	=	Main Memory Cycle Time
t_{cache}	=	Cache Cycle Time

A normalized graph showing the effective cycle time for a varying hit rate with a constant main memory cycle time of 200ns on a cache that allows zero wait states operation, is given in Figure 1. From the graph, it can be seen how dramatically the hit rate affects the effective cycle time of the system e.g. for a decrease in the hit rate from 99% to 89%, the effective cycle time of the cache will almost double.

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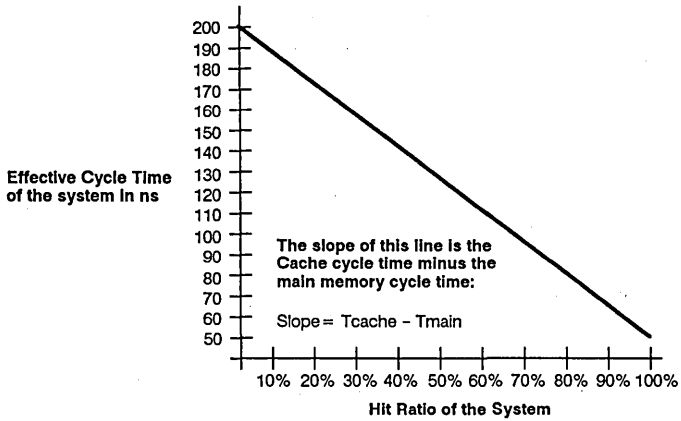


Figure 1. Effective Cycle Time vs. Hit Rate

CACHE ASSOCIATIVITY

Associativity, the number of unique cache memory banks of a cache design, is fundamental to the design of a cache system. The associativity determines the cache architecture, affects, to a degree, the overall performance of the system, plays a role in the selection of the replacement algorithm (pertains to the method used to update the cache memory), and indirectly sets the page size.

Associativity and Cache Architecture

After the designer decides on a cache memory size, he or she must then decide on the associativity so as to obtain the optimized cost/performance ratio. The architecture of the cache memory is dictated by its associativity. For example, if the designer selected a cache memory size of 32Kbytes, the direct mapped cache memory will be one 8K bank of 32 bit words. A 32Kbytes two-way set cache will have two 4K banks of 32 bit words. Finally a 32Kbytes four way set design will have four 2K banks of 32 bit words.

Associativity and Page Size

Because of the different architectures for caches of different associativity, the page size for a given sized cache will vary with the degree of associativity. For the direct mapped 32Kbytes cache, given above, the page size will be 8K doublewords. Similarly, the two-way set associative design will have a page size of 4K doublewords and the four-way set associative will have a page size of 2K doublewords. Since the size of the page is smaller for caches of higher degrees of associativity, the number of main memory pages will also vary with associativity (See Figure 3).

Associativity and Mapping Cache To Main Memory

The 80386's 32-bit address field to be viewed as two fields, a page field (given by the tag) and a line offset field (See Figure 5). Since the page size of main memory is dictated by the size of the cache a direct mapped cache with a cache memory size of 32Kbytes will have a main memory page size of 32Kbytes (or 8K 32-Bit words). Since the page size of main memory is the same size as the cache memory, every address in cache memory directly maps to the associated line in a page of memory i.e. line 5 of the cache maps to line 5 of the main memory page (Figure 2). In this example we will use a line length of 8 bytes. The address 17635 matches the tag 1763X, X refers to an octal digit from 0 to 7. The data associated with the tag 1763X have addresses from 17630 to 17637. Therefore the address 17635 refers to the sixth element in that line. The corresponding data is 72.

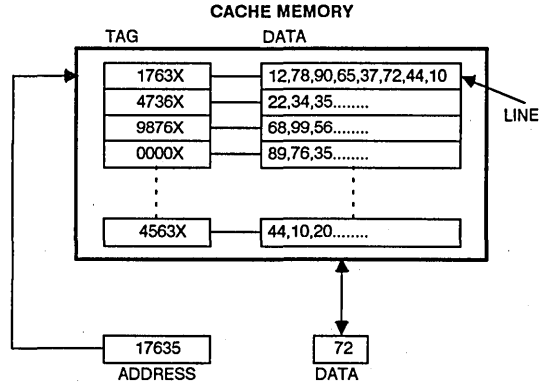
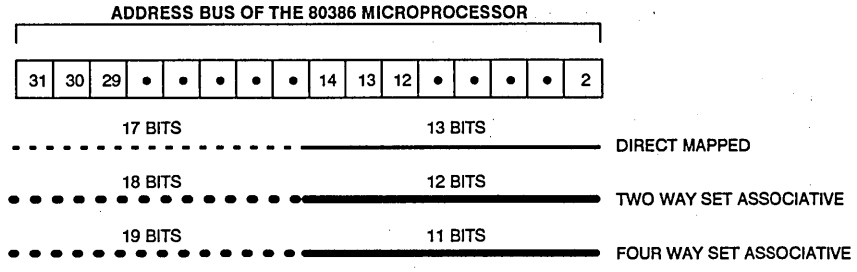


Figure 2. Mapping to Main Memory

Since the page size is affected by the associativity of the cache, the addressing scheme for fixed sizeJcaches of different associativity will also be affected. As shown in Figure 3, the page field for a direct mapped cache is 17 bits while the line offset field is 13 bits. This contrasts to a four way set which has a page field of 19 bits and a line offset field of 11 bits.

The addressing scheme for a cache based on the Intel 80386 is also determined by the size of the cache. If the cache size is 32Kbytes (8K x 32) the 13 LSBs of the 80386 microprocessor address bus will be needed to address each four byte line in the cache. This leaves 17 bits to define the number of pages in main memory i.e. 217 = 128K pages. In summary, an 8K doubleword cache divides main memory into 128K pages of 8K doublewords each.



Solid Lines : Address bits that are used to Address the Tag Memory

Dashed Lines: Address bits that are stored in the Tag Memory

	Direct Mapped	Two way set	Four way set
To address the Tag memory	A(2:14) -> 13 bits	A(2:13) -> 12 bits	A(2:12) -> 11 bits
To store in the Tag memory	A(15:31) -> 17 bits	A(14:31) -> 18 bits	A(13:31) -> 19 bits
Page Size	8K	4K	2K
Number of pages	128K	256K	512K
Number of cache memory banks	1 Bank	2 Banks	4 Banks
Absolute size of the cache memory	1 x 8K	2 x 4K	4 x 2K

Figure 3. Associativity, Architecture, Addressing, and Page Size for a fixed size cache. In the implementation that follows the cache size is 32 KBytes. Figure 3 shows how the address bus of the 80386 should be divided for different associativity of the same size cache (32 KBytes).

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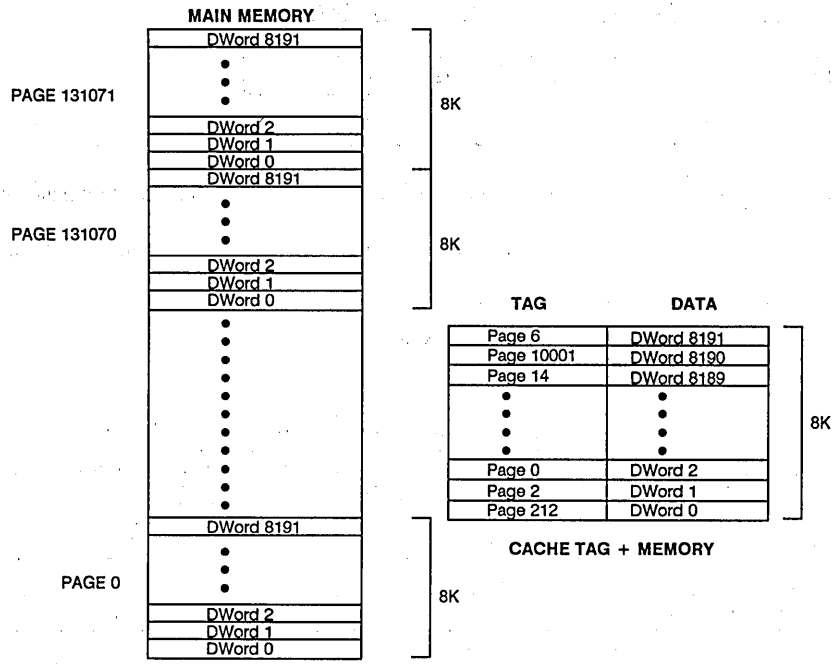
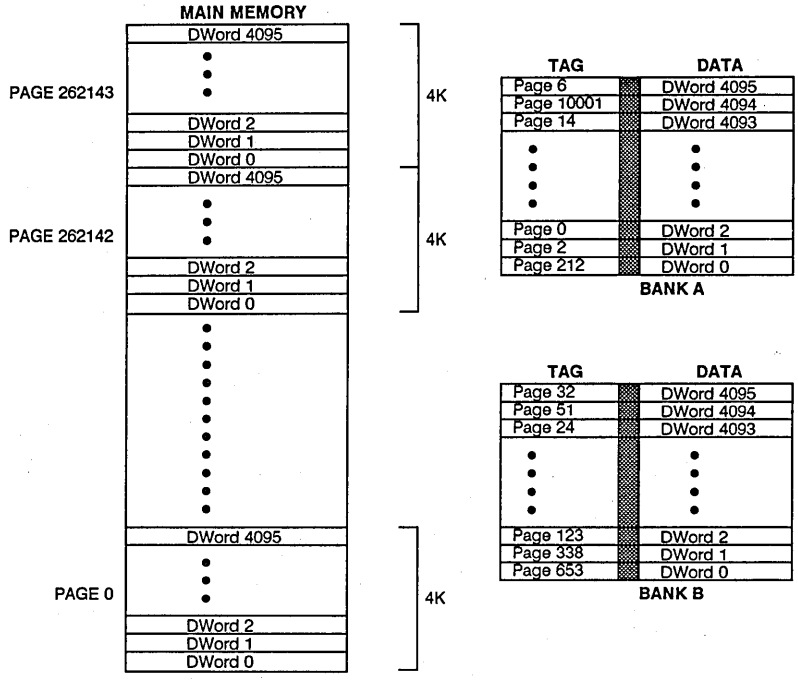


TOTAL MEMORY = Number of Pages x Page Size x DWord

= 128K x 8K x 4Bytes

= 4 GigaBytes

Figure 4A. Direct Memory Mapped representation of a 32 KBytes Cache



TOTAL MEMORY = Number of Pages x Page Size x DWord
= 256K x 4K x 4Bytes
= 4 GigaBytes

Figure 4B. Two-Way Set Associative Memory Map for a cache with a total size of 32 KBytes

The operation of comparison for the cache tag, for the latter example, uses the 13 LSBs of the microprocessor address bus to address the cache tag and compares this accessed address to the 17 MSBs of the microprocessor address bus (Figure 5). Additionally, the valid bit(s) is(are) also examined. If a match occurs the cache memory is enabled and the microprocessor reads the data from cache memory.

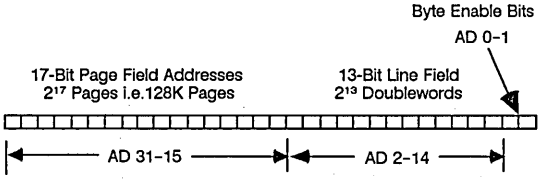


Figure 5. Local Address Bus For 80386 Direct Mapped Design

Performance as a Function of Associativity

The differences in the architectural structure of caches of different associativity results in different performance levels for equivalent program. If one examines the direct mapped architecture, one will notice that it will not permit more than one page/line offset conflict in its cache i.e. page 1/line 2 and page 2/line 2 can not coexist in cache memory. For a two-way set, one will notice that the design will not permit more than two page/offset line conflicts i.e. page 1/line 2 and page 2/line 2 can exist in the cache concurrently, but page 1/line 2, page 2/line 2 and page 3/line 2 can not. Similarly, a four way set will not permit more than 4 page/line offset conflicts.

Thrashing

Because of the existence of page/line offset conflicts, certain programs may result in a situation coined as thrashing—which results in a significant increase in the miss rate. As an example of a program which results in thrashing, consider a direct mapped cache design where the microprocessor must process two lines of code in a repetitive loop e.g. the microprocessor must first read the code on page 2/line 1, then read the code on page 3/line 1 and then go back and read the code on page 2/line 1. For a direct mapped design, such a code structure (or trace) will result in consecutive misses.

Although thrashing occurs most often in direct mapped systems, it can also occur in two-way set or four way set designs. This, of course, is due to the fact that the number of page/line offset conflicts supported by these designs is also limited.

In this example a smaller line size in a direct mapped cache reduces thrashing more than the more common approach of a bigger line size in a two way set associative cache.

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REPLACEMENT ALGORITHMS

Replacement algorithms for caches pertain to the method used to update the cache memory. The replacement algorithm is important in that it will affect the hit rate of the system which in turn alters the effective cycle time of the system (and hence the MIPs rating) Replacement algorithms, are designed such that the cache is updated with data or code that will be most frequently used by the microprocessor. Conversely, replacement algorithms are also designed to delete data or code that is least frequently used.

There are several types of replacement algorithms used for caches. Three of these are the least recently used (LRU) algorithm, the First In First Out (FIFO) algorithm and the random replacement algorithm. The least recently used algorithm, on a cache read miss, replaces the data/code in the cache that in relation to the other code/data was not used last. The random replacement algorithm replaces data/code in the cache by random selection. Finally, the FIFO algorithm replaces data that entered the cache first i.e. the oldest data in the cache.

The associativity of the cache, i.e. direct mapped, two-way set, or four way set, often dictates the replacement algorithm chosen. For direct mapped caches, for example, there is no need to consider a replacement algorithm. This is because the direct mapped hardware design requires that the cache be updated, on a miss, with the corresponding page/line address from main memory.

For the two-way set cache, because of its design, one has the option, on a cache miss, to update either of two cache addresses (in one of the two ways). The LRU algorithm is often used here because it only requires one memory bit in the cache tag to determine which way of the cache was accessed last. On a cache miss, the LRU bit is checked, and, for example, if it is set, the data in way 1 is replaced. On the other hand, if it is reset, the data in way 2 is updated.

For caches with associativity greater than or equal to 4, a random replacement algorithm is often used. This is because it offers a hit rate comparable to that of other algorithms and requires a pseudorandom number generator to implement.

LINE SIZE SELECTION

Line size is a term used in cache design that refers to the unit of transfer (in Bytes) between the cache and main memory. For the majority of 32-bit systems, the line size is often chosen to be 4 bytes A line size of 4 bytes simplifies controller logic and problems associated with byte boundaries. The line size, however, has an affect on the overall performance of a system. As one increases the line size, the effective hit rate of the system goes up (for a fixed size cache) which increases the overall MIPs performance of the system. On the other hand, a larger line size will result in an increase in the amount of system bus traffic. Which is, of course, due to the greater number of bytes transferred on a cache miss.

Depending on the type of system design, the size of the line chosen will affect the overall system performance. For multiprocessing systems, where it is desirable to keep system bus traffic to a minimum, a small line size is often opted for.

Table 1 illustrates the affect of line size for different size caches on the overall system throughput, where "a" is the marginal transfer time per byte and "b" is the overhead per miss.

Cache Size (bytes)	a = 15 ns/byte b = 360ns	a = 15 ns/byte b = 160ns	b = 600ns
32	4 - 16	4 - 8	8 - 16
64	8 - 16	4 - 16	8 - 32
128	8 - 16	4 - 16	8 - 32
256	8 - 32	8 - 16	16 - 32
512	8 - 32	8 - 16	16 - 64
1024	8 - 32	8 - 16	16 - 64
2048	16 - 32	8 - 32	16 - 128
4096	16 - 64	8 - 32	32 - 128
8192	16 - 64	8 - 64	> = 64
16384	16 - 128	8 - 128	> = 64
32768	16 - 128	8 - 128	> = 64

Table 1. Optimized Line Size vs. Cache Size and Delays. This table was taken from A. Smith's paper on cache memories.

COHERENCY– DEFINITION AND COMPONENTS OF

Coherency is defined as the capability of cache memory to replicate in real time the current contents of main memory. Cache coherency is necessary in all cache based microprocessor designs where an external device can control the bus and write to main memory. If a system has a DMA device, more than one microprocessor, or memory mapped I/O devices, coherency logic must be considered.

WRITE COHERENCY HARDWARE

Write operations require special considerations in cache design. For a microprocessor write operation to main memory, in order to maintain local cache and main memory coherency, the local cache memory must be updated along with main memory.

In order to ensure write coherency, there are a number of hardware techniques. The three most popular design techniques are the copy-back, write-through, and buffered write through schemes. Each of these techniques offers different advantages. The copy-back and buffered write through schemes feature increased system throughput. On the other hand, the write-through scheme offers minimized support logic.

For a write-through based cache design, every time the microprocessor write occurs the code/data is written simultaneously to the cache and main memory. Because of the fact that main memory is slower than cache memory, the time to implement a write is governed by the cycle time of main memory. This, of course, puts a limitation on the effective cycle time of a cache system based on a write through scheme.

A hardware modification to the write-through design that allows for a reduction in the effective cycle time is a high speed buffer. This design, often referred to as a buffered write-through or posted write, improves the performance by allowing the microprocessor to operate out of the cache, at cache speeds, after a microprocessor write operation. This is in direct contrast to the write-through which requires that the microprocessor wait for the completion of the main memory write cycle. In a buffered write-through cache system, when a write occurs, the cache and buffer are updated with the write data, allowing the microprocessor to read from the cache again. During this time, the buffered write-through logic takes control of the system bus and updates main memory by

downloading the file buffer. Adding a buffer, of course, increases the number of components for the cache module.

A copy back system operates on the use of a dirty bit that is stored along with the cache tag address. For a copy-back scheme, when a cache write hit occurs, the associated dirty bit is set which indicates that the data in the cache is no longer coherent with main memory. When another bus master requests control of the bus, before releasing the bus, the cache controller will update all the locations in the main memory that are not coherent with the content of the cache memory as a result of cache write hits. A cache write miss will occur when the microprocessor attempts to write to a location that was not cached earlier.

The disadvantage of a copy-back system becomes apparent in the design of multiprocessor and multi-master based systems. In these systems, any external read from main memory requires that all caches in the system be checked to see if the dirty bit has been set for each address written. If the dirty bit has been set, the associated data entry in the cache must be downloaded to main memory before an external device accesses that address.

Although, the buffered write through has a somewhat lower performance than a copy-back (because of main memory traffic during write misses), write-through and buffered write through are often preferred to use in multiprocessing systems. This is because, as mentioned above, there are a number of coherency issues that must be dealt with for a copy-back scheme.

COHERENCY LOGIC— FOR DMA AND MULTIPROCESSOR SYSTEMS

In order to maintain coherency for multiprocessing and DMA applications, a cache design needs to be able to monitor the system bus for external device writes to main memory. If a write to main memory occurs from an external device, it is necessary to inform the cache memory of the address written to so that the cache controller can decide whether or not to invalidate the cache memory contents (either by flushing the entire cache or by clearing the associated valid bit of the entry).

Architectures for Cache Coherency

There are two common architectures used to achieve coherency in microprocessor based systems; a time-multiplexed cache tag architecture and a dual cache tag architecture. For the multiplexed cache tag architecture, the cache is time multiplexed between the system address bus and the local address bus. This permits the controller to check if the system address location written to is in the cache memory. For the dual cache tag system, one cache tag is used to monitor the local address bus and another cache tag (the SNOOP tag) is dedicated solely to monitoring the system address bus.

Dual Cache Tag vs. Time-Multiplexed Cache Tag Architecture

The advantages of a dual cache tag system over a time-multiplexed cache system are seen when one examines the timing requirements of the two, i.e. the dual cache tag design can work with a much shorter microprocessor cycle time. The time-multiplexed scheme uses the same physical tag memory to tag the addresses present in the cache memory (tag) and checks the main memory's address bus activity (SNOOP). When the processor requests data of any address, the page field of its address bus is compared against the one stored in the tag memory, if they match a hit occurs else a miss is issued. The remaining part of the cycle, the tag memory acts as a SNOOP memory i.e. it monitors the main memory's address bus activity for any write to an address with a matching page field. In the latter case a SNOOP hit is issued and the controller could either invalidate that particular entry or flush the content of the entire cache.

As can be seen from the above, the time-multiplexed scheme requires two sequential cache tag comparisons, i.e. the CPU address bus is compared against the contents of the cache tag and then the system bus is compared against the contents of the cache tag. This, of course, results in a delay time equal to the time it takes to perform two accesses to cache tag memory plus the time it takes to multiplex between the system bus and the CPU bus.

The dual cache tag scheme when compared to the time-multiplexed scheme permits a significant reduction in the microprocessor cycle time. This is because, as opposed to the time-multiplexed scheme, the dual cache tag scheme allows for the system bus address tags (SNOOP tag) and the CPU address bus tag (cache tag) to function at the same time. On the instigation of a system bus transfer, the system address bus page field (or tag) is compared against the page field stored in the SNOOP tag. At the same time, the CPU bus page field is compared against the page field stored in the CPU bus cache tag. If the SNOOP tag page address does not match the system bus page address, the controller continues onto its next cycle. If, on the other hand, the SNOOP tag did match the system address page field, the associated valid bit of both cache tags are cleared or both cache tags will be reset.

This means, of course, that the microprocessor cycle time required for the dual cache scheme (equal to the time it takes to perform one cache tag access and comparison) is less than one-half of that required by the time multiplexed scheme (equal to the time it takes to perform two cache tag accesses and comparisons).

Implementing a Dual Cache Coherency Architecture

For implementing a dual cache coherency system, IDT7174's cache tag SRAMs can be used to form both the microprocessor cache tag block and the system bus cache tag block (SNOOP tag)—as shown in Figure 7. For a dual cache based system, the SNOOP memory is always identical to the microprocessor cache memory. This is accomplished by writing the same information at the same time to both system (SNOOP) and CPU cache tag memories. The operation of the dual cache is such that when another bus master has control of the system bus and writes data to a previously cached address in main memory, a SNOOP hit occurs. A SNOOP hit will result in the controller either invalidating a particular entry in both cache tags or flushing all the entries in both cache tags.

DESIGNING A CACHE TAG UNIT

In order to optimize cache design, the IDT7174 may be used (Figure 6). This Cache Tag SRAM (8K x 8) has built-in features that help and simplify cache tag design. These include a match output, a reset input, CEMOS™ technology, and three state I/O. The match output is high whenever the address stored in the IDT7174, accessed by the address pins, matches the address at the I/O pins. The tag is addressed by pins A0-A12 and the tag is compared to the stored tag on the I/O pins via an internal comparator—if they match, the match output goes high. For cache design applications, the match output drives the cache controller which in case of a match (hit) places the data contents of the cache memory on the microprocessor data bus. The reset input (active low) allows the entire contents of the cache tag memory to be cleared which permits reset on system power up and the cache to be flushed (for coherency applications).

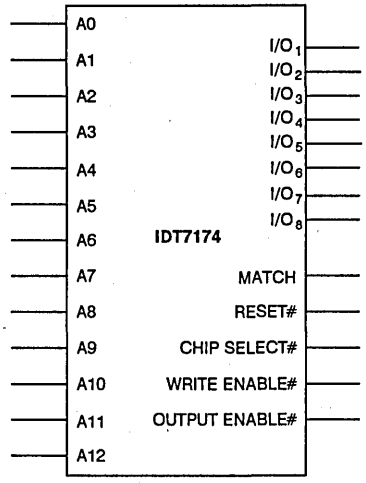

Figure 6. The IDT7174 8K x 8 Cache Tag SRAM

The IDT7174 features an address to match time of 20ns, making it suitable for applications up to 40MHz along with fast SRAMs to build the cache memory for two-cycle machines such as the Intel 80386). It is also cascadable in depth and width which allows caches to be easily designed for a variety of different microprocessor address bus widths.

Figure 7 illustrates a cache tag SRAM comprised of three IDT7174's organized as IDT8192 23-bit words. If used in a microprocessor based system, main memory would be divided into 8 Million pages. The lower address bits specify the line offset in the cache where the lower page address tag is stored. The 23 bit page address (within the cache tag SRAM) accessed by the 13 lower microprocessor address bus bits is compared against the 23-Bit microprocessor page address. If there is a match from all three, the wired AND match output will go high indicating that the needed data is in the cache memory.

I/O 8 of the last IDT7174 is the cache data valid bit. This bit is used to indicate that the data in the cache is valid. On power up or a cache flush the valid bit is very useful.

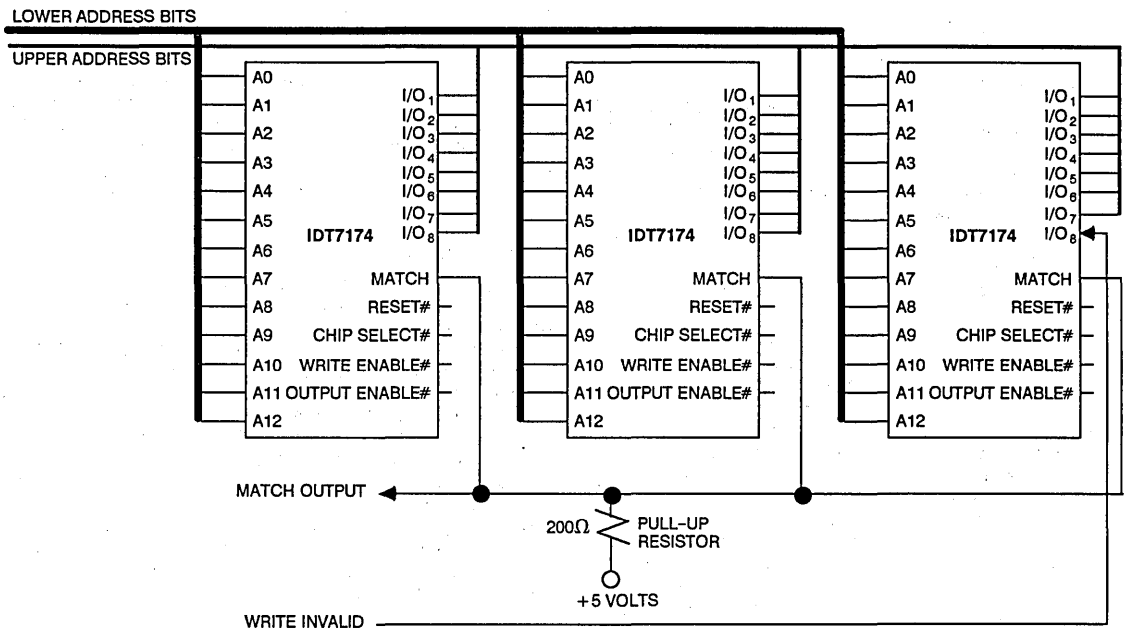

Figure 7. A Cache Tag Unit

A CACHE CONTROLLER AND MEMORY MODULE FOR THE 80386

For the design of a cache controller, one must become familiar with the microprocessor that is being used, its interface and signaling requirements. As well, one must decide on the cache's associativity, depth, configuration and ensure that all critical microprocessor and system timing requirements are met. The design of the cache controller must then be considered to allow for functions such as coherency, bus arbitration, and state machine sequencing (to control the interface to the system bus and the microprocessor).

For the design that follows, an 80386 microprocessor is used (25MHz Version) which incorporates a dual cache tag coherency architecture.

80386 Microprocessor Cache Considerations

In the following processor description and cache system implementation, when a "#" sign follows the name of a signal it indicates that this signal is active low, if there is no "#" sign at the end of a signal name, it means that it is an active high signal.

The 80386 microprocessor from Intel is the current mainstay of both the PC market and low end workstation market. The 80386 is currently used in the leading edge IBM PCs, Compaq's microcomputer and in Sun's new multitasking workstation.

The 80386 (Figure 8) is based on low power CMOS technology and comes in 16MHz, 20MHz, and 25MHz versions.

As illustrated in Figure 8, the 80386 has an effective 32 bit address bus giving an address space of 4 Gigabytes. The address bus consists of address lines A2-A31 and four byte enable lines BE0#-BE3#. The byte enable signals allow the 80386 to address one or an adjacent combination of the 4 bytes contained in the 80386's 32-bit word.

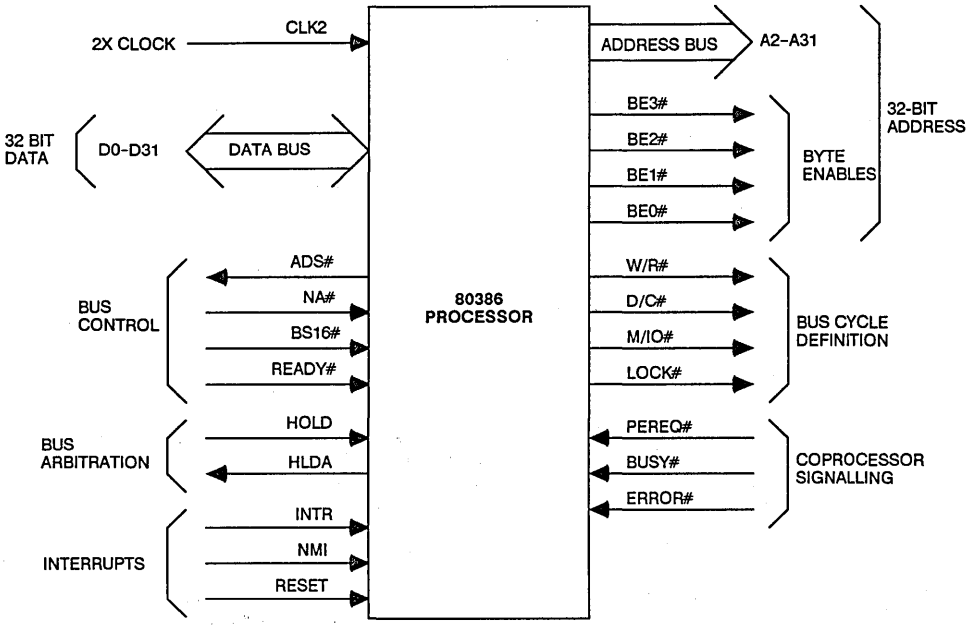

Figure 8. The 80386 Microprocessor

80386 Microprocessor Signals

The 80386 microprocessor signals can be divided into bus cycle definition signals, bus control signals, bus arbitration signals, and interrupt signals. The bus cycle definition signals define attributes and conditions of the current bus cycle in progress, e.g. memory read or I/O write. The bus control signals, on the other hand, control the operation of either the bus or microprocessor, e.g. inform the microprocessor of the completion of a cycle or the transfer of a 16 bit word. Bus arbitration signals are used to arbitrate the control of the bus by competing bus masters, e.g. HOLD and HOLD Acknowledge. Finally, interrupt signals are used to interrupt the current process of the microprocessor so that another process may be executed, e.g. NMI#.

80386 Bus Cycle Definition Signals

Lock# (Lock) indicates that the current microprocessor cycle under execution can not be interrupted i.e. by an interrupt signal.

W/R# (Write or Read) signals whether or not the microprocessor is in a read cycle or write cycle.

M/IO# (Memory or I/O Cycle) indicates whether or not the cycle is a memory access or I/O access.

D/C# (Data or Control Cycle) signals whether or not the current bus cycle is a data or control cycle.

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80386 Bus Control Signals

ADS# (Address Status) is an address status signal which indicates that the address issued by the microprocessor is valid and ready for sampling.

READY# is an input to the microprocessor that indicates the end of the current bus cycle.

NA# (Next Address) is an input to the microprocessor that is used to instigate the high-speed pipeline mode.

BS#16 (Bus Size 16) is an input to the microprocessor that informs the microprocessor that 16-Bit data is to be transferred

Interrupt and Interface Signals

CLK2 is the microprocessor clock input provided by a crystal (twice the microprocessor clock frequency). This signal is divided by two inside the microprocessor.

RESET is an input to the microprocessor that forces the 80386 to a known state.

Bus Arbitration Signals

HOLD is an input signal to the 80386 that requests that the 80386 relinquish control of either the local bus or system bus so that an external master can take control of the bus.

HLDA (Hold Acknowledge) is an output from the microprocessor that signals to an external bus master that it has received and acknowledged a HOLD signal and has released the bus.

Microprocessor Cycles

Figure 9 illustrates the basic timing for a microprocessor cycle. CLK2 serves as the timing reference for the microprocessor bus cycles. This signal is divided by two to form the internal CLK signal (for a 25MHz 80386, CLK2 would be 50MHz and CLK would be 25MHz). The bus cycle of the microprocessor consists of two bus states, T1 and T2, which are further subdivided into two phases each, 01 and 02.

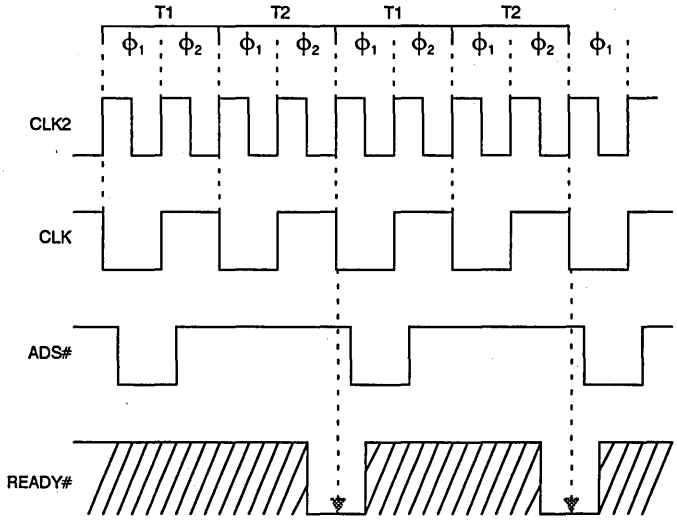

Figure 9. Basic Timing Waveform for 80386 2 State Cycle

The Intel 80386 requires a minimum of two 25MHz cycles to complete any instruction. The start of a microprocessor cycle is characterized by ADS# going low which indicates that there is a valid address on the microprocessor bus. At the end of bus state T2, the microprocessor checks the READY# input to see if the cycle is finished. If READY# is low, it means that the current cycle is completed which allows the microprocessor to start a new bus cycle. On the other hand, if READY# is high at the end of T2, the processor will stay in the T2 bus state until it sees a low level on the READY input. For this condition, all added T2 bus states are called wait states (Figure 10). In cache design, for a miss, the READY input remains high until data is returned from main memory. If there is no pending action required by the microprocessor after T2, the microprocessor will enter in an idle state, Ti (ADS# will remain high—Figure 11).

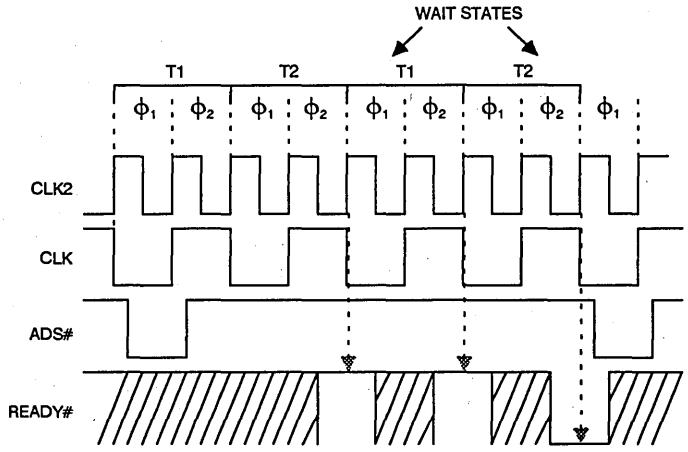

Figure 10. An 80386 Bus Cycle With 2 Wait States

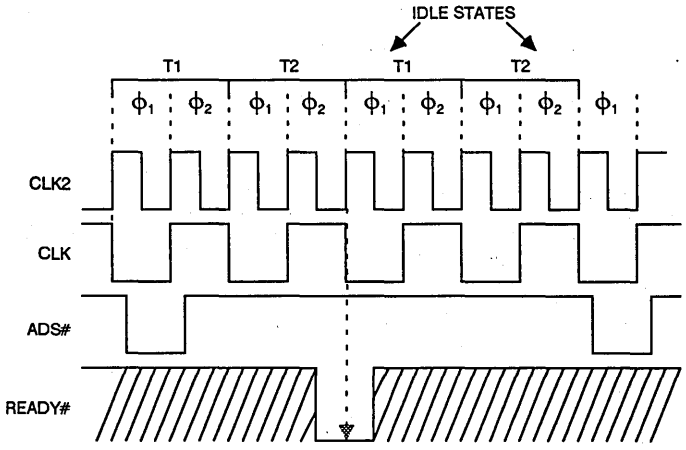

Figure 11. An 80386 Cycle Followed By Two Idle States

When designing a cache system with the 80386 microprocessor, it is important to remember that the only time when the microprocessor probes the READY# input is at the end of T2. The rest of the time, the processor ignores the logic state of the READY# input.

Another bus cycle that is important in the design of a controller for cache memory operation is the hold-hold acknowledge cycle (Figure 12). When another bus master (e.g. DMA Device) wants to take control over the bus, it asserts the HOLD signal that feeds the microprocessor. When the microprocessor sees the HOLD signal go high, it will finish the current bus cycle it is executing, float its data, control and address buses, and then issue a HLDA (hold acknowledge) signal to the external bus master. However, if the LOCK# pin is active on the microprocessor, a HOLD will not be acknowledged by the microprocessor. The lock signal effectively prevents any device from interrupting the microprocessor process in progress.

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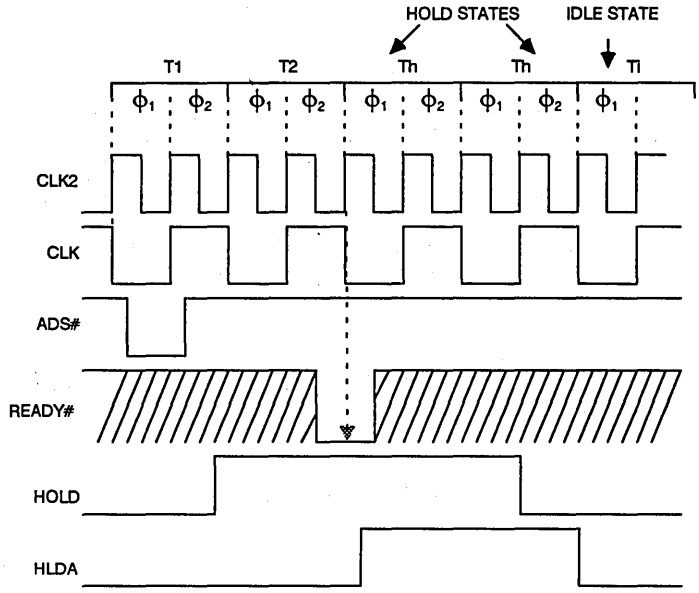

Figure 12. A Two Hold 80386 Cycle Followed By An Idle State

State Diagram

Figure 13 shows the state diagram for the 80386 operating in non-pipelined mode. After the microprocessor is first turned on, a RESET pulse will put the 80386 into a known state. When the 80386 receives a RESET pulse, it will automatically fetch its first instruction from address 0FFFFFFF0H. Usually, at this address, there is an unconditional jump to the location where the bootstrap routine is located(the BIOS).

For pipelined mode the NA# pin must be asserted. For a discussion of pipelined mode for the 80386 refer to the Intel 386 Microprocessor Reference Manual.

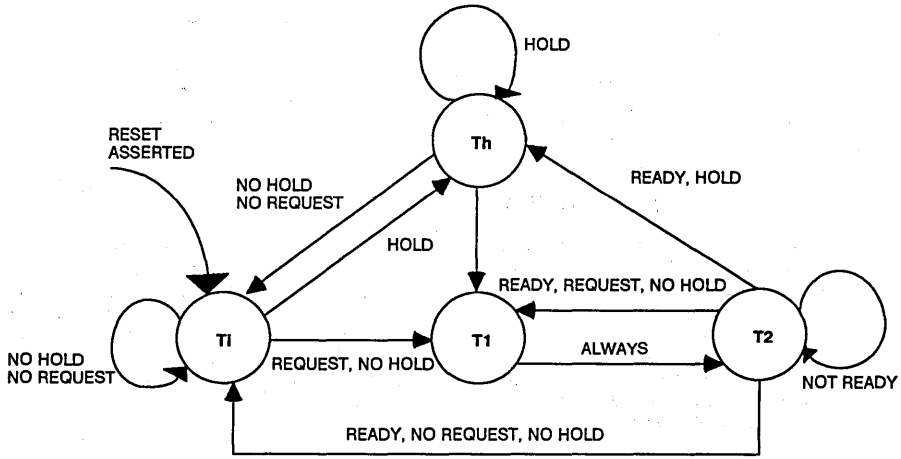

Figure 13. State Diagram For The 80386

CACHE CONTROLLER DESIGN

Cache Associativity, Depth, Page Size, and Line Size Selection

One of the first considerations for the design of a cache controller is the selection of the cache memory. For this design, a direct mapped cache is selected with a cache size of 8K x 32. The 8K data cache divides main memory into 128K pages of 8K doublewords (a doubleword is 32 bits or 4 bytes). The line size selected for this cache design is 4 bytes.

It should be recalled that for a direct mapped cache (Figure 2) every line in the cache will map to a corresponding line in a page (given by the tag) in main memory e.g.. line 0 of the cache will always map to line 0 of a main memory page (given by tag). This, of course, means that it is impossible to have more than one unique line address in a direct mapped cache e.g.. line 0/page 1 and line 0/page 3 can never coexist in the cache.

Cache Controller Hardware Overview

Figure 14 illustrates the block diagram of the dual cache controller to be designed for the 25MHz version of the 80386. The design consists of; two cache tag SRAM blocks, one for the system bus and one for the CPU bus; three PALS used for the design of the cache controller state machine; a data cache SRAM block for the microprocessor; and a number of 74F logic blocks that serve as data/address/control logic and system bus drivers.

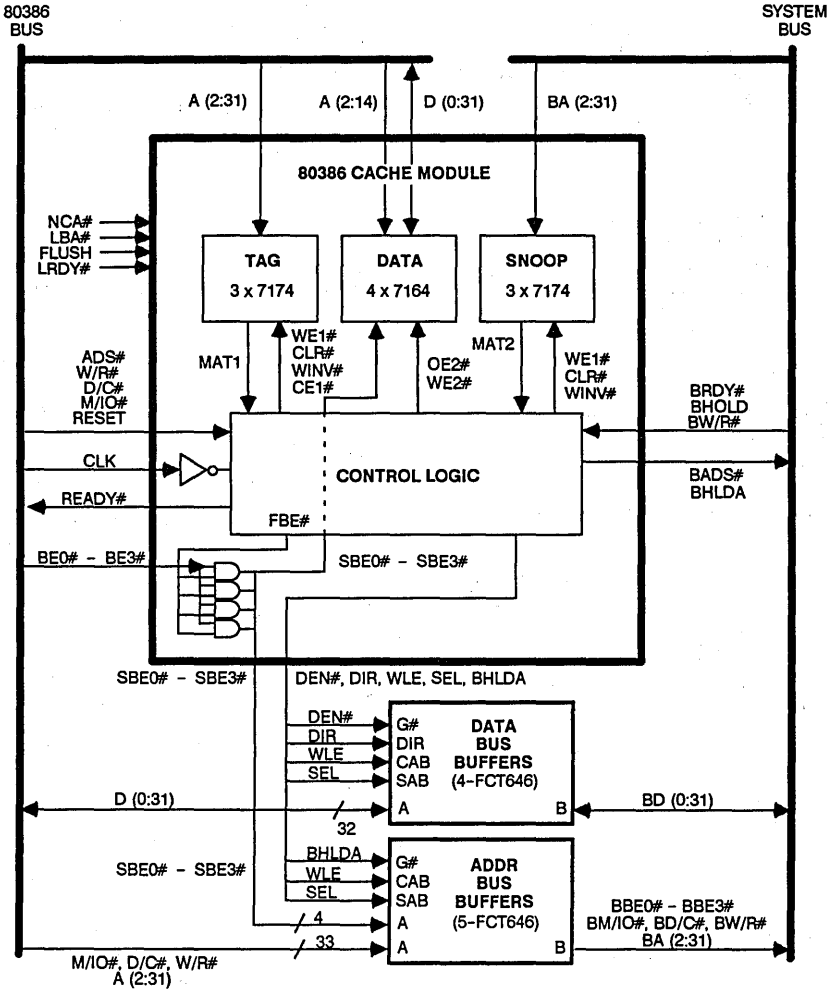

Figure 14. Block Diagram of the Complete Cache System

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For the CPU cache tag, a 8K x 24 cache tag is used (Figure 28 and 30) which is constructed from three IDT7174 cache tag SRAMs. The system bus cache tag (SNOOP tag) is constructed exactly the same i.e. with three IDT7174's.

For proper termination of a bus cycle, a 74F64 And Or Invert gate is used (Figure 31) to drive the READY input of the 80386. The 74F64 is used in order to meet the critical timing requirements of the READY signal.

The buffer network is built from nine IDT74FCT646's to form the address, data and control bus buffers. The IDT74FCT646 is a Fast CMOS Octal Transceiver Register with an 8-Bit A register and an 8-bit B Register. The 646 block allows for the bidirectional transfer and temporary storage of 32 bits of data. The DIR (direction) pin is used to control the direction of data flow between the processor's data bus and the system's data bus (Figure 14).

The system bus tag (SNOOP tag) monitors the addresses on the system's address bus when an externally controlled data transfer takes place (e.g. DMA). If the SNOOP tag detects an address that is contained in the CPU cache tag (when BHLDA is active and when a write occurs), the entire content of both cache tags is flushed via the reset input of the IDT7174.

SIGNAL DESCRIPTION

- **BA (2) - BA (31)** are the 30 address pins that connect the system address bus to the cache module. These 30 pins form the BA bus or the board address bus.
- **BHOLD** is an input to the cache module. BHOLD (bus hold) is asserted by system when another bus master wants to take control of the bus. BHOLD is active high.
- **BHLDA** is an output from the cache module to the system. When Bhold is asserted by another bus master, the cache module responds by activating BHLDA (bus hold acknowledge), the other bus master is then granted control of the bus.
- **BRDY#** is an input to the cache module. When the system asserts this pin, it indicates that the current memory cycle is complete. BRDY# is active low.
- **SBE0# - SBE3#** are four output signals from the cache module. They are the individual byte enables for the memory. These four signals are active low.
- **BADS#** is an output from the cache module to the system. When BADS# (board address status) is asserted, it indicates that the BA bus is stable. BADS# is active low.
- **BW/R#** is an input to the cache module from the system. BW/R# (board write read) is used in the SNOOP function of the module and helps the device to detect when a write has occured to an active cache address.
- **RESET** is an input to both the cache module and the 80386. The RESET signal comes from the system and is asserted for 8 or more CLK periods so that the processor and the cache module will be placed in a known reset state. The tags of the cache will be cleared. RESET is active high.
- **FLUSH** is an input to the cache module. While FLUSH is asserted, it will cause the tags to clear. This pin is a "programmable reset". This signal is active high.
- **LRDY#** is an input to the cache module. LRDY# is an indication to the module that a local bus cycle is complete. This signal is active low.
- **W/R#** is an input to the cache module. When W/R# is high it indicates that the 80386 is executing a write cycle and when it is low it shows that the processor is executing a read cycle.
- **ADS#** is an input to the cache module. This signal shows the status of the A bus. When ADS# is low it indicates that the address bits A (2) - A (31) are stable. This signal is active low.

The Microprocessor Interface

The microprocessor interface consists of four byte enable pins. The bus cycle status pins i.e. D/C#, MI/O#, W/R#, clock and reset signals, the address status pin ADS#, and the four local control signals FLUSH#, LRDY#, READY#, RESET, LBA# and NCA# (see Figure 15 for a complete description of the microprocessor and system interface pins).

The NCA# input is for decoding non-cacheable addresses such as I/O memory space. The designer needs to design a decoder that recognizes non-cacheable addresses. The decoder output ties directly to the NCA# input. LBA# is used to indicate that the 80386 is working with a local device (such as a coprocessor).

System Bus Interface

The system bus interface consists of the buffered data bus (BD0:31), the buffered address bus, (BA2:31), the bus byte enable signals (BBE0#-BBE3#), the system bus control signals (BM/IO#, BDC#, and BW/R#), and the system control signals of BRDY#, BHOLD, BADS# and BHLDA. It should be noted that the 80386 equivalent front end signals of the controller module are prefixed by the letter B (For a complete listing of system bus interface signals, see Figure 15).

- **CLK** is an input to the cache module. It is identical to the 80386 clock.
- **A (2) - A (31)** are the 30 address pins that connect the 80386 address bus to the cache module. These 30 signals are the A bus.
- **BE0# - BE3#** These four byte enable signals are outputs from the 80386 and are tied directly to the byte enable inputs of the cache module.
- **NCA#** is an input to the cache module, while active it indicates to the device that the current address present on the address bus, A (2) - A (31), is a non cache-address. This signal is active low.
- **D/C#** is an input to the cache module. D/C#, data-control, is used by the 80386 to indicate a data cycle or a control cycle. While low the processor is in a control cycle and while high in a data cycle. No cache operations are permitted in control cycles.
- **M/IO#** is an input to the cache module, while low it indicates that the 80386 is addressing an I/O device and while high it indicates the processor is addressing memory. No cache operations are permitted for I/O devices.
- **LBA#** is an input to the cache module, while active it indicates that the processor is accessing another device on the local bus, for example the 80387 coprocessor. Local bus addresses are not cache addresses.
- **DIR, DEN#** are outputs from the cache module. These signals control the data bus buffers and the address bus buffers (external to the module). DIR determines the direction of the flow of the data bus buffers. DEN# is the enable signal and is used to turn on the bus drivers.
- **WLE** is an output from the cache module to the data bus buffers and to the address bus buffers. WLE is used to latch write data into the write buffers.
- **SEL** is an output from the cache module. It is used to select the latches in the data bus buffers and the address bus buffers.
- **D (0) - D (31)** These 32 signals are the data bus connecting directly to the data bus of the 80386. They are also connected to the data bus buffers.
- **READY#** is an output from the cache module. When asserted it indicates to the 80386 that the current cycle is finished. This signal is active low.

Figure 15. Functional Cache Controller and 80386 Signal Descriptions

Timing Diagrams for the Cache Design

Figures 16 through 26 illustrate the cache controller and memory module timing diagrams for a number of different bus cycles, namely cache read miss, cache read hit, write cache hit, write cache miss, read LBA, write LBA, read NCA, write NCA, BHOLD, and BHLDA. Figures 25 and 26 illustrate the cache tag and cache memory timing for both the cache and SNOOP tag.

Cache Read Miss and Hit Cycles

The cache read hit cycle, illustrated in Figure 16, begins by ADS# going low followed by the W/R# signal going low (to indicate a read). The controller responds by driving WE1# high. The WE#1 signal which drives both the local bus cache tag and the SNOOP tag sets the two cache tags up for a read and compare operation. After the read and compare operation is complete, the MAT1 signal will be valid. At this point in time (at the beginning of bus state T2) the cache controller samples MAT1. If MAT1 is high, it indicates that the cache memory has valid data. The controller responds to this condition by sending its OE# signal low which in turn enables the output of the cache memory to drive the microprocessor data bus with its associated 32-bit data word.

On the other hand, if MAT1 was low, the controller would respond by entering into a cache read miss cycle (as shown in Figure 17). This condition indicates that the address is not cached. For the cache read miss cycle, the cache controller drives the DEN# signal low which connects the local data bus to the system data bus. The control signals ADS# and W/R# are duplicated by BADS# and BW/R# which are placed on the system bus to allow main memory access. The system bus responds with the required data and then drives BRDY# low when done. During the main memory access, the controller updates the cache memory with the new data, the local bus cache tag and the SNOOP tag with the associated tag. After the controller receives the BRDY# signal from the system bus, it then drives READY# low which terminates the bus cycle. It should be noted here, that for the cache read miss, the READY# signal is held high an amount of time equal to the main memory cycle time.

Cache Write Hit and Miss Cycles

When the microprocessor writes data to memory it may enter into a write hit cycle or a write miss cycle (Figures 18 and 19). As with the cache read hit cycle, the beginning of the cycle is instigated by ADS# going low, but with W/R# going high. This state results in the controller enabling the local and SNOOP cache tags for a read and compare operation. If MAT1 is returned high to the controller from this tag, a write hit has occurred which results in the controller enabling the cache memory for a write operation (via the WE2# line). At this time the CPU data bus is written into the cache memory.

For either a cache hit or miss cycle, the cache controller also drives the WLE line of the posted write latch such that the address and data bus contents are captured for the system bus. For a write miss, the controller exhibits similar timing as it does for the write hit. However, for a write miss, the cache controller will start writing to both cache and main memory as if it was handling a write hit cycle. If later during T2 it was determined that a miss had occured (via MAT1) then the new content of that cache location does not correspond to the tag address. The WINV# signal will be driven low to invalidate the corresponding tag in the cache tag and the SNOOP tag (see Figures 28 and 30).

LBA and NCA Read and Miss Timings

LBA and NCA both deal with special conditions. The LBA (local bus access) cycle occurs when another device is to be accessed on the local bus for a read or write operation. For the Intel 80386 this is most often a numerics coprocessor. In order to read data from a coprocessor on the local bus, (Figure 20), the LBA input to the cache controller is activated. The cache controller then disables the cache memory (via WE2# and OE2#) the tag and the SNOOP memory (via WE1#). The local ready signal (LRDY) is sent from the coprocessor to the controller indicating the end of the LBA cycle.

NCA (non-cacheable address) cycles are entered into whenever the NCA input to the cache controller is active. The NCA is usually employed to keep I/O data from entering the cache. An active NCA# input results in the controller disabling the cache memory, cache tag and the SNOOP tag. This, of course, keeps the undesired addresses from entering the cache. As noted in Figure 22, the NCA cycle has added wait states due to the fact that the speed of the I/O device is limited. The designer has also the option of mapping the address space in several sections and choosing what section of the address space will be cacheable. This is accomplished by connecting the NCA# input to the output of an appropriate decoder. During NCA# cycles the cache ensemble is totally transparent.

Cache Memory and Cache Tag Timing

Figures 25 and 26 illustrate the timing specifications for the cache memory, the cache tag and the SNOOP tag. The associated tables give the necessary memory timing delays for the 16MHz, 20MHz and 25MHz versions of the 80386 microprocessor. As seen in the table, the READY# signal AC timing specification is met by use of an 74F64 AOI with a delay that is less than 6ns.

READ HIT TIMING

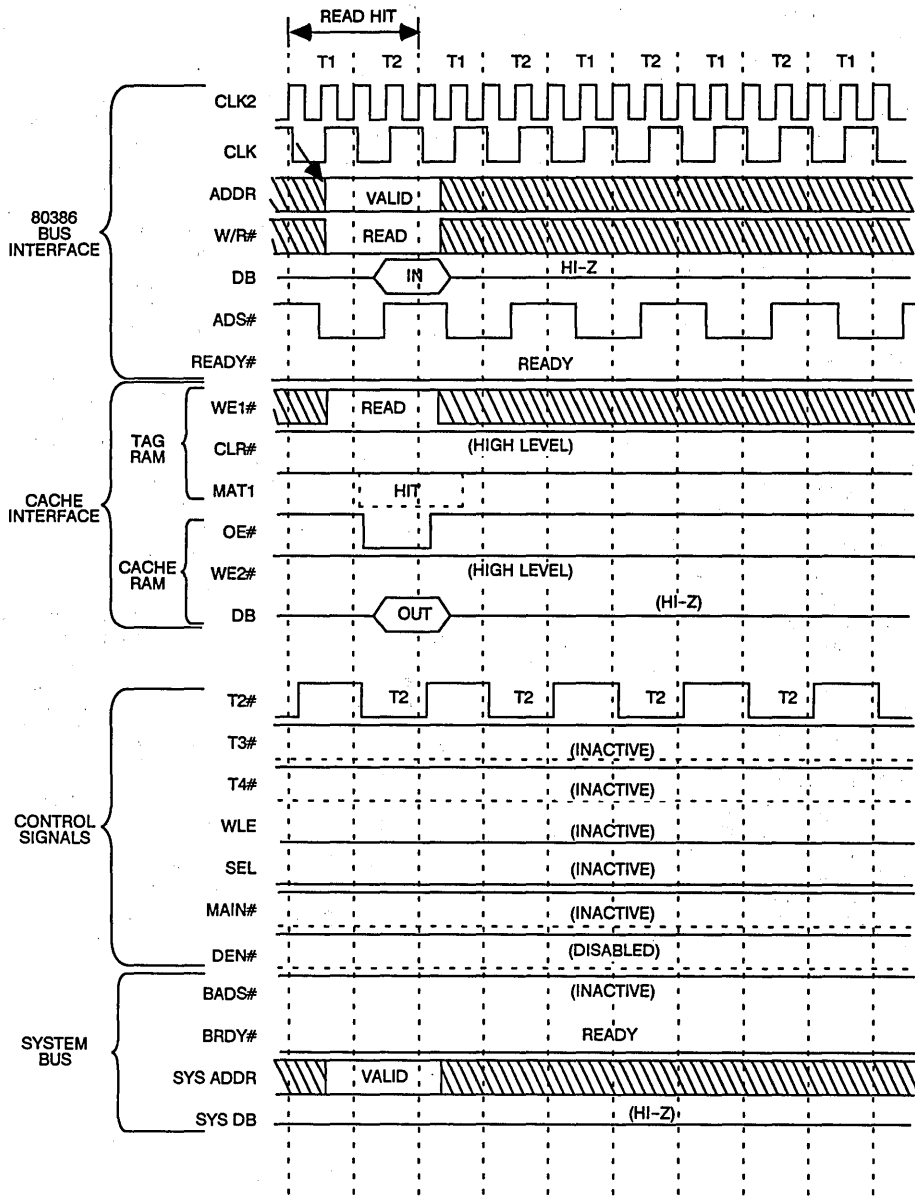
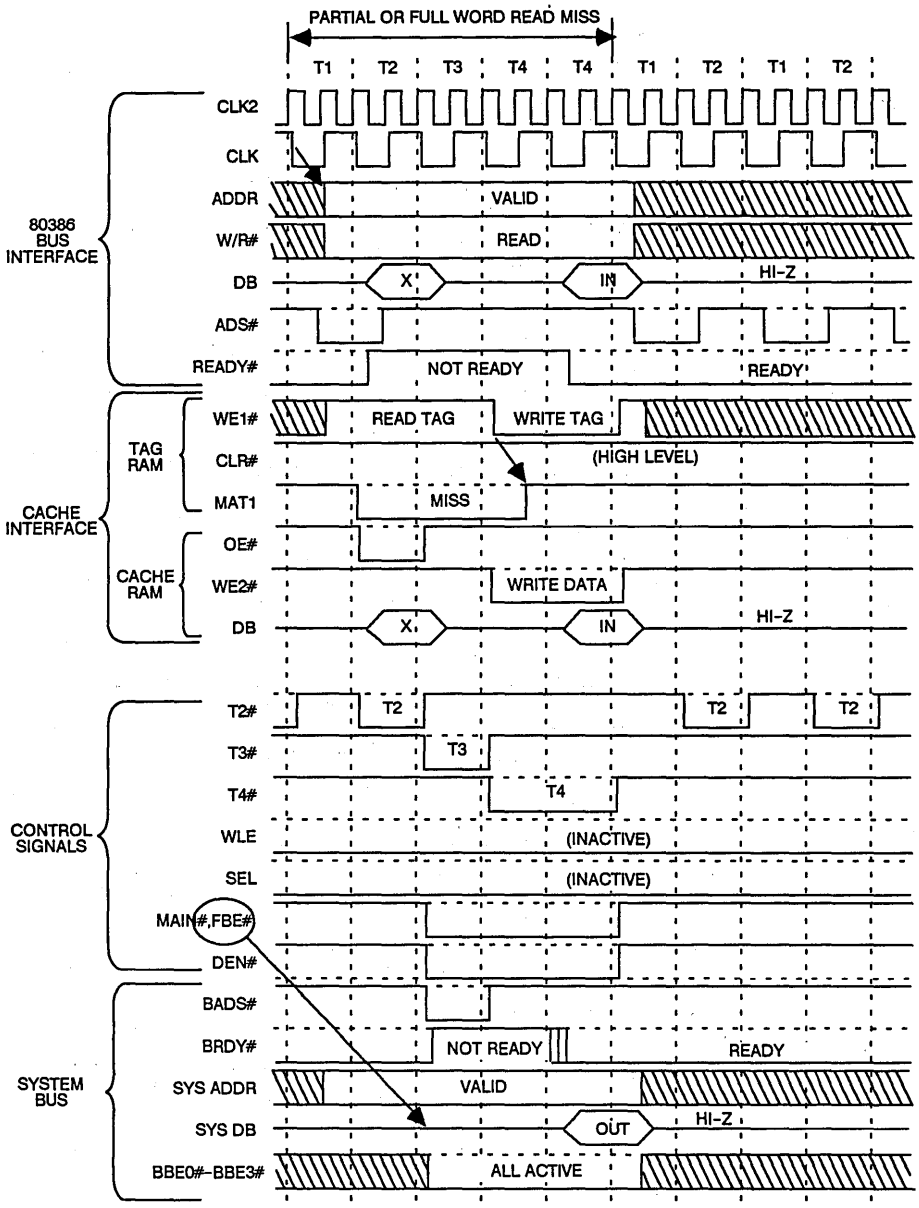


Figure 16. Read Hit Timing

READ MISS TIMING



Note: FBE causes all FB lines to be activated.

Figure 17. Read Miss Timing

WRITE HIT TIMING

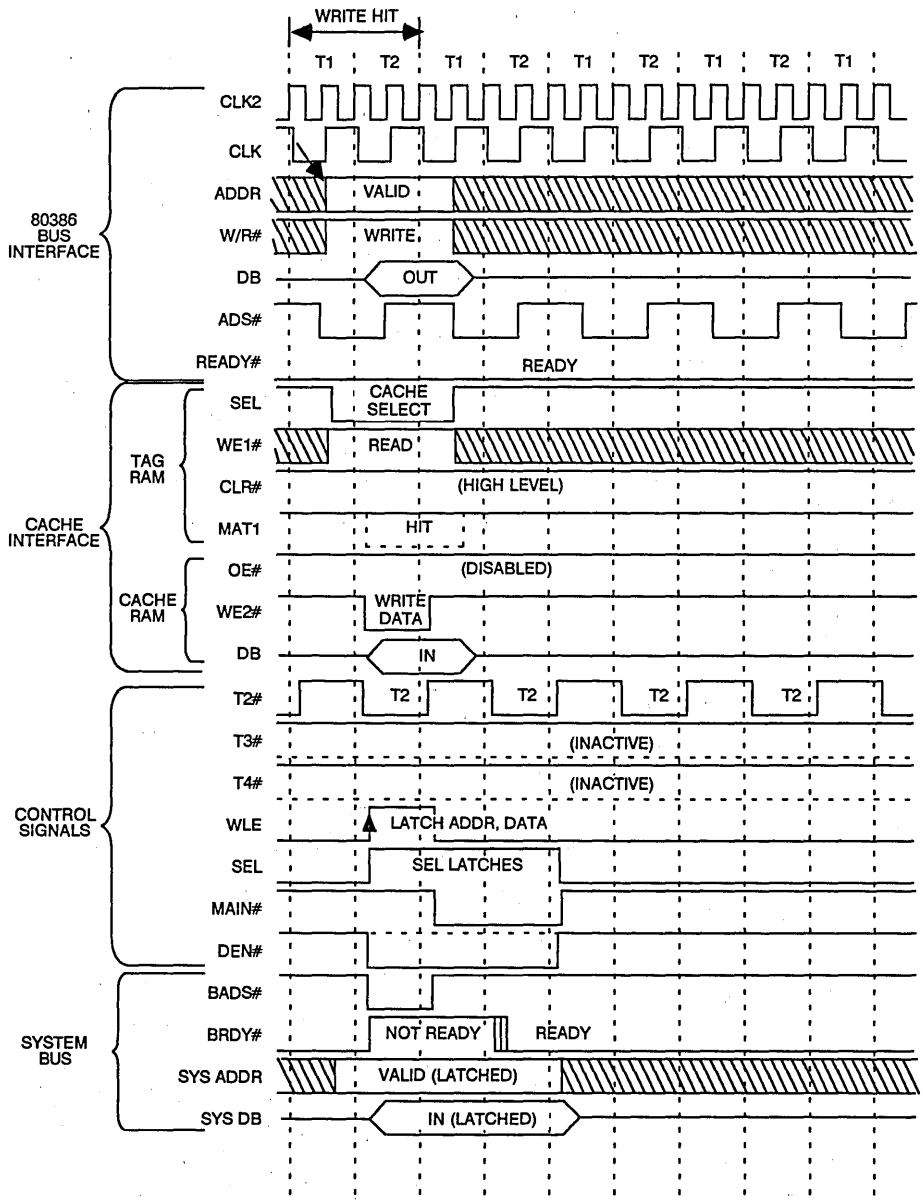


Figure 18. Write Hit Timing

WRITE MISS TIMING

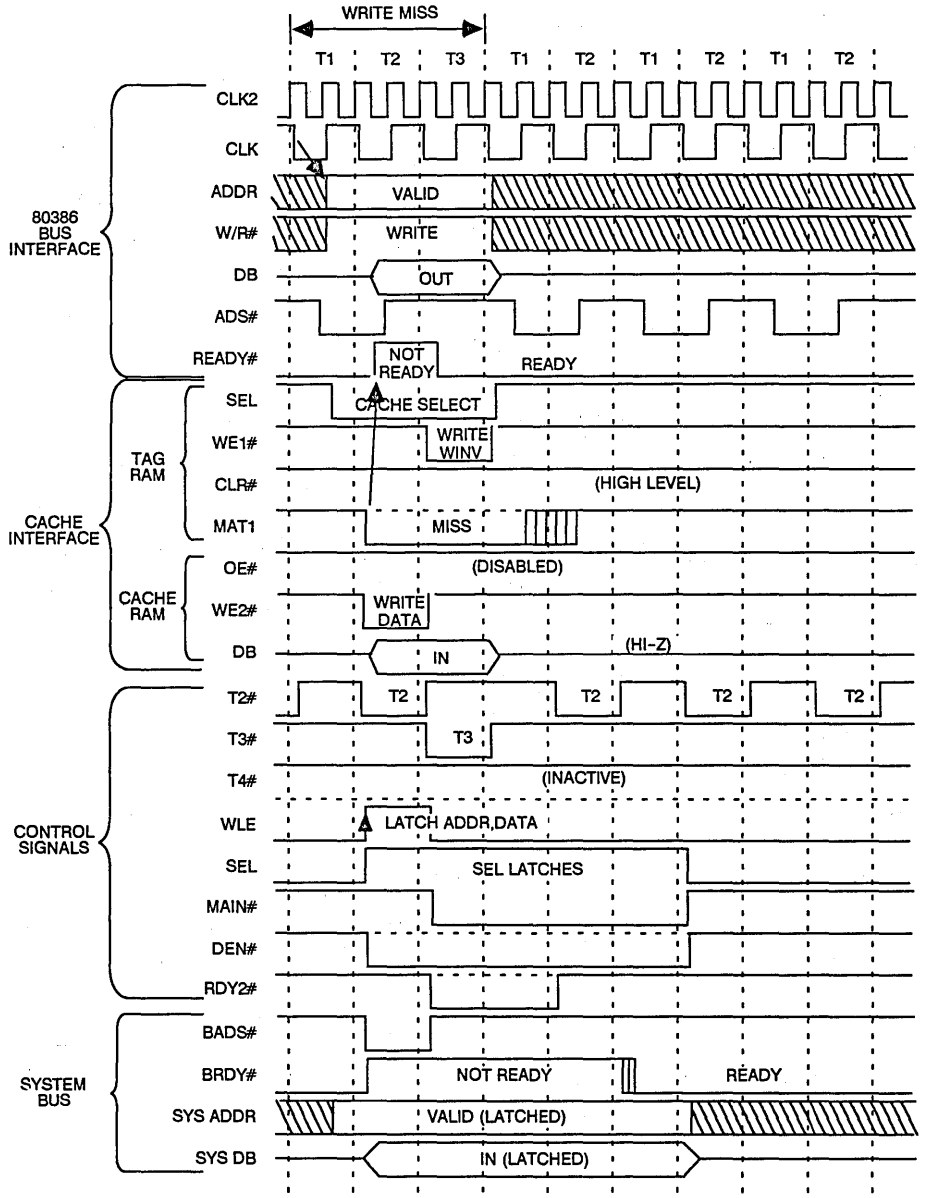


Figure 19. Write Miss Timing

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READ LBA TIMING

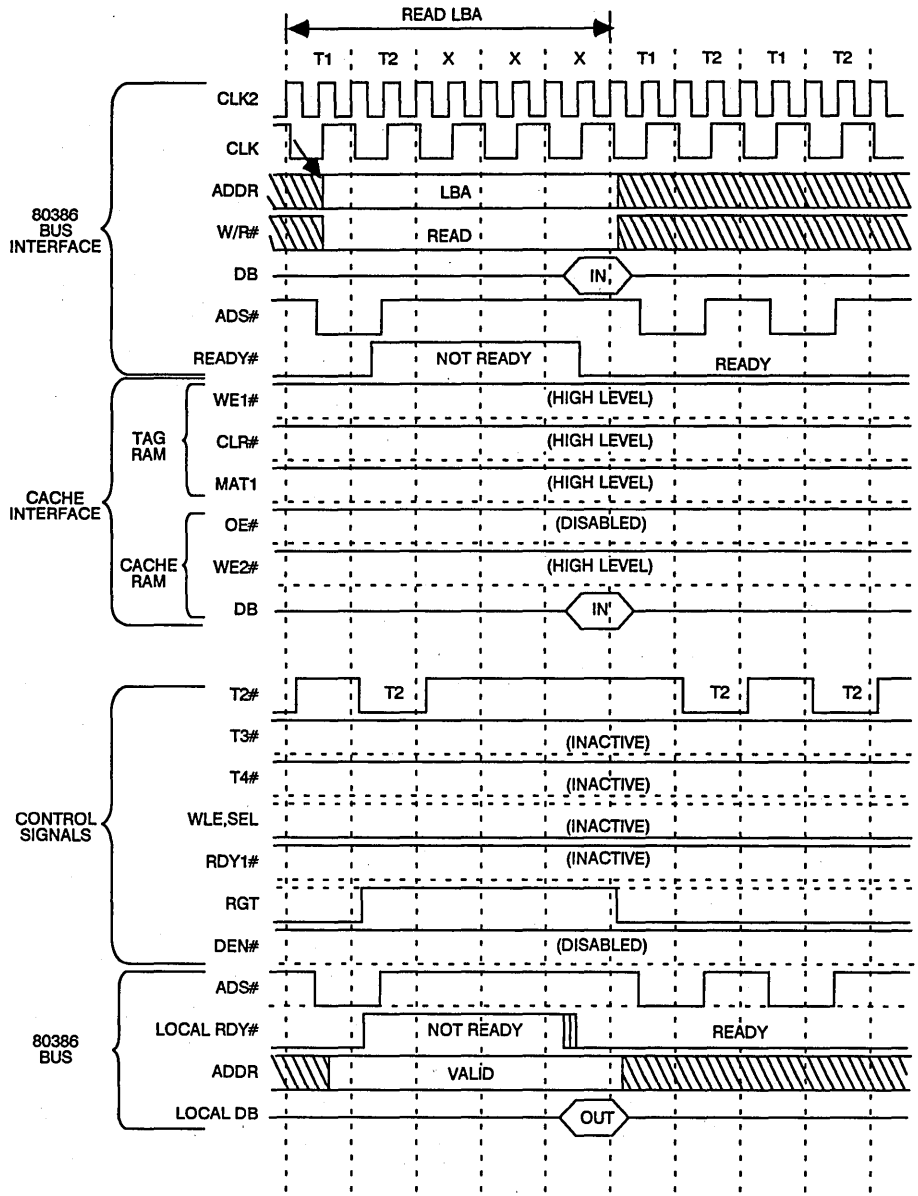

Figure 20. Read Local Bus Access Timing

WRITE LBA TIMING

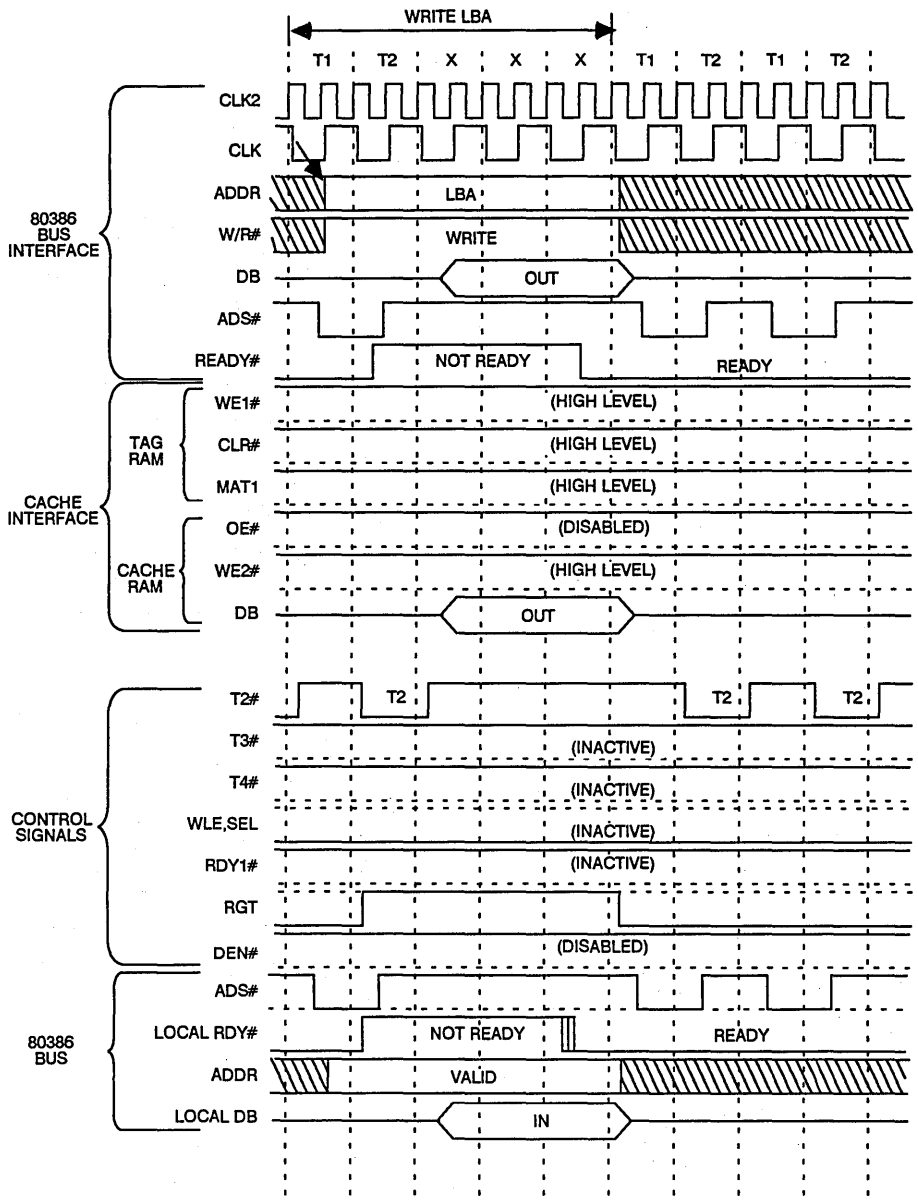

Figure 21. Write Local Bus Access Timing

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READ NCA TIMING

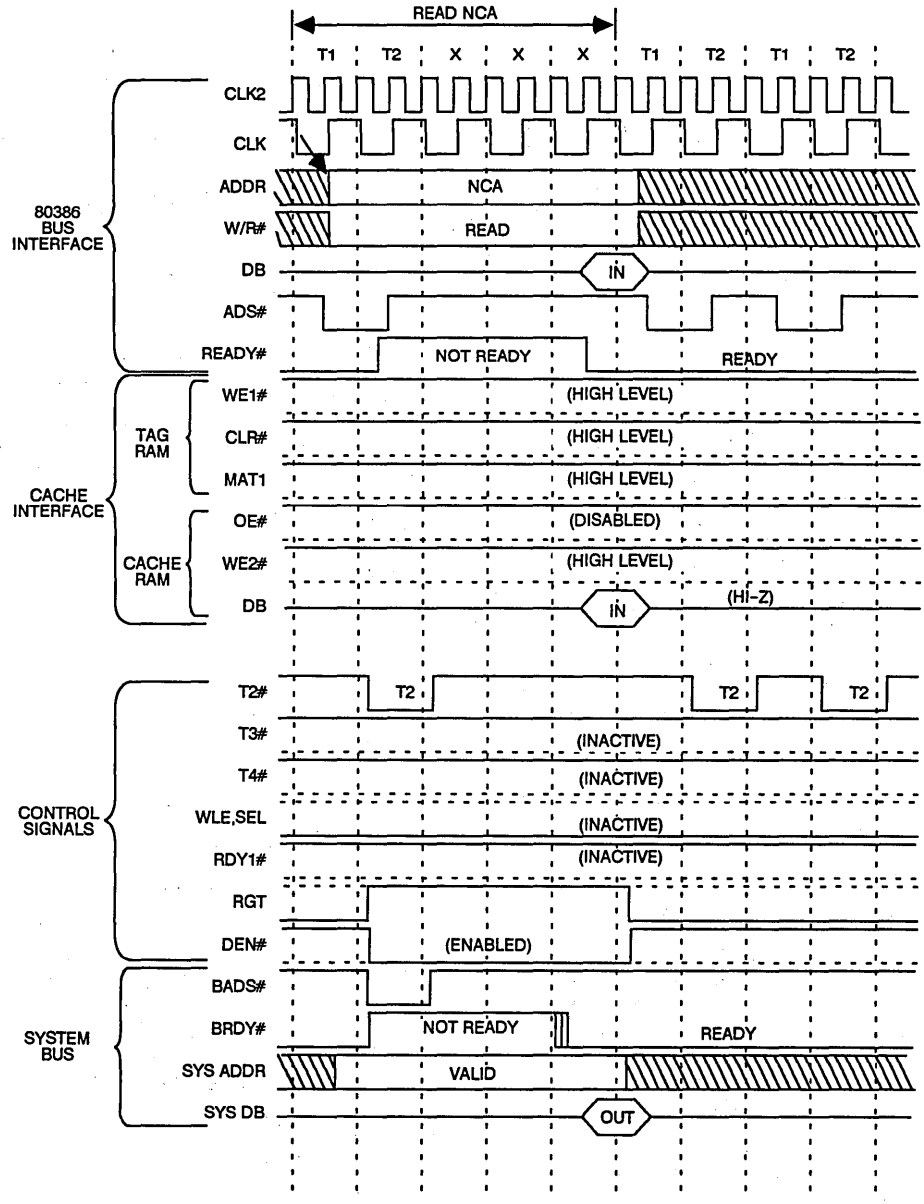

Figure 22. Read Non-Cached Addresse Timing

WRITE NCA TIMING

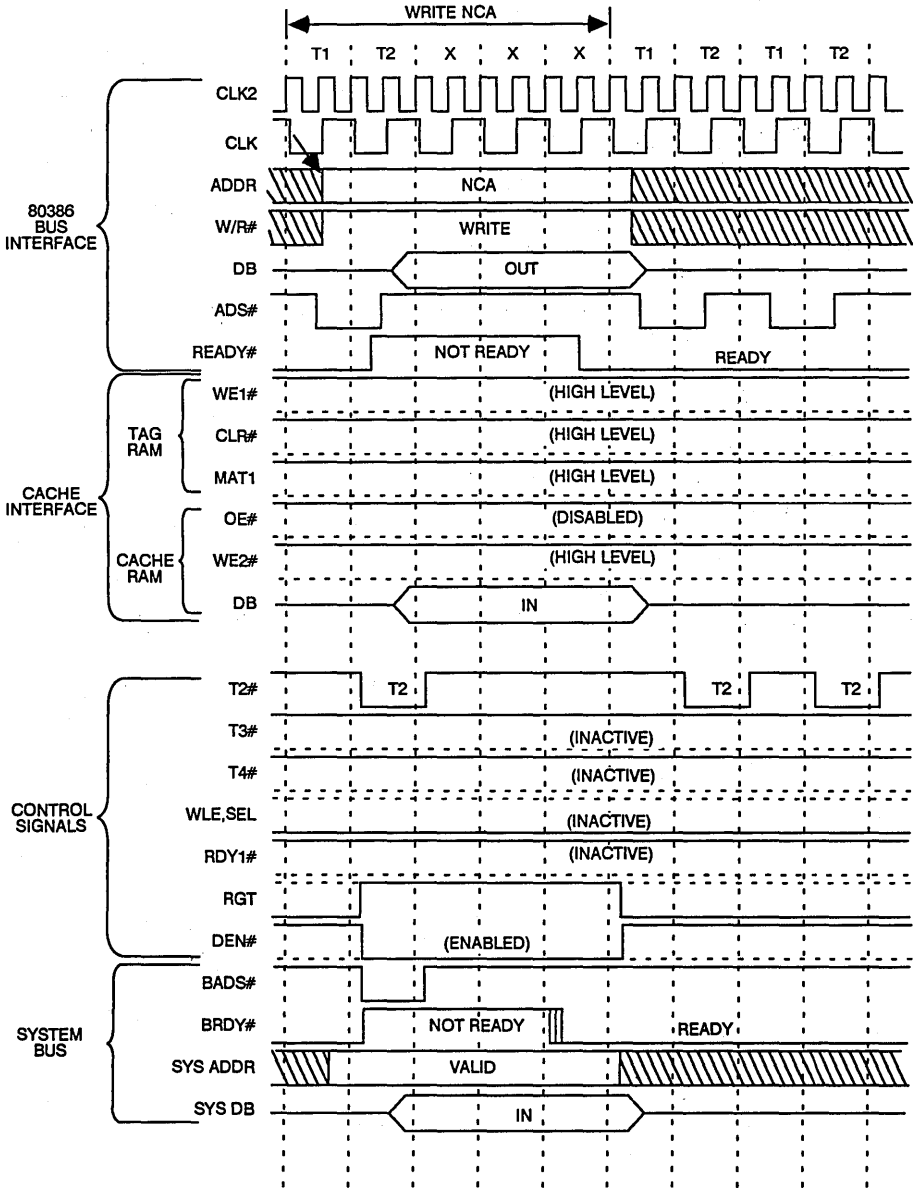

Figure 23. Write Non-Cached Addresse Timing

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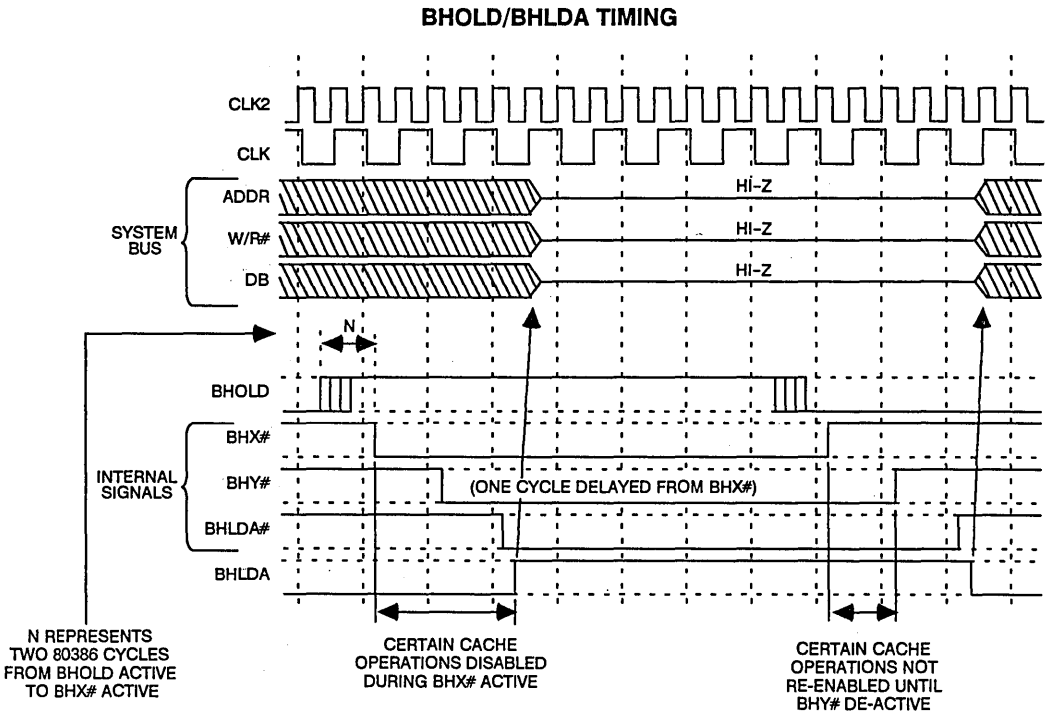
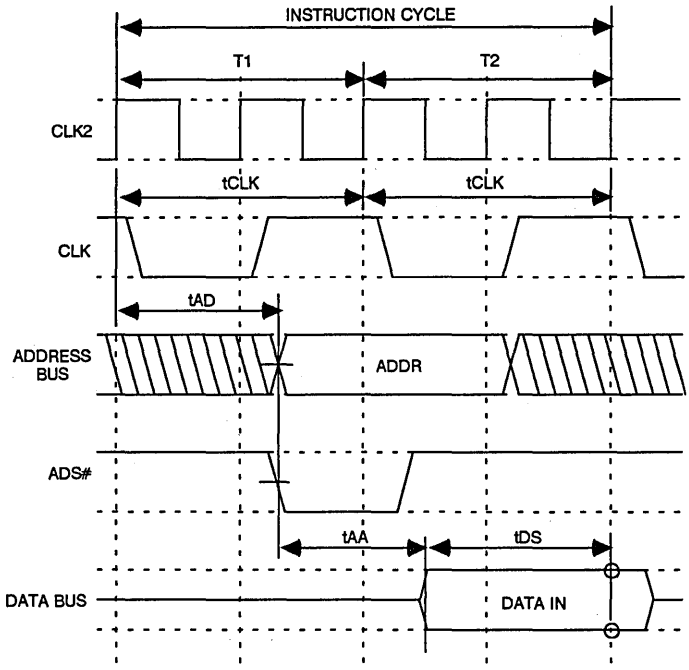


Figure 24. Hold and Hold Acknowledge Timing



SPEC ANALYSIS

Parameters	80386 Clock Rate			Units
	16MHz	20MHz	25MHz	
tCLK	62	50	40	ns
tAD	40	35	30	ns
tDS	10	10	5	ns
tAA	72	55	45	ns

Figure 25. Cache Memory Timing

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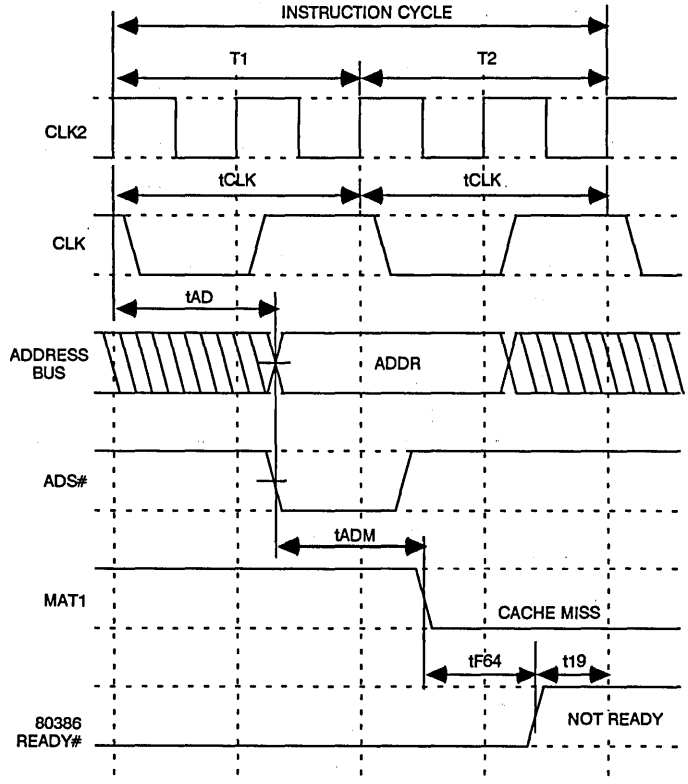

SPEC ANALYSIS

Parameters	80386 Clock Rate			Units
	16MHz	20MHz	25MHz	
tCLK	62	50	40	ns
tAD	40	35	30	ns
tADM	58	48	34	ns
tF64	6	6	6	ns
t19	20	11	10	ns

Figure 26. Cache Tag and SNOOP Timing

Top Level Diagram Description and Operation

Figure 27 illustrates the top level diagram of the cache controller and memory module. The block CRAM is the cache memory, TRAM is the cache tag for the local bus, SNOOP is the cache tag for the system bus (SNOOP tag), and CTRL is a PAL based state machine which controls the timing and state sequences for interfacing to; the cache memory; the SNOOP and local cache tags; and the system and microprocessor buses.

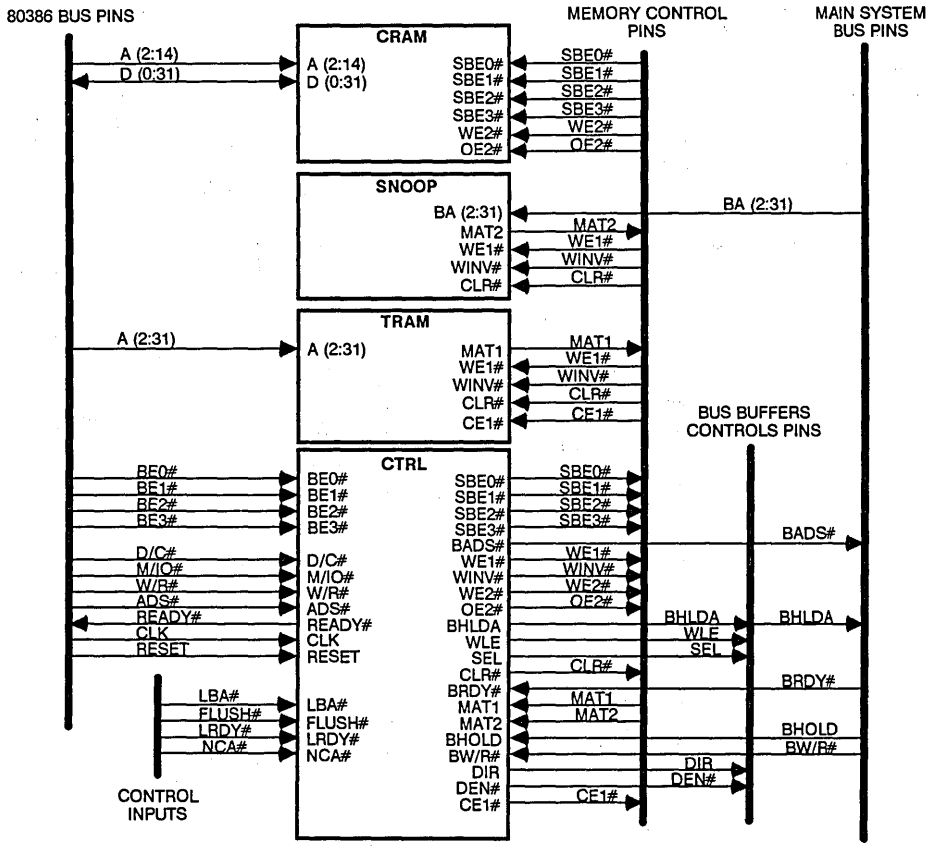

Figure 17. Top Level Diagram of the Cache Controller Module

TRAM Block

Figure 28 represents the connections of the local address bus (80386 address bus) to the cache tag SRAM (CRAM). A(2:31) are the address lines which come directly from the 80386 address bus. The cache tag is addressed using address bus bits A(2) through A(14). A(15) through A(31) are the address bits that are recorded in the memory of the cache tag. MAT1 is an input to the cache controller indicating a hit or a miss.

CE#1, WE#1, CLR# and WINV# are control signals which come from the CTRL block (the internal PALs) to the cache tag. WINV# is used to invalidate a write entry in the cache. For instance, for an 80386 write cycle, the controller will start to write data to the cache and main memory at the same time. However, if it is determined later on in the cycle that a write miss occurred, the WINV# signal will write a logic low in the 24th bit of the tag which invalidates the tag address at the cache's page offset location. CE#1 is used to keep non-cacheable addresses from entering the tag. If a non-cacheable address is detected (via the NCA# input), CE#1 will be disabled which in turn floats the IDT7174 cache tag's I/Os. The CLR# signal is an input signal to the tag and the SNOOP and is used to flush the cache on SNOOP hits.

CRAM Block

Figure 28 illustrates the cache memory which is used to store the associated data of the tag addresses. The cache memory consists of four IDT7164 8K x 8 SRAMs. A(2:14) are the same address lines that address the cache tag memory of Figure 27 i.e. the microprocessor address bus. D(0:31) is the 32 bit data bus of the 80386. The data bus is divided into 4 bytes with each byte being stored in a unique IDT7164 SRAM.

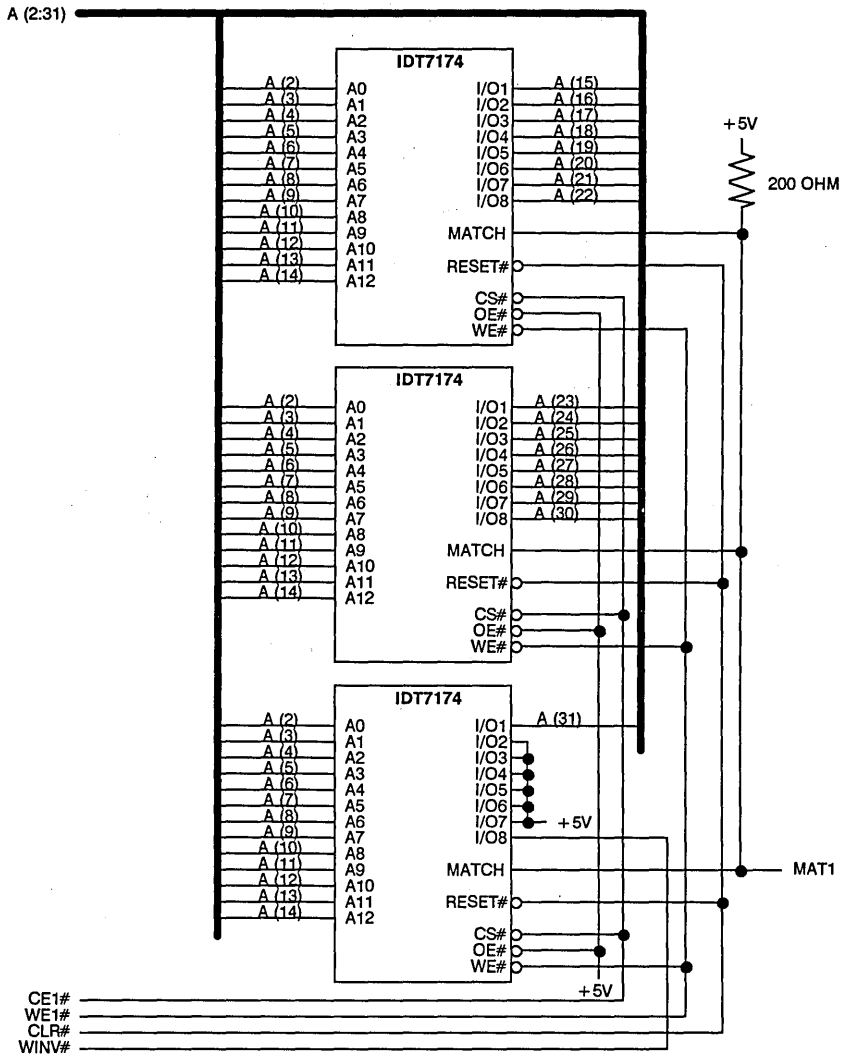

Figure 28. Cache Tag Block (TRAM)

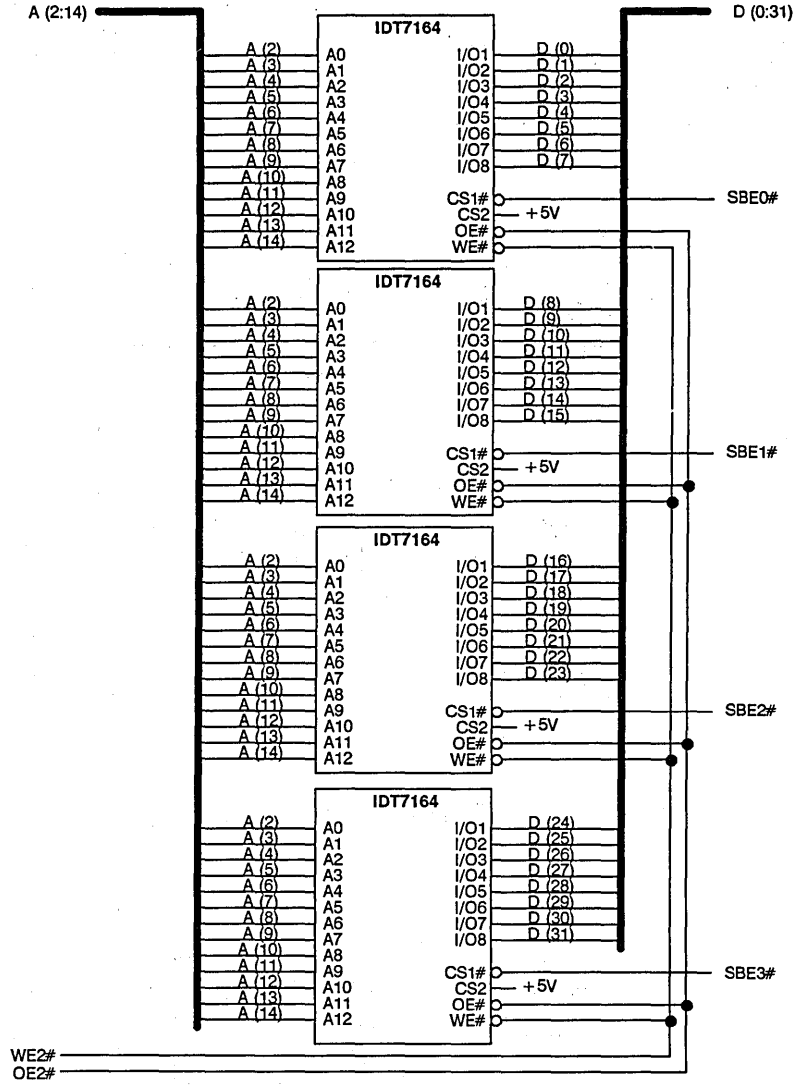

Figure 29. Cache Memory Block (CRAM)

SBE(0#:3#), WE2#, and OE2# are signals generated by the CTRL block (Figure 34) which control the operation of the cache memory. SBE (0#:3#) are used to select a specific byte of the 32-bit doubleword via their direct connection to the IDT7164s. In the case of a read miss, if the microprocessor wants to read just one byte instead of the full 32-bit doubleword, the controller will update the entire 32-bit double word in the data cache (so as to ensure valid data in the cache). In order to update the full 32-bit doubleword, the force byte enable signal, FBE#, is gated with the byte enable signals, BE(0#:3#), of the 80386 to form SBE(0#:3#) as shown in Figure 34. WE2# and OE2#, from the CTRL block, are used to control the read and write operation of the cache memory.

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SNOOP Block

The SNOOP (Figure 30) is very similar to the tag. BA(2:31), the system address bus, is the main memory address bus that the SNOOP monitors. BA(2:14) is used to address the SNOOP and BA(15:30) is the address recorded in the SNOOP. As mentioned previously, the design of the controller module is such that the SNOOP and the tag always contain the same information.

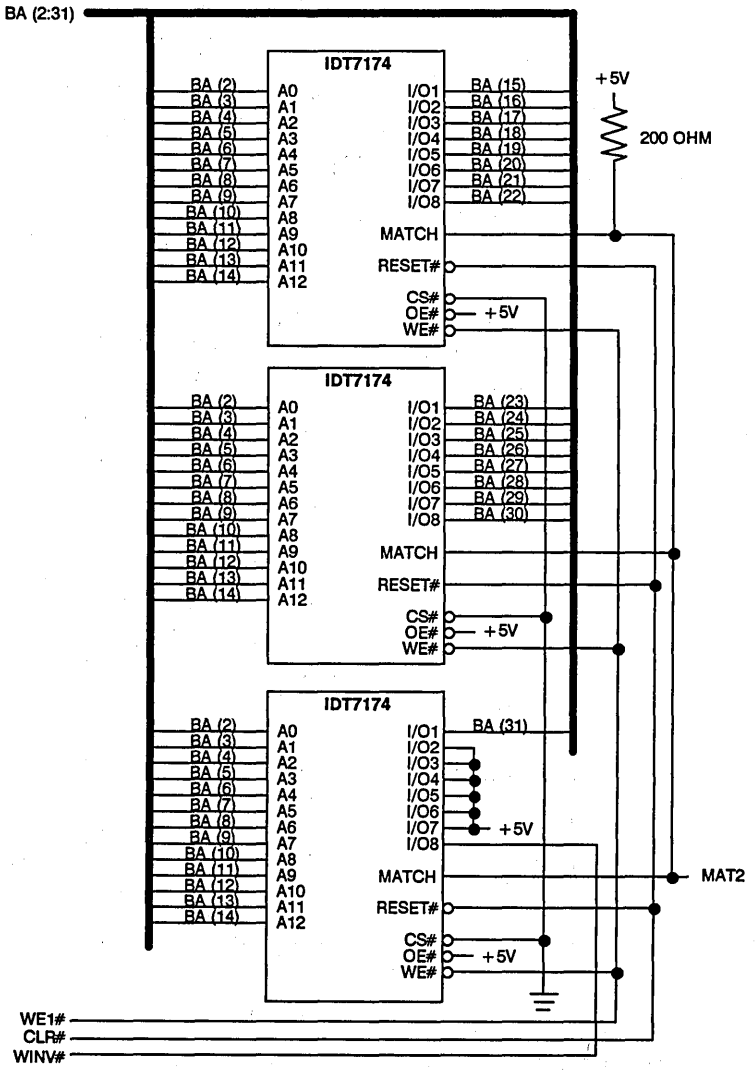


Figure 30. SNOOP Block (SNOOP)

The WINV#, CLR# and WE1# signals are used in the exact same way as the tag memory of Figure 28. Functionally the only difference between the tag memory and the SNOOP memory is the fact that the SNOOP memory is always monitoring the main memory address bus.

The only output of the SNOOP block is MAT2 which ties directly to the control block to indicate a SNOOP hit or miss. On a SNOOP hit, the cache controller will flush the entire contents of the tag (TRAM) and the SNOOP tag via the clear line (CLR#).

Posted Write Logic Design and Operation

The posted write logic comes into action when a write occurs. For the posted write operation, the IDT74FCT646 octal transceiver registers are controlled by the WLE (write latch enable), signal. The WLE line, on a microprocessor to memory write, latches the data and its address into the 646s and continue on without wait states while the cache control logic downloads the posted write buffer to main memory (the posted write operation can not be interrupted by an external system bus request i.e. it is locked). In a case where two write miss cycles occur back to back, the 80386 will have a number of wait states depending on the main memory access time.

For a write hit, the timing (Figure 18) is the same as that of the read hit (Figure 16). For a write miss however, the bus cycle is extended by an extra clock period (Figure 19).

Design of the Cache Controller Block (CTRL)

The design of the cache controller requires determining the state machine cycles of the 80386 and replicating them through a PAL based state machine. For this design, three 22V10 PALs were used (Figure 32) to form the PALs block of the controller in Figure 31.

As shown in Figure 31, the READY# input is generated by the use of the 74F64. For Figure 31, it should also be noted that all inputs to the PALs block are on the left side, all outputs are on the right side and buses are represented as dark vertical lines. For Figure 32 it should be noted that the pin out are shown for 28-Lead PLCC packages.

The designer **should use caution if he plans to implement the PAL design** given in this application note. In particular, the pin assignment should not be changed. This is because the internal structure of the PALs may not accommodate a term swap between pins. For example, if the signals WINV# and DIR of PAL1 (Figure 32) were interchanged (WINV# to pin 19 and DIR to pin 17), the JEDEC fuse map will not run because pin 17 does not have enough inputs (internally) to handle the equations for DIR.

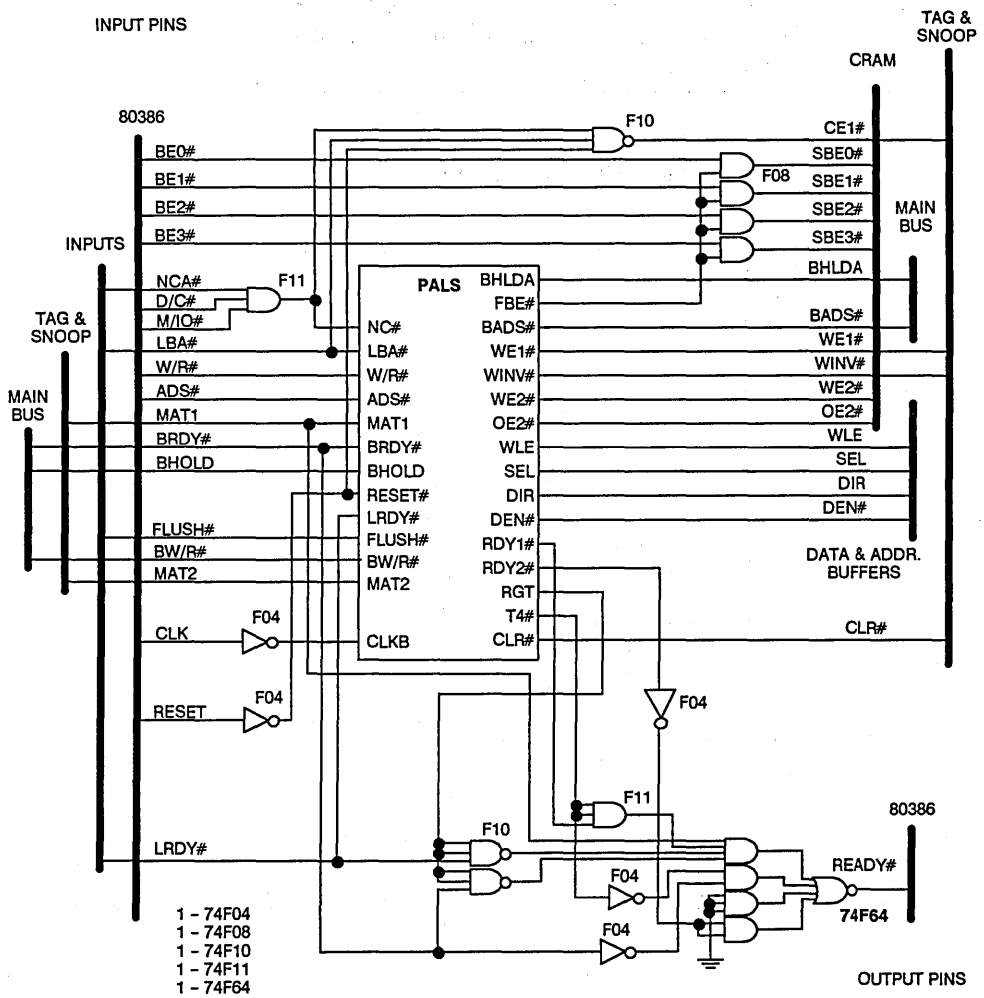
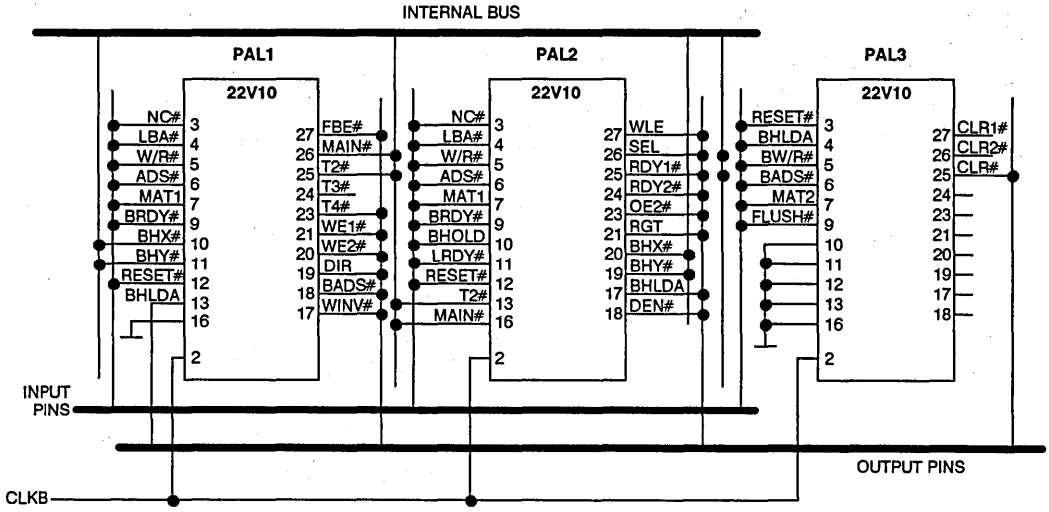


Figure 31. The Controller Block (CTRL)



PINS ARE FOR 28-LEAD PLCC PACKAGES.

Figure 32. The PALs of the CTRL Block

PAL Equations

The equations for the three PALS are presented in Tables 2 through 6. The PALASM source code for the PALs is also given for generating the corresponding JEDEC fuse map.

SIGNAL NAME	INPUTS										INTERNALS						DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHX#	BHY#	BHLDA	RESET#	T2#	T3#	T4#	MAIN#	FBE#	DIR	
FBE#	H	H	L		L			H		H	L			H	H		Read Miss, no Main
	H	H	L		L	L	H			H	L			L	H		Read Miss, Main
						H				H					L		Stay until Ready
MAIN#	H	H	H					H		H	L			H			Write
	H	H	L		L			H		H	L			H			Read Miss, no Main
	H	H	L		L	L	H			H	L			L			Read Miss, Main
						H				H				L			Stay until Ready
T2#				L						H							ADS
	H	H	L		L	H				H	L			L			Stay if Rd Miss, not Rdy
	H	H	H							H	L			L			Stay if Write, Main
	L	H								H	L			L			Stay if NCA, Main
	H	H	L		L			L		H	L						Stay if Read Miss, BHOLD
	H	H	H					L		H	L						Stay if Write, BHOLD
T3#	H	H	L		L			H		H	L			H			T2,Rd Miss, no Main
	H	H	L		L	L	H			H	L			L			T2,Rd Miss, Main
	H	H	H		L			H		H	L			H			T2,Wr Miss, no Main
T4#	H	H	L							H		L					T3, Read
						H				H			L				Stay until Ready

Table 2. First Part of PAL1's Equations

Tables 2 and 3 show the equations for PAL1. A horizontal line in these tables means an AND function between the present terms. The lines grouped together for a signal are ORed vertically. As an example, the logic equation defining the signal FBE# is as follows:

$$\begin{aligned}\text{FBE\#} = {} & \text{NC\#} \bullet \text{LBA\#} \bullet \overline{\text{W/R\#}} \bullet \overline{\text{MAT1}} \bullet \text{BHY\#} \bullet \text{RESET\#} \bullet \overline{\text{T2\#}} \bullet \text{MAIN\#} \bullet \text{FBE\#} \\ & + \\ & \text{NC\#} \bullet \text{LBA\#} \bullet \overline{\text{W/R\#}} \bullet \overline{\text{MAT1}} \bullet \overline{\text{BRDY\#}} \bullet \text{BHX\#} \bullet \text{RESET\#} \bullet \overline{\text{T2\#}} \bullet \overline{\text{MAIN\#}} \bullet \text{FBE\#} \\ & + \\ & \text{BRDY\#} \bullet \text{RESET\#} \bullet \overline{\text{FBE\#}}\end{aligned}$$

Bared signal = logic low level
Unbared signal = logic high level

Each line is accompanied on the right hand side by a short comment describing the situation to which it relates.

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SIGNAL NAME	INPUTS										INTERNALS						DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHX#	BHY#	BHLDA	RESET#	T2#	T3#	T4#	MAIN#	FBE#	DIR	
WE1#	H	H	H		L			H		H	L			H			Write Miss, no Main
	H	H	L		L					H		L					Read Miss
	H	H	L			H				H			L	L			Stay until Rd Miss, Ready
WE2#	H	H	H	L						H				H			Write, ADS
	H	H	L		L					H		L					Read Miss
	H	H	L			H				H			L	L			Stay until Rd Miss, Ready
WINV#	H	H	H		L			H		H	L			H			Write Miss, no Main
BADS#	H	H	L		L		H	H		H	L			H			Read Miss, no Main
	H	H	L		L	L	H			H	L			L			Read Miss, Main
	L	H		L			H			H				H			NCA, no Main
	L	H				L	H			H				L			NCA,wait for Main
	L	H					H	L		H				H			NCA, after BHOLD
	H	H	H	L			H	H		H				H			Write, no Main
	H	H	H			L	H			H				L			Write, wait for Main
	H	H	H			L	H	L		H				H			Write, after BHOLD
DIR		H	H	L			H			H				H			Write, no Main
		H	H			L	H			H				L			Write, wait for Main
						H			L	H						H	Stay until Ready (no BH)
		H	H					L		H	L					H	Stay until BHOLD
		H	H			L	H	L		H				H		L	Write, after BHOLD

Table 3. Second Part of PAL1's Equations

SIGNAL NAME	INPUTS											INTERNALS								DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHOLD	LRDY#	T2#	MAIN#	RESET#	BHX#	BHY#	RDY1#	RGT	BHLDA	SEL	DEN#	RDY2#	
WLE	H	H	H	L						H	H									Write, no Main
	H	H	H			L				L	H									Write, wait for Main
SEL	H	H	H	L						H	H									Write, no Main
	H	H	H			L				L	H									Write, wait for Main
						H					H						L	H		Stay until Ready (no BH)
	H	H	H						L		H		L					H		Stay until BHOLD
RDY1#	H	H	H	L		H				L	H	H								Write while Main
						H				L	H		L							Stay until Ready
	H	H	H	L							H	L								Write while BHOLD
											H		L	L						Stay until released
	L	H				H				L	H	H								NCA, Main
	L	H		L							H	L								NCA while BHOLD
	L	H							L		H		L							NCA while BHOLD
RDY2#	H	H	H		L				L	H	H	H	H							T2,Wr Miss, no Main
				H							H								L	Stay until next ADS#
OE2#	H	H	L	L	H						H									Read Hit

Table 4. First Part of PAL2's Equations

SIGNAL NAME	INPUTS											INTERNALS								DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHOLD	LRDY#	T2#	MAIN#	RESET#	BHX#	BHY#	RDY1#	RGT	BHLDA	SEL	DEN#	RDY2#	
RGT	L	H		L		L				H	H	H			L					NCA, not Busy
	L	H									H	H	L		L					NCA after BHOLD
	L	H				L			L	L	H	H			L					NCA, wait for Main
		L		L							H				L					LBA
		H				H					H				H					Stay NCA until Ready
		L						H			H				H					Stay LBA until Ready
BHX#							H		L	H	H	H								BHOLD, no Main
						L	H		L	L	H	H								BHOLD, Main
							H				H	L								Stay until no BHOLD
BHY#											H	L								One cycle after BHX
BHLDA						L	H				H		L			L				BHY when Ready
							H				H					H				Stay until no BHOLD
DEN#	H	H	L		L				L	H	H		H					H		Read Miss, no Main
	H	H	L		L	L				L	H									Read Miss, wait for Main
		H	H	L						H	H	H								Write, no Main
		H	H			L				L	H	H								Write, wait for Main
	L	H	L	L						H	H		H					H		Read NCA, no Main
	L	H	L			L				L	H									Read NCA, wait for Main
						H					H							L		Stay until Ready
		H	H			L				H	H	H	L					H		Write, after BHOLD
	L	H				L				H	H	H	L					H		NCA, after BHOLD

Table 5. Second Part of PAL2's Equations

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SIGNAL NAME	INPUTS						INTERNALS		DESCRIPTION
	RESET	BHLDA	BW/R#	M/IO2	BADS#	FLUSH#	CLR1#	CLR2#	
CLR1#	H	H	H		L				Snoop Write while BHLDA
CLR2#	H			H				L	Write Hit while BHLDA
CLR#	H			H				L	Write Hit while BHLDA
	H						L		Stay one more cycle
	H					L			External FLUSH
	L								System RESET

Table 6. PAL3's Equations

These equations were developed by closely analyzing the logical timing diagrams for the 80386 under all the possible states. A combination of several of these states following each other were also looked at. The timing waveforms for the controller were then developed in order to meet its specifications and handle the 80386 operations. Once the timing waveforms were done then the equations were derived and the PALs programed.

The software PALASM was used to compile the equations for the PALs into their corresponding JEDEC fuse map. The source code for each PAL's program is presented below. The nomenclature in PALASM is somewhat deceptive in that an apparently logical "high" term might mean a logical "low". In the pin declaration part of the source code an active low signal is represented by a "/" preceding its name. In the description of the equations, however, if a term is written as it was declared (in the pin declaration) it will be perceived as a logic high, yet if the signal is written in the opposite sense than in the declaration then PALASM understands it as a logic low.

Keeping the above in mind, it will become clear to the reader how Tables 2 through 6 match their respective PAL code.

```
TITLE           Controller1
PATTERN         N.A.
REVISION        1.1
AUTHOR          Mammad Safai
COMPANY         Integrated Device Technology Inc.
DATE            09-21-1988

CHIP CONTROL_PAL1 PAL22V10

;PINS
;1    2    3    4    5    6    7    8    9    10
CLKB /XNC /LBA /W_R /ADS MAT1 /BRDY /BHX /BHY /RESET
;11   12   13   14   15   16   17   18   19   20
BHLDA  GND  NC  /WINV /BADS  DIR /WE2 /WE1 /T4  /T3
;21  22       23   24   25
/T2 /MAIN  /FBE  VCC  GLOBAL

EQUATIONS

GLOBAL.RSTF  = RESET

DIR    := /BHX * /LBA * /W_R * ADS * /RESET * /MAIN
        +
        /BHX * /LBA * /W_R * BRDY * /RESET * MAIN
        +
        /BRDY * /BHLDA * /RESET * DIR
        +
        /LBA * /W_R * BHY * /RESET * T2 * DIR
        +
        /LBA * /W_R * BRDY * /BHX * BHY * /RESET * /MAIN *
        /DIR

FBE    := /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN */FBE
        +
        /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
        T2 * MAIN * /FBE
        +
        /BRDY * /RESET * FBE

MAIN   := /XNC * /LBA * /W_R * /BHY * /RESET * T2 * /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
        T2 * MAIN
        +
        /BRDY * /RESET * MAIN

T2     := ADS * /RESET
        +
        /XNC * /LBA * W_R * /MAT1 * /BRDY * /RESET * T2 *
        MAIN
        +
        /XNC * /LBA * /W_R * /RESET * T2 * MAIN
        +
        XNC * /LBA * /RESET * T2 * MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * BHY * /RESET * T2
        +
        /XNC * /LBA * /W_R * BHY * /RESET * T2

T3     := /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
        T2 * MAIN
        +
        /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN

T4     := /XNC * /LBA * W_R * /RESET * T3
        +
        BRDY * /RESET * T4

WE1    := /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * /RESET * T3
        +
        /XNC * /LBA * W_R * /BRDY * /RESET * T4 * MAIN

WE2    := /XNC * /LBA * /W_R * ADS * /RESET * /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * /RESET * T3
        +
        /XNC * /LBA * W_R * /BRDY * /RESET * T4 * MAIN

WINV   := /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
        /MAIN

BADS   := /XNC * /LBA * W_R * /MAT1 * /BHX * /BHY * /RESET *
        T2 * /MAIN
        +
        /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
        T2 * MAIN
        +
        XNC * /LBA * ADS * /BHX * /RESET * /MAIN
        +
        XNC * /LBA * BRDY * /BHX * /RESET * MAIN
        +
        XNC * /LBA * /BHX * BHY * /RESET * /MAIN
        +
        /XNC * /LBA * /W_R * ADS * /BHX * /BHY * /RESET *
        /MAIN
        +
        /XNC * /LBA * /W_R * BRDY * /BHX * /RESET * MAIN
        +
        /XNC * /LBA * /W_R * BRDY * /BHX * BHY * /RESET *
        /MAIN
```

14

```
TITLE           Controller2
PATTERN         N.A.
REVISION        1.1
AUTHOR          Mammad Safai
COMPANY         Integrated Device Technology Inc.
DATE            09-01-1988

CHIP CONTROL_PAL2 PAL22V10

;PINS
;1    2    3    4    5    6    7    8    9    10
CLKB /XNC /LBA /W_R /ADS MAT1 /BRDY BHOLD /LRDY
/RESET
;11  12   13   14   15   16   17   18   19   20
/T2 GND /MAIN BHLDA /DEN /BHY /BHX RGT /OE2 /RDY2
;21   22   23   24   25
/RDY1 SEL WLE VCC GLOBAL

EQUATIONS

GLOBAL.RSTF = RESET

WLE   := /XNC * /LBA * /W_R * ADS * /MAIN * /RESET
       +
       /XNC * /LBA * /W_R * BRDY * MAIN * /RESET

SEL   := /XNC * /LBA * /W_R * ADS * /MAIN * /RESET
       +
       /XNC * /LBA * /W_R * BRDY * MAIN * /RESET
       +
       /BRDY * /RESET * /BHLDA * SEL
       +
       /XNC * /LBA * /W_R * T2 * /RESET * BHY * SEL

RDY1  := /XNC * /LBA * /W_R * ADS * /BRDY * MAIN * /RESET
       * /BHX
       +
       /BRDY * MAIN * /RESET * RDY1
       +
       /XNC * /LBA * /W_R * ADS * /RESET * BHX
       +
       /RESET * BHY * RDY1
       +
       XNC * /LBA * /BRDY * MAIN * /RESET * /BHX
       +
       XNC * /LBA * ADS * /RESET * BHX
       +
       XNC * /LBA * T2 * /RESET * BHY

RDY2  := /XNC * /LBA * /W_R * /MAT1 * T2 * /MAIN * /RESET *
       /BHX * /BHY
       +
       /ADS * /RESET * RDY2

OE2   := /XNC * /LBA * W_R * ADS * MAT1 * /RESET

RGT   := XNC * /LBA * ADS * BRDY * /MAIN * /RESET * /BHX *
       /RGT
       +
       XNC * /LBA * /RESET * /BHX * BHY * /RGT
       +
       XNC * /LBA * BRDY * T2 * MAIN * /RESET * /BHX * /RGT
       +
       LBA * ADS * /RESET * /RGT
       +
       /LBA * /BRDY * /RESET * RGT
       +
       LBA * /LRDY * /RESET * RGT

BHX   := BHOLD * T2 * /MAIN * /RESET * /BHX
       +
       BRDY * BHOLD * T2 * MAIN * /RESET * /BHX
       +
       BHOLD * /RESET * BHX

BHY   := /RESET * BHX

BHLDA := BRDY * BHOLD * /RESET * BHY * /BHLDA
       +
       BHOLD * /RESET * BHLDA

DEN   := /XNC * /LBA * W_R * /MAT1 * T2 * /MAIN * /RESET *
       /BHY * /DEN
       +
       /XNC * /LBA * W_R * /MAT1 * BRDY * MAIN * /RESET
       +
       /LBA * /W_R * ADS * /MAIN * /RESET * /BHX
       +
       /LBA * /W_R * BRDY * MAIN * /RESET * /BHX
       +
       XNC * /LBA * W_R * ADS * /MAIN * /RESET * /BHY *
       /DEN
       +
       XNC * /LBA * W_R * BRDY * MAIN * /RESET
       +
       /BRDY * /RESET * DEN
       +
       /W_R * /LBA * BRDY * /MAIN * /RESET * /BHX * BHY *
       /DEN
       +
       XNC * /LBA * BRDY * /MAIN * /RESET * /BHX * BHY *
       /DEN
```

```
TITLE           Controller3
PATTERN         N.A.
REVISION        1.0
AUTHOR          Mammad Safai
COMPANY         Integrated Device Technology Inc.
DATE            09-28-1988

CHIP CONTROL_PAL3 PAL22V10

;PINS
;1    2      3      4      5      6      7      8   9   10
CLKB /RESET BHLDA /BW_R /BADS MAT2 /FLUSH NC  NC
NC
;11  12    13    14    15    16    17    18    19    20
NC  GND   NC    NC    NC    NC    NC    NC    NC    NC
;21     22     23     24     25
/CLR  /CLR2  /CLR1  VCC   GLOBAL

EQUATIONS

GLOBAL.RSTF  = RESET

CLR1  :=      /RESET * BHLDA * /BW_R * BADS

CLR2  :=      /RESET * MAT2 * CLR1

CLR   :=      /RESET * MAT2 * CLR1
            +
              /RESET * CLR2
            +
              /RESET * FLUSH
            +
              RESET
```

CONCLUSION

The design of cache based microprocessor systems is optimized by the use of a cache controller based on a dual cache tag scheme. Such an architecture is adaptable to present day 25MHz systems as well is easily adapted to future higher speed microprocessors. Posted writes further improves the effective cycle time (with the IDT74FCT646s).

At the heart of this design is the IDT7174 cache tag SRAM. This device with an address to match time of 20ns gives a wide margin for the two cycle 80386 operating at 25MHz. Faster microprocessor can be easily accommodated without changes to this design.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = \text{to exp}\left[\frac{Ea}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

t_A = lifetime at elevated junction (T_J) temperature
t_O = normal lifetime at normal junction (T_O) temperature
Ea = activation energy (ev)
k = Boltzmann's constant (8.617×10^{-5} ev/k)

I.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883C to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelope (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degrees celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$

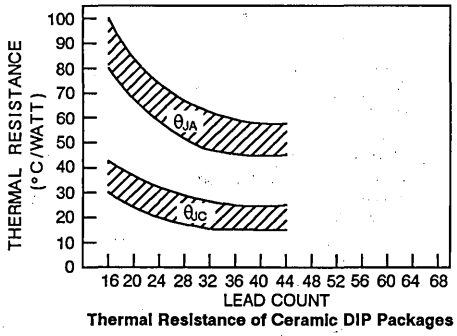
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JA} + \theta_{CA}]$$

where

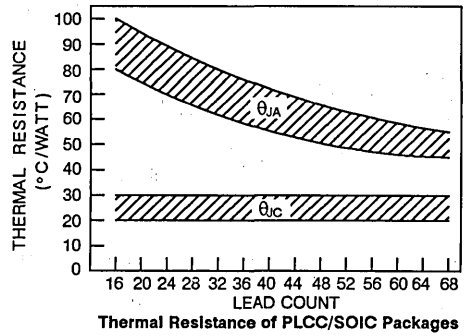
$$\frac{\theta_{JC} = T_J - T_C}{P} \qquad \frac{\theta_{CA} = T_C - T_A}{P}$$

θ = Thermal resistance, junction to reference point
J = Junction
P = Operational power of device (dissipated)
T_A = Ambient temperature in degrees celsius (normally +70°C)
T_J = Junction temperature of integrated device
T_C = Temperature of case/package
θ_{CA} = **Case to Ambient,** thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC} = **Junction to Case,** thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on package material properties and package geometry.)
θ_{JA} = **Junction to Ambient,** thermal resistance—usually measured with respect to the temperature of a specified volume of Still Air. (Dependent on $\theta_{JC} + \theta_{JA}$ which includes the influence of area and environmental condition.)

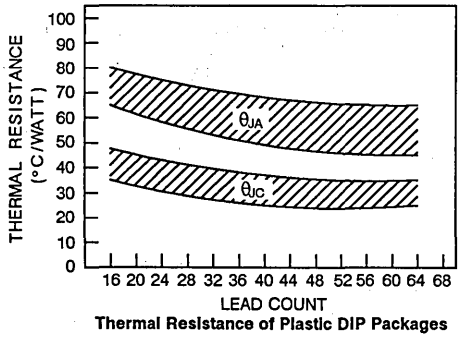
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30-86, G32-86.



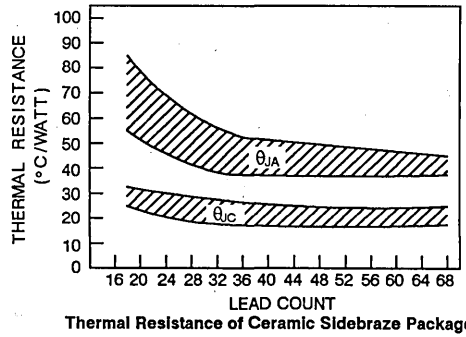
Thermal Resistance of Ceramic DIP Packages



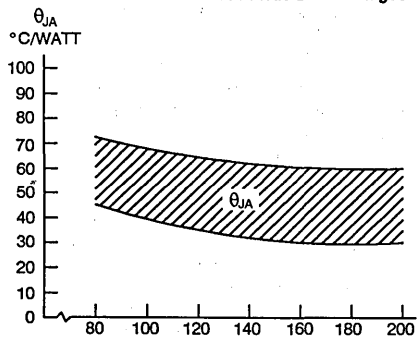
Thermal Resistance of PLCC/SOIC Packages



Thermal Resistance of Plastic DIP Packages

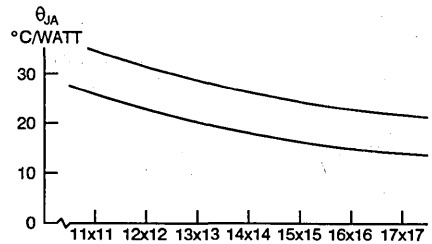


Thermal Resistance of Ceramic Sidebraze Packages

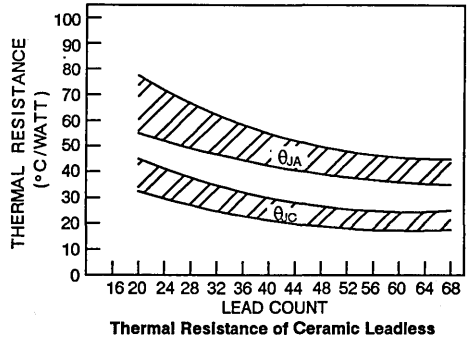


PPGA Packages

Package Laminate Material: Hi Temp. Epoxy or Triazine (BT)



PGA Thermal Resistance



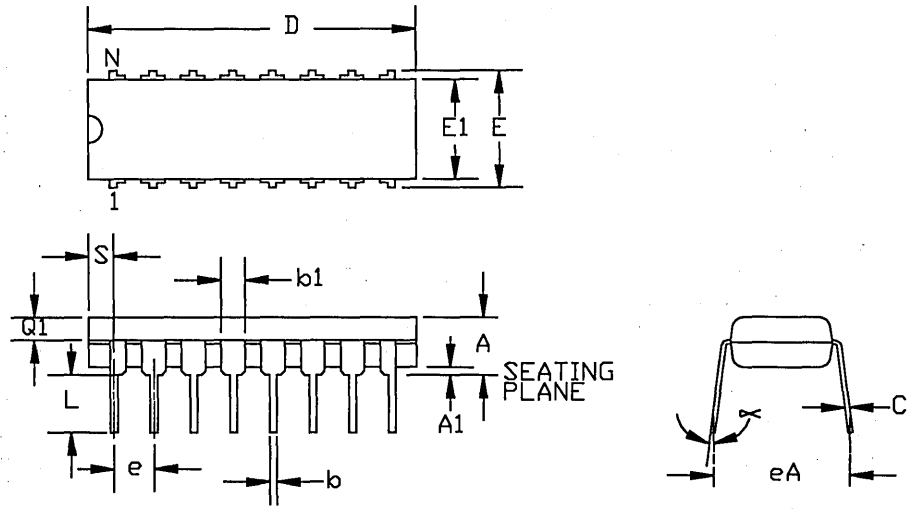
Thermal Resistance of Ceramic Leadless Chip Carrier (LCC) Packages

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINE INDEX

MODULE PACKAGING

PLASTIC DUAL IN-LINE PACKAGES



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

[3] D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

16-28 PIN PLASTIC DIP (300 MIL)

DWG # / # OF PINS (N)	P16-1 16 (300 MIL)		P18-1 18 (300 MIL)		P20-1 20 (300 MIL)		P22-1 22 (300 MIL)		P24-1 24 (300 MIL)		P28-2 28 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.140	.165	.145	.165	.145	.165	.145	.165	.145	.170
A1	.015	.035	.015	.035	.015	.035	.015	.035	.015	.035	.015	.030
b	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.070	.050	.065	.050	.065	.045	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.745	.760	.885	.910	1.022	1.040	1.050	1.060	1.240	1.255	1.345	1.360
E	.300	.325	.300	.325	.300	.325	.300	.320	.300	.320	.300	.325
E1	.247	.260	.247	.260	.240	.280	.240	.270	.250	.275	.270	.290
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150	.120	.150	.120	.150	.120	.150
∝	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.040	.060	.025	.070	.020	.040	.055	.075	.020	.040
Q1	.050	.070	.050	.070	.055	.075	.055	.075	.055	.070	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)

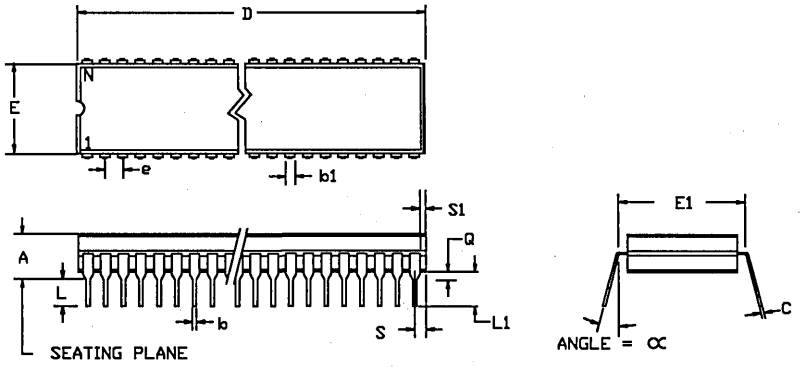
24–48 PIN PLASTIC DIP (600 MIL)

DWG # / # OF PINS (N)	P24–2 24 (600 MIL)		P28–1 28 (600 MIL)		P32–1 32 (600 MIL)		P40–1 40 (600 MIL)		P48–1 48 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
∝	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.065	.075	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.070	.080	.060	.080	.060	.080

64 PIN PLASTIC DIP (900 MIL)

DWG # / # OF PINS (N)	P64–1 64 (900 MIL)	
	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
∝	0°	15°
S	.045	.065
Q1	.080	.090

DUAL IN-LINE PACKAGES



NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.
[3] THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16-28 PIN CERDIP (300 MIL)

DWG # / # OF LEADS (N)	D16-1 16 (300 MIL)		D18-1 18 (300 MIL)		D20-1 20 (300 MIL)		D22-1 22 (300 MIL)		D24-1 24 (300 MIL)		D28-3 28 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.016	.020	.014	.023	.014	.023	.014	.023	.014	.023	.014	.023
b1	.045	.065	.038	.065	.038	.065	.038	.065	.038	.065	.038	.065
C	.009	.013	.009	.014	.009	.014	.009	.014	.009	.014	.009	.014
D	.750	.830	.880	.940	.935	1.060	1.050	1.180	1.240	1.280	1.440	1.490
E	.240	.310	.220	.310	.220	.310	.220	.310	.220	.310	.220	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150		.150		.150		.150		.150		.150	
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005		.005		.005		.005		.005		.005	
ANGLE (DEG)	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24–40 PIN CERDIP (600 MIL)

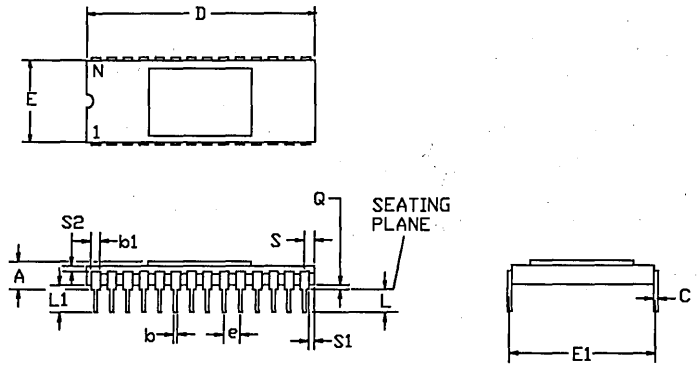
DWG # / # OF LEADS (N)	D24–2 24 (600 MIL)		D28–1 28 (600 MIL)		D40–1 40 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.160	.220
b	.014	.023	.015	.020	.015	.020
b1	.038	.065	.045	.060	.045	.060
C	.008	.015	.008	.013	.008	.012
D	1.230	1.290	1.440	1.490	2.020	2.070
E	.500	.560	.510	.545	.510	.545
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150		.150		.150	
Q	.015	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005		.005		.005	
∝	0°	15°	0°	15°	0°	15°

28–40 PIN CERDIP (WIDE BODY)

DWG # / # OF LEADS (N)	D28–2 28 (WIDE BODY)		D32–1 32 (WIDE BODY)		D40–2 40 (WIDE BODY)	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.015	.020	.015	.020	.015	.020
b1	.045	.060	.038	.065	.045	.060
C	.008	.013	.008	.015	.008	.012
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150		.150		.150	
Q	.020	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005		.005		.005	
∝	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-28 PIN SIDEBRAZE (300 MIL)

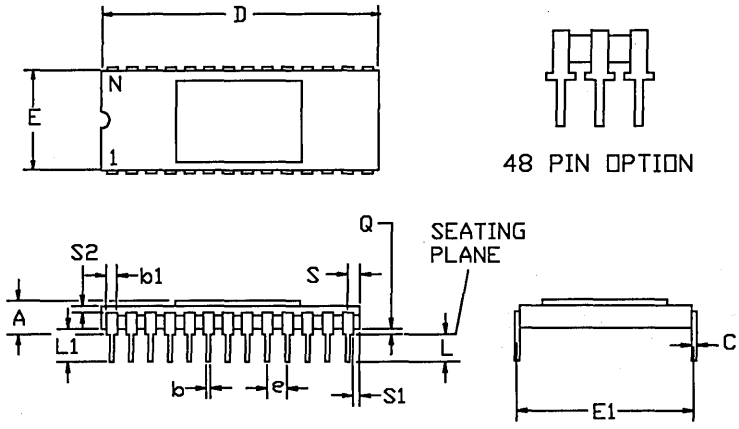


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1	
# OF LEADS (N)	20 (300 MIL)		22 (300 MIL)		24 (300 MIL)		28 (300 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.100	.200	.100	.200	.100	.200	.100	.200
b	.014	.023	.014	.023	.014	.023	.014	.023
b1	.038	.060	.030	.060	.038	.060	.030	.060
C	.008	.015	.008	.015	.008	.015	.008	.015
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420
E	.220	.310	.260	.310	.220	.310	.220	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200
L1	.150		.150		.150		.150	
Q	.015	.060	.015	.060	.015	.060	.015	.060
S	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005		.005		.005		.005	
S2	.005		.005		.005		.005	

DUAL IN-LINE PACKAGES (Continued)

28–48 PIN SIDEBRAZE (400 MIL)

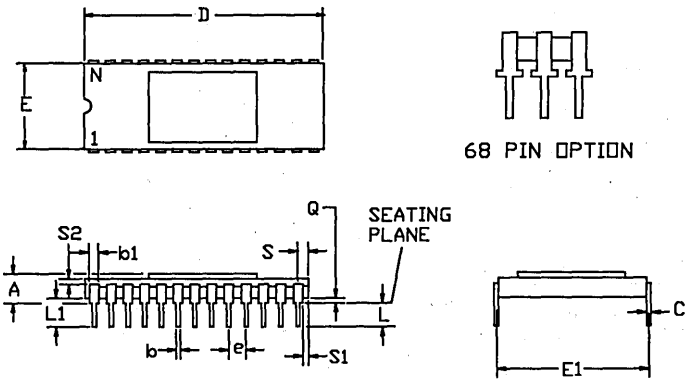


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LEADS (N)	28 (400 MIL)		32 (400 MIL)		48 (400 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.030	.060	.030	.060	.030	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150		.150		.150	
Q	.030	.060	.030	.060	.030	.060
S	.030	.065	.030	.065	.030	.065
S1	.005		.005		.005	
S2	.005		.005		.005	

DUAL IN-LINE PACKAGES (Continued)

24-68 PIN SIDEBRAZE (600 MIL)

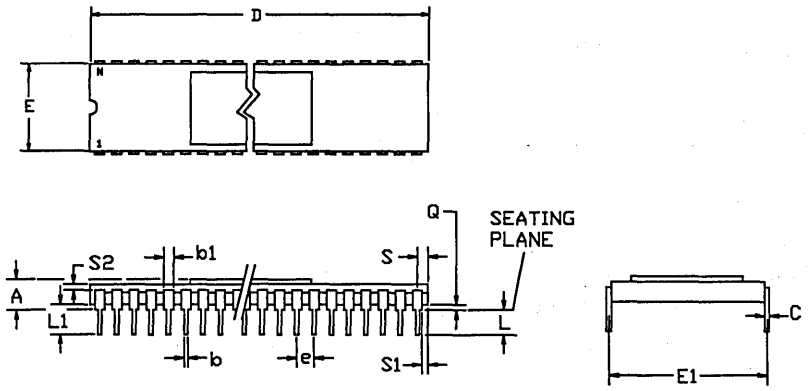


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LEADS (N)	24 (600 MIL)		28 (600 MIL)		32 (600 MIL)		40 (600 MIL)		48 (600 MIL)		68 (600 MIL)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.100	.190	.100	.190	.100	.190	.100	.190	.100	.190	.100	.190
b	.015	.022	.015	.022	.015	.022	.015	.022	.015	.022	.015	.022
b1	.040	.060	.040	.060	.040	.060	.040	.060	.040	.060	.040	.060
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.180	1.230	1.380	1.420	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.590	.620	.590	.620	.590	.620	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150		.150		.150		.150		.150		.150	
Q	.030	.060	.030	.060	.030	.060	.030	.060	.030	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005		.005		.005		.005		.005		.005	
S2	.010		.010		.010		.010		.005		.005	

DUAL IN-LINE PACKAGES (Continued)

64 PIN SIDEBRAZE (900 MIL)



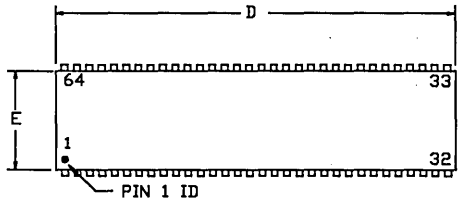
NOTES
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

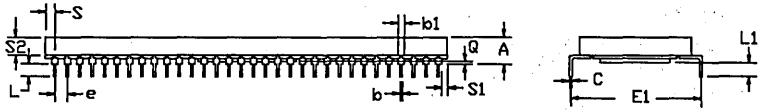
DWG #	C64-1	
# OF LEADS (N)	64 (900 MIL)	
	MIN	MAX
A	.110	.190
b	.014	.023
b1	.030	.060
C	.008	.015
D	3.160	3.230
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.175
L1	.150	
Q	.030	.060
S	.030	.065
S1	.005	
S2	.005	

15

DUAL IN-LINE PACKAGES (Continued)

64 PIN TOPBRAZE (900 MIL)



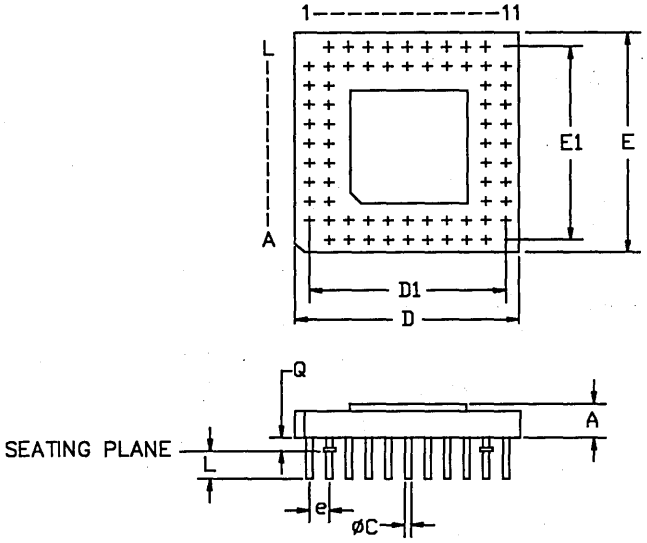


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # # OF LEADS (N)	C64-2 64 (900 MIL)	
	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.165	3.235
E	.785	.815
E1	.885	.915
e	.100 BSC	
L	.125	.175
L1	.150	
Q	.030	.060
S	.030	.065
S1	.005	
S2	.005	

PLASTIC PIN GRID ARRAY

68–208 PIN PGA (CAVITY UP)



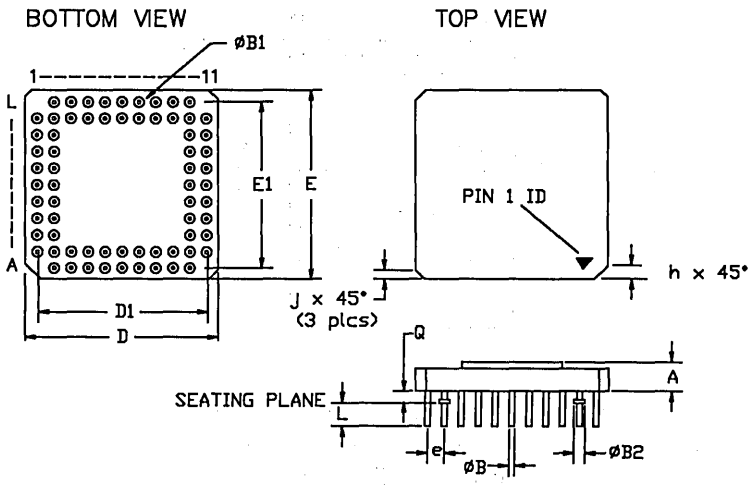
NOTES:

1. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
2. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
3. DIM "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
4. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
5. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68–2		PG 84–2		PG 208–2	
# OF PINS (N)	68 PIN		84 PIN		208 PIN	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.115	.160	.115	.160	.115	.160
C	.016	.020	.016	.020	.016	.020
D	1.140	1.180	1.140	1.180	1.740	1.780
D1	1.000 BSC		1.000 BSC		1.600 BSC	
E	1.140	1.180	1.140	1.180	1.740	1.780
E1	1.000 BSC		1.000 BSC		1.600 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.160	.100	.160	.100	.160
M	11		11		17	
Q	.040	.070	.040	.070	.040	.070

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

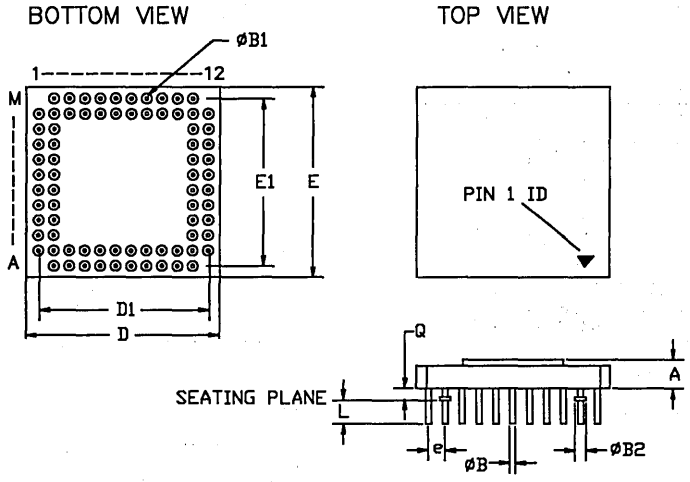


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG #	G68-1	
NO. OF LEADS	68-LEADS	
	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1		.080
ØB2	.040	.060
D	1.140	1.180
D1	1.000 BSC	
E	1.140	1.180
E1	1.000 BSC	
e	.100 BSC	
h	.055	.085
J	.015	.025
L	.120	.140
N	68	
Q	.040	.060
M	11	

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP)



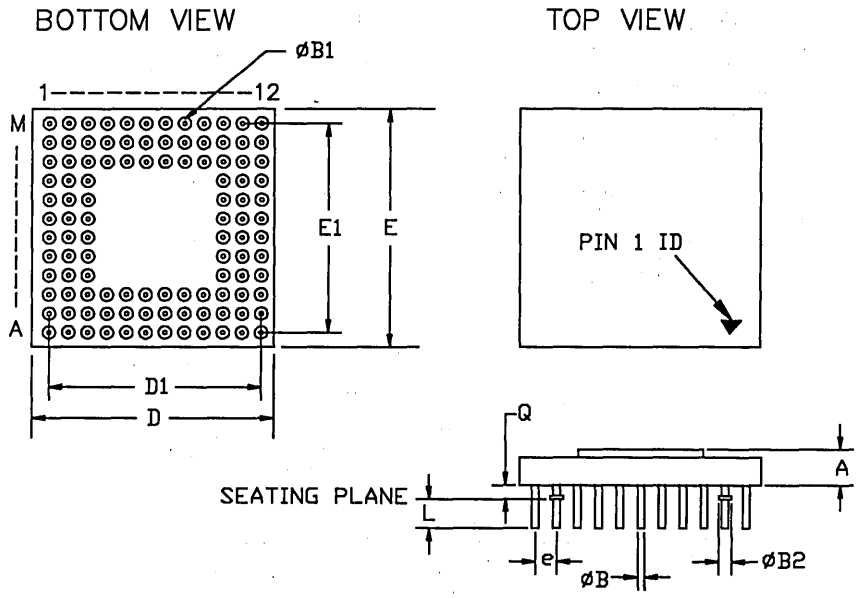
NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G84-1 84-LEADS	
	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D	1.180	1.235
D1	1.100 BSC	
E	1.180	1.235
E1	1.100 BSC	
e	.100 BSC	
h		
J		
L	.120	.140
N	84	
Q	.040	.060
M	12	

15

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

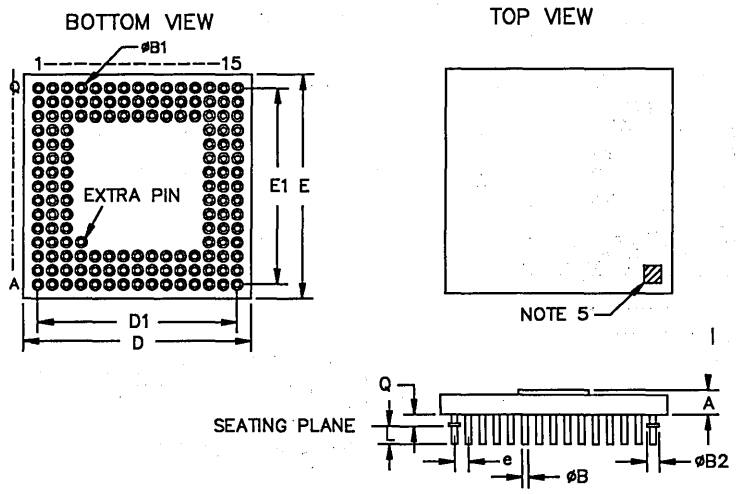


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G108-1 108-LEADS	
	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1		.080
ØB2	.040	.060
D	1.188	1.212
D1	1.100 BSC	
E	1.188	1.212
E1	1.100 BSC	
e	.100 BSC	
h		
J		
L	.120	.140
N	108	
Q	.040	.060
M	12	

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP)

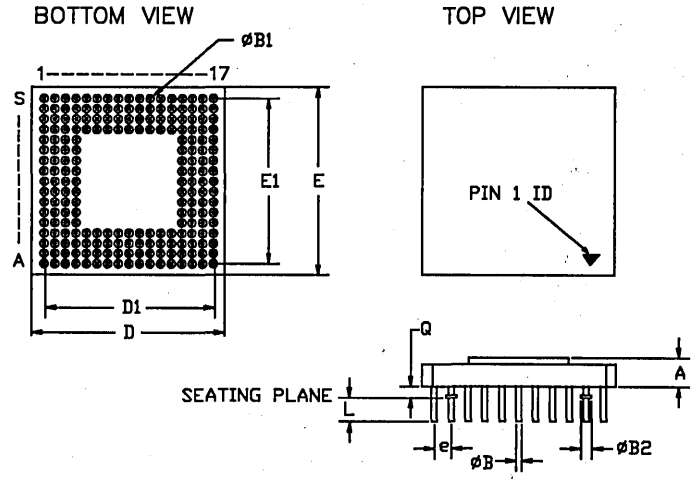


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
[5] INDEX MARK INDICATES APPROX LOCATION.
[6] EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

DWG # G144–2 NO. OF LEADS 144–LEADS	MIN	MAX
A	.082	.125
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D	1.559	.1590
D1	1.400 BSC	
E	1.559	1.590
E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
(NOTE 6) N	145	
Q	.040	.060
M	15	

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY UP)

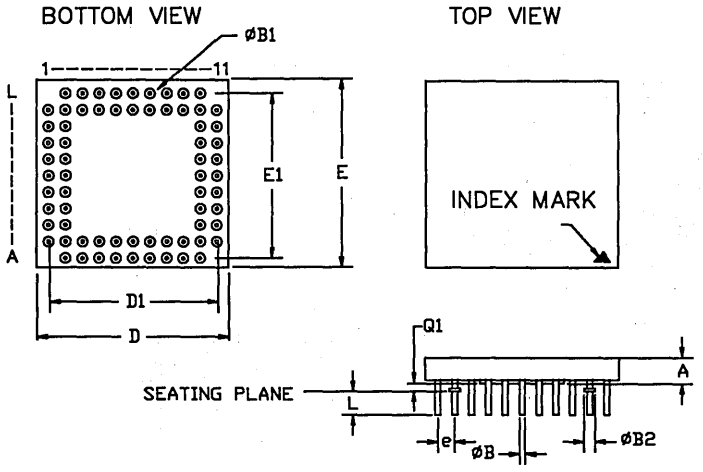


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G208-1 208-LEADS	
	MIN	MAX
A	.070	.145
øB	.016	.020
øB1		.080
øB2	.040	.060
D	1.732	1.780
D1	1.600 BSC	
E	1.732	1.780
E1	1.600 BSC	
e	.100 BSC	
h		
J		
L	.125	.140
N	208	
Q	.040	.060
M	17	

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

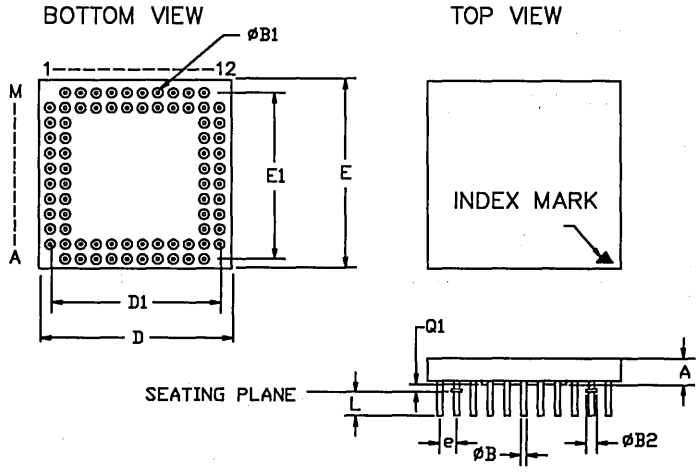


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G68-2 68-LEADS	
	MIN	MAX
A	.077	.095
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D	1.098	1.122
D1	1.000 BSC	
E	1.098	1.122
E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
N	68	
Q1	.025	.060
M	11	

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN)

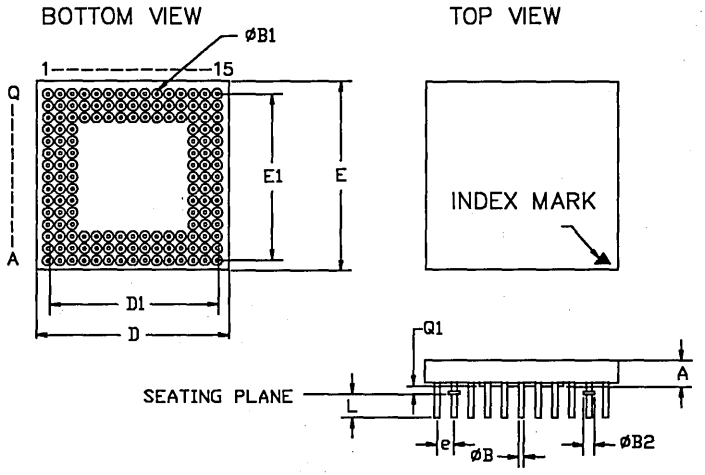


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G84-2 84-LEADS	
	MIN	MAX
A	.077	.095
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D	1.180	1.235
D1	1.100 BSC	
E	1.180	1.235
E1	1.100 BSC	
e	.100 BSC	
L	.100	.140
N	84	
Q1	.025	.060
M	12	

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

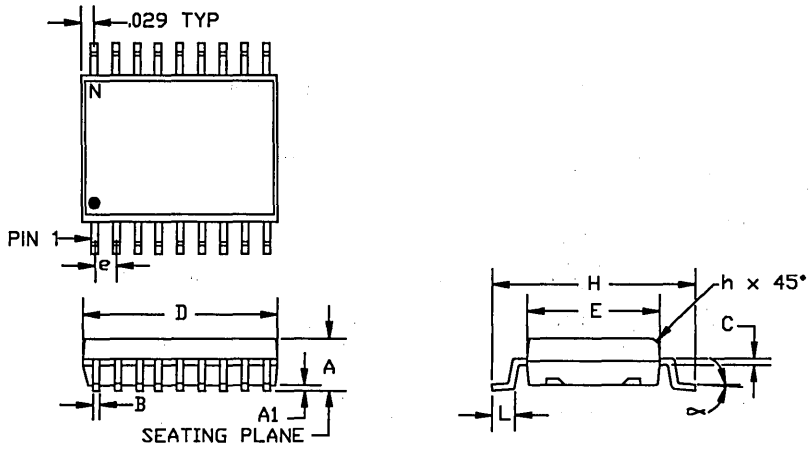


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
[4] SYMBOL "N" REPRESENTS THE NUMBER OF PINS.

DWG # NO. OF LEADS	G144-1 144-LEADS	
	MIN	MAX
A	.082	.100
øB	.016	.022
øB1	.060	.080
øB2	.040	.060
D	1.559	1.590
D1	1.400 BSC	
E	1.559	1.590
E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
N	144	
Q1	.025	.060
M	15	

SMALL OUTLINE IC

16–28 PIN SMALL OUTLINE (GULL WING)

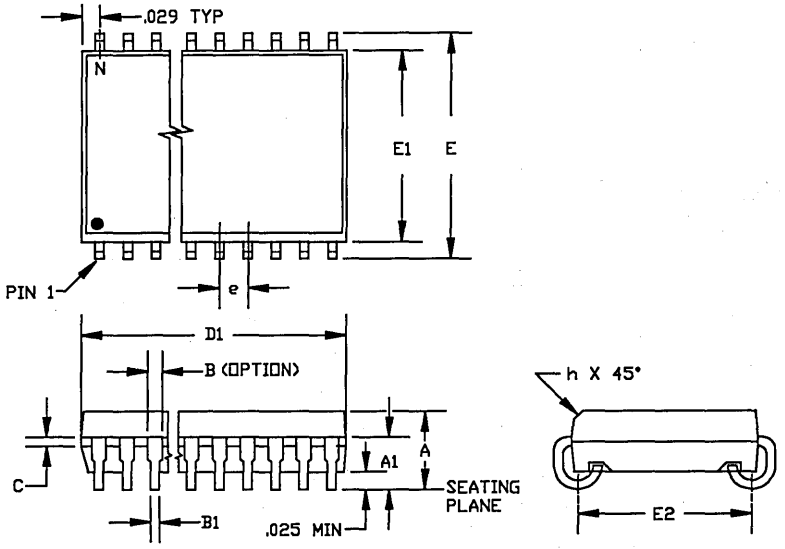


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

DWG #	SO16-1		SO18-1		SO20-2		SO24-2		SO24-3		SO28-2		SO28-3	
# OF LDS (N)	16 LD		18 LD		20 LD		24 LD		24 LD		28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043	.110	.120	.095	.1043	.110	.120
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.014
B	.014	.020	.014	.020	.014	.020	.014	.020	.014	.018	.014	.020	.014	.019
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.006	.010
D	.403	.413	.447	.462	.497	.511	.600	.614	.620	.630	.700	.712	.718	.728
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.340	.350
h	.010	.020	.010	.020	.010	.020	.010	.020	.012	.020	.010	.020	.012	.020
H	.400	.419	.400	.419	.400	.419	.400	.419	.406	.419	.400	.419	.462	.478
L	.018	.045	.018	.045	.018	.045	.018	.045	.028	.045	.018	.045	.028	.045
∝	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)

20–28 PIN SMALL OUTLINE (J–BEND)

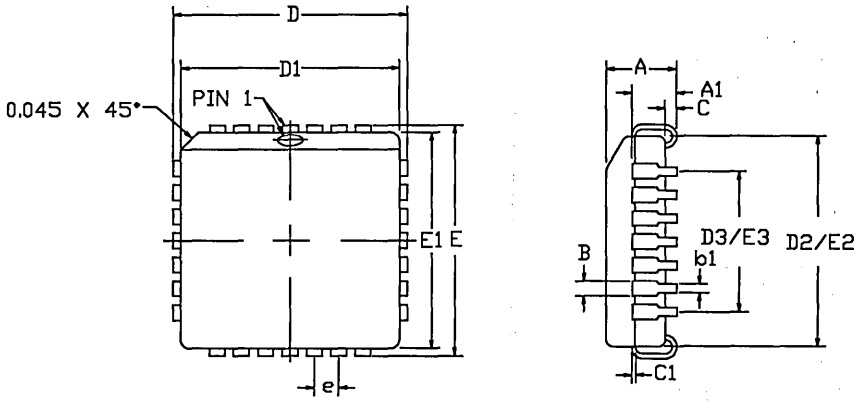


NOTES:
1. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
3. D1 & E1 INCLUDE MOLD MISMATCH & ARE DETERMINED AT THE PARTING LINE.

DWG #	SO20–1		SO24–4		SO28–4	
# OF LDS (N)	20 LD (.300")		24 LD (.300")		28 LD (.350")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.130	.148
A1	.090	.094	.082	.095	.082	.095
B	.026	.030	.026	.032	.026	.032
B1	.014	.020	.015	.020	.016	.020
C	.007	.011	.007	.011	.007	.011
D1	.500	.512	.620	.630	.720	.730
E	.336	.347	.335	.345	.380	.390
E1	.292	.299	.295	.305	.345	.355
E2	.262	.272	.260	.280	.310	.330
e	.050 BSC		.050 BSC		.050 BSC	
h	.010 R		.012	.020	.012	.020

PLASTIC LEADED CHIP CARRIERS

20–84 PIN PLCC



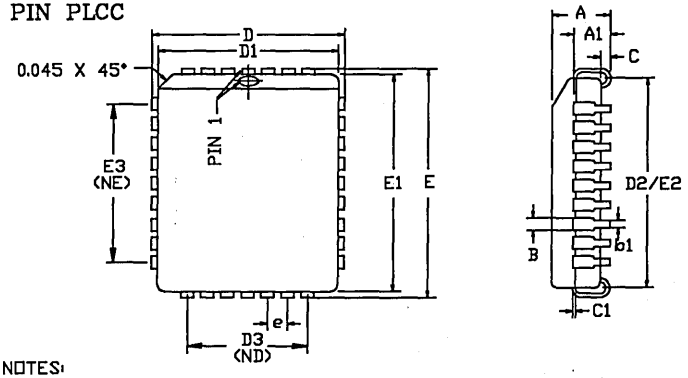
NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
[5] ND & NE = # LEADS IN D & E DIRECTIONS

DWG #	J20-1		J28-1		J44-1		J52-1		J68-1		J84-1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200	REF	.300	REF	.500	REF	.600	REF	.800	REF	1.000	REF
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC	.050	BSC
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

32 PIN PLCC



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

[3] D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

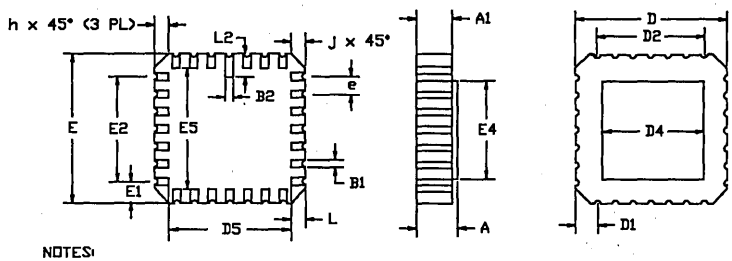
[4] FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

[5] ND & NE = # LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	J32-1	
# OF LDS	32 LD	
SYMBOL	MIN	MAX
A	.120	.140
A1	.075	.095
B	.026	.032
b1	.013	.021
C	.015	.040
C1	.008	.012
D	.485	.495
D1	.449	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.549	.553
E2	.490	.530
E3	.400	REF
e	.050	BSC
ND/NE	7 / 9	

LEADLESS CHIP CARRIERS

20–44 PIN LCC (SQUARE)



NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.
[3] ND=NE – NUMBER OF LEADS PER SIDE.

DWG # / # OF PINS (N)	L20–2 20		L28–1 28		L44–1 44	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120
A1	.054	.066	.054	.077	.054	.088
B1	.022	.028	.022	.028	.022	.028
B2	.022	.041	.022	.041	.022	.041
D	.342	.358	.442	.458	.640	.660
D1	.075 REF		.075 REF		.075 REF	
D2	.200 BSC		.300 BSC		.500 BSC	
D4		.358		.458		.560
D5	.250 REF		.350 REF		.550 REF	
E	.342	.358	.442	.458	.640	.660
E1	.075 REF		.075 REF		.075 REF	
E2	.200 BSC		.300 BSC		.500 BSC	
E4		.358		.458		.560
E5	.250 REF		.350 REF		.550 REF	
e	.050 BSC		.050 BSC		.050 BSC	
h	.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055
L2	.077	.093	.077	.093	.077	.093
N	20		28		44	
ND	5		7		11	

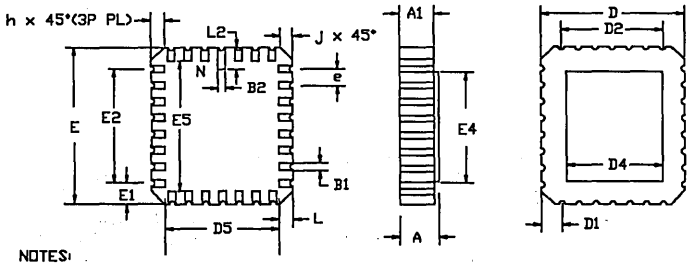
LEADLESS CHIP CARRIERS (Continued)

48–68 PIN LCC (SQUARE)

DWG # / # OF LEADS (N)	L48–1 48 (.040")		L52–1 52		L68–2 68		L68–1 68 (.025")	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.120	.061	.087	.082	.098	.065	.098
A1	.045	.090	.051	.077	.072	.088	.055	.075
B1	.017	.023	.022	.028	.022	.028	.010	.014
B2	.017	.033	.022	.041	.022	.055	.008	.024
D	.554	.572	.739	.761	.938	.962	.554	.566
D1	.060 REF		.075 REF		.075 REF		.080 REF	
D2	.440 BSC		.600 BSC		.800 BSC		.400 BSC	
D4		.546		.661		.862		.535
D5	.480 REF		.650 REF		.850 REF		.430 REF	
E	.554	.572	.739	.761	.938	.962	.554	.566
E1	.060 REF		.075 REF		.075 REF		.080 REF	
E2	.440 BSC		.600 BSC		.800 BSC		.400 BSC	
E4		.546		.661		.862		.535
E5	.480 REF		.650 REF		.850 REF		.430 REF	
e	.040 BSC		.050 BSC		.050 BSC		.025 BSC	
h	.012 RADIUS		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.033	.047	.045	.055	.045	.055	.045	.055
L2	.077	.093	.077	.093	.077	.093	.077	.093
N	48		52		68		68	
ND	12		13		17		17	

LEADLESS CHIP CARRIERS (Continued)

20–24 PIN LCC (RECTANGULAR)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

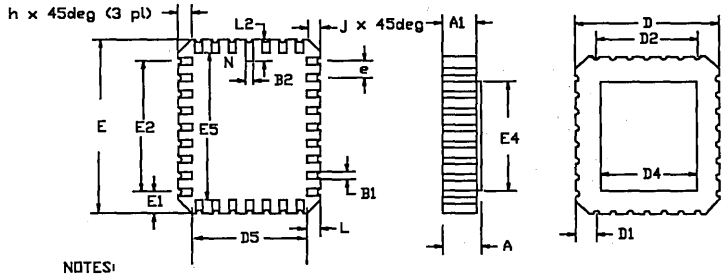
[3] ND = # LEADS ON 'D' SIDE

[4] NE = # LEADS ON 'E' SIDE

DWG #	L20-1		L22-1		L24-1	
# OF PINS (N)	20		22		24	
	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.075	.064	.100	.064	.100
A1	.050	.065	.054	.063	.054	.066
B1	.022	.028	.022	.028	.022	.028
B2	.022	.041	.022	.041	.022	.041
D	.284	.296	.284	.296	.292	.308
D1	.075 REF		.070 REF		.050 REF	
D2	.150 BSC		.150 BSC		.200 BSC	
D4		.280		.280		.308
D5	.200 REF		.200 REF		.210 REF	
E	.420	.431	.480	.496	.392	.408
E1	.085 REF		.095 REF		.050 REF	
E2	.250 BSC		.300 BSC		.300 BSC	
E4		.410		.480		.408
E5	.335 REF		.400 REF		.310 REF	
e	.050 BSC		.050 BSC		.050 BSC	
h	.012 RADIUS		.012 RADIUS		.025 REF	
J	.012 RADIUS		.012 RADIUS		.015 REF	
L	.045	.051	.039	.051	.045	.055
L2	.083	.095	.083	.097	.077	.093
N	20		22		24	
ND	4		4		5	
NE	6		7		7	

LEADLESS CHIP CARRIERS (Continued)

28–32 PIN LCC (RECTANGULAR)



NOTES:

[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

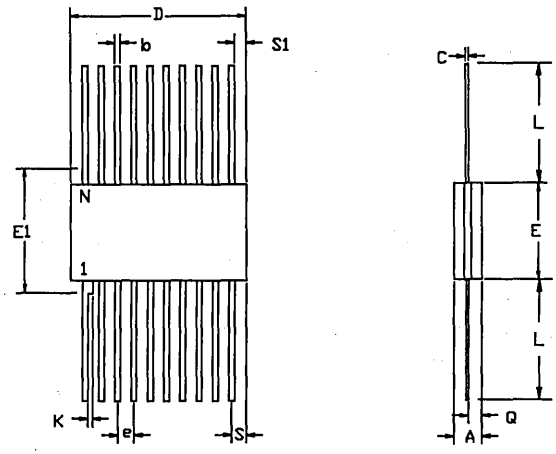
[3] ND = # LEADS ON 'D' SIDE

[4] NE = # LEADS ON 'E' SIDE

DWG #	L28-2		L32-1	
# OF LEADS (N)	28		32	
	MIN	MAX	MIN	MAX
A	.060	.120	.060	.120
A1	.050	.088	.050	.088
B1	.022	.028	.022	.028
B2	.022	.041	.022	.041
D	.342	.358	.442	.458
D1	.075 REF		.075 REF	
D2	.200 BSC		.300 BSC	
D4		.358		.458
D5	.250 REF		.350 REF	
E	.540	.560	.540	.560
E1	.075 REF		.075 REF	
E2	.400 BSC		.400 BSC	
E4		.558		.558
E5	.450 REF		.450 REF	
e	.050 BSC		.050 BSC	
h	.040 REF		.040 REF	
J	.020 REF		.020 REF	
L	.045	.055	.045	.055
L2	.077	.093	.077	.093
N	28		32	
ND	5		7	
NE	9		9	

CERPACKS

16–28 LEAD CERPACK



NOTES:

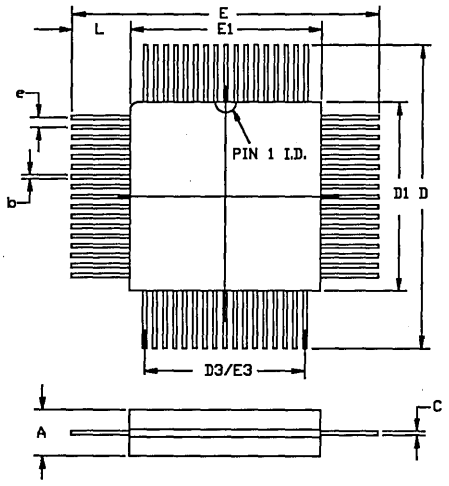
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	E16–1 16 LEADS		E20–1 20–LEADS		E24–1 24–LEADS		E28–1 28–LEADS		E28–2 28–LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006	.003	.009	.003	.006
D		.440		.540		.640		.740		.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1		.305		.305		.440		.550		.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S		.045		.045		.045		.045		.045
S1	.005		.005		.005		.000		.005	

CERQUADS

68 LEAD (STRAIGHT LEADS)

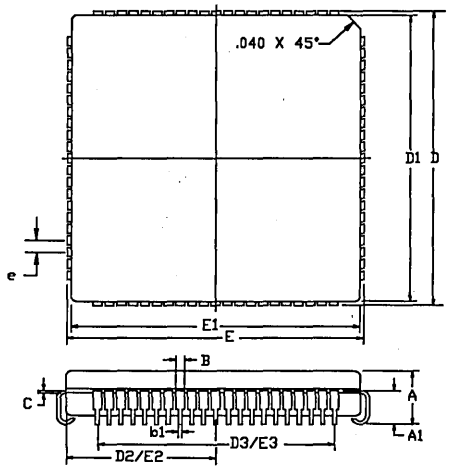


[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.
[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # No. OF LD	CQ68-1 68 LD	
	MIN	MAX
A	.120	.140
b	.008	.013
C	.0045	.008
D	.922	1.080
D1	.460	.500
D3	.400 REF	
e	.025 BSC	
E	.922	1.080
E1	.460	.500
E3	.400 REF	
L	.200	.300

CERQUADS (Continued)

84 LD (J-BEND)

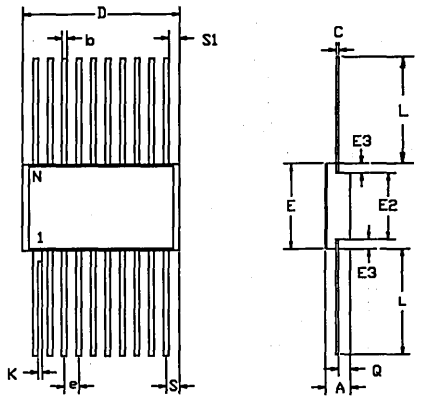


NOTES:
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
[2] BSC - BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	CQ84-1 84 -LEADS	
	MIN	MAX
A	.155	.200
A1	.090	.120
B	.026	.032
b1	.017	.021
C	.006	.010
D / E	1.170	1.180
D1 / E1	1.138	1.162
D2 / E2	.548	.568
D3 / E3	1.000 REF	
e	.050 BSC	
N	84	

FLATPACKS

20–28 LEAD FLATPACK



NOTES:

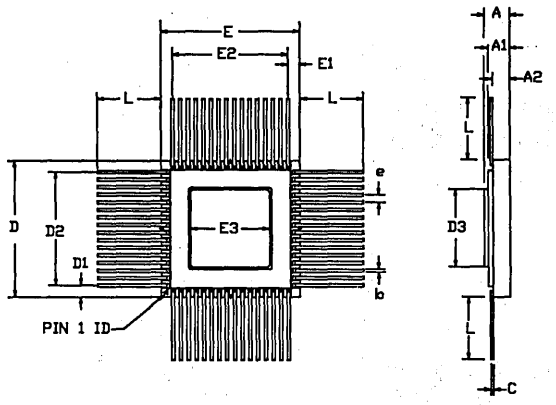
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

DWG # / # OF LEADS (N)	F20–1 20–LEADS		F20–2 20–LEADS (.295 BODY)		F24–1 24–LEADS		F28–1 28–LEADS		F28–2 28–LEADS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.007	.003	.006	.003	.007	.004	.007	.003	.009
D		.490		.490		.640	.710	.740		.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.460	.520
E2	.130		.130		.180		.180		.180	
E3	.030		.030		.030		.040		.030	
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015					.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.040	.026	.045
S		.045		.045		.045		.045		.045
S1	.005		.005		.005		.005		.000	

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK



NOTES:

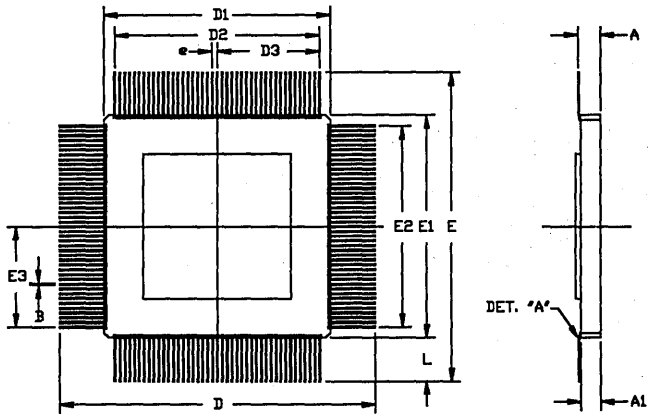
[1] ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE STATED.

[2] BSC – BASIC PIN SPACING BETWEEN CENTERS.

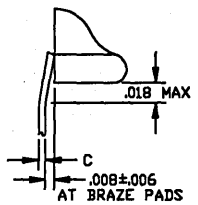
DWG # / # OF LEADS (N)	F48–1 48–LEADS		F64–1 64–LEADS	
	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D		.750	.885	.915
D1	.100 REF		.075 REF	
D2	.550 BSC		.750 BSC	
D3		.630	.505	.535
e	.050 BSC		.050 BSC	
E		.750	.885	.915
E1	.100 REF		.075 REF	
E2	.550 BSC		.750 BSC	
E3		.630	.505	.535
L	.350	.450	.350	.450
ND	12		16	
NE	12		16	

FLATPACKS (Continued)

172 LEAD QUAD FLATPACK

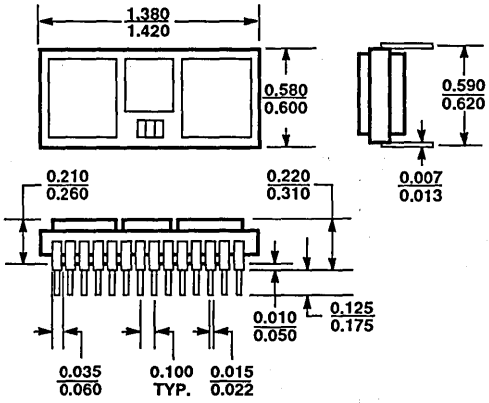


DWG # / # OF LEADS	F172-1 172-LEADS	
	MIN	MAX
A		.130
A1		.105
B	.006	.010
C	.004	.008
D / E	1.580	1.620
D1 / E1	1.135	1.165
D2 / E2	1.050 BSC	
D3 / E3	.525 BSC	
e	.025 BSC	
L	.220	.230
N	172	
ND	43	

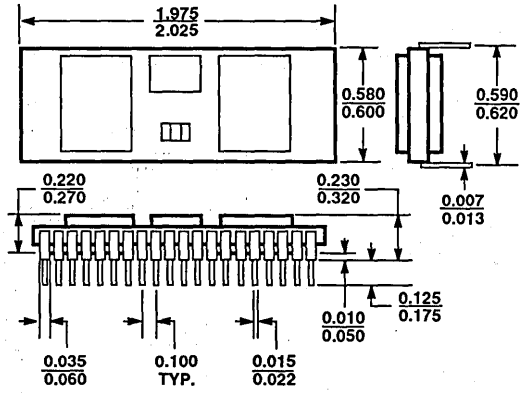


DETAIL A

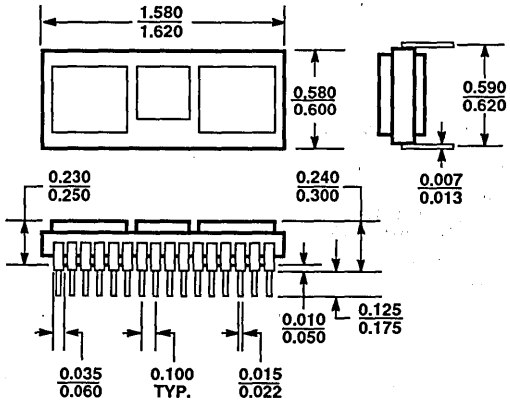
(M1) 28-PIN SIDEBRAZE DIP



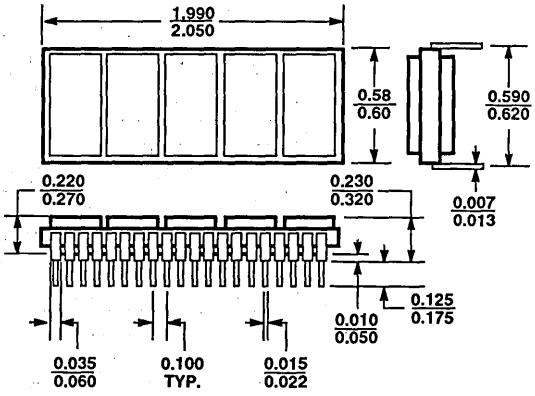
(M4) 40-PIN SIDEBRAZE DIP



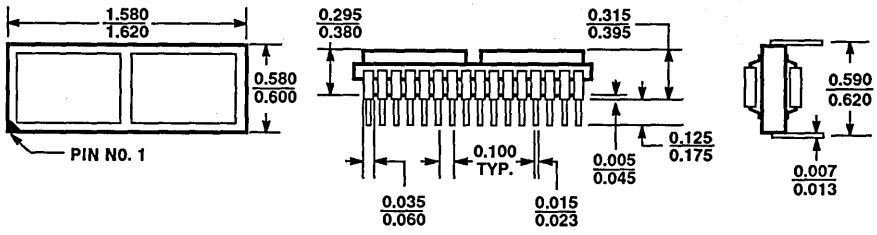
(M2) 32-PIN SIDEBRAZE DIP



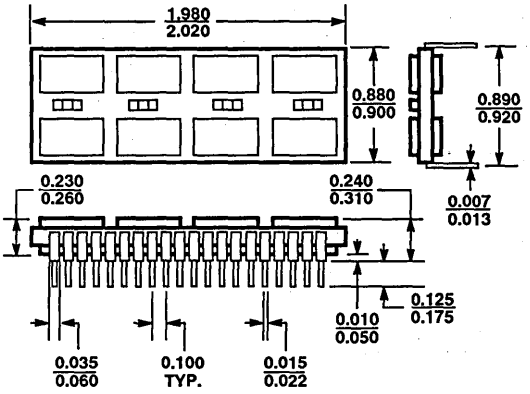
(M5) 40-PIN SIDEBRAZE DIP



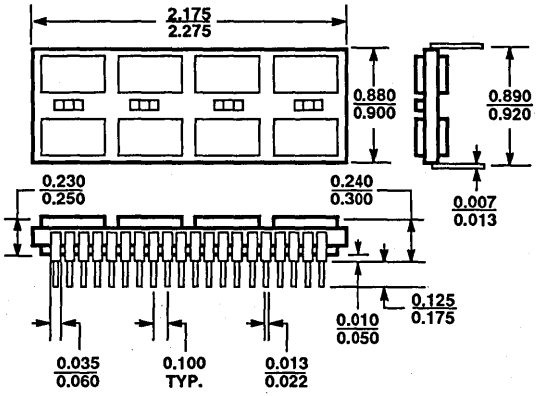
(M3) 32-PIN SIDEBRAZE DIP



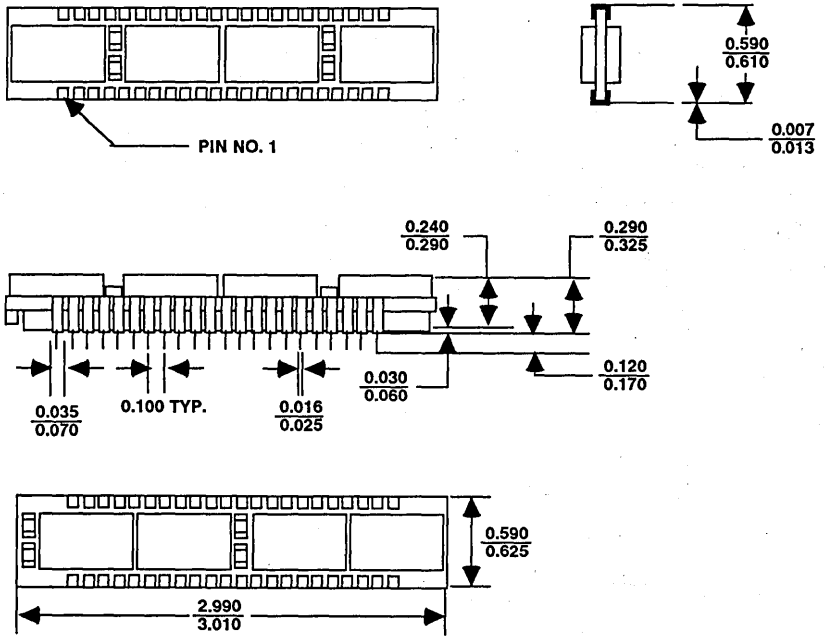
(M6) 40-PIN SIDEBRAZE DIP



(M7) 40-PIN SIDEBRAZE DIP

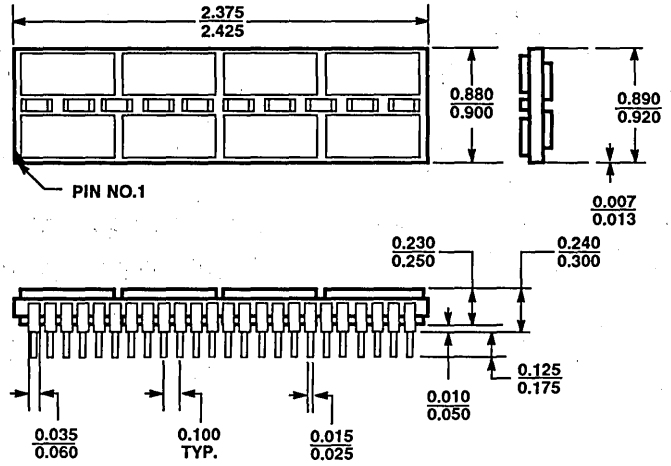


(M8) 44-PIN FR-4 DIP

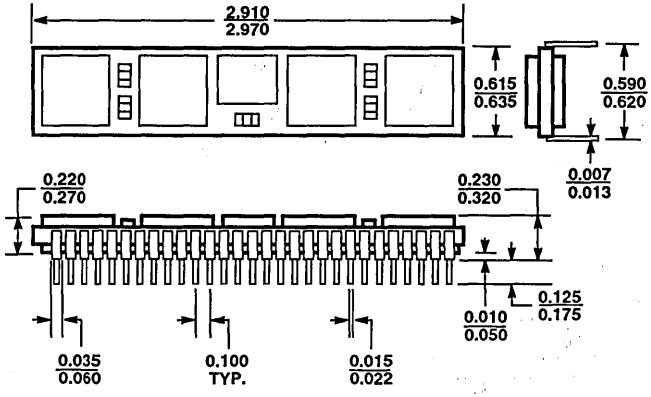


15

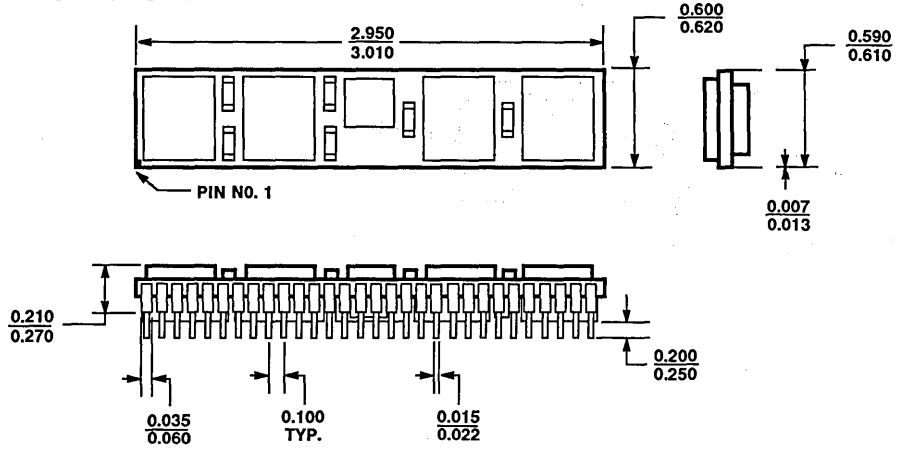
(M9) 48-PIN CERAMIC DIP



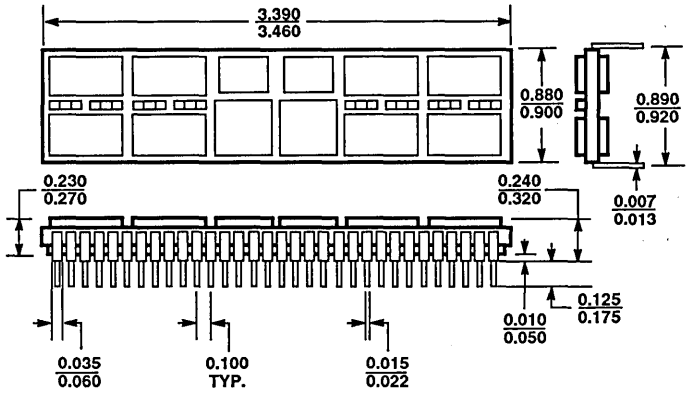
(M10) 58-PIN SIDEBRAZE DIP



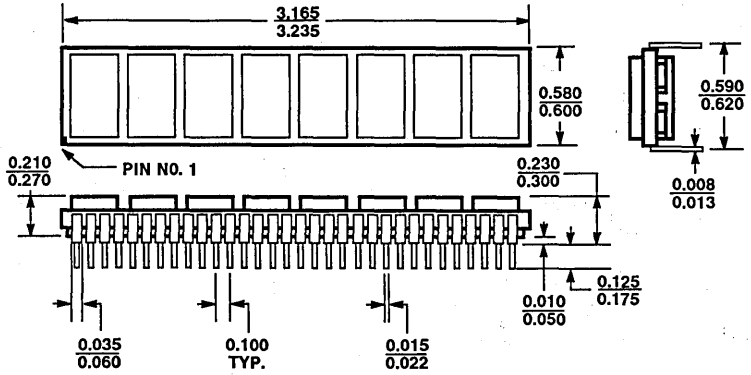
(M11) 60-PIN CERAMIC DIP



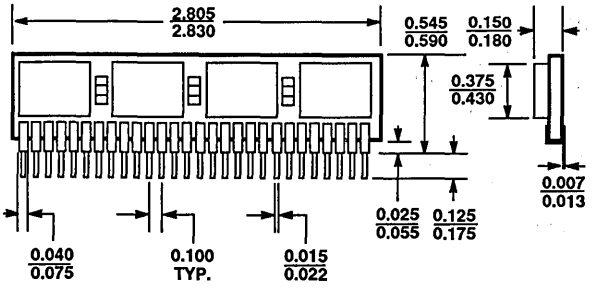
(M12) 64-PIN SIDEBRAZE DIP



(M13) 64-PIN CERAMIC DIP

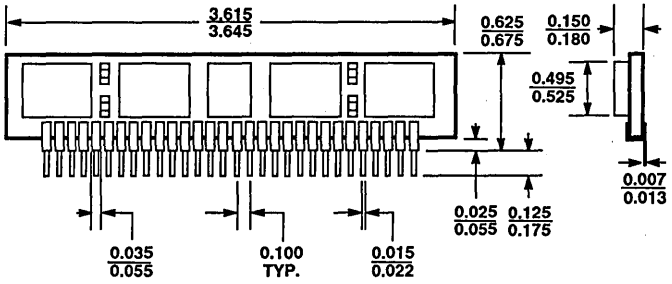


(M14) 28-PIN FR-4 SIP

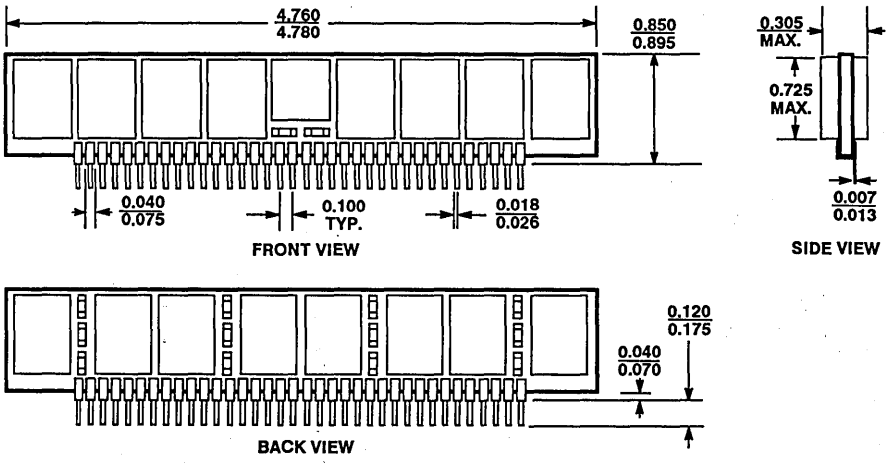


15

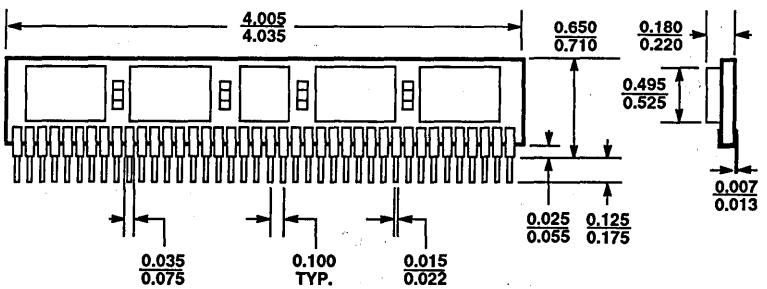
(M15) 30-PIN FR-4 SIP



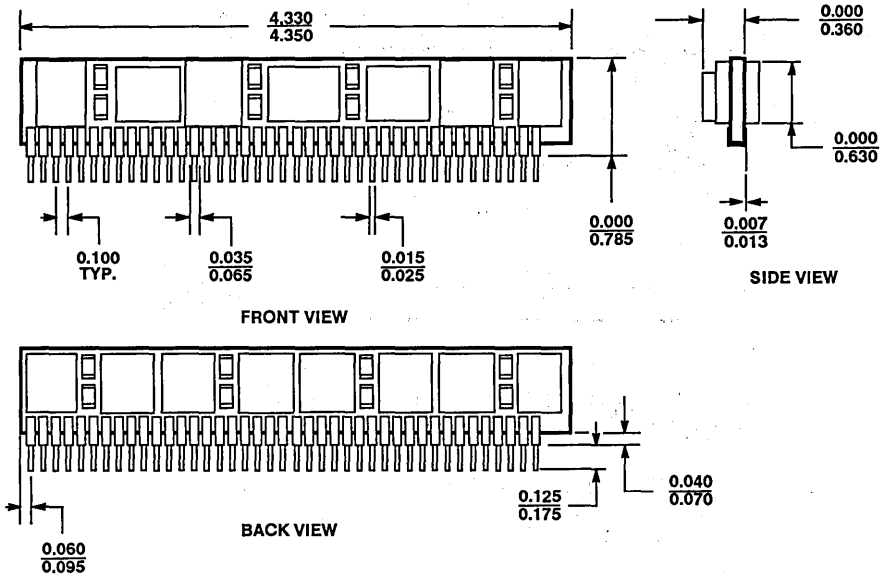
(M16) 36-PIN FR-4 SIP



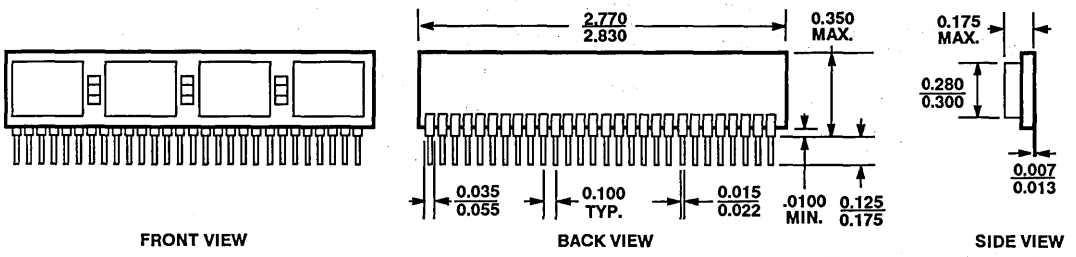
(M17) 40-PIN FR-4 SIP



(M18) 43-PIN FR-4 SIP



(M19) 28-PIN CERAMIC SIP



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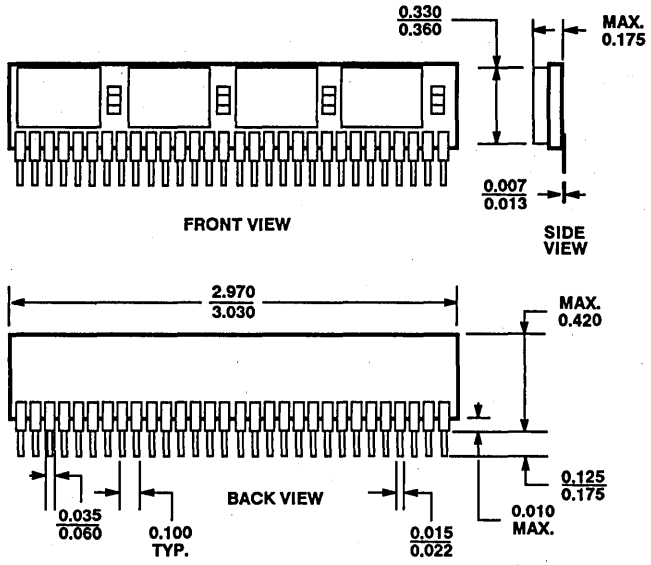
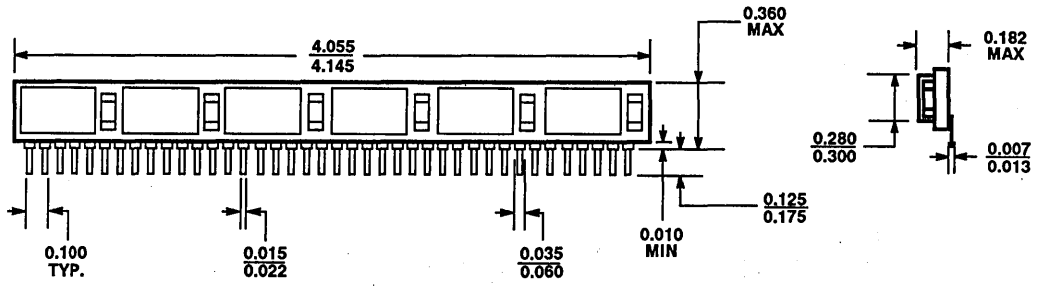
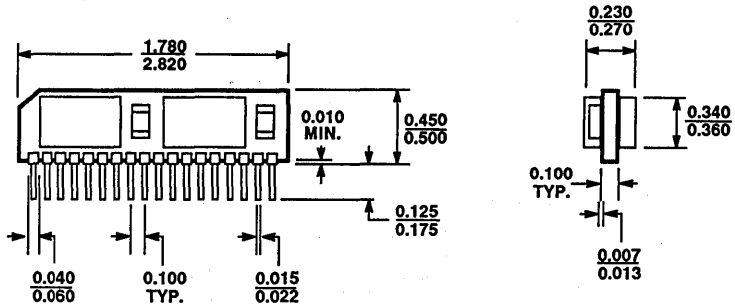
(M20) 30-PIN CERAMIC SIP



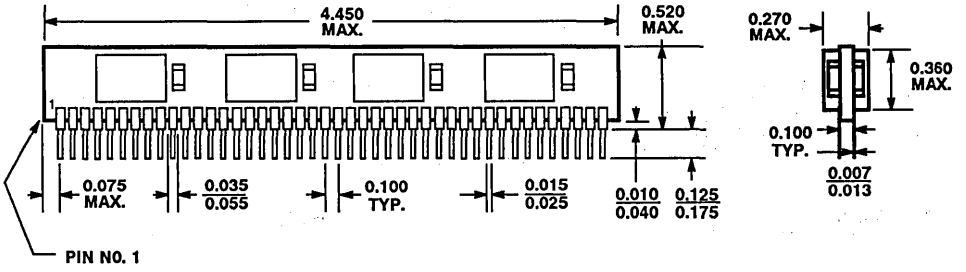
(M21) 40-PIN CERAMIC SIP



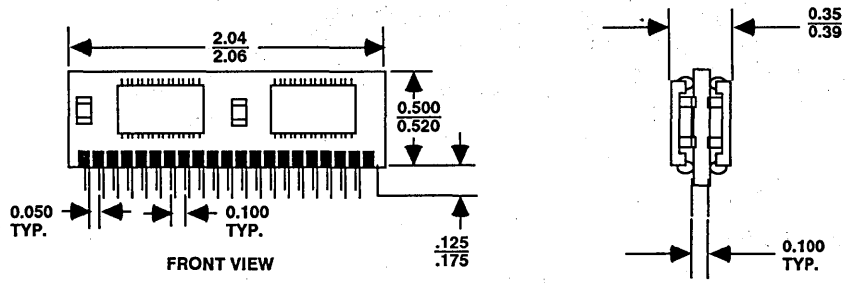
(M22) 36-PIN CERAMIC DUAL SIP



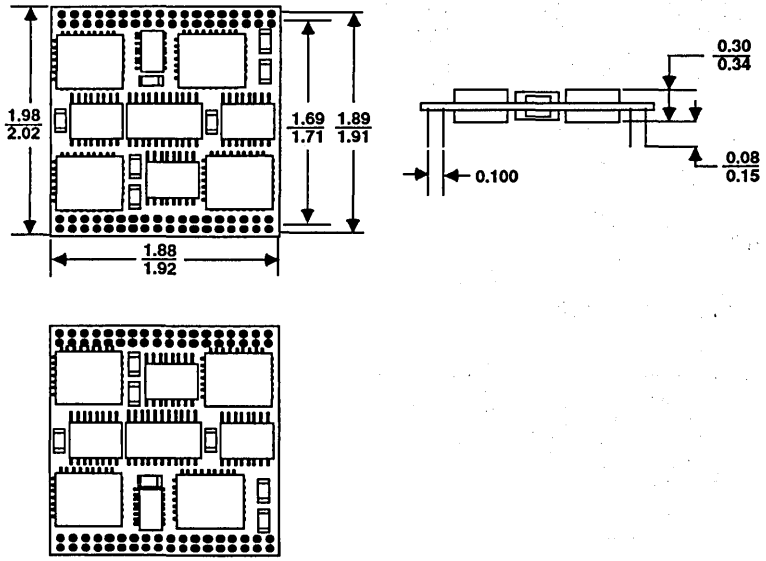
(M23) 88-PIN CERAMIC DUAL SIP



(M24) 40-PIN FR-4 ZIP



(M25) 92-PIN FR-4 QIP



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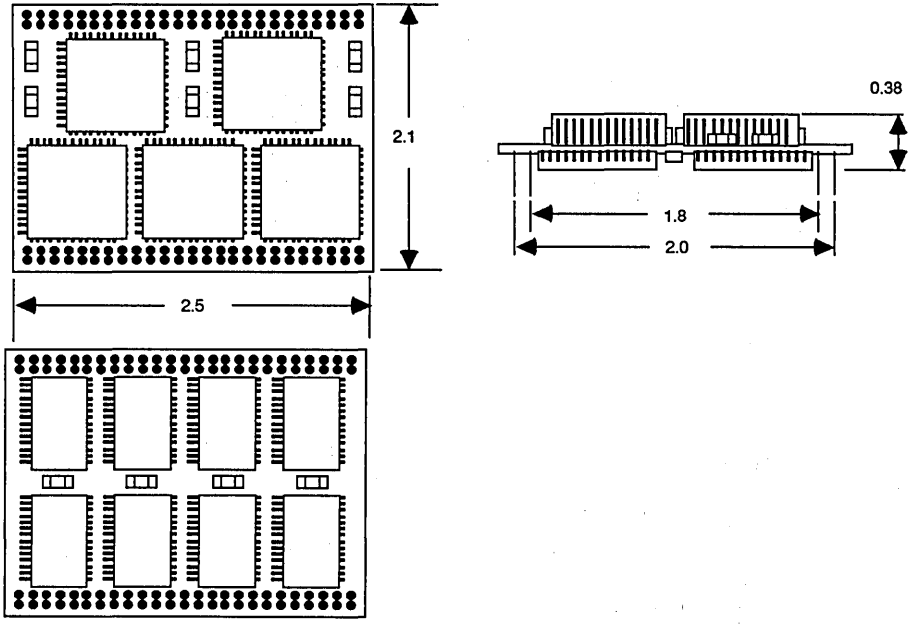
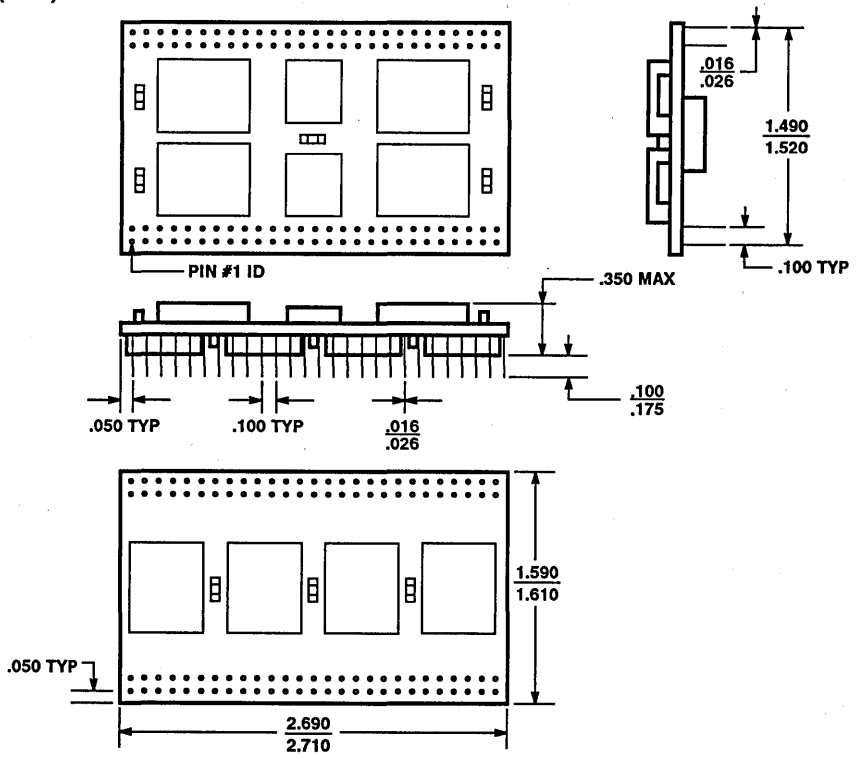
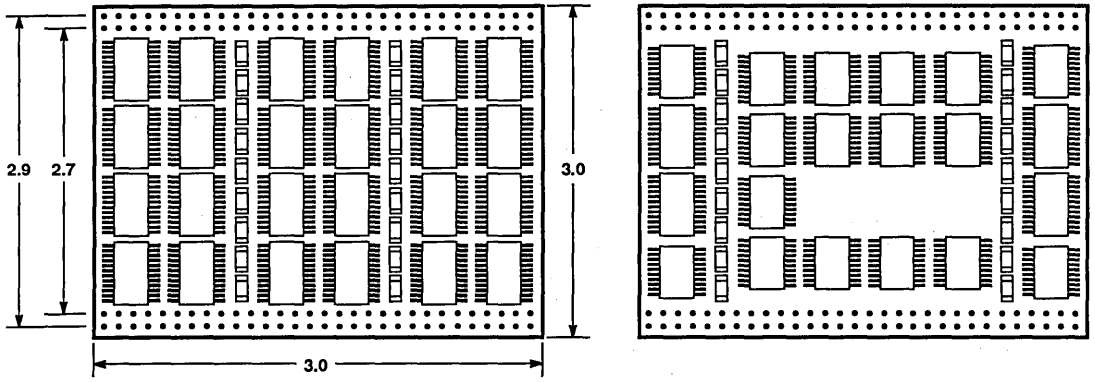
(M26) 100-PIN FR-4 QIP



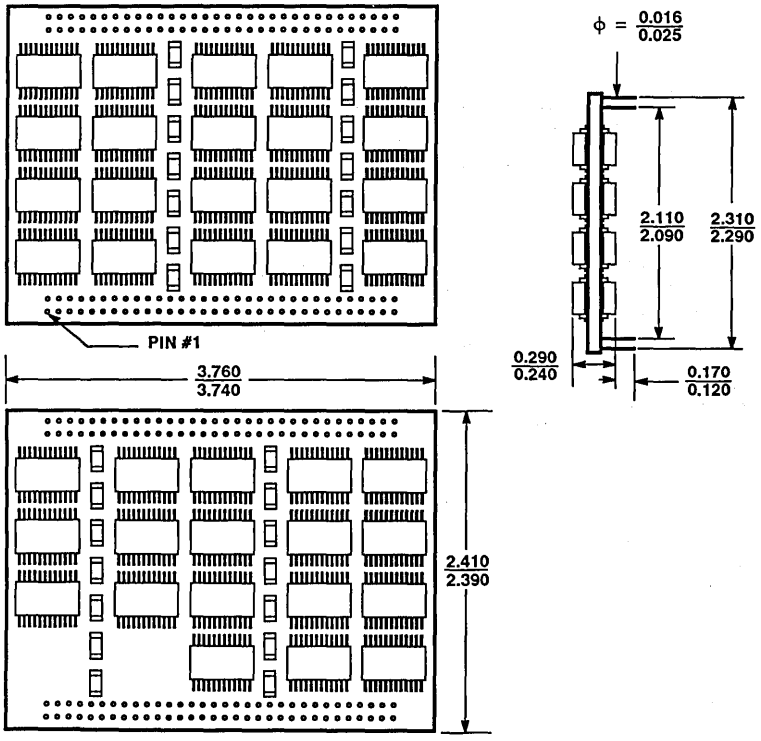
(M27) 108-PIN FR-4 QIP



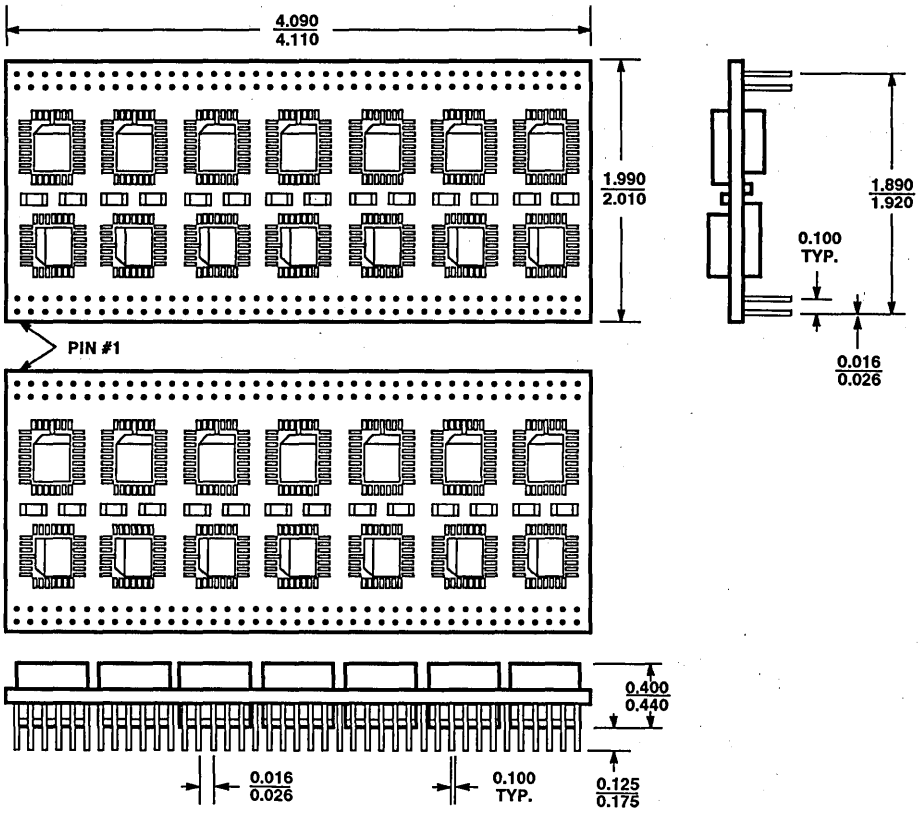
(M28) 120-PIN FR-4 QIP



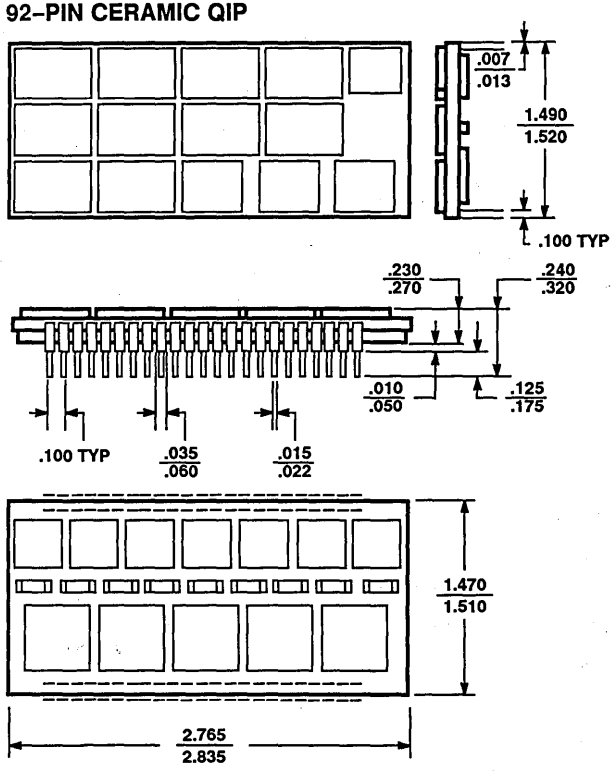
(M29) 128-PIN FR-4 QIP



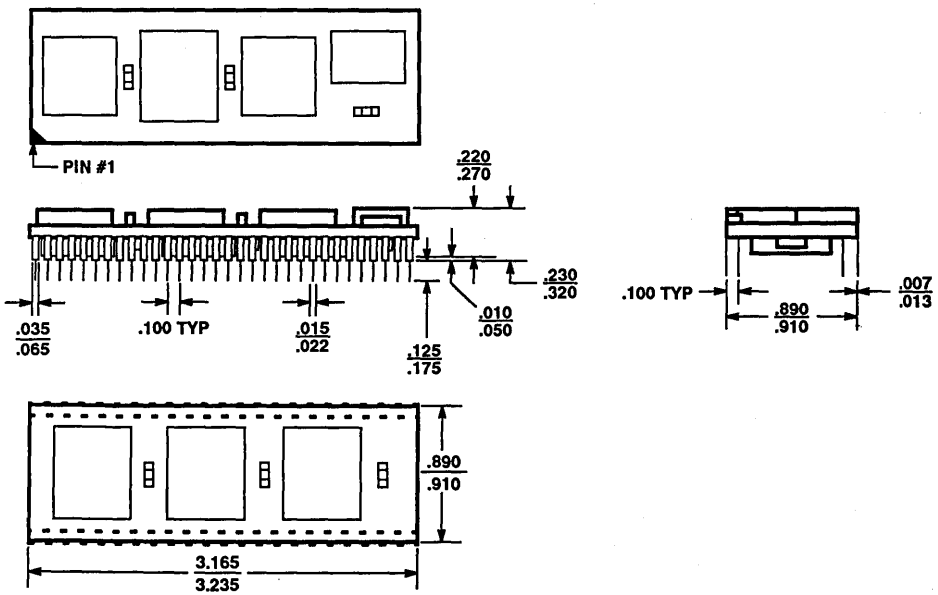
(M30) 164–PIN FR-4 QIP



(M31) 92-PIN CERAMIC QIP



(M32) 128-PIN CERAMIC QIP



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Integrated Device Technology, Inc. has sales representatives and distributors covering each geographic area. Contact the nearest IDT Area Sales Office for the number of the local IDT sales office in your region. Integrated Device Technology Area Sales Offices are located in:

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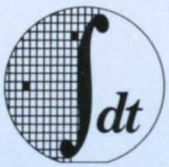

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