1992 DATA BOOK

SPECIALIZED MEMORIES AND MODULES

Integrated Device Technology, Inc.

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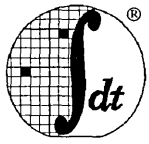

Integrated Device Technology, Inc.

1992
SPECIALIZED MEMORIES & MODULES DATA BOOK

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CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books — Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1992 Specialized Memories and Modules Data Book is comprised of new and revised data sheets for the FIFO, Specialty Memory and Subsystem product groups. Also included is a current packaging section for the products included in this book. This section will be updated in each subsequent data book to reflect packages offered for products included in that book.

The 1992 Specialized Memories and Modules Data Book's Table of Contents contains a listing of the products contained in that data book only. In the past we have included products that appeared in other IDT data books. The numbering scheme for the book is consistent with the 1990-91 data books. The number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speed, lower power, and package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, and Cross Reference Guides. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

ABOUT THE COVER

The cover features an IDT7025 wafer shown at approximately 2.5x magnification along with an IDT7MP6086 module shown at 1x magnification. The IDT7025 is a 30ns 8K x 16 dual-port which is the deepest dual-port available in the industry, offering simultaneous access to memory from either port. The IDT7MP6086 is one of IDT's CacheRAM™ modules. Available in a variety of configurations, and using the IDT71589 CacheRAM as a base, these cache modules offer up to 256KBytes of secondary cache in high-performance 486 microprocessor designs.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

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1992 SPECIALIZED MEMORIES & MODULES DATA BOOK (CONTINUED) ..... PAGE

FIFO PRODUCTS (CONTINUED)

FIFO MODULES

Please refer to Subsystems Products listing for FIFO Modules.

SPECIALTY MEMORY PRODUCTS

1992 SPECIALIZED MEMORIES & MODULES DATA BOOK (CONTINUED)

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

NUMERICAL TABLE OF CONTENTS (CONTINUED)

NUMERICAL TABLE OF CONTENTS (CONTINUED)

ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

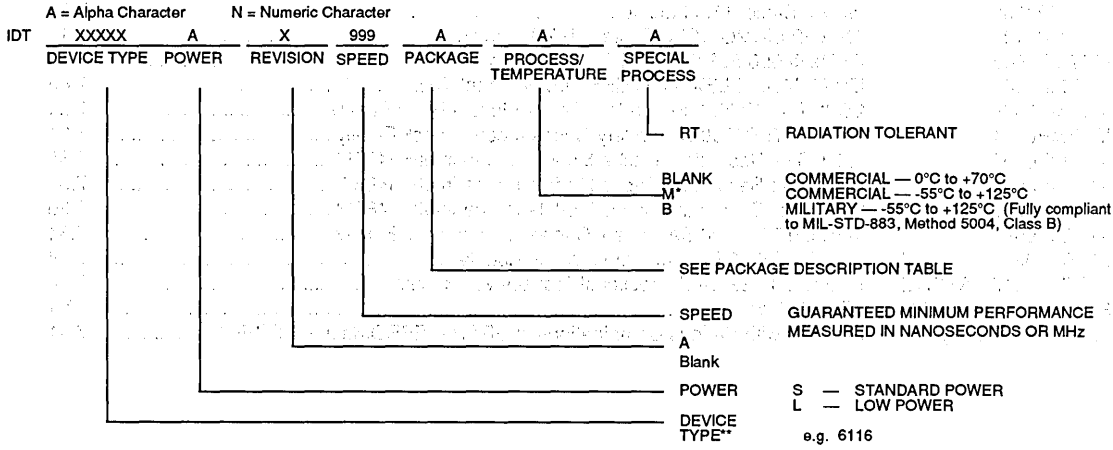
A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

AC (ACTIVITY CODE)
F = Consult Factory
N = New Part
O = Obsolete Part
D = Decrease in Price
I = Increase in Price
W = Non Returnable
* = Leadership Product
% = 5% Program (for North American Distributors Only)

Federal Supply Code Number/Cage Number – 61772
Dun & Bradstreet Number – 03-814-2600
Federal Tax I.D. – 94-2669985
TLX# – 887766
FAX# – 408-727-3468

PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character

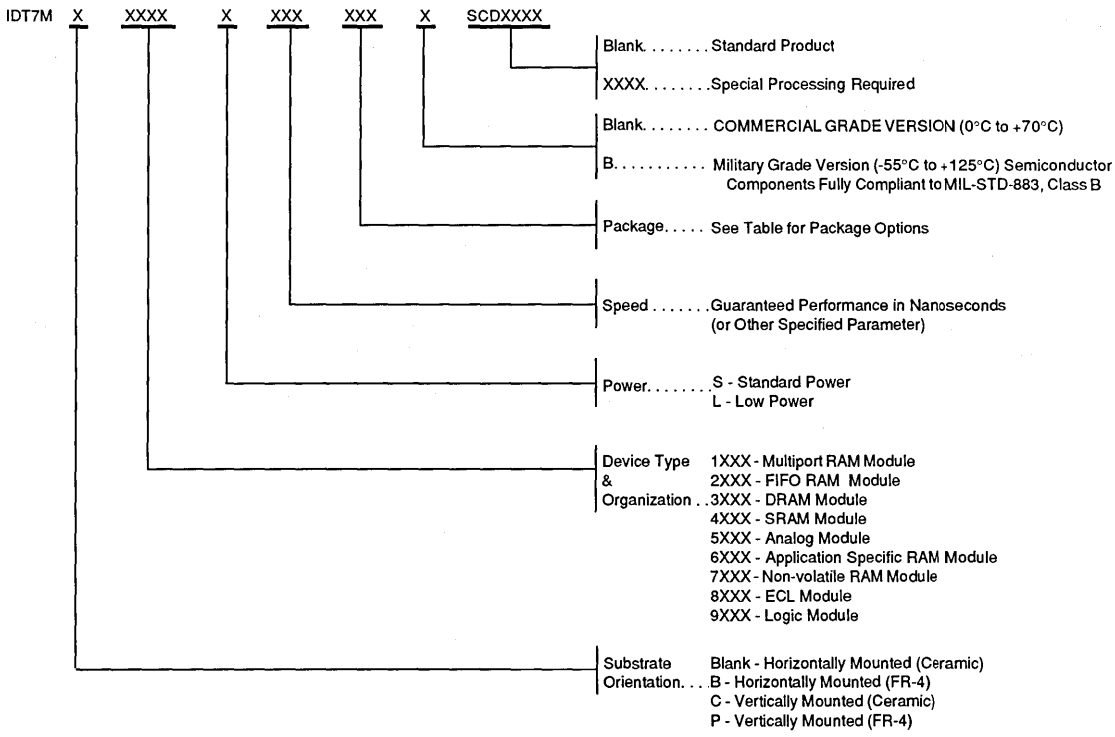


PACKAGE DESCRIPTION TABLE

C	CERAMIC SIDEBRAZE	PF	PLASTIC FLATPACK
D	CERDIP	SO	PLASTIC SMALL OUTLINE IC
F	FLATPACK	TC	SIDEBRAZE THINDIP (300 MIL)
G	PIN GRID ARRAY	TP	PLASTIC THIN DUAL IN-LINE
J	PLASTIC LEADED CHIP CARRIER	QE	CERQUAD GULL WING
L	LEADLESS CHIP CARRIER	XE	CERPACK (F11 CONFIG. ONLY)
P	PLASTIC DIP	XL	FINE-PITCH LCC
Y	SOJ		

*Consult Factory
**For Logic, the "54" series (e.g. IDT54FCT138) — -55°C to +125°C
the "74" series (e.g. IDT74FCT138) — 0°C to +70°C

MODULE ORDERING INFORMATION



Code	Substrate and Pin Type	Component Type
P	FR-4 DIP (Dual In-Line Package)	Plastic
C	CERAMIC DIP (Dual In-Line Package)	Ceramic
N	CERAMIC DIP (Dual In-Line Package)	Plastic
K	FR-4 QIP (Quad In-Line Package)	Plastic
CK	CERAMIC QIP (Quad In-Line Package)	Ceramic
H	FR-4 HIP (Hex In-Line Package)	Plastic
CH	CERAMIC QIP (Quad In-Line Package)	Ceramic
NH	CERAMIC QIP (Quad In-Line Package)	Plastic
G	CERAMIC PGA (Pin Grid Array)	Ceramic
S	FR-4 SIP (Single In-Line Package)	Plastic
CS	CERAMIC SIP (Single In-Line Package)	Ceramic
V	FR-4 DSIP (Dual Single In-Line Package)	Plastic
CV	CERAMIC DSIP (Dual Single In-Line Package)	Ceramic
Z	FR-4 ZIP (Zip-zap In-Line Package)	Plastic
M	FR-4 SIMM (Single In-Line Memory Module)	Plastic

NOTES:

1. FR-4 is a multi-layered, glass filled epoxy laminate substrate.
2. Ceramic is a multi-layered, co-fired ceramic substrate.
3. Plastic refers to all surface mount devices available in various non-hermetically sealed packages (i.e. SOIC, SOJ, Flat Packs, etc.).
4. Ceramic refers to all surface mount devices available in various hermetically sealed packages (i.e. LCC, ceramic Flat Packs, etc.).

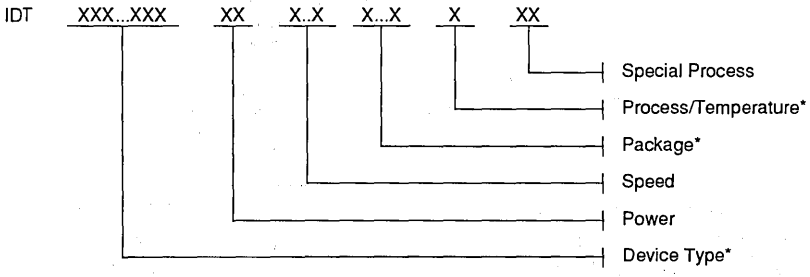
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

EXAMPLE FOR SUBSYSTEM MODULES

See Ordering Information (section 1.4), page 2.

High-Speed CMOS FIFOs

- Broadest range of FIFOs in the industry
- Highest performance FIFO products
- Most innovative FIFO products
- MIL-STD-883 compliant

CLOCKED FIFOs

- Ultra-high performance — Com'l. - 67MHz and Mil. - 50MHz
- 8-, 9- and 18-bit wide buses for today's processors
- Separate clock and enable signals for read and write
- Read and write clocks can be asynchronous or coincident
- Programmable depths for Almost-Empty and Almost-Full flags
- Simple depth and width expansion
- Various densities — 64 to 4K

BIDIRECTIONAL FIFOs

- Bus-matching BiFIFOs for 18-to-9 bit, 36-to-9 bit or 36-to-18 bit connections
- Parallel BiFIFOs for 9-to-9 bit or 18-to-18 bit connections
- Bypass path for direct status/command interchange
- Programmable depths for Almost-Empty and Almost- Full flags
- Built-in DMA handshake signals

CLOCKED BIDIRECTIONAL FIFOs

- Ultra-high performance — 40MHz
- 18-bit wide buses
- Read and write clocks can by asynchronous or coincident
- Separate clock and enable for each bus
- Programmable depths for Almost-Empty and Almost-Full flags

PARALLEL FIFOs

- Extremely high performance — 15ns
- High density — up to 16K x 9
- Asynchronous or simultaneous reads and writes
- Simple width and depth expansion
- Space-efficient packaging
- Multiple flags —Full, Empty and Half-Full

FLAGGED FIFOs

- Output enable for direct bus connections
- Multiple flags — Full, Empty, Almost-Empty and Almost-Full

PARALLEL/SERIAL FIFOs

- Dedicated P/S and S/P architectures in space-efficient packages
- Configurable architecture — P/S, S/P, P/P, S/S for design flexibility
- FLEXISHIFT™ allows easy serial word width selection
- Multiple flags — Full, Full-1, Almost-Full, Half-Full, Almost Empty, Empty+1, Empty

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page
CLOCKED FIFO†						
IDT72420	64 x 8	20	15	770	NOW	E 5.8
IDT72200	256 x 8	20	15	770	NOW	E 5.8
IDT72210	512 x 8	20	15	770	NOW	E 5.8
IDT72220	1K x 8	25	20	770	NOW	E 5.8
IDT72230	2K x 8	25	20	770	NOW	E 5.8
IDT72240	4K x 8	25	20	770	NOW	E 5.8
IDT72421	64 x 9	20	15	770	NOW	E 5.9
IDT72201	256 x 9	20	15	770	NOW	E 5.9
IDT72211	512 x 9	20	15	770	NOW	E 5.9
IDT72221	1K X 9	25	20	770	NOW	E 5.9
IDT72231	2K x 9	25	20	770	NOW	E 5.9
IDT72241	4K x 9	25	20	770	NOW	E 5.9
IDT72215L	512 x 18	25	20	1375	NOW	E 5.10
IDT72225L	1K x 18	25	20	1375	NOW	E 5.10
IDT72215LB	512 x 18 (Depth Expandable)	25	20	1375	3Q'92	E 5.11
IDT72225LB	1K x 18 (Depth Expandable)	25	20	1375	3Q'92	E 5.11
IDT72235LB	2K x 18 (Depth Expandable)	25	20	1375	NOW	E 5.11
IDT72245LB	4K x 18 (Depth Expandable)	25	20	1375	NOW	E 5.11
BIDIRECTIONAL FIFOs						
IDT7251	512 x 18 — 1K x 9 Bus Matching	40	35	1210	NOW	E 5.14
IDT72510	512 x 18 — 1K x 9 Bus Matching	40	35	1210	NOW	E 5.14
IDT72511	512 x 18 — 512 x 18	40	35	1210	NOW	E 5.15
IDT7252	1K x 18 — 2K x 9 Bus Matching	40	35	1210	NOW	E 5.14

† — Clocked FIFO speeds are cycle times. All others are **access** times.

■ = additional or new information exists since the publication of Data Book Update 1

HIGH-SPEED CMOS FIFO

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page
IDT72520	IK x 18 — 2K x 9 Bus Matching	40	35	1210	NOW	E 5.14
IDT72521	1K x 18 — 1K x 18	40	35	1265	NOW	E 5.15
IDT7271	512 x 9 Single Memory Bank	TBD	25	825	NOW	E 5.17
IDT7272	1K x 9 Single Memory Bank	TBD	25	825	NOW	E 5.17
IDT7273	2K x 9 Single Memory Bank	TBD	25	825	NOW	E 5.17
CLOCKED BIDIRECTIONAL FIFOs†						
IDT72605	256 x 18 — 2562 x 18	30	25	1375	3Q'92	E 5.16
IDT72615	512 x 18 — 512 x 18	30	25	1375	NOW	E 5.16
PARALLEL FIFOs						
IDT72401	64 x 4	35MHz	45MHz	192	NOW	E 5.12
IDT72402	64 x 5	35MHz	45MHz	192	NOW	E 5.12
IDT72403	64 x 4 with $\overline{OE}$	35MHz	45MHz	192	NOW	E 5.12
IDT72404	64 x 5 with $\overline{OE}$	35MHz	45MHz	192	NOW	E 5.12
IDT72413	64 x 5 with $\overline{OE}$, Almost-Empty, Almost-Full flags	35MHz	45MHz	192	NOW	E 5.13
IDT7200	256 x 9	20	15	770	NOW	E 5.1
IDT7201	512 x 9	20	15	770	NOW	E 5.1
IDT7202	1K x 9	20	15	770	NOW	E 5.1
IDT7203	2K x 9	30	20	880	NOW	E 5.2
IDT7204	4K x 9	30	20	880	NOW	E 5.2
IDT7205	8K x 9	30	20	770	NOW	E 5.2
IDT7206	16K x 9	30	20	880	NOW	E 5.2
FLAGGED FIFOs						
IDT72021	IK x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	30	25	660	NOW	E 5.3
IDT72031	2K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	40	35	660	NOW	E 5.3
IDT72041	4K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	40	35	660	NOW	E 5.3
PARALLEL/SERIAL FIFOs						
IDT72103	2K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FLEXISHIFT	40	35	770	NOW	E 5.4
IDT72104	4K x 9 configurable Parallel/Serial I/O, multiple flags, 50 MHz serial rate and FLEXISHIFT	40	35	770	NOW	E 5.4
IDT72105	256 x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	30	25	550	NOW	E 5.5
IDT72115	512 x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	30	25	550	NOW	E 5.5
IDT72125	1K x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	30	25	550	NOW	E 5.5
IDT72131	2K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT	40	35	770	NOW	E 5.6
IDT72132	2K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT	40	35	770	NOW	E 5.7
IDT72141	4K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FLEXISHIFT	40	35	770	NOW	E 5.6
IDT72142	4K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FLEXISHIFT	40	35	770	NOW	E 5.7

† — Clocked FIFO speeds are **cycle** times. All others are **access** times. ■ = additional or new information exists since the publication of Data Book Update 1

High-Speed CMOS/BiCMOS Multi-Port RAMs

- Now offering 15ns dual-port SRAMs!
- First synchronous dual-port is available and allows for self-timed write cycles.
- All dual-ports have true dual-ported memory cells which allow simultaneous access from both ports.
- World's first FourPort™ SRAMs.
- Complete family of x8, x9 and x16 dual-ports.
- Dense dual-ports (128K).
- MIL-STD-883 compliant

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
DUAL-PORT RAMs						
IDT7130	8K (1K x 8) MASTER: industry's most popular dual-port SRAM	30	25	325	NOW	E 6.1
IDT7140	8K (1K x 8) SLAVE: functions with IDT7130 to provide 16-bit words or wider; pin-compatible with IDT7130	30	25	325	NOW	E 6.1
IDT7030	8K (1K x 8) MASTER: high-speed dual-port in DIP package with center-pin ground	30	25	325	NOW	E 6.2
IDT7040	8K (1K x 8) SLAVE: high-speed dual-port in DIP package with center-pin ground	30	25	325	NOW	E 6.2
IDT7132	16K (2K x 8) MASTER: fastest available speeds in this industry standard product; now multiple sources	30	25	325	NOW	E 6.3
IDT7142	16K (2K x 8) SLAVE: functions with IDT7132 to provide 16-bit words or wider; pin-compatible with IDT7132	30	25	325	NOW	E 6.3
IDT7032	16K (2K x 8) MASTER: high-speed dual-port in DIP package with center-pin ground	30	25	325	NOW	E 6.4
IDT7042	16K (2K x 8) SLAVE: high-speed dual-port in DIP package with center-pin ground	30	25	325	NOW	E 6.4
IDT71321	16K (2K x 8) MASTER: high-speed dual-port with interrupt output	30	25	325	NOW	E 6.5
IDT71421	16K (2K x 8) SLAVE: functions with IDT71321 to provide 16-bit words or wider; pin-compatible with IDT71321	30	25	325	NOW	E 6.5
IDT7133	32K (2K x 16) MASTER: high-speed dual-port with busy	35	25	500	NOW	E 6.8
IDT7143	32K (2K x 16) SLAVE: functions with IDT7133 to provide 32-bit words or wider	35	25	500	NOW	E 6.8
IDT7134	32K (4K x 8) high-speed operation in systems where on-chip arbitration is not needed	35	25	500	NOW	E 6.9
IDT71342	32K (4K x 8) with semaphores	45	35	500	NOW	E 6.10
IDT7024	64K (4K x 16) with busy, interrupt semaphore and master/slave select	35	25	750	NOW	E 6.14
IDT7005	64K (8K x 8) with busy, interrupt, semaphore and master/slave select	45	35	750	NOW	E 6.13
IDT7025	128K (8K x 16) industry's largest monolithic dual-port RAM with busy, interrupt, semaphores and master/slave select	35	25	750	NOW	E 6.16
IDT7006	128K (16K x 8) with busy, interrupt, semaphore and master/slave select	45	35	750	NOW	E 6.15
IDT7012	18K (2K x 9) high-speed operation in systems where on-chip arbitration is not needed	30	25	400	NOW	E 6.6

◘ = additional or new information exists since the publication of Data Book Update 1

High-Speed CMOS/BiCMOS Multi-Port RAMs

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Data Book Page
IDT70121	18K (2K x 9) MASTER: high-speed dual-port with busy and interrupt	30	25	400	NOW	E 6.7
IDT70125	18K (2K x 9) SLAVE: functions with IDT70121 to provide 18-bit words or wider with busy and interrupt	30	25	400	NOW	E 6.7
FourPort RAMs						
IDT7050	8K (1K x 8) FourPort SRAM offers increased system performance in multiprocessor systems that have a need to communicate in real time	30	25	750	NOW	E 6.17
IDT7052	16K (2K x 8) FourPort SRAM offers added benefits for high-speed systems in which multiple access is required in the same cycle	30	25	750	NOW	E 6.18
SYNCHRONOUS DUAL-PORT RAM						
IDT7099	36K (4K x 9) Synchronous dual-port with registered data input, address, and control lines. Speeds listed are cycle time	25	20	900	NOW	E 6.12
BICMOS DUAL-PORT RAM						
IDT7014	36K (4K x 9) high-speed, dual-port processed using our BiCEMOS process	20	15	900	NOW	E 6.11

■ = additional or new information exists since the publication of Data Book Update 1

High-Speed CMOS and BiCMOS Module Products

- High-density, high-performance module products for commercial and military applications
- Standard module products are used in a wide range of applications, such as personal computers, workstations, video systems, data communications, telecommunications, add-on VME-type cards, test systems, DSP systems, electronic surveillance, guidance systems, and intelligent controller systems.
- Fully customized module solutions are available to achieve optimum system integration and performance. Custom modules take advantage of IDT's experienced design, test, and manufacturing teams all working with the highest-performance components available.
- Modules are built using state-of-the-art techniques in surface-mount technology. Typically, monolithic components are double-sided surface mounted onto multi-layered FR-4 epoxy laminate substrates or co-fired ceramic substrates
- A wide variety of module packages are available offering the optimum combination of pin count and board area. Some of these packages include industry standard DIPs, ZIPs, SIMMs and PGAs, in addition to other unique module packaging, such as SIPs, DSIPs, QIPs, HIPs, and advanced high-density connectors
- FourPort multichip module available, as well as custom multichip module capabilities

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Avail.	Data Book Page
CUSTOM MODULES AND MULTICHIP MODULES					
Memory-based Modules – SRAM, DRAM, non-volatile RAM				NOW	
CPU-based Modules – RISC, CISC, DSP, custom ASIC				NOW	
Please consult factory or call your local sales representative for more details.					
SRAM MONOLITHICS					
IDT71M024	128K x 8 Static RAM	60	60	NOW	E 7.33
IDT71M025	128K x 8 Static RAM	60	60	NOW	E 7.33
SRAM MODULES					
IDT7MP4104	1M x 32 Static RAM Module	—	20	3Q'92	E 7.14
IDT7MP4045	256K x 32 Static RAM Module	—	20	NOW	E 7.17
IDT7M4077	256K x 32 Static RAM Module	**25**	**20**	NOW	E 7.15
IDT7MB4067	256K x 32 Static RAM Module	—	20	NOW	E 7.16
IIDT7M4013	128K x 32 Static RAM Module	**25**	**20**	NOW	E 7.18
IDT7MP4036	64K x 32 Static RAM Module	—	**12**	NOW	E 7.19
IDT7M4003	32K x 32 Static RAM Module	**25**	**20**	NOW	E 7.18
DT7MP4031	16K x 32 Static RAM Module	—	**10**	NOW	E 7.20
IDT7MB4065	256K x 20 Static RAM Module	—	20	NOW	E 7.21
IDT7MP4047	512K x 16 Static RAM Module	—	70	NOW	E 7.22
IDT7MP4046	256K x 16 Static RAM Module	—	70	NOW	E 7.22
IDT7MB4066	256K x 16 Static RAM Module	—	20	NOW	E 7.21
IDT7MP4027	64K x 16 Static RAM Module	—	**12**	NOW	E 7.23
IDT7MB4040	256K x 9 Static RAM Module	—	**12**	NOW	E 7.24
IDT7MB4084	2M x 8 Static RAM Module	—	55	3Q'92	E 7.25
IDT7MP4059	2M x 8 Static RAM Module	—	55	3Q'92	E 7.26
IDT7M4048	512K x 8 Static RAM Module	30	25	NOW	E 7.27
IDT7MB4048	512K x 8 Static RAM Module	—	25	NOW	E 7.27
IDT7MP4058	512K x 8 Static RAM Module	—	70	NOW	E 7.29
IDT7M4068	256K x 8 Static RAM Module	30	25	NOW	E 7.30
IDT7MB4068	256K x 8 Static RAM Module	—	**20**	NOW	E 7.30
IDT7MP4034	256K x 8 Static RAM Module	—	**12**	NOW	E 7.32
486 MICROPROCESSOR SECONDARY CACHE MODULES					
IDT7MB6091	128KB Secondary Cache Module for the 486 CPU	—	33MHz	NOW	E 7.37
IDT7MB6089	128KB Secondary Cache Module for the 486 CPU	—	33MHz	NOW	E 7.36

■ = additional or new information exists since the publication of Data Book Update 1

High-Speed CMOS and BiCMOS Module Products

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Avail.	Data Book Page
IDT7MP6085	128KB Secondary Cache Module for the 486 CPU	—	50MHz	NOW	E 7.35
IDT7MP6086	128KB Secondary Cache Module for the 486 CPU	—	50MHz	NOW	E 7.38
IDT7MP6087	256KB Secondary Cache Module for the 486 CPU	—	50MHz	NOW	E 7.35
R4000 MICROPROCESSOR SECONDARY CACHE MODULES					
IDT7MP6048	Flexi-Cache™ Development Tool for the IDT79R4000 CPU (1MB version)	—	**17**	NOW	E 7.40
IDT7MP6068	Flexi-Cache™ Development Tool for the IDT79R4000 CPU (4MB version)	—	25	2H'92	E 7.40
IDT7MP6074	256KB Secondary Cache Module Block for the IDT79R4000 CPU	—	**15**	2H'92	E 7.34
IDT7MP6084	1MB Secondary Cache Module Block for the IDT79R4000 CPU	—	**17**	2H'92	E 7.34
IDT7MP6094	4MB Secondary Cache Module Block for the IDT79R4000 CPU	—	25	2H'92	E 7.34
DUAL-PORT MODULES					
IDT7M1014	4K x 36 Dual-Port Module	20	15	4Q'92	E 7.4
IDT7M1024	4K x 36 Synchronous Dual-Port Module	25	20	4Q'92	E 7.5
IDT7M1012	2K x 36 Dual-Port Module	35	30	NOW	E 7.6
IDT7M1002	16K x 32 Dual-Port Module	40	35	NOW	E 7.3
IDT7MB6036	128K x 16 Dual-Port (Shared Memory) Module	—	**40**	NOW	E 7.7
IDT7MB1006	64K x 16 Dual-Port Module	—	35	NOW	E 7.8
IDT7MB6046	64K x 16 Dual-Port (Shared Memory) Module	—	**40**	NOW	E 7.7
IDT7MB1008	32K x 16 Dual-Port Module	—	35	NOW	E 7.8
IDT7MB6056	32K x 16 Dual-Port (Shared Memory) Module	—	**40**	NOW	E 7.8
IDT7M1005	16K x 9 Dual-Port Module	45	35	NOW	E 7.9
IDT7M1004	8K x 9 Dual-Port Module	45	35	NOW	E 7.9
IDT7M1001	128K x 8 Dual-Port Module	50	40	NOW	E 7.10
IDT7MP1021	128K x 8 Dual-Port Module	—	40	1Q'93	E 7.11
IDT7M1003	64K x 8 Dual-Port Module	50	40	NOW	E 7.10
IDT7MP1023	64K x 8 Dual-Port Module	—	40	NOW	E 7.11
IDT7M137	32K x 8 Dual-Port Module	55	40	NOW	B 8.3
FourPort MODULES					
IDT70M74	4K x 16 FourPort Multichip Module	30	25	1H'93	E 7.2
FIFO MODULES					
IDT7M208	64K x 9 FIFO Module	35	25	NOW	E 7.13
IDT7M207	32K x 9 FIFO Module	**35**	**25**	NOW	E 7.13
IDT7MP2009	32K x 18 FIFO Module	—	**25**	NOW	E 7.12
IDT7MP2010	16K x 18 FIFO Module	—	30	NOW	E 7.12
Flexi-Pak™ MODULES					
IDT7M7004	1M EEPROM Module	95	75	NOW	E 7.42
IDT7M7005	512K SRAM/512K EEPROM Module	**25**/95	**20**/75	NOW	E 7.43
LOGIC MODULES					
IDT7MP9244	32-bit Buffer/Driver Module	—	C	NOW	E 7.44
IDT7MP9245	32-bit Bidirectional Transceiver Module	—	C	NOW	E 7.44

■ = additional or new information exists since the publication of Data Book Update 1

Integrated Device Technology, Inc.

FIFO
CROSS REFERENCE GUIDE

AMD	IDT
Am7200	IDT7200S/L
Am7200-25PC	25TP
Am7200-35PC	35TP
Am7200-50PC	50TP
Am7200-65PC	65TP
Am7200-80PC	80TP
Am7200-25DC	25D
Am7200-35DC	35D
Am7200-50DC	50D
Am7200-65DC	65D
Am7200-80DC	80D
Am7200-25RC	25TP
Am7200-35RC	35TP
Am7200-50RC	50TP
Am7200-65RC	65TP
Am7200-80RC	80TP
Am7200-25JC	25J
Am7200-35JC	35J
Am7200-50JC	50J
Am7200-65JC	65J
Am7200-80JC	80J
Am7200-40/BXA	40DB
Am7200-50/BXA	50DB
Am7200-65/BXA	65DB
Am7200-80/BXA	80DB
Am7201	IDT7201SA/LA
Am7201-25PC	25P
Am7201-35PC	35P
Am7201-50PC	50P
Am7201-65PC	65P
Am7201-80PC	80P
Am7201-25RC	25TP
Am7201-35RC	35TP
Am7201-50RC	50TP
Am7201-65RC	65TP
Am7201-80RC	80TP
Am7201-25JC	25J
Am7201-35JC	35J
Am7201-50JC	50J
Am7201-65JC	65J
Am7201-80JC	80J
Am7201-25DC	25D
Am7201-35DC	35D
Am7201-50DC	50D
Am7201-65DC	65D
Am7201-80DC	80D
Am7201-40/BXA	40DB
Am7201-50/BXA	50DB
Am7201-65/BXA	65DB
Am7201-80/BXA	80DB
Am7202	IDT7202SA/LA
Am7202-25PC	25P
Am7202-35PC	35P
Am7202-50PC	50P
Am7202-65PC	65P
Am7202-80PC	80P
Am7202-25RC	25TP
Am7202-35RC	35TP

AMD	IDT
Am7202	IDT7202SA/LA
Am7202-50RC	50TP
Am7202-65RC	65TP
Am7202-80RC	80TP
Am7202-25JC	25J
Am7202-35JC	35J
Am7202	IDT7202SA/LA
Am7202-50JC	50J
Am7202-65JC	65J
Am7202-80JC	80J
Am7202-25DC	25D
Am7202-35DC	35D
Am7202-50DC	50D
Am7202-65DC	65D
Am7202-80DC	80D
Am7202-40/BXA	40DB
Am7202-50/BXA	50DB
Am7202-65/BXA	65DB
Am7202-80/BXA	80DB
Am7203	IDT7203S/L
Am7203-25PC	25P
Am7203-35PC	35P
Am7203-50PC	50P
Am7203-65PC	65P
Am7203-80PC	80P
Am7203-25RC	25TP
Am7203-35RC	35TP
Am7203-50RC	50TP
Am7203-65RC	65TP
Am7203-80RC	80TP
Am7203-25JC	25J
Am7203-35JC	35J
Am7203-50JC	50J
Am7203-65JC	65J
Am7203-80JC	80J
Am7203-35DC	35D
Am7203-50DC	50D
Am7203-65DC	65D
Am7203-80DC	80D
Am7203-40/BXA	40DB
Am7203-50/BXA	50DB
Am7203-65/BXA	65DB
Am7203-80/BXA	80DB
Am7204	IDT7204S/L
Am7204-25PC	25P
Am7204-35PC	35P
Am7204-50PC	50P
Am7204-65PC	65P
Am7204-80PC	80P
Am7204-25JC	25J
Am7204-35JC	35J
Am7204-50JC	50J
Am7204-65JC	65J
Am7204-80JC	80J
Am7204-35DC	35D
Am7204-50DC	50D
Am7204-65DC	65D
Am7204-80DC	80D

AMD	IDT
Am7204	IDT7204S/L
Am7204-40/BXA	40DB
Am7204-50/BXA	50DB
Am7204-65/BXA	65DB
Am7204-80/BXA	80DB
67C401	IDT72401L
67C401-35N	35P
67C401-25N	25P
67C401-15N	15P
67C401-10N	10P
67C401-35J	35D
67C401	IDT72401L
67C401-25J	25D
67C401-15J	15D
67C401-10J	10D
67401	
67401A-N	15P
67401-N	10P
67401A-J	15D
67401-J	10D
C67401	
C67401A-N	15P
C67401-N	10P
C67401A-J	15D
C67401-J	10D
57C401	
57C401-12J	15DB
57401	
57401A-J	10DB
57401-J	10DB
C57401	
C57401A-J	10DB
C57401-J	10DB
67C402	IDT72402L
67C402-35N	35P
67C402-25N	25P
67C402-15N	15P
67C402-10N	10P
67C402-35J	35D
67C402-25J	25D
67C402-15J	15D
67C402-10J	10D
67402	
67402A-N	15P
67402-N	10P
67402A-J	15D
67402-J	10D
C67402	
C67402A-N	15P
C67402-N	10P
C67402A-J	15D
C67402-J	10D
57C402	
57C402-12J	15DB
57402	
57402A-J	10DB
57402-J	10DB
C57402	

AMD	IDT
C57402	IDT72402L
57402A-J	10DB
57402-J	10DB
C57402	
C57402A-J	10DB
C57402-J	10DB
67C4013	IDT72403L
67C4013-35N	35P
67C4013-25N	25P
67C4013-15N	15P
67C4013-10N	10P
67C4013-35J	35D
67C4013-25J	25D
67C4013-15J	15D
67C4013-10J	10D
57C4013	
57C4013-12J	15DB
67C4023	IDT72404L
67C4023-35N	35P
67C4023-25N	25P
67C4023-15N	15P
67C4023-10N	10P
67C4023-35J	35D
67C4023-25J	25D
67C4023-15J	15D
67C4023-10J	10D
57C4023	
57C4023-12J	15DB
67C4033	IDT72413L
67C4033-15N	25P
67C4033-10N	25P
67C4033-15J	25D
67C4033-10J	25D
67C413	
67C413-40N	45P
67C413-40J	45D
67413	
67413-25N	25P
67413A-35N	35P
67413-25J	25D
67413A-35J	35D
57C4033	
57C4033-12J	25DB

MOSEL	IDT
MS7200	IDT7200
MS7200-25NC	25TP
MS7200-35NC	35TP
MS7200-50NC	50TP
MS7200-80NC	80TP
MS7200-25JC	25J
MS7200-35JC	35J
MS7200-50JC	50J
MS7200-80JC	80J
MS7200L-25NC	25TP
MS7200L-35NC	25TP
MS7200L-50NC	25TP
MS7200L-80NC	25TP
MS7200L-25JC	25J
MS7200L-35JC	35J
MS7200L-50JC	50J
MS7200L-80JC	80J
MS7201	IDT7201
MS7201-50PC	50P
MS7201-65PC	65P
MS7201-80PC	80P
MS7201-120PC	120P
MS7201A	
MS7201A-25JC	25J
MS7201A-35JC	35J
MS7201A-50JC	50J
MS7201A-80JC	80J
MS7201A-25NC	25TP
MS7201A-35NC	35TP
MS7201A-50NC	50TP
MS7201A-80NC	80TP
MS7201A-25PC	25P
MS7201A-35PC	35P
MS7201A-50PC	50P
MS7201A-80PC	80P
MS7201AL-25JC	25J
MS7201AL-35JC	35J
MS7201AL-50JC	50J
MS7201AL-80JC	80J
MS7201AL-25NC	25TP
MS7201AL-35NC	35TP
MS7201AL-50NC	50TP
MS7201AL-80NC	80TP
MS7201AL-25PC	25P
MS7201AL-35PC	35P
MS7201AL-50NC	50P
MS7201AL-80PC	80P
MS7202A	IDT7202S/L
MS7202A-25JC	25J
MS7202A-35JC	35J
MS7202A-50JC	50J
MS7202A-80JC	80J
MS7202A-25NC	25TP
MS7202A-35NC	35TP
MS7202A-50NC	50TP
MS7202A-80NC	80TP
MS7202A-25PC	25P
MS7202A-35PC	35P

MOSEL	IDT
MS7202A	IDT7202S/L
MS7202A-50PC	50P
MS7202A-80PC	80P
MS7202AL-25JC	25J
MS7202AL-35JC	35J
MS7202AL-50JC	50J
MS7202AL-80JC	80J
MS7202AL-25NC	25TP
MS7202AL-35NC	35TP
MS7202AL-50NC	50TP
MS7202AL-80NC	80TP
MS7202AL-25PC	25P
MS7202AL-35PC	35P
MS7202AL-50PC	50P
MS7202AL-80PC	80P
MS7203	IDT7203
MS7203-35JC	35J
MS7203-50JC	50J
MS7203-80JC	80J
MS7203-35NC	35TP
MS7203-50NC	50TP
MS7203-80NC	80TP
MS7203-35PC	35P
MS7203-50PC	50P
MS7203-80PC	80P
MS7203L-35JC	35J
MS7203L-50JC	50J
MS7203L-80JC	80J
MS7203L-35NC	35TP
MS7203L-50NC	50TP
MS7203L-80NC	80TP
MS7203L-35PC	35P
MS7203L-50PC	50P
MS7203L-80PC	80P

SGS	IDT
MK4501	IDT7201SA/LA
MK4501N-65	65P
MK4501N-80	80P
MK4501N-10	80P
MK4501N-12	120P
MK4501N-15	120P
MK4501N-20	120P
MK4501K-65	65J
MK4501K-80	80J
MK4501K-10	80J
MK4501K-12	120J
MK4501K-15	120J
MK4501K-20	120J
MK4503	IDT7203S/L
MK4503N-50	50P
MK4503N-65	65P
MK4503N-80	80P
MK4503N-10	80P
MK4503N-12	120P
MK4503N-15	120P
MK4503N-20	120P
MK4503K-50	50J
MK4503K-65	65J
MK4503K-80	80J
MK4503K-10	80J
MK4503K-12	120J
MK4503K-15	120J
MK4503K-20	120J

Dallas	IDT
DS2009	IDT7201SA/LA
DS2009-35	35P
DS2009-50	50P
DS2009-65	65P
DS2009-80	80P
DS2009R-35	35J
DS2009R-50	50J
DS2009R-65	65J
DS2009R-80	80J
DS2010	IDT7202SA/LA
DS2010-35	35P
DS2010-50	50P
DS2010-65	65P
DS2010-80	80P
DS2010R-35	35J
DS2010R-50	50J
DS2010R-65	65J
DS2010R-80	80J
DS2011	IDT7203S/L
DS2011-35	35P
DS2011-50	50P
DS2011-65	65P
DS2011-80	80P
DS2011R-35	35J
DS2011R-50	50J
DS2011R-65	65J
DS2011R-80	80J

QSI	IDT
QS8201	IDT7201SA/LA
QS8201-15	15TP
QS8201-20P	20TP
QS8201-25P	25TP
QS8201-35P	35TP
QS8201-50P	50TP
QS8201-80TP	80TP
QS8201-15JR	15J
QS8201-20JR	20J
QS8201-25JR	25J
QS8201-35JR	35J
QS8201-50JR	50J
QS8201-80JR	80J
QS8201-25P6	25P
QS8201-35P6	35P
QS8201-50P6	50P
QS8201-80P6	80P
QS8201-15S3	15SO
QS8201-20S3	20SO
QS8201-25S3	25SO
QS8201-35S3	35SO
QS8201-50S3	50SO
QS8202	IDT7202SA/LA
QS8202-15	15TP
QS8202-20P	20TP
QS8202-25P	25TP
QS8202-35P	35TP
QS8202-50P	50TP
QS8202-80TP	80TP
QS8202-15JR	15J
QS8202-20JR	20J
QS8202-25JR	25J
QS8202-35JR	35J
QS8202-50JR	50J
QS8202-80JR	80J
QS8202-25P6	25P

TI	IDT
54/74ALS236	IDT72401L
SN74ALS236-30N	35P
SN54ALS236-25J	25DB
54/74ALS234	IDT72403L
SN74ALS234-30N	35P
SN54ALS234-25J	25DB
54/74ALS235	IDT72413L
SN74ALS235-25N	25P
SN74ALS235-25DW	25SO
SN54ALS235-20J	25DB

Samsung	IDT
KM75C01A	IDT7201SA/LA
KM75C01AP-15	15P
KM75C01AP-20	20P
KM75C01AP-25	25P
KM75C01AP-35	35P
KM75C01AP-50	50P
KM75C01AP-80	80P
KM75C01AJ-15	15J
KM75C01AJ-20	20J
KM75C01AJ-25	25J
KM75C01AJ-35	35J
KM75C01AJ-50	50J
KM75C01AJ-80	80J
KM75C01AN-15	15TP
KM75C01AN-20	20TP
KM75C01AN-25	25TP
KM75C01AN-35	35TP
KM75C01AN-50	50TP
KM75C01AN-80	80TP
KM75C02A	IDT7202SA/LA
KM75C02AP-15	15P
KM75C02AP-20	20P
KM75C02AP-25	25P
KM75C02AP-35	35P
KM75C02AP-50	50P
KM75C02AP-80	80P
KM75C02AJ-15	15J
KM75C02AJ-20	20J
KM75C02AJ-25	25J
KM75C02AJ-35	35J
KM75C02AJ-50	50J
KM75C02AJ-80	80J
KM75C02AN-15	15TP
KM75C02AN-20	20TP
KM75C02AN-25	25TP
KM75C02AN-35	35TP
KM75C02AN-50	50TP
KM75C02AN-80	80TP
KM75C03A	IDT7203SA/LA
KM75C03AP-25	25P
KM75C03AP-35	35P
KM75C03AP-50	50P
KM75C03AP-80	80P
KM75C03AJ-25	25J
KM75C03AJ-35	35J
KM75C03AJ-50	50J
KM75C03AJ-80	80J
KM75C03AN-25	25TP
KM75C03AN-35	35TP
KM75C03AN-50	50TP
KM75C03AN-80	80TP

SHARP	IDT
LH5495	IDT7200L
LH5495D-15	15TP
LH5495D-25	25TP
LH5495D-35	35TP
LH5495U-15	15J
LH5495U-25	25J
LH5495U-35	35J
LH5496	IDT7201L
LH5496-20	20P
LH5496-25	25P
LH5496-35	35P
LH5496-50	50P
LH5496D-15	15TP
LH5496D-20	20TP
LH5496D-25	25TP
LH5496D-35	35TP
LH5496D-50	50TP
LH5496U-15	15J
LH5496U-20	20J
LH5496U-25	25J
LH5496U-35	35J
LH5497	IDT7202L
LH5497-20	20P
LH5497-25	25P
LH5497-35	35P
LH5497-50	50P
LH5497D-20	20TP
LH5497D-25	25TP
LH5497D-35	35TP
LH5497D-50	50TP
LH5497U-20	20J
LH5497U-25	25J
LH5497U-35	35J
LH5498	IDT7203
LH5498-20	20P
LH5498-25	25P
LH5498-35	35P
LH5498-50	50P
LH5498D-20	20TP
LH5498D-25	25TP
LH5498D-35	35TP
LH5498D-50	50TP
LH5498U-20	20J
LH5498U-25	25J
LH5498U-35	35J
LH5499	IDT7204
LH5499-20	20P
LH5499-25	25P
LH5499-35	35P
LH5499-50	50P
LH5499U-20	20J
LH5499U-25	25J
LH5499-U35	35J

Cypress	IDT
CY7C420	IDT7201SA/LA
CY7C420-30PC	25P
CY7C420-40PC	35P
CY7C420-65PC	65P
CY7C420-30DC	25D
CY7C420-40DC	35D
CY7C420-65DC	65D
CY7C420-30DMB	30DB
CY7C420-40DMB	40DB
CY7C420-65DMB	65DB
CY7C421	
CY7C421-30PC	25TP
CY7C421-40PC	35TP
CY7C421-65PC	65TP
CY7C421-30JC	25J
CY7C421-40JC	35J
CY7C421-65JC	65J
CY7C421-30VC	25Y
CY7C421-40VC	35Y
CY7C421-65VC	65Y
CY7C421-30DC	25TC
CY7C421-40DC	35TC
CY7C421-65DC	65TC
CY7C421-30DMB	30TCB
CY7C421-40DMB	40TCB
CY7C421-65DMB	65TCB
CY7C421-30LMB	30LB
CY7C421-40LMB	40LB
CY7C421-65LMB	65LB
CY7C424	IDT7202SA/LA
CY7C424-30PC	25P
CY7C424-40PC	35P
CY7C424-65PC	65P
CY7C424-30DC	25D
CY7C424-40DC	35D
CY7C424-65DC	65D
CY7C424-30DMB	30DB
CY7C424-40DMB	40DB
CY7C424-65DMB	65DB
CY7C425	
CY7C425-30PC	25TP
CY7C425-40PC	35TP
CY7C425-65PC	65TP
CY7C425-30JC	25J
CY7C425-40JC	35J
CY7C425-65JC	65J
CY7C425-30VC	25Y
CY7C425-40VC	35Y
CY7C425-65VC	65Y
CY7C425-30DC	25TC
CY7C425-40DC	35TC
CY7C425-65DC	65TC
CY7C425-30DMB	30TCB
CY7C425-40DMB	40TCB
CY7C425-65DMB	65TCB
CY7C425-30LMB	30LB
CY7C425-40LMB	40LB
CY7C425-65LMB	65LB

Cypress	IDT
CY7C428	IDT7203S/L
CY7C428-20PC	20P
CY7C428-25PC	25P
CY7C428-30PC	25P
CY7C428-40PC	35P
CY7C428-65PC	65P
CY7C428-20DC	20D
CY7C428-25DC	25D
CY7C428-30DC	25D
CY7C428-40DC	35D
CY7C428-65DC	65D
CY7C428-25DMB	20DB
CY7C428-30DMB	30DB
CY7C428-40DMB	40DB
CY7C428-65DMB	65DB
CY7C429	
CY7C429-20PC	20TP
CY7C429-25PC	25TP
CY7C429-30PC	25TP
CY7C429-40PC	35TP
CY7C429-65PC	65TP
CY7C429-20JC	20J
CY7C429-25JC	25J
CY7C429-30JC	25J
CY7C429-40JC	35J
CY7C429-65JC	65J
CY7C429-20DC	20TC
CY7C429-25DC	25TC
CY7C429-30DC	25TC
CY7C429-40DC	35TC
CY7C429-65DC	65TC
CY7C429-20VC	20Y
CY7C429-25VC	25Y
CY7C429-30VC	30Y
CY7C429-40VC	40Y
CY7C429-65VC	65Y
CY7C429-25DMB	20TCB
CY7C429-30DMB	30TCB
CY7C429-40DMB	40TCB
CY7C429-65DMB	65TCB
CY7C432/433	IDT7204S
CY7C432-25PC	25P
CY7C432-30PC	25P
CY7C432-40PC	35P
CY7C432-65PC	65P
CY7C432-25DC	25D
CY7C432-30DC	25D
CY7C432-40DC	35D
CY7C432-65DC	65D
CY7C432-25DMB	25DB
CY7C432-30DMB	30DB
CY7C432-40DMB	40DB
CY7C432-65DMB	65DB
CY7C433	
CY7C433-25PC	25TP
CY7C433-30PC	25TP
CY7C433-40PC	35TP
CY7C433-65PC	65TP

Cypress	IDT
CY7C433	IDT7204S
CY7C433-25VC	25Y
CY7C433-30VC	35Y
CY7C433-40VC	40Y
CY7C432/433	IDT7204S
CY7C433-65VC	65Y
CY7C433-25JC	25J
CY7C433-30JC	25J
CY7C433-40JC	35J
CY7C433-65JC	65J
CY7C433-30DMB	30TCB
CY7C433-40DMB	40TCB
CY7C433-65DMB	65TCB
CY7C433-30LMB	30LB
CY7C433-40LMB	40LB
CY7C433-65LMB	65LB
CY3341	IDT72401L
CY3341-2PC	10P
CY3341PC	10P
CY3341-2DC	10D
CY3341DC	10D
CY3341-2DMB	10DB
CY3341DMB	10DB
CY7C401	
CY7C401-25PC	25P
CY7C401-15PC	15P
CY7C401-10PC	10P
CY7C401-5PC	10P
CY7C401-25DC	25D
CY7C401-15DC	15D
CY7C401-10DC	10D
CY7C401-5DC	10D
CY7C401-25DMB	25DB
CY7C401-15DMB	15DB
CY7C401-10DMB	10DB
CY7C402	IDT72402L
CY7C402-25PC	25P
CY7C402-15PC	15P
CY7C402-10PC	10P
CY7C402-5PC	10P
CY7C402-25DC	25D
CY7C402-15DC	15D
CY7C402-10DC	10D
CY7C402-5DC	10D
CY7C402-25DMB	25DB
CY7C402-15DMB	15DB
CY7C402-10DMB	10DB
CY7C403	IDT72403L
CY7C403-25PC	25P
CY7C403-15PC	15P
CY7C403-10PC	10P
CY7C403-25DC	25D
CY7C403-15DC	15D
CY7C403-10DC	10D
CY7C403-25DMB	25DB
CY7C403-15DMB	15DB
CY7C403-10DMB	10DB

Cypress	IDT
CY7C404	IDT72404L
CY7C404-25PC	25P
CY7C404-15PC	15P
CY7C404-10PC	10P
CY7C404-25DC	25D
CY7C404-15DC	15D
CY7C404-10DC	10D
CY7C404-25DMB	25DB
CY7C404-15DMB	15DB
CY7C404-10DMB	10DB

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SMP
CROSS REFERENCE GUIDE

CYPRESS	IDT
CY7C130-35PC	IDT7130SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
35LC	35L48
45LC	45L48
55LC	55L48
45DMB	45CB
55DMB	55CB
45LMB	45L48B
55LMB	55L48B
CY7C131-25JC	IDT7130SA25J
35JC	35J
45JC	45J
55JC	55J
35LC	35L52
45LC	45L52
55LC	55L52
45LMB	45L52B
55LMB	55L52B
CY7C132-35PC	IDT7132SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
35LC	35L48
45LC	45L48
55LC	55L48
45DMB	45CB
55DMB	55CB
45LMB	45L48B
55LMB	55L48B
CY7C136-25JC	IDT71321SA25J
35JC	35J
45JC	45J
55JC	55J
35LC	35L52
45LC	45L52
55LC	55L52
45LMB	45L52B
55LMB	55L52B

CYPRESS	IDT
CY7C140-35PC	IDT7140SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
35LC	35L48
45LC	45L48
55LC	55L48
45DMB	45CB
55DMB	55CB
45LMB	45L48B
55LMB	55L48B
CY7C141-25JC	IDT7140SA25J
35JC	35J
45JC	45J
55JC	55J
35LC	35L52
45LC	45L52
55LC	55L52
45LMB	45L52B
55LMB	55L52B
CY7C142-35PC	IDT7142SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
35LC	35L48
45LC	45L48
55LC	55L48
45DMB	45CB
55DMB	55CB
45LMB	45L48B
55LMB	55L48B
CY7C146-25JC	IDT71421SA25J
35JC	35J
45JC	45J
55JC	55J
35LC	35L52
45LC	45L52
55LC	55L52
45LMB	45L52B
55LMB	55L52B

AMD	IDT
AM2130-55PC	IDT7130SA55P
70PC	70P
10PC	100P
55DC	55C
70DC	70C
10DC	100C
70/BXC	70CB
10/BXC	100CB
12/BXC	120CB

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SSD
CROSS REFERENCE GUIDE

CYPRESS/MULTICHIP P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	CYPRESS/MULTICHIP ORG/PACKAGE
CYM1240HD-35MB	7M4042S35CB		1 MEG (256K X 4) JEDEC
CYM1240HD-45MB	7M4042S45CB		28 PIN DIP
CYM1420HD-25C	8M824S25C	8MB824S25P	1 MEG (128K X 8) JEDEC
CYM1420HD-30C	8M824S30C	8MB824S30P	32 PIN DIP
CYM1420PD-30C	8M824S30N	8MB824S30P	
CYM1420HD-35C	8M824S35C	8MB824S35P	
CYM1420PD-35C	8M824S35N	8MB824S35P	
CYM1420HD-45C	8M824S45C	8MB824S45P	
CYM1420PD-45C	8M824S45N	8MB824S45P	
CYM1420HD-55C	8M824S50C		
	8M824S50N		
CYM1420HD-70C	8M824S70C		
	8M824S70N		
CYM1420HD-35MB	8M824S40CB		
CYM1420HD-45MB	8M824S45CB		
CYM1420HD-55MB	8M824S55CB		
CYM1421HD-70MB	8M824S70CB		1 MEG (128K X 8) JEDEC
CYM1421HD-85MB	8M824S85CB		32 PIN DIP
CYM1421HD-100MB	8M824S100CB		[Low power version]
CYM1422PS-30C	8MP824S30S		1 MEG (128K X 8)
CYM1422PS-35C	8MP824S35S		30 PIN SIP
CYM1422PS-45C	8MP824S40S		
CYM1422PS-55C	8MP824S50S		
CYM1441PZ-25C		7MP4034S25Z	2 MEG (256K X 8) JEDEC
CYM1441PZ-35C		7MP4034S35Z	60 PIN ZIP
CYM1441PZ-45C		7MP4034S45Z	
CYM1460PS-35C	7MP4008S35S		4 MEG (512K X 8)
CYM1460PS-45C	7MP4008S45S		36 PIN SIP
CYM1460PS-55C	7MP4008S55S		
CYM1460PS-70C	7MP4008S70S		
CYM1461PS-70C	7MP4058L70S	7MP4008S70S	4 MEG (512K X 8)
CYM1461PS-85C	7MP4058L85S	7MP4008L85S	36 PIN SIP
CYM1461PS-100C	7MP4058L100S	7MP4008L100S	
CYM1464PD-25C	7MB4048S25P		4 MEG (512K X 8) JEDEC
CYM1464PD-30C	7MB4048S30P		32 PIN DIP
CYM1464PD-35C	7MB4048S35P		
CYM1464PD-45C	7MB4048S45P		
CYM1464PD-55C	7MB4048S55P		
CYM1464PD-70C	7M4048L70N		
CYM1465PD-85C	7M4048L85N		4 MEG (512K X 8) JEDEC
CYM1465PD-100C	7M4048L100N		32 PIN DIP
CYM1465PD-120C	7M4048L120N		
CYM1465PD-150C	7M4048L120N		
CYM1466HD-35C	7M4048S35C		4 MEG (512K X 8) JEDEC
CYM1466LHD-35C	7M4048L35C		32 PIN DIP
CYM1466HD-35MB	7M4048S35CB		
CYM1466LHD-35MB	7M4048L35CB		
CYM1466HD-45C	7M4048S45C		
CYM1466LHD-45C	7M4048L45C		
CYM1466HD-45MB	7M4048S45CB		
CYM1466LHD-45MB	7M4048L45CB		
CYM1466HD-55C	7M4048S55C		
CYM1466LHD-55C	7M4048L55C		
CYM1466HD-55MB	7M4048S55CB		
CYM1466LHD-55MB	7M4048L55CB		

CYM1466HD-70C	7M4048S70C		4 MEG (512K X 8) JEDEC
CYM1466LHD-70C	7M4048L70C		32 PIN DIP
CYM1466HD-70MB	7M4048S70CB		
CYM1466LHD-70MB	7M4048L70CB		
CYM1466HD-85C	7M4048S85C		
CYM1466LHD-85C	7M4048L85C		
CYM1466HD-85MB	7M4048S85CB		
CYM1466LHD-85MB	7M4048L85CB		
CYM1466HD-100C	7M4048S100C		
CYM1466LHD-100C	7M4048L100C		
CYM1466HD-100MB	7M4048S100CB		
CYM1466LHD-100MB	7M4048L100CB		
CYM1466HD-120C	7M4048S120C		
CYM1466LHD-120C	7M4048L120C		
CYM1466HD-120MB	7M4048S120CB		
CYM1466LHD-120MB	7M4048L120CB		
CYM1540PS-30C		7MB4040S25P	2 MEG (256K X 9)
CYM1540PS-35C		7MB4040S35P	44 PIN SIP
CYM1540PS-45C		7MB4040S45P	
CYM1541PD-25C	7MB4040S25P		2 MEG (256K X 9)
CYM1541PD-35C	7MB4040S35P		44 PIN DIP
CYM1541PD-45C	7MB4040S45P		
CYM1610HD-20C		7MC4005S20CV	256K (16K X 16)
CYM1610HD-25C		7MC4005S25CV	40 PIN DIP
CYM1610HD-35C		7MC4005S35CV	
CYM1610HD-45C	8M656S40C		
CYM1610HD-50C	8M656S50C		
CYM1610HD-25MB		7MC4005S25CVB	
CYM1610HD-35MB		7MC4005S35CVB	
CYM1610HD-45MB	8M656S40CB		
CYM1610HD-50MB	8M656S50CB		
CYM1611HV-20C	7MC4005S20CV		256K (16K X 16)
CYM1611HV-25C	7MC4005S25CV		36 PIN DSIP
CYM1611HV-30C	7MC4005S30CV		
CYM1611HV-35C	7MC4005S35CV		
CYM1611HV-45C	7MC4005S45CV		
CYM1611PV-20C	7MC4005S20CV		
CYM1611PV-25C	7MC4005S25CV		
CYM1611PV-30C	7MC4005S30CV		
CYM1611PV-35C	7MC4005S35CV		
CYM1611PV-45C	7MC4005S45CV		
CYM1620HD-30C	8M624S30C		1 MEG (64K X 16) JEDEC
CYM1620HD-35C	8M624S35C		40 PIN DIP
CYM1620HD-45C	8M624S45C		
CYM1620HD-50C	8M624S50C		
CYM1620HD-45MB	8M624S45CB		
CYM1620HD-50MB	8M624S50CB		
CYM1621HD-25C	7M624S25C		1 MEG (64K X 16),
CYM1621HD-30C	7M624S30C		(128K X 8), (256K X 4)
CYM1621HD-35C	7M624S35C		40 PIN DIP
CYM1621HD-45C	7M624S45C		
CYM1621HD-25MB	7M624S25CB		
CYM1621HD-30MB	7M624S30CB		
CYM1621HD-35MB	7M624S35CB		
CYM1621HD-45MB	7M624S45CB		
CYM1622HV-20C	7MP4027S20V		1 MEG (64K X 16)
CYM1622HV-25C	7MP4027S25V		40 PIN DSIP
CYM1622HV-35C	7MP4027S35V		
CYM1622HV-45C	7MP4027S45V		

CYM1623HD-70MB	8M624S70CB		1 MEG (64K X 16) JEDEC
CYM1623HD-85MB	8M624S85CB		40 PIN DIP
CYM1623HD-100MB	8M624S100CB		[low power version]
CYM1624PV-20C	7MP4028S20V		1 MEG (64K X 16)
CYM1624PV-25C	7MP4028S25V		40 PIN DSIP
CYM1624PV-35C	7MP4028S35V		
CYM1624PV-45C	7MP4028S45V		
CYM1626PS-30C	8MP624S30S		1 MEG (64K X 16)
CYM1626PS-35C	8MP624S35S		40 PIN SIP
CYM1626PS-45C	8MP624S45S		
CYM1641HD-25C	7M4016S25C		4 MEG (256K X 16)
CYM1641HD-35C	7M4016S35C		48 PIN DIP
CYM1641HD-45C	7M4016S45C		
CYM1641HD-55C	7M4016S55C		
CYM1641HD-35MB	7M4016S35CB		
CYM1641HD-45MB	7M4016S45CB		
CYM1641HD-55MB	7M4016S55CB		
CYM1821PZ-12C	7MP4031B12Z		512K (16K X 32) JEDEC
CYM1821PZ-15C	7MP4031S15Z		64 FR-4 ZIP
CYM1821PZ-20C	7MP4031S20Z		
CYM1821PZ-25C	7MP4031S25Z		
CYM1821PZ-35C	7MP4031S35Z		
CYM1821PZ-45C	7MP4031S35Z		
CYM1822HV-20C	7MC4032S20CV		512K (16K X 32)
CYM1822HV-25C	7MC4032S25CV		88 PIN DSIP
CYM1822HV-30C	7MC4032S30CV		
CYM1822HV-35C	7MC4032S35CV		
CYM1822HV-45C	7MC4032S45CV		
CYM1828HG-20C	7M4003S20CH		1 MEG (32K X 32)
CYM1828HG-25C	7M4003S25CH		66 PIN HIP
CYM1828HG-25MB	7M4003S25CHB		
CYM1828HG-30C	7M4003S30CH		
CYM1828HG-30MB	7M4003S30CHB		
CYM1828HG-35C	7M4003S35CH		
CYM1828HG-35MB	7M4003S35CHB		
CYM1828HG-45C	7M4003S45CH		
CYM1828HG-45MB	7M4003S45CHB		
CYM1828HG-55C	7M4003S50CH		
CYM1828HG-55MB	7M4003S50CHB		
CYM1828HG-70C	7M4003S50CH		
CYM1828HG-70MB	7M4003S70CHB		
CYM1830HD-25C	7M4017S25C		2 MEG (64K X 32)
CYM1830HD-30C	7M4017S30C		60 PIN DIP
CYM1830HD-35C	7M4017S35C		
CYM1830HD-45C	7M4017S45C		
CYM1830HD-55C	7M4017S50C		
CYM1830HD-35MB	7M4017S35CB		
CYM1830HD-45MB	7M4017S45CB		
CYM1830HD-55MB	7M4017S50CB		
CYM1831PZ-15C	7MP4036B15Z		2 MEG (64K X 32) JEDEC
CYM1831PZ-20C	7MP4036S20Z		64 PIN ZIP
CYM1831PZ-25C	7MP4036S25Z		
CYM1831PZ-30C	7MP4036S30Z		
CYM1831PZ-35C	7MP4036S35Z		
CYM1831PZ-45C	7MP4036S35Z		
CYM1831PM-15C	7MP4036B15M		2 MEG (64K X 32) JEDEC
CYM1831PM-20C	7MP4036S20M		64 PIN SIMM
CYM1831PM-25C	7MP4036S25M		
CYM1831PM-30C	7MP4036S30M		
CYM1831PM-35C	7MP4036S35M		
CYM1831PM-45C	7MP4036S35M		

CYM1832PZ-25C		7MP4036S25Z	2 MEG (64K X 32)
CYM1832PZ-35C		7MP4036S35Z	60 PIN ZIP
CYM1832PZ-45C		7MP4036S35Z	
CYM1832PZ-55C		7MP4036S35Z	
CYM1838HG-20C	7M4013S20CH		4 MEG (128K X 32)
CYM1838HG-25C	7M4013S25CH		66 PIN HIP
CYM1838HG-25MB	7M4013S25CHB		
CYM1838HG-30C	7M4013S30CH		
CYM1838HG-30MB	7M4013S30CHB		
CYM1838HG-35C	7M4013S35CH		
CYM1838HG-35MB	7M4013S35CHB		
CYM1838HG-45C	7M4013S45CH		
CYM1838HG-45MB	7M4013S45CHB		
CYM1838HG-55C	7M4013S50CH		
CYM1838HG-55MB	7M4013S50CHB		
CYM1838HG-70C	7M4013S50CH		
CYM1838HG-70MB	7M4013S70CHB		
CYM1840PD-20C	7MB4067S20P		8 MEG (256K X 32)
CYM1840PD-25C	7MB4067S25P		60 PIN DIP
CYM1840HD-25C		7MB4067S25P	
CYM1840PD-30C	7MB4067S30P		
CYM1840HD-30C		7MB4067S30P	
CYM1840PD-35C	7MB4067S35P		
CYM1840HD-35C		7MB4067S35P	
CYM1840PD-45C	7MB4067S45P		
CYM1840HD-45C		7MB4067S45P	
CYM1840PD-55C	7MB4067S45P		
CYM1840HD-55C		7MB4067S45P	
CYM1841PZ-20C	7MP4045S20Z		8 MEG (256K X 32) JEDEC
CYM1841PZ-25C	7MP4045S25Z		64 PIN ZIP
CYM1841PZ-30C	7MP4045S30Z		
CYM1841PZ-35C	7MP4045S35Z		
CYM1841PZ-45C	7MP4045S45Z		
CYM1841PZ-55C	7MP4045S55Z		
CYM1841PM-20C	7MP4045S20M		8 MEG (256K X 32) JEDEC
CYM1841PM-25C	7MP4045S25M		64 PIN SIMM
CYM1841PM-30C	7MP4045S30M		
CYM1841PM-35C	7MP4045S35M		
CYM1841PM-45C	7MP4045S45M		
CYM1841PM-55C	7MP4045S55M		
CYM4210HD-30C	7205SL25P		8K X 9 FIFO
CYM4210HD-40C	7205SL25P		28 PIN DIP
CYM4210HD-50C	7205SL50P		
CYM4210HD-60C	7205SL50P		
CYM4210HD-85C	7205SL80P		
CYM4210HD-40MB	7205SL30DB		
CYM4210HD-50MB	7205SL50DB		
CYM4210HD-60MB	7205SL50DB		
CYM4210HD-85MB	7205SL80DB		
CYM4220HD-30C	7206SL25P		16K X 9 FIFO
CYM4220HD-40C	7206SL25P		28 PIN DIP
CYM4220HD-50C	7206SL50P		
CYM4220HD-60C	7206SL50P		
CYM4220HD-85C	7206SL80P		
CYM4220HD-40MB	7M206S40CB		
CYM4220HD-50MB	7M206S50CB		
CYM4220HD-60MB	7M206S60CB		
CYM4220HD-85MB	7M206S85CB		

DENSE-PAC P/N	IDT P/N DIRECT EQUIVALENT	IDT P/N SIMILAR PART	DENSE-PAC ORG/PACKAGE
DPS128M8N-70	71M024-70		1M (128K X 8) Monolithic
DPS128M8N-85	71M024-85		32 PIN DIP
DPS128M8N-100	71M024-100		
DPS128M8N-120	71M024-120		
DPS128M8N-150	71M024-120		
DPS16X5-XXX	7MP564		80K (16K X 5)
	7MP564		28 PIN SIP
DPS16X17-25	7MC4005S25CV		256K (16K X 16)
DPS16X17-35	7MC4005S35CV		36 PIN DSIP
DPS16X17-45	7MC4005S45CV		
DPS16X17-55	7MC4005S55CV		
DPS257-XXX	7M656		256K (16K X 16)
	7M656		(32K X 8)
	7M656		(64K X 4)
	7M656		40 PIN DIP
DPS1024-25C		7M624	1 MEG (256K X 4),
DPS1024-35C		7M624	(128K X 8), (64K X 16)
DPS1024-45C		7M624	42 PIN DIP
DPS1024-55C		7M624	
DPS1026-25C		7M624	1 MEG (256K X 4),
DPS1026-35C		7M624	(128K X 8), (64K X 16)
DPS1026-45C		7M624	40 PIN DIP
DPS1026-55C		7M624	
DPS1027-25C	7M624S25C		1 MEG (256K X 4),
DPS1027-35C	7M624S35C		(128K X 8), (64K X 16)
DPS1027-45C	7M624S45C		40 PIN DIP
DPS1027-55C	7M624S55C		
DPS128X32V3-70	7M4013S70CHB		4 MEG (128K X 32)
DPS128X32V3-85	7M4013S85CHB		66 PIN HIP
DPS128X32V3-100	7M4013S100CHB		
DPS128X32V3-120	7M4013S100CHB		
DPS128X32V3-150	7M4013S100CHB		
DPS2516-25C		7M4016	4 MEG (256K X 16)
DPS2516-35C		7M4016	44 PIN DIP
DPS2516-45C		7M4016	
DPS2516-55C		7M4016	
DPS4648-85C		7M812	512K (64K X 8)
DPS4648-100C		7M812	32 PIN DIP
DPS4648-120C		7M812	
DPS4648-150C		7M812	
DPS5124-45C		7MP4034	2 MEG (512K X 4),
DPS5124-55C		7MP4034	(256K X 8)
			54 PIN DIP
DPS6432-35C	7M4017S35C		2 MEG (64K X 32)
DPS6432-45C	7M4017S45C		60 PIN DIP
DPS6432-55C	7M4017S55C		
DPS6432-70C	7M4017S70C		
DPS6433-85C		7MP4034, 7M4017	2 MEG (64K X 32)
DPS6433-100C		7MP4034, 7M4017	(128K X 16), (256K X 8)
DPS6433-120C		7MP4034, 7M4017	60 PIN DIP
DPS6433-150C		7MP4034, 7M4017	[low power version]
DPS6433-55C		7M4017S55C	2 MEG (64K X 32)
DPS6433-70C		7M4017S70C	60 PIN DIP
DPS6433-100C		7M4017S70C	[low power version]
DPS8645-XXX	7MP456		256K (64K X 4)
	7MP456		28 PIN SIP

DPS8808-XXX	7M864		64K (8K X 8)
	7M864		28 PIN DIP
DPS8M612-85C	8M612S85C		512K (32K X 16)
DPS8M612-100C	8M612S100C		40 PIN DIP
DPS8M612-120C	8M612S100C		
DPS8M612-150C	8M612S100C		
DPS8M624-85C	8M624S85C		1 MEG (64K X 16)
DPS8M624-100C	8M624S100C		40 PIN DIP
DPS8M624-120C	8M624S100C		
DPS8M624-150C	8M624S100C		
DPS8M656-35C		8M656S40C	256K (16K X 16)
DPS8M656-40C	8M656S40C		40 PIN DIP
DPS8M656-70C	8M656S70C		
DPS10241-25C		7MC4001S35C	1 MEG (1024K X 1)
DPS10241-35C	7MC4001S35CS		30 PIN SIP
DPS10241-45C	7MC4001S45CS		
DPS10241-55C	7MC4001S55CS		
DPS40256-XXX	8M856		256K (32K X 8)
	8M856		28 PIN DIP
DPS41257-XXX	8M856		256K (32K X 8)
	8M856		28 PIN DIP
DPS41288-70C	8M824S70C	8M824L70N	1 MEG (128K X 8)
DPS41288-85C		8M824L85N	32 PIN DIP
DPS41288-100C		8M824L100N	
DPS45128-85C		7MP4008	4 MEG (512K X 8)
DPS45128-100C		7MP4008	48 PIN DIP
DPS45128-120C		7MP4008	
DPS45128-150C		7MP4008	
DPS45129-85C	7M4016S55C		4 MEG (256K X 16)
DPS45129-100C	7M4016S55C		48 PIN DIP
DPS45129-120C	7M4016S55C		
DPS45129-150C	7M4016S55C		
DPS512S8-85C	7M4048L85N		4 MEG (512K X 8)
DPS512S8-100C	7M4048L100N		32 PIN DIP
DPS512S8-120C	7M4048L120N		
DPS512S8-150C	7M4048L120N		
DPS3232V	7M4003SXXCH		1 MEG (32K X 32)
			66 PIN HIP
DPE3232V	7M7004SXXCH		1 MEG (32K X 32) EEPROM
			66 PIN HIP
EDI P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**EDI ORG/PACKAGE**
EDI88128-70	71M025-70		1M (128K X 8) Monolithic
EDI88128-85	71M025-85		32 PIN DIP (1 CS)
EDI88128-100	71M025-100		
EDI88130-70	71M024-70		1M (128K X 8) Monolithic
EDI88130-85	71M024-85		32 PIN DIP (2 CS)
EDI88130-100	71M024-100		
EDI8M8128C35C6C	8M824S35C	8M824S35N, 8MP824S35S	1 MEG (128K X 8) JEDEC
EDI8M8128C45C6C	8M824S45C	8M824S45N, 8MP824S45S	32 PIN DIP
EDI8M8128C55C6C	8M824S50C	8M824S50N, 8MP824S50S	
EDI8M8128C45C6B	8M824S45CB		
EDI8M8128C55C6B	8M824S50CB		
EDI8M8128C70C6B	8M824S70CB		
EDI8M8128C60P6C	8M824S60N	8M824S60C, 8MP824S60S	1 MEG (128K X 8) JEDEC
EDI8M8128C70P6C	8M824L70N	8M824S70C, 8MP824L70S	32 PIN DIP
EDI8M8128C100P6C	8M824L100N	8MP824L100S	
EDI8M8128C120P6C	8M824L100N	8MP824L100S	
EDI8M8128C150P6C	8M824L100N	8MP824L100S	

EDI8M8128C85C6B	8M824S85CB		1 MEG (128K X 8) JEDEC
EDI8M8128C1006CB	8M824S100CB		32 PIN DIP
EDI8M8128C1206CB	8M824S100CB		[low power version]
EDI8M8128C1506CB	8M824S100CB		
EDI8M8256C70P6C	7M4068L70N		2 MEG (256K X 8) JEDEC
EDI8M8256C85P6C	7M4068L85N		32 PIN DIP
EDI8M8256C100P6C	7M4068L100N		
EDI8M8256C120P6C	7M4068L120N		
EDI8M8256C150P6C	7M4068L120N		
EDI8F8257C85B6C	7M4068L85N		2 MEG (256K X 8) JEDEC
EDI8F8257C100B6C	7M4068L100N		32 PIN DIP
EDI8F8257C120B6C	7M4068L120N		
EDI8F8257C150B6C	7M4068L120N		
EDI8M8257C85P6C	7M4068L85N		2 MEG (256K X 8) JEDEC
EDI8M8257C100P6C	7M4068L100N		32 PIN DIP
EDI8M8257C120P6C	7M4068L120N		
EDI8M8257C150P6C	7M4068L120N		
EDI8F8257C45MSC		7MP4034S45Z	2 MEG (256K X 8)
EDI8F8257C55MSC		7MP4034S45Z	36 PIN SIP
EDI8F8257C70MSC		7MP4034S45Z	
EDI8F8258C45MSC		7MP4034S45Z	2 MEG (256K X 8)
EDI8F8258C55MSC		7MP4034S45Z	36 PIN SIP
EDI8F8258C70MSC		7MP4034S45Z	
EDI8M8512C85P6C	7M4048L85N		4 MEG (512K X 8) JEDEC
EDI8M8512C100P6C	7M4048L100N		32 PIN DIP
EDI8M8512C120P6C	7M4048L120N		
EDI8M8512C150P6C	7M4048L120N		
EDI8M8512C85C6B	7M4048S85CB		
EDI8M8512C100C6B	7M4048S100CB		
EDI8M8512C120C6B	7M4048S120CB		
EDI8M8512C150C6B	7M4048S120CB		
EDI8F8512C25M6C	7MB4048S25P		4 MEG (512K X 8) JEDEC
EDI8F8512C30M6C	7MB4048S30P		32 PIN DIP
EDI8F8512C35M6C	7MB4048S35P		
EDI8F8512C45M6C	7MB4048S45P		
EDI8F8512C55M6C	7MB4048S55P		
EDI8F8512C70M6C	7M4048L70N		
EDI8M8512C30M6B	7M4048S30CB		
EDI8M8512C35M6B	7M4048S35CB		
EDI8M8512C45M6B	7M4048S45CB		
EDI8M8512C55M6B	7M4048S55CB		
EDI8M8512C70M6B	7M4048S70CB		
EDI8F1664C100PC	8M624S70C	8MP624L100S	1 MEG (64K X 16)
EDI8F1664C120PC	8M624S70C	8MP624L100S	40 PIN DIP
EDI8F1664C150PC	8M624S70C	8MP624L100S	
EDH816H16C-25CC-Z	7MC4005S25CV		256K (16K X 16)
EDH816H16C-35CC-Z	7MC4005S35CV		36 PIN DSIP
EDH816H16C-45CC-Z	7MC4005S45CV		
EDH816H16C-25CMHR-Z	7MC4005S25CVB		
EDH816H16C-35CMHR-Z	7MC4005S35CVB		
EDH816H16C-45CMHR-Z	7MC4005S45CVB		
EDI8M1664C45C6C	8M624S40C		1 MEG (64K X 16) JEDEC
EDI8M1664C55C6C	8M624S50C		40 PIN DIP
EDI8M1664C60C6C	8M624S60C		
EDI8M1664C70C6C	8M624S70C		
EDI8M1664C85C6C	8M624S850C		
EDI8M1664C100C6C	8M624S100C		
EDI8M1664C55C6B	8M624S50CB		
EDI8M1664C60C6B	8M624S60CB		
EDI8M1664C70C6B	8M624S70CB		
EDI8M1664C85C6B	8M624S85CB		
EDI8M1664C100C6B	8M624S100CB		

EDI8M1664C25C9C	7M624S25C		1 MEG (64K X 16)
EDI8M1664C35C9C	7M624S35C		40 PIN DIP
EDI8M1664C45C9C	7M624S45C		
EDI8M1664C55C9C	7M624S55C		
EDI8M1664C70C9C	7M624S70C		
EDI8M1664C25C9B	7M624S25CB		
EDI8M1664C35C9B	7M624S35CB		
EDI8M1664C45C9B	7M624S45CB		
EDI8M1664C55C9B	7M624S55CB		
EDI8M1664C70C9B	7M624S70CB		
EDI8M16256C25C9C	7M4016S25C		4 MEG (256K X 16)
EDI8M16256C35C9C	7M4016S35C		48 PIN DIP
EDI8M16256C45C9C	7M4016S45C		
EDI8M16256C55C9C	7M4016S55C		
EDI8M16256C70C9C	7M4016S55C		
EDI8M16256C35C9B	7M4016S35CB		
EDI8M16256C45C9B	7M4016S45CB		
EDI8M16256C55C9B	7M4016S55CB		
EDI8M16256C70C9B	7M4016S55CB		
EDI8M16257C35M6C		7MB4066S35P	4 MEG (256K X 16)
EDI8M16257C45M6C		7MB4066S45P	40 PIN DIP
EDI8M16257C55M6C		7MB4066S55P	
EDI8M16257C70M6C		7MB4066S55P	
EDI8F3264C25M6C		7M4017S25C	2 MEG (64K X 32)
EDI8F3264C35M6C	7M4017S35C		60 PIN DIP
EDI8F3264C45M6C	7M4017S45C		
EDI8F3264C55M6C	7M4017S50C		
EDI8M3264C25C6B	7M4017S30CB		
EDI8M3264C35C6B	7M4017S35CB		
EDI8M3264C45C6B	7M4017S45CB		
EDI8M3264C55C6B	7M4017S50CB		
EDI8F3264C15MZC	7MP4036B15Z		2 MEG (64K X 32) JEDEC
EDI8F3264C20MZC	7MP4036S20Z		64 PIN ZIP
EDI8F3264C25MZC	7MP4036S25Z		
EDI8F3264C35MZC	7MP4036S30Z		
EDI8F3264C45MZC	7MP4036S35Z		
EDI8F3264C55MZC	7MP4036S35Z		
EDI8F32128C15BZC	7MP4095B15Z		4 MEG (128K X 32) JEDEC
EDI8F32128C20BZC	7MP4095S20Z		64 PIN ZIP
EDI8F32128C25BZC	7MP4095S25Z		
EDI8F32128C35BZC	7MP4095S35Z		
EDI8F32128C45BZC	7MP4095S45Z		
EDI8F32128C15BMC	7MP4095B15M		4 MEG (128K X 32) JEDEC
EDI8F32128C20BMC	7MP4095S20M		64 PIN SIMM
EDI8F32128C25BMC	7MP4095S25M		
EDI8F32128C35BMC	7MP4095S35M		
EDI8F32128C45BMC	7MP4095S45M		
EDI8F32256C20B6C	7MB4067S20P		8 MEG (256K X 32)
EDI8F32256C25B6C	7MB4067S25P		60 PIN DIP
EDI8F32256C30B6C	7MB4067S30P		
EDI8F32256C35B6C	7MB4067S35P		
EDI8F32256C45B6C	7MB4067S45P		
EDI8F32256C55B6C	7MB4067S55P		
EDI8F32256C70B6C	7MB4067S55P		
EDI8F32256C20BZC	7MP4045S20Z		8 MEG (256K X 32) JEDEC
EDI8F32256C25BZC	7MP4045S25Z		64 PIN ZIP
EDI8F32256C35BZC	7MP4045S35Z		
EDI8F32256C45BZC	7MP4045S45Z		
EDI8F32256C55BZC	7MP4045S55Z		

EDI8F32256C20BMC	7MP4045S20M		8 MEG (256K X 32) JEDEC
EDI8F32256C25BMC	7MP4045S25M		64 PIN SIMM
EDI8F32256C35BMC	7MP4045S35M		
EDI8F32256C45BMC	7MP4045S45M		
EDI8F32256C55BMC	7MP4045S55M		
EDI8M8130C50CC		8M824	1 MEG (128K X 8)
EDI8M8130C60CC		8M824	32 PIN DIP
EDI8M8130C70CC		8M824	[dual chip enable]
EDI8M8130C80CC		8M824	
EDI8M8130C90CC		8M824	
EDI8M8130C100CC		8M824	
EDI8M8130C120CC		8M824	
EDI8M8130C150CC		8M824	
EDI8M8130C50CB		8M824	
EDI8M8130C60CB		8M824	
EDI8M8130C70CB		8M824	
EDI8M8130C80CB		8M824	
EDI8M8130C90CB		8M824	
EDI8M8130C100CB		8M824	
EDI8M8130C120CB		8M824	
EDI8M8130C150CB		8M824	
EDI8M8130P90CB		8M824	1 MEG (128K X 8)
EDI8M8130P100CB		8M824	32 PIN DIP
EDI8M8130P120CB		8M824	[dual chip enable]
EDI8M8130P150CB		8M824	[low power version]
EDI8M864C50CC		7M812	512K (64K X 8)
EDI8M864C60CC		7M812	32 PIN DIP
EDI8M864C70CC		7M812	
EDI8M864C80CC		7M812	
EDI8M864C90CC		7M812	
EDI8M864C100CC		7M812	
EDI8M864C120CC		7M812	
EDI8M864C150CC		7M812	
EDI8M864C50CB		7M812	
EDI8M864C60CB		7M812	
EDI8M864C70CB		7M812	
EDI8M864C80CB		7M812	
EDI8M864C90CB		7M812	
EDI8M864C100CB		7M812	
EDI8M864C120CB		7M812	
EDI8M864C150CB		7M812	
EDH81H256C-55	7MC156S55CS	7MP156	256K (256K X 1)
EDH81H256C-70	7MC156S70CS		28 PIN SIP
EDH84H64C-35CC-D3		7MP456	256K (64K X 4)
EDH84H64C-45CC-D3			24 PIN DIP
EDH84H64C-55CC-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CMHR-D3			
EDH84H64C-35CC-S	7MP456S35S		256K (64K X 4)
EDH84H64C-45CC-S	7MP456S45S		28 PIN SIP
EDH84H64C-55CC-S	7MP456S55S		

EDH8808HC-55CMHR		8M864L55CB	64K (8K X 8)
EDH8808HC-70CMHR		8M864L75CB	28 PIN DIP
EDH8808C-10CMHR	8M864L85CB		
EDH8808C-12CMHR	8M864L120CB		
EDH8808C-15CMHR	8M864L150CB		
EDH8808CL-20CMHR	8M864L150CB		
EDH8808CL-25CMHR	8M864L150CB		
EDH8808A-10CMHR	7M864L85CB		
EDH8808A-12CMHR	7M864L120CB		
EDH8088A-15CMHR	7M864L150CB		
EDH8808AL-20CMHR	7M864L150CB		
EDH8808AL-25CMHR	7M864L150CB		
EDH8832C-12C	8M856L85C	7M856S	256K (32K X 8)
EDH8832C-15C	8M856L85C	7M856S	28 PIN DIP
EDH8832C-20C	8M856L85C	7M856S	
EDH8832C-12CMHR	8M856L100CB	7M856S	
EDH8832C-15CMHR	8M856L100CB	7M856S	
EDH8832C-20CMHR	8M856L100CB	7M856S	
EDH8832HC-45CMHR	7M856S45CB	8M856L	256K (32K X 8)
EDH8832HC-55CMHR	7M856S55CB	8M856L	28 PIN DIP
EDH8832HC-70CMHR	7M856S65CB	8M856L	
EDH8832HC-85CMHR	7M856S75CB	8M856L	
INOVA P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**INOVA ORG/PACKAGE**
S128K8-70	71M024-70		1M (128K X 8) Monolithic
S128K8-85	71M024-85		32 PIN DIP (2 CS)
S128K8-100	71M024-100		
S128K8T-70	71M025-70		1M (128K X 8) Monolithic
S128K8T-85	71M025-85		32 PIN DIP (1 CS)
S128K8T-100	71M025-100		
MICRON TECHNOLOGY P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**MICRON TECHNOLOGY ORG/PACKAGE**
MT5C1008-70	71M024-70		1M (128K X 8) Monolithic
			32 PIN DIP
MT4S1288-30	8M824S30C		1 MEG (128K X 8) JEDEC
MT4S1288-35	8M824S35C		32 PIN DIP
MT4S1288-45	8M824S45C		
MT2S3216-30	8M612S30C		512K (32K X 16) JEDEC
MT2S3216-35	8M612S35C		40 PIN DIP
MT2S3216-45	8M612S45C		
MT4S6416-30	8M624S30C		1 MEG (64K X 16) JEDEC
MT4S6416-35	8M624S35C		40 PIN DIP
MT4S6416-45	8M624S45C		
MT8S1632-12	7MP4031B12Z		512K (16K X 32) JEDEC
MT8S1632-15	7MP4031S15Z		64 PIN ZIP
MT8S1632-20	7MP4031S20Z		
MT8S1632-25	7MP4031S25Z		
MT8S1632-30	7MP4031S30Z		
MT8S1632-35	7MP4031S35Z		
MT8S1632-45	7MP4031S35Z		
MT8S6432-15	7MP4036B15Z		2 MEG (64K X 32) JEDEC
MT8S6432-20	7MP4036S20Z		64 PIN ZIP
MT8S6432-25	7MP4036S25Z		
MT8S6432-30	7MP4036S25Z		
MT8S6432-35	7MP4036S35Z		
MT8S6432-45	7MP4036S35Z		

MT4S12832-20	7MP4095S20Z		4 MEG (128K X 32) JEDEC
MT4S12832-25	7MP4095S25Z		64 PIN ZIP
MT4S12832-35	7MP4095S35Z		
MT4S12832-45	7MP4095S45Z		
MT8S25632-20	7MP4045S20Z		8 MEG (256K X 32) JEDEC
MT8S25632-25	7MP4045S25Z		64 PIN ZIP
MT8S25632-35	7MP4045S35Z		
MT8S25632-45	7MP4045S45Z		
MOSAIC P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**MOSAIC ORG/PACKAGE**
MSM8128S-70	71M024-70		1M (128K X 8) Monolithic
MSM8128S-85	71M024-85		32 PIN DIP (2 CS)
MSM8128S-100	71M024-100		
MSM8128S-120	71M024-120		
MSM8128SX-70	71M025-70		1M (128K X 8) Monolithic
MSM8128SX-85	71M025-85		32 PIN DIP (1 CS)
MSM8128SX-100	71M025-100		
MSM8128SX-120	71M025-120		
MS1256CS-25		7MP156, 7MC156	256K (256K X 1)
MS1256CS-35		7MP156, 7MC156	25 PIN SIP
MS8128SLU-55	8M824S50C	8M824SXXN, 8MP824	1 MEG (128K X 8)
MS8128SU-70	8M824S70C		32 PIN DIP
MS8128SL-10	8M824S70C		
MS8256RKL-10		7MP4034	2 MEG (256K X 8)
MS8256RKL-12		7MP4034	32 PIN SIP
MS8512FKX-85	7M4048L85N		4 MEG (512K X 8) JEDEC
MS8512FKX-10	7M4048L100N		32 PIN DIP
MS8512FKX-12	7M4048L120N		
MS8512SCMB-85	7M4048S85CB		4 MEG (512K X 8) JEDEC
MS8512SCMB-10	7M4048S100CB		32 PIN DIP
MS8512SCMB-12	7M4048S120CB		
MS8512SC-25	7MB4048S25P		4 MEG (512K X 8) JEDEC
MS8512SC-30	7MB4048S30P		32 PIN DIP
MS8512SC-35	7MB4048S35P		
MS8512SC-45	7MB4048S45P		
MS8512SC-55	7MB4048S55P		
MS8512SC-70	7M4048L70N		
MS8512SCMB-30	7M4048S30CB		4 MEG (512K X 8) JEDEC
MS8512SCMB-35	7M4048S35CB		32 PIN DIP
MS8512SCMB-45	7M4048S45CB		
MS8512SCMB-55	7M4048S50CB		
MS8512SCMB-70	7M4048S70CB		
MS8512RKX-10	7MP4008L100S	7MP4058L100S	4 MEG (512K X 8)
MS8512RKX-12	7MP4008L100S	7MP4058L120S	36 PIN SIP
MS8512RKX-15	7MP4008L100S	7MP4058L120S	
MS1664FKX-30	8M624S30C		1 MEG (64K X 16) JEDEC
MS1664FKX-35	8M624S35C		40 PIN DIP
MS1664FKX-45	8M624S45C		
MS1664BCX-25	7M624S25C		1 MEG (64K X 16)
MS1664BCX-35	7M624S35C		40 PIN DIP
MS1664BCXMB-25	7M624S25CB		
MS1664BCXMB-35	7M624S35CB		
MS3216RKX-12	7MP4031B12Z		512K (16K X 32) JEDEC
MS3216RKX-15	7MP4031S15Z		64 PIN ZIP
MS3216RKX-20	7MP4031S20Z		
MS3216RKX-25	7MP4031S25Z		
MS3216RKX-35	7MP4031S35Z		
MS3216RKX-45	7MP4031S35Z		

PUMA 2S1000	7M4003SXXCH		1 MEG (32K X 32)
			66 PIN HIP
PUMA 2S4000	7M4013SXXCH		4 MEG (128K X 32)
			66 PIN HIP
PUMA 2E1000	7M7004SXXCH		1 MEG (32K X 32) EEPROM
			66 PIN HIP
MS3264FKX-25		7MP4036S25Z	2 MEG (64K X 32)
MS3264FKX-35	7M4017S35C		60 PIN DIP
MS3264FKX-45	7M4017S40C		
MS3264FKX-55	7M4017S50C		
MS3264RKX-15	7MP4036B15Z		2 MEG (64K X 32) JEDEC
MS3264RKX-20	7MP4036S20Z		64 PIN ZIP
MS3264RKX-25	7MP4036S25Z		
MS3264RKX-35	7MP4036S35Z		
MS3264RKX-20	7MP4036S45Z		
MS32256FKX-25	7MB4067S25P		8 MEG (256K X 32)
MS32256FKX-30	7MB4067S30P		60 PIN DIP
MS32256FKX-35	7MB4067S35P		
MS32256FKX-45	7MB4067S45P		
MS32256FKX-55	7MB4067S55P		
MS32256RKX-20	7MP4045S20Z		8 MEG (256K X 32) JEDEC
MS32256RKX-25	7MP4045S25Z		64 PIN ZIP
MS32256RKX-30	7MP4045S30Z		
MS32256RKX-35	7MP4045S35Z		
MS32256RKX-45	7MP4045S45Z		
MS32256RKX-55	7MP4045S55Z		
MOTOROLA P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**MOTOROLA ORG/PACKAGE**
MCM32257-20	7MP4045S20		8 MEG (256K X 32) JEDEC
MCM32257-25	7MP4045S25		64 PIN ZIP
MCM3264-12	7MP4036B12		2 MEG (64K X 32) JEDEC
MCM3264-15	7MP4036B15		64 PIN ZIP
MCM3264-20	7MP4036S20		
MCM8256-15		7MP4034S15Z	2 MEG (256K X 8) JEDEC
MCM8256-20		7MP4034S20Z	60 PIN ZIP
SMART MODULAR P/N	**IDT P/N DIRECT EQUIVALENT**	**IDT P/N SIMILAR PART**	**SMART MODULAR ORG/PACKAGE**
SM68512-85	7M4048L85N		4 MEG (512K X 8) JEDEC
SM68512-10	7M4048L100N		32 PIN DIP
SM68512-12	7M4048L120N		
SM232128-20	7MP4095S20Z		4 MEG (128K X 32) JEDEC
SM232128-25	7MP4095S25Z		64 PIN ZIP
SM232128-35	7MP4095S35Z		
SM232256-20	7MP4045S20Z		8 MEG (256K X 32) JEDEC
SM232256-25	7MP4045S25Z		64 PIN ZIP
SM232256-35	7MP4045S35Z		
SM332256-20	7MP4045S20M		8 MEG (256K X 32) JEDEC
SM332256-25	7MP4045S25M		64 PIN ZIP
SM332256-35	7MP4045S35M		

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCEMOS™ ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036/E	6116
5962-88740	6116LA
84132/B	6167
5962-86015/A	7187
5962-86859	6198/7198/7188
5962-86705/D	6168
5962-85525/B	7164
5962-88552/B	71256L
5962-88662/A	71256S
5962-88611/A	71682L
5962-88681/A	71258S
5962-88545	71258L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294/B	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875/B	7130/7140
5962-87002/C	7132/7142
5962-88610/A	7133S/7143S
5962-88665/A	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846/A	72404
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L

SMD	
LOGIC	**IDT**
5962-87630/B	54FCT244/A
5962-87629/C	54FCT245/A
5962-86862/B	54FCT299/A
5962-87644/A	54FCT373/A
5962-87628/C	54FCT374/A
5962-87627/B	54FCT377/A
5962-87654/A	54FCT138/A
5962-87655/A	54FCT240/A
5962-87656/A	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543/A	54FCT521/A
5962-88640/A	54FCT161/A
5962-88639/A	54FCT573/A
5962-88656	54FCT823A/B
5962-88657/A	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736/A	29FCT520A/B
5962-88775	54FCT646
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733/A	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708/A	39C10B & C
5962-88533/A	49C460A
5962-88613/A	39C60A
5962-88643/A	49C410
5962-88743/A	75C48S
5962-89517	49C402/A
5962-86893	7216L
5962-87686	7217L
5962-88733/A	7210

2509 tbl 01

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

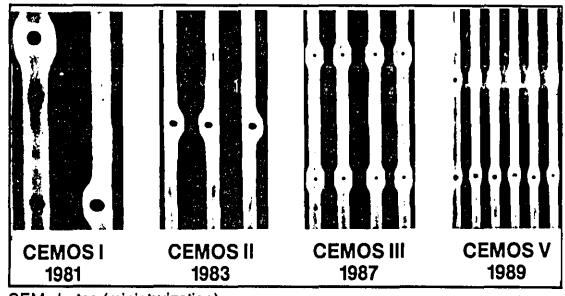
	CEMOS I	CEMOS II A	CEMOS II C	CEMOS III	CEMOS V	CEMOS VI
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization) 2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

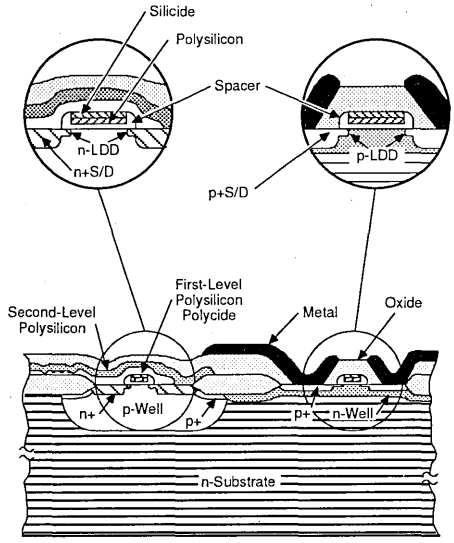


Figure 3. IDT CEMOS Device Cross Section

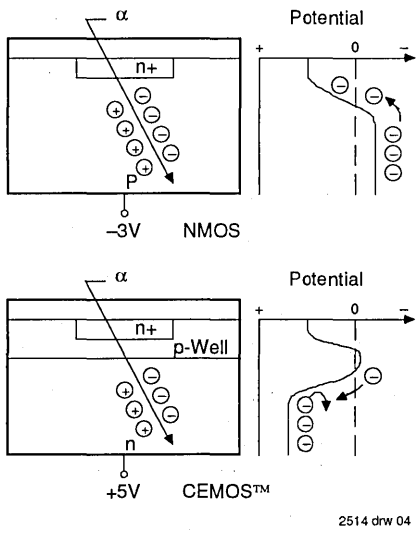


Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

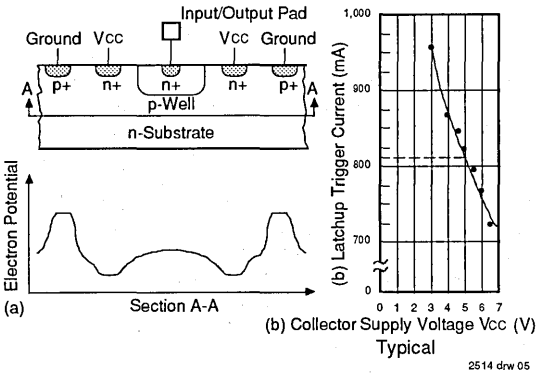


Figure 5. IDT CEMOS Latchup Suppression

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20-60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CEMOS™ and BiCEMOS™ products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem.modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surfac-mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, , Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

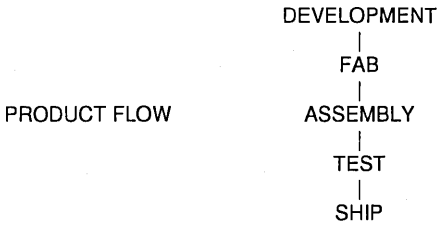
Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

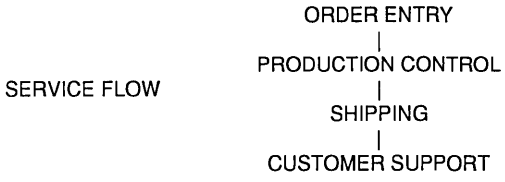
"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.



These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade. With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level

tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

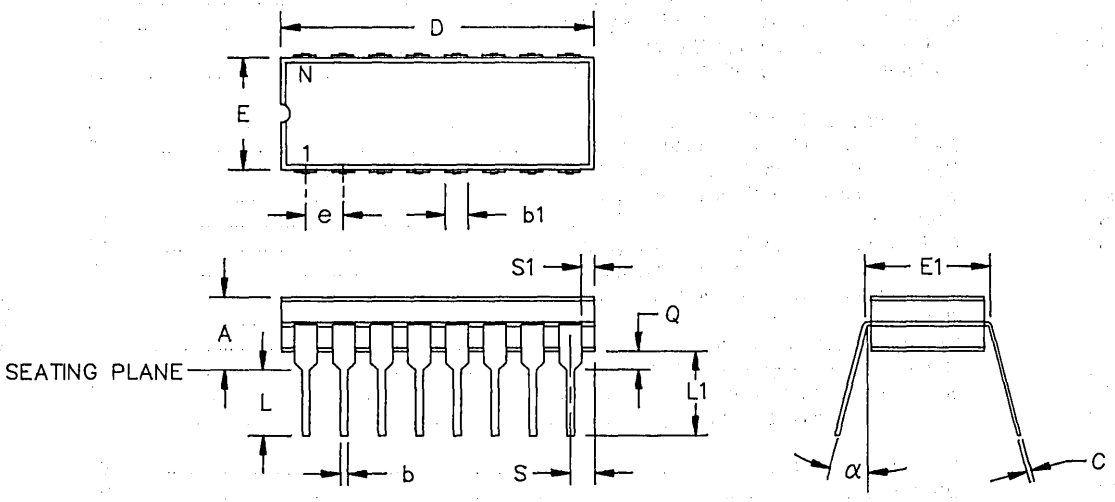
MODULE PACKAGE DIAGRAM OUTLINES

Module package diagrams are located at the back of each Subsystems data sheet.

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (400 & 600 MIL)

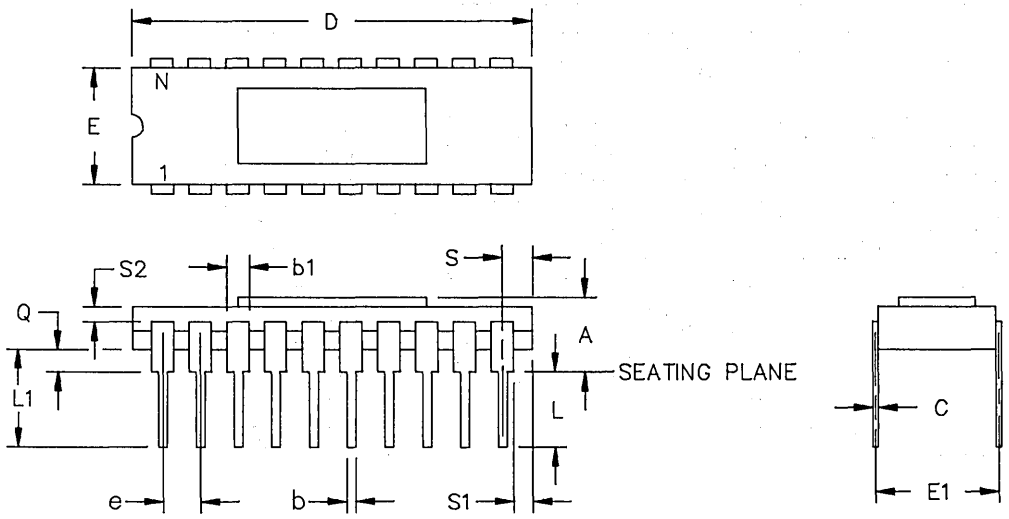
DWG #	D24-3		D24-2		D28-1		D40-1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.045	.060	.045	.065	.045	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.600	.510	.600
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

32 LEAD CERDIP (WIDE BODY)

DWG #	D32-1	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.120	.210
b	.014	.023
b1	.045	.065
C	.008	.014
D	1.625	1.675
E	.570	.600
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	.030	.080
S1	.005	–
α	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

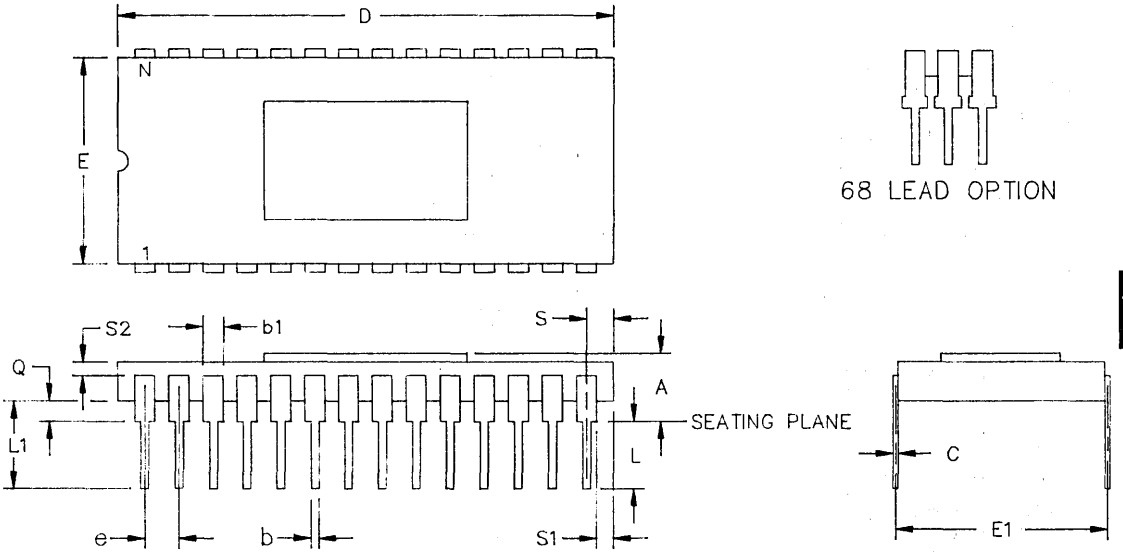


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

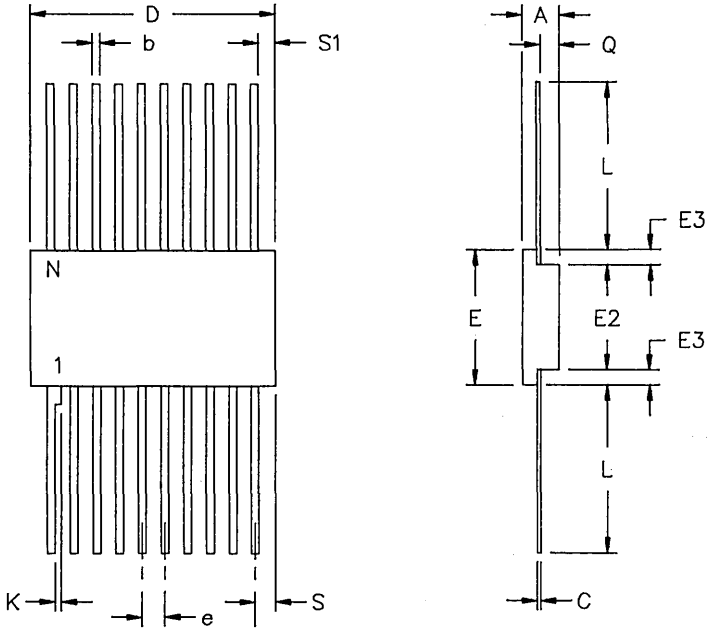


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.012	.008	.012	.008	.014	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.595	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.100	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS

20-28 LEAD FLATPACK

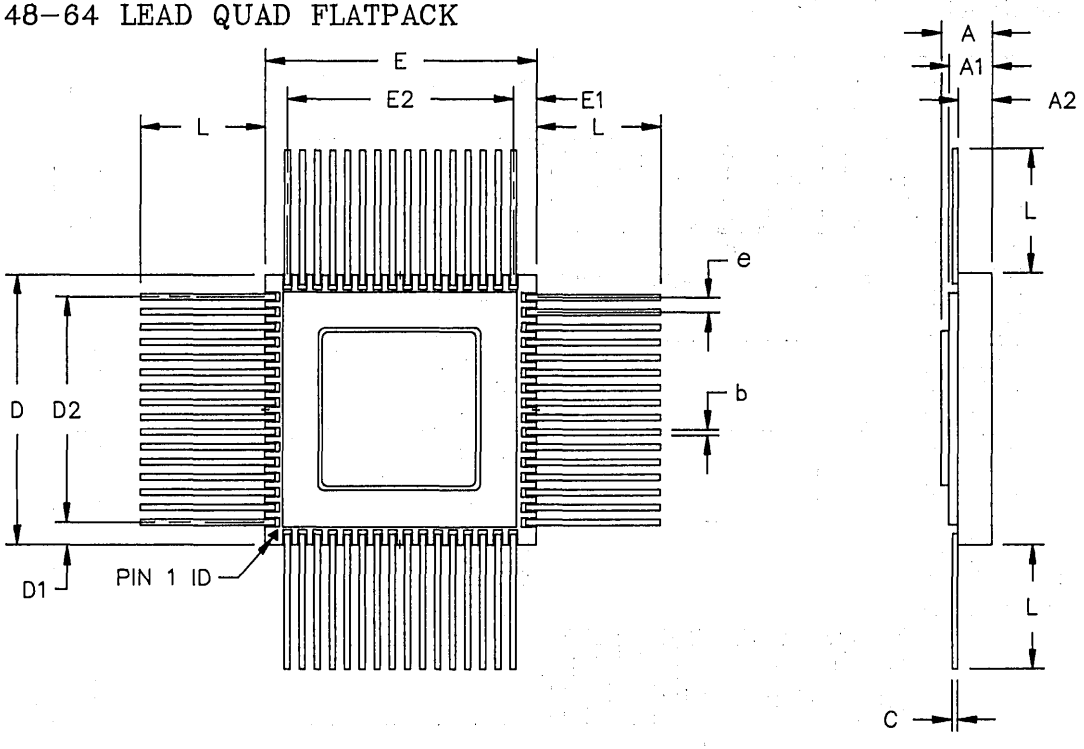


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20-1		F20-2		F24-1		F28-1		F28-2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.004	.007	.004	.007	.004	.007	.004	.007	.004	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.480	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015	–	–	–	–	–	–
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.000	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK

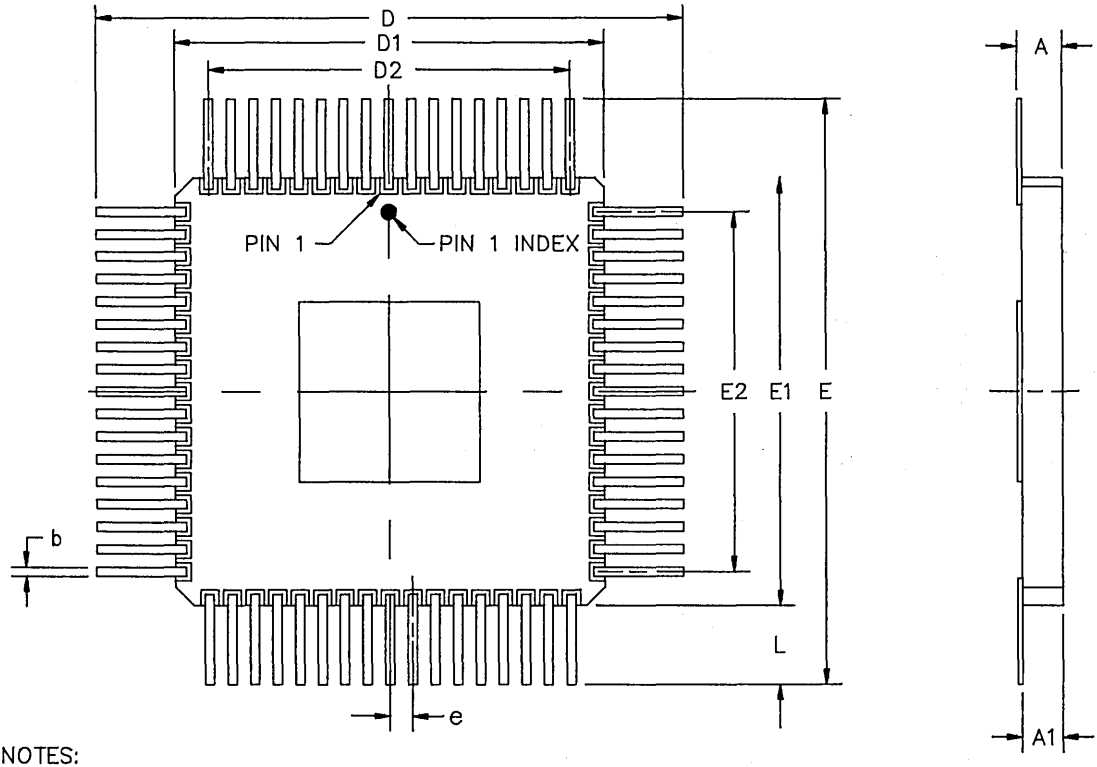


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK

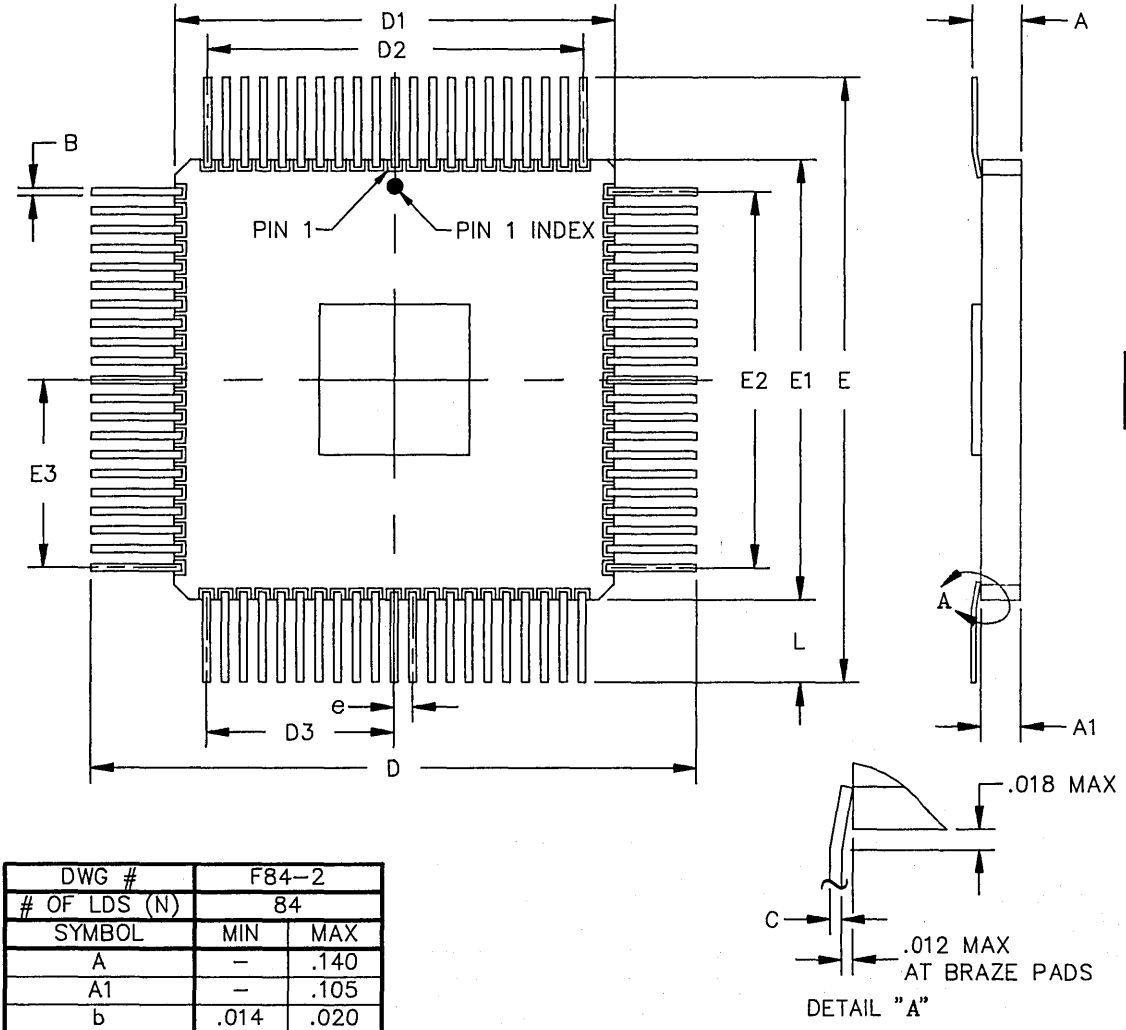


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
b	.014	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	17	

FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY UP)

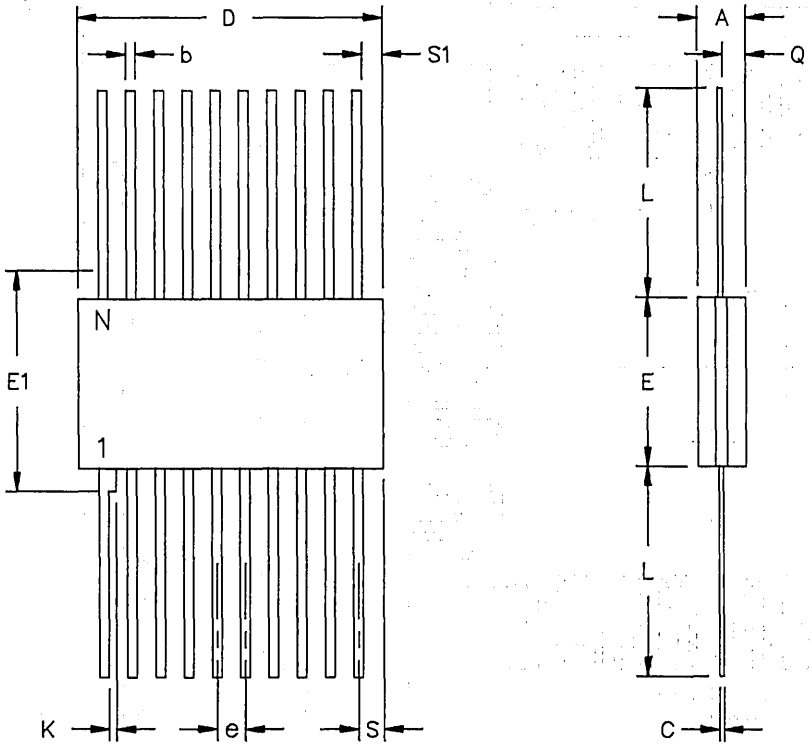


DWG #	F84-2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.940	1.960
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

CERPACKS

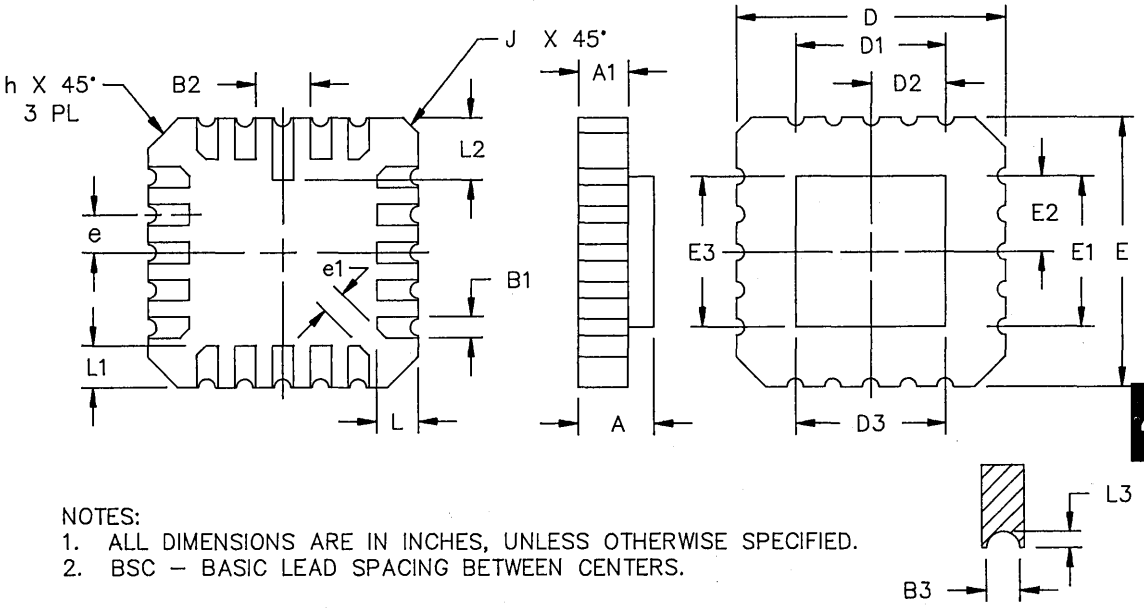
16–28 LEAD CERPACK



NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

LEADLESS CHIP CARRIERS



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

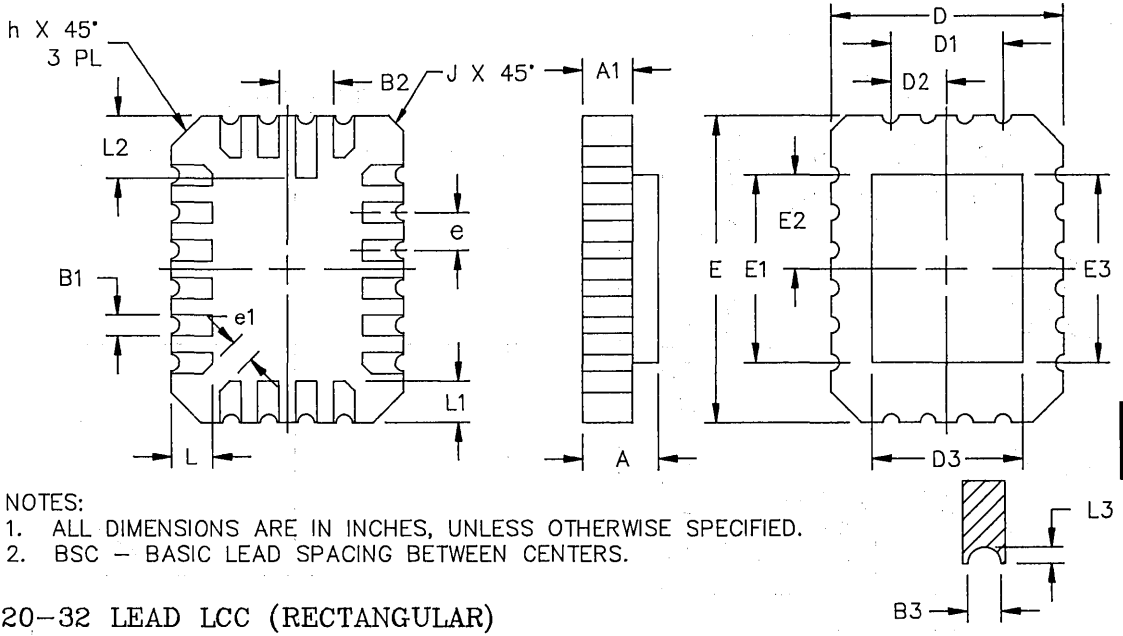
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.075	.095	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



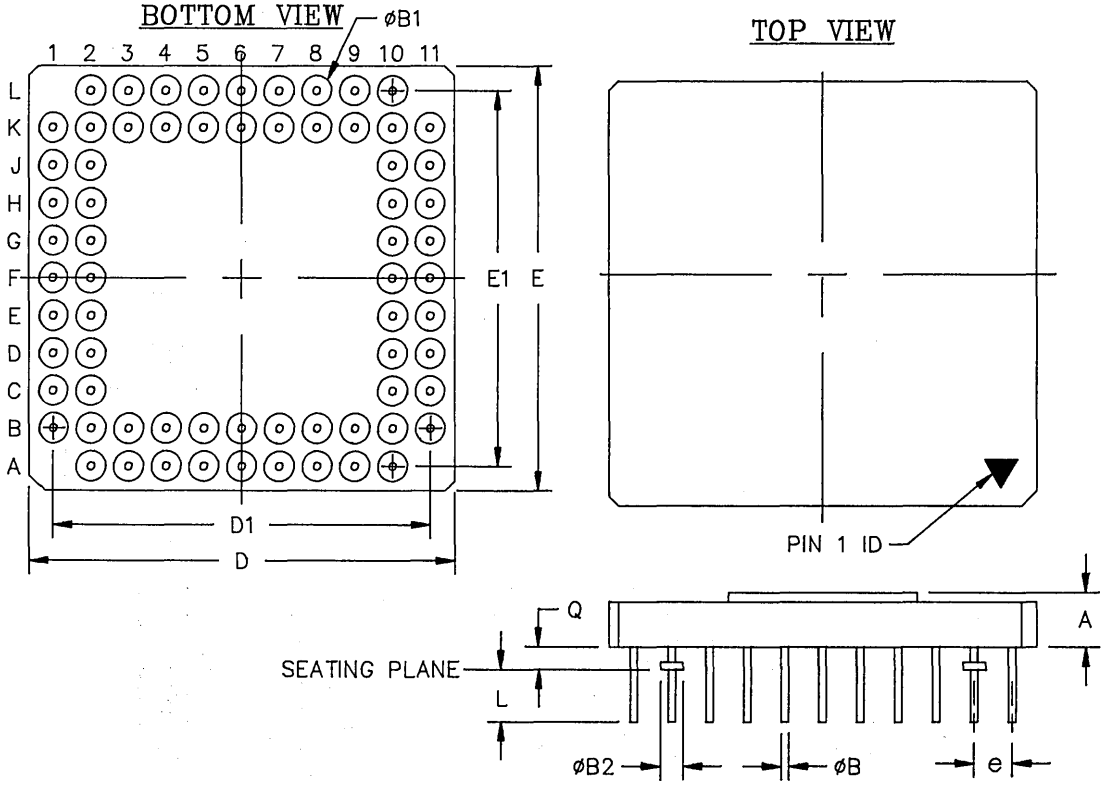
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

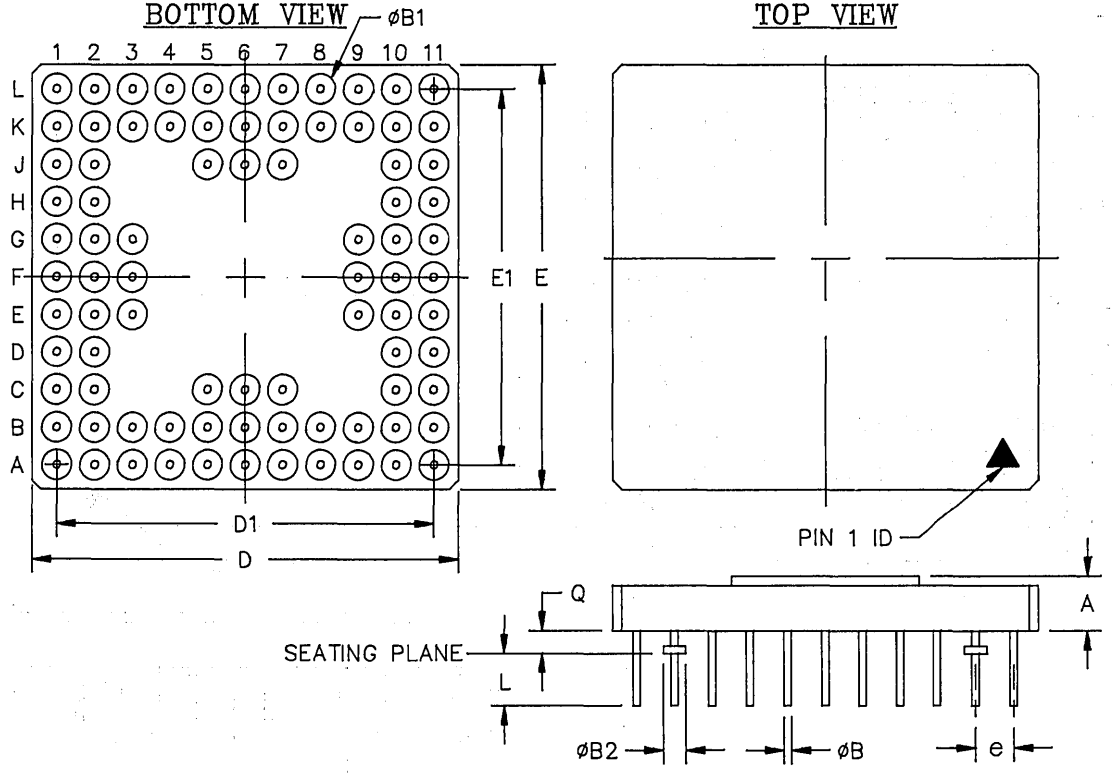


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

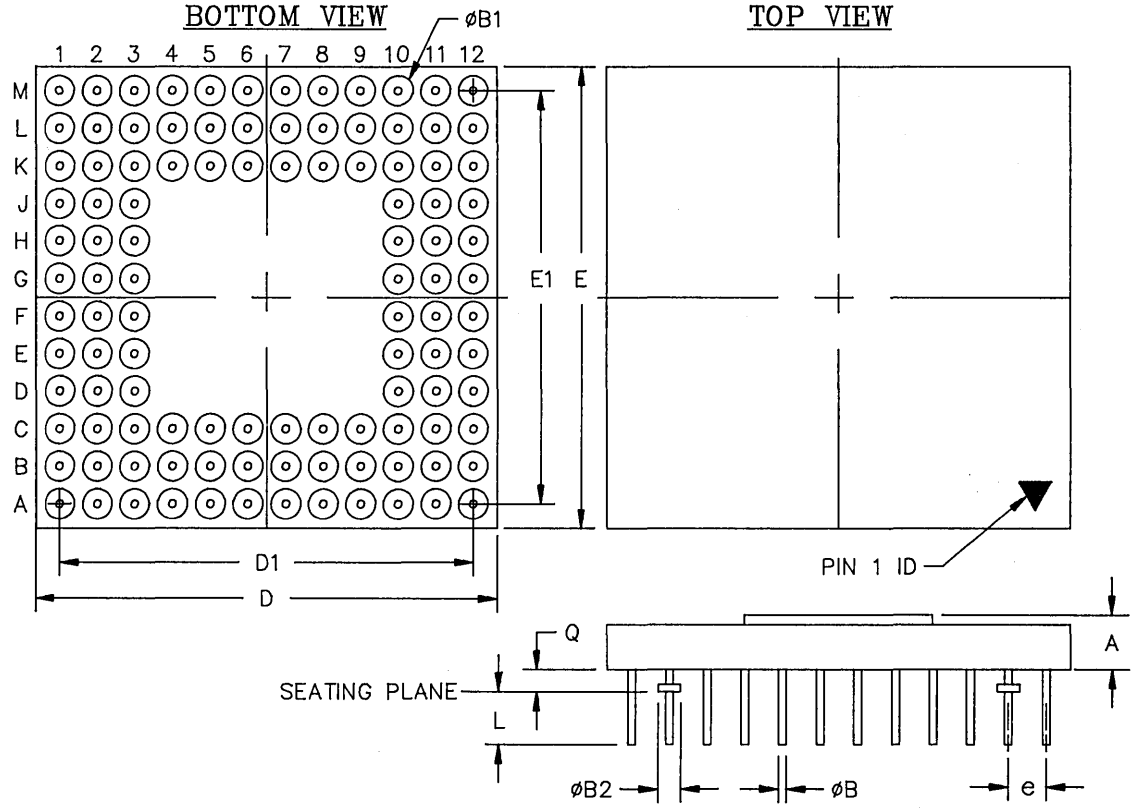


DWG #	G84-3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

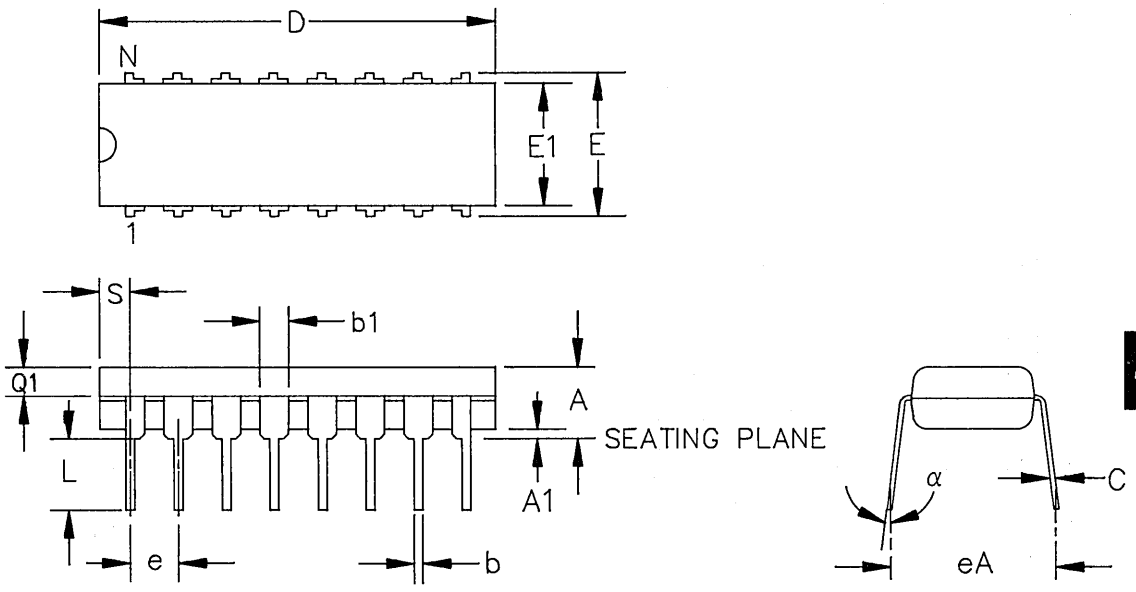


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

16-32 LEAD PLASTIC DIP (300 MIL)

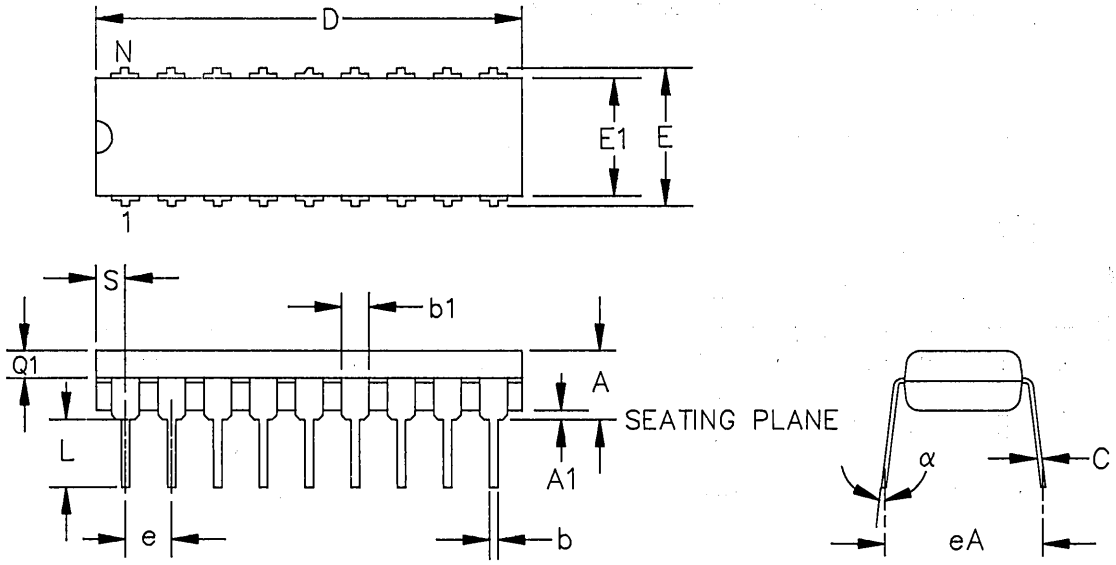


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

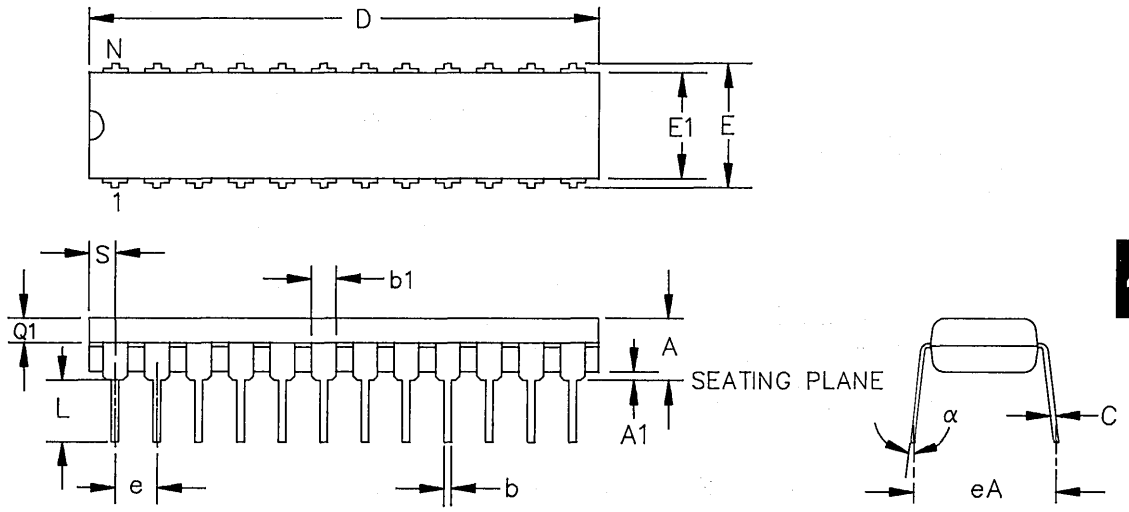


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

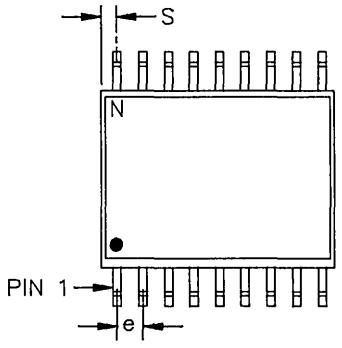
24-48 LEAD PLASTIC DIP (600 MIL)



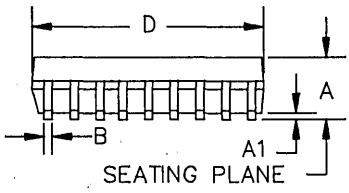
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

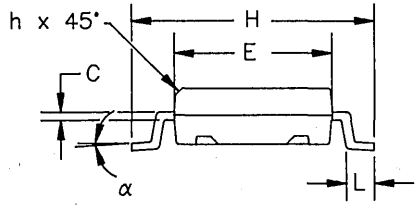
DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

SMALL OUTLINE IC



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

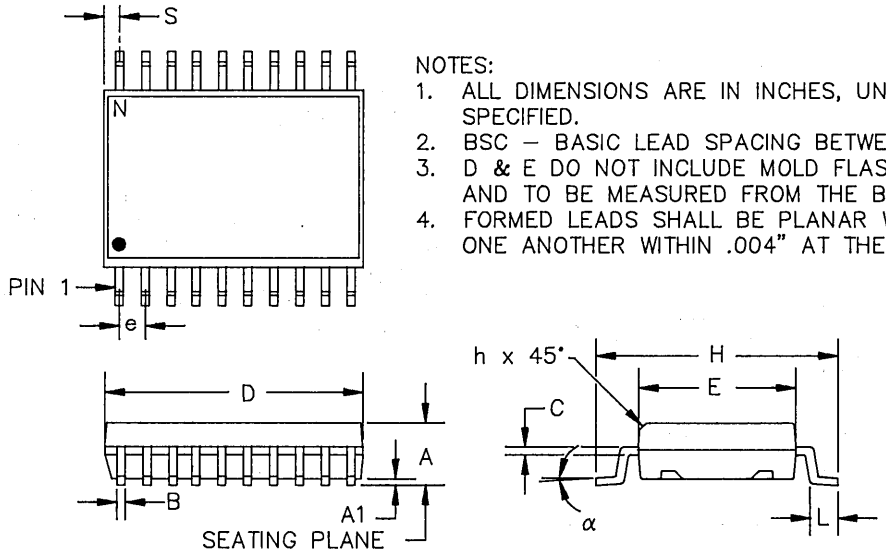




16–24 LEAD SMALL OUTLINE (GULL WING – JEDEC)

DWG #	SO16–1		SO18–1		SO20–2		SO24–2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



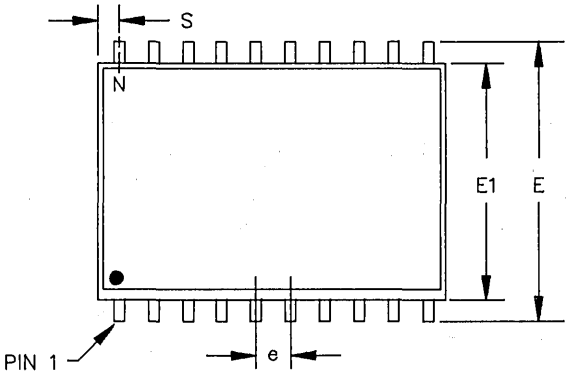
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

4

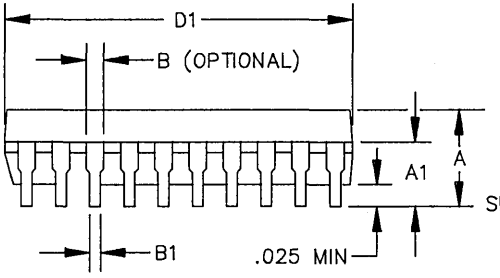
28 LEAD SMALL OUTLING (GULL WING – JEDEC)

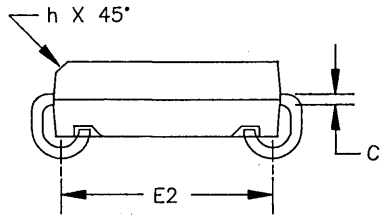
DWG #	SO28–2		SO28–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE



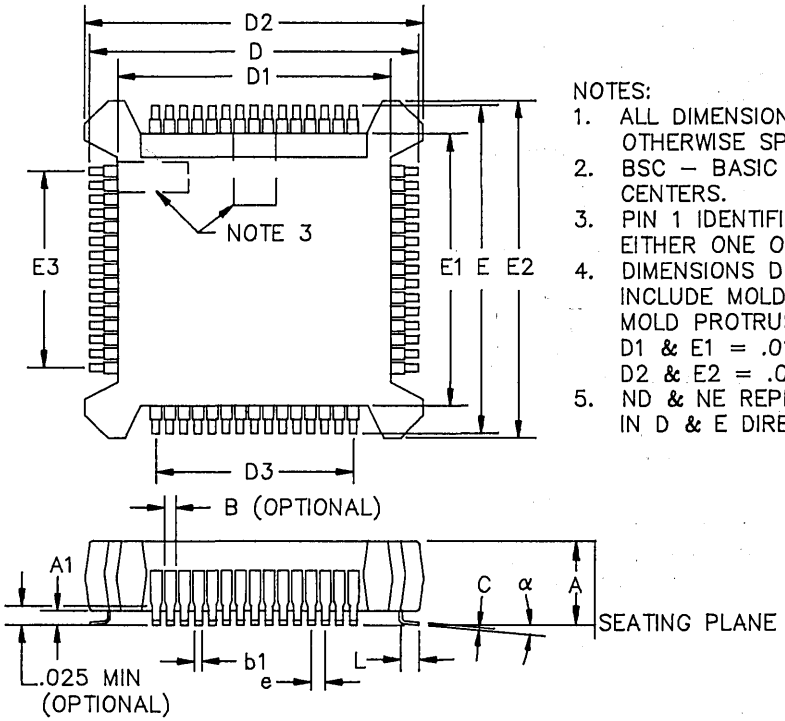


20–32 LEAD SMALL OUTLINE (J–BEND, 300 MIL)

DWG #	SO20–1		SO24–4		SO24–8		SO28–5		SO32–2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

PLASTIC QUAD FLATPACKS

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)



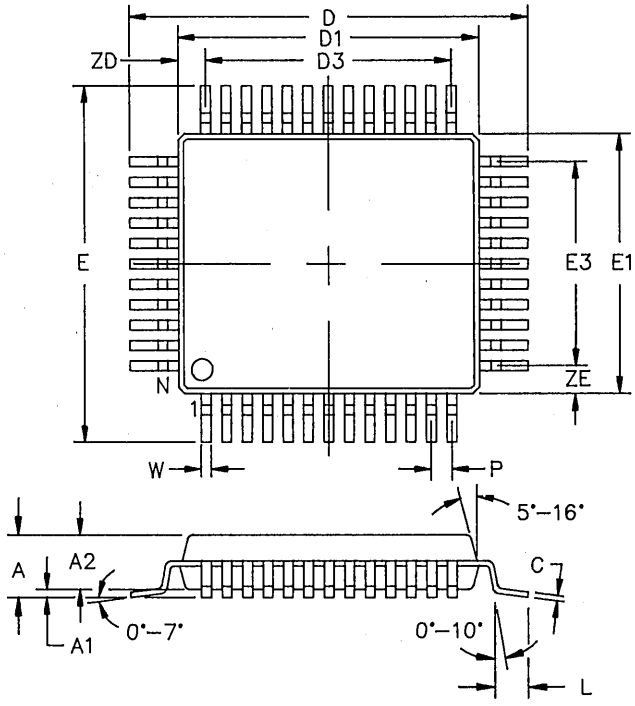
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

4

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80 & 100 LEAD RECTANGULAR PLASTIC QUAD FLATPACK (EIAJ)

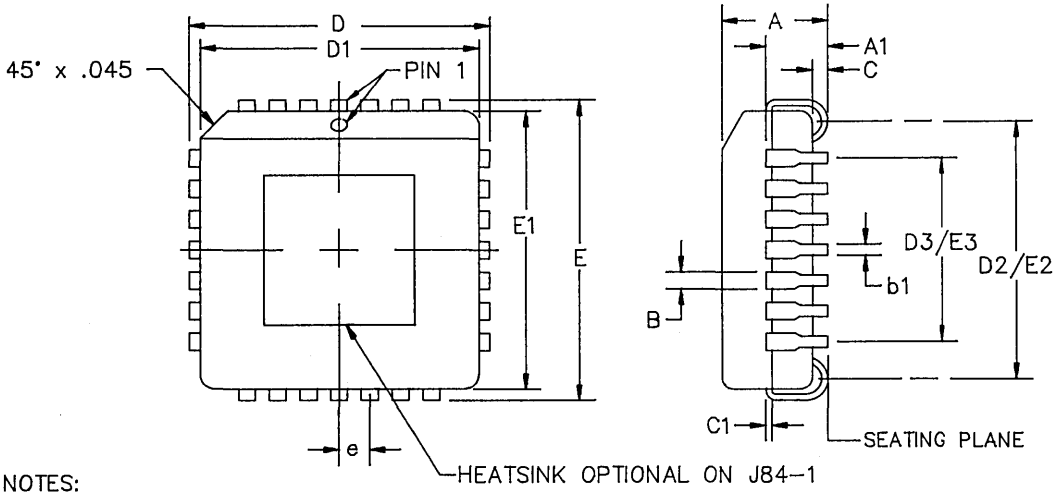


DWG #	PQ80–2		PQ100–2	
# OF LDS (N)	80		100	
SYMBOLS	MIN	MAX	MIN	MAX
A	2.80	3.40	2.80	3.40
A1	.25	–	.25	–
A2	2.54	3.05	2.54	3.05
C	.13	.20	.13	.20
D	23.65	24.15	23.65	24.15
D1	19.90	20.10	19.90	20.10
D3	18.40 REF		18.85 REF	
E	17.65	18.15	17.65	18.15
E1	13.90	14.10	13.90	14.10
E3	12.00 REF		12.35 REF	
L	.65	.95	.65	.95
ND/NE	16/24		20/30	
P	.80 BSC		.65 BSC	
W	.30	.45	.25	.40
ZD	.80		.575	
ZE	1.00		.825	

NOTES:
1. ALL DIMENSIONS ARE IN METRIC, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .254 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



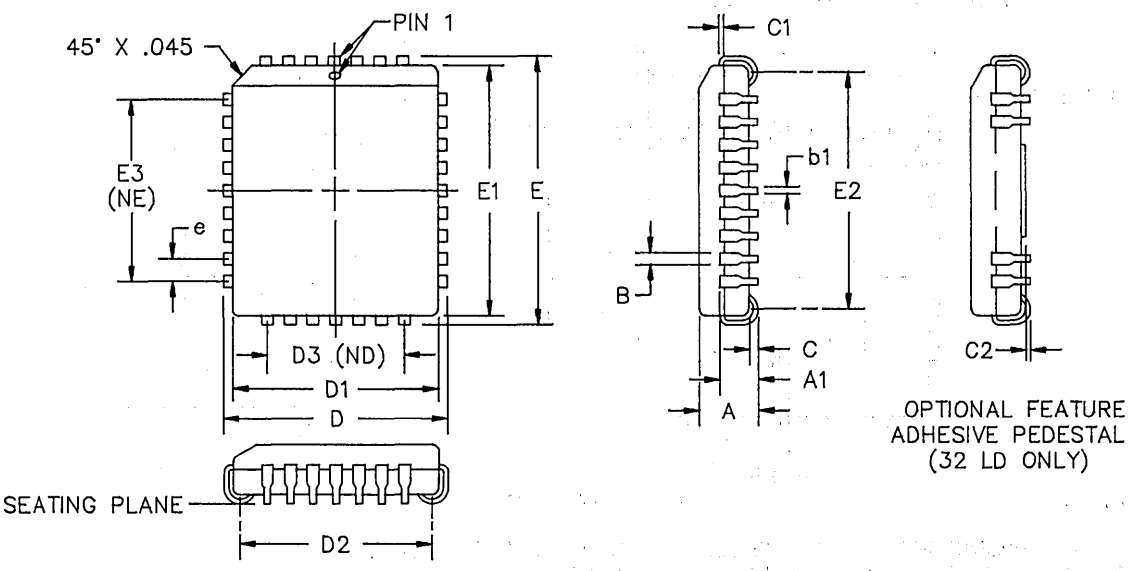
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)



DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

FIFO MEMORIES

Integration of IDT high-speed static RAM technology with internal support logic yields high-performance, high-density FIFO memories. A FIFO is used as a memory buffer between two asynchronous systems with simultaneous read/write access. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses. Since these FIFOs are built with an internal RAM pointer architecture, there is no fall-through time between a write to a memory location and a read from that memory location. System performance is significantly improved over the shift register-based arschitecture of previous FIFO designs which are handicapped with long fall-through times.

IDT offers the widest selection of monolithic FIFOs, ranging from shallow 64x4 and 64x5 to the high-density 16Kx9. Shallow FIFOs regulate data flow in tightly couped computational engines. High-density FIFOs store large blocks in networking, telecommunication and data storage systems. The IDT7200 FIFO family (256x9 through the 16Kx9 FIFOs) are all pin and function compatible, making density upgrades simple. All IDT FIFOs can be cascaded to greater word depths and expanded to greater word widths with no external support logic.

IDT's high-speed SyncFIFO™ is ideal for multiprocessor systems, workstations and high-end graphics. The innovative architecture of the SyncFIFO (internal I/O registers with separate clock and enable inputs), along with wider data bus, simplifies design and reduces interface logicc.

The Parallel-Serial FIFOs incorporate a serial input or a serial output shifter for serial-to-parallel or parallel-to-serial bus interface. The Parallel-Serial FIFOs also offer six status flags for flexible data throttling.

A variety of packages are available: standard plactic FIP and CERDIP, surface mount ceramic LCC, PLCC and SOIC, and high-reliability flatpack. Increasing board density is the overwhelming goal of IDT's package development efforts, as demonstrated by the introduction of the 300 mil ThinDIP.

FIFO modules, composed of four LCC devices mounted on a multi-layer co-fired ceramic substrate, increase densities to 32Kx18 which are pin-compatible with current monolithic versions.

IDT is committed to offering FIFOs of increasing density, speed and enhanced architectural innovations, such as Flexishift™ and the BiFIFO, for easier system interface.

TABLE OF CONTENTS

1992 FIFO TABLE OF CONTENTS (CONTINUED)

SUBSYSTEMS PRODUCTS (Please refer to pages indicated in Section 7 of this book.)

FIFO MODULES

5

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT, 512 x 9-BIT, 1K x 9-BIT

IDT7200S/L
IDT7201SA/LA
IDT7202SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- 1K x 9 organization (IDT7202A)
- Low power consumption
  - — Active: 770mW (max.)
  - —Power-down: 27.5mW (max.)
- Ultra high speed—15ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87531, 5962-89666, 5962-89863 and 5962-89536 are listed on this function.

DESCRIPTION:

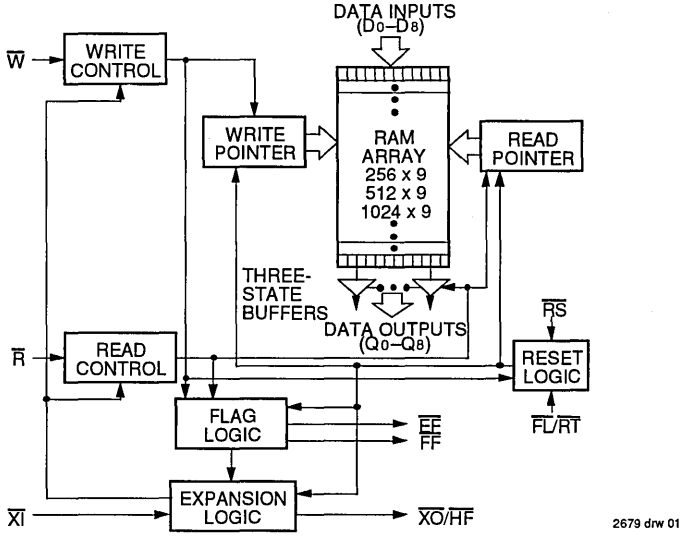
The IDT7200/7201A/7202A are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 25ns (40MHz).

The devices utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

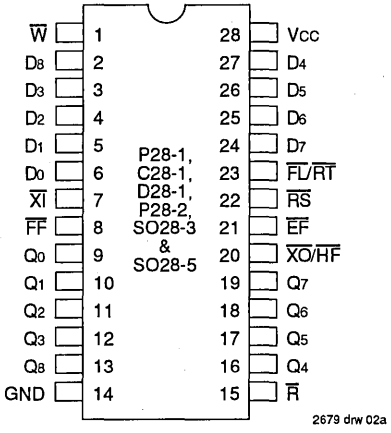
The IDT7200/7201A/7202A are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

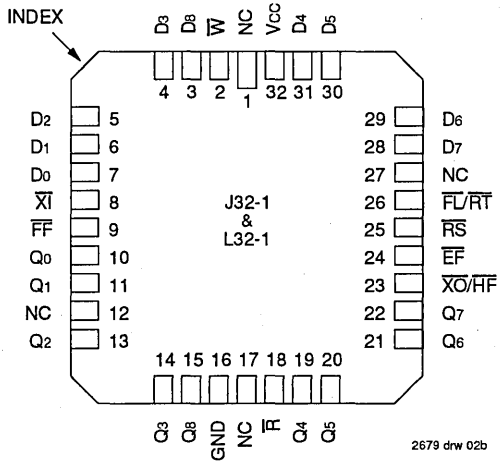


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/FLATPACK
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2679 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Mlitary	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2679 tbl 03

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2679 tbl 02

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

Symbol	Parameter	IDT7200 IDT7201A IDT7202A Commercial t_A = 15,20ns			IDT7200 IDT7201A IDT7202A Military t_A = 20ns			IDT7200 IDT7201A IDT7202A Commercial t_A = 25,35ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	−1	—	1	−10	—	10	−1	—	1	µA
I_{LO}[2]	Output Leakage Current	−10	—	10	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	125[4]	—	—	140[4]	—	—	125[4]	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	15	—	—	20	—	—	15	mA
I_{CC3}(L)[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.5	—	—	0.9	—	—	0.5	mA
I_{CC3}(S)[3]	Power Down Current (All Input = V_{CC} - 0.2V)			5			9	—	—	5	mA

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DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

Symbol	Parameter	IDT7200 IDT7201A IDT7202A Military t_A = 30,40ns			IDT7200 IDT7201A IDT7202A Commercial t_A = 50,65,80,120ns			IDT7200 IDT7201A IDT7202A Military t_A = 50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	−10	—	10	−1	—	1	−10	—	10	µA
I_{LO}[2]	Output Leakage Current	−10	—	10	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	140[4]	—	50	80	—	70	100	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	20	—	5	8	—	8	15	mA
I_{CC3}(L)[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.9	—	—	0.5	—	—	0.9	mA
I_{CC3}(S)[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	9	—	—	5	—	—	9	mA

NOTES:
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1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5.0V±10%, TA = –55°C to +125°C)

		Commercial		Com'l & Mil.		Commercial		Military		Commercial		
		7200S/L15 7201SA/LA15 7202SA/LA15		7200S/L20 7201SA/LA20 7202SA/LA20		7200S/L25 7201SA/LA25 7202SA/LA25		7200S/L30 7201SA/LA30 7202SA/LA30		7200S/L35 7201SA/LA35 7202SA/LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{RTF}	Retransmit Low to Flags Valid	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

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AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5.0V±10%, TA = –55°C to +125°C)

		Military		Commmercial and Military								
		7200S/L40 7201SA/LA40 7202SA/LA40		7200S/L50 7201SA/LA50 7202SA/LA50		7200S/L65 7201SA/LA65 7202SA/LA65		7200S/L80 7201SA/LA80 7202SA/LA80		7200S/L120 7201SA/LA120 7202SA/LA120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{RTF}	Retransmit Low to Flags Valid	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	15	—	15	—	15	—	15	—	ns

NOTES:

2679 tbl 07

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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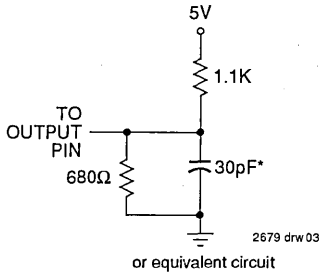

Figure 1. Output Load

* Includes scope and jig capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A/7202A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512/1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for IDT7200, 512 writes for the IDT7201A and 1024 writes for the IDT7202A.

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EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS ($Q_0 - Q_8$)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

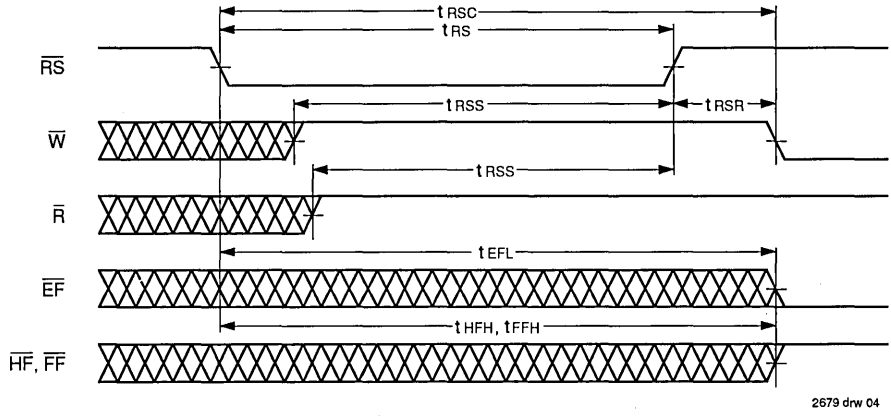

Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

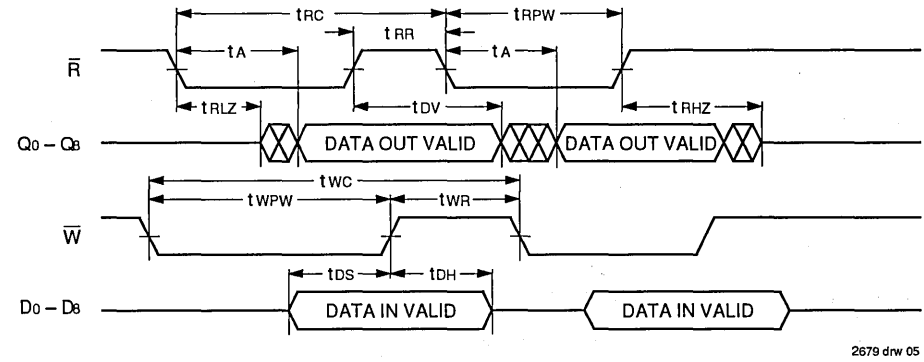

Figure 3. Asynchronous Write and Read Operation

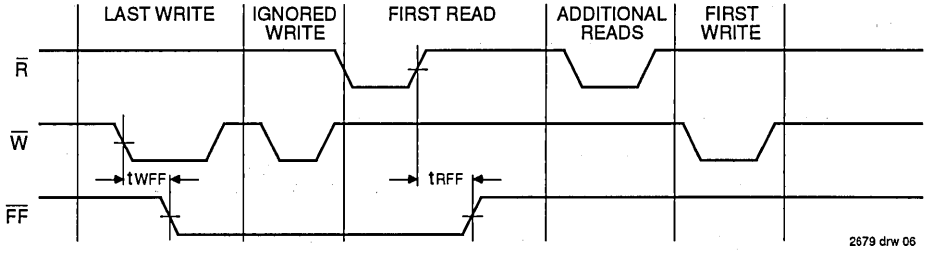

Figure 4. Full Flag From Last Write to First Read

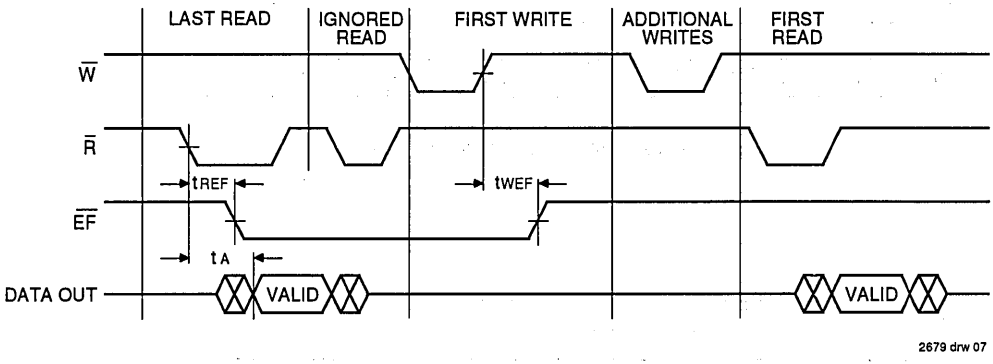

Figure 5. Empty Flag From Last Read to First Write

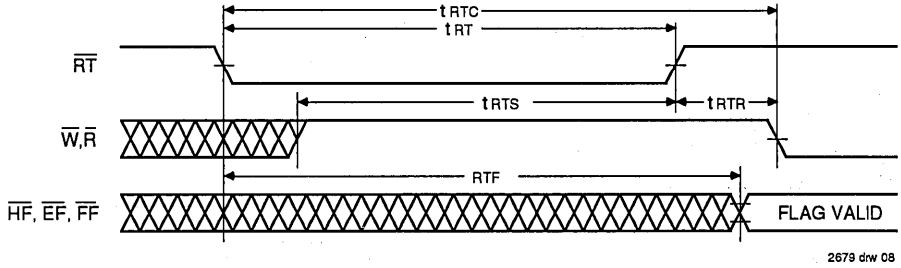

Figure 6. Retransmit

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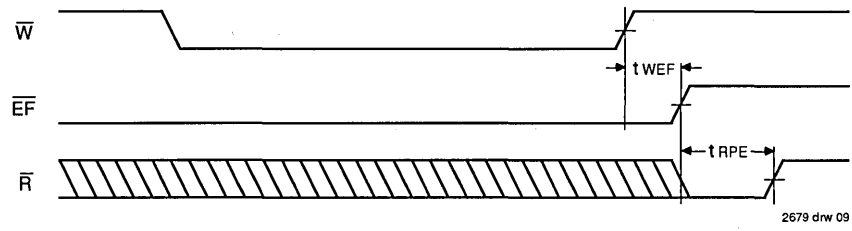

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

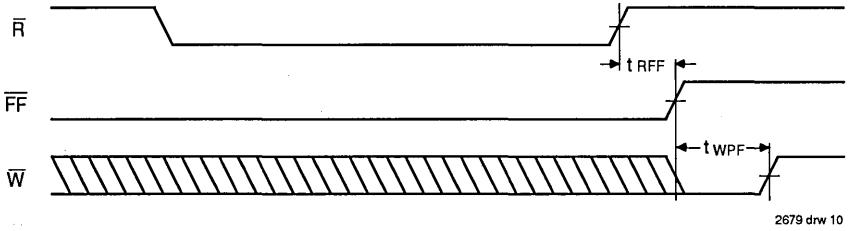

Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse

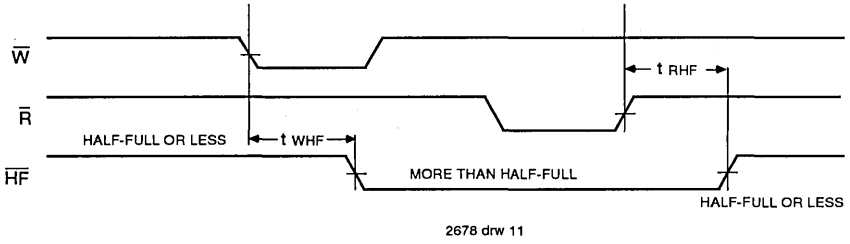

Figure 9. Half-Full Flag Timing

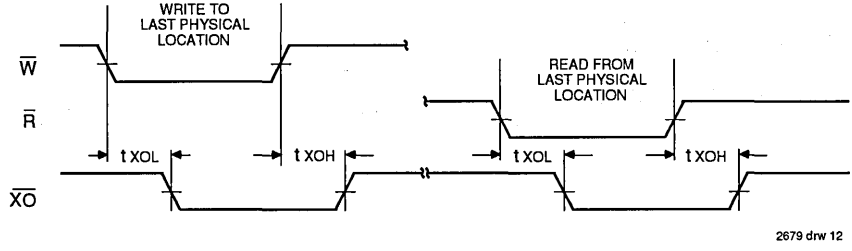

Figure 10. Expansion Out

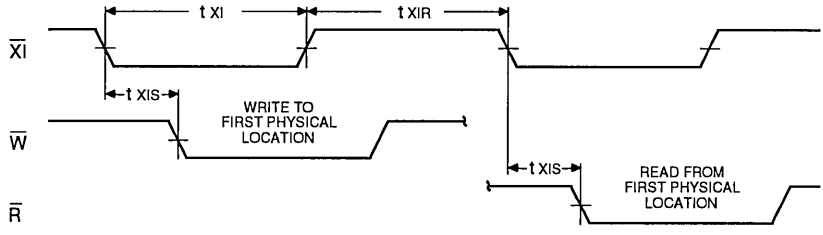

Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7200/7201A/7202A may be used when the application requirements are for 256/512/1024 words or less. The IDT7200/7201A/7202A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7200/7201A/7202A can easily be adapted to applications when the requirements are for greater than 256/512/1024 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201A/7202As. Any depth can be attained by adding additional IDT7200/7201A/7202As. The IDT7200/7201A/7202A operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7200/7201A/7202As. Any word width can be attained by adding additional IDT7200/7201A/7202As (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201A/7202As as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

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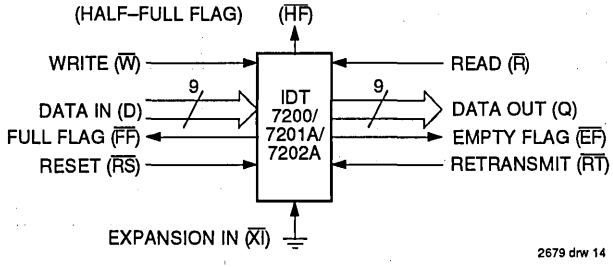

Figure 12. Block Diagram of Single 256/512/1024 x 9 FIFO

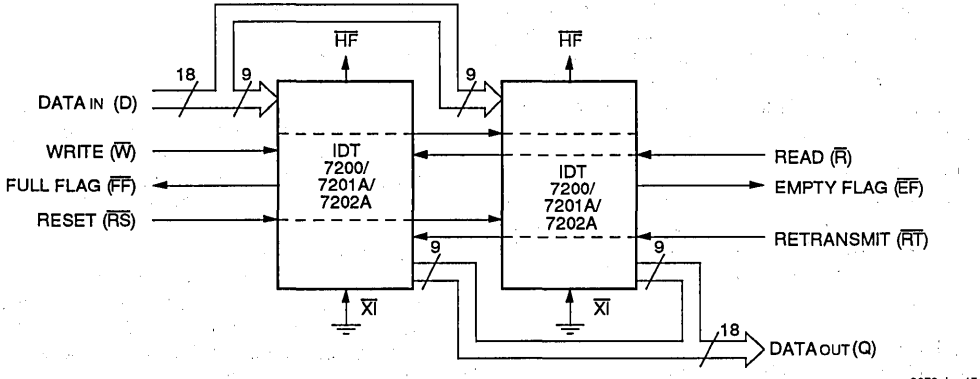

Figure 13. Block Diagram of 256/512/1024 x 18 FIFO Memory Used in Width Expansion Mode

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is High.

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TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

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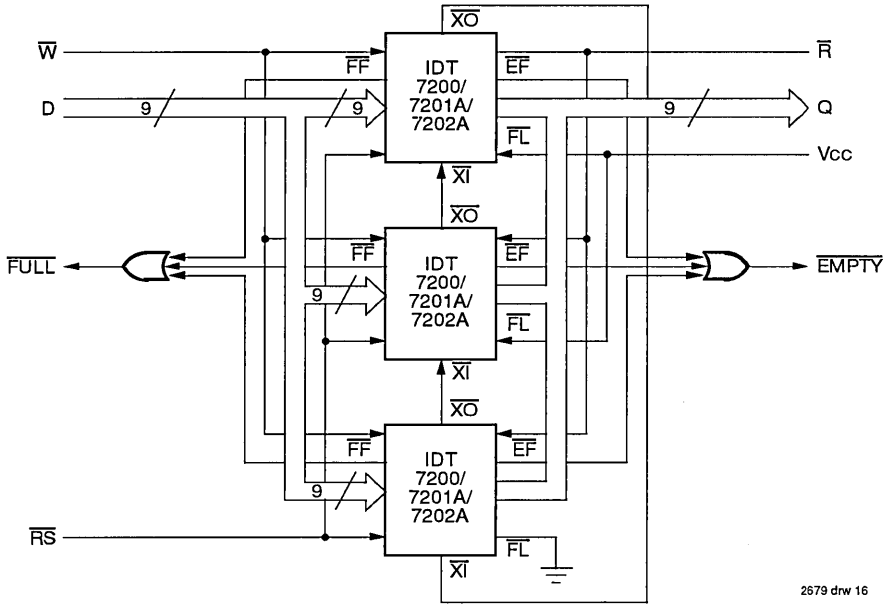

Figure 14. Block Diagram of 768 x 9/1536 x 9/3072 x 9 FIFO Memory (Depth Expansion)

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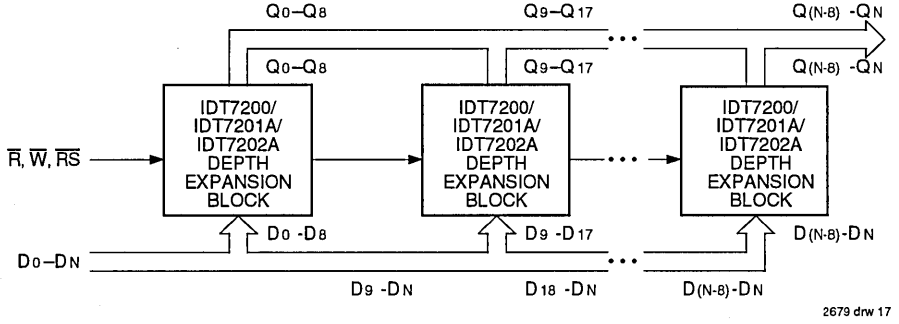

Figure 15. Compound FIFO Expansion

NOTES:
1. For depth expsansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

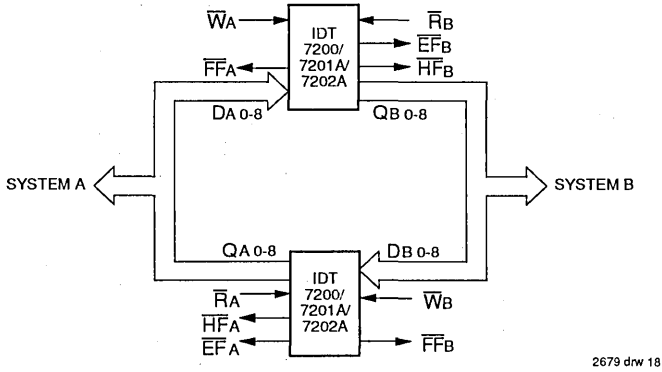

Figure 16. Bidirectional FIFO Mode

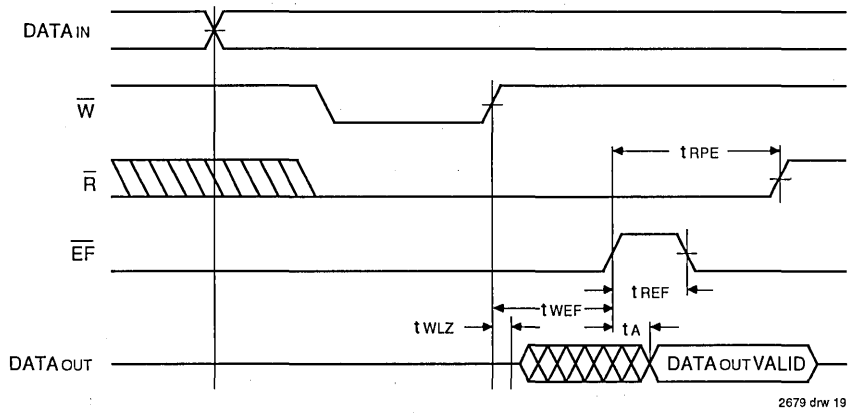

Figure 17. Read Data Flow-Through Mode

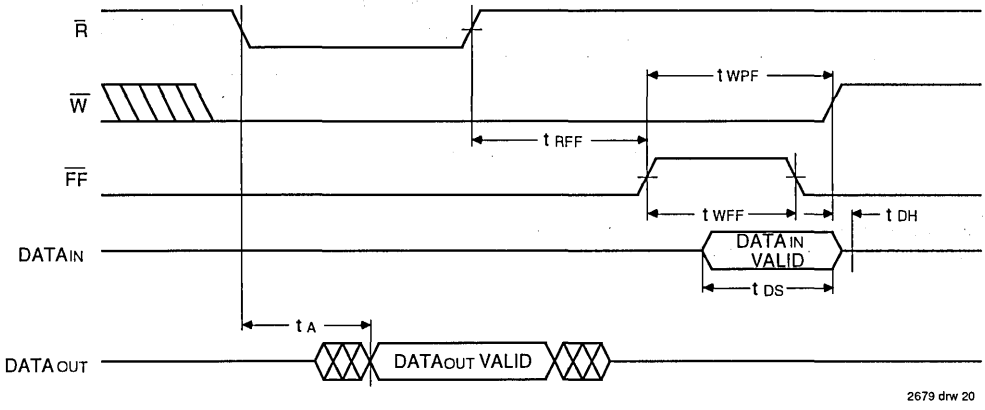

Figure 18. Write Data Flow-Through Mode

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT, 4096 x 9-BIT, 8192 x 9-BIT & 16384 x 9-BIT

IDT7203
IDT7204
IDT7205
IDT7206

FEATURES:

- First-In/First-Out dual-port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- 8192 x 9 organization (IDT7205)
- 16384 x 9 organization (IDT7206)
- High-speed: 20ns access time
- Low power consumption
  - — Active: 770mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function.

DESCRIPTION:

The IDT7203/7204/7205/7206 are dual-port memories buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. All FIFOs have a read/write cycle time of 30ns (33MHz).

The devices 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed low. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7203/7204/7205/7206 are fabricated using IDT's high-speed CEMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering, and other applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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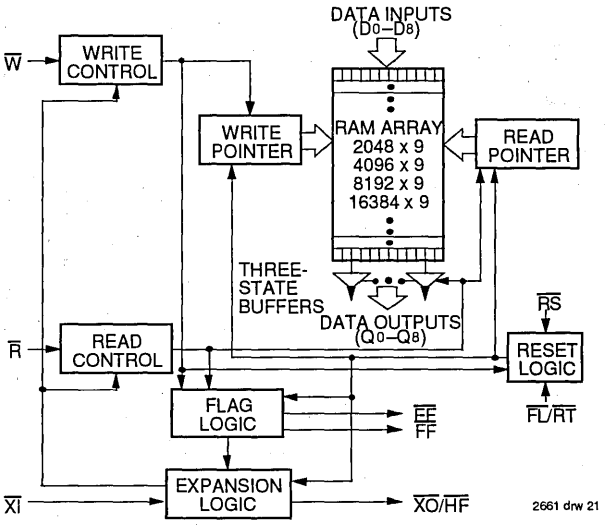
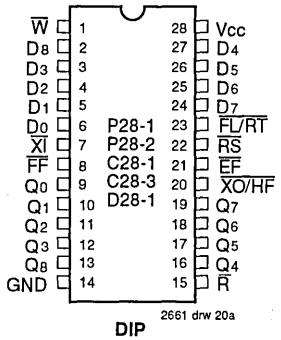
FUNCTIONAL BLOCK DIAGRAM

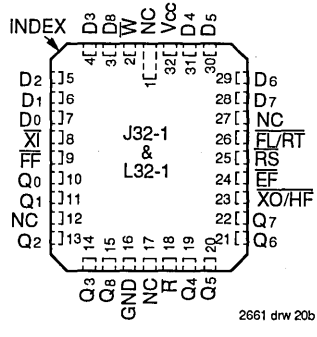


CEMOS is a trademark of Integrated Device Techology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

Consult Factory for CERPACK Pinout

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to +155	° C
IOUT	DC Output Current	50	50	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

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NOTES:

1. VIH = 2.6V for $\overline{XI}$ input (commercial).
   VIH = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V±10%, TA = 0°C to +70°C; Military: VCC = 5.0V±10%, TA = –55°C to +125°C)

Symbol	Parameter	IDT7203/7204/ IDT7205 Commercial tA = 20ns			IDT7203/7204/ IDT7205/7206 Commercial tA = 25,35,50,80,120ns			IDT7203/7204/ IDT7205/7206 Military tA = 30,40,50,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	–1	—	1	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage IOH = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage IOH = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	120(4)	—	—	120(4)	—	—	150(4)	mA
ICC2(3)	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL/RT}$=VIH)	—	—	12	—	—	12	—	—	25	mA
ICC3(L)(3)	Power Down Current (All Input = VCC - 0.2V)	—	—	2	—	—	2	—	—	4	mA
ICC3(S)(3)	Power Down Current (All Input = VCC - 0.2V)	—	—	8	—	—	8	—	—	12	mA

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NOTES:

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{R}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

		Commercial		Commercial		Military		Commercial		
		7203S/L20 7204S/L20 7205S/L20 7206S/L20		7203S/L25 7204S/L25 7205S/L25 7206S/L25		7203S/L30 7204S/L30 7205S/L30 7206S/L30		7203S/L35 7204S/L35 7205S/L35 7206S/L35		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width (2)	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Low to Data Bus Low (3)	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write High to Data Bus Low Z (3,4)	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z (3)	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width (2)	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width(2)	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time(3)	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width(2)	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time (3)	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	30	—	35	—	40	—	45	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	30	—	35	—	40	—	45	ns
t_{RTF}	Retransmit Low to Flags Valid	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width(2)	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	15	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

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AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

		Military		Commercial and Military						
		7203S/L40 7204S/L40 7205S/L40 7206S/L40		7203S/L50 7204S/L50 7205S/L50 7206S/L50		7203S/L80 7204S/L80 7205S/L80 7206S/L80		7203S/L120 7204S/L120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	20	—	15	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width [2]	40	—	50	—	80	—	120	—	ns
t_{RLZ}	Read Low to Data Bus Low [3]	5	—	10	—	10	—	10	—	ns
t_{WLZ}	Write High to Data Bus Low Z [3,4]	10	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read High to Data Bus High Z [3]	—	25	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width [2]	40	—	50	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[3]	40	—	50	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	40	—	50	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time [3]	40	—	50	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	100	—	140	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	50	—	65	—	100	—	140	ns
t_{RTF}	Retransmit Low to Flags Valid	—	50	—	65	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	35	—	45	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	40	—	50	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	35	—	45	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	80	—	120	—	ns
t_{XOL}	Read/Write Low to $\overline{XO}$ Low	—	40	—	50	—	80	—	120	ns
t_{XOH}	Read/Write High to $\overline{XO}$ High	—	40	—	50	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	40	—	50	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	15	—	ns

NOTES:

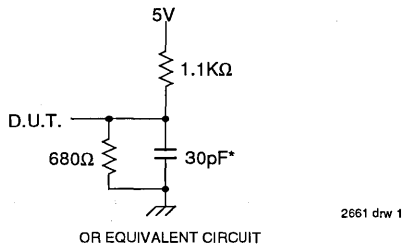
2661 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2661 tbl 06



2661 drw 1

OR EQUIVALENT CIRCUIT

Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

2661 tbl 07

1. This parameter is sampled and not 100% tested.
2. With output deselected.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low on the falling edge of the last write signal. inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096/8192/16384 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

5

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 2048/4096/8192/16384 writes.

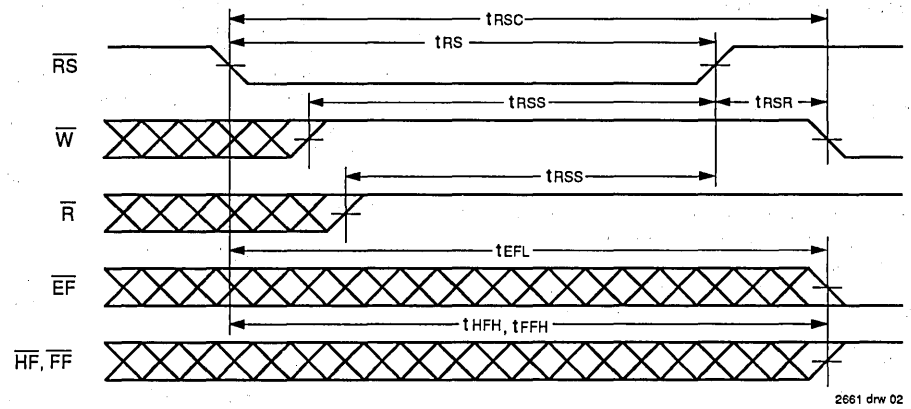
EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8) — Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTE:
1. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

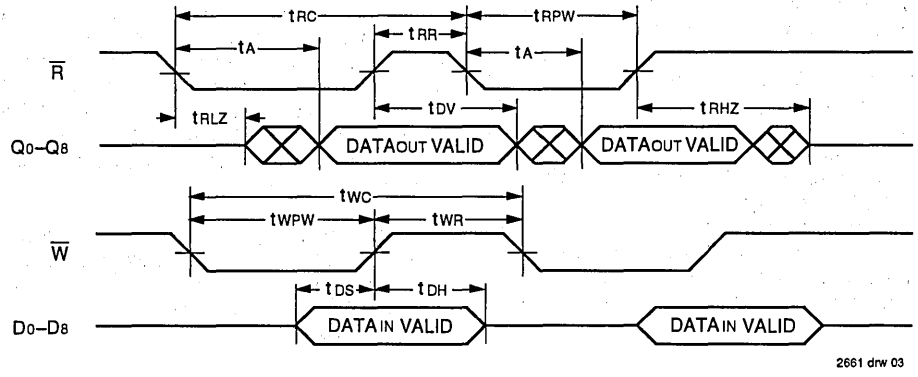


Figure 3. Asynchronous Write and Read Operation

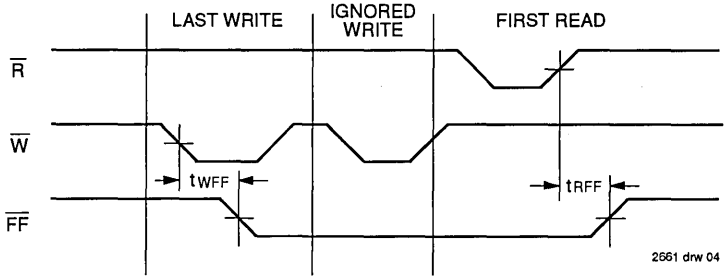


Figure 4. Full FlagTiming From Last Write to First Read

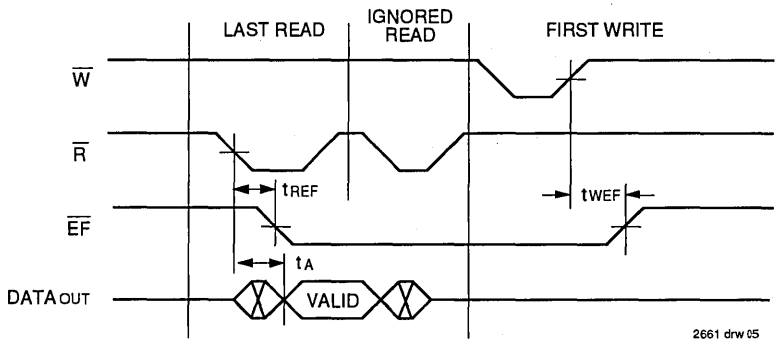
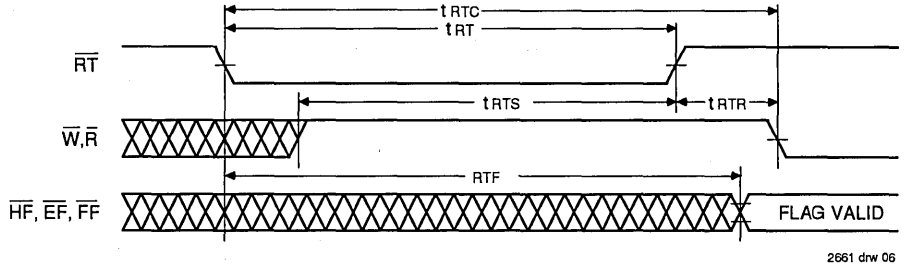


Figure 5. Empty Flag Timing From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

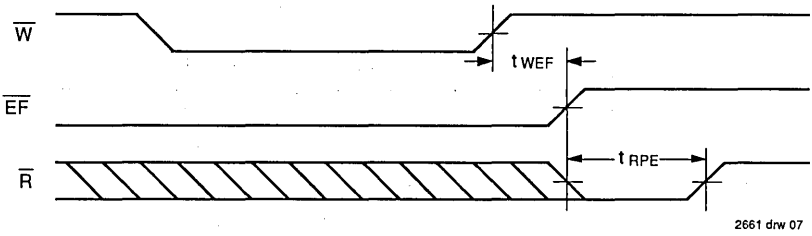


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

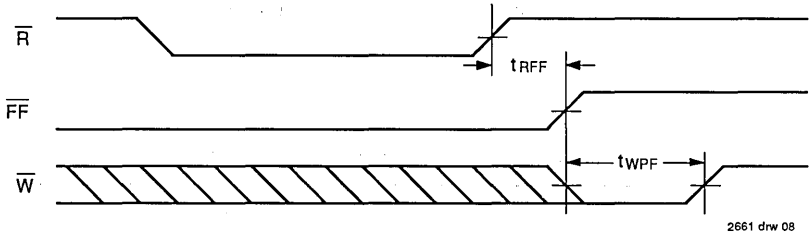


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse.

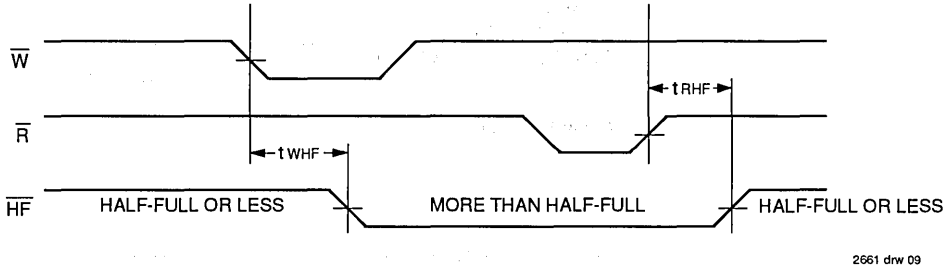


Figure 9. Half-Full Flag Timing

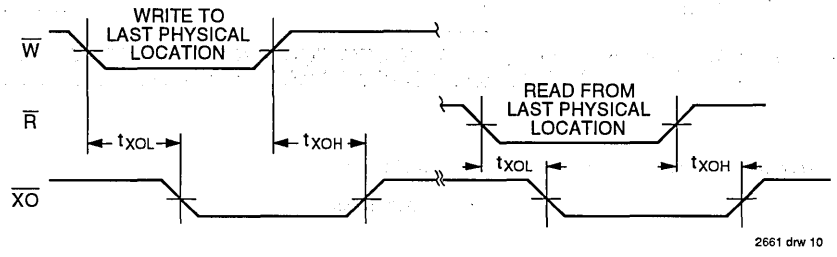


Figure 10. Expansion Out

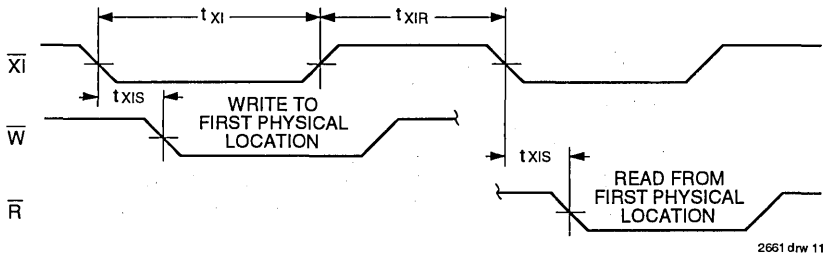


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7203/7204/7205/7206 may be used when the application requirements are for 2048/4096/8192/16384 words or less. The IDT7203/7204/7205/7206 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7203/7204/7205/7206 can easily be adapted to applications when the requirements are for greater than 2048/4096/8192/16384 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206s. Any depth can be attained by adding additional IDT7203/7204/7205/7206s. The IDT7203/7204/7205/7206 operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206s. Any word width can be attained by adding additional IDT7203/7204/7205/7206s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

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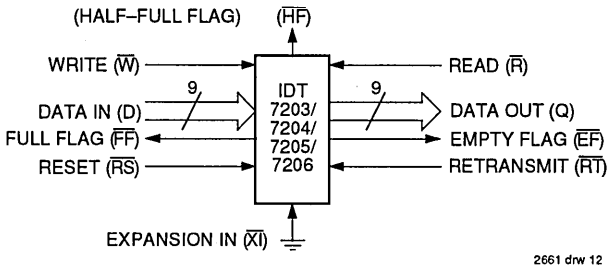
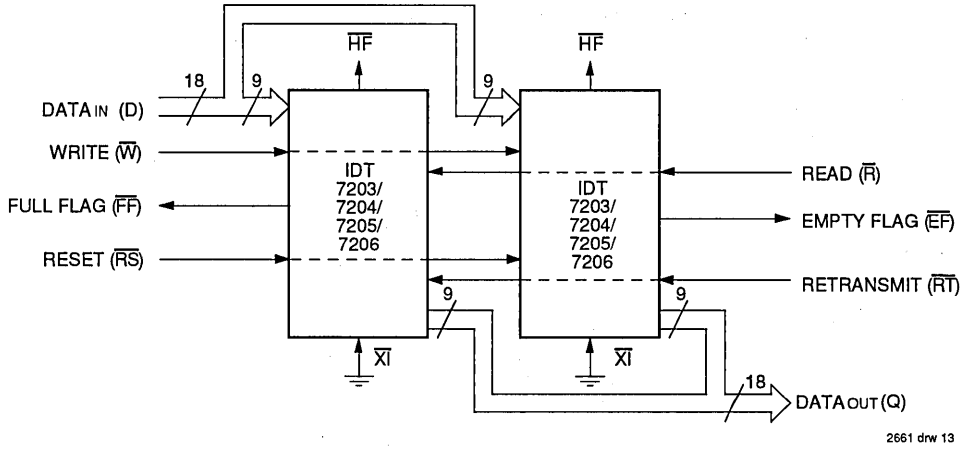


Figure 12. Block Diagram of 2048 x 9/4096 x 9/8192 x 9/16384 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18/8192 x 18/16384 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will Increment if flag is high.

2661 tbl 07

TABLE II – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2661 tbl 08

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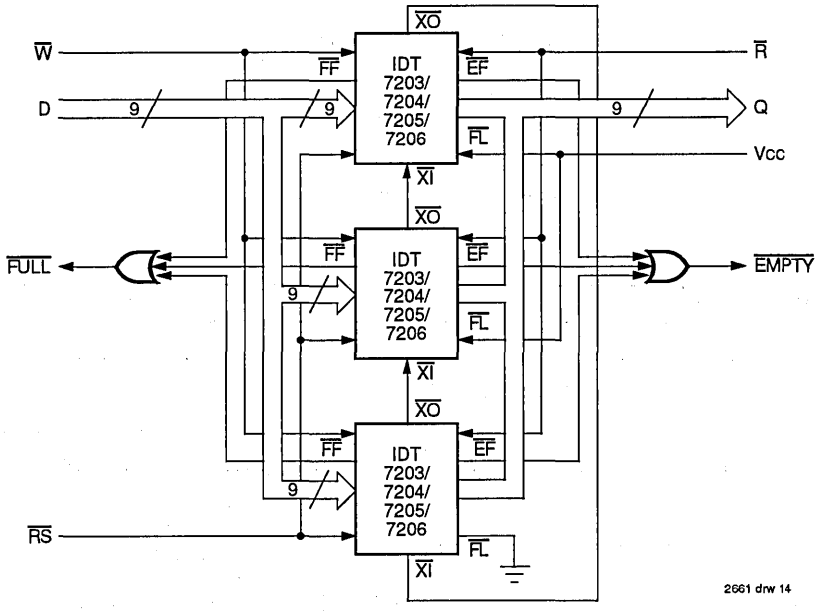
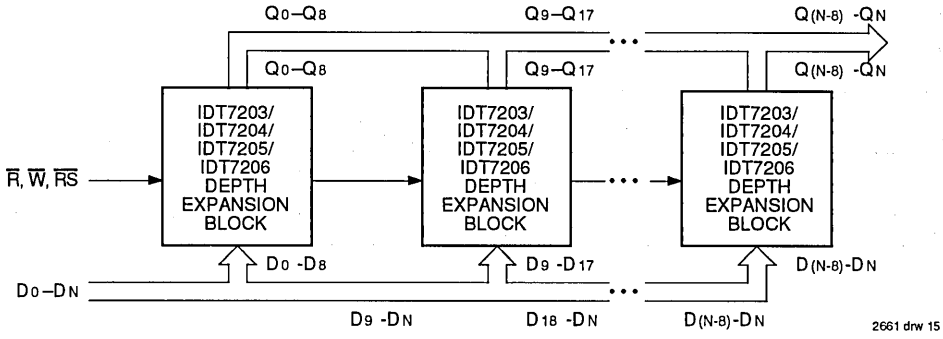


Figure 14. Block Diagram of 6149 x 9/12298 x 9/24596 x 9/49152 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

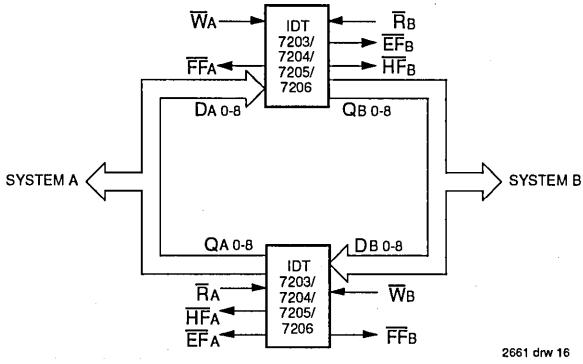


Figure 16. Bidirectional FIFO Operation

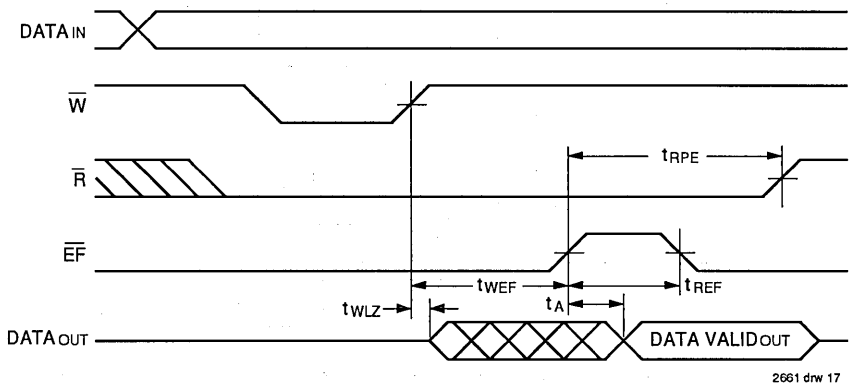


Figure 17. Read Data Flow-Through Mode

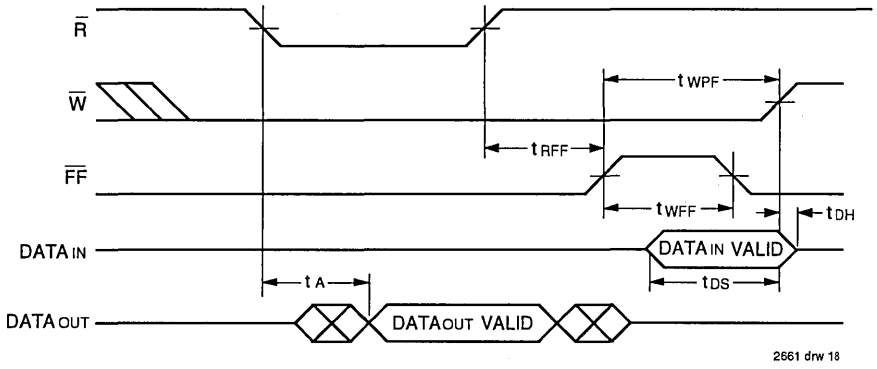


Figure 18. Write Data Flow-Through Mode

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Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 18-BIT, 512 x 18-BIT & 1K x 18-BIT

ADVANCE INFORMATION
IDT72005
IDT72015
IDT72025

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 18 organization (IDT72005)
- 512 x 18 organization (IDT72015)
- 1K x 18 organization (IDT72025)
- High speed—25ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Status Flags: Empty, Full, Almost Full, Almost Empty
- Two OE pins for bus matching applications
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72005/72015/72025 are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

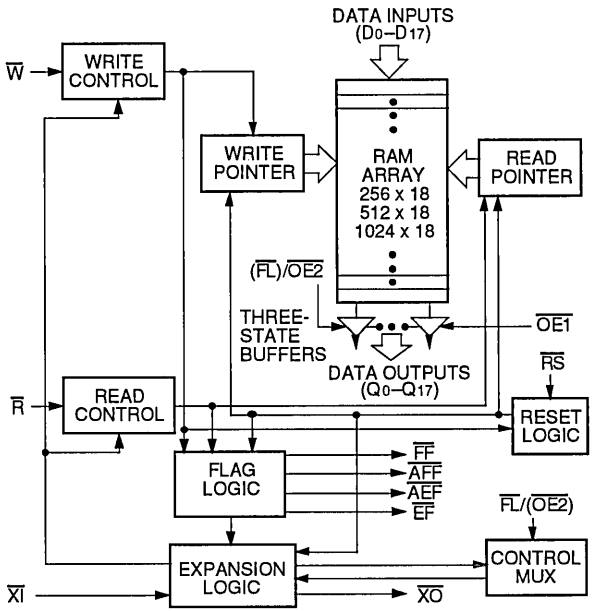
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 25ns (40MHz).

The device utilizes an 18-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features two $\overline{OE}$ pins for bus matching applications. In single device mode, these pins can be used to read data at different time intervals.

These FIFOs have two end point flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$); and two partial flags with fixed offsets, Almost Full ($\overline{AFF}$) and Almost Empty ($\overline{AEF}$) for higher memory utilization. All flags are active Low outputs.

The IDT72005/72015/72025 are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2553 drw 01

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Integrated Device Technology, Inc.

CMOS PARALLEL FLAGGED FIFO WITH $\overline{OE}$ 1K x 9, 2K x 9, 4K x 9

IDT72021
IDT72031
IDT72041

FEATURES:

- First-In/First-Out dual-port memory
- Bit organization
  - IDT72021—1K x 9
  - IDT72031—2K x 9
  - IDT72041—4K x 9
- Ultra high speed
  - IDT72021—25ns access time, 35ns cycle time
  - IDT72031—35ns access time, 45ns cycle time
  - IDT72041—35ns access time, 45ns cycle time
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost Empty/Almost Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags, ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's CEMOS™ technology. Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B, for high reliability systems.

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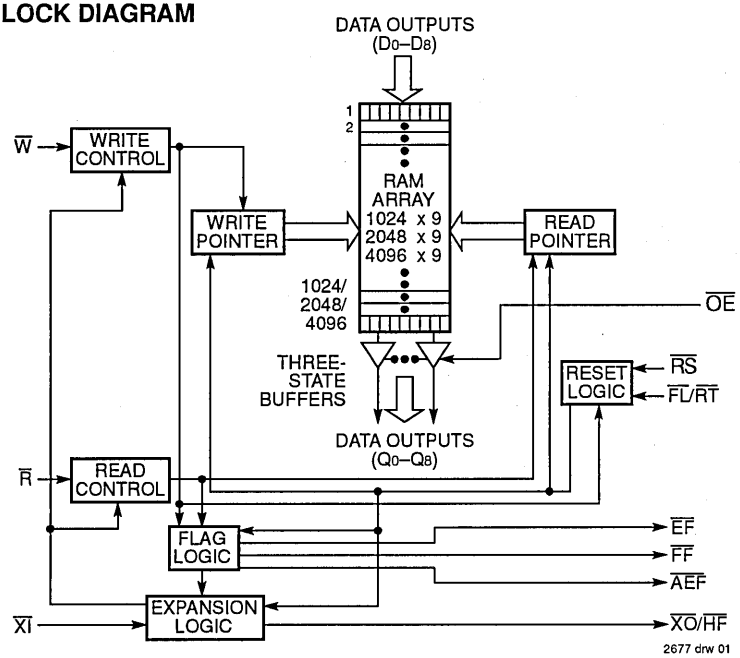
FUNCTIONAL BLOCK DIAGRAM



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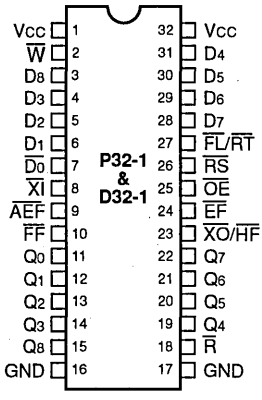
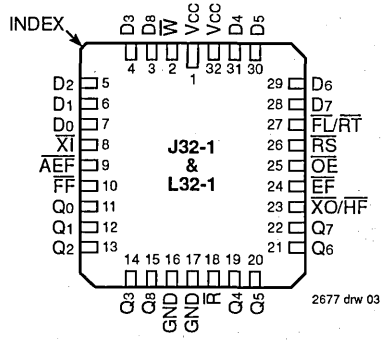
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be high during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	When WRITE is low, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{FF}$ must be high. When the FIFO is full ($\overline{FF}$-low), the internal WRITE operation is blocked.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked. The three-state output buffer is controlled by the read signal and the external output control ($\overline{OE}$).
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ and $\overline{W}$ must be high before setting $\overline{FL/RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$-low indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set high, the data flow through the three-state output buffer is inhibited regardless of an active READ operation. A read operation does increment the read pointer in this situation. When $\overline{OE}$ is set low, Q0-Q8 are still in a high impedance condition if no READ occurs. For a complete READ operation with data ppearing on Q0-Q8, both $\overline{R}$ and $\overline{OE}$ should be asserted low.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO/HF}$	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q0–Q8	Outputs	O	Data outputs for 9-bit wide data.

2677 tbl 01

STATUS FLAG

Number of Words in FIFO						
1K	2K	4K	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

2677 tbl I 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2677 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2677 tbl 03

1. These parameters are sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2677 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS — IDT72021

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72021 Commercial t_A=25,35ns			IDT72021 Military t_A=30,40ns			IDT72021 Commercial t_A=50,65,80,120ns			IDT72021 Military t_A=50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}(3,4)	Active Power Supply Current	—	—	120	—	—	140	—	50	80	—	70	100	mA
I_{CC2}(3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	12	—	—	20	—	5	8	—	8	15	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA

2677 tbl 06

DC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72031 IDT72041 Commercial t_A=35,50,65,80,120ns			IDT72031 IDT72041 Military t_A=40,50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3,5)	Active Power Supply Current	—	75	120	—	100	150	mA
I_{CC2}(3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	2	—	—	4	mA

NOTES:

2677 tbl 07

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with $\overline{OE}$ = HIGH.
4. Tested at f = 20MHz.
5. Tested at f = 15.3 MHz.

AC ELECTRICAL CHARACTERISTICS — IDT72021[1]

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = –55°C to +125°C)

		Com'l		Mil.		Com'l		Mil.		
		72021 x 25		72021 x 30		72021 x 35		72021 x 40		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Shift Frequency	—	28.5	—	25	—	22.2	—	20	MHz
tRC	$\overline{R}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tA	Access Time	—	25	—	30	—	35	—	40	ns
tRR	$\overline{R}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	18	—	20	—	20	—	25	ns
tWC	$\overline{W}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tWR	$\overline{W}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	$\overline{RS}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRSS	$\overline{RS}$ Set-up Time	25	—	30	—	35	—	40	—	ns
tRSR	$\overline{RS}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRTC	$\overline{RT}$ Cycle Time	35	—	40	—	45	—	50	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	25	—	30	—	35	—	40	—	ns
tRTR	$\overline{RT}$ Recovery Time	10	—	10	—	10	—	10	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	35	—	40	—	45	—	50	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	35	—	40	—	45	—	50	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	25	—	30	—	30	—	35	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	25	—	30	—	30	—	35	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	25	—	30	—	35	—	40	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	25	—	30	—	30	—	35	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	25	—	30	—	30	—	35	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	35	—	40	—	45	—	50	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	35	—	40	—	45	—	50	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	25	—	30	—	35	—	40	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	12	0	15	0	17	0	20	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	12	0	15	0	17	0	20	ns
tAOE	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	15	—	18	—	20	—	25	ns

NOTES:

2677 tbl 08

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS — IDT72021[1] (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Military and Commercial								
		72021 x 50		72021 x 65		72021 x 80		72021 x 120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	$\overline{R}$ Cycle Time	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	50	—	65	—	80	—	120	ns
t_{RR}	$\overline{R}$ Recovery Time	15	—	15	—	20	—	20	—	ns
t_{RPW}	$\overline{R}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	10	—	10	—	10	—	10	—	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	30	—	30	—	30	—	35	ns
t_{WC}	$\overline{W}$ Cycle Time	65	—	80	—	100	—	140	—	ns
t_{WPW}	$\overline{W}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
t_{WR}	$\overline{W}$ Recovery Time	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	5	—	10	—	10	—	10	—	ns
t_{RSC}	$\overline{RS}$ Cycle Time	65	—	80	—	100	—	140	—	ns
t_{RS}	$\overline{RS}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
t_{RSS}	$\overline{RS}$ Set-up Time	50	—	65	—	80	—	120	—	ns
t_{RSR}	$\overline{RS}$ Recovery Time	15	—	15	—	20	—	20	—	ns
t_{RTC}	$\overline{RT}$ Cycle Time	65	—	80	—	100	—	140	—	ns
t_{RT}	$\overline{RT}$ Pulse Width[2]	50	—	65	—	80	—	120	—	ns
t_{RTR}	$\overline{RT}$ Recovery Time	15	—	15	—	20	—	20	—	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	65	—	80	—	100	—	140	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	65	—	80	—	100	—	140	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	—	45	—	60	—	60	—	60	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	—	45	—	60	—	60	—	60	ns
t_{RPE}	$\overline{R}$ Pulse Width After $\overline{EF}$ High	50	—	65	—	80	—	120	—	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	—	45	—	60	—	60	—	60	ns
t_{WFF}	$\overline{W}$ Low to $\overline{EF}$ Low	—	45	—	60	—	60	—	60	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	—	65	—	80	—	100	—	140	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	—	65	—	80	—	100	—	140	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	50	—	65	—	80	—	120	—	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	65	—	80	—	100	—	140	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	65	—	80	—	100	—	140	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable)[3]	0	25	0	30	0	30	0	30	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	25	0	30	0	30	0	30	ns
t_{AOE}	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	30	—	40	—	40	—	40	ns

NOTES:

2677 tbl 09

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041[1]

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = −55°C to +125°C)

Symbol	Parameter	72031 x 35 72041 x 35		72031 x 40 72041 x 40		72031 x 50 72041 x 50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	22.2	—	20	—	15	MHz
tRC	$\overline{R}$ Cycle Time	45	—	50	—	65	—	ns
tA	Access Time	—	35	—	40	—	50	ns
tRR	$\overline{R}$ Recovery Time	10	—	10	—	15	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	35	—	40	—	50	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	—	5	—	10	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	20	—	25	—	30	ns
tWC	$\overline{W}$ Cycle Time	45	—	50	—	65	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	35	—	40	—	50	—	ns
tWR	$\overline{W}$ Recovery Time	10	—	10	—	15	—	ns
tDS	Data Set-up Time	18	—	20	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	5	—	ns
tRSC	$\overline{RS}$ Cycle Time	45	—	50	—	65	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	35	—	40	—	50	—	ns
tRSS	$\overline{RS}$ Set-up Time	35	—	40	—	50	—	ns
tRSR	$\overline{RS}$ Recovery Time	10	—	10	—	15	—	ns
tRTC	$\overline{RT}$ Cycle Time	45	—	50	—	65	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	35	—	40	—	50	—	ns
tRTR	$\overline{RT}$ Recovery Time	10	—	10	—	15	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	30	—	35	—	45	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	30	—	35	—	45	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	45	—	50	—	65	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	45	—	50	—	65	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	17	0	20	0	25	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	17	0	20	0	25	ns
tAOE	$\overline{OE}$ Low Data Valid (Q0–Q8)	—	20	—	25	—	30	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 10

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AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041[1] (Continued)

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = –55°C to +125°C)

Symbol	Parameter	72031 x 65 72041 x 65		72031 x 80 72041 x 80		72031 x 120 72041 x 120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	12.5	—	10	—	7	MHz
tRC	$\overline{R}$ Cycle Time	80	—	100	—	140	—	ns
tA	Access Time	—	65	—	80	—	120	ns
tRR	$\overline{R}$ Recovery Time	15	—	20	—	20	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRLZ	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	10	—	10	—	10	—	ns
tWLZ	$\overline{W}$ Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse High	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse High to Data Bus at High Z[3]	—	30	—	30	—	35	ns
tWC	$\overline{W}$ Cycle Time	80	—	100	—	140	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	65	—	80	—	120	—	ns
tWR	$\overline{W}$ Recovery Time	15	—	20	—	20	—	ns
tDS	Data Set-up Time	30	—	40	—	40	—	ns
tDH	Data Hold Time	10	—	10	—	10	—	ns
tRSC	$\overline{RS}$ Cycle Time	80	—	100	—	140	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRSS	$\overline{RS}$ Set-up Time	65	—	80	—	120	—	ns
tRSR	$\overline{RS}$ Recovery Time	15	—	20	—	20	—	ns
tRTC	$\overline{RT}$ Cycle Time	80	—	100	—	140	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	65	—	80	—	120	—	ns
tRTR	$\overline{RT}$ Recovery Time	15	—	20	—	20	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tREF	$\overline{R}$ Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tRFF	$\overline{R}$ High to $\overline{FF}$ High	—	60	—	60	—	60	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ High	65	—	80	—	120	—	ns
tWEF	$\overline{W}$ High to $\overline{EF}$ High	—	60	—	60	—	60	ns
tWFF	$\overline{W}$ Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tWHF	$\overline{W}$ Low to $\overline{HF}$ Low	—	80	—	100	—	140	ns
tRHF	$\overline{R}$ High to $\overline{HF}$ High	—	80	—	100	—	140	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ High	65	—	80	—	120	—	ns
tRF	$\overline{R}$ High to Transitioning $\overline{AEF}$	—	80	—	100	—	140	ns
tWF	$\overline{W}$ Low to Transitioning $\overline{AEF}$	—	80	—	100	—	140	ns
tOEHZ	$\overline{OE}$ High to High-Z (Disable)[3]	0	30	0	30	0	30	ns
tOELZ	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	30	0	30	0	30	ns
tAOE	$\overline{OE}$ Low Data Valid (Q_0–Q_8)	—	40	—	40	—	40	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2677 tbl 11

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2677 tbl 12

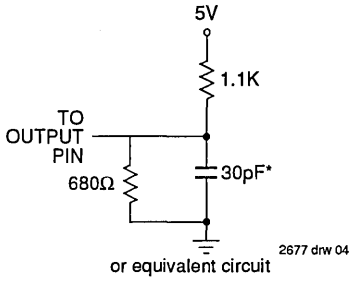


Figure 1. Output Load

* Includes scope and jig capacitances.

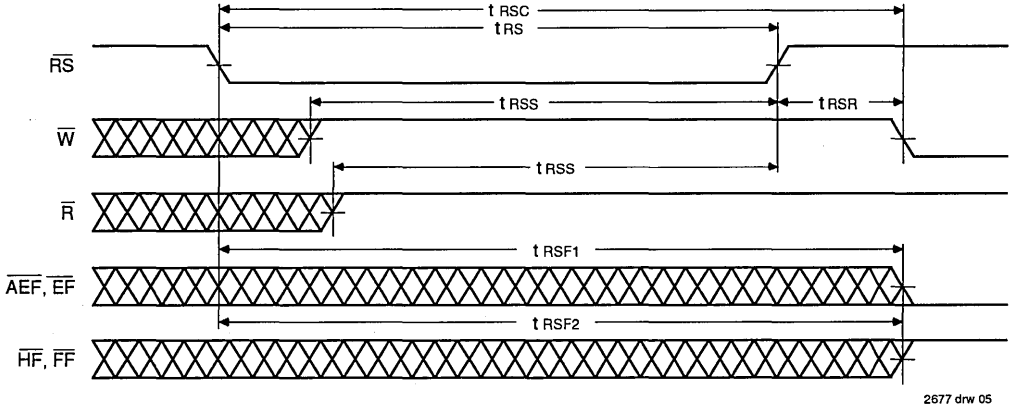


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Reset, but flags will be valid at tRSC.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

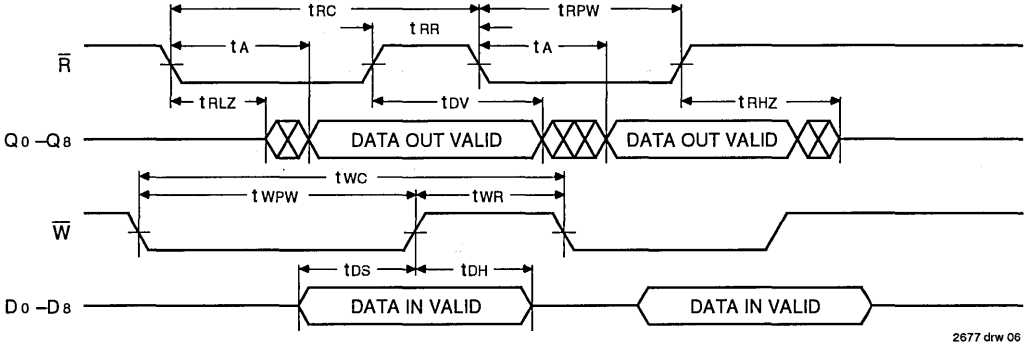


Figure 3. Asynchronous Write and Read Operation

NOTE:
1. Assume $\overline{OE}$ is asserted low.

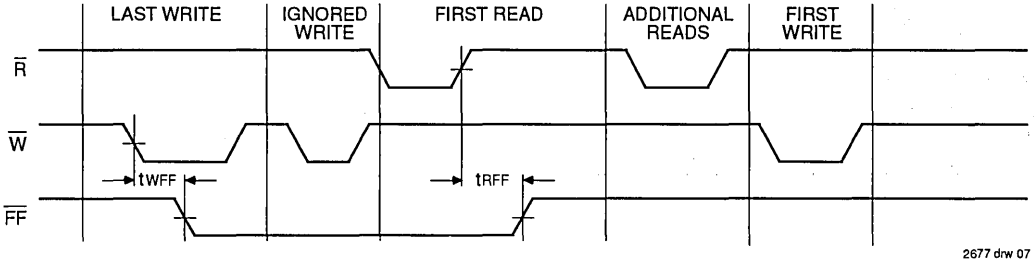


Figure 4. Full Flag From Last Write to First Read

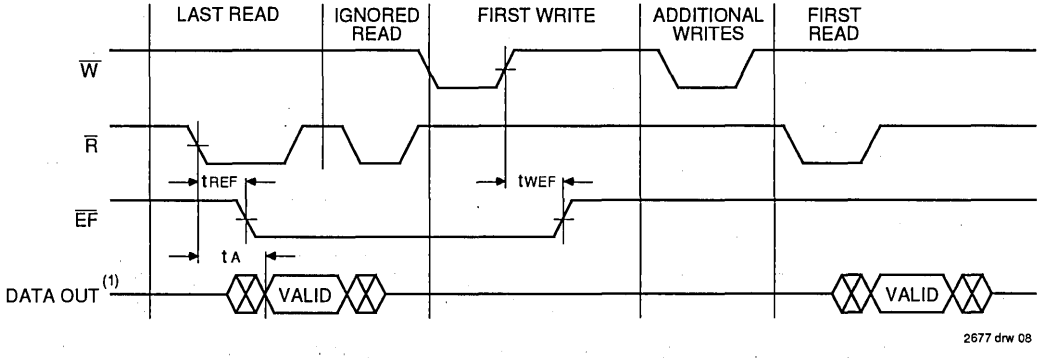


Figure 5. Empty Flag From Last Read to First Write

NOTE:
1. Assume $\overline{OE}$ is asserted low.

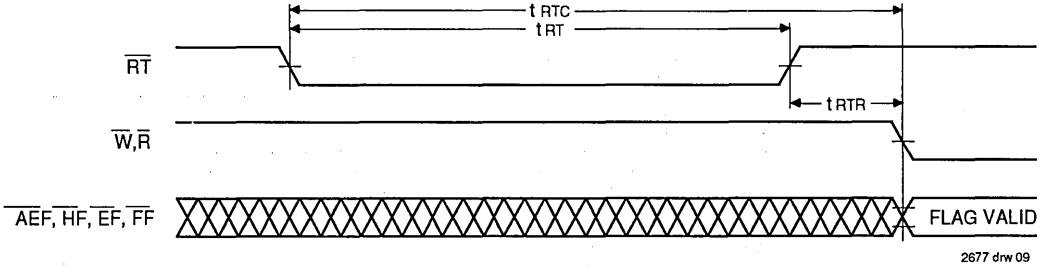


Figure 6. Retransmit

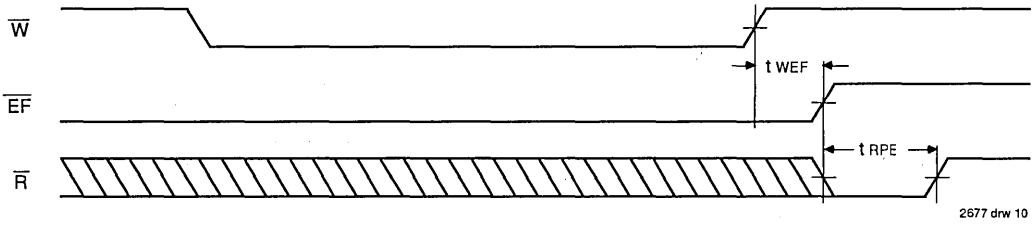


Figure 7. Empty Flag Timing

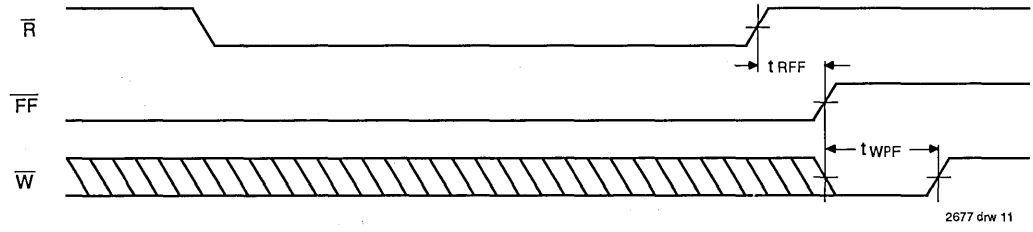


Figure 8. Full Flag Timing

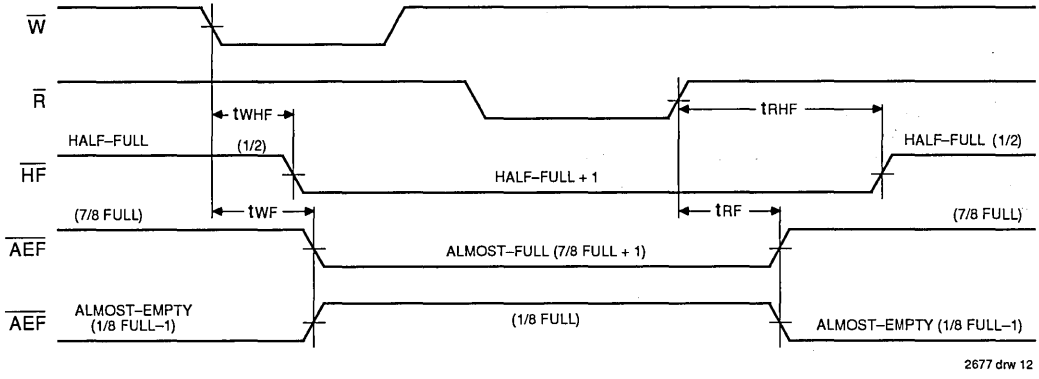


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

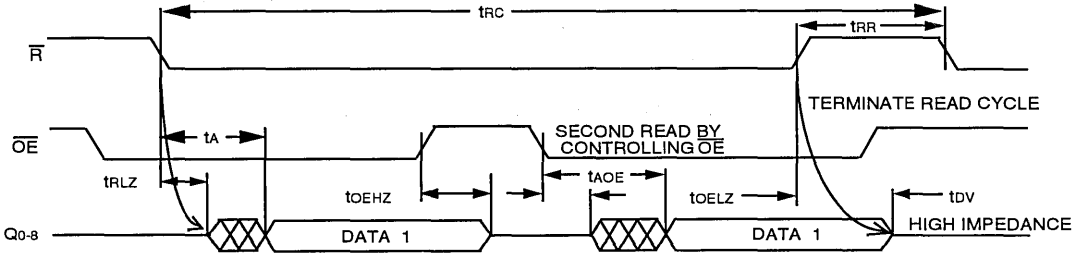


Figure 10. Output Enable and Read Operation Timings

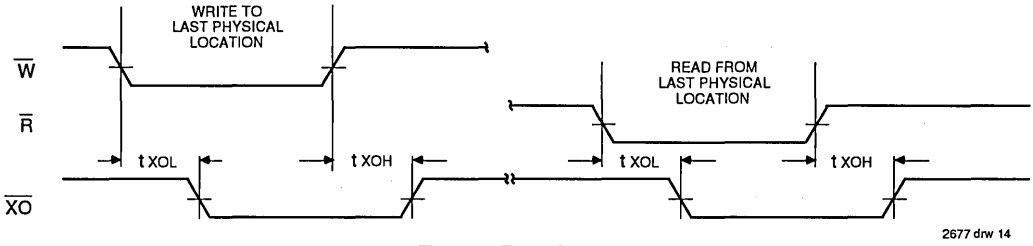


Figure 11. Expansion Out

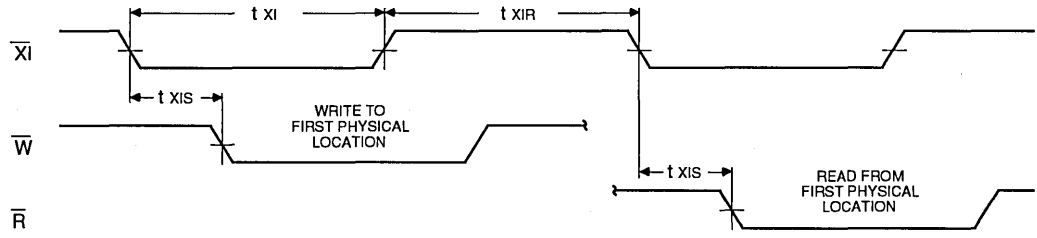


Figure 12. Expansion In

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 13).

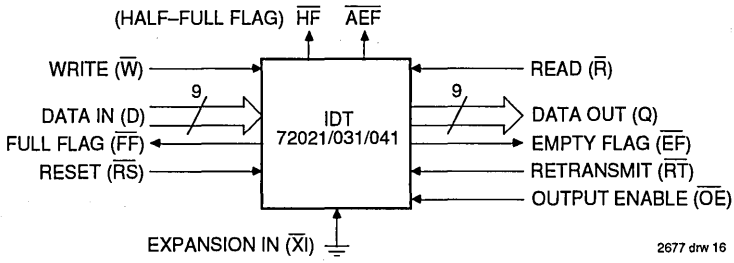


Figure 13. Block Diagram of Single 1K/2K/4K x 9 FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$) can be detected from any one device. Figure 14 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.

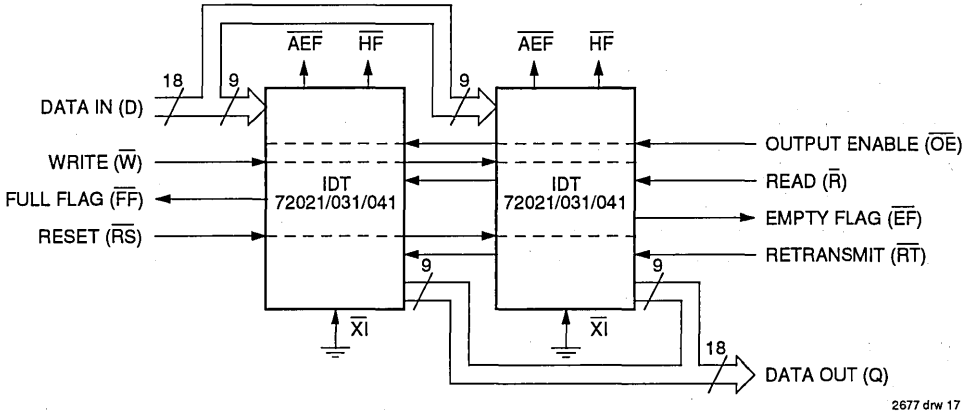


Figure 14. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, $\overline{HF}$ and $\overline{AEF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

5

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 15 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 15.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 15.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techinques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 16).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 17. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 18), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge. It remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will be deassert the Empty Flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line, being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X	X

NOTE: 2677 tbl 13
1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE: 2677 tbl 14
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15. $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output, $\overline{AEF}$ = Almost Empty/Almost Full Flag.

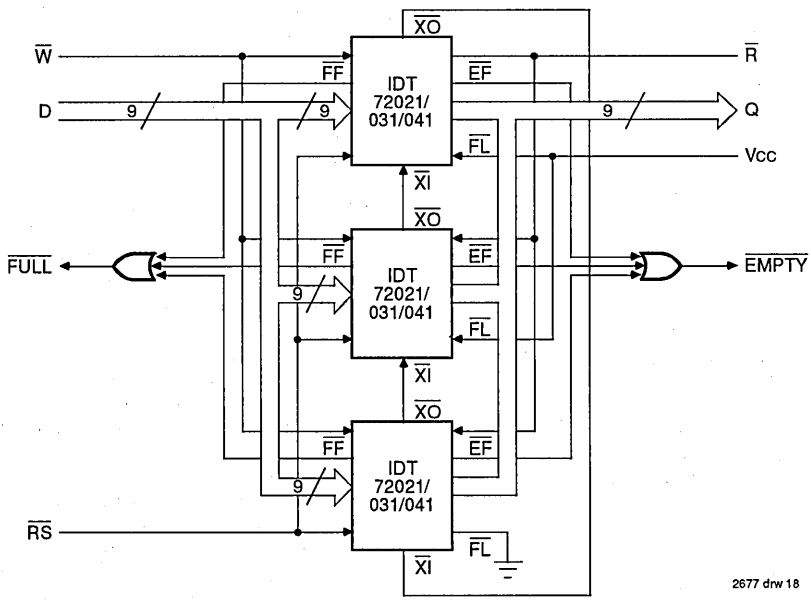


Figure 15. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)

NOTE:
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

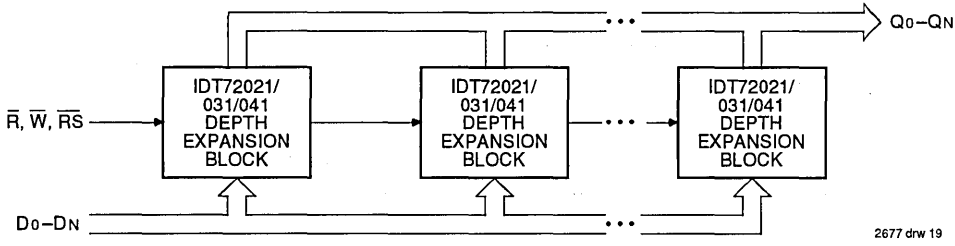


Figure 16. Compound FIFO Expansion

NOTES:
1. For depth expansion block see section od Depth Expansion and Figure 15.
2. For Flag detection see section on Width Expansion and Figure 14.

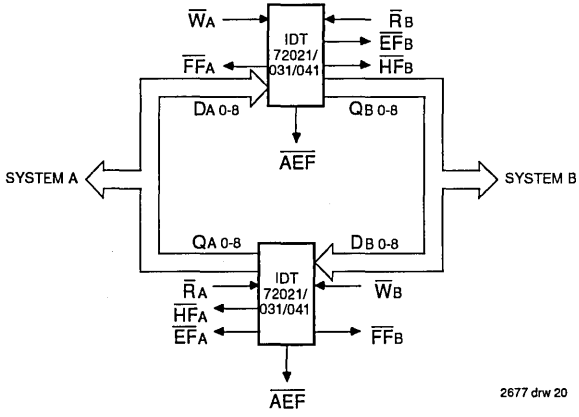


Figure 17. Bidirectional FIFO Mode

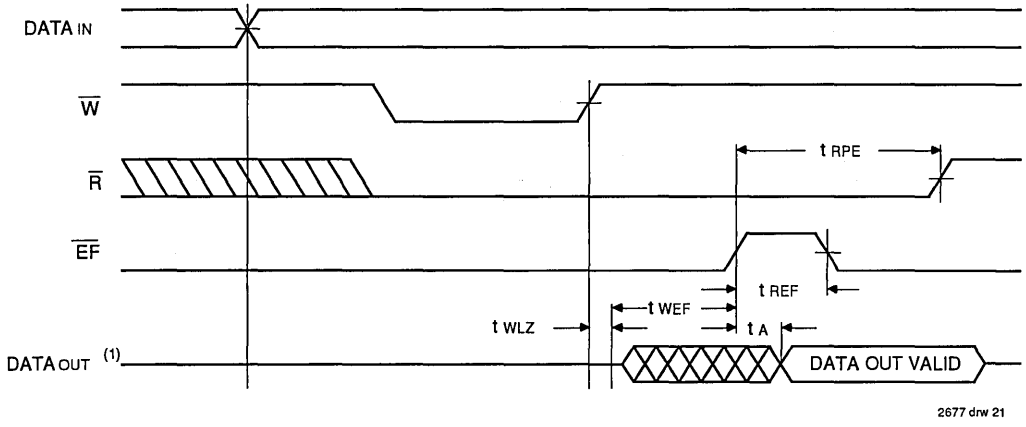


Figure 18. Read Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted low.

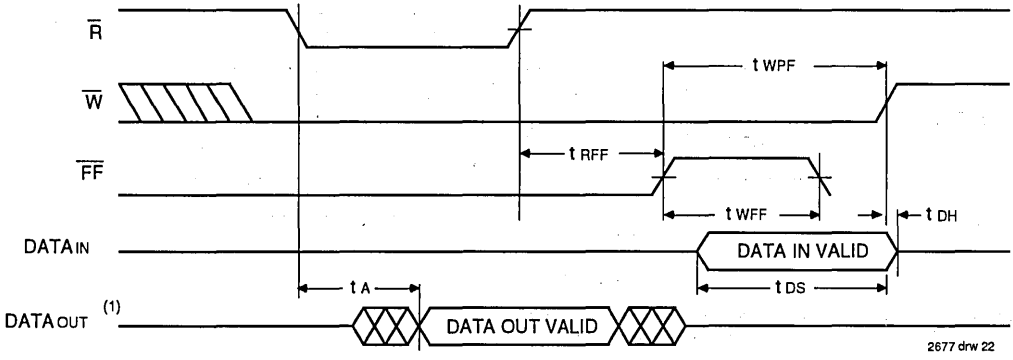


Figure 19. Write Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted low.

Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT72103
IDT72104

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial input/output frequency
- Serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel operations
- Expandable in both depth and width with no external components
- Flexishift™ — Sets programmable serial word width from 4 bits to any width with no external components
- Multiple flags: Full, Almost-Full (Full-1/8),Full-Minus-One, Empty, Almost-Empty (Empty + 1/8), Empty-Plus One, and Half-Full
- Asynchronous and simultaneous read or write operations
- Dual-port, zero fall-through time architecture
- Retransmit capability in single-device mode
- Packaged in 40-pin ceramic and plastic DIP, 44-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

APPLICATIONS:

- High-speed data acquisition systems
- Local area network (LAN) buffer
- High-speed modem data buffer
- Remote telemetry data buffer
- FAX raster video data buffer
- Laser printer engine data buffer
- High-speed parallel bus-to-bus communications
- Magnetic media controllers
- Serial link buffer

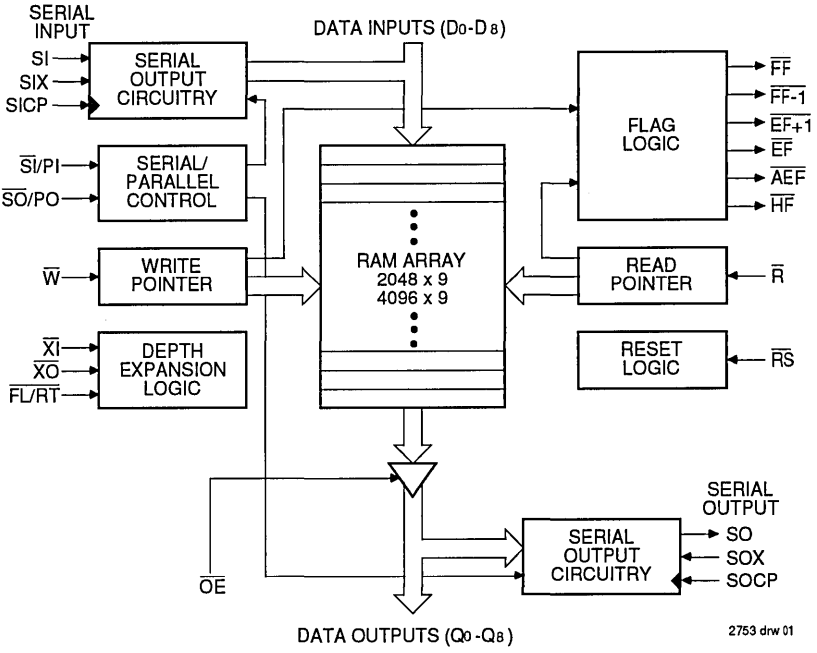
DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs to be used with high-performance systems for functions such as serial communications, laser printer engine control and local area networks.

A serial input, a serial output and two 9-bit parallel ports make four modes of data transfer possible: serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel. The IDT72103/ 72104 are expandable in both depth and width for all of these operational configurations.

5

FUNCTIONAL BLOCK DIAGRAM



CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

DESCRIPTION (CONTINUED)

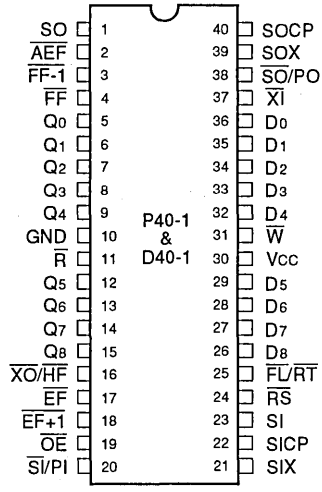
The IDT72103/72104 may be configured to handle serial word widths of four or greater using IDT's unique Flexishift feature. Flexishift allows serial width and depth expansion without external components. For example, you may configure a 4K x 24 FIFO using three IDT72104s in a serial width expansion configuration.

Seven flags are provided to signal memory status of the FIFO. The flags are $\overline{FF}$ (Full), $\overline{AF}$ (7/8 full), $\overline{FF-1}$ (Full-minus-one), $\overline{EF}$ (Empty), $\overline{AE}$ (1/8 full), $\overline{EF+1}$ (Empty-plus-one), and $\overline{HF}$ (Half-full).

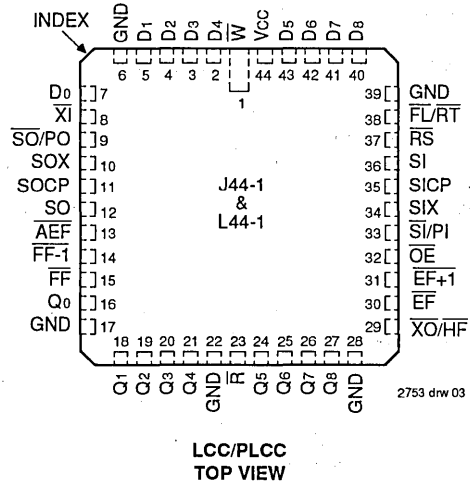
Read ($\overline{R}$) and Write ($\overline{W}$) control pins are provided for asynchronous and simultaneous operations. An output enable ($\overline{OE}$) control pin is available on the parallel output port for high impedance control. The depth expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/72104 are manufactured using IDT's CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2753 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2753 tbl 04

1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2753 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0-D8	Data Inputs Serial Input Word Width Select	I/O	In a parallel input configuration - data inputs for 9-bit wide data. In a serial input configuration - one of the nine output pins is used to select the serial input word width.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{EF}$, $\overline{EF+1}$, $\overline{AEF}$ are all LOW after a reset, while $\overline{FF}$, $\overline{FF-1}$, $\overline{HF}$ are HIGH after a reset.
$\overline{W}$	Write	I	A parallel word write cycle is initiated on the falling edge of $\overline{W}$ if the $\overline{FF}$ is high. When the FIFO is full, FF will go low inhibiting further write operations to prevent data overflow. In a serial input configuration, data bits are clocked into the input shift register and the write pointer does not advance until a full parallel word is assembled. One of the pins, Di, is connected to $\overline{W}$ and advances the write pointer every i-th serial input clock.
$\overline{R}$	Read	I	A read cycle is initiated on the falling edge of $\overline{R}$ if the $\overline{EF}$ is high. After all the data from the FIFO has been read $\overline{EF}$ will go low Inhibiting further read operations. In a serial output configuration, a data word is read from memory into the output shift register. One of the pins, Qj, is connected to $\overline{R}$ and advances the read pointer every j-th serial output clock.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual-purpose pin. In multiple-device mode, $\overline{FL/RT}$ is grounded to indicate the first device loaded. In single-device mode, $\overline{FL/RT}$ acts as the retransmit input. Single-device mode is initiated by grounding the $\overline{XI}$ pin.
$\overline{XI}$	Expansion In	I	In single-device mode, $\overline{XI}$ is grounded. In depth expansion or daisy chain mode, $\overline{XI}$ is connected to the $\overline{XO}$ pin of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled. When $\overline{OE}$ is HIGH, the parallel output buffers are placed in a high-impedance state.
Q0-Q8	Data Outputs / Serial Output Word Width Select	O	In a parallel output configuration - data outputs for 9-bit wide data. In a serial output configuration - one of nine output pins used to select the serial output word width.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is asserted LOW when the FIFO is full and further write operations are inhibited. When the $\overline{FF}$ is HIGH, the FIFO is not full and data can be written into the FIFO.
$\overline{FF-1}$	Full-1 Flag	O	$\overline{FF-1}$ goes LOW when the FIFO memory array is one word away from being full. It will remain LOW when every memory location is filled.

2753 tbl 01

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PIN DESCRIPTION

Symbol	Name	I/O	Description
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	$\overline{HF}$ is LOW when the FIFO is more than half-full in the single device or width expansion modes. The $\overline{HF}$ will remain LOW until the difference between the write and read pointers is less than or equal to one-half of the FIFO memory. In depth expansion mode, a pulse is written from $\overline{XO}$ to $\overline{XI}$ of the next device when the last location in the FIFO is filled. Another pulse is sent from $\overline{XO}$ to $\overline{XI}$ of the next device when the last FIFO location is read.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the FIFO is empty to 1/8 full or 7/8 full to completely full. If $\overline{AEF}$ is HIGH, then the FIFO is greater than 1/8 full, but less than 7/8 full.
$\overline{EF+1}$	Empty+1 Flag	O	$\overline{EF+1}$ is LOW when there is zero or one word word in the FIFO memory array.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ goes LOW when the FIFO is empty and further read operations are inhibited. $\overline{FF}$ is HIGH when the FIFO is not empty and data reads are permitted.
SI	Serial Input	I	Data input for serial data.
SO	Serial Output	O	Data output for serial data.
SICP	Serial Input Clock	I	This pin is the serial input clock. On the rising edge of the SICP signal, new serial data bits are read into the serial input shift register.
SOCP	Serial Output Clock	I	This pin is the serial output clock. On the rising edge of the SOCP signal, new serial data bits are read from the serial output shift register.
SIX	Serial Input Expansion	I	SIX controls the serial input expansion for word widths greater than 9 bits. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device. In parallel input configurations or serial input configurations of 9 bits or less, SIX is tied HIGH.
SOX	Serial Output Expansion	I	SOX controls the serial output expansion for word widths greater than 9 bits. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. In parallel output configurations or serial output configurations of 9 bits or less, SOX is tied HIGH.
$\overline{SI}$/PI	Serial/Parallel Input	I	When this pin is HIGH, the FIFO is in a parallel input configuration and accepts input data through D_0-D_8. When $\overline{SI}$/PI is LOW, the FIFO is in a serial input configuration and data is input through SI.
$\overline{SO}$/PO	Serial/Parallel Output	I	When this pin is HIGH, the FIFO is in a parallel output configuration and sends output data through Q_0-Q_8. When $\overline{SO}$/PO is LOW the FIFO is in a serial output configuration and data is input through SO.
GND	Ground		One ground pin for the DIP package and five ground pins for the LCC/PLCC packages.
Vcc	Power		One + 5V power pin.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72103/72104 Commercial t_A = 35, 50, 65, 80, 120 ns			IDT72103/72104 Military t_A = 40, 50, 65, 80, 120 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}[1]	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}[2]	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA[4]	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA[5]	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Average V_{CC} Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3}(L)$[3,6]	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3}(S)$[3,6]	Power Down Current	—	—	8	—	—	12	mA

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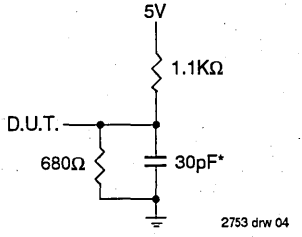
NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. For SO, I_{OUT} = -8mA.
5. For SO, I_{OUT} =16mA.
6. SOCP = SICP ≤ 0.2V; other Inputs = V_{CC} -0.2V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2753 tbl 07



or equivalent circuit

Figure 1. Ouput Load

*Includins jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.			
		IDT72103x35 IDT72104x35		IDT72103x40 IDT72104x40		IDT72103x50 IDT72104x50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
f_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	50	—	50	—	40	MHz	—
PARALLEL-OUTPUT MODE TIMINGS									
t_A	Access Time	—	35	—	40	—	50	ns	4
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns	4
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns	4
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns	4
t_{WLZ}	Write Pulse Low to Data Bus at Low Z[1]	5	—	5	—	15	—	ns	15
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	5	—	5	—	10	—	ns	4
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	—	20	—	25	—	30	ns	4
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS									
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns	3
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns	3
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns	3
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns	3
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns	3
RESET TIMINGS									
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns	2,18
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns	2,18
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns	2,18
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns	2,17,18
RESET TO FLAG TIMINGS									
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ Low	—	45	—	50	—	65	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ Low	—	45	—	50	—	65	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY									
t_{RSQL}	Reset Going Low to Q_{0-8} Low	20	—	20	—	35	—	ns	18
t_{RSQH}	Reset Going High to Q_{0-8} High	20	—	20	—	35	—	ns	18
t_{RSDL}	Reset Going Low to D_{0-8} Low	20	—	20	—	35	—	ns	17
RETRANSMIT TIMINGS									
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns	5
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns	5
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns	5
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns	5
PARALLEL MODE FLAG TIMINGS									
t_{REF}	Read Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns	6
t_{RFF}	Read High to $\overline{FF}$ High	—	30	—	35	—	45	ns	7
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	45	—	45	—	65	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	35	—	40	—	50	—	ns	15
t_{WEF}	Write High to $\overline{EF}$ High	—	30	—	35	—	45	ns	6
t_{WFF}	Write Low to $\overline{FF}$ Low	—	30	—	35	—	45	ns	7
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	45	—	50	—	65	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	35	—	40	—	50	—	ns	16

2753 tbl 08

NOTE:
1. Values guaranteed by design, not tested.

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Commercial and Military						Unit	Timing Figure
		IDT72103x65 IDT72104x65		IDT72103x80 IDT72104x80		IDT72103x120 IDT72104x120			
		Min.	Max.	Min.	Max.	Min.	Max.		
f_S	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	33	—	28	—	25	MHz	—
PARALLEL-OUTPUT MODE TIMINGS									
t_A	Access Time	—	65	—	80	—	120	ns	4
t_{RR}	Read Recovery Time	15	—	20	—	20	—	ns	4
t_{RPW}	Read Pulse Width	65	—	80	—	120	—	ns	4
t_{RC}	Read Cycle Time	80	—	100	—	140	—	ns	4
t_{WLZ}	Write Pulse Low to Data Bus at Low Z[1]	15	—	20	—	20	—	ns	15
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	10	—	10	—	10	—	ns	4
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	—	30	—	35	—	35	ns	4
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS									
t_{DS}	Data Set-up Time	30	—	40	—	40	—	ns	3
t_{DH}	Data Hold Time	10	—	10	—	10	—	ns	3
t_{WC}	Write Cycle Time	80	—	100	—	140	—	ns	3
t_{WPW}	Write Pulse Width	65	—	80	—	120	—	ns	3
t_{WR}	Write Recovery Time	15	—	20	—	20	—	ns	3
RESET TIMINGS									
t_{RSC}	Reset Cycle Time	80	—	100	—	140	—	ns	2,18
t_{RS}	Reset Pulse Width	65	—	80	—	120	—	ns	2,18
t_{RSS}	Reset Set-up Time	65	—	80	—	120	—	ns	2,18
t_{RSR}	Reset Recovery Time	15	—	20	—	20	—	ns	2,17,18
RESET TO FLAG TIMINGS									
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ Low	—	80	—	100	—	140	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ Low	—	80	—	100	—	140	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY									
t_{RSQL}	Reset Going Low to Q_{0-8} Low	50	—	65	—	105	—	ns	18
t_{RSQH}	Reset Going High to Q_{0-8} High	50	—	65	—	105	—	ns	18
t_{RSDL}	Reset Going Low to D_{0-8} Low	50	—	65	—	105	—	ns	17
RETRANSMIT TIMINGS									
t_{RTC}	Retransmit Cycle Time	80	—	100	—	140	—	ns	5
t_{RT}	Retransmit Pulse Width	65	—	80	—	120	—	ns	5
t_{RTS}	Retransmit Set-up Time	65	—	80	—	120	—	ns	5
t_{RTR}	Retransmit Recovery Time	15	—	20	—	20	—	ns	5
PARALLEL MODE FLAG TIMINGS									
t_{REF}	Read Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns	6
t_{RFF}	Read High to $\overline{FF}$ High	—	60	—	60	—	60	ns	7
t_{RF}	Read High to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	80	—	100	—	140	ns	8,9,10
t_{RE}	Read Low to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	80	—	100	—	140	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	65	—	80	—	120	—	ns	15
t_{WEF}	Write High to $\overline{EF}$ High	—	60	—	60	—	60	ns	6
t_{WFF}	Write Low to $\overline{FF}$ Low	—	60	—	60	—	60	ns	7
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	80	—	100	—	140	ns	8,9,10
t_{WE}	Write High to Transitioning $\overline{AEF}$ and $\overline{EF+1}$	—	80	—	100	—	140	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	65	—	80	—	120	—	ns	16

2753 tbl 09

NOTE:
1. Values guaranteed by design, not tested.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial IDT72103x35 IDT72104x35 Min.	Commercial IDT72103x35 IDT72104x35 Max.	Military IDT72103x40 IDT72104x40 Min.	Military IDT72103x40 IDT72104x40 Max.	Mil. and Com'l. IDT72103x50 IDT72104x50 Min.	Mil. and Com'l. IDT72103x50 IDT72104x50 Max.	Unit	Timing Figure
DEPTH EXPANSION MODE TIMINGS									
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	35	—	40	—	50	ns	13
t_{XOH}	Read/Write to $\overline{XO}$ High	—	35	—	40	—	50	ns	13
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns	14
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns	14
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS									
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	12	—	12	—	15	—	ns	19
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns	19
t_{S3}	SIX Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	7	—	7	—	7	—	ns	19
t_{SICW}	Serial In Clock Width High/Low	8	—	8	—	10	—	ns	19
t_{S5}	SI/PI Set-up Time to SICP Rising Edge	35	—	40	—	50	—	ns	19
SERIAL-OUTPUT MODE TIMINGS									
t_{S6}	SO/PO Set-up Time to SOCP Rising Edge	35	—	40	—	50	—	ns	20
t_{S7}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	7	—	7	—	7	—	ns	20
t_{SOCW}	Serial Out Clock Width High/Low	8	—	8	—	10	—	ns	20
SERIAL MODE RECOVERY TIMINGS									
t_{REFSO}	Recovery Time SOCP after $\overline{EF}$ Goes High	35	—	40	—	80	—	ns	22
t_{RFFSI}	Recovery Time SICP after $\overline{FF}$ Goes High	15	—	15	—	15	—	ns	23
SERIAL MODE FLAG TIMINGS									
t_{SOCEF}	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ Low	—	20	—	25	—	25	ns	22
t_{SOCFF}	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ High	—	30	—	35	—	40	ns	24
t_{SOCF}	SOCP Rising Edge to $\overline{FF}$-1, $\overline{HF}$, $\overline{AEF}$ High	—	30	—	35	—	40	ns	24,26
t_{SOCF}	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF}$+1 Low	—	30	—	35	—	40	ns	22,26
t_{SICEF}	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ High	—	45	—	50	—	65	ns	21
t_{SICFF}	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ Low	—	30	—	35	—	40	ns	23
t_{SICF}	SICP Rising Edge to $\overline{EF}$+1, $\overline{AEF}$ High	—	45	—	50	—	65	ns	21,25
t_{SICF}	SICP Rising Edge to $\overline{FF}$-1, $\overline{HF}$, $\overline{AEF}$ High	—	45	—	50	—	65	ns	23,25
SERIAL-INPUT MODE TIMINGS									
t_{PD1}	SICP Rising Edge to D[1]	5	17	5	17	5	20	ns	17,19
SERIAL-OUTPUT MODE TIMINGS									
t_{PD2}	SOCP Rising Edge to Q[1]	5	17	5	17	5	20	ns	20
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	16	5	16	ns	20
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	5	22	ns	20
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns	20
OUTPUT ENABLE/DISABLE TIMINGS									
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	16	—	16	—	16	ns	12
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns	12
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns	12

NOTE:
1. Values guaranteed by design, not tested.

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AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial and Military IDT72103x65 IDT72104x65 Min.	Max.	IDT72103x80 IDT72104x80 Min.	Max.	IDT72103x120 IDT72104x120 Min.	Max.	Unit	Timing Figure
DEPTH EXPANSION MODE TIMINGS									
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns	13
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns	13
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns	14
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns	14
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS									
tS2	Serial Data In Set-up Time to SICP Rising Edge	15	—	20	—	20	—	ns	19
tH2	Serial Data In Hold Time to SICP Rising Edge	0	—	5	—	5	—	ns	19
tS3	SIX Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
tS4	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
tH4	$\overline{W}$ Hold Time to SICP Rising Edge	10	—	12	—	15	—	ns	19
tSICW	Serial In Clock Width High/Low	10	—	15	—	15	—	ns	19
tS5	SI/PI Set-up Time to SICP Rising Edge	65	—	80	—	120	—	ns	19
SERIAL-OUTPUT MODE TIMINGS									
tS6	SO/PO Set-up Time to SOCP Rising Edge	65	—	80	—	120	—	ns	20
tS7	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
tS8	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
tH8	$\overline{R}$ Hold Time to SOCP Rising Edge	10	—	12	—	15	—	ns	20
tSOCW	Serial Out Clock Width High/Low	10	—	15	—	15	—	ns	20
SERIAL MODE RECOVERY TIMINGS									
tREFSO	Recovery Time SOCP after $\overline{EF}$ Goes High	65	—	80	—	120	—	ns	22
tRFFSI	Recovery Time SICP after $\overline{FF}$ Goes High	15	—	20	—	20	—	ns	23
SERIAL MODE FLAG TIMINGS									
tSOCEF	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ Low	—	30	—	30	—	30	ns	22
tSOCFF	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ High	—	50	—	60	—	60	ns	24
tSOCF	SOCP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ High	—	50	—	60	—	60	ns	24,26
tSOCF	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$ Low	—	50	—	60	—	60	ns	22,26
tSICEF	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ High	—	80	—	80	—	80	ns	21
tSICFF	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ Low	—	50	—	60	—	60	ns	23
tSICF	SICP Rising Edge to $\overline{EF+1}$, $\overline{AEF}$ High	—	80	—	80	—	80	ns	21,25
tSICF	SICP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ High	—	80	—	80	—	80	ns	23,25
SERIAL-INPUT MODE TIMINGS									
tPD1	SICP Rising Edge to D[1]	5	25	5	30	5	35	ns	17,19
SERIAL-OUTPUT MODE TIMINGS									
tPD2	SOCP Rising Edge to Q[1]	5	25	5	30	5	35	ns	20
tSOHZ	SOCP Rising Edge to SO at High-Z[1]	5	20	5	25	5	30	ns	20
tSOLZ	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	30	5	35	ns	20
tSOPD	SOCP Rising Edge to Valid Data on SO	—	22	5	30	5	35	ns	20
OUTPUT ENABLE/DISABLE TIMINGS									
tOEHZ	Output Enable to High-Z (Disable)[1]	—	20	—	25	—	30	ns	12
tOELZ	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns	12
tAOE	Output Enable to Data Valid (Q_{0-8})	—	25	—	30	—	35	ns	12

NOTE:
1. Values guaranteed by design, not tested.

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GENERAL SIGNAL DESCRIPTION

INPUTS:

Data Inputs (D_0-D_8)

The parallel-in mode is selected by connecting the $\overline{SI}$/PI pin to V_{CC}. D_0-D_8 are the data input lines.

The serial-input mode is selected by grounding the $\overline{SI}$/PI pin. The D_0-D_8 lines are control output pins used to program the serial word width.

Reset ($\overline{RS}$)

Reset is accomplished whenever the $\overline{RS}$ input is taken to a low state. Both internal read and write pointers are set to the first location during reset. A reset is required after power up before a write operation can take place. Both Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be high during reset.

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of $\overline{W}$ provided the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold times must be met with respect to the rising edge of $\overline{W}$. Data is stored in the RAM array sequentially and independently of any on going read operation.

When the FIFO is full, the $\overline{FF}$ will go low inhibiting further write operations to prevent data overflow. After a valid read operation is completed, the $\overline{FF}$ will go high after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of $\overline{R}$, provided the $\overline{EF}$ is not set. Data is accessed on a first-in/first out basis independent of any on going write operations. After $\overline{R}$ goes high, the Data Outputs (Q_0-Q_8) go to a high impedance condition until the next read operation. When all the data has been read from the FIFO, the $\overline{EF}$ will go low, and Q_0-Q_8 will go to a high impedance state inhibiting further read operations. After the completion of a valid write operation, the $\overline{EF}$ will go high after t_{WEF} allowing a valid read to begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

In the depth-expansion mode, the $\overline{FL}/\overline{RT}$ pin is grounded to indicate that it is the first device loaded. In the single-device mode, the $\overline{FL}/\overline{RT}$ pin acts as the retransmit input. The single-device mode is initiated by grounding the Expansion-In ($\overline{XI}$) pin.

The IDT72103/72104 can be made to retransmit data when the $\overline{RT}$ input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. During retransmit, $\overline{R}$ and $\overline{W}$ must be set high and the $\overline{FF}$ will be affected depending on the relative locations of the read and write pointers. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not available in the depth expansion mode.

Expansion In ($\overline{XI}$)

The $\overline{XI}$ pin is grounded to indicate an operation in the the single-device mode. In the depth expansion or daisy-chain mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device.

Output Enable ($\overline{OE}$)

When $\overline{OE}$ is high, the parallel output buffers are tristated. When $\overline{OE}$ is low, both parallel and serial outputs are enabled.

Serial Input (SI)

Serial data is read into the serial input register via the SI pin. In both depth and serial width expansion modes, the serial-input signals of the different FIFOs in the expansion array are connected together.

Serial Input Clock (SICP)

Serial data is read into the serial input register on the rising edge of the SICP signal. In both depth and serial width expansion modes, the SICP signals of the different FIFOs in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of the SOCP signal. In both depth and serial width expansion modes, the SOCP signals of the different FIFOs in the expansion array are connected together.

Serial Input Expansion (SIX)

The SIX pin is tied high for single-device serial or parallel input operation. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device.

Serial Output Expansion (SOX)

The SOX pin is tied high for single-device serial or parallel output operation. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device.

Serial/Parallel Input ($\overline{SI}$/PI)

The $\overline{SI}$/PI pin programs whether the IDT72103/72104 accepts parallel or serial data as input. When this pin is low, the FIFO expects serial data and the D_0-D_8 pins become output pins used to program the write signal and the serial input word width. For instance, connecting D_8 to $\overline{W}$ will program a serial word width of 7 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The $\overline{SO}$/PO pin programs whether the IDT72103/72104 outputs parallel or serial data. When this pin is low, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to program the read signal and the serial output word width.

OUTPUTS:

Data Outputs (Q_0-Q_8)

Data outputs for 9-bit wide data. These output lines are in a high impedance condition whenever $\overline{R}$ is in a high state. The serial output mode is selected by grounding the $\overline{SO}$/PO pin. The Q_0-Q_8 lines are control pins used to program the serial word width.

Serial Output ($\overline{SO}$)

Serial data is output on the SO pin. In both depth and serial width expansion modes the serial output signals of the different FIFOs in the expansion array are connected together. Following reset, SO is tristated until the first rising edge of the Serial Out Clock (SOCP) signal. Data is clocked out least significant bit first. In the serial width expansion mode, SO is tristated again after the ninth bit is output.

Full Flag ($\overline{FF}$)

$\overline{FF}$ is asserted low when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by any additional write pulses.

Full Flag - Serial In Mode

When the FIFO is loaded serially, the Serial In Clock (SICP) asserts the $\overline{FF}$. On the second rising edge of the SICP for the last word in the FIFO, the $\overline{FF}$ will assert low, and it will remain asserted until the next read operation. Note that when the FF is asserted, the last SICP for that word will have to be stretched as shown in Figure 23.

Full Flag - Parallel-In Mode

When the FIFO is in the Parallel-In mode, the falling edge of $\overline{W}$ asserts the $\overline{FF}$ (low). The $\overline{FF}$ is then de-asserted (high) by subsequent read operations - either serial or parallel.

Full-Minus-One Flag ($\overline{FF-1}$)

The $\overline{FF-1}$ flag is asserted low when the FIFO is one word away from being full. It will remain asserted when the FIFO is full.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

In the single-device mode, the XO/$\overline{HF}$ pin operates as a $\overline{HF}$ pin when the $\overline{XI}$ pin is grounded. After half of the memory is filled, the $\overline{HF}$ will be set to low at the falling edge of the next write operation. It will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the FIFO total memory. The $\overline{HF}$ is then reset by the rising edge of the read operation.

In the multiple-device mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device. The $\overline{XO}$ pin signals a pulse to the next device when the previous device reaches the best location of memory in the daisy chain configuration.

Almost-Empty or Almost-Full Flag ($\overline{AEF}$)

The $\overline{AEF}$ asserts low if there are 0-255 or 1793-2048 bytes in the IDT72103, 2K x 9 FIFO. The $\overline{AEF}$ asserts low if there are 0-511 or 3585-4096 bytes in the IDT72104, 4K x 9 FIFO.

Empty-Plus-One Flag ($\overline{EF+1}$)

In the parallel-output mode, the $\overline{EF+1}$ flag is asserted low when there is one word or less in the FIFO. It will remain low when the FIFO is empty.

In the serial-output mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ flag. It goes low when the second to the last word is read from the RAM array and is ready to be shifted out.

Empty Flag ($\overline{EF}$) - Parallel-Out Mode

When the FIFO is in the parallel out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line will cause the $\overline{EF}$ line to be asserted low. This is shown in Figure 6. The $\overline{EF}$ is then de-asserted high by either the rising edge of $\overline{W}$ or the rising edge of SICP, as shown in Figure 6.

Empty Flag - Serial-Out Mode

The use of the EF is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted low after the first bit of the last word is shifted out. This is shown in Figure 22.

5

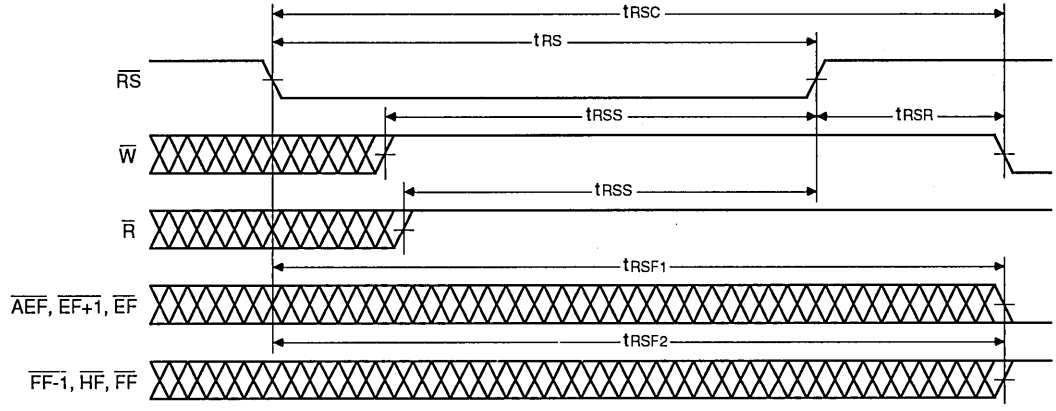
TABLE 1 — STATUS FLAGS

Number of Words in FIFO IDT72103	Number of Words in FIFO IDT72104	$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	(1) $\overline{EF+1}$	$\overline{EF}$
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1024	512-2048	H	H	H	H	H	H
1025-1792	2049-3584	H	H	H	L	H	H
1793-2046	3585-4094	H	H	L	L	H	H
2047	4095	H	L	L	L	H	H
2048	4096	L	L	L	L	H	H

NOTE:
1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

2753 tbl 12

PARALLEL TIMINGS:



NOTE:
1. All flags may change status during Reset, but flags will be valid at tRSC.

Figure 2. Reset

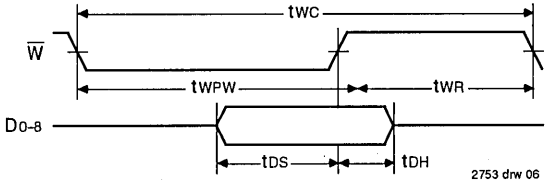


Figure 3. Write Operation in Parallel Data In Mode

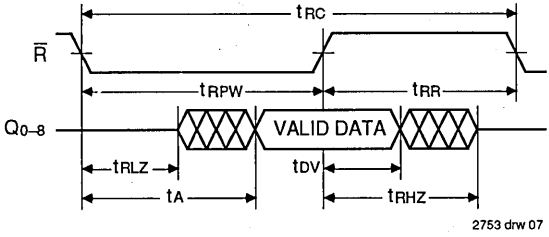
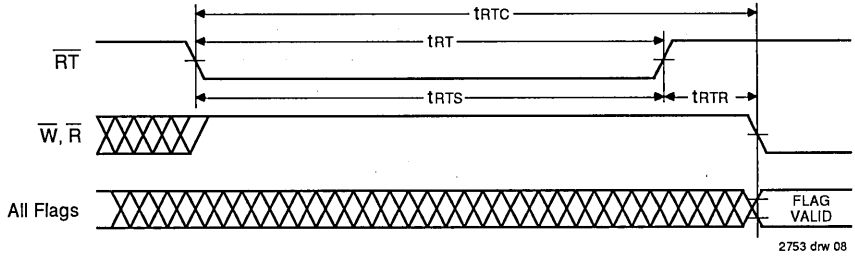
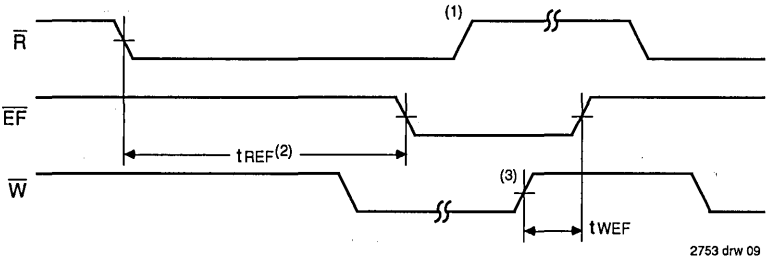


Figure 4. Read Operation in Parallel Data Out Mode



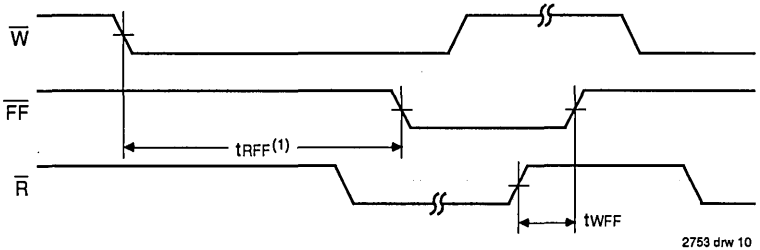
NOTE:
1. All flags may change status during Retransmit, but flags will be valid at tRTC.

Figure 5. Retransmit



NOTES:
1. Data is valid on this edge.
2. The Empty Flag is asserted by R in the Parallel-Out mode and is specified by tREF. The EF flag is deasserted by the rising edge of W.
3. First rising edge of Write after EF is set.

Figure 6. Empty Flag Timings in Parallel Out Mode



NOTE:
1. For the assertion time, tWFF is used when data is written in the Parallel mode. The FF is de-asserted by the rising edge of R.

Figure 7. Full Flag Timings in Parallel-In Mode

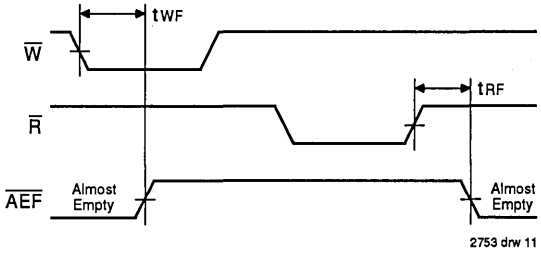


Figure 8. Almost-Empty Flag Region

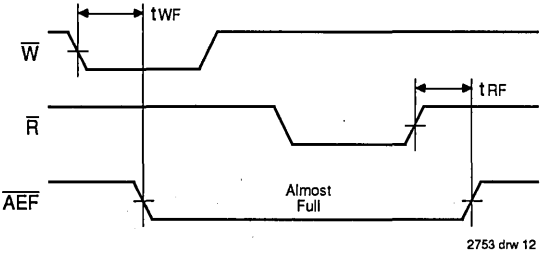


Figure 9. Almost-Full Flag Region

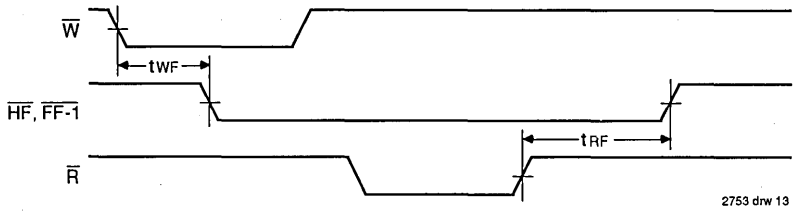


Figure 10. Half-Full and Full-minus-1 Flag Timings

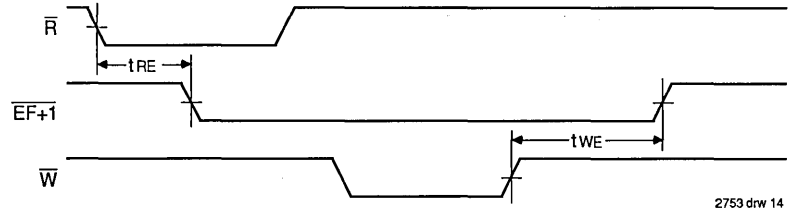


Figure 11. Empty+1 Flag Timings

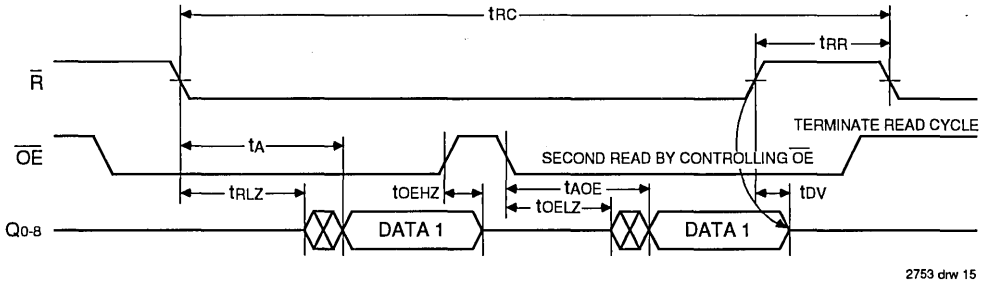


Figure 12. Output Enable Timings

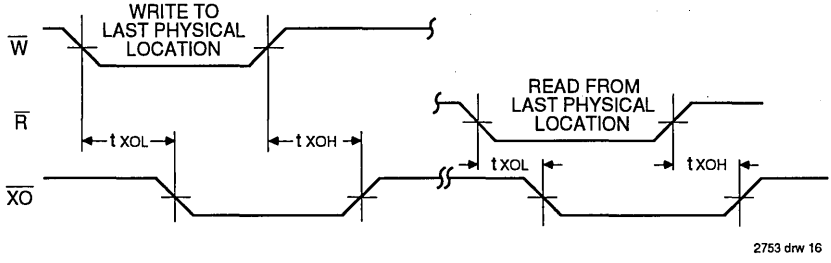


Figure 13. Expansion-Out

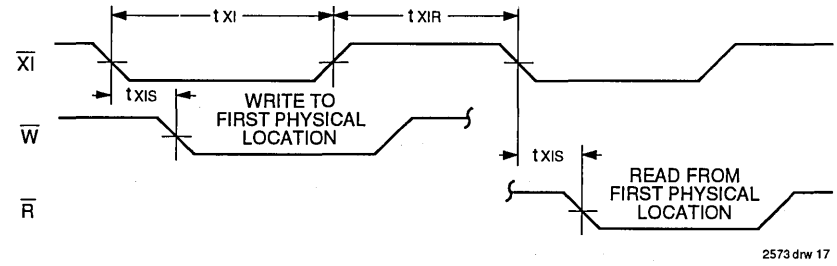


Figure 14. Expansion-In

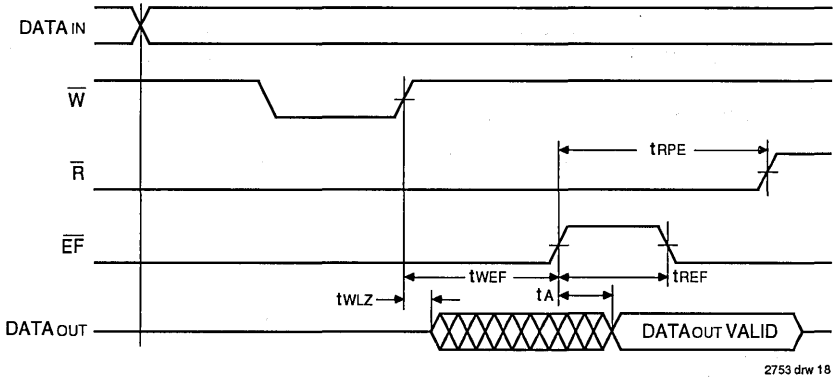


Figure 15. Read Data Flow-Through Mode

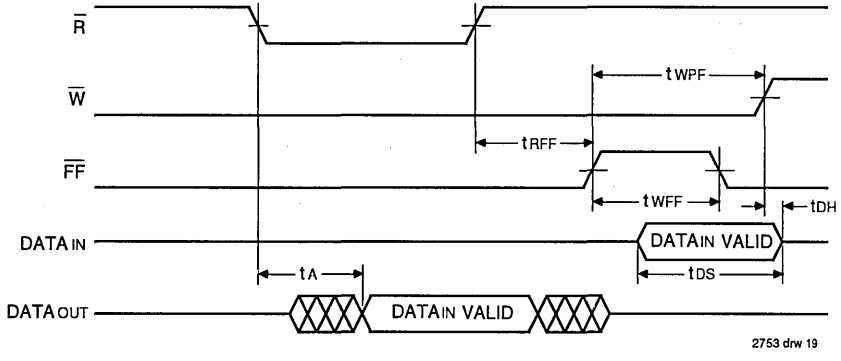
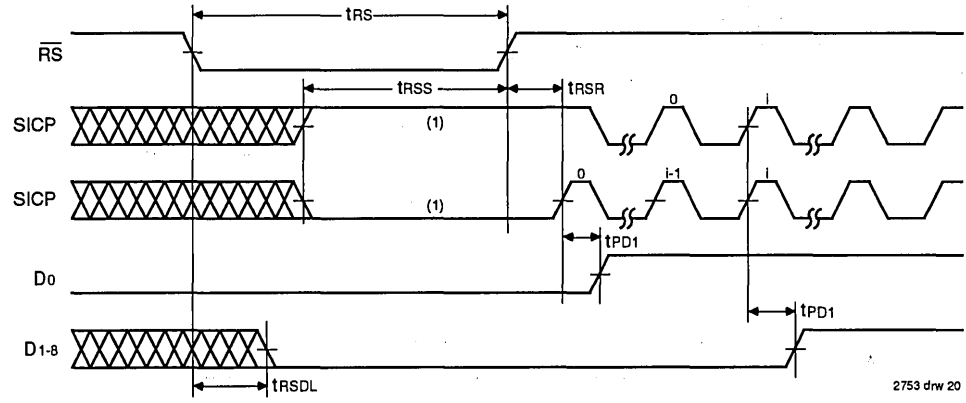


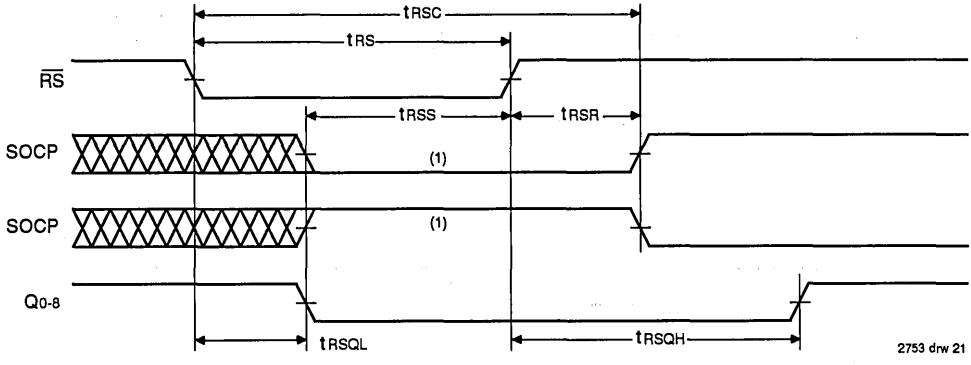
Figure 16. Write Data Flow-Through Mode

SERIAL TIMINGS:



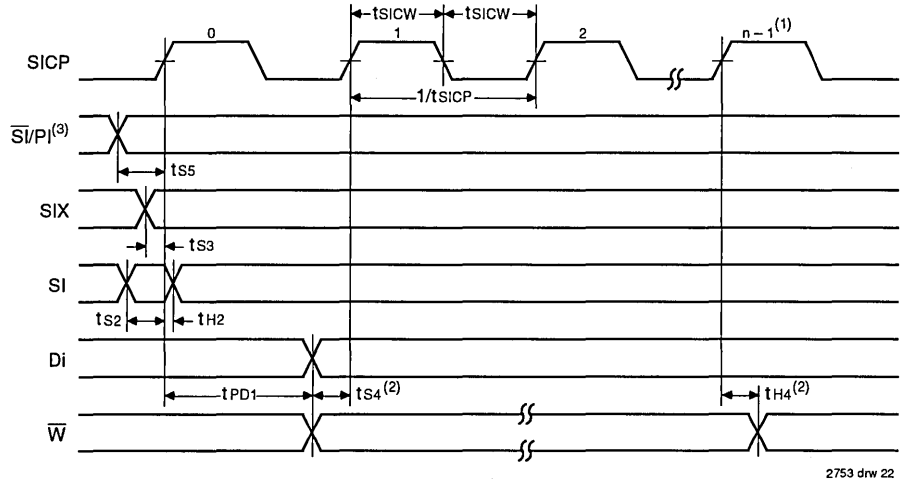
NOTE:
1. SICP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

Figure 17. Reset Timings for Serial-In Mode



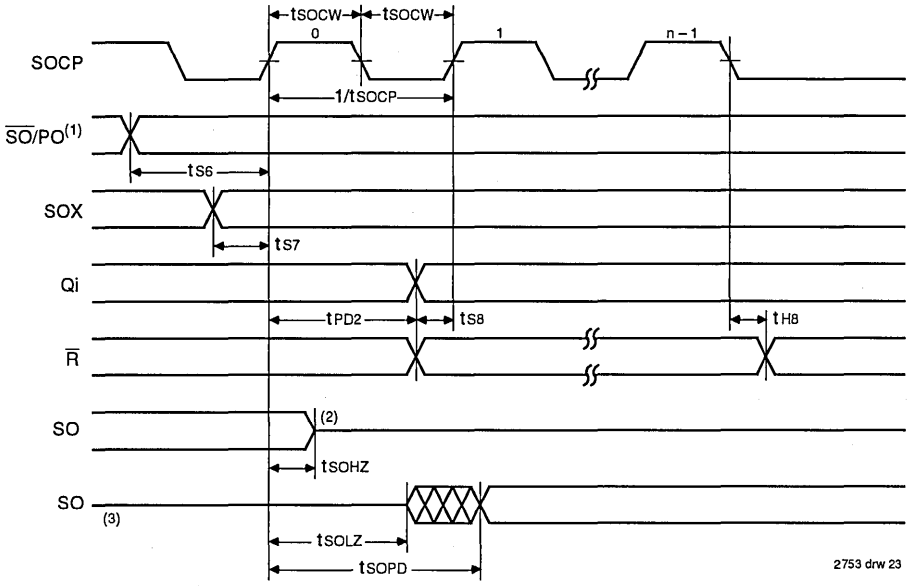
NOTE:
1. SOCP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

Figure 18. Reset Timings for Serial-Out Mode



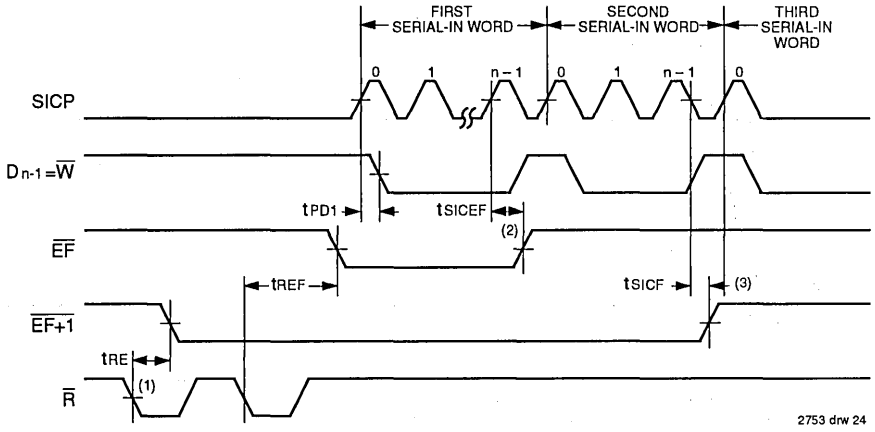
NOTES:
1. For the stand alone mode, N ≥ 4 and the input bits are numbered 0 to N-1.
2. For the recommended interconnections, Di is to be directly tied to $\overline{W}$ and the t_{S4} and t_{H4} requirements will be satisfied. For users that modify $\overline{W}$ externally, t_{S4} and t_{H4} requirements have to be met.
3. After $\overline{SI}$/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

Figure 19. Write Operation In Serial-In Mode



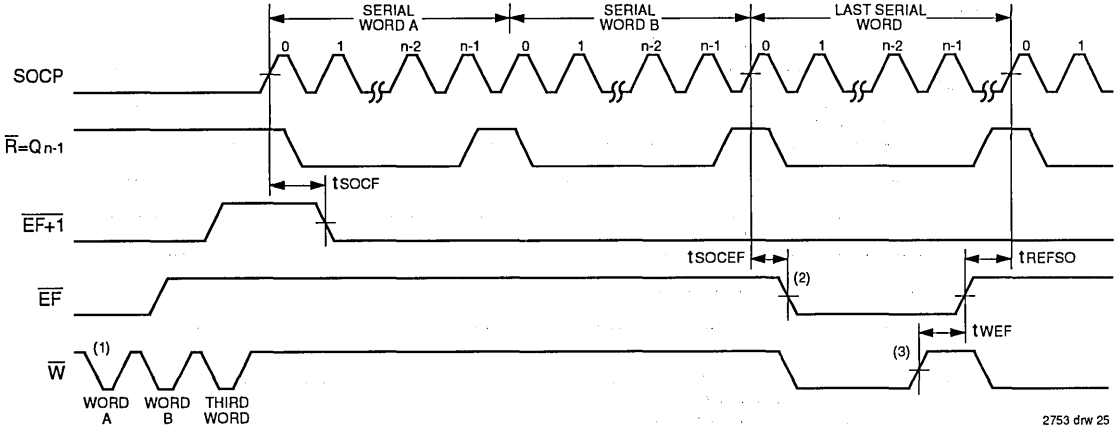
NOTES:
1. After $\overline{SO}$/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.
2. For single device: Read out the last bit before $\overline{EF}$ is asserted.
   For Serial Width Expansion mode: Read out the last bit of the current memory location from the active device.
3. For single device: The operation starts after Reset.
   For Serial Width Expansion mode: Read the first bit of the current memory location from the active device.

Figure 20. Read Operation In Serial-Out Mode



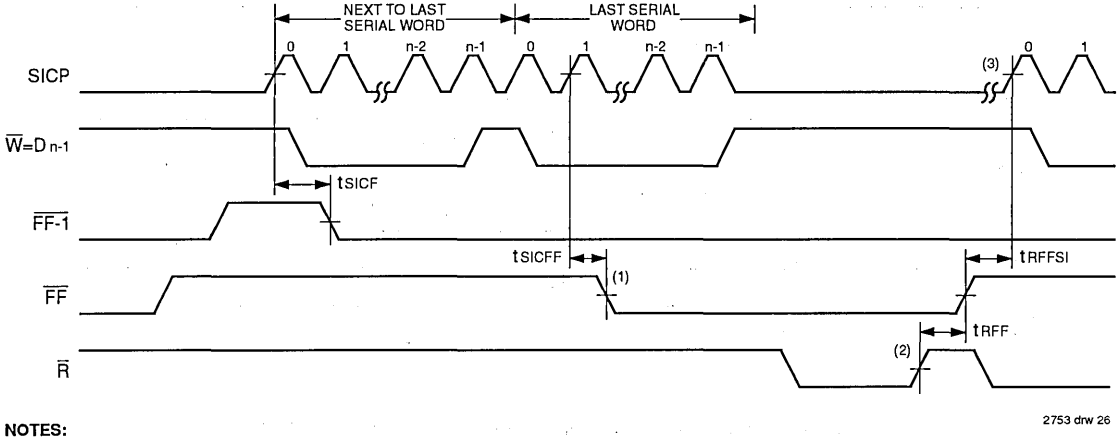
NOTES:
1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is de-asserted after the N–1 rising edge of SICP of the first serial-in word. In the Serial-Out mode, a new read operation can begin t_{REFSO} after $\overline{EF}$ goes HIGH. In the Parallel-Out mode, a new read operation can occur immedately after $\overline{FF}$ goes HIGH.
3. The $\overline{EF+1}$ Flag is de-asserted after the N–1 rising edge of SICP of the second serial-in word.

Figure 21. Empty Flag and Empty+1 Flag De-assertion in the Serial-In Mode



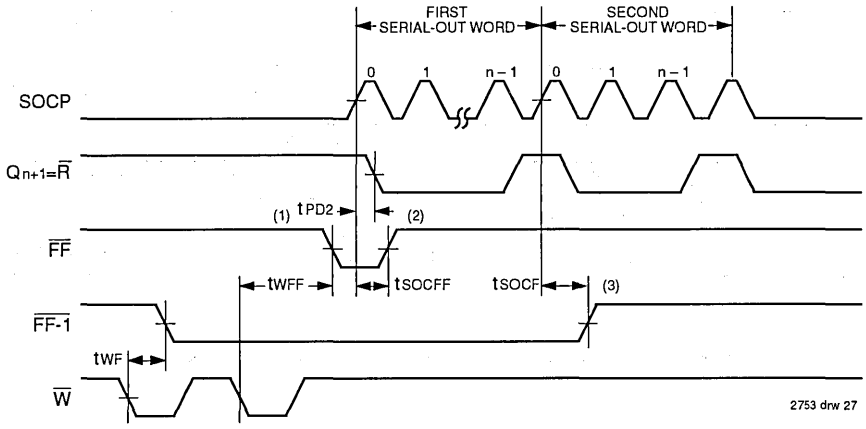
NOTES:
1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag ($\overline{EF}$) is asserted in Serial-Out mode by using the t_{SOCEF} parameter. This parameter is measured in the worst case condition from the rising edge of the SOCP used to clock data bit 0. Whenever $\overline{EF}$ goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the $\overline{EF}$ flag is de-asserted by the rising edge of $\overline{W}$. In the Serial-In mode, the $\overline{EF}$ flag is de-asserted by the rising edge of $\overline{W}$.
3. First Write rising edge after $\overline{EF}$ is set.
4. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 22. Empty Flag and Empty+1 Flag Assertion in the Serial-Out Mode (FIFO Being Emptied)



NOTES:
1. The Full Flag is asserted in the Serial-In mode by using the tSICFF parameter. This parameter is measured in the worst case condition from the rising edge of SICP followed by a (tPD1+tWFF) delay from the first rising edge of SICP of the last word.
2. First Read rising edge after FF is set.
3. SICP should not be clocked until FF goes HIGH.

Figure 23. Full Flag and Full-1 Flag Assertion in the Serial-In Mode (FIFO Being Filled)



NOTES:
1. The FIFO is full and a new read sequence is started.
2. On the first rising edge of SOCP, the FF is de-asserted. In the Serial-In mode, a new write operation can begin following tRFFS1 after FF, goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after FF goes HIGH.
3. The FF-1 flag is de-asserted after the first SOCP of the second serial word.

Figure 24. Full Flag and Full-1 Flag De-assertion in the Serial-Out Mode

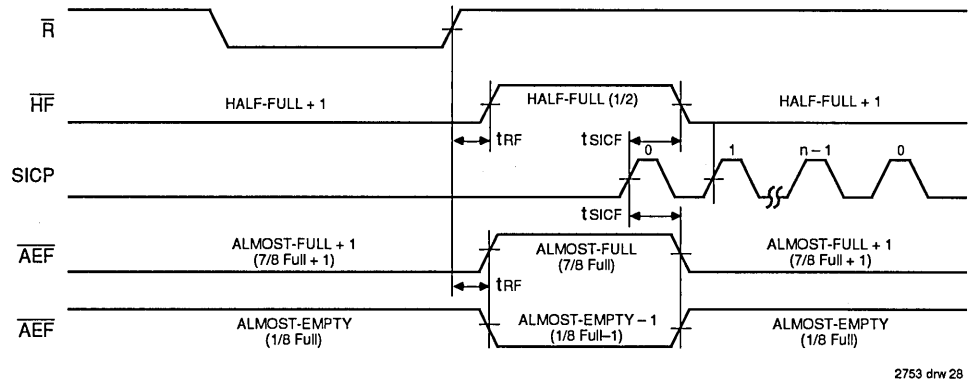


Figure 25. Half-Full, Almost-Full and Almost-Empty Timings for Serial-In Mode

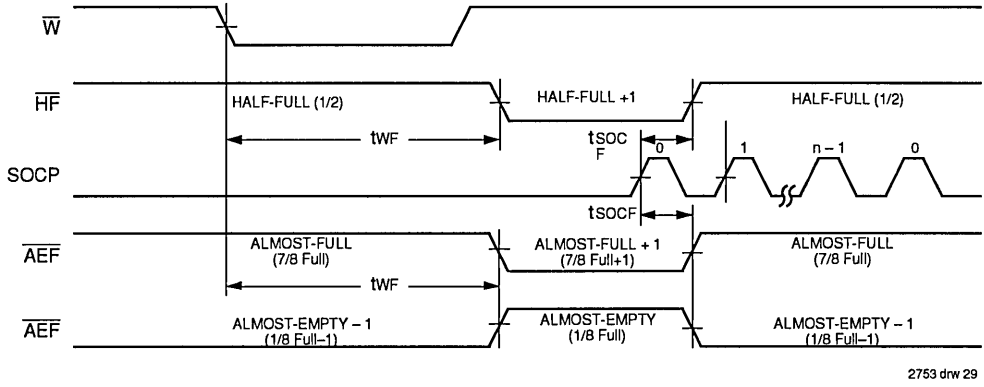


Figure 26. Half-Full, Almost-Full and Almost-Empty Timings for Serial-Out Mode

OPERATING DESCRIPTION

PARALLEL OPERATING MODES:

Parallel Data Input

By setting $\overline{SI}$/PI high, data is written into the FIFO in parallel through the D_0-D_8 input data lines.

Parallel Data Output

By setting $\overline{SO}$/PO high, the parallel-out mode is chosen. In the parallel-out mode, as shown in Figure 4, data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes high.

Alternately, the user can access the FIFO by keeping $\overline{R}$ low and enabling data on the bus by asserting $\overline{OE}$. When $\overline{R}$ is low, the $\overline{OE}$ is high and the output bus is tri-stated. When $\overline{R}$ is high, the output bus is disabled irrespective of $\overline{OE}$. The enable and disable timings for $\overline{OE}$ are shown in Figure 12.

Single Device Mode

A single ID172103/72104 may be used when application requirements are for 2048/4096 words or less. The IDT72103/72104 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (See Figure 27). In this mode, the $\overline{HF}$/$\overline{XO}$ is used as an Half-Full flag.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one of the connected devices. Figure 28 demonstrates an 18-bit word width by using two IDT72103/72104s. Any word width can be attained by adding additional IDT72103/72104.

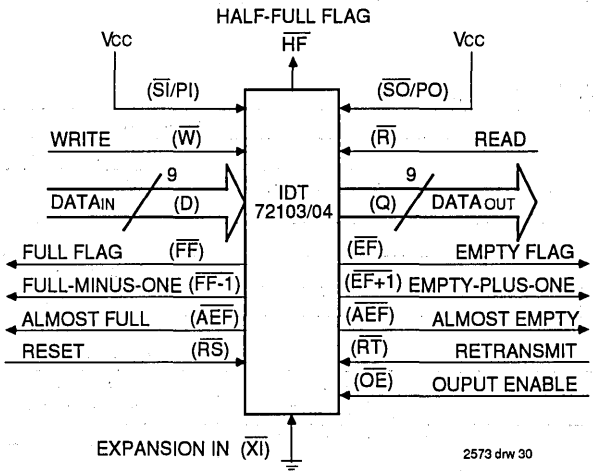


Figure 27. Block Diagram of Single 2048 x 9/4096 x 9 FIFO in Parallel Mode

5

INPUT CONFIGURATION TABLE

Pin	Parallel Input	Serial Input			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SI}$/PI	HIGH	LOW	LOW	LOW	LOW
SI	HIGH	Input Data	Input Data	Input Data	Input Data
SICP	HIGH	Input Clock	Input Clock	Input Clock	Input Clock
SIX	HIGH	HIGH	HIGH	D_8 of next least significant device	D_8 of next least significant device
$\overline{W}$	Write Control	Di	Di of most significant device	Di of most significant device	Di of most significant device
D_0-D_8	Input Data	No connect except Di	No connect except D_8	No connect except D_8	No connect except Di
Di[1]	—	$\overline{W}$	—	—	$\overline{W}$ of all devices
D_8	—	—	SIX of next most significant device	SIX of next most significant device	—

2753 tbl 13

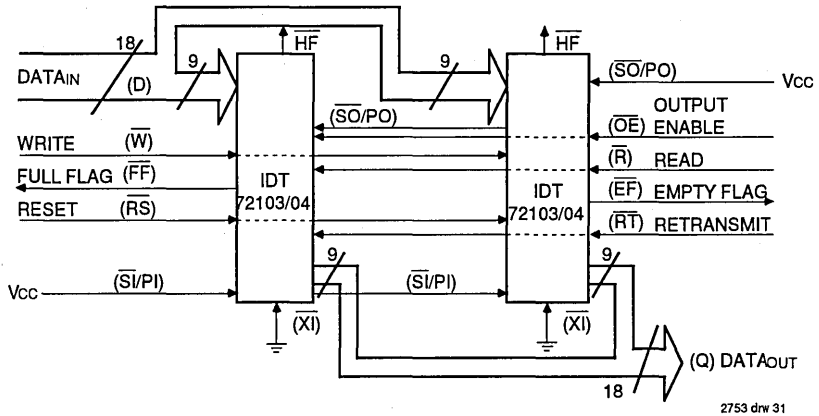
NOTE:
1. Di refers to the most significant bit of the serial word. If multiple devices are width cascaded, Di is the most significant bit from the most significant device.

OUTPUT CONFIGURATION TABLE

Pin	Parallel Output	Serial Output			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SO}$/PO	HIGH	LOW	LOW	LOW	LOW
SO	—	Output Data	Output Data	Output Data	Output Data
SOCP	HIGH	Output Clock	Output Clock	Output Clock	Output Clock
SOX	HIGH	HIGH	HIGH	Q_8 of next least significant device	Q_8 of next least significant device
$\overline{R}$	Read Control	Qi	Qi of most significant device	Qi of most significant device	Qi of most significant device
Q_0-Q_8	Output Data	No connect except Di	No connect except Q_8	No connect except Q_8	No connect except Qi
Qi[1]	—	$\overline{R}$	—	—	$\overline{R}$ of all devices
Q_8	—	—	SOX of next most significant device	SOX of next most significant device	—

2753 tbl 14

NOTE:
1. Qi refers to the most significant bit of the serial word. If multiple devices are width cascaded, Qi is the most significant bit from the most significant device.



NOTE:
1. Flag detection is accomplished by monitoring all the flag signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

Figure 28. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion in Parallel Mode

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION IN PARALLEL MODE

Mode	Inputs[2]			Internal Status[1]		Outputs		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTES:
1. Pointer will increment if appropriate flag is HIGH.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

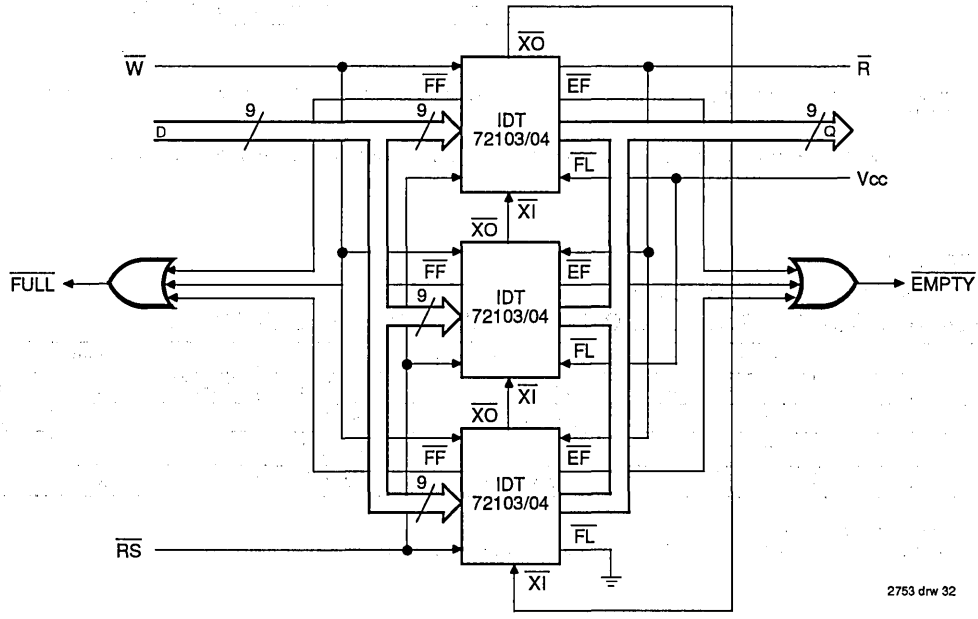
2753 tbl 15

5

Depth Expansion (Daisy Chain) Mode

The IDT72103/4 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 29 demonstrates Depth Expansion using three IDT72103/4s. Any memory depth can be attained by adding additional IDT72103/4s. The IDT72103/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input pin.
2. All other devices must have the $\overline{FL}$ pin in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 29.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 29.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

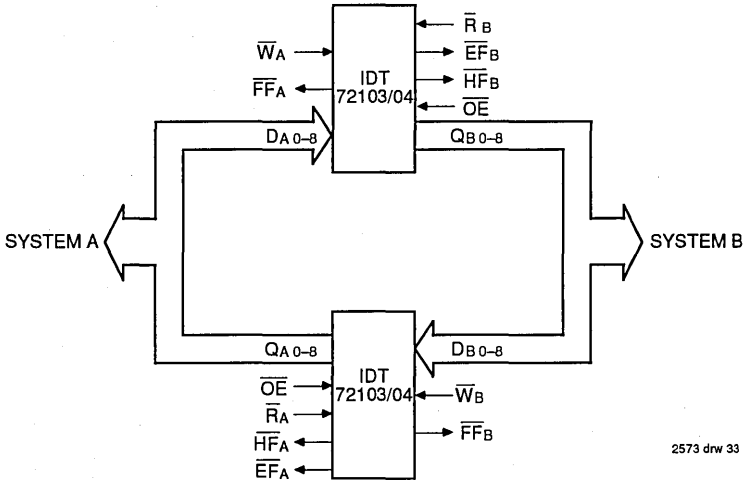


NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.

Figure 29. Block Diagram of 6,144 x 9/12,288 x 9-FIFO Memory, Depth Expansion In Parallel Mode

Bidirectional Mode

Applications requiring data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/4 as shown in Figure 30. Both Depth Expansion and Width Expansion may be used in this mode.



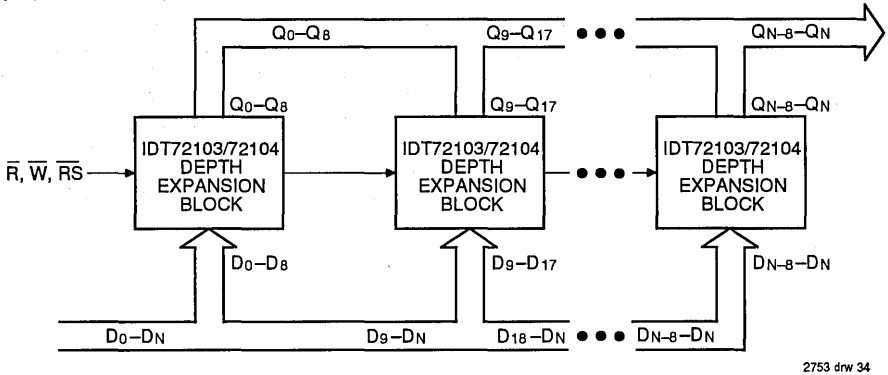
NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.

Figure 30. Bidirectional FIFO Mode

5

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 31).



NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.
2. For depth expansion block see DEPTH EXPANSION Section and Figure 29.
3. For Flag Detection see WIDTH EXPANSION SECTION and Figure 28.

Figure 31. Compound FIFO Expansion

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs[2]			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

2753 tbl 16

SERIAL OPERATING MODES:

Serial Data Input

The Serial Input mode is selected by grounding the $\overline{SI}$/PI line. The D_{0-8} lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which, are meant for connection to the $\overline{W}$ input. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits, connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D_8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D_8 of the next least significant device.

Figure 32 shows the relationship of the SIX, SICP and D_{0-8} lines. In the stand alone case (Figure 32), on the first LOW-to-HIGH of SICP, the D_{1-7} lines go LOW and the D0 line remains HIGH. On the next SICP clock edge, the D_1 goes HIGH, then D_2 and so on. This continues until the D line, which is connected to $\overline{W}$, goes HIGH. On the next clock cycle, after $\overline{W}$ is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D_0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D_8. When D_8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D_0 goes HIGH; then on the next cycle D_1 and so on. A D_i output from the most significant device is issued to create the $\overline{W}$ for all cascaded devices.

The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q_0. The second bit shifted in is on Q_1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D_{0-8} lines to determine whether to store it or not.

The example shown in Figure 34 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

SINGLE DEVICE SERIAL INPUT CONFIGURATION

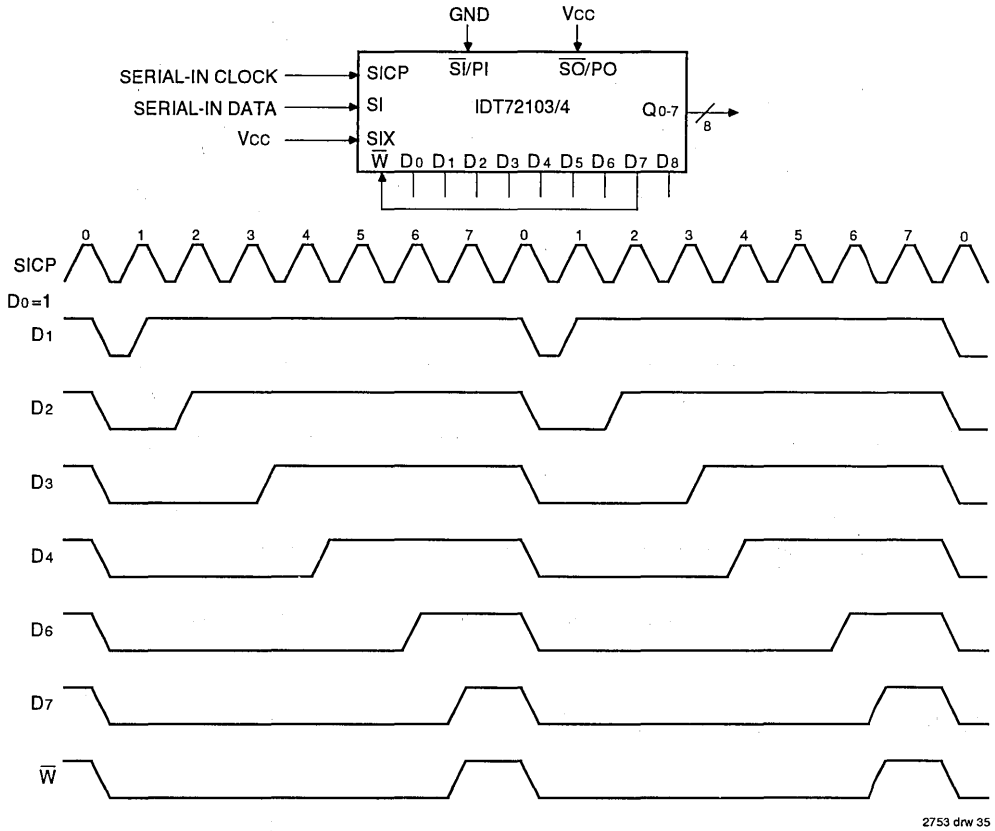


Figure 32. Serial-In Mode Where 8-Bit Parallel Output Data is Read

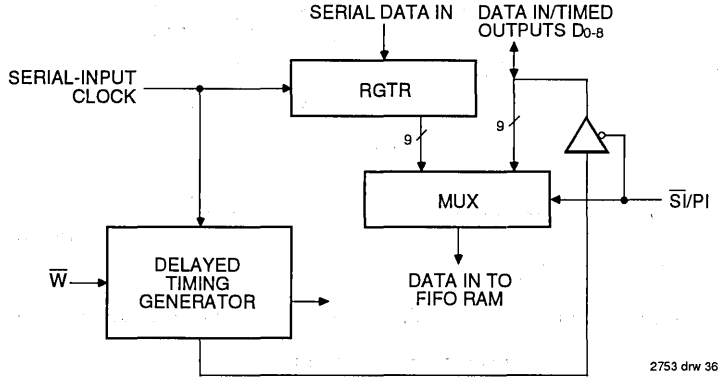


Figure 33. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

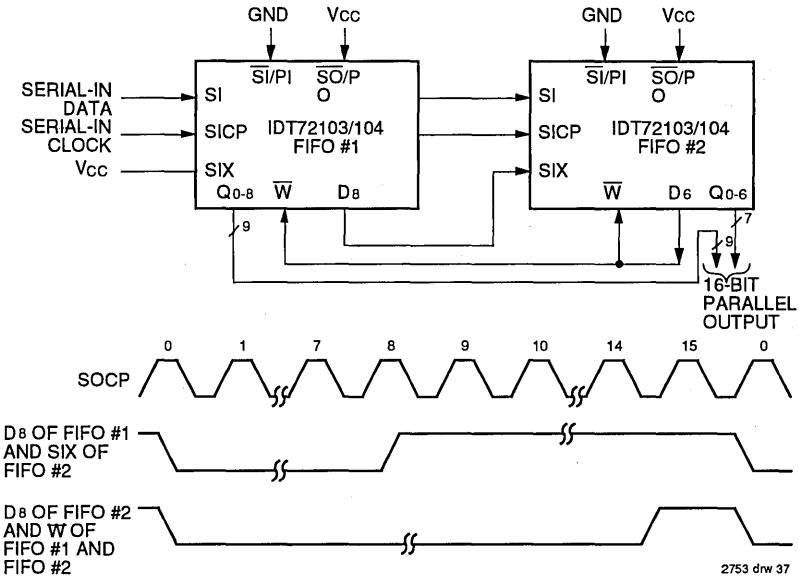
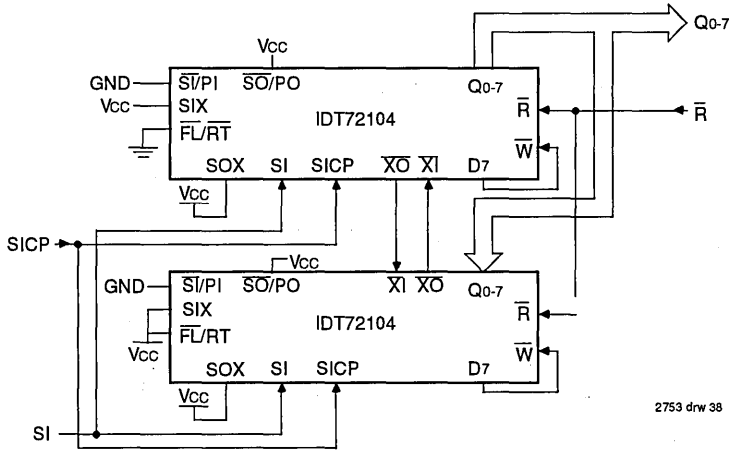


Figure 34. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

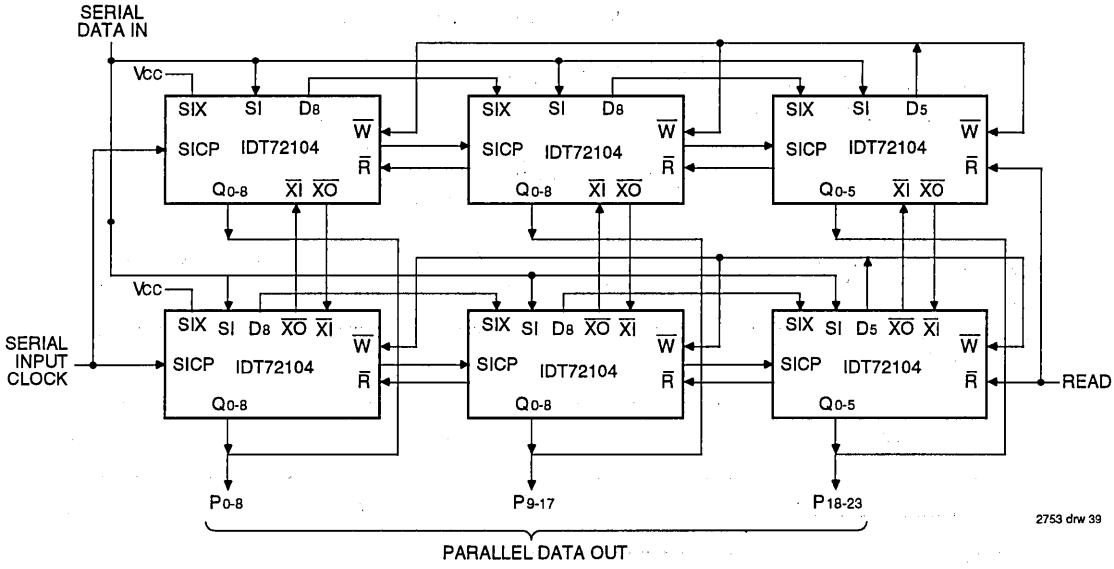
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND and SO/PO pins are tied to Vcc. OE is tied LOW. For FF and EF connections see Figure 29.

Figure 35. An 8K x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND. SO/PO pins are tied to Vcc. For FF and EF connections see Figure 29.

Figure 36. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

5

Serial Data Output

The Serial Output mode is selected by setting the SO/PO line low. When in the Serial-Out mode, one of the Q1-8 lines should be used to control the R signal. In the Serial-Out mode, the Q0-8 are taps off a digital delay line. By selecting one of these taps and connecting n to the input, the width of the serial word to be read and shifted is programmed. For instance, if the Q5 line is connected to the R input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit First. If the input mode of the FIFO is parallel, the information that was written into the D0 bit will come out as the first bit of the serial word. The second bit of the serial stream will be the D1 bit and so on.

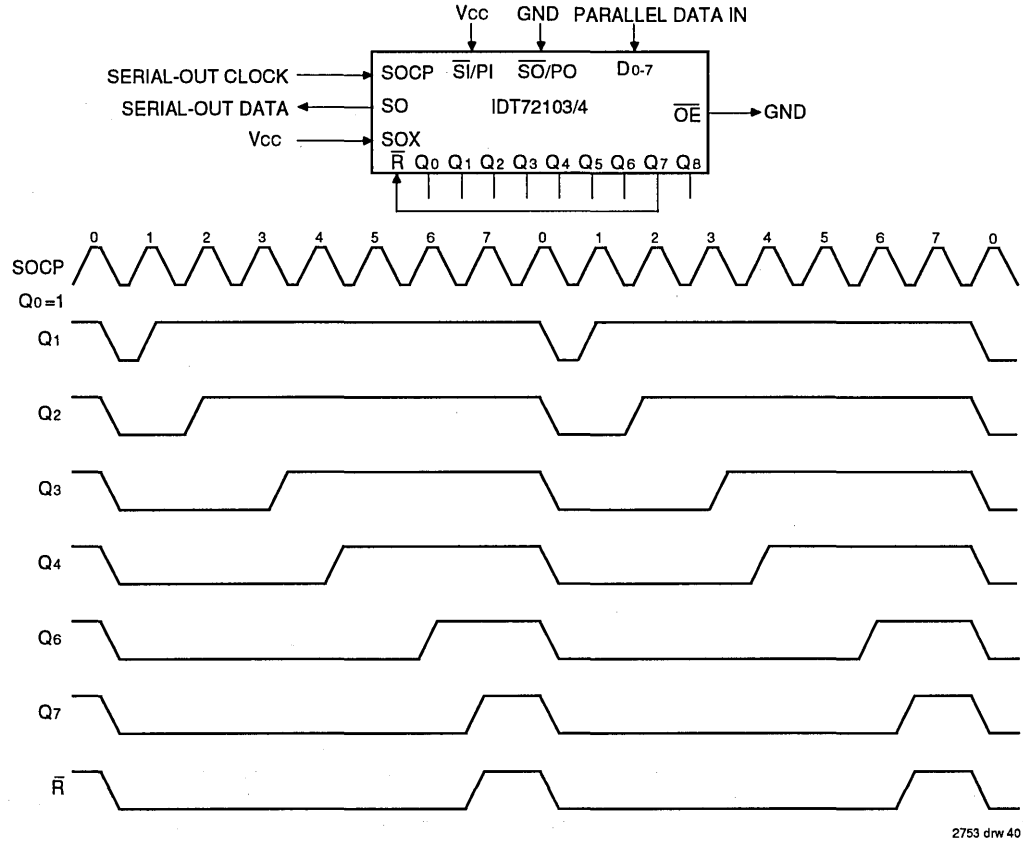
In the stand alone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q0 go LOW and a new serial word is started. On the next clock cycle, Q1 will go HIGH, Q2 on the next clock cycle and so on, as shown in Figure 37. This continues until the Q line, which is connected to R, goes HGIH at which point all of the Q lines go LOW on the next clock and a new word is started.

In the cascaded case, word width of more than 9 bits can be achieved by using more than one device. By tieing the SOX line of the least significant device HIGH and the SOX of the subsequent devices to Q8 of the previous devices, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the lines go low except for Q0. Just as in the stand alone case, on each consecutive clock cycle, each Q line goes HIGH in the order of least to most significant. When Q8 (which is connected to the SOX input of the next device) goes HIGH, the D0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all R inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is tri-stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 39 shows an example of the interconnections for a 16-bit serialized FIFO.

SINGLE DEVICE SERIAL OUTPUT CONFIGURATION



NOTE:
1. Input data is loaded in 8-bit quantities and read out serially.

Figure 37. Serial-Out Configuration

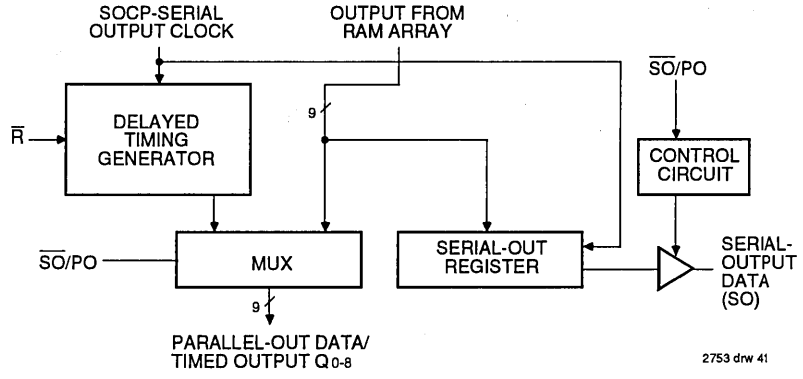
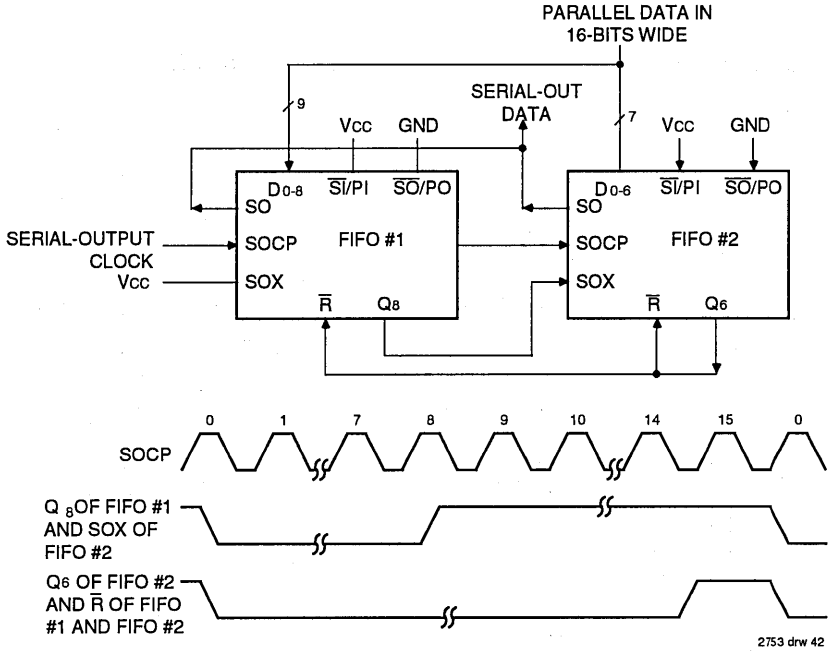


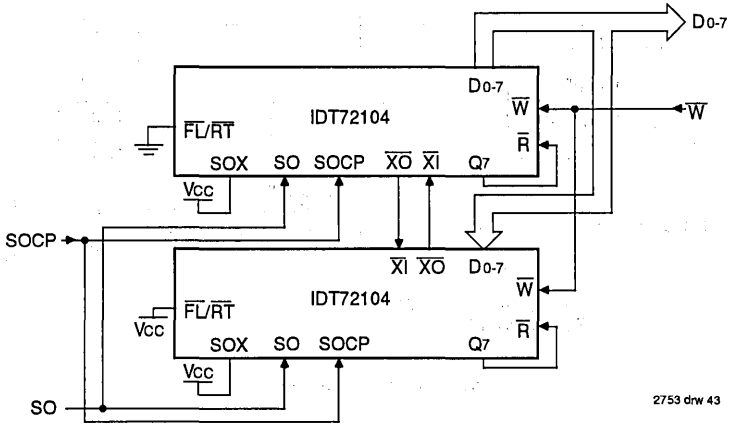
Figure 38. Serial-Output Circuitry



NOTE:
1. The parallel Data In is tied to D0-8 of FIFO #1 and D0-6 of FIFO #2.

Figure 39. Serial-Output for 16-Bit Parallel Data In

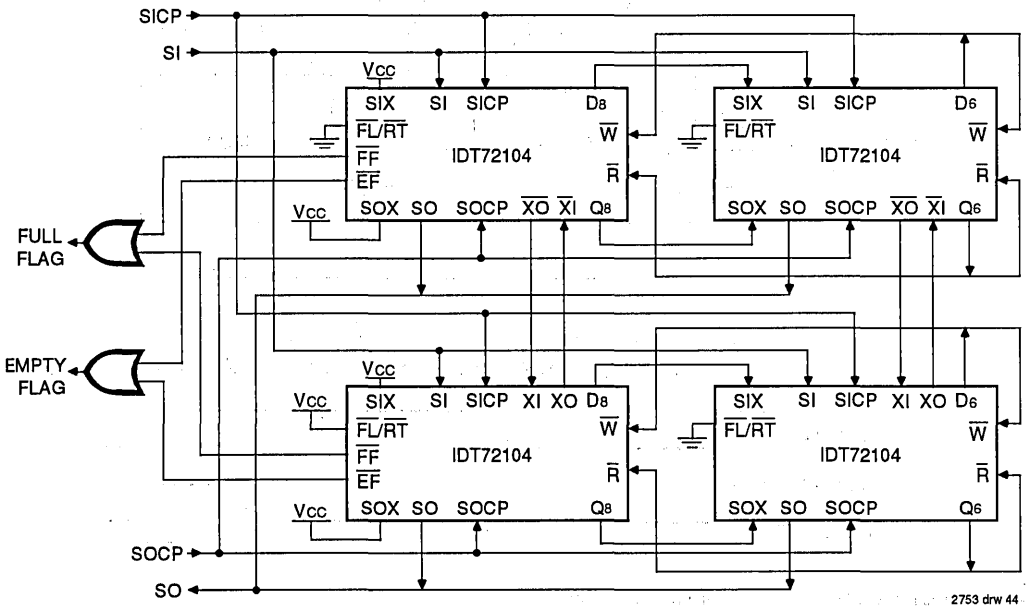
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to Vcc and SO/PO pins are tied to GND. OE is tied LOW. For FF and EF connections see Figure 17.

Figure 40. An 8K x 8 Parallel-In Serial-Out FIFO

SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All RS pins are connected together. All OE pins are connected LOW. All SI/PI and SO/PO pins are grounded.

Figure 41. 128K x 1 Serial-In Serial-Out FIFO

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 256 x 16, 512 x 16, 1024 x 16

IDT72105
IDT72115
IDT72125

FEATURES:

- 25ns parallel port access time, 35ns cycle time
- 45MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the $\overline{FL}$/DIR pin
- Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full
- Dual-port zero fall-through architecture
- Available in 28-pin 300 mil plastic and ceramic DIP, 28-pin SOIC, 32-pin LCC and 32-pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72105/72115/72125s are very high speed, low power dedicated parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port with 256, 512 and 1K word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

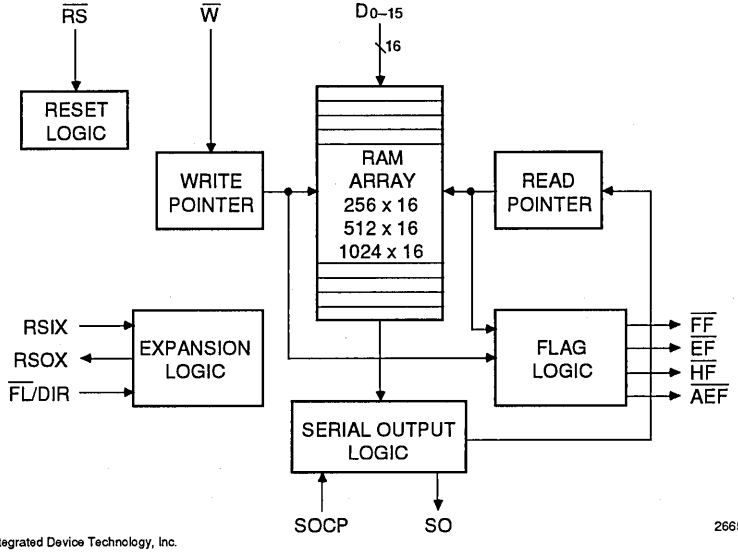
The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

The IDT72105/15/25 are fabricated using IDT's leading edge, submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

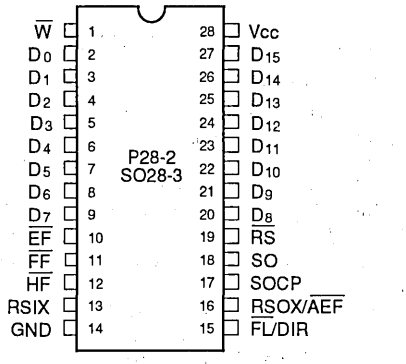
5

FUNCTIONAL BLOCK DIAGRAM



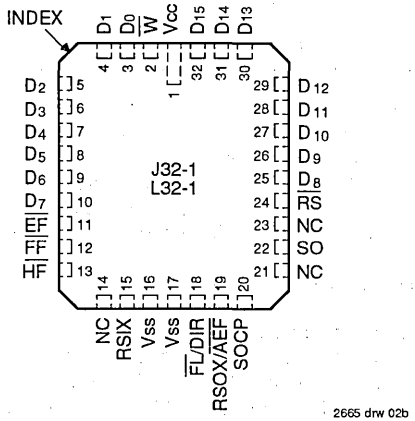
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

2665 drw 02a



LCC/PLCC
TOP VIEW

2665 drw 02b

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D15	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/ Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) pin controls shift direction after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{HF}$	Half-Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half-full. When $\overline{HF}$ is HIGH, the device is empty to half-full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When $\overline{AEF}$ is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
Vcc	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

2665 tbl 01

STATUS FLAGS

Number of Words in FIFO						
IDT72105	IDT72115	IDT72125	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1–31	1–63	1–127	H	L	H	H
32–128	64–256	128–512	H	H	H	H
129–224	257–448	513–896	H	H	L	H
225–255	449–511	897–1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	° C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	° C
T_{STG}	Storage Temperature	-55 to + 125	-65 to + 155	° C
I_{OUT}	DC Output Current	50	50	mA

2665 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

2665 tbl 04

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

5

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72105/IDT72115/ IDT72125 Commercial			IDT72105/IDT72115/ IDT72125 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA(5)	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA(6)	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	50	100	—	75	125	mA
I_{CC2}(3)	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = V_{IH})(SOCP = V_{IL})	—	4	8	—	4	12	mA
I_{CC3}(3,4,7)	Power Down Current	—	1	6	—	1	8	mA

2665 tbl 05

NOTES:
1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. SOCP = V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = Vcc - 0.2V; SOCP = 0.2V; all other inputs ≥ Vcc - 0.2 or ≤ 0.2V.
5. For SO, I_{OUT} = -4mA.
6. For SO, I_{OUT} = 16mA.
7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V±10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Figure	COM'L 72105L25 72115L25 72125L25 Min.	COM'L 72105L25 72115L25 72125L25 Max.	MILITARY 72105L30 72115L30 72125L30 Min.	MILITARY 72105L30 72115L30 72125L30 Max.	COM'L AND MILITARY 72105L50 72115L50 72125L50 Min.	COM'L AND MILITARY 72105L50 72115L50 72125L50 Max.	COM'L AND MILITARY 72105L80 72115L80 72125L80 Min.	COM'L AND MILITARY 72105L80 72115L80 72125L80 Max.	Unit
t_S	Parallel Shift Frequency	—	—	28.5	—	25	—	15	—	10	MHz
t_{SOCP}	Serial Shift Frequency	—	—	50	—	45	—	40	—	28	MHz
PARALLEL INPUT TIMINGS											
t_{WC}	Write Cycle Time	2	35	—	40	—	65	—	100	—	ns
t_{WPW}	Write Pulse Width	2	25	—	30	—	50	—	80	—	ns
t_{WR}	Write Recovery Time	2	10	—	10	—	15	—	20	—	ns
t_{DS}	Data Set-up Time	2	12	—	13	—	15	—	15	—	ns
t_{DH}	Data Hold Time	2	0	—	1	—	2	—	5	—	ns
t_{WEF}	Write High to $\overline{EF}$ High	5, 6	—	35	—	40	—	45	—	50	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	4, 7	—	35	—	40	—	45	—	50	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	40	—	45	—	50	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	7	25	—	30	—	50	—	80	—	ns
SERIAL OUTPUT TIMINGS											
t_{SOCP}	Serial Clock Cycle Time	3	20	—	22	—	25	—	35	—	ns
t_{SOCW}	Serial Clock Width High/Low	3	8	—	9	—	10	—	15	—	ns
t_{SOPD}	SOCP Rising Edge to SO Valid Data	3	—	14	—	15	—	15	—	17	ns
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	3	3	14	3	14	3	15	3	17	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	3	3	14	3	14	3	15	3	17	ns
t_{SOCEF}	SOCP Rising Edge to $\overline{EF}$ Low	5, 6	—	35	—	40	—	45	—	50	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	4, 7	—	35	—	40	—	45	—	50	ns
t_{SOCF}	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	40	—	45	—	50	ns
t_{REFSO}	SOCP Delay After $\overline{EF}$ High	6	35	—	40	—	65	—	100	—	ns
RESET TIMINGS											
t_{RSC}	Reset Cycle Time	1	35	—	45	—	65	—	100	—	ns
t_{RS}	Reset Pulse Width	1	25	—	30	—	50	—	80	—	ns
t_{RSS}	Reset Set-up Time	1	25	—	30	—	50	—	80	—	ns
t_{RSR}	Reset Recovery Time	1	10	—	15	—	15	—	20	—	ns
EXPANSION MODE TIMINGS											
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	7	—	8	—	10	—	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	1	—	2	—	5	—	ns
t_{DIRS}	DIR Set-up Time to SOCP Rising Edge	9	10	—	11	—	12	—	12	—	ns
t_{DIRH}	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	5	—	5	—	ns
t_{SOXD1}	SOCP Rising Edge to RSOX Rising Edge	9	—	15	—	17	—	17	—	20	ns
t_{SOXD2}	SOCP Rising Edge to RSOX Falling Edge	9	—	15	—	17	—	17	—	20	ns
t_{SIXS}	RSIX Set-up Time to SOCP Rising Edge	9	5	—	5	—	8	—	15	—	ns
t_{SIXPW}	RSIX Pulse Width	9	10	—	10	—	15	—	20	—	ns

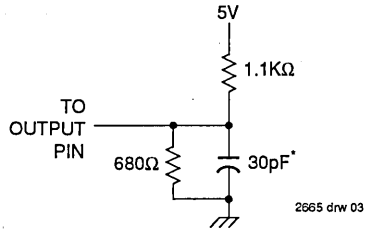
NOTE:
1. Values guaranteed by design.

2665 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

2665 tbl 08

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

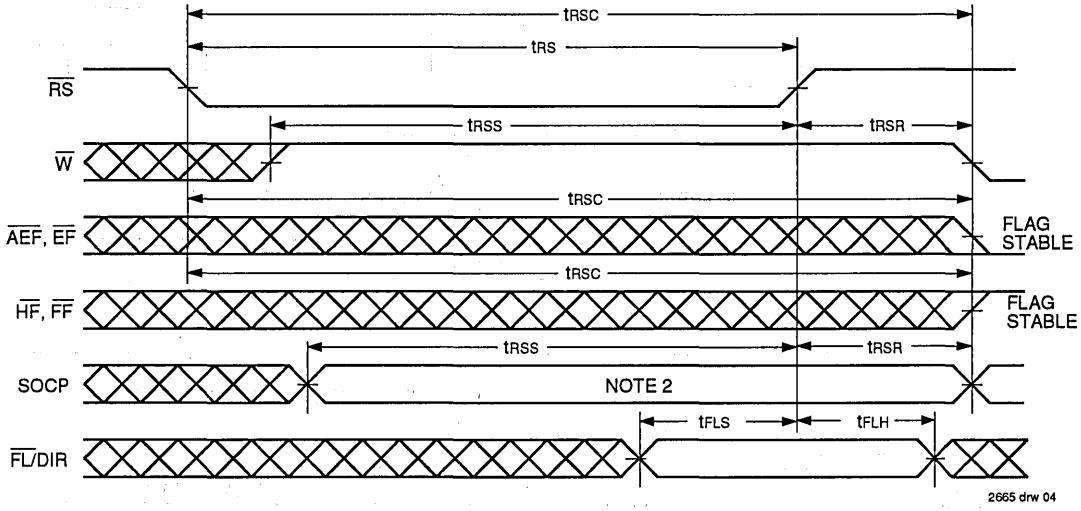
The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is internally inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. SOCP should be in the steady low or high during tRSS. The first low-high (or high-low) transition can begin after tRSR.

Figure 1. Reset

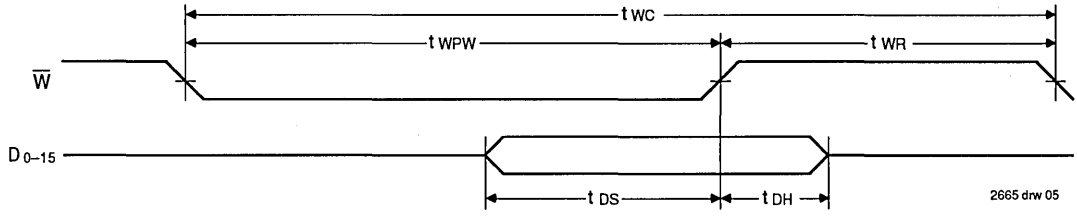
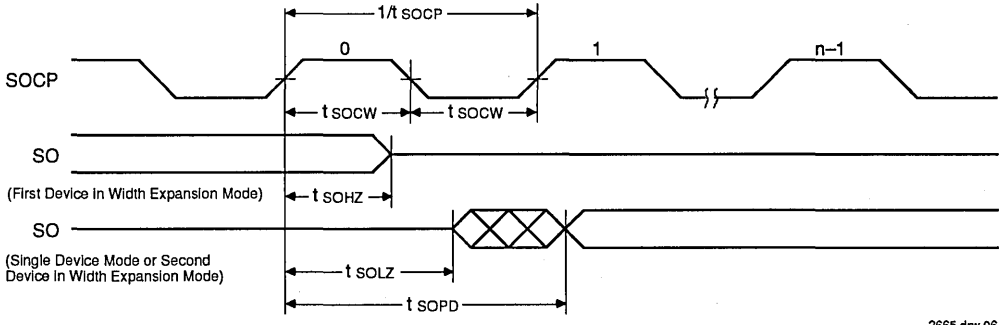


Figure 2. Write Operation



NOTE:
1. In Single Device Mode, SO will not tri-state except after reset.

Figure 3. Read Operation

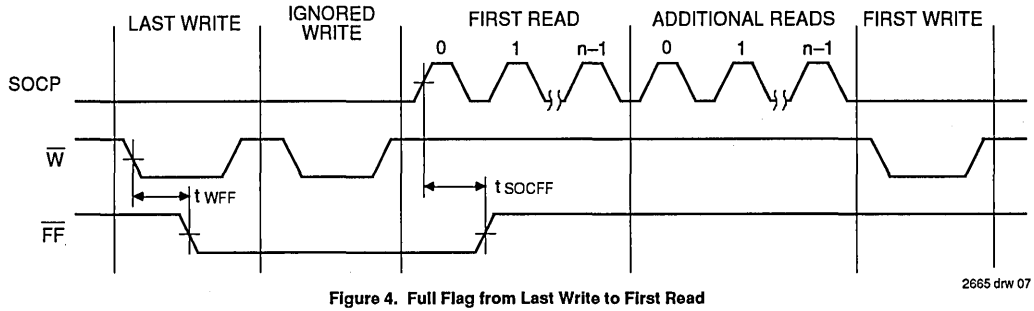
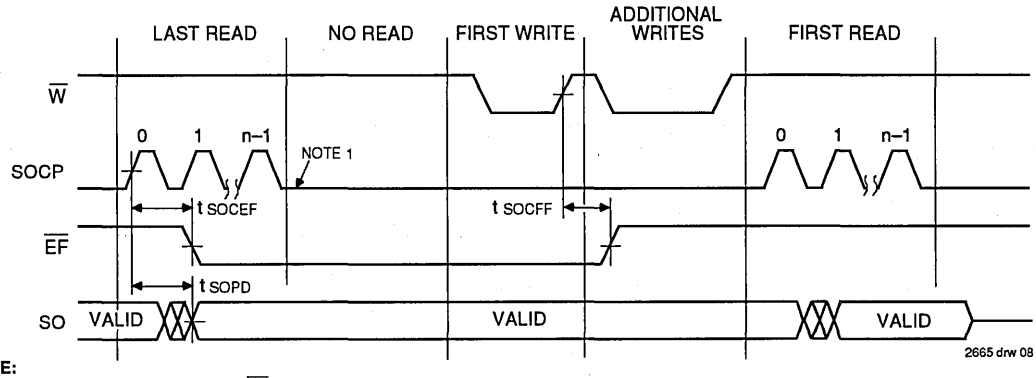
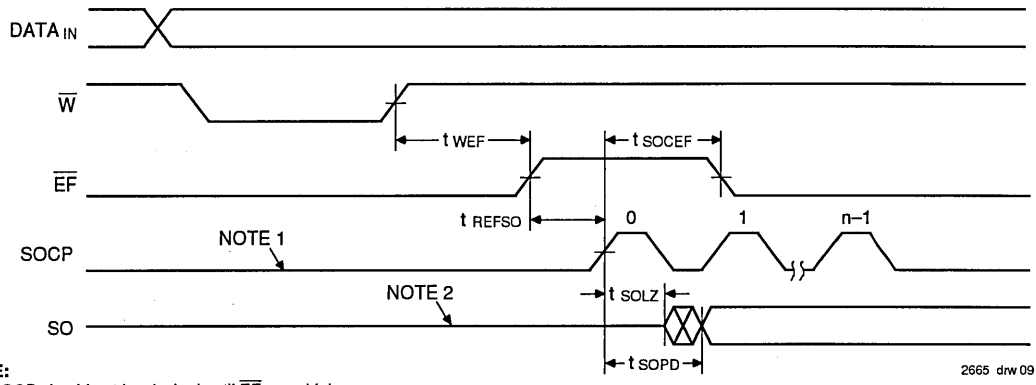


Figure 4. Full Flag from Last Write to First Read



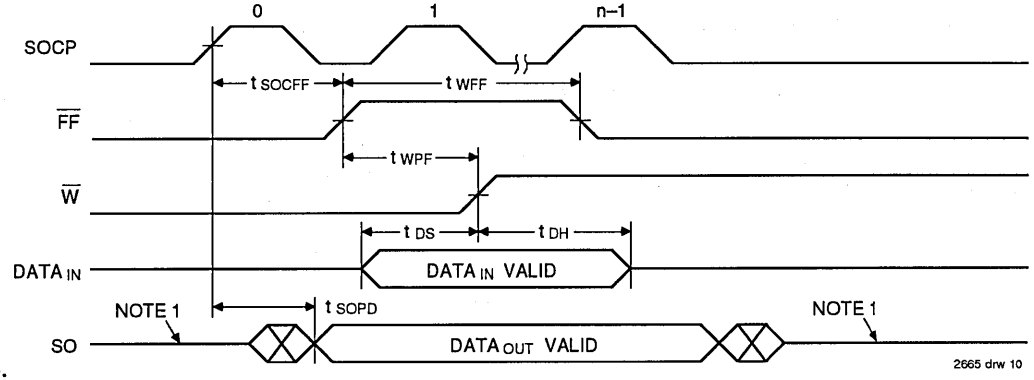
NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.
2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing



NOTE:
1. Single Device Mode will not tri-state but will retain the last valid data.

Figure 7. Full Boundary Condition Timing

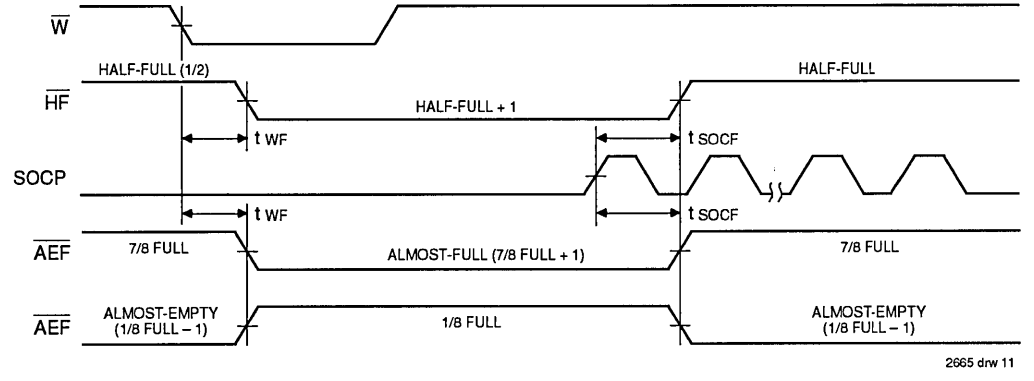


Figure 8. Half-Full, Almost-Full and Almost-Empty Timings

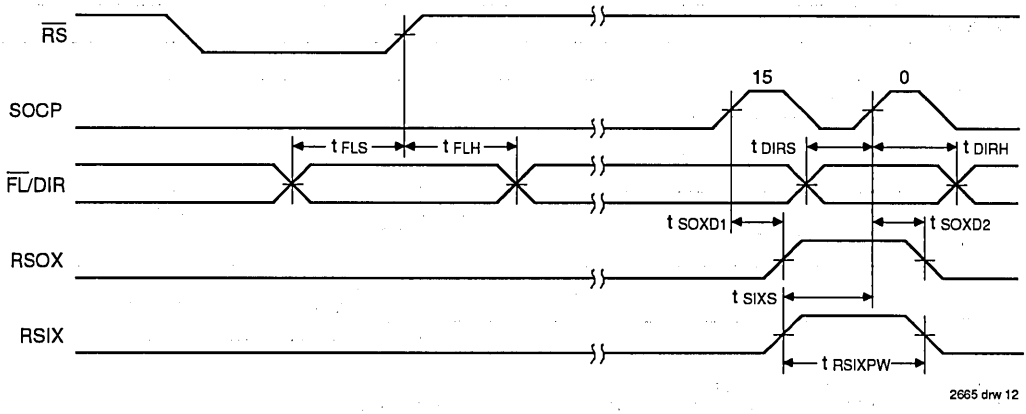


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost-Empty and Almost-Full Flag.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

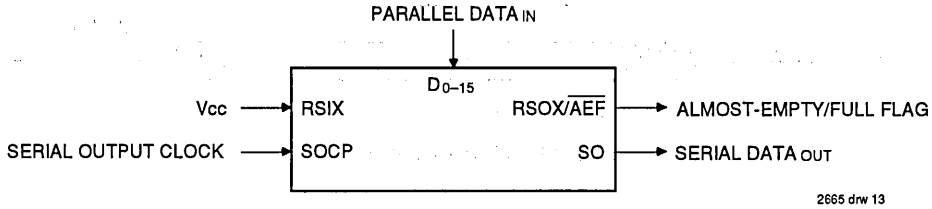


Figure 10. Single Device Configuration

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

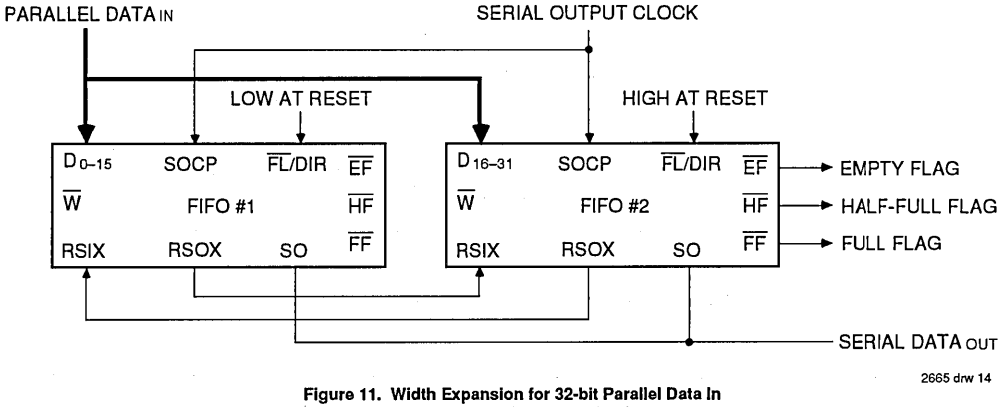
2665 tbl 09

Table 1. Reset and First Load Truth Table–Single Device Configuration

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half-Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty/Almost-Full flag is not available. The RSOX pin is used for expansion.

Depth Expansion (Daisy Chain) Mode



2665 drw 14

Figure 11. Width Expansion for 32-bit Parallel Data In

The IDT72105/15/25 can easily be adapted to applications requiring greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25s and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO is being written. A word of data must be written sequentially into each FIFO so that the data will be read in the correct sequence. The IDT72105/15/25 operates in the Depth Expansion Mode when the following conditions are met:

1. The first device must be programmed by holding $\overline{FL}$ LOW at Reset. All other devices must be programmed by holding $\overline{FL}$ high at reset.
2. The Read Serial Out Expansion pin (RSOX) of each device must be tied to the Read Serial In Expansion pin (RSIX) of the next device (see Figure 12).
3. External logic is needed to generate composite Empty, Half-Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

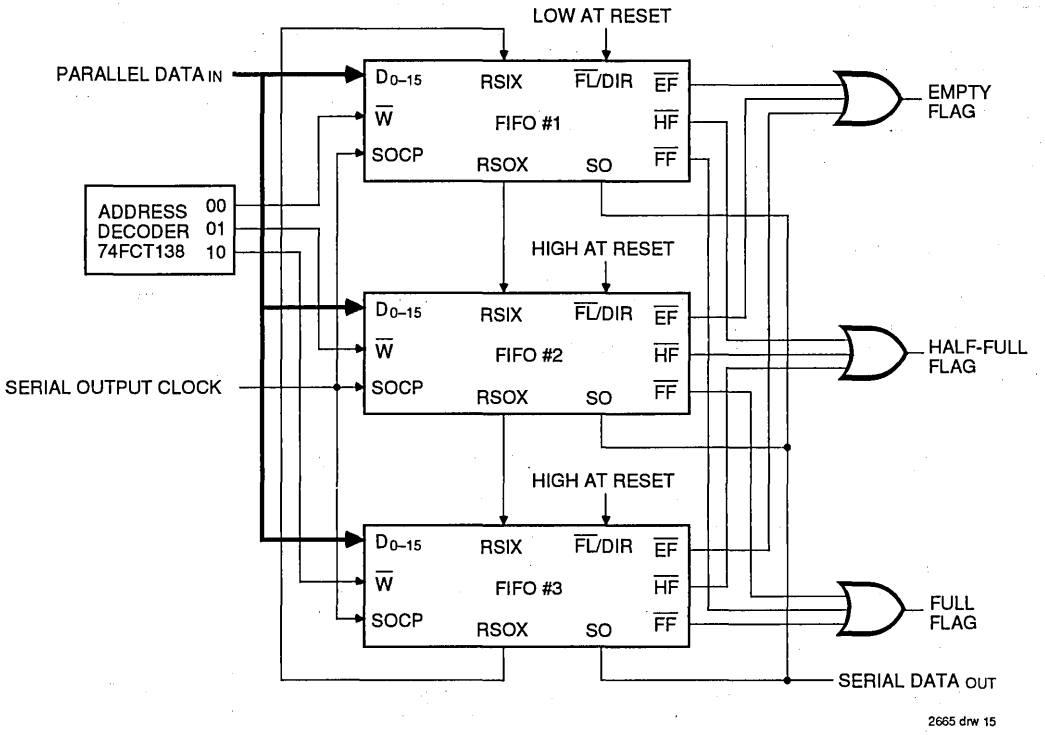


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half- Full Flag Output, $\overline{FF}$ = Full Flag Output.

2665 tbl 10

Table 2. Reset and First Load Truth Table–Width/Depth Compound Expansion Mode

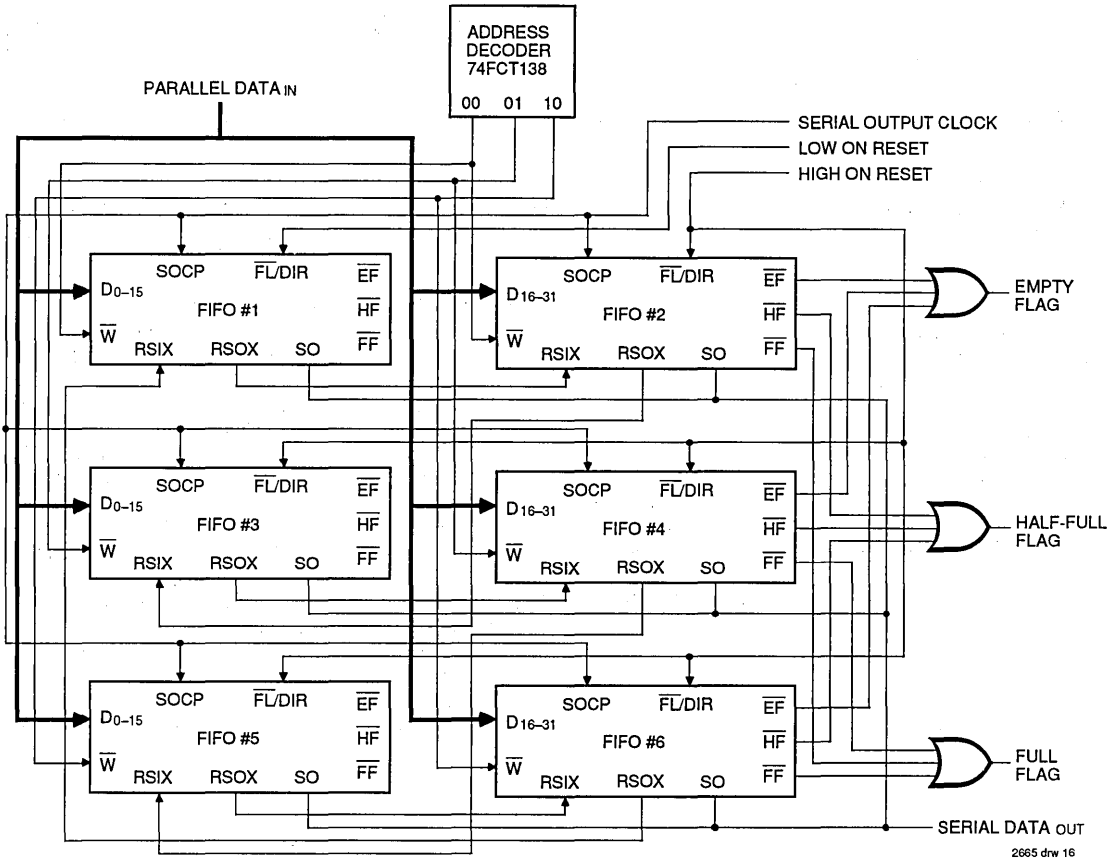


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

5

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT72131
IDT72141

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 7-9, 16-18, 32-36 bit using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low power CEMOS™ technology
- Available in 28-pin ceramic, plastic DIP and 32-pin plastic leaded chip corner (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

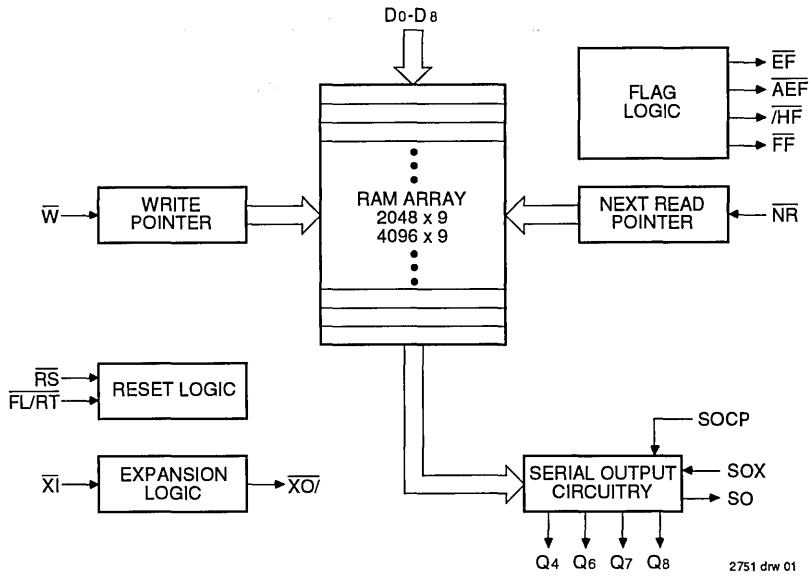
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDTs serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDTs unique Flexishift serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDTs high-speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0–D_8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high and SOCP must be low during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width , connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{W}$ must be high and SOCP must be low before setting $\overline{FL}/\overline{RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, the SOX pin of the least significant device is tied high. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. Data is then clocked out least significant bit first. For single device operation, SOX is tied high.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. See the description on page 6 for more details.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when HF is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 and Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Single ground at 0V.

2751 tbl 01

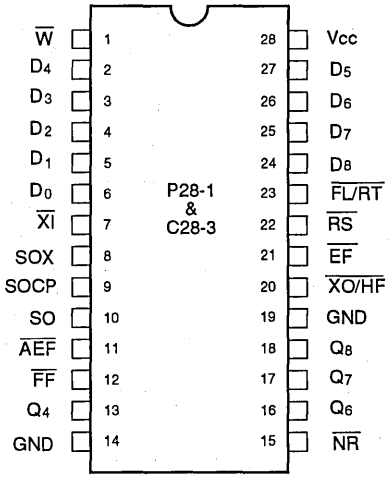
STATUS FLAGS

Number of Words in FIFO					
IDT72131	IDT72141	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2751 tbl 02

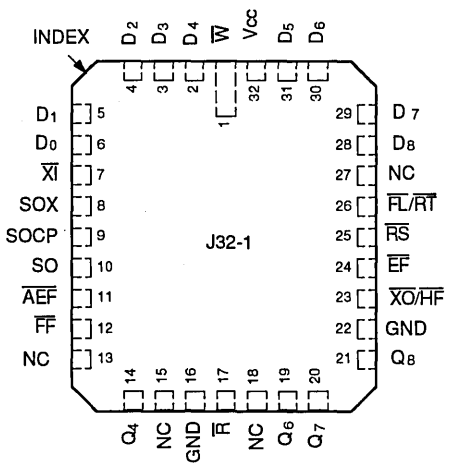
5

PIN CONFIGURATIONS



2751 drw 02a

DIP
TOP VIEW



2751 drw 02b

PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2751 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2751 tbl 04
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2751 tbl 05
1. This parameter is sampled and not 100% tested.

5

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		IDT72131/IDT72141 Commercial			IDT72131/IDT72141 Military			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -8mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 16mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}(3)	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$(3,4)	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3(S)}$(3,4)	Power Down Current	—	—	8	—	—	12	mA

NOTES: 2751 tbl 06
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{W}$ = V_{CC} -0.2V; SOCP ≤ 0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72131x35 IDT72141x35		IDT72131x40 IDT72141x40		IDT72131x50 IDT72141x50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz
PARALLEL INPUT TIMINGS								
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns
t_{WEF}	Write High to $\overline{EF}$ High	—	30	—	35	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	—	30	—	35	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	—	40	—	50	—	ns
SERIAL OUTPUT TIMINGS								
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	5	16	5	16	5	26	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	5	22	5	22	5	22	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns
t_{SOCW}	Serial In Clock Width High/Low	8	—	8	—	10	—	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ Low	—	20	—	25	—	25	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	—	30	—	35	—	40	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	—	30	—	35	—	40	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ High	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{RSQL}	Reset to Q Low	20	—	20	—	35	—	ns
t_{RSQH}	Reset to Q High	20	—	20	—	35	—	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	35	—	40	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	35	—	40	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

2751 tbl 07

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Military and Commercial						Unit
		IDT72131x65 IDT72141x65		IDT72131x80 IDT72141x80		IDT72131x120 IDT72141x120		
		Min.	Max.	Min.	Max.	Min.	Max.	
tS	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz
tSOCP	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz
PARALLEL INPUT TIMINGS								
tDS	Data Set-up Time	30	—	40	—	40	—	ns
tDH	Data Hold Time	10	—	10	—	10	—	ns
tWC	Write Cycle Time	80	—	100	—	140	—	ns
tWPW	Write Pulse Width	65	—	80	—	120	—	ns
tWR	Write Recovery Time	15	—	20	—	20	—	ns
tWEF	Write High to $\overline{EF}$ High	—	60	—	60	—	60	ns
tWFF	Write Low to $\overline{FF}$ Low	—	60	—	60	—	60	ns
tWF	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	80	—	100	—	140	ns
tWPF	Write Pulse Width After $\overline{FF}$ High	65	—	80	—	120	—	ns
SERIAL OUTPUT TIMINGS								
tSOHZ	SOCP Rising Edge to SO at High Z[1]	5	20	5	25	5	35	ns
tSOLZ	SOCP Rising Edge to SO at Low Z[1]	5	22	5	30	5	35	ns
tSOPD	SOCP Rising Edge to Valid Data on SO	—	22	—	30	—	35	ns
tSOX	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns
tSOCW	Serial In Clock Width High/Low	10	—	15	—	15	—	ns
tSOCEF	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ Low	—	30	—	30	—	30	ns
tSOCFF	SOCP Rising Edge to $\overline{FF}$ High	—	50	—	60	—	65	ns
tSOCF	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	—	50	—	60	—	65	ns
tREFSO	Recovery Time SOCP After $\overline{EF}$ High	65	—	80	—	120	—	ns
RESET TIMINGS								
tRSC	Reset Cycle Time	80	—	100	—	140	—	ns
tRS	Reset Pulse Width	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	15	—	20	—	20	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tRSQL	Reset to Q Low	50	—	65	—	105	—	ns
tRSQH	Reset to Q High	50	—	65	—	105	—	ns
RETRANSMIT TIMINGS								
tRTC	Retransmit Cycle Time	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	15	—	20	—	20	—	ns
DEPTH EXPANSION MODE TIMINGS								
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

2751 tbl 08

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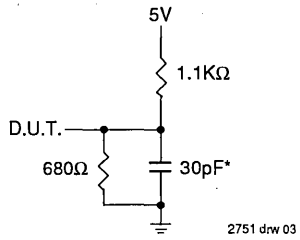
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2751 tbl 09



or equivalent circuit

Figure A. Ouput Load

*Including jig and scope capacitances

FUNCTIONAL DESCRIPTION

Parallel Data Input

The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full-Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked once the last bit of the last word has been clocked out. If it is, then two things will occur. One, the SO pin will go high-Z and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D0, then D1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q4, Q6, Q7 or Q8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.

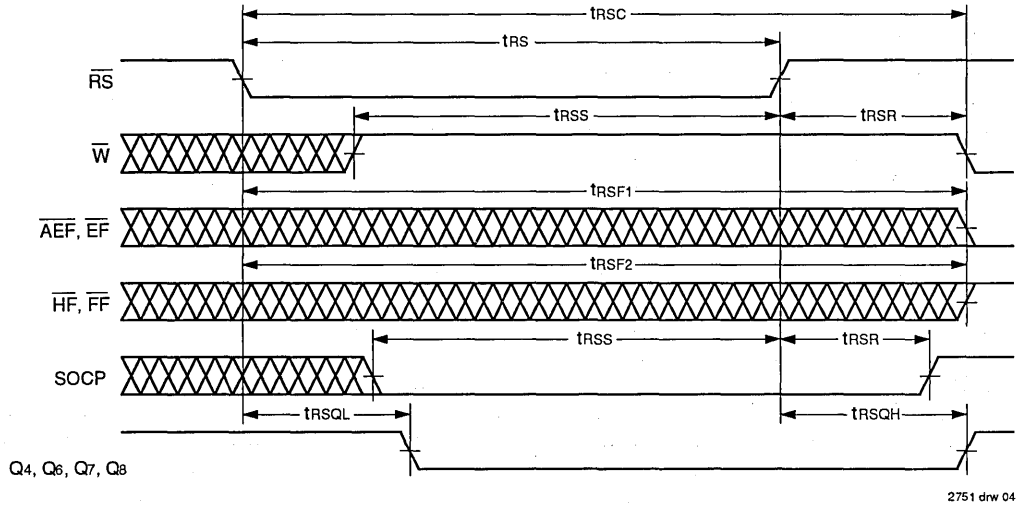


Figure 1. Reset

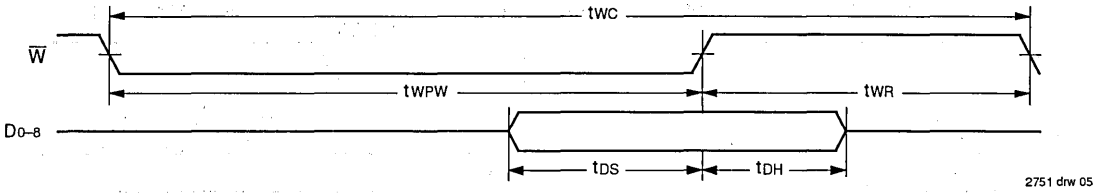


Figure 2. Write Operation

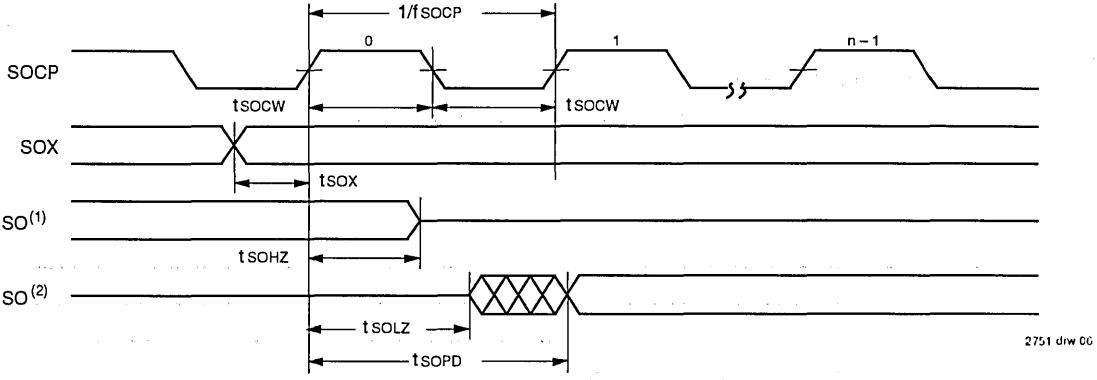


Figure 3. Read Operation

NOTES:
1. This timing applies to the Active Device in Width Expansion Mode.
2. This timing applies to Single Device Mode at Empty Boundary ($\overline{EF}$ = low) and the Next Active Device in Width Expansion Mode.

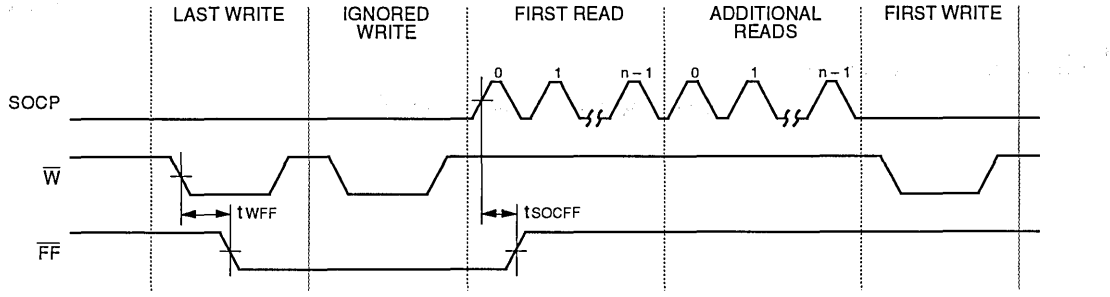
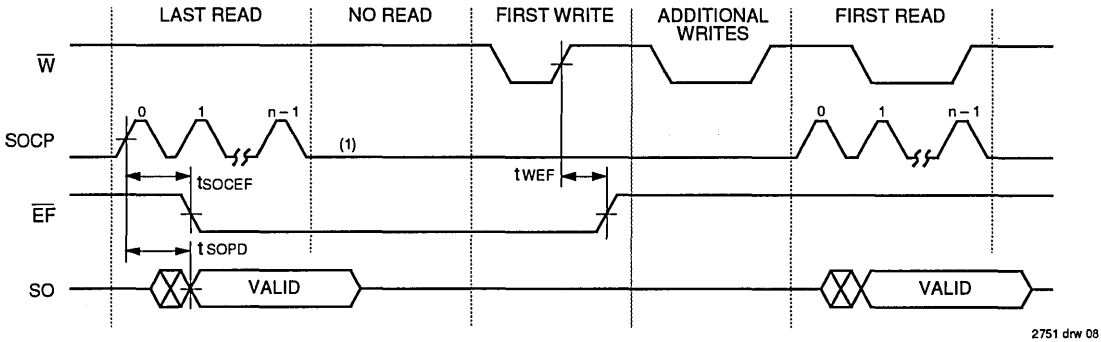
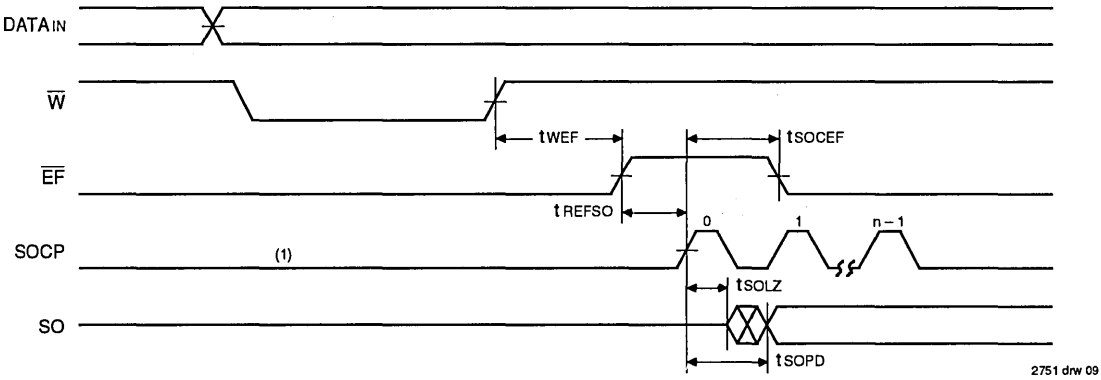


Figure 4. Full Flag from Last Write to First Read



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

Figure 6. Empty Boundary Condition Timing

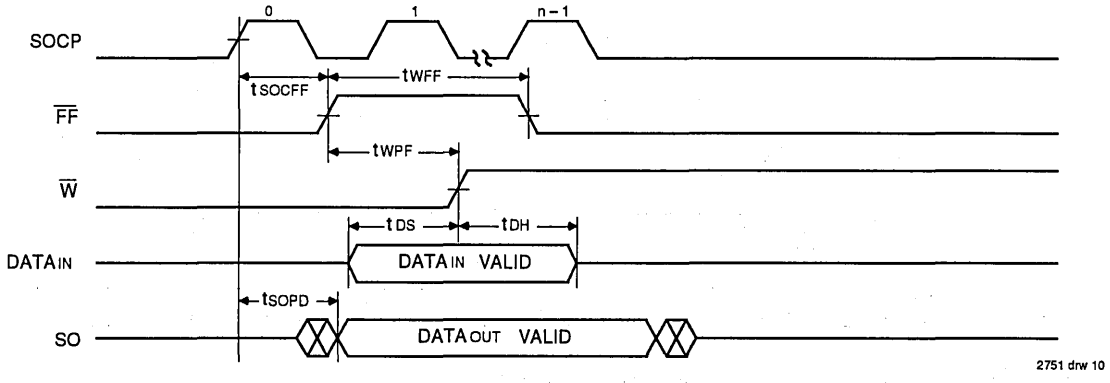


Figure 7. Full Boundry Condition Timing

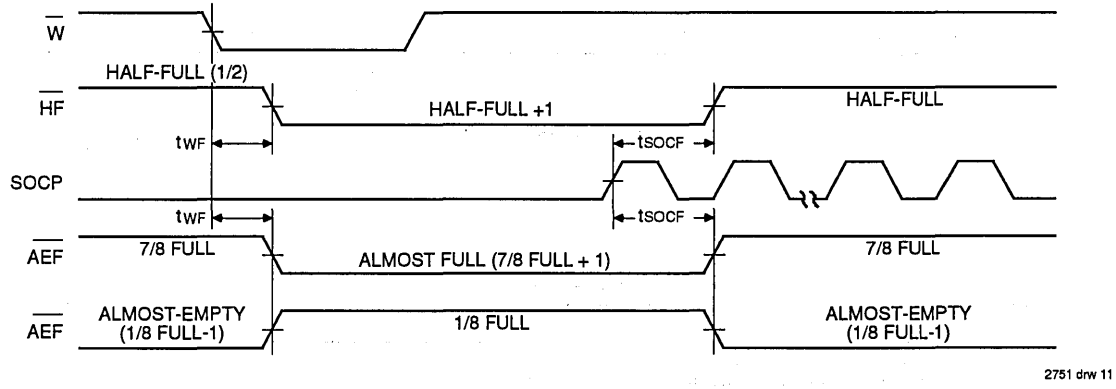
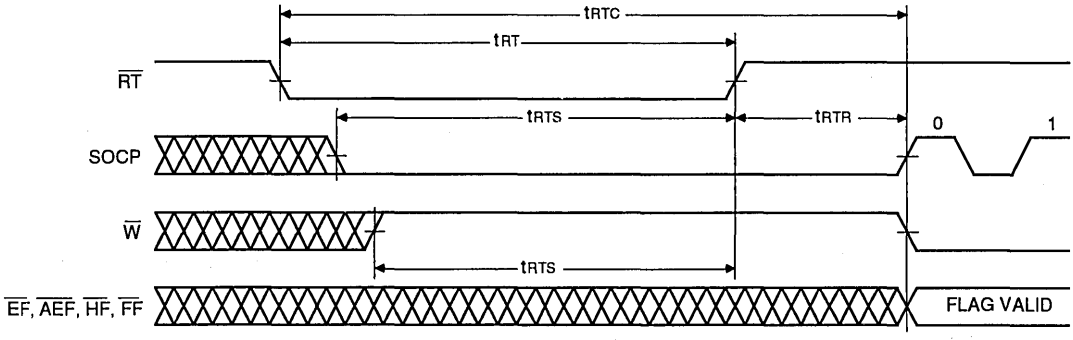


Figure 8. Half Full, Almost Full and Almost Empty Timings

5



NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 9. Retransmit

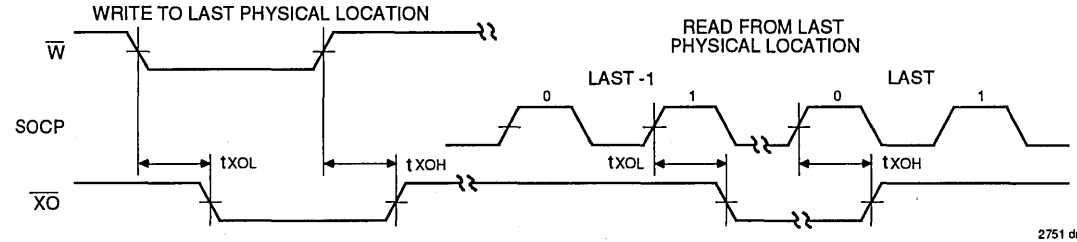


Figure 10. Expansion-Out

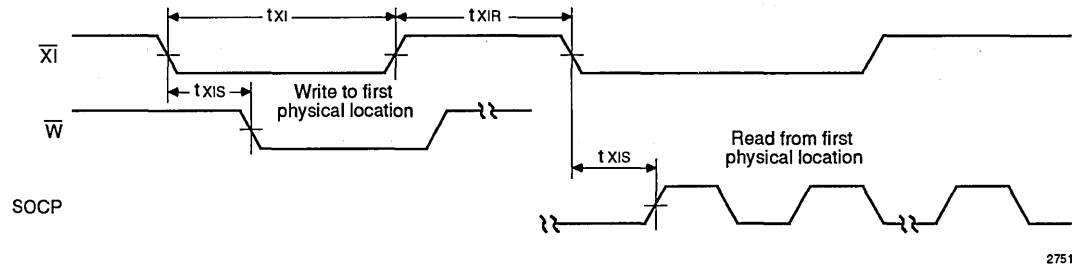


Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q4, Q6, Q7, Q8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SOCP clock pulse. This continues until the Q line connected to $\overline{NR}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

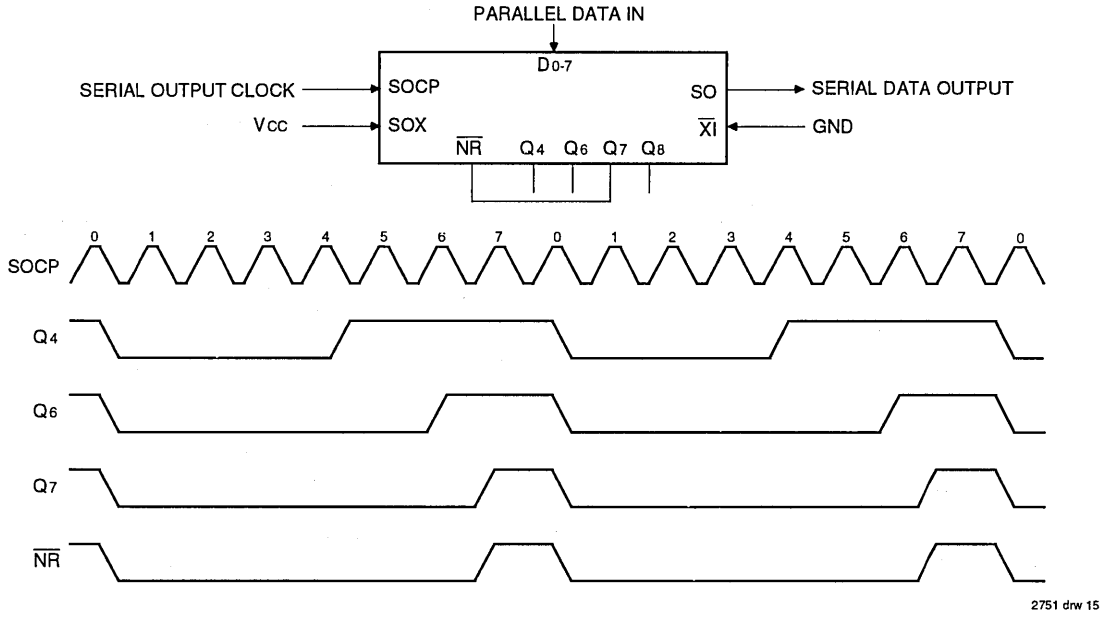


Figure 12. Eight-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

2751 tbl 10

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the Do of that device goes HIGH, the cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit-bus.

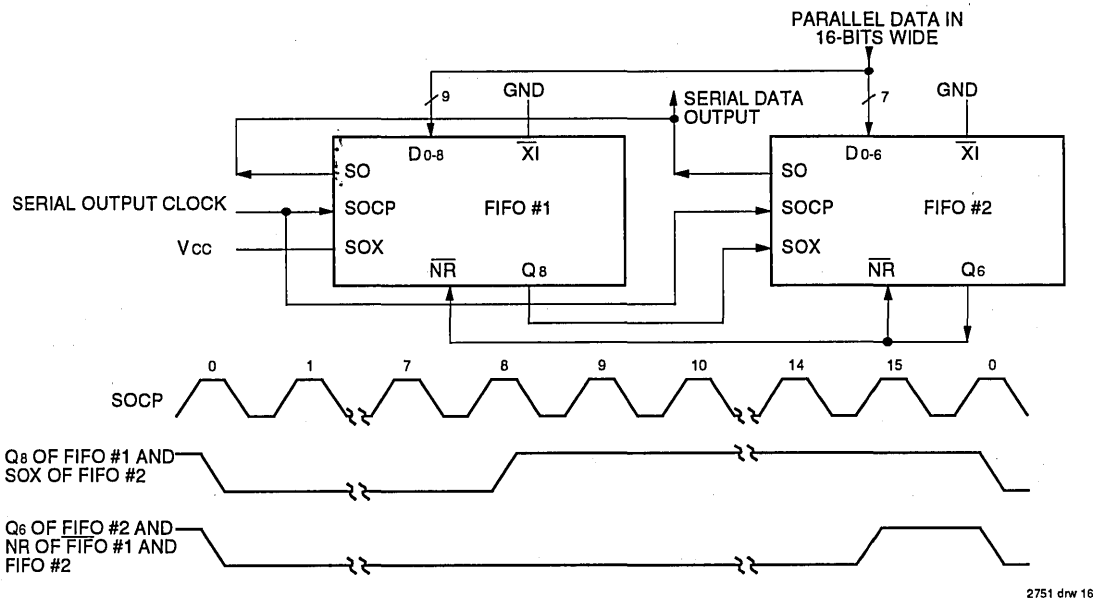
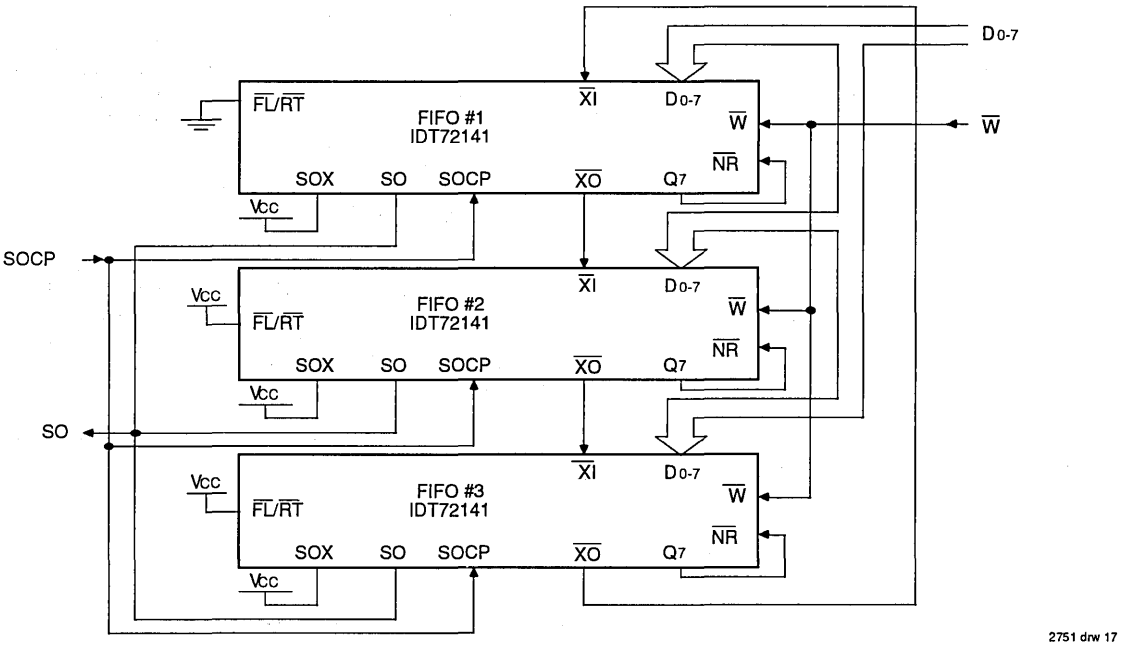


Figure 13. Width Wxpansion for 16-bit Parallel Data In. The Parallel Data In is tied to D0-8 of FIFO #1 and D0-6 of FIFO #2.

Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.



2751 drw 17

Figure 14. A 12K x 8 Parallel-In Serial-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset-All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

2751 tbl 11

Integrated Device Technology, Inc.

CMOS SERIAL-TO-PARALLEL FIFO 2048 x 9-BIT 4096 x 9-BIT

IDT72132
IDT72142

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 8, 9, 16-18, and 32-36 bit using Flexshift™ serial input without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CEMOS™ technology
- Available in a 28-pin ceramic, plastic DIP and 32-pin plastic leaded chip carrier (PLCC) packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

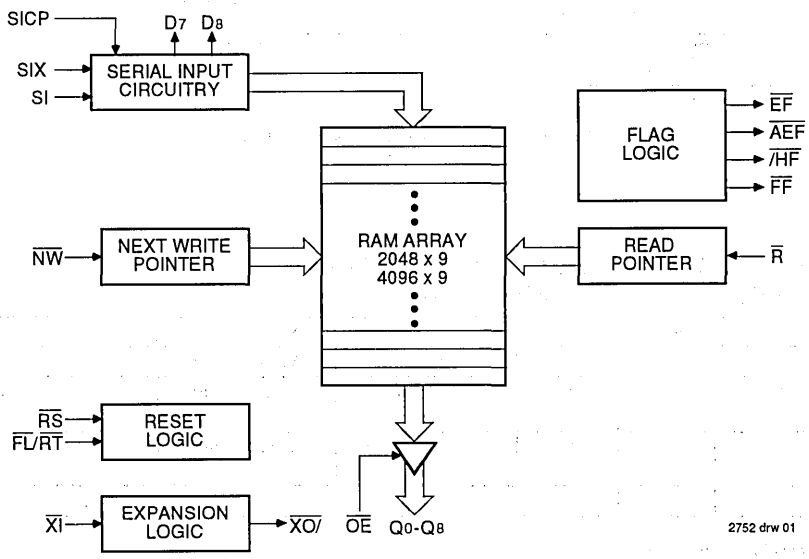
The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDTs parallel-to-serial FIFOs (IDT72131/72141) for bidirectional serial data buffering.

The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDTs unique Flexshift serial expansion logic (SIX, $\overline{NW}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDTs high-speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



CEMOS and Flexishift are trademarks of Integrated Device Technology, Inc.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
SI	Serial Input	I	Serial data is shifted in least significant bit first. In the serial cascade mode, the Serial Input (SI) pins are tied together and SIX plus D_7, D_8 determine which device stores the data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$, and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ must be high during an $\overline{RS}$ cycle.
$\overline{NW}$	Next Write	I	To program the Serial In word width , connect $\overline{NW}$ with one of the Data Set pins (D_7, D_8).
SICP	Serial Input Clock	I	Serial data is read into the serial input register on the rising edge of SICP. In both Depth and Serial Word Width Expansion modes, all of the SICP pins are tied together.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of SICP. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked and Q_0-Q_8 are in a high impedance condition.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ must be high and SICP must be low before setting $\overline{FL}/\overline{RT}$ low. Retransmit is not possible in depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SIX	Serial Input Expansion	I	In the Expansion mode, the SIX pin of the least significant device is tied high. The SIX pin of all other devices is connected to the D_7 or D_8 pin of the previous device. For single device operation, SIX is tied high.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three state buffers inhibit data flow.
Q_0–Q_8	Output Data	O	Data outputs for 9-bit wide data.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and data must not be clocked by SICP. When $\overline{FF}$ is high, the device is not full. See the diagram on page 7 for more details.
$\overline{EF}$	Empty Flag Almost-Full Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Half-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
D_7, D_8	Data Set	O	The appropriate Data Set pin (D_7, D_8) is connected to $\overline{NW}$ to program the Serial In data word width. For example: D_7 - $\overline{NW}$ programs a 8-bit word width, D_8 - $\overline{NW}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Three grounds at 0V.

2752 tbl 01

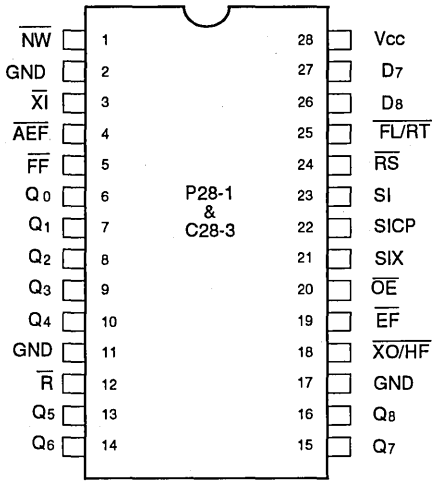
STATUS FLAGS

Number of Words in FIFO					
IDT72132	IDT72142	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2752 tbl 02

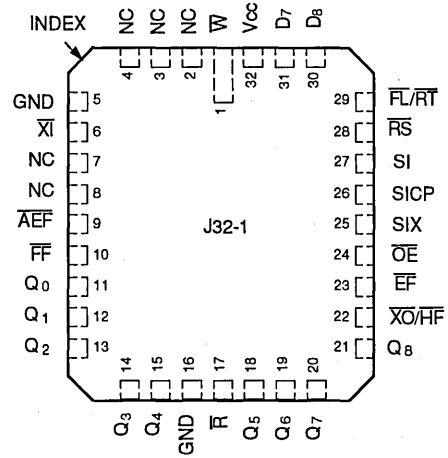
5

PIN CONFIGURATIONS



2752 drw 02

DIP
TOP VIEW



2752 drw 02b

PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2752 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2752 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2752 tbl 05

1. This parameter is sampled and not 100% tested.

5

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72132/IDT72142 Commercial			IDT72132/IDT72142 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$(3,4)	Power Down Current	—	—	2	—	—	4	mA
$I_{CC3(S)}$(3,4)	Power Down Current	—	—	8	—	—	12	mA

NOTES: 2752 tbl 06

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{R}$ = V_{CC} -0.2V; SICP ≤ 0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72132x35 IDT72142x35		IDT72132x40 IDT72142x40		IDT72132x50 IDT72142x50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SICP}	Serial-InShift Frequency	—	50	—	50	—	40	MHz
PARALLEL OUTPUT TIMINGS								
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[1]	5	—	5	—	10	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[1]	—	20	—	25	—	30	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	15	—	15	—	15	ns
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns
SERIAL INPUT TIMINGS								
t_{SIS}	Serial Data in Set-Up Time to SICP Rising Edge	12	—	12	—	15	—	ns
t_{SIH}	Serial Data in Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns
t_{SIX}	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
t_{SICW}	Serial-In Clock Width High/Low	8	—	8	—	10	—	ns
FLAG TIMINGS								
t_{SICEF}	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	45	—	50	—	65	ns
t_{SICFF}	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	30	—	35	—	40	ns
t_{SICF}	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RFFSI}	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	15	—	15	—	ns
t_{REF}	Read Low to $\overline{EF}$ Low	—	30	—	35	—	45	ns
t_{RFF}	Read High to $\overline{FF}$ High	—	30	—	35	—	45	ns
t_{RF}	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	45	—	50	—	65	ns
t_{RSDL}	Reset to D Low	20	—	20	—	35	—	ns
t_{POI}	SICP Rising Edge to D	5	17	5	17	5	20	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	45	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	45	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	16	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested

2752 tbl 07

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

		Military and Commercial						
		IDT72132x65 IDT72142x65		IDT72132x80 IDT72142x80		IDT72132x120 IDT72142x120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
ts	Parallel Shift Frequency	—	12.5	—	10	—	7	MHz
tSOCP	Serial-Out Shift Frequency	—	33	—	28	—	25	MHz
PARALLEL OUTPUT TIMINGS								
tA	Access Time	—	65	—	80	—	120	ns
tRR	Read Recovery Time	15	—	20	—	20	—	ns
tRPW	Read Pulse Width	65	—	80	—	120	—	ns
tRC	Read Cycle Time	80	—	100	—	140	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z[1]	10	—	10	—	10	—	ns
tRHZ	Read Pulse Highto Data Bus at High Z[1]	—	30	—	35	—	35	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	ns
tOEHZ	Output Enable to High-Z (Disable)[1]	—	20	—	25	—	30	ns
tOELZ	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
tAOE	Output Enable to Data Valid (Q_{0-8})	—	25	—	30	—	35	ns
SERIAL INPUT TIMINGS								
tSIS	Serial Data in Set-Up Time to SICP Rising Edge	15	—	20	—	20	—	ns
tSIH	Serial Data in Hold Time to SICP Rising Edge	0	—	5	—	5	—	ns
tSIX	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
tSICW	Serial-In Clock Width High/Low	10	—	15	—	15	—	ns
FLAG TIMINGS								
tSICEF	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ High	—	80	—	80	—	80	ns
tSICFF	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ Low	—	50	—	60	—	60	ns
tSICF	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	80	—	80	—	80	ns
tRFFSI	Recovery Time SICP After $\overline{FF}$ Goes High	15	—	20	—	20	—	ns
tREF	Read Low to $\overline{EF}$ Low	—	60	—	60	—	60	ns
tRFF	Read High to $\overline{FF}$ High	—	60	—	60	—	60	ns
tRF	Read High to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	80	—	100	—	140	ns
tRPE	Read Pulse Width After $\overline{EF}$ High	65	—	80	—	120	—	ns
RESET TIMINGS								
tRSC	Reset Cycle Time	80	—	100	—	140	—	ns
tRS	Reset Pulse Width	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	15	—	20	—	20	—	ns
tRSF1	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	—	80	—	100	—	140	ns
tRSF2	Reset to $\overline{HF}$ and $\overline{FF}$ High	—	80	—	100	—	140	ns
tRSDL	Reset to D Low	50	—	65	—	105	—	ns
tPOI	SICP Rising Edge to D	5	25	5	30	5	35	ns
RETRANSMIT TIMINGS								
tRTC	Retransmit Cycle Time	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time	65	—	80	—	120	—	ns
tRTR	Retransmit Recovery Time	15	—	20	—	20	—	ns
DEPTH EXPANSION MODE TIMINGS								
tXOL	Read/Write to $\overline{XO}$ Low	—	65	—	80	—	120	ns
tXOH	Read/Write to $\overline{XO}$ High	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

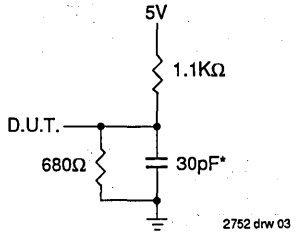
NOTE:
1. Guaranteed by design minimum times, not tested.

2752 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2752 tbl 09



or equivalent circuit

Figure A. Output Load

*Includies jig and scope capacitances

FUNCTIONAL DESCRIPTION

Serial Data Input

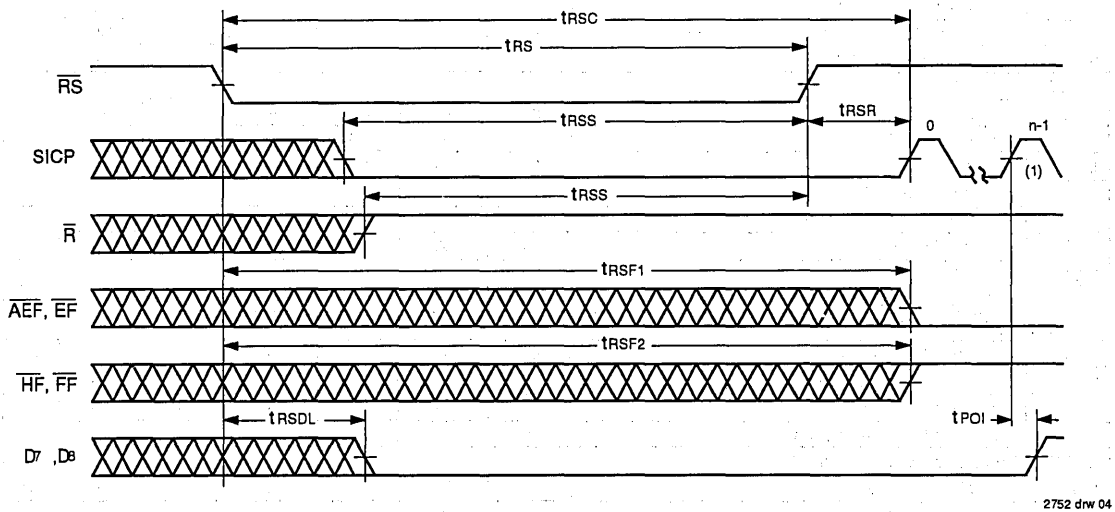
The serial data is input on the SI pin. The data is clocked in on the rising edge of SICP providing the Full Flag ($\overline{FF}$) is not asserted. If the Full Flag is asserted then the next parallel data word is inhibited from moving into the RAM array. NOTE: SICP should not be clocked once the last bit of the last word has been shifted in, as indicated by $\overline{NW}$ high and $\overline{FF}$ low. If it is, then then the input data will be lost.

The serial word is shifted in Least Significant Bit first. Thus, when the FIFO is read, the Least Significant Bit will come out on Q_0 and the second bit is on Q_1 and so on. The serial word width must be programmed by connecting the appropriate Data Set line (D_7, D_8) to the $\overline{NW}$ input. The data set lines are taps off a digital delay line. Selecting one of these taps programs the width of the serial word to be written in.

Parallel Data Output

A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. The data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$.



NOTE:
1. Input bits are numbered 0 to n-1. D_7 and D_8 correspond to n=8 and n=9 respectively

Figure 1. Reset

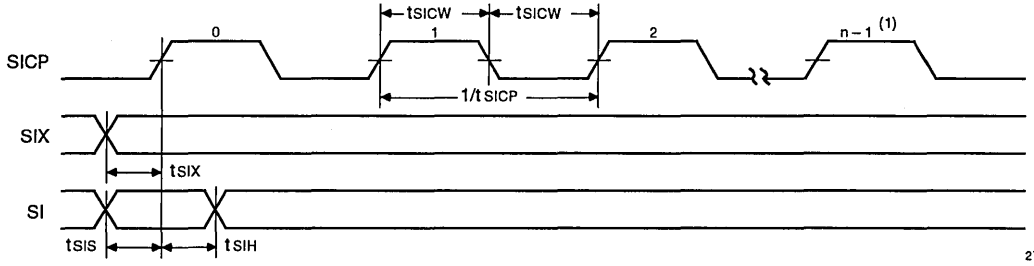


Figure 2. Write Operation

NOTE:
1. Input bits are numbered 0 to n-1.

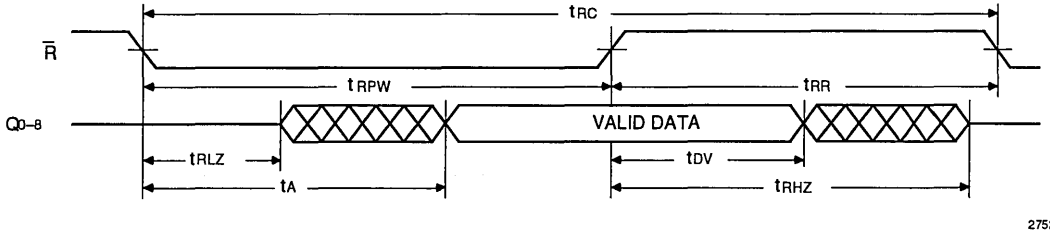


Figure 3. Read Operation

5

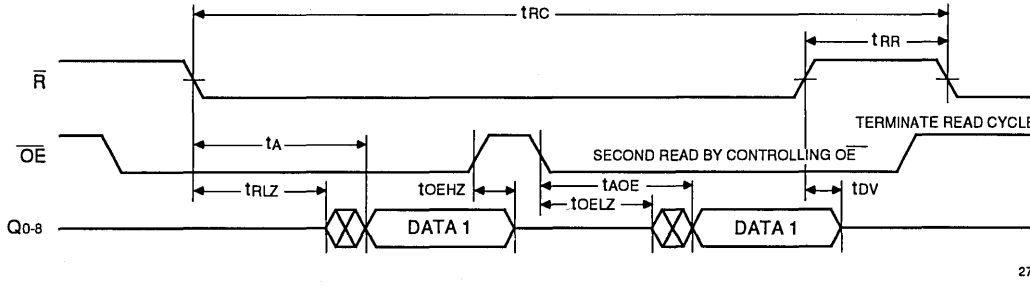
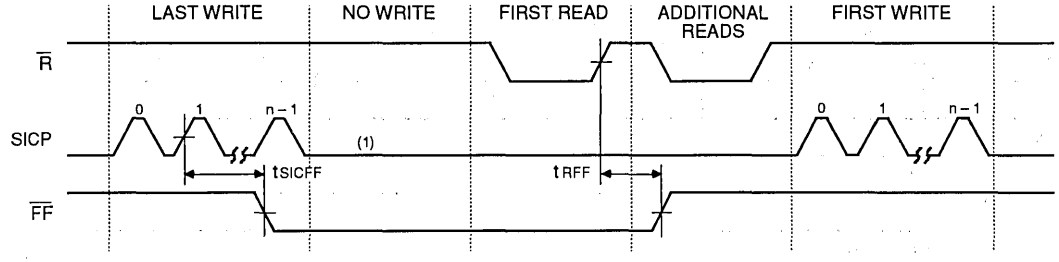


Figure 4. Output Enable Timings



NOTE:
1. SICP should not be clocked until $\overline{FF}$ goes high.

Figure 5. Full Flag from Last Write to First Read

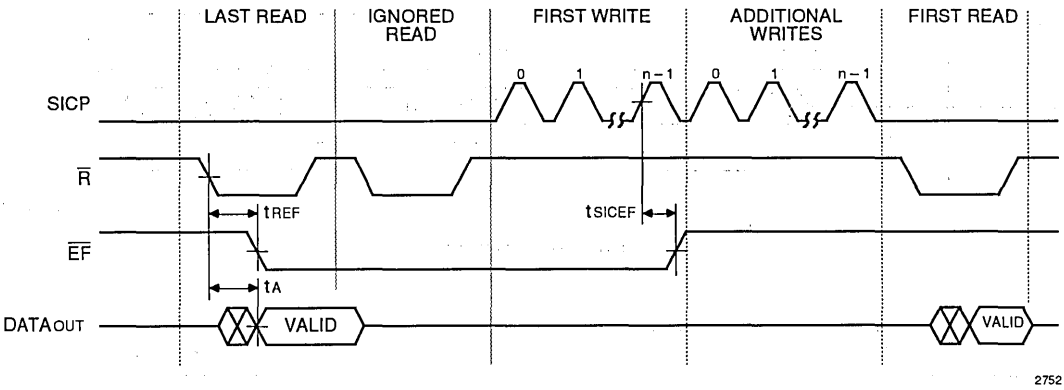


Figure 6. Empty Flag from Last Read to First Write

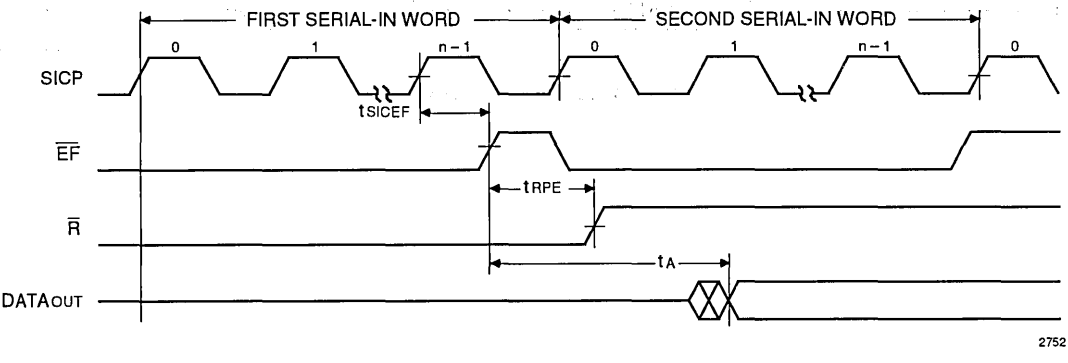
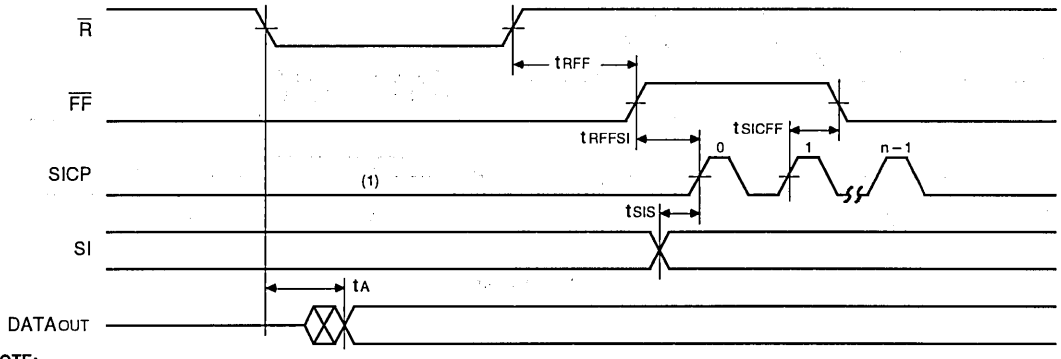


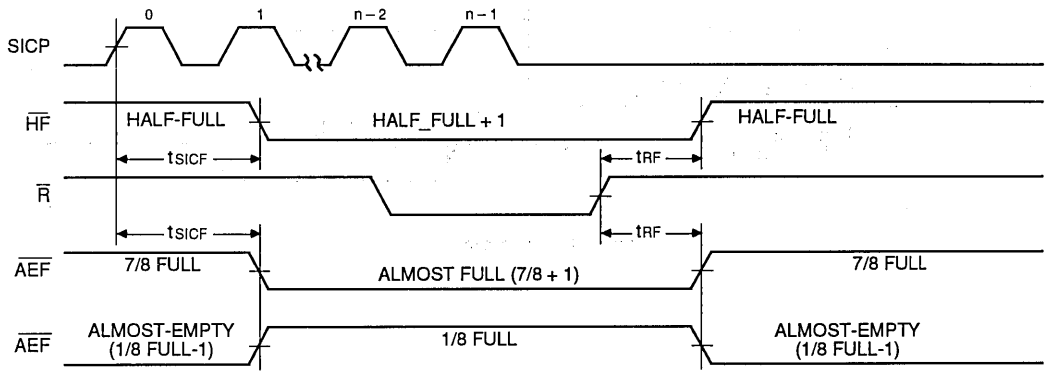
Figure 7. Empty Boundry Condition Timing



NOTE:
1. SICP should remain low until after FF goes high.

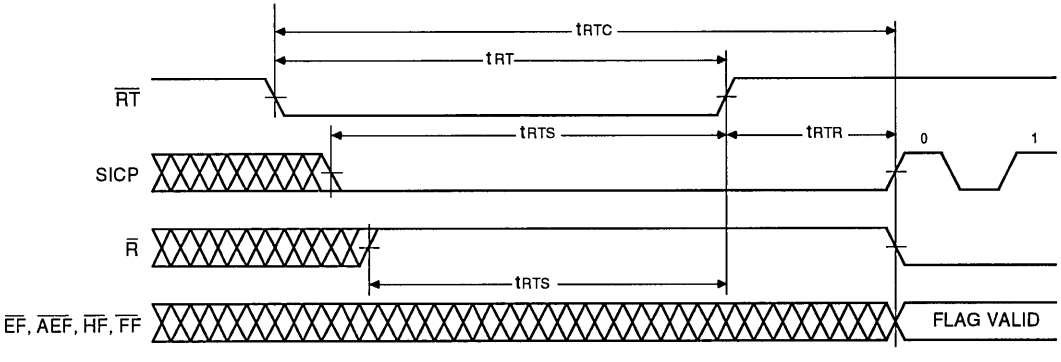
2752 drw 11

Figure 8. Full Boundry Condition Timing



2752 drw 12

Figure 9. Half Full, Almost Full and Almost Empty Timings



2752 drw 13

NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 10. Retransmit

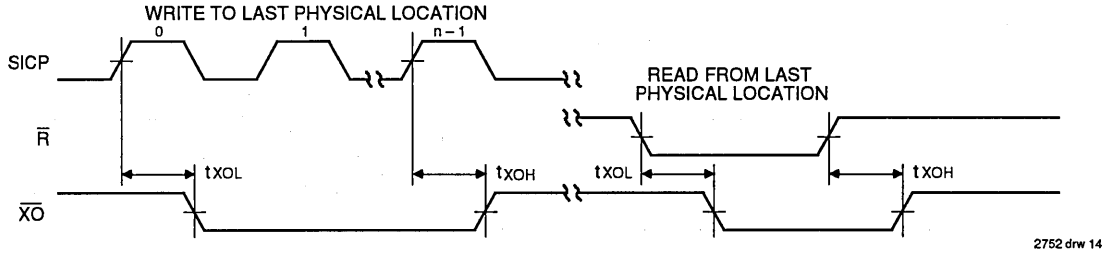


Figure 11. Expansion-Out

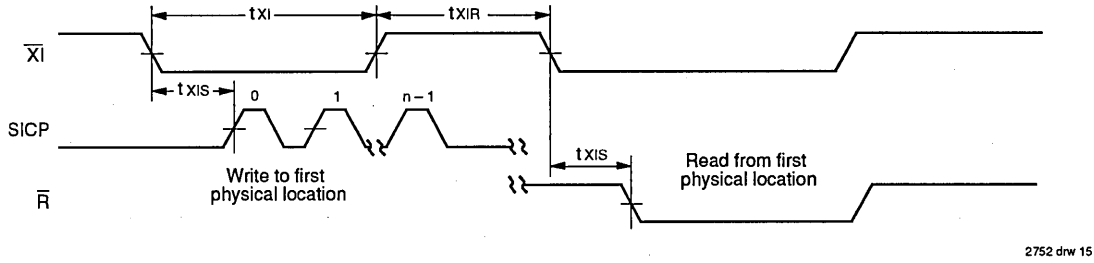


Figure 12. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SIX line is tied HIGH and not used. On the first LOW-to-HIGH of the SICP clock, both of the Data Set lines (D_7, D_8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SICP clock pulse. This continues until the D line connected to $\overline{NW}$ goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SICP.

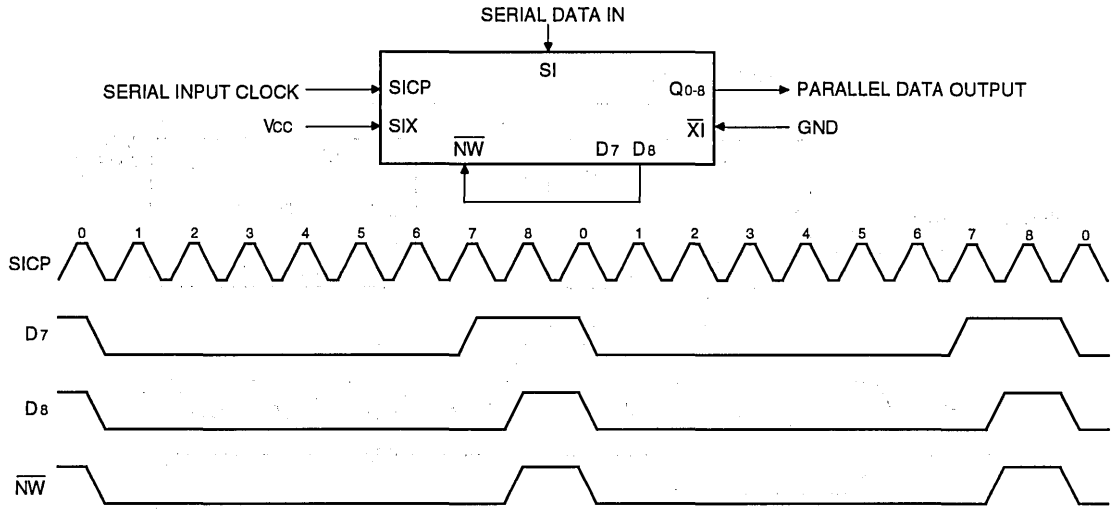


Figure 13. Nine-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SIX line of the least significant device HIGH and the SIX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SICP, both the Data Set lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant.

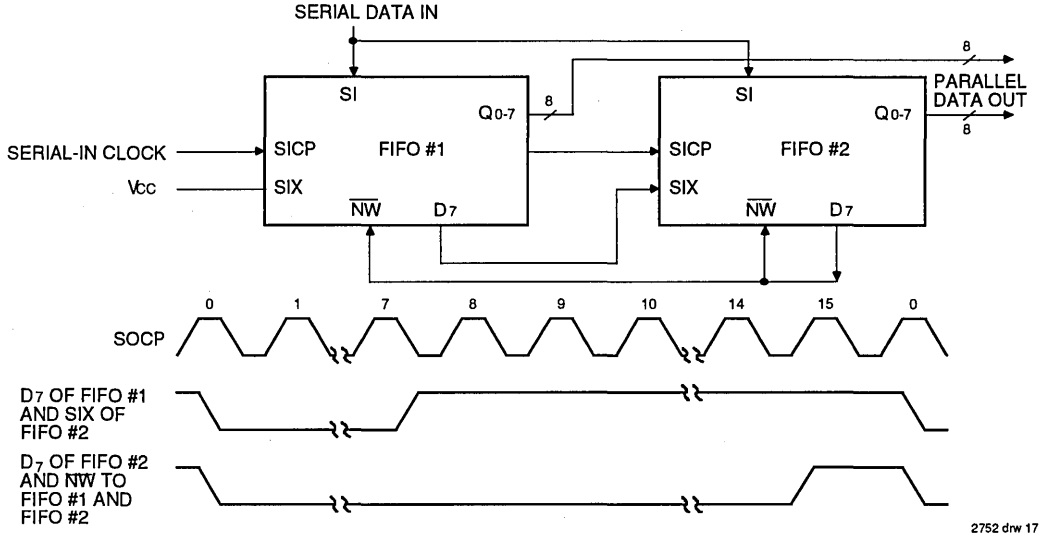


Figure 14. Serial-In to Parallel-Out Data of 16 Bits

Depth Expansion (Daisy Chain) Mode

The IDT72132/42 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 15 demonstrates Depth Expansion using three IDT72132/42. Any depth can be attained by adding additional IDT72132/42 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin and Expansion In ($\overline{XI}$) pin of each device must be tied together.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite ($\overline{FF}$) or ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag (HF) are not available in the Depth Expansion mode.

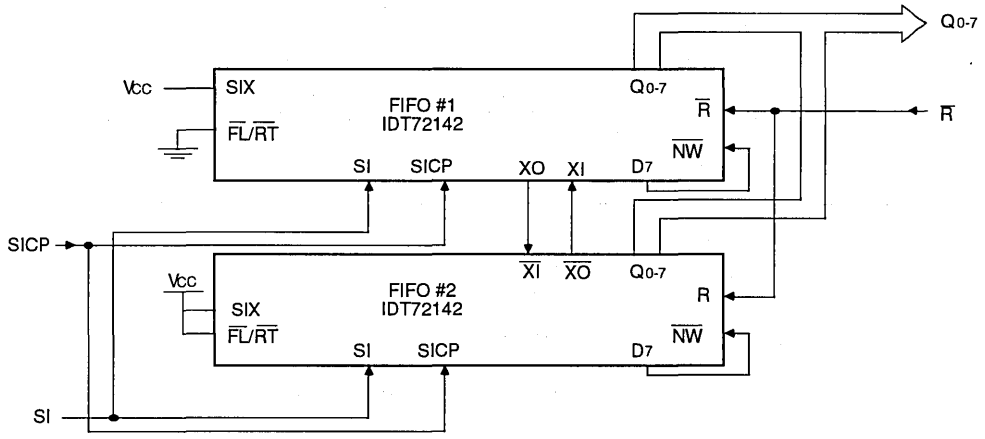


Figure 15. An 8K x 8 Serial-In Parallel-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION

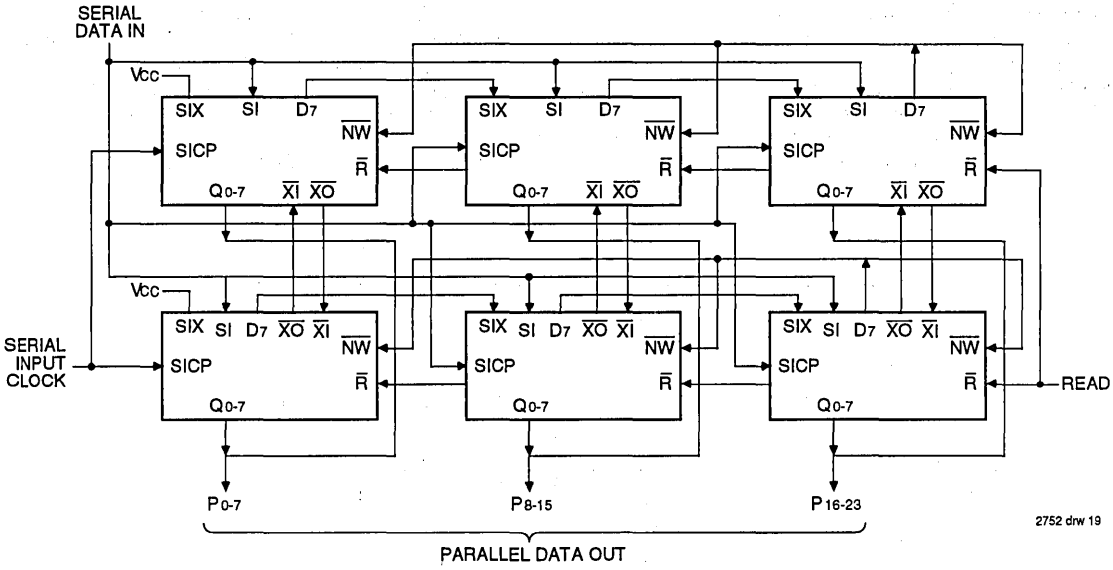


Figure 16. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72142s

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 64 x 8-BIT, 256 x 8-BIT, 512 x 8-BIT, 1024 x 8-BIT, 2048 x 8-BIT & 4096 x 8-BIT

IDT72420
IDT72200
IDT72210
IDT72220
IDT72230
IDT72240

FEATURES:

- 64 x 8-bit organization (IDT72420)
- 256 x 8-bit organization (IDT72200)
- 512 x 8-bit organization (IDT72210)
- 1024 x 8-bit organization (IDT72220)
- 2048 x 8-bit organization (IDT72230)
- 4096 x 8-bit organization (IDT72240)
- 15ns read/write cycle time (IDT72420/72200/72210)
- 20ns read/write cycle time (IDT72220/72230/72240)
- Read and write clocks can be asynchronous or coincident
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Almost-empty and almost-full flags set to Empty+7 and Full-7, respectively
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in 28-pin 300 mil plastic DIP and 300 mil ceramic DIP
- For surface mount product please see the IDT72421/72201/72211/72221/72231/72241 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72420/72200/72210/72220/72230/72240 SyncFIFO™ are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72420/72200/72210/72220/72230/72240 have a 64, 256, 512, 1024, 2048, and 4096 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, local area networks (LANs), and interprocessor communication.

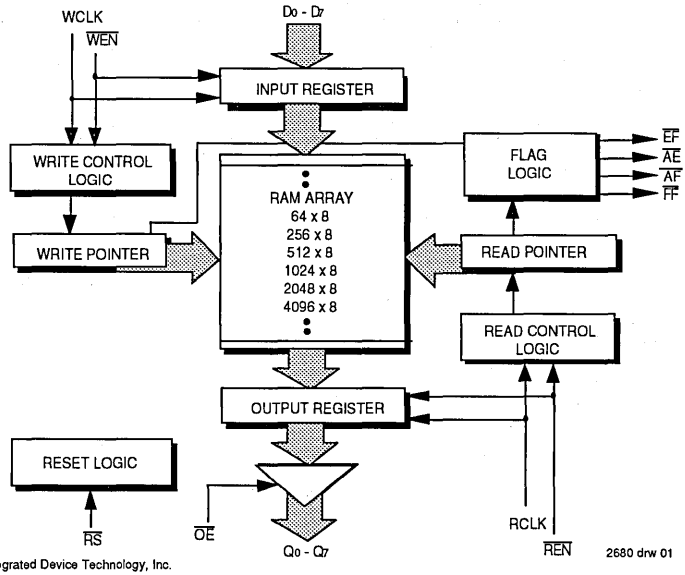
These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a write enable pin ($\overline{WEN}$). Data is read into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

These Synchronous FIFOs have two end-point flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two partial flags, Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$), are provided for improved system control. The partial ($\overline{AE}$) flags are set to Empty+7 and Full-7 for $\overline{AE}$ and $\overline{AF}$ respectively.

The IDT72420/72200/72210/72220/72230/72240 are fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM



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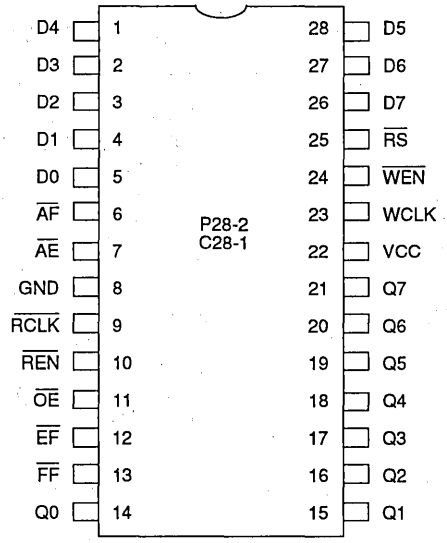
PIN CONFIGURATION



DIP TOP VIEW

2680 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0 - D_7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
Q_0 - Q_7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{AE}$	Almost-Empty Flag	O	When $\overline{AE}$ is LOW, the FIFO is almost empty based on the offset Empty+7. $\overline{AE}$ is synchronized to RCLK.
$\overline{AF}$	Almost-Full Flag	O	When $\overline{AF}$ is LOW, the FIFO is almost full based on the offset Full-7. $\overline{AF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
V_{CC}	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2680 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	–55 to + 125	°C
T_{BIAS}	Temperature Under Bias	–55 to + 125	–65 to + 135	°C
T_{STG}	Storage Temperature	–55 to + 125	–65 to + 135	°C
I_{OUT}	DC Output Current	50	50	mA

2680 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

2680 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1, 2)	Output Capacitance	V_{OUT} = 0V	10	pF

2680 tbl 04

NOTES:

1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72420 IDT72200 IDT72210 Commercial t_{CLK} = 15, 20, 25,35, 50 ns Min.	Typ.	Max.	IDT72420 IDT72200 IDT72210 Military t_{CLK} = 20, 25,35, 50 ns Min.	Typ.	Max.	Units
I_{LI}(1)	Input Leakage Current (any input)	-1	—	1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	140	—	—	160	mA

2680 tbl 05

Symbol	Parameter	IDT72220 IDT72230 IDT72240 Commercial t_{CLK} = 20, 25, 35, 50 ns Min.	Typ.	Max.	IDT72220 IDT72230 IDT72240 Military t_{CLK} = 25, 35, 50 ns Min.	Typ.	Max.	Units
I_{LI}(1)	Input Leakage Current (any input)	-1	—	1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(4)	Active Power Supply Current	—	—	160	—	—	180	mA

2680 tbl 06

NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.

3 & 4. Measurements are made with outputs open. Tested at f_{CLK} = 20 MHz.
(3) Typical I_{CC1} = 65 + (f_{CLK} * 1.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
(4) Typical I_{CC1} = 80 + (f_{CLK} * 2.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
f_{CLK} = 1 / t_{CLK}
C_L = external capacitive load (30 pF typical)

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

		Com'l.		Commercial & Military								
		IDT72200L15 IDT72210L15 IDT72420L15		IDT72200L20 IDT72210L20 IDT72420L20		IDT72200L25 IDT72210L25 IDT72420L25		IDT72200L35 IDT72210L35 IDT72420L35		IDT72200L50 IDT72210L50 IDT72420L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
t_A	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
t_{CLK}	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
t_{CLKH}	Clock High Time	6	—	8	—	10	—	14	—	20	—	ns
t_{CLKL}	Clock Low Time	6	—	8	—	10	—	14	—	20	—	ns
t_{DS}	Data Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{DH}	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{ENS}	Enable Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{ENH}	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{RS}	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Set-up Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	20	—	25	—	35	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	3	10	3	13	3	15	3	28	ns
t_{OHZ}	Output Enable to Output in High Z[2]	3	8	3	10	3	13	3	15	3	28	ns
t_{WFF}	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{REF}	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AF}	Write Clock to Almost-Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AE}	Read Clock to Almost-Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	12	—	15	—	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	28	—	35	—	40	—	42	—	45	—	ns

NOTES:

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1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72220L20 IDT72230L20 IDT72240L20 Min.	Max.	Commercial & Military IDT72220L25 IDT72230L25 IDT72240L25 Min.	Max.	IDT72220L35 IDT72230L35 IDT72240L35 Min.	Max.	IDT72220L50 IDT72230L50 IDT72240L50 Min.	Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	5	—	6	—	8	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	8	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	20	—	25	—	35	—	50	—	ns
tRSR	Reset Recovery Time	20	—	25	—	35	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	10	3	13	3	15	3	23	ns
tOHZ	Output Enable to Output in High Z[2]	3	10	3	13	3	15	3	23	ns
tWFF	Write Clock to Full Flag	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	12	—	15	—	20	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	35	—	40	—	42	—	45	—	ns

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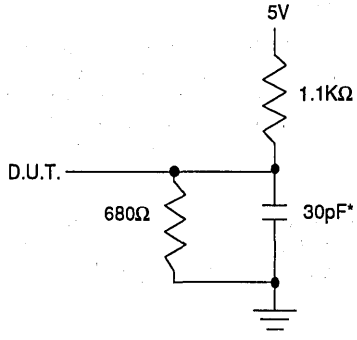
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2680 tbl 09



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or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_7) - Data inputs for 8-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) - Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Almost Empty Flag ($\overline{AE}$) will be reset to low after t_{RSF}. During reset, the output register is initialized to all zeros.

Write Clock (WCLK) - A write cycle is initiated on the low-to-high transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the low-to-high transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) are synchronized with respect to the low-to-high transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable ($\overline{WEN}$) - When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

Read Clock (RCLK) - Data can be read on the outputs on the low-to-high transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) are synchronized with respect to the low-to-high transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enable ($\overline{REN}$) - When Read Enable ($\overline{REN}$) is low, data is read from the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a valid read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) - When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

OUTPUTS:

Full Flag ($\overline{FF}$) - The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 64 writes for the IDT72420, 256 writes for the IDT72200, 512 writes for the IDT72210, 1024 writes for the IDT72220, 2048 writes for the IDT72230, and 4096 writes for the IDT72240.

The Full Flag ($\overline{FF}$) is synchronized with respect to the low-to-high transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) - The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the low-to-high transition of the read clock (RCLK).

Almost Full Flag ($\overline{AF}$) - The Almost Full Flag ($\overline{AF}$) will go low when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Full Flag ($\overline{AF}$) will go low after 57 writes for the IDT72420, 249 writes for the IDT72200, 505 writes for the IDT72210, 1017 writes for the IDT72220, 2041 writes for the IDT72230 and 4089 writes for the IDT72240.

The Almost Full Flag ($\overline{AF}$) is synchronized with respect to the low-to-high transition of the write clock (WCLK).

Almost Empty Flag ($\overline{AE}$) - The Almost Empty Flag ($\overline{AE}$) will go low when the FIFO reaches the Almost-Empty condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Empty Flag ($\overline{AE}$) will go high after 8 writes for the IDT72420, IDT72200, IDT72210, IDT72220, IDT72230 and IDT72240.

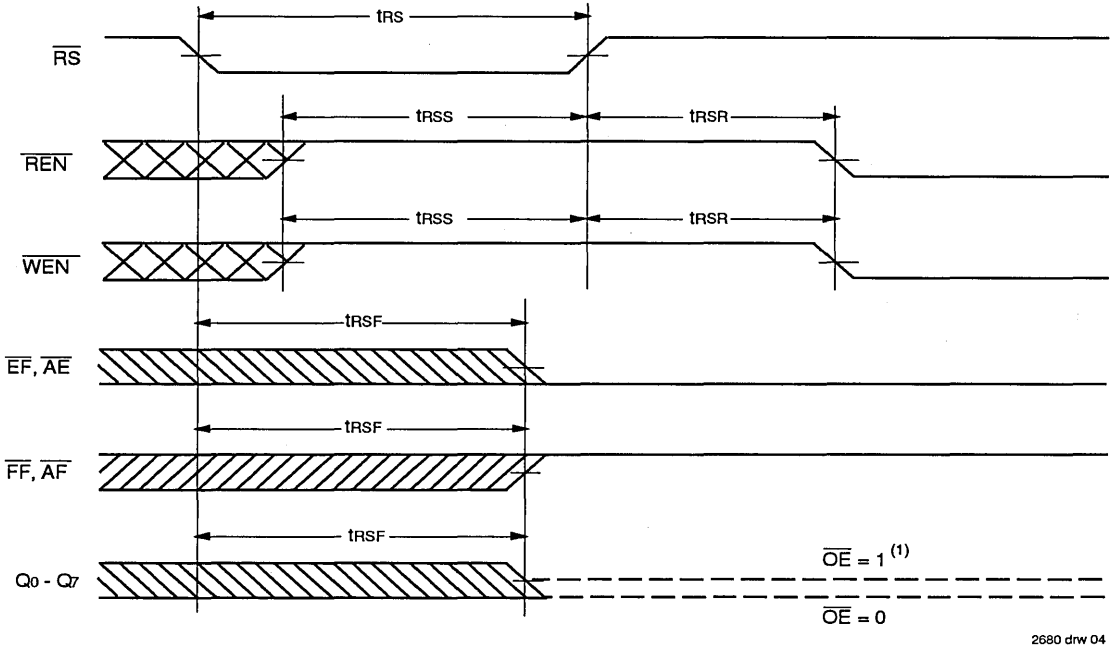
The Almost Empty Flag ($\overline{AE}$) is synchronized with respect to the low-to-high transition of the read clock (RCLK).

Data Outputs (Q_0 - Q_7) - Data outputs for a 8-bit wide data.

TABLE 1: STATUS FLAGS

Number of Words In FIFO									
IDT72420	IDT72200	IDT72210	IDT72220	IDT72230	IDT72240	$\overline{FF}$	$\overline{AF}$	$\overline{AE}$	$\overline{EF}$
0	0	0	0	0	0	H	H	L	L
1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	H	H	L	H
8 to 56	8 to 248	8 to 504	8 to 1016	8 to 2040	8 to 4088	H	H	H	H
57 to 63	249 to 255	505 to 511	1017 to 1023	2041 to 2047	4089 to 4095	H	L	H	H
64	256	512	1024	2048	4096	L	L	H	H

2680 tbl 10



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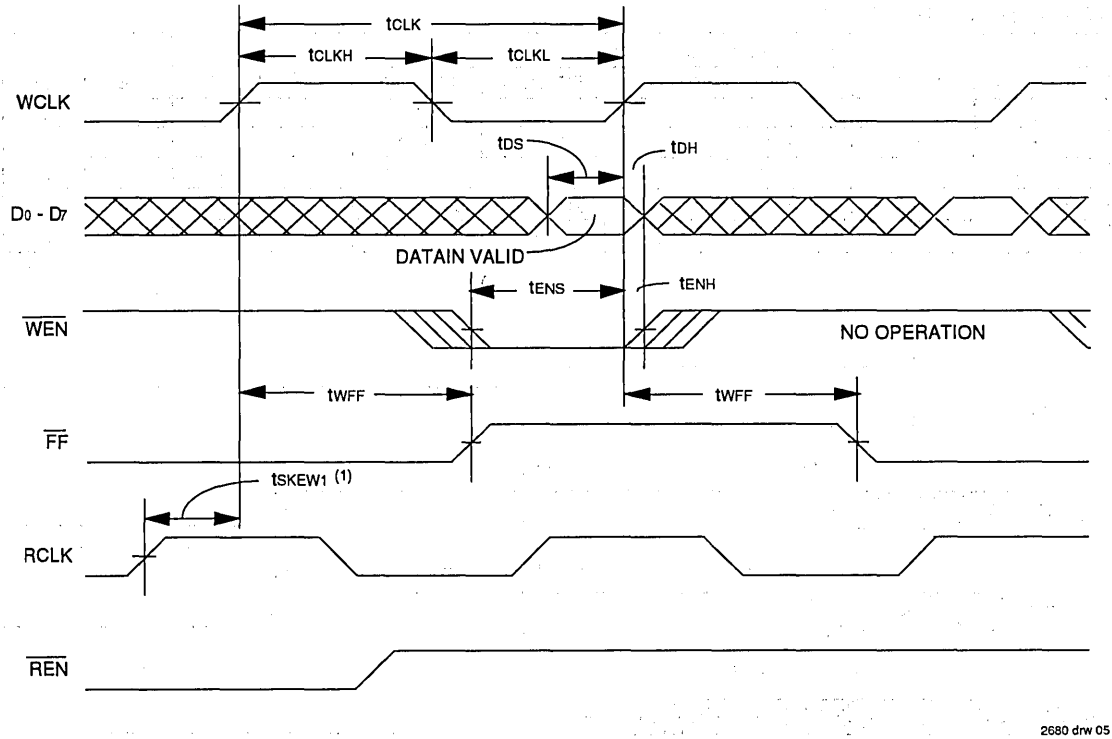
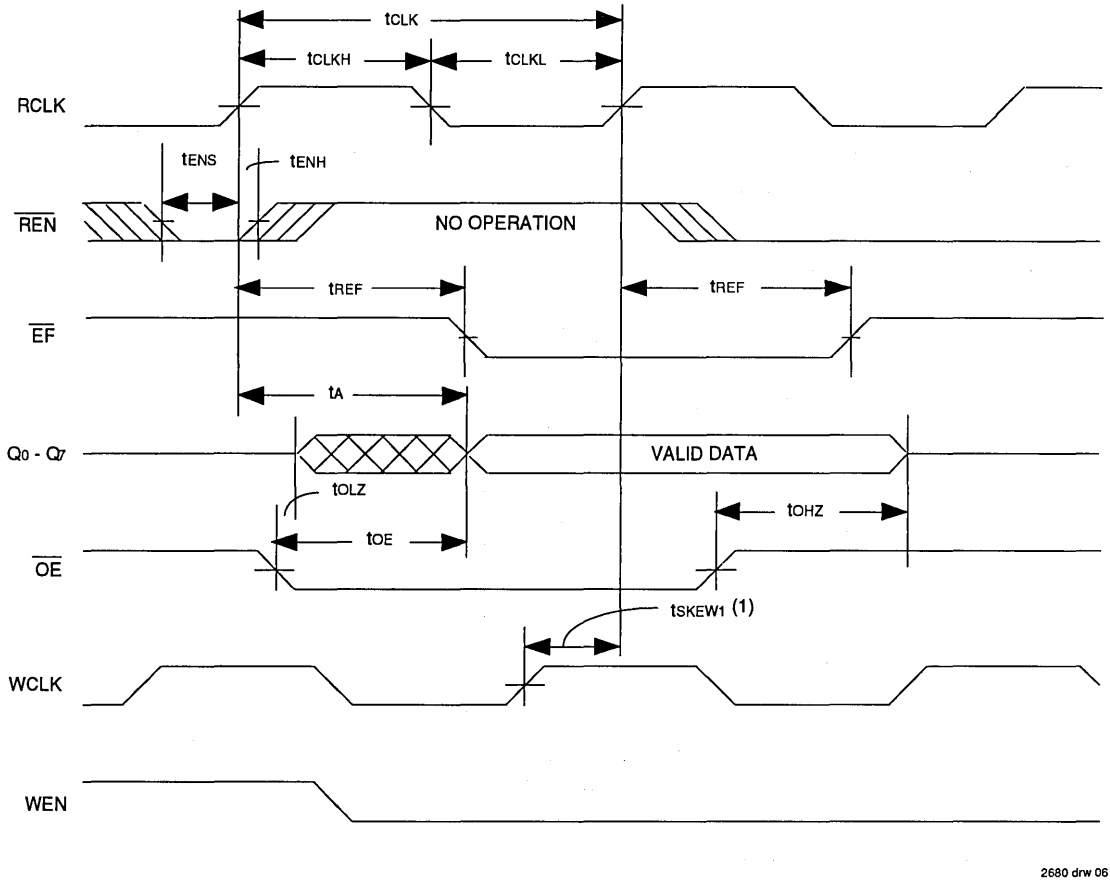
NOTE:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 2. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 3. Write Cycle Timing



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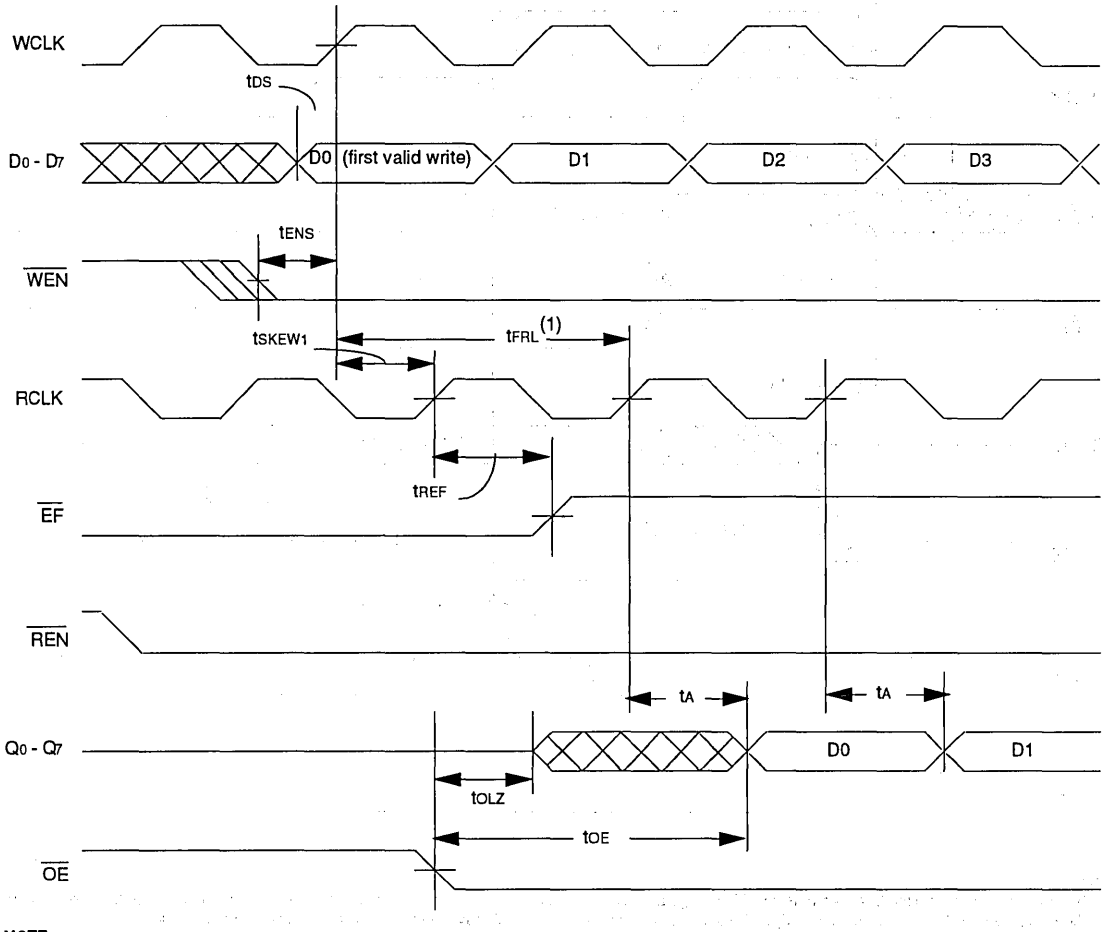
NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 4. Read Cycle Timing

5



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

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Figure 5. First Data Word Latency Timing

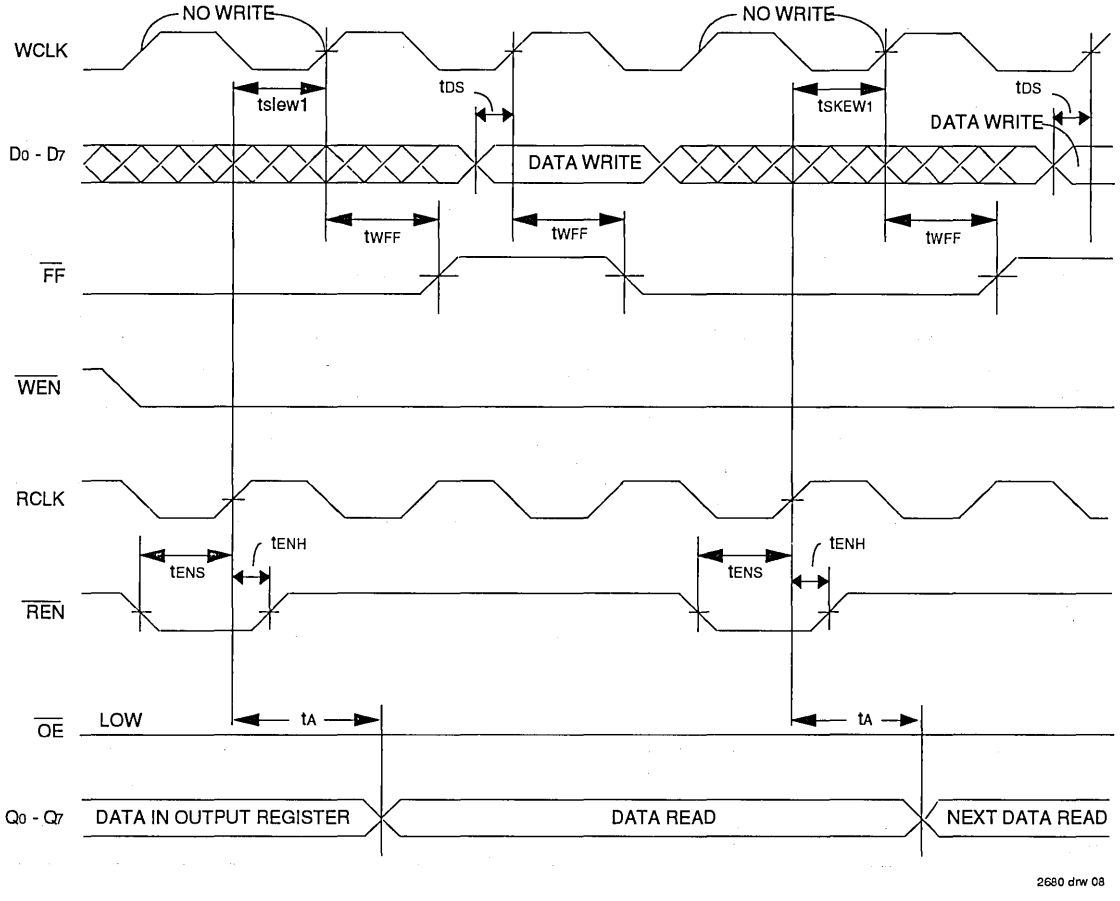
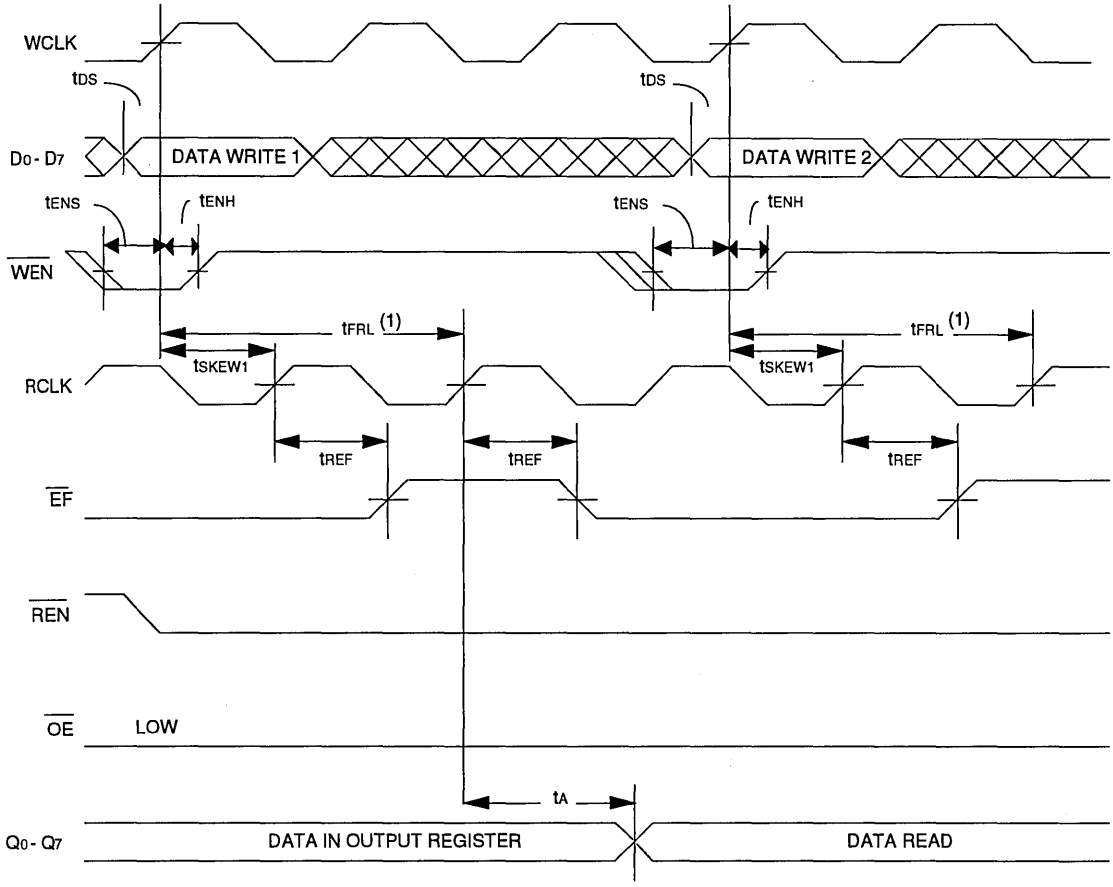


Figure 6. Full Flag Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

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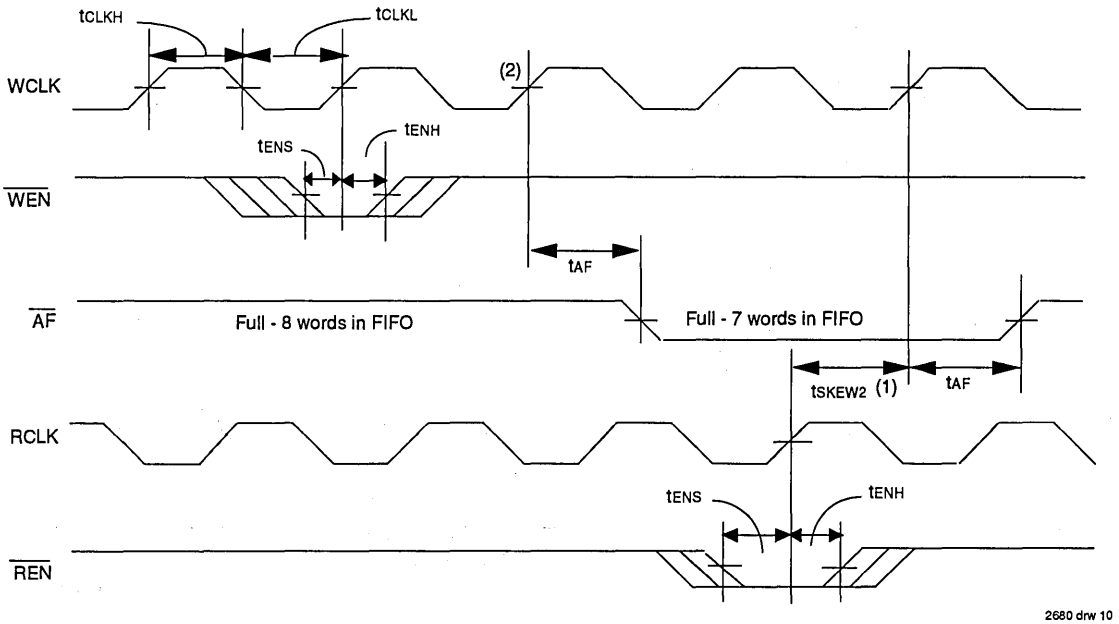
Figure 7. Empty Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{AF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{AF}$ may not change state until the next WCLK edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - 6 words in the FIFO when $\overline{AF}$ goes low.

Figure 8. Almost Full Flag Timing

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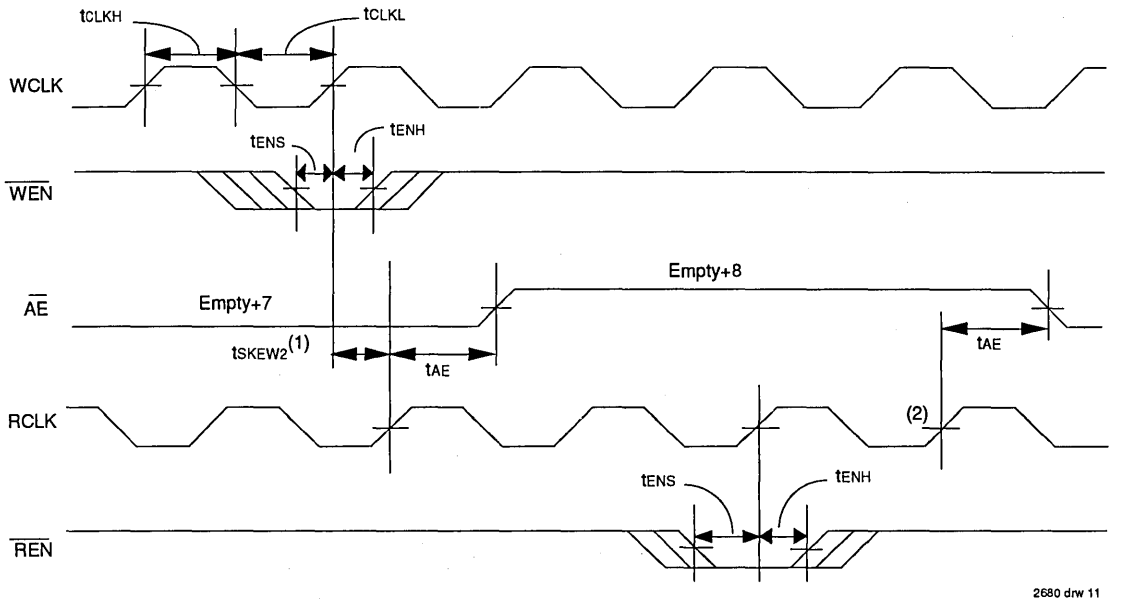

NOTES:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{AE}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{AE}$ may not change state until the next RCLK edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty - 6 words in the FIFO when $\overline{AE}$ goes low.

Figure 9. Almost Empty Flag Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72420/72200/72210/72220/72230/72240 may be used when the application requirements are for 64/256/512/1024/2048/4096 words or less. See Figure 10.

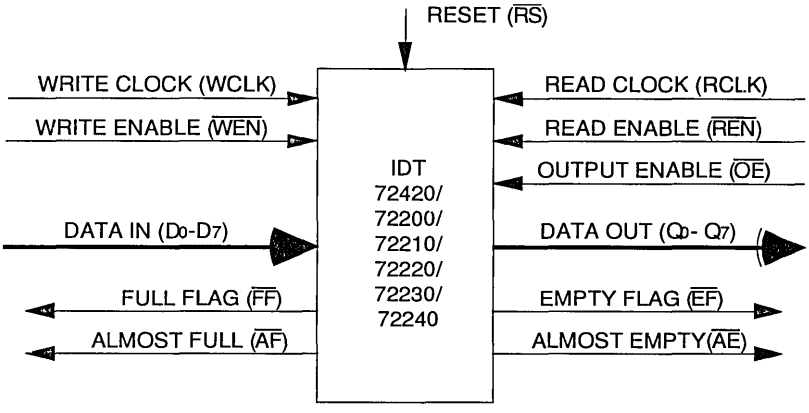

Figure 10. Block Diagram of Single 64 x 8/256 x 8/512 x 8/1024 x 8/2048 x 8/4096 x 8 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags (EF and FF) The partial status flags (AE and AF) can be detected from any one device. Figure 11 demonstrates a 16-bit word width by using two IDT72420/72200/72210/72220/72230/72240s. Any word width can be attained by adding additional IDT72420/72200/72210/72220/72230/72240s.

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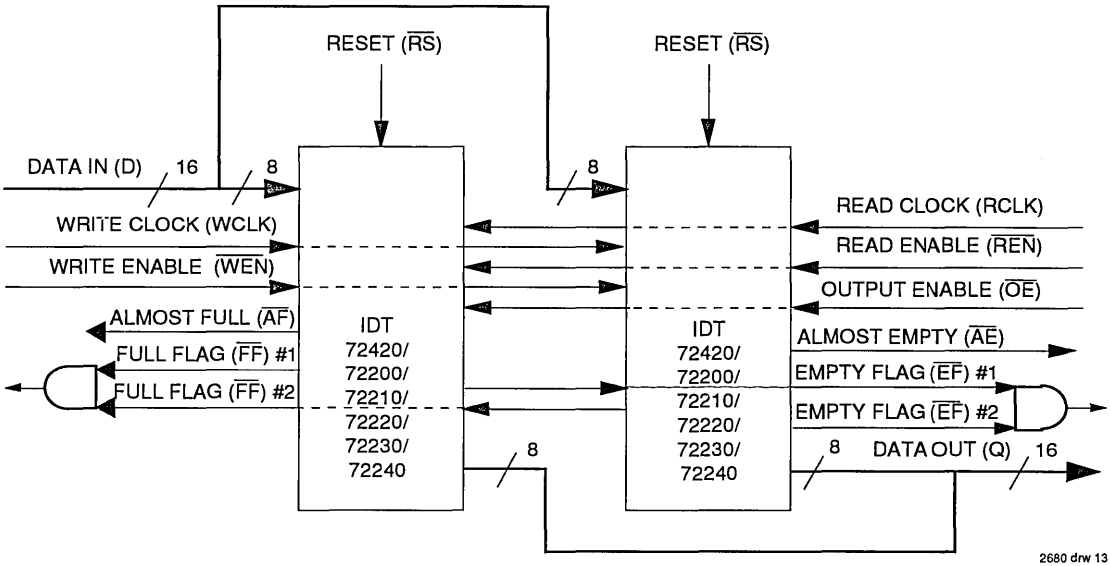


Figure 11. Block Diagram of 64 x 16/256 x 16/512 x 16/1024 x 16/2048 x 16/4096 x 16 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72420/72200/72210/72220/72230/72240 can be adapted to applications when the requirements are for greater than 64/256/512/1024/2048/4096 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner.

Please see the Application Note "DEPTH EXPANSION IDT'S SYNCHRONOUS FIFOs USING RING COUNTER APPROACH" for details of this configuration.

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 64 X 9-BIT, 256 x 9-BIT, 512 x 9-BIT, 1024 X 9-BIT, 2048 X 9-BIT & 4096 x 9-BIT

IDT72421
IDT72201
IDT72211
IDT72221
IDT72231
IDT72241

FEATURES:

- 64 x 9-bit organization (IDT72421)
- 256 x 9-bit organization (IDT72201)
- 512 x 9-bit organization (IDT72211)
- 1024 x 9-bit organization (IDT72221)
- 2048 x 9-bit organization (IDT72231)
- 4096 x 9-bit organization (IDT72241)
- 15ns read/write cycle time (IDT72421/72201/72211)
- 20ns read/write cycle time (IDT72221/72231/72241)
- Read and write clocks can be independent
- Dual-ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be set to any depth
- Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively
- Output enable puts output data bus in high impedance state
- Advanced submicron CEMOS™ technology
- Available in 32-pin plastic leaded chip carrier (PLCC) and ceramic leadless chip carrier (LCC)
- For Through-Hole product please see the IDT72420/72200/72210/72220/72230/72240 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72421/72201/72211/72221/72231/72241 SyncFIFO™ are very high-speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72421/72201/72211/72221/72231/72241 have a 64, 256, 512, 1024, 2048, and 4096 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks and interprocessor communication.

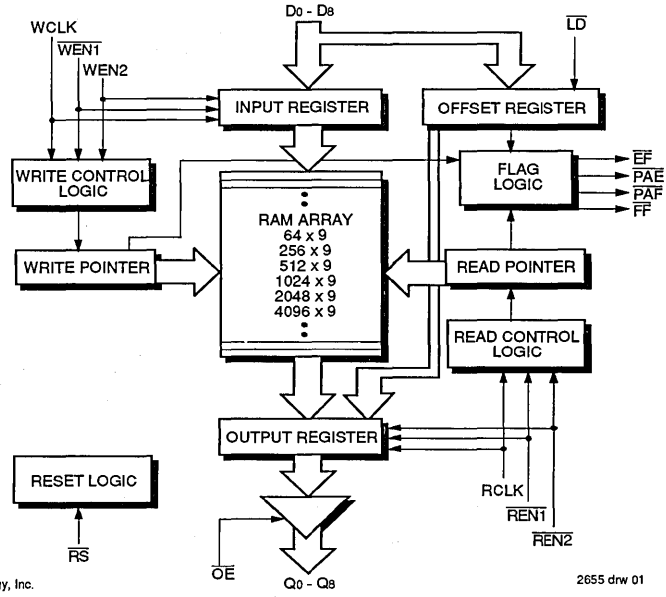
These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is read into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$).

The IDT72421/72201/72211/72221/72231/72241 are fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM



2655 drw 01

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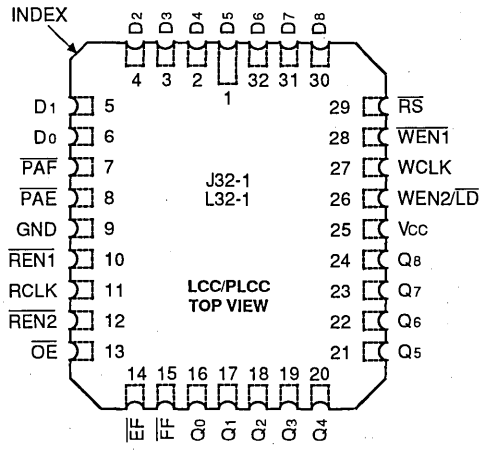
PIN CONFIGURATION



2655 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2/ Load	I	The FIFO is configured at reset to have either two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
Q0-Q8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are asserted.
$\overline{REN1}$	Read Enable 1	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{REN2}$	Read Enable 2	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
VCC	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2655 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

2655 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

2655 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

2655 tbl 04

NOTES:
1. With output deselected ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72421 IDT72201 IDT72211 Commercial t_{CLK} = 15, 20, 25,35, 50ns Min.	Typ.	Max.	IDT72421 IDT72201 IDT72211 Military t_{CLK} = 20, 25,35, 50ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	140	—	—	160	mA

2655 tbl 05

Symbol	Parameter	IDT72221 IDT72231 IDT72241 Commercial t_{CLK} = 20, 25, 35, 50ns Min.	Typ.	Max.	IDT72221 IDT72231 IDT72241 Military t_{CLK} = 25, 35, 50ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(4)	Active Power Supply Current	—	—	160	—	—	180	mA

2655 tbl 06

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3 & 4. Measurements are made with outputs open. Tested at f_{CLK} = 20MHz.
(3) Typical I_{CC1} = 65 + (f_{CLK} * 1.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
(4) Typical I_{CC1} = 80 + (f_{CLK} * 2.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
f_{CLK} = 1/t_{CLK}.
C_L = external capacitive load (30pF typical)

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72421L15 IDT72201L15 IDT72211L15		Commercial & Military IDT72421L20 IDT72201L20 IDT72211L20		IDT72421L25 IDT72201L25 IDT72211L25		IDT72421L35 IDT72201L35 IDT72211L35		IDT72421L50 IDT72201L50 IDT72211L50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
t_A	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
t_{CLK}	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
t_{CLKH}	Clock High Time	6	—	8	—	10	—	14	—	20	—	ns
t_{CLKL}	Clock Low Time	6	—	8	—	10	—	14	—	20	—	ns
t_{DS}	Data Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{DH}	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{ENS}	Enable Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{ENH}	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{RS}	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Set-up Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	20	—	25	—	35	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	3	10	3	13	3	15	3	28	ns
t_{OHZ}	Output Enable to Output in High Z[2]	3	8	3	10	3	13	3	15	3	28	ns
t_{WFF}	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{REF}	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AF}	Write Clock to Almost-Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AE}	Read Clock to Almost-Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	12	—	15	—	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	28	—	35	—	40	—	42	—	45	—	ns

NOTES:

2655 tbl 07

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Com'l. IDT72221L20 IDT72231L20 IDT72241L20 Min.	Max.	Commercial and Military IDT72221L25 IDT72231L25 IDT72241L25 Min.	Max.	IDT72221L35 IDT72231L35 IDT72241L35 Min.	Max.	IDT72221L50 IDT72231L50 IDT72241L50 Min.	Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	5	—	6	—	8	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	8	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	20	—	25	—	35	—	50	—	ns
tRSR	Reset Recovery Time	20	—	25	—	35	—	50	—	ns
tRSF	Reset to Flag Time and Output Time	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	10	3	13	3	15	3	28	ns
tOHZ	Output Enable to Output in High Z[2]	3	10	3	13	3	15	3	28	ns
tWFF	Write Clock to Full Flag	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	—	30	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	12	—	15	—	20	—	30	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	35	—	40	—	42	—	45	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

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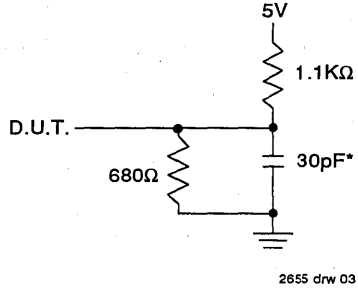
AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2655 tbl 09



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or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_8) — Data inputs for 9-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$) — If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is low, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN1}$, $\overline{REN2}$) — When both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are low, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When either Read Enable ($\overline{REN1}$, $\overline{REN2}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a valid read can begin. The Read Enables ($\overline{REN1}$, $\overline{REN2}$) are ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) — When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

Write Enable 2/Load (WEN2/$\overline{LD}$) — This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set low at Reset ($\overline{RS}$=low), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is low and Write Enable 2/Load (WEN2/$\overline{LD}$) is high, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is high and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is low, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set low at Reset ($\overline{RS}$=low). The IDT72421/72201/72211/72221/72231/72241 devices contain four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set low, data on the inputs D is written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low, and Write Enable 1 ($\overline{WEN1}$) is low, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low and both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are set low. Data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

A read and write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN1}$	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

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NOTE:
1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

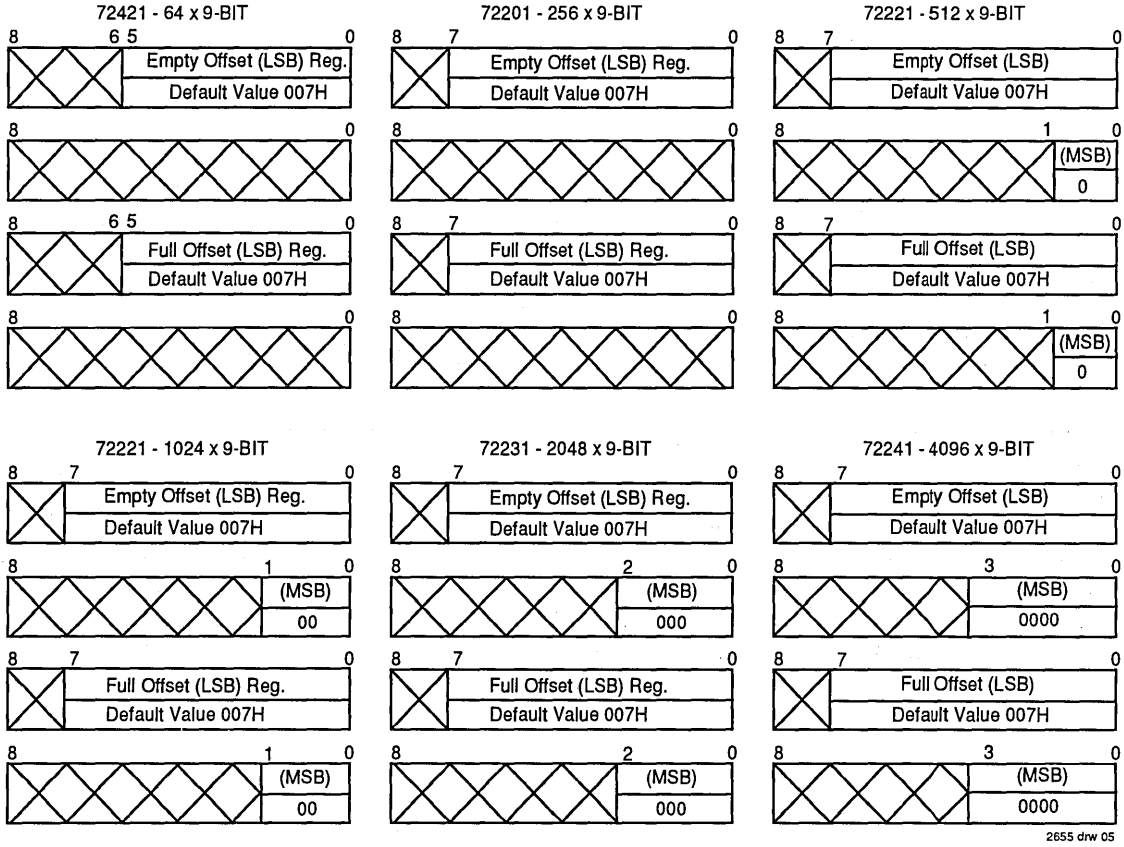

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Figure 3. Offset Register Location and Default Values

OUTPUTS:

Full Flag ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 64 writes for the IDT72421, 256 writes for the IDT72201, 512 writes for the IDT72211, 1024 writes for the IDT72221, 2048 writes for the IDT72231, and 4096 writes for the IDT72241.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$) — The Programmable Almost-Full Flag ($\overline{PAF}$) will go low when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full Flag ($\overline{PAF}$) will go low after (64-m) writes for the IDT72421, (256-m) writes for the IDT72201, (512-m) writes for the IDT72211, (1024-m) writes for the IDT72221, (2048-m) writes for the IDT72231, and (4096-m) writes for the IDT72241. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will go low at Full-7 words.

The Programmable Almost-Full Flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$) — The Programmable Almost-Empty Flag ($\overline{PAE}$) will go low when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag ($\overline{PAE}$) will go high after "n+1" for the IDT72421/72201/72211/72221/72231/72241.

If there is no Empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will go low at Empty+7 words.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q_0 - Q_8) — Data outputs for a 9-bit wide data.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO						
72421	72201	72211	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (64-(m+1))	(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	H	H	H	H
(64-m)[2] to 63	(256-m)[2] to 255	(512-m)[2] to 511	H	L	H	H
64	256	512	L	L	H	H

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NUMBER OF WORDS IN FIFO						
72221	72231	72241	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (1024-(m+1))	(n+1) to (2048-(m+1))	(n+1) to (4096-(m+1))	H	H	H	H
(1024-m)[2] to 1023	(2048-m)[2] to 2047	(4096-m)[2] to 4095	H	L	H	H
1024	2048	4096	L	L	H	H

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)

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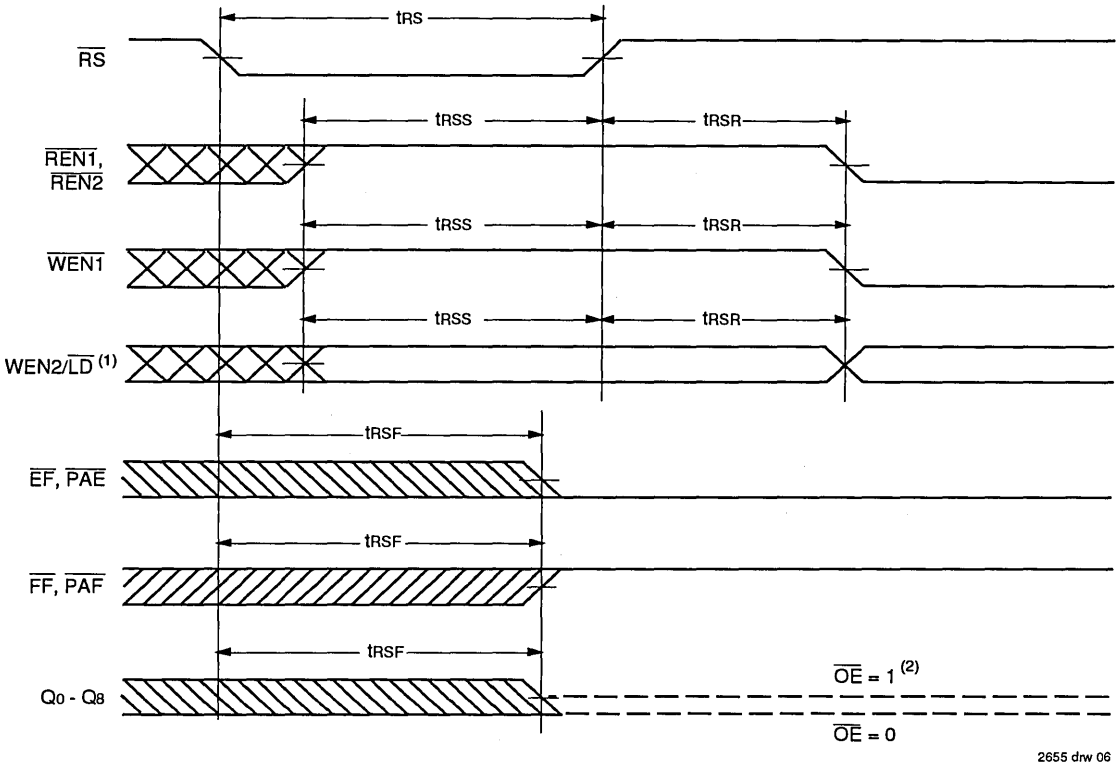
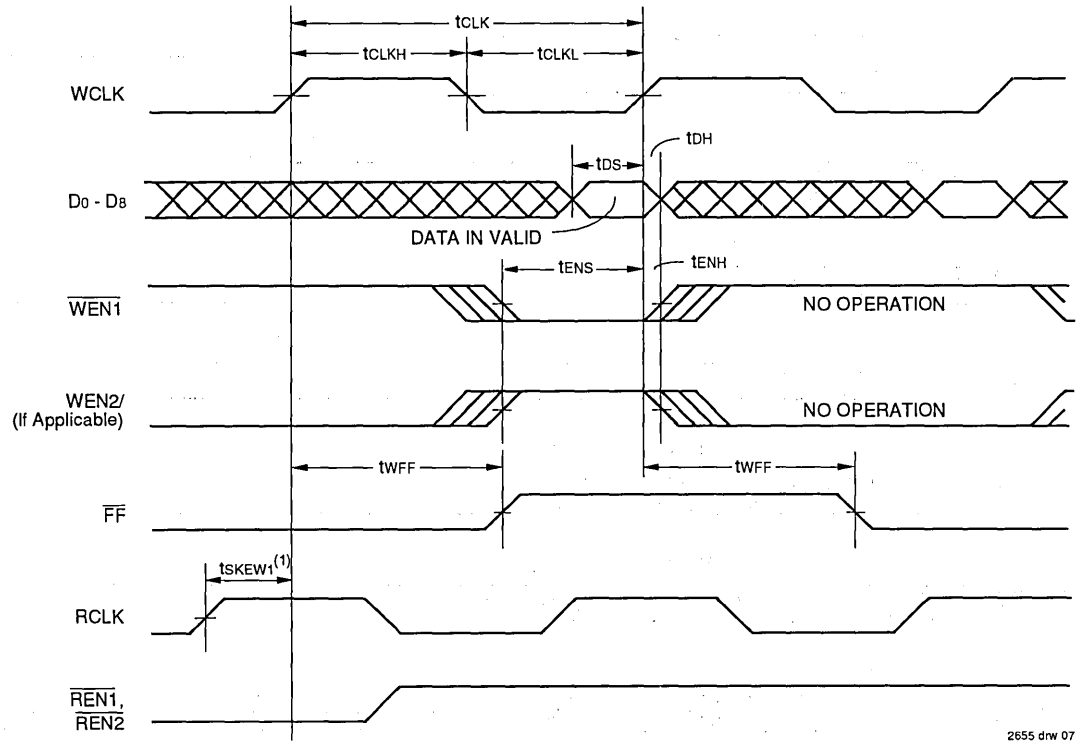


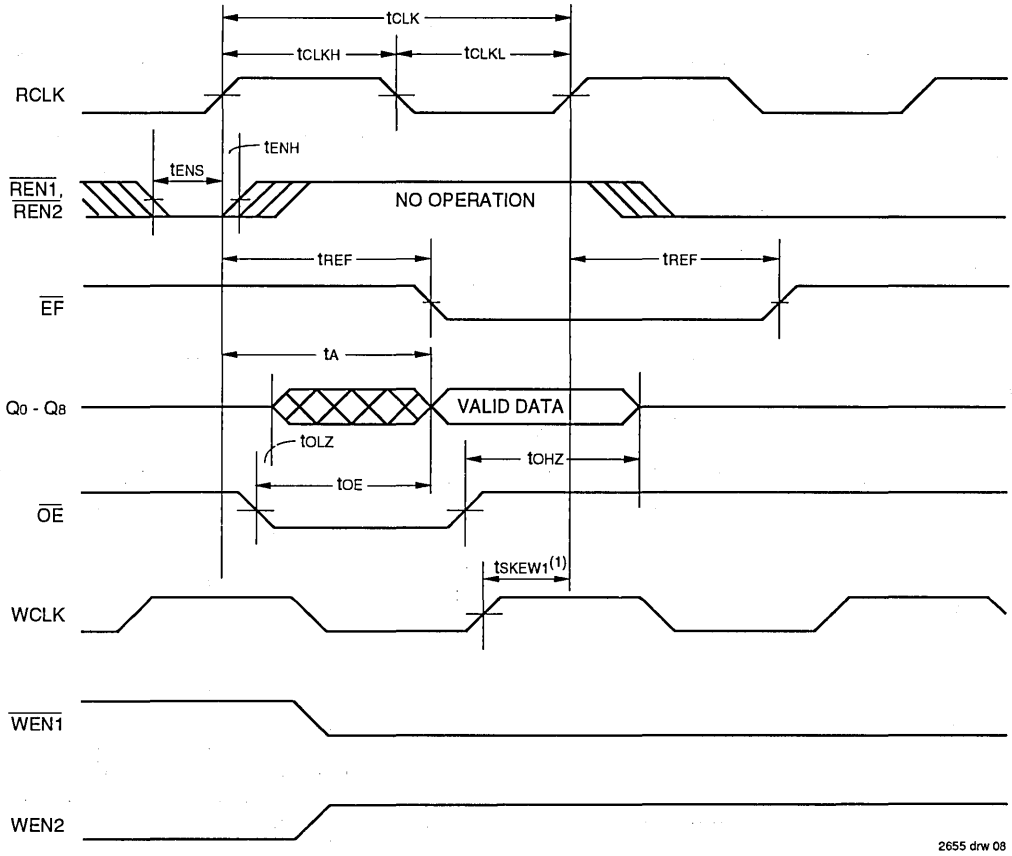
NOTES:
1. Holding WEN2/$\overline{LD}$ high during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ low during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running furing reset.

Figure 4. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

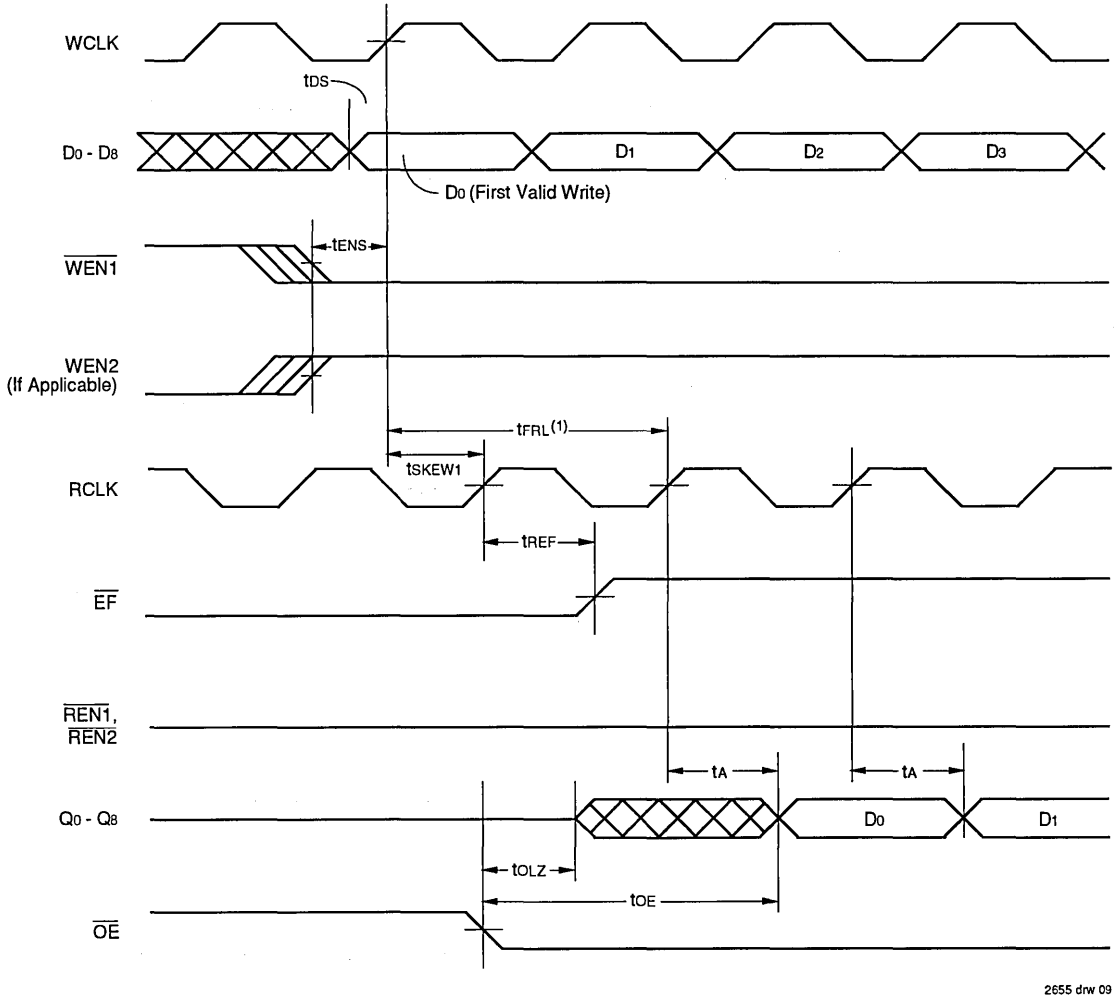
Figure 5. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 6. Read Cycle Timing

5



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing

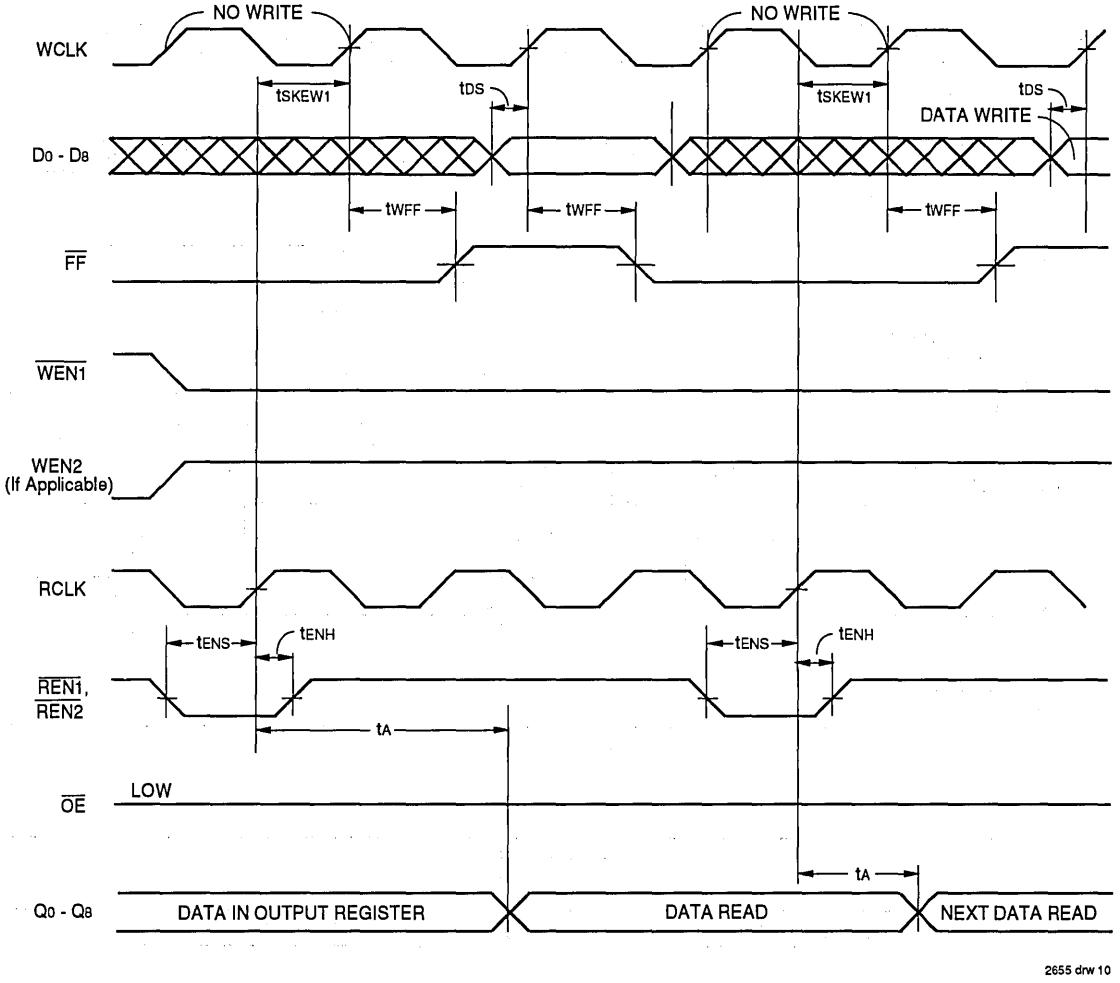


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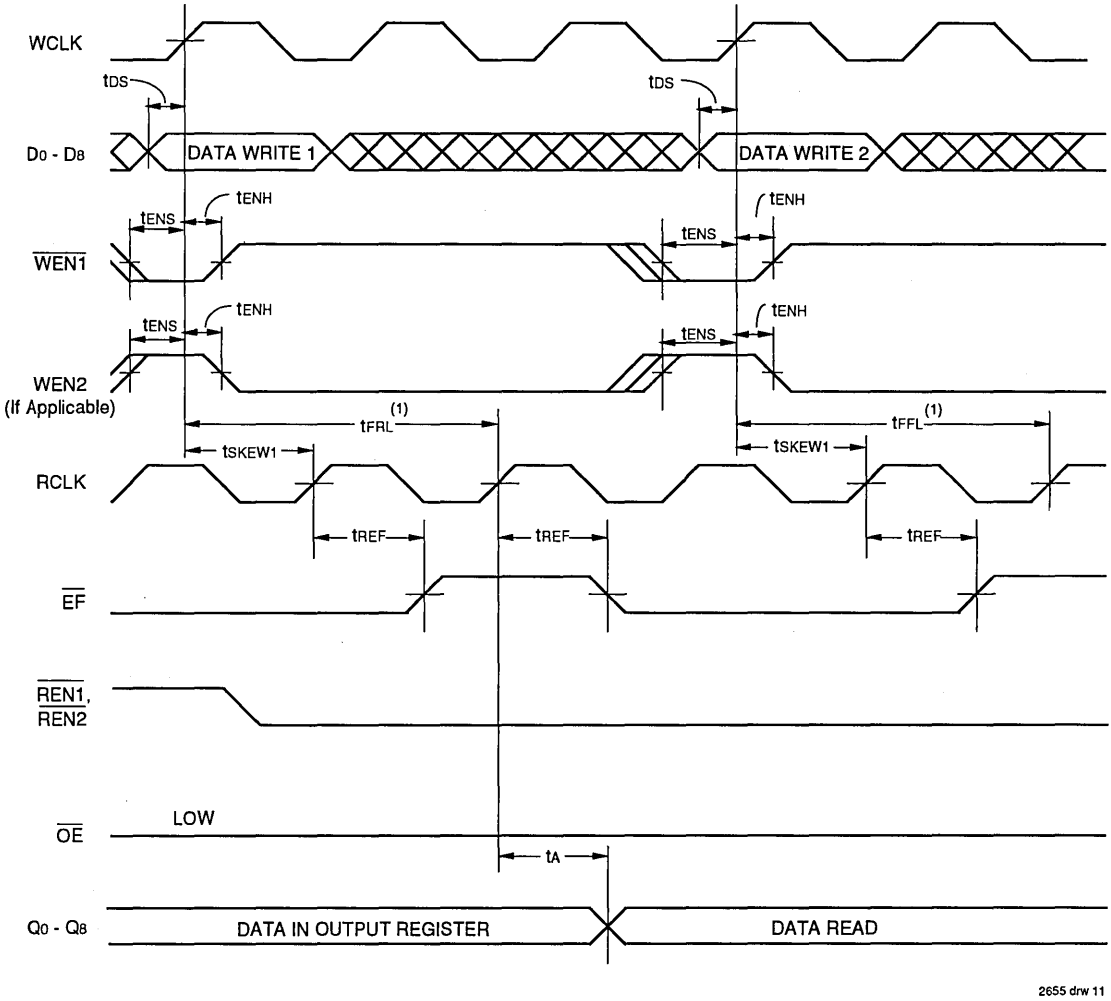
Figure 8. Full Flag Timing



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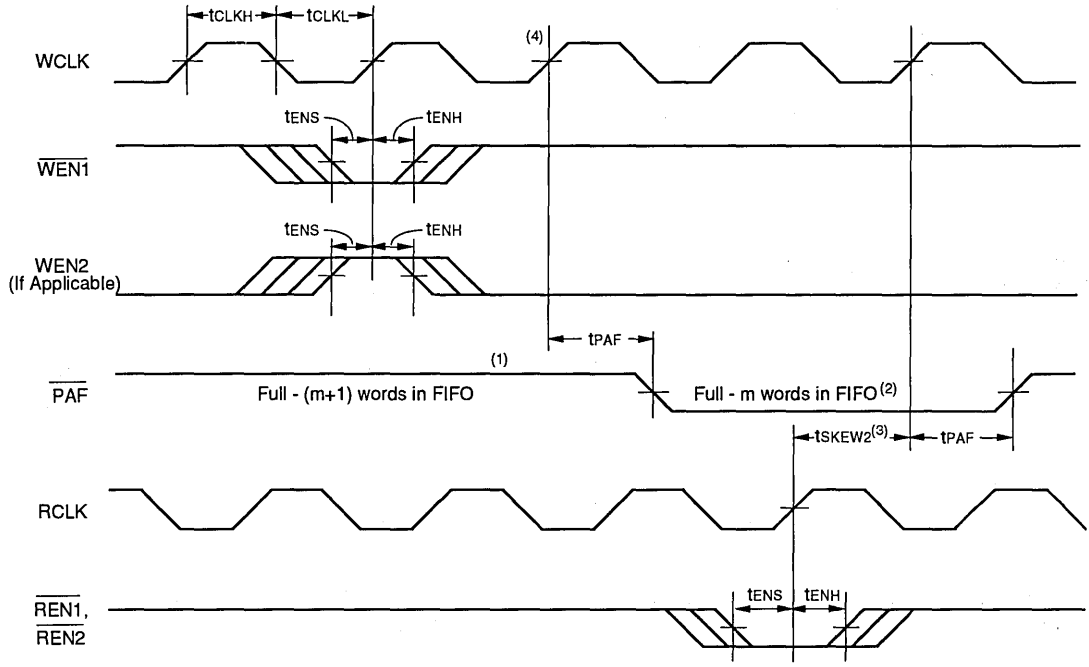
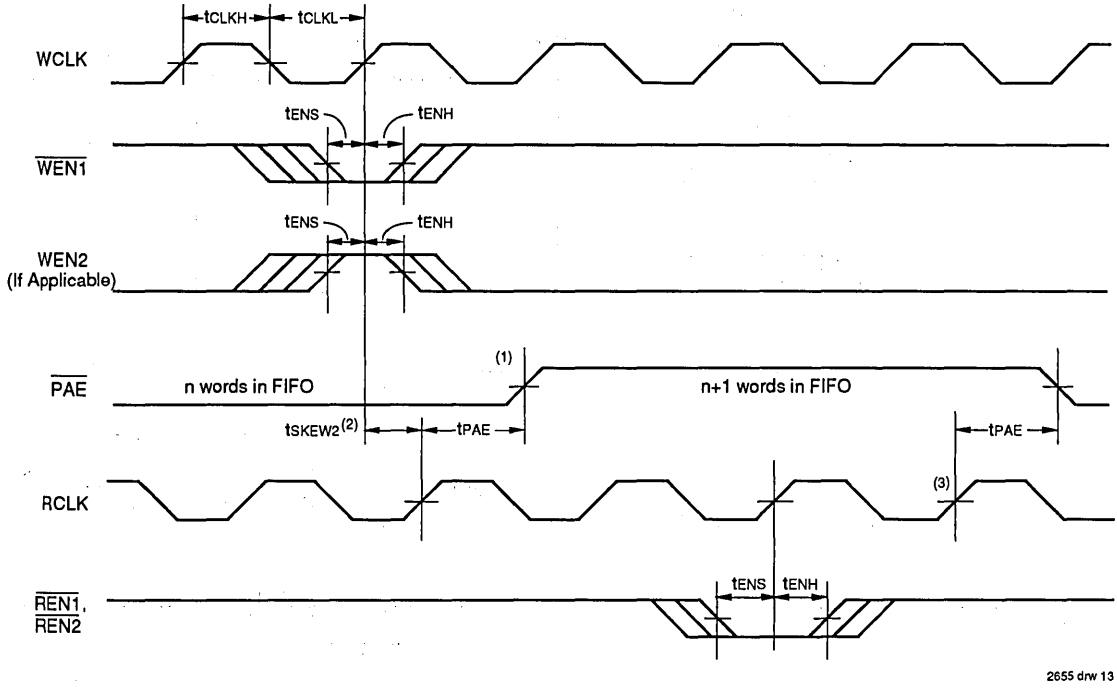
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. Empty Flag Timing



2655 drw 12

NOTES:
1. PAF offset = m.
2. 64 - m words in for IDT72421, 256 - m words in FIFO for IDT72201, 512 - m words for IDT72211, 1024 - m words for IDT72221, 2048 - m words for IDT72231, 4096 - m words for IDT72241.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes low.



NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes low.

Figure 11. Programmable Empty Flag Timing

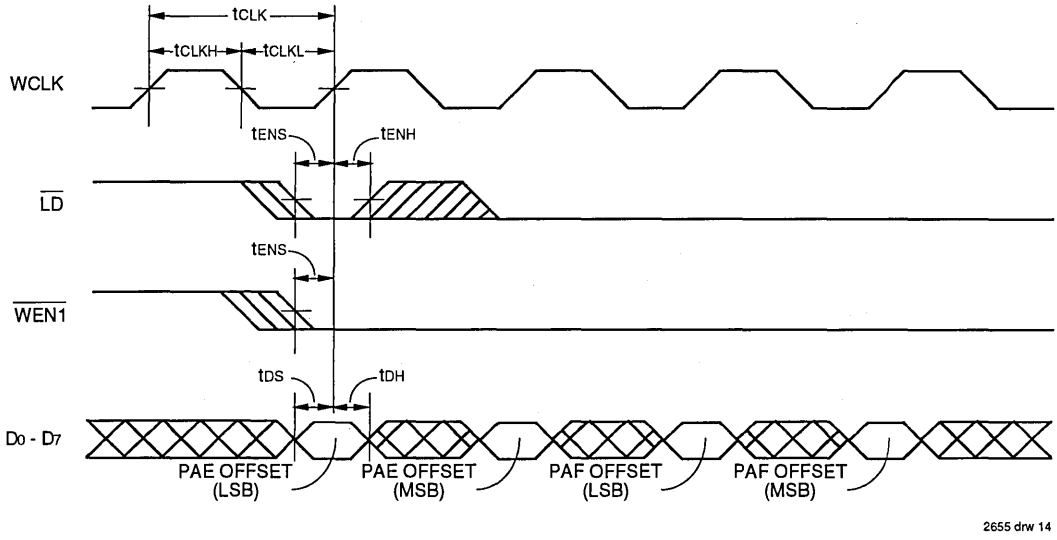


Figure 12. Write Offset Registers Timing

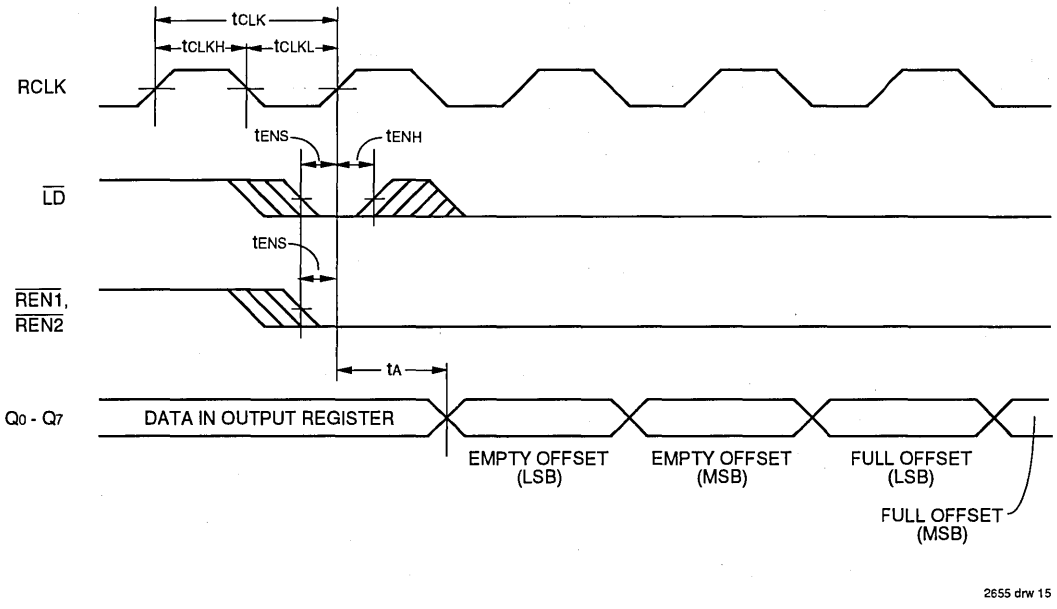


Figure 13. Read Offset Registers Timing

5

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72421/72201/72211/72221/72231/72241 may be used when the application requirements are for 64/256/512/1024/2048/4096 words or less. When the IDT72421/72201/72211/72221/72231/72241 are in a Single Device Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low at Reset so that the pin operates as a control to load and read the programmable flag offsets.

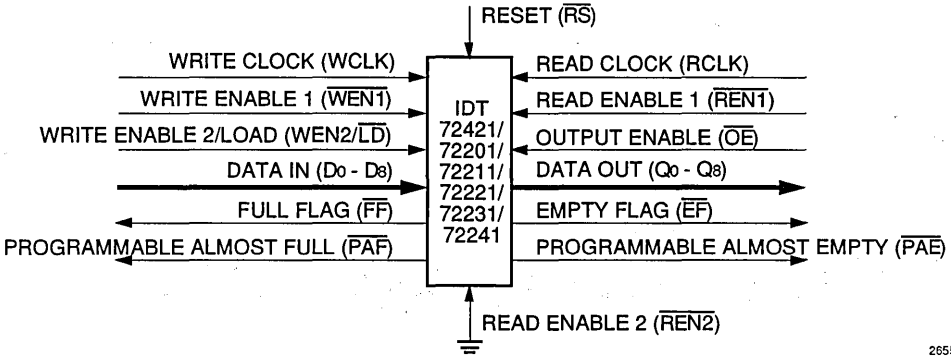


Figure 14. Block Diagram of Single 64 x 9/256 x 9/512 x 9/1024 x 9/2048 x 9/4096 x 9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{AE}$ and $\overline{AF}$) can be detected from any one device. Figure 15 demonstrates a 18-bit word width by using two IDT72421/72201/72211/72221/72231/72241s. Any word width can be attained by adding additional IDT72421/72201/72211/72221/72231/72241s.

When the IDT72421/72201/72211/72221/72231/72241 are in a Width Expansion Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low at Reset so that the pin operates as a control to load and read the programmable flag offsets.

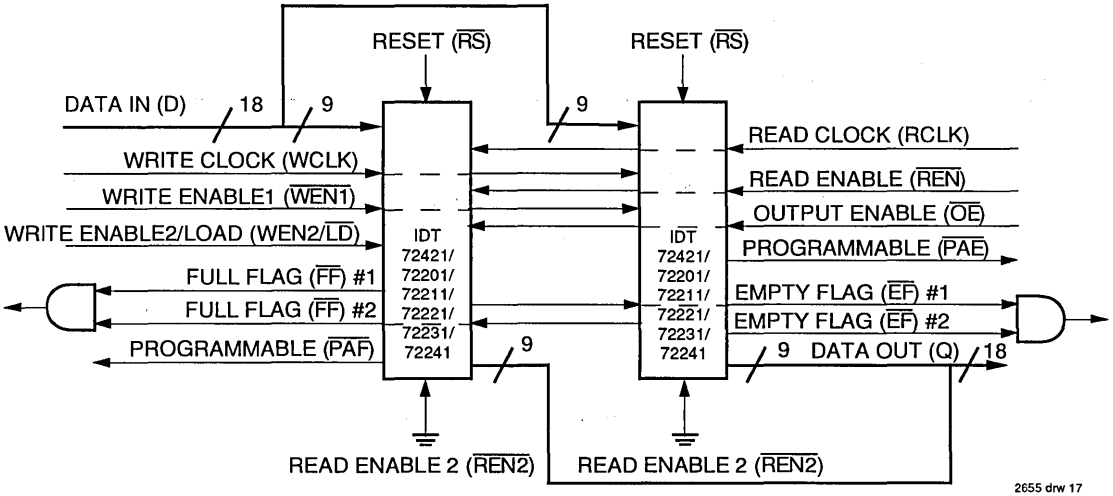


Figure 15. Block Diagram of 64 x 18/256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72421/7221/72211/72221/72231/72241 can be adapted to applications when the requirements are for greater than 64/256/512/1024/2048/4096 words. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT72421/7221/72211/72221/72231/72241 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held high during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

Please see the Applicatioin Note" DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

5

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 512 x 18-BIT & 1024 x 18-BIT

IDT72215L
IDT72225L

FEATURES

- 512 x 18-bit and 1024 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in width
- Read and write clocks can be independent or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead flatpack (FP), pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

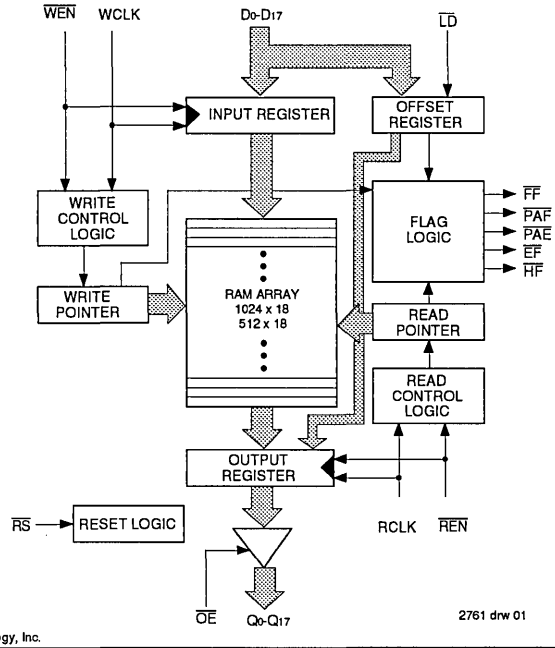
The IDT72215L and IDT72225L are very high speed, low-power first-in, first-out (FIFO) memories with read and write controls. The IDT72215L has a 512 x 18-bit memory array, while the IDT72225L has a 1024 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK) and a data input enable pin ($\overline{WEN}$). Data is written into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run independent of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The loading of the programmable flag offsets can be controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is also available.

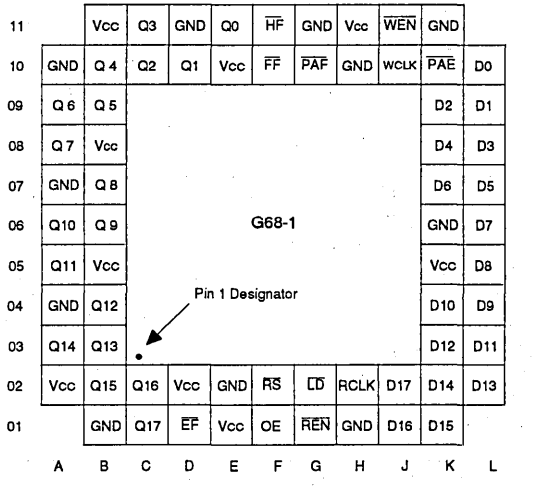
The IDT72215L/72225L is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



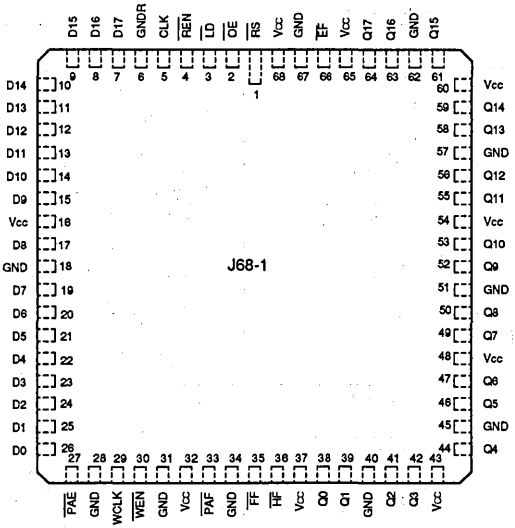
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



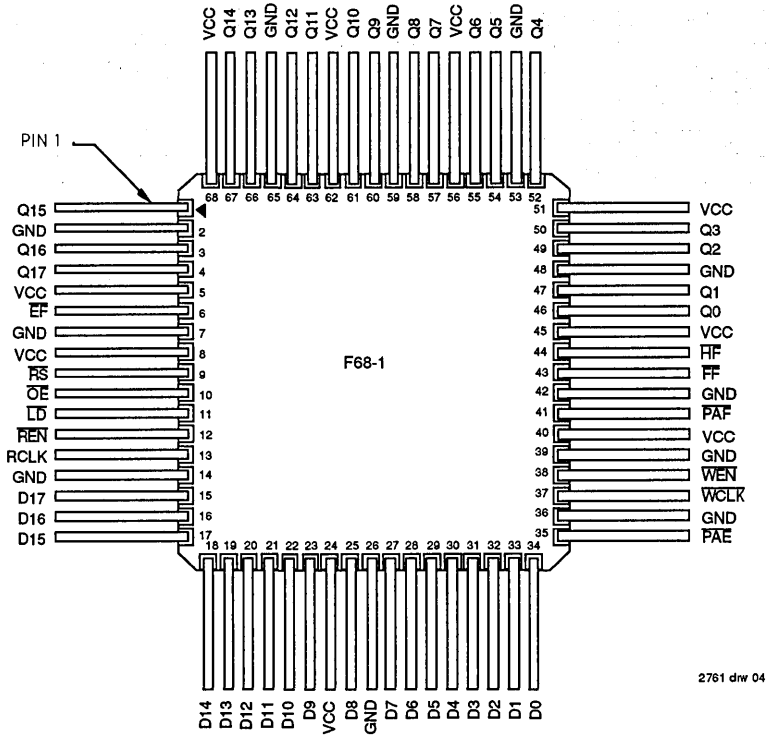
PGA
TOP VIEW

2761 drw 02



PLCC
TOP VIEW

2761 drw 03



2761 drw 04

FLATPACK
TOP VIEW

5

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D0 - D17	Inputs	I	Data inputs for 18-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is low, a write cycle is initiated on the low-to-high transition of the write clock WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is low, data can be loaded into the FIFO on the low-to-high transition of every WCLK clock. When the FIFO is full ($\overline{FF}$ - low), the internal WRITE operation is blocked.
RCLK	Read Clock	I	When $\overline{REN}$ is enabled (low), data can be read on the outputs on the low-to-high transition of the read clock RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is low, data can be read from the FIFO on the low-to-high transition of every RCLK clock. When $\overline{REN}$ is high, the output register holds the previous data. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is enabled (low), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (high), the Q output bus is in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is low, data on the inputs D0-D15 is written to the offset registers on the low-to-high transition of the WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full. $\overline{FF}$ is synchronized with WCLK.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. $\overline{EF}$ is synchronized with RCLK.
$\overline{PAF}$	Programmable Almost Full Flag	O	When $\overline{PAF}$ is low, the device is almost full based on the programmable full offset. If there is no offset specified, the default value is 63 for 72215, and 127 for 72225.
$\overline{PAE}$	Programmable Almost Empty Flag	O	When $\overline{PAE}$ is low, the device is almost empty based on the programmable empty offset. If there is no offset specified, the default value is 63 for 72215, and 127 for 72225.
$\overline{HF}$	Half-Full Flag	O	The device is more than half full when $\overline{HF}$ is low.
Q0-Q17	Outputs	O	Data outputs for 18-bit wide data.
Vcc	Power Supply		Nine +5 V power supply pins.
GND	Ground		Eleven Ground pins.

2761 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

2761 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

2761 tbl 03

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72215L/72225L Commercial t_{CLK} = 20, 25, 35, 50ns Min.	Typ.	Max.	IDT72215L/72225L Military t_{CLK} = 25, 35, 50ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	250	—	—	250	mA
I_{CC2}(3)	Average Standby Current (All inputs = V_{CC} - 0.2V, except RCLK and WCLK wchich are free running)	—	—	70	—	—	85	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20MHz with outputs open.

2761 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

2761 tbl 05

NOTES:
1. Characterized values, not currently tested.
2. With output deselected, ($\overline{OE}$ = high).

AC ELECTRICAL CHARACTERISTICS (1)

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Com'l. 72215L/25L20 Min.	Com'l. 72215L/25L20 Max.	Commercial & Military 72215L/25L25 Min.	72215L/25L25 Max.	72215L/25L35 Min.	72215L/25L35 Max.	72215L/25L50 Min.	72215L/25L50 Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	—	13	—	15	—	20	—	25	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	10	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	7	—	8	—	10	—	10	—	ns
tDH	Data Hold Time(1)	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	7	—	9	—	11	—	12	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	30	—	ns
tRSR	Reset Recovery Time	15	—	20	—	25	—	35	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low Z(3)	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	17	—	20	ns
tOHZ	Output Enable to Output in High Z(3)	1	9	1	12	1	17	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	—	30	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	30	—	35	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	30	—	35	ns
tHF	Clock to Half-Full Flag	—	20	—	22	—	30	—	35	ns
tSKW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKW1	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

2761 tbl 06

NOTES:
1. Allow an additional two (2) ns hold time when programming the offset registers.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2761 tbl 07

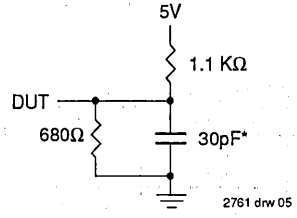


Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

Inputs

DATA IN (D0 - D17)

Data inputs for 18-bit wide data.

Controls:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost Full Flag ($\overline{PAF}$) will be reset to high after tRSF. The Empty Flag ($\overline{EF}$) and Programmable Almost Empty Flag ($\overline{PAE}$) will be reset to low after tRSF.

WRITE CLOCK (WCLK)

A write cycle is initiated on the low-to-high transition of the write clock (WCLK) if $\overline{WEN}$ is low. Data set-up and hold times must be met in respect to the low-to-high transition of the write clock (WCLK).

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after tWFF, allowing a write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the low-to-high transition of the read clock (RCLK) if $\overline{REN}$ is low.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is low, data that has been stored in the output register on the previous read cycle can be read on the outputs on the low-to-high transition of every read clock (RCLK), if Output Enable ($\overline{OE}$) is enabled. At the same time, data is read from the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a write is performed, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

LOAD ($\overline{LD}$)

The IDT72215L and IDT72225L devices contain two 16-bit offset registers and a 6-bit blank register which can be loaded with data from the data inputs, or read on the data outputs. When the Load ($\overline{LD}$) pin is set low and $\overline{WEN}$ is set low, data on the inputs D0 - D15 is written into the Empty offset register on the first low-to-high transition of the write clock (WCLK). When the Load ($\overline{LD}$) pin and Write Enable ($\overline{WEN}$) are held low then data is written into the Full offset register on the second low-to-high transition of the write clock (WCLK) and into the blank register on the third transition. The blank register must be written with all zeros. The fourth transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Load ($\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Load ($\overline{LD}$) pin is set low, and Write Enable ($\overline{WEN}$) is low, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Load ($\overline{LD}$) pin is set low and $\overline{REN}$ is set low. Data can be read on the low-to-high transition of the read clock (RCLK), when $\overline{REN}$ is enabled (low).

A read and a write should not be performed simultaneously to the offset registers.

Outputs:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 512 writes for the IDT72215L and 1024 writes for the IDT72225L.

The Full Flag ($\overline{FF}$) is updated on the low-to-high transition of the write clock (WCLK).

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is updated on the low-to-high transition of the read clock (RCLK).

5

PROGRAMMABLE ALMOST FULL FLAG ($\overline{PAF}$)

The Programmable Almost Full Flag ($\overline{PAF}$) will go low when the FIFO reaches the Almost Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Full Flag ($\overline{PAF}$) will go low after (512 - m) writes for the IDT72215L and (1024 - m) writes for the IDT72225L. The offset 'm' is defined in the FULL offset register.

If there is no Full offset specified, the Programmable Almost Full Flag ($\overline{PAF}$) default value is 63 for 72215L, and 127 for 72225L.

The Programmable Almost Full Flag ($\overline{PAF}$) going low is updated on the low-to-high transition of the write clock (WCLK). $\overline{PAF}$ is reset to high on the low-to-high transition of the read clock (RCLK).

PROGRAMMABLE ALMOST EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost Empty Flag ($\overline{PAE}$) will go low when the read pointer is 'n' locations less than the write pointer. The offset 'n' is defined in the EMPTY offset register. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Empty Flag ($\overline{PAE}$) will go high after n writes for both the IDT72215L and the IDT72225L. The Programmable Almost Empty Flag ($\overline{PAE}$) will be low when the FIFO is empty up to n writes, if the read pointer is not moved.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) default value is 63 for 72215L, and 127 for 72225L.

The Programmable Almost Empty Flag ($\overline{PAE}$) going low is updated on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the wirte clock (WCLK).

HALF-FULL FLAG ($\overline{HF}$)

After half of the memory is filled, and at the low-to-high transition of the next write cycle, the Half-Full Flag ($\overline{HF}$) goes low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to high by the low-to-high transition of the read clock (RCLK).

DATA OUTPUTS (Q0 - Q17)

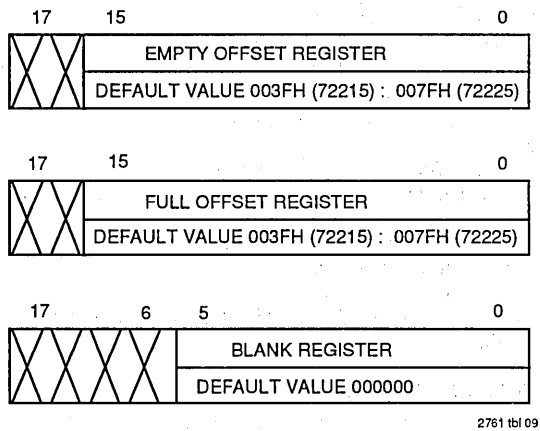
Q_0 - Q_{17} are data outputs for 18-bit wide data.

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	SELECTION
0	0	↑	WRITING TO OFFSET REGISTERS: EMPTY OFFSET FULL OFFSET BLANK REGISTER
0	1	↑	INCREMENTING OFFSET REGISTER COUNTER BUT NOT WRITING: EMPTY OFFSET FULL OFFSET BLANK REGISTER
1	0	↑	WRITE INTO FIFO
1	1	↑	NO OPERATION

2761 tbl 08

Figure 2. Write Offset Register

NOTE:
1. The same selection sequence applies to reading from the register. $\overline{REN}$ is enabled and read is performed on the low-to-high transition of RCLK.



2761 tbl 09

Figure 3. Offset Register Location and Default Values

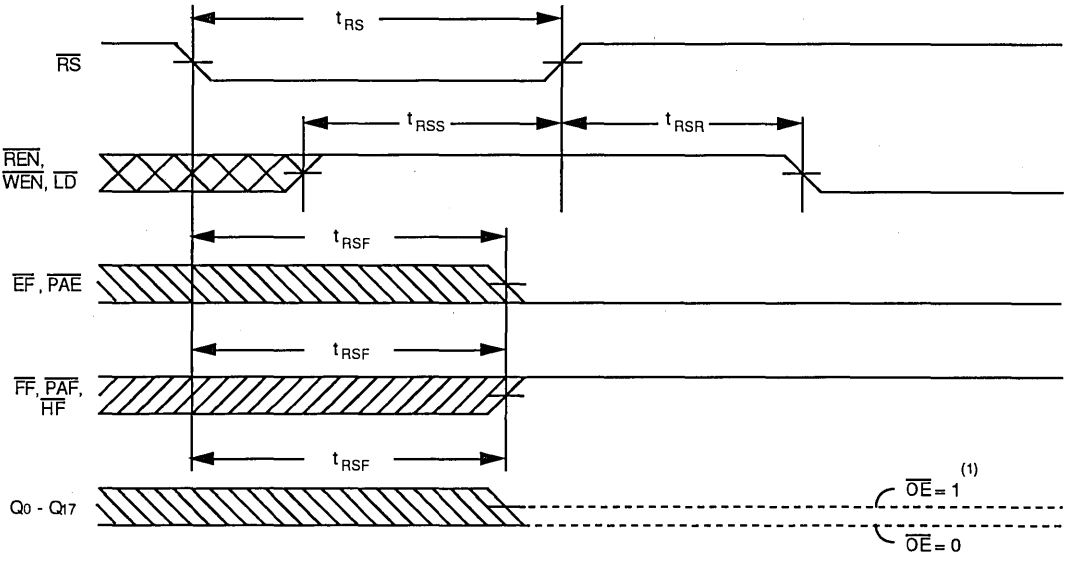


Figure 5. Reset Timing[2]

2761 drw 06

NOTES:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

5

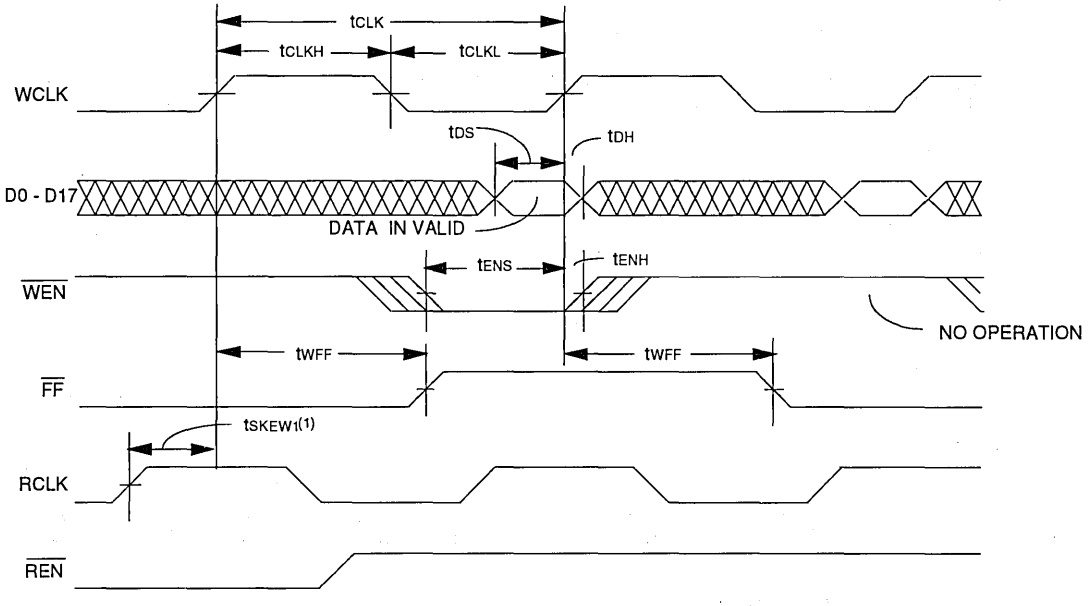


Figure 6. Write Cycle Timing

2761 drw 07

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee $\overline{FF}$ will go high during the current clock cycle. If the time between therising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

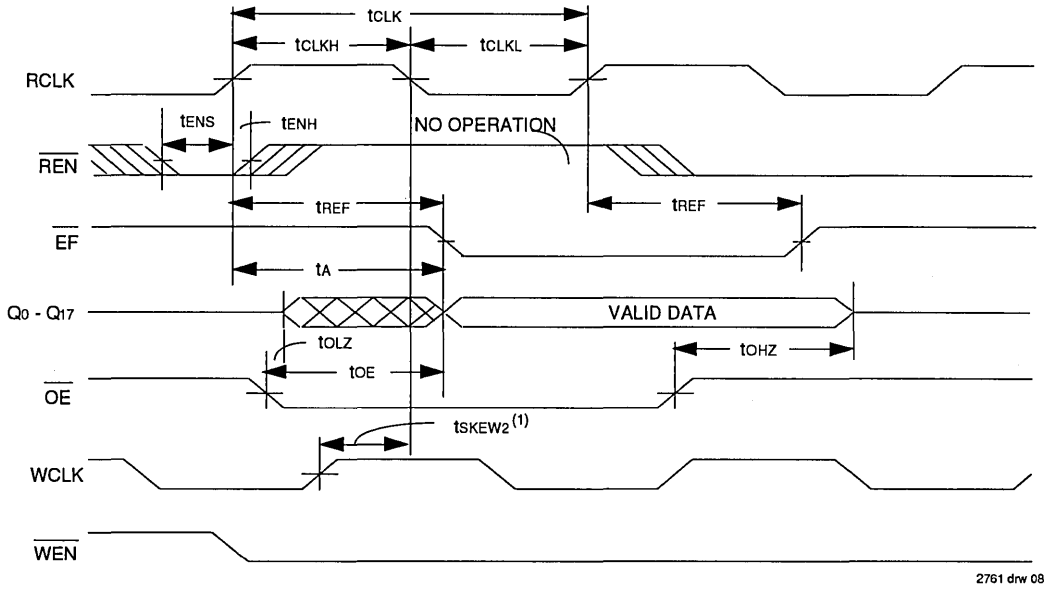


Figure 7. Read Cycle Timing

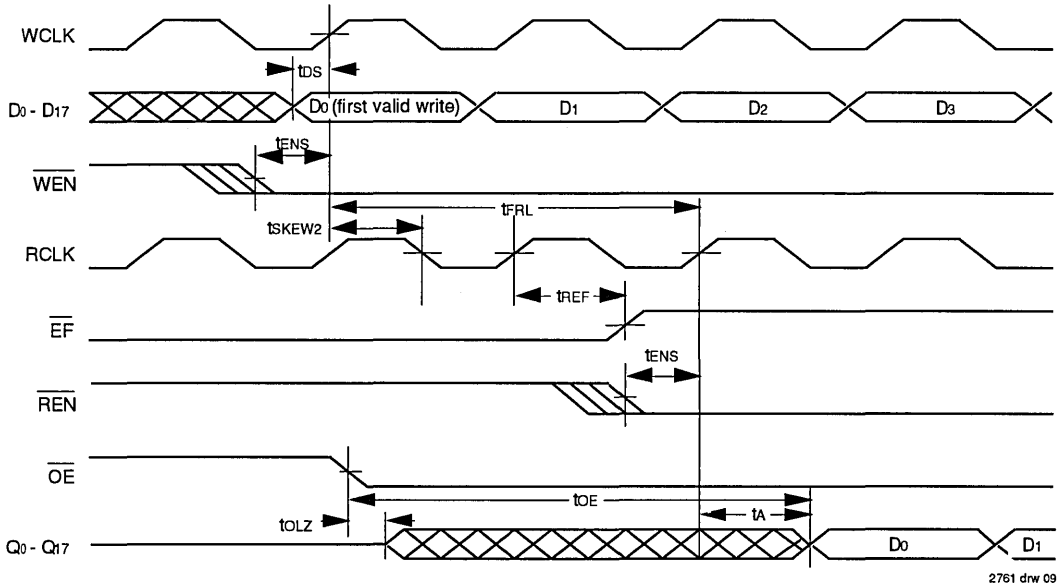


Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2.5 * t_{CLK} + t_{SKEW2} or 1.5 * tCLK + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

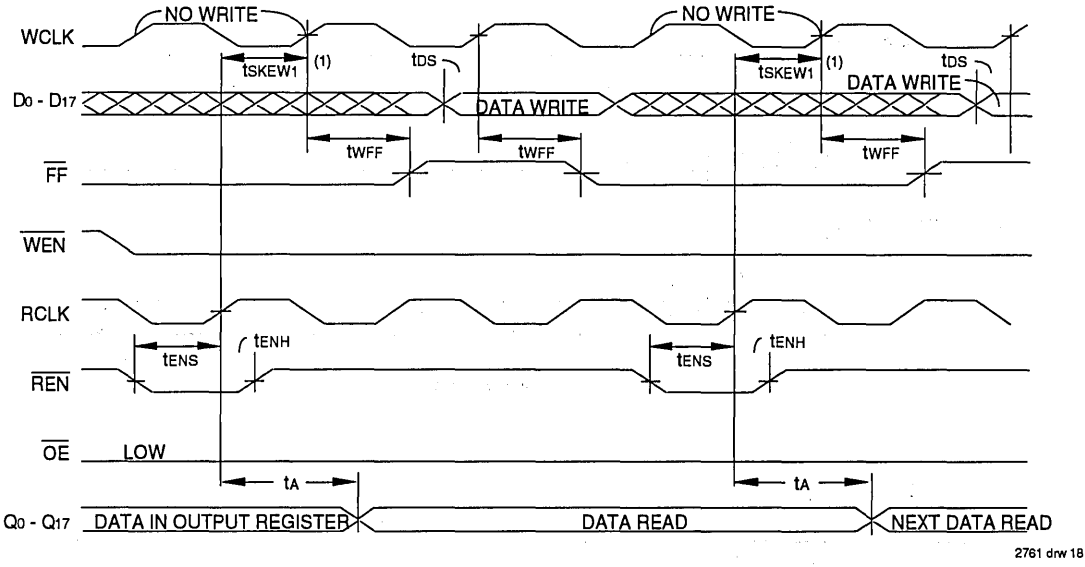


Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee $\overline{FF}$ will go high during the current clock cycle. If the time between therising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

5

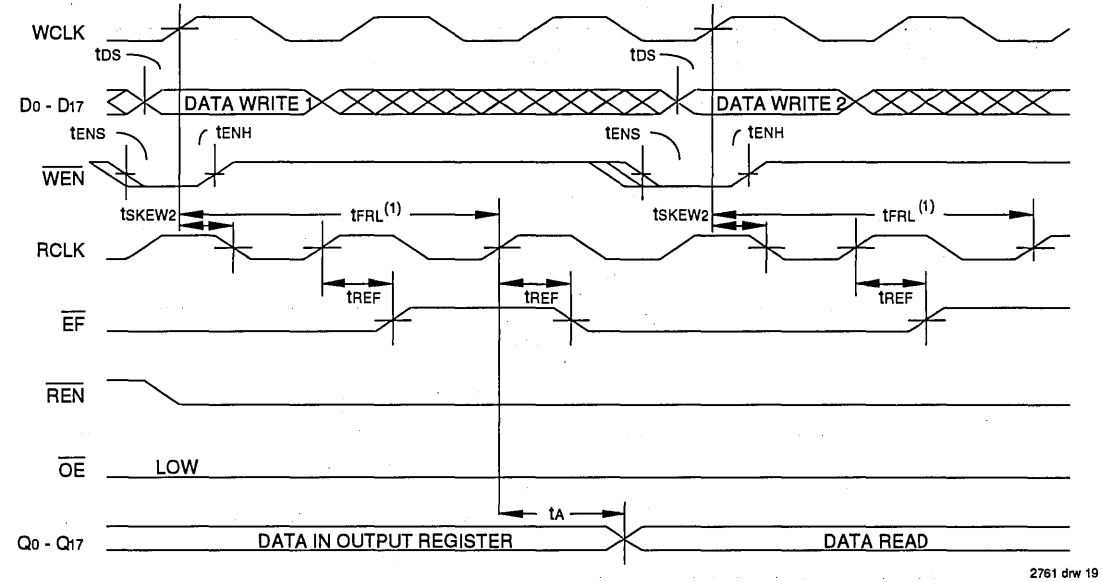


Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2.5 * t_{CLK} + t_{SKEW2} or 1.5 * tCLK + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

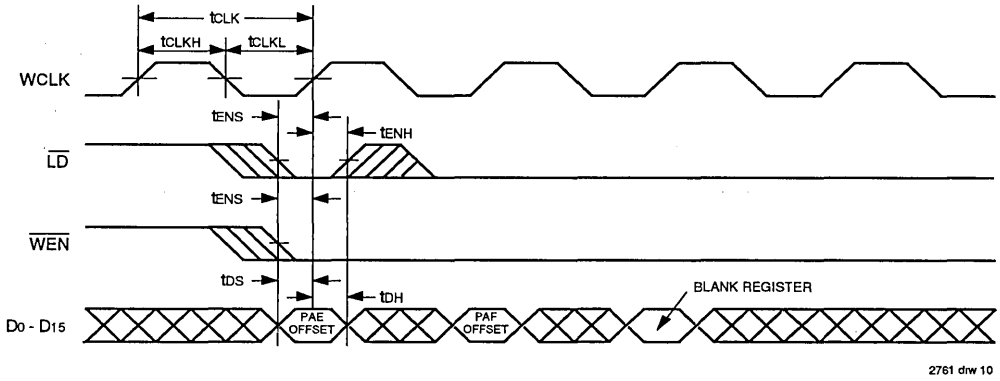


Figure 11. Write Programmable Registers

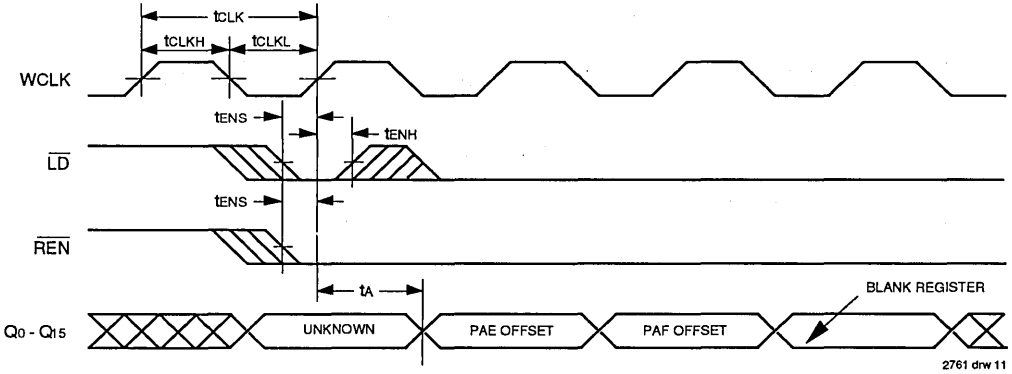
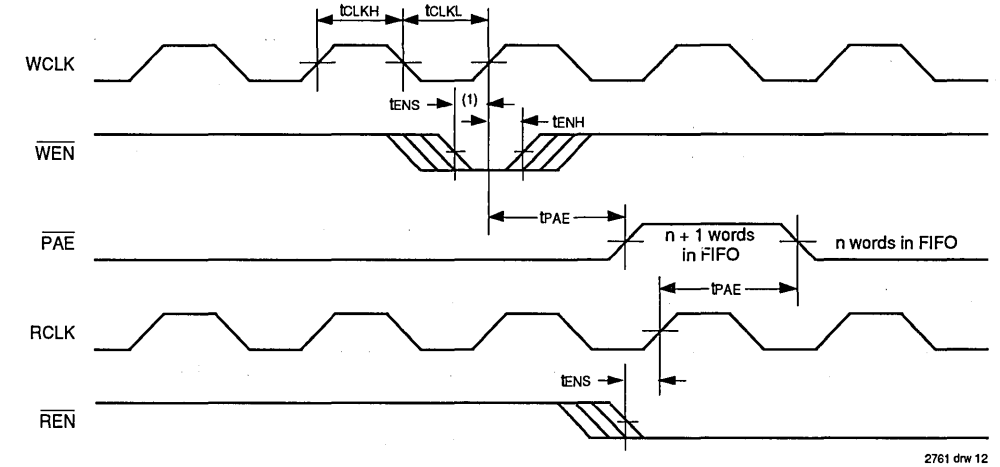


Figure 12. Read Programmable Registers



NOTE 1: PAE offset = n. Number of data words written into FIFO already = n.

Figure 13. Programmable Almost Empty Flag Timing

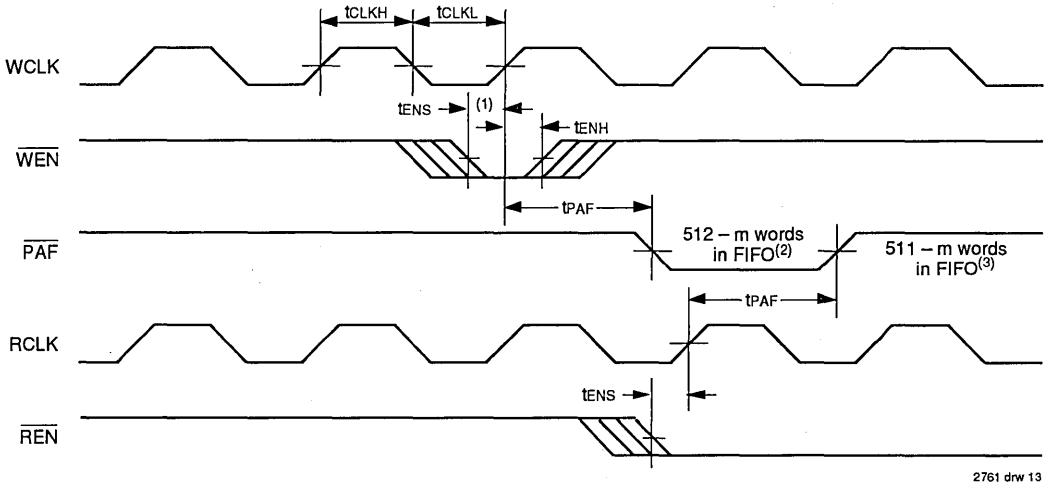


Figure 14. Programmable Almost Full Flag Timing

NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 511 – m for the IDT72215L and 1023 – m for the IDT72225L.
2. 512 - m words in FIFO for IDT72215L. 1024 - m words in FIFO for IDT72225L.
3. 511 - m words in FIFO for IDT72215L. 1023 - m words in FIFO for IDT72225L.

5

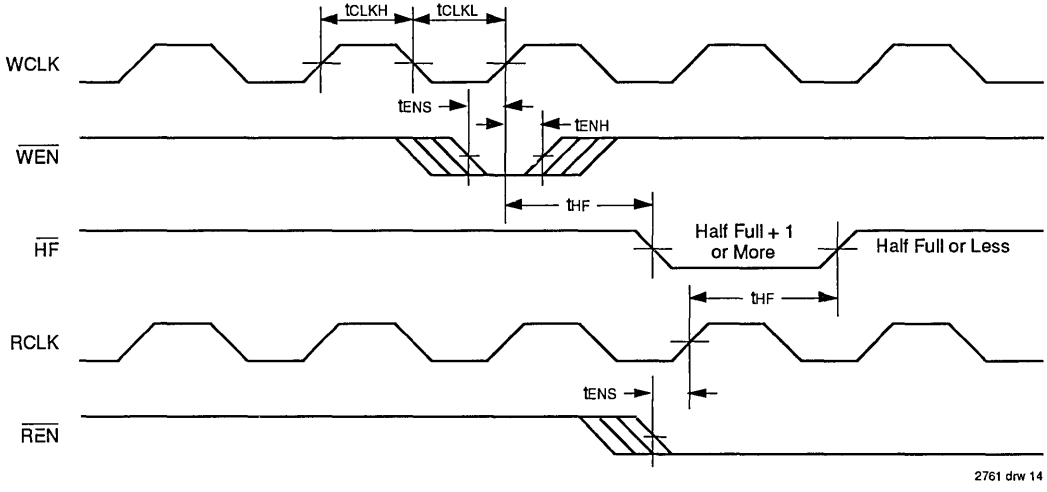


Figure 15. Half-Full Flag Timing

OPERATING CONFIGURATIONS:

SINGLE DEVICE CONFIGURATION

A single IDT72215/72225 may be used when the application requirements are for 512/1024 words or less.

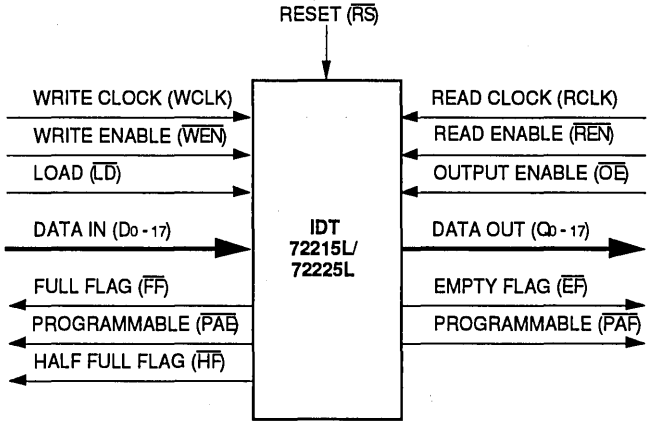


Figure 16. Block Diagram of Single 512 x 18/ 1024 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Asynchronous status flags ($\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$) can be detected from any one device. Synchronous status flags ($\overline{EF}$ and $\overline{FF}$) should be gated through an AND gate because the flag deassertions may vary among different FIFOs by one cycle. Figure 17 demonstrates a 36-word width by using two IDT72215L/72225Ls. Any word width can be attained by adding additional IDT72215L/72225Ls. Please see the Application Note AN-83 "Width Expansion of SyncFIFOs (Clocked FIFOs).

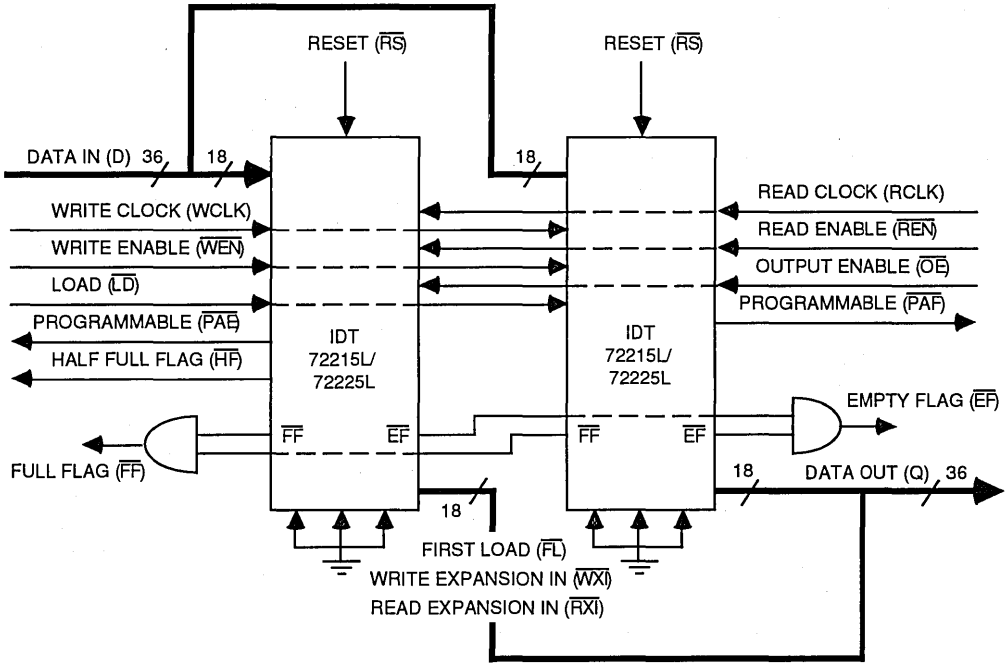


Figure 17. Block Diagram of 512 x 36/ 1024 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

NOTE:
1. Flag detection is accomplished by monitoring the flag signals on either (any) device used in width expansion configuration. Do not connect any output control signals together.

DEPTH EXPANSION

The IDT72215L/72225L can be adapted to applications when the requirements are for greater than 512/1024 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner. Please contact IDT Applications Engineering for details.

The 72215LB/72225LB Depth Expandable versions of this part incorporate an on-chip depth expansion technique. Please see the 72215LB/72225LB data sheet for details. The 72215LB/72225LB version will supersede this part.

Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 256 x 18-BIT, 512 x 18-BIT, 1024 x 18-BIT 2048 x 18-BIT & 4096 x 18-BIT

PRELIMINARY
IDT72205LB
IDT72215LB
IDT72225LB
IDT72235LB
IDT72245LB

FEATURES:

- 256 x 18-bit memory array (72205B)
- 512 x 18-bit memory array (72215B)
- 1024 x 18-bit memory array (72225B)
- 2048 x 18-bit memory array (72235B)
- 4096 x 18-bit memory array (72245B)
- 15ns read / write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance state
- High-performance submicron CEMOS™ technology
- Available in a 68-lead flat pack (FP), pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

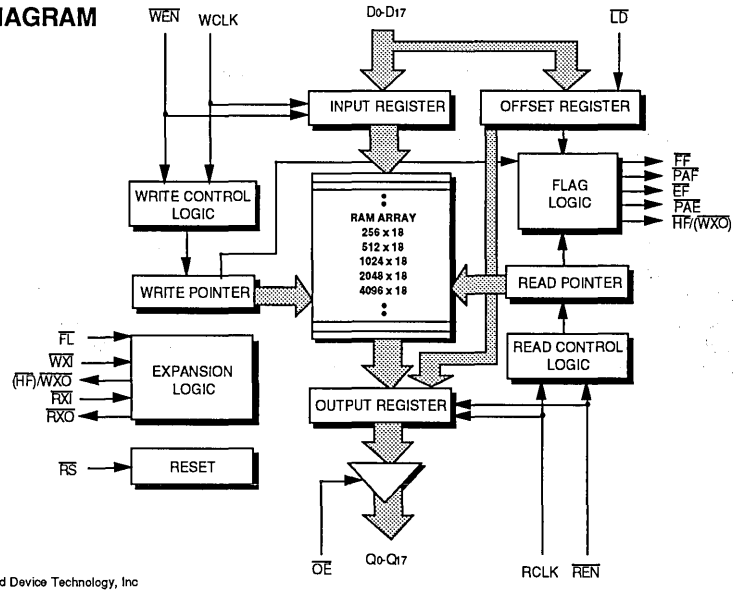
Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are depth expandable using a daisy-chain technique. The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. In depth expansion configuration, FL is grounded on the first device and set to high for all other devices in the daisy chain.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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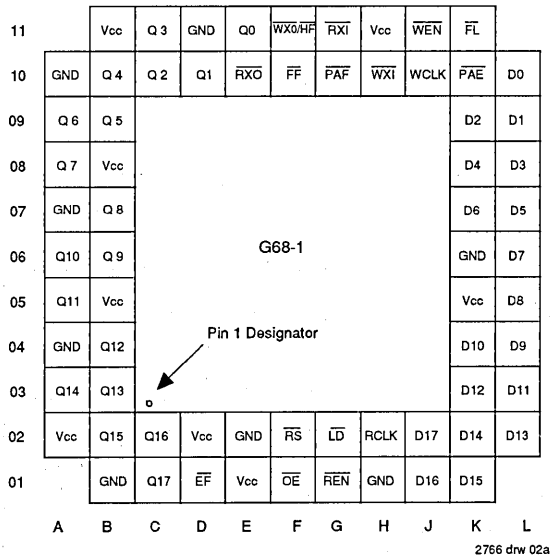
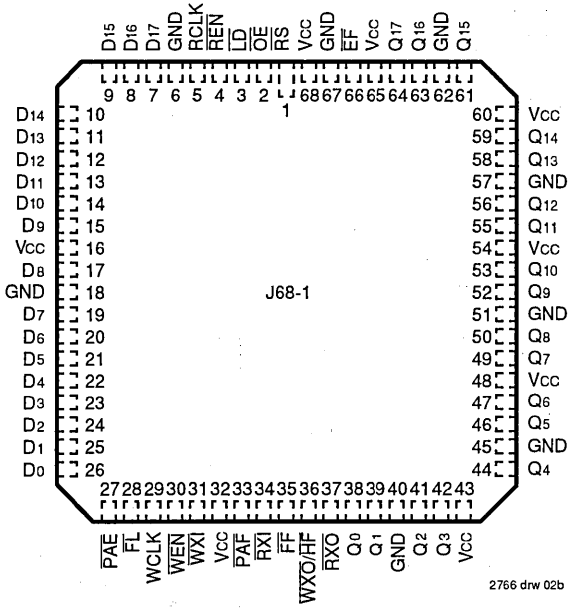
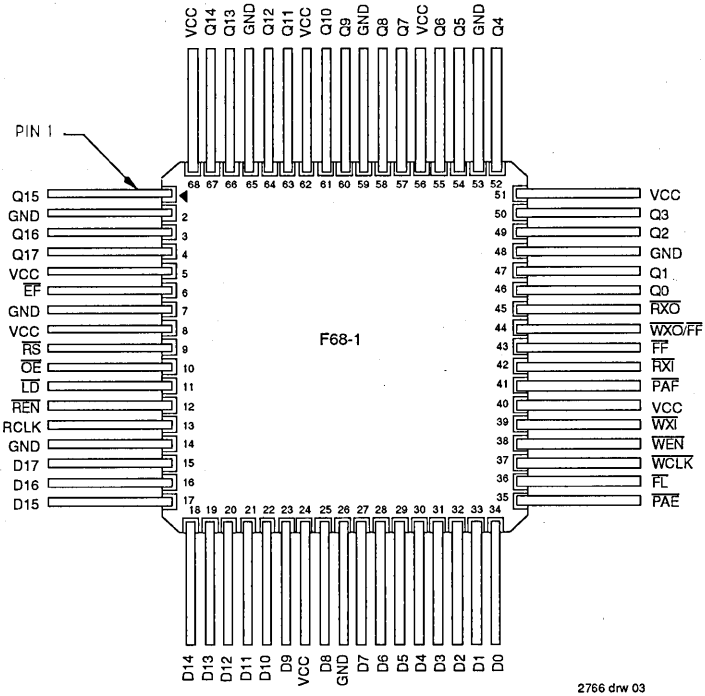
PIN CONFIGURATIONS



PGA
TOP VIEW



PLCC
TOP VIEW



FLATPACK
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is low, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	When $\overline{REN}$ is low, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D_0–D_{11} is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q_0–Q_{11} is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhib ited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for 72205B, 63 from empty for 72215B, and 127 from empty for 72225B/72235B/72245B.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for 72205B, 63 from full for 72215B, and 127 from full for 72225B/72235B/72245B.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q_0–Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
V_{CC}	Power		Eight +5 volt power supply pins.
GND	Ground		Eight ground pins.

2766 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2766 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 2766 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72205LB IDT72215LB IDT72225LB IDT72235LB IDT72245LB Commercial t_{CLK} = 20, 25, 35, 50ns			IDT72205LB IDT72215LB IDT72225LB IDT72235LB IDT72245LB Military t_{CLK} = 25, 30, 35, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	200	—	—	250	mA
I_{CC2}(3)	Average Standby Current (All Input = V_{CC} – 0.2V, except RCLK and WCLK which are free-running)	—	—	70	—	—	85	mA

NOTES: 2766 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20 MHz with outputs open.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	VIN = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2766 tbl 05

1. With output deselected, (OE=High).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = –55°C to +125°C)

		Commercial				Commercial and Military						
		72205LB15 72215LB15 72225LB15 72235LB15 72245LB15		72205LB20 72215LB20 72225LB20 72235LB20 72245LB20		72205LB25 72215LB25 72225LB25 72235LB25 72245LB25		72205LB35 72215LB35 72225LB35 72235LB35 72245LB35		72205LB50 72215LB50 72225LB50 72235LB50 72245LB50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	6.5	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	6.5	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	20	—	30	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	20	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	35	—	35	—	40	—	45	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High Z[2]	1	8	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	28	—	30	—	35	—	40	—	40	ns
tHF	Clock to Half-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tXO	Clock to Expansion Out	—	10	—	12	—	15	—	20	—	30	ns
tXI	Expansion In Pulse Width	6.5	—	8	—	10	—	14	—	20	—	ns
tXIS	Expansion In Set-Up Time	5	—	8	—	10	—	15	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	10	—	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	10	—	14	—	16	—	18	—	20	—	ns

2766 tbl 06

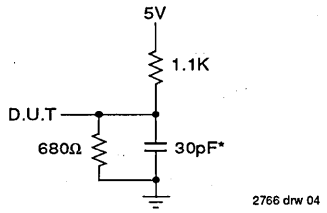
NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2766 tbl 07



2766 drw 04

Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})
Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}.

WRITE CLOCK (WCLK)
A write cycle is initiated on the low-to-high transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the low-to-high transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)
When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF} allowing a write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)
Data can be read on the outputs on the low-to-high transition of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set low.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)
When Read Enable ($\overline{REN}$) is low, data is loaded into the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a write is performed, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)
When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

LOAD ($\overline{LD}$)
The IDT72205LB/72215LB/72225LB/72235LB/72245LB devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load ($\overline{LD}$) pin is set low and WEN is set low, data on the inputs D0-D11 is written into the Empty offset register on the first low-to-high transition of the write clock (WCLK). When the Load ($\overline{LD}$) pin and Write Enable (WEN) are held low then data is written into the Full offset register on the second low-to-high transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Load ($\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Load ($\overline{LD}$) pin is set low, and Write Enable (WEN) is low, the next offset register in sequence is written.

When the Load pin is low and Write Enable is high, the offset register counter increments without writing into the offset registers.

The contents of the offset registers can be read on the output lines when the Load ($\overline{LD}$) pin is set low and REN is set low. Data can be read on the low-to-high transition of the read clock (RCLK) when REN is enabled (low).

A read and a write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	SELECTION
0	0		WRITING TO OFFSET REGISTERS: EMPTY OFFSET FULL OFFSET 
0	1		INCREMENTING OFFSET REGISTER COUNTER BUT NOT WRITING: EMPTY OFFSET FULL OFFSET 
1	0		WRITE INTO FIFO
1	1		NO OPERATION

NOTE: 2766 drw 05
1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the low-to-high transition of RCLK.

Figure 2. Write Offset Register

FIRST LOAD ($\overline{FL}$)

First Load ($\overline{FL}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, First Load ($\overline{FL}$) is grounded to indicate it is the first device loaded and is set to high for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT ($\overline{RXI}$)

This is a dual purpose pin. Read Expansion In ($\overline{RXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

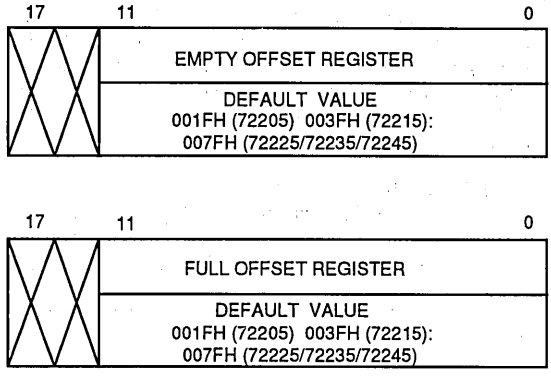
The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 256 writes for the IDT72205LB, 512 writes for the IDT72215LB, 1024 writes for the IDT72225LB, 2048 writes for the IDT72235LB and 4096 writes for the IDT72245LB.

The Full Flag ($\overline{FF}$) is updated on the low-to-high transition of the write clock (WCLK).

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is updated on the low-to-high transition the read clock (RCLK).



NOTE: 2766 drw 06
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

TABLE I — STATUS FLAGS

Number of Words In FIFO									
72205	72215	72225	72235	72245	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
(n+1) to 128	(n+1) to 256	(n+1) to 512	(n+1) to 1024	(n+1) to 2048	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1024-(m+1))	1025 to (2048-(m+1))	2049 to (4096-(m+1))	H	H	L	H	H
(256-m) [2] to 255	(512-m) [2] to 511	(1024-m) [2] to 1023	(2048-m) [2] to 2047	(4096-m) [2] to 4095	H	L	L	H	H
256	512	1024	2048	4096	L	L	L	H	H

NOTES: 2966 tbl 08
1. n = Empty Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)
2. m = Full Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go low when FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Full Flag ($\overline{PA}$) will go low after (256-m) writes for the IDT72205LB, (512-m) writes for the IDT72215LB, (1024-m) writes for the IDT72225LB, (2048–m) writes for the IDT72235LB and (4096–m) writes for the IDT72245LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will be low when the device is 31 away from completely full for 72205LB, 63 away from completely full for 72215LB, and 127 away from completely full for 72225LB/72235LB/72245LB.

The Programmable Almost-Full Flag ($\overline{PAF}$) is asserted low on the low-to-high transition of the write clock (WCLK). $\overline{PAF}$ is reset to high on the low-to-high transition of the read clock (RCLK). Thus $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go low when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) will be low when the device is 31 away from completely empty for 72205LB, 63 away from completely empty for 72215LB, and 127 away from completely empty for 72225LB/72235LB/72245LB.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is asserted low on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the write clock (WCLK). Thus $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the low-to-high transition of the next write cycle, the Half-Full Flag goes low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to high by the low-to-high transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

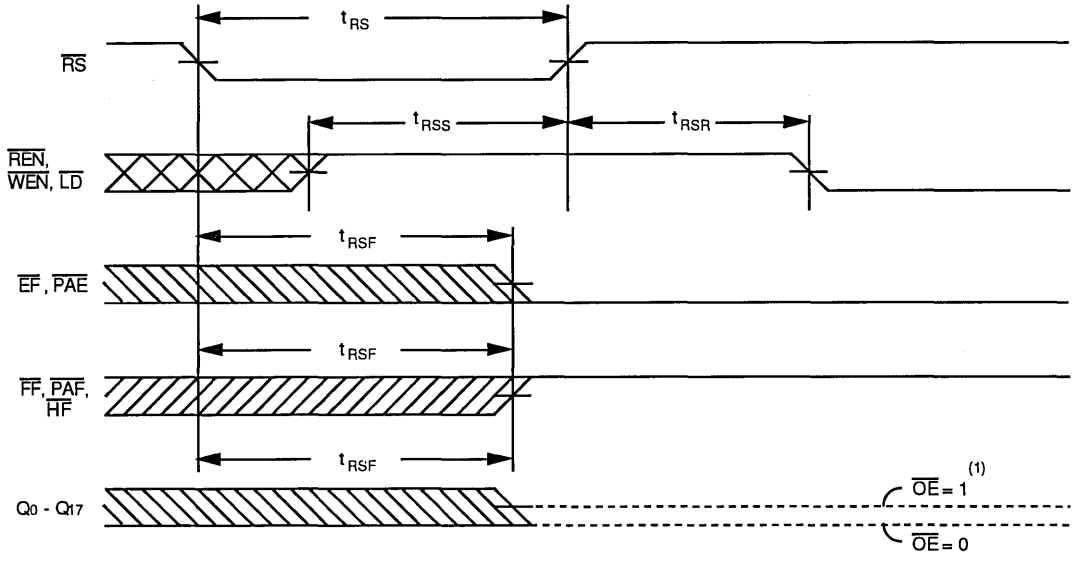
In the Depth Expansion or Daisy Chain mode, Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q_0-Q_{17})

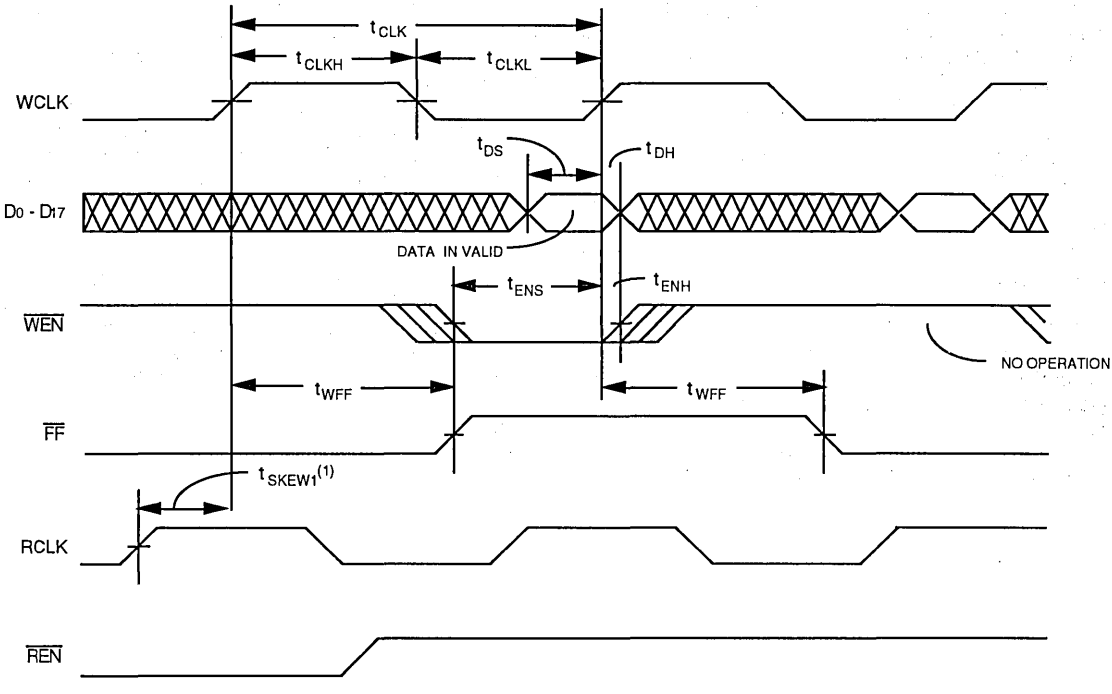
Q_0-Q_{17} are data outputs for 18-bit wide data.



2766 drw 07

NOTES:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

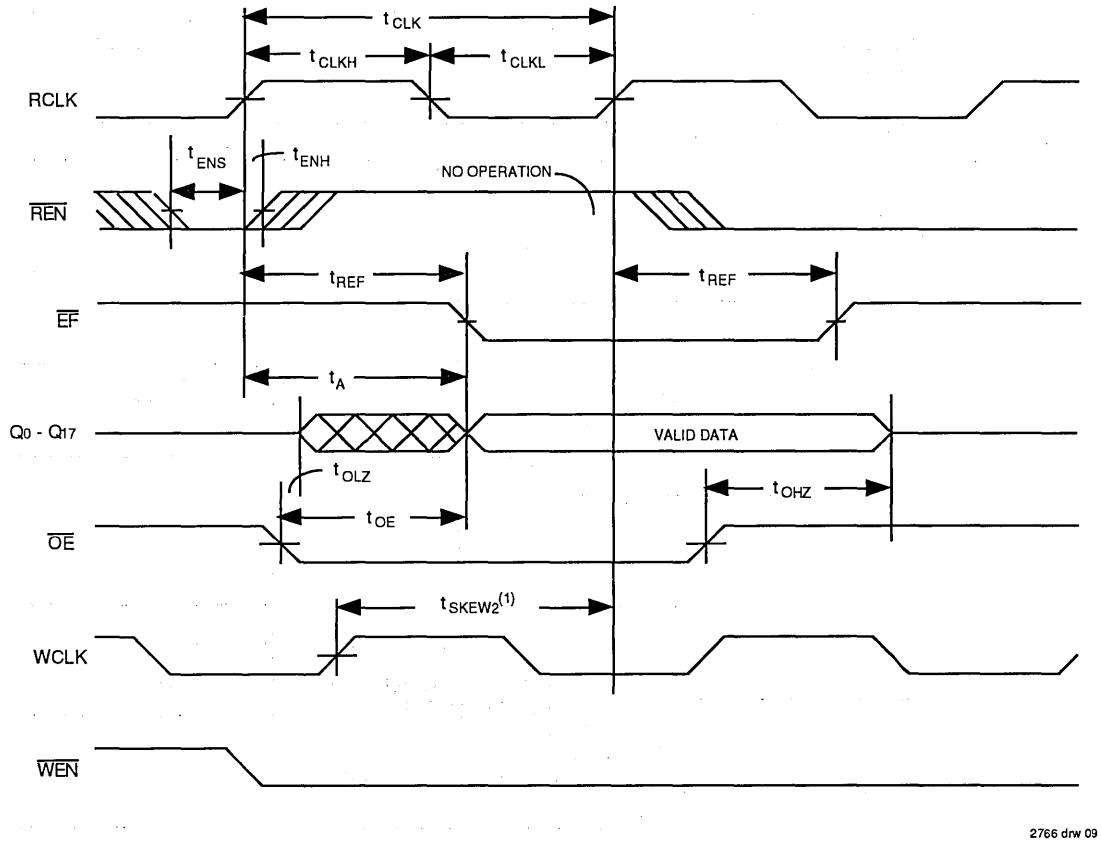
Figure 5. Reset Timing[2]



2766 drw 08

NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 6. Write Cycle Timing

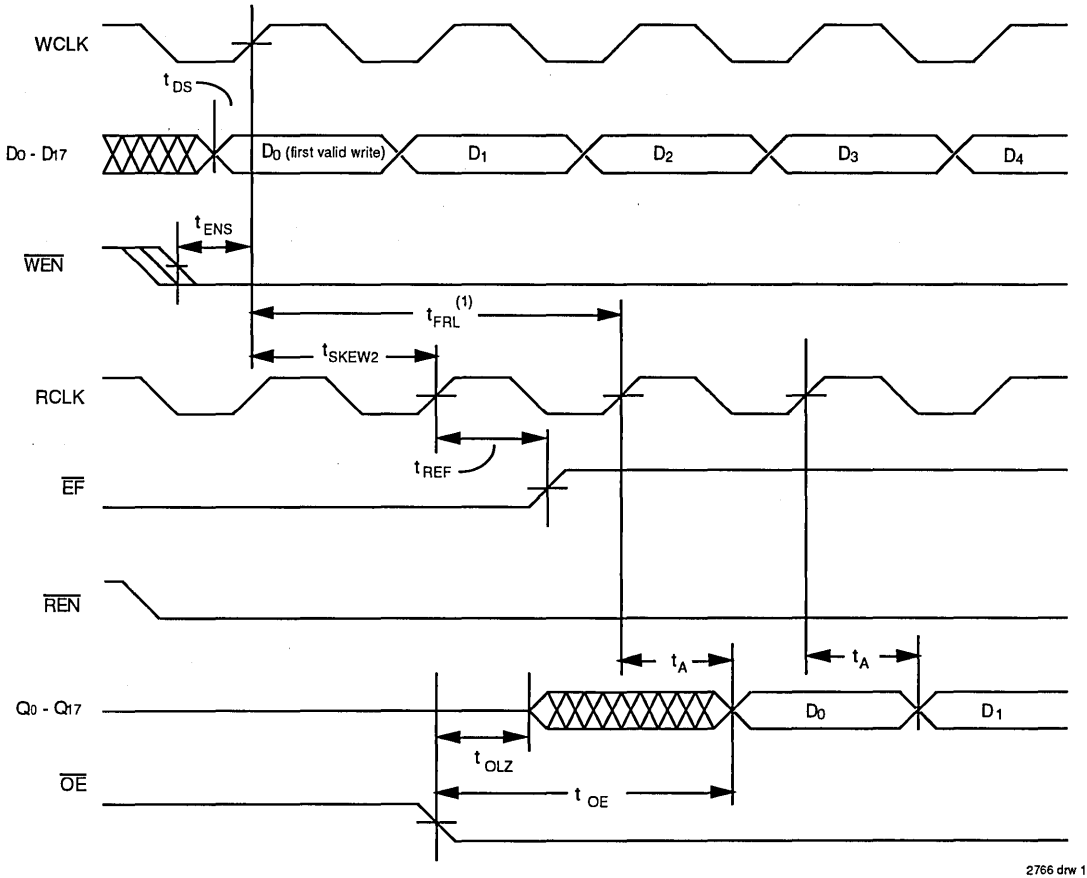


2766 drw 09

NOTE:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 7. Read Cycle Timing

5



NOTES:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
2. The first word is available the cycle after $\overline{EF}$ goes high, always.

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

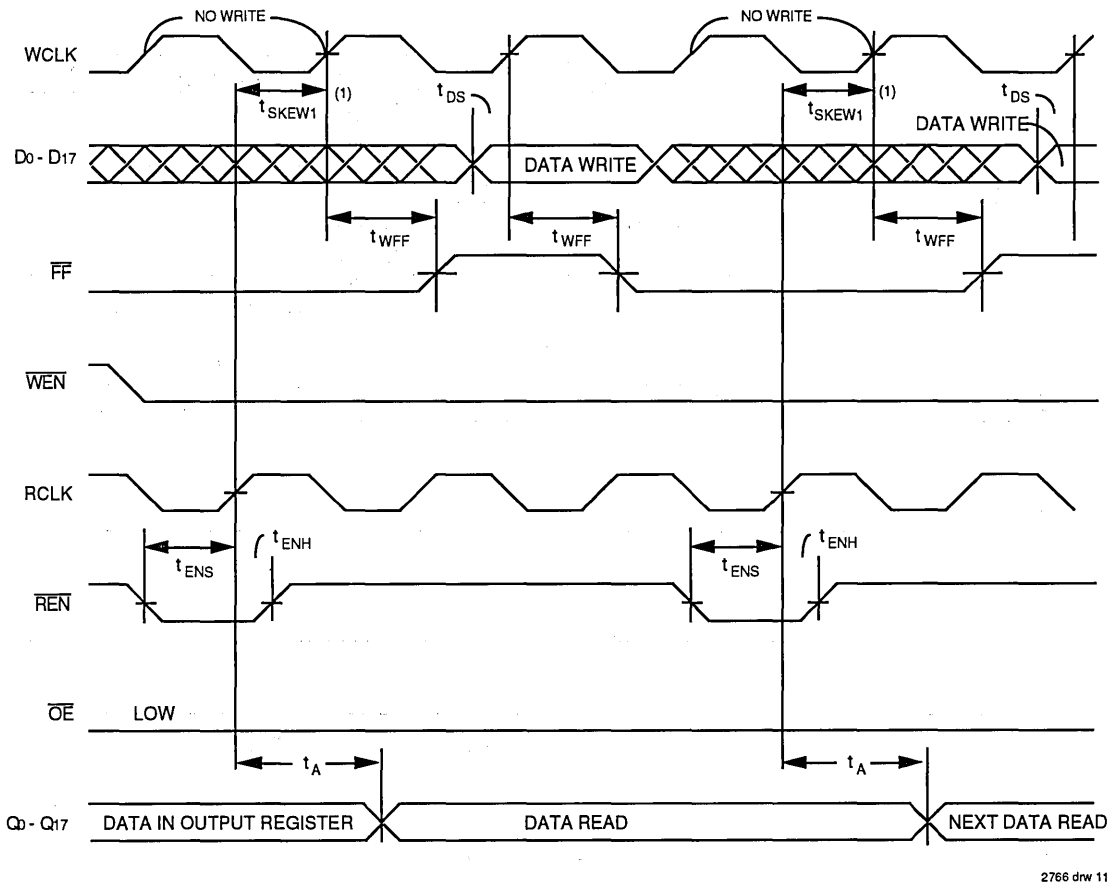


Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

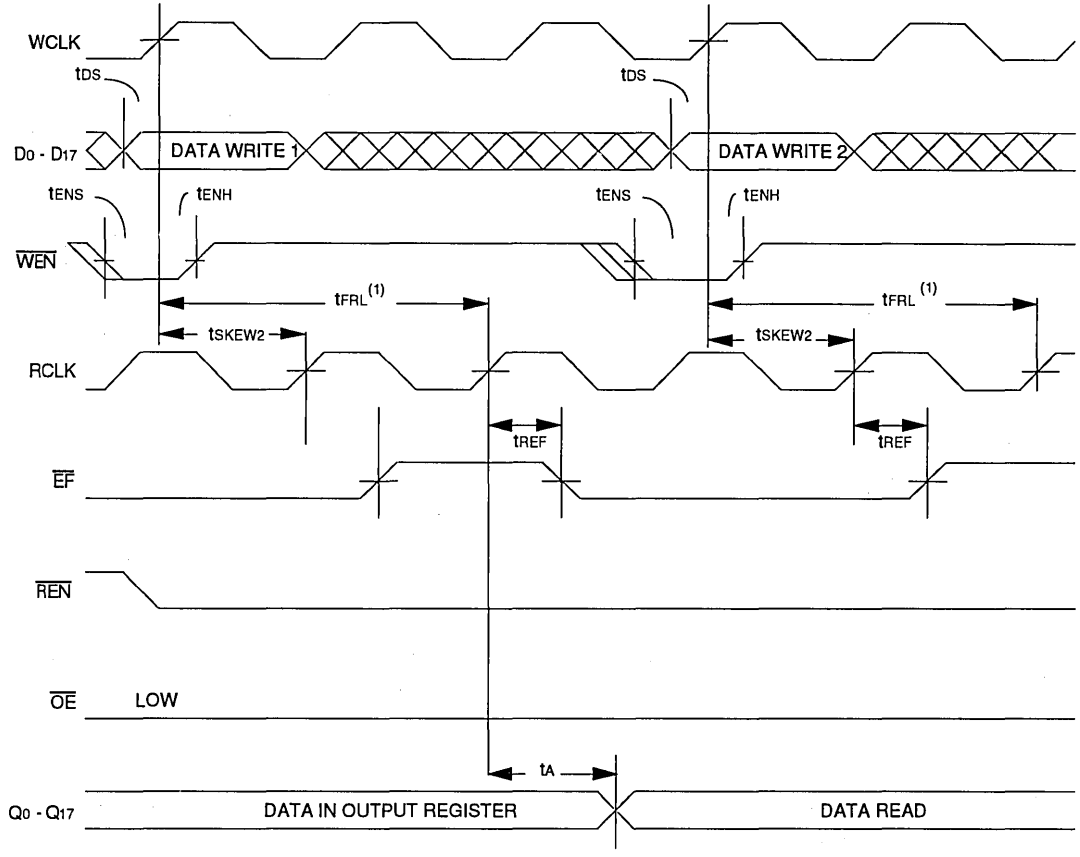


Figure 10. Empty Flag Timing

NOTE:

1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2}, or t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

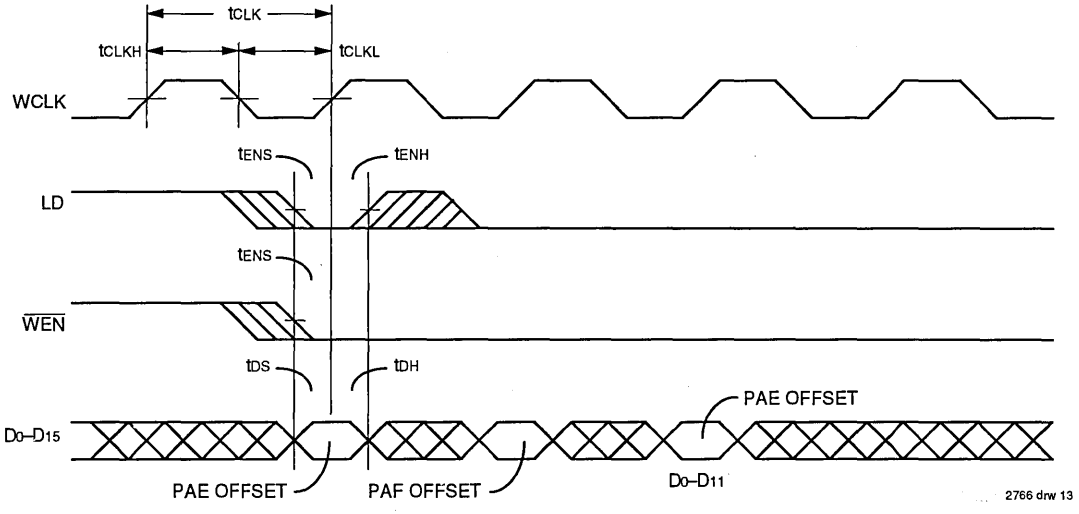


Figure 11. Write Programmable Registers

5

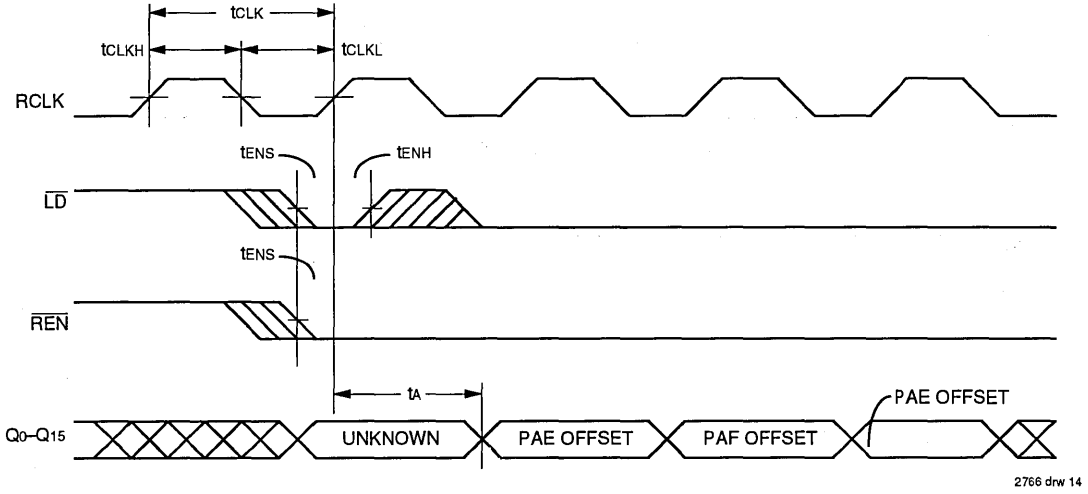
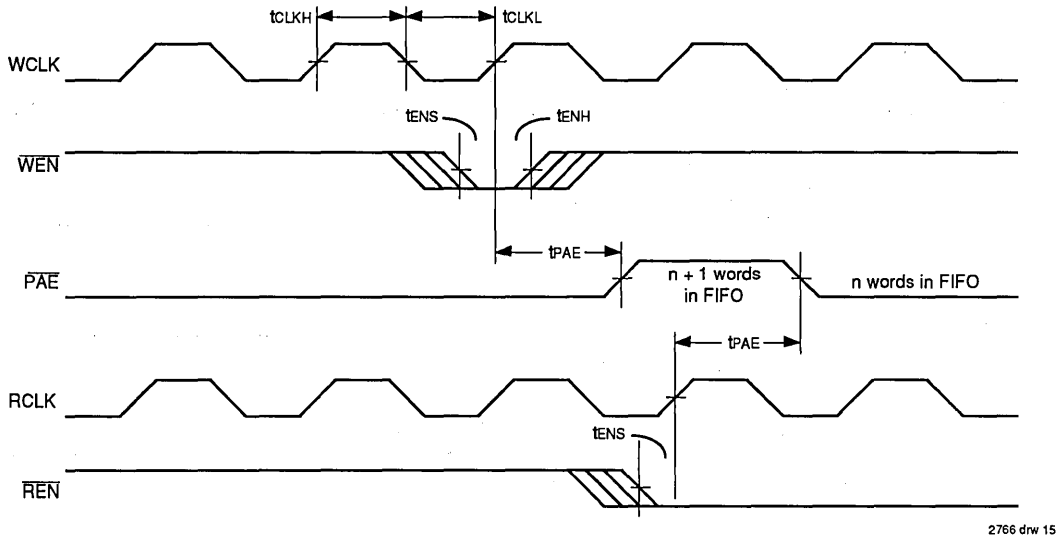
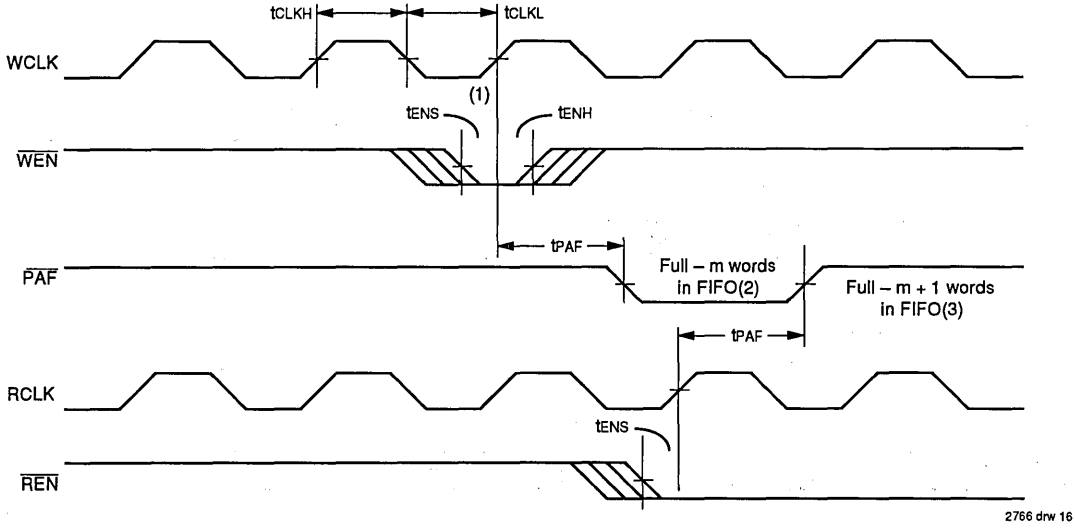


Figure 12. Read Programmable Registers



NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

Figure 13. Programmable Almost Empty Flag Timing



NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 256 - m + 1 for the IDT72205B, 512 - m + 1 for the IDT72215B, 1024 - m + 1 for the IDT72225B, 2048 – m + 1 for the IDT72235B and 4096 – m +1 for the IDT72245B.
2. 256 - m words in IDT72205B, 512 - m words in IDT72215B, 1024 - m words in IDT72225B, 2048 – m words in IDT72235B and 4096 – m words in IDT72245B.
3. 256 - m + 1 words in IDT72205B, 512 - m + 1 words in IDT72215B, 1024 - m + 1 words in IDT72225B, 2048 – m + 1 words in IDT72235B and 4096 – m + 1 words in IDT72245B.

Figure 14. Programmable Almost-Full Flag Timing

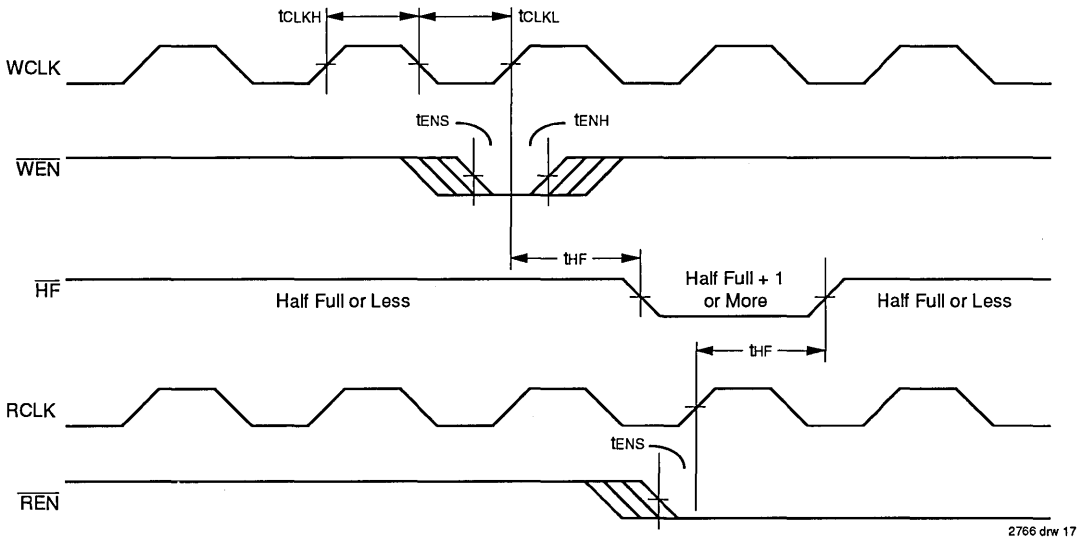
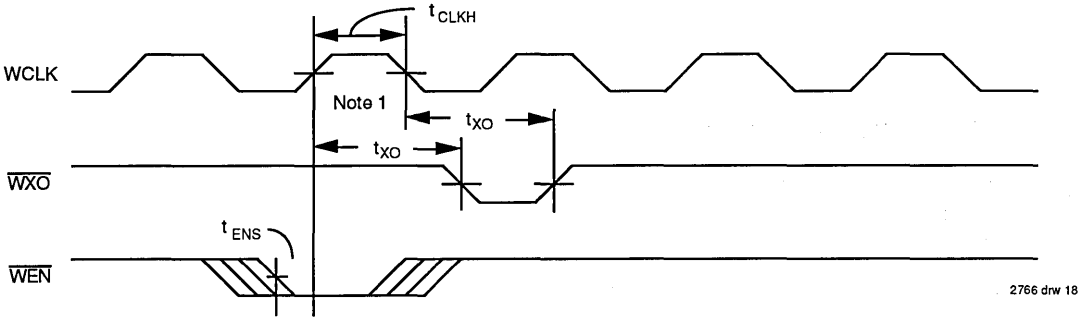
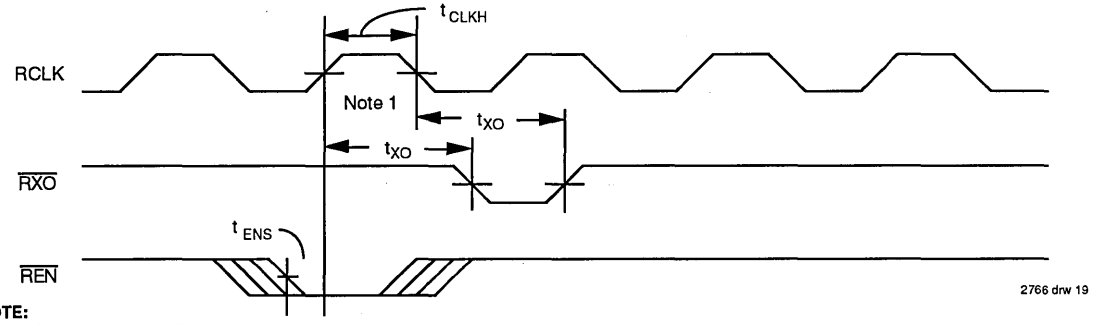


Figure 15. Half-Full Flag Timing



NOTE:
1. Write to Last Physical Location.

Figure 16. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 17. Read Expansion Out Timing

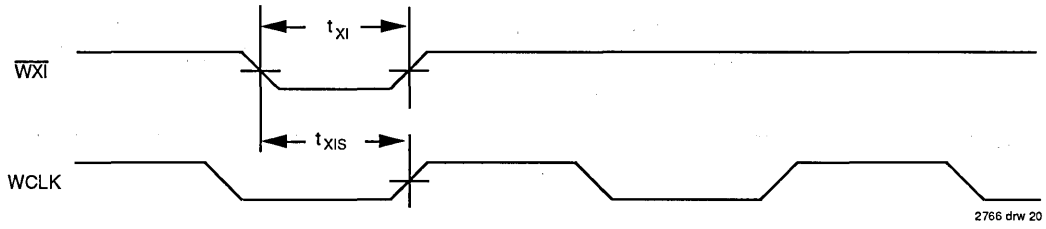


Figure 18. Write Expansion In Timing

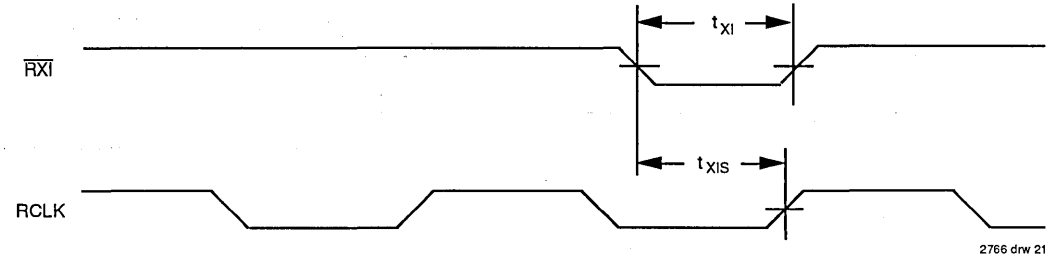


Figure 19. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72205LB/72215LB/72225LB/72235LB/72245LB may be used when the application requirements are for 256/512/1024/2048/4096 words or less. The IDT72205LB/72215LB/72225LB/72235LB/72245LB are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded (Figure 20).

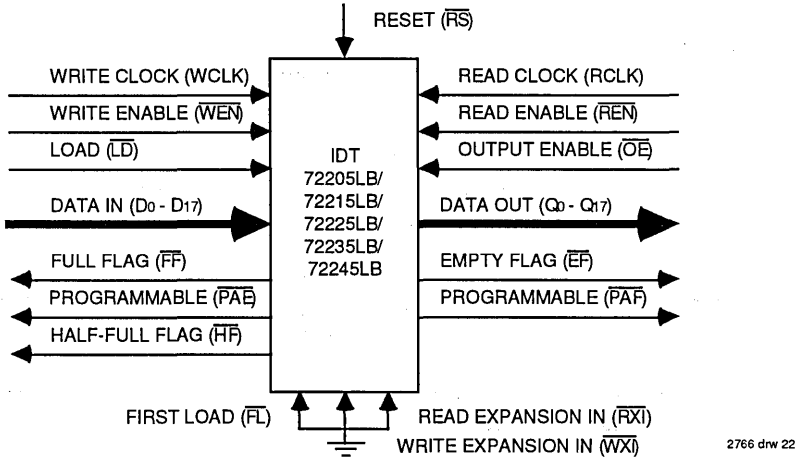
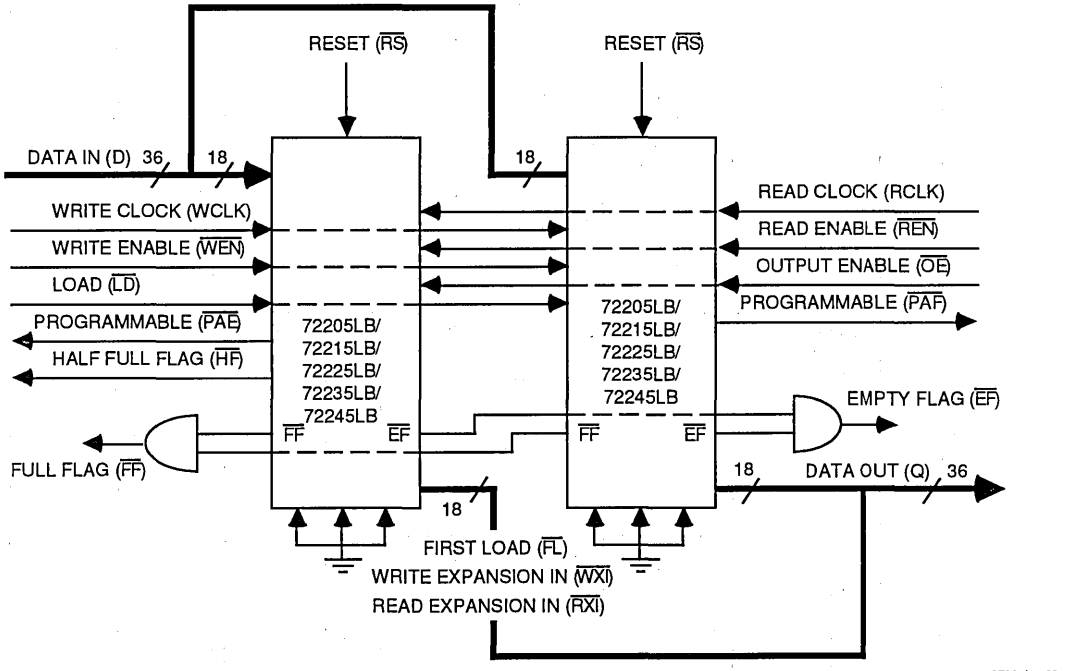


Figure 20. Block Diagram of Single 256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the Empty Flag and Full Flag. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems the user must create composite flags by ANDing the Empty Flags of every FIFO, and separately ANDing all Full Flags. Figure 21 demonstrates a 36-word width by using two IDT72205B/72215B/72225B/72235B/72245Bs. Any word width can be attained by adding additional IDT72205B/72215B/72225B/72235B/72245Bs. Please see the application note AN-83 "Width Expansion of SyncFIFO (Clocked FIFOs).



2766 drw 23

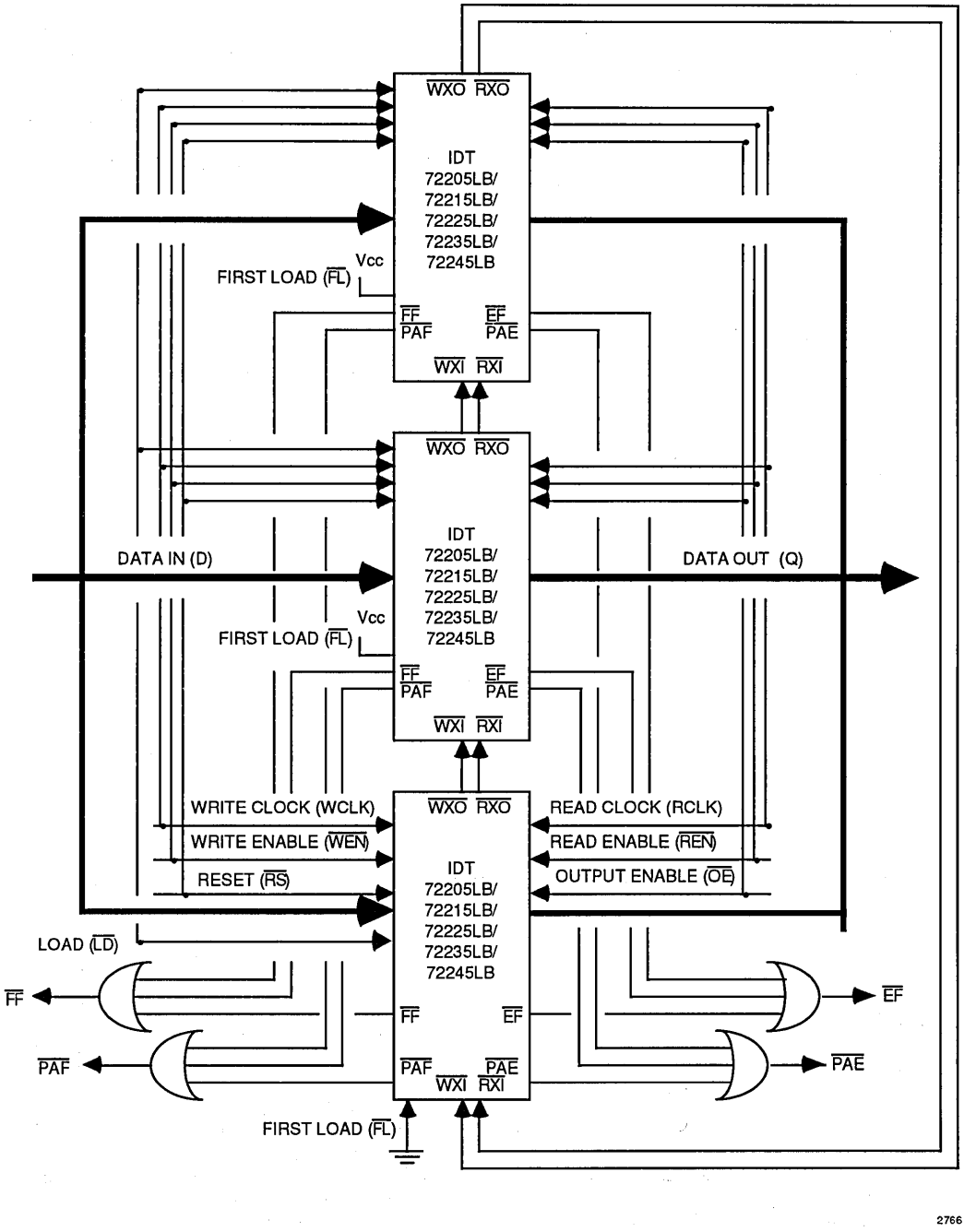
NOTE:
1. Do not connect any output control signals directly together.

Figure 21. Block Diagram of 256 x 36/512 x 36/1024 x 36/2048 x 36/4096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72205LB/72215LB/72225LB/72235LB/72245LB can easily be adapted to applications requiring more than 256/512/1024/2048/4096 words of buffering. Figure 22 shows Depth Expansion using three IDT72205LB/72215LB/72225LB/72235LB/72245LBs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the high state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of the next device. See Figure 24.
4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device. See Figure 24.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in the Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together every respective flags for monitoring. The composite PAE and PAF flags are not precise.



2766 drw 24

Figure 22. Block Diagram of 768 x 18/1536 x 18/3072 x 18/6144 x 18/12288 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

Integrated Device Technology, Inc.

CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

IDT72401
IDT72402
IDT72403
IDT72404

FEATURES:

- First-In/First-Out dual-port memory
- 64 x 4 organization (IDT72401/03)
- 64 x 5 organization (IDT72402/04)
- IDT72401/02 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low power consumption
  — Active: 175mW (typ.)
- Maximum shift rate — 45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in CERDIP, plastic DIP and SOIC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86846 and 5962-89523 is listed on this function.

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous high-performance First-In/First-Out memories organized as 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input ($D_{0-D3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output remains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The Output Ready can also be used to cascade multiple devices together.

Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

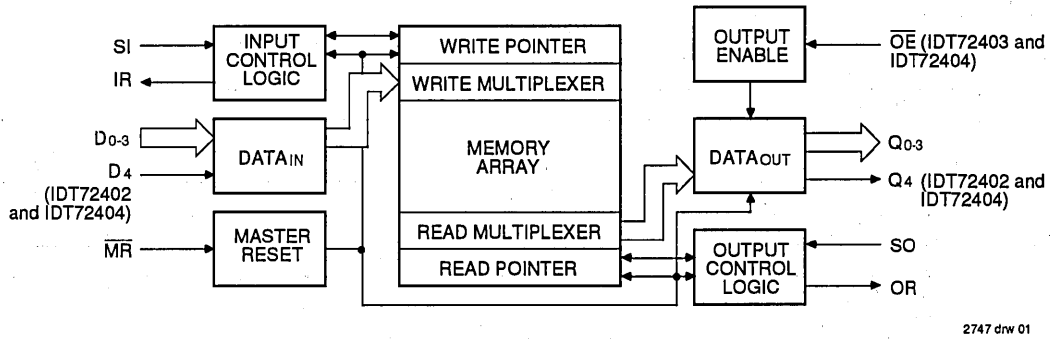
Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

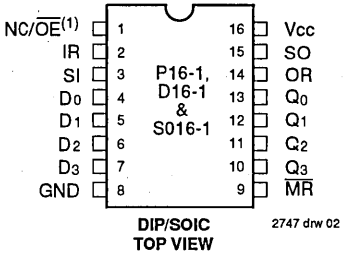
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

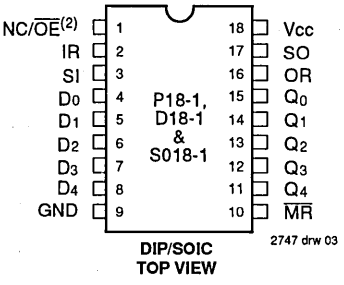
IDT72401/IDT72403



DIP/SOIC TOP VIEW

2747 drw 02

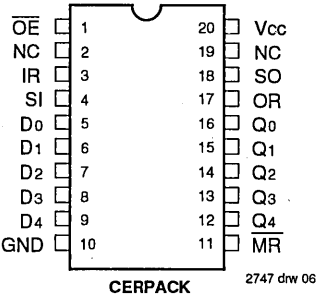
IDT72402/IDT72404



DIP/SOIC TOP VIEW

2747 drw 03

(IDT72404 Only)



CERPACK TOP VIEW

2747 drw 06

NOTES:
1. Pin 1: NC - No Connection IDT72401, $\overline{OE}$ - IDT72403
2. Pin 1: NC - No Connection IDT72402,$\overline{OE}$ - IDT72404

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temp.	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temp.	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2747 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Mil. Supply Voltage	4.5	5.0	5.5	V
Vcc	Com'l. Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL(1)	Input High Voltage	—	—	0.8	V

NOTE: 2747 tbl 03
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2747 tbl 02
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
VIC(1)	Input Clamp Voltage			—	—	—
VIL	Low-Level Input Current	Vcc = Max., GND ≤ VI ≤ Vcc		-10	—	µA
VIH	High-Level Input Current	Vcc = Max., GND ≤ VI ≤ Vcc		—	10	µA
VOL	Low-Level Output Current	Vcc = Min., IOL = 8mA		—	0.4	V
VOH	High-Level Output Current	Vcc = Min., IOH = -4mA		2.4	—	V
IOS(2)	Output Short-Circuit Current	Vcc = Max., VO = GND		-20	-90	mA
IHZ	Off-State Output Current	Vcc = Max., VO = 2.4V		—	20	µA
ILZ	(IDT72403 and IDT72404)	Vcc = Max., VO = 0.4V		-20	—	µA
ICC(3, 4)	Supply Current	Vcc = Max., f = 10MHz	Com'l.	—	35	mA
			Military	—	45	

NOTES: 2747 tbl 04
1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Guaranteed but not tested.
3. Icc measurements are made with outputs open. $\overline{OE}$ is HIGH for IDT72403/72404.
4. For frequencies greater than 10MHZ, Icc = 35mA + (1.5mA x [f - 10MHz]) commercial, and Icc = 45mA + (1.5mA x [f - 10MHz]) military.

OPERATING CONDITIONS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	11	—	11	—	11	—	ns
t_{SIL}	Shift in LOW TIme	2	11	—	17	—	24	—	25	—	30	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	20	—	30	—	40	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	11	—	11	—	11	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	24	—	25	—	25	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	25	—	25	—	25	—	30	—	ns
t_{MRS}	Master Reset Pulse to SI	8	10	—	10	—	10	—	25	—	35	—	ns
t_{SIR}	Data Set-up to IR	4	3	—	3	—	5	—	5	—	5	—	ns
t_{HIR}	Data Hold from IR	4	13	—	15	—	20	—	30	—	30	—	ns
t_{SOR}[4]	Data Set-up to OR HIGH	7	0	—	0	—	0	—	0	—	0	—	ns

2747 tbl 05

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{IN}	Shift In Rate	2	—	45	—	35	—	25	—	15	—	10	MHz
t_{IRL}[1]	Shift In to Input Ready LOW	2	—	18	—	18	—	21	—	35	—	40	ns
t_{IRH}[1]	Shift In to Input Ready HIGH	2	—	18	—	20	—	28	—	40	—	45	ns
t_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	—	15	—	10	MHz
t_{ORL}[1]	Shift Out to Output Ready LOW	5	—	18	—	18	—	19	—	35	—	40	ns
t_{ORH}[1]	Shift Out to Output Ready HIGH	5	—	19	—	20	—	34	—	40	—	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	—	5	—	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift (Next Word)	5	—	19	—	20	—	34	—	40	—	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	30	—	34	—	40	—	65	—	65	ns
t_{MRORL}	Master Reset to OR LOW	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	—	20	—	20	—	25	—	35	—	40	ns
t_{OOE}[3]	Output Valid from $\overline{OE}$ LOW	9	—	12	—	15	—	20	—	30	—	35	ns
t_{HZOE}[3,4]	Output HIGH-Z from $\overline{OE}$ HIGH	9	—	12	—	12	—	15	—	25	—	30	ns
t_{IPH}[2,4]	Input Ready Pulse HIGH	4	9	—	9	—	11	—	11	—	11	—	ns
t_{OPH}[2,4]	Ouput Ready Pulse HIGH	7	9	—	9	—	11	—	11	—	11	—	ns

NOTES:

2747 tbl 06

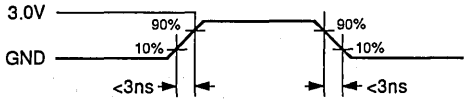
1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between Vcc and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 and IDT72404 only.
4. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

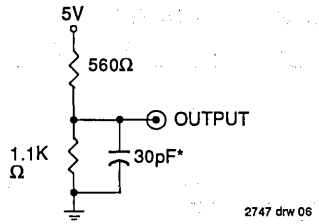
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2754 tbl 07

ALL INPUT PULSES:



2747 drw 05



2747 drw 06

or equivalent circuit

Figure 1. AC Test Load

*Including scope and jig

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT (D0-3, 4)

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input. The IDT72402 and IDT72404 have a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the Do-3, 4 lines.

SHIFT OUT (SO)

Shift Out controls the output of data of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output (Qo-3, 4) lines.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Qo-3, 4) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE ($\overline{OE}$) (IDT72403 AND IDT72404 ONLY)

Output enable is used to read FIFO data onto a bus. Output Enable is active LOW.

OUTPUTS:

DATA OUTPUT (Qo-3, 4)

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output. The IDT72402 and IDT72404 have a 5-bit data output.

FUNCTIONAL DESCRIPTION

These 64 x 4 and 64 x 5 FIFOs are designed using a dual port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO Reset

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Qo-3, 4) will be LOW.

Data Input

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH, indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

Data Output

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out. Previous data remains on the output until the HIGH-to-LOW transition of Shift Out (SO).

Fall-Through Mode

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO.

TIMING DIAGRAMS

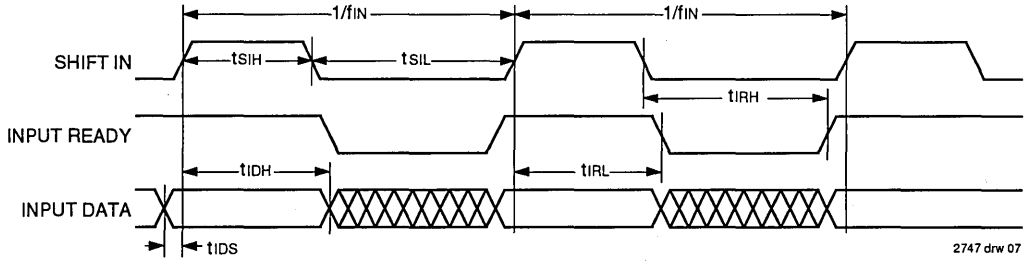
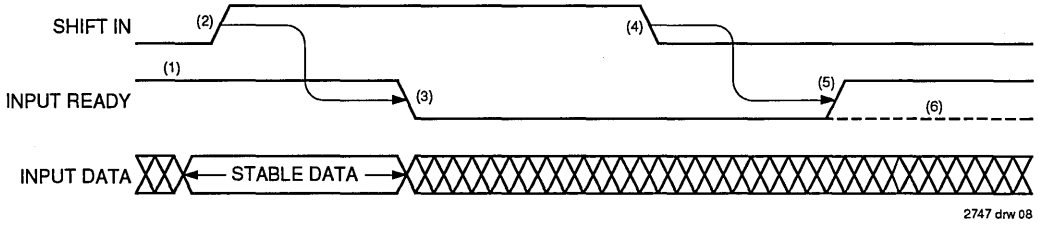


Figure 2. Input Timing

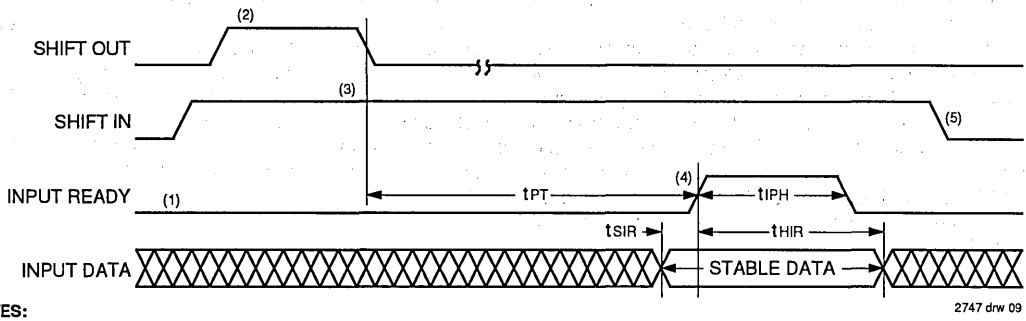


NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the Input Ready remains LOW.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

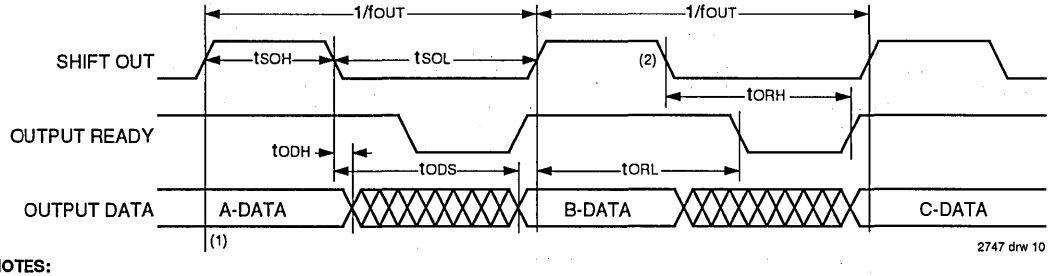
Figure 3. The Mechanism of Shifting Data Into the FIFO

TIMING DIAGRAMS (Continued)



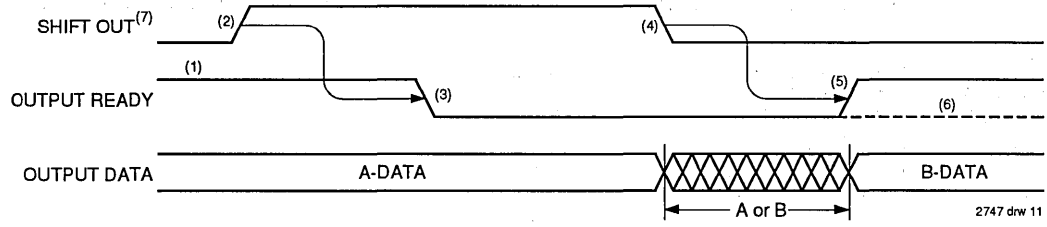
NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

Figure 4. Data Is Shifted In Whenever Shift In and Input Ready are Both HIGH



NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

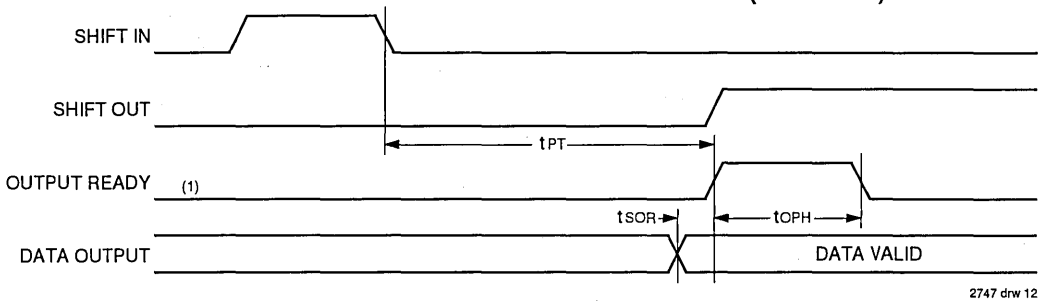


NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. The read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then Output Ready stays LOW and the A DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

Figure 6. The Mechanism of Shifting Data Out of the FIFO

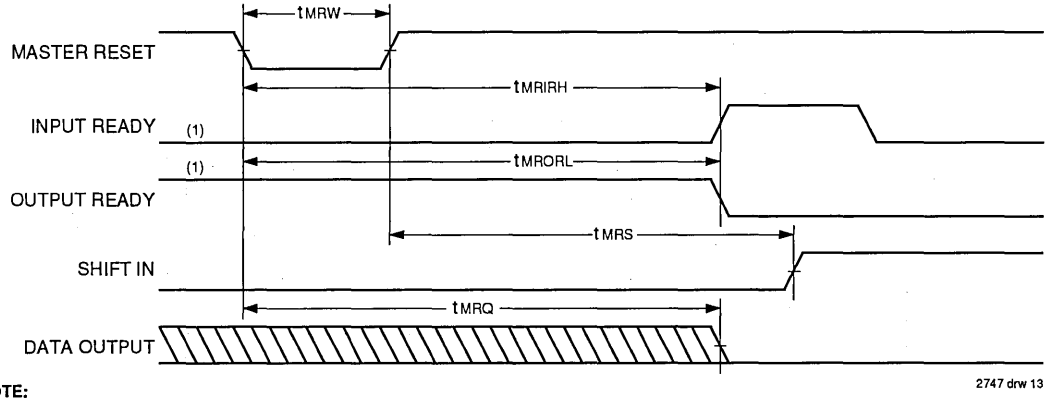
TIMING DIAGRAMS (Continued)

TIMING DIAGRAMS (Continued)



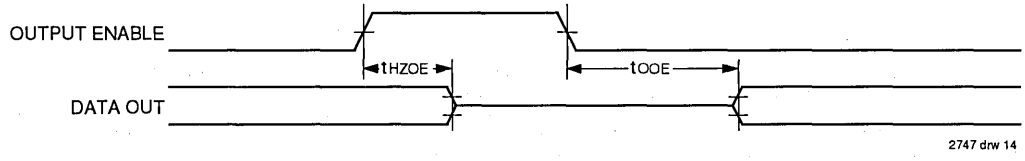
NOTE:
1. FIFO initially empty.

Figure 7. tPT and tOPH Specification



NOTE:
1. Worst case, FIFO initially full.

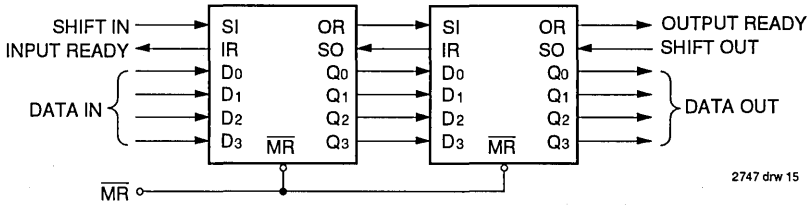
Figure 8. Master Reset Timing



NOTE:
1. High-Z transitions are referenced to the steady-state VOH -500mV and VOL +500mV levels on the output. tHZOE is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

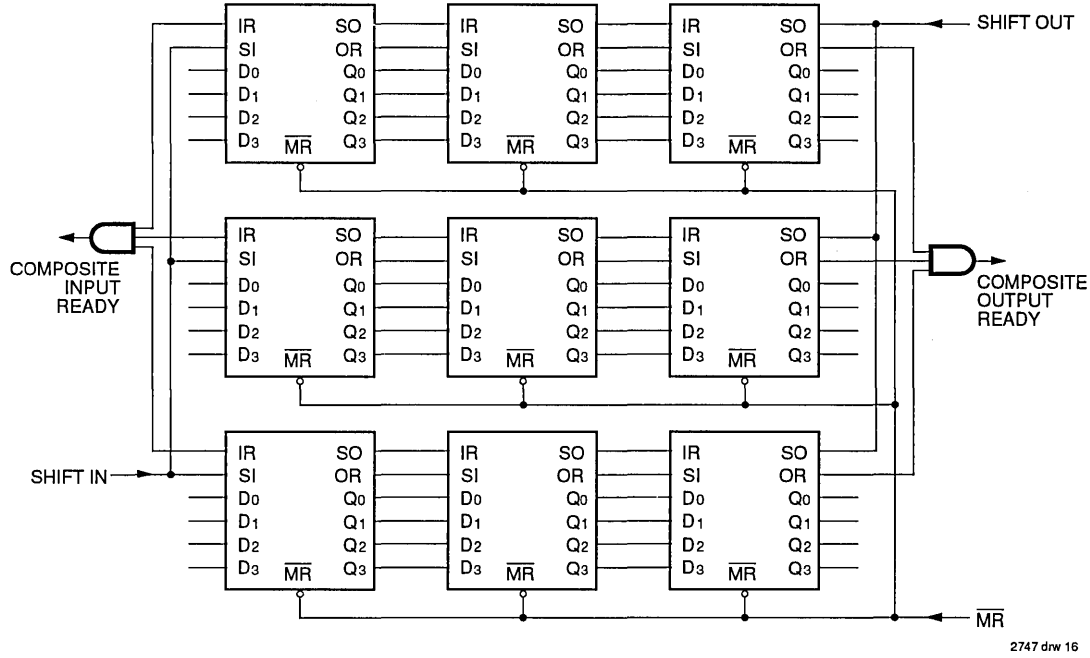
Figure 9. Output Enable Timing, IDT72403 and IDT72404 Only

APPLICATIONS



NOTE:
1. FIFOs can be easily cascaded to any desired path. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 10. 128 x 4 Depth Expansion



NOTES:
1. When the memory is empty, the last word will remain on the outputs until the Master Reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the Master Reset is brought Low, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the Master Reset goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the Master Reset is ended, IR will go HIGH, but the data in the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable on depth and width. However, in forming wider words, two external gates are required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT72413

FEATURES:

- First-In/First-Out dual-port memory—45MHz
- 64 x 5 organization
- Low power consumption
  - — Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CEMOS™ technology
- Available in plastic DIP, CERDIP and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72413 is a 64 x 5, high speed First-In/First-Out (FIFO) that loads and empties data on a first-in-first-out basis. It is expandable in bit width. All speed versions are cascadable in depth.

The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

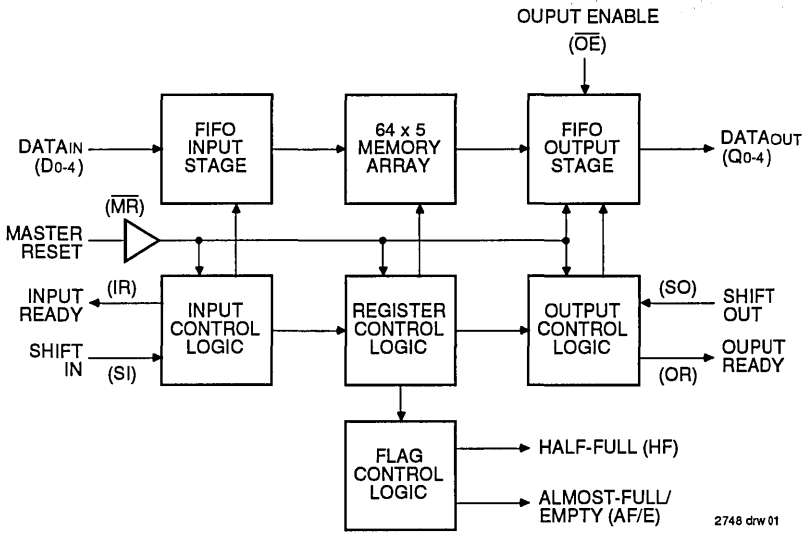
The IDT72413 is pin and functionally compatible to the MMI67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

The IDT72413 is fabricated using IDTs high-performance CEMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

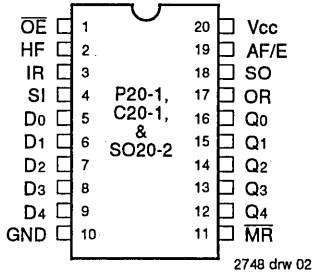
5

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2748 drw 02

DIP/SOIC
TOP VIEW

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}[1]	Input Low Voltage	—	—	0.8	V

NOTE: 2748 tbl 03
1. 1.5V undershoots are allowed for 10ns once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2748 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2748 tbl 02
1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently listed.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions			Min.	Max.	Unit
V_{IC}[1]	Input Clamp Voltage				—	—	
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			-10	—	µA
I_{IH}	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}			—	10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min.	I_{OL} (Q_{0-4})	Mil. 12mA	—	0.4	V
				Com'l. 24mA			
			I_{OL} (IR, OR)[2]	8mA			
			I_{OL} (HF, AF/E)	8mA			
V_{OH}	High-Level Output Current	V_{CC} = Min.	I_{OH} (Q_{0-4})	-4mA	2.4	—	V
			I_{OH} (IR, OR)	-4mA			
			I_{OH} (HF, AF/E)	-4mA			
I_{OS}[3]	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V		-20	-90	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max.	V_O = 2.4V		—	20	µA
I_{LZ}		V_{CC} = Max.	V_O = 0.4V		-20	—	
I_{CC}[4]	Supply Current	V_{CC} = Max., $\overline{OE}$=HIGH		Mil.	—	70	mA
		Inputs LOW, f=25MHz		Com'l.	—	60	

NOTES: 2748 tbl 04

1. FIFO is able to withstand a -1.5V undershoot for less than 10ns.
2. Care should be taken to minimize as much as possible the DC and capactive load on IR and OR when operating at frequencies above 25mHz.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Guaranteed by design, but not currently tested.
4. For frequencies greater than 25MHz, I_{CC} = 60mA + (1.5mA x [f - 25MHz]) commercial and I_{CC} = 70mA + (1.5mA x [f - 25MHz]) military.

5

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

			Military		Military & Commercial		Commercial		
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	16	—	ns
t_{SIL}[1]	Shift in LOW TIme	2	11	—	17	—	20	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	25	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	16	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	20	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	30	—	35	—	ns
t_{MRS}[3]	Master Reset Pulse to SI	8	20	—	35	—	35	—	ns

NOTE: 2748 tbl 05

1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C to +125°C)

			Military		Military & Commercial				
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	—	18	—	18	—	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	—	18	—	20	—	25	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	—	18	—	18	—	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	—	19	—	20	—	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift Next Word	5	—	19	—	20	—	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	25	—	28	—	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	—	25	—	28	—	30	ns
t_{MRIRH}[3]	Master Reset ↑ to Input Ready HIGH	8	—	25	—	28	—	30	ns
t_{MRIRL}[2]	Master Reset ↓ to Input Ready LOW	8	—	25	—	28	—	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	—	20	—	25	—	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	—	25	—	28	—	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	—	25	—	28	—	40	ns
t_{IPH}[3]	Input Ready Pulse HIGH	4	5	—	5	—	5	—	ns
t_{OPH}[3]	Ouput Ready Pulse HIGH	7	5	—	5	—	5	—	ns
t_{ORD}[3]	Output Ready ↑ HIGH to Valid Data	5	—	5	—	5	—	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	—	28	—	28	—	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	—	28	—	28	—	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	—	28	—	28	—	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	—	28	—	28	—	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	—	28	—	28	—	40	ns
t_{HFL}	Shif Out ↑ to HF LOW	11	—	28	—	28	—	40	ns
t_{PHZ}[3]	Output Disable Delay	12	—	12	—	12	—	15	ns
t_{PLZ}[3]		12	—	12	—	12	—	15	
t_{PLZ}[3]	Output Enable Delay	12	—	15	—	15	—	20	ns
t_{PHZ}[3]		12	—	15	—	15	—	20	

NOTES:

2748 tbl 06

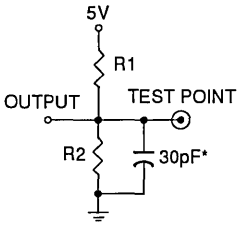
1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1μF directly between VCC and GND with very short lead length is recommended.
2. If the FIFO is full, (IR = HIGH), $\overline{MR}$ ↓ forces IR to go LOW, and $\overline{MR}$ ↑ causes IR to go HIGH.
3. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

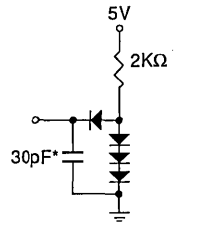
2754 tbl 08

STANDARD TEST LOAD



or equivalent circuit

DESIGN TEST LOAD



2748 drw 03

*Including scope and jig

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

Figure 1. Output Load

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a Shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D0-4 lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the outputs data from the FIFO.

MASTER RESET ($\overline{MR}$)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY(IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data, Input Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT ENABLE ($\overline{OE}$)

Output Enable is used to enable the FIFO outputs onto a bus. Output Enable is active LOW.

ALMOST-FULL/EMPTY FLAG (AFE)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

TIMING DIAGRAMS

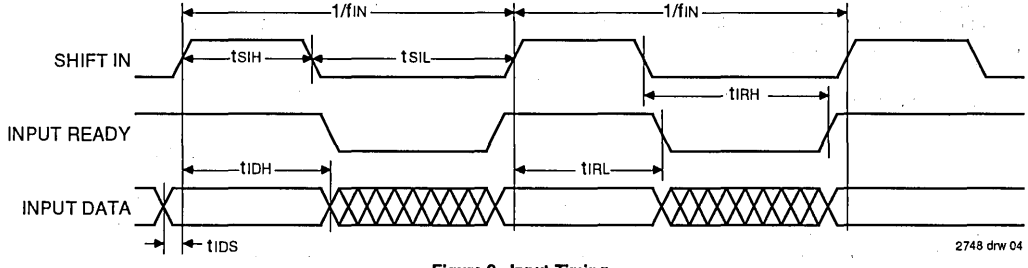
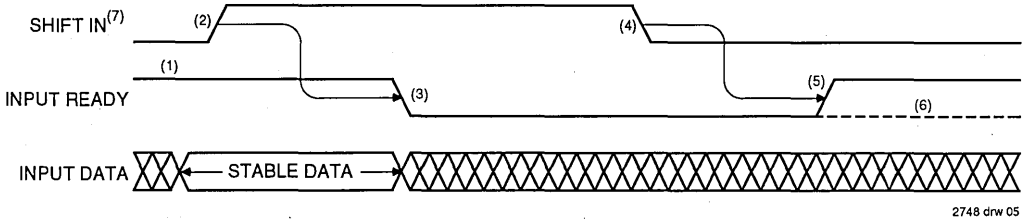


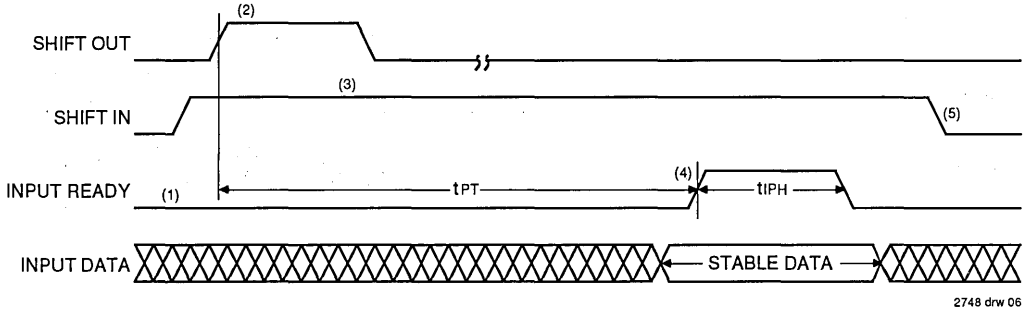
Figure 2. Input Timing

TIMING DIAGRAMS (Continued)



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. **Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).**

Figure 3. The Machanism of Shifting Data Into the FIFO

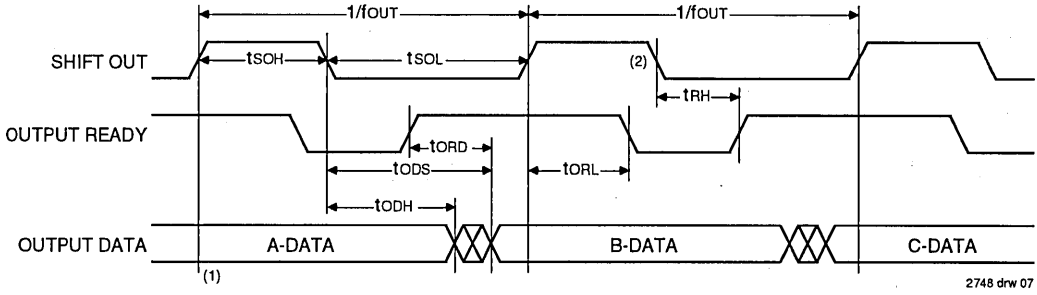


NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

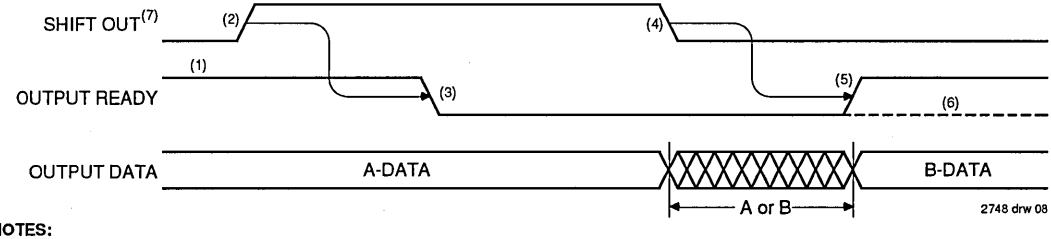
5

TIMING DIAGRAMS (Continued)



NOTES:
1. This data is loaded consecutively A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

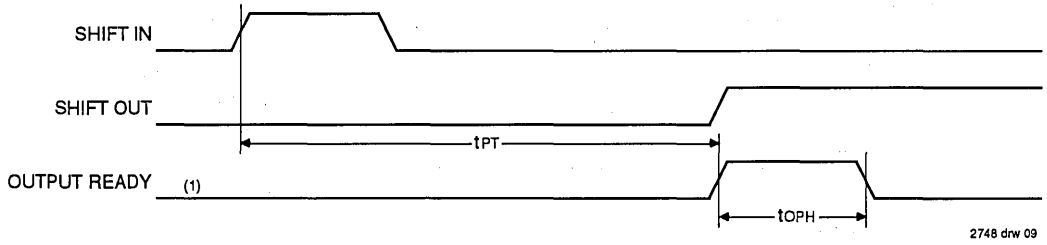
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after tORD ns.
6. If the FIFO has only one word loaded (A DATA) , Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

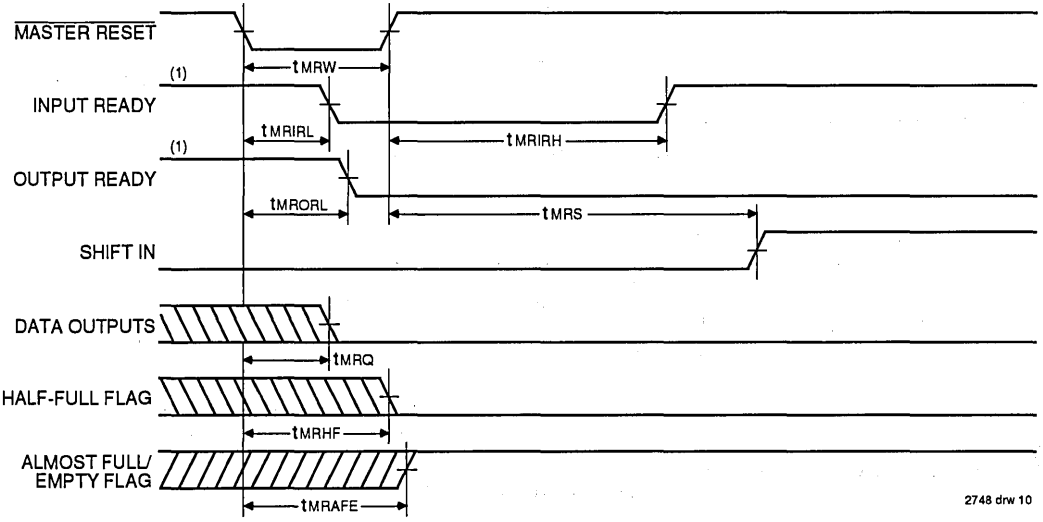
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO initailly empty.

Figure 7. tPT and tOPH Specification

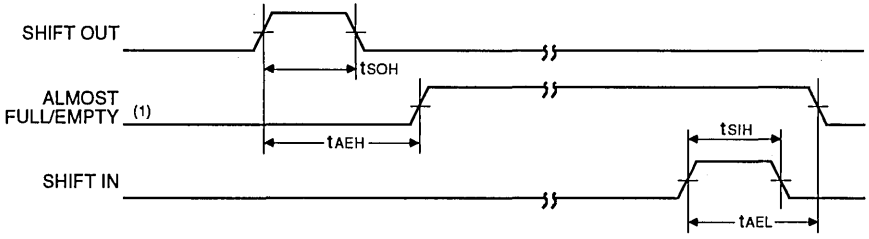


NOTE:
1. FIFO is partially full.

Figure 8. Master Reset Timing

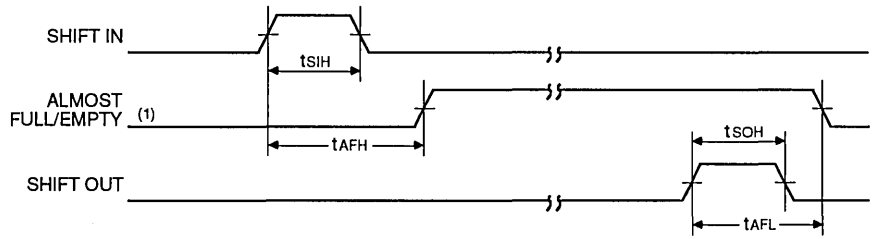
5

TIMING DIAGRAMS (Continued)



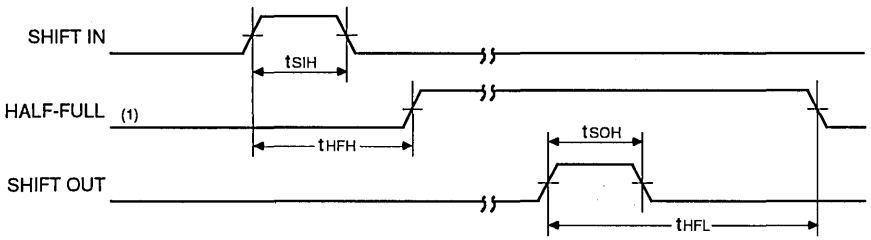
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. t_{AEH} and t_{AEL} Specifications



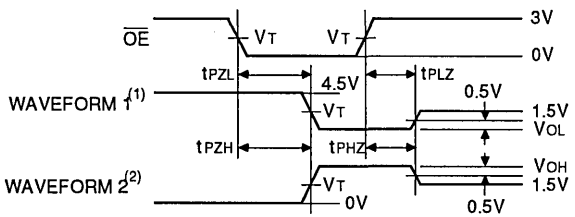
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. t_{AFH} and t_{AFL} Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

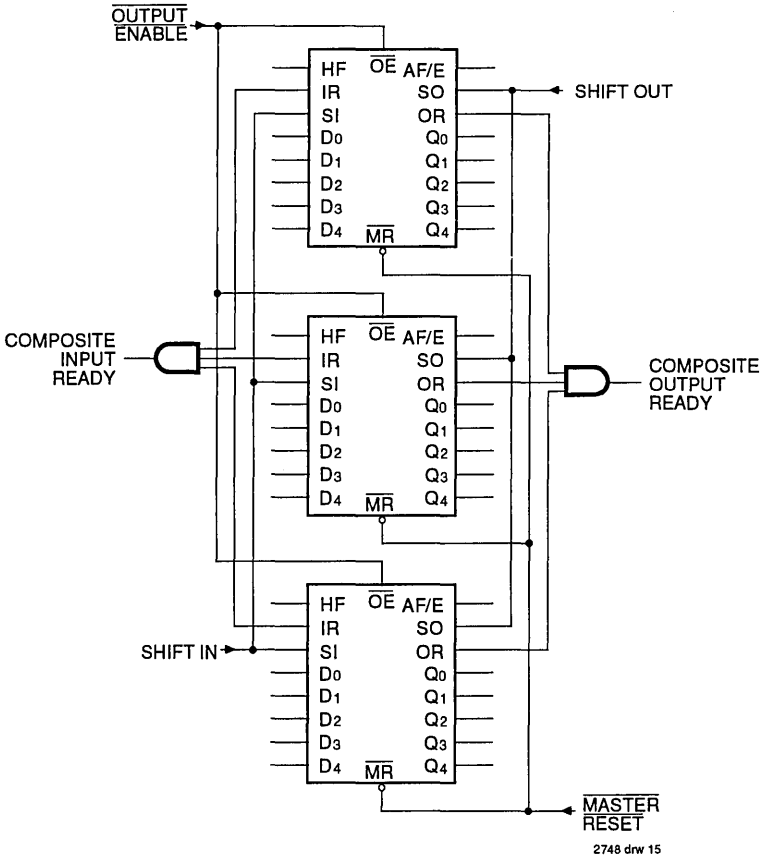
Figure 11. t_{HFL} and t_{HFH} Specifications



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

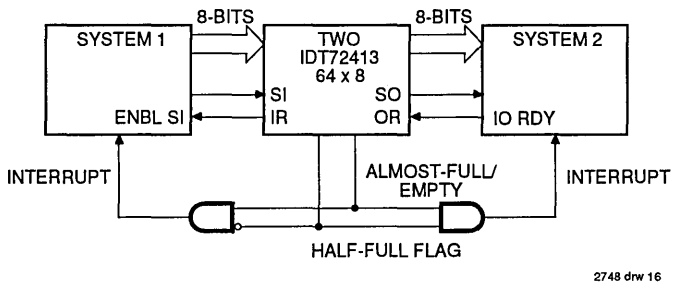
Figure 12. Enable and Disable

APPLICATIONS



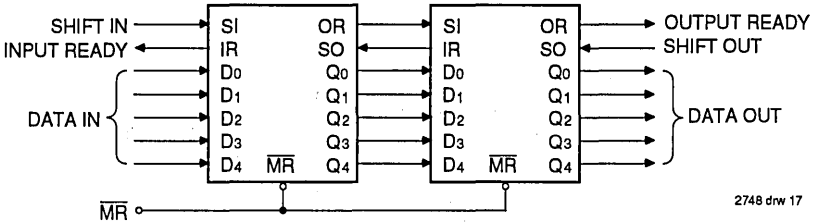
NOTE:
1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

Figure 13. 64 x 15 FIFO with IDT72413



NOTE:
1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

Figure 14. Application for IDT72413 for Two Asynchronous Systems



NOTE:
1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

Integrated Device Technology, Inc.

BUS-MATCHING BIDIRECTIONAL FIFO 512 x 18-BIT – 1024 x 9-BIT 1024 x 18-BIT – 2048 x 9-BIT

IDT7251 IDT7252 IDT72510 IDT72520

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18 - Bit – 1024 x 9 - Bit (IDT7251, IDT72510)
- 1024 x 18 - Bit – 2048 x 9 - Bit (IDT7252, IDT72520)
- 18 bit data bus on Port A side and 9 bit data bus on Port B side
- Can be configured for 18-to-9-bit, 36-to-9-bit, or 36-to-18-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight internal flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities.
- On-chip parity checking and generation
- Standard DMA control pins for data exchange with peripherals
- IDT7251 and IDT7252 available in 48-pin plastic or ceramic DIP
- IDT72510 and IDT72520 available in 52-pin PLCC packages (includes LDRER, LDREW, RESET, and one extra GND pin)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7251, IDT72510, IDT7252, and IDT72520 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. The BiFIFOs incorporate bus matching logic to convert the 18-bit wide memory data paths to the 9-bit wide Port B data bus. The BiFIFOs have a bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

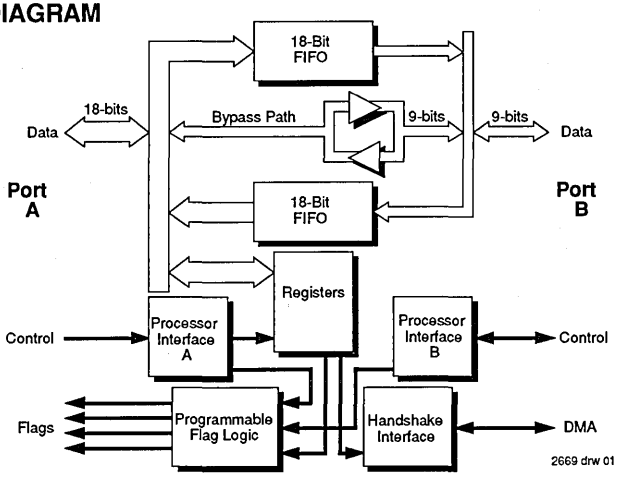
Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFOs have programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLG_A-FLG_D) through one Configuration Register.

Port B has parity, reread/rewrite and DMA functions. Parity generation and checking can be done by the BiFIFO on data passing through Port B. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFOs have three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

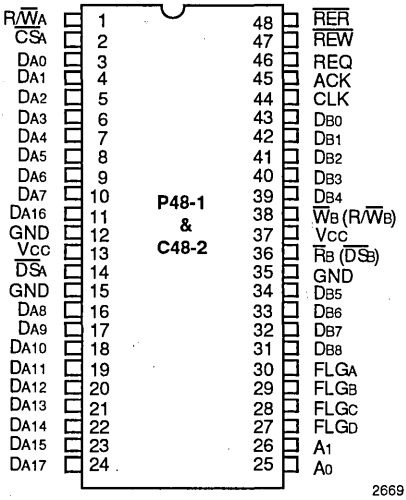
5

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATIONS

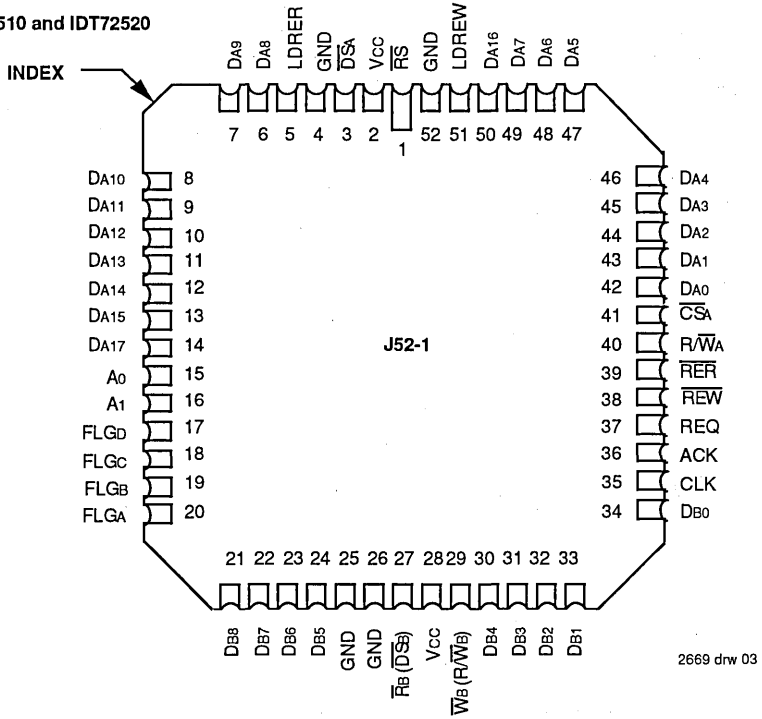
IDT7251 and IDT7252



2669 drw 02

DIP
TOP VIEW

IDT72510 and IDT72520



2669 drw 03

PLCC
TOP VIEW

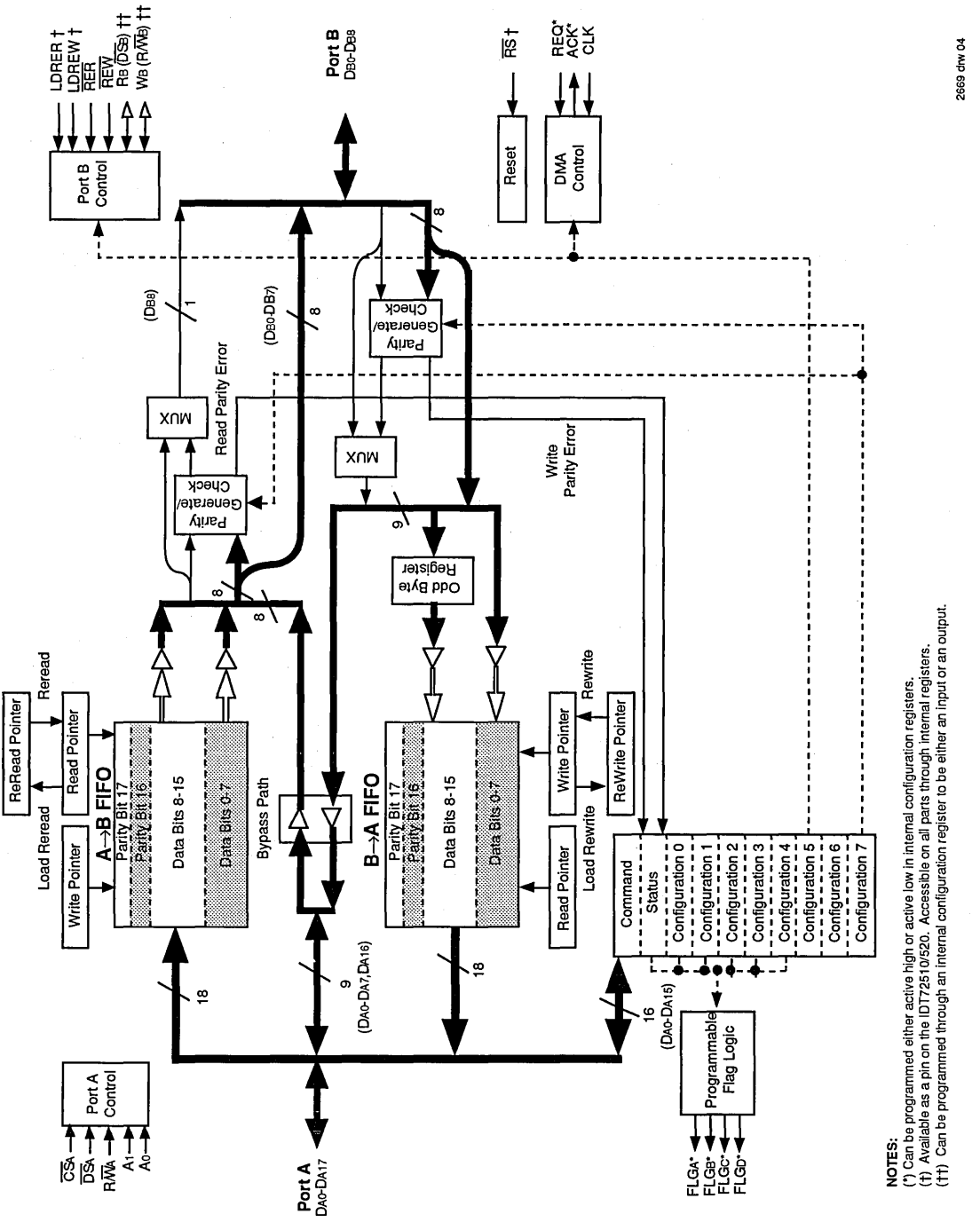
PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_{A0}-D_{A15}	Data A	I/O	Data inputs and outputs for 16 bits of the 18-bit Port A bus.
D_{A16}-D_{A17}	Parity A	I/O	D_{A16} is the parity bit for D_{A0}-D_{A7}. D_{A17} is the parity bit for D_{A8}-D_{A15}. D_{A16} and D_{A17}can be used as two extra data bits if the parity generate function is disabled.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
$R/\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is LOW, data is written into Port A on the rising edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B7}	Data B	I / O	Data inputs & outputs for 8 bits of the 9-bit Port B bus.
D_{B8}	Parity B	I / O	D_{B8} is the parity bit for D_{B0}-D_{B7}. D_{B8} can be used as a data bit if the parity generate function is disabled.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$or written on the rising edge of $\overline{DS}_B$through Port B. The Default is Intel-style processor mode ($\overline{R}_B$ as an input).
$\overline{W}_B$ ($R/\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface ($R/\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read ($R/\overline{W}_B$ = HIGH) or written ($R/\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The Default is Intel-style processor mode ($\overline{W}_B$ as an input).
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH. This signal is a pin on the IDT72510/520; it is accessible through the Command Register on all four parts.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH. This signal is a pin on the IDT72510/520; it is accessible through the Command Register on all four parts.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and $R/\overline{W}_B$ when Port B is in the peripheral mode.
FLG_A-FLG_D	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full, and Full. If parity checking is enabled, the FLG_A pin can also be assigned as a parity error output.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions. Hardware reset pin is only available for IDT72510/72520. Software reset can be achieved through command register for all four devices.
V_{CC}	Power		There are two +5V power pins on all four devices.
GND	Ground		There are three Ground pins at 0V for the IDT7251/52. There are four ground pins for the IDT72510/520.

2669 tbl 01

5

DETAILED BLOCK DIAGRAM



NOTES:
(*) Can be programmed either active high or active low in internal configuration registers.
(†) Available as a pin on the IDT72510/520. Accessible on all parts through internal registers.
(††) Can be programmed through an internal configuration register to be either an input or an output.

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFOs can be used in three different bus configurations: 18 bits to 9 bits, 36 bits to 9 bits and 36 bits to 18 bits. One BiFIFO can be used for the 18- to 9-bit configuration, and two BiFIFOs are required for 36- to 9-bit or 36- to 18-bit configurations. Bits 11 and 12 of Configuration Register 5 determine the BiFIFO configuration (see Table 11 for Configuration Register 5 format).

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFOs. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFOs, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 9-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 9-bit processor or a 9-bit peripheral. Bits 11 and 12 of Configuration Register 5 should be set to **00** for a stand-alone configuration. Figures 1 and 2 show the BiFIFO in 18- to 9-bit configurations for processor and peripheral interface modes respectively.

36- to 9-bit Configurations

Two BiFIFOs can be hooked together to create a 36-bit to 9-bit configuration. This means that a 36-bit processor can talk to a 9-bit processor or a 9-bit peripheral. Both BiFIFOs are programmed simultaneously through Port A by placing one command word on the most significant 16 data bits and one command word on the least significant 16 data bits (parity bits should be ignored).

One BiFIFO must be programmed as the master device and the other BiFIFO is the slave device. Bits 11 and 12 of Configuration Register 5 are set to 10 for the slave device and **11** for the master device. The first two 9-bit words on Port B are read from or written to the slave device and the next two 9-bit words go to the master device.

When both BiFIFOs are in peripheral interface mode, the Port B interface pins of the master device are outputs and this BiFIFO controls the bus. The Port B interface pins of the slave device are inputs driven by the master BiFIFO. Two BiFIFOs are connected in Figure 4 to create a 36- to 9-bit peripheral interface.

The two BiFIFOs shown in Figure 3 are configured to connect a 36-bit processor to a 9-bit processor.

36-BIT PROCESSOR to 18-BIT PROCESSOR CONFIGURATION

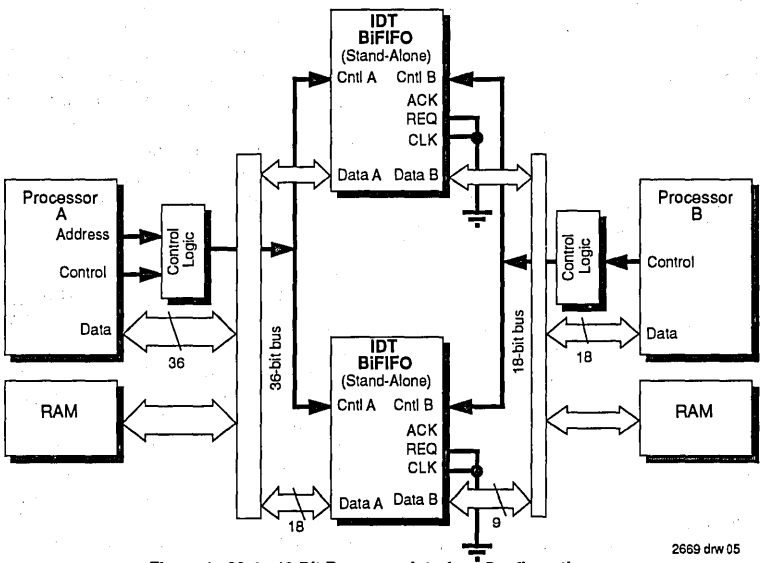


Figure 1. 36- to 18-Bit Processor Interface Configuration

NOTE:
1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36-BIT PROCESSOR to 18-BIT PERIPHERAL CONFIGURATION

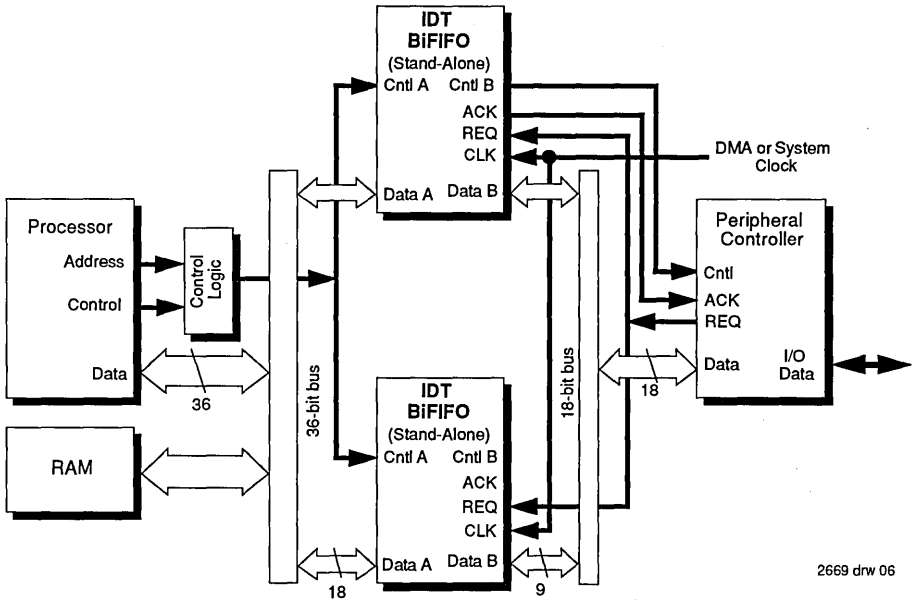


Figure 2. 36- to 18-Bit Peripheral Interface Configuration

NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36- to 18-bit Configurations

In a 36- to 18-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 16 data bits to each device with the 4 parity bits ignored.

Both BiFIFOs must be programmed into stand-alone mode for a 36-bit processor to communicate with an 18-bit processor or an 18-bit peripheral. This means that bits 11 and 12 of Configuration Register 5 must be set to **00**.

This configuration can be extended to wider bus widths (54- to 27-bits, 72- to 36-bits, ...) by adding more BiFIFOs to the configuration. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the set-up and hold time requirements for these pins are met during reset. Figures 1 and 3 show BiFIFOs in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in the peripheral interface mode. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, both pins should be pulled-up to V_{CC} with 10K resistors.

If the BiFIFOs are in stand-alone configuration mode (18-to 9-bit, 36- to 18-bit, ...), then the Port B interface pins are all outputs. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows stand-alone configuration BiFIFOs connected to a peripheral.

In a 36- to 9-bit configuration, the master device controls the bus. The Port B interface pins of the master device are outputs and the interface pins of the slave device are inputs. A 36- to 9-bit configuration of two BiFIFOs connected to a peripheral is shown in Figure 4.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte with parity (DA_0-DA_7, DA_{16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (DA_0-DA_{15}) are passed by Port A.

36-BIT PROCESSOR to 9-BIT PROCESSOR CONFIGURATION

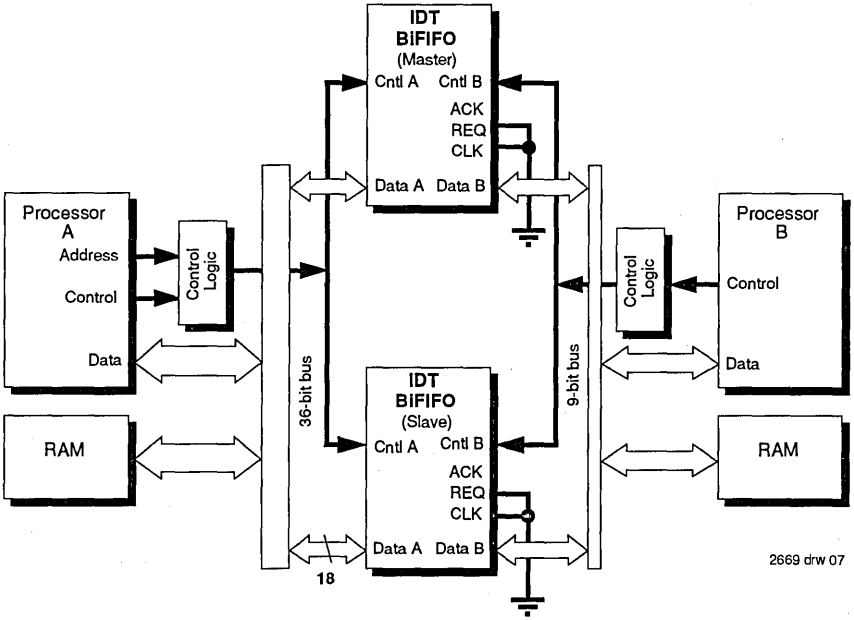


Figure 3. 36- to 9-Bit Processor Interface Configuration

NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

5

36-BIT PROCESSOR to 9-BIT PERIPHERAL CONFIGURATION

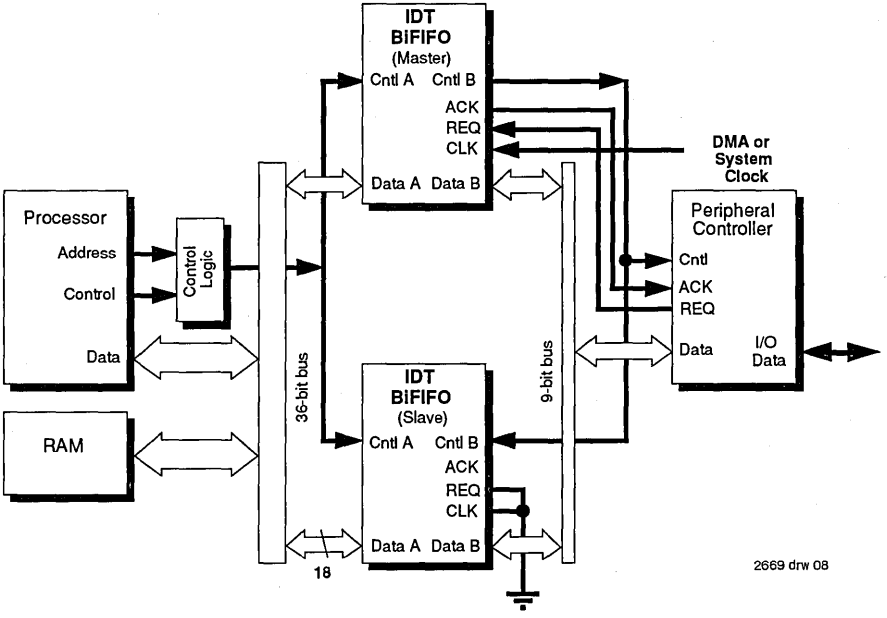


Figure 4. 36- to 9-Bit Peripheral Interface Configuration

NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

PORT A RESOURCES

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

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Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0, and A_1

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 9-bit configuration or in a 36- to 9-bit configuration. Only in the 36- to 18-bit configuration is the bypass path 18 bits wide.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 11) is set to **1** for peripheral interface mode. In a 36- to 9-bit configuration, both Port B data buses will be active. Data written into Port A will appear on both master and slave Port B buses concurrently. To avoid Port B bus contention, the data on D_{A0}-D_{A7} and D_{A16} of both BiFIFOs should be exactly the same. Data read from Port A will appear on pins D_{A0}-D_{A7} and D_{A16} of both BiFIFOs within the same 36-bit word.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 5. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, to modify the Port B Read and Write Pointers, and to clear Port B parity errors. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by changing the Port B Read Pointer with the Reread Pointer or by changing the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

The BiFIFO supports two Status Register formats. Status Register format 1 gives all the internal flag status, while Status Register format 0 provides the data in the Odd Byte Register. Table 6 gives the operands for selecting the appropriate Status Register format. See Table 8 for the details of the two Status Register formats.

Two commands are provided to increment the Port B Read and Write Pointers in case reread/rewrite is performed. Incrementing the pointers guarantees that pointers will be on a word boundary when an odd number of bytes is transmitted through Port B. No operands are required for these commands.

When parity check errors occur on Port B, a clear parity error command is needed to remove the parity error. There are no operands for these commands.

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Set Status Register Format (see Table 6)
1000	Increment in byte for A→B FIFO Read Pointer (Port B)
1001	Increment in byte for B→A FIFO Write Pointer (Port B)
1010	Clear Write Parity Error Flag
1011	Clear Read Parity Error Flag

2669 tbl 03

Table 2. Functions Performed by Port A Commands

Reset

The IDT72510 and IDT72520 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set

COMMAND FORMAT

15			12	11	8	7			3	2	0
X	X	X	X	Command Opcode		X	X	X	X	X	Command Operand

2669 tbl 04

Figure 5. Format for Commands Written into Port A

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2669 tbl 05

Table 3. Reset Command Functions

to **6420H**, and Configuration Registers 5 and 7 are **0000H**. Additionally, Status Register format 0 is selected, all the pointers including the Reread and Rewrite Pointers are set to **0**, the odd byte register valid bit is cleared, the DMA direction is set to B→A write, the internal DMA request circuitry is cleared (set to its initial state), and all parity errors are cleared.

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The request (REQ) DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 7 shows the BiFIFO state after the different hardware and software resets.

SELECT CONFIGURATION REGISTER COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2669 tbl 06

Table 4. Select Configuration Register Command Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2669 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATUS REGISTER FORMAT COMMAND FUNCTIONS

Operands	Function
XX0	Status Register Format 0
XX1	Status Register Format 1

2669 tbl 08

Table 6. Command Functions to Set the Status Register Format

5

STATE AFTER RESET

	Hardware Reset	Software Reset				
	($\overline{RS}$ asserted, IDT72510 & IDT72520 only)	B→A (001)	A→B (010)	B→A and A→B (011)	Internal Request (100)	All (111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
Odd byte register valid bit	clear	clear	—	clear	—	clear
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear
Parity errors	clear	—	—	—	—	—

2669 tbl 09

Table 7. The BiFIFO State After a Reset Command

Status Register

The Status Register reports the state of the programmable flags, the DMA read/write direction, the Odd Byte Register valid bit, and parity errors. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1).

There are two Status Register formats that are set by a Status Register format command. Format **0** stores the Odd Byte Register data in the lower eight bits of the Status Register, while format **1** reports the flag states and the DMA read/write direction in the lower eight bits. The upper eight bits are identical for both formats. The flag states, the parity errors, the Odd Byte Register valid bit, and the Status Register format are all in the upper eight bits of the Status Register. See Table 8 for both Status Register formats.

Configuration Registers

The eight Configuration Register formats are shown in Table 9. Configuration Registers 0-3 contain the programmable flag offsets for the Almost Empty and Almost Full flags. These offsets are set to **0** when a hardware reset or a software reset all is applied. Note that Table 9 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 10. The default condition for Configuration Register 4 is **6420H** as shown in Table 7. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 11. Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bit 1 changes the byte order for data coming through Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK, respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Bits 11 and 12 set the width expansion mode. For 18- to 9-bit configurations or 36- to 18-bit configurations, the BiFIFO should be set in stand-alone mode. For a 36- to 9-bit configuration, one BiFIFO must be in slave mode and the other BiFIFO must be in master mode. The master BiFIFO allows the first two bytes transferred across Port B to go to the slave BiFIFO, then the next two bytes go to the master BiFIFO.

Configuration Register 7 controls the parity functions of Port B as shown in Table 12. Either parity generation or parity

STATUS REGISTER FORMAT 0

Bit	Signal
0	Odd Byte Register
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 0
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 10

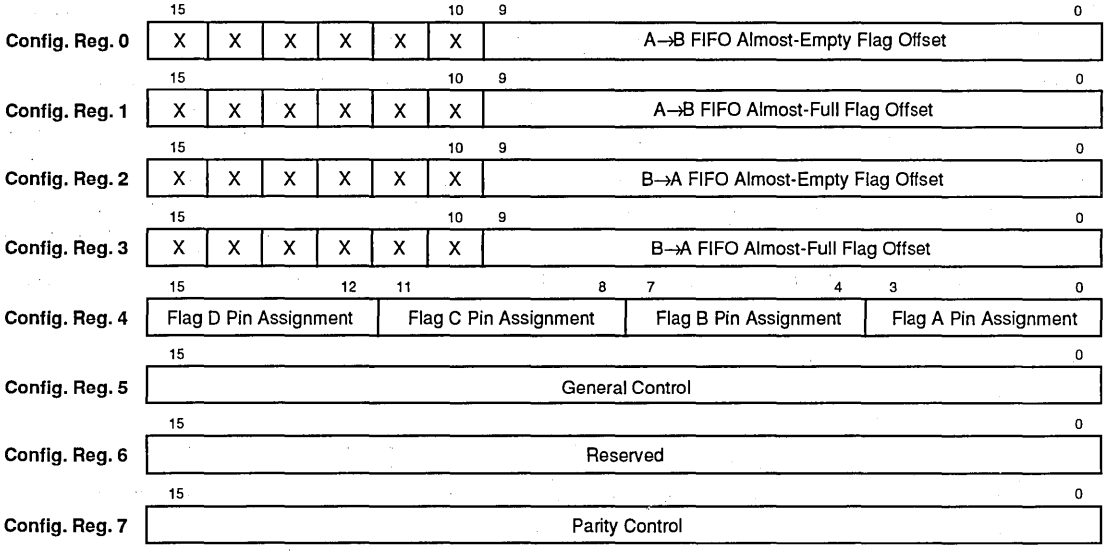
STATUS REGISTER FORMAT 1

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 1
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669tbl 11

Table 8. The Two Status Register Formats

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT7251 and IDT72510.

2669 tbl 12

Table 9. The BiFIFO Configuration Register Formats

checking is enabled for data read and written through Port B. Bit 8 controls parity checking and generation for B→A write data. Bit 9 controls parity checking and generation for A→B read data. Bit 10 controls whether the parity is odd or even. Bit 11 is used to assign the internal parity checking error to the FLGA pin. When the parity error is assigned to FLGA, the Configuration Register 4 flag assignment for FLGA is ignored.

Programmable Flags

The IDT BiFIFO has eight internal flags; four of these flags have programmable offsets, the other four are empty or full. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 9). The offset (or depth) of FIFO RAM array is based on the unit of an 18-bit word. The flags are asserted at the depths shown in Table 13. After a hardware reset or a software reset all, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 10). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register in Status Register format 1. In Status Register format 0, only four flags can be found in the Status Register (see Table 8).

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2669 tbl 13

Table 10. Configuration Register 4 Internal Flag Assignments to External Flag Pins.

5

Port B Interface

Port B also has parity, reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 11). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

Two 9-bit words are put together to create each 18-bit word stored in the internal FIFOs. The first 9-bit word written to Port B goes into the Odd Byte Register shown in the detailed block diagram. The Odd Byte Register valid bit (Bit 8) in the Status Register is **1** when this first 9-bit word is written. The data bits from Port B (D_{B0}-D_{B7}) are also stored in the lower 8 bits of the Status Register when Status Register format 0 is selected (see Table 8). The second write on Port B moves the 9-bits from Port B and the 9-bits in the Odd Byte Register into the B→A FIFO and advances the B→A Write Pointer. The Status Register valid bit is set to **0** after the second write.

When Port B reads data from the A→B FIFO, two buffers choose which 9 of the 18 memory bits are sent to Port B. These buffers alternate between the upper 9 bits (D_{A8}-D_{A15}, D_{A17}) and the lower 9 bits (D_{A0}-D_{A7}, D_{A16}). The A→B Read

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
	$\overline{R}_B$ & $\overline{W}_B$ or $\overline{DS}_B$ & R/$\overline{W}_B$	1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Byte Order of 18-bit Word	0	Lower byte D_{A7}-D_{A0} and parity D_{A16} are read or written first on Port B
		1	Upper byte D_{A15}-D_{A8} and parity D_{A17} are read or written first on Port B
2	Full Flag Definition	0	Full Flag is asserted when write pointer meets read pointer
		1	Full Flag is asserted when write pointer meets reread pointer
3	Empty Flag Definition	0	Empty Flag is asserted when read pointer meets write pointer
		1	Empty Flag is asserted when read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read and Write	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
	Timing Control for Peripheral Mode	1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock	0	internal clock = CLK
	Frequency Control	1	internal clock = CLK divided by 2
10	Port B Interface	0	Processor interface mode (Port B controls are inputs)
	Mode Control	1	Peripheral interface mode (Port B controls are outputs)
12-11	Width Expansion Mode Control	00	Stand-alone mode (18- to 9-bits, 36- to 18-bits)
		01	Reserved
		10	Slave width expansion mode (36- to 9-bits)
		11	Master width expansion mode (36- to 9-bits)
13	Unused		
14	Unused		
15	Unused		

2669 tbl 14

Table 11. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 7 FORMAT

BIT	FUNCTION		
0-7	Unused		
8	Parity Input Control B→A	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
9	Parity Output Control A→B	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even Control	0	Odd
		1	Even
11	Assign Parity Error to Flag A Pin	0	No Parity Error Output
		1	Parity Error on Flag A Pin
12-15	Unused		

2669 tbl 15

Table 12. BiFIFO Configuration Register 7 Format

Pointer is advanced after every two Port B reads.

The BiFIFO can be set to order the 9-bit data so the first 9-bits go to the LSB (D_{A0}-D_{A7}, D_{A16}) or the MSB (D_{A8}-D_{A15}, D_{A17}) of Port A. This data ordering is controlled by bit 1 of Configuration Register 5 (see Table 11).

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 11).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and $R/\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 sets whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins, respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an Empty A→B FIFO or if a write is attempted on a Full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, $R/\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Parity Checking and Generation

Parity generation or checking is performed by the BiFIFO on data passing through Port B. Parity can either be odd or even as determined by Bit 10 of Configuration Register 7.

When parity checking is enabled, D_{B8} is treated as a data bit. D_{B8} data will be passed to D_{A16} (bypass operation) or stored in the RAM array (FIFO operation) for B->A operation;

INTERNAL FLAG TRUTH TABLE

Number of Words In FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D - (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D - m	D - 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE:

2669 tbl 16

1. BiFIFO flags can be assigned to external flag pins to be observed. D = FIFO depth (IDT7251/510 = 512, IDT7252/520 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 13. Internal Flag Truth Table.

similarly, DA16 or parity bits from the RAM array will be passed to DB8 for A->B operations. A->B read parity errors and B->A write parity errors are shown in Bit 9 and 10 in the Status Register. If an external parity error signal is required, a logical OR of the two parity error bits is brought out to FLGA pin by setting Bit 11 of Configuration Register 7.

Parity generation creates the ninth bit. This ninth bit is placed on DB8 for A->B read operation, and on DA16 or RAM array for B->A write operation.

It is recommended that if the parity pins (DB8, DA16, and DA17) are not used, they should be pulled down with 10K resistors for noise immunity.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block form being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to prevent the data block from being read. In this case, the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

REREAD OPERATIONS

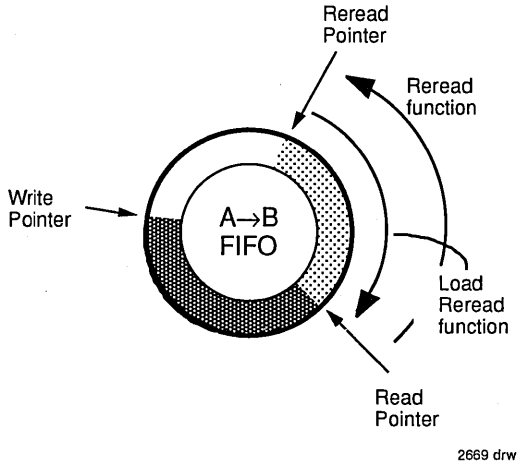


Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS

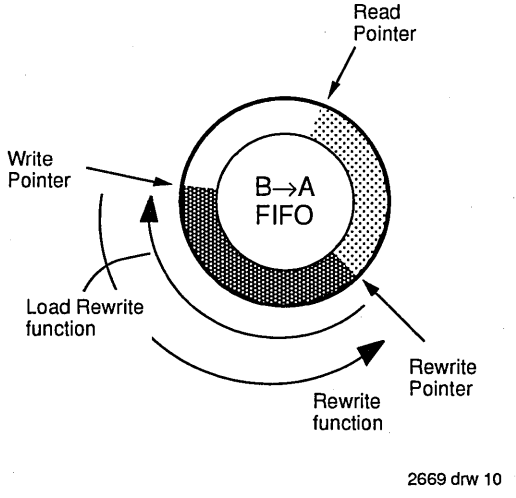


Figure 7. BiFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage With Respect To Ground	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2669 tbl 17

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage Commercial	2.0	—	—	V
VIH	Input HIGH Voltage Military	2.2	—	—	V
VIL(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2669 tbl 18

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

		IDT7251L IDT7252L IDT72510L IDT72520L Commercial tA = 35, 40, 50, 80ns			IDT7251L IDT7252L IDT72510L IDT72520L Military tA = 40, 50, 80ns			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
ILO(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
VOH	Output Logic "1" Voltage IOUT = -1mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage IOUT = 4mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Average VCC Power Supply Current	—	150	220	—	180	250	mA
ICC2(3)	Average Standby Current ($\overline{RB}$ = $\overline{WB}$ = $\overline{DS}_A$ = V IH)	—	16	30	—	24	50	mA

NOTES: 2669 tbl 19

1. Measurements with 0.4V ≤ VIN ≤ VCC, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ VIH. 2. Measurements with 0.4V ≤ VOUT ≤ VCC, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ VIH. 3. Masurements are made with outputs open. Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

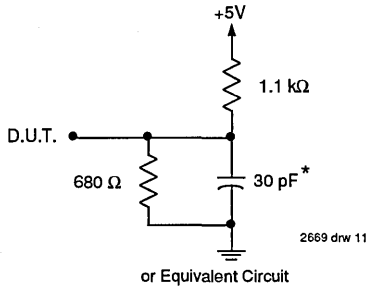
2669 tbl 20

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	8	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	12	pF

NOTES: 2669 tbl 21

1. With output deselected.
2. Characterized values, not currently tested.



or Equivalent Circuit

Figure 8. Output Load

* Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = -55°C to +125°C)

		Commercial		Commercial and Military							
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Timing Figure
RESET TIMING (Port A and Port B)											
tRSC	Reset cycle time	45	—	50	—	65	—	100	—	ns	9
tRS	Reset pulse width	35	—	40	—	50	—	80	—	ns	9
tRSS	Reset set-up time	35	—	40	—	50	—	80	—	ns	9
tRSR	Reset recovery time	10	—	10	—	15	—	20	—	ns	9
tRSF	Flag reset pulse width	—	45	—	50	—	65	—	100	ns	9
PORT A TIMING											
taA	Port A access time	—	35	—	40	—	50	—	80	ns	12, 14, 15
taLZ	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	12, 15, 16
taHZ	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	12, 14, 15, 16
taDV	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
taRC	Read cycle time	45	—	50	—	65	—	100	—	ns	12
taRPW	Read pulse width	35	—	40	—	50	—	80	—	ns	12, 14, 15
taRR	Read recovery time	10	—	10	—	15	—	20	—	ns	12
tas	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	10	—	ns	10, 12, 16
taH	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	10	—	ns	10, 12
taDS	Data set-up time	18	—	20	—	30	—	40	—	ns	11, 12, 14, 15
taDH (1)	Data hold time	0	—	5	—	5	—	10	—	ns	11, 12, 14, 15
taWC	Write cycle time	45	—	50	—	65	—	100	—	ns	12
taWPW	Write pulse width	35	—	40	—	50	—	80	—	ns	11, 12, 14
taWR	Write recovery time	10	—	10	—	15	—	20	—	ns	12
taWRCOM	Write recovery time after a command	35	—	40	—	50	—	80	—	ns	11

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Commercial		Commercial and Military							
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B PROCESSOR INTERFACE TIMING											
t_{bA1}	Port B access time with no parity	—	35	—	40	—	50	—	80	ns	13, 14, 15
t_{bA2}	Port B access time with parity	—	42	—	48	—	60	—	90	ns	13, 14, 15
t_{bLZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	13, 14, 15
t_{bHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	13, 14, 15
t_{bDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	10	—	ns	13, 14, 15, 16
t_{bRC}	Read cycle time	45	—	50	—	65	—	100	—	ns	13
t_{bRPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	13
t_{bRR}	Read recovery time	10	—	10	—	15	—	20	—	ns	13
t_{bS}	$R\overline{W}_B$ set-up time	5	—	5	—	5	—	10	—	ns	13
t_{bH}	$R\overline{W}_B$ hold time	5	—	5	—	5	—	10	—	ns	13
t_{bDS1}	Data set-up time with no parity	18	—	20	—	30	—	40	—	ns	13, 14, 15
t_{bDH1}	Data hold time with no parity	0	—	5	—	5	—	10	—	ns	13, 14, 15
t_{bDS2}	Data set-up time with parity	22	—	25	—	35	—	45	—	ns	13, 14, 15
t_{bDH2}	Data hold time with parity	0	—	5	—	5	—	10	—	ns	13, 14, 15
t_{bWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	13
t_{bWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	13, 15
t_{bWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
t_{bA1}	Port B access time with no parity	—	40	—	45	—	55	—	85	ns	17
t_{bA2}	Port B access time with parity	—	42	—	48	—	60	—	90	ns	17
t_{bCKC}	Clock cycle time	20	—	20	—	25	—	40	—	ns	17
t_{bCKH}	Clock pulse HIGH time	6	—	8	—	10	—	16	—	ns	17
t_{bCKL}	Clock pulse LOW time	6	—	8	—	10	—	16	—	ns	17
t_{bREQS}	Request set-up time	5	—	5	—	10	—	10	—	ns	17
t_{bREQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
t_{bACKL}	Delay from a rising clock edge to ACK switching	—	18	—	20	—	25	—	35	ns	17

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V±10%, TA = 0°C to +70°C; Military: Vcc = 5V±10%, TA = -55°C to +125°C)

		Commercial		Commercial and Military							
		IDT7251L35 IDT7252L35 IDT72510L35 IDT72520L35		IDT7251L40 IDT7252L40 IDT72510L40 IDT72520L40		IDT7251L50 IDT7252L50 IDT72510L50 IDT72520L50		IDT7251L80 IDT7252L80 IDT72510L80 IDT72520L80			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B RETRANSMIT and PARITY TIMING											
t_{DSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	15	—	ns	9, 18
t_{DPER}	Parity error time	25	—	25	—	30	—	30	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	20	—	25	—	30	—	40	ns	16
t_{BYD}	Bypass delay	—	15	—	20	—	20	—	30	ns	16
t_{ABYDV}	Bypass data valid time from $\overline{DS_A}$	15	—	15	—	15	—	15	—	ns	16
t_{BBYDV} (3)	Bypass data valid time from $\overline{DS_B}$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING											
t_{REF}	Read clock edge to Empty Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	50	—	55	—	60	—	75	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	50	—	55	—	60	—	75	ns	21, 23

NOTES:
1. Read and Write are internal signals derived from $\overline{DS_A}$, $R/\overline{W_A}$, $\overline{DS_B}$, $R/\overline{W_B}$, $\overline{R_B}$, and $\overline{W_B}$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.

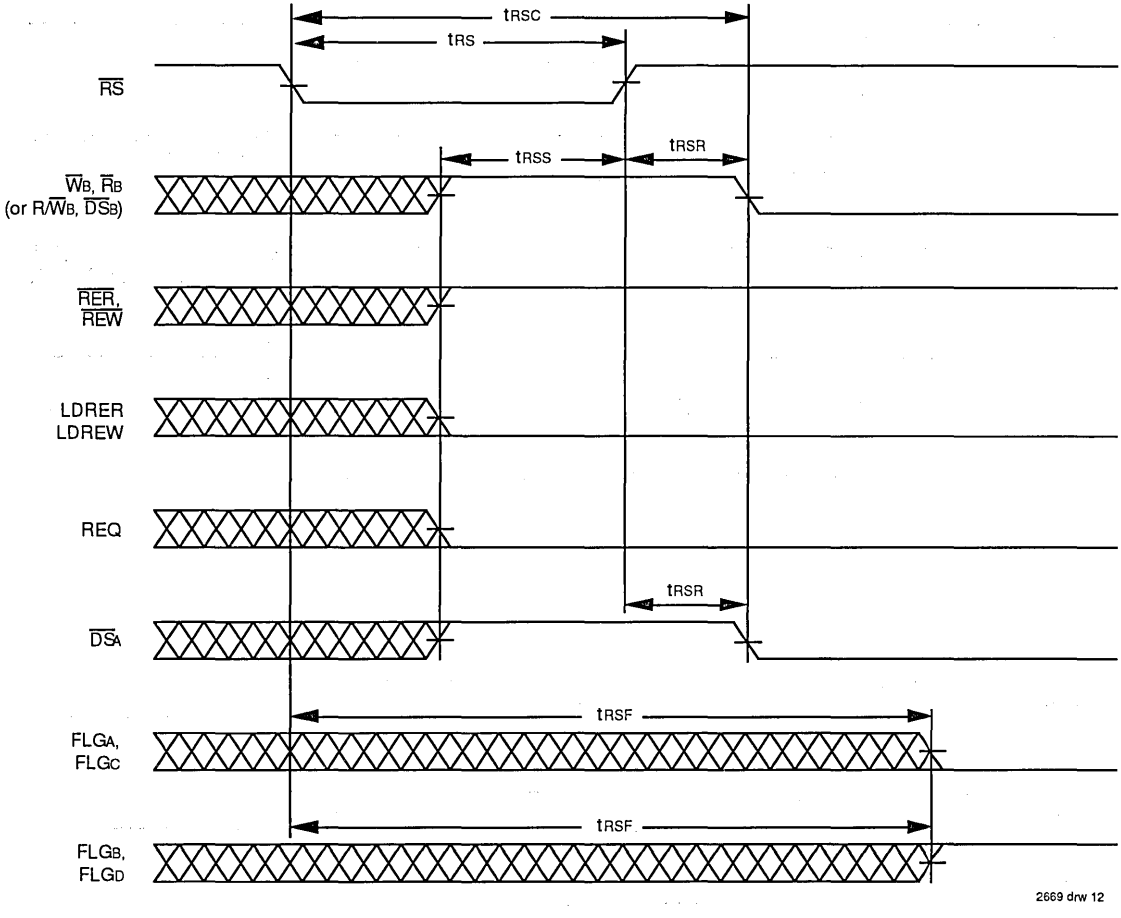


Figure 9. Hardware Reset Timing for IDT72510/520

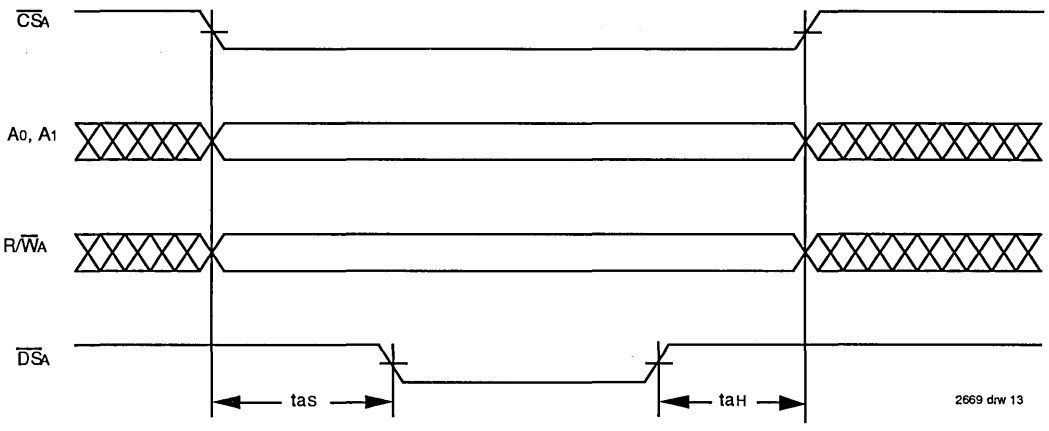


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

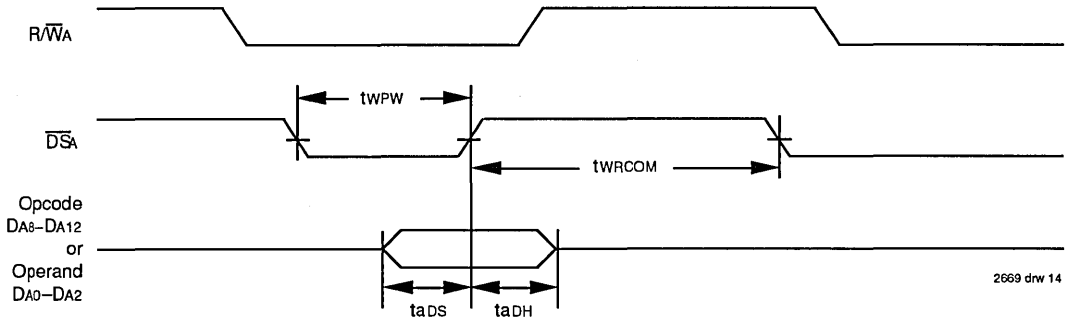
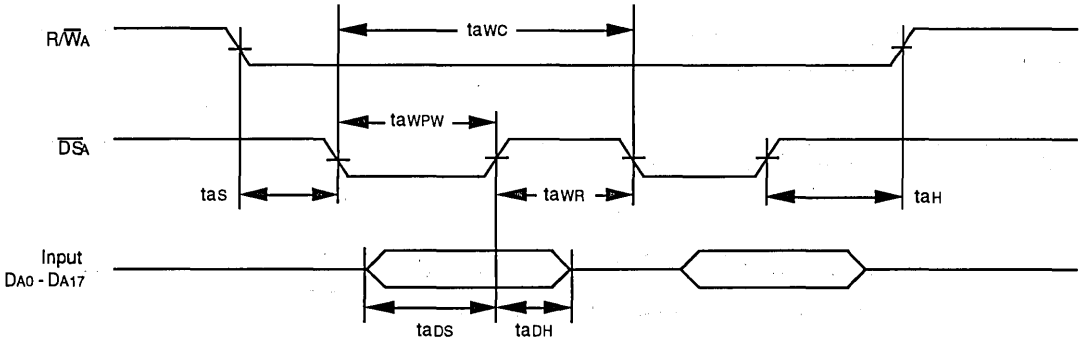


Figure 11. Port A Command Timing (Write)

WRITE



READ

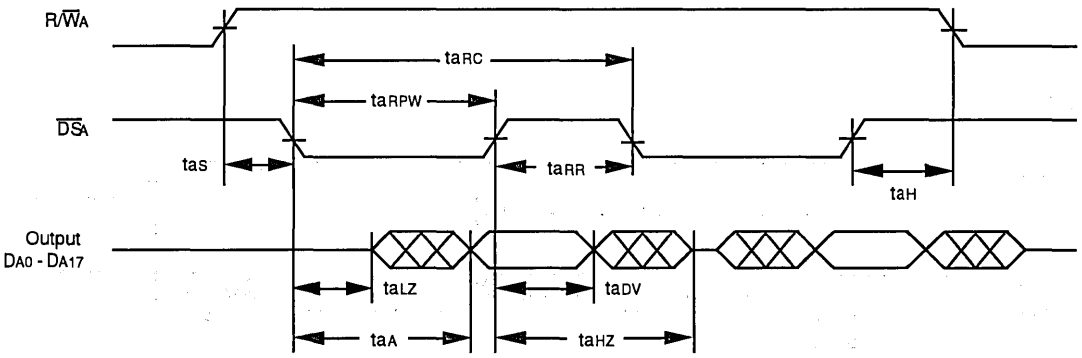
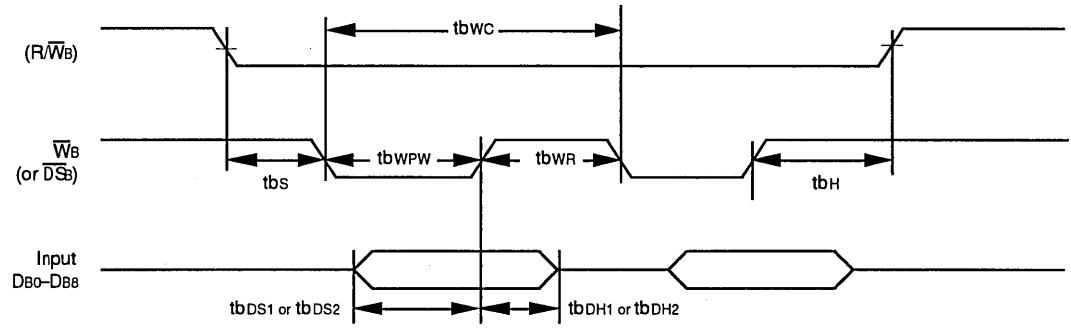


Figure 12. Read and Write Timing for Port A

2669 drw 15

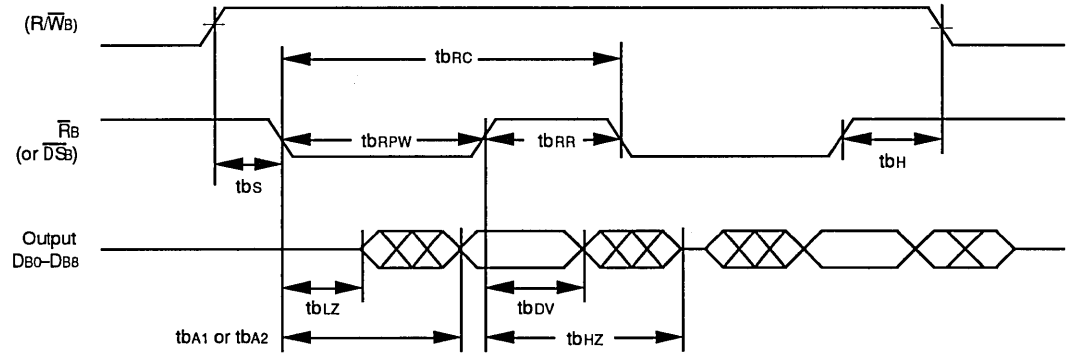
5

WRITE



NOTES:
1. tbDS1 and tbDH1 are with parity checking or if parity is ignored, tbDS2 and tbDH2 are with parity generation.
2. $\overline{R}_B$ = 1

READ

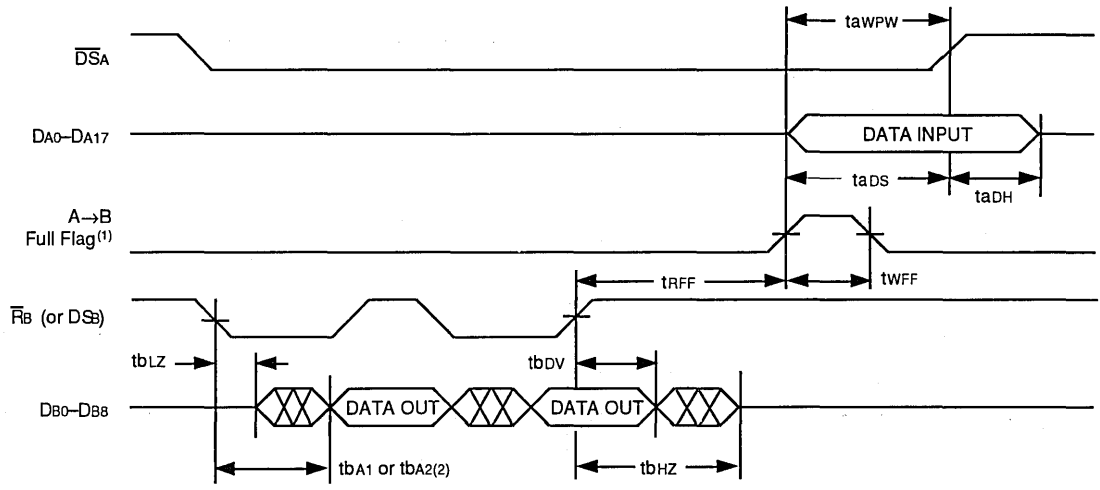


NOTES:
1. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
2. $\overline{W}_B$ = 1

2669 drw 18

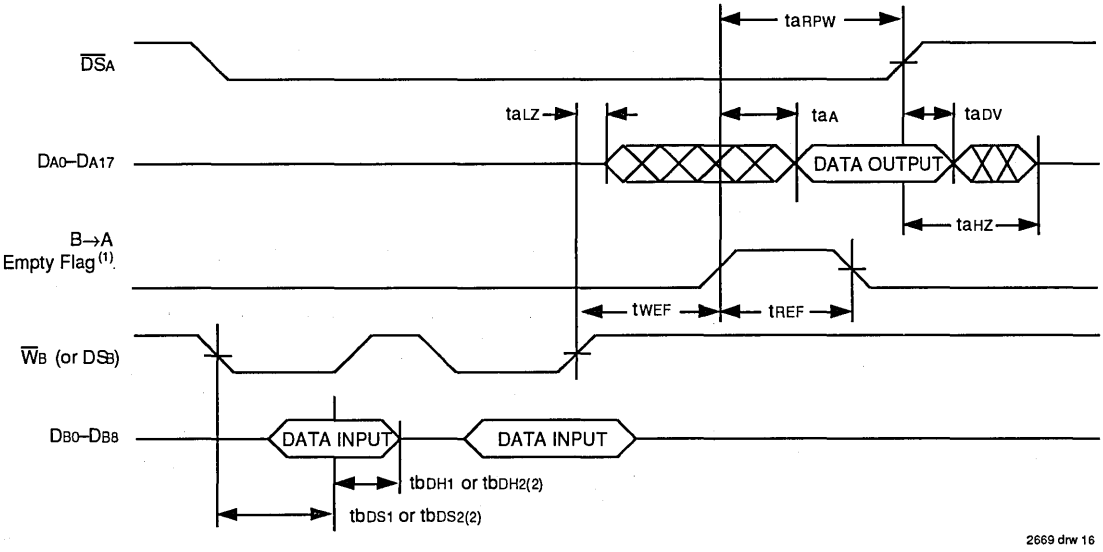
Figure 13. Port B Read and Write Timing. Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. tb_{A1} is with parity checking or if parity is ignored, tb_{A2} is with parity generation.
3. R/$\overline{W}$A = 0.

B→A FIFO READ FLOW-THROUGH

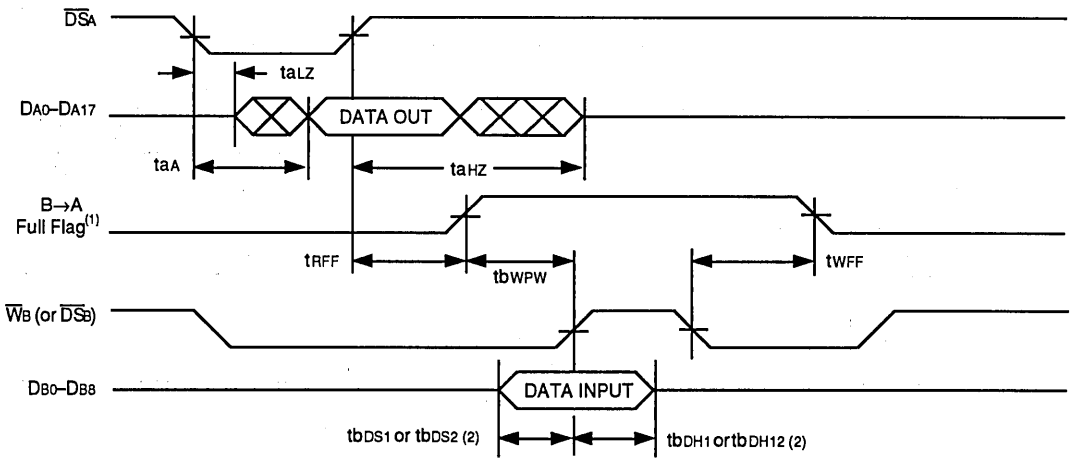


2669 drw 16

NOTES:
1. Assume the flag pin is programmed active low.
2. tb_{DS1} & tb_{DH1} is with parity checking or if parity is ignored, tb_{DS2} & tb_{DH2} is with parity generation.
3. R/$\overline{W}$A = 1.

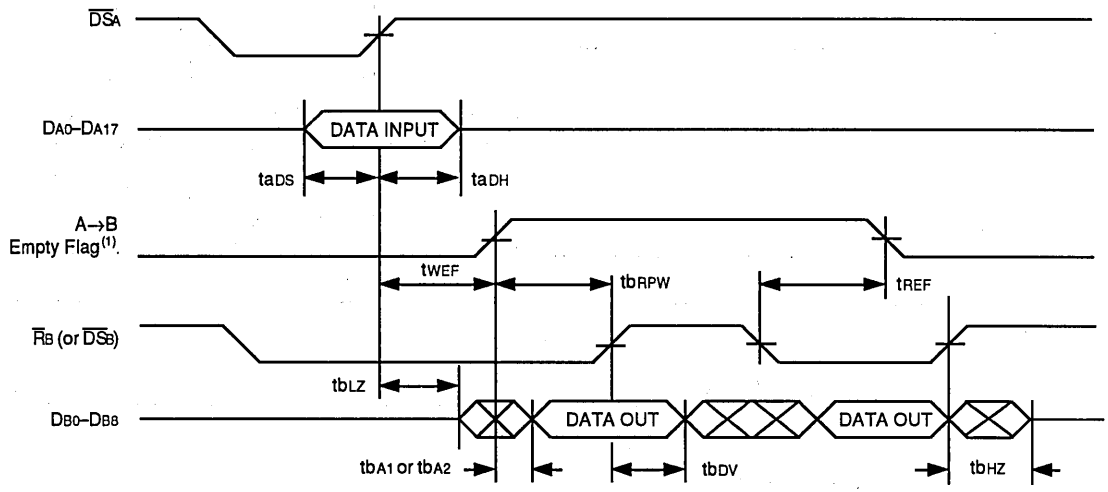
Figure 14. Port A Read and Write Flow-Through Timing. Processor Interface Mode Only

B→A FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. t_{bDS1} & t_{bDH1} are with parity checking or if parity is ignored, t_{bDS2} & t_{bDH2} are with parity generation.
3. $R\overline{W}_A$ = 1.

A→B FIFO READ FLOW-THROUGH

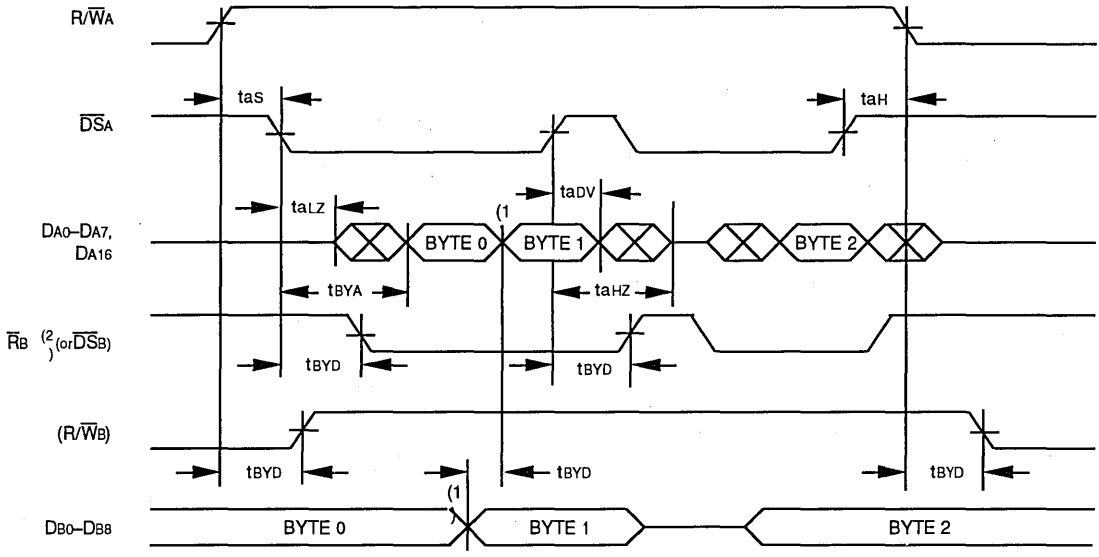


2669 drw 19

NOTES:
1. Assume the flag pin is programmed active low.
2. t_{bA1} are with parity checking or if parity is ignored, t_{bA2} are with parity generation.
3. $R\overline{W}_A$ = 0.

Figure 15. Port B Read and Write Flow-Through Timing

B→A READ BYPASS

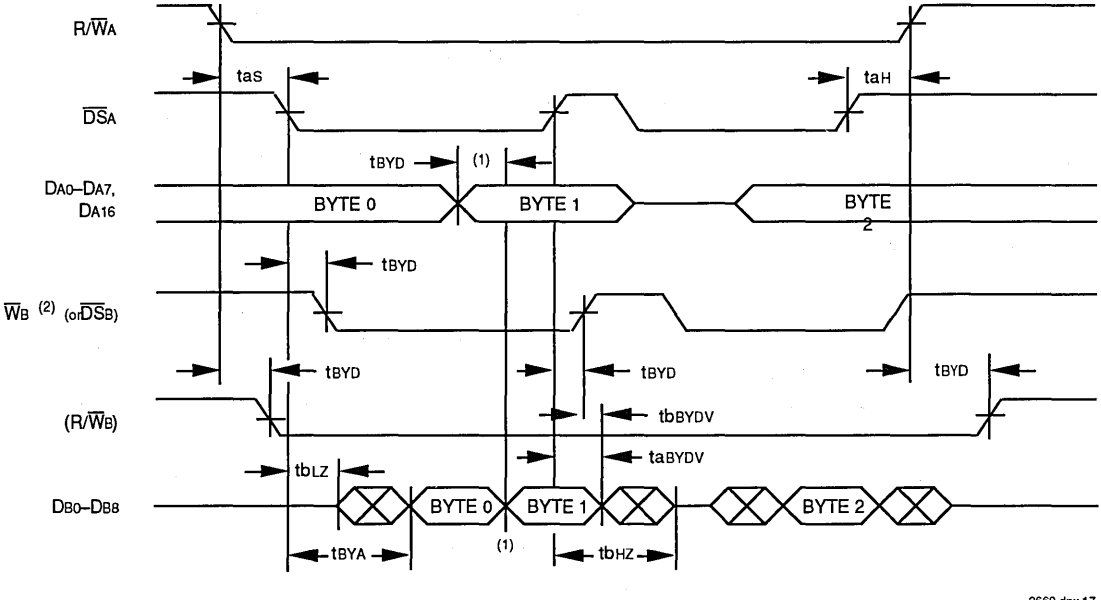


NOTE:

1. Once the bypass starts, any data changes on Port B bus (Byte 0 → Byte 1) will be passed to Port A bus.
2. $\overline{W_B} = 1$.

5

A→B WRITE BYPASS



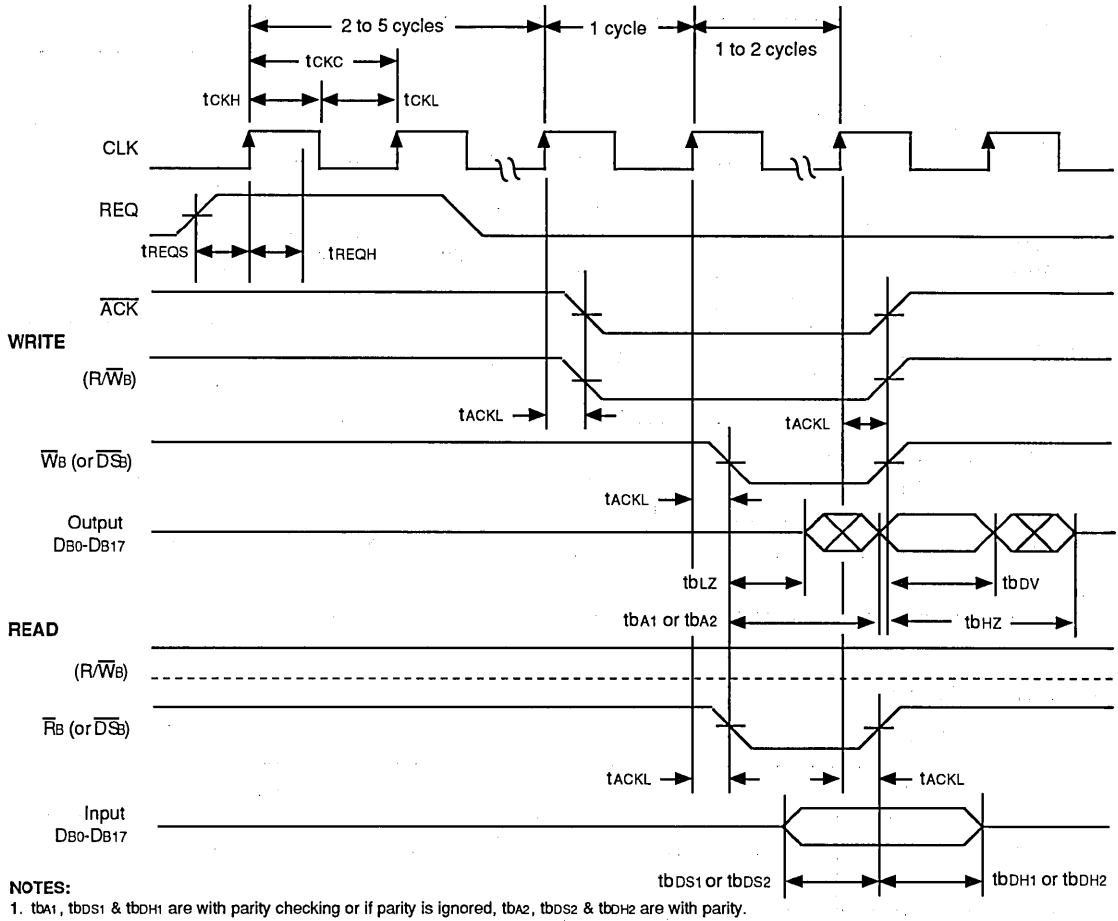
2669 drw 17

NOTE:

1. Once the bypass starts, any data changes on Port A bus (Byte 0 → Byte 1) will be passed to Port B bus.
2. $\overline{R_B} = 1$

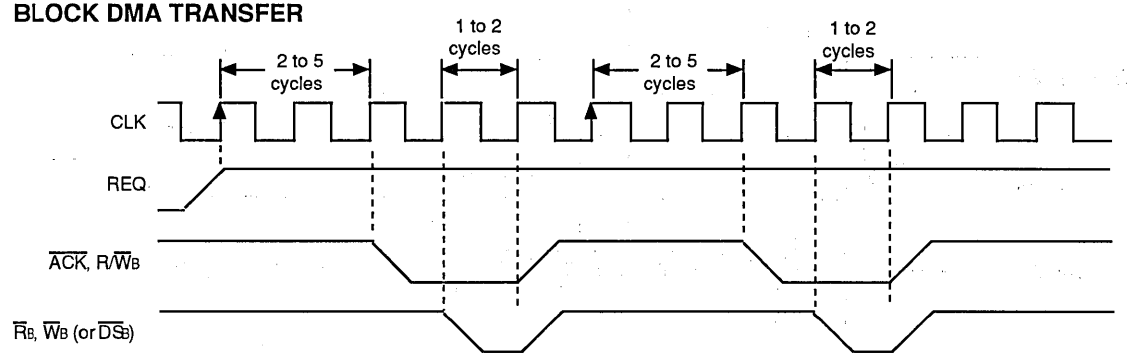
Figure 16. Bypass Path Timing. BiFIFO Must be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



NOTES:
1. t_{bA1}, t_{bDS1} & t_{bDH1} are with parity checking or if parity is ignored, t_{bA2}, t_{bDS2} & t_{bDH2} are with parity.

BLOCK DMA TRANSFER



2669 drw 20

Figure 17. Port B Read and Write DMA Timing. Peripheral Interface Mode Only

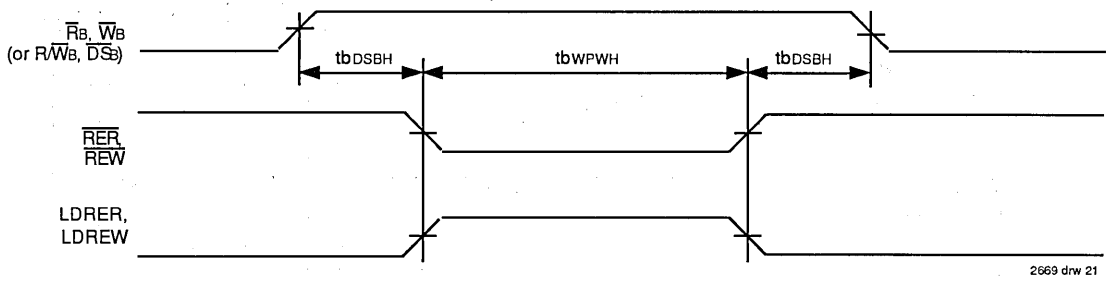
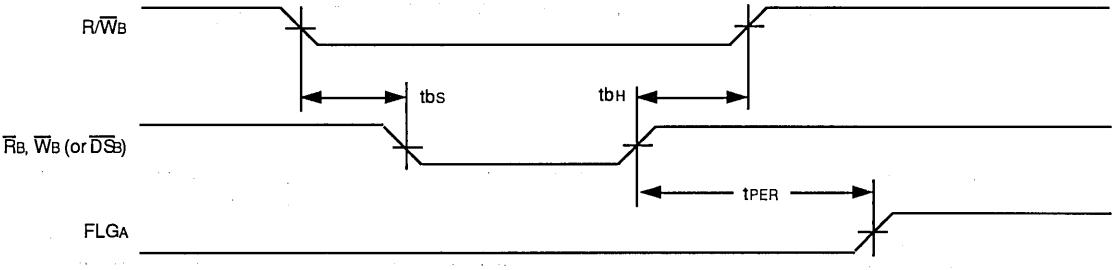
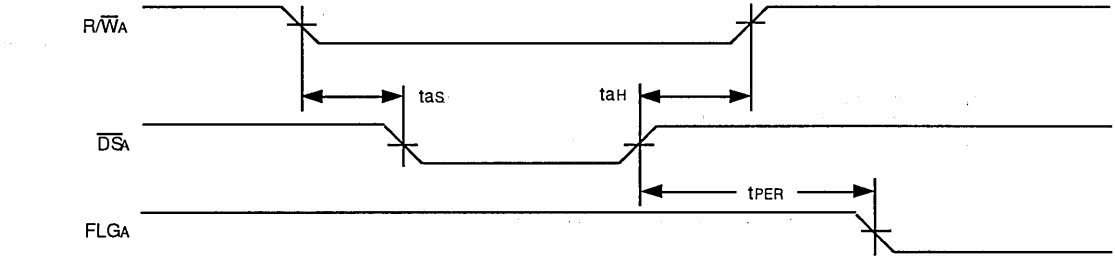


Figure 18. Port B Reread and Rewrite Timing for Intelligent Retransmit

Set Parity Error: FLGA is assigned as the parity error pin

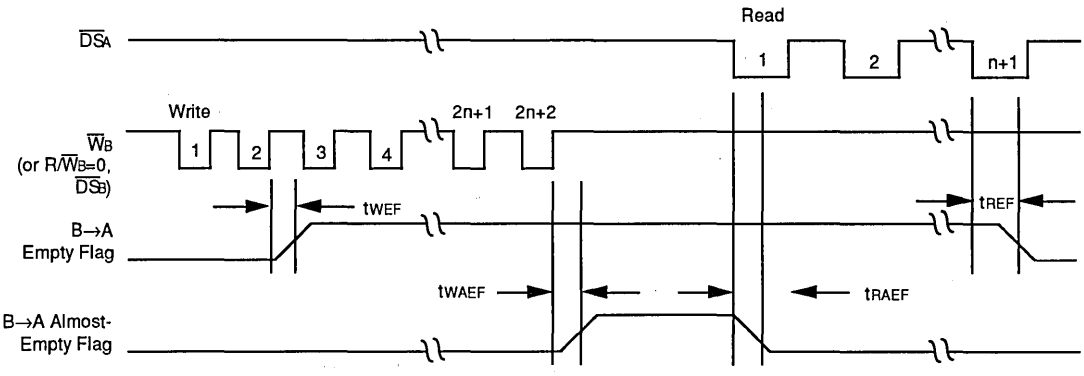


Clear Parity Error: Command written into Port A clears parity error on FLGA pin



NOTE:
1. FLGA is the only pin that can be assigned as a parity error output.

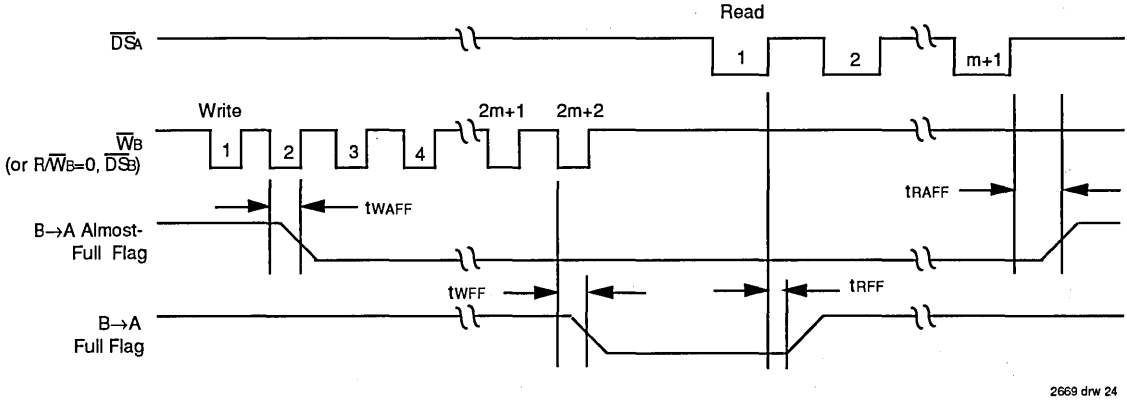
Figure 19. Port B Parity Error Timing



NOTES:

1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W}_A$ = 1

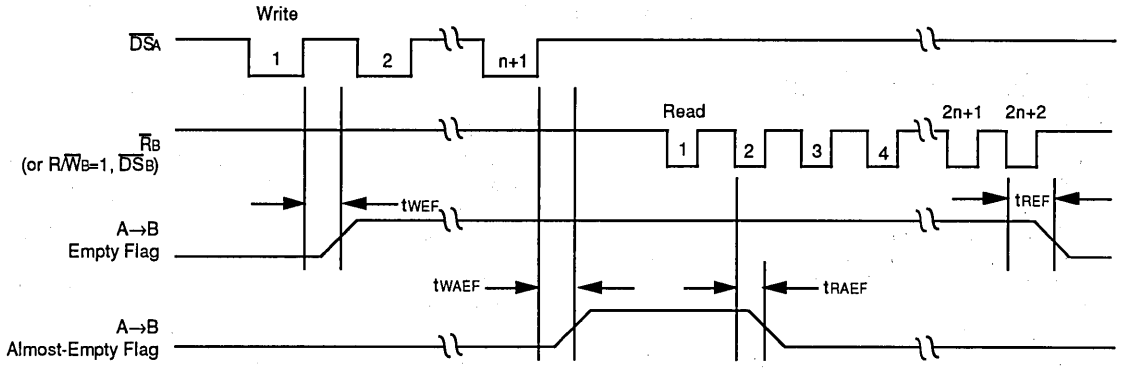
Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO. (n = Programmed Offset)



NOTES:

1. B→A FIFO initially contains D–(M+1) data words. D = 512 for IDT 7251/510; D = 1024 for IDT7252/520.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W}_A$ = 1

Figure 21. Full and Almost-Full Flag Timing for B→A FIFO. (m = Programmed Offset)

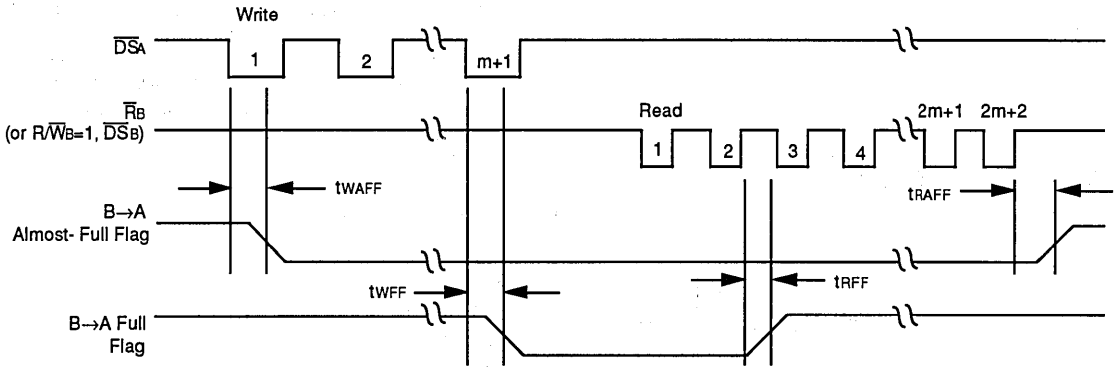


2669 drw 25

NOTES:

1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W}_A$ = 1

Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO. (n = Programmed Offset)



2669 drw 26

NOTES:

1. A→B FIFO initially contains D-(M+1) data words. D = 512 for IDT7251/510; D = 1024 for IDT7252/520.
2. Assume the flag pins are programmed active low.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/$\overline{W}_A$ = 0

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO. (m = Programmed Offset)

Integrated Device Technology, Inc.

PARALLEL BIDIRECTIONAL FIFO 512 x 18-BIT & 1024 x 18-BIT

IDT72511
IDT72521

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18 - Bit - 512 x 18 - Bit (IDT72511)
- 1024 x 18 - Bit - 1024 x 18 - Bit (IDT72521)
- 18-bit data buses on Port A side and Port B side
- Can be configured for 18-to-18-bit or 36-to-36-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities
- Six general-purpose programmable I/O pins
- Standard DMA control pins for data exchange with peripherals
- 68-pin PGA and PLCC packages

DESCRIPTION:

The IDT72511 and IDT72521 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

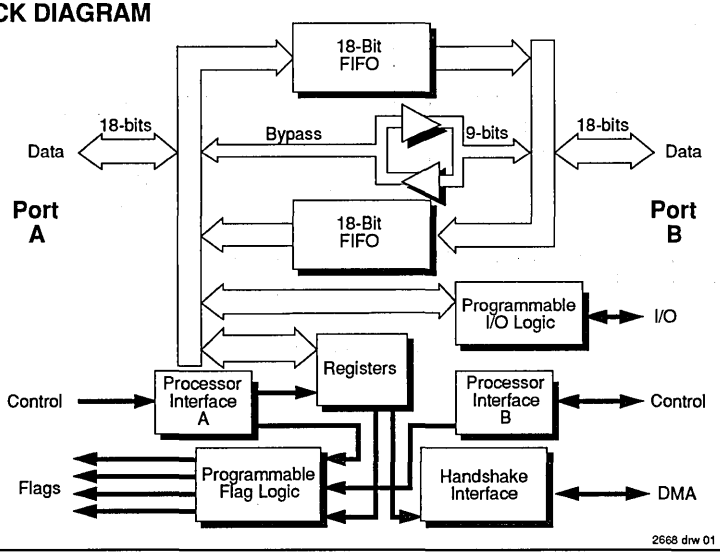
The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. Port B is also 18 bits wide and can be connected to another processor or a peripheral controller. The BiFIFOs have a 9-bit bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFO has programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through one Configuration Register.

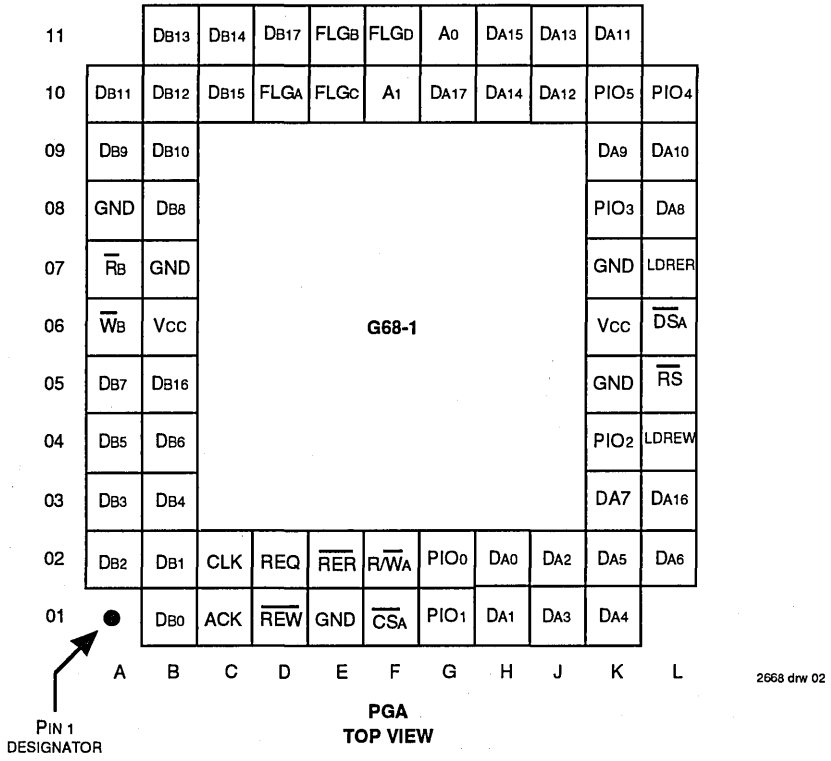
Port B has programmable I/O, reread/rewrite and DMA functions. Six programmable I/O pins are manipulated through two Configuration Registers. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFO has three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

SIMPLIFIED BLOCK DIAGRAM

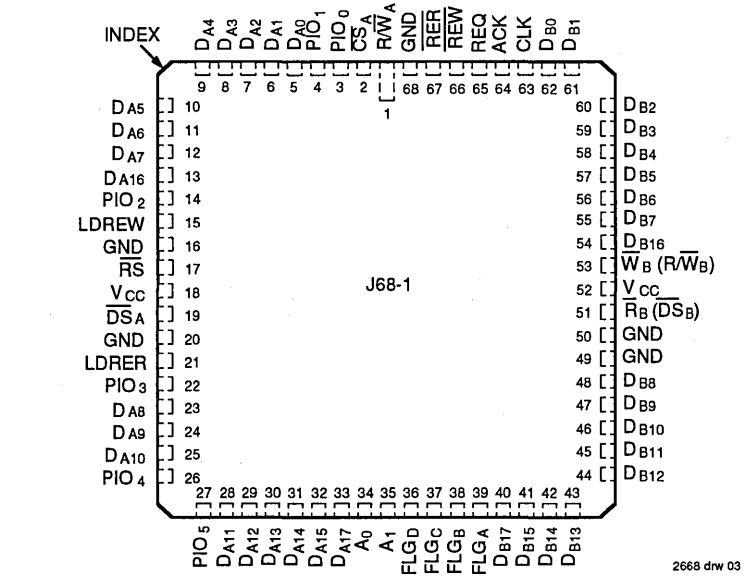


2668 drw 01

PIN CONFIGURATIONS



PGA
TOP VIEW



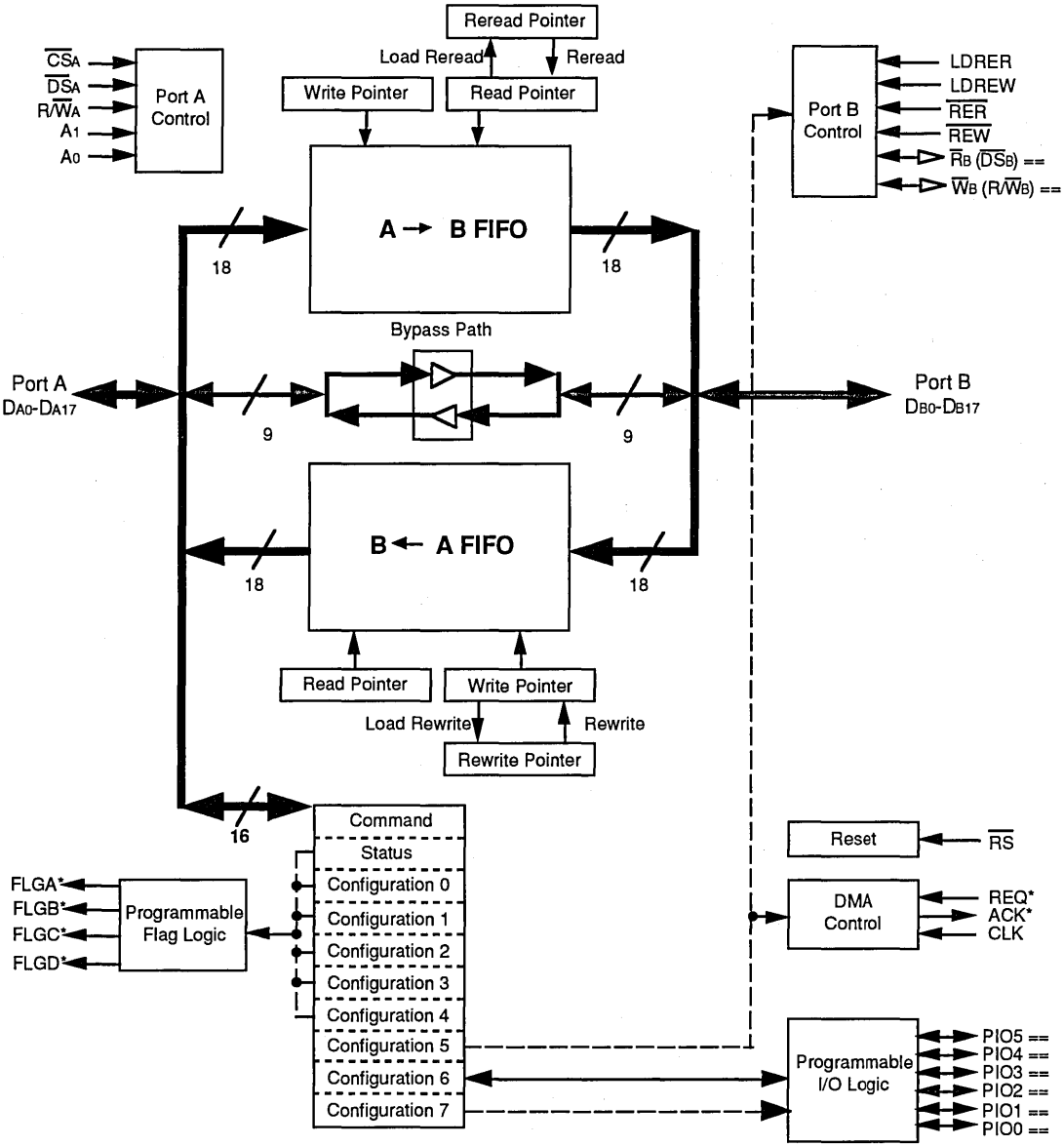
PLCC
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs and outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
$R/\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is LOW, data is written into Port A on the rising edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs and outputs for the 18-bit Port B bus.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$ or written on the rising edge of $\overline{DS}_B$ through Port B. The default is Intel-style processor mode. ($\overline{R}_B$ as an input).
$\overline{W}_B$ ($R/\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface ($R/\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read ($R/\overline{W}_B$ = HIGH) or written ($R/\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The default is Intel-style processor mode ($\overline{W}_B$ as an input.)
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and $R/\overline{W}_B$ when Port B is in the peripheral mode.
FLG_A-FLG_D	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full and Full.
PIO_0-PIO_5	Programmable Inputs/ Outputs	I/O	Six general purpose I/O pins. The input or output direction of each pin can be set independently.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions.
V_{CC}	Power		There are two +5V power pins.
GND	Ground		There are five Ground pins at 0V.

2668 tbl 01

DETAILED BLOCK DIAGRAM



NOTES:

(*) Can be programmed either active high or active low in internal configuration registerers.

(††) Can be programmed through an internal configuration register to be either an input or an output.

2668 drw 04

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFO can be used in different bus configurations: 18 bits to 18 bits and 36 bits to 36 bits. One BiFIFO can be used for the 18- to 18-bit configuration, and two BiFIFOs are required for 36- to 36-bit configuration. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, ...) by adding more BiFIFOs to the configuration.

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFO, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 18-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 18-bit processor or an 18-bit peripheral. The upper BiFIFO shown in each of the Figures 1 and 2 can be used in 18- to 18-bit configurations for processor and peripheral interface modes respectively.

36- to 36-bit Configurations

In a 36- to 36-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 18 data bits to each device. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the setup and hold time requirements for these pins are met during reset. Figure 1 shows the BiFIFO in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in peripheral interface mode. In this mode, all the Port B interface pins are all outputs. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, these two pins should be pulled up to Vcc with 10K resistors. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows a BiFIFO configuration connected to a peripheral.

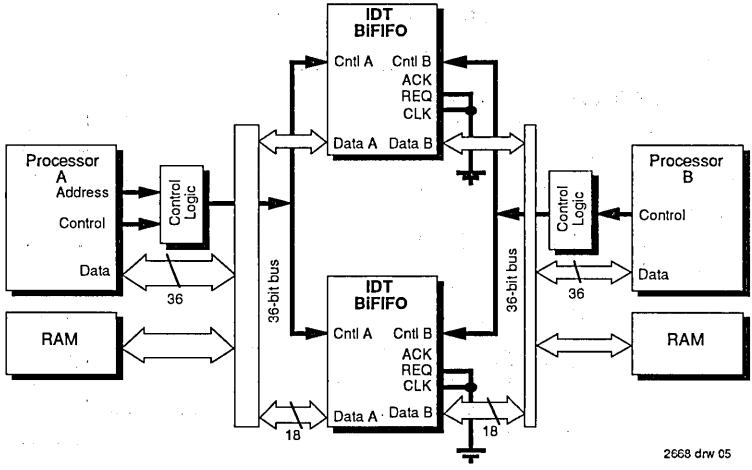


Figure 1. 36-Bit Processor to 36-Bit Processor Configuration

NOTE:

1. 36- to 36-bit processor interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

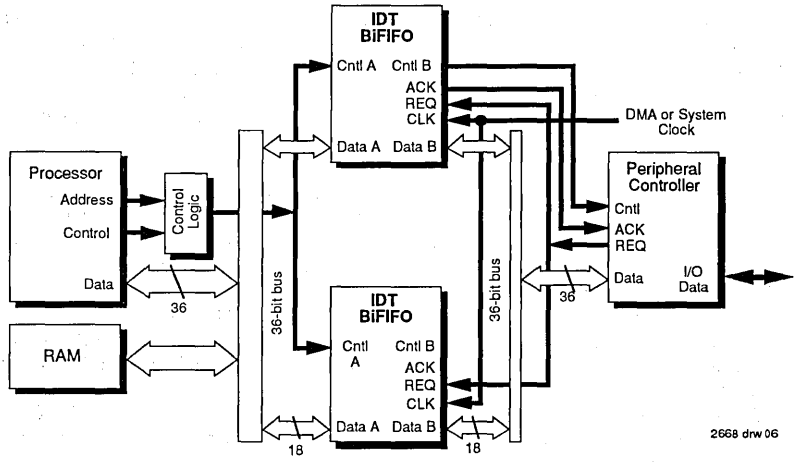


Figure 2. 36-Bit Processor to 36-Bit Peripheral Configuration

NOTE:
1. 36- to 36-bit peripheral interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed, 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte (D_{A0}-D_{A7}, D_{A16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (D_{A0}-D_{A15}) are passed by Port A.

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 18-bit configuration or 18 bits wide in a 36- to 36-bit configuration.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 10) is set to **1** for peripheral interface mode.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 3. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, and to modify the Port B Read and Write Pointers. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by interchanging the Port B Read Pointer with the Reread Pointer or by interchanging the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

COMMAND FORMAT

15			12	11	8	7			3	2	0
X	X	X	X	Command Opcode		X	X	X	X	X	Command Operand

2668 tbl 02

Figure 3. Format for Commands Written into Port A

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

Two commands are provided to increment the Port B Read and Write Pointers. No operands are required for these commands.

Reset

The IDT72511 and IDT72521 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to **6420H**, and Configuration Registers 5, 6 and 7 are **0000H**. Additionally, all the pointers including the Reread and Rewrite Pointers are set to **0**, the DMA direction is set to B→A write, and the internal DMA request circuitry is cleared (set to its initial state).

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The internal request DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 6 shows the BiFIFO state after the different hardware and software resets

Status Register

The Status Register reports the state of the programmable flags and the DMA read/write direction. The Status Register is read by setting $\overline{CS}_A = 0$, $A_1 = 1$, $A_0 = 1$ (see Table 1). See Table 7 for the Status Register format.

Configuration Registers

The eight Configuration Register formats are shown in Table 8. Configuration Registers 0-3 contain the programmable

PORT A RESOURCE SELECTION

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2668 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0 and A_1

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Reserved
1000	Increment A→B FIFO Read Pointer (Port B)
1001	Increment B→A FIFO Write Pointer (Port B)
1010	Reserved
1011	Reserved

2668 tbl 04

Table 2. Functions Performed by Port A Commands

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2668 tbl 05

Table 3. Reset Command Functions

SELECT CONFIGURATION REGISTER/ COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2668 tbl 06

Table 4. Select Configuration Register Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2668 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATE AFTER RESET

	Hardware Reset (RS asserted)	Software Reset				
		B→A(001)	A→B(010)	B→A and A→B(011)	Internal Request (100)	All(111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 6-7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear

2668 tbl 08

Table 6. The BiFIFO State After a Reset Command

flag offsets for the Almost-Empty and Almost-Full flags. These offsets are set to **0** when a hardware reset or a software Reset All is applied. Note that Table 8 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLGA-FLGD). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 9. The default condition for Configuration Register 4 is **6420H** as shown in Table 6. The default flag assignments are: FLGD is assigned B→A $\overline{\text{Full}}$, FLGC is assigned B→A $\overline{\text{Empty}}$, FLGB is assigned A→B $\overline{\text{Full}}$, FLGA is assigned A→B $\overline{\text{Empty}}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 10.

Bit 0 sets the Intel-style interface ($\overline{\text{RB}}$, $\overline{\text{WB}}$) or Motorola-style interface ($\overline{\text{DS}}$B, R/$\overline{\text{W}}$B) for Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{\text{RB}}$, $\overline{\text{WB}}$, and $\overline{\text{DS}}$B are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{\text{RB}}$, $\overline{\text{WB}}$, $\overline{\text{DS}}$B, R/$\overline{\text{W}}$B) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Six PIO pins can be programmed as an input or output by the corresponding mask bits in Configuration Register 7. The format of Configuration Register 7 is shown in Figure 5. Each bit of the register set the I/O direction independently. A logic **1** indicates that the corresponding PIO pin is an output, while a logic **0** indicates that the PIO pin is an input. This I/O mask register can be read or written.

A programmed output PIOi pin (i = 0, 1, . . . 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIOi pin allows Port A bus to sample the data on DAi by reading Configuration Register 6.

5

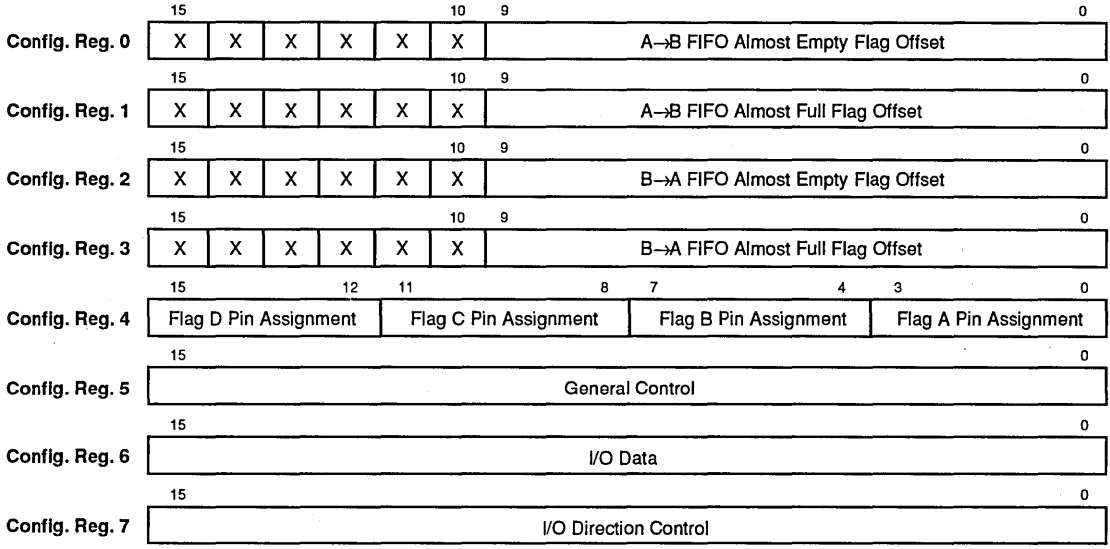
STATUS REGISTER FORMAT

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2668 tbl 09

Table 7. The Status Register Format

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72511.

2668 tbl 10

Table 8. The BiFIFO Configuration Register Formats

Programmable Flags

The IDT BiFIFO has eight internal flags. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 8). The flags are asserted at the depths shown in Table 11. After a hardware reset or a software Reset All, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident after reset because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 9). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register.

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2668 tbl 11

Table 9. Configuration Register 4 Internal Flag Assignments to External Flag Pins

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ and $\overline{W}_B$ or $\overline{DS}_B$ and R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Unused		
2	Full Flag Definition	0	Write pointer meets read pointer
		1	Write pointer meets reread pointer
3	Empty Flag Definition	0	Read pointer meets write pointer
		1	Read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read & Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	Internal clock = CLK
		1	Internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
11	Unused		
12	Unused		
13	Unused		
14	Unused		
15	Unused		

2668 tbl 12

Table 10. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 6 FORMAT

15	6	5	4	3	2	1	0
Unused		PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

2668 tbl 13

Figure 4. BiFIFO Configuration Register 6 Format for Programmable I/O Data

CONFIGURATION REGISTER 7 FORMAT

15	6	5	4	3	2	1	0
Unused		MIO5	MIO4	MIO3	MIO2	MIO1	MIO0

2668 tbl 23

Figure 5. BiFIFO Configuration Register 7 Format for Programmable I/O Direction Mask

Port B Interface

Port B has reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 10). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 10).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 set whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an empty A→B FIFO or if a write is attempted on a full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block from being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D – (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D – m	D – 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE: 2668 tbl 14

1. BiFIFO flags must be assigned to external flag pins to be observed. D = FIFO depth (IDT72511 = 512, IDT72521 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 11. Internal Flag Truth Table

prevent the data block from being read. In this case the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

Programmable Input/Output

The BiFIFO has six programmable I/0 pins (PIO_0 - PIO_5) which are controlled by Port A through Configuration Registers 6 and 7. Data from the programmable I/O pins is mapped directly to the six least significant bits of Configuration Register 6. Figure 4 shows the format of Configuration Register 6. This data is read or written by Port A on the data pins (DA_0- DA_5). A programmed output PIO_i pin (i = 0, 1, . . . , 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample its data on DA_i by reading Configuration Register 6. The read and write timing for the programmable I/O pins is shown in Figure 19. The direction of each programmable I/O pin can be set independently by programming the mask in Configuration Register 7. Each P10 pin has a corresponding input/output direction mask bit in Configuration Register 7. Figure 5 shows the format of Configuration Register 7. Setting a mask bit to a logic 1 makes the corresponding I/O pin an output. Mask bits set to logic 0 force the corresponding I/O pin to an input.

REREAD OPERATIONS

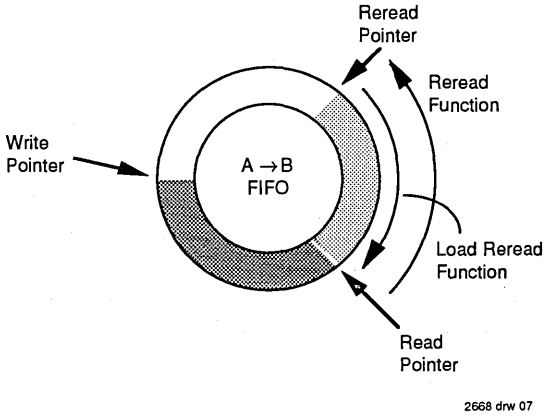


Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS

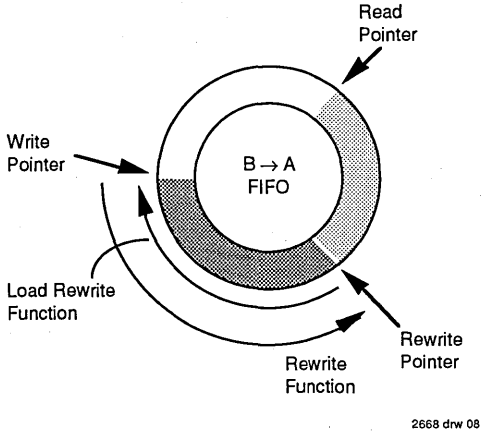


Figure 7. BiFIFO Rewrite Operations

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage With Respect To Ground	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2668 tbl 15

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage Commercial	2.0	—	—	V
V_{IH}	Input HIGH Voltage Military	2.2	—	—	V
V_{IL}(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2668 tbl 16

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72511L IDT72521L Commercial t_A = 35, 40, 50, 80ns Min.	Typ.	Max.	IDT72511L IDT72521L Military t_A = 40, 50, 80ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)(4)	Average VCC Power Supply Current	—	150	230	—	180	250	mA
I_{CC2}(3)	Average Standby Current ($\overline{R_B}$ = $\overline{W_B}$ = $\overline{DS_A}$ = V_{IH})	—	16	30	—	24	50	mA

NOTES: 2668 tbl 17

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}
2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}
3. Measurements are made with outputs open.
4. Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

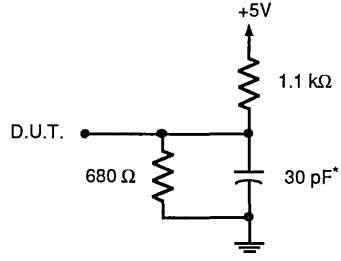
2668 tbl 18

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2668 tbl 19

1. With output deselected.
2. Characterized values, not currently tested.



OR EQUIVALENT CIRCUIT

2668 drw 09

Figure 8. Output Load
*Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to + 125°C)

Symbol	Parameter	Commercial		Commercial and Military						Unit	Timing Figure
		IDT72511L35 IDT72521L35		IDT72511L40 IDT72521L40		IDT72511L50 IDT72521L50		IDT72511L80 IDT72521L80			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
RESET TIMING (Port A and Port B)											
tRSC	Reset cycle time	45	—	50	—	65	—	100	—	ns	9
tRS	Reset pulse width	35	—	40	—	50	—	80	—	ns	9
tRSS	Reset set-up time	35	—	40	—	50	—	80	—	ns	9
tRSR	Reset recovery time	10	—	10	—	15	—	20	—	ns	9
tRSF	Reset to flag time	—	45	—	50	—	65	—	100	ns	9
PORT A TIMING											
taA	Port A access time	—	35	—	40	—	50	—	80	ns	12, 14, 15
taLZ	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	12, 15, 16
taHZ	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	12, 14, 15, 16
taDV	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
taRC	Read cycle time	45	—	50	—	65	—	100	—	ns	12
taRPW	Read pulse width	35	—	40	—	50	—	80	—	ns	12, 14, 15
taRR	Read recovery time	10	—	10	—	15	—	20	—	ns	12
taS	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	10	—	ns	10, 12, 16
taH	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	10	—	ns	10, 12
taDS	Data set-up time	18	—	20	—	30	—	40	—	ns	11, 12, 14, 15
taDH(1)	Data hold time	2	—	5	—	5	—	10	—	ns	11, 12, 14, 15
taWC	Write cycle time	45	—	50	—	65	—	100	—	ns	12
taWPW	Write pulse width	35	—	40	—	50	—	80	—	ns	11, 12, 14
taWR	Write recovery time	10	—	10	—	15	—	20	—	ns	12
taWRCOM	Write recovery time after a command	35	—	40	—	50	—	80	—	ns	11

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

2668 tbl 20

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to + 125°C)

Symbol	Parameter	Commercial		Commercial and Military						Unit	Timing Figure
		IDT72511L35 IDT72521L35		IDT72511L40 IDT72521L40		IDT72511L50 IDT72521L50		IDT72511L80 IDT72521L80			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
PORT B PROCESSOR INTERFACE TIMING											
t_{BA}	Port B access time	—	35	—	40	—	50	—	80	ns	13, 14, 15
t_{BLZ}	Read or write pulse LOW to data bus at low Z	5	—	5	—	5	—	10	—	ns	13, 14, 15
t_{BHZ}	Read or write pulse HIGH to data bus at high Z	—	20	—	25	—	30	—	30	ns	14, 13, 15
t_{BDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	10	—	ns	13, 14, 15, 16
t_{BRC}	Read cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BRPW}	Read pulse width	35	—	40	—	50	—	80	—	ns	13
t_{BRR}	Read recovery time	10	—	10	—	15	—	20	—	ns	13
t_{BS}	R/$\overline{W}_B$ set-up time	5	—	5	—	5	—	10	—	ns	13
t_{BH}	R/$\overline{W}_B$ hold time	5	—	5	—	5	—	10	—	ns	13
t_{BDS}	Data set-up time	18	—	20	—	30	—	40	—	ns	13, 14, 15
t_{BDH}	Data hold time	2	—	5	—	5	—	10	—	ns	13, 14, 15
t_{BWC}	Write cycle time	45	—	50	—	65	—	100	—	ns	13
t_{BWPW}	Write pulse width	35	—	40	—	50	—	80	—	ns	13, 15
t_{BWR}	Write recovery time	10	—	10	—	15	—	20	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
t_{BA}	Port B access time	—	40	—	45	—	55	—	85	ns	17
t_{BCKC}	Clock cycle time	20	—	20	—	25	—	40	—	ns	17
t_{BCKH}	Clock pulse HIGH time	6	—	8	—	10	—	16	—	ns	17
t_{BCKL}	Clock pulse LOW time	6	—	8	—	10	—	16	—	ns	17
t_{BREQS}	Request set-up time	5	—	5	—	10	—	10	—	ns	17
t_{BREQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
t_{BACKL}	Delay from a rising clock edge to ACK switching	—	18	—	20	—	25	—	35	ns	17

2668 tbl 21

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L35 IDT72521L35 Min.	Max.	Commercial and Military IDT72511L40 IDT72521L40 Min.	Max.	IDT72511L50 IDT72521L50 Min.	Max.	IDT72511L80 IDT72521L80 Min.	Max.	Unit	Timing Figure
PORT B RETRANSMIT TIMING											
t_{BDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	15	—	ns	9, 18
PROGRAMMABLE I/O TIMING											
t_{PIOA}	Programmable I/O access time	—	25	—	25	—	30	—	30	ns	19
t_{PIOS}	Programmable I/O set-up time	10	—	10	—	15	—	15	—	ns	19
t_{PIOH}	Programmable I/O hold time	10	—	10	—	15	—	15	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	20	—	25	—	30	—	40	ns	16
t_{BYD}	Bypass delay	—	15	—	20	—	20	—	30	ns	16
t_{aBYDV}	Bypass data valid time from $\overline{DS_A}$	15	—	15	—	15	—	15	—	ns	16
t_{bBYDV} (3)	Bypass data valid time from $\overline{DS_B}$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING (1) (2)											
t_{REF}	Read clock edge to Empty Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	35	—	40	—	45	—	60	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	50	—	55	—	60	—	75	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	50	—	55	—	60	—	75	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	50	—	55	—	60	—	75	ns	21, 23

NOTES:

2668 tbl 22

1. Read and write are internal signals derived from $\overline{DS_A}$, $R/\overline{W_A}$, $\overline{DS_B}$, $R/\overline{W_B}$, $\overline{R_B}$, and $\overline{W_B}$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.

5

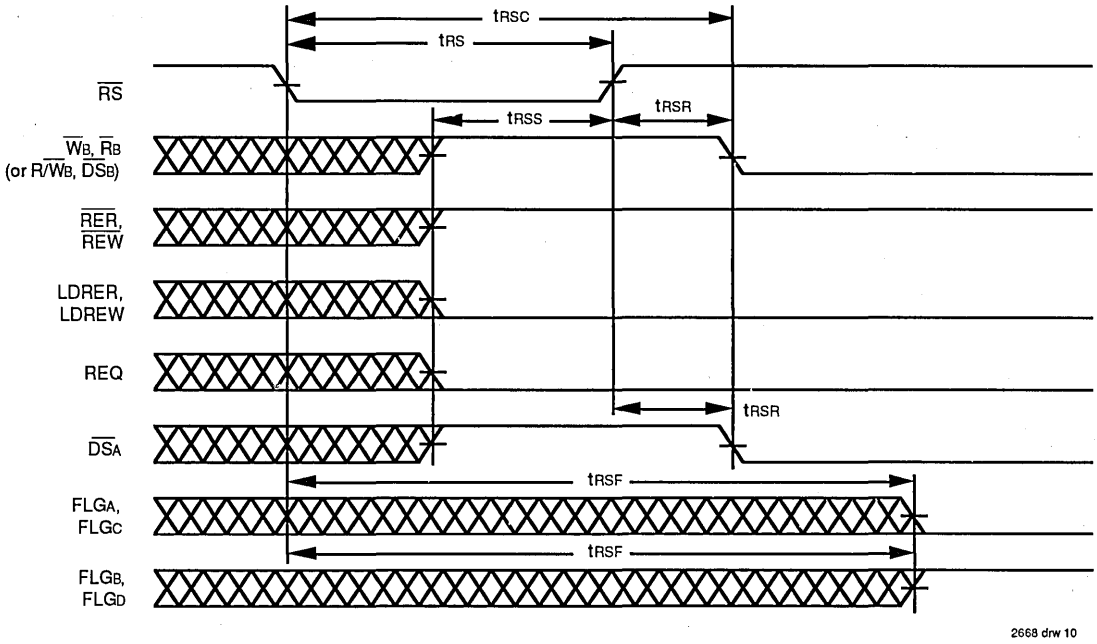


Figure 9. Hardware Reset Timing

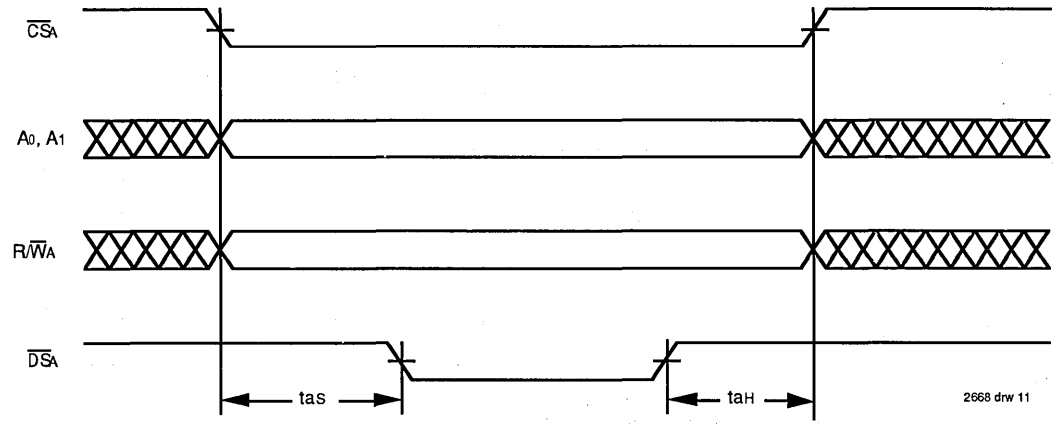


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

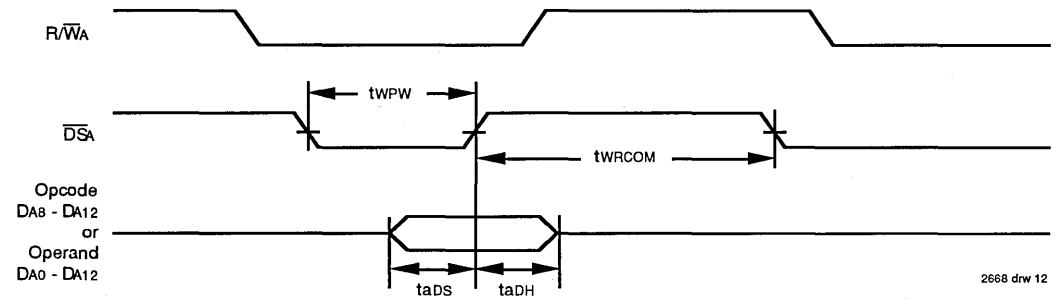
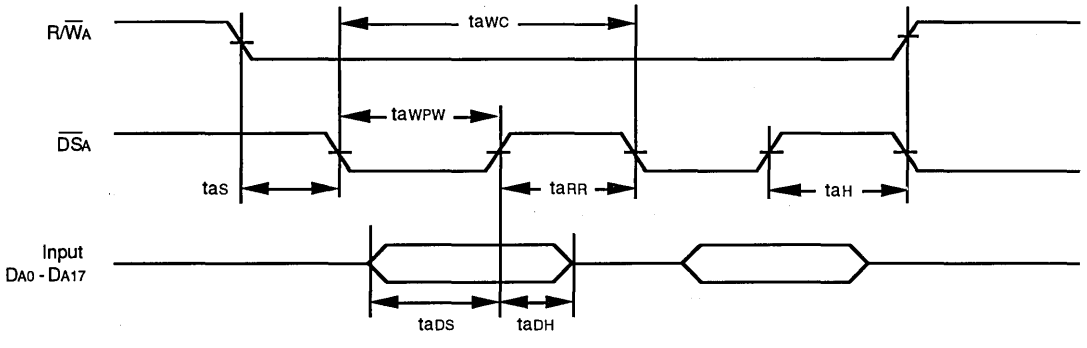


Figure 11. Port A Command Timing (write).

WRITE



READ

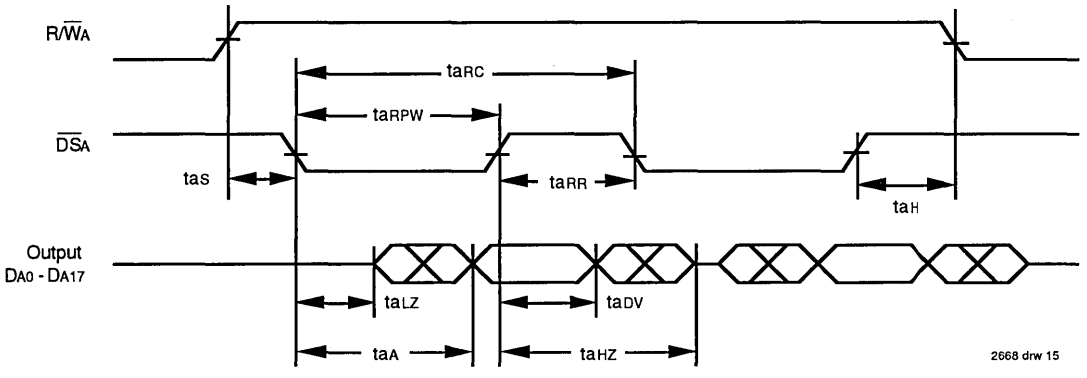
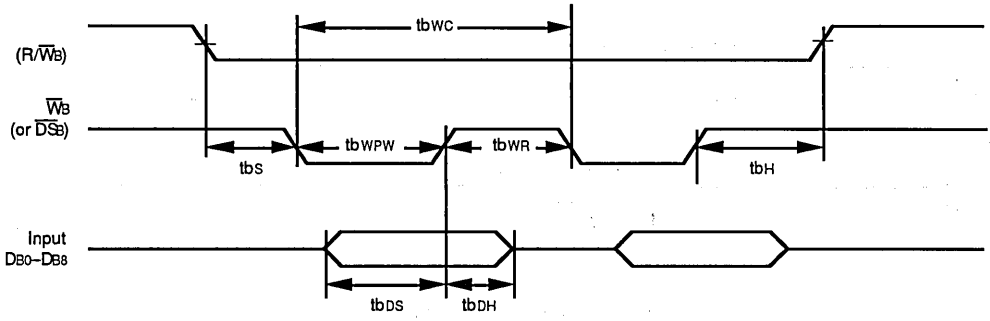


Figure 12. Read and Write Timing for Port A

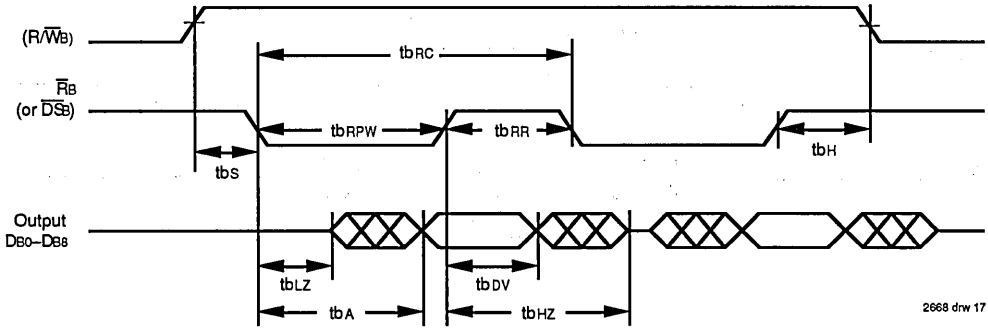
5

WRITE



NOTE:
1. $\overline{F}$B = 1

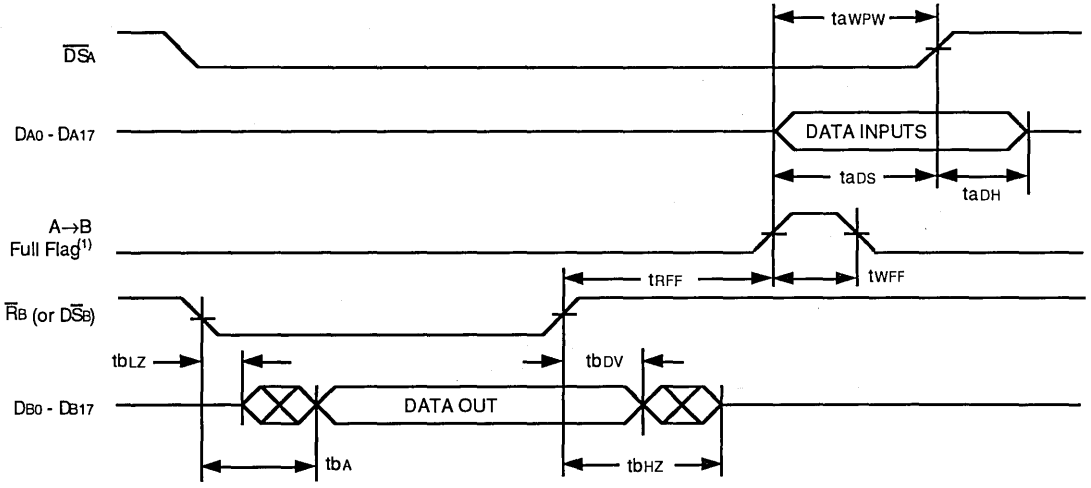
READ



NOTE:
1. $\overline{W}$B = 1

Figure 13. Port B Read and Write Timing, Processor Interface Mode Only

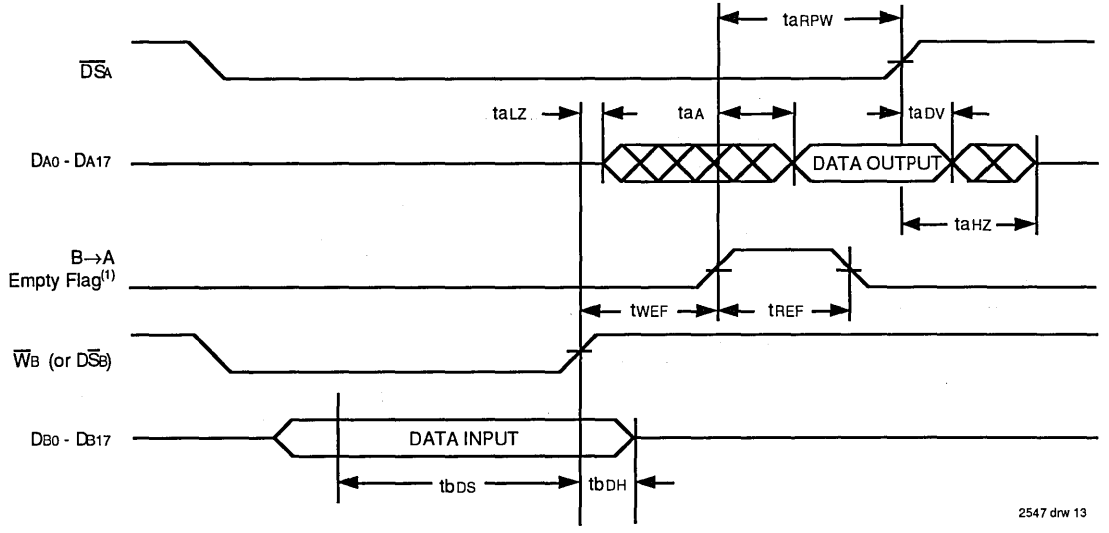
A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}$A = 0

5

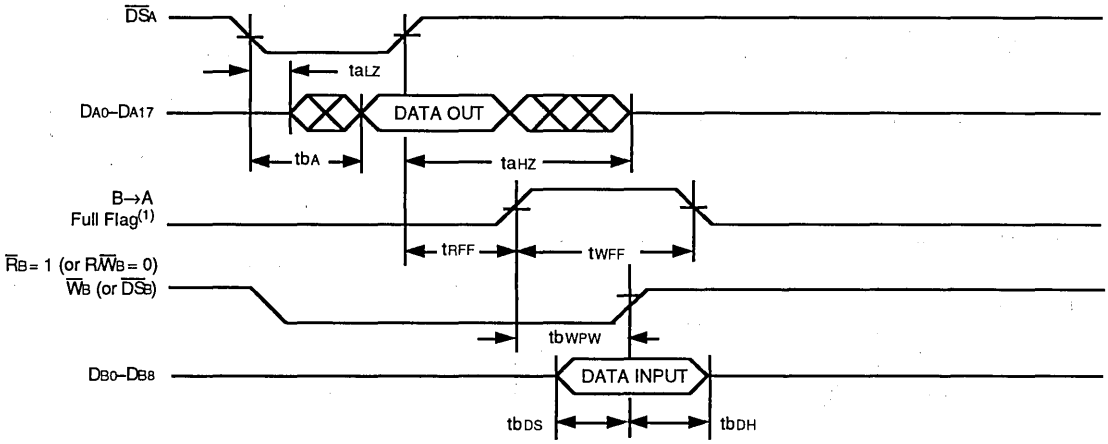
B→A FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}$A = 1

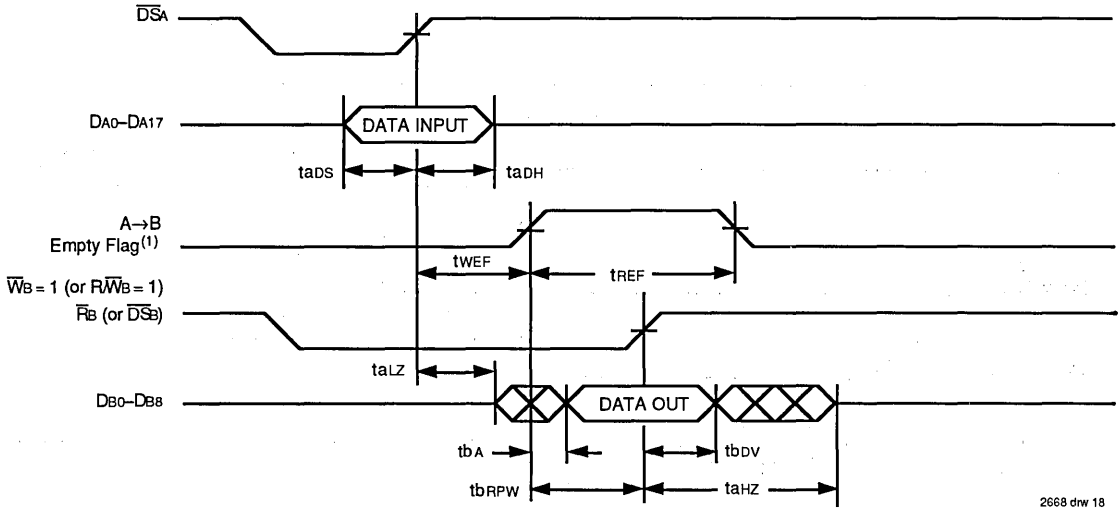
Figure 14. Port A Read and Write Flow-Through Timing, Processor Interface Mode Only

B→A FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}_A$ = 1

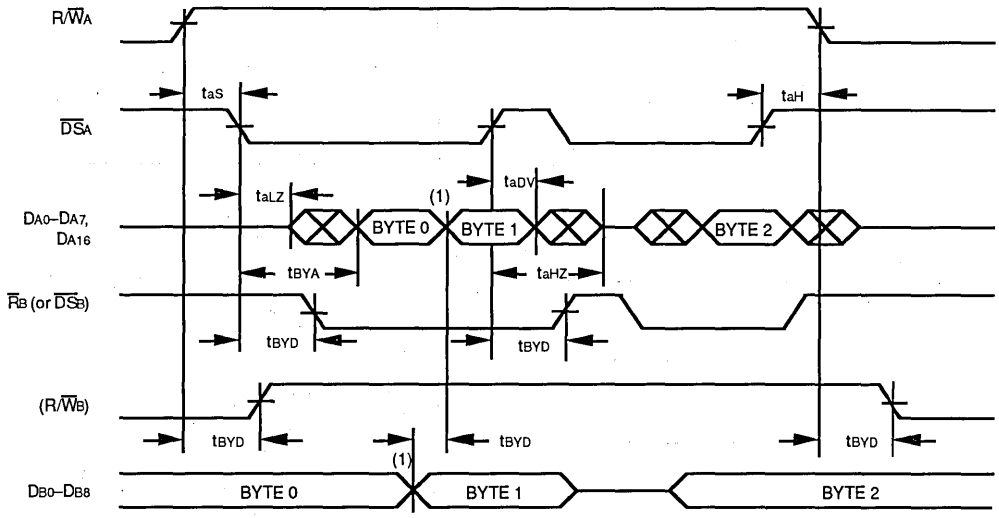
A→B FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active low.
2. R/$\overline{W}_A$ = 0

Figure 15. Port B Read and Write Flow-Through Timing, Processor Interface Mode Only

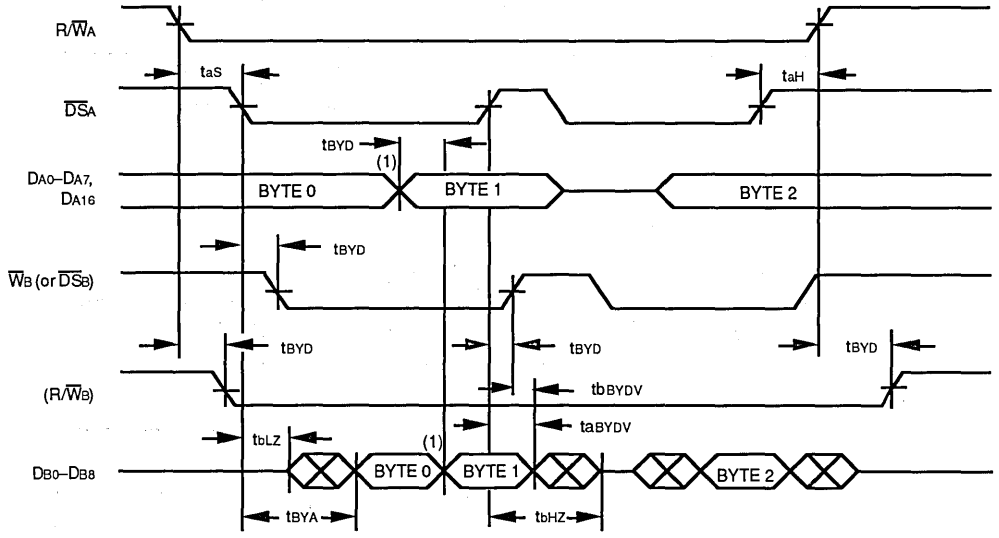
B→A READ BYPASS



NOTES:

1. Once the bypass mode starts, any data change on Port B bus (Byte 0→Byte 1) will be passed to Port A bus.
2. $\overline{W}_B$ = 1

A→B WRITE BYPASS



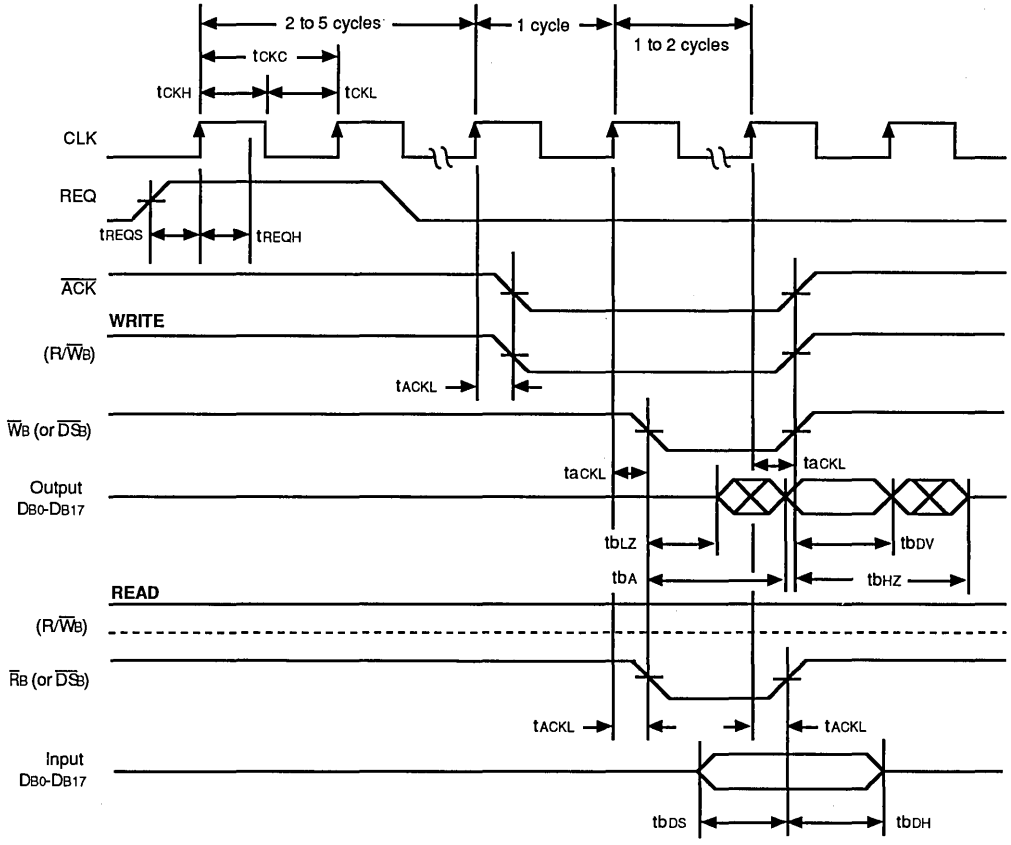
2668 drw 16

NOTES:

1. Once the bypass mode starts, any data change on Port A bus (Byte 0→Byte 1) will be passed to Port B bus.
2. $\overline{R}_B$ = 1

Figure 16. Bypass Path Timing, BiFIFO Must Be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



BLOCK DMA TRANSFER

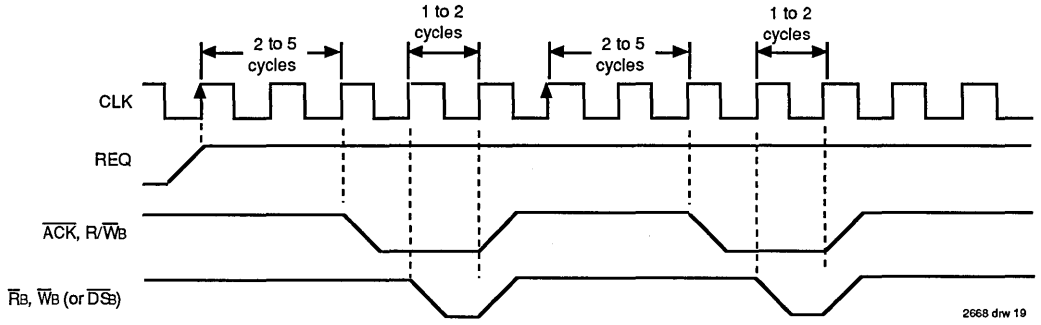


Figure 17. Port B Read and Write DMA timing. Peripheral Interface Mode Only

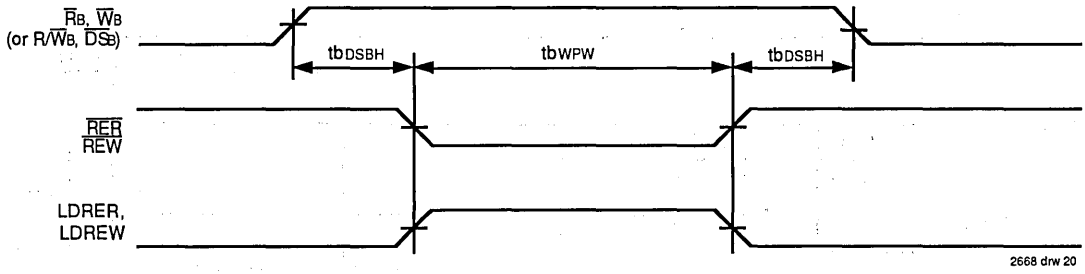


Figure 18. Port B Reread and Rewrite Timing for Intelligent Reread/Rewrite

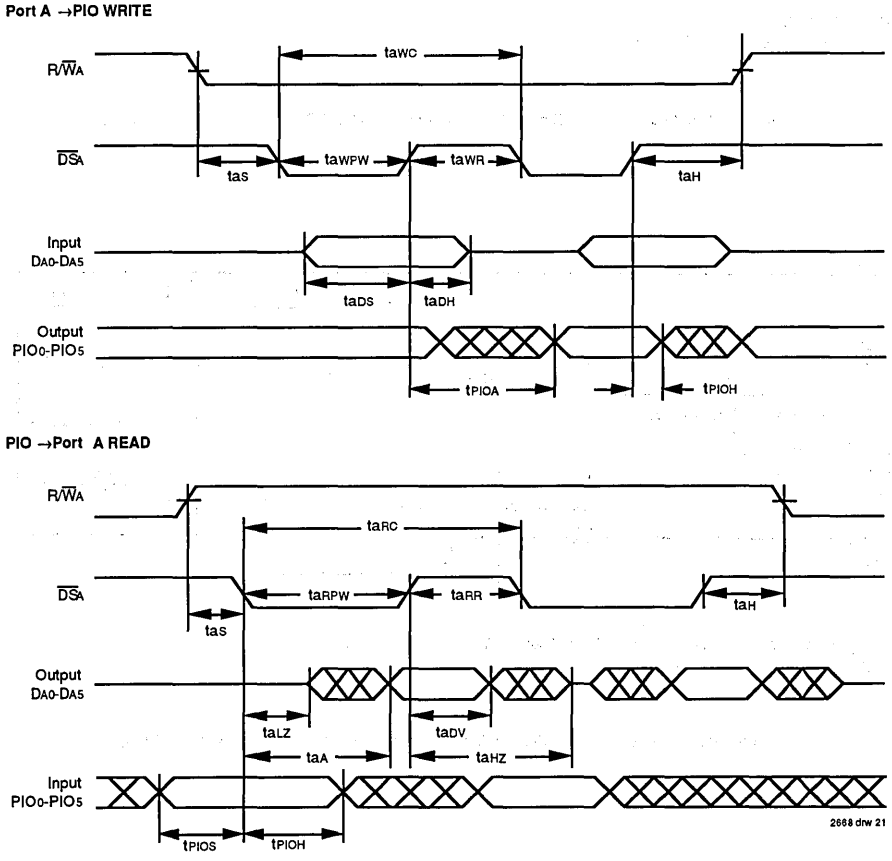
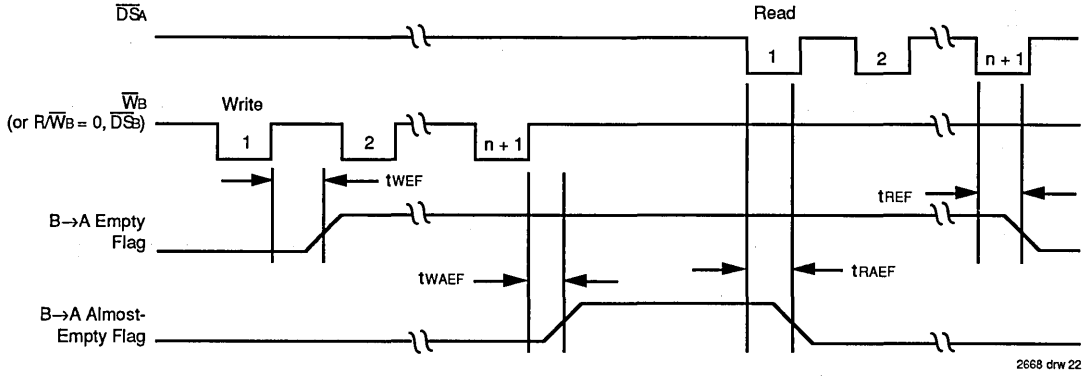
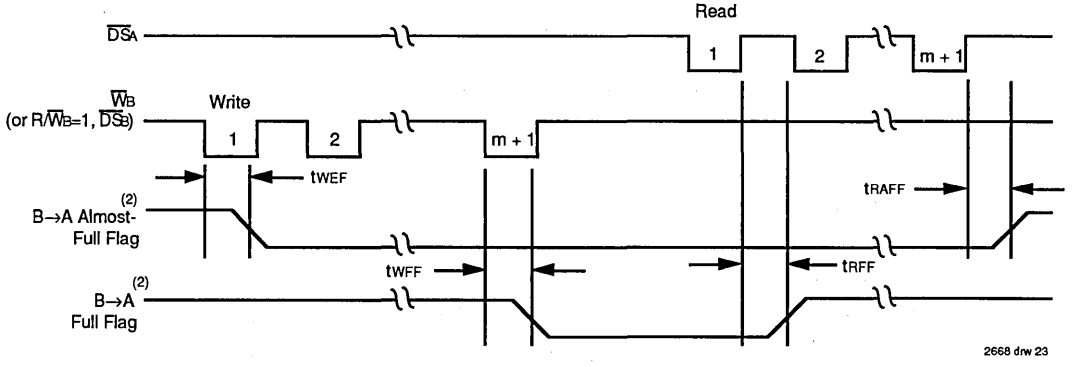


Figure 19. Programmable I/O Timing



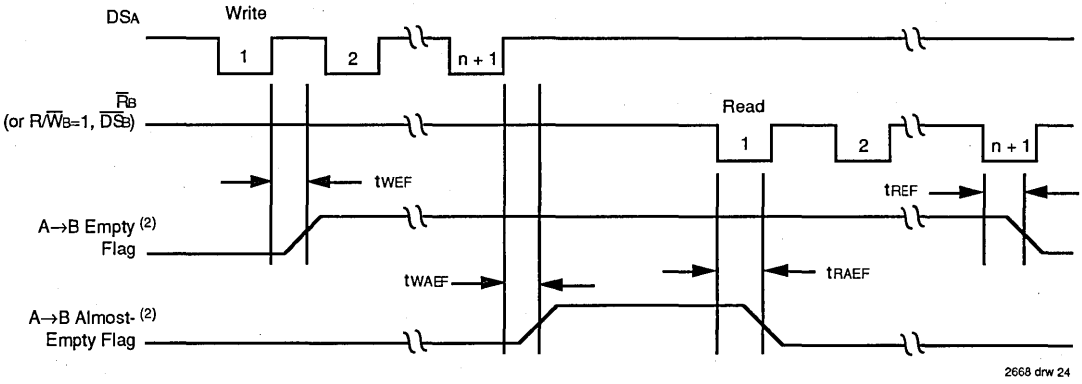
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. R/WA = 1

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO, (n = programmed offset)



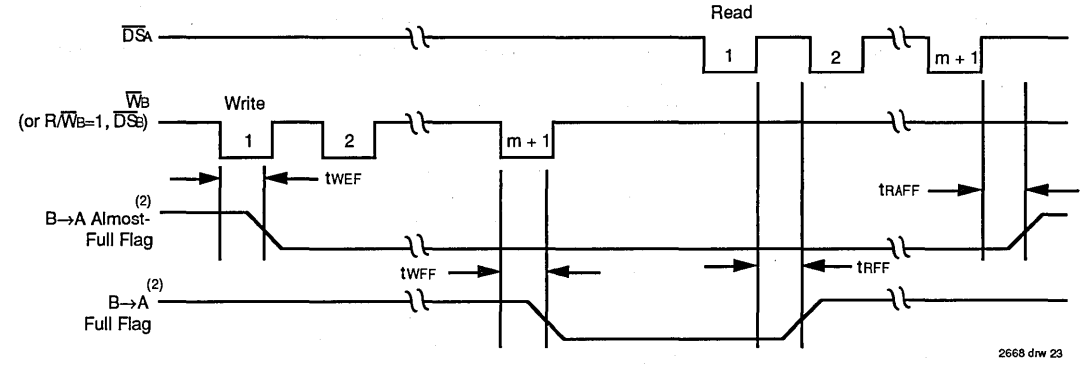
NOTES:
1. B→A FIFO initially contains D − (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active low.
3. R/WA = 1

Figure 21. Full and Almost-Full Flag Timing for B→A FIFO, (m = programmed offset)



NOTES:
1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active low.
3. R/WA = 1

Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO, (n = programmed offset)



NOTES:
1. B→A FIFO initially contains D − (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active low.
3. R/WA = 1

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO, (m = programmed offset)

5

Integrated Device Technology, Inc.

PARALLEL SyncBiFIFO™ (CLOCKED BIDIRECTIONAL FIFO) 256 x 18-BIT AND 512 x 18-BIT

PRELIMINARY
IDT72605
IDT72615

FEATURES:

- Two independent FIFO memories for fully bidirectional data transfers
- 256 x 18 organization (IDT 72605)
- 512 x 18 organization (IDT 72615)
- Synchronous interface for fast (25ns) read and write cycle times
- Each data port has an independent clock and read/write control
- Output enable is provided on each port as a three-state control of the data bus
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Programmable flag offset can be set to any depth in the FIFO
- The synchronous BiFIFO is packaged in a 68-pin PGA and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72605 and IDT72615 are very high speed, low power bidirectional FIFO memories with synchronous interface for fast read and write cycle times. The SyncBiFIFO™ is a data buffer that can store or retrieve information from two sources simultaneously. Two dual-port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction.

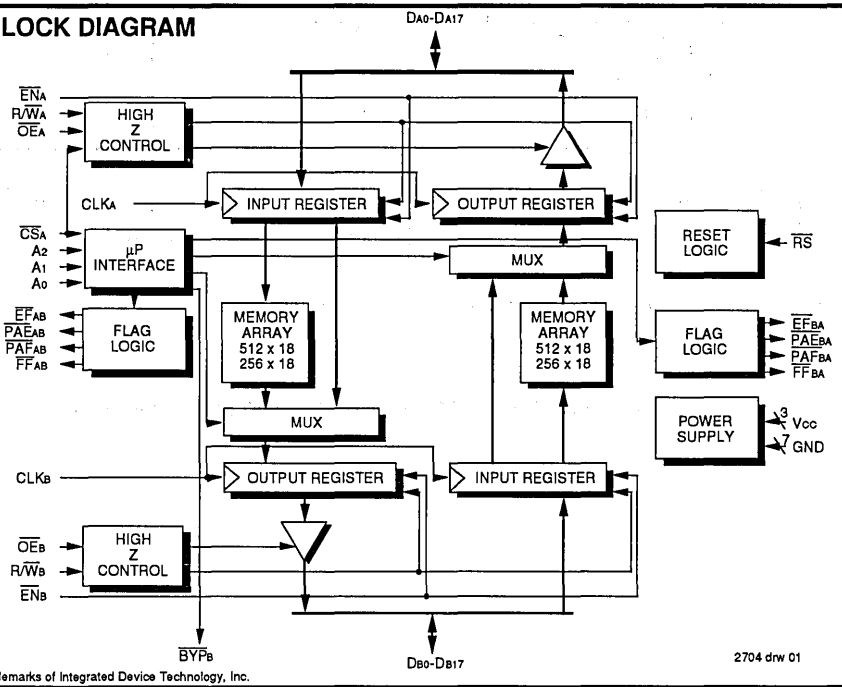
The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high impedance state.

Bypass control allows data to be directly transferred from input to output register in either direction.

The SyncBiFIFO has eight flags. The flag pins are full, empty, almost-full, and almost-empty for both FIFO memories. The offset depths of the almost-full and almost-empty flags can be programmed to any location.

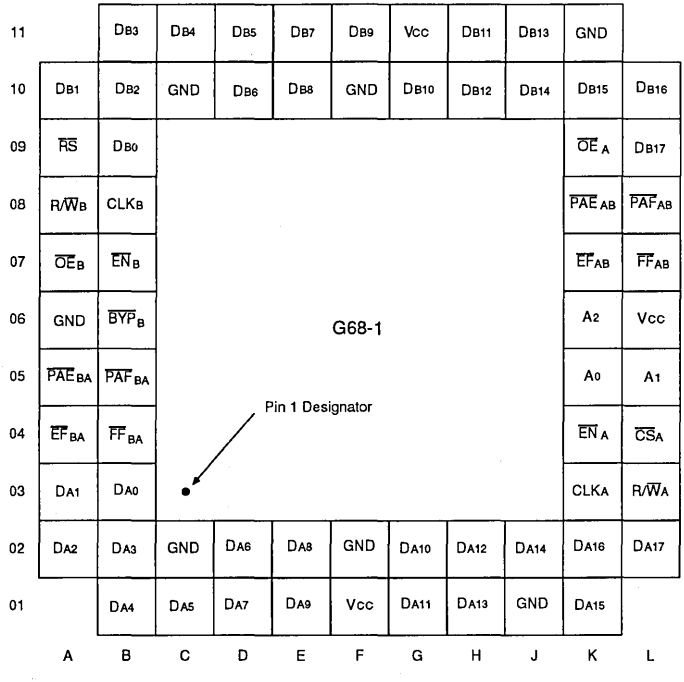
The SyncBiFIFO is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



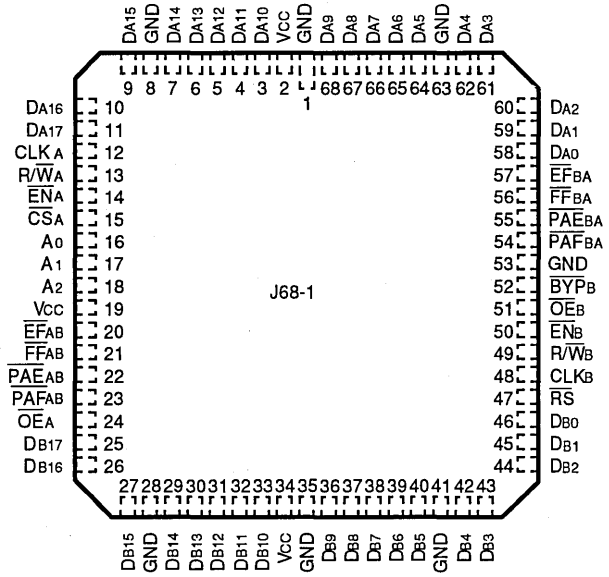
SyncBiFIFO and CEMOS are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2704 drw 02

PGA
Top View



PLCC
Top View

2704 drw 03

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs & outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when $\overline{CS}_A$ is LOW. Port A is inactive if $\overline{CS}_A$ is HIGH.
$R/\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. If $R/\overline{W}_A$ is LOW, Data A input data is written into Port A. If $R/\overline{W}_A$ is HIGH, Data A output data is read from Port A. In bypass mode, when $R/\overline{W}_A$ is LOW, message is written into A→B output register. If $R/\overline{W}_A$ is HIGH, message is read from B→A output register.
CLK_A	Clock A	I	CLK_A is typically a free running clock. Data is read or written into Port A on the rising edge of CLK_A.
$\overline{EN}_A$	Enable A	I	When $\overline{EN}_A$ is LOW, data can be read or written to Port A. When $\overline{EN}_A$ is HIGH, no data transfers occur.
$\overline{OE}_A$	Output Enable A	I	When $R/\overline{W}_A$ is HIGH , Port A is an output bus and $\overline{OE}_A$ controls the high impedance state of D_{A0}-D_{A17}. If $\overline{OE}_A$ is HIGH, Port A is in a high impedance state. If $\overline{OE}_A$ is LOW while $\overline{CS}_A$ is LOW and $R/\overline{W}_A$ is HIGH, Port A is in an active (low impedance) state.
A_0, A_1, A_2	Addresses	I	When $\overline{CS}_A$ is asserted, A_0, A_1, A_2 and $R/\overline{W}_A$ are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs & outputs for the 18-bit Port B bus.
$R/\overline{W}_B$	Read/Write B	I	This pin controls the read or write direction of Port B. If $R/\overline{W}_B$ is LOW, Data B input data is written into Port B. If $R/\overline{W}_B$ is HIGH, Data B output data is read from Port B. In bypass mode, when $R/\overline{W}_B$ is LOW, message is written into A→B output register. If $R/\overline{W}_B$ is HIGH, message is read from B→A output register.
CLK_B	Clock B	I	Clock B is typically a free running clock. Data is read or written into Port B on the rising edge of CLK_B.
$\overline{EN}_B$	Enable B	I	When $\overline{EN}_B$ is LOW, data can be read or written to Port B. When $\overline{EN}_B$ is HIGH, no data transfers occur.
$\overline{OE}_B$	Output Enable B	I	When $R/\overline{W}_B$ is HIGH , Port B is an output bus and $\overline{OE}_B$ controls the high impedance state of D_{B0}-D_{B17}. If OE_B is HIGH, Port B is in a high impedance state. If $\overline{OE}_B$ is LOW while $R/\overline{W}_B$ is HIGH, Port B is in an active (low impedance) state.
$\overline{EF}_{AB}$	A→B Empty Flag	O	When $\overline{EF}_{AB}$ is LOW, the A→B FIFO is empty and further data reads from Port B are inhibited. When $\overline{EF}_{AB}$ is HIGH, the FIFO is not empty. $\overline{EF}_{AB}$ is synchronized to CLK_B. In the bypass mode, $\overline{EF}_{AB}$ HIGH indicates that data D_{A0}-D_{A17} is available for passing through. After the data D_{B0}-D_{B17} has been read, $\overline{EF}_{AB}$ goes LOW.
$\overline{PAE}_{AB}$	A→B Programmable Almost-Empty Flag	O	When $\overline{PAE}_{AB}$ is LOW, the A→B FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{AB}$ Register. When $\overline{PAE}_{AB}$ is HIGH, the A→B FIFO contains more than offset in $\overline{PAE}_{AB}$ Register. The default offset value for $\overline{PAE}_{AB}$ Register is 8. $\overline{PAE}_{AB}$ is synchronized to CLK_B.
$\overline{PAF}_{AB}$	A→B Programmable Almost-Full Flag	O	When $\overline{PAF}_{AB}$ is LOW, the A→B FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{AB}$ Register. When PAF_{AB} is HIGH, the A→B FIFO contains less than or equal to the depth minus the offset in PAF_{AB} Register. The default offset value for PAF_{AB} Register is 8. $\overline{PAF}_{AB}$ is synchronized to CLK_A.
$\overline{FF}_{AB}$	A→B Full Flag	O	When $\overline{FF}_{AB}$ is LOW, the A→B FIFO is full and further data writes into Port A are inhibited. When $\overline{FF}_{AB}$ is HIGH, the FIFO is not full. $\overline{FF}_{AB}$ is synchronized to CLK_A. In bypass mode, $\overline{FF}_{AB}$ tells Port A that a message is waiting in Port B's output register. If $\overline{FF}_{AB}$ is LOW, a bypass message is in the register. If $\overline{FF}_{AB}$ is HIGH, Port B has read the message and another message can be written into Port A.
$\overline{EF}_{BA}$	B→A Empty Flag	O	When $\overline{EF}_{BA}$ is LOW, the B→A FIFO is empty and further data reads from Port A are inhibited. When $\overline{EF}_{BA}$ is HIGH, the FIFO is not empty. $\overline{EF}_{BA}$ is synchronized to CLK_A. In the bypass mode, $\overline{EF}_{BA}$ HIGH indicates that data D_{B0}-D_{B17} is available for passing through. After the data D_{A0}-D_{A17} has been read, $\overline{EF}_{BA}$ goes LOW on the following cycle.
$\overline{PAE}_{BA}$	B→A Programmable Almost-Empty Flag	O	When $\overline{PAE}_{BA}$ is LOW, the B→A FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{BA}$ Register. When $\overline{PAE}_{BA}$ is HIGH, the B→A FIFO contains more than offset in $\overline{PAE}_{BA}$ Register. The default offset value for $\overline{PAE}_{BA}$ Register is 8. $\overline{PAE}_{BA}$ is synchronized to CLK_A.
$\overline{PAF}_{BA}$	B→A Programmable Almost-Full Flag	O	When $\overline{PAF}_{BA}$ is LOW, the B→A FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{BA}$ Register. When $\overline{PAF}_{BA}$ is HIGH, the B→A FIFO contains less than or equal to the depth minus the offset in $\overline{PAF}_{BA}$ Register. The default offset value for $\overline{PAF}_{BA}$ Register is 8. $\overline{PAF}_{BA}$ is synchronized to CLK_B.

2704 tbl 01

PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
$\overline{FF}_{BA}$	B→A Full Flag	O	When $\overline{FF}_{BA}$ is LOW, the B→A FIFO is full and further data writes into Port B are inhibited. When $\overline{FF}_{BA}$ is HIGH, the FIFO is not full. $\overline{FF}_{BA}$ is synchronized to CLK_B. In bypass mode, $\overline{FF}_{BA}$ tells Port B that a message is waiting in Port A's output register. If $\overline{FF}_{BA}$ is LOW, a bypass message is in the register. If $\overline{FF}_{BA}$ is HIGH, Port A has read the message and another message can be written into Port B.
$\overline{BYP}_B$	Port B Bypass Flag	O	This flag informs Port B that the Synchronous BiFIFO is in bypass mode. When BYP_B is LOW, Port A has placed the FIFO into bypass mode. If $\overline{BYP}_B$ is HIGH, the Synchronous BiFIFO passes data into memory. $\overline{BYP}_B$ is synchronized to CLK_B.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all Synchronous BiFIFO functions.
V_{CC}	Power		There are three +5V power pins.
GND	Ground		There are seven Ground pins at 0V.

2704 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2704 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2704 tbl 04
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2704 tbl 05
1. With output deselected.
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72615L IDT72605L Commercial t_{CLK} = 25, 35, 50ns Min.	Typ.	Max.	IDT72615L IDT72605L Military t_{CLK} = 30, 35, 50ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Average Vcc Power Supply Current	—	—	230	—	—	250	mA

2704 tbl 06

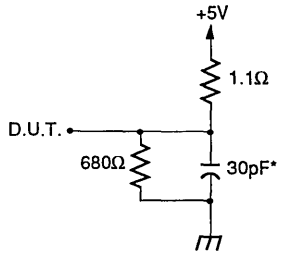
NOTES:
1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}; 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open. Testing frequency f=20MHz

5

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2

2704 tbl 07



or equivalent circuit 2704 drw 05

Figure 2. Output Load

* Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = -55°C to +125°C)

		Com'l.		Mil.		Com'l. and Mil.					
		IDT72615L25 IDT72605L25		IDT72615L30 IDT72605L30		IDT72615L35 IDT72605L35		IDT72615L50 IDT72605L50			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Timing Figures
f_{CLK}	Clock frequency	—	40	—	33	—	28	—	20	MHz	—
t_{CLK}	Clock cycle time	25	—	30	—	35	—	50	—	ns	4,5,6,7
t_{CLKH}	Clock high time	10	—	12	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{CLKL}	Clock low time	10	—	12	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{RS}	Reset pulse width	25	—	30	—	35	—	50	—	ns	3
t_{RSS}	Reset set-up time	15	—	18	—	21	—	30	—	ns	3
t_{RSR}	Reset recovery time	15	—	18	—	21	—	30	—	ns	3
t_{RSF}	Reset to flags in intial state	—	25	—	30	—	35	—	50	ns	3
t_A	Data access time	3	15	3	18	3	21	3	25	ns	5,7,8,9,10,11
t_{CS}	Control signal set-up time(1)	6	—	7	—	8	—	10	—	ns	4,5,6,7,8,9,10,11,12, 13,14,15
t_{CH}	Control signal hold time(1)	1	—	1	—	1	—	1	—	ns	4,5,6,7,10,11,12,13, 14,15
t_{DS}	Data set-up time	6	—	7	—	8	—	10	—	ns	4,6,8,9,10,11
t_{DH}	Data hold time	1	—	1	—	1	—	1	—	ns	4,6
t_{OE}	Output Enable LOW to output data valid(2)	3	13	3	16	3	20	3	28	ns	5,7,8,9,10,11
t_{OLZ}	Output Enable LOW to data bus at low Z(2)	0	—	0	—	0	—	0	—	ns	5,7,8,9,10,11
t_{OHZ}	Output Enable HIGH to data bus at high Z(2)	3	13	3	16	3	20	3	28	ns	5,7,10,11
t_{FF}	Clock to Full Flag time	—	15	—	18	—	21	—	30	ns	4,6,10,11
t_{EF}	Clock to Empty Flag time	—	15	—	18	—	21	—	30	ns	5,7,8,9,10,11
t_{PAE}	Clock to Programmable Almost Empty Flag time	—	15	—	18	—	21	—	30	ns	12,14
t_{PAF}	Clock to Programmable Almost Full Flag time	—	15	—	18	—	21	—	30	ns	13,15
t_{SKEW1}	Skew between CLK_A & CLK_B for Empty/Full Flags(2)	12	—	15	—	17	—	20	—	ns	4,5,6,7,8,9,10,11
t_{SKEW2}	Skew between CLK_A & CLK_B for Programmable Flags(2)	19	—	22	—	25	—	34	—	ns	4, 7,12,13,14,15

2704 tbl 08

NOTES

1. Control signals refer to $\overline{CS}_A$, $R/\overline{W}_A$, $\overline{EN}_A$, A_2, A_1, A_0, $R/\overline{W}_B$, $\overline{EN}_B$.
2. Minimum values are guaranteed by design.

FUNCTIONAL DESCRIPTION

IDT's SyncBiFIFO is versatile for both multiprocessor and peripheral applications. Data can be stored or retrieved from two sources simultaneously.

The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Two dual-port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high impedance state. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the 18-bit bypass path.

The SyncBiFIFO can be used in multiples of 18-bits. In a 36- to 36-bit configuration, two SyncBiFIFOs operate in parallel. Both devices are programmed simultaneously, 18 data bits to each device. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, etc.) by adding more SyncBiFIFOs to the configuration. Figure 1 show multiple SyncBiFIFOs configured for multiprocessor communication.

The microprocessor or microcontroller connected to Port A controls all operations of the SyncBiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B interfaces with a second processor. The Port B control pins are inputs driven by the second processor.

RESET

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state with $\overline{CS}_A$, $\overline{EN}_A$ and $\overline{EN}_B$ HIGH. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The A→B and B→A FIFO Empty Flags ($\overline{EF}_{AB}$, $\overline{EF}_{BA}$) and Programmable Almost Empty Flags ($\overline{PAE}_{AB}$, $\overline{PAE}_{BA}$) will be set to low after t_{RSF}. The A→B and B→A FIFO Full Flags ($\overline{FF}_{AB}$, $\overline{FF}_{BA}$) and Programmable Almost Full Flags ($\overline{PAF}_{AB}$, $\overline{PAF}_{BA}$) will be set to high after t_{RSF}. After the reset, the offsets of the Almost-Empty Flags and Almost- Full Flags for the A→B and B→A FIFO offset default to 8.

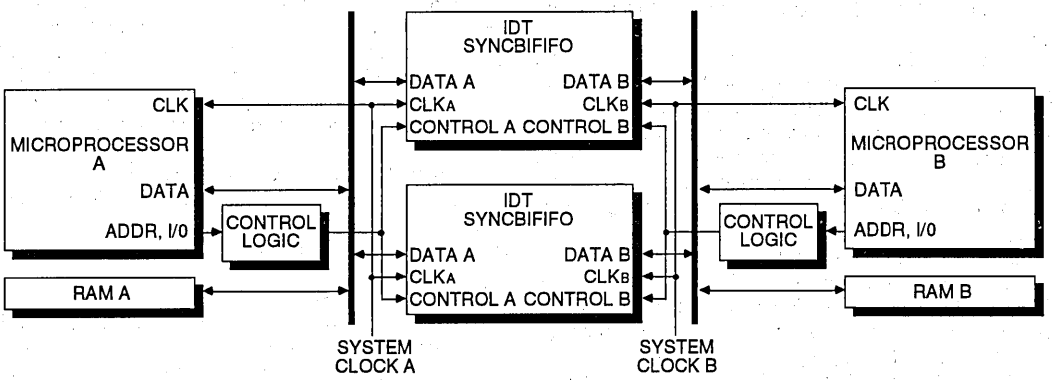
PORT A INTERFACE

The SyncBiFIFO™ is straightforward to use in microprocessor-based systems because each port has a standard microprocessor control set. Port A interfaces with microprocessor through the three address pins (A_2-A_0) and a Chip Select $\overline{CS}_A$ pins. When $\overline{CS}_A$ is asserted, A_2,A_1,A_0 and $R/\overline{W}_A$ are used to select one of six internal resources (Table 1).

With A_2=0 and A_1=0, A_0 determines whether data can be read out of output register or be written into the FIFO (A_0=0), or the data can pass through the FIFO through the bypass path (A_0=1).

With A_2=1, four programmable flags (two A→B FIFO programmable flags and two B→A FIFO programmable flags) can be selected: the A→B FIFO Almost-Empty Flag Offset (A_1=0, A_0=0), A→B FIFO Almost-Full Flag Offset (A_1=0, A_0=1), B→A FIFO Almost-Empty Flag Offset (A_1=1, A_0=0), B→A FIFO Almost-Full Flag Offset (A_1=1, A_0=1).

Port A is disabled when $\overline{CS}_A$ is deasserted and data A is in high impedance state.



2704 drw 04

NOTES:
1. Upper SyncBiFIFO only is used in 18- to 18-bit configuration.
2. Control A Consists of $R/\overline{W}_A$, $\overline{EN}_A$, $\overline{OE}_A$, $\overline{CS}_A$, A_2, A_1, A_0. Control B consists of $R/\overline{W}_B$, $\overline{EN}_B$, $\overline{OE}_B$.

Figure 1. 36- to 36-bit Processor Interface Configuration

$\overline{CS}_A$	R/$\overline{W}_A$	$\overline{EN}_A$	$\overline{OE}_A$	Data A I/O	Port A Operation
0	0	0	0	I	Data A is written on CLKA ↑. This write cycle immediately following low impedance cycle is prohibited.
0	0	0	1	I	Data A is written on CLKA ↑.
0	0	1	X	I	Data A is ignored
0	1	0	0	O	Data is read(1) from RAM array to output register on CLKA ↑, Data A is low impedance
0	1	0	1	O	Data is read(1) from RAM array to output register on CLKA ↑, Data A is high impedance
0	1	1	0	O	Output register does not change(2), Data A is low impedance
0	1	1	1	O	Output register does not change(2), Data A is high impedance
1	0	X	X	I	Data A is ignored(3)
1	1	X	X	O	Data A is high impedance(3)

2704 tbl 09

NOTES

1. When $A_2A_1A_0$ = 000, the next B→A FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data from the Port B input register is read from the Port A output register. If $A_2A_1A_0$ = 1XX, a flag offset register is selected and its offset is read out through Port A output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port A output register does not change and the B→A read pointer does not advance.
3. If $\overline{CS}_A$ is HIGH, then BYP_B is HIGH. No bypass occur under this condition.

Table 1. Port A Operation Control Signals

BYPASS PATH

The bypass paths provide direct communication between Port A and Port B. There are two full 18-bit bypass paths, one in each direction. During a bypass operation, data is passed directly between the input and output registers, and the FIFO memory is undisturbed.

Port A initiates and terminates all bypass operations. The bypass flag, $\overline{BYP}_B$, is asserted to inform Port B that a bypass operation is beginning. The bypass flag state is controlled by the Port A controls, although the $\overline{BYP}_B$ signal is synchronized to CLK_B. So, $\overline{BYP}_B$ is asserted on the next rising edge of CLK_B when $A_2A_1A_0$=001and CS_A is Low. When Port A returns to normal FIFO mode ($A_2A_1A_0$=000 or CS_A is High), $\overline{BYP}_B$ is deasserted on the next CLK_B rising edge.

Once the SyncBiFIFO is in bypass mode, all data transfers are controlled by the standard Port A (R/$\overline{W}_A$, CLK_A, $\overline{EN}_A$, $\overline{OE}_A$) and Port B (R/$\overline{W}_B$, CLK_B, $\overline{EN}_B$, $\overline{OE}_B$) interface pins. Each bypass path can be considered as a one word deep FIFO. Data is held in each input register until it is read. Since the controls of each port operate independently, Port A can be reading bypass data at the same time Port B is reading bypass data.

When R/$\overline{W}_A$ and $\overline{EN}_A$ is LOW, data on pins D_{A0}-D_{A17} is written into Port A input register. Following the rising edge of CLK_A for this write, the A→B Full Flag ($\overline{FF}_{AB}$) goes LOW. Subsequent writes into Port A are blocked by internal logic until $\overline{FF}_{AB}$ goes HIGH again. On the next CLK_B rising edge, the A→B Empty Flag ($\overline{EF}_{AB}$) goes HIGH indicating to Port B that data is available. Once R/$\overline{W}_B$ is HIGH and $\overline{EN}_B$ is LOW, data is read into the Port B output register. $\overline{OE}_B$ still controls whether Port B is in a high-impedance state. When $\overline{OE}_B$ is LOW, the output register data appears at D_{B0}-D_{B17}. $\overline{EF}_{AB}$ goes LOW following the CLK_B rising edge for this read. $\overline{FF}_{AB}$ goes HIGH on the next CLK_A rising edge, letting Port A know that another word can be written through the bypass path.

Bypass data transfers from Port B to Port A work in a similar manner with $\overline{EF}_{BA}$ and $\overline{FF}_{BA}$ indicating the Port A output register state.

When the Port A address changes from bypass mode ($A_2A_1A_0$=001) to FIFO mode ($A_2A_1A_0$=000) on the rising edge of CLK_A, the data held in the Port B output register may be overwritten. Unless Port A monitors the $\overline{BYP}_B$ pin and waits for Port B to clock out the last bypass word, data from the A→B FIFO will overwrite data in the Port B output register. $\overline{BYP}_B$ will go HIGH on the rising edge of CLK_B signifying that Port B has finished its last bypass operation. Port B must read any bypass data in the output register on this last CLK_B clock or it is lost and the SyncBiFIFO returns to FIFO operations. It is especially important to monitor $\overline{BYP}_B$ when CLK_B is much slower than CLK_A to avoid this condition. $\overline{BYP}_B$ will also go HIGH after $\overline{CS}_A$ is brought HIGH; in this manner the Port B bypass data may also be lost.

Since the Port A processor controls $\overline{CS}_A$ and the bypass mode, this scenario can be handled for B→A bypass data. The Port A processor must be set up to read the last bypass word before leaving bypass mode.

PORT A CONTROL SIGNALS

The Port A control signals pins dictate the various operations shown in Table 2. Port A is accessed when $\overline{CS}_A$ is LOW, and is inactive if $\overline{CS}_A$ is HIGH. R/$\overline{W}_A$ and $\overline{EN}_A$ lines determine when Data A can be written or read. If R/$\overline{W}_A$ and $\overline{EN}_A$ are LOW, data is written into input register on the low-to-high transition of CLK_A. If R/$\overline{W}_A$ is HIGH and $\overline{OE}_A$ is LOW, data comes out of bus and is read from output register into three-state buffer. Refer to pin descriptions for more information.

$\overline{CS}_A$	A_2	A_1	A_0	Read	Write
0	0	0	0	B→A FIFO	A→B FIFO
0	0	0	1	18-bit Bypass Path	
0	1	0	0	A→B FIFO Almost-Empty Flag Offset	
0	1	0	1	A→B FIFO Almost-Full Flag Offset	
0	1	1	0	B→A FIFO Almost-Empty Flag Offset	
0	1	1	1	B→A FIFO Almost-Full Flag Offset	
1	X	X	X	Port A Disabled	

2704 tbl 10

Table 2. Accessing Port A Resources Using $\overline{CS}_A$, A_2, A_1, and A_0

PROGRAMMABLE FLAGS

The IDT SyncBiFIFO has eight flags: four flags for A→B FIFO ($\overline{EF}_{AB}$, $\overline{PAE}_{AB}$, $\overline{PAF}_{AB}$, $\overline{FF}_{AB}$), and four flags for B→A FIFO ($\overline{EF}_{BA}$, $\overline{PAE}_{BA}$, $\overline{PAF}_{BA}$, $\overline{FF}_{BA}$). The Empty and Full flags are fixed, while the Almost Empty and Almost Full offsets can be set to any depth through the Flag Offset Registers (see Table 3). The flags are asserted at the depths shown in the Flag Truth Table (Table 4). After reset, the programmable flag offsets are set to 8. This means the Almost Empty flags are asserted at Empty + 8 words deep, and the Almost Full flags are asserted at Full - 8 words deep.

The $\overline{PAE}_{AB}$ is synchronized to CLK_B, while $\overline{PAF}_{AB}$ is synchronized to CLK_A; and $\overline{PAE}_{BA}$ is synchronized to CLK_A, while $\overline{PAF}_{BA}$ is synchronized to CLK_B. If the minimum time (t_{SKEW2}) between a rising CLK_B and a rising CLK_A is met, the flag will change state on the current clock; otherwise, the flag may not change state until the next clock rising edge. For the specific flag timings, refer to Figures 12-15.

5

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{PAE}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Full Flag Offset								
$\overline{PAE}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Full Flag Offset								

2704 tbl 11

NOTE:
1. Bit 8 must be set to 0 for the IDT72605 (256 x 18) Synchronous BiFIFO.

Table 3. Flag Offset Register Format

Number of Words in FIFO					
From	To	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	Low	Low	High	High
1	n	High	Low	High	High
n+1	D-(m+1)	High	High	High	High
D-m	D-1	High	High	Low	High
D	D	High	High	Low	Low

n = Programmable Empty Offset ($\overline{PAE}_{AB}$ Register or $\overline{PAE}_{BA}$ Register)
m = Programmable Full Offset ($\overline{PAF}_{AB}$ Register or $\overline{PAF}_{BA}$ Register)
D = FIFO Depth (IDT72605 = 256 words, IDT72615= 512 words)

2704 tbl 12

Table 4. Internal Flag Truth Table

PORT B CONTROL SIGNALS

The Port B control signal pins dictate the various operations shown in Table 5. Port B is independent of $\overline{CS}_A$. $R/\overline{W}_B$ and $\overline{EN}_B$ lines determine when Data can be written or read in Port B. If $R/\overline{W}_B$ and $\overline{EN}_B$ are LOW, data is written into input register, and on low-to-high transition of CLK_B data is written into input register and the FIFO memory. If $R/\overline{W}_B$ is HIGH and $\overline{OE}_B$ is LOW, data comes out of bus and is read from output register into three-state buffer. In bypass mode, if $R/\overline{W}_B$ is LOW, bypass messages are transferred into B→A output register. If $R/\overline{W}_A$ is HIGH, bypass messages are transferred into A→B output register. Refer to pin descriptions for more information.

$R/\overline{W}_B$	$\overline{EN}_B$	$\overline{OE}_B$	Data B I/O	Port B Operation
0	0	0	I	Data B is written on CLK_B ↑. This write cycle immediately following output low impedance cycle is prohibited
0	0	1	I	Data B is written on CLK_B ↑.
0	1	X	I	Data B is ignored
1	0	0	O	Data is read(1) from RAM array to output register on CLK_B ↑, Data B is low impedance
1	0	1	O	Data is read(1) from RAM array to output register on CLK_B ↑, Data B is high impedance
1	1	0	O	Output register does not change(2), Data B is low impedance
1	1	1	O	Output register does not change(2), Data B is high impedance

2704 tbl 13

NOTES:
1. When $A_2A_1A_0$ = 000 or 1XX, the next A→B FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data is read from the Port B output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port B output register does not change and the A→B read pointer does not advance.

Table 5. Port B Operation Control Signals

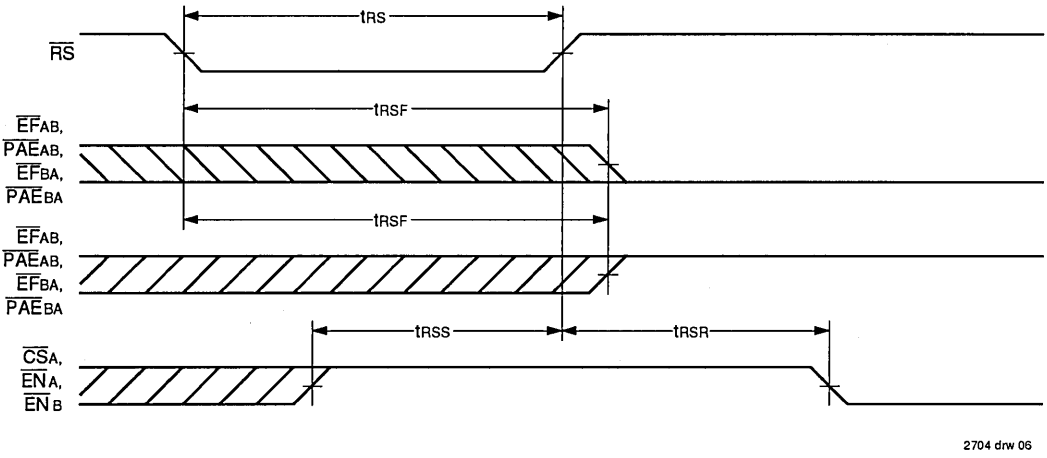


Figure 3. Reset Timing

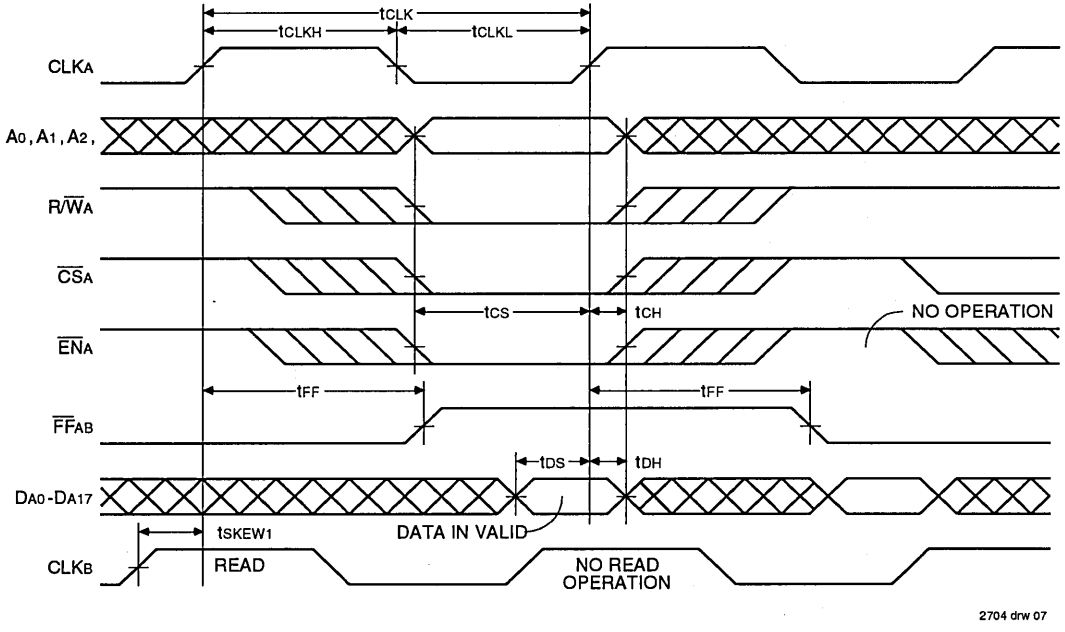


Figure 4. Port A (A→B) Write Timing

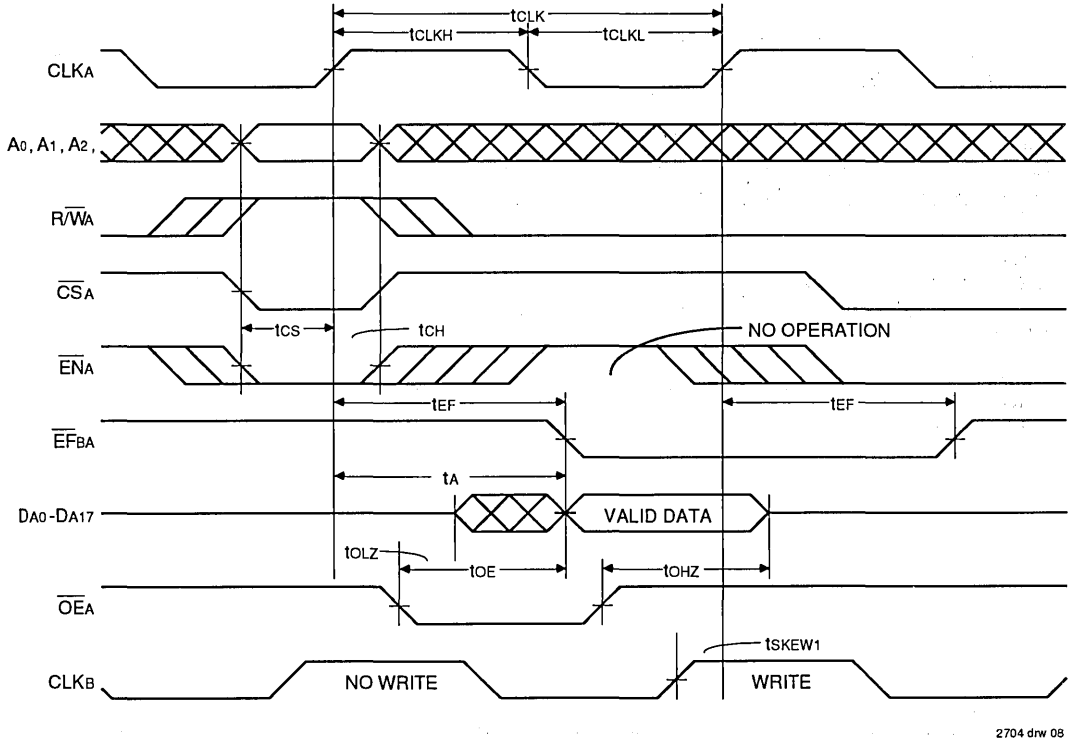


Figure 5. Port A (B→A) Read Timing

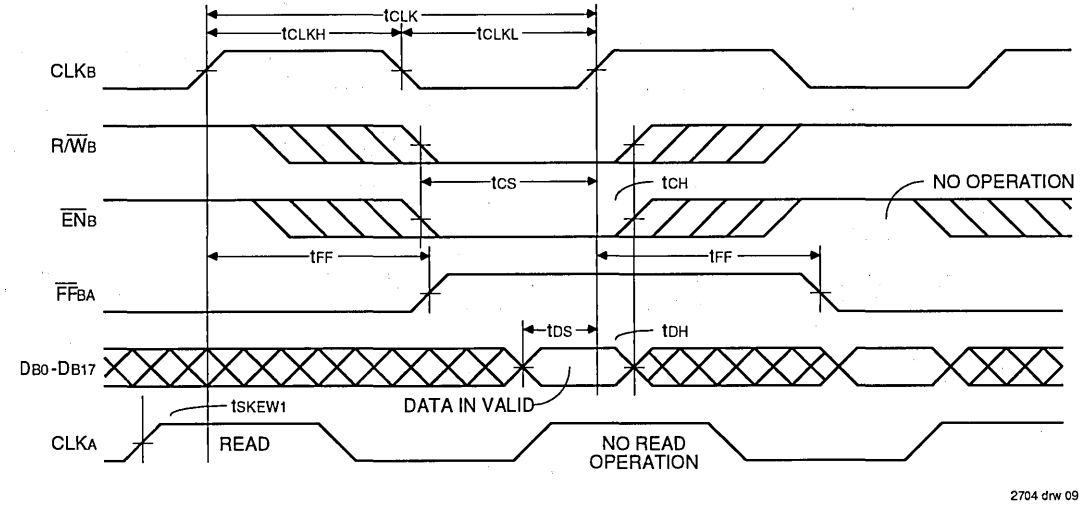


Figure 6. Port B (B→A) Write Timing

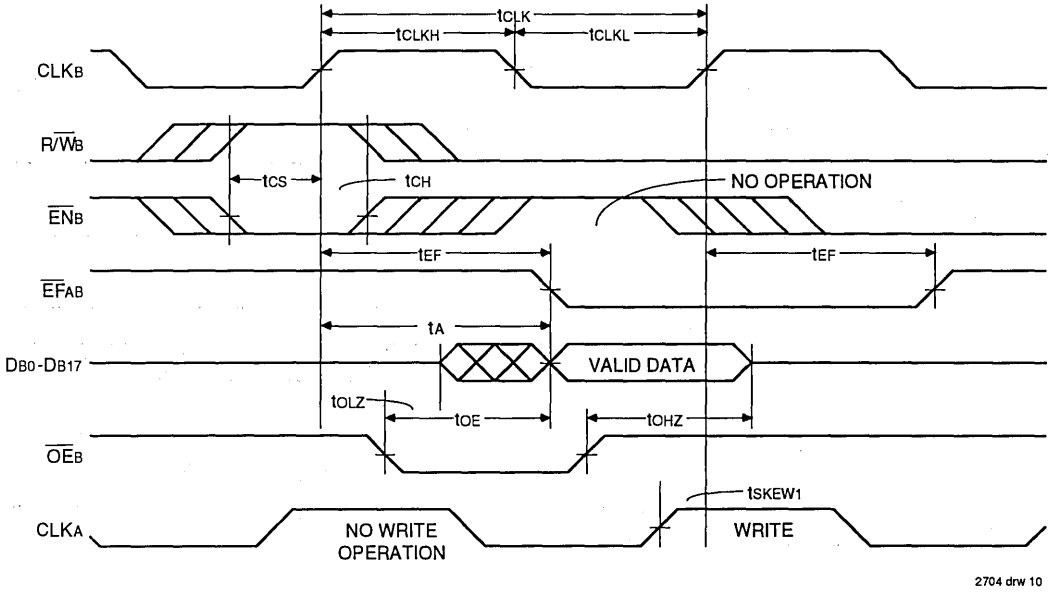


Figure 7. Port B (A→B) Read Timing

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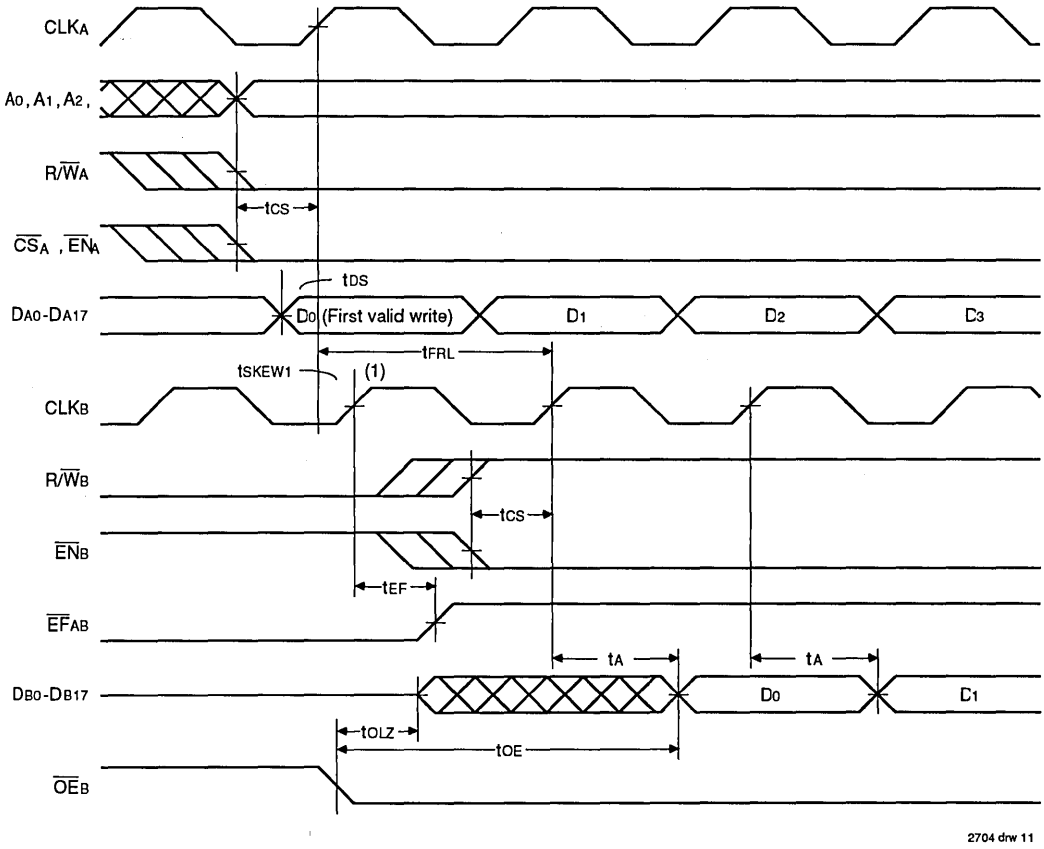
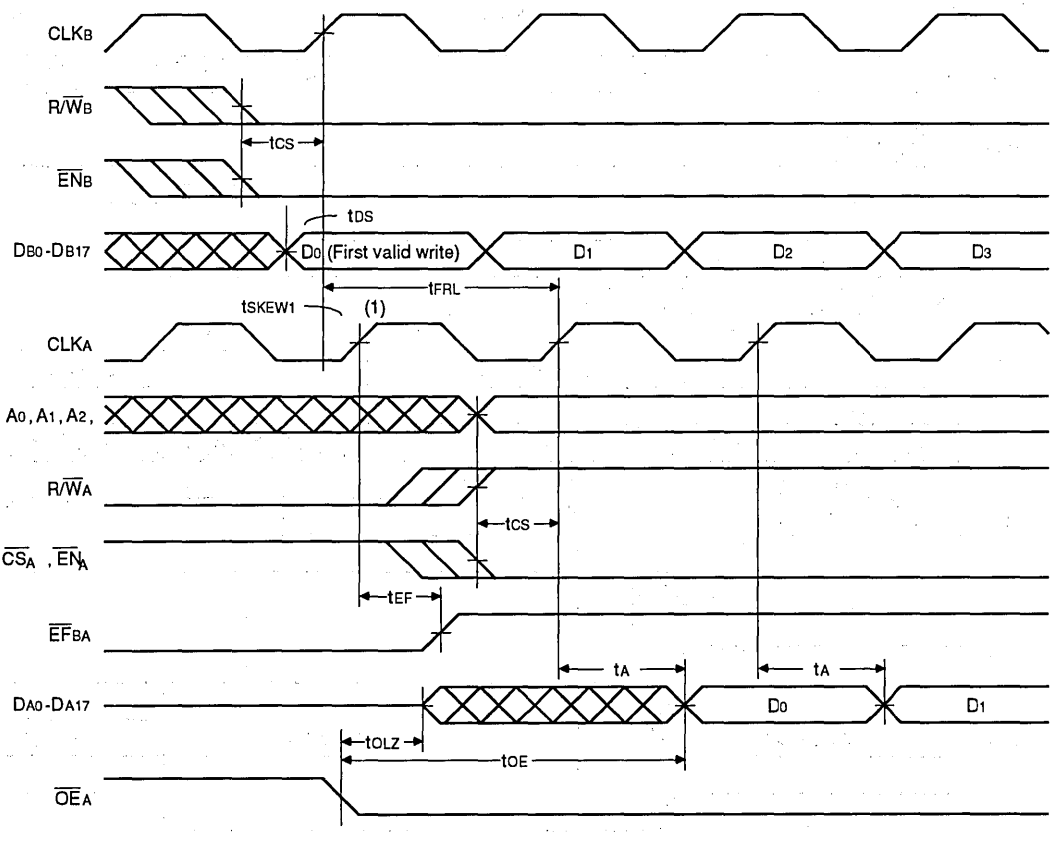


NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = Low).

Figure 8. A→B First Data Word Latency after Reset for Simultaneous Read and Write



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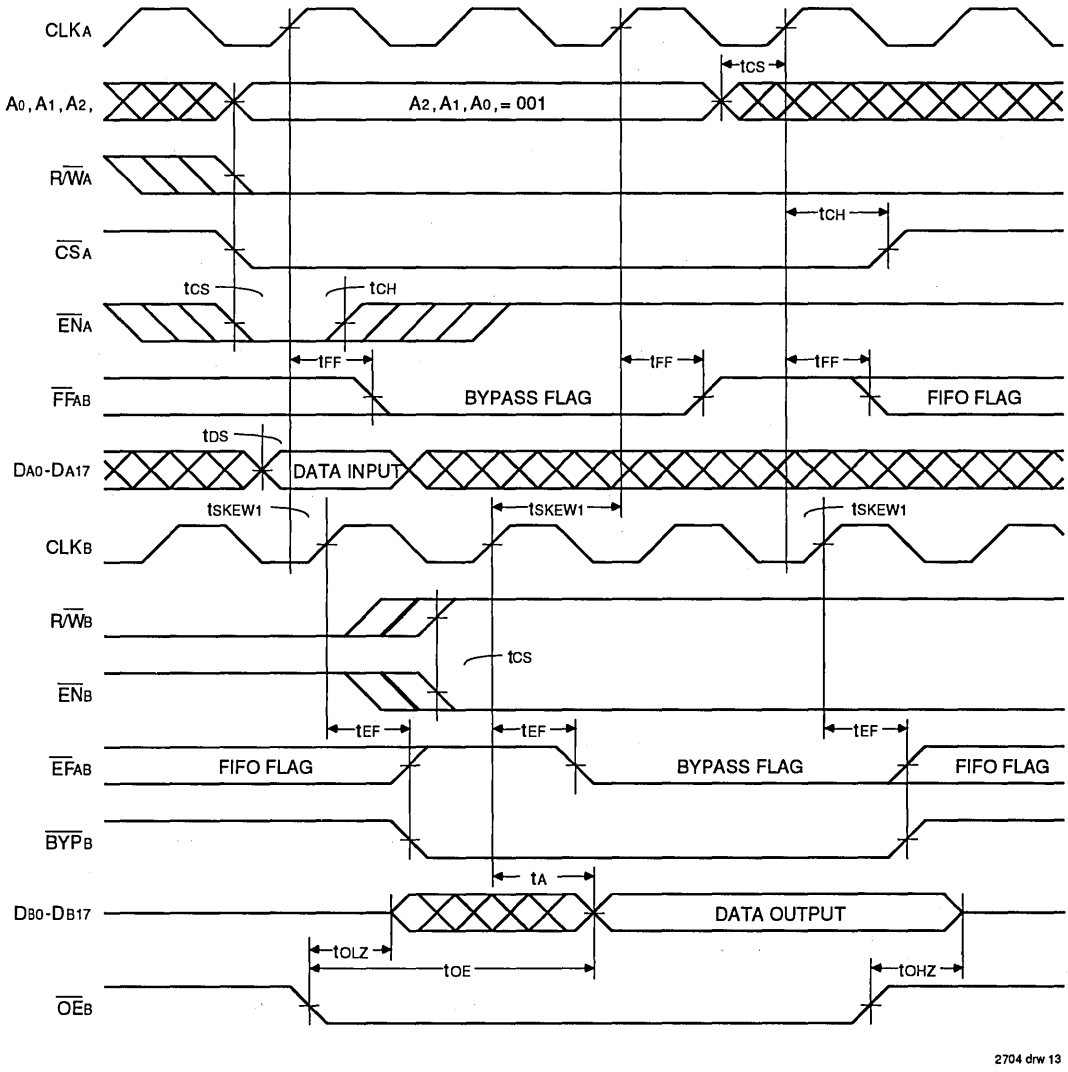
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = Low).

Figure 9. B→A First Data Word Latency after Reset for Simultaneous Read and Write

5



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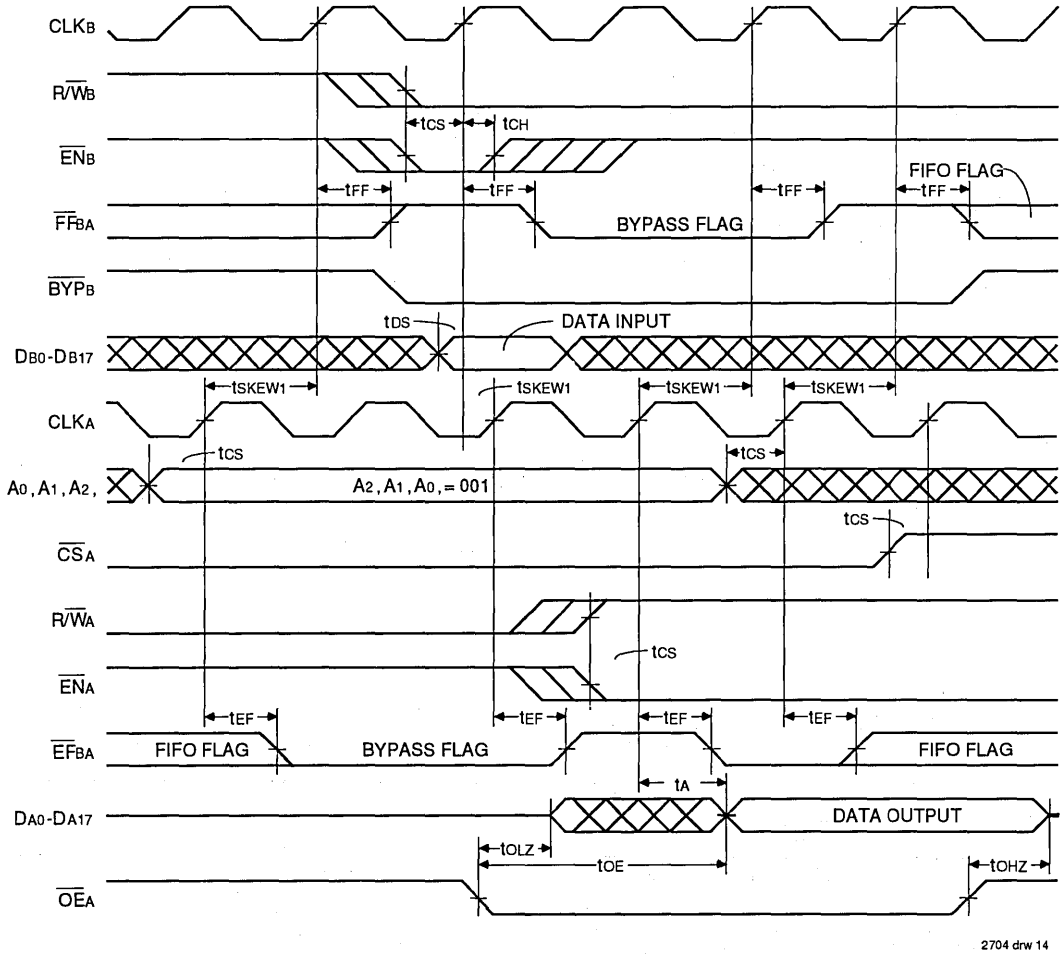
NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA low-to-high transition.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from low-to-high; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

Figure 10. A→B Bypass Timing



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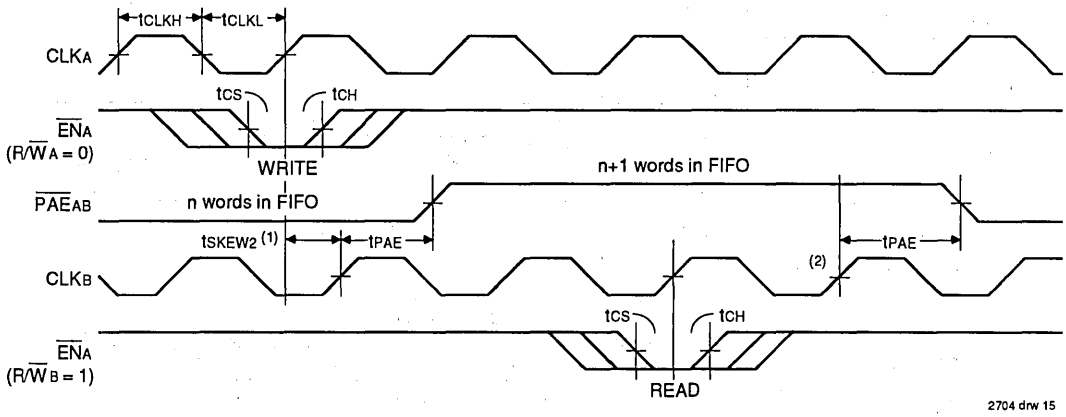
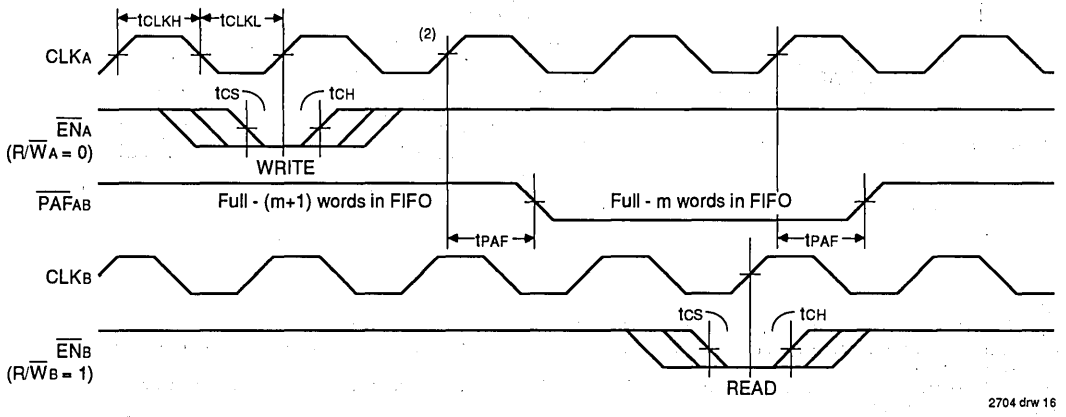
NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA going low-to-high.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from low-to-high; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

Figure 11. B→A Bypass Timing



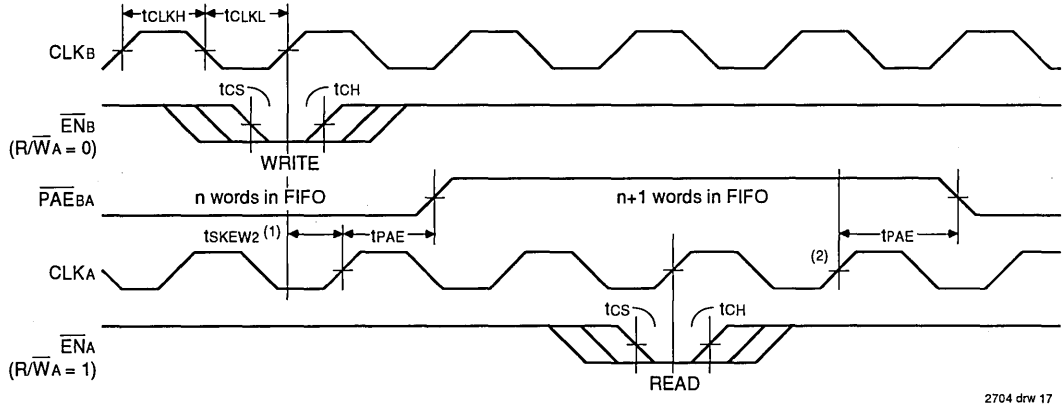
NOTES:
1. t_{SKEW2} the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{PAE}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKA and the rising edge of CLKB is less than t_{SKEW}, then $\overline{PAE}_{AB}$ may not go HIGH until the next CLKB rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n + 1) words in the FIFO when $\overline{PAE}$ goes low.

Figure 12. A→B Programmable Almost-Empty Flag Timing



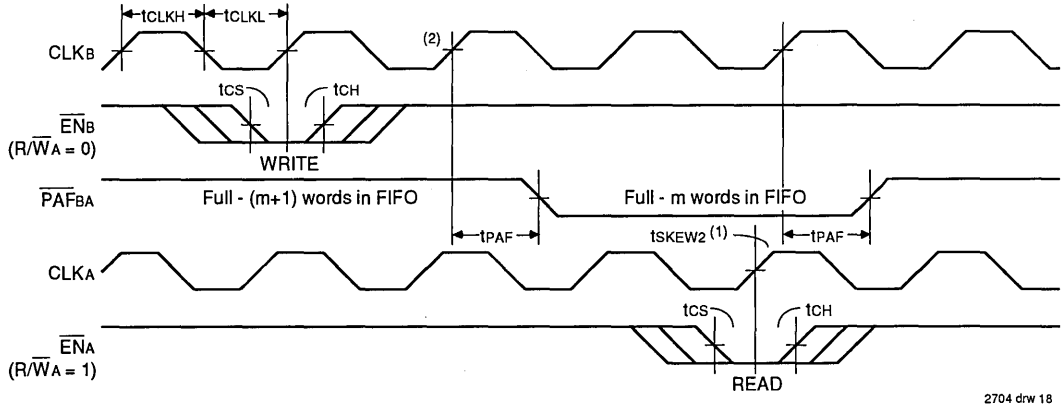
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAF}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than t_{SKEW2}, then $\overline{PAF}_{AB}$ may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes low.

Figure 13. A→B Programmable Almost-Full Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAE}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than t_{SKEW2}, then $\overline{PAE}_{BA}$ may not go HIGH until the next CLKA rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n - 1) words in the FIFO when $\overline{PAE}$ goes low.

Figure 14. B→A Programmable Almost-Empty Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAF}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than t_{SKEW2}, then $\overline{PAF}_{BA}$ may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes low.

Figure 15. B→A Programmable Almost-Full Flag Timing

Integrated Device Technology, Inc.

PARALLEL ASYNCHRONOUS SINGLE-BANK BIDIRECTIONAL FIFO 512 x 9-BIT, 1024 x 9-BIT, 2048 x 9-BIT

PRELIMINARY
IDT7271
IDT7272
IDT7273

FEATURES:

- Bidirectional data transfer
- 512 x 9 organization (IDT7271)
- 1024 x 9 organization (IDT7272)
- 2048 x 9 organization (IDT7273)
- Fast 25ns access time
- Single bank FIFO memory with data flow in one direction at a time
- Direction pin controls data flow from Port A-to-B, or Port B-to-A
- Full and Empty flags
- Fixed Almost-Full and Almost-Empty partial flags
- Bypass and Diagnostic modes
- 32-pin DIP, PLCC, LCC and SOJ
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7271/7272/7273 are very high speed, low power FIFO memories that enhance processor-to-processor and processor-to-peripheral communications. The 727x family use a single bank of memory; therefore, allowing one port to be accessed at any time. A direction pin (DIR) is provided to determine data flow direction. When the DIR pin is Low , data flows from port A-to-B. Data flows in the opposite direction when the DIR pin is High .

A device reset can be initiated at any time by bringing the Reset ($\overline{RS}$) pin LOW while holding the Read ($\overline{RD}$), Bypass ($\overline{BYP}$), Diagnostic ($\overline{DIAG}$) and Write ($\overline{WR}$) pins High .

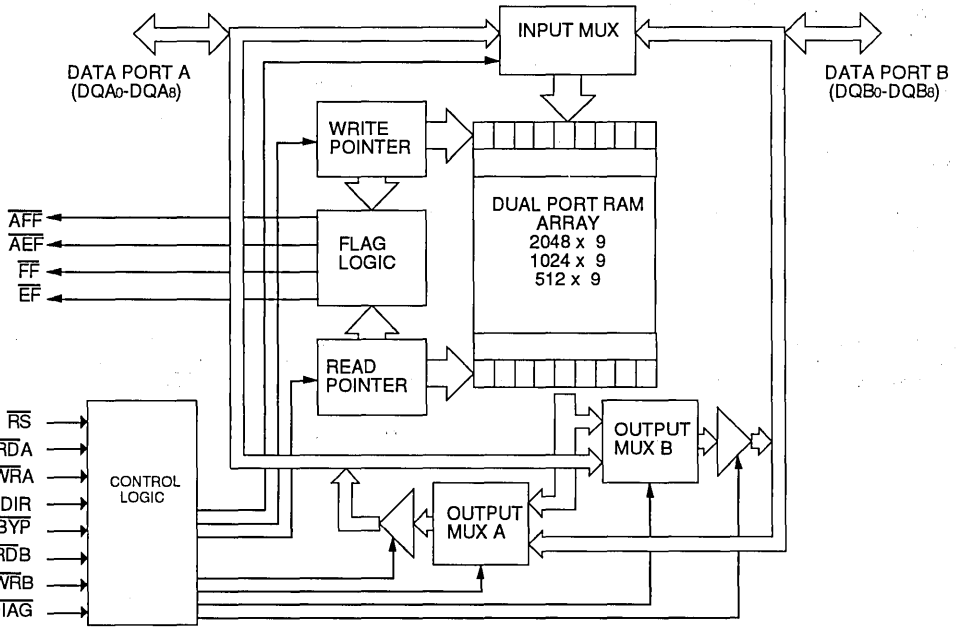
There are four separate flags on these BiFIFOs. The two end-point flags are Empty ($\overline{EF}$) and Full ($\overline{FF}$); and the two partial flags with fixed offset size of 07H (eight bytes from the boundaries) are Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$). All flags are active low.

Bypass control allows data to be directly transferred from port A to port B, or vice versa, without going through the memory array. The bypass mode can be set by asserting the $\overline{BYP}$ pin (active Low).

The diagnostic mode allows written data to be read through the same port. This provides systems memory self-test upon power up or after a system failure.

The IDT7271/2/3 are fabricated using IDT's high speed submicron CEMOS™ technology. Military grade products are manufactured in compliant with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAMS



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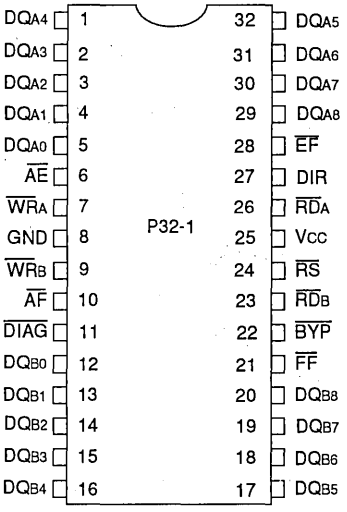
2529 drw 01

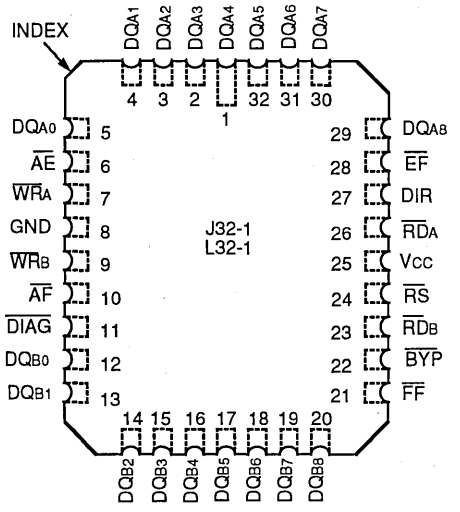
COMMERCIAL TEMPERATURE RANGE **APRIL 1992**

PIN CONFIGURATIONS



DIP
TOP VIEW

2529 drw 02



PLCC/LCC
TOP VIEW

2529 drw 03

PIN DESCRIPTION

Symbol	Name	I/O	Description
DQA0-DQA8	Data A	I/O	9-bit data pins for port A. The DIR pin controls direction of these pins (input or output)
DQB0-DQB8	Data B	I/O	9-bit data pins for port B. The DIR pin controls state of these pins (inputs or outputs)
$\overline{RD}_A$	Read A	I	This input pin controls port A read operation. In bypass mode this pin controls the A port output enables. Active Low input.
$\overline{RD}_B$	Read B	I	This input pin controls port B read operation. Active Low input.
$\overline{WR}_A$	Write A	I	This input pin controls port A write operation. In bypass mode this pin controls the port B output enables. Active Low input.
$\overline{WR}_B$	Write B	I	This input pin controls port B write operation. Active Low input.
DIR	Direction	I	This input pin determines data flow direction. When it is Low, data flows from port A to port B. When it is High, data flows in the opposite direction.
$\overline{DIAG}$	Diagnostic	I	Once the data is loaded, the $\overline{DIAG}$ pin can be asserted followed by the DIR pin's state change, the written data can then be read through the same port.
$\overline{BYP}$	Bypass	I	This input pin sets the FIFO in the bypass mode, in which the FIFO acts as a transceiver. Active Low input.
$\overline{RS}$	Reset	I	This pin resets all functions. Active Low input.
$\overline{AE}$	Partial Flag	O	This output pin is asserted when the FIFO is almost empty. Active Low output.
$\overline{AF}$	Partial Flag	O	This output pin is asserted when the FIFO is almost full. Active Low output.
$\overline{FF}$	Full Flag	O	This output is asserted when the FIFO is completely full. Active Low output.
$\overline{EF}$	Empty Flag	O	This output is asserted when the FIFO is completely empty. Active Low output.
VCC	Power		One +5V power pins.
GND	Ground		One ground pin at 0V.

2529 tbl 01

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2529 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Votage Commercial	2.0	—	—	V
V_{IH}	Input High Votage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Com'l. and Mil.	—	—	0.8	V

NOTE: 2529 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C + 125°C)

Symbol	Parameter	IDT7271L IDT7272L IDT7273L Commercial t_A = 25, 35, 50ns Min.	Typ.	Max.	IDT7271L IDT7272L IDT7273L Military t_A = 30, 35, 50ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	µA
I_{OL}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Average VCC Power Supply Current	—	75	120	—	100	150	mA
I_{CC2}(3)	Average Standby Current ($\overline{RA}$ = $\overline{WA}$ = $\overline{RB}$ = $\overline{WB}$ = $\overline{RS}$ = V_{IH})	—	8	15	—	12	25	mA
I_{CC3}(3)	Power Down Current (All Inputs = Vcc - 0.2V)	—	—	8	—	—	12	mA

NOTES: 2529 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

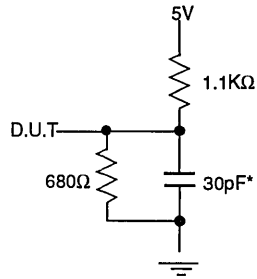
2529 tbl 05

CAPACITANCE(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}(3)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(2,3)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2529 tbl 06

1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.



2529 drw 04

Figure 1. Output Load

*Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C + 125°C)

		Commercial		Military		Commercial and Military				
		IDT7271L25 IDT7272L25 IDT7273L25		IDT7271L30 IDT7272L30 IDT7273L30		IDT7271L35 IDT7272L35 IDT7273L35		IDT7271L50 IDT7272L50 IDT7273L50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Reset Timing										
tRSC	Reset Cycle Time	35	—	40	—	45	—	65	—	ns
tRS	Reset Pulse Width	25	—	30	—	35	—	50	—	ns
tRSS	Reset Set-up Time	25	—	30	—	35	—	50	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
tRFV	Reset to Flag Valid	—	25	—	30	—	35	—	50	ns
Read/Write Timing										
tA	Read Access Time	—	25	—	30	—	35	—	50	ns
tRC	Read Cycle Time	35	—	40	—	45	—	65	—	ns
tRPW	Read Pulse Width	25	—	30	—	35	—	50	—	ns
tRR	Read Recovery Time	10	—	10	—	10	—	15	—	ns
tDV	Data valid from read pulse HIGH	3	—	3	—	3	—	3	—	ns
tRHZ	Read HIGH to data bus at High Z	—	18	—	20	—	20	—	30	ns
tRLZ	Read LOW to data bus at Low Z	3	—	3	—	3	—	3	—	ns
tWC	Write Cycle Time	35	—	40	—	45	—	65	—	ns
tWPW	Write Pulse Width	25	—	30	—	35	—	50	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	15	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	1	—	5	—	ns
Direction Change, Diagnostic and Bypass Timing										
tDFWL	DIR Change to Write Low	25	—	30	—	35	—	50	—	ns
tDFV	DIR Change to Valid Flags	—	20	—	25	—	30	—	45	ns
tDRL	DIR Change to Read Low	20	—	25	—	30	—	35	—	ns
tDHDGL	DIR Change to DIAG High	0	—	0	—	1	—	5	—	ns
tDRSU	DIR Setup	10	—	15	—	20	—	30	—	ns
tDGLDC	DIAG Low to DIR Change	10	—	15	—	20	—	30	—	ns
tDGHWL	DIAG High to Write Low	25	—	30	—	35	—	50	—	ns
tDGWR	DIAG Low to Write Low (either port)	10	—	15	—	20	—	30	—	ns
tBYSU	BYP Set-up Time	10	—	15	—	20	—	30	—	ns
tBYA	Bypass Access Time	—	25	—	30	—	35	—	50	ns
tBYD	Bypass Delay Time	—	25	—	30	—	35	—	50	ns
Flag Timing										
tFEFV	Full or Empty Flag Valid	—	20	—	25	—	30	—	40	ns
tAFAEV	Almost-Full or Empty Flag Valid	—	35	—	40	—	45	—	65	ns

2529 tbl 07

5

FUNCTIONAL DESCRIPTION

IDT's Single-Bank BiFIFO family is versatile for both multiprocessor and peripheral applications. The 727x family is a low-cost solution for bidirectional systems where data flow in only one direction at a time is needed. The Single-Bank BiFIFO implies that there is only one bank of memory shared by two ports, with a direction pin provided for altering data flow direction.

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the writing side; $\overline{EF}$ is monitored on the reading side). In general a write cycle cannot be allowed to begin if $\overline{FF}$ is asserted and a read cycle cannot be allowed to begin if $\overline{EF}$ is asserted. For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Reset

A reset is initiated by bringing the Reset ($\overline{RS}$) pin Low, while holding the Read ($\overline{RD}$), Bypass ($\overline{BYP}$), Diagnostic ($\overline{DIAG}$) and Write ($\overline{WR}$) pins High. After a device reset, all internal pointers are cleared and flags are adjusted accordingly. For proper device operation, all control inputs pins must be stable before the reset signal is deasserted. A recovery time is required before loading the device or altering operation mode (Bypass, Diagnostic, etc).

Flags

There are four separate flags on the 7271/2/3 BiFIFO, two partial flags, a full flag and an empty flag. All are active low. The two partial flags are the Almost Full ($\overline{AF}$) and the Almost Empty ($\overline{AE}$) flags, each with a fixed offset size of 07H (eight bytes from the empty or full conditions). These can be used as an early warning signal. The two other flags are fixed at Empty $\overline{EF}$ and Full $\overline{FF}$. These are asserted during the last read or write operation respectively. These are used to prevent device overflow or underflow.

Data Flow Direction

Data can only flow from one port to another at any given time. The direction of data flow is determined by the state of the DIR pin. When the DIR pin is Low, data can be written only into port A. Data can be read only out of port B. Data flows in the opposite direction when the DIR pin is High . Data flow function can be changed at any time. By altering the DIR state, the two read and write pointers are reset and data flows in the opposite direction. The falling edge of the first write cycle is used to determine the end of the reset cycle. Flags outputs reflect the pointer states and thus change on the change of the DIR signal.

Bypass Mode

Asserting the $\overline{BYP}$ pin (active Low) places the device in the bypass mode. The FIFO functions as a simple transciever in this mode. Data can be directly written into or read out of a device which is connected to the B port by a device connected to the A port.

While in this mode, both $\overline{RDB}$ and $\overline{WRB}$ must be held High. By asserting the $\overline{WRA}$, data on the A port will be driven out the B port. By asserting the $\overline{RDA}$, data on the B port will be driven out the A port. The $\overline{WRA}$ signal is used to enable the B port's bus drivers. The $\overline{RDA}$ signal is used enable the A ports. $\overline{WRA}$ and $\overline{RDA}$ must not be low at the same time.

Entering and exiting the bypass mode does not affect the internal pointers. The state of the DIR pin is ignored in the bypass mode. If DIR changes state in Bypass mode, the pointers will not reset until leaving the Bypass mode. If DIR changes state momentarily in Bypass mode there is no effect. Bypass mode does not alter flag states.

Diagnostic Mode

Many systems require memory testing upon power up or after a system failure. The 727x family has a built-in diagnostic mode for self test. When in the diagnostic mode, written data can be read through the same port by altering the state of the DIR pin. In this case, the pointers are not reset (with direction change) allowing the retrieval of written data. The read and write pointers are reset upon exiting the diagnostic mode. The leading edge of the first write cycle experienced after leaving diagnostic mode is used to terminate the reset cycle. Flag operations are normal in diagnostic mode, reflecting only the relative states of the read and write pointers. Thus they change on the rising edge of the $\overline{DIAG}$ signal when the pointers are reset upon leaving diagnostic mode.

The state of the DIR pin is latched when $\overline{DIAG}$ is brought low, determining which port of the FIFO is used for diagnostics. If DIR is Low at the High-to-Low transition of $\overline{DIAG}$, A port is used for diagnostics. If High, B port is used. Figure 12 shows diagnostics for B port, but the timing also applies to A port diagnostics if DIR is inverted.

Data can be loaded into the memory array before or after setting the part into diagnostic mode. The $\overline{DIAG}$ pin must be asserted before by the DIR pin's first state change. Once in the diagnostic mode, data that has been written can be retrieved through the same port by reading from that port. Reading and writing can continue indefinately until the diagnostic mode has been exited.

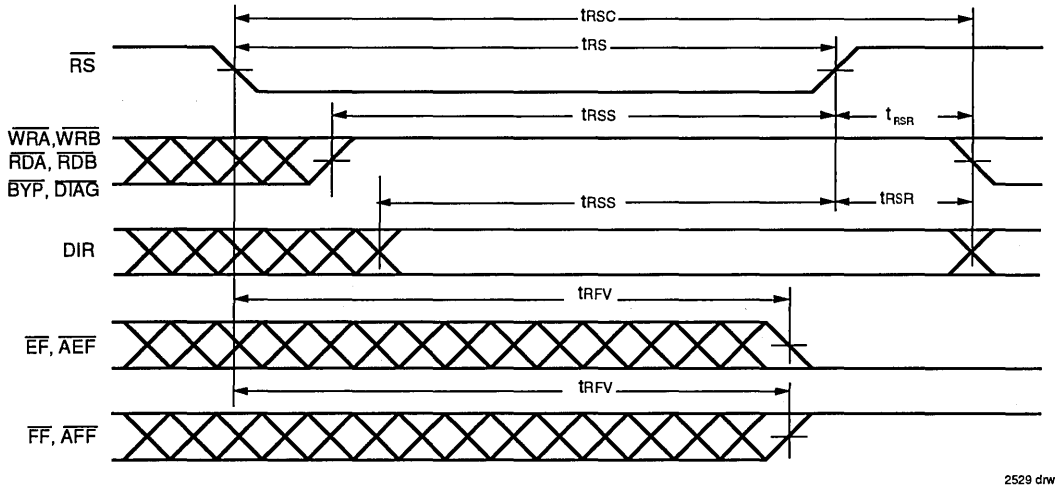


Figure 2. Reset Cycle Timing

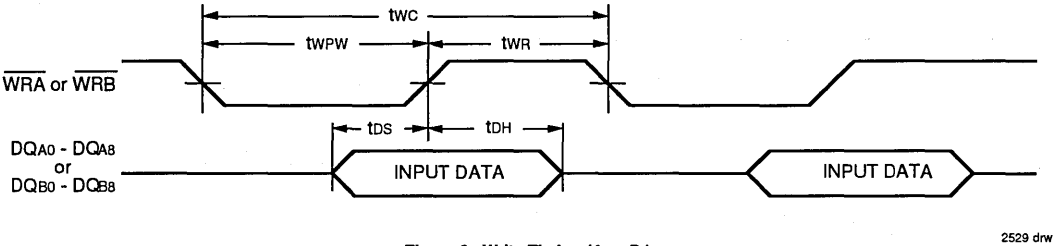


Figure 3. Write Timing (A or B)

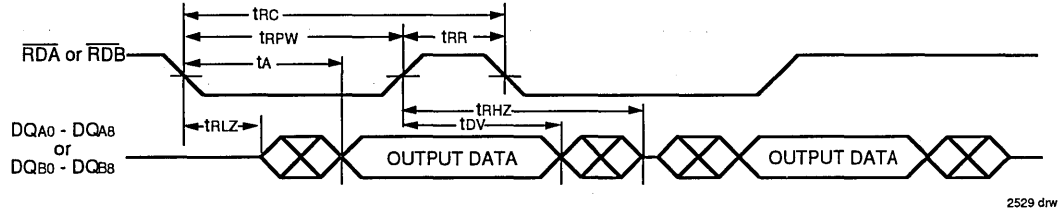


Figure 4. Read Timing (A or B)

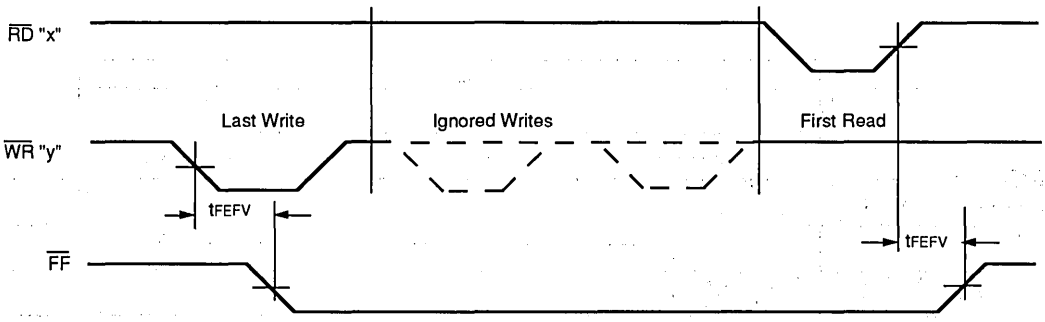


Figure 5. Full Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 08

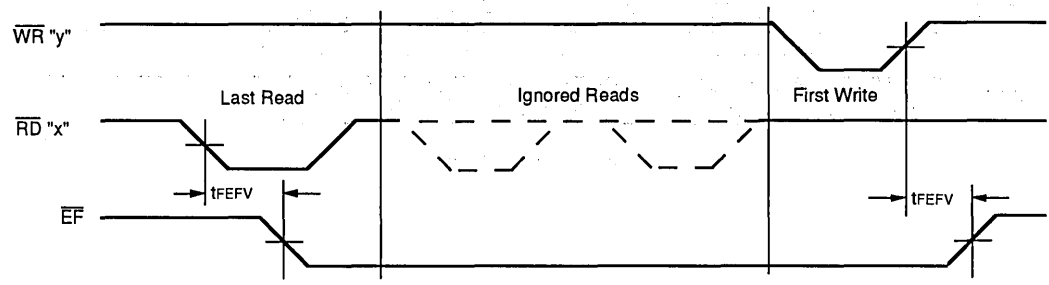


Figure 6. Empty Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 09

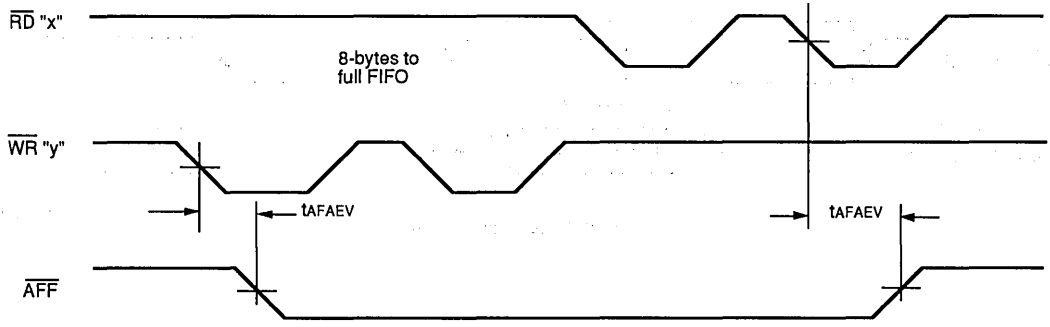


Figure 7. Almost Full Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 10

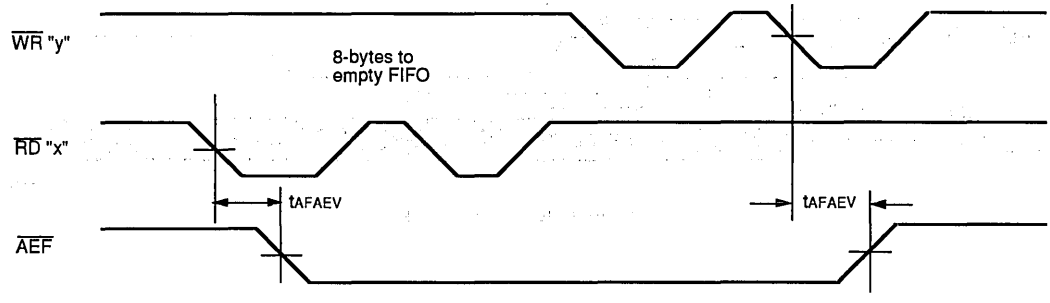


Figure 8. Almost Empty Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 11

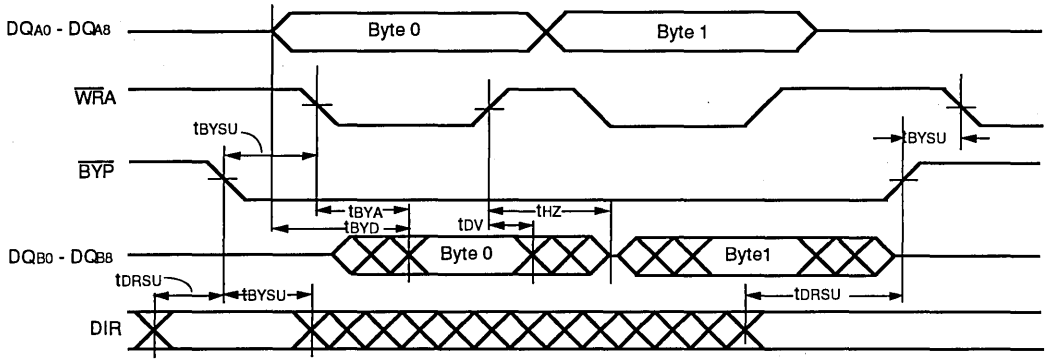
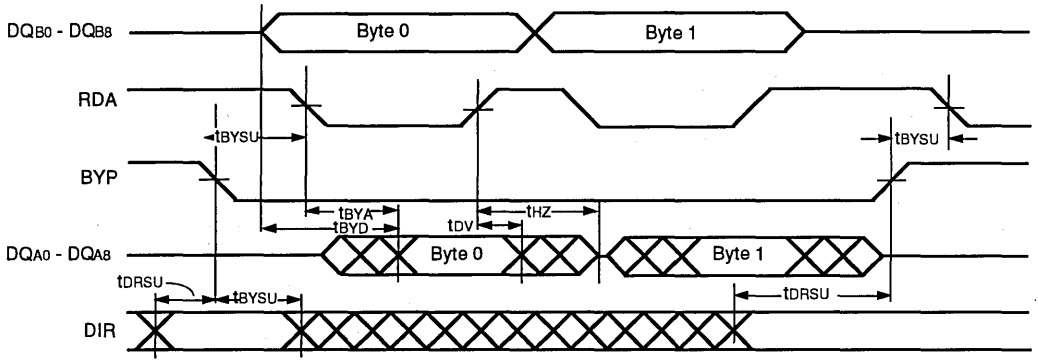


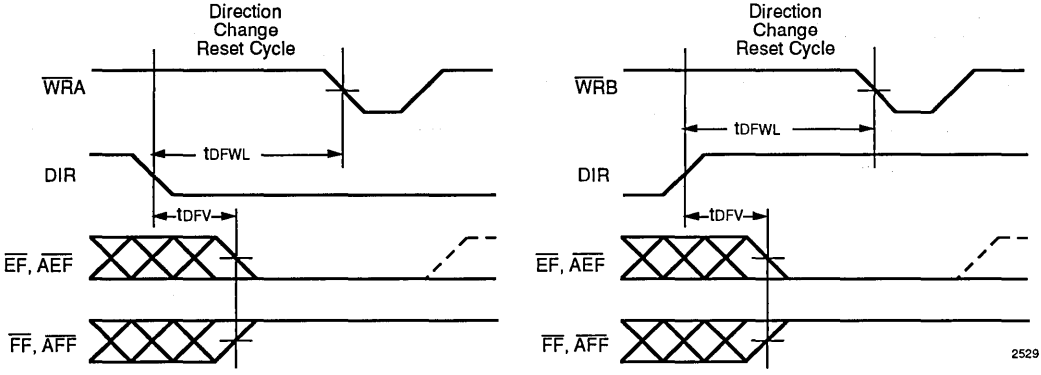
Figure 9. Bypass mode: Data flow from A to B

2529 drw 12



2529 drw 13

Figure 10. Bypass mode: Data Flow from B to A



2529 drw 14

Figure 11. Data Flow Direction Change and Reset cycle Timing

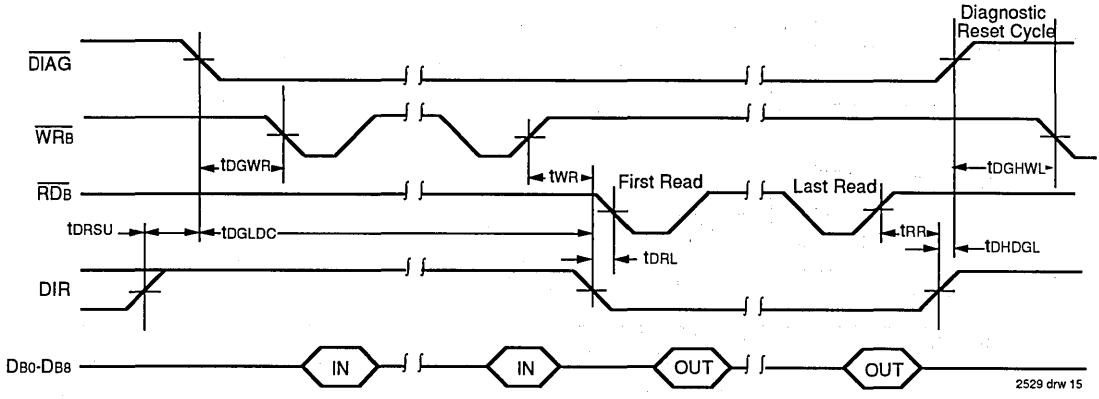


Figure 12. Diagnostic Mode Read/Write Timing and Diagnostic Reset Cycle.

TABLE I — OPERATING MODES

$\overline{RS}$	$\overline{BYP}$	$\overline{DIAG}$	DIR	$\overline{RDA}$	$\overline{WRA}$	$\overline{RDB}$	$\overline{WRB}$	Operating Mode
⎍	1	1	x	1	1	1	1	Device reset
1	1	0	0	1	⎍	1	1	Diagnostic mode: data is being loaded through A port
1	1	0	1	⎍	1	1	1	Diagnostic mode: data is being retrieved through A port
1	1	0	1	1	1	1	⎍	Diagnostic mode: data is being loaded through B port
1	1	0	0	1	1	⎍	1	Diagnostic mode: data is being retrieved through B port
1	0	1	X	1	0	1	1	Bypass mode: Data flows from A port to B port
1	0	1	X	0	1	1	1	Bypass mode: Data flows from B port to A port
1	1	1	0	1	⎍	⎍	1	FIFO Mode: Asynchronous read/write. Data flows from port A to port B.
1	1	1	1	⎍	1	1	⎍	FIFO Mode: Asynchronous read/write. Data flows from port B to port A

2529 tbl 07

Unspecified states are not allowed

MULTI-PORT RAMS

Integrated Device Technology has emerged as the leading multi-port RAM supplier by combining CEMOS/BiCEMOS technology with innovative circuit design. With system performance advantages as a goal, we have brought system design expertise together with circuit and technology expertise in defining dual-port and four-port RAM products. Our dual-port memories are now industry standards. The synergistic relationship between advanced process technology, system expertise and unique design capability add value beyond that normally achieved. As an example, our dual-port memories provide arbitration along with a completely tested solution to the metastability problem. Various arbitration techniques are available to the designer to prevent contention and system wait states. On-chip hardware arbitration, "semaphore" token passing or software arbitration allow the most efficient memory to be selected for each application. At IDT, innovation counts only when it provides system advantages to the user.

Both commercial and military versions of all IDT memories are available. Our military devices are manufactured and processed strictly in conformance with all the administrative processing and performance requirements of MIL-STD-883. Because we anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As the leading supplier of military specialty RAMs, IDT provides performance and quality levels second to none.

Our commercial dual-port and four-port memories, in fact, share most processing steps with military devices.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES

- High-speed access
  - —Military: 25/30/35/45/55/70/90/100/120ns (max.)
  - —Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - —IDT7130/IDT7140SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT7130/IDT7140LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION

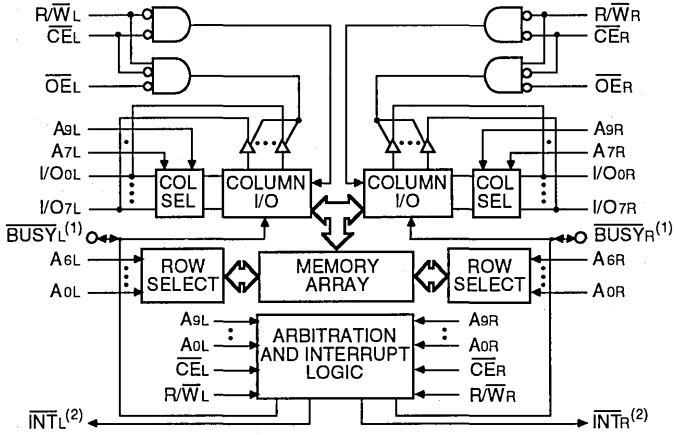
The IDT7130/IDT7140 are high speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-Lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2689 drw 01

NOTES:
1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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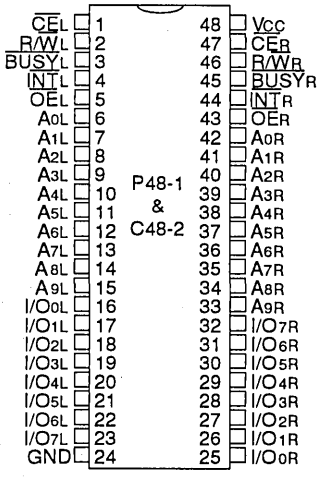
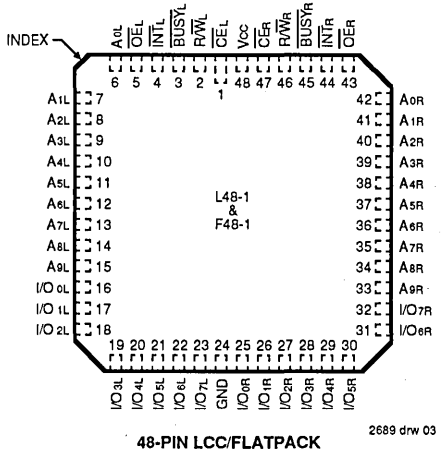
PIN CONFIGURATIONS



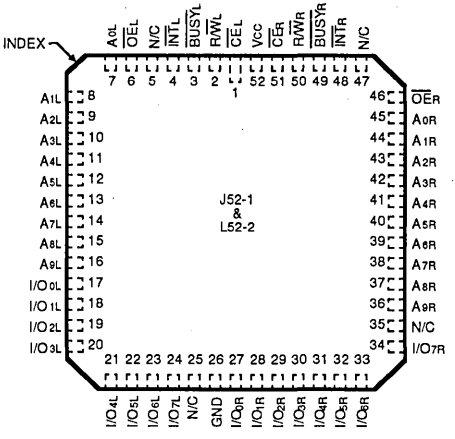
2689 drw 02

DIP
TOP VIEW



2689 drw 03

48-PIN LCC/FLATPACK
TOP VIEW



2689 drw 04

52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2689 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2689 tbl 02

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7130SA IDT7140SA Min.	IDT7130SA IDT7140SA Max.	IDT7130LA IDT7140LA Max.	IDT7130LA IDT7140LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[9]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2689 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1,8] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7130 x 20[2,6] 7140 x 20[2,6] Typ.	Max.	7130 x 25[6] 7140 x 25[6] Typ.	Max.	7130 x 30[6] 7140 x 30[6] Typ.	Max.	7130 x 35[7] 7140 x 35[7] Typ.	Max.	7130 x 45 7140 x 45 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	125	300	125	295	125	290	75	230	mA
				LA	—	—	125	240	125	235	125	230	75	185	
			Com'l.	SA	125	265	125	260	125	255	75	195	75	190	
				LA	125	215	125	210	125	205	75	155	75	145	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	—	—	30	80	30	80	30	80	25	65	mA
				LA	—	—	30	60	30	60	30	60	25	55	
			Com'l.	SA	30	65	30	65	30	65	25	65	25	65	
				LA	30	45	30	45	30	45	25	45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	80	195	80	190	80	185	40	135	mA
				LA	—	—	80	160	80	155	80	150	40	110	
			Com'l.	SA	80	180	80	175	80	170	40	130	40	120	
				LA	80	145	80	140	80	135	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				LA	0.2	5	0.2	5	0.2	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	70	185	70	180	70	175	40	125	mA
				LA	—	—	70	150	70	145	70	140	35	95	
			Com'l.	SA	70	175	70	170	70	165	40	115	40	105	
				LA	70	140	70	135	70	130	35	90	35	80	

2689 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages, see 7030/40 data sheet.
7. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.
8. Vcc=5V, TA=+25°C for Typ.
9. At Vcc≤2.0V input leakages are undefined.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1,6] (Continued) (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	Version		7130 x 55 7140 x 55 Typ.	7130 x 55 7140 x 55 Max.	7130 x 70 7140 x 70 Typ.	7130 x 70 7140 x 70 Max.	7130 x 90 7140 x 90 Typ.	7130 x 90 7140 x 90 Max.	7130 x 100 7140 x 100 Typ.	7130 x 100 7140 x 100 Max.	7130 x 120[3] 7140 x 120[3] Typ.	7130 x 120[3] 7140 x 120[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
			Com'l.	SA	65	180	65	180	65	180	65	180	—	—	
				LA	65	140	65	135	65	130	65	130	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
			Com'l.	SA	25	65	25	60	25	55	25	55	—	—	
				LA	25	45	25	40	25	35	25	35	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
			Com'l.	SA	40	115	40	110	40	110	40	110	—	—	
				LA	40	85	40	85	40	75	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			Com'l.	SA	40	100	40	100	40	95	40	95	—	—	
				LA	35	75	35	75	35	70	35	70	—	—	

NOTES:

2689 tbl 06

1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.

DATA RETENTION CHARACTERISTICS (LA Version Only)

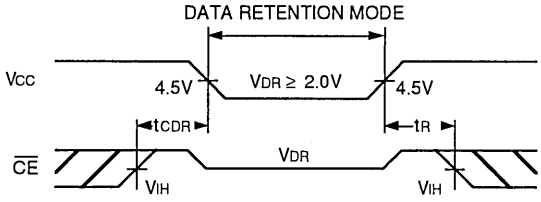
Symbol	Parameter	Test Conditions		IDT7130LA/IDT7140LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:

2689 tbl 07

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2689 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2689 tbl 08

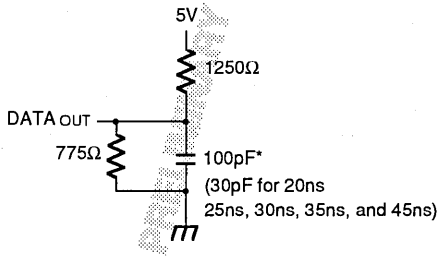


Figure 1. Output Load

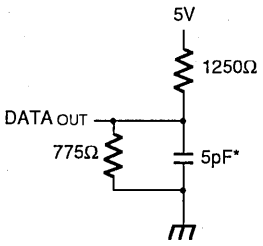


Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)

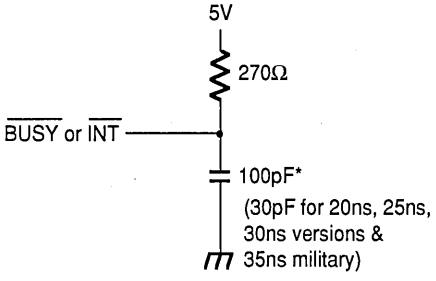


Figure 3. BUSY and INT Output Load

* Including scope and jig

2689 drw 06

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7130 x 20[2,6] 7140 x 20[2,6] Min.	Max.	7130 x 25[6] 7140 x 25[6] Min.	Max.	7130 x 30[6] 7140 x 30[6] Min.	Max.	7130 x 35[7] 7140 x 35[7] Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2689 tbl 09

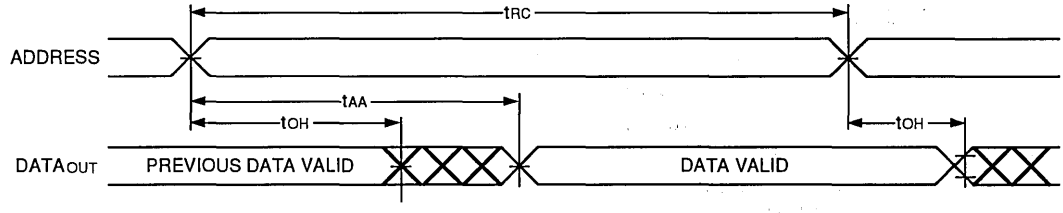
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5] (Continued)

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120[3] 7140 x 120[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
tAA	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
tACE	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
tAOE	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
tOH	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
tLZ	Output Low Z Time[1,4]	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2689 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages, see 7030/40 data sheet.
7. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

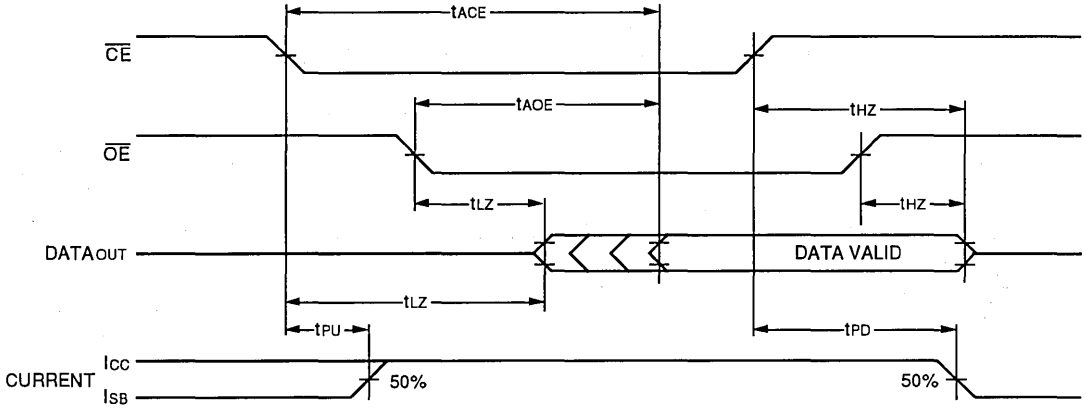
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]



2689 drw 07

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)



2689 drw 08

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

Symbol	Parameter	7130 x 20(2,8) 7140 x 20(2,8) Min.	Max.	7130 x 25(8) 7140 x 25(8) Min.	Max.	7130 x 30(8) 7140 x 30(8) Min.	Max.	7130 x 35(9) 7140 x 35(9) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time (1, 4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z (1, 4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write (1, 4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 11

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(3) 7140 x 120(3) Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	55	—	70	—	90	—	100	—	120	—	ns
tEW	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAW	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	40	—	50	—	55	—	55	—	65	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
tHZ	Output High Z Time (1, 4)	—	30	—	35	—	40	—	40	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z (1, 4)	—	30	—	35	—	40	—	40	—	50	ns
tOW	Output Active From End of Write (1, 4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages, see 7030/40 data sheet.
9. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

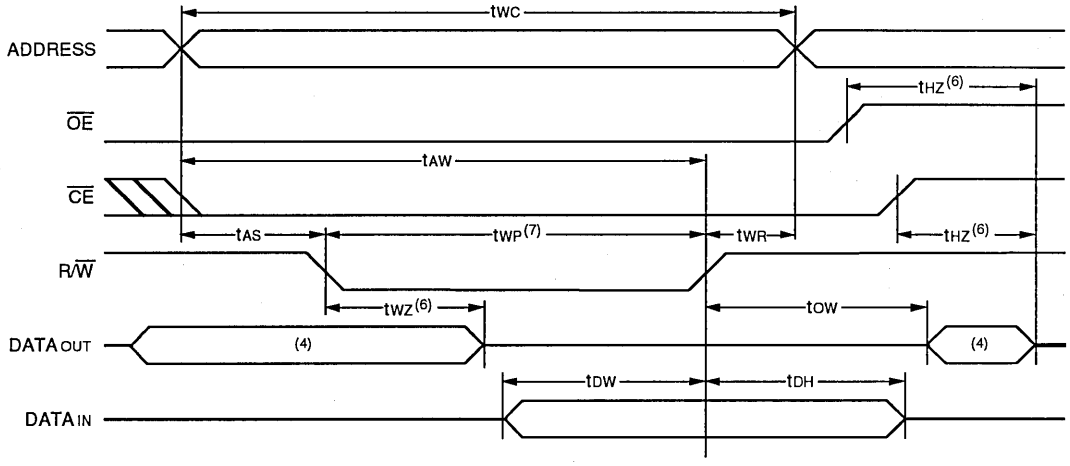
CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2689 tbl 13

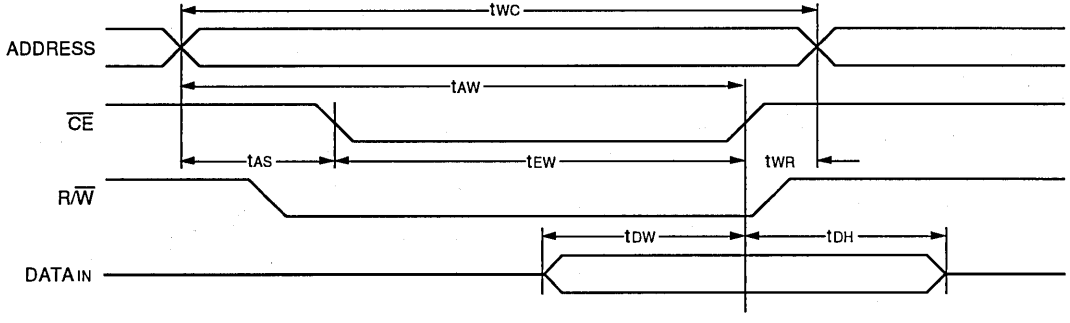
NOTE:
1. This parameter is determined by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2689 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2689 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7130 x 20[1,10] 7140 x 20[1,10] Min.	Max.	7130 x 25[10] 7140 x 25[10] Min.	Max.	7130 x 30[10] 7140 x 30[10] Min.	Max.	7130 x 35[11] 7140 x 35[11] Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	BUSY Disable Time to Address	—	20	—	20	—	25	—	30	—	35	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	20	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	35	—	35	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY[7]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	35	—	35	—	35	—	45	ns

2689 tbl 14

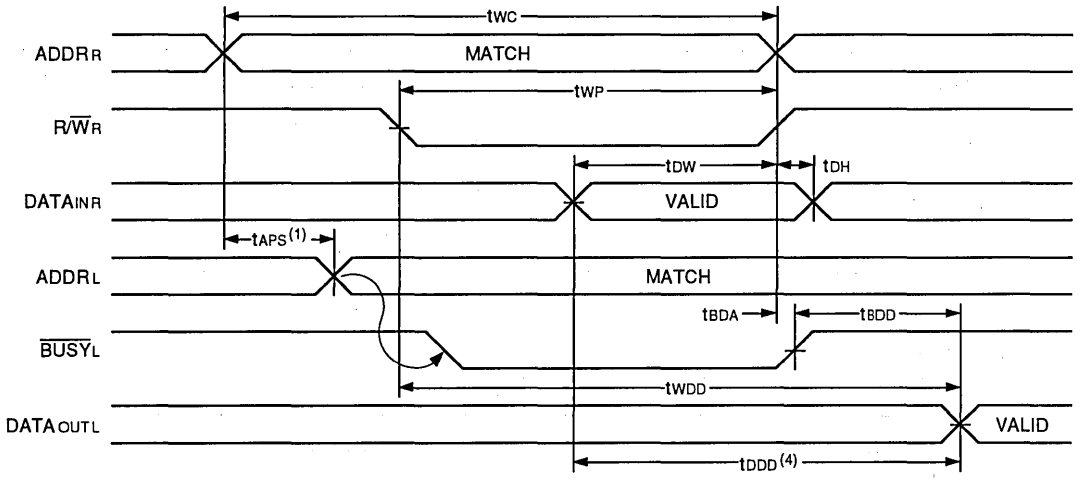
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120[2] 7140 x 120[2] Min.	Max.	Unit
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	BUSY Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	BUSY Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	BUSY Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay[3]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY[7]	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	55	—	70	—	90	—	100	—	120	ns

2689 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7130 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD-tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7140 Only)".
10. Not available in DIP packages, see 7030/40 data sheet.
11. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

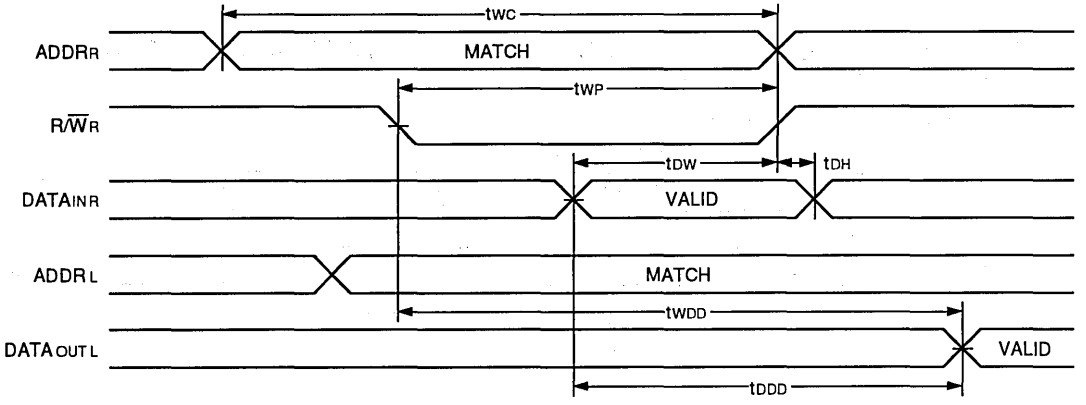
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7130 ONLY)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

2689 drw 11

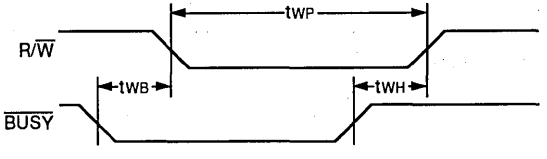
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7140 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

2689 drw 12

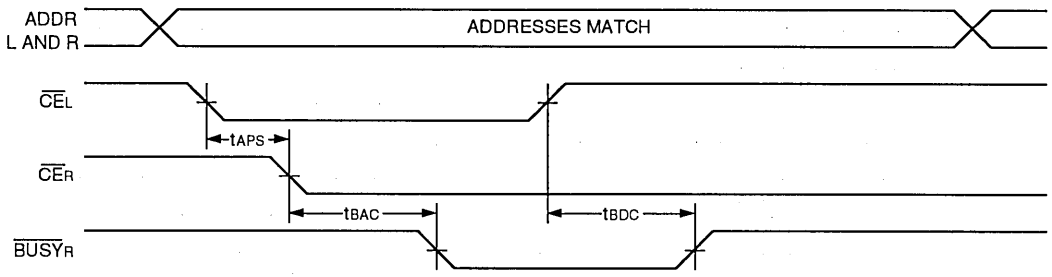
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7140 ONLY)



2689 drw 13

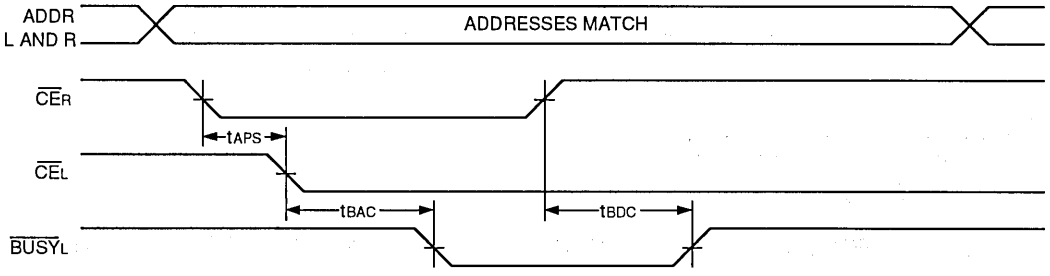
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7130 ONLY)

$\overline{CE}_L$ VALID FIRST:



$\overline{CE}_R$ VALID FIRST:

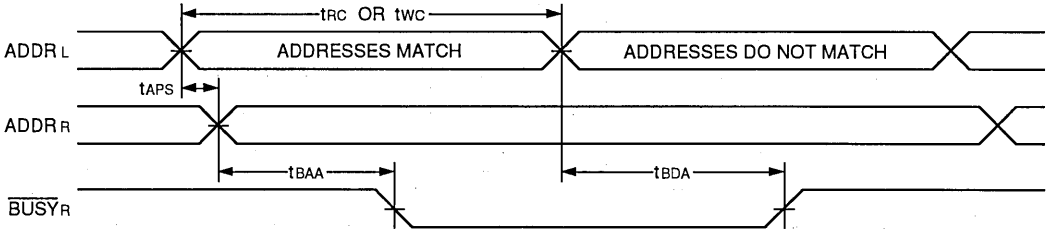
2689 drw 14



2689 drw 15

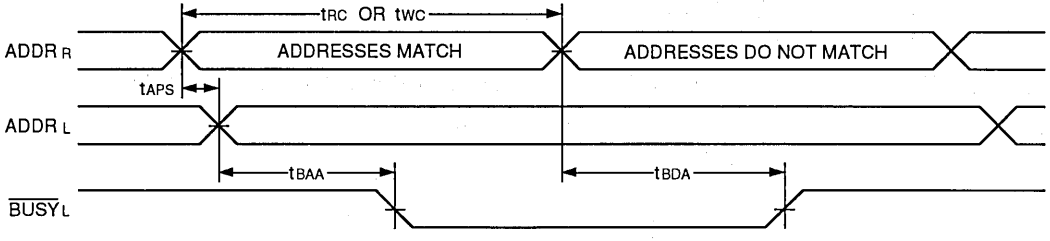
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (FOR MASTER IDT7130 ONLY)

LEFT ADDRESS VALID FIRST:



2689 drw 16

RIGHT ADDRESS VALID FIRST:



2689 drw 17

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (3)

Symbol	Parameter	7130 x 20(1,4) 7140 x 20(1,4) Min.	Max.	7130 x 25(4) 7140 x 25(4) Min.	Max.	7130 x 30(4) 7140 x 30(4) Min.	Max.	7130 x 35(5) 7140 x 35(5) Min.	Max.	7130 x 45 7140 x 45 Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	—	35	—	40	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	—	35	—	40	ns

2689 tbl 16

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

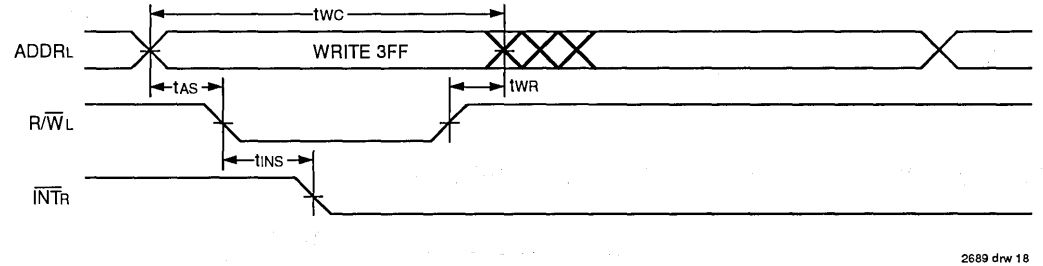
Symbol	Parameter	7130 x 55 7140 x 55 Min.	Max.	7130 x 70 7140 x 70 Min.	Max.	7130 x 90 7140 x 90 Min.	Max.	7130 x 100 7140 x 100 Min.	Max.	7130 x 120(2) 7140 x 120(2) Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	45	—	50	—	55	—	60	—	70	ns
tINR	Interrupt Reset Time	—	45	—	50	—	55	—	60	—	70	ns

2689 tbl 17

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (SA or LA).
4. Not available in DIP packages, see 7030/40 data sheet.
5. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

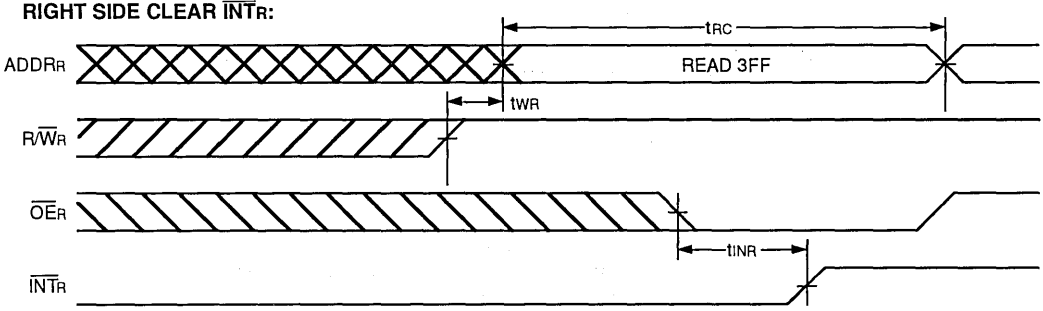
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2689 drw 18

RIGHT SIDE CLEAR $\overline{INT}_R$:

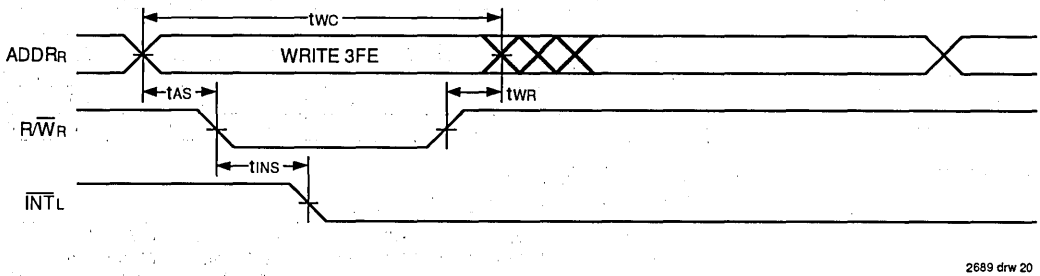


2689 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power up.

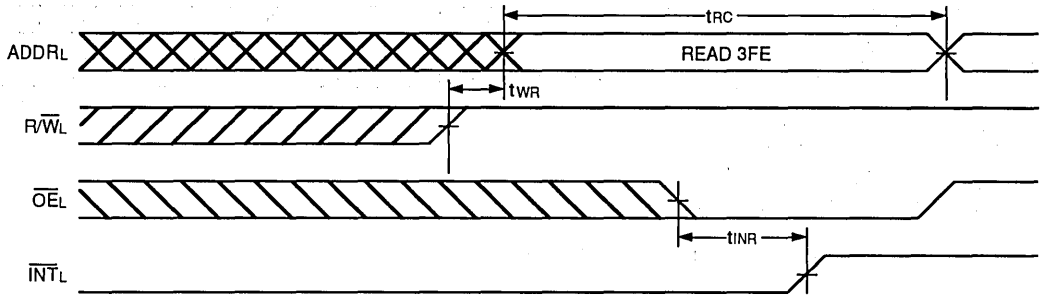
TIMING WAVEFORM OF INTERRUPT MODE(1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



2689 drw 20

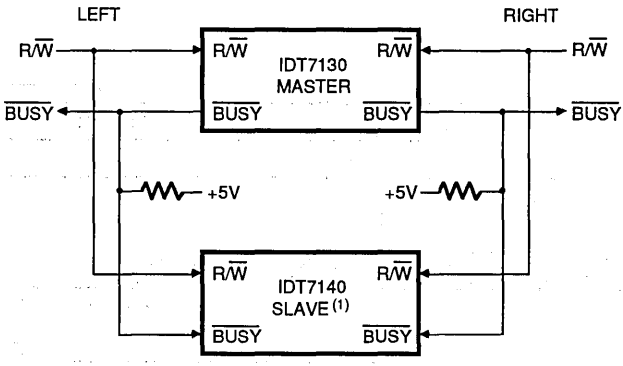
LEFT SIDE CLEAR $\overline{INT}_L$:



2689 drw 21

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2689 drw 22

NOTE:
1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/IDT7140 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory(2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2689 tbl 18

NOTES:
1. A_{0L}-$A_{9L} \neq A_{0R}$-A_{9R}
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG(1, 4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_{9R}	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2689 tbl 19

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III – ARBITRATION (2)

Left Port		Right Port		Flags(1)		
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A_{0R}-A_{9R}	L	≠ A_{0L}-A_{9L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R}-A_{9R}	LL5R	= A_{0L}-A_{9L}	H	L	L-Port Wins
RL5L	= A_{0R}-A_{9R}	RL5L	= A_{0L}-A_{9L}	L	H	R-Port Wins
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	H	L	Arbitration Resolved
LW5R	= A_{0R}-A_{9R}	LW5R	= A_{0L}-A_{9L}	L	H	Arbitration Resolved

2689 tbl 20

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

PRELIMINARY
IDT7030SA/LA
IDT7040SA/LA

FEATURES:

- High-speed access
  - —Military: 25/35/45ns (max.)
  - —Commercial: 20/25/35ns (max.)
- Low-power operation
  - —IDT7030/40SA
    - Active: 400mW (typ.)
    - Standby: 7mW (typ.)
  - —IDT7030/40LA
    - Active: 400mW (typ.)
    - Standby: 2mW (typ.)
- MASTER IDT7030 easily expands data bus width to 16-or-more-bits using SLAVE IDT7040
- On-chip port arbitration logic (IDT7030 only)
- $\overline{BUSY}$ output flag on IDT7030; $\overline{BUSY}$ input on IDT7040
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

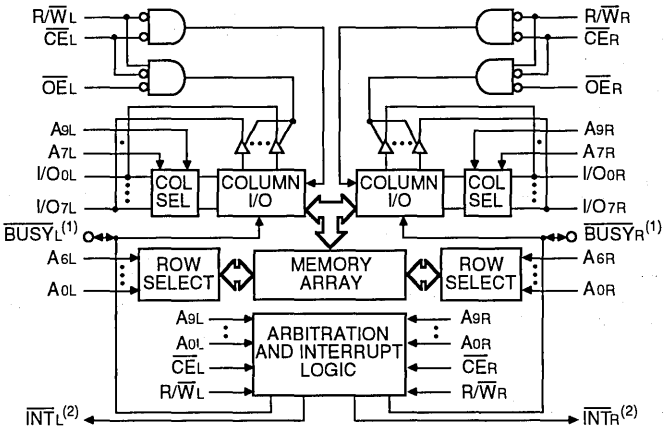
The IDT7030/IDT7040 are high speed 1K x 8 dual-port static RAMs. The IDT7030 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7040 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7030/IDT7040 devices are packaged in 48-pin sidebraze or plastic DIPs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2690 drw 01

NOTES:
1. IDT7030 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7040 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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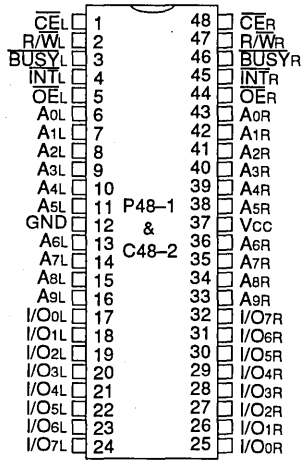
PIN CONFIGURATIONS



2690 drw 02

DIP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2690 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2690 tbl 04

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2690 tbl 02

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2690 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7030SA IDT7040SA Min.	IDT7030SA IDT7040SA Max.	IDT7030LA IDT7040LA Max.	IDT7030LA IDT7040LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2690 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7030 x 20[2] 7040 x 20[2] Typ.	7030 x 20[2] 7040 x 20[2] Max.	7030 x 25 7040 x 25 Typ.	7030 x 25 7040 x 25 Max.	7030 x 35 7040 x 35 Typ.	7030 x 35 7040 x 35 Max.	7030 x 45[3] 7040 x 45[3] Typ.	7030 x 45[3] 7040 x 45[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	125	300	125	290	125	285	mA
				LA	—	—	125	240	125	230	125	225	
			Com'l.	SA	125	265	125	260	125	250	—	—	
				LA	125	215	125	210	125	200	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	SA	—	—	30	80	30	80	30	80	mA
				LA	—	—	30	60	30	60	30	60	
			Com'l.	SA	30	65	30	65	30	65	—	—	
				LA	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	80	195	80	185	80	180	mA
				LA	—	—	80	160	80	150	80	145	
			Com'l.	SA	80	180	80	175	80	165	—	—	
				LA	80	145	80	140	80	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	SA	—	—	1.0	30	1.0	30	1.0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f=f_{MAX}[4]	Mil.	SA	—	—	70	185	70	175	70	170	mA
				LA	—	—	70	150	70	140	70	135	
			Com'l.	SA	70	175	70	170	70	160	—	—	
				LA	70	140	70	135	70	125	—	—	

NOTES:

2690 tbl 06

1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At V_{CC}≤2.0V input leakages are undefined.

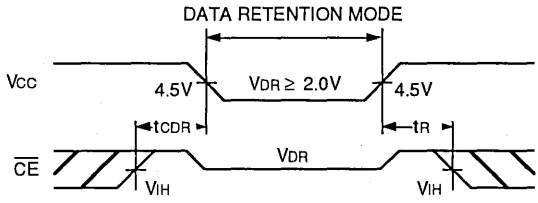
6

DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7030LA/IDDT7040LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ - 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current	$V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2690 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2690 tbl 08

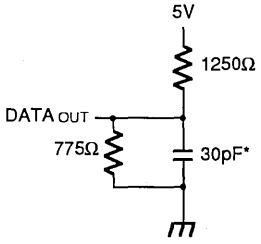


Figure 1. Output Load

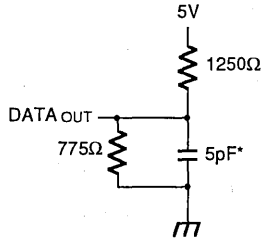
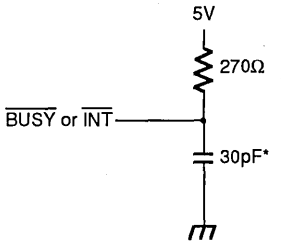


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})



2690 drw 04

Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig

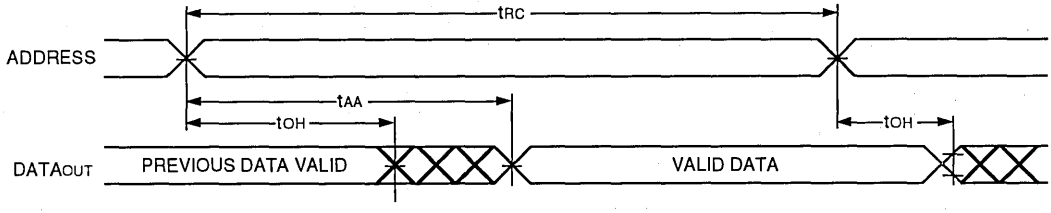
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7030 x 20[2] 7040 x 20[2] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[3] 7040 x 45[3] Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	ns

2690 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

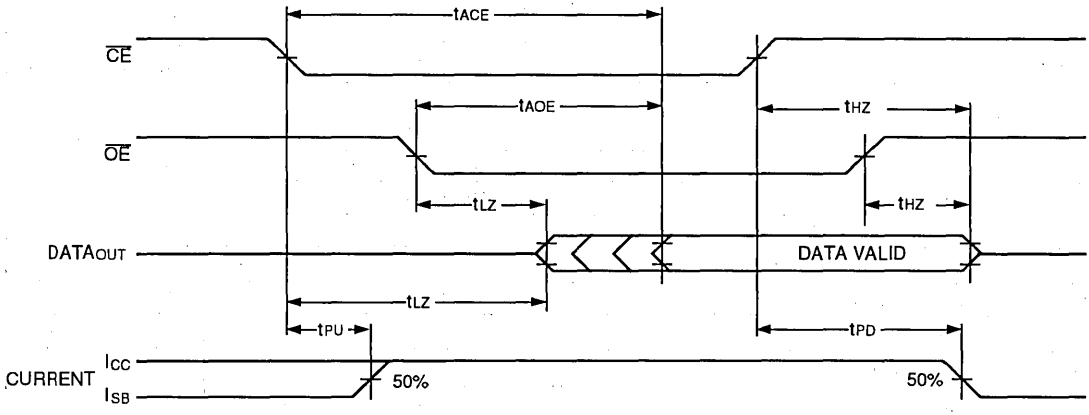
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



2690 drw 05

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1,3]



2690 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

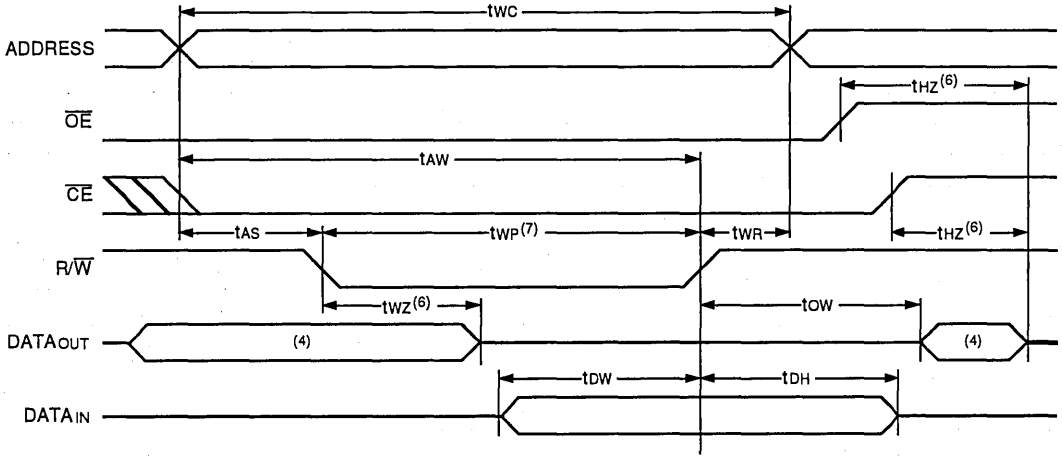
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7030 x 20[2] 7040 x 20[2] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[3] 7040 x 45[3] Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time[5]	20	—	25	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	20	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10	—	15	—	20	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	ns

2690 tbl 10

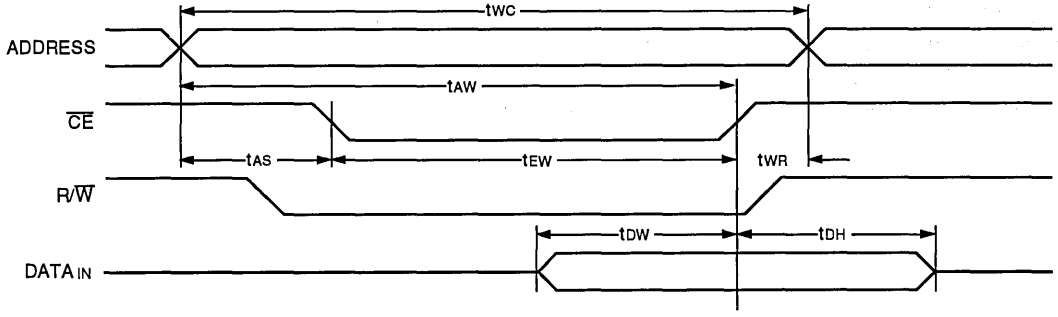
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2690 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2690 drw 08

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

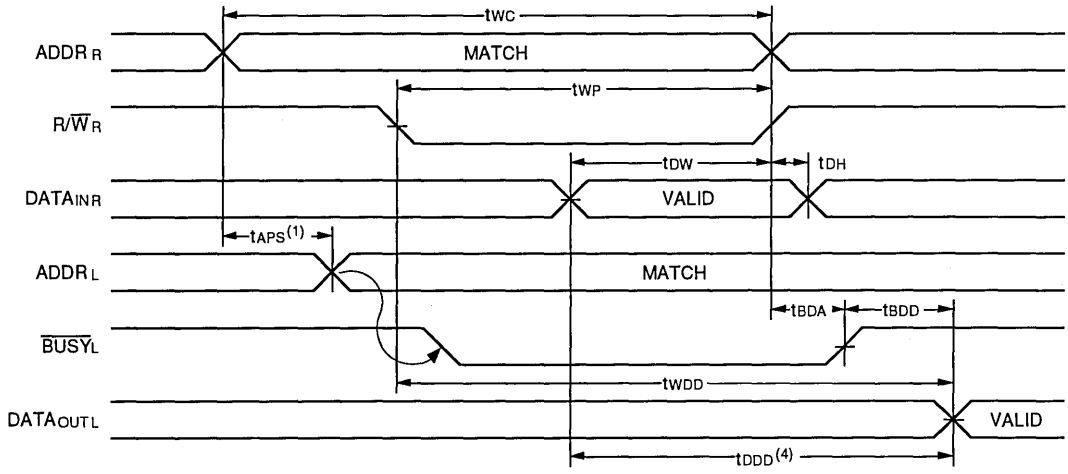
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7030 x 20[1] 7040 x 20[1] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[2] 7040 x 45[2] Min.	Max.	Unit
Busy Timing (For Master IDT7030 Only)										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	35	—	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	20	—	20	—	30	—	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	30	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	25	ns
t_{WDD}	Write Pulse to Data Delay[3]	—	50	—	50	—	60	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[3]	—	35	—	35	—	45	—	55	ns
t_{APS}	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7040 Only)										
t_{WB}	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[7]	12	—	15	—	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay[9]	—	50	—	50	—	60	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[9]	—	35	—	35	—	45	—	55	ns

2690 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7030 only)".
4. To ensure that the earlier of the two ports wins.
5. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD}-t_{WP} (actual) or t_{DDD}-t_{DW} (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (for Slave IDT7040 Only)".

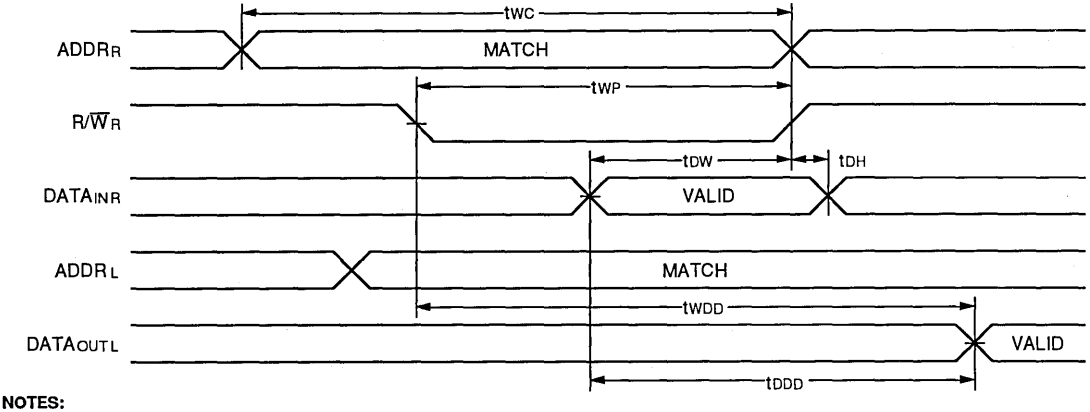
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1,2,3] (FOR MASTER IDT7030 ONLY)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

2690 drw 09

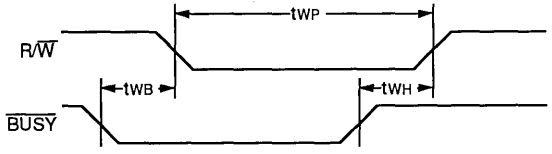
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1,2,3] (FOR SLAVE IDT7040 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

2690 drw 10

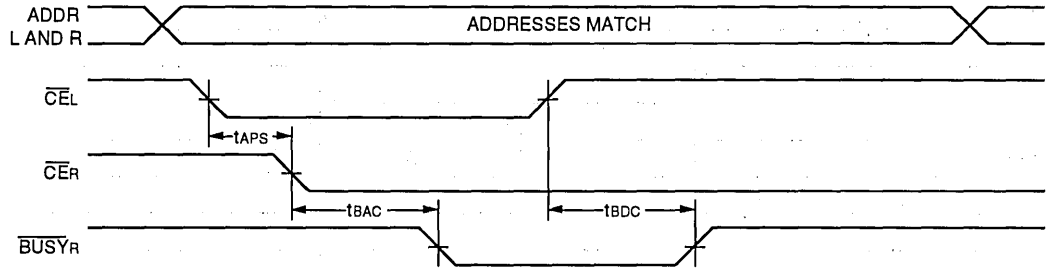
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7040 ONLY)



2690 drw 11

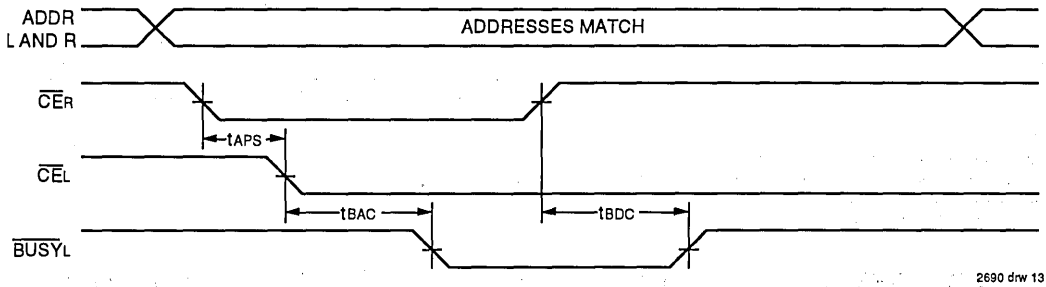
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7030 ONLY)

$\overline{CE}_L$ VALID FIRST:



$\overline{CE}_R$ VALID FIRST:

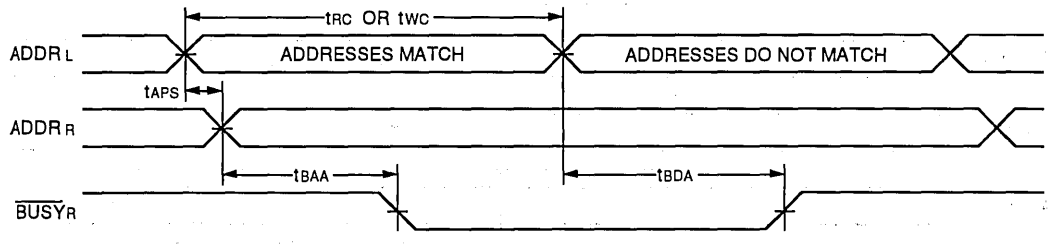
2690 drw 12



2690 drw 13

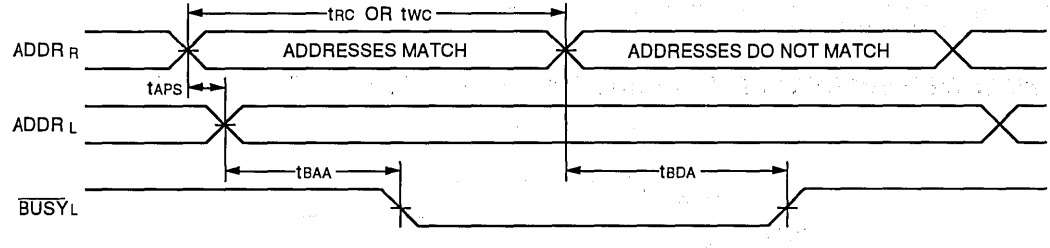
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION[1] (FOR MASTER IDT7030 ONLY)

LEFT ADDRESS VALID FIRST:



2690 drw 14

RIGHT ADDRESS VALID FIRST:



2690 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

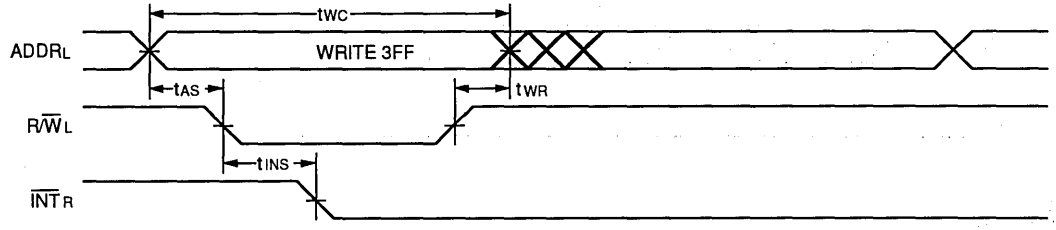
Symbol	Parameter	7030 x 20[1] 7040 x 20[1] Min.	Max.	7030 x 25 7040 x 25 Min.	Max.	7030 x 35 7040 x 35 Min.	Max.	7030 x 45[2] 7040 x 45[2] Min.	Max.	Unit
Interrupt Timing										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	35	—	40	ns
tINR	Interrupt Reset Time	—	20	—	25	—	35	—	40	ns

2690 tbl 12

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. "x" in part numbers indicates power rating (SA or LA).

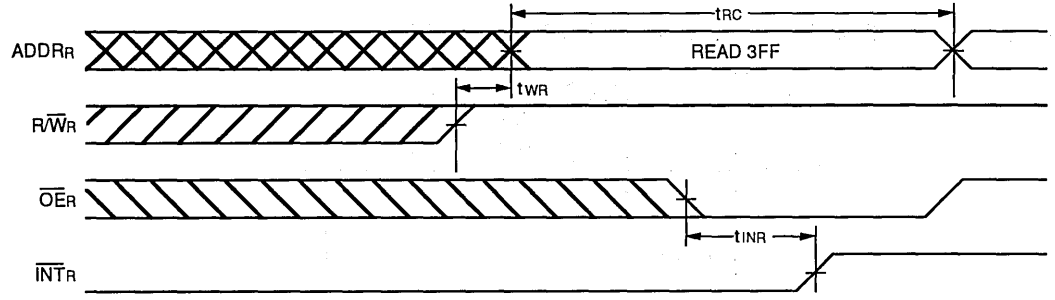
TIMING WAVEFORM OF INTERRUPT MODE[1,2]

LEFT SIDE SETS $\overline{INT}_R$:



2690 drw 16

RIGHT SIDE CLEARS $\overline{INT}_R$:



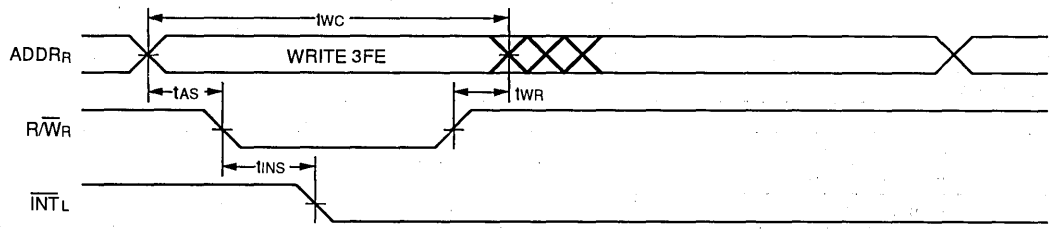
2690 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power up.

6

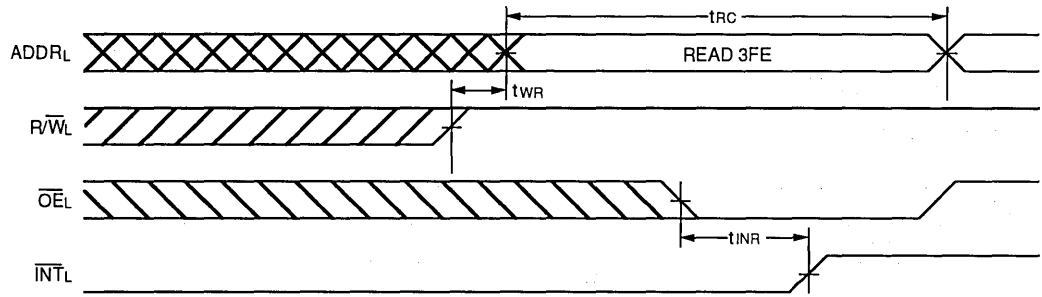
TIMING WAVEFORM OF INTERRUPT MODE[1,2]

RIGHT SIDE SETS $\overline{INT}_L$:



2690 drw 18

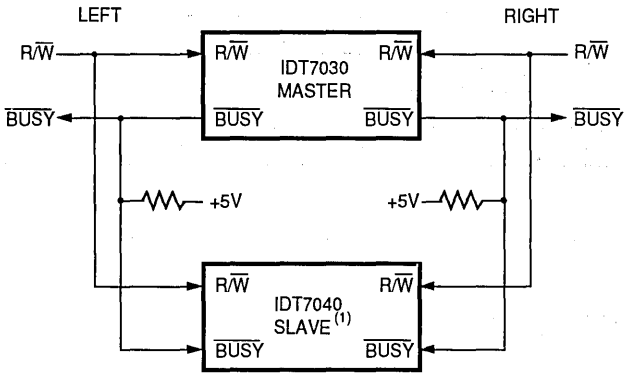
LEFT SIDE CLEARS $\overline{INT}_L$:



2690 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2690 drw 20

NOTE:
1. No arbitration in IDT7040 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7040 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT7030/IDT7040 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7030/IDT7040 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE (HEX). Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$) the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMS must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory [2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port [3]
H	L	H	Z	High Impedance Outputs

2690 tbl 13

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right INTR Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right INTR Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left INTL Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left INTL Flag

NOTES:
1. Assume $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

2690 tbl 14

TABLE II – ARBITRATION[1,2]

Left Port		Right Port		Flags[1]		
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠A0R-A9R	L	≠A0L-A9L	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	=A0R-A9R	LL5R	=A0L-A9L	H	L	L-Port Wins
RL5L	=A0R-A9R	RL5L	=A0L-A9L	L	H	R-Port Wins
LW5R	=A0R-A9R	LW5R	=A0L-A9L	H	L	Arbitration Resolved
LW5R	=A0R-A9R	LW5R	=A0L-A9L	L	H	Arbitration Resolved

2690 tbl 15

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH. LV5R = Left Address Valid ≥ 5ns before right address. RV5L = Right Address Valid ≥ 5ns before left address. Same = Left and Right Addresses match within 5ns of each other. LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$. RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$. LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132SA/LA
IDT7142SA/LA

FEATURES:

- High-speed access
  - — Military: 25/30/35/45/55/70/90/100/120ns (max.)
  - — Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - — IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation —2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002
- Industrial temperature range (-40°C to +85°C) is available, tested to miliary electrical specifications

DESCRIPTION:

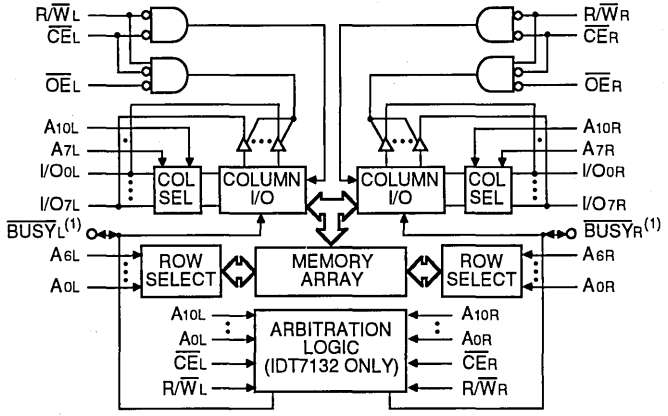
The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and a 48-lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

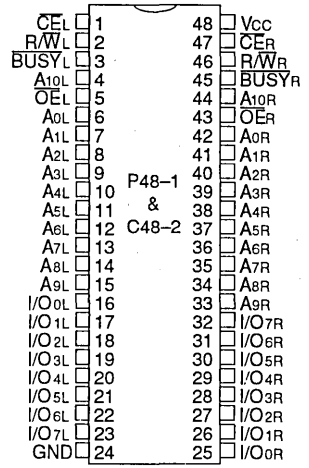


2692 drw 01

NOTE:
1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.

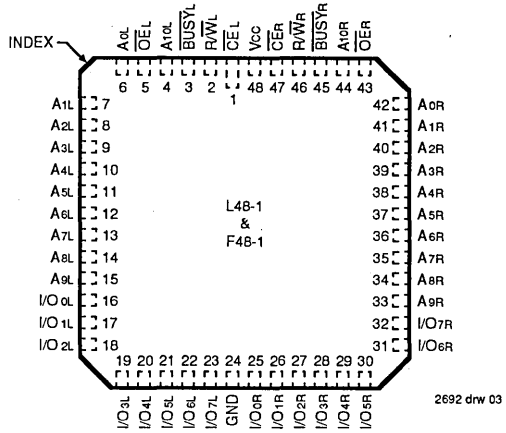
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



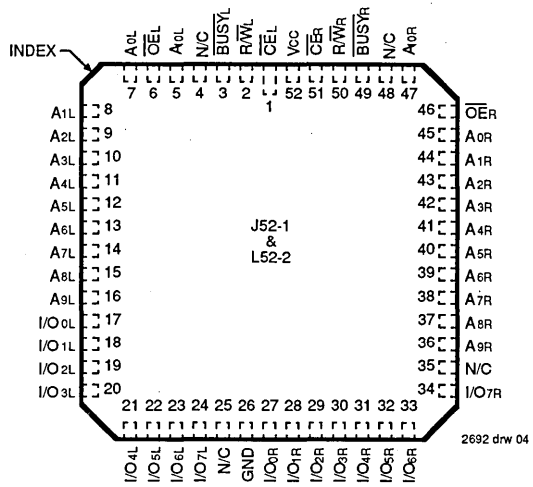
DIP
TOP VIEW

2692 drw 02



2692 drw 03

48-PIN LCC/FLATPACK
TOP VIEW



2692 drw 04

52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2692 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2692 tbl 02

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2692 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7132SA IDT7142SA Min.	IDT7132SA IDT7142SA Max.	IDT7132LA IDT7142LA Max.	IDT7132LA IDT7142LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[9]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2692 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLE VOLTAGE RANGE[1,8] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7132 x 20[2,6] 7142 x 20[2,6] Typ.	Max.	7132 x 25[6] 7142 x 25[6] Typ.	Max.	7132 x 30[6] 7142 x 30[6] Typ.	Max.	7132 x 35[7] 7142 x 35[7] Typ.	Max.	7132 x 45 7142 x 45 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil. SA	—	—	125	300	125	295	125	290	75	230	mA
			Mil. LA	—	—	125	240	125	235	125	230	75	185	
			Com'l. SA	125	265	125	260	125	255	75	195	75	190	
			Com'l. LA	125	215	125	210	125	205	75	155	75	145	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil. SA	—	—	30	80	30	80	30	80	25	65	mA
			Mil. LA	—	—	30	60	30	60	30	60	25	55	
			Com'l. SA	30	65	30	65	30	65	25	65	25	65	
			Com'l. LA	30	45	30	45	30	45	25	45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	—	—	80	195	80	190	80	185	40	135	mA
			Mil. LA	—	—	80	160	80	155	80	150	40	110	
			Com'l. SA	80	180	80	175	80	170	40	130	40	120	
			Com'l. LA	80	145	80	140	80	135	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil. SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
			Mil. LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			Com'l. LA	0.2	5	0.2	5	0.2	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	—	—	70	185	70	180	70	175	40	125	mA
			Mil. LA	—	—	70	150	70	145	70	140	35	95	
			Com'l. SA	70	175	70	170	70	165	40	115	40	105	
			Com'l. LA	70	140	70	135	70	130	35	90	35	80	

2692 tbl 05

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.
8. V_{CC}=5V, T_A=+25°C for Typ.
9. At $V_{CC} \leq$2.0V input leakages are undefined.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1,8] (Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7132 x 55 7142 x 55 Typ.	Max.	7132 x 70 7142 x 70 Typ.	Max.	7132 x90 7142 x 90 Typ.	Max.	7132 x 100 7142 x 100 Typ.	Max.	7132 x 120[3] 7142 x 120 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
			Com'l.	SA	65	180	65	180	65	180	65	180	—	—	
				LA	65	140	65	135	65	130	65	130	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
			Com'l.	SA	25	65	25	60	25	55	25	55	—	—	
				LA	25	45	25	40	25	35	25	35	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
			Com'l.	SA	40	115	40	110	40	110	40	110	—	—	
				LA	40	85	40	85	40	75	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			Com'l.	SA	40	100	40	100	40	95	40	95	—	—	
				LA	35	75	35	75	35	70	35	70	—	—	

2692 tbl 06

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.
8. V_{CC}=5V, T_A=+25°C for Typ.

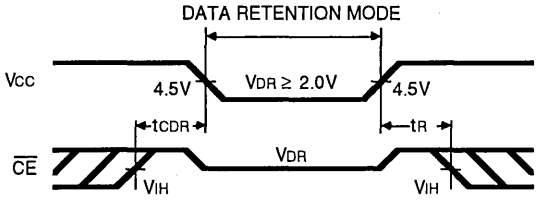
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7132LA/IDT7142LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2692 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2692 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, & 3

2692 tbl 08

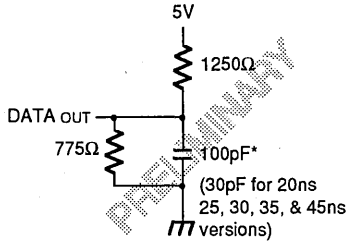


Figure 1. Output Load

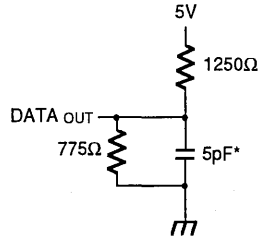


Figure 2. Output Load
(for tHV, tLZ, tWZ, and tOW)

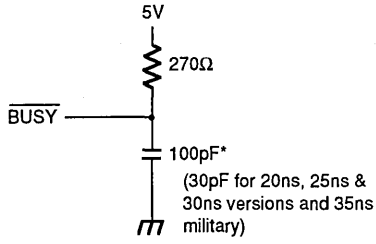


Figure 3. Busy Output Load
(IDT7132 only)

* Including scope and jig

2692 drw 06

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7132 x 20[2,6] 7142 x 20[2,6] Min.	Max.	7132 x 25[6] 7142 x 25[6] Min.	Max.	7132 x 30[6] 7142 x 30[6] Min.	Max.	7132 x 35[7] 7142 x 35[7] Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 09

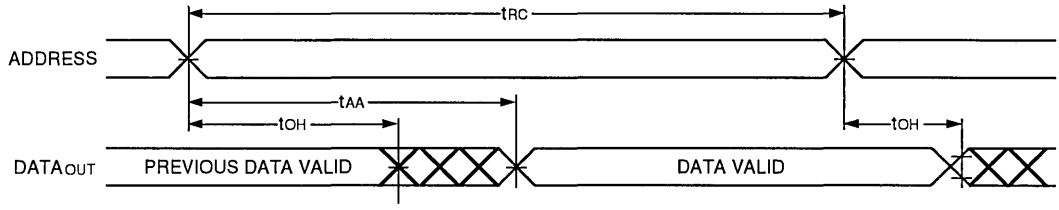
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5] (Continued)

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120[3] 7142 x 120[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
tAA	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
tACE	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
tAOE	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
tOH	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
tLZ	Output Low Z Time[1,4]	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

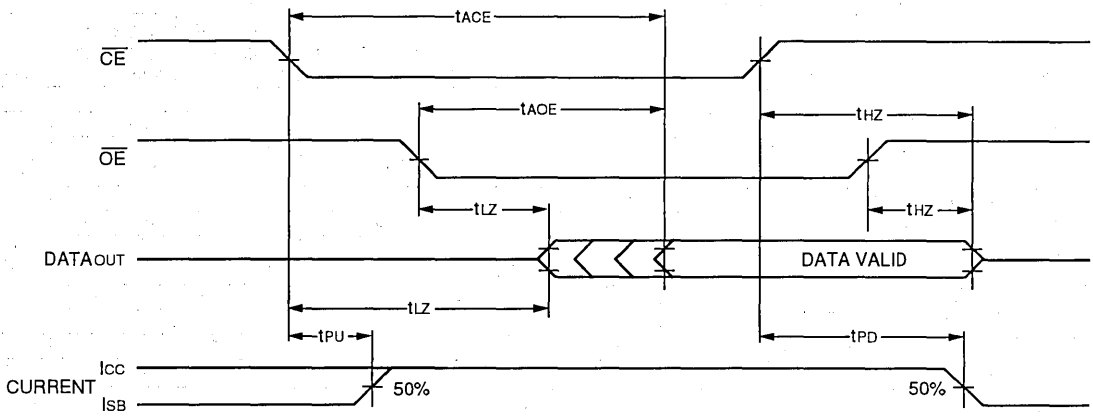
TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



2692 drw 07

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2692 drw 08

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

Symbol	Parameter	7132 x 20(2,8) 7142 x 20(2,8) Min.	Max.	7132 x 25(8) 7142 x 25(8) Min.	Max.	7132 x 30(8) 7142 x 30(8) Min.	Max.	7132 x 35(9) 7142 x 35(9) Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(6)	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write(1,4)	0	—	0	—	0	—	0	—	0	—	ns

2692 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages — see 7032/7042 data sheet.
9. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7] (Continued)

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120[3] 7142 x 120[3] Min.	Max.	Unit
Write Cycle												
t_{WC}	Write Cycle Time[5]	55	—	70	—	90	—	100	—	120	—	ns
t_{EW}	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[6]	40	—	50	—	55	—	55	—	65	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
t_{HZ}	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	—	30	—	35	—	40	—	40	—	50	ns
t_{OW}	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

2692 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

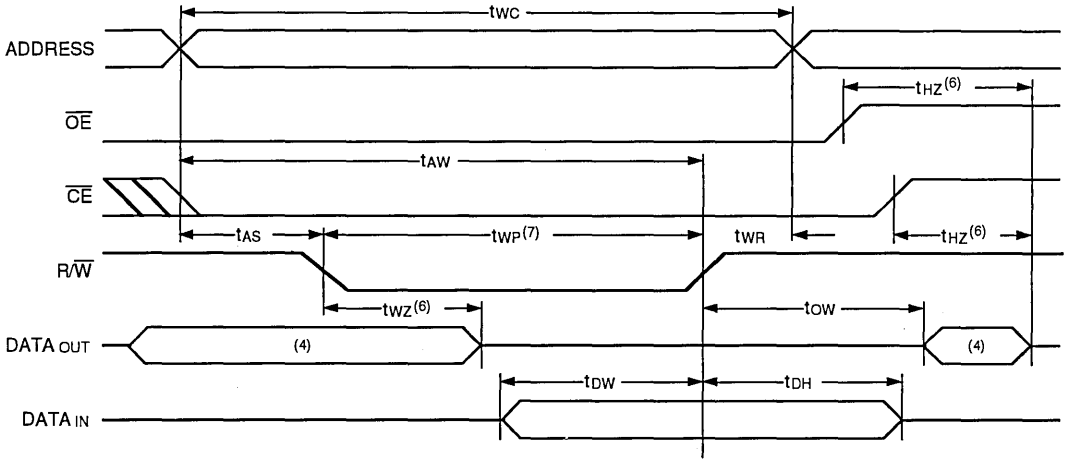
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

2692 tbl 13

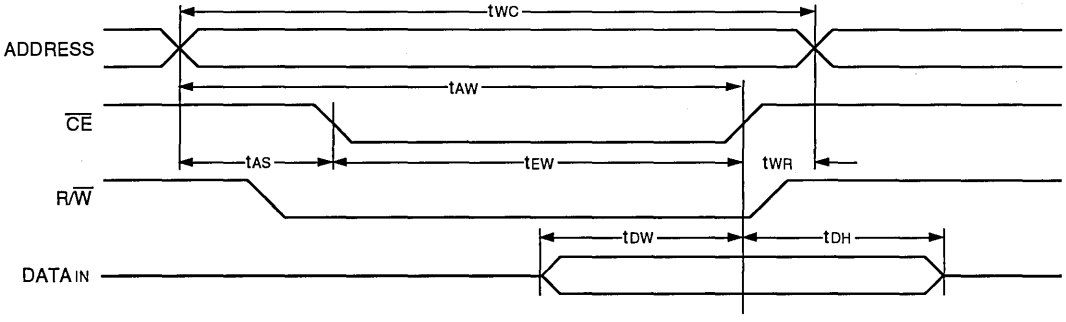
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2692 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2692 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 20 [1,10] 7142 x 20 [1,10] Min.	Max.	7132 x 25 [10] 7132 x 25 [10] Min.	Max.	7132 x 30 [10] 7142 x 30 [10] Min.	Max.	7132 x 35 [11] 7132 x 35 [11] Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	20	—	25	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay [3]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	35	—	35	—	35	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	35	—	35	—	35	—	35	—	45	ns

2692 tbl 14

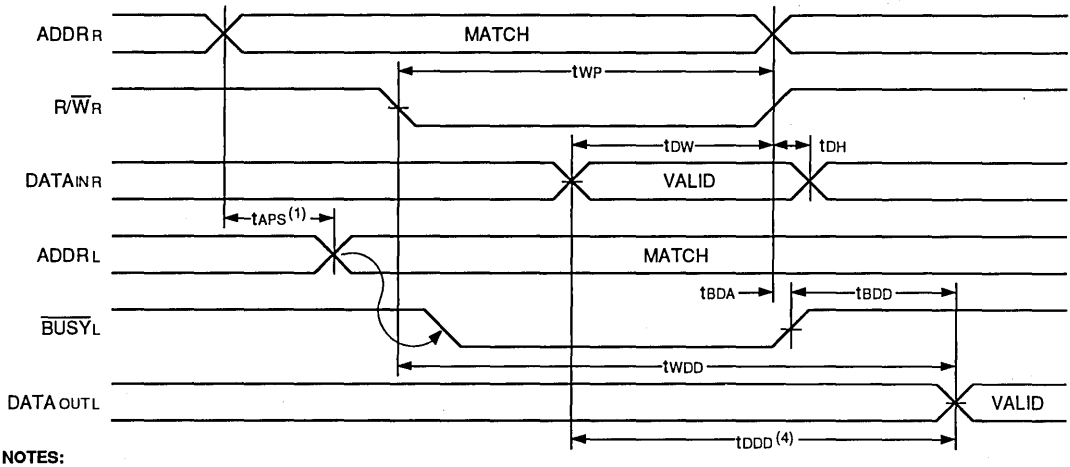
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120 [2] 7142 x 120 [2] Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay [3]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	55	—	70	—	90	—	100	—	120	ns

2692 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7132 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual)
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7142 Only)".
10. Not available in DIP packages — see 7032/7042 data sheet.
11. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

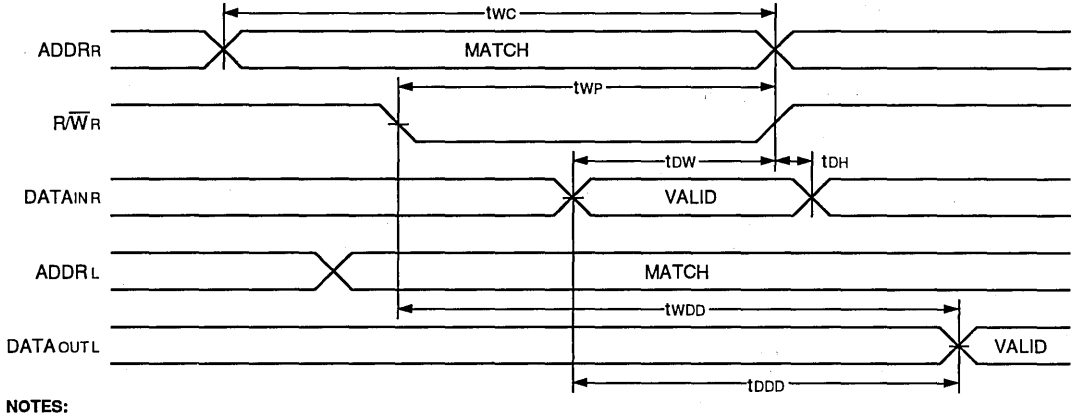
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7132 ONLY)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

2692 drw 11

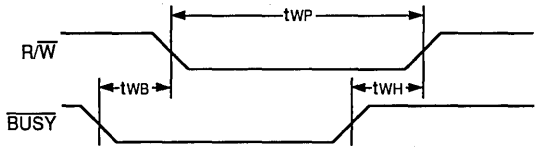
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7142 ONLY)



NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

2692 drw 12

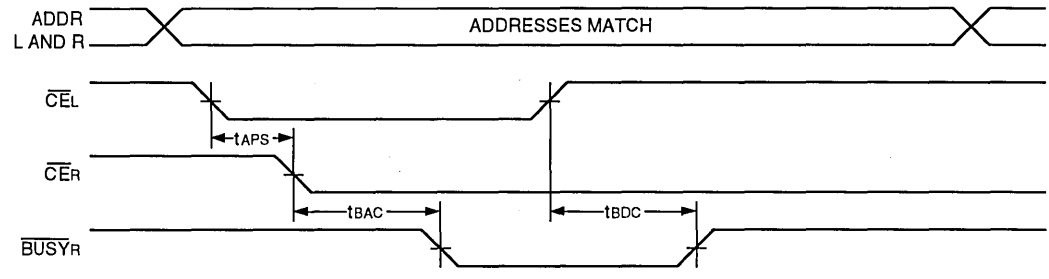
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7142 ONLY)



2692 drw 13

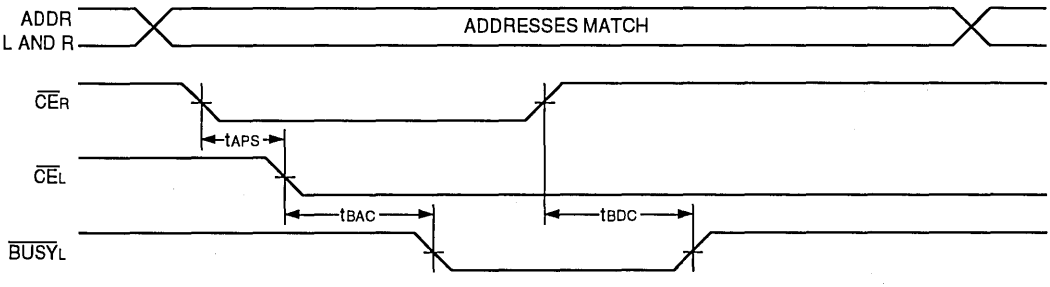
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7132 ONLY)

$\overline{CE}_L$ VALID FIRST:



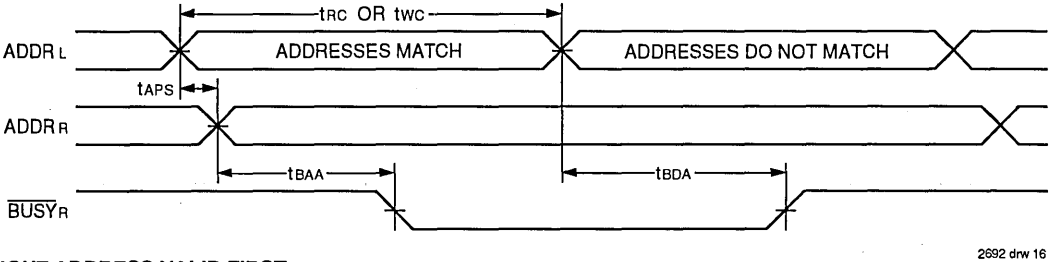
2692 drw 14

$\overline{CE}_R$ VALID FIRST:



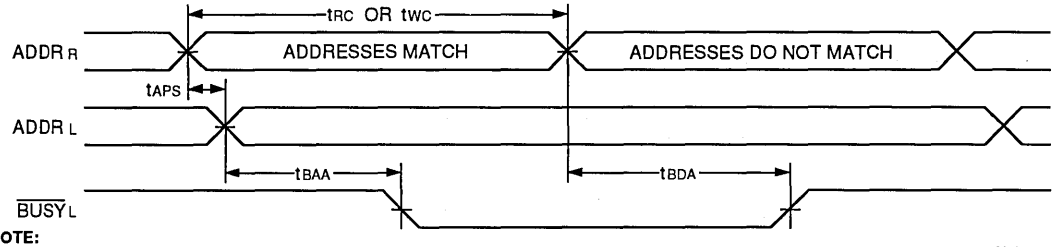
2692 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (FOR MASTER IDT7132 ONLY)



2692 drw 16

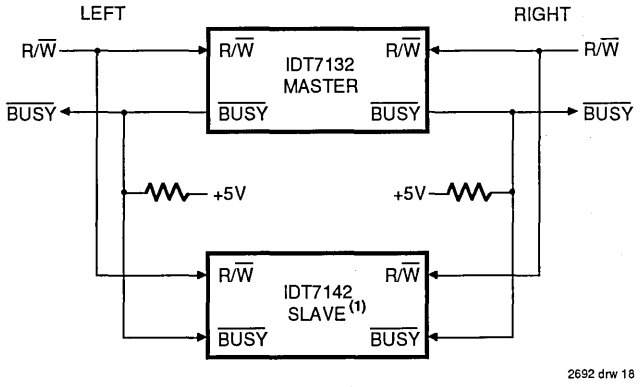
RIGHT ADDRESS VALID FIRST:



NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

2692 drw 17

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7142 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port (1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance

2692 tbl 16

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – ARBITRATION(1,2)

Left Port		Right Port		Flags		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A0R -A10R	L	≠ A0L -A10L	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A0R -A10R	LL5R	= A0L -A10L	H	L	L-Port Wins
RL5L	= A0R -A10R	RL5L	= A0L -A10L	L	H	R-Port Wins
LW5R	= A0R -A10R	LW5R	= A0L -A10L	H	L	Arbitration Resolved
LW5R	= A0R -A10R	LW5R	= A0L -A10L	L	H	Arbitration Resolved

2692 tbl 17

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

PRELIMINARY
IDT7032SA/LA
IDT7042SA/LA

FEATURES

- High-speed access
  - —Military: 25/35/45ns (max.)
  - —Commercial: 20/25/35ns (max.)
- Low-power operation
  - —IDT7032/42SA
    - Active: 400mW (typ.)
    - Standby: 7mW (typ.)
  - —IDT7032/42LA
    - Active: 400mW (typ.)
    - Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7032 easily expands data bus width to 16-or-more-bits using SLAVE IDT7042
- On-chip port arbitration logic (IDT7032 only)
- $\overline{BUSY}$ output flag on IDT7032; $\overline{BUSY}$ input on IDT7042
- Battery backup operation -2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

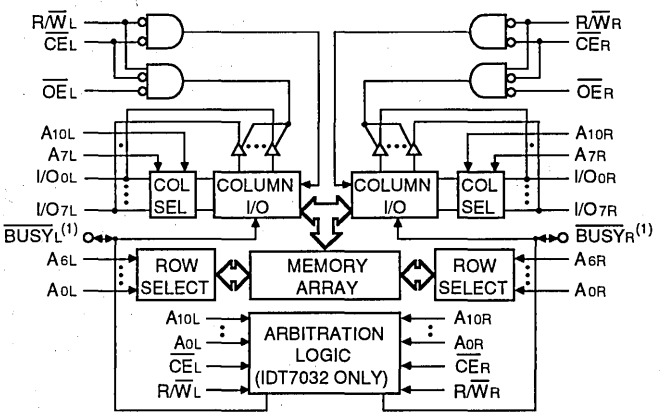
The IDT7032/IDT7042 are high speed 2K x 8 dual-port static RAMs. The IDT7032 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7042 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independant ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7032/7042 devices are packaged in 48-pin sidebraze or plastic DIPs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

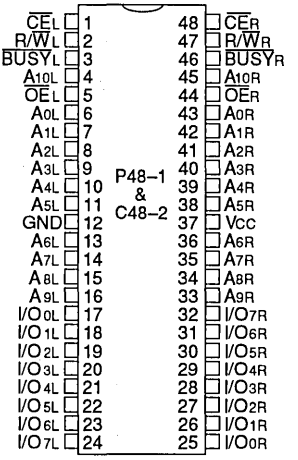


2693 drw 01

NOTE:
1. IDT7032 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7042 (SLAVE): $\overline{BUSY}$ is input.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2693 drw 02

DIP
Top View

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2693 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2693 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2693 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7032SA IDT7042SA Min.	IDT7032SA IDT7042SA Max.	IDT7032LA IDT7042LA Max.	IDT7032LA IDT7042LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2693 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7032 x 20[2] 7042 x 20[2] Typ.	7032 x 20[2] 7042 x 20[2] Max.	7032 x 25 7042 x 25 Typ.	7032 x 25 7042 x 25 Max.	7032 x 35 7042 x 35 Typ.	7032 x 35 7042 x 35 Max.	7032 x 45[3] 7042 x 45[3] Typ.	7032 x 45[3] 7042 x 45[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	SA	—	—	125	300	125	290	125	285	mA
				LA	—	—	125	240	125	230	125	225	
			COM'L.	SA	125	265	125	260	125	250	—	—	mA
				LA	125	215	125	210	125	200	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	MIL.	SA	—	—	30	80	30	80	30	80	mA
				LA	—	—	30	60	30	60	30	60	
			COM'L.	SA	30	65	30	65	30	65	—	—	mA
				LA	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	—	—	80	195	80	185	80	180	mA
				LA	—	—	80	160	80	150	80	145	
			COM'L.	SA	80	180	80	175	80	165	—	—	mA
				LA	80	145	80	140	80	130	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL.	SA	—	—	1.0	30	1.0	30	1.0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	
			COM'L.	SA	1.0	15	1.0	15	1.0	15	—	—	mA
				LA	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	MIL.	SA	—	—	70	185	70	175	70	170	mA
				LA	—	—	70	150	70	140	70	135	
			COM'L.	SA	70	175	70	170	70	160	—	—	mA
				LA	70	140	70	135	70	125	—	—	

2693 tbl 05

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At $V_{CC} \leq$2.0V input leakages are undefined.

6

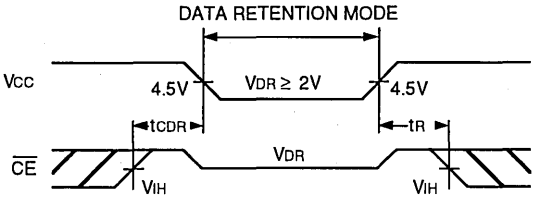
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7032LA/IDT7042LA Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		MIL.	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2693 tbl 06

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2693 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2693 tbl 07

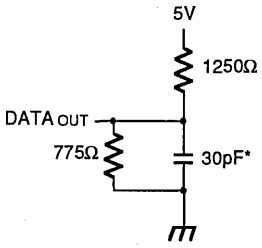


Figure 1. Output Load

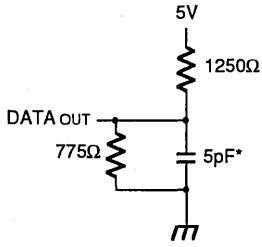


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

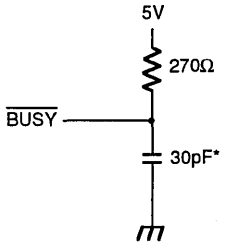


Figure 3. $\overline{BUSY}$ Output Load (IDT7032 only)

2693 drw 04

* Including scope and jig

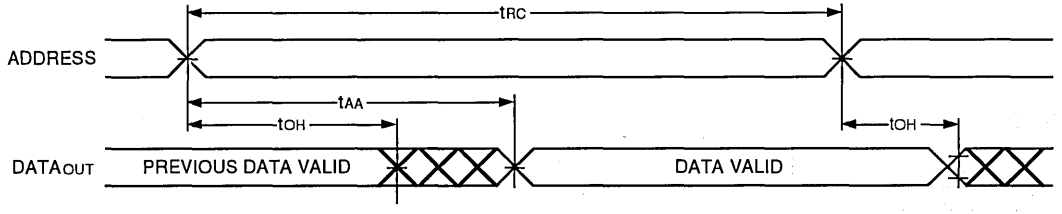
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	7032 x 20(2) 7042 x 20(2) Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45(3) 7042 x 45(3) Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1,4)	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time(1,4)	—	8	—	10	—	15	—	20	ns
tPU	Chip Enable to Power Up Time(4)	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(4)	—	50	—	50	—	50	—	50	ns

2693 tbl 08

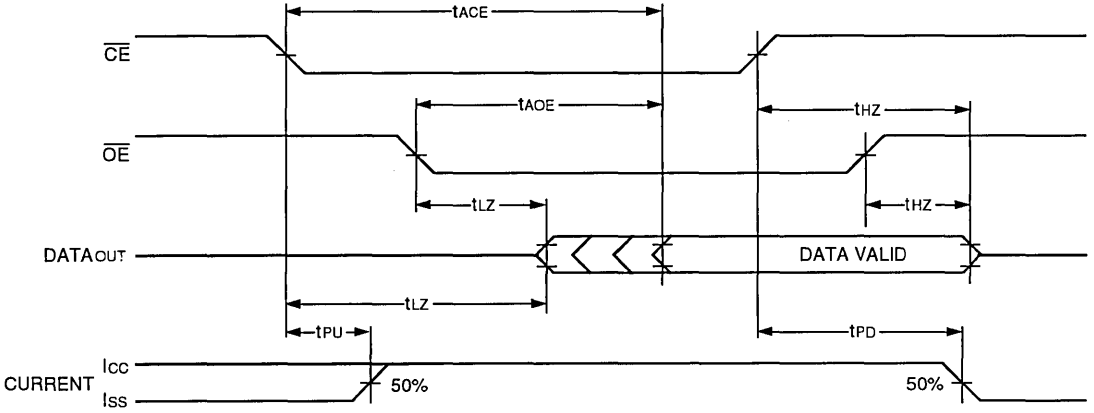
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2693 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

2693 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	7032 x 20[2] 7042 x 20[2] Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45[3] 7042 x 45[3] Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time[5]	20	—	25	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[6]	15	—	20	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	20	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10	—	15	—	20	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	ns

2693 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "X" in part numbers indicates power rating (SA or LA).

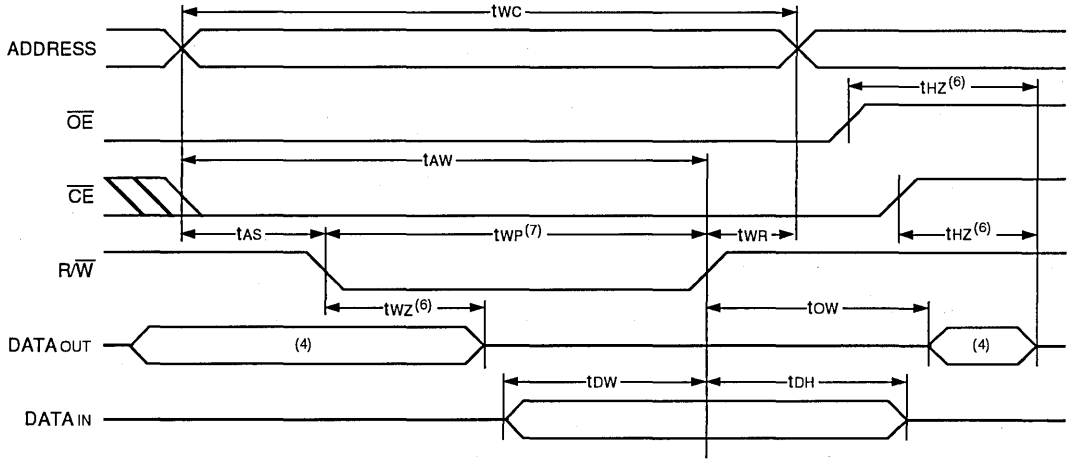
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2693 tbl 10

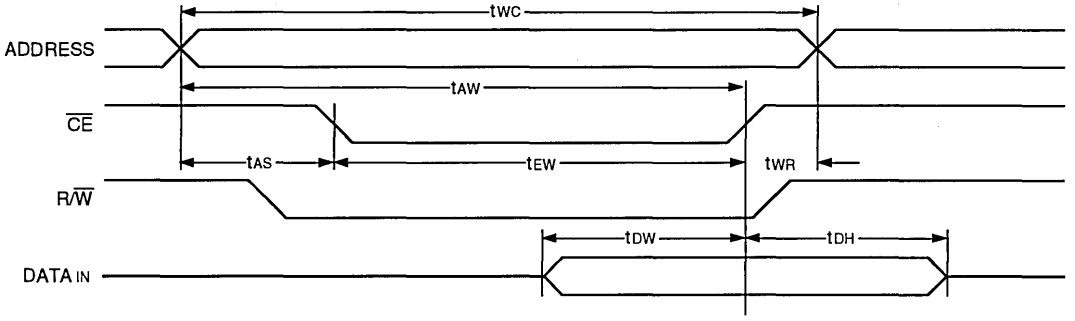
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING) (1,2,3,7)



2693 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING) (1,2,3,5)



2693 drw 08

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

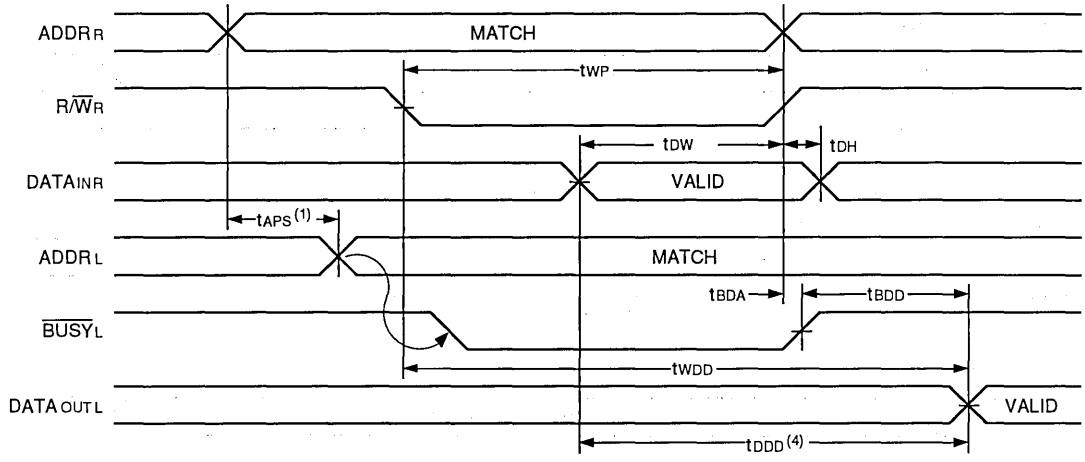
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(8)

Symbol	Parameter	7032 x 20(1) 7042 x 20(1) Min.	Max.	7032 x 25 7042 x 25 Min.	Max.	7032 x 35 7042 x 35 Min.	Max.	7032 x 45(2) 7042 x 45(2) Min.	Max.	Unit
Busy Timing (For Master IDT7032 Only)										
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	20	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	25	ns
tWDD	Write Pulse to Data Delay (3)	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay (3)	—	35	—	35	—	45	—	55	ns
tAPS	Arbitration Priority Set-up Time (4)	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data (5)	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7042 Only)										
tWB	Write to $\overline{BUSY}$ Input (6)	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ (7)	12	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay (9)	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay (9)	—	35	—	35	—	45	—	55	ns

2693 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7032 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7042 Only)".

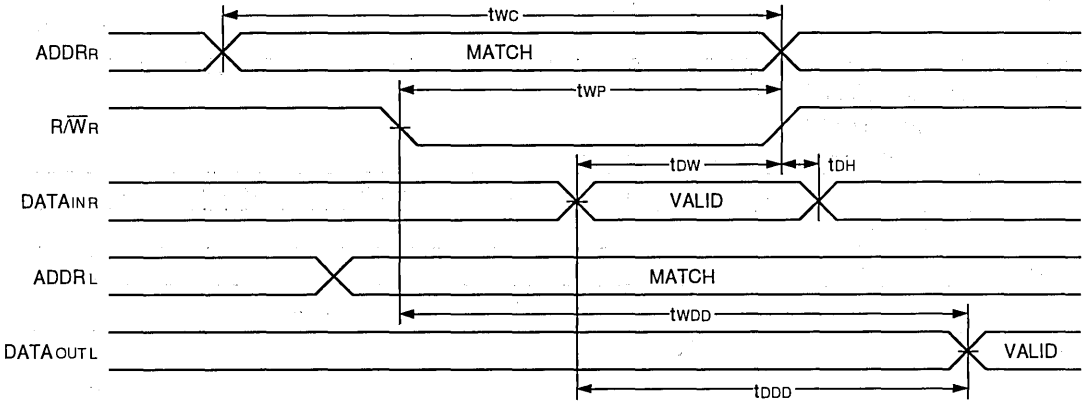
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3)(FOR MASTER IDT7032 ONLY)



2693 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

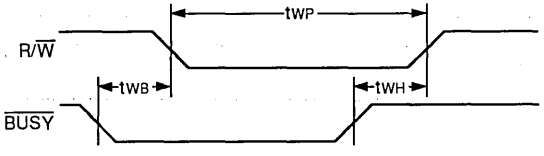
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1,2,3) (FOR SLAVE IDT7042 ONLY)



2693 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

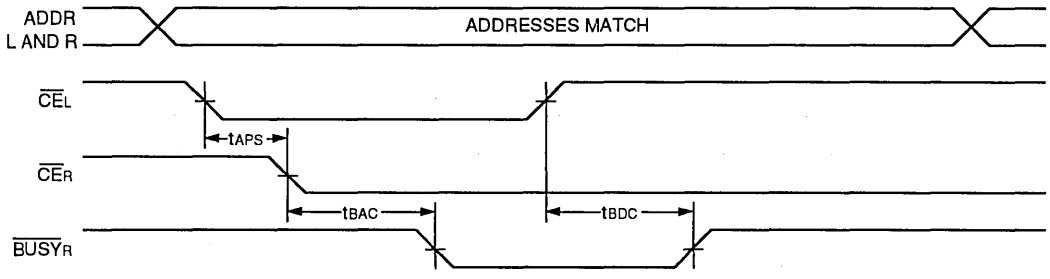
TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7042 ONLY)



2693 drw 11

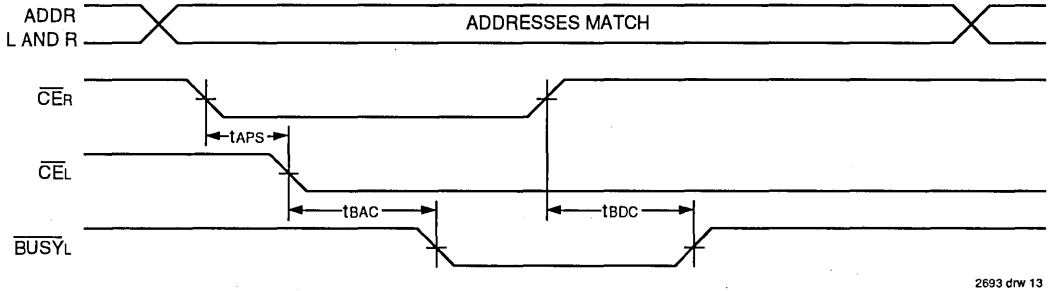
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7032 ONLY)

$\overline{CE}_L$ VALID FIRST:



2693 drw 12

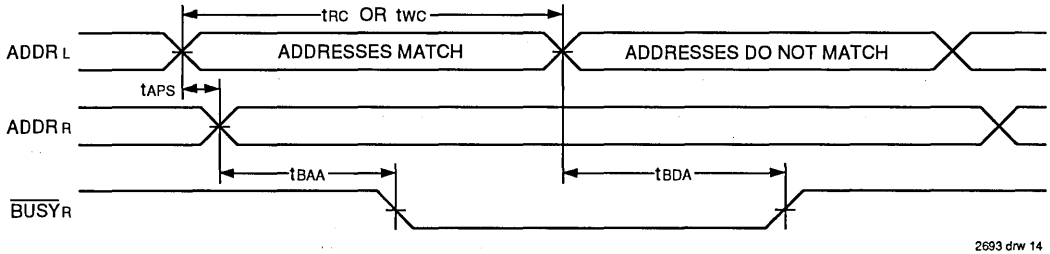
$\overline{CE}_R$ VALID FIRST:



2693 drw 13

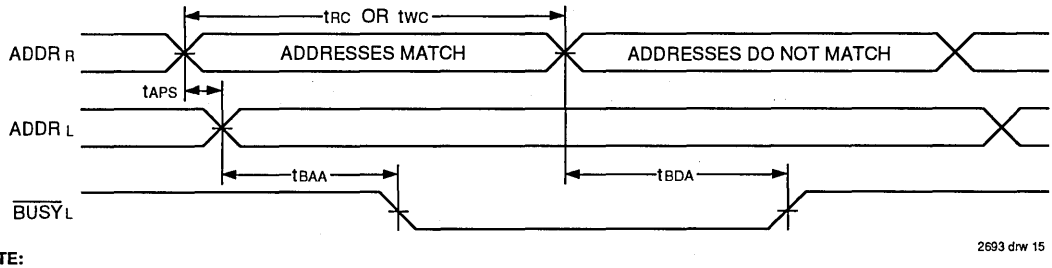
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (1) (FOR MASTER IDT7032 ONLY)

LEFT ADDRESS VALID FIRST:



2693 drw 14

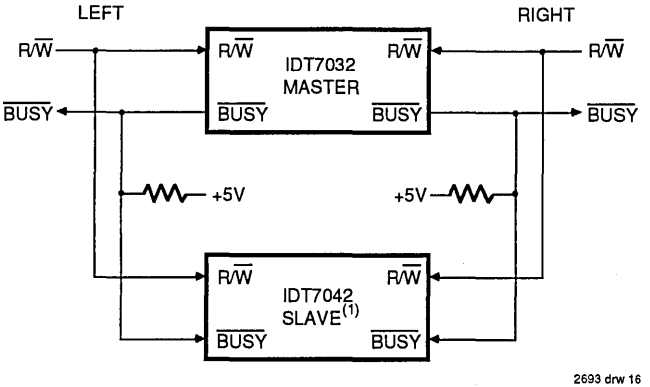
RIGHT ADDRESS VALID FIRST:



2693 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTE:
1. No arbitration in IDT7042 (SLAVE). BUSY-IN inhibits write in IDT7042 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT7032/42 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another aciti-vates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMS must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL (4)

Left Or Right Port (1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written into Memory (2)
H	L	L	DATAOUT	Data in Memory Output on Port (3)
H	L	H	Z	High Impedance Outputs

2693 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – ARBITRATION (1,2)

Left Port		Right Port		Flags (2)		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$ - A_{10R}	L	$\neq A_{0L}$ - A_{10L}	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= A_{0R} - A_{10R}	LL5R	= A_{0L} - A_{10L}	H	L	L-Port Wins
RL5L	= A_{0R} - A_{10R}	RL5L	= A_{0L} - A_{10L}	L	H	R-Port Wins
LW5R	= A_{0R} - A_{10R}	LW5R	= A_{0L} - A_{10L}	H	L	Arbitration Resolved
LW5R	= A_{0R} - A_{10R}	LW5R	= A_{0L} - A_{10L}	L	H	Arbitration Resolved

2693 tbl 13

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  - —Military: 25/30/35/45/55/70ns (max.)
  - —Commercial: 20/25/30/35/45/55ns (max.)
- Low-power operation
  - —IDT71321/IDT71421SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT71321/421LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation -2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 dual-port static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT71421 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

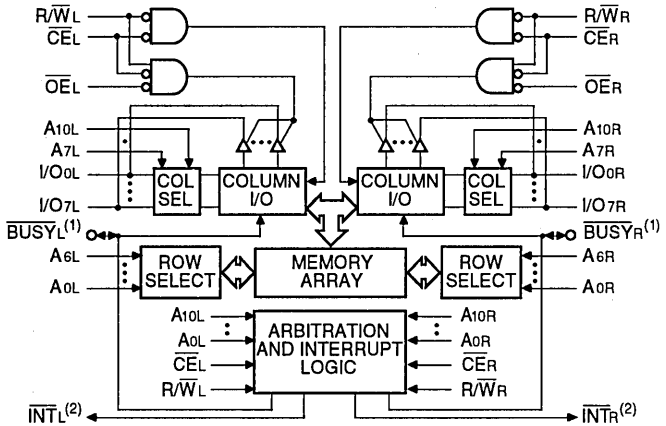
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin LCCs and PLCCs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

6

FUNCTIONAL BLOCK DIAGRAM

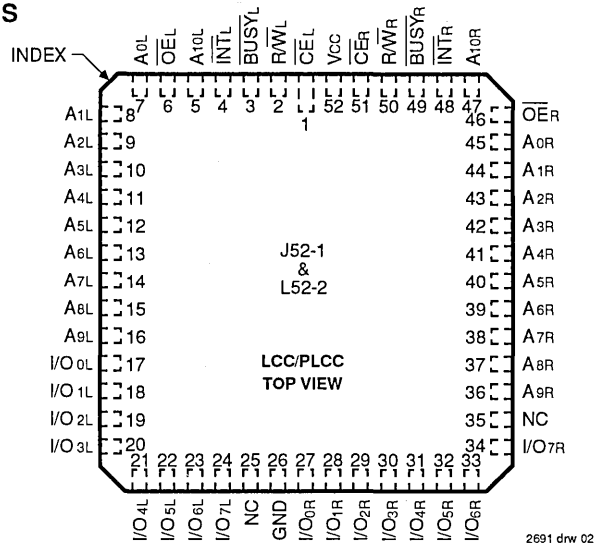


2691 drw 01

NOTES:
1. IDT71321 (MASTER): $\overline{BUSY}$ is open output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2691 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2691 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2691 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2691 tbl 03

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71321SA IDT71421SA Min.	IDT71321SA IDT71421SA Max.	IDT71321LA IDT71421LA Min.	IDT71321LA IDT71421LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$/$\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

1. At Vcc≤2.0V input leakages are undefined.

2691 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x20[2] 71421x20[2] Typ.	71321x20[2] 71421x20[2] Max.	71321x25/30 71421x25/30 Typ.	71321x25/30 71421x25/30 Max.	71321x35 71421x35 Typ.	71321x35 71421x35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	—	—	125/125	300/295	125	290	mA
				LA	—	—	125/125	240/235	125	230	
			Com'l.	SA	125	265	125/125	260/255	75	195	
				LA	125	215	125/125	210/205	75	155	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	—	—	30/30	80/80	30	80	mA
				LA	—	—	30/30	60/60	30	60	
			Com'l.	SA	30	65	30/30	65/65	25	65	
				LA	30	45	30/30	45/45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	80/80	195/190	80	185	mA
				LA	—	—	80/80	160/155	80	150	
			Com'l.	SA	80	180	80/80	175/170	40	130	
				LA	80	145	80/80	140/135	40	95	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	—	—	1.0/1.0	30/30	1.0	30	mA
				LA	—	—	0.2/0.2	10/10	0.2	10	
			Com'l.	SA	1.0	15	1.0/1.0	15/15	1.0	15	
				LA	0.2	5	0.2/0.2	5/5	0.2	4.0	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	—	—	70/70	185/180	70	175	mA
				LA	—	—	70/70	150/145	70	140	
			Com'l.	SA	70	175	70/70	170/165	40	115	
				LA	70	140	70/70	135/130	35	90	

2691 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71321x45 71421x45 Typ.	71321x45 71421x45 Max.	71321x55 71421x55 Typ.	71321x55 71421x55 Max.	71321x70[3] 71421x70[3] Typ.	71321x70[3] 71421x70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	SA	75	230	65	230	65	225	mA
				LA	75	185	65	185	65	180	
			Com'l.	SA	75	190	65	180	—	—	
				LA	75	145	65	140	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}[4]	Mil.	SA	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	55	
			Com'l.	SA	25	65	25	65	—	—	
				LA	25	45	25	45	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	135	40	135	40	135	mA
				LA	40	110	40	110	40	110	
			Com'l.	SA	40	120	40	115	—	—	
				LA	40	85	40	85	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	Mil.	SA	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	—	—	
				LA	0.2	4.0	0.2	4.0	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	SA	40	125	40	120	40	110	mA
				LA	35	95	35	90	35	80	
			Com'l.	SA	40	115	40	100	—	—	
				LA	35	80	35	75	—	—	

2691 tbl 06

NOTES:
1. "x" in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC} = 5V, T_A = +25°C for Typ.

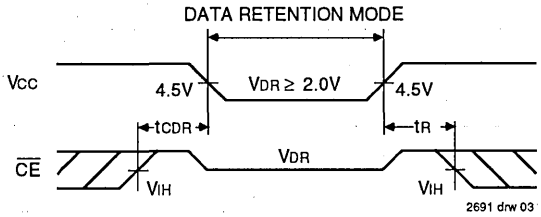
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Condition		IDT71321LA/IDT71421LA Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	—	0	V
I_{CCDR}	Data Retention Current		MIL.	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2691 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2691 tbl 08

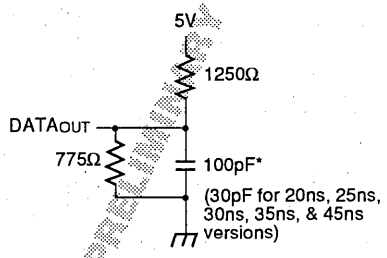


Figure 1. Output Load

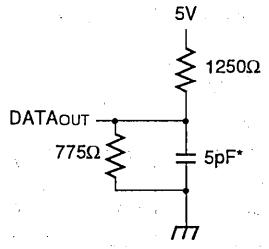


Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)

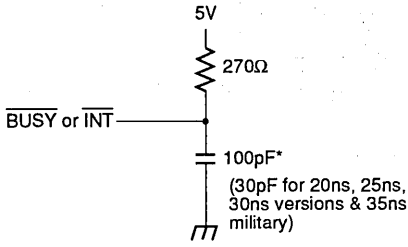


Figure 3. $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

2691 drw 04

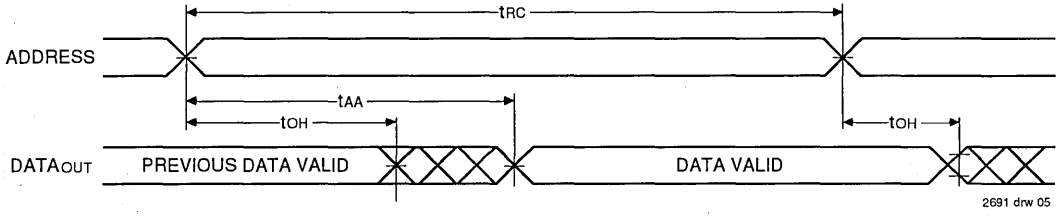
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	71321x20 (2) 71421x20 (2) Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70(3) 71421x70(3) Min.	Max.	Unit
Read Cycle														
tRC	Read Cycle Time	20	—	25/30	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	20	—	25/30	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	10	—	12/15	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0/0	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10/12	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0/0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50/50	—	50	—	50	—	50	—	50	ns

2691 tbl 09

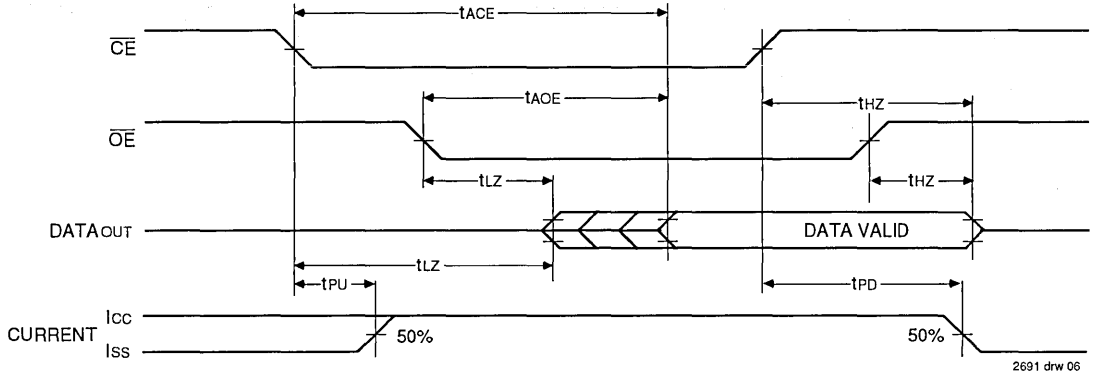
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1,2,4)



2691 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2691 drw 06

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	71321x20 [2] 71421x20 [2] Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	20	—	25/30	—	35	—	ns
tEW	Chip Enable to End of Write	15	—	20/25	—	30	—	ns
tAW	Address Valid to End of Write	15	—	20/25	—	30	—	ns
tAS	Address Set-up Time	0	—	0/0	—	0	—	ns
tWP	Write Pulse Width [6]	15	—	20/25	—	30	—	ns
tWR	Write Recovery Time	0	—	0/0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12/15	—	20	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10/12	—	15	ns
tDH	Data Hold Time	0	—	0/0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	8	—	10/12	—	15	ns
tOW	Output Active From End of Write[1,4]	0	—	0/0	—	0	—	ns

2691 tbl 10

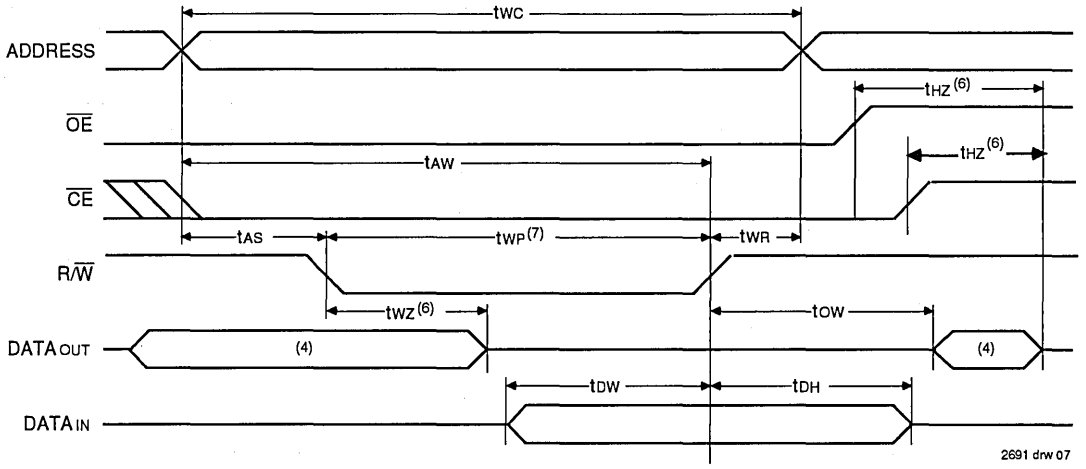
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7] (CONTINUED)

Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70[3] 71421x70[3] Min.	Max.	Unit
Write Cycle								
tWC	Write Cycle Time[5]	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width [6]	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	30	—	ns
tHZ	Output High Z Time[1,4]	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	20	—	30	—	35	ns
tOW	Output Active From End of Write[1,4]	0	—	0	—	0	—	ns

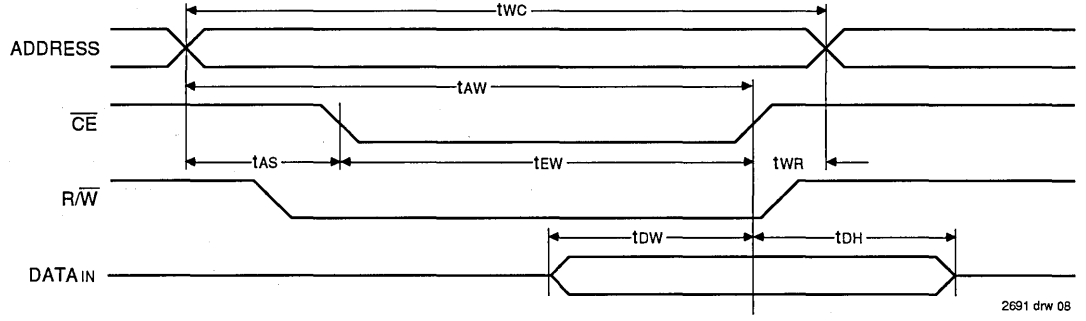
NOTES:
2691 tbl 11

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING (1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING (1,2,3,5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	71321x20 [1] 71421x20 [1] Min.	Max.	71321x25/30 71421x25/30 Min.	Max.	71321x35 71421x35 Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	BUSY Access Time to Address	—	20	—	25/30	—	35	ns
tBDA	BUSY Disable Time to Address	—	20	—	20/25	—	30	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20/25	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	20	—	20/25	—	25	ns
tWDD	Write Pulse to Data Delay [3]	—	50	—	50/50	—	60	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	35	—	35/35	—	35	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5/5	—	5	—	ns
tBDD	BUSY Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to BUSY Input [6]	0	—	0/0	—	0	—	ns
tWH	Write Hold After BUSY [7]	12	—	15/20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	50	—	50/50	—	60	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	35	—	35/35	—	35	ns

2691 tbl 12

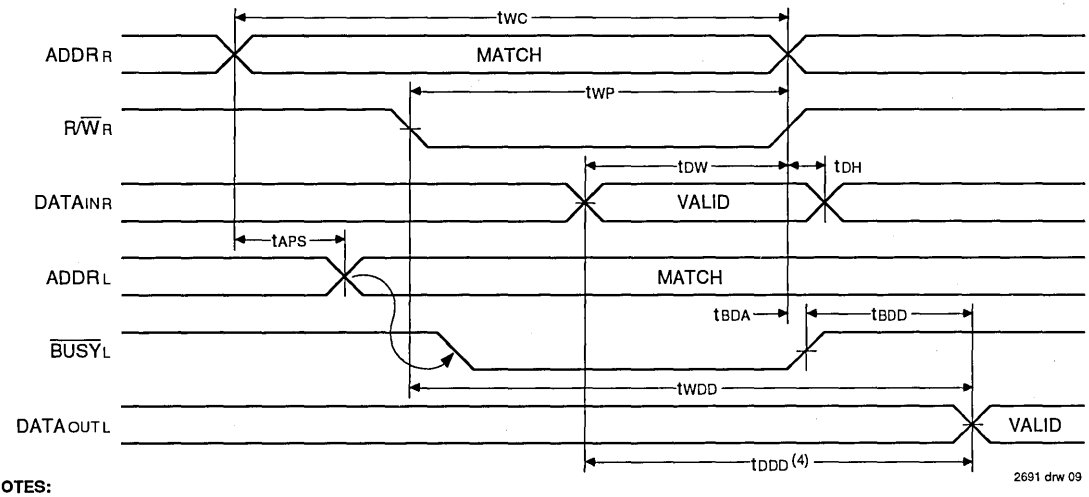
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8] (CONTINUED)

Symbol	Parameter	71321x45 71421x45 Min.	Max.	71321x55 71421x55 Min.	Max.	71321x70 [2] 71421x70 [2] Min.	Max.	Unit
Busy Timing (For Master IDT71321 Only)								
tBAA	BUSY Access Time to Address	—	35	—	45	—	45	ns
tBDA	BUSY Disable Time to Address	—	35	—	40	—	40	ns
tBAC	BUSY Access Time to Chip Enable	—	30	—	35	—	35	ns
tBDC	BUSY Disable Time to Chip Enable	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay [3]	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	45	—	55	—	70	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT71421 Only)								
tWB	Write to BUSY Input [6]	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY [7]	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	70	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	45	—	55	—	70	ns

2691 tbl 13

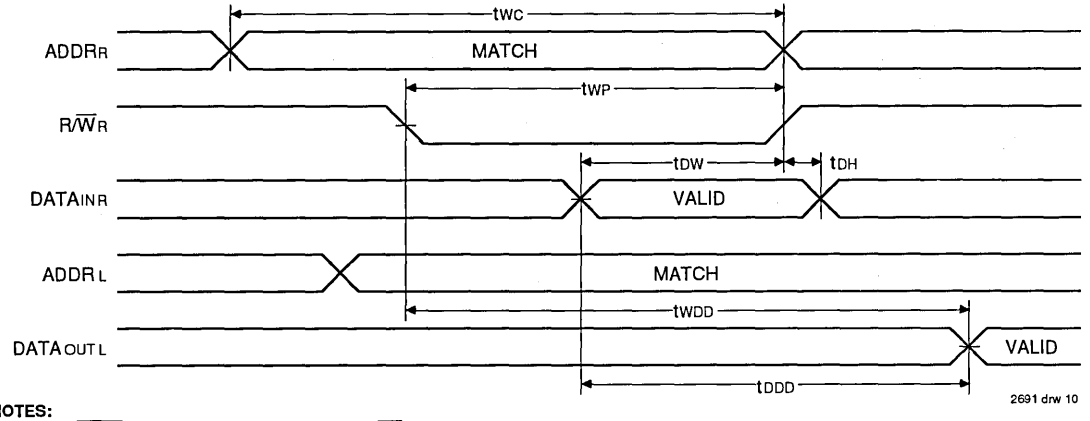
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (For Master IDT71321 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual).
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT71421 Only)".

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT71321)



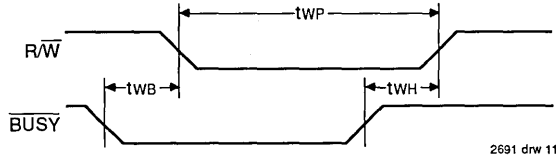
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT71421 ONLY)



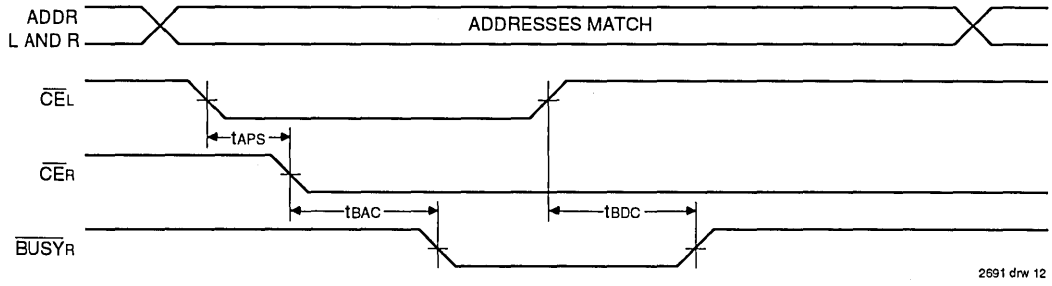
NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH BUSY (FOR SLAVE IDT71421)



TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT71321 ONLY)

$\overline{CE}_L$ VALID FIRST:



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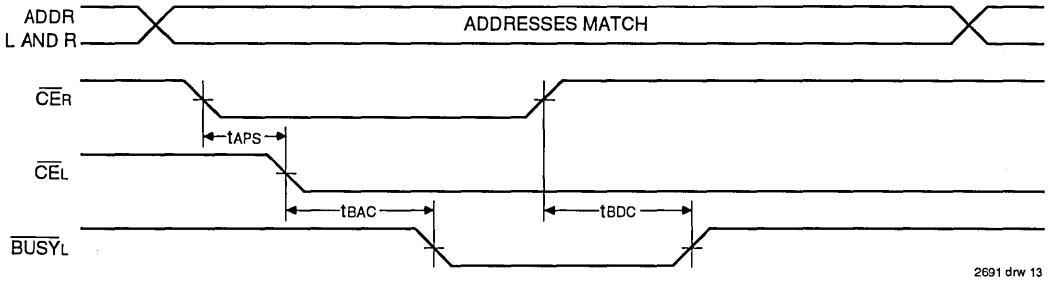
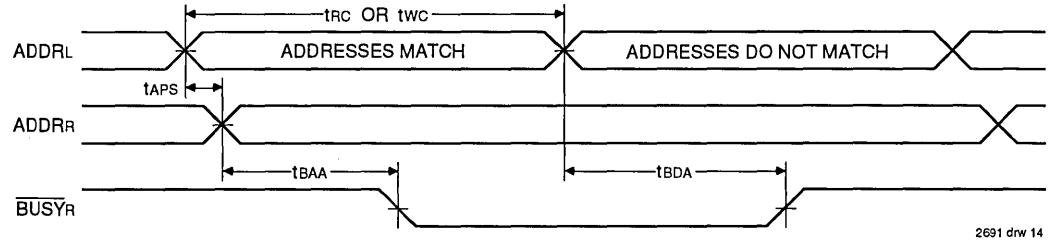
$\overline{CE}_R$ VALID FIRST:



2691 drw 13

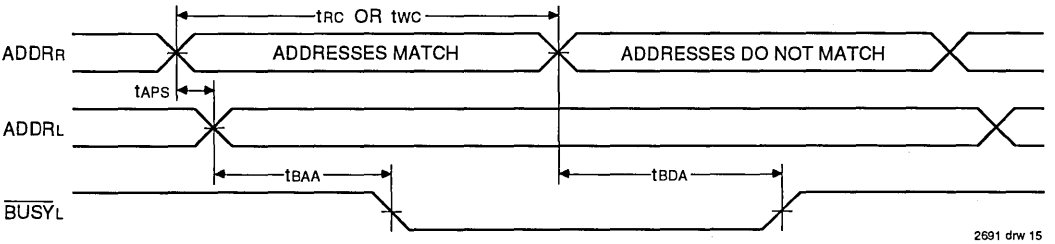
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT71321 ONLY)(1)

LEFT ADDRESS VALID FIRST:



2691 drw 14

RIGHT ADDRESS VALID FIRST:



2691 drw 15

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	71321SA/LA20(1) 71421SA/LA20(1) Min.	Max.	71321SA/LA25/30 71421SA/LA25/30 Min.	Max.	71321SA/LA35 71421SA/LA35 Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25/30	—	35	ns
tINR	Interrupt Reset Time	—	20	—	25/30	—	35	ns

2691 tbl 14

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (CONTINUED)

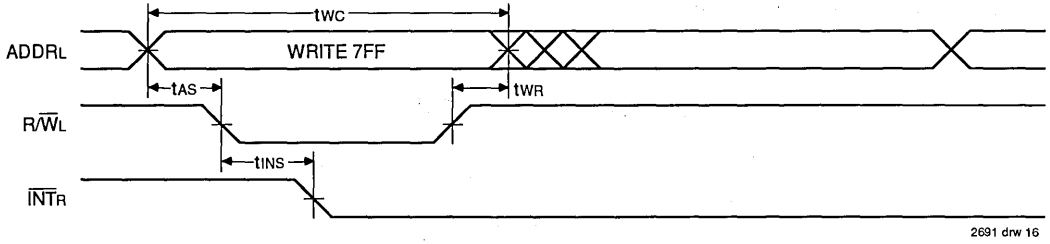
Symbol	Parameter	71321SA/LA45 71421SA/LA45 Min.	Max.	71321SA/LA55 71421SA/LA55 Min.	Max.	71321SA/LA70(2) 71421SA/LA70(2) Min.	Max.	Unit
Interrupt Timing								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	40	—	45	—	50	ns

2691 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

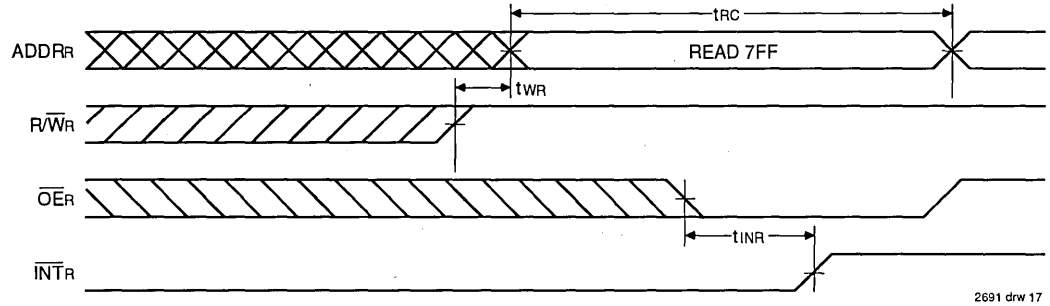
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS $\overline{INT}_R$:



2691 drw 16

RIGHT SIDE CLEARS $\overline{INT}_R$:

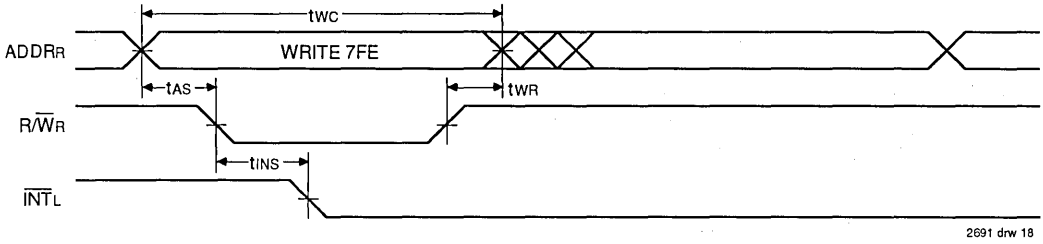


2691 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (HIGH) during power up.

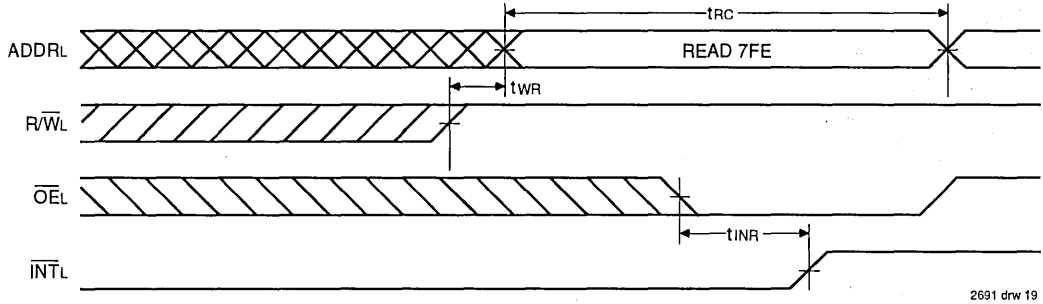
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

RIGHT SIDE SETS $\overline{INT}_L$:



2691 drw 18

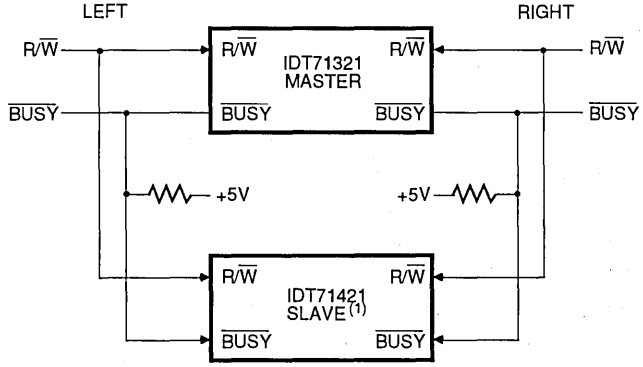
LEFT SIDE CLEARS $\overline{INT}_L$:



2691 drw 19

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
2. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (HIGH) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2691 drw 20

NOTE:
1. No arbitration in IDT71421 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT71421 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT71321/IDT71421 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$)is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag (INT_R) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE_L}$ and $\overline{CE_R}$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY_L}$ while another acitivates its $\overline{BUSY_R}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMS in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Disabled and in Power Down Mode ISB2 or ISB4
X	H	X	Z	CER = CEL = H, Power Down Mode, ISB1 or ISB3
L	L	X	DATAIN	Data on Port Written into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2691 tbl 16

NOTES:
1. AOL-A10L ≠ AOR-A10R
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see tWDD and tDDD timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2691 tbl 17

NOTE:
1. This parameter is determined by device characterization but is not 100% tested.

TABLE II – INTERRUPT FLAG(1, 4)

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	AOL-A10L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	AOL-A10R	$\overline{INT}$R	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}$R Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}$L Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

2691 tbl 18

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = H.
2. If $\overline{BUSY}$L = L, then NC.
3. If $\overline{BUSY}$R = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE.

TABLE III – ARBITRATION(1, 2)

Left Port		Right Port		Flags		
$\overline{CE}$L	AOL-A10L	$\overline{CE}$R	AOR-A10R	$\overline{BUSY}$L	$\overline{BUSY}$R	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ AOR-A10R	L	≠ AOL-A10L	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= AOR-A10R	LL5R	= AOL-A10L	H	L	L-Port Wins
RL5L	= AOR-A10R	RL5L	= AOL-A10L	L	H	R-Port Wins
LW5R	= AOR-A10R	LW5R	= AOL-A10L	H	L	Arbitration Resolved
LW5R	= AOR-A10R	LW5R	= AOL-A10L	L	H	Arbitration Resolved

2691 tbl 19

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7012

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT7012S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT7012L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asychronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit
- Battery backup operation — 2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is avalable, tested to military electrical specifications

DESCRIPTION:

The IDT7012 is a high-speed 2K x 9 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port location.

The IDT7012 provides two independent ports with separate control, address, and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

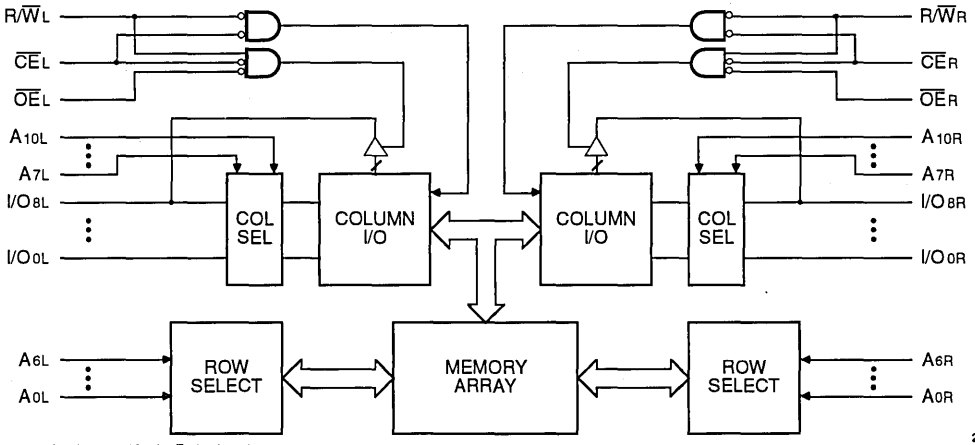
The IDT7012 utilizes a 9-bit wide data path to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7012 is packaged in 48-pin sidebrazed or plastic DIPs, 48-pin LCCs and 48-pin flatpacks. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

6

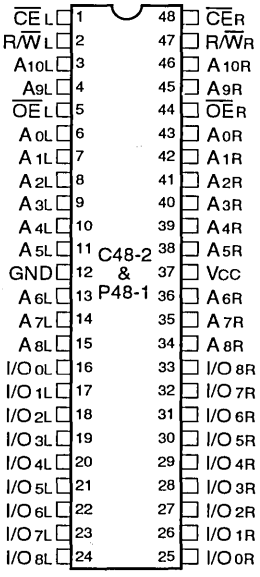
FUNCTIONAL BLOCK DIAGRAM



2653 drw 01

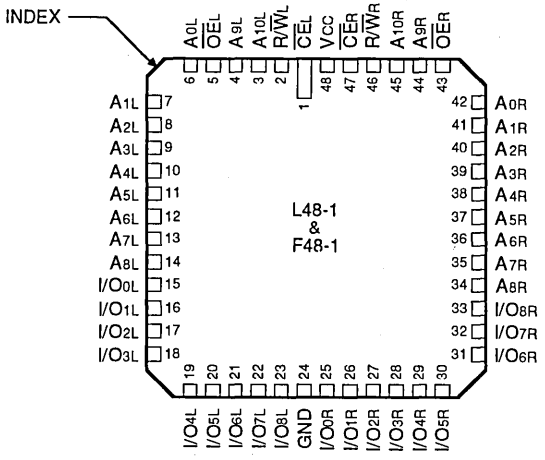
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2653 drw 02

DIP
TOP VIEW



2653 drw 03

LCC/FLATPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2653 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2653 tbl 13

NOTE:
1. This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2653 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	–	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

2653 tbl 03

NOTE:
1. VIL = –3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	7012S		7012L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2653 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7012 x 25[2]		7012 x 35		7012 x 45		7012 x 55		7012 x 70[3]		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	125	290	125	285	125	280	125	275	mA
				L	—	—	125	230	125	225	125	220	125	215	
			Com'l.	S	125	260	125	250	125	245	125	240	—	—	
				L	125	220	125	210	125	205	125	200	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil.	S	—	—	30	80	30	80	30	80	30	80	mA
				L	—	—	30	60	30	60	30	60	30	60	
			Com'l.	S	30	65	30	65	30	65	30	65	—	—	
				L	30	45	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	80	185	80	180	80	175	80	170	mA
				L	—	—	80	150	80	145	80	140	80	135	
			Com'l.	S	80	175	80	165	80	160	80	155	—	—	
				L	80	145	80	135	80	130	80	125	—	—	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	70	175	70	170	70	165	70	160	mA
				L	—	—	70	140	70	135	70	130	70	125	
			Com'l.	S	70	170	70	160	70	155	70	150	—	—	
				L	70	140	70	130	70	125	70	120	—	—	

2653 tbl 05

NOTES:

1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At V_{CC}≤2.0V input leakages are undefined.

6

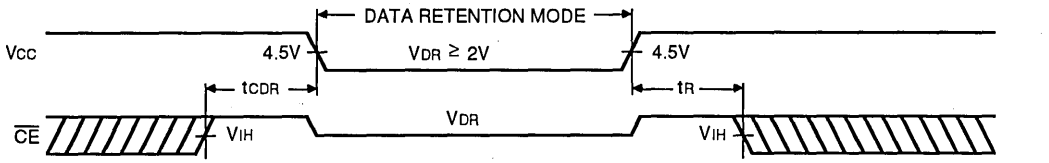
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		7012L Min.	7012L Typ.[1]	7012L Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$		2	—	—	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

2653 tbl 06

DATA RETENTION WAVEFORM

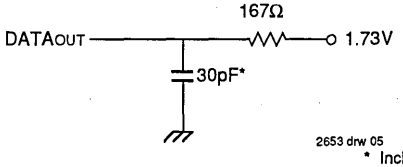


2653 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

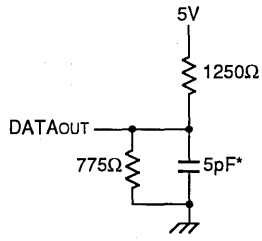
2653 tbl 07



2653 drw 05

* Including scope and jig.

Figure 1. Equivalent Output Load



2653 drw 06

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

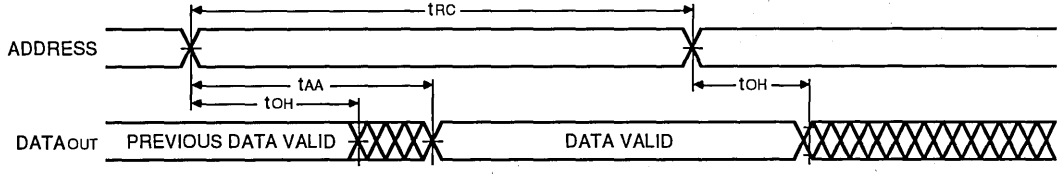
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	7012 x 25(2)		7012 x 35		7012 x 45		7012 x 55		7012 x 70(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max	
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time(1,4)	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power-Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power-Down Time(4)	—	50	—	50	—	50	—	50	—	50	ns

2653 tbl 08

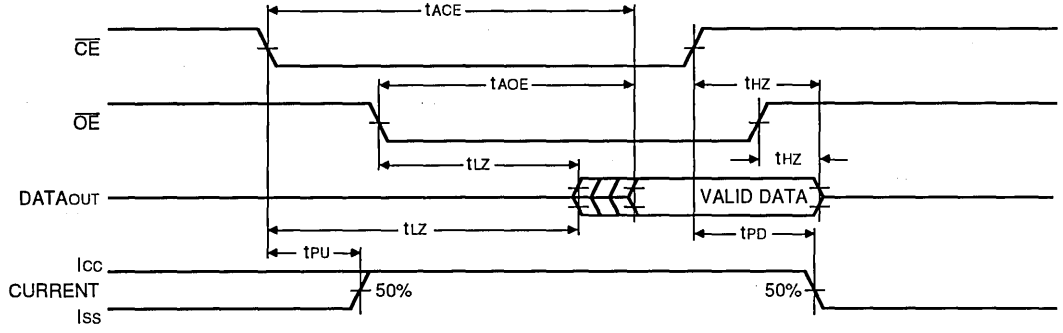
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1, 2, 4)



2653 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1, 3)



2653 drw 10

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

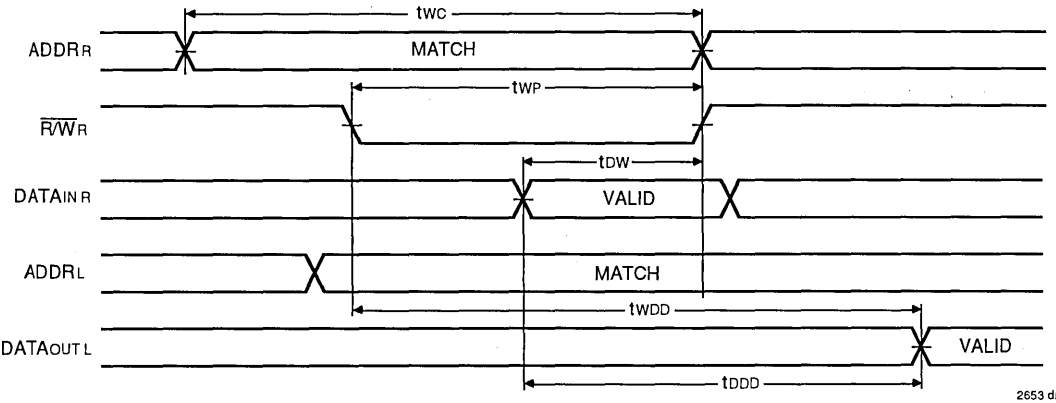
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	7012 x 25(2)		7012 x 35		7012 x 45		7012 x 55		7012 x 70(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(5)	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write(1,4)	0	—	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay	—	35	—	45	—	55	—	65	—	80	ns

2653 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
6. "x" in part numbers indicates power rating (S or L).

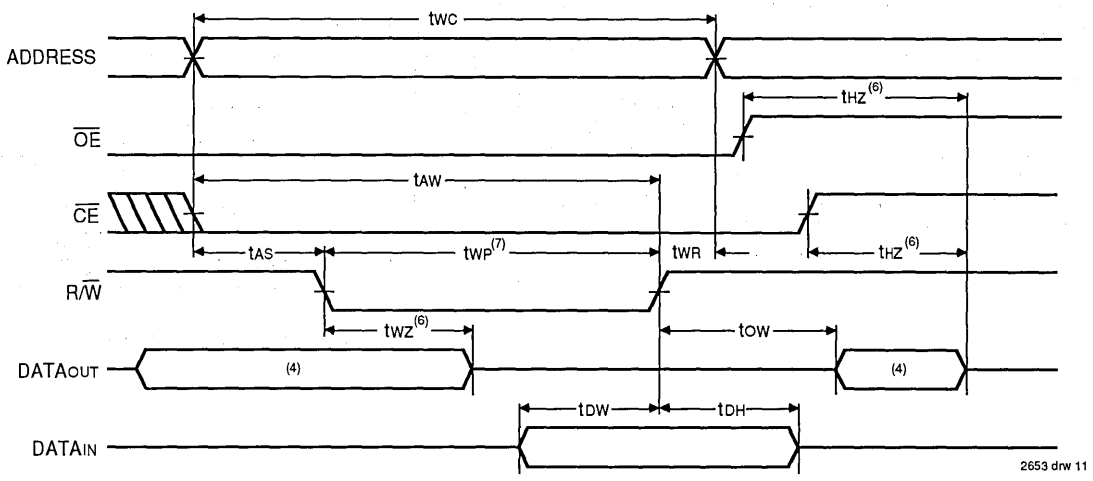
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1)



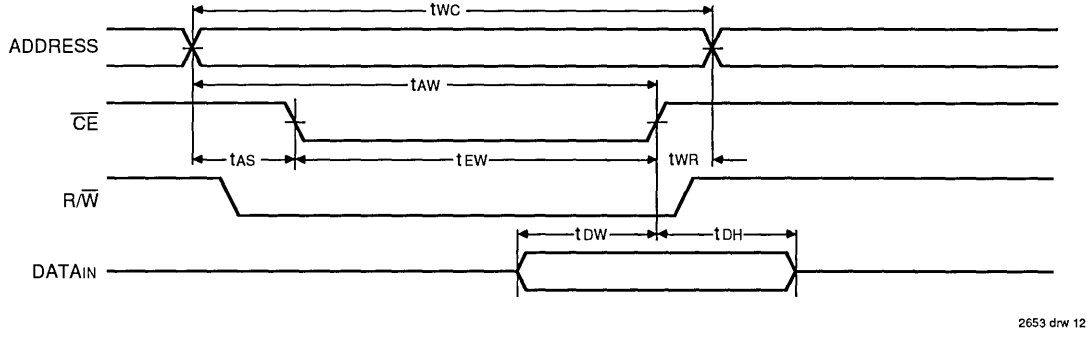
2653 drw 14

NOTE:
1. Write cycle parameters should be adhered to in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

FUNCTIONAL DESCRIPTION

The IDT7012 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the truth table below.

TRUTH TABLE NON-CONTENTION READ/WRITE CONTROL

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES: 2653 tbl 11

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

PRELIMINARY
IDT70121S/L
IDT70125S/L

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70121/70125S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT70121/70125L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

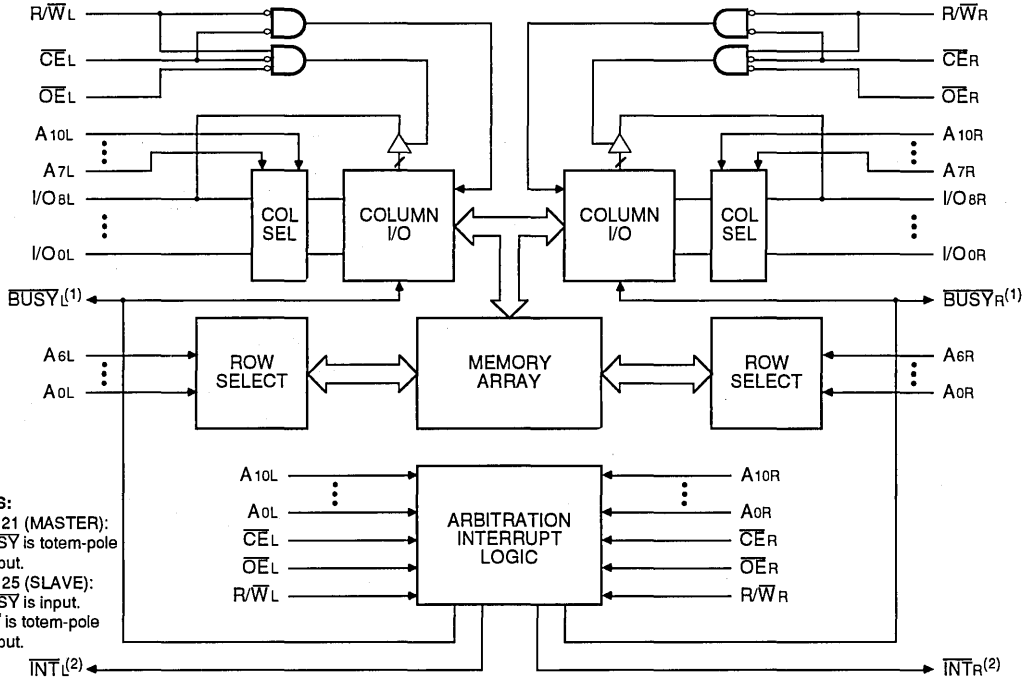
DESCRIPTION:

The IDT70121/IDT70125 are high-speed 2K x 9 dual-port static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70125 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is totem-pole output.
   70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.

CEMOS is a trademark of Integrated Device Technology, Inc.

2654 drw 01

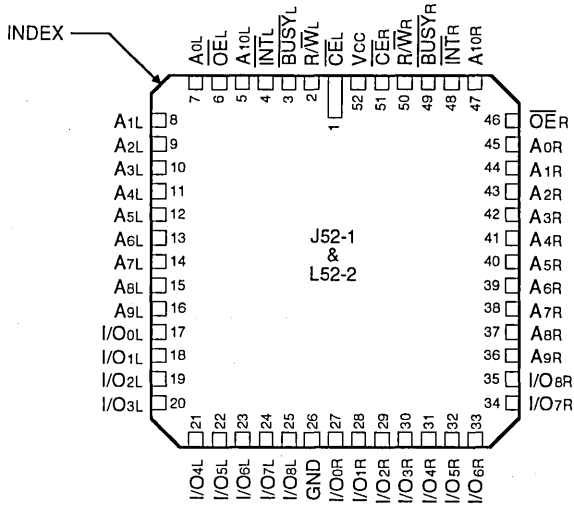
DESCRIPTION (Continued):

applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70121/IDT70125 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS



2654 drw 02

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2654 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2654 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	–	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2654 tbl 03

1. V_{IL} = –3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	70121S 70125S Min.	70121S 70125S Max.	70121L 70125L Min.	70121L 70125L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2654 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121 x 25[2] 70125 x 25[2] Typ.	70121 x 25[2] 70125 x 25[2] Max.	70121 x 35 70125 x 35 Typ.	70121 x 35 70125 x 35 Max.	70121 x 45 70125 x 45 Typ.	70121 x 45 70125 x 45 Max.	70121 x 55 70125 x 55 Typ.	70121 x 55 70125 x 55 Max.	70121 x 70[3] 70125 x 70[3] Typ.	70121 x 70[3] 70125 x 70[3] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	125	290	125	285	125	280	125	275	mA
				L	—	—	125	230	125	225	125	220	125	215	
			Com'l.	S	125	260	125	250	125	245	125	240	—	—	
				L	125	220	125	210	125	205	125	200	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	Mil.	S	—	—	30	80	30	80	30	80	30	80	mA
				L	—	—	30	60	30	60	30	60	30	60	
			Com'l.	S	30	65	30	65	30	65	30	65	—	—	
				L	30	45	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	80	185	80	180	80	175	80	170	mA
				L	—	—	80	150	80	145	80	140	80	135	
			Com'l.	S	80	175	80	165	80	160	40	155	—	—	
				L	80	145	80	135	80	130	40	125	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \ge V_{CC}$ – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	Mil.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	70	175	70	170	70	165	70	160	mA
				L	—	—	70	140	70	135	70	130	70	125	
			Com'l.	S	70	170	70	160	70	155	70	150	—	—	
				L	70	140	70	130	70	125	70	120	—	—	

2654 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At $V_{CC} \le$2.0V input leakages are undefined.

6

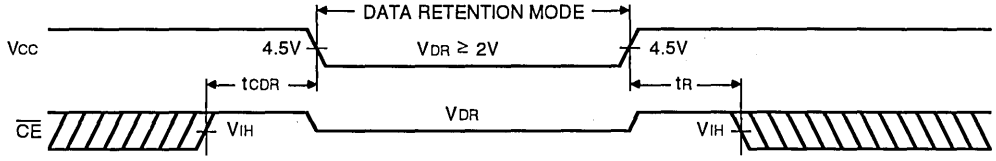
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		70121L/70125L Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2654 tbl 06

1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

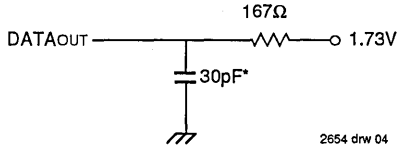


2654 drw 03

AC TEST CONDITIONS

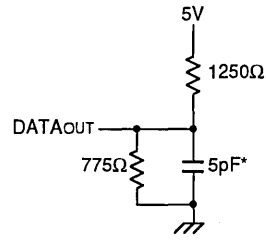
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2654 tbl 07



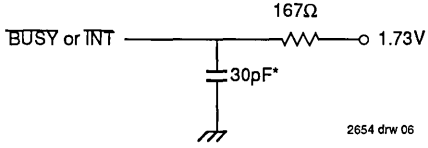
2654 drw 04

Figure 1. Equivalent Output Load



2654 drw 05

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})



2654 drw 06

Figure 3. Equivalent $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

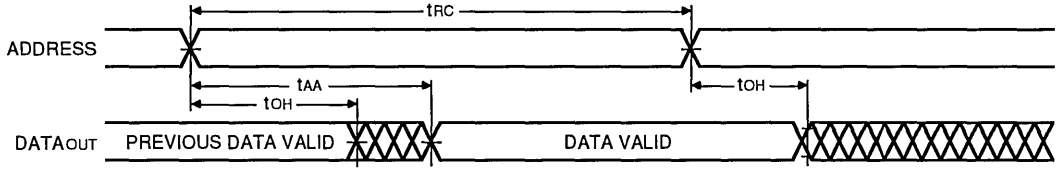
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	70121 x 25[2] 70125 x 25[2] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[3] 70125 x 70[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power-Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power-Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

NOTES:
2654 tbl 08

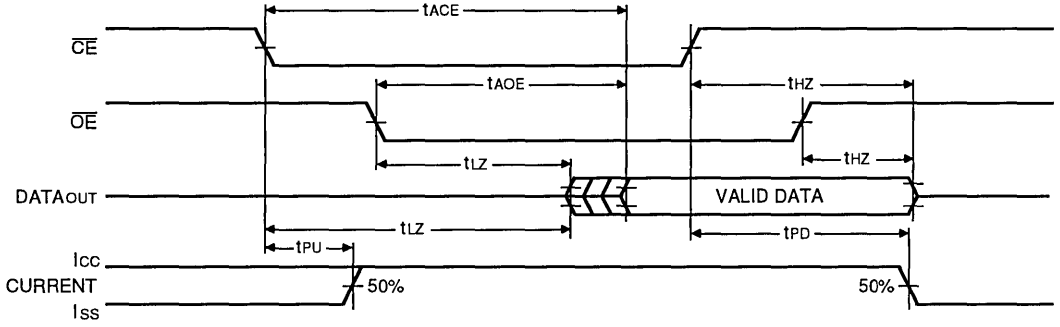
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



2654 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1,3]



NOTES:
2654 drw 09

1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to, or coincident with, CE transition low.
4. OE = VIL.

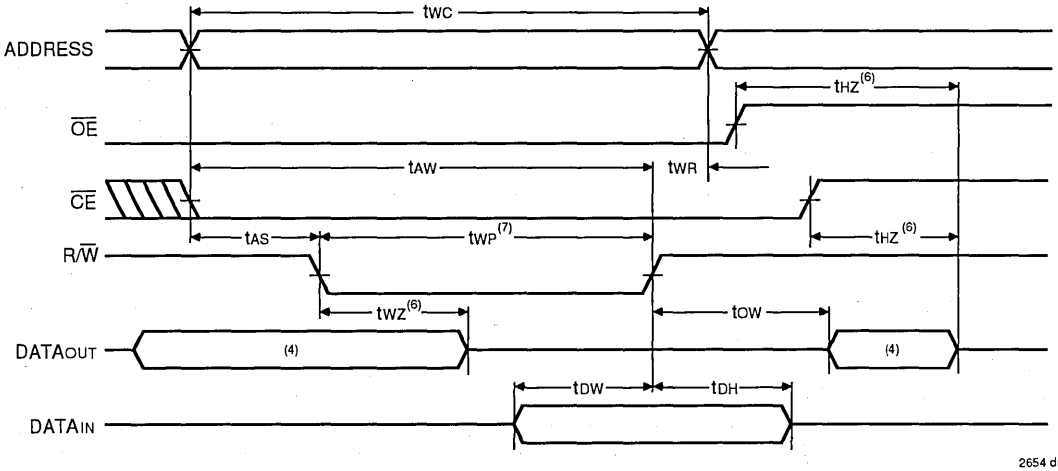
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	70121 x 25[2] 70125 x 25[2] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[3] 70125 x 70[3] Min.	Max.	Unit
Write Cycle												
t_{WC}	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[7]	20	—	30	—	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
t_{HZ}	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	—	10	—	15	—	20	—	30	—	35	ns
t_{OW}	Output Active from End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

2654 tbl 09

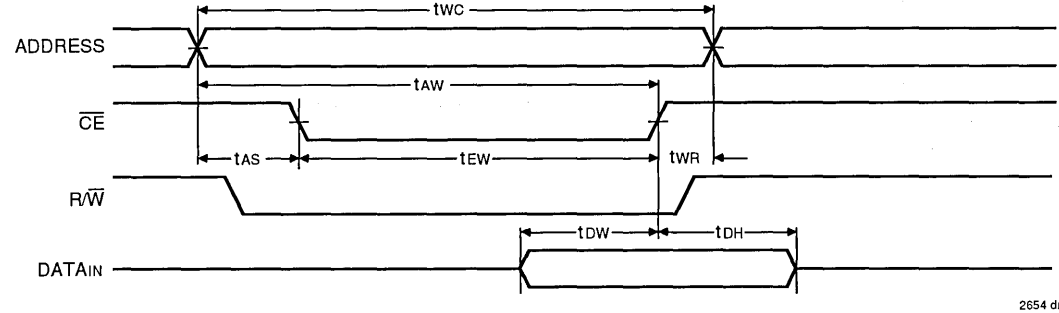
NOTES:
1. Transition is measured ±500mV from low or high voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. "x" in part numbers indicates power rating (S or L).
7. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,2,3,7)



2654 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,2,3,5)



2654 drw 11

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

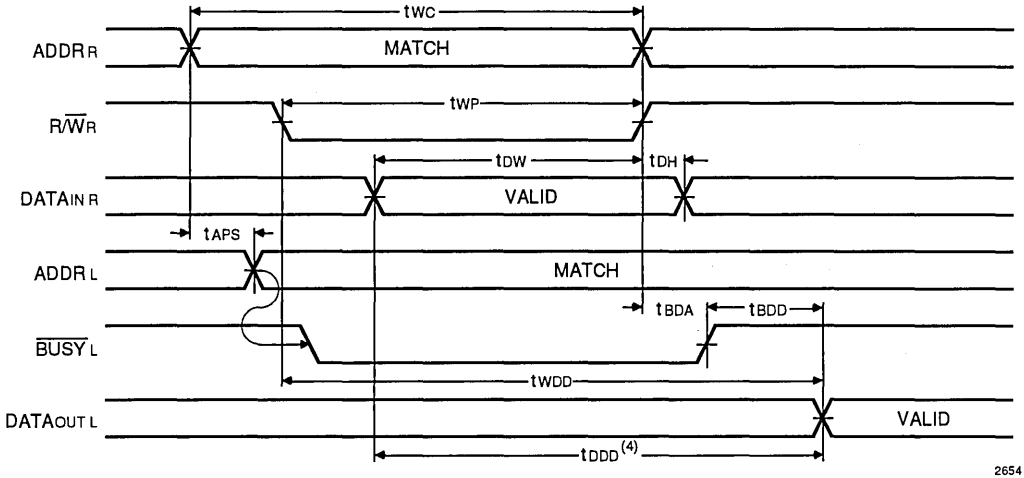
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Busy Timing (For Master IDT70121 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT70125 Only)												
tWB	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

2654 tbl 10

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT70121 Only)."
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
6. To ensure that a write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ Port-to-Port Delay (For SLAVE IDT70125 Only)."

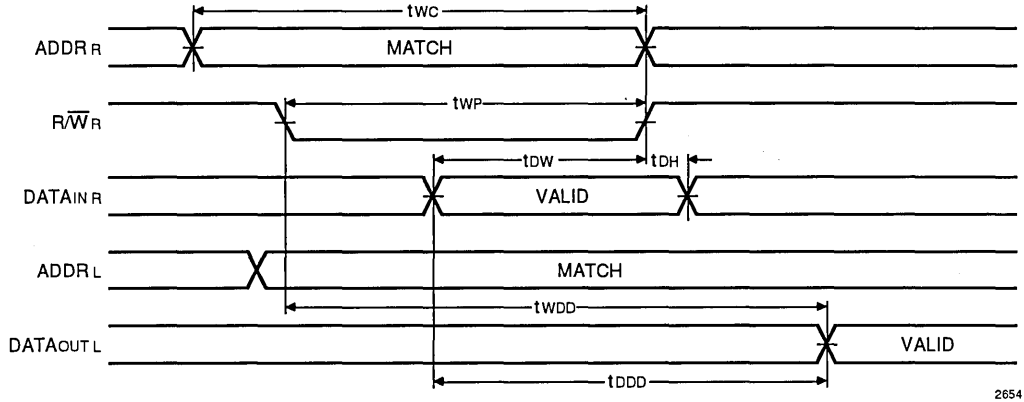
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$(1,2,3) (FOR MASTER IDT70121)



2654 drw 12

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

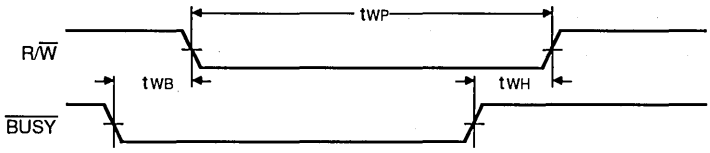
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1,2,3) (FOR SLAVE IDT70125 ONLY)



2654 drw 13

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

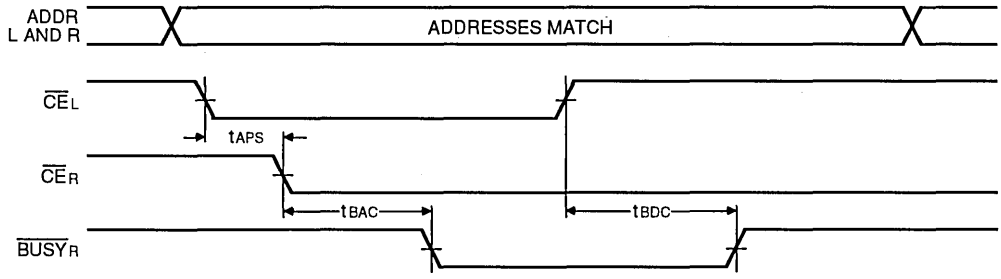
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (FOR SLAVE IDT70125 ONLY)



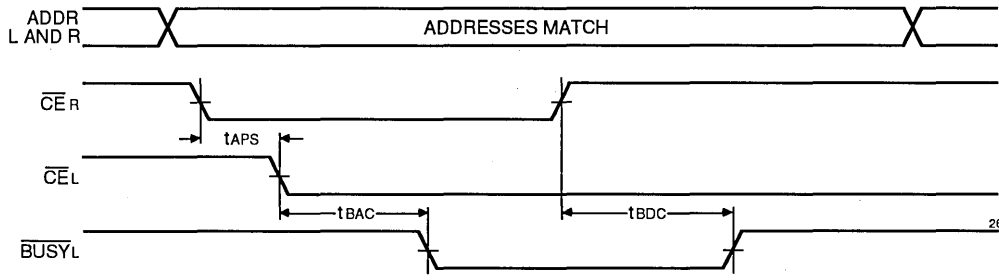
2654 drw 14

TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT70121 ONLY)

$\overline{CE}_L$ VALID FIRST:



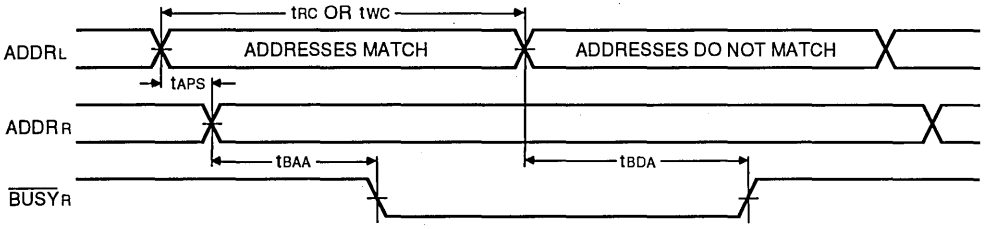
$\overline{CE}_R$ VALID FIRST:



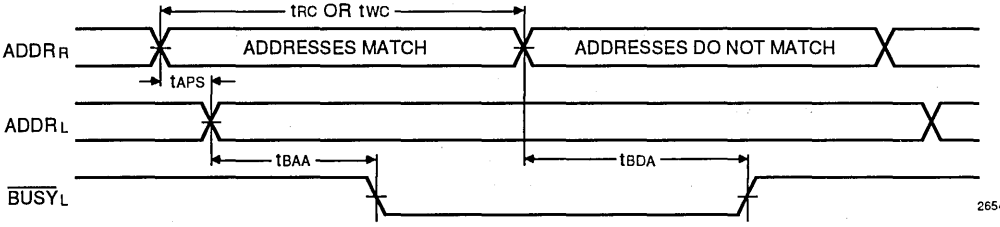
2654 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT70121 ONLY)[1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



2654 drw 16

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	35	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	25	—	35	—	40	—	45	—	50	ns

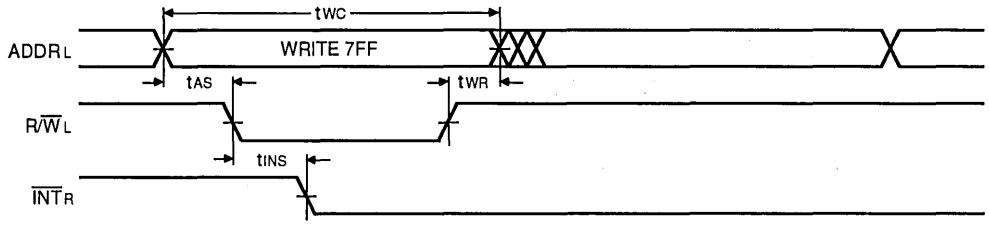
NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. "X" in part numbers indicates power rating (S or L).

2654 tbl 11

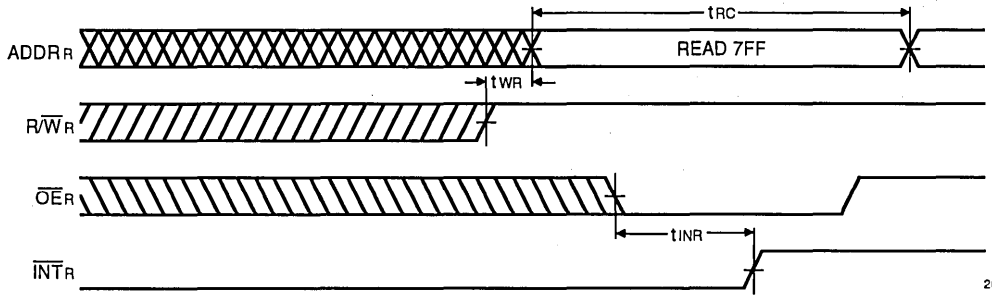
6

TIMING WAVEFORM OF INTERRUPT MODE[1,2]

LEFT SIDE SETS $\overline{INT}_R$:



RIGHT SIDE CLEARS $\overline{INT}_R$:

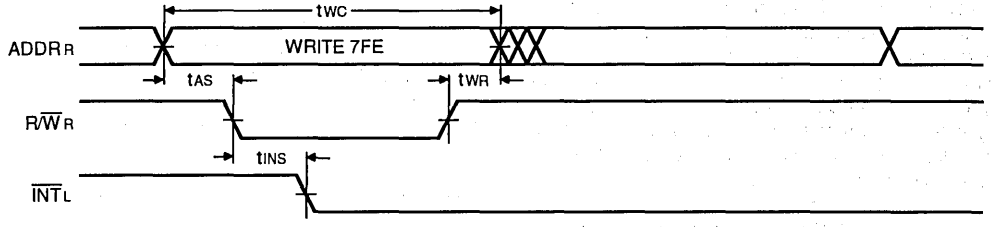


2654 drw 17

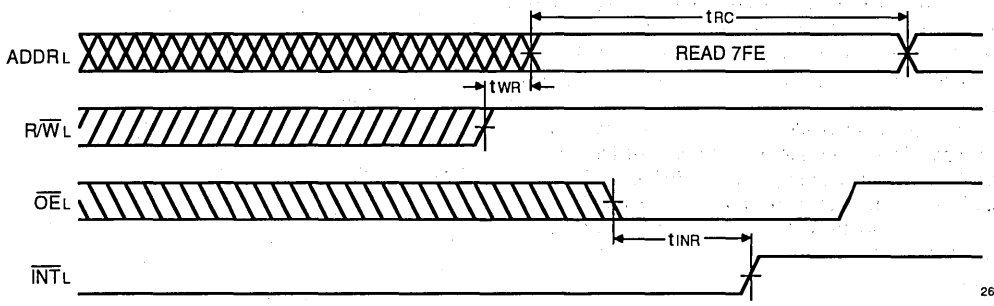
NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power-up.

TIMING WAVEFORM OF INTERRUPT MODE[1,2]

RIGHT SIDE SETS $\overline{INT}_L$:



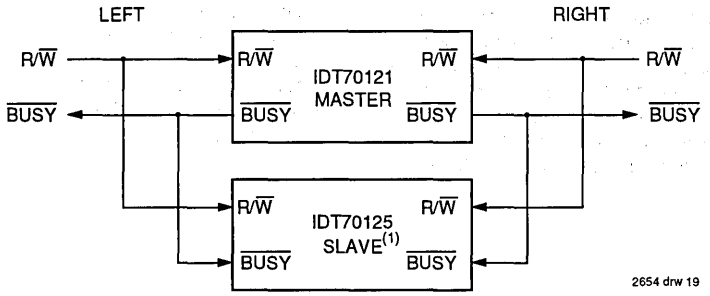
LEFT SIDE CLEARS $\overline{INT}_L$:



2654 drw 18

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power-up.

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2654 drw 19

NOTE:
1. No arbitration in IDT70125 (SLAVE). $\overline{BUSY}_{IN}$ inhibits write in IDT70125 (SLAVE).

6

FUNCTIONAL DESCRIPTION

The IDT70121/IDT70125 provide two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE_R}$ = $\overline{CE_L}$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2654 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

2654 tbl 13

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{10L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{10R}$	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2654 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III. ARBITRATION[2]

Left Port		Right Port		Flags[1]		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2654 tbl 15

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and right $\overline{CE}$ = LOW within 5ns of each other.

6

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

PRELIMINARY
IDT7133SA/LA
IDT7143SA/LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70/90ns (max.)
  - — Commercial: 25/35/45/55/70/90ns (max.)
- Low-power operation
  - — IDT7133/43SA
    Active: 500 mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic PGA, Flatpack, and PLCC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

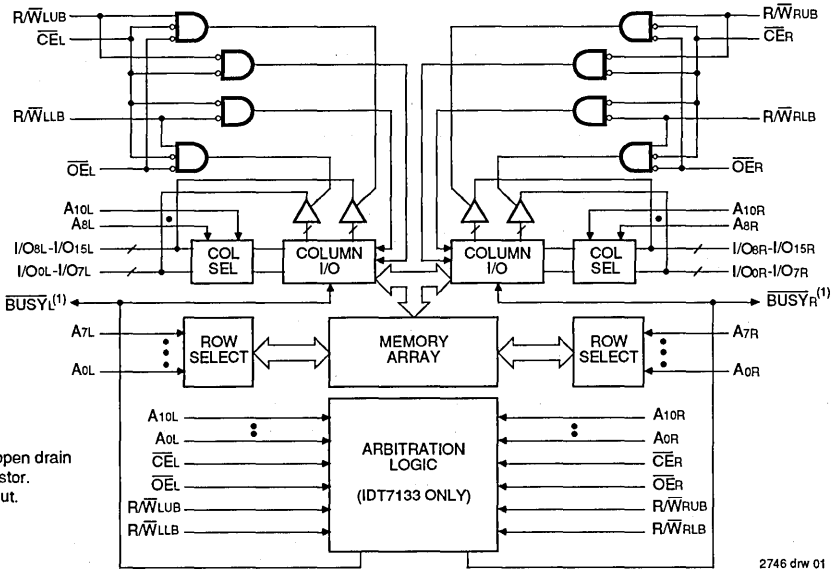
The IDT7133/7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 500mW of power at maximum access times as fast as 25ns. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, and 68-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2746 drw 01

NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

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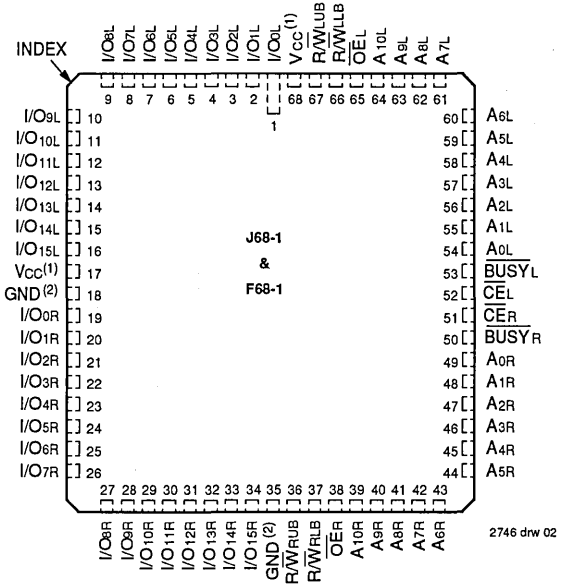
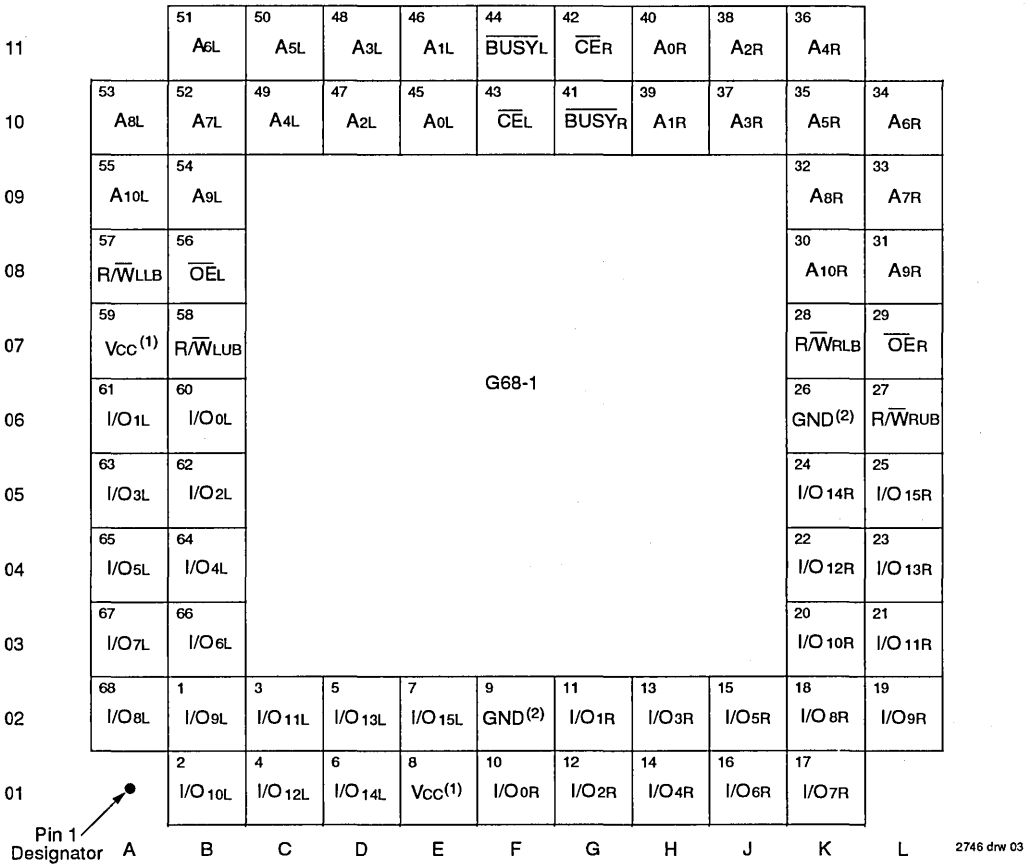
PIN CONFIGURATIONS



PLCC/FLATPACK
TOP VIEW

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte

6



2746 drw 03

PGA
TOP VIEW

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2746 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	$V_{I/O}$ = 0V	11	pF

NOTE: 2746 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2746 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2746 tbl 04

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133SA IDT7143SA		IDT7133LA IDT7143LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[6]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2746 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7133x25[1] 7143x25[1]		7133x35 7143x35		7133x45 7143x45		7133x55 7143x55		7133x70/90 7143x70/90		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[4]	MIL.	S	—	—	—	325	—	320	—	315	—	310	mA
				L	—	—	—	295	—	290	—	285	—	280	
			COM'L.	S	—	300	—	295	—	290	—	285	—	280	
				L	—	270	—	265	—	260	—	255	—	250	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4]	MIL.	S	—	—	25	85	25	80	25	80	25	75	mA
				L	—	—	25	75	25	70	25	70	25	65	
			COM'L.	S	25	80	25	75	25	75	25	70	25	70	
				L	25	70	25	65	25	65	25	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[4] Active Port Outputs Open	MIL.	S	—	—	—	220	—	210	—	210	—	200	mA
				L	—	—	—	200	—	190	—	190	—	180	
			COM'L.	S	—	200	—	190	—	190	—	180	—	180	
				L	—	180	—	170	—	170	—	160	—	160	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1	30	1	30	1	30	1	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[5]	COM'L.	S	1	15	1	15	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or	MIL.	S	—	—	—	210	—	200	—	200	—	190	mA
				L	—	—	—	190	—	180	—	180	—	170	
		$V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	COM'L.	S	—	190	—	180	—	180	—	170	—	170	
				L	—	170	—	160	—	160	—	150	—	150	

NOTES:

2746 tbl 06

1. 0°C to +70°C temperature range only.
2. V_{CC} = 5V, T_A = +25°C.
3. "x" in part number indicates power rating (SA or LA).
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. At $V_{CC} \le$2.0V input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

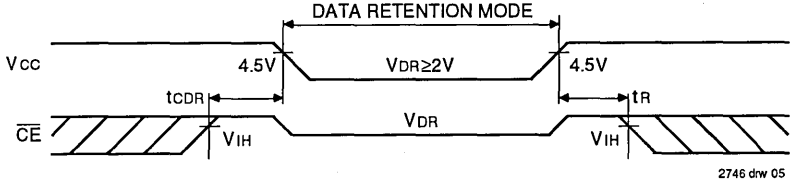
Symbol	Parameter	Test Condition		IDT7133LA/IDT7143LA Min.	IDT7133LA/IDT7143LA Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	ns

NOTES:

2746 tbl 07

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2746 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2746 tbl 08

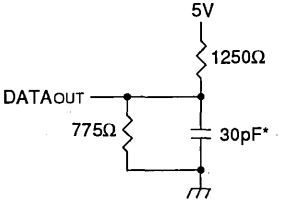


Figure 1. Output Load

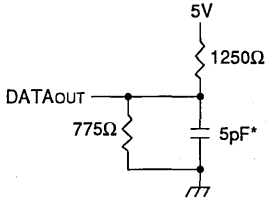


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

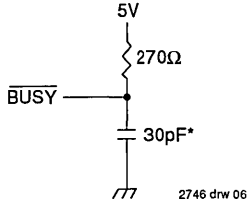


Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

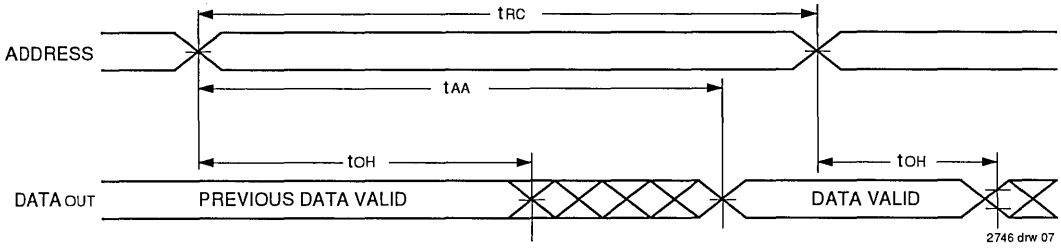
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	IDT7133x25[2] IDT7143x25[2] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70/90 IDT7143x70/90 Min.	Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70/90	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70/90	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70/90	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40/40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0/0	—	ns
tLZ	Output Low Z Time[1, 3]	0	—	0	—	0	—	5	—	5/5	—	ns
tHZ	Output High Z Time[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	0	—	0/0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50	—	50	—	50/50	ns

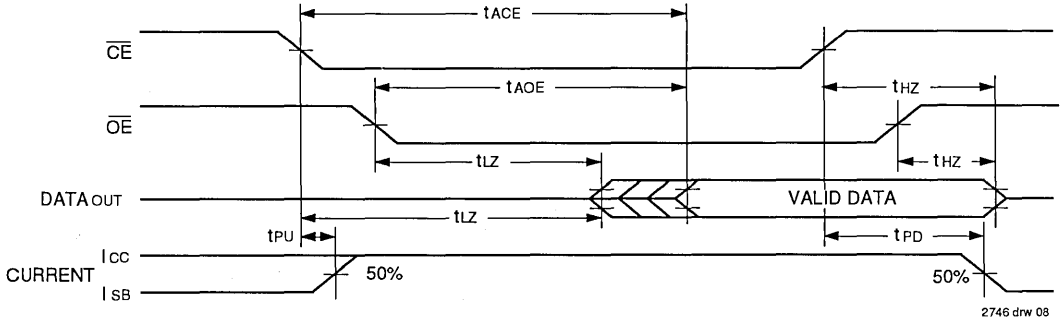
2746 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. "x" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x25[2] IDT7143x25[2] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70/90 IDT7143x70/90 Min.	Max.	Unit
WRITE CYCLE												
tWC	Write Cycle Time[4]	25	—	35	—	45	—	55	—	70/90	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	40	—	50/50	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	40	—	50/50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0/0	—	ns
tWP	Write Pulse Width[6]	20	—	25	—	30	—	40	—	50/50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0/0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	30/30	—	ns
tHZ	Output High Z Time[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
tDH	Data Hold Time[5]	0	—	0	—	5	—	5	—	5/5	—	ns
tWZ	Write Enable to Output in High Z[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
tOW	Output Active from End of Write[1, 3, 5]	0	—	0	—	5	—	5	—	5/5	—	ns

NOTES: 2746 tbl 10

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, tWC = tBAA + tWR + tWP.
5. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
7. "x" in part number indicates power rating (SA or LA).

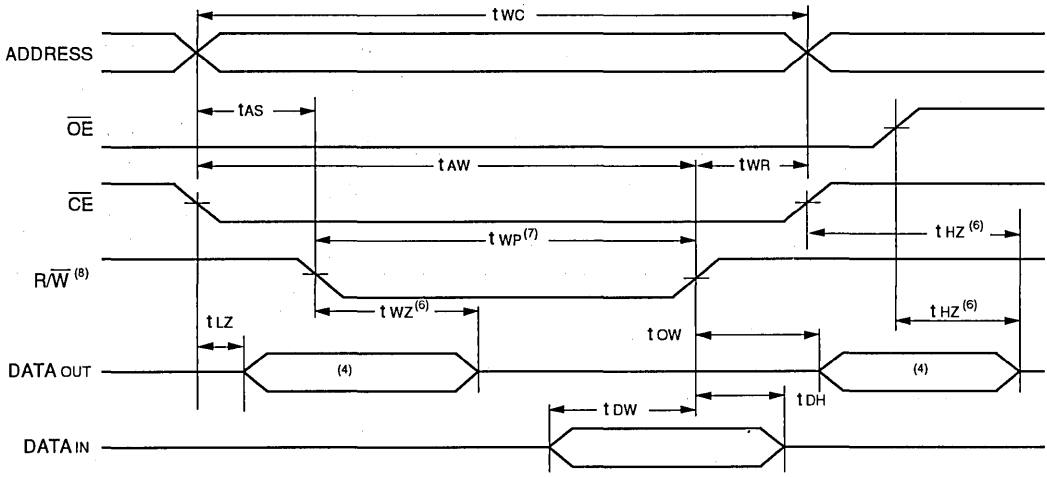
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[8]

Symbol	Parameter	IDT7133x25[1] IDT7143x25[1] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70/90 IDT7143x70/90 Min.	Max.	Unit
BUSY TIMING (For MASTER IDT7133)												
tBAA	$\overline{BUSY}$ Access Time from Address	—	25	—	35	—	45	—	50	—	55/55	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	—	20	—	30	—	40	—	40	—	45/45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	25	—	30	—	35	—	35/35	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	25	—	30	—	30/30	ns
tWDD	Write Pulse to Data Delay[2]	—	50	—	60	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	45	—	55	—	55	—	70/70	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	—	Note 3	—	Note 3	ns
tAPS	Arbitration Priority Set Up Time[4]	5	—	5	—	5	—	5	—	5/5	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)												
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	—	—	0/0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	20	—	25	—	30	—	30	—	30/30	—	ns
tWDD	Write Pulse to Data Delay[7]	—	50	—	60	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay[7]	—	35	—	45	—	55	—	55	—	70/70	ns

NOTES: 2746 tbl 11

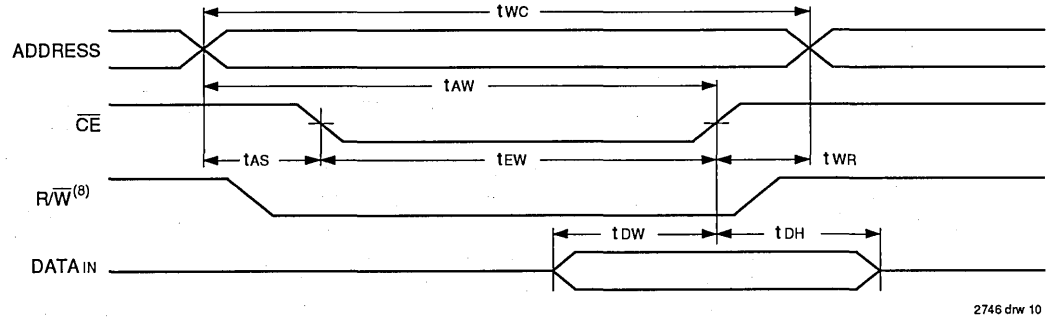
1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH BUSY (For Master IDT7133)"
3. tBDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (For Slave IDT7143)"
8. "x" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 3, 7)



2746 drw 09

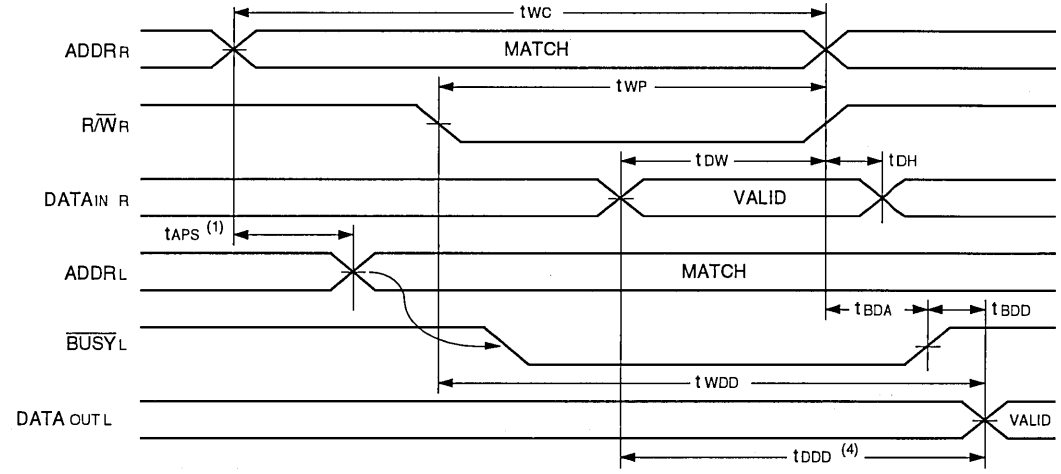
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2, 3, 5)



2746 drw 10

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. R/$\overline{W}$ for either upper or lower byte.

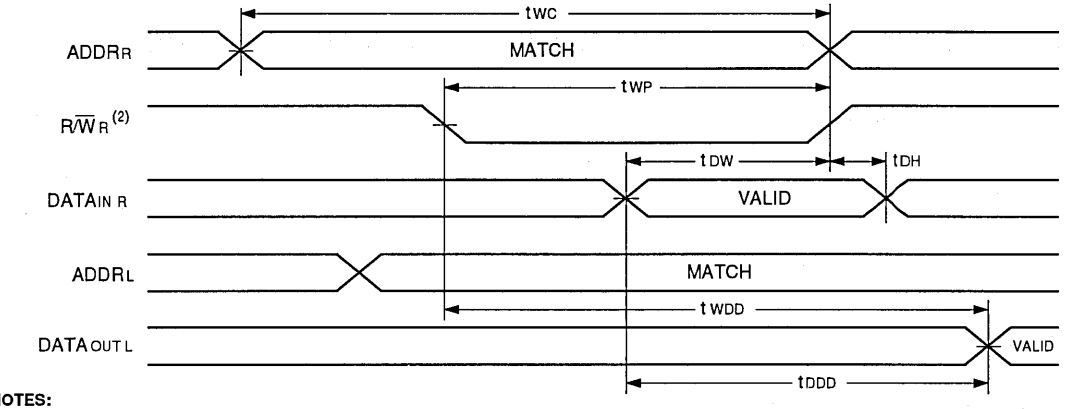
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1, 2, 3] (For MASTER IDT7133)



2746 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

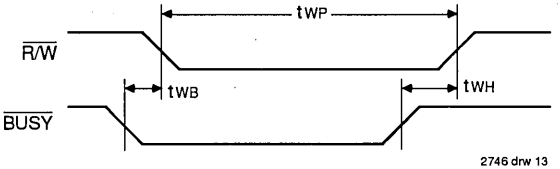
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1, 2, 3] (For SLAVE IDT7143)



2746 drw 12

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

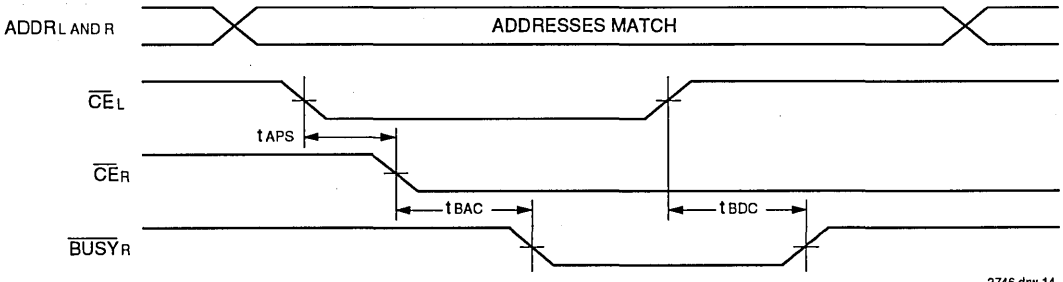
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (For SLAVE IDT7143)



2746 drw 13

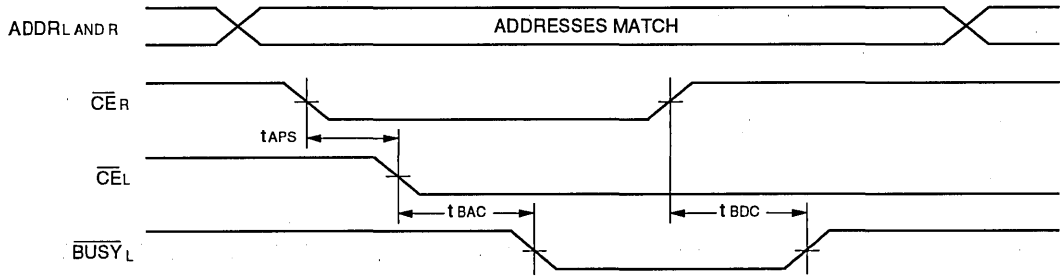
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (For MASTER IDT7133)

$\overline{CE}_L$ VALID FIRST:



2746 drw 14

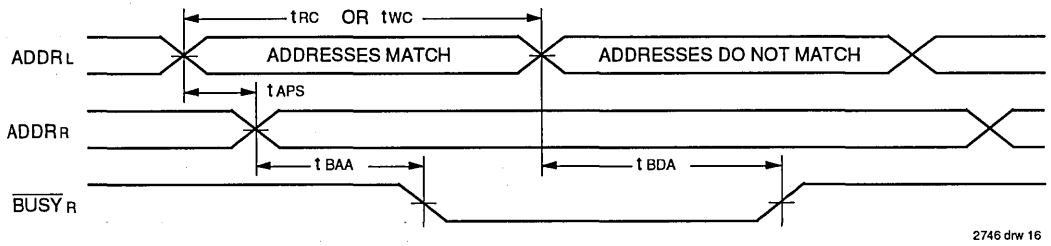
$\overline{CE}_R$ VALID FIRST:



2746 drw 15

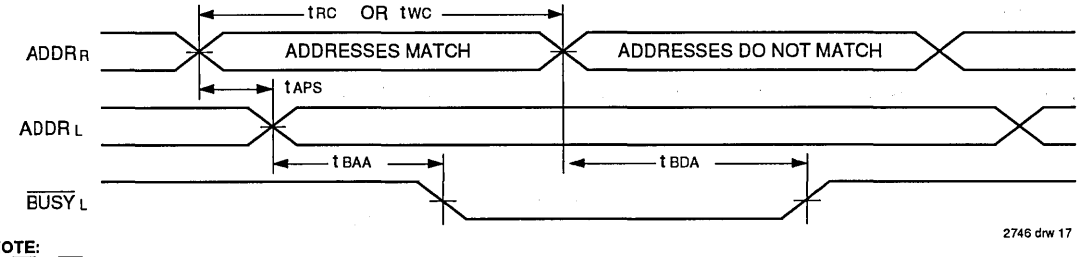
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (For MASTER IDT7133)

LEFT ADDRESS VALID FIRST:



2746 drw 16

RIGHT ADDRESS VALID FIRST:



2746 drw 17

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. The devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is pemitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that a write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to 32 bits or more in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinately for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory[2]
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance, LB = Lower Byte, UB = Upper Bytle

2746 tbl 12

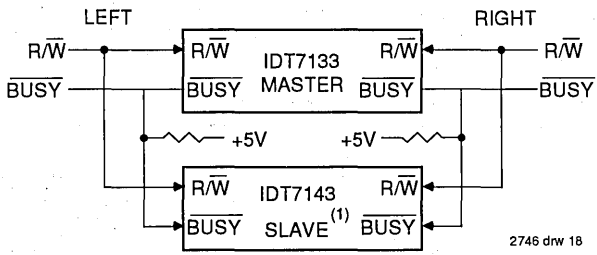
TABLE II — ARBITRATION[1]

LEFT PORT		RIGHT PORT		FLAGS		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	X	X	H	H	No Contention
X	X	H	X	H	H	No Contention
L	≠ $A_{0R} - A_{10R}$	L	≠ $A_{0L} - A_{10L}$	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	= $A_{0R} - A_{10R}$	LL5R	= $A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	= $A_{0R} - A_{10R}$	RL5L	= $A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2746 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care
   LV5R = Left Address Valid ≥ 5ns before right address
   RV5L = Right Address Valid ≥ 5ns before left address
   Same = Left and Right Address match within 5ns of each other
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other

32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2746 drw 18

NOTES:
1. No arbitration in IDT7143 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7143 (SLAVE).

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

PRELIMINARY
IDT7134SA
IDT7134LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

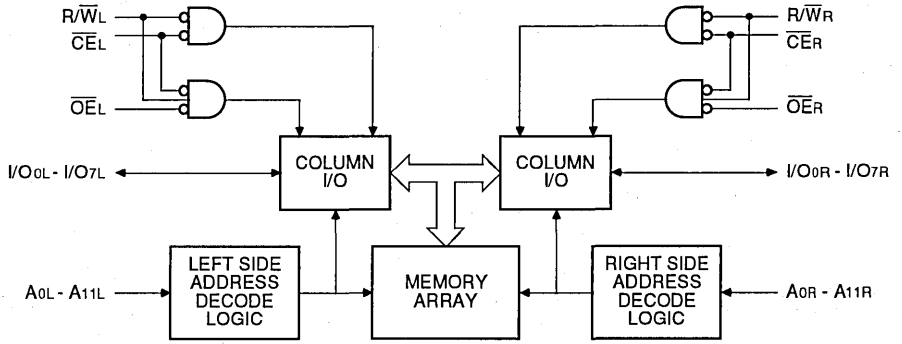
The IDT7134 is an extremely high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-port typically on only 500mW of power at maximum access times as fast as 25ns. Low -power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin LCC, and 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

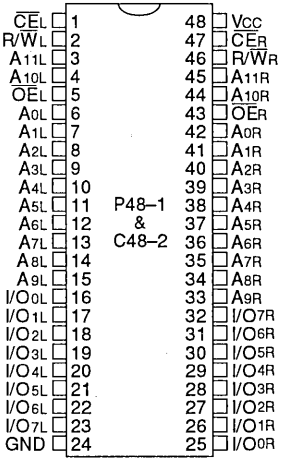


2720 drw 01

6

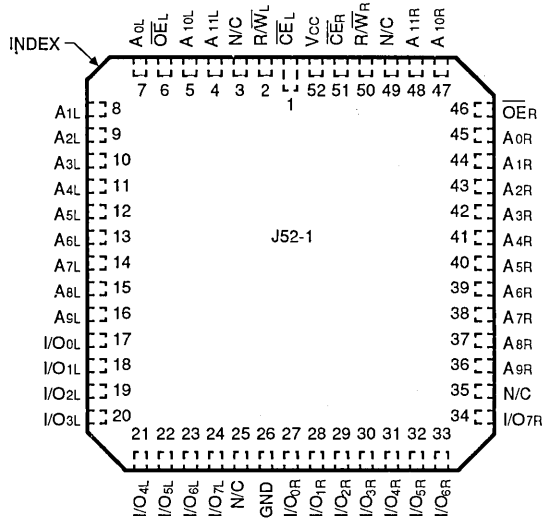
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2720 drw 02

DIP
TOP VIEW



2720 drw 03

PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM(2)	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2720 tbl 01

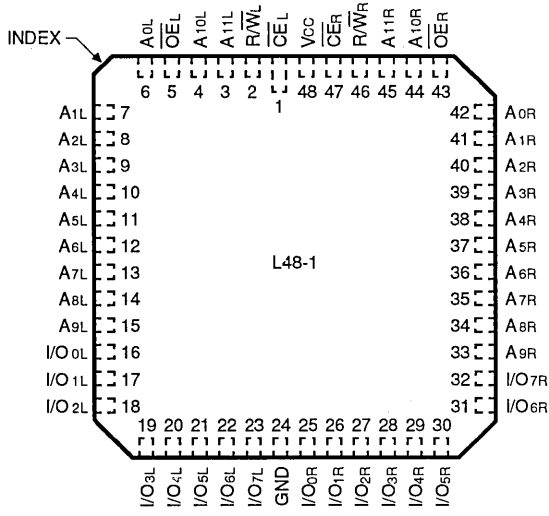
NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

2720 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.



2720 drw 04

LCC
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2720 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2720 tbl 04

NOTES:
1. VIL (min.) = –3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Vcc = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134SA		IDT7134LA		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current(5)	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage	IOL = 6mA	—	0.4	—	0.4	V
		IOL = 8mA	—	0.5	—	0.5	V
VOH	Output High Voltage	IOH = –4mA	2.4	—	2.4	—	V

2720 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7134X25(4)		7134X35		7134X45		7134X55		7134X70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ VIL Outputs Open f = fMAX(3)	MIL.	S	—	—	—	300	—	280	—	270	—	270	mA
				L	—	—	—	260	—	240	—	220	—	220	
			COM'L.	S	—	280	—	260	—	240	—	240	—	240	
				L	—	240	—	220	—	200	—	200	—	200	
ISB1	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}$L and $\overline{CE}$R ≥ VIH f = fMAX(3)	MIL.	S	—	—	25	75	25	70	25	70	25	70	mA
				L	—	—	25	55	25	50	25	50	25	50	
			COM'L.	S	25	80	25	75	25	70	25	70	25	70	
				L	25	50	25	45	25	40	25	40	25	40	
ISB2	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}$L or $\overline{CE}$R ≥ VIH Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	—	200	—	190	—	180	—	180	mA
				L	—	—	—	170	—	160	—	150	—	150	
			COM'L.	S	—	180	—	170	—	160	—	160	—	160	
				L	—	150	—	140	—	130	—	130	—	130	
ISB3	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}$L and $\overline{CE}$R ≥ Vcc - 0.2V VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, f = 0(3)	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
ISB4	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}$L or $\overline{CE}$R ≥ Vcc - 0.2V VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	—	190	—	180	—	170	—	170	mA
				L	—	—	—	160	—	150	—	140	—	140	
			COM'L.	S	—	170	—	160	—	150	—	150	—	150	
				L	—	140	—	130	—	120	—	120	—	120	

2720 tbl 06

NOTES:
1. "X" in part number indicates power rating (SA or LA).
2. Vcc = 5V, TA = +25°C.
3. fMAX = 1/tRC = All inputs cycling at f = 1/tRC (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby ISB3.
4. 0°C to +70°C temperature range.
5. At Vcc≤2.0V input leakages are undefined.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

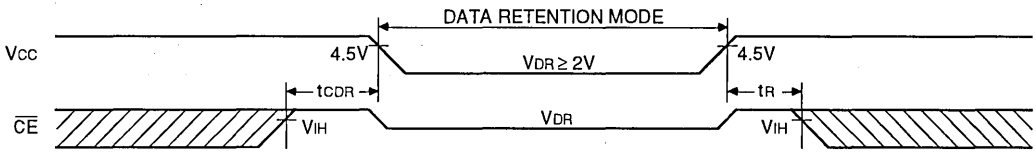
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	VCC for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

2720 tbl 07

LOW V_{CC} DATA RETENTION WAVEFORM

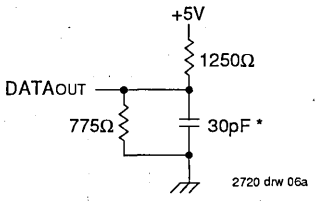


2720 drw 05

AC TEST CONDITIONS

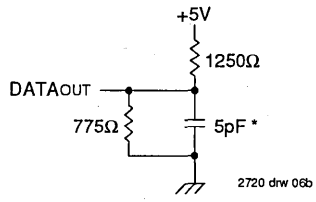
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2720 tbl 08



2720 drw 06a

Figure 1. Output Load



2720 drw 06b

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

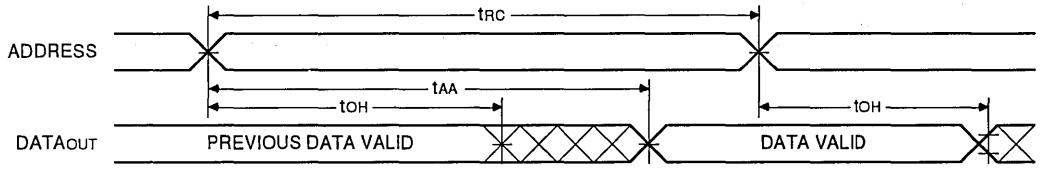
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	7134X25[3]		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	0	—	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	—	50	ns

NOTES:
2720 tbl 09

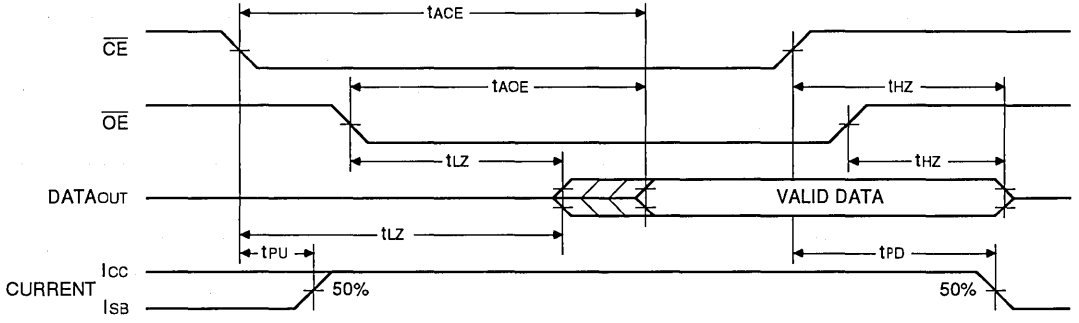
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2720 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2720 drw 08

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

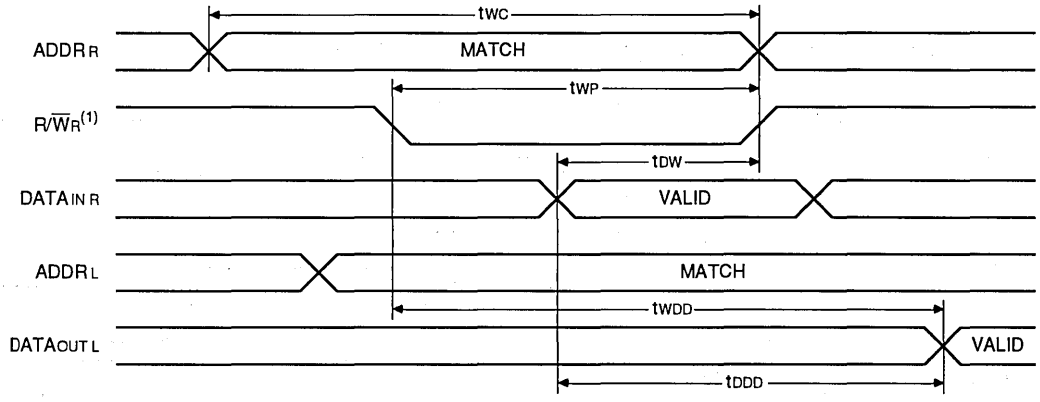
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	7134X25(5)		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE												
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	30	—	40	—	50	—	60	—	ns
tWR	Write RecoveryTime	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time(3)	0	—	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 3)	3	—	3	—	3	—	3	—	3	—	ns
tWDD	Write Pulse to Data Delay(4)	—	50	—	70	—	80	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay(4)	—	35	—	55	—	55	—	65	—	70	ns

2720 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. 0°C to +70°C temperature range only.
6. "X" in part number indicates power rating (SA or LA).

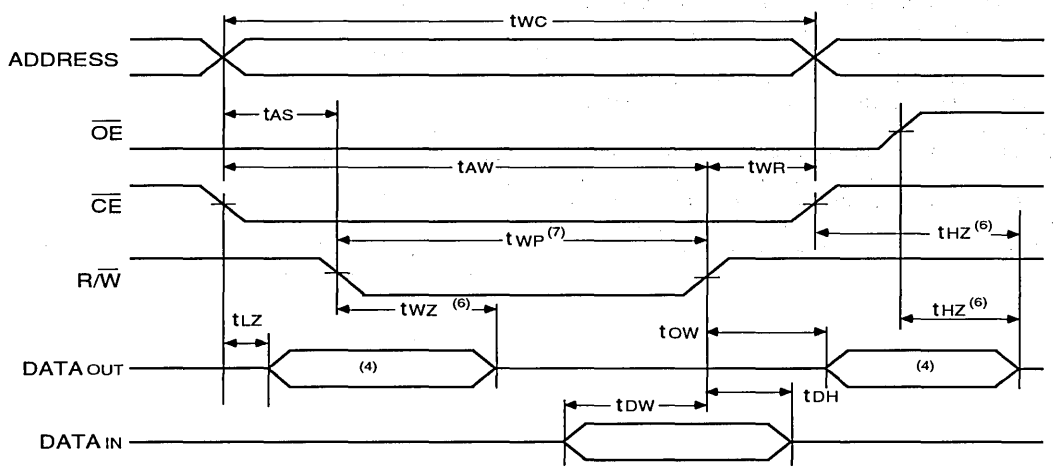
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1)



2720 drw 09

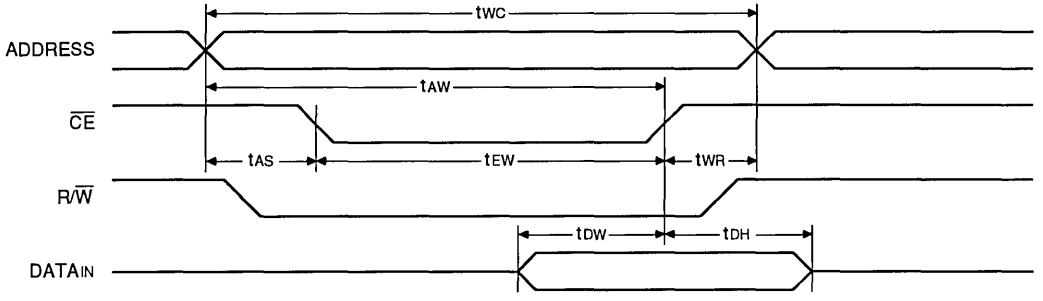
NOTE:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 4, 6, 7)



2720 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2720 drw 11

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

6

FUNCTIONAL DESCRIPTION

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

TABLE I – READ/WRITE CONTROL

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

2720 tbl 11

NOTE:
1. $A_{OL} - A_{11L} \neq A_{OR} - A_{11R}$
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

PRELIMINARY
IDT71342SA
IDT71342LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT71342SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT71342LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature raange (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

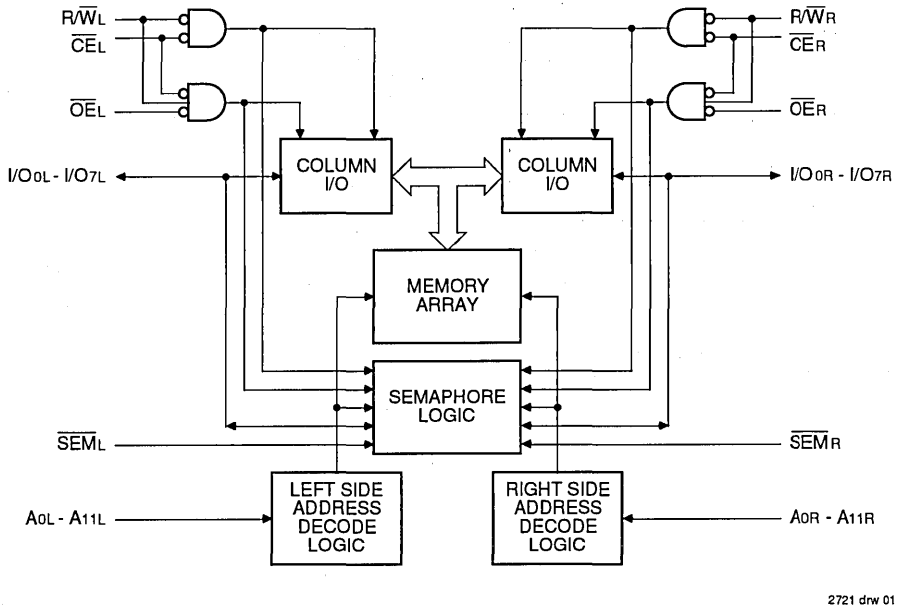
The IDT71342 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 500mW of power at maximum access times as fast as 25ns. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery. The device is packaged in either a hermetic 52-pin leadless chip carrier or a 52-pin PLCC.

The IDT71342 military devices are manufactured in compliance with the latest revision of MIL-STD-883, Class B.

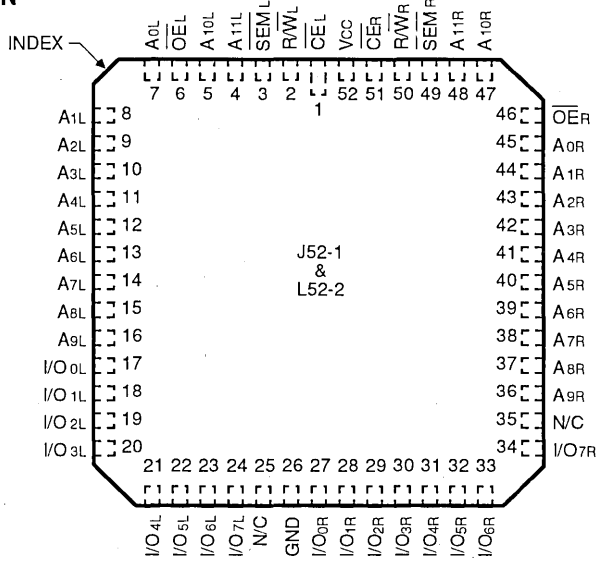
FUNCTIONAL BLOCK DIAGRAM



2721 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



LCC/PLCC
TOP VIEW

2721 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

2721 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

2721 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2721 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2721 tbl 04

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT71342SA		IDT71342LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2721 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		71342X25[4]		71342X35		71342X45		71342X55		71342X70		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ V_{IL} Outputs Open	MIL.	S	—	—	—	300	—	280	—	270	—	270	mA
				L	—	—	—	260	—	240	—	220	—	220	
		$\overline{SEM}$ = Don't Care f = f_{MAX}[3]	COM'L.	S	—	280	—	260	—	240	—	240	—	240	
				L	—	240	—	220	—	200	—	200	—	200	
I_{CC1}	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ ≥ V_H Outputs Open	MIL.	S	—	—	—	190	—	170	—	170	—	170	mA
				L	—	—	—	170	—	150	—	150	—	150	
		$\overline{SEM}$ ≤ V_L f = f_{MAX}[3]	COM'L.	S	—	200	—	185	—	170	—	170	—	170	
				L	—	170	—	155	—	140	—	140	—	140	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} $\overline{SEM_L}$ = $\overline{SEM_R}$ ≥ V_{IH}	MIL.	S	—	—	25	75	25	70	25	70	25	70	mA
				L	—	—	25	55	25	50	25	50	25	50	
		f = f_{MAX}[3]	COM'L.	S	25	80	25	75	25	70	25	70	25	70	
				L	25	50	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs	MIL.	S	—	—	—	200	—	190	—	180	—	180	mA
				L	—	—	—	170	—	160	—	150	—	150	
		Open, f = f_{MAX}[3] $\overline{SEM_L}$ = $\overline{SEM_R}$ ≥ V_{IH}	COM'L.	S	—	180	—	170	—	160	—	160	—	160	
				L	—	150	—	140	—	130	—	130	—	130	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V $\overline{SEM_L}$ = $\overline{SEM_R}$ ≥ V_{CC} - 0.2V, f = 0[3]	COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	—	190	—	180	—	170	—	170	mA
				L	—	—	—	160	—	150	—	140	—	140	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V $\overline{SEM_L}$ = $\overline{SEM_R}$ ≥ V_{CC} — 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	—	170	—	150	—	150	—	150	—	150	
				L	—	140	—	130	—	120	—	120	—	120	

2721 tbl 06

NOTES:
1. "X" in part number indicates power rating (SA or LA).
2. V_{CC} = 5V, T_A = +25°C.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
4. 0°C to +70°C temperature range.
5. At Vcc≤2.0V input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

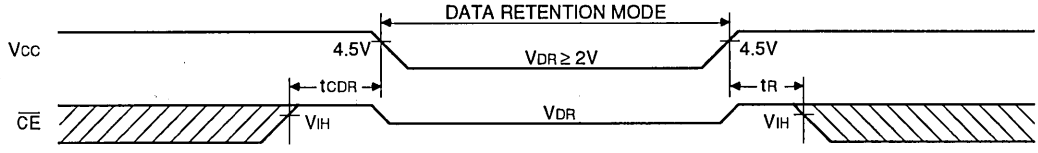
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	VCC for Data Retention	—		2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V	MIL.	—	100	4000	µA
		$\overline{CE} \geq V_{HC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2721 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM

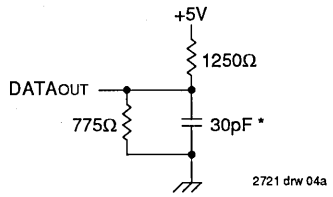


2721 drw 03

AC TEST CONDITIONS

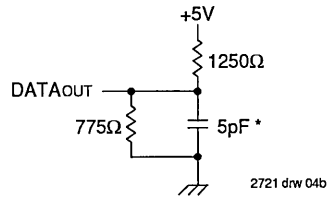
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2721 tbl 08



2721 drw 04a

Figure 1. Output Load



2721 drw 04b

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

*Including scope and jig

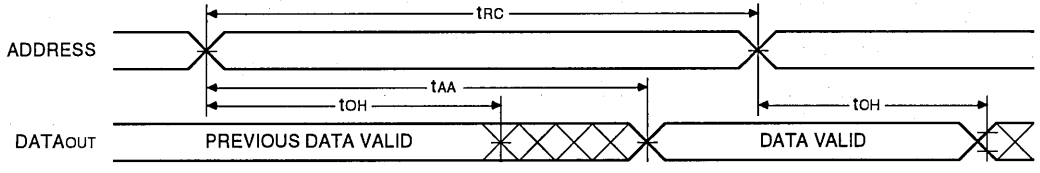
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[6]

Symbol	Parameter	71342X25[5]		71342X35		71342X45		71342X55		71342X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	0	—	0	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	—	50	ns
tSOP	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	15	—	15	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[4]	—	50	—	70	—	80	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	55	—	55	—	65	—	70	ns

2721 tbl 09

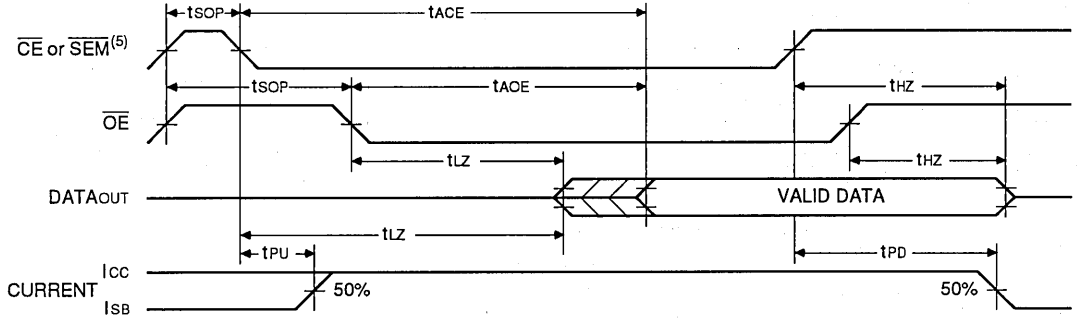
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.
4. Port to Port delay through RAM cells from writing port to a reading port.
5. 0°C to +70°C temperature range only.
6. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2721 drw 05

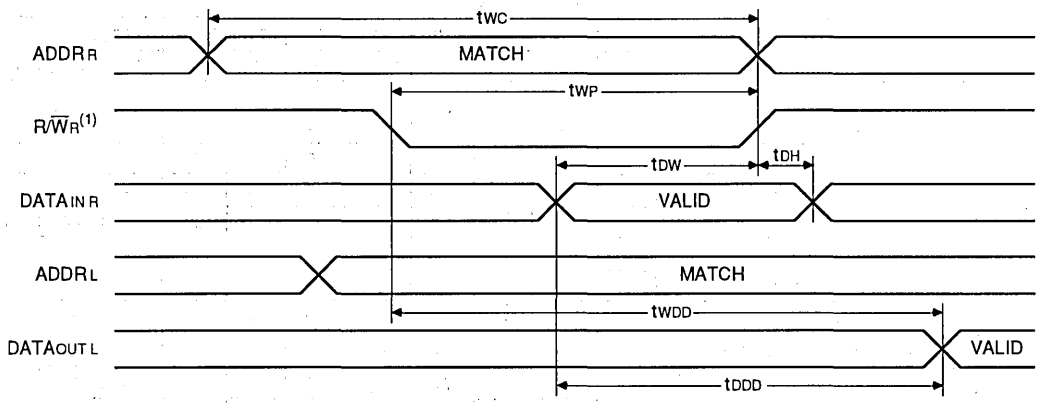
TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2721 drw 06

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.
5. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2)



2721 drw 07

NOTES:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. Device is continuously enabled for both ports.

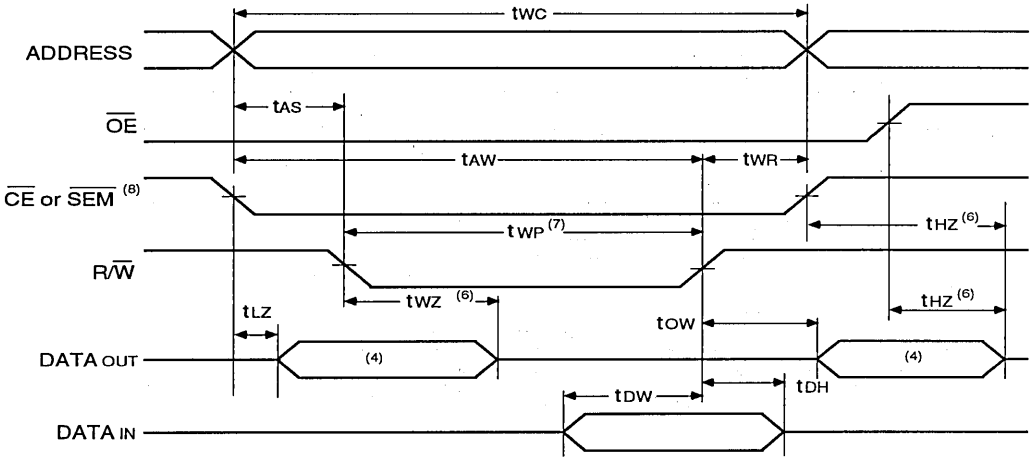
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	7134X25(5)		7134X35		7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	WRITE CYCLE											
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	20	—	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	20	—	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	30	—	40	—	50	—	60	—	ns
tWR	Write RecoveryTime	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z(1, 2)	—	15	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	3	—	3	—	3	—	3	—	3	—	ns
tSWR	SEM Flag Write to Read Time	10	—	10	—	10	—	10	—	10	—	ns
tSPS	SEM Flag Contention Window	10	—	10	—	10	—	10	—	10	—	ns

2721 tbl 10

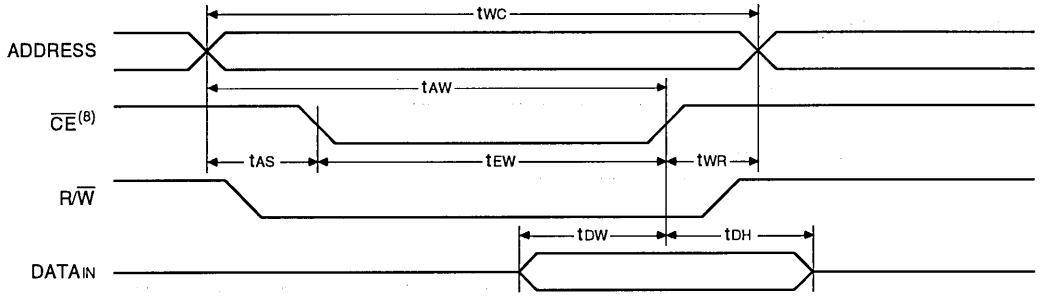
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. This condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 0°C to +70°C temperature range only.
6. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



2720 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)

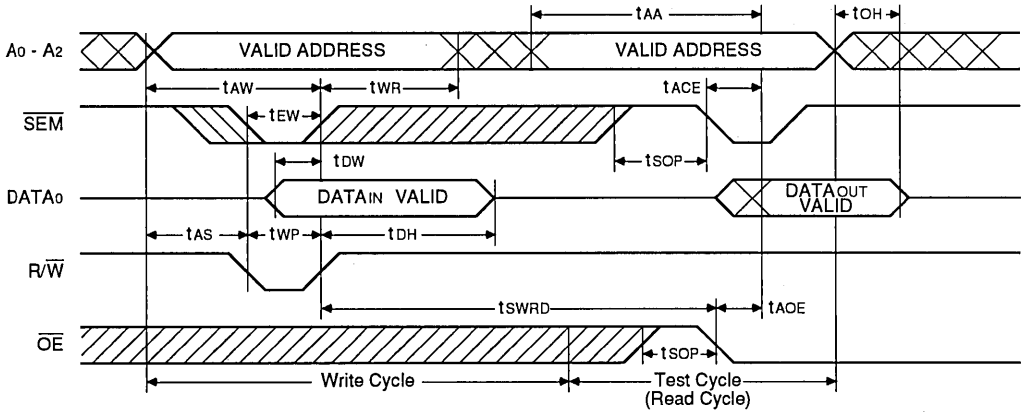


2721 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH, $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.

6

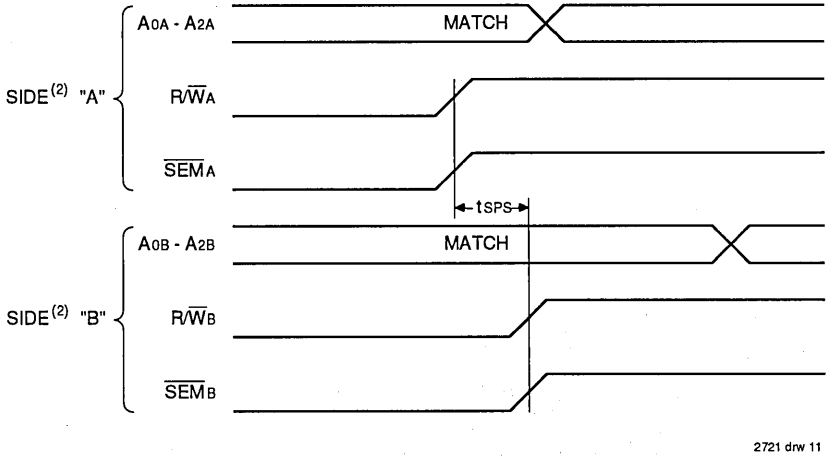
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



2721 drw 10

NOTE:
1. $\overline{CE}$ = V_{IH} for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



2721 drw 11

NOTES:
1. D_{OR} = D_{OL} = V_{IL}, $\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH}, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast dual-port 4K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from or written to at the same time, with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table 1 where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through the address pins A_0–A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a processor writes a zero in the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume

control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

TABLE I — NON-CONTENTION READ/WRITE CONTROL

Left or Right Port(1)					
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	Function
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	$DATA_{OUT}$	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
↑	H	L	X	$DATA_{IN}$	Port Data Bit D0 Written Into Semaphore Flag
H	L	H	L	$DATA_{OUT}$	Data in Memory Output on Port
L	L	H	X	$DATA_{IN}$	Data on Port Written Into Memory
X	L	L	X	—	Not Allowed

2721 tbl 11

NOTE:
1. $A_{OL} = A_{10L} \neq A_{0R} - A_{10R}$
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
   ↑ = Low-to-High transition.

TABLE II — EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE(1)

Function	$D_0 - D_7$ Left	$D_0 - D_7$ Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left side has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2721 tbl 12

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES–Some examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's dual-port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of the memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to by any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

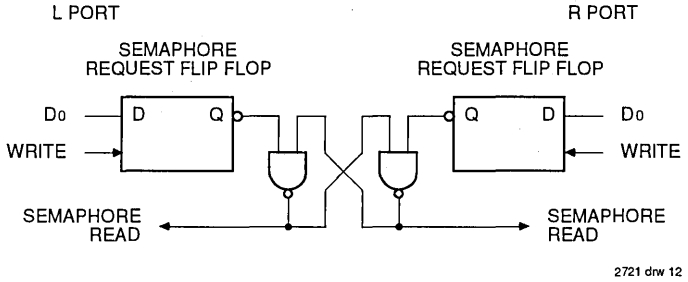


Figure 3. IDT71342 Semaphore Logic

Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) DUAL-PORT RAM

PRELIMINARY
IDT7014S

FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 20/25/35ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7014S
    Active: 900mW (typ.)
- IDT'S BiCEMOS™ process
- Fully asynchronous operation from either port
- TTL-compatible; single 5V (±10%) power supply
- Available in 52-pin plastic leaded chip carrier
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

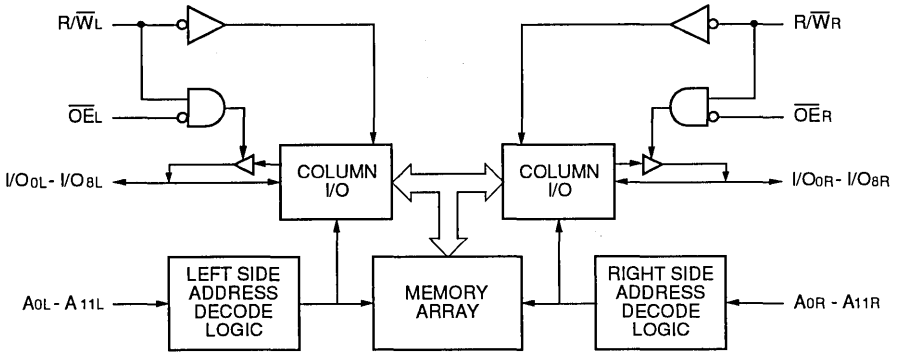
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7014 utilitizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's BiCEMOS™ high-performance technology, these dual-ports typically operate on only 900mW of power at maximum access times as fast as 15ns.

The IDT7014 is packaged in a 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

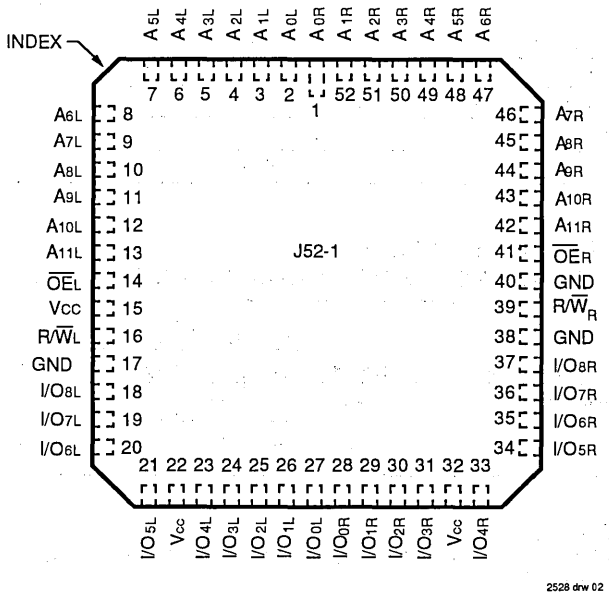
FUNCTIONAL BLOCK DIAGRAM



2528 drw 01

BiCEMOS™ is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



52-Pin PLCC
Top View

NOTES:
1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.

6

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage	-0.5 to Vcc	-0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2528 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.
3. I/O terminals only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2528 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2528 tbl 03

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7014S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	V

2528 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7014S15[1]		IDT7014S20		IDT7014S25		IDT7014S35[2]		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}[3]	Mil.	—	—	—	260	—	255	—	250	mA
			Com'l.	—	250	—	245	—	240	—	—	

2528 tbl 05

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC TEST CONDITIONS" of input levels of GND to 3V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2528 tbl 06

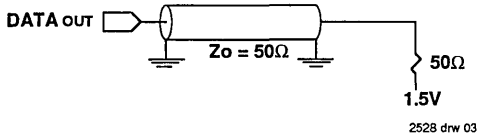
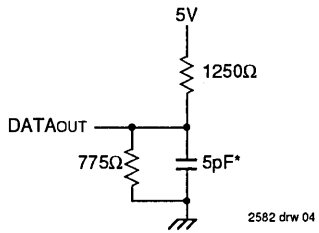


Figure 1. Output load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

2528 tbl 07



* Including scope and jig.

Figure 2. Output Load (for t_{HZ}, t_{WZ}, and t_{OW})

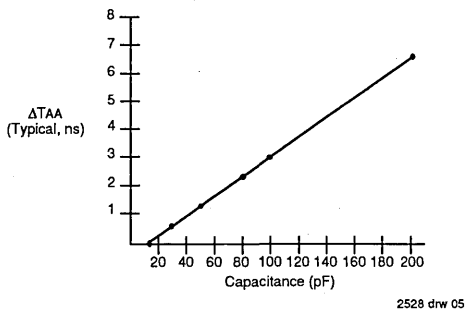


Figure 3. Lumped Capacitive Load, Typical Derating.

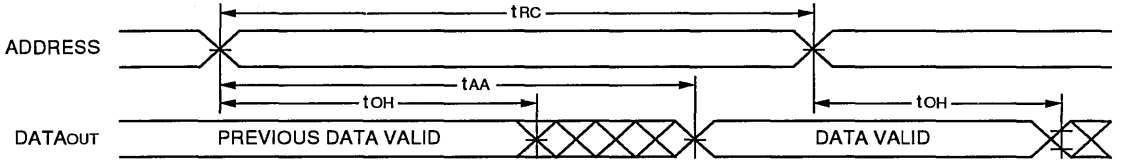
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	7014X15[3]		7014X20		7014X25		7014X35[4]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	35	ns
tAOE	Output Enable Access Time	—	8	—	10	—	12	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	0	—	0	—	0	—	3	—	ns
tHZ	Output High Z Time[1, 2]	—	7	—	9	—	11	—	15	ns

2528 tbl 08

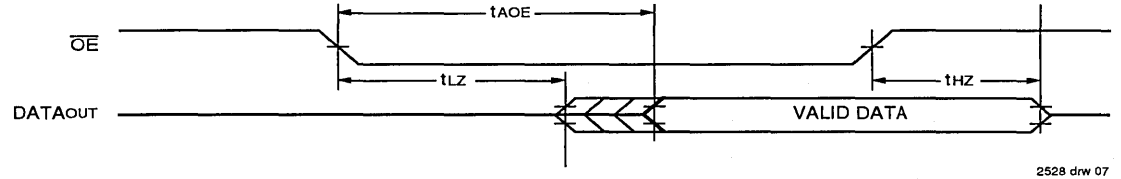
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figure 1).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.
4. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2]



2528 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2528 drw 07

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. $\overline{OE}$ = VIL.
3. Addresses valid prior to $\overline{OE}$ transition low.

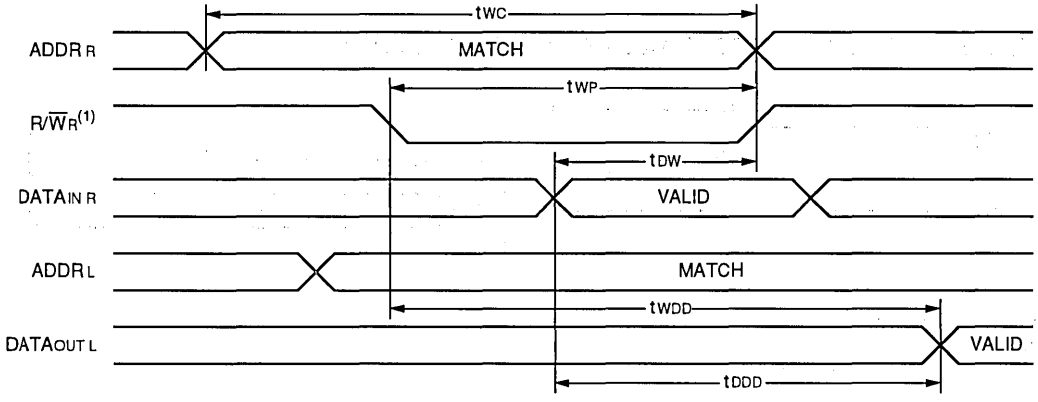
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	7014S15[5]		7014S20		7014S25		7014S35[6]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tAW	Address Valid to End of Write	14	—	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	30	—	ns
tWR	Write RecoveryTime	1	—	2	—	2	—	2	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	25	—	ns
tHZ	Output High Z Time[1, 2]	—	7	—	9	—	11	—	15	ns
tDH	Data Hold Time[3]	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	7	—	9	—	11	—	15	ns
tOW	Output Active from End of Write[1, 2, 3]	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	30	—	40	—	45	—	55	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	25	—	30	—	35	—	45	ns

NOTES:
2528 tbl 09

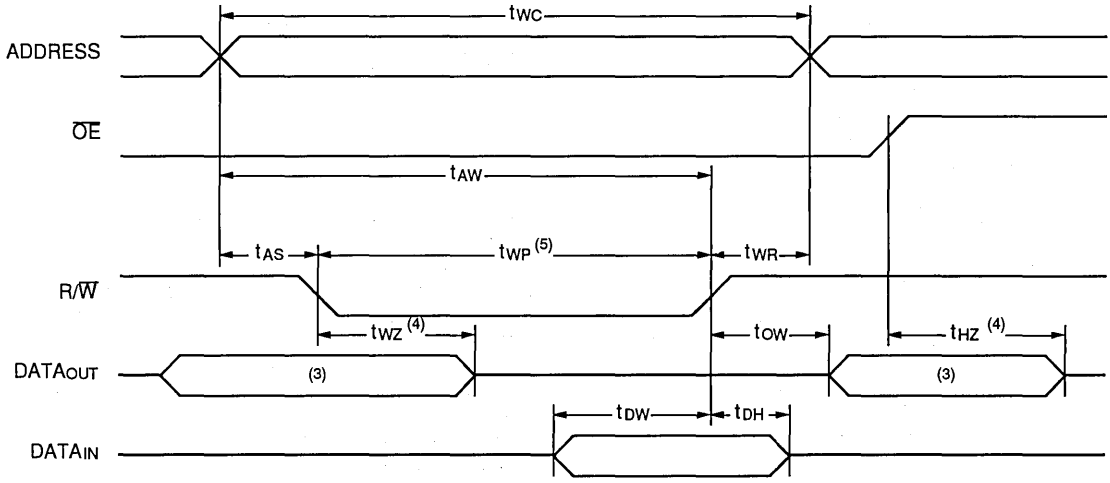
1. Transition is measured ±500mV from low or high impedance voltage with load (Figure 1).
2. This parameter is guaranteed but not tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. 0°C to +70°C temperature range only.
6. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY



2528 drw 08

TIMING WAVEFORM OF WRITE CYCLE(1, 2, 3, 4, 5)



2528 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. t_{WR} is measured from R/$\overline{W}$ going high to the end of write cycle.
3. During this period, the I/O pins are in the output state, and input signals must not be applied.
4. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
5. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

FUNCTIONAL DESCRIPTION

The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of CEMOS™ Dual Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

TABLE I – READ/WRITE CONTROL

Left or Right Port(1)			
R/$\overline{W}$	$\overline{OE}$	D_{0-8}	Function
L	X	DATAIN	Data on port written into memory
H	L	DATAOUT	Data in memory output on port
X	H	Z	High impedance outputs

2528 tbl 10

NOTE:
1. A_{OL} - $A_{11L} \neq A_{OR}$ - A_{11R}
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) SYNCHRONOUS DUAL-PORT RAM

PRELIMINARY
IDT7099S

FEATURES:

- High-speed clock-to-data output times
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7099S
    - Active: 900 mW (typ.)
    - Standby: 50 mW (typ.)
- 4K X 9 bits
- Architecture based on dual-port RAM cells
  - — Allows full simultaneous access from both ports
  - — Independent bit/byte read and write inputs for control functions
- IDT's BiCEMOS™ process technology
- Synchronous operation
  - — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 15ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 20ns cycle times, 50MHz operation
- Clock enable feature
- Guaranteed data output hold times
- Available in 68-pin PGA and PLCC
- Military product compliant to MIL-STD-883, Class B

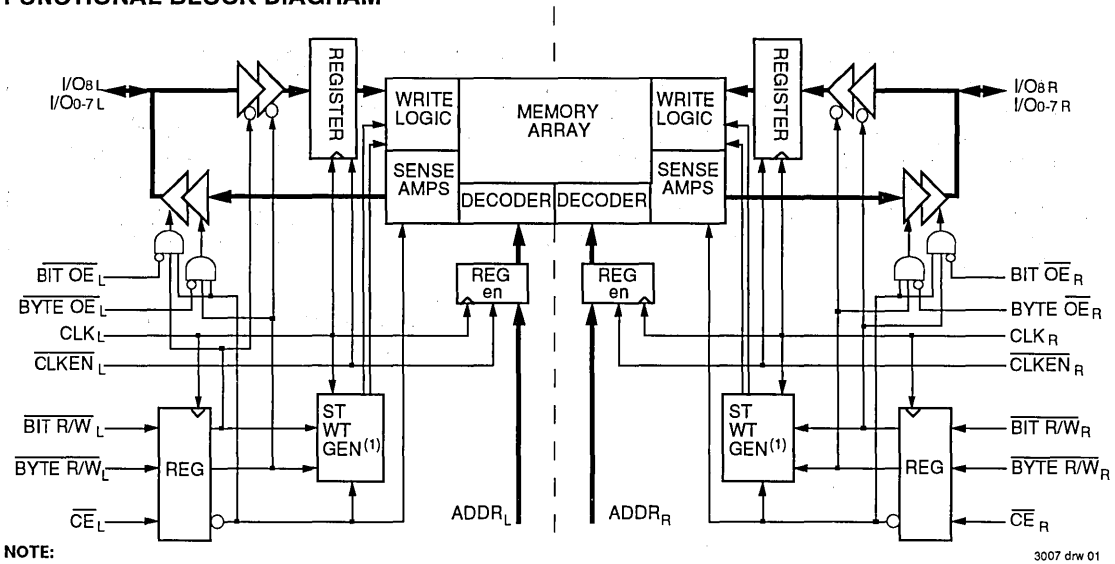
DESCRIPTION:

The IDT7099 is a high-speed 4K x 9 bit synchronous dual-port RAM. The memory array is based on dual-port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts. Changing data direction from reading to writing normally requires one dead cycle.

Fabricated using IDT's BiCEMOS™ high-performance technology, these dual-ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 15ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7099 is packaged in a 68-pin PGA or 68-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM

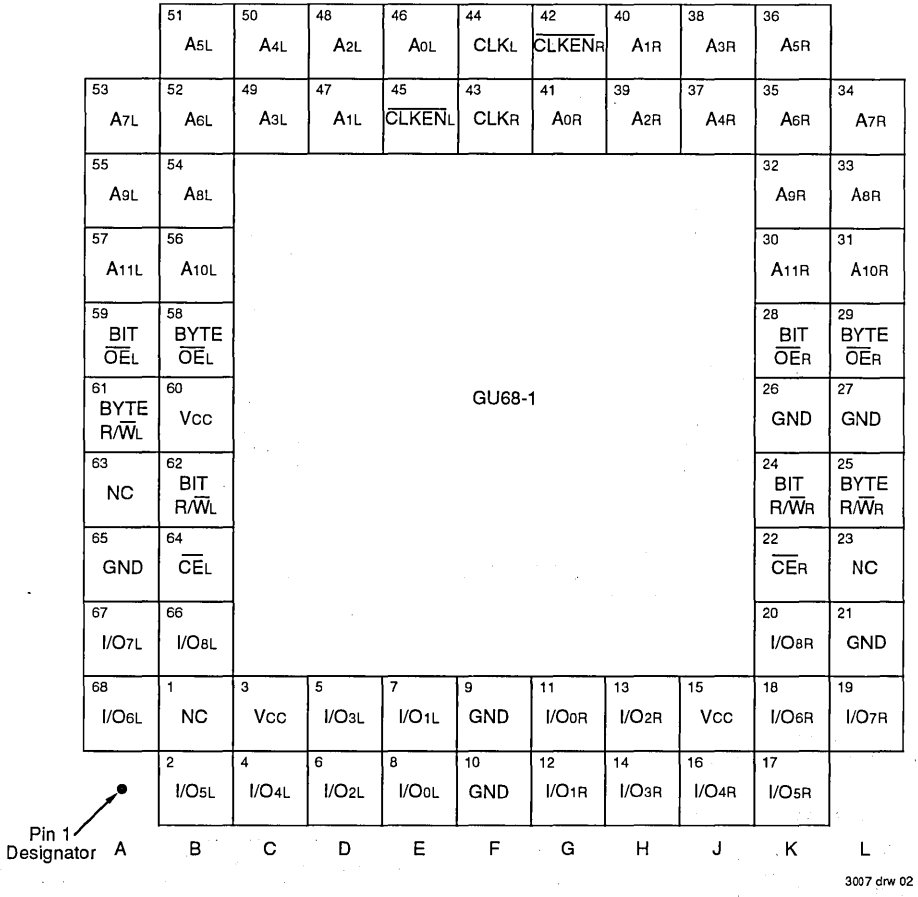


NOTE:
1. Self-timed write generator.

3007 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

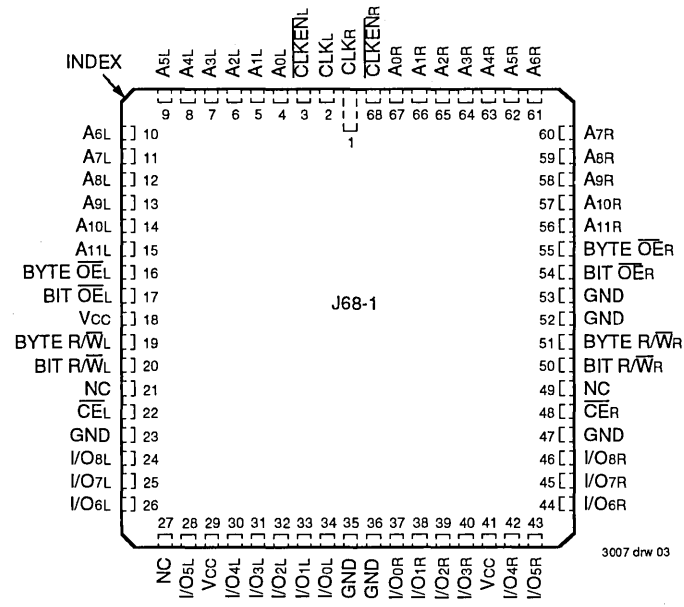


68-Pin PGA
Top View

NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.

6

PIN CONFIGURATIONS (CONTINUED)



68-Pin PLCC
Top View

NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	-0.5 to VCC	-0.5 to VCC	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3007 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.
3. I/O terminals only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3007 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

3007 tbl 03

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7099S Min.	IDT7099S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	VCC = 5.5V, VIN = 0V to VCC	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to VCC	—	10	µA
V_{OL}	Output Low Voltage	IOL = 4mA	—	0.4	V
V_{OH}	Output High Voltage	IOH = –4mA	2.4	—	V

3007 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

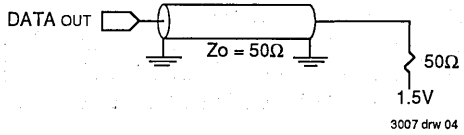
Symbol	Parameter	Test Condition	Version	IDT7099S15[1] Typ.	IDT7099S15[1] Max.	IDT7099S20 Typ.	IDT7099S20 Max.	IDT7099S25 Typ.	IDT7099S25 Max.	IDT7099S30[2] Typ.	IDT7099S30[2] Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[3]	Mil.	—	—	—	390	—	370	—	360	mA
			Com'l.	—	390	—	360	—	340	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$ f = f_{MAX}[3]	Mil.	—	—	—	190	—	170	—	140	mA
			Com'l.	—	220	—	180	—	160	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open, f = f_{MAX}[3]	Mil.	—	—	—	290	—	270	—	250	mA
			Com'l.	—	300	—	270	—	250	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0[4]	Mil.	—	—	—	20	—	20	—	20	mA
			Com'l.	—	10	—	10	—	10	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, Active Port Outputs Open, f = f_{MAX}[3]	Mil.	—	—	—	280	—	260	—	240	mA
			Com'l.	—	290	—	260	—	240	—	—	

3007 tbl 05

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tCLK, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
4. f = 0 means no address, clock, or control lines change. Applies only to inputs at CMOS level standby.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3



3007 drw 04

Figure 1. Output load.

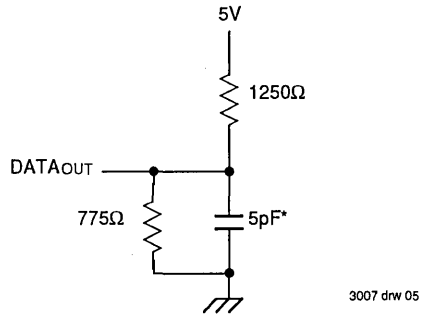


Figure 2. Output Load (for tCLZ, tCHZ, tOLZ, and tOHZ).

*Including scope and jig.

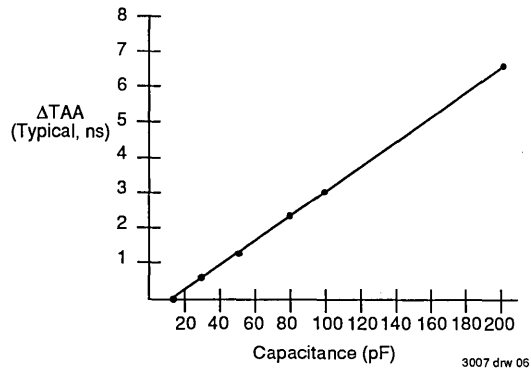


Figure 3. Lumped Capacitive Load, Typical Derating.

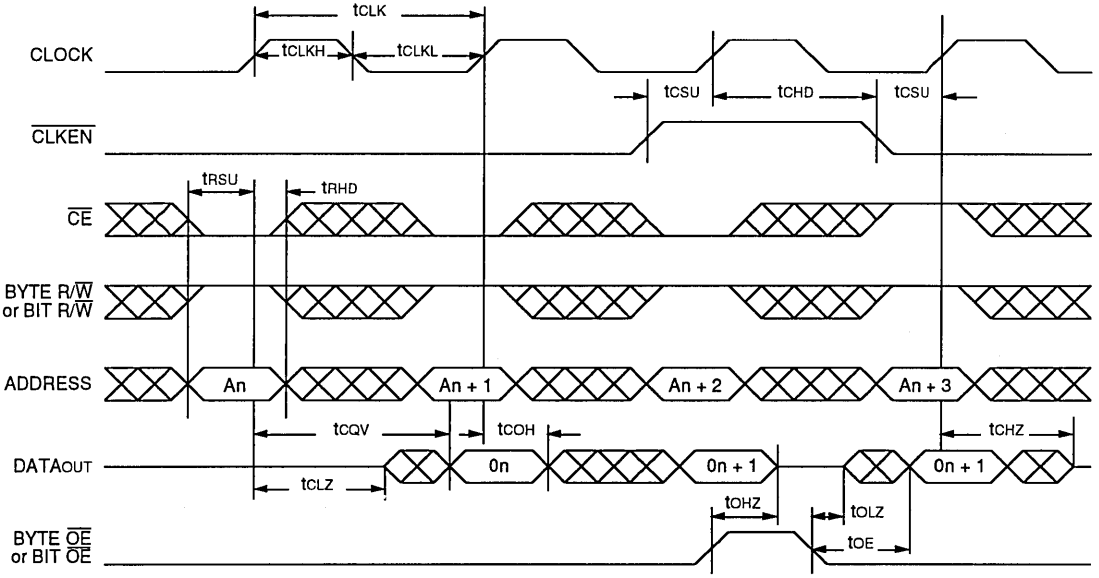
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

		Commercial						Military						
		7099S15		7099S20		7099S25		7099S20		7099S25		7099S30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCLK	Clock Cycle Time	20	—	20	—	25	—	20	—	25	—	30	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
tCQV	Clock High to Output Valid	—	15	—	20	—	25	—	20	—	25	—	30	ns
tRSU	Registered Signal Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
tRHD	Registered Signal Hold Time	1	—	1	—	1	—	2	—	2	—	2	—	ns
tCOH	Data Output Hold After Clock High	3	—	3	—	3	—	3	—	3	—	3	—	ns
tCLZ	Clock High to Output Low Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
tCHZ	Clock High to Output High Z	2	7	2	9	2	12	2	9	2	12	2	15	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	—	10	—	12	—	15	ns
tOLZ	Output Enable to Output Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output High Z	—	7	—	9	—	11	—	9	—	11	—	14	ns
tCSU	Clock Enable, Disable Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
tCHD	Clock Enable, Disable Hold Time	2	—	2	—	2	—	3	—	3	—	3	—	ns
Port-to-Port Delay														
tCWDD	Write Port Clock High to Read Data Delay	—	30	—	35	—	45	—	35	—	45	—	55	ns

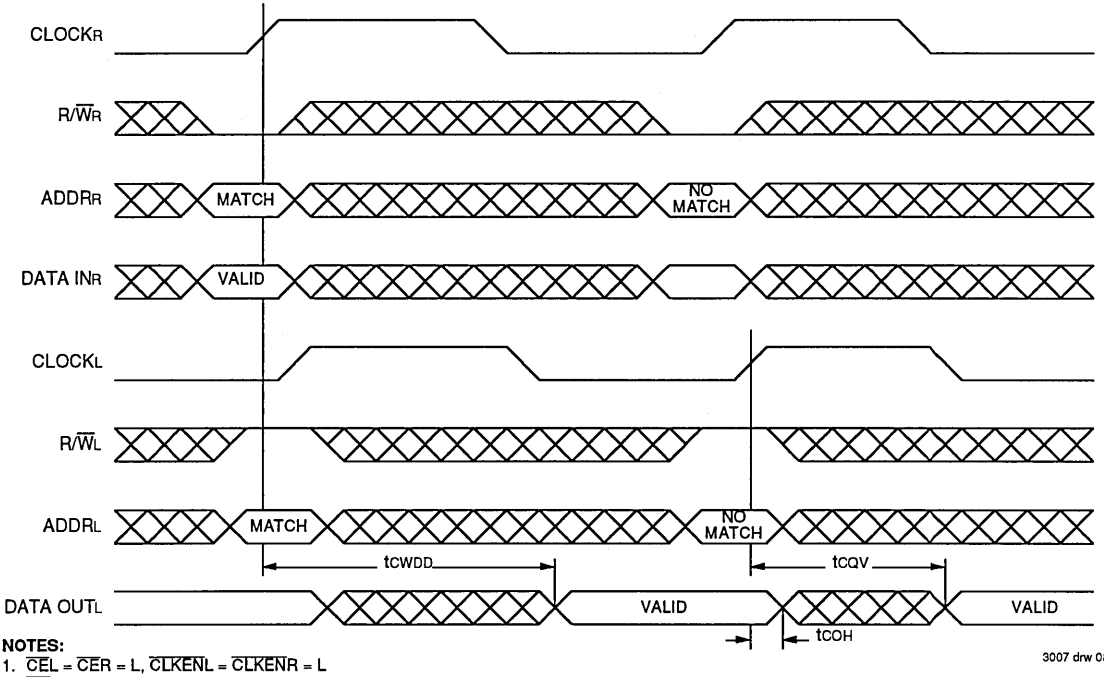
3007 tbl 06

TIMING WAVEFORM OF READ CYCLE, EITHER SIDE(1,2)



3007 drw 07

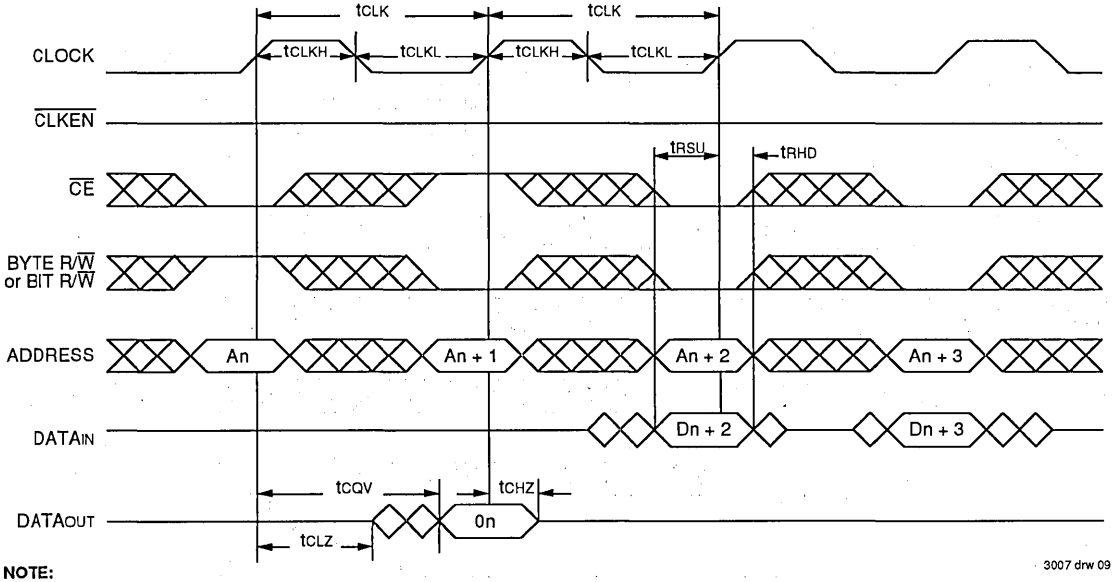
TIMING WAVEFORM OF READ CYCLE WITH PORT-TO-PORT DELAY



3007 drw 08

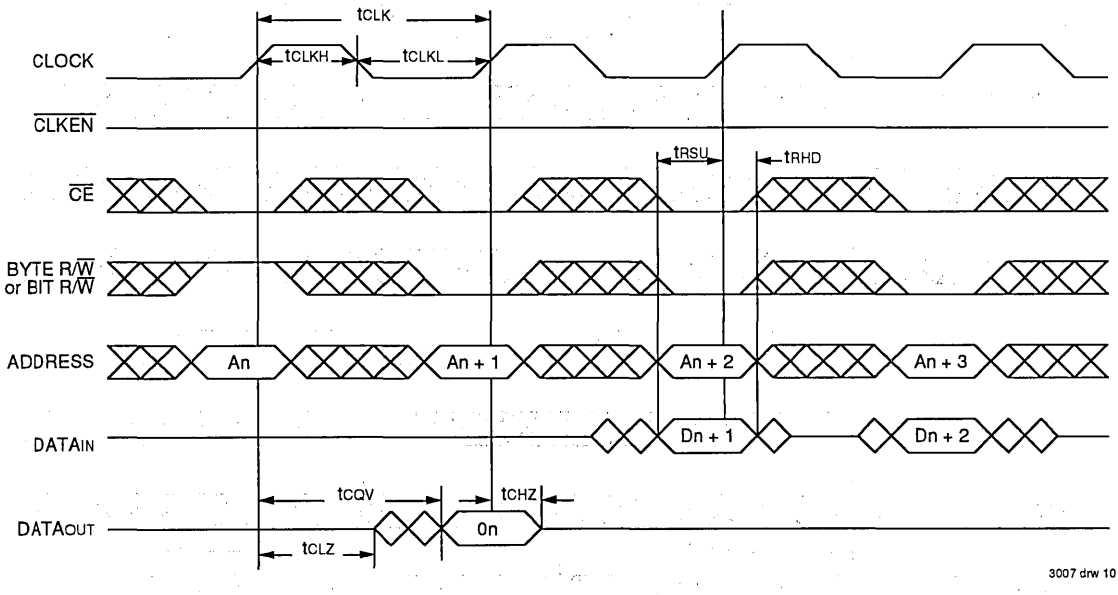
NOTES:
1. $\overline{CEL}$ = $\overline{CER}$ = L, $\overline{CLKENL}$ = $\overline{CLKENR}$ = L
2. $\overline{OE}$ = L for the reading port.

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ HIGH(1)



NOTE:
1. $\overline{OE}$ low throughout.

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ LOW(1,2)



NOTES:
1. During dead cycle, if $\overline{CE}$ is low, data will be written into array.
2. $\overline{OE}$ low throughout.

FUNCTIONAL DESCRIPTION

The IDT7099 provides a true synchronous dual-port static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is independent of the high and low periods of the clock. This allows the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the BYTE R/$\overline{W}$ and BIT R/$\overline{W}$ pins are low for at least one clock cycle before any write is attempted. A high on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The device has separate bit write, byte write, bit enable, and byte enable pins to allow for independent control.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

3007 tbl 07

TRUTH TABLES

TRUTH TABLE I: READ/WRITE CONTROL[1]

Inputs						Outputs		
Synchronous				Asynchronous				
Clk	$\overline{CE}$	Byte R/$\overline{W}$	Bit R/$\overline{W}$	Byte $\overline{OE}$	Bit $\overline{OE}$	I/O0-7	I/O8	Mode
↑	h	h	h	X	X	Hi-Z	Hi-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	h	X	X	DATAIN	Hi-Z	Deselected, Power Down, Byte Data Input Enabled
↑	h	h	l	X	X	Hi-Z	DATAIN	Deselected, Power Down, Bit Data Input Enabled
↑	h	l	l	X	X	DATAIN	DATAIN	Deselected, Power Down, Data Input Enabled
↑	l	l	h	X	L	DATAIN	DATAOUT	Write Byte, Read Bit
↑	l	l	h	X	H	DATAIN	Hi-Z	Write Byte Only
↑	l	h	l	L	X	DATAOUT	DATAIN	Read Byte, Write Bit
↑	l	h	l	H	X	Hi-Z	DATAIN	Write Bit Only
↑	l	l	l	X	X	DATAIN	DATAIN	Write Byte, Write Bit
↑	l	h	h	L	L	DATAOUT	DATAOUT	Read Byte, Read Bit
↑	l	h	h	H	L	Hi-Z	DATAOUT	Read Bit Only
↑	l	h	h	L	H	DATAOUT	Hi-Z	Read Byte Only
↑	l	h	h	H	H	Hi-Z	Hi-Z	Data I/O Disabled

3007 tbl 08

TRUTH TABLE II: CLOCK ENABLE FUNCTION TABLE[1]

	Inputs		Register Inputs		Register Outputs	
Operating Mode	Clk	$\overline{CLKEN}$	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	↑	l	h	h	H	H
Load "0"	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	N/C	N/C
	X	H	X	X	N/C	N/C

3007 tbl 09

NOTE:
1. H = High voltage level steady state, h = High voltage level one set-up time prior to the low-to-high clock transition, L = Low voltage level steady state
l = Low voltage level one set-up time prior to the low-to-high clock transition, X = Don't care, N/C = No change

Integrated Device Technology, Inc.

HIGH-SPEED 8K x 8 DUAL-PORT STATIC RAM

IDT7005S/L

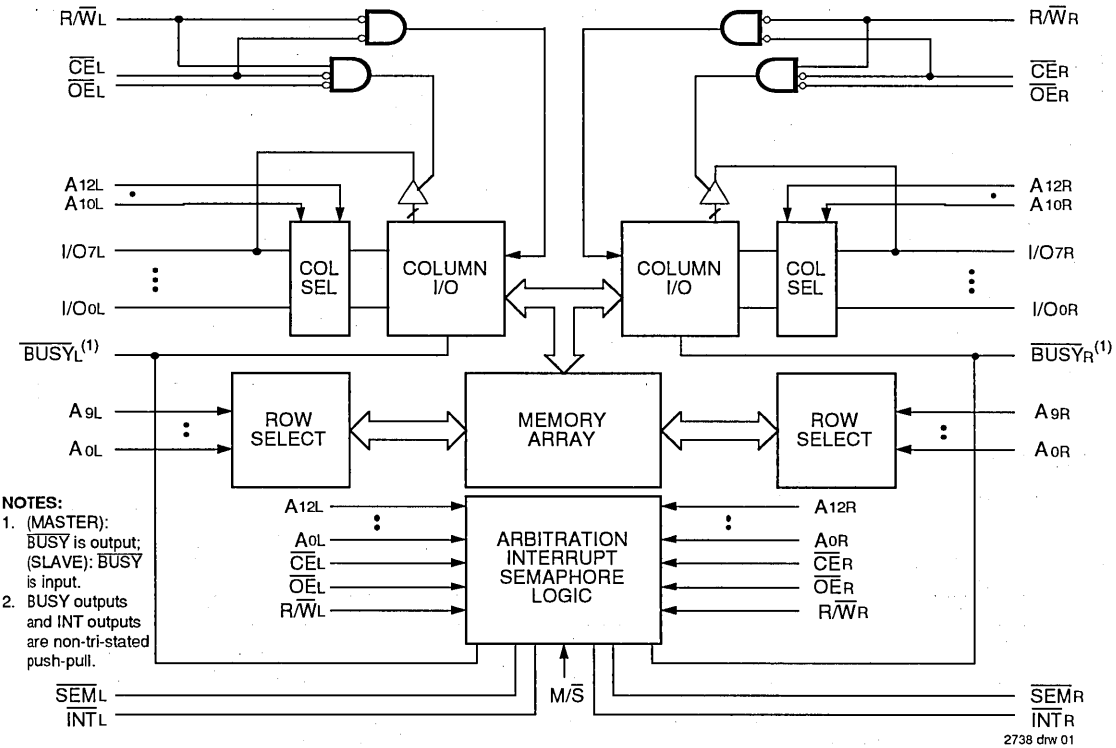
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55ns (max.)
- Low-power operation
  - — IDT7005S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7005L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7005 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, LCC and PLCC
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7005 is a high-speed 8K x 8 dual-port static RAM. The IDT7005 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-bit or wider

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and INT outputs are non-tri-stated push-pull.

2738 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

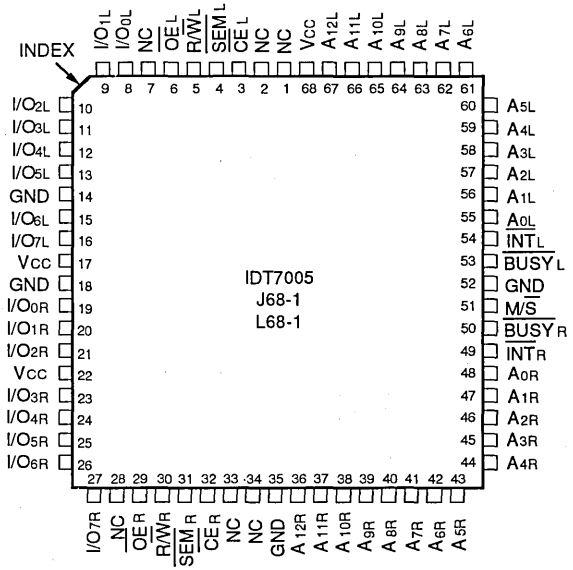
memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 750mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7005 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a LCC, and a PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS

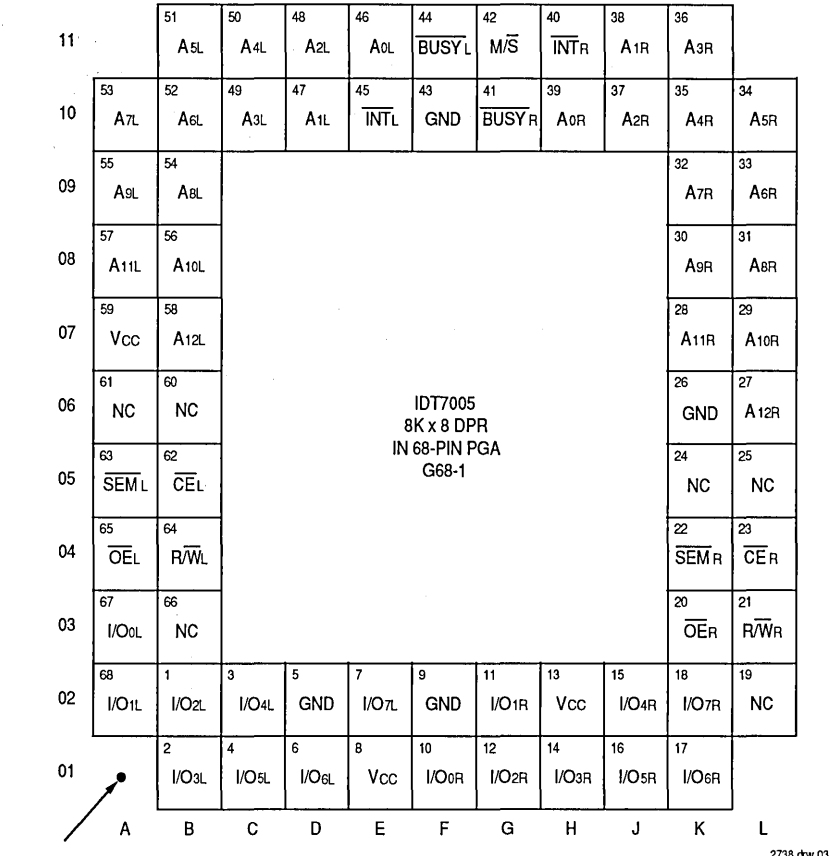


2738 drw 02

LCC/PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



68-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2738 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{12L} \neq A_{0R} — A_{12R}$

2738 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	⎍	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2738 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES:
2738 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
2738 tbl 03
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2738 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTES:
2738 tbl 06
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7005S		IDT7005L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2738 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X35 COM'L ONLY Typ.[2]	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ V_{IL}, Outputs Open $\overline{SEM}$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	160	340	
				L	160	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ ≥ V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	20	70	
				L	20	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH}	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	95	240	
				L	95	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	mA
				L	—	10	
			COM'L.	S	1.0	15	
				L	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	90	220	
				L	90	180	

NOTES:

2738 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At V_{CC}≤2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X45 Typ.[2]	7005X45 Max.	7005X55 Typ.[2]	7005X55 Max.	7005X70 MIL ONLY Typ.[2]	7005X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	155	400	150	395	140	390	mA
				L	155	340	150	335	140	330	
			COM'L.	S	155	340	150	335	—	—	
				L	155	290	150	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	16	85	13	85	10	85	mA
				L	16	65	13	65	10	65	
			COM'L.	S	16	70	13	70	—	—	
				L	16	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ Active Port Outputs Open $f = f_{MAX}$[3] $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	90	290	85	290	80	290	mA
				L	90	250	85	250	80	250	
			COM'L.	S	90	240	85	240	—	—	
				L	90	210	85	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, $f = 0$[4] $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, $f = f_{MAX}$[3]	MIL.	S	85	260	80	260	75	260	mA
				L	85	215	80	215	75	215	
			COM'L.	S	85	220	80	220	—	—	
				L	85	180	80	180	—	—	

NOTES:

2738 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

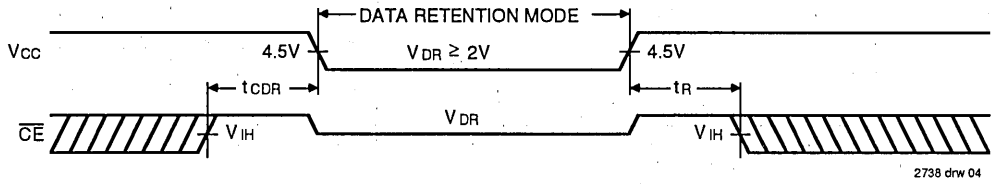
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2738 tbl 09

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

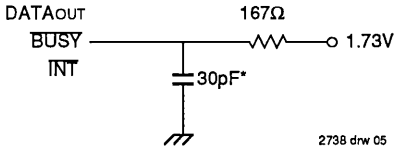


2738 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

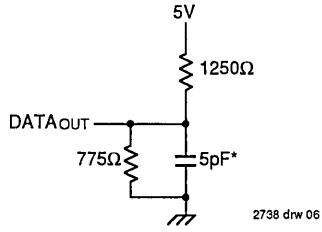
2738 tbl 10



2738 drw 05

* Including scope and jig.

Figure 1. Equivalent Output Load



2738 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
READ CYCLE				
t_{RC}	Read Cycle Time	35	—	ns
t_{AA}	Address Access Time	—	35	ns
t_{ACE}	Chip Enable Access Time[3]	—	35	ns
t_{AOE}	Output Enable Access Time	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	ns
t_{LZ}	Output Low Z Time[1, 2]	3	—	ns
t_{HZ}	Output High Z Time[1, 2]	—	15	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	ns

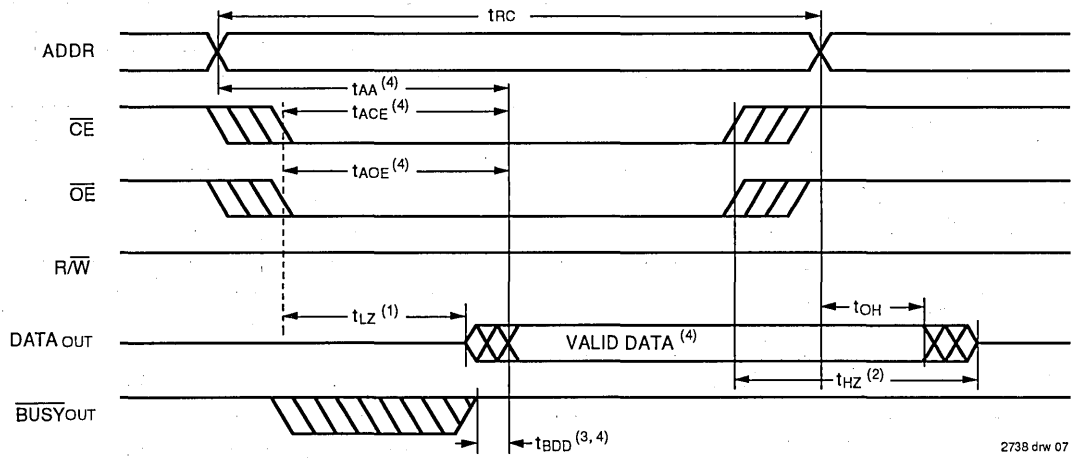
Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL ONLY Min.	IDT7005X70 MIL ONLY Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2738 tbl 11

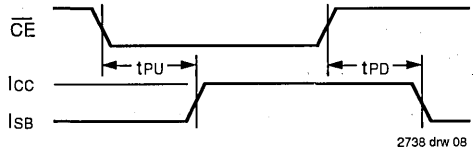
6

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	Max.	Unit
WRITE CYCLE				
t_{WC}	Write Cycle Time	35	—	ns
t_{EW}	Chip Enable to End of Write(3)	30	—	ns
t_{AW}	Address Valid to End of Write	30	—	ns
t_{AS}	Address Set-up Time(3)	0	—	ns
t_{WP}	Write Pulse Width	30	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	ns
t_{HZ}	Output High Z Time(1, 2)	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	ns
t_{WZ}	Write Enable to Output in High Z(1, 2)	—	15	ns
t_{OW}	Output Active from End of Write(1, 2, 4)	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	ns

Symbol	Parameter	IDT7005X45 Min.	Max.	IDT7005X55 Min.	Max.	IDT7005X70 MIL. ONLY Min.	Max.	Unit
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
t_{AW}	Address Valid to End of Write	40	—	45	—	50	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	40	—	ns
t_{HZ}	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

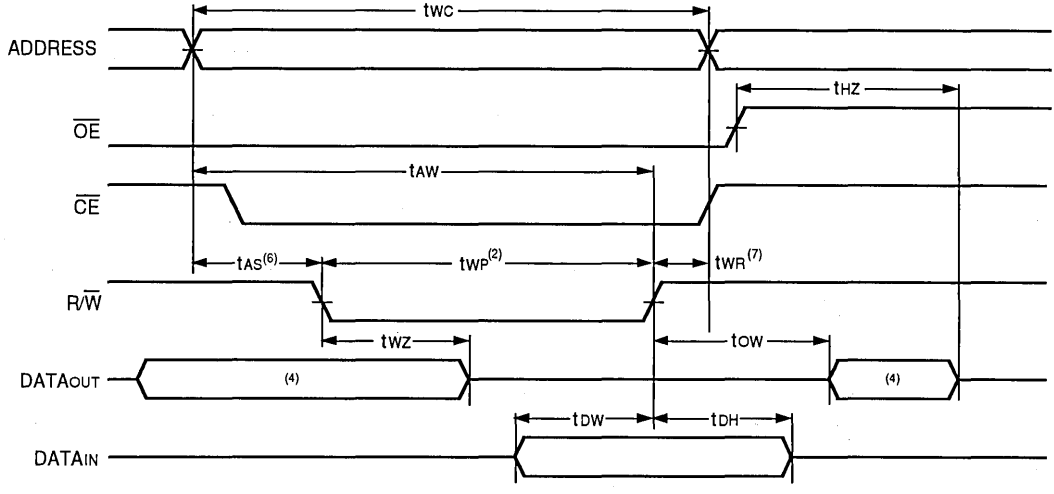
NOTES:

2738 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. X in part numbers indicates power rating (S or L).

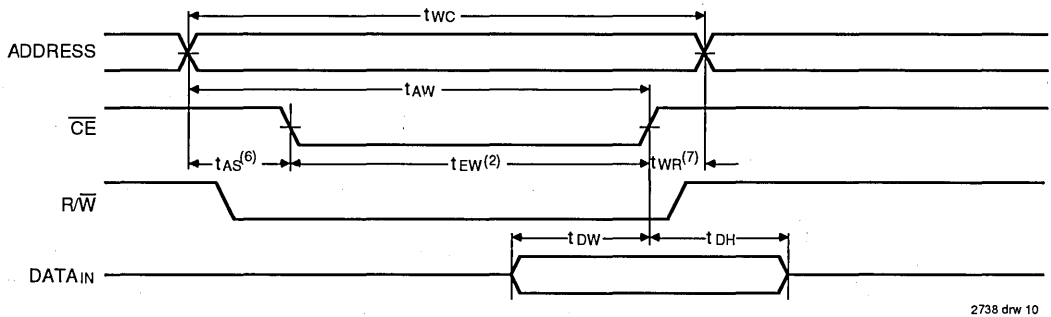
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



2738 drw 09

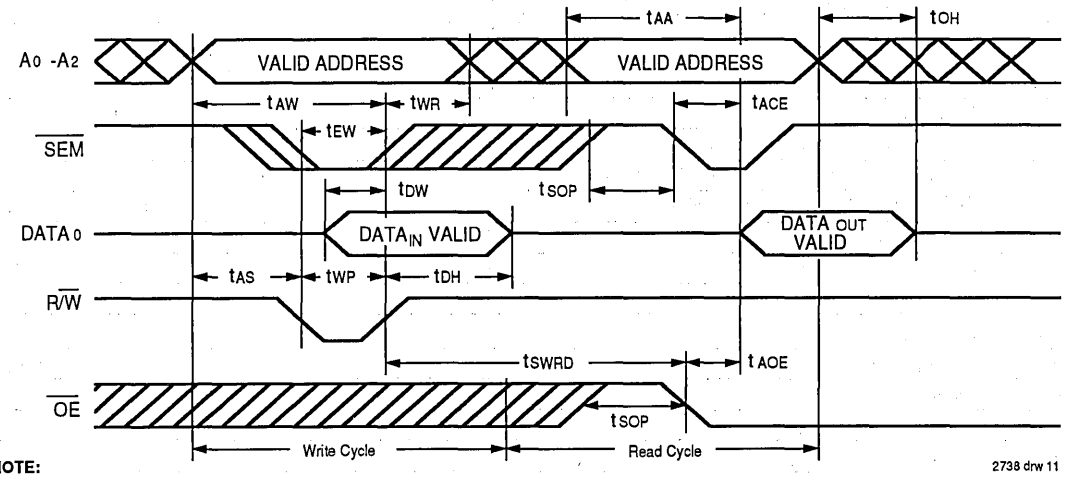
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



2738 drw 10

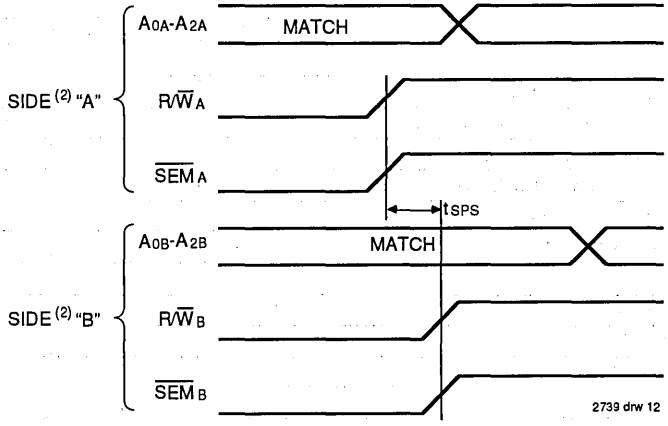
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or byte control.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, R/$\overline{W}$, or byte control.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

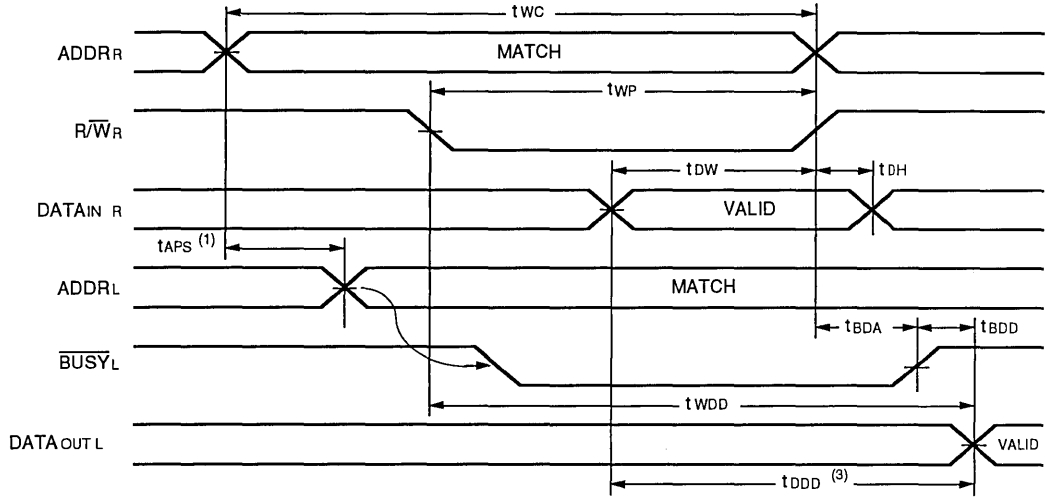
Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)				
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	25	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)				
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	25	—	ns
PORT-TO-PORT DELAY TIMING				
t_{WDD}	Write Pulse to Data Delay(1)	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	45	ns

Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	—	40	—	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	30	—	40	—	40	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	25	—	35	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay(1)	—	70	—	80	—	95	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	55	—	65	—	80	ns

NOTES: 2738 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H) or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)"".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual) or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

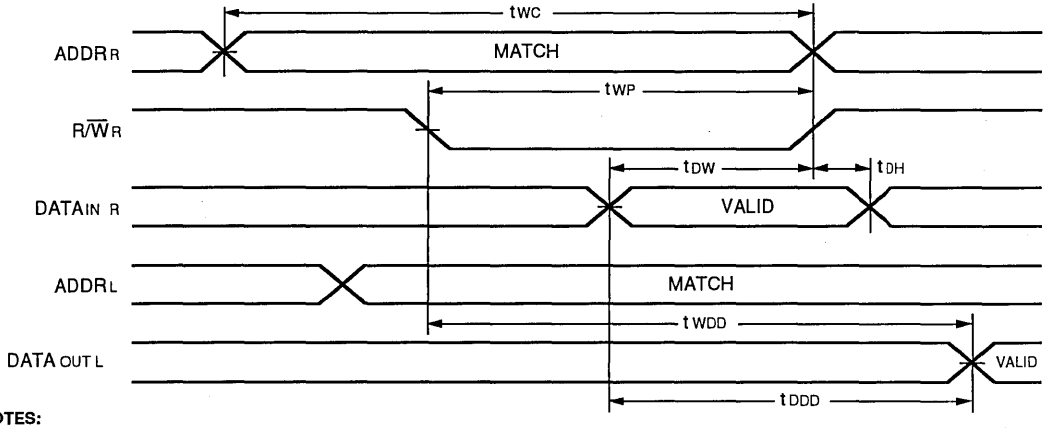
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2738 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

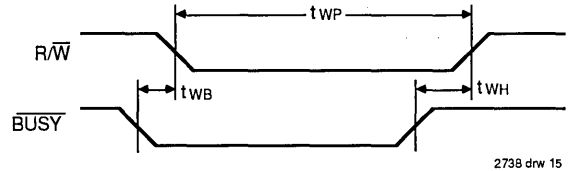
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



2738 drw 14

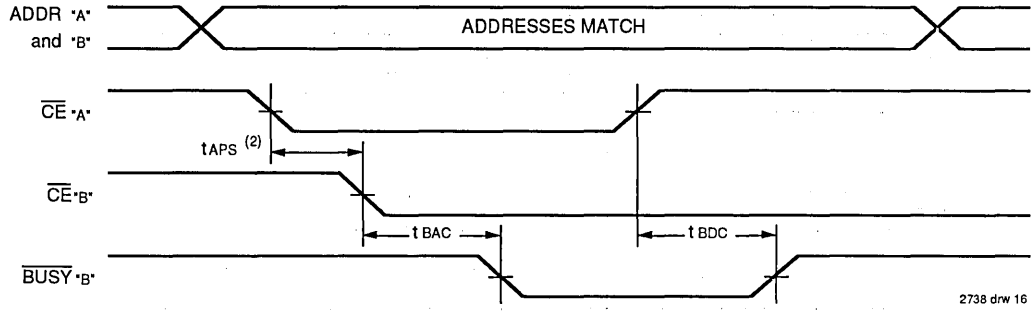
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

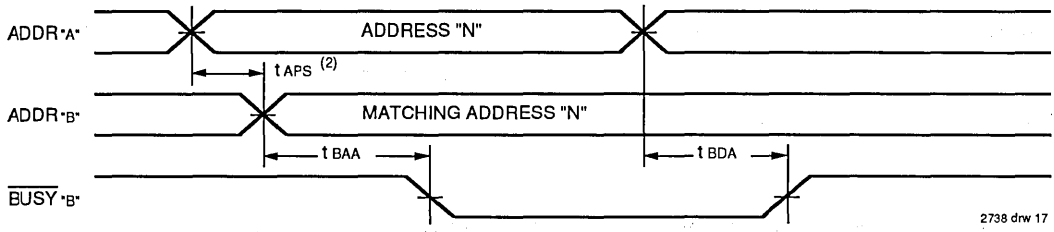


2738 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

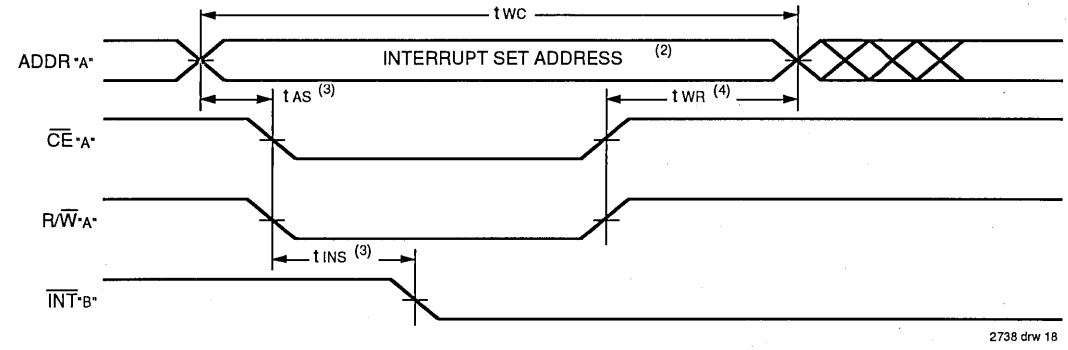
Symbol	Parameter	IDT7005X35 COM'L ONLY Min.	IDT7005X35 COM'L ONLY Max.	Unit
INTERRUPT TIMING				
tAS	Address Set-up Time	0	—	ns
tWR	Write Recovery Time	0	—	ns
tINS	Interrupt Set Time	—	30	ns
tINR	Interrupt Reset Time	—	30	ns

Symbol	Parameter	IDT7005X45 Min.	IDT7005X45 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

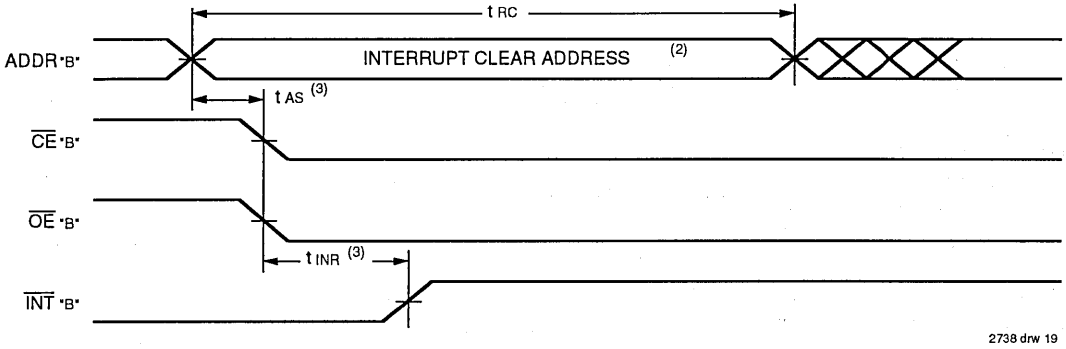
NOTE:
1. "x" in part numbers indicates power rating (S or L).

2738 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2738 drw 18



2738 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

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TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

2738 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2738 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}x$ outputs on the IDT7005 are push pull, not open drain outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2738 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7005.

FUNCTIONAL DESCRIPTION

The IDT7005 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7005 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (8 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

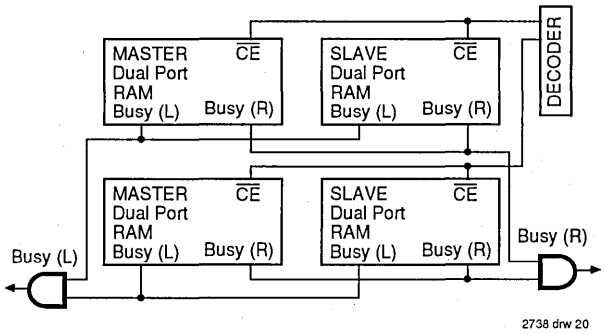

Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7005 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7005 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7005 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7005 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7005 is an extremely fast dual-port 8K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7005 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7005's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7005 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

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An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7005 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be

reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7005's dual-port RAM. Say the 8K x 8 RAM was to be divided into two 4K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

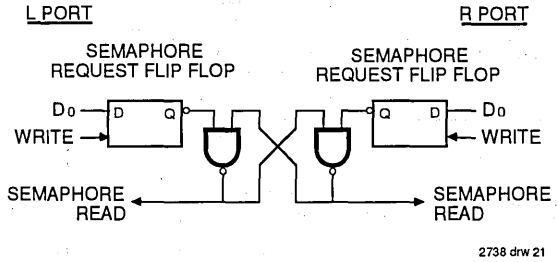


Figure 4. IDT7005 Semaphore Logic

Integrated Device Technology, Inc.

HIGH-SPEED 4K x 16 DUAL-PORT STATIC RAM

IDT7024S/L

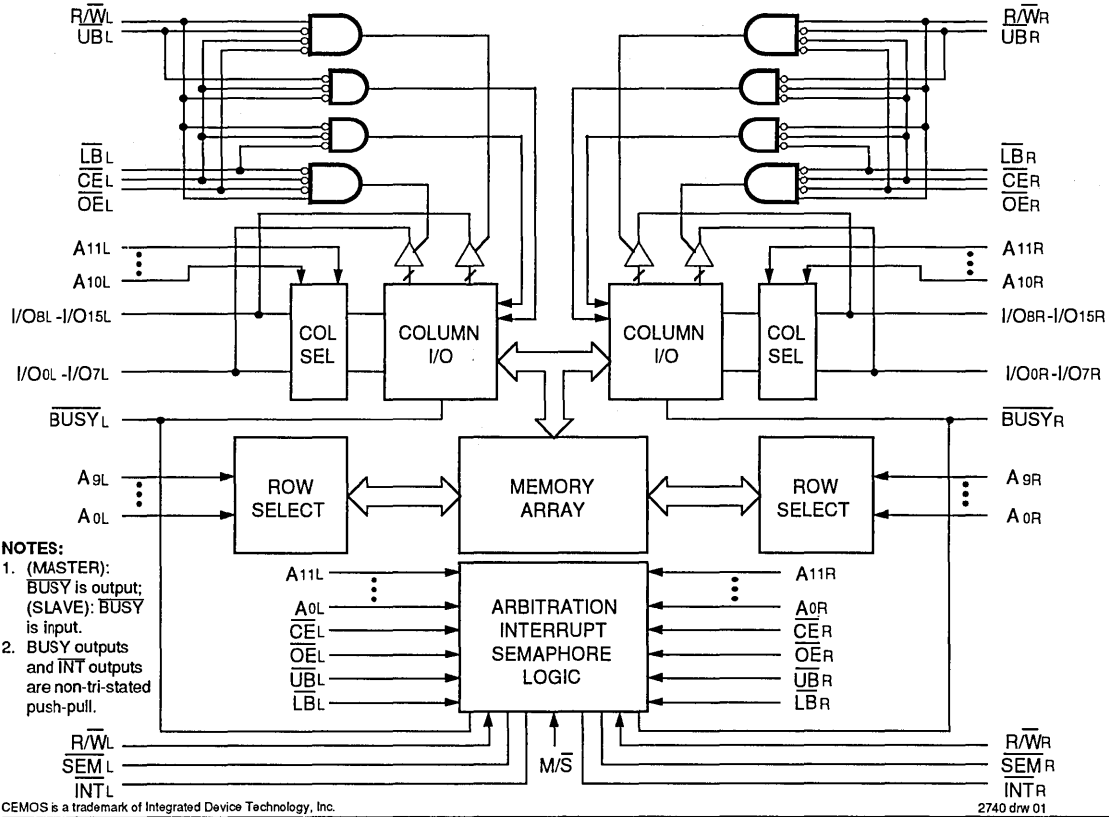
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/30/35/45/55ns (max.)
- Low-power operation
  - — IDT7024S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7024L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7024 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack and PLCC
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7024 is a high-speed 4K x 16 dual-port static RAM. The IDT7024 is designed to be used as a stand-alone 64K-bit

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

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2740 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES **APRIL 1992**

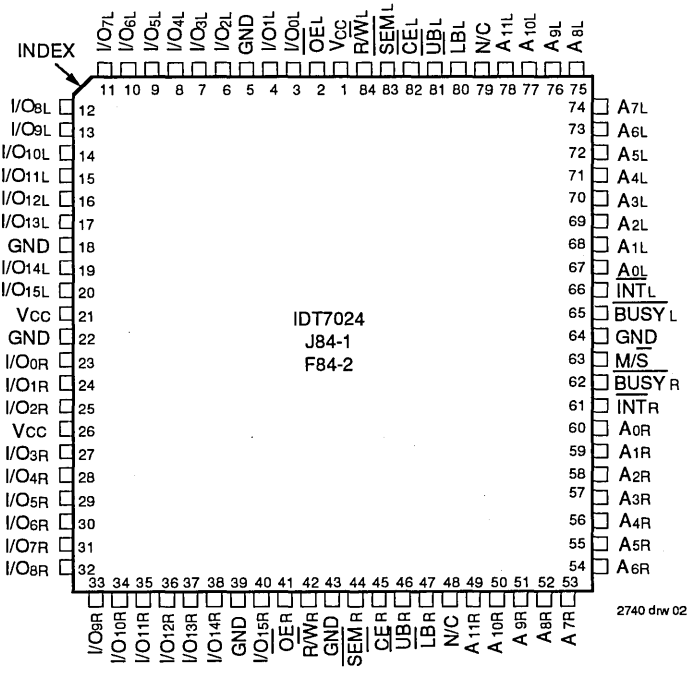
dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7024 is packaged in a ceramic 84-pin PGA, an 84-pin quad flatpack, and a PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

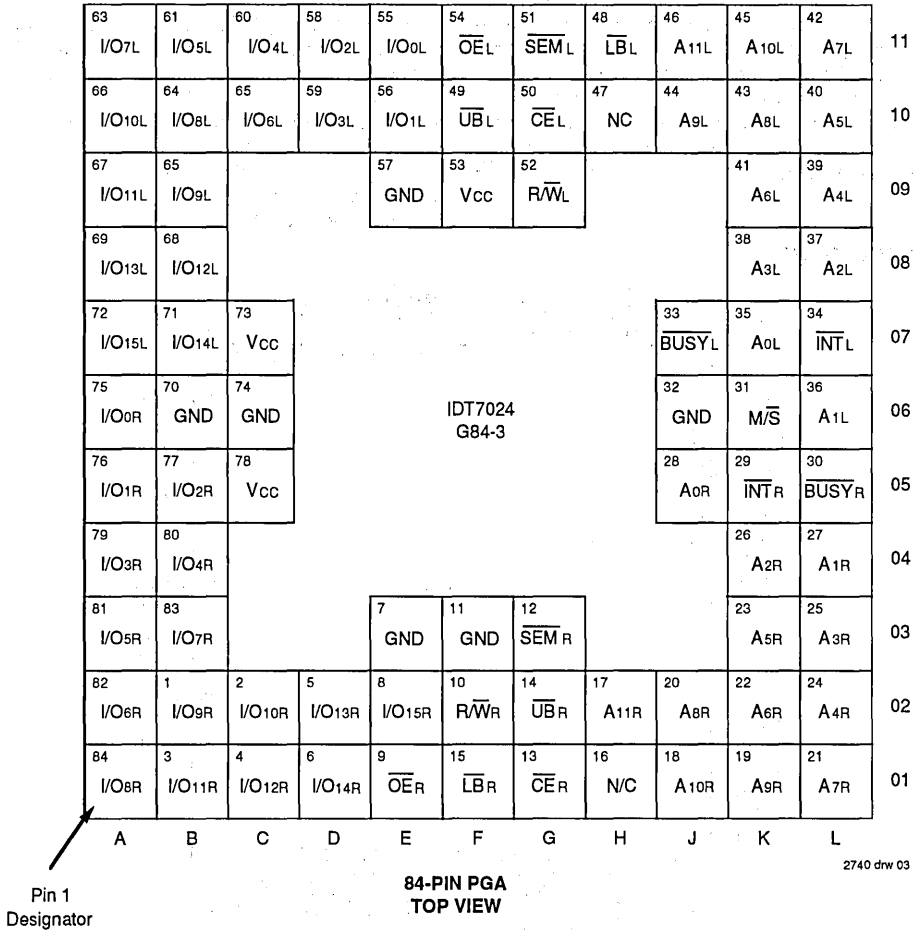
PIN CONFIGURATIONS



PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



84-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{11L}$	$A_{0R} - A_{11R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2740 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected: Power Down
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{11L} \neq A_{0R} — A_{11R}$

2740 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2740 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

2740 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2740 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

2740 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2740 tbl 03

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7024S		IDT7024L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2740 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X25 COM'L ONLY		7024X30 COM'L ONLY		7024X35		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	160	400	mA
				L	—	—	—	—	160	340	
			COM'L.	S	170	360	165	350	160	340	
				L	170	310	165	300	160	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$ $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	20	85	mA
				L	—	—	—	—	20	65	
			COM'L.	S	25	70	22	70	20	70	
				L	25	50	22	50	20	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	—	—	95	290	mA
				L	—	—	—	—	95	250	
			COM'L.	S	105	250	100	250	95	240	
				L	105	220	100	215	95	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	90	260	mA
				L	—	—	—	—	90	215	
			COM'L.	S	100	230	95	230	90	220	
				L	100	190	95	190	90	180	

NOTES:

2740 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At V_{CC} ≤ 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X45 Typ.[2]	7024X45 Max.	7024X55 Typ.[2]	7024X55 Max.	7024X70 MIL ONLY Typ.[2]	7024X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open, $\overline{SEM} \ge V_{IH}$, f = f_{MAX}[3]	MIL.	S	155	400	150	395	140	390	mA
				L	155	340	150	335	140	330	
			COM'L.	S	155	340	150	335	—	—	
				L	155	290	150	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$, $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$, f = f_{MAX}[3]	MIL.	S	16	85	13	85	10	85	mA
				L	16	65	13	65	10	65	
			COM'L.	S	16	70	13	70	—	—	
				L	16	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$, Active Port Outputs Open, f = f_{MAX}[3], $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	90	290	85	290	80	290	mA
				L	90	250	85	250	80	250	
			COM'L.	S	90	240	85	240	—	—	
				L	90	210	85	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4], $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V, $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	85	260	80	260	75	260	mA
				L	85	215	80	215	75	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V	COM'L.	S	85	220	80	220	—	—	
		Active Port Outputs Open, f = f_{MAX}[3]		L	85	180	80	180	—	—	

NOTES:

2740 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

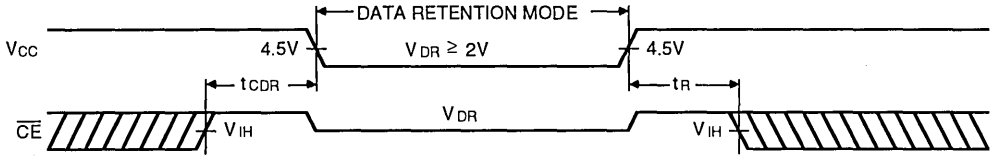
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2740 tbl 09

DATA RETENTION WAVEFORM

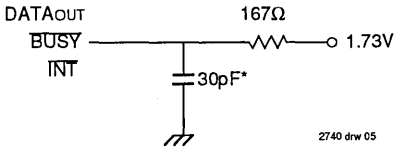


2740 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

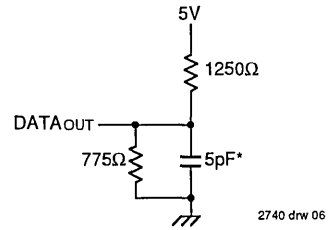
2740 tbl 10



2740 drw 05

* Including scope and jig.

Figure 1. Equivalent Output Load



2740 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	30	—	35	—	ns
tAA	Address Access Time	—	25	—	30	—	35	ns
tACE	Chip Enable Access Time[3]	—	25	—	30	—	35	ns
tABE	Byte Enable Access Time[3]	—	25	—	30	—	35	ns
tAOE	Output Enable Access Time	—	13	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	15	—	15	—	ns

Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tABE	Byte Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2740 tbl 11

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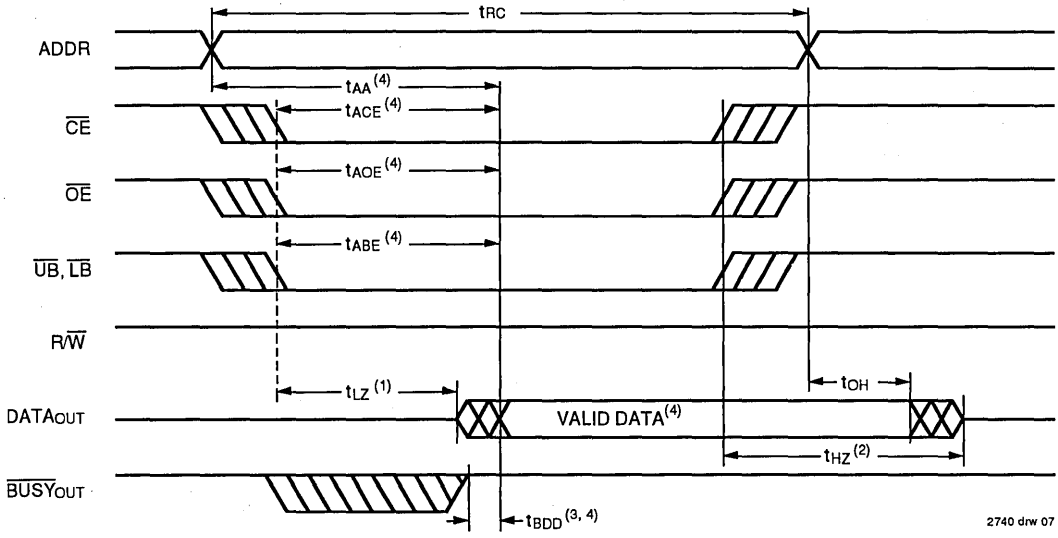
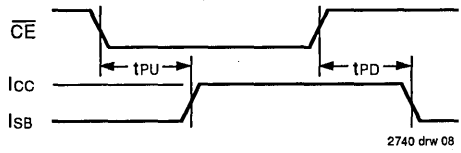
WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted firs $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7024X25 COM'L ONLY		IDT7024X30 COM'L ONLY		IDT7024X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	30	—	35	—	ns
tEW	Chip Enable to End of Write(3)	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	—	15	—	15	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	—	15	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

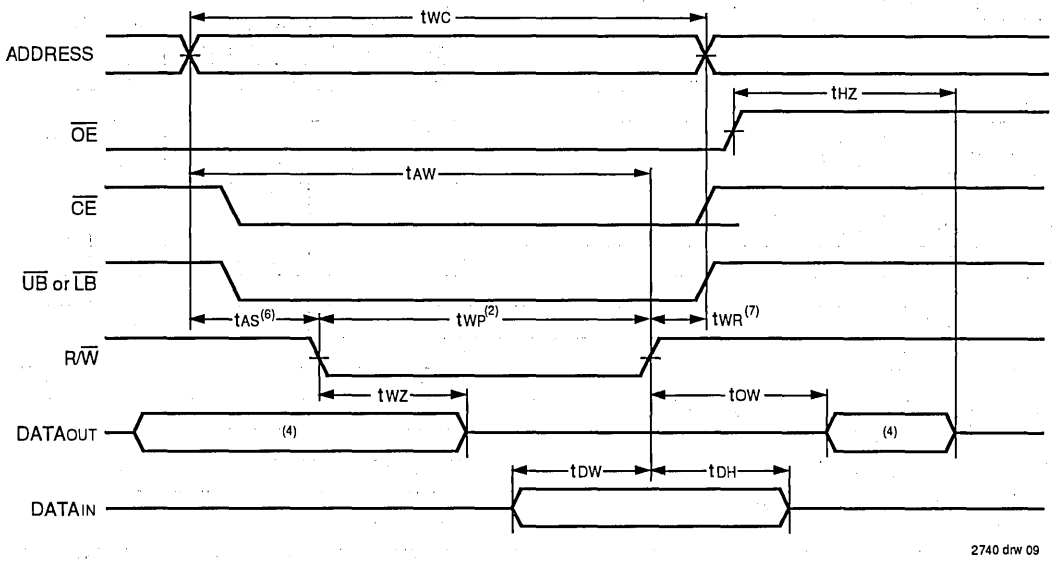
Symbol	Parameter	IDT7024X45		IDT7024X55		IDT7024X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

NOTES:

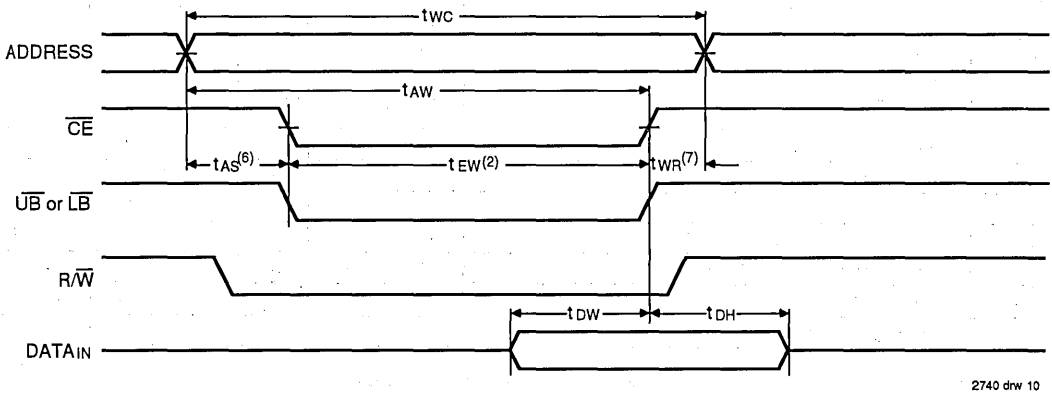
2740 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)

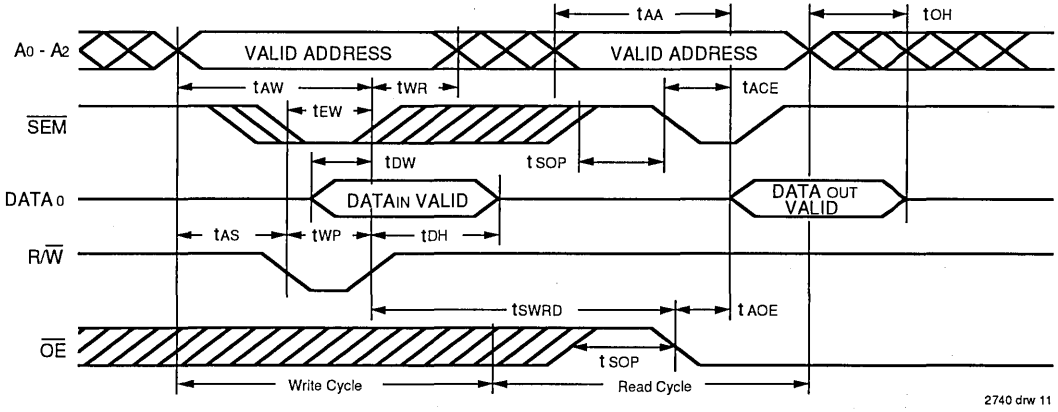


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,3,5,8)



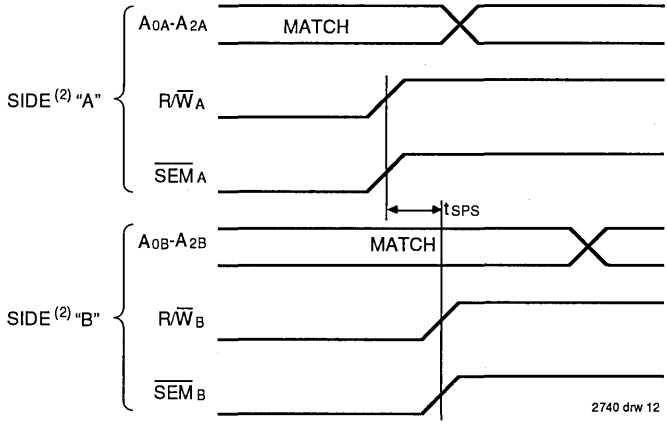
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$ or byte control.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, R/$\overline{W}$ or byte control.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	IDT7024X25 COM'L ONLY Min.	IDT7024X25 COM'L ONLY Max.	IDT7024X30 COM'L ONLY Min.	IDT7024X30 COM'L ONLY Max.	IDT7024X35 Min.	IDT7024X35 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	25	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Low	—	20	—	25	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip High	—	17	—	20	—	25	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	17	—	20	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(1)	—	50	—	55	—	60	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	35	—	40	—	45	ns

Symbol	Parameter	IDT7024X45 Min.	IDT7024X45 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL. ONLY Min.	IDT7024X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(1)	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	55	—	65	—	80	ns

NOTES:

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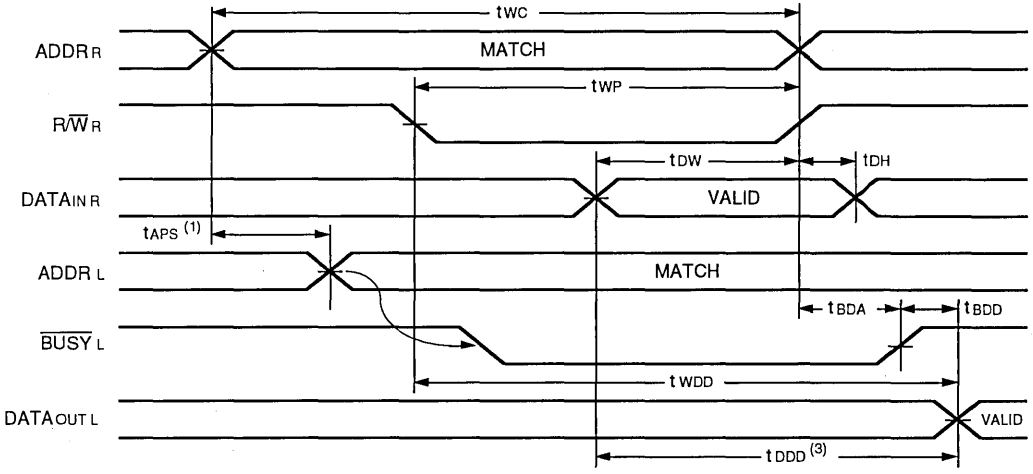
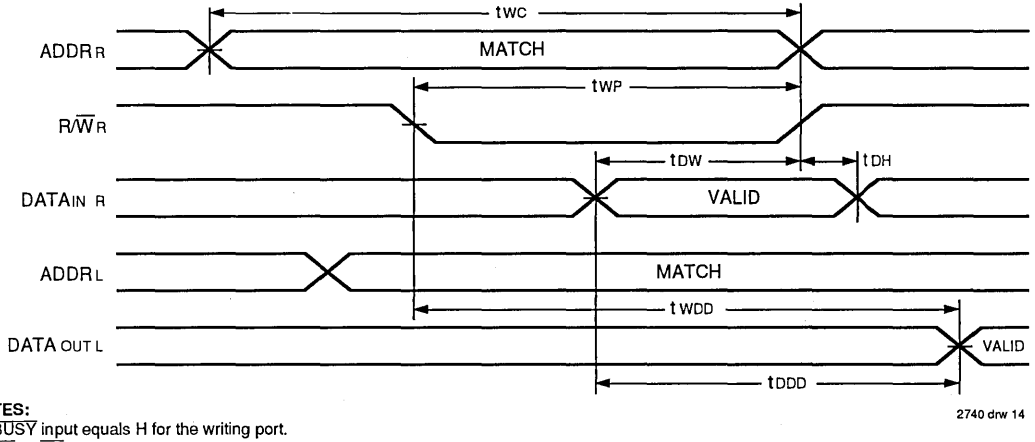
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



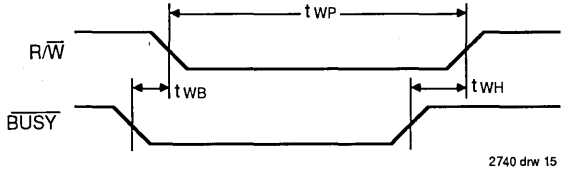
NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)

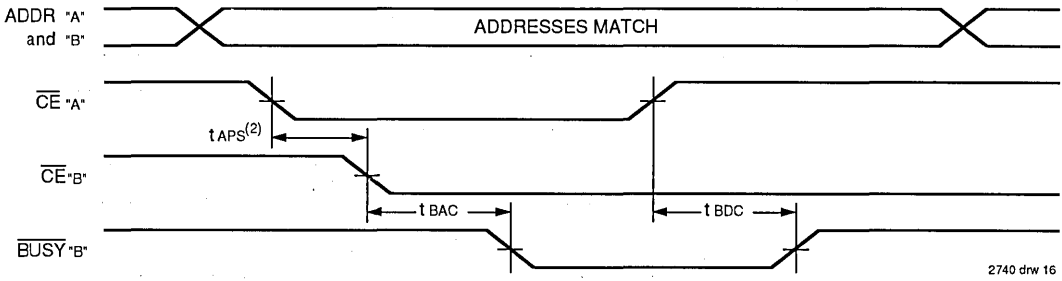


NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

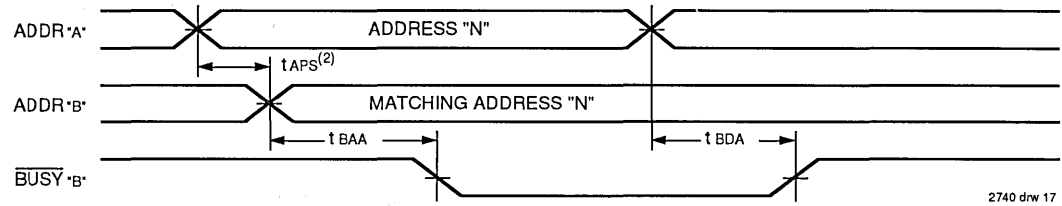
TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)



WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

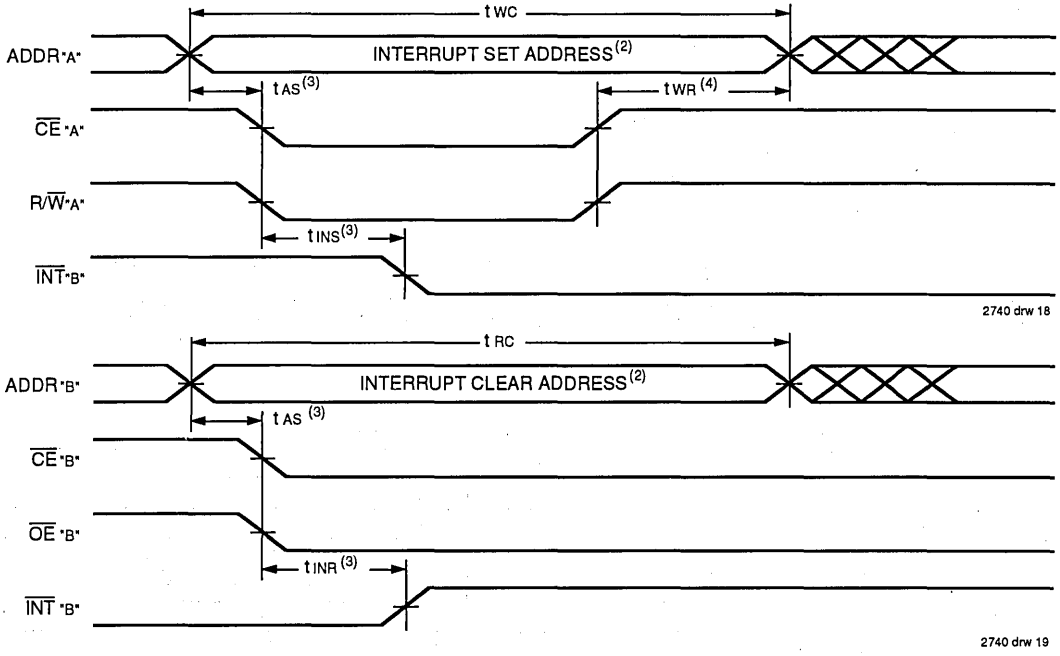
Symbol	Parameter	IDT7024X25 COM'L ONLY Min.	IDT7024X25 COM'L ONLY Max.	IDT7024X30 COM'L ONLY Min.	IDT7024X30 COM'L ONLY Max.	IDT7024X35 Min.	IDT7024X35 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	ns

Symbol	Parameter	IDT7024X45 Min.	IDT7024X45 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL. ONLY Min.	IDT7024X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

NOTE:
1. "x" in part numbers indicates power rating (S or L).

2740 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

6

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{11L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{11R}	$\overline{INT}_R$	Function
L	L	X	FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

2740 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{11L} A_{0R}-A_{11R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2740 tbl 16

NOTES:

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7024 are push pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2740 tbl 17

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7024.

FUNCTIONAL DESCRIPTION

The IDT7024 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7024 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location FFE (HEX). The left port clears the interrupt by reading address location FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location FFF. The message (16 bits) at FFE or FFF is user-defined. If the interrupt function is not used, address locations FFE and FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

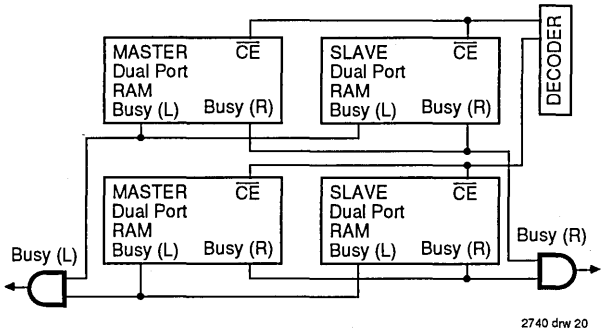


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7024 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7024 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7024 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7024 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7024 is an extremely fast dual-port 4K x 16 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7024 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7024's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7024 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

6

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7024 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be

reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7024's dual-port RAM. Say the 4K x 16 RAM was to be divided into two 2K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

6

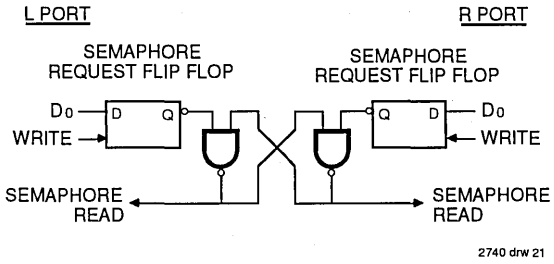


Figure 4. IDT7024 Semaphore Logic

Integrated Device Technology, Inc.

HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

IDT7006S/L

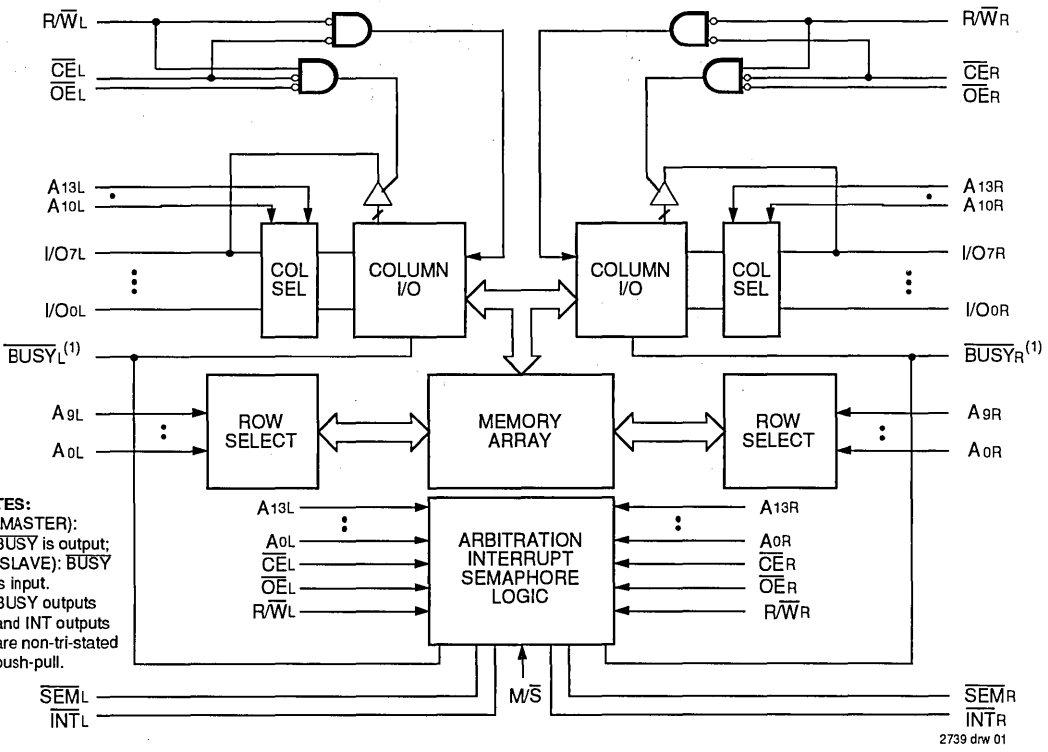
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55ns (max.)
- Low-power operation
  - — IDT7006S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7006L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, LCC and PLCC
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7006 is a high-speed 16K x 8 dual-port static RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 16-bit-or-more word systems. Using the IDT

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and INT outputs are non-tri-stated push-pull.

CEMOS is a trademark of Integrated Device Technology, Inc.

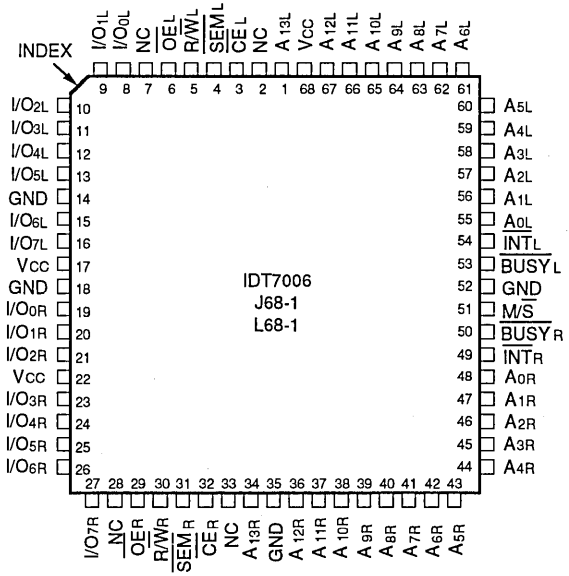
MASTER/SLAVE dual-port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 750mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7006 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a LCC, and a PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS



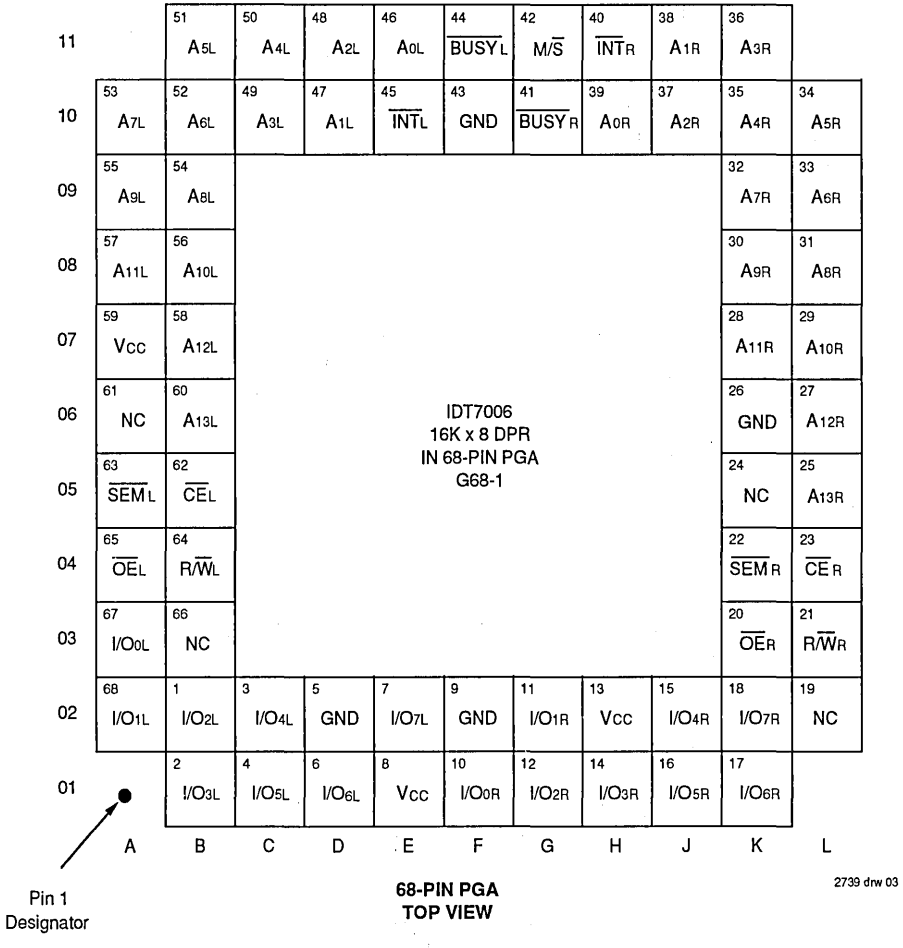
2739 drw 02

LCC/PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

6

PIN CONFIGURATIONS (Continued)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2739 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} - A_{13L} \neq A_{0R} - A_{13R}$

2739 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2739 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

2739 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2739 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2739 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. $V_{IL} \geq$ -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

2739 tbl 06

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7006S		IDT7006L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2739 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X35 COM'L ONLY Typ.[2]	7006X35 COM'L ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open; $\overline{SEM} \ge V_{IH}$; f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	160	340	
				L	160	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$; $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$; f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	20	70	
				L	20	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$; Active Port Outputs Open; f = f_{MAX}[3]; $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	95	240	
				L	95	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V; $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]; $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	1.0	15	
				L	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V; $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V; $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V; Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	mA
				L	—	—	
			COM'L.	S	90	220	
				L	90	180	

2739 tbl 08

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At Vcc≤2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X45 Typ.[2]	7006X45 Max.	7006X55 Typ.[2]	7006X55 Max.	7006X70 MIL ONLY Typ.[2]	7006X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current	$\overline{CE} \le V_{IL}$, Outputs Open	MIL.	S	155	400	150	395	140	390	mA
		$\overline{SEM} \ge V_{IH}$		L	155	340	150	335	140	330	
	(Both Ports Active)	$f = f_{MAX}$[3]	COM'L.	S	155	340	150	335	—	—	
				L	155	290	150	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$	MIL.	S	16	85	13	85	10	85	mA
		$\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$		L	16	65	13	65	10	65	
	Level Inputs)	$f = f_{MAX}$[3]	COM'L.	S	—	70	13	70	—	—	
				L	—	50	13	50	—	—	
I_{SB2}	Standby Current	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$	MIL.	S	90	290	85	290	80	290	mA
	(One Port — TTL	Active Port Outputs Open		L	90	250	85	250	80	250	
	Level Inputs)	$f = f_{MAX}$[3]	COM'L.	S	90	240	85	240	—	—	
		$\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$		L	90	210	85	210	—	—	
I_{SB3}	Full Standby Current (Both Ports — All	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
	CMOS Level Inputs)	$V_{IN} \ge V_{CC}$ - 0.2V or	COM'L.	S	1.0	15	1.0	15	—	—	
		$V_{IN} \le 0.2V$, $f = 0$[4]		L	0.2	5	0.2	5	—	—	
		$\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V									
I_{SB4}	Full Standby Current (One Port — All	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V	MIL.	S	85	260	80	260	75	260	mA
	CMOS Level Inputs)	$\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V		L	85	215	80	215	75	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or	COM'L.	S	85	220	80	220	—	—	
		$V_{IN} \le 0.2V$									
		Active Port Outputs Open, $f = f_{MAX}$[3]		L	85	180	80	180	—	—	

NOTES:

2739 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

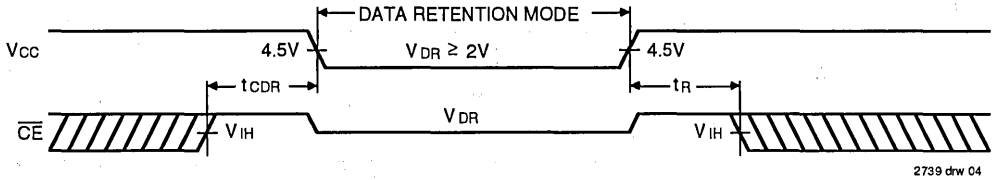
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2739 tbl 09

DATA RETENTION WAVEFORM

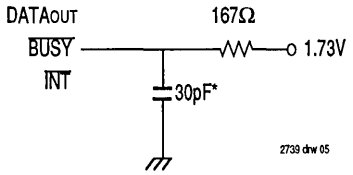


2739 drw 04

AC TEST CONDITIONS

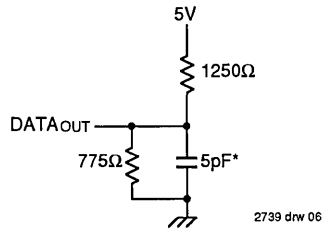
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2739 tbl 10



2739 drw 05

Figure 1. Equivalent Output Load



2739 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
READ CYCLE				
t_{RC}	Read Cycle Time	35	—	ns
t_{AA}	Address Access Time	—	35	ns
t_{ACE}	Chip Enable Access Time[3]	—	35	ns
t_{AOE}	Output Enable Access Time	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	ns
t_{LZ}	Output Low Z Time[1, 2]	3	—	ns
t_{HZ}	Output High Z Time[1, 2]	—	15	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL ONLY Min.	IDT7006X70 MIL ONLY Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2739 tbl 11

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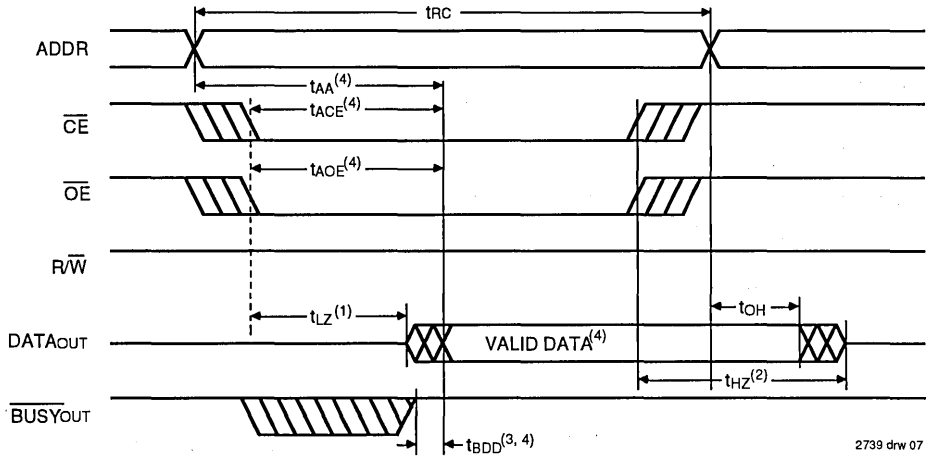
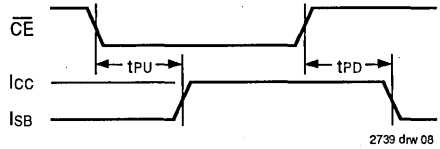
WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{ABE}, t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7006X35 Min.	IDT7006X35 Max.	Unit
WRITE CYCLE				
tWC	Write Cycle Time	35	—	ns
tEW	Chip Enable to End of Write(3)	30	—	ns
tAW	Address Valid to End of Write	30	—	ns
tAS	Address Set-up Time(3)	0	—	ns
tWP	Write Pulse Width	30	—	ns
tWR	Write Recovery Time	0	—	ns
tDW	Data Valid to End of Write	25	—	ns
tHZ	Output High Z Time(1, 2)	—	15	ns
tDH	Data Hold Time(4)	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	15	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	ns

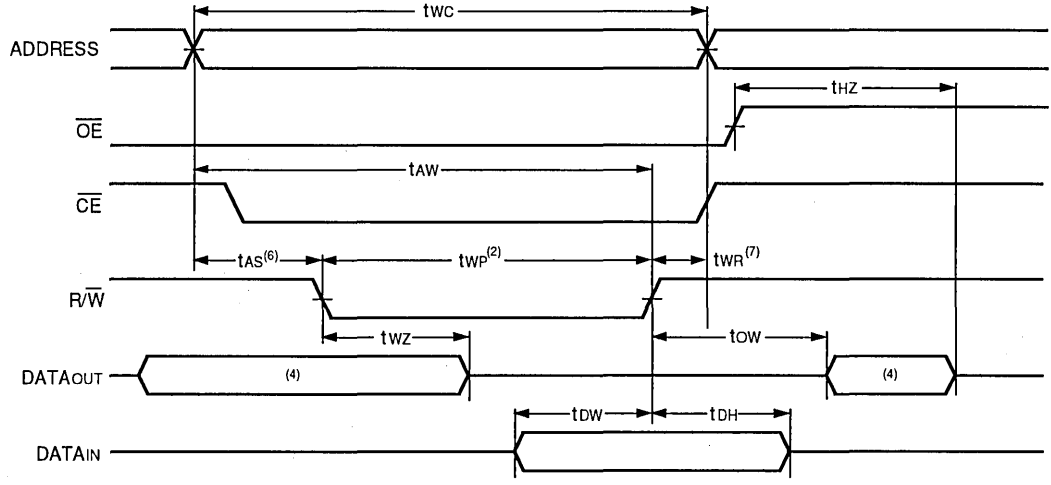
Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
tAW	Address Valid to End of Write	40	—	45	—	50	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	25	—	30	—	40	—	ns
tHZ	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
tOW	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

NOTES:

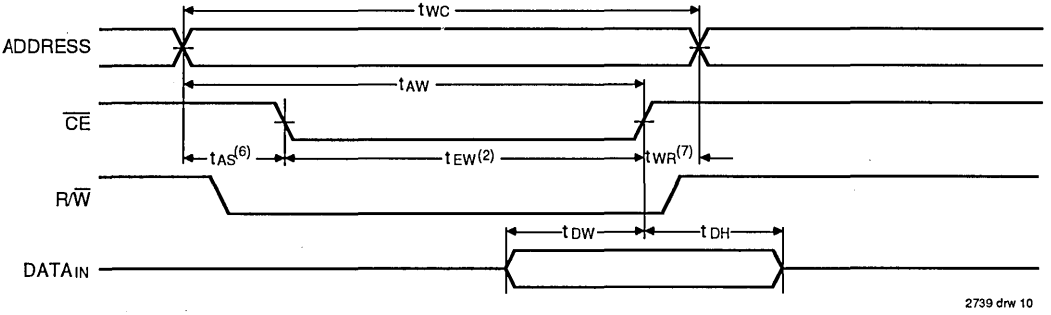
2739 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)

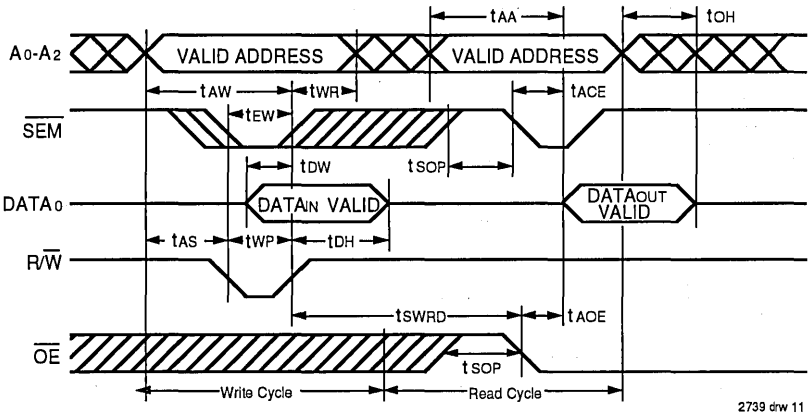


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



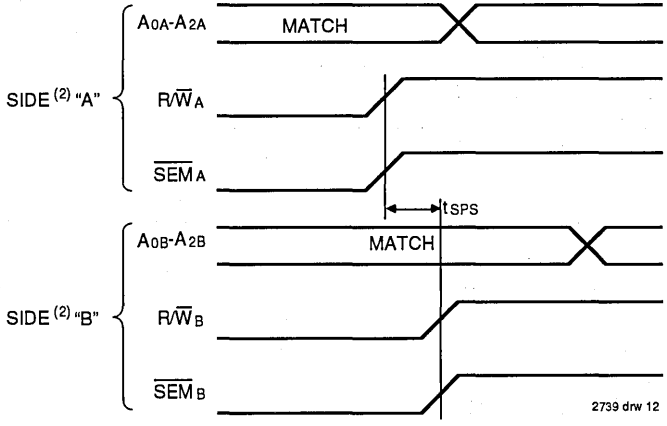
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or byte control.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, R/$\overline{W}$, or byte control.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

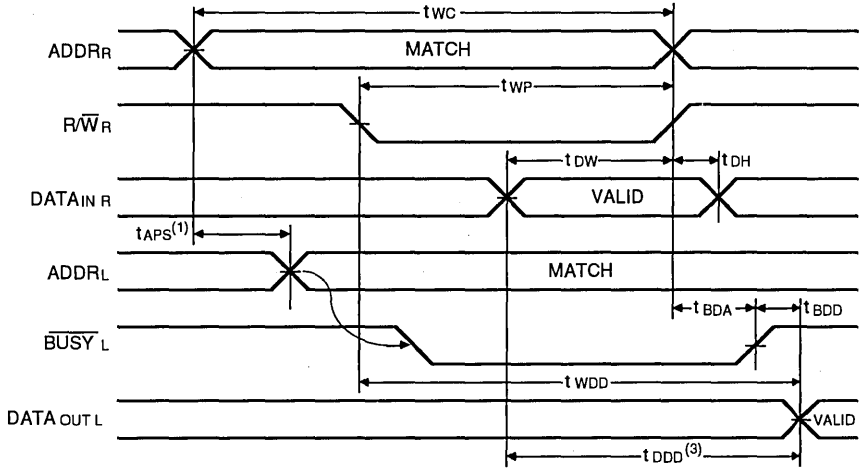
Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)				
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	25	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)				
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	ns
PORT-TO-PORT DELAY TIMING				
tWDD	Write Pulse to Data Delay[1]	—	60	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	55	—	65	—	80	ns

NOTES: 2739 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

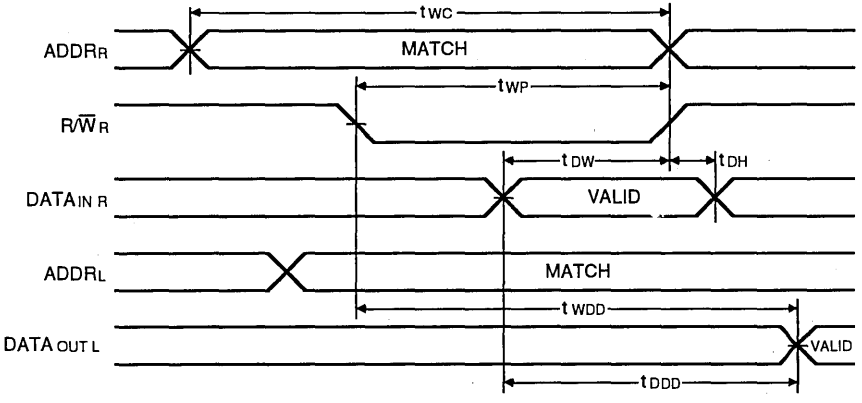
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2739 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = L$
3. $\overline{OE}$ = L for the reading port.

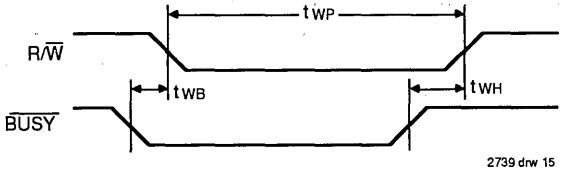
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2](M/$\overline{S}$ = L)



2739 drw 14

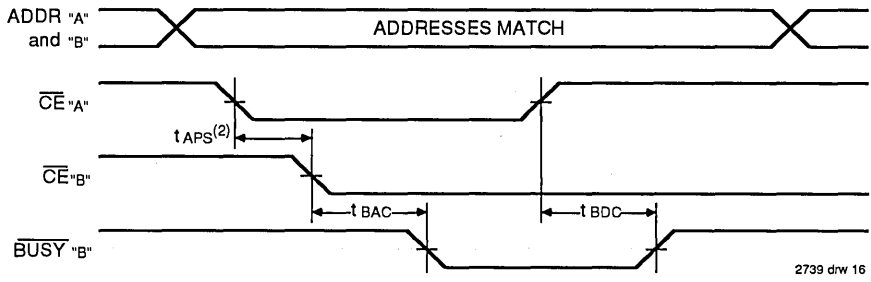
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L = \overline{CE}_R = L$

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

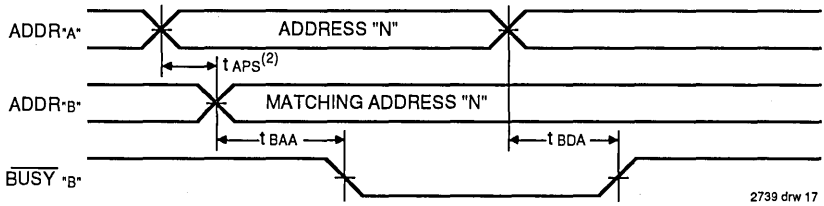


2739 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

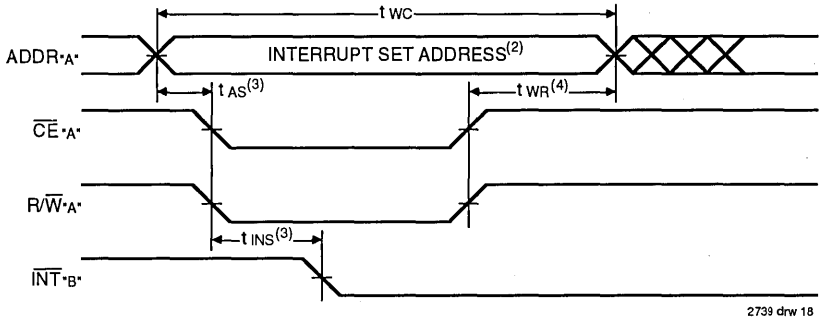
Symbol	Parameter	IDT7006X35 COM'L ONLY Min.	IDT7006X35 COM'L ONLY Max.	Unit
INTERRUPT TIMING				
tAS	Address Set-up Time	0	—	ns
tWR	Write Recovery Time	0	—	ns
tINS	Interrupt Set Time	—	30	ns
tINR	Interrupt Reset Time	—	30	ns

Symbol	Parameter	IDT7006X45 Min.	IDT7006X45 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

2739 tbl 14

WAVEFORM OF INTERRUPT TIMING(1)



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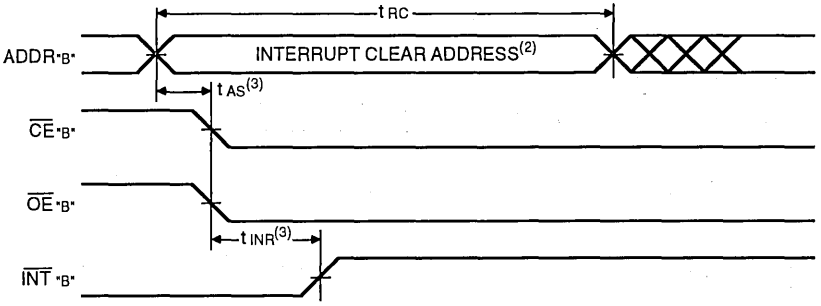


2739 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

6

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG(1)

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{13L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{13R}	$\overline{INT}_R$	Function
L	L	X	3FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

2739 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2739 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7006 are push pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2739 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7006.

FUNCTIONAL DESCRIPTION

The IDT7006 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7006 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FFE (HEX). The left port clears the interrupt by reading address location 3FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

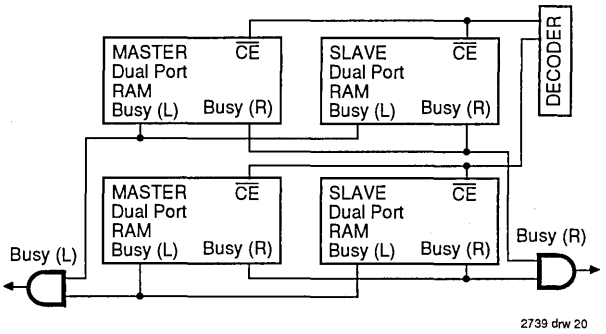


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7006 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7006 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7006 RAM array in width while using busy logic, one master part is used to decide which side of the RAMs array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7006 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7006 is an extremely fast dual-port 16K x 8 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7006 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7006s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7006 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7006 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be

reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7006's dual-port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

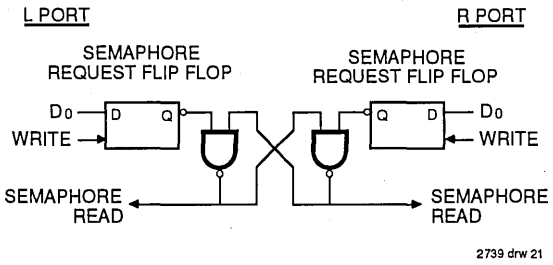


Figure 4. IDT7006 Semaphore Logic

Integrated Device Technology, Inc.

HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

IDT7025S/L

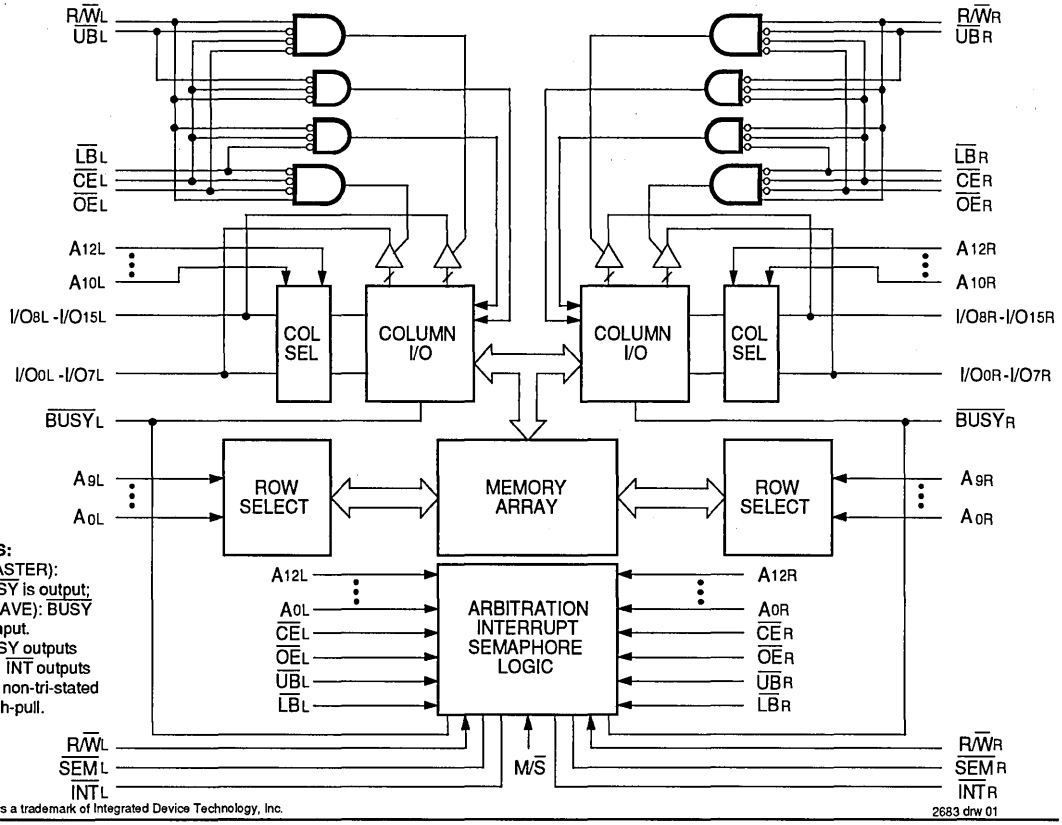
FEATURES:

- True dual-ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/45/55/70ns (max.)
  - — Commercial: 25/30/35/45/55ns (max.)
- Low-power operation
  - — IDT7025S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7025L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack and PLCC
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7025 is a high-speed 8K x 16 dual-port static RAM. The IDT7025 is designed to be used as a stand-alone 128K-

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

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2683 drw 01

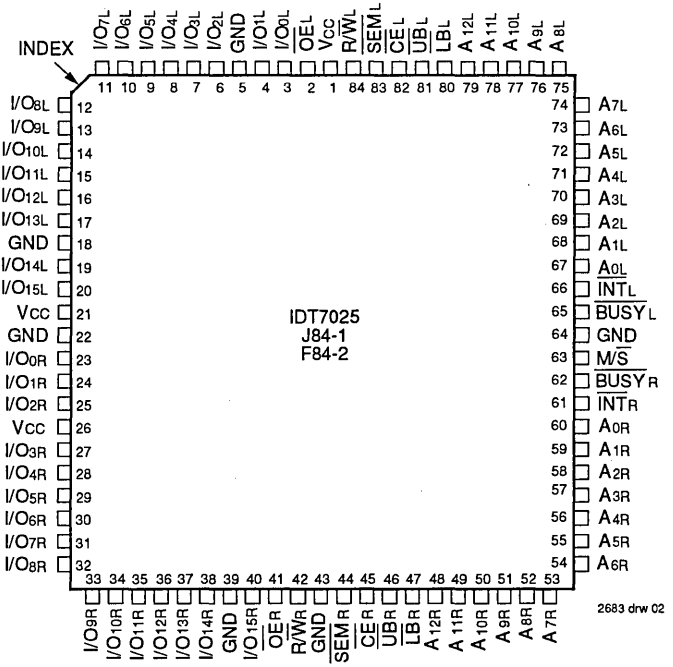
bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7025 is packaged in a ceramic 84-pin PGA, an 84-pin quad flatpack, and a PLCC. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

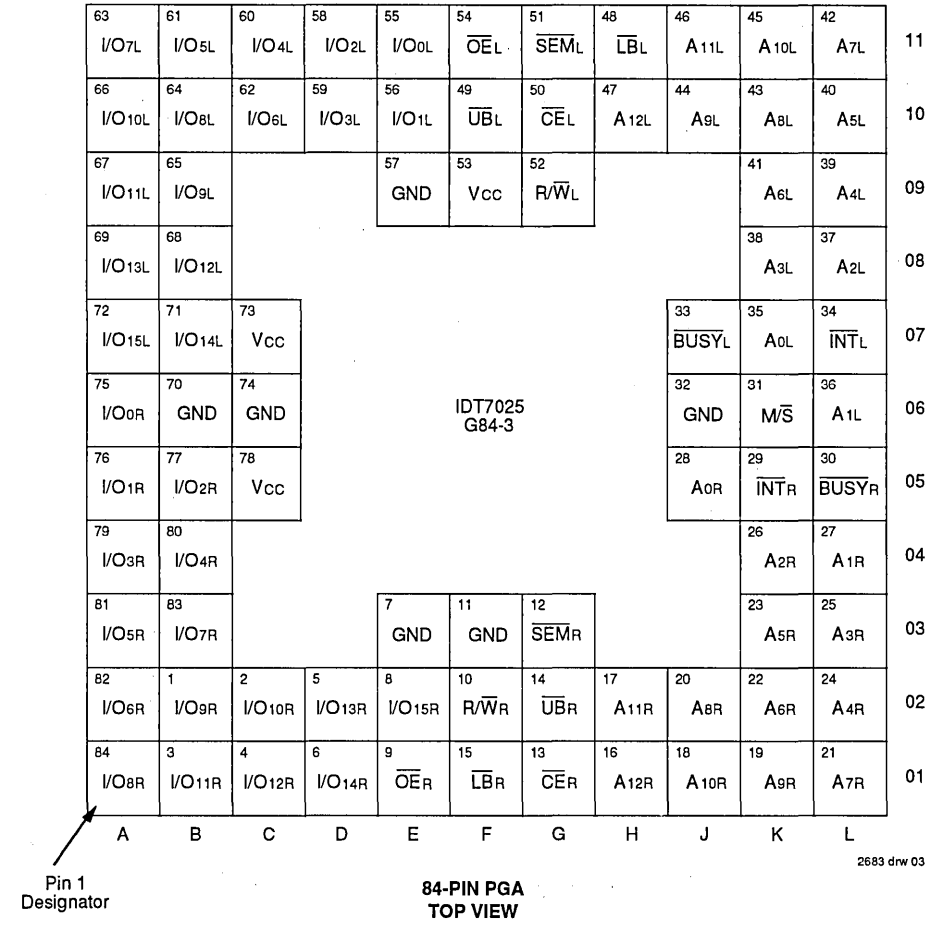
PIN CONFIGURATIONS



PLCC/FLATPACK
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN CONFIGURATIONS (Continued)



84-PIN PGA
TOP VIEW

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2683 tbl 18

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected: Power Down
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{12L} \neq A_{0R} — A_{12R}$

2683 tbl 01

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2683 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V.

2683 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2683 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL≥ -3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

2683 tbl 06

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2682 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7025S		IDT7025L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2683 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X25 COM'L ONLY		7025X30 COM'L ONLY		7025X35		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	160	400	mA
				L	—	—	—	—	160	340	
			COM'L.	S	170	360	165	350	160	340	
				L	170	310	165	300	160	290	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$ $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	20	85	mA
				L	—	—	—	—	20	65	
			COM'L.	S	25	70	22	70	20	70	
				L	25	50	22	50	20	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$ Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{IH}$	MIL.	S	—	—	—	—	95	290	mA
				L	—	—	—	—	95	250	
			COM'L.	S	105	250	100	250	95	240	
				L	105	220	100	215	95	210	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	90	260	mA
				L	—	—	—	—	90	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	100	230	95	230	90	220	
				L	100	190	95	190	90	180	

2653 tbl 08

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At Vcc≤2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X45 Typ.[2]	7025X45 Max.	7025X55 Typ.[2]	7025X55 Max.	7025X70 MIL ONLY Typ.[2]	7025X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$, Outputs Open $\overline{SEM} \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	155	400	150	395	140	390	mA
				L	155	340	150	335	140	330	
			COM'L.	S	155	340	150	335	—	—	
				L	155	290	150	285	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R \ge V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$ $f = f_{MAX}$[3]	MIL.	S	16	85	13	85	10	85	mA
				L	16	65	13	65	10	65	
			COM'L.	S	16	70	13	70	—	—	
				L	16	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ Active Port Outputs Open $f = f_{MAX}$[3] $\overline{SEM}_R = \overline{SEM}_L \ge V_{IH}$	MIL.	S	90	290	85	290	80	290	mA
				L	90	250	85	250	80	250	
			COM'L.	S	90	240	85	240	—	—	
				L	90	210	85	210	—	—	
I_{SB3}	Full Standby Current (Bcth Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ - 0.2V $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$, f = 0[4] $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ - 0.2V $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC}$ - 0.2V	MIL.	S	85	260	80	260	75	260	mA
				L	85	215	80	215	75	215	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le 0.2V$ Active Port Outputs Open, $f = f_{MAX}$[3]	COM'L.	S	85	220	80	220	—	—	
				L	85	180	80	180	—	—	

NOTES:

2683 tbl 08

1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

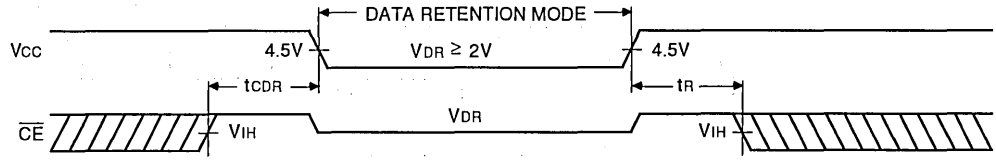
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2683 tbl 09

1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

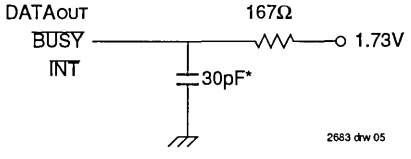


2683 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

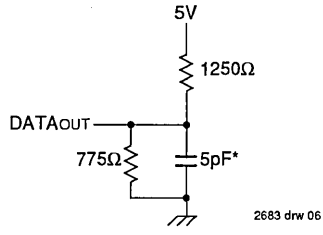
2683 tbl 10



2683 drw 05

* Including scope and jig.

Figure 1. Equivalent Output Load



2683 drw 06

Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7025X25 COM'L ONLY		IDT7025X30 COM'L ONLY		IDT7025X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	30	—	35	—	ns
tAA	Address Access Time	—	25	—	30	—	35	ns
tACE	Chip Enable Access Time[3]	—	25	—	30	—	35	ns
tABE	Byte Enable Access Time[3]	—	25	—	30	—	35	ns
tAOE	Output Enable Access Time	—	13	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	15	—	15	—	ns

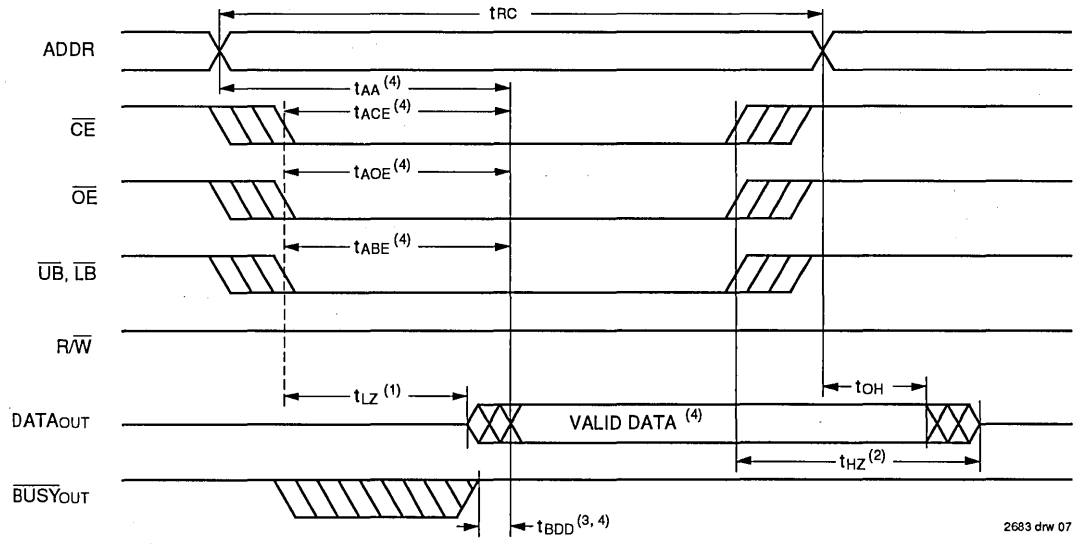
Symbol	Parameter	IDT7025X45		IDT7025X55		IDT7025X70 MIL ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	45	—	55	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
tABE	Byte Enable Access Time[3]	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	25	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

2683 tbl 11

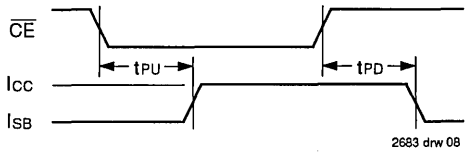
6

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, OE, CE, LB, or UB.
2. Timing depends on which signal is de-asserted first CE, OE, LB, or UB.
3. tBDD delay i s required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. SEM = H.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7025X25 COM'L ONLY Min.	IDT7025X25 COM'L ONLY Max.	IDT7025X30 COM'L ONLY Min.	IDT7025X30 COM'L ONLY Max.	IDT7025X35 Min.	IDT7025X35 Max.	Unit
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{EW}	Chip Enable to End of Write(3)	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	ns
t_{HZ}	Output High Z Time(1, 2)	—	15	—	15	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z(1, 2)	—	15	—	15	—	15	ns
t_{OW}	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

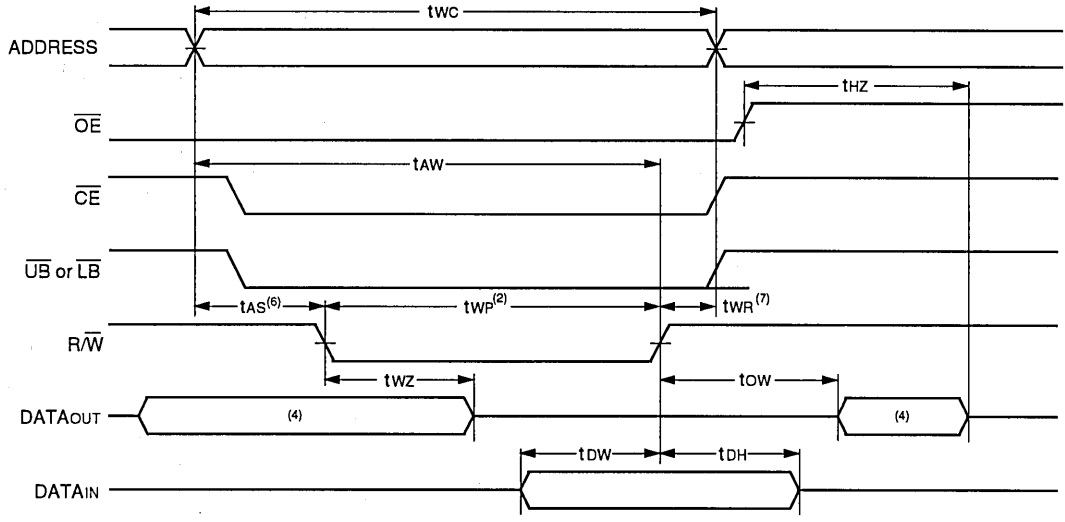
Symbol	Parameter	IDT7025X45 Min.	IDT7025X45 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End of Write(3)	40	—	45	—	50	—	ns
t_{AW}	Address Valid to End of Write	40	—	45	—	50	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	40	—	ns
t_{HZ}	Output High Z Time(1, 2)	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z(1, 2)	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write(1, 2, 4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	ns

2683 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. X in part numbers indicates power rating (S or L).

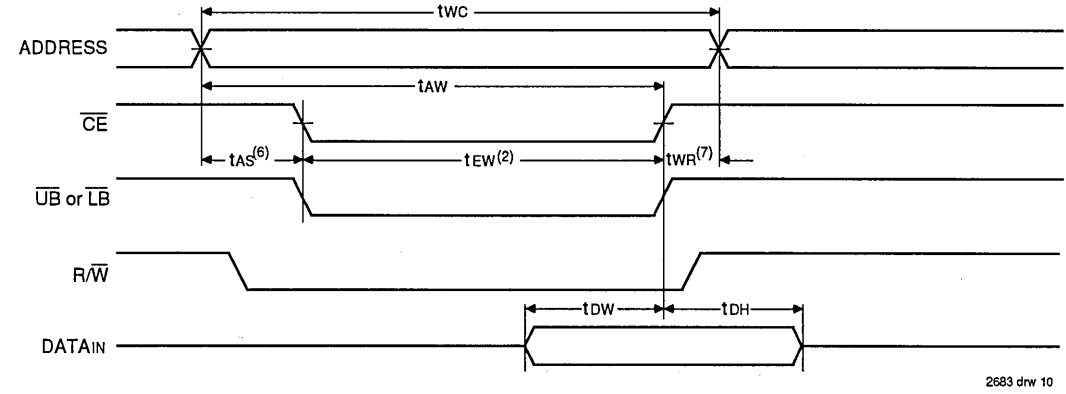
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



2683 drw 09

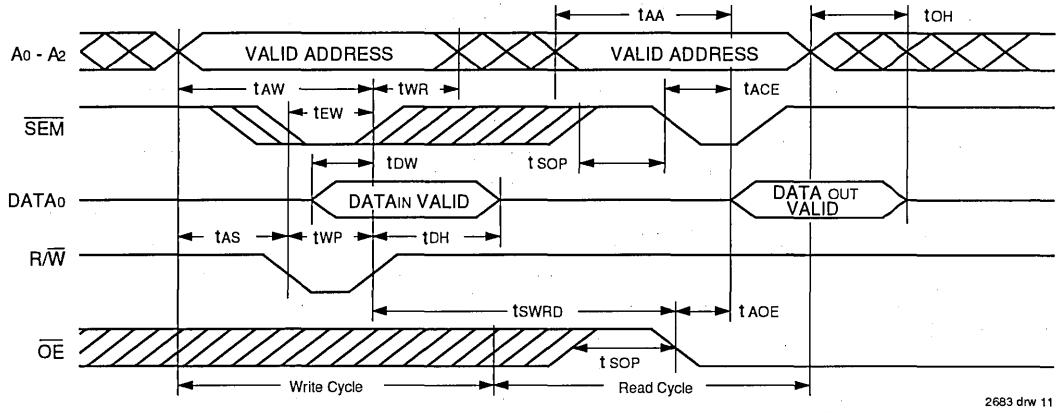
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,3,5,8)



2683 drw 10

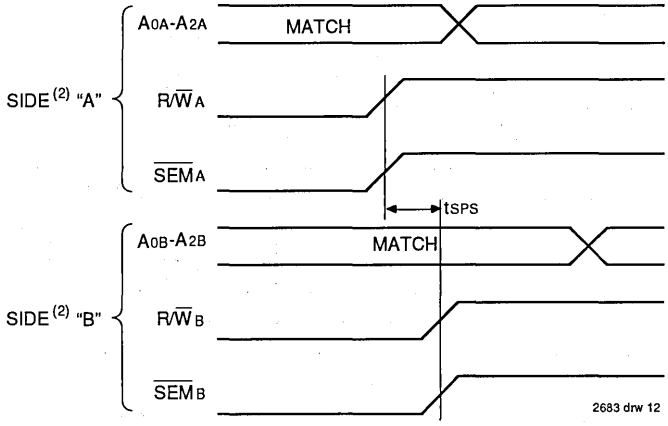
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$ or byte control.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, R/$\overline{W}$ or byte control.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

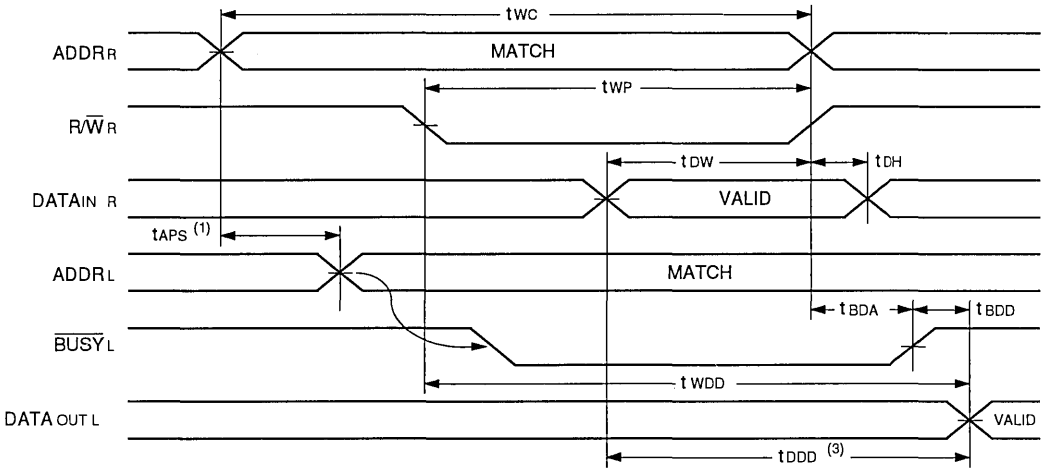
Symbol	Parameter	IDT7025X25 COM'L ONLY Min.	IDT7025X25 COM'L ONLY Max.	IDT7025X30 COM'L ONLY Min.	IDT7025X30 COM'L ONLY Max.	IDT7025X35 Min.	IDT7025X35 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	30	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	25	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	20	—	25	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	17	—	20	—	25	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	17	—	20	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	50	—	55	—	60	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	35	—	40	—	45	ns

Symbol	Parameter	IDT7025X45 Min.	IDT7025X45 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	30	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	30	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	25	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	55	—	65	—	80	ns

NOTES: 2683 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

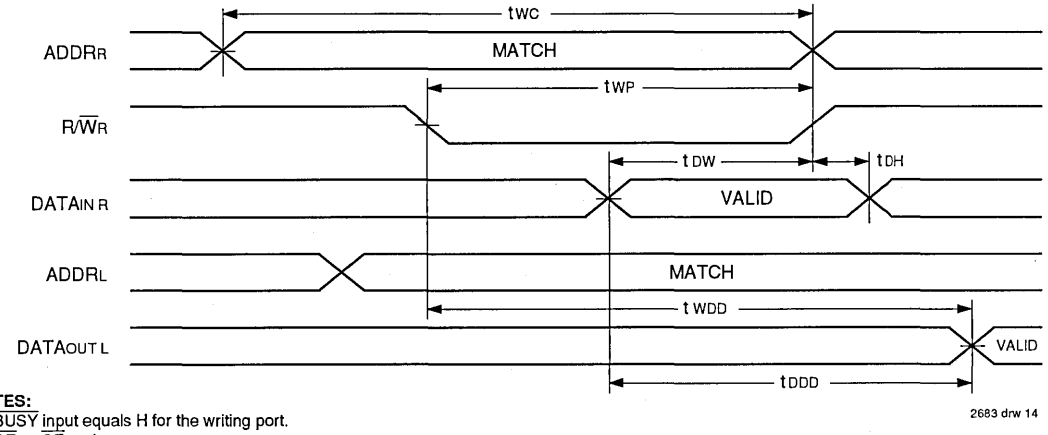
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)



2683 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

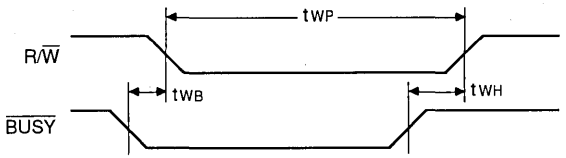
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2] (M/$\overline{S}$ = L)



2683 drw 14

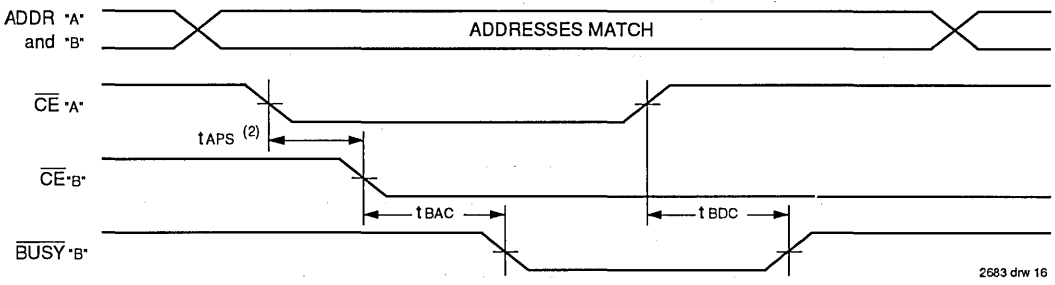
NOTES:
1. $\overline{BUSY}$ input equals H for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

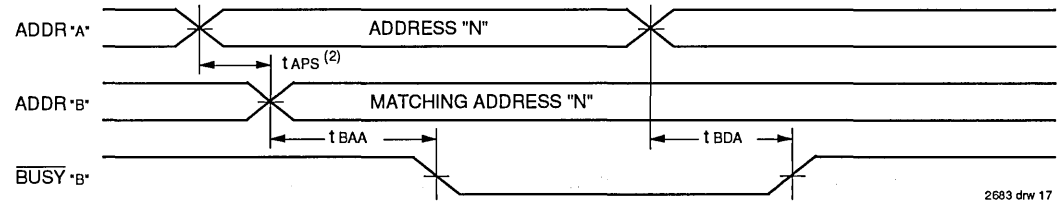


2683 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

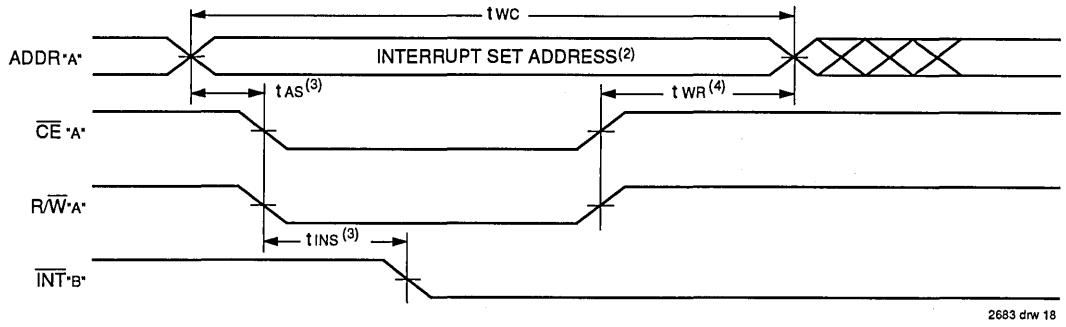
Symbol	Parameter	IDT7025X25 COM'L ONLY Min.	IDT7025X25 COM'L ONLY Max.	IDT7025X30 COM'L ONLY Min.	IDT7025X30 COM'L ONLY Max.	IDT7025X35 Min.	IDT7025X35 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	ns

Symbol	Parameter	IDT7025X45 Min.	IDT7025X45 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	35	—	40	—	50	ns
tINR	Interrupt Reset Time	—	35	—	40	—	50	ns

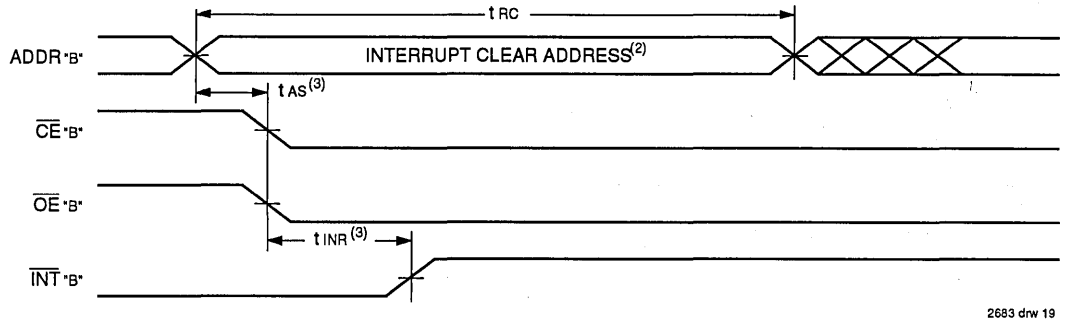
NOTE:
1. "x" in part numbers indicates power rating (S or L).

2683 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2683 drw 18



2683 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

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TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2683 tbl 15

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2683 tbl 16

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7025 are push pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneouly.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2683 tbl 17

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.

FUNCTIONAL DESCRIPTION

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

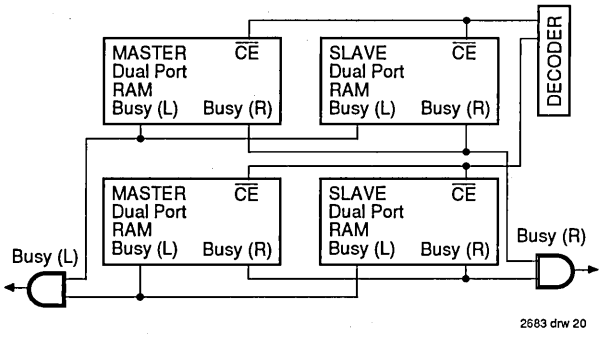


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7025 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7025 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7025 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7025 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7025 is an extremely fast dual-port 8K x 16 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7025 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7025's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7025 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more

6

common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the dual-port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a

one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's dual-port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of dual-port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of dual-port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the dual-port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

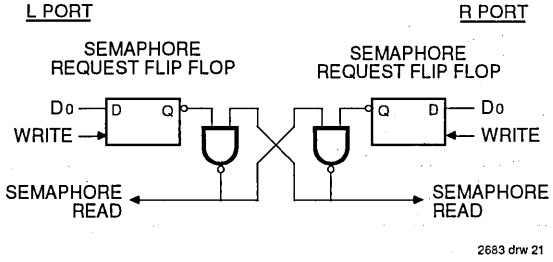


Figure 4. IDT7025 Semaphore Logic

Integrated Device Technology, Inc.

HIGH-SPEED 1K x 8 FourPort™ STATIC RAM

IDT7050S
IDT7050L

FEATURES:

- High-speed access
  - — Military: 30/35/45ns (max.)
  - — Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - — IDT7050S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7050L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical sspecification

DESCRIPTION:

The IDT7050 is a high-speed 1K x 8 FourPort static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

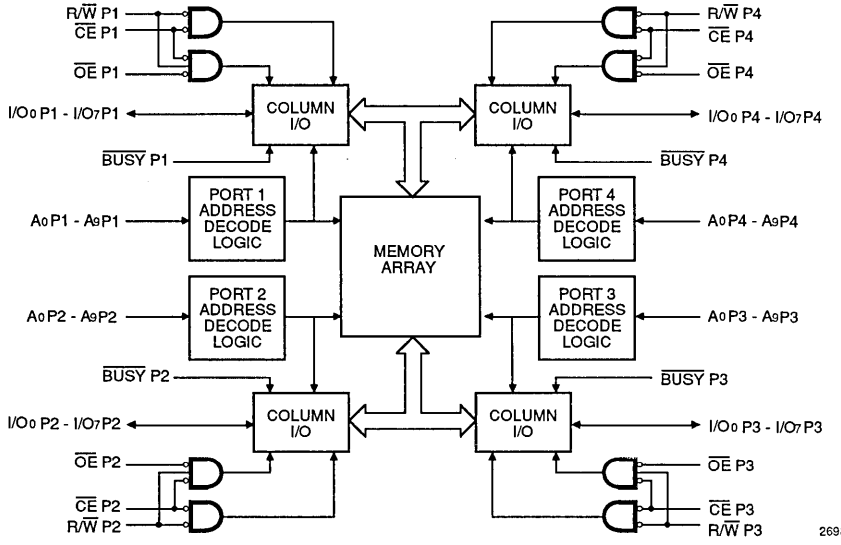
The IDT7050 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7050 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7050 is packaged in a ceramic 108-pin PGA and a plastic 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



FourPort is a trademark of Integrated Device Technology, Inc.

A	B	C	D	E	F	G	H	J	K	L	M	
81 R/$\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 NC	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 NC	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
92 NC	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 NC	08
95 A_8 P1	94 A_7 P1	93 V_{CC}							44 GND	43 A_7 P4	42 A_8 P4	07
96 A_9 P1	97 NC	98 $\overline{CE}$ P1							39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

IDT7050
G108-1 (1,2,3)

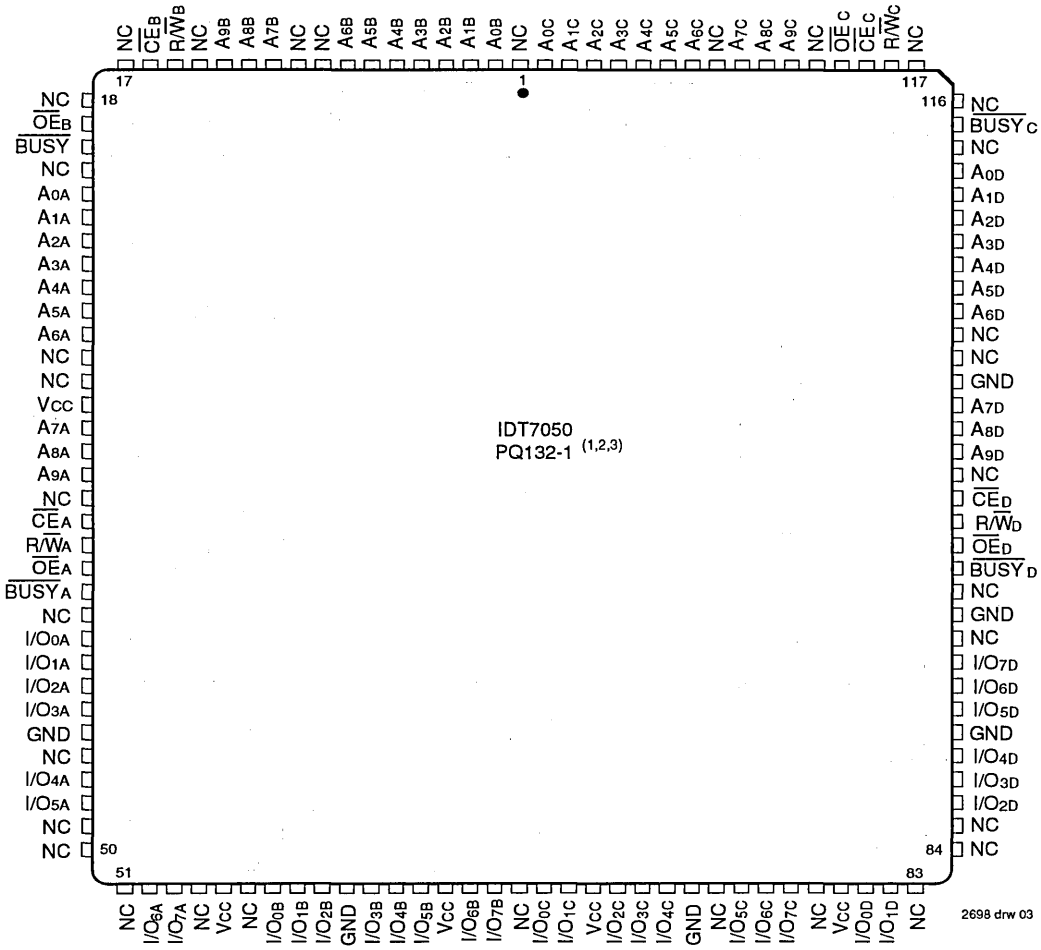
TOP VIEW

2698 drw 02

Pin 1
Designator

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.

6



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no - connect pin.

PIN CONFIGURATIONS

Symbol	Pin Name
A_0 P1 – A_9 P1	Address Lines – Port 1
A_0 P2 – A_9 P2	Address Lines – Port 2
A_0 P3 – A_9 P3	Address Lines – Port 3
A_0 P4 – A_9 P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
$R/\overline{W}$ P1	Read/Write – Port 1
$R/\overline{W}$ P2	Read/Write – Port 2
$R/\overline{W}$ P3	Read/Write – Port 3
$R/\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
V_{CC}	Power

2698 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2698 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2698 tbl 03

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2698 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2698 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7050S		IDT7050L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2698 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7050x25[3]		IDT7050x30		IDT7050x35		IDT7050x45		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = 0[4]	MIL.	S	—	—	150	360	150	360	150	360	mA
				L	—	—	150	300	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	150	300	
				L	150	250	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[5]	MIL.	S	—	—	220	400	210	395	195	390	mA
				L	—	—	190	335	180	330	170	325	
			COM'L.	S	225	350	220	340	210	335	195	330	
				L	195	305	190	295	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \ge V_{IH}$ f = f_{MAX}[5]	MIL.	S	—	—	45	115	40	110	35	105	mA
				L	—	—	40	85	35	80	30	75	
			COM'L.	S	60	85	45	80	40	75	35	70	
				L	50	70	40	65	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1.5	30	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	.3	4.5	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]	COM'L.	S	1.5	15	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	.3	1.5	

NOTES:
2698 tbl 07

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for Typ.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
6. For the case of one port, divide the appropriate current by four.
7. At $V_{CC} \le$2.0V input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

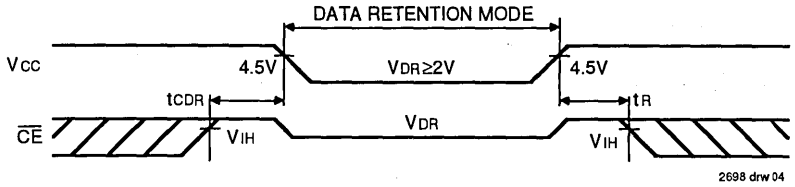
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \ge V_{HC}$	MIL.	—	25	1800	µA
		$V_{IN} \ge V_{HC}$ or $\le V_{LC}$	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2698 tbl 08

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

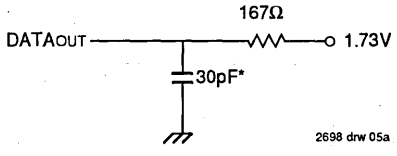
LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2698 tbl 09



*Including scope and jig

Figure 1. Equivalent Output Load

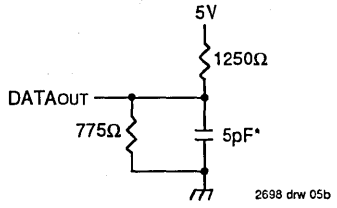


Figure 2. Output Load (for tLZ, tHZ, tWZ, tOW)

6

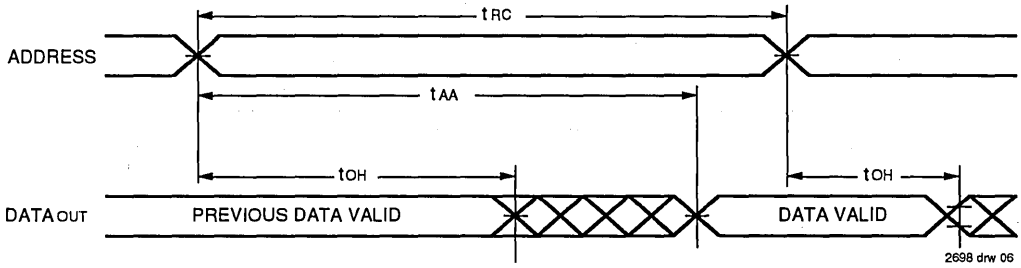
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7050S25[1,3] IDT7050L25[1,3] Min.	Max.	IDT7050S30 IDT7050L30 Min.	Max.	IDT7050S35 IDT7050L35 Min.	Max.	IDT7050S45 IDT7050L45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,2]	3	—	3	—	5	—	5	—	ns
tHZ	Output High Z Time[1,2]	—	15	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	20	—	30	—	50	—	50	ns

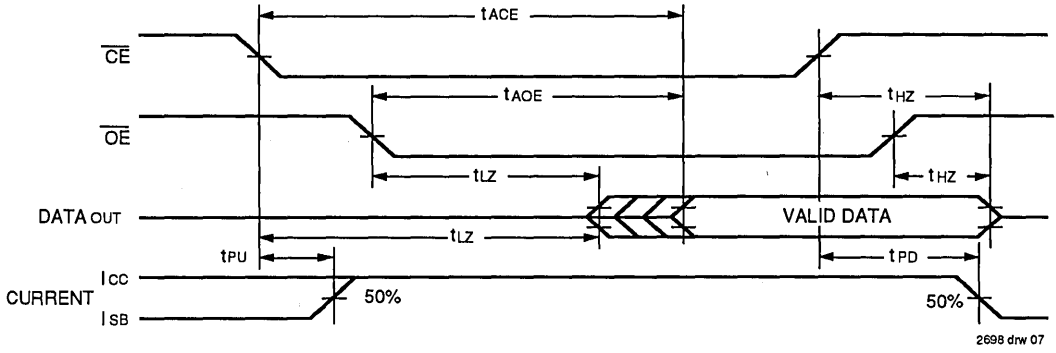
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

2698 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7050S25[7] IDT7050L25[7]		IDT7050S30 IDT7050L30		IDT7050S35 IDT7050L35		IDT7050S45 IDT7050L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[3]	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	15	—	15	—	15	—	20	ns
tOW	Output Active from End of Write[1, 2]	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	45	—	50	—	55	—	65	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	40	—	45	—	55	ns
BUSY INPUT TIMING										
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	15	—	20	—	20	—	20	—	ns

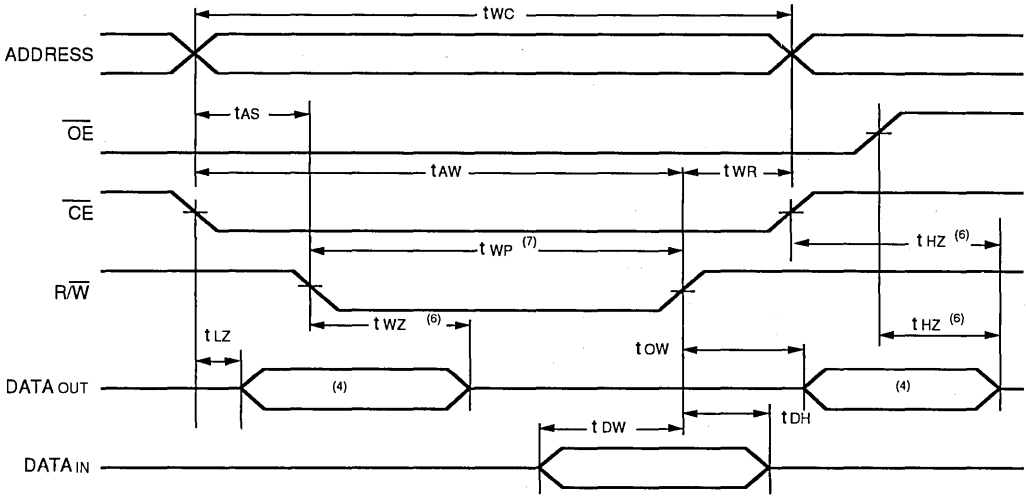
NOTES:

2698 tbl 11

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

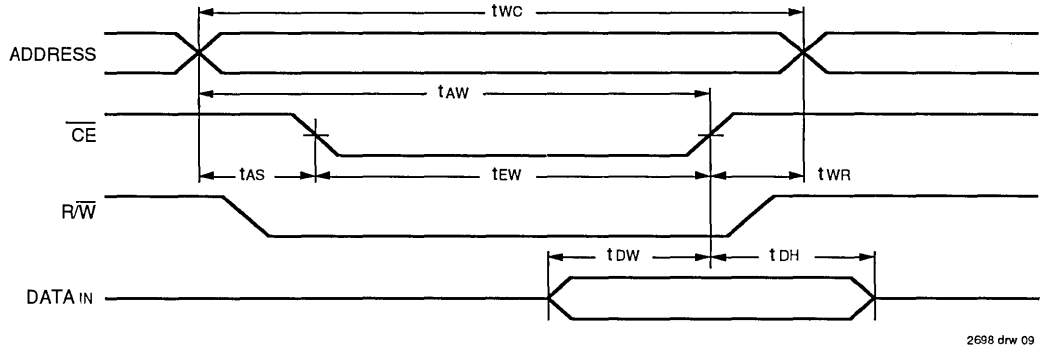
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



2698 drw 08

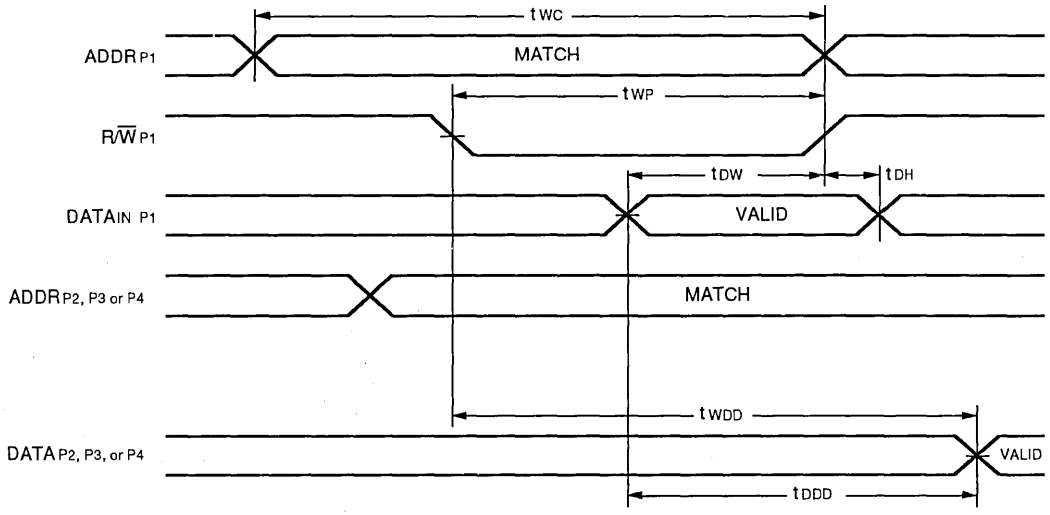
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2698 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

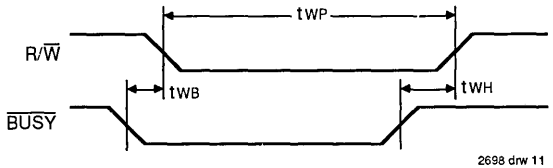
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



2698 drw 10

NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2698 drw 11

FUNCTIONAL DESCRIPTION

The IDT7050 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I – READ/WRITE CONTROL

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$ = H Power Down Mode, I_{SB1} or I_{SB}
L	L	X	$DATA_{IN}$	Data on port written into memory(2, 3)
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

2698 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 8 FourPort™ STATIC RAM

IDT7052S
IDT7052L

FEATURES:

- High-speed access
  - — Military: 30/35/45ns (max.)
  - — Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - — IDT7052S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7052L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7052 is a high-speed 2K x 8 FourPort static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

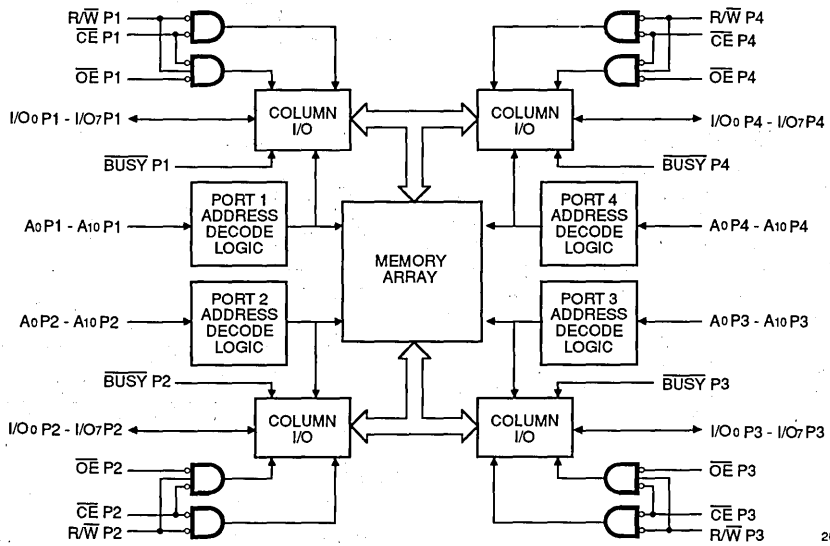
The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM typically operates on only 750mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50μW from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin PGA and a plastic 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



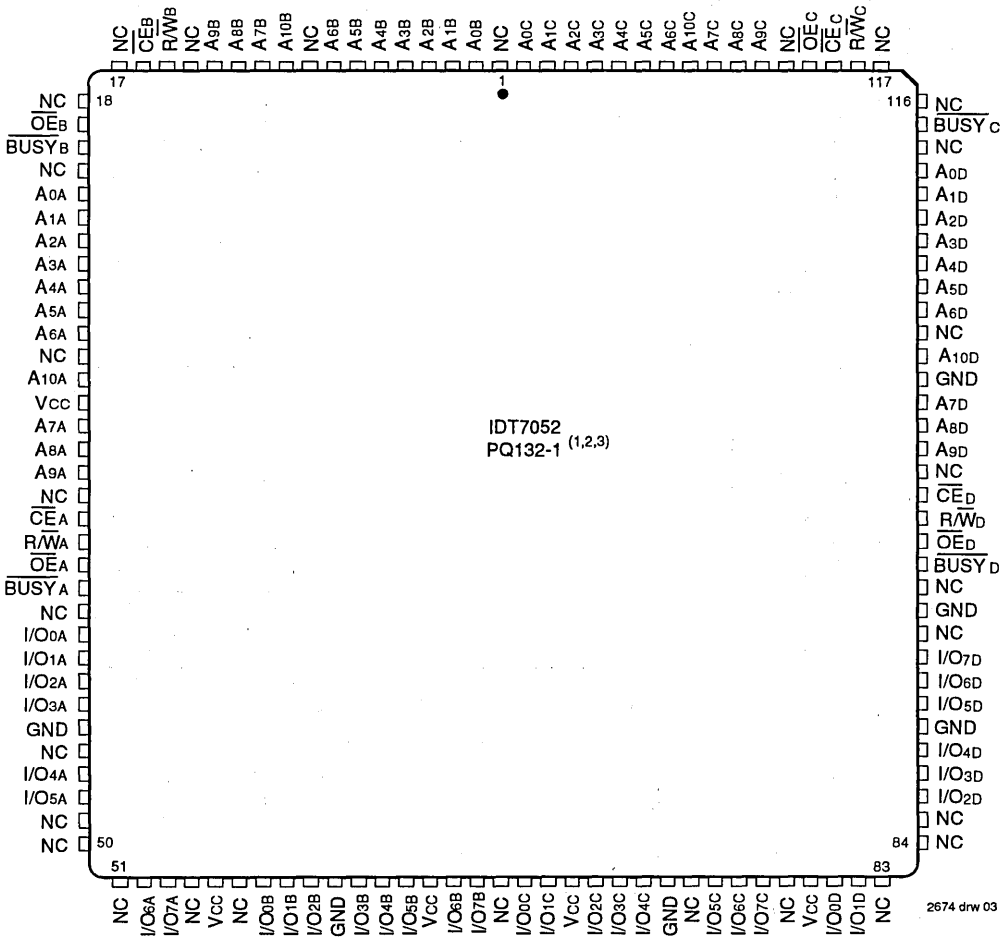
FourPort is a trademark of Integrated Device Technology, Inc.

A	B	C	D	E	F	G	H	J	K	L	M	
81 R/$\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 A_{10} P2	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 A_{10} P3	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
92 A_{10} P1	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 A_{10} P4	08
95 A_8 P1	94 A_7 P1	93 V_{CC}			IDT7052 G108-1 (1,2,3)				44 GND	43 A_7 P4	42 A_8 P4	07
96 A_9 P1	97 NC	98 $\overline{CE}$ P1			TOP VIEW				39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

2674 drw 02

Pin 1 Designator

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no-connect pin.



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. NC denotes no-connect pin.

PIN CONFIGURATIONS

Symbol	Pin Name
A_0 P1 – A_{10} P1	Address Lines – Port 1
A_0 P2 – A_{10} P2	Address Lines – Port 2
A_0 P3 – A_{10} P3	Address Lines – Port 3
A_0 P4 – A_{10} P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
$R/\overline{W}$ P1	Read/Write – Port 1
$R/\overline{W}$ P2	Read/Write – Port 2
$R/\overline{W}$ P3	Read/Write – Port 3
$R/\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
V_{CC}	Power

2674 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2674 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2674 tbl 03

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2674 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2674 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7052S		IDT7052L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2674 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2, 6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7052x25[3]		IDT7052x30		IDT7052x35		IDT7052x45		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = 0[4]	MIL.	S	—	—	150	360	150	360	150	360	mA
				L	—	—	150	300	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	150	300	
				L	150	250	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}[5]	MIL.	S	—	—	220	400	210	395	195	390	mA
				L	—	—	190	335	180	330	170	325	
			COM'L.	S	225	350	220	340	210	335	195	330	
				L	195	305	190	295	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE} \ge V_{IH}$ f = f_{MAX}[5]	MIL.	S	—	—	45	115	40	110	35	105	mA
				L	—	—	40	85	35	80	30	75	
			COM'L.	S	60	85	45	80	40	75	35	70	
				L	50	70	40	65	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE} \ge V_{CC}$ - 0.2V	MIL.	S	—	—	1.5	30	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	.3	4.5	
		$V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]	COM'L.	S	1.5	15	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	.3	1.5	

NOTES:

2674 tbl 07

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for Typ.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
6. For the case of one port, divide the above appropriate current by four.
7. At $V_{CC} \le$2.0V input leakages are undefined.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

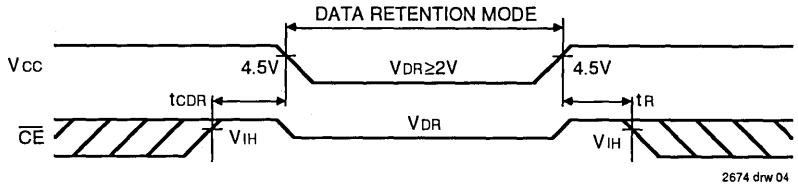
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \ge V_{HC}$	MIL.	—	25	1800	µA
		$V_{IN} \ge V_{HC}$ or $\le V_{LC}$	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:

2674 tbl 08

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

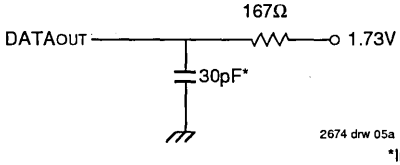
LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2674 tbl 09



*Including scope and jig

Figure 1. Equivalent Output Load

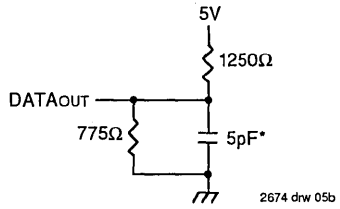


Figure 2. Output Load (for tLZ, tHZ, twz, tow)

6

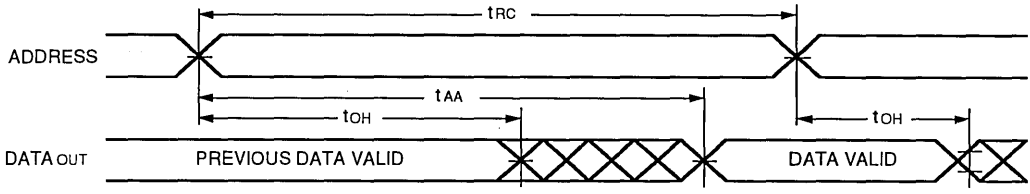
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052S25[1] IDT7052L25[1] Min.	Max.	IDT7052S30 IDT7052L30 Min.	Max.	IDT7052S35 IDT7052L35 Min.	Max.	IDT7052S45 IDT7052L45 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1, 2]	3	—	3	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	20	—	30	—	50	—	50	ns

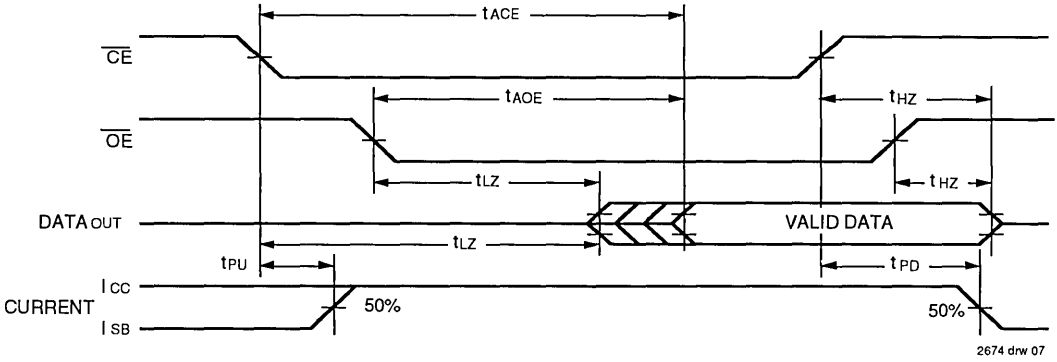
2674 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

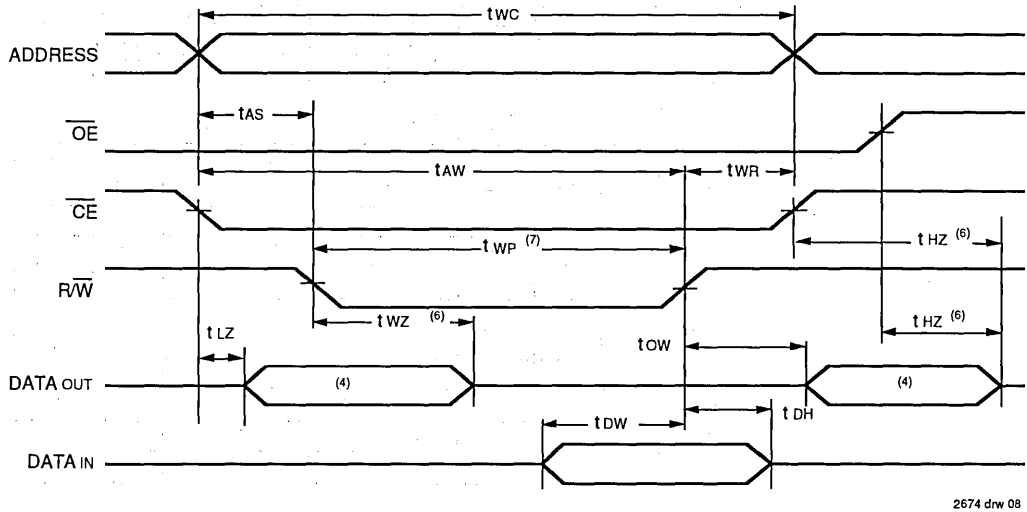
Symbol	Parameter	IDT7052S25[7] IDT7052L25[7] Min.	Max.	IDT7052S30 IDT7052L30 Min.	Max.	IDT7052S35 IDT7052L35 Min.	Max.	IDT7052S45 IDT7052L45 Min.	Max.	Unit
WRITE CYCLE										
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[3]	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time[1, 2]	—	15	—	15	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	15	—	15	—	15	—	20	ns
tOW	Output Active from End of Write[1, 2]	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	45	—	50	—	55	—	65	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	35	—	40	—	45	—	55	ns
BUSY INPUT TIMING										
tWB	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	15	—	20	—	20	—	20	—	ns

NOTES:
2698 tbl 11

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

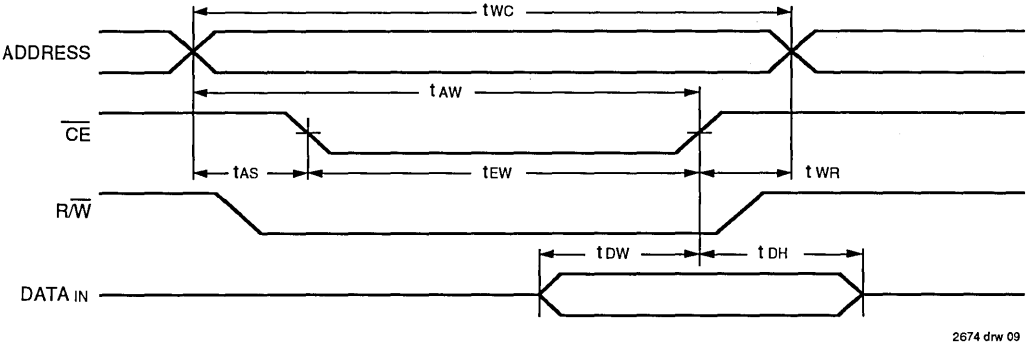
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



2674 drw 08

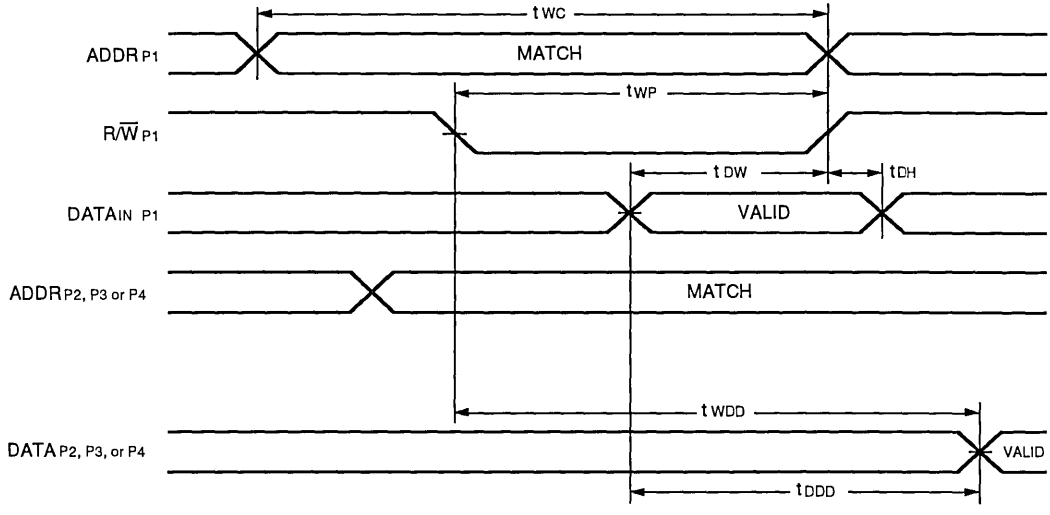
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2674 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

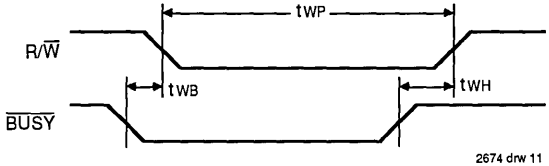
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



2698 drw 10

NOTES:
1. Assume BUSY input at HI and CE at LO for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its OE at LO.

TIMING WAVEFORM OF WRITE WITH BUSY INPUT



2674 drw 11

6

FUNCTIONAL DESCRIPTION

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by CE. The CE controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected (CE high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (OE). In the read mode, the port's OE turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I – READ/WRITE CONTROL

Any Port(1)				
R/W	CE	OE	D0-7	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	CEP1 = CEP2 = CEP3 = CEP4 = H Power Down Mode, ISB or ISB1
L	L	X	DATAIN	Data on port written into memory(2, 3)
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

2698 tbl 12

NOTES:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If BUSY = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

SUBSYSTEMS PRODUCTS

IDT Subsystems Division has the resources and experience to deliver the highest quality RAM module products. IDT's combination of advanced design, assembly, and test capabilities give customers the highest levels of quality, service and performance. Product offerings include a number JEDEC standards as well as specialized and application specific RAM modules, including the world's highest performance and densest SRAMs, Dual-Port RAMs, and FIFOs. Custom capabilities allow our customers to enjoy the benefits of parametically tested complete memory-based subsystems including extremely high performance caches for a wide range of processors and complete memory subsystems including multi-megabyte microprocessor main memories.

IDT modules products provide a number of benefits to the high performance system designer:

For system designers of high performance systems, modules solve a number of major problems through the benefits they provide. The biggest benefit of modules is that they save significant amounts of space for designers packing ever more performance in less space by utilizing double sided surface mount technology (SMT). Modules allow designers to take advantage of SMT for performance critical memory paths without the investments or the volume necessary to justify employing SMT for an entire system. Since systems at the high performance end of the spectrum tend to be lower volume, it makes sense to take advantage of module technology to enjoy the space savings and performance advantages of SMT without the cost. In addition, decoupling capacitors are mounted next to or underneath the active memory components on the module, thus eliminating the need to consider them or the real estate they consume.

Numerous module packaging options are available which allow designers to tradeoff board area, height and mechanical stability. Vertical mount module options (modules in which mounted components are oriented in a vertical fashion) such as single in-line packages (SIPs), dual-row SIPs (DSIPs), zig-zag in-line packages (ZIPs) and single-in-line memory modules (SIMMs) are ideal packages for applications requiring the highest density. Many of these vertical mount modules are maximum 0.5 inch tall, which is well within the board space requirements for card rack type systems. Horizontal mount module options include dual in-line packages (DIPs), quad in-line packages (QIPs), and hex in-line packages (HIPs). These modules are ideal for those applications requiring the most in mechanical stability and those with many I/O pins.

Design, manufacturing, and marketing often disagree on the size of memory that their high performance system will offer. By allowing the decision to made at manufacturing time by having module solutions with different memory sizes and common pinouts, the module user lets the market dictate memory requirements. JEDEC has defined standards for memory pinouts including 16K x 32, 64K x 32 and 256K x 32 SRAM in the same 64 lead SIMM/ZIP which are among the most common industry standard SRAM modules.

Testing is both a design and manufacturing problem that is often an afterthought. By providing a pretested higher level block, modules simplify the test issue for both design and manufacturing. Since the module is tested using full parametric AC/DC guardbanded test patterns over the specified operating temperature range, designers are guaranteed a level of performance for a larger block of their system versus a spec for an individual component. System board test is simplified because a major block of memory has been fully tested at the module level, thus simplifying the test method and debug cycle at the board level.

Time to market is always a very important issue. Studies have shown that a major portion of profits are made in the early part of the product life cycle before competition drives down prices to a level based on manufacturing costs rather than a unique level of value. Integrating the high performance memory into an module shortens the design cycle by simplifying board design by leveraging off the module manufacturer's design expertise. System board layout and the design cycle are simplified because the number of input/outputs (I/Os) are reduced by combining common component address, data, control, and power pins.

Module solutions help reduce hidden costs that are not often taken into account. Since active and passive components necessary to realize an module solution are combined onto a single substrate, the module user reduces inventory and handling costs by combining a number of diverse components into one single component.

IDT Subsystems products provide an ideal solution for system designers to integrate high performance RAM in order to maximize density, performance and cost-effectiveness for both commercial and military applications.

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Integrated Device Technology, Inc.

IDT SUBSYSTEMS CUSTOM MODULE CAPABILITIES

INTRODUCTION

IDT Subsystems is available for design and manufacturing of a wide range of custom products. From dense memory modules to sophisticated multi-processor subsystems, we are the leading supplier of custom modules to commercial and military customers. This experience provides the basis of our professional approach to meet your needs. Custom module solutions can provide significant benefits to you:

- **Application Specific**

Encompassing all of your design criteria (electrical, mechanical, environmental), a custom solution is specially tailored to perform in your application.

- **Faster Time to Market**

Acting as an extension of your design team, we can provide the additional resources you need to bring your product out in time to meet *your* window of opportunity.

- **Manufacturing Ease/Guaranteed Performance**

100% of IDT Subsystem products are tested over guardbanded temperature and supply voltage to ensure datasheet conformance. This guaranteed performance reduces time-consuming debugging and provides you with confidence that your system will perform well at your customer's installation.

- **Density**

More capability into smaller space is what it takes to stay competitive. IDT Subsystems can help you using the packaging technology appropriate for your needs. Double-sided surface mounted components on FR-4 substrates offer quick-turn solutions. TAB mounted die and other approaches on a wide variety of substrates can offer substantial density advantages, especially for high pincount devices such as processors and ASICs. We can help you evaluate and compare alternatives to make the best selection for your application.

CUSTOM MODULE DEVELOPMENT FLOW

Figure 1 illustrates our custom module development flow, from initial concept through manufacturing and delivery. The initial concept is the starting point for discussions with the customer and Subsystems Engineering. Specifications, mechanical requirements, and other needs are reviewed and discussed to select the best components and assembly technology for the application.

All specifications are reviewed with you prior to substrate fabrication to ensure adherence to your requirements.

PACKAGING FLEXIBILITY

Packaging options provide you with the flexibility to fit your function within the available space. Military and hostile environments typically require the use of ceramic substrates while FR-4 is most often used in commercial and industrial temperature applications. Newer die packaging technologies such as TAB, flip-chip and others offer density and performance advantages not attainable by conventional through-hole or surface mount assemblies.

IDT Subsystems can provide you with the technology to fit your needs through prototype/beta testing, pilot production, and volume manufacturing. Contact the factory for more details.

CEMOS is a trademark of Integrated Device Technology, Incorporated

CUSTOM PRODUCT DEVELOPMENT OVERVIEW

Customer requirements gathered and understood to prepare proposal which fits electrical, mechanical, and business needs.

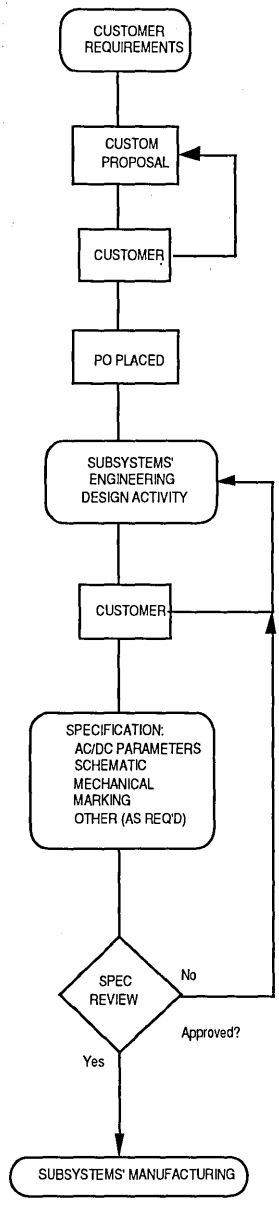
Custom development proposal written and presented to customer for evaluation and feedback. Changes are made as required to ensure customer will receive desired end product.

Subsystems' Engineering begins design. This process often involves communication with customer engineering group.

Subsystems' Engineering finshes design, and obtains approval within Subsystems' Marketing, Production, Assembly, and Test groups.

Complete custom specification delivered to customer for review and approval prior to ordering motherboard fabrication.

Custom module approval received; motherboard and other parts ordered for assembly kitting.



Integrated Device Technology, Inc.

4K x 16 FourPort™ STATIC RAM MULTICHIP MODULE

PRELIMINARY
IDT70M74

FEATURES:

- High density 64K-bit FourPort™ static RAM multichip module
- High-speed access
  - — Commercial: 25, 30, 35, 45ns (max.)
  - — Military: 30, 35, 45ns (max.)
- Low-power CEMOS™ operation
- Fully asynchronous read/write operation from each of the four ports: Ports A, B, C, D
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible inputs/outputs
- Single 5V (±10%) power supply
- Available in 180-pin hermetic PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

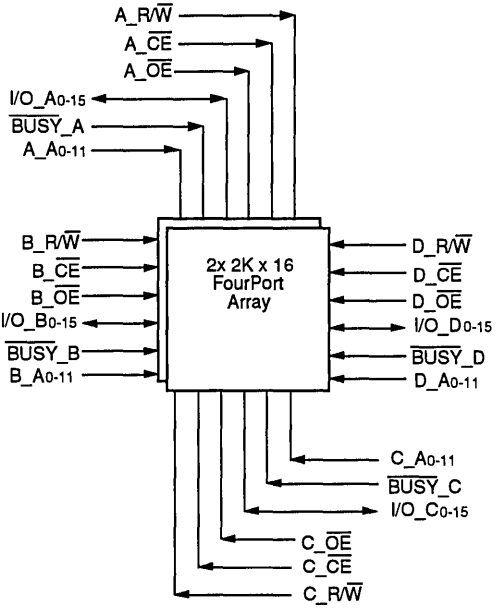
The IDT70M74 is a high-speed 4K x 16 FourPort static RAM multichip module designed to be used in systems where multiple access in a common RAM is required. This FourPort static RAM module offers increased system performance in multiprocesser systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT70M74 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. Arbitratation is not provided on the module; therefore, it is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this four port RAM module typically operates on only 3W of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 0.5mW from a 2V battery.

The IDT70M74 is packaged in a ceramic, hermetically sealed 180-pin PGA. Military grade product is manufactured in compliance with the latest revision of Mil-Std-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



2817 drw 01

FourPort and CEMOS are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	$\overline{BSY}$_B	R/$\overline{W}$_B(1)	R/$\overline{W}$_B(0)	GND	A_B(7)	A_B(3)	A_B(0)	Vcc	A_C(3)	A_C(7)	GND	R/$\overline{W}$_C(0)	R/$\overline{W}$_C(1)	$\overline{BSY}$_C	GND
B	$\overline{OE}$_B(0)	$\overline{OE}$_B(1)	R/$\overline{W}$_B(2)	$\overline{CE}$_B(2)	$\overline{CE}$_B(0)	A_B(8)	A_B(4)	A_B(1)	A_C(0)	A_C(4)	A_C(8)	$\overline{CE}$_C(0)	$\overline{CE}$_C(2)	R/$\overline{W}$_C(2)	$\overline{OE}$_C(1)	$\overline{OE}$_C(0)
C	$\overline{OE}$_B(2)	$\overline{OE}$_B(3)	R/$\overline{W}$_B(3)	$\overline{CE}$_B(3)	$\overline{CE}$_B(1)	A_B(9)	A_B(5)	A_B(2)	A_C(1)	A_C(5)	A_C(9)	$\overline{CE}$_C(1)	$\overline{CE}$_C(3)	R/$\overline{W}$_C(3)	$\overline{OE}$_C(3)	$\overline{OE}$_C(2)
D	A_A(0)	A_A(1)	A_A(2)			A_B(10)	A_B(6)	GND	A_C(2)	A_C(6)	A_C(10)			A_D(2)	A_D(1)	A_D(0)
E	GND	A_A(3)	A_A(4)											A_D(4)	A_D(3)	GND
F	A_A(5)	A_A(6)	A_A(7)	A_A(8)									A_D(8)	A_D(7)	A_D(6)	A_D(5)
G	A_A(9)	$\overline{CE}$_A(0)	$\overline{CE}$_A(1)	A_A(10)									A_D(10)	$\overline{CE}$_D(1)	$\overline{CE}$_D(0)	A_D(9)
H	VCC	$\overline{CE}$_A(2)	$\overline{CE}$_A(3)	GND				**TOP VIEW**					GND	$\overline{CE}$_D(3)	$\overline{CE}$_D(2)	Vcc
J	R/$\overline{W}$_A(0)	R/$\overline{W}$_A(1)	R/$\overline{W}$_A(2)	R/$\overline{W}$_A(3)									R/$\overline{W}$_D(3)	R/$\overline{W}$_D(2)	R/$\overline{W}$_D(1)	R/$\overline{W}$_D(0)
K	$\overline{OE}$_A(0)	$\overline{OE}$_A(1)	$\overline{OE}$_A(2)	$\overline{OE}$_A(3)									$\overline{OE}$_D(3)	$\overline{OE}$_D(2)	$\overline{OE}$_D(1)	$\overline{OE}$_D(0)
L	I/O_A(0)	I/O_A(1)	I/O_A(2)	$\overline{BSY}$_A									$\overline{BSY}$_D	I/O_D(2)	I/O_D(1)	I/O_D(0)
M	GND	I/O_A(3)	I/O_A(4)											I/O_D(4)	I/O_D(3)	GND
N	I/O_A(5)	I/O_A(6)	I/O_A(7)	GND		I/O_B(8)	I/O_B(12)	I/O_B(15)	GND	I/O_C(12)	I/O_C(8)			I/O_D(7)	I/O_D(6)	I/O_D(5)
P	I/O_A(8)	I/O_A(9)	I/O_A(10)	I/O_B(2)	I/O_B(4)	I/O_B(7)	I/O_B(11)	I/O_B(14)	I/O_C(15)	I/O_C(11)	I/O_C(7)	I/O_C(4)	I/O_C(2)	I/O_D(10)	I/O_D(9)	I/O_D(8)
Q	I/O_A(11)	I/O_A(12)	I/O_A(13)	I/O_B(1)	I/O_B(3)	I/O_B(6)	I/O_B(10)	I/O_B(13)	I/O_C(14)	I/O_C(10)	I/O_C(6)	I/O_C(3)	I/O_C(1)	I/O_D(13)	I/O_D(12)	I/O_D(11)
R		I/O_A(14)	I/O_A(15)	I/O_B(0)	GND	I/O_B(5)	I/O_B(9)	Vcc	I/O_C(13)	I/O_C(9)	I/O_C(5)	GND	I/O_C(0)	I/O_D(15)	I/O_D(14)	GND

2817 drw 02

PIN NAMES

Symbol	Pin Name
A_A(0-11)	Address Inputs – Port A
A_B(0-11)	Address Inputs – Port B
A_C(0-11)	Address Inputs – Port C
A_D(0-11)	Address Inputs – Port D
I/O_A(0-15)	Data I/O – Port A
I/O_B(0-15)	Data I/O – Port B
I/O_C(0-15)	Data I/O – Port C
I/O_D(0-15)	Data I/O – Port D
R/$\overline{W}$_A(0-3)	Read/Write – Port A
R/$\overline{W}$_B(0-3)	Read/Write – Port B
R/$\overline{W}$_C(0-3)	Read/Write – Port C
R/$\overline{W}$ _D(0-3)	Read/Write – Port D
$\overline{CE}$_A(0-3)	Chip Enable – Port A
$\overline{CE}$_B(0-3)	Chip Enable – Port B
$\overline{CE}$ _C(0-3)	Chip Enable – Port C
$\overline{CE}$ _D(0-3)	Chip Enable – Port D
$\overline{OE}$_A(0-3)	Output Enable – Port A
$\overline{OE}$ _B(0-3)	Output Enable – Port B
$\overline{OE}$_C(0-3)	Output Enable – Port C
$\overline{OE}$ _D(0-3)	Output Enable – Port D
$\overline{BUSY}$_A	Write Disable – Port A
$\overline{BUSY}$_B	Write Disable – Port B
$\overline{BUSY}$_C	Write Disable – Port C
$\overline{BUSY}$_D	Write Disable – Port D
Vcc	Power
GND	Ground

2817 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2817 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	50	pF

NOTE: 2817 tbl 03

1. This parameter is guaranteed by design, but not tested

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2817 tbl 04

TRUTH TABLE

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-15	Function
X	H	X	Z	Port Disabled and in Power Down Mode
X	H	X	Z	$\overline{CE}_{P1}$ = $\overline{CE}_{P2}$ = $\overline{CE}_{P3}$ = $\overline{CE}_{P4}$ = H Power Down Mode, ISB or ISB1
L	L	X	DATAIN	Data on port written into memory(2, 3)
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

NOTES: 2817 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2817 tbl 05

1. VIL (min.) = -3.0V for pulse width less than 20ns.

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT70M74 Min.	IDT70M74 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	40	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

2817 tbl 07

DC ELECTRICAL CHARACTERISTICS(1, 5, 6)

(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Condition	Version	-25ns(2) Typ.	-25ns(2) Max.	-30ns Typ.	-30ns Max.	-35ns Typ.	-35ns Max.	-45ns Typ.	-45ns Max.	Unit
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ ≤ V_{IL} Outputs Open f = 0(3)	Military	—	—	600	1440	600	1440	600	1440	mA
			Commercial	600	1200	600	1200	600	1200	600	1200	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ ≤ V_{IL} Outputs Open f = f_{MAX}(4)	Military	—	—	880	1600	840	1580	780	1560	mA
			Commercial	900	1400	880	1360	840	1340	780	1320	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE}$ ≥ V_{IH} f = f_{MAX}(4)	Military	—	—	180	460	160	440	140	420	mA
			Commercial	240	340	180	320	160	300	140	280	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports $\overline{CE}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0(3)	Military	—	—	6	120	6	120	6	120	mA
			Commercial	6	60	6	60	6	60	6	60	

2817 tbl 08

NOTES:
1. V_{CC} = 5V, T_A = +25°C for Typ.
2. 0°C to +70°C temperature range only.
3. f = 0 means no address or control lines change.
4. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. For the case of one port, divide the above appropriate current by four.
6. Typical values are guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS(1)(L VERSION ONLY)

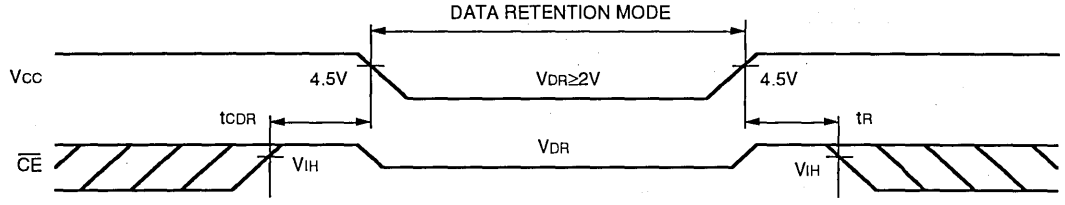
(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	Military	—	100	7200	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	Commercial	—	100	2400	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2817 tbl 09

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by design, but not tested.

LOW Vcc DATA RETENTION WAVEFORM

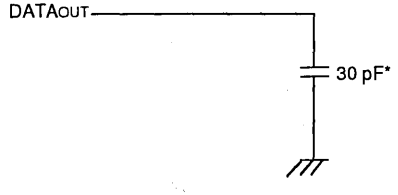


2817 drw 03

AC TEST CONDITIONS

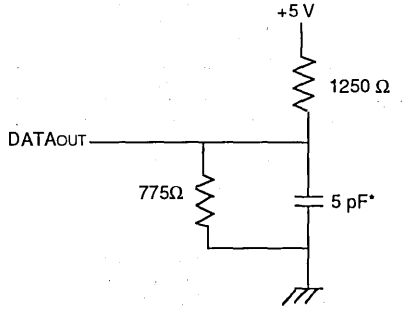
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2817 tbl 10



2817 drw 04

Figure 1. Output Load



2817 drw 05

Figure 2. Output Load (for tOLZ, tOHZ, tWHZ, tOW)

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25ns(3) Min.	-25ns(3) Max.	-30ns Min.	-30ns Max.	-35ns Min.	-35ns Max.	-45ns Min.	-45ns Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	30	—	35	—	45	ns
tOE	Output Enable Access Time	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
tOLZ(1, 2)	$\overline{OE}$ Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tOHZ(1, 2)	$\overline{OE}$ Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tCLZ(1, 2)	$\overline{CE}$ Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tCHZ(1, 2)	$\overline{CE}$ Disable to Output in High Z	—	15	—	15	—	15	—	20	ns
tPU(2)	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD(2)	Chip Disable to Power Down Time	—	20	—	30	—	50	—	50	ns

2817 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design, but not tested.
3. 0°C to +70°C temperature range only.

7

AC ELECTRICAL CHARACTERISTICS

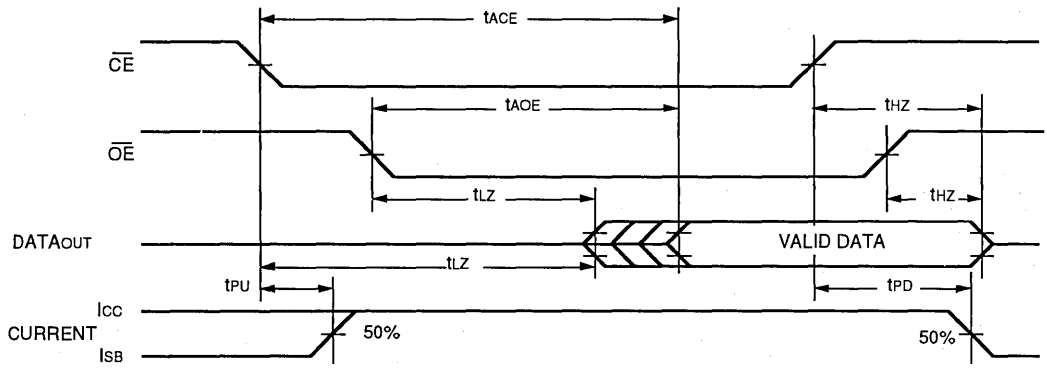
(V_{CC} = 5.0V ± 10%, T_A=-55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25ns[7] Min.	-25ns[7] Max.	-30ns Min.	-30ns Max.	-35ns Min.	-35ns Max.	-45ns Min.	-45ns Max.	Unit
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	ns
t_{CE}	Chip Enable to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}[3]	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	15	—	15	—	20	—	20	—	ns
t_{OHZ}[1, 2]	$\overline{OE}$ to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1, 2]	Write Enabled to Output in High Z	—	15	—	15	—	15	—	20	ns
t_{OW}[1, 2]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{WDD}[4]	Write Pulse to Data Delay	—	45	—	50	—	55	—	65	ns
t_{DDD}[4]	Write Data Valid to Read Data Delay	—	35	—	40	—	45	—	55	ns
$\overline{BUSY}$ CYCLE										
t_{WB}[5]	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	ns
t_{WH}[6]	Write Hold After $\overline{BUSY}$	15	—	20	—	20	—	20	—	ns

NOTES:
2817 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design, but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

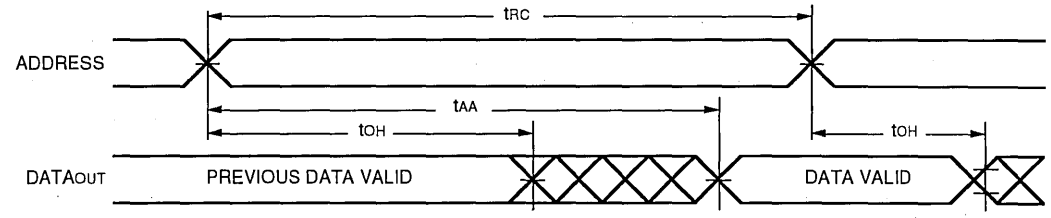
TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT[1, 3]



2817 drw 06

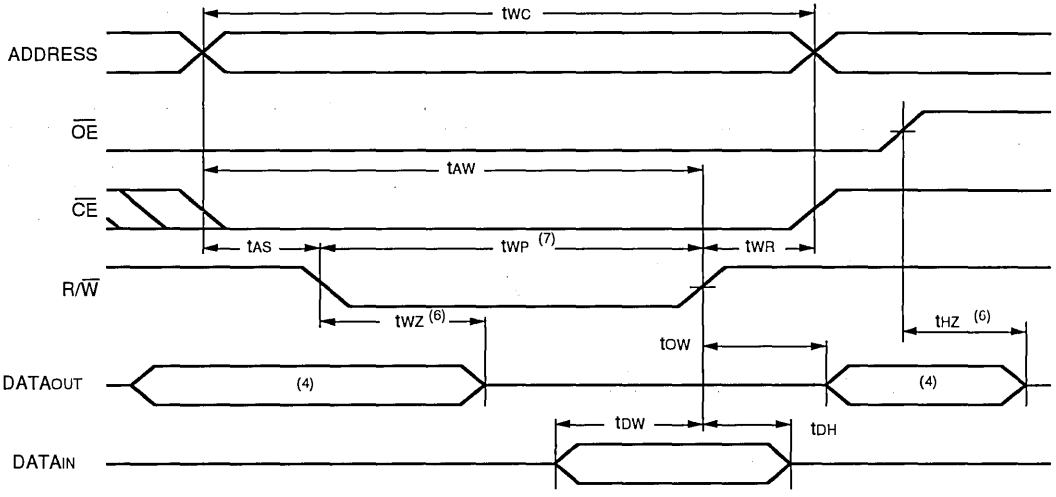
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 2, 4)



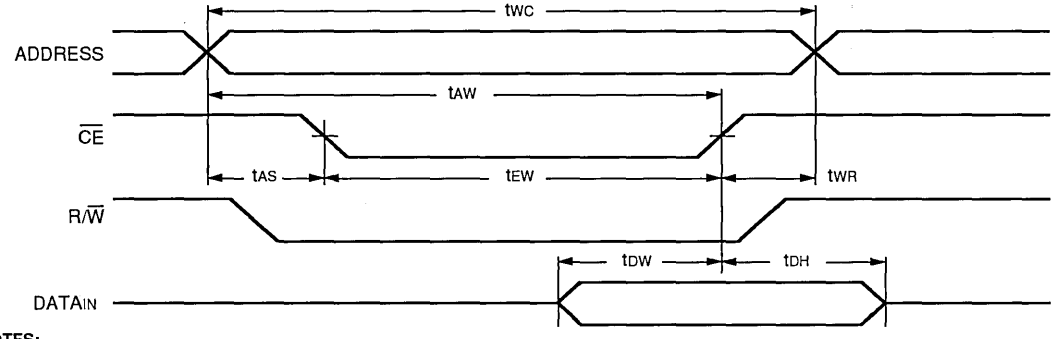
2817 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 7)



2817 drw 08

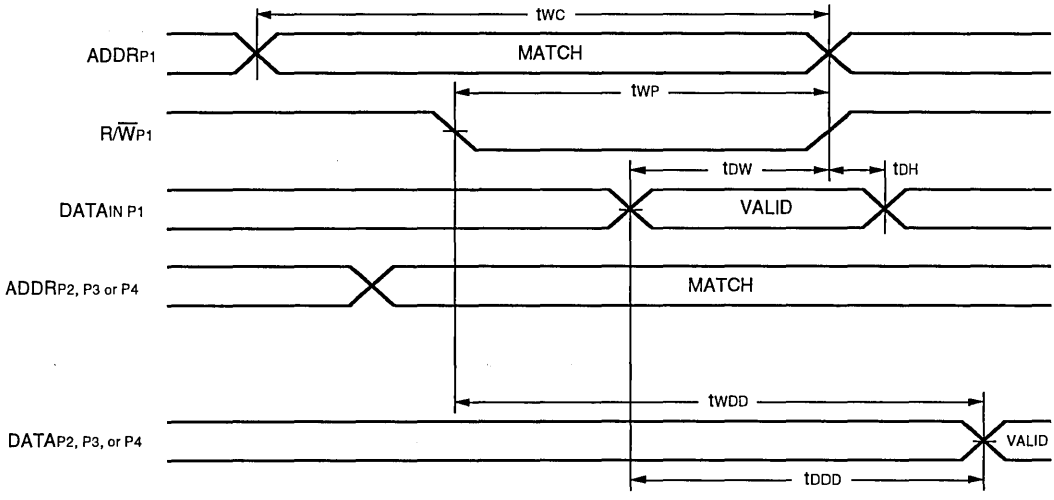
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



2817 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

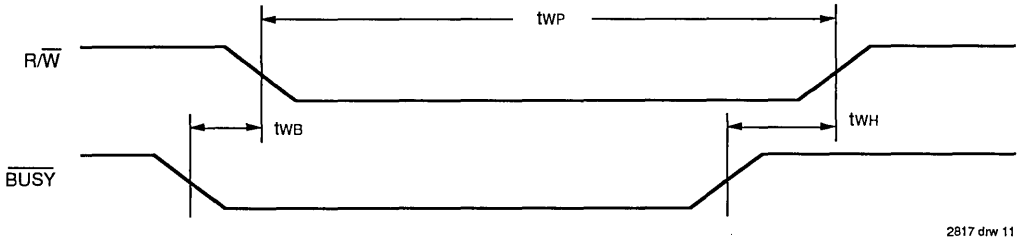
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1, 2, 3)



2817 drw 10

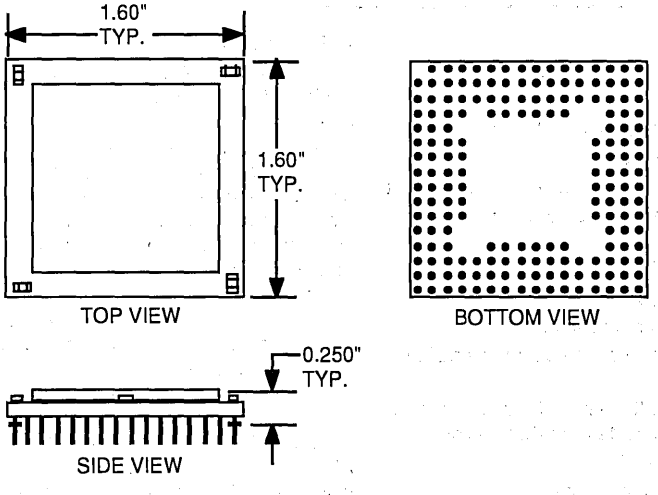
NOTES:
1. Assume $\overline{BUSY}$ input at HIGH and $\overline{CE}$ at LOW for the writing port.
2. Write cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LOW.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2817 drw 11

PACKAGE DIMENSIONS



2817 drw 12

7

Integrated Device Technology, Inc.

16K x 32 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1002

FEATURES

- High density 512K CMOS dual-port RAM module
- Fast access times
  - — Commercial: 25, 30, 35, 40, 45, 55, 65ns
  - — Military: 30, 40, 45, 55, 65ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 64 bits or more using the Master/Slave function
- Separate byte read/write signals for byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted fine pitch (25 mil) LCC packages allow through-hole module to fit into 121 pin PGA footprint
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION

The IDT7M1002 is a 16K x 32 high speed CMOS Dual-Port static RAM Module constructed on a co-fired ceramic substrate using four 16K x 8 (IDT7006) Dual-Port static RAMs in surface-mounted LCC packages. The IDT7M1002 module is designed to be used as stand-alone 512K dual-port RAM or as a combination Master/Slave dual-port RAM for 64-bit or more word width systems. Using the IDT Master/Slave approach in such system applications results in full-speed, error-free operation without the need for additional discrete logic.

The module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ & $\overline{INT}$.

The IDT7M1002 module is packaged in a ceramic 121 pin PGA (Pin Grid Array) 1.35 inches on a side. Maximum access times as fast as 25ns are available over the commercial temperature range and 30ns over the military temperature range.

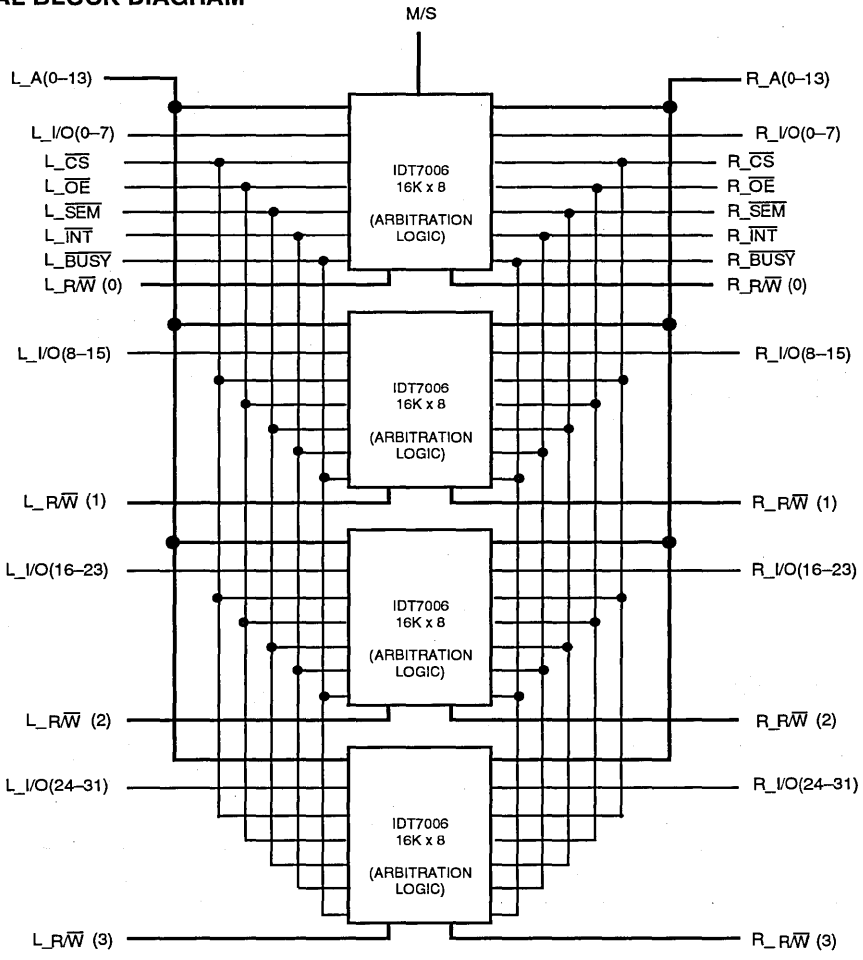
All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	L_I/O(24)	L_I/O(26)	L_I/O(28)	L_I/O(30)	L_$\overline{CS}$	L_$\overline{OE}$	L_R/$\overline{W}$(3)	R_$\overline{OE}$	R_$\overline{CS}$	R_I/O(30)	R_I/O(28)	R_I/O(26)	R_I/O(24)
B	L_I/O(23)	L_I/O(25)	L_I/O(27)	L_I/O(29)	L_I/O(31)	L_A(0)	L_R/$\overline{W}$(4)	R_A(0)	R_I/O(31)	R_I/O(29)	R_I/O(27)	R_I/O(25)	R_I/O(23)
C	L_I/O(21)	L_I/O(22)	VCC	L_A(3)	L_A(2)	L_A(1)	GND	R_A(1)	R_A(2)	R_A(3)	GND	R_I/O(22)	R_I/O(21)
D	L_I/O(19)	L_I/O(20)	L_A(4)	GND							R_A(4)	R_I/O(20)	R_I/O(19)
E	L_I/O(17)	L_I/O(18)	L_A(5)								R_A(5)	R_I/O(18)	R_I/O(17)
F	L_$\overline{SEM}$	L_I/O(16)	L_A(6)				PGA				R_A(6)	R_I/O(16)	R_$\overline{SEM}$
G	L_$\overline{BUSY}$	L_$\overline{INT}$	GND				TOP VIEW				GND	R_$\overline{INT}$	R_$\overline{BUSY}$
H	L_R/$\overline{W}$(1)	L_R/$\overline{W}$(2)	L_A(7)								R_A(7)	R_R/$\overline{W}$ (2)	R_R/$\overline{W}$ (1)
I	L_I/O(15)	L_I/O(14)	L_A(8)								R_A(8)	R_I/O(14)	R_I/O(15)
J	L_I/O(13)	L_I/O(12)	L_A(9)								R_A(9)	R_I/O(12)	R_I/O(13)
K	L_I/O(11)	M/$\overline{S}$	GND	L_A(10)	L_A(11)	L_A(12)	GND	R_A(12)	R_A(11)	R_A(10)	VCC	GND	R_I/O(11)
L	L_I/O(10)	L_I/O(8)	L_I/O(6)	L_I/O(4)	L_I/O(2)	L_A(13)	R_R/$\overline{W}$ (4)	R_A(13)	R_I/O(2)	R_I/O(4)	R_I/O(6)	R_I/O(8)	R_I/O(10)
M	L_I/O(9)	L_I/O(7)	L_I/O(5)	L_I/O(3)	L_I/O(1)	L_I/O(0)	R_R/$\overline{W}$ (3)	R_I/O(0)	R_I/O(1)	R_I/O(3)	R_I/O(5)	R_I/O(7)	R_I/O(9)

2795 drw 01

FUNCTIONAL BLOCK DIAGRAM



2795 drw 02

PIN NAMES

Left Port	Right Port	Description
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–31)	R_I/O (0–31)	Data Inputs/Outputs
L_R/W (1–4)	R_R/W (1–4)	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_BUSY	R_BUSY	Busy Flag
L_INT	R_INT	Interrupt Flag
L_SEM	R_SEM	Semaphore Control
M/S		Master/Slave Control
Vcc		Power
GND		Ground

2795 tbl 01

7

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commerical	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2795 tbl 02

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2795 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2795 tbl 04

NOTE:
1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min. I_{OL} = 4mA Voltage	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA	2.4	—	V

2795 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, $\overline{SEM}$ = Don't Care Outputs Open, f = f_{MAX}	—	1360	—	1600	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	280	—	340	mA
I_{SB1}	Standby Suppy Current (One Port Inactive)	V_{CC} = Max., L_$\overline{CS}$ or R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	1000	—	1160	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	L_$\overline{CS}$ and R_$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $< 0.2V$ L_$\overline{SEM}$ and R_$\overline{SEM} \geq V_{CC} - 0.2V$	—	60	—	120	mA

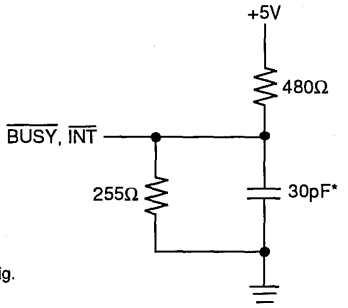
2795 tbl 06

CAPACITANCE [1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN} (1)	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	V_{IN} = 0V	40	pF
$C_{IN(2)}$	Input Capacitance (R/$\overline{W}$, $\overline{I/O}$, $\overline{INT}$)	V_{IN} = 0V	12	pF
$C_{IN(3)}$	Input Capacitance ($\overline{BUSY}$, M/$\overline{S}$)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance (I/O)	V_{OUT} = 0V	12	pF

2795 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.



*Including scope and jig.

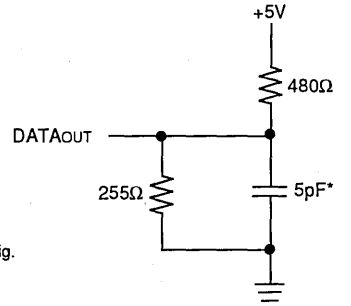
Figure 1. Output Load

2795 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2795 tbl 08



*Including scope and jig.

Figure 2. Output Load

2795 drw 04

(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1002SxxG, 7M1002SxxGB										
		-25[10]		-30[10]		-35[10]		-40		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
t_{OE}	Output Enable Access Time	—	15	—	11	—	20	—	22	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{LZ}[1]	Output to Low Z	3	—	3	—	3	—	3	—	5	—	ns
t_{HZ}[1]	Output to High Z	—	15	—	15	—	15	—	17	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	15	—	15	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns

(Continued on next page)

2795 tbl 09

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

		7M1002SxxG, 7M1002SxxGB										
		-25[10]		-30[10]		-35[10]		-40		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle (continued)												
t_{DW}	Data Valid to End of Write	18	—	22	—	25	—	25	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{HZ}[1]	Output to High Z	—	15	—	15	—	15	—	17	—	20	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	10	—	10	—	ns
Busy Cycle-Master Mode[3]												
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	25	—	30	—	35	—	35	—	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	20	—	25	—	30	—	30	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	20	—	25	—	30	—	30	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Deselect	—	20	—	25	—	25	—	25	—	25	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	35	—	40	—	45	—	50	—	55	ns
t_{APS}[6]	Arbitration Priority Set-Up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	ns
Busy Cycle-Slave Mode[4]												
t_{WB}[7]	Write to BUSY Input	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold after BUSY	20	—	25	—	25	—	25	—	25	—	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	—	70	ns
Interrupt Timing												
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	20	—	25	—	30	—	32	—	35	ns
t_{INR}	Interrupt Reset Time	—	20	—	25	—	30	—	32	—	35	ns

2795 tbl 10

NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).
10. Preliminary specifications.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	-55		-65		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55	—	65	—	ns
t_{AA}	Address Access Time	—	55	—	65	ns
t_{ACS}[2]	Chip Select Access Time	—	55	—	65	ns
t_{OE}	Output Enable Access Time	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}[1]	Output to Low Z	5	—	5	—	ns
t_{HZ}[1]	Output to High Z	—	25	—	30	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	55	—	65	—	ns
t_{CW}[2]	Chip Select to End of Write	45	—	50	—	ns
t_{AW}	Address Valid to End of Write	45	—	50	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	30	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{HZ}[1]	Output to High Z	—	25	—	30	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	ns
Busy Cycle-Master Mode[3]						
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	40	—	40	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Deselect	—	35	—	35	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	65	—	75	ns
t_{APS}[6]	Arbitration Priority Set-Up Time	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	ns

(Continued on next page)

2795 tbl 11

7

AC ELECTRICAL CHARACTERISTICS

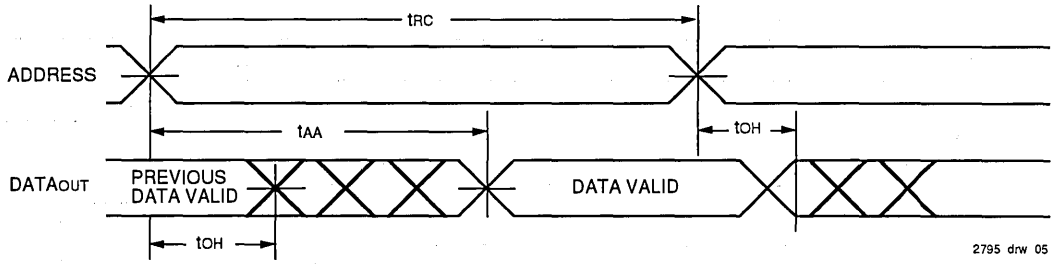
(V_{CC} = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	-55		-65		Unit
		Min.	Max.	Min.	Max.	
Busy Cycle-Slave Mode[4]						
t_{WB}[7]	Write to BUSY Input	0	—	0	—	ns
t_{WH}[8]	Write Hold after BUSY	25	—	25	—	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	80	—	90	ns
Interrupt Timing						
t_{AS}	Address Set-Up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	40	—	45	ns
t_{INR}	Interrupt Reset Time	—	40	—	45	ns

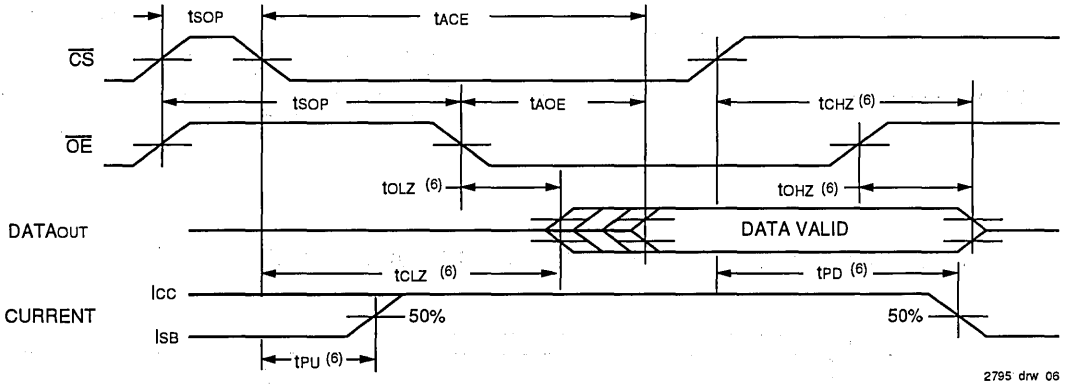
2795 tbl 12

NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



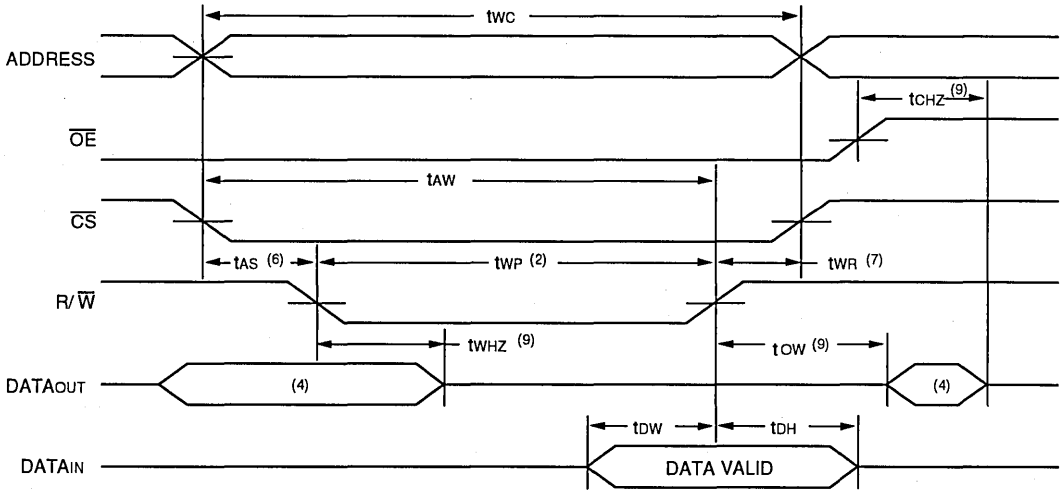
TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3, 5)



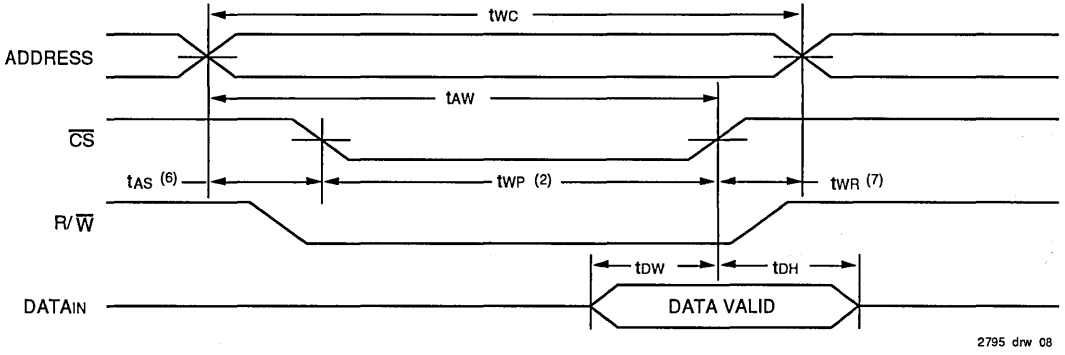
NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled $\overline{CS} \leq V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
6. This parameter is guaranteed by design but not tested.

7

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 2, 4)

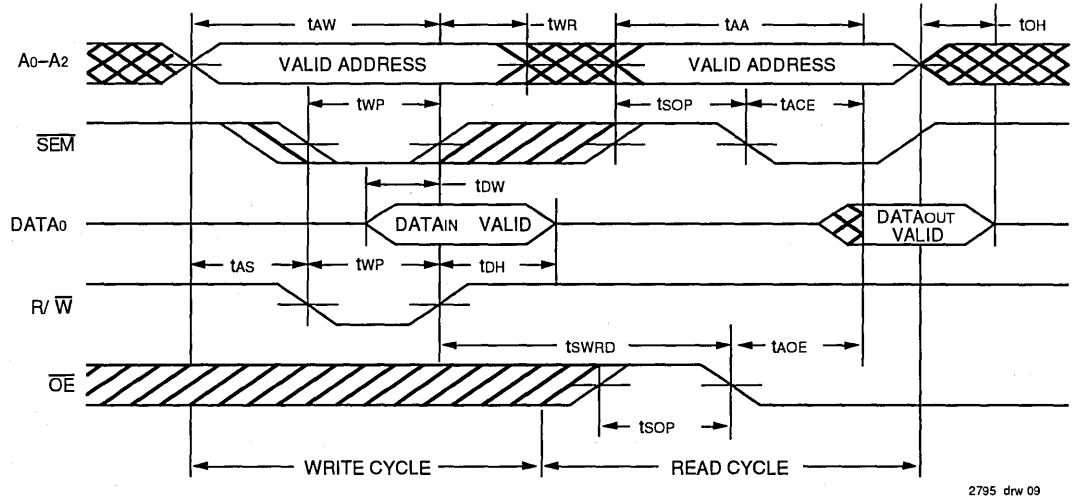


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 4)



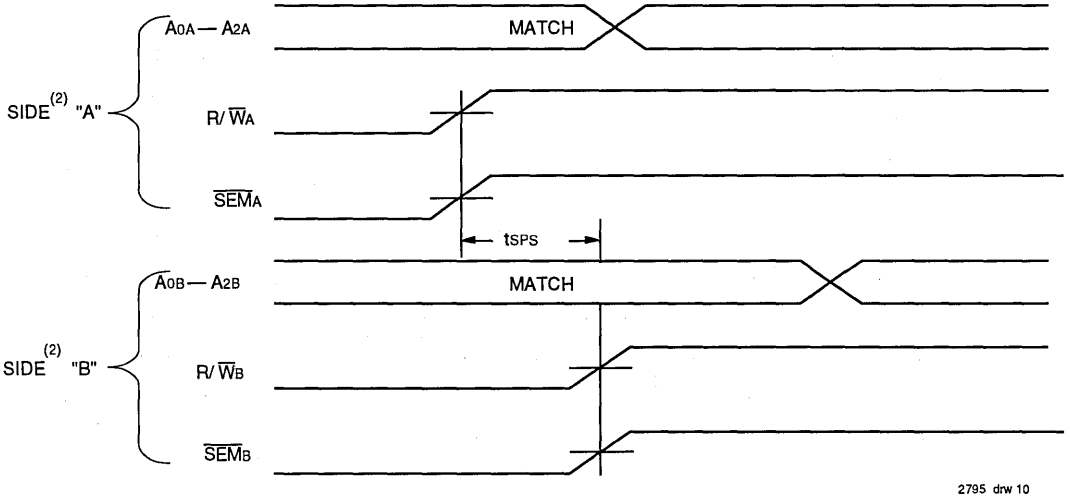
NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE, EITHER SIDE (1)



NOTE:
1. $\overline{CS} \geq V_{IH}$ for the duration of the above timing (both write and read cycle).

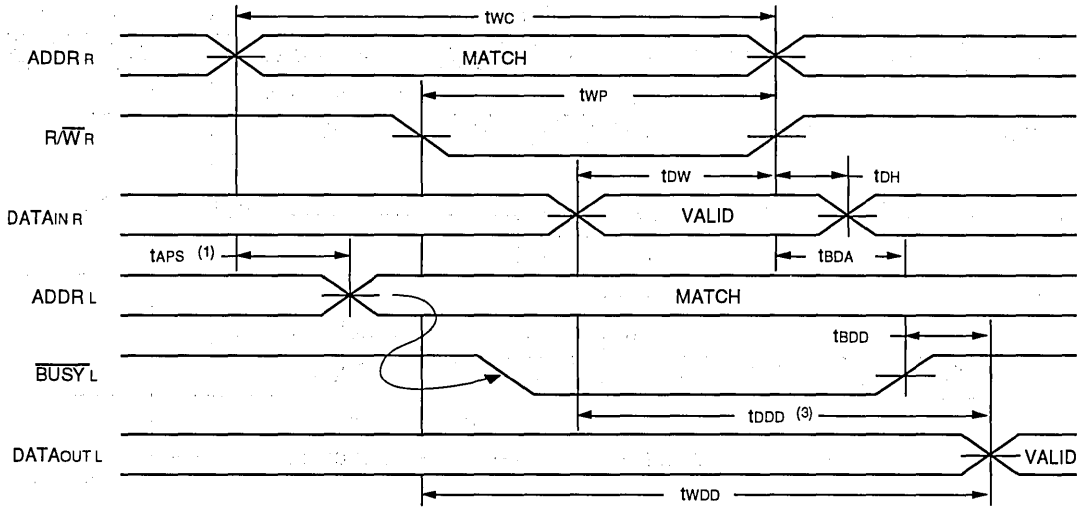
TIMING WAVEFORM OF SEMAPHORE CONTENTION (1, 3, 4)



NOTES:
1. $D_{OR} = D_{OL} \leq V_{IL}$, ($L\_\overline{CS} = R\_\overline{CS}$) $\geq V_{IH}$ Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

7

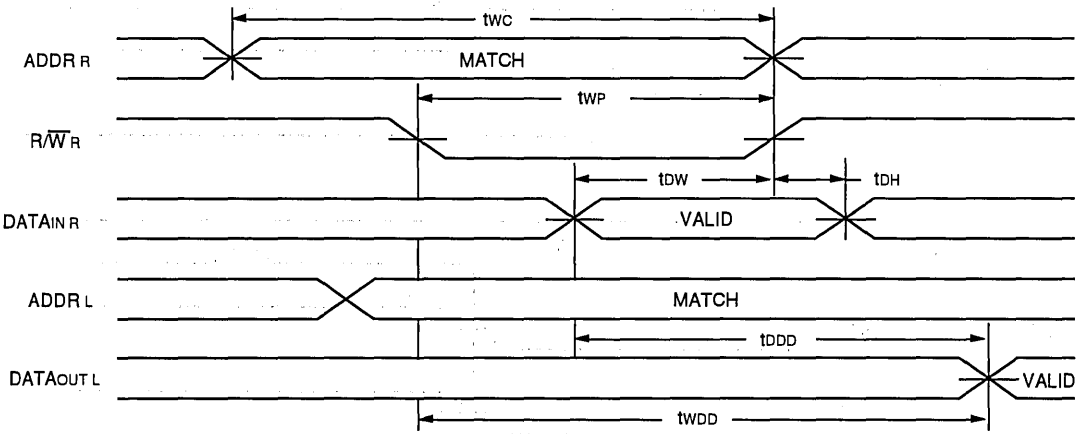
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)(2)



2795 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL
3. $\overline{OE}$ ≤ VIL for the reading port.

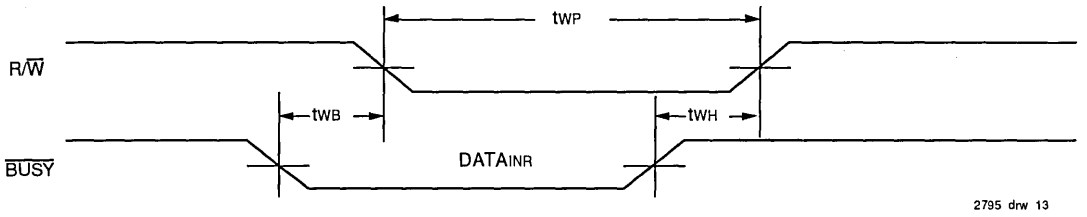
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (M/$\overline{S}$ ≤ VIH) (1, 2)



2795 drw 12

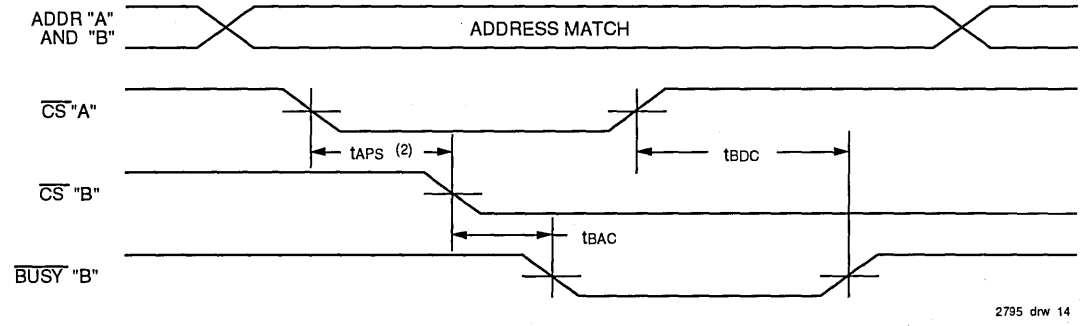
NOTES:
1. $\overline{BUSY}$ input equals High for the writing port.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (M/$\overline{S}$ ≤ VIL)



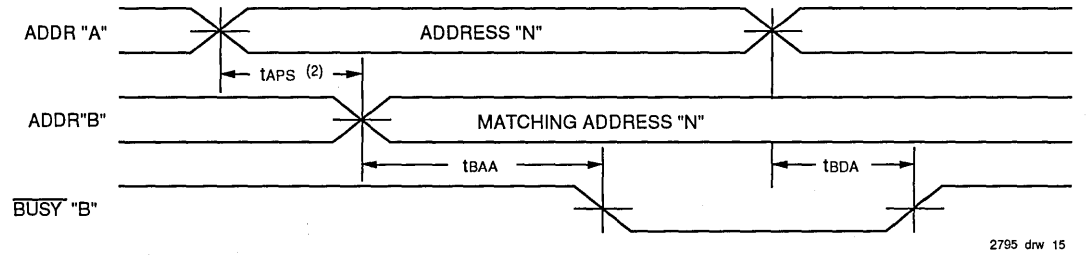
2795 drw 13

TIMING WAVEFORM OF BUSY ARBITRATION ($\overline{CS}$ CONTROLLED TIMING) (1)



2795 drw 14

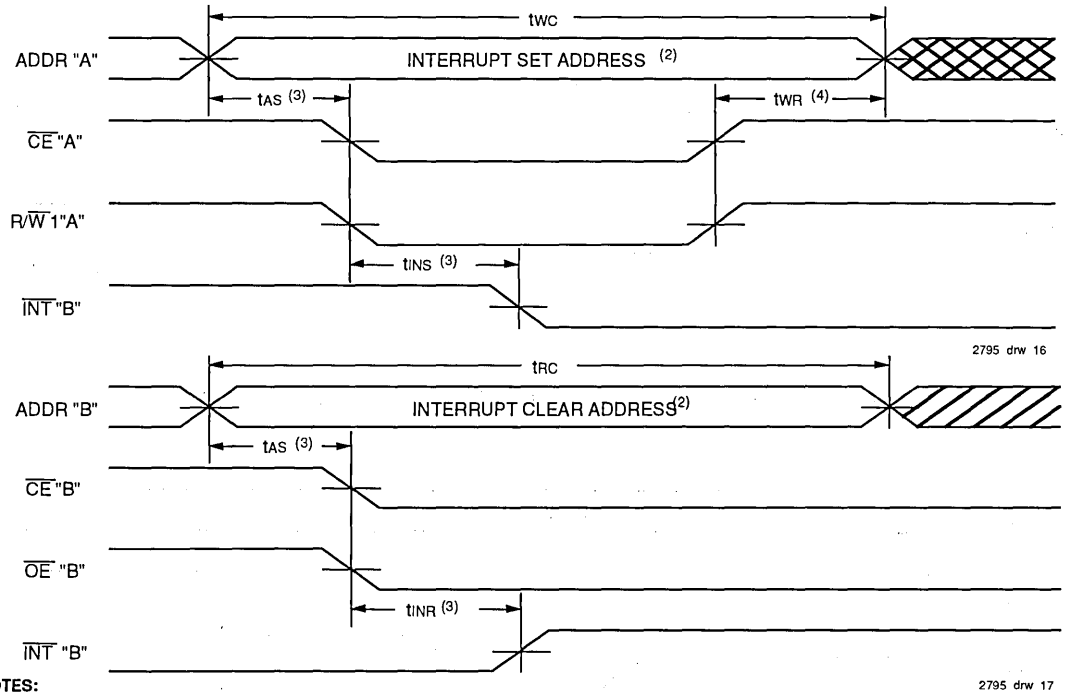
TIMING WAVEFORM OF BUSY ARBITRATION (CONTROLLED BY ADDRESS MATCH TIMING) (1)



2795 drw 15

NOTES:
1. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

TIMING WAVEFORM OF INTERRUPT CYCLE (1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLE I: Non-Contention Read/Write Control (1)

Inputs				Outputs	Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_In	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).
2. ⎍⎍ denotes a LOW to HIGH waveform transition.

2795 tbl 13

TRUTH TABLE II: Semaphore Read/Write Control

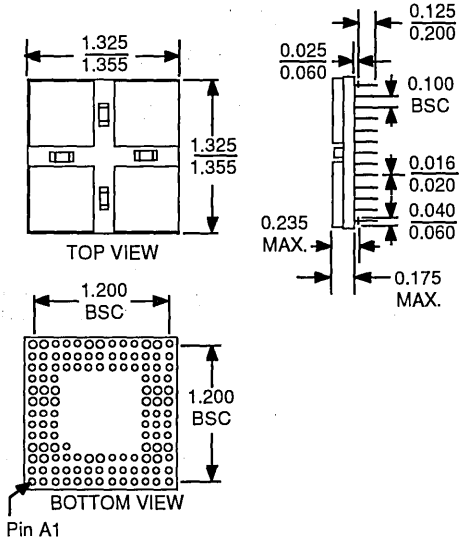
Inputs(2)				Outputs	Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	H	L	L	Data_OUT	Read Data in Semaphore Flag
H	⎍⎍	X	L	Data_IN	Write Data_IN (0, 8, 16, 24)
L	X	X	L	—	Not Allowed

2795 tbl 14

INTERRUPT/BUSY FLAGS, DEPTH & WIDTH EXPANSION, MASTER/SLAVE CONTROL, SEMAPHORES

For more details regarding Interrupt/Busy flags, depth and/or width expansion, master/slave control, or semaphore operations, please consult the IDT7006 data sheet.

PACKAGE DIMENSIONS



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7

Integrated Device Technology, Inc.

4K x 36 BiCMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7M1014

FEATURES

- High density 4K x 36 BiCMOS Dual-Port Static RAM module
- Fast access times
  - — Commercial: 15, 20, 25, 30ns
  - — Military: 20, 25, 30ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a ceramic PGA footprint
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION

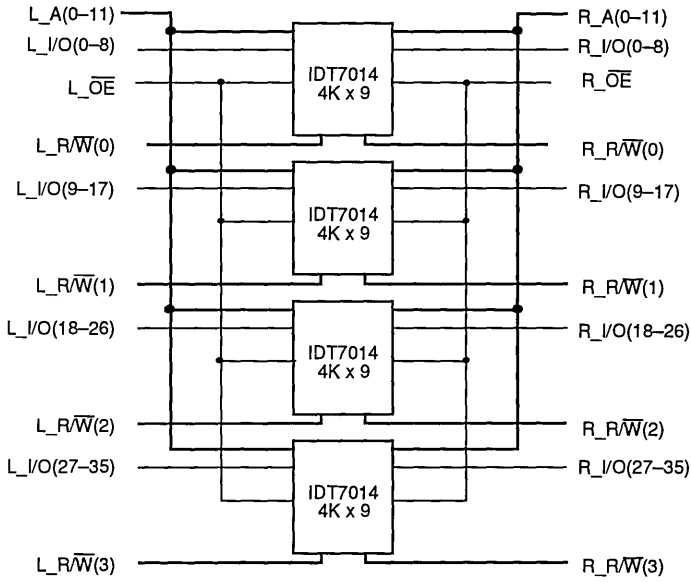
The IDT7M1014 is a 4K x 36 asynchronous high speed BiCMOS Dual-Port static RAM module constructed on a co-fired ceramic substrate using 4 IDT7014 (4K x 9) asynchronous Dual-Port RAMs. The IDT7M1014 module is designed to be used as stand alone 36-bit dual-port RAM.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1014 module is packaged in a ceramic PGA (Pin Grid Array). Maximum access times as fast as 15ns and 20ns are available over the commercial and military temperature range respectively.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2819 drw 01

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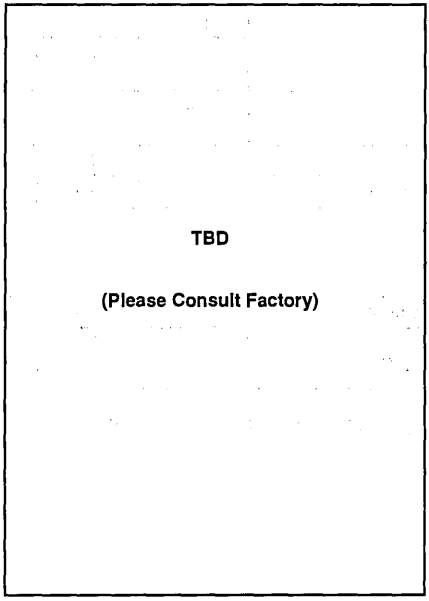
PIN CONFIGURATION



PIN NAMES

Left Port	Right Port	Names
L_R/$\overline{W}$(0-3)	R_R/$\overline{W}$(0-3)	Read/Write Enables
L_$\overline{OE}$	R_$\overline{OE}$	Output Enables
L_A (0–11)	R_A (0–11)	Address Inputs
L_I/O (0–35)	R_I/O (0–35)	Data Input/Outputs
Vcc		Power
GND		Ground

2819 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2819 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.
3. I/O terminals only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2819 tbl 03

1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2819 tbl 04

CAPACITANCE TABLE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$)	V_{IN} = 0V	50	pF
C_{IN}(2)	Input Capacitance (Data, R/$\overline{W}$)	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	15	pF

NOTE: 2819 tbl 05

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage V_{IN} = GND to V_{CC}	V_{CC} = Max.	—	40	µA
$\|I_{LO}\|$	Output Leakage $\overline{OE} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	V_{CC} = Max.	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	V

2819 ttbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC}	Operating Current	V_{CC} = Max., Outputs Open, f = f_{MAX}(1)	—	1040	mA

2819 tbl 07

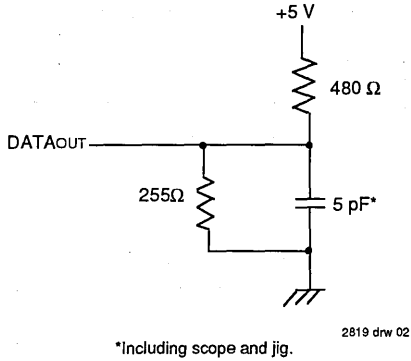
NOTES:

1. At f=f_{MAX}, address and data inputs (except $\overline{OE}$) are cycling at the maximum frequency of read cycle of 1/tRC, and using "AC TEST CONDITIONS" of input levels of GND to 3V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-3

2819 tbl 08



*Including scope and jig.

Figure 1. Output Load
(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

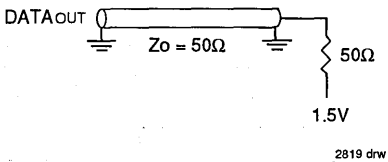


Figure 2. Alternate Output Load

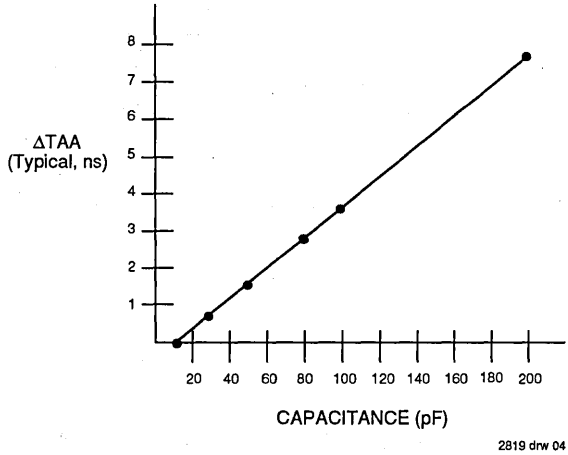


Figure 3. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

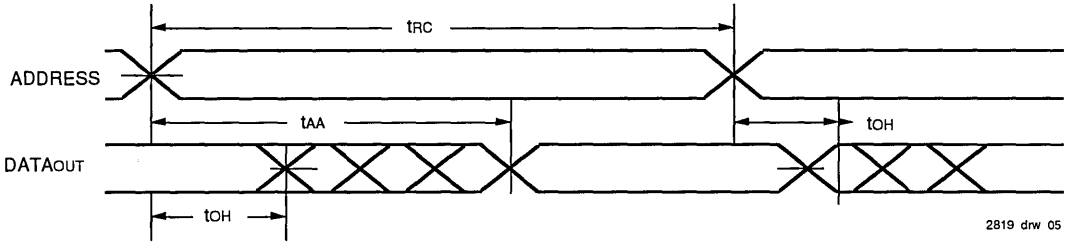
(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1014SxxG, 7M1014SxxGB								
		-15[3]		-20		-25		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{OE}	Output Enable Access Time	—	8	—	10	—	12	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	9	—	11	—	15	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AW}	Address Valid to End of Write	14	—	15	—	20	—	30	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	1	—	2	—	2	—	2	—	ns
t_{DW}	Data Valid to End of Write	10	—	12	—	15	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	7	—	9	—	11	—	15	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay	—	30	—	40	—	45	—	55	ns
t_{DDD}[1]	Write Data Valid to Read Data Delay	—	25	—	30	—	35	—	45	ns

NOTES:
2819 tbl 09

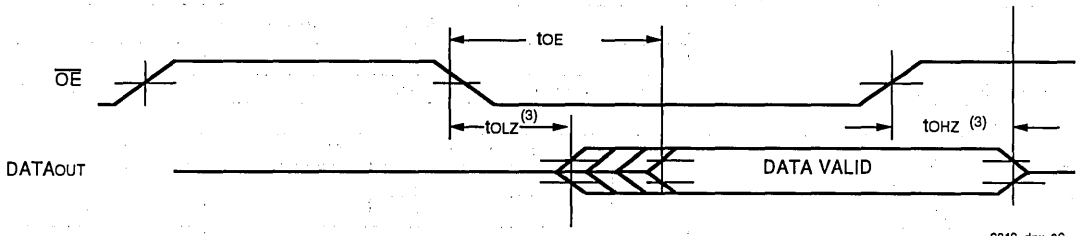
1. This parameter is guaranteed by design but not tested.
2. Port-to-Port delay through the RAM cells from the writing port to the reading port.
3. Commercial specification only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) [1,2]



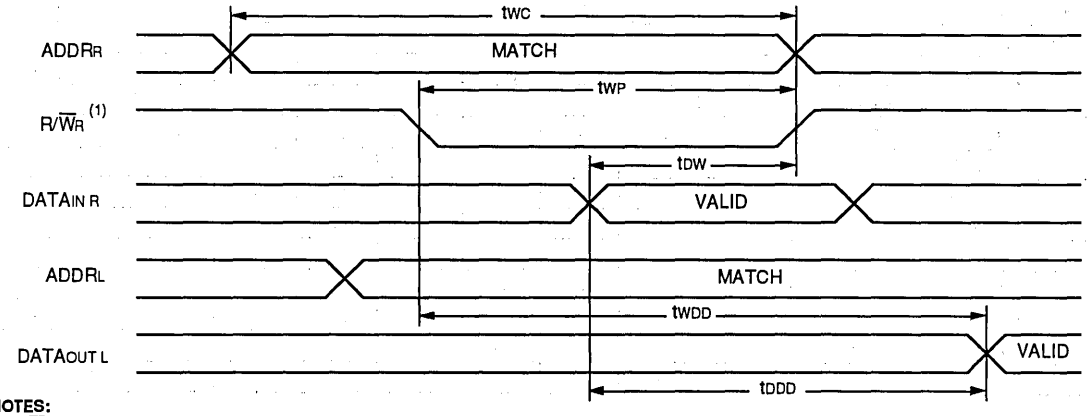
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. $\overline{OE} \leq V_{IL}$

TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 2)



2819 drw 06

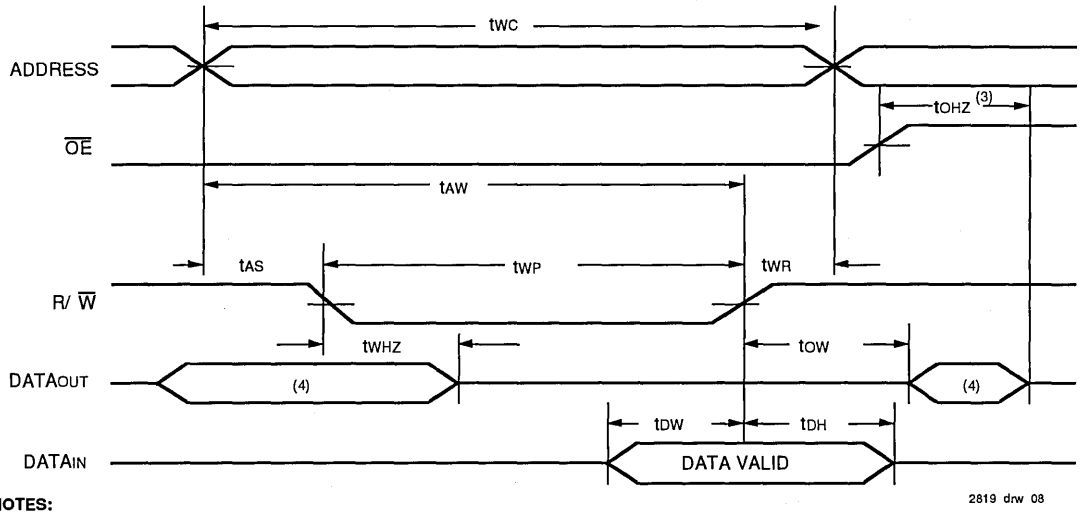
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY



2819 drw 07

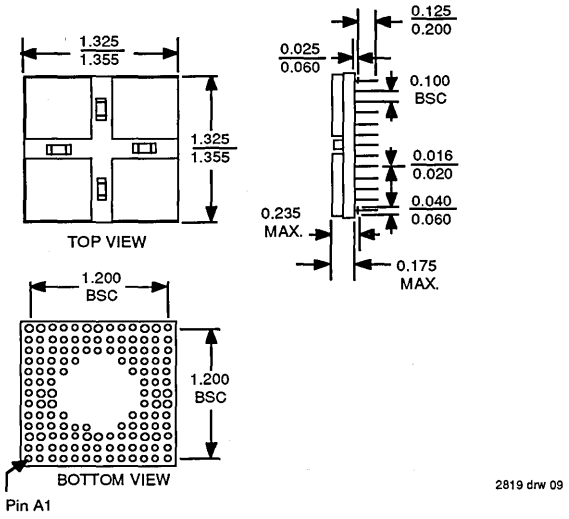
NOTES:
1. R/W is high for Read Cycles.
2. Adress valid prior to OE transition low.
3. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE (EITHER SIDE) (1,2)



NOTES:
1. R/$\overline{W}$ is high during all address transitions.
2. If $\overline{OE}$ is low during the write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high, this requirement does not apply, and the write pulse can be as short as the specified tWP.
3. This parameter is guaranteed by design but not tested.
4. During this period, the I/O pins are in the output state and input signals must not be applied.

PACKAGE DIMENSIONS



Integrated Device Technology, Inc.

4K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM MODULE

ADVANCE INFORMATION
IDT7M1024

FEATURES:

- High density 4K x 36 Synchronous Dual-Port SRAM module
- 50MHz operation
- IDT's BiCEMOS™ process technology
- Architecture based on dual-port RAM cells
  - — Allows full simultaneous access from both ports
- Synchronous operation
  - — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 15ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 20ns cycle time, 50MHz operation
- Clock enable feature
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION:

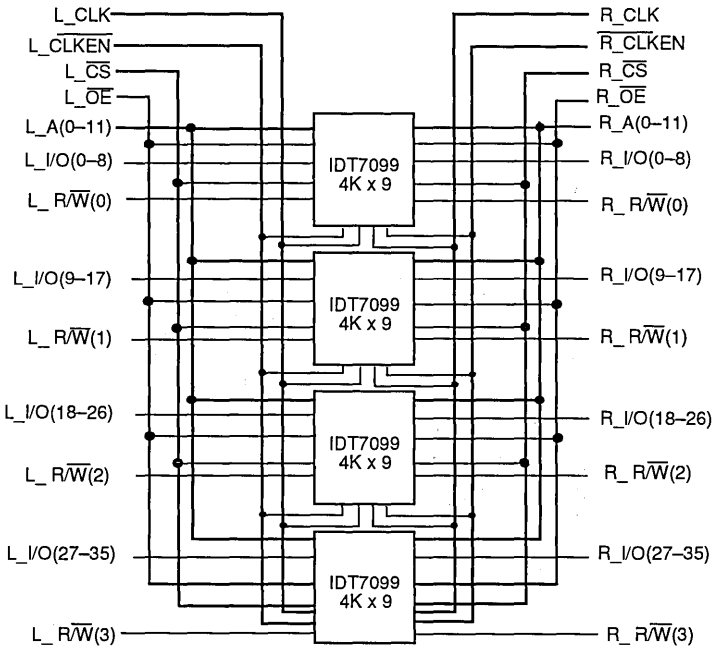
The IDT7M1024 is a 4K x 36 bit high speed synchronous Dual-Port static RAM module constructed on a co-fired ceramic substrate using four IDT7099 (4K x 9) Dual-Port RAMs. The IDT7M1024 module is designed to be used as a stand alone 36-bit Dual-Port static RAM.

The IDT7099 (4K x 9) Dual-Port RAMs have registers on address inputs, control and data lines, providing for low set-up and hold times for the IDT7M1024 module.

The IDT7M1024 module is packaged in a 144-pin ceramic PGA (Pin Grid Array), with a cycle time as fast as 20ns providing 50MHz operation.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

2809 drw 01

Integrated Device Technology, Inc.

2K x 36 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1012

FEATURES

- High density 2K x 36 CMOS Dual-Port Static RAM module
- Fast access times
  - — Commercial: 25, 30, 40, 50, 60ns
  - — Military: 30, 40, 50, 60, 70ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a 121-pin PGA footprint
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION

The IDT7M1012 is a 2K x 36 high speed CMOS Dual-Port static RAM module constructed on a co-fired ceramic substrate using four IDT7012 (2K x 9) Dual-Port RAMs. The IDT7M1012 modules are designed to be used as stand alone 36-bit dual-port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1012 module is packaged in a 121-pin ceramic PGA (Pin Grid Array), resulting in package dimensions of only 1.36" x 1.36" x 0.28". Maximum access times as fast as 25ns/30ns are available over the commercial/military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION[1]

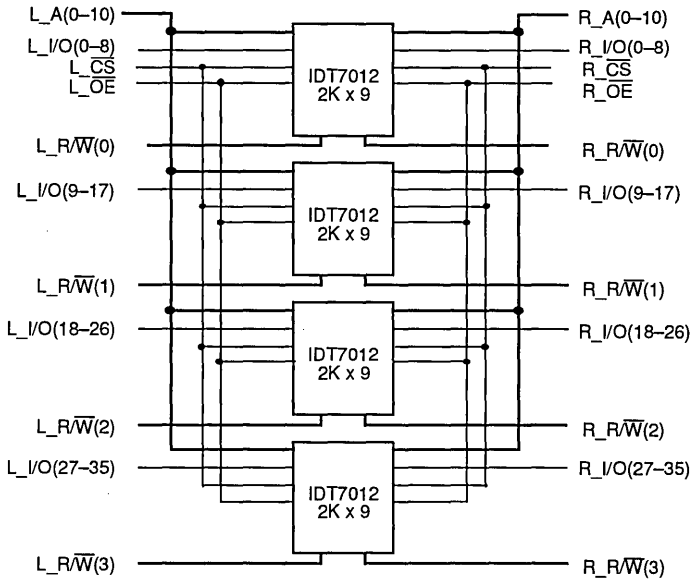
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	GND	L_R/$\overline{W}$(3)	R_R/$\overline{W}$(3)	R_I/O(20)	R_I/O(22)	R_I/O(25)	L_I/O(27)	L_I/O(28)	L_I/O(30)	L_I/O(32)	L_R/$\overline{W}$(4)	R_R/$\overline{W}$(4)	R_I/O(35)	A
B	L_I/O(18)	R_I/O(18)	R_I/O(19)	R_I/O(21)	R_I/O(23)	R_I/O(24)	R_I/O(26)	L_I/O(29)	L_I/O(31)	L_I/O(33)	VCC	L_I/O(34)	R_I/O(34)	B
C	L_I/O(19)	L_I/O(23)	VCC	L_A(0)	L_A(9)	L_A(10)	GND	R_A(10)	R_A(9)	R_A(0)	GND	L_I/O(35)	R_I/O(33)	C
D	L_I/O(20)	L_I/O(24)	L_A(1)	GND							R_A(1)	R_I/O(27)	R_I/O(32)	D
E	L_I/O(21)	L_I/O(25)	L_A(2)								R_A(2)	R_I/O(28)	R_I/O(31)	E
F	L_I/O(22)	L_I/O(26)	L_A(3)								R_A(3)	R_I/O(29)	R_I/O(30)	F
G	GND	L_$\overline{CS}$	GND				PGA Top View				GND	R_$\overline{CS}$	GND	G
H	L_R/$\overline{W}$(1)	L_$\overline{OE}$	R_R/$\overline{W}$(1)								L_R/$\overline{W}$(2)	R_$\overline{OE}$	R_R/$\overline{W}$(2)	H
J	L_I/O(0)	R_I/O(3)	L_A(4)								R_A(4)	L_I/O(15)	R_I/O(17)	J
K	L_I/O(1)	R_I/O(2)	L_A(5)								R_A(5)	L_I/O(16)	R_I/O(16)	K
L	L_I/O(2)	R_I/O(1)	GND	L_A(6)	L_A(7)	L_A(8)	GND	R_A(8)	R_A(7)	R_A(6)	VCC	GND	R_I/O(15)	L
M	L_I/O(3)	R_I/O(0)	VCC	R_I/O(4)	R_I/O(5)	R_I/O(7)	R_I/O(8)	L_I/O(11)	L_I/O(12)	L_I/O(13)	L_I/O(14)	L_I/O(17)	R_I/O(14)	M
N	L_I/O(4)	L_I/O(5)	L_I/O(6)	L_I/O(7)	L_I/O(8)	R_I/O(6)	L_I/O(9)	L_I/O(10)	R_I/O(9)	R_I/O(10)	R_I/O(11)	R_I/O(12)	R_I/O(13)	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

2821 drw 01

NOTES:

1. For the IDT7M1011 (1K x 36 version), Pins C6 and C8 (L_A(10) and R_A(10) respectively) must be connected to VCC for proper operation of the module.

FUNCTIONAL BLOCK DIAGRAMS



2821 drw 02

PIN NAMES

Left Port	Right Port	Names
L_CS	R_CS	Chip Selects
L_R/W(1-4)	R_R/W(1-4)	Read/Write Enables
L_OE	R_OE	Output Enables
L_A (0–10)	R_A (0–10)	Address Inputs
L_I/O (0–35)	R_I/O (0–35)	Data Input/Outputs
VCC		Power
GND		Ground

2821 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

2821 tbl 02

NOTE:
1. VIL = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2821 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2821 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE TABLE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$)	V_{IN} = 0V	50	pF
C_{IN}(2)	Input Capacitance (Data, R/$\overline{W}$)	V_{IN} = 0V	15	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2821 tbl 05

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	V

2821 tbl 06

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.(1)	Max.(2)	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, Outputs Open, f = f_{MAX}	—	1040	1240	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., $\overline{CS}$_L and $\overline{CS}$_R ≥ V_{IH} Outputs Open, f = f_{MAX}	—	260	320	mA
I_{SB1}	Standby Supply Current (One Port Inactive)	V_{CC} = Max., $\overline{CS}$_L o $\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	700	800	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}$_L and $\overline{CS}$_R ≥ V_{CC} –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V	—	60	120	mA

NOTES:
1. For commercial grade (0°C to +70°C) versions only.
2. For military grade (-55°C to +125°C) versions only.

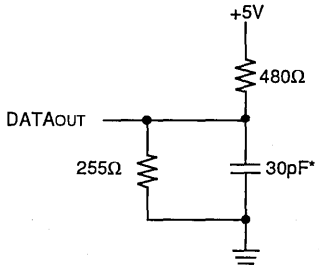
2821 tbl 07

7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2821 tbl 08



*Including scope and jig.

Figure 1. Output Load 2821 drw 03

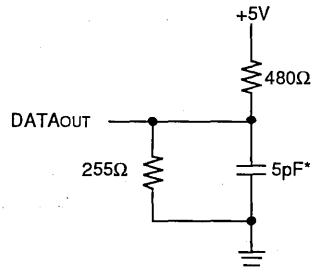


Figure 2. Output Load 2821 drw 04
(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

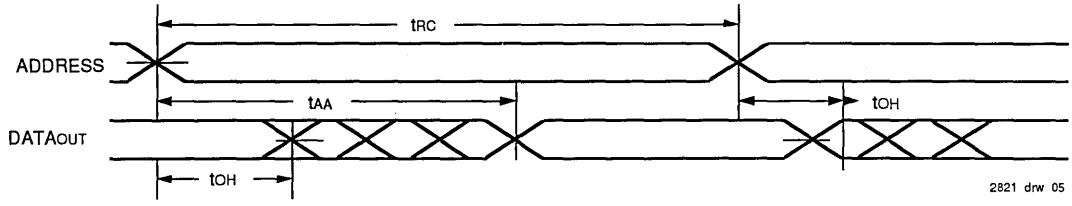
(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1012SxxG, 7M1012SxxGB												
		-25[3]		-30		-40		-50		-60		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	40	—	50	—	60	—	70	ns
t_{OE}	Output Enable Access Time	—	12	—	15	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle														
t_{WC}	Write Cycle Time	25	—	30	—	40	—	50	—	60	—	70	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	12	—	15	—	20	—	20	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	12	—	15	—	20	—	30	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

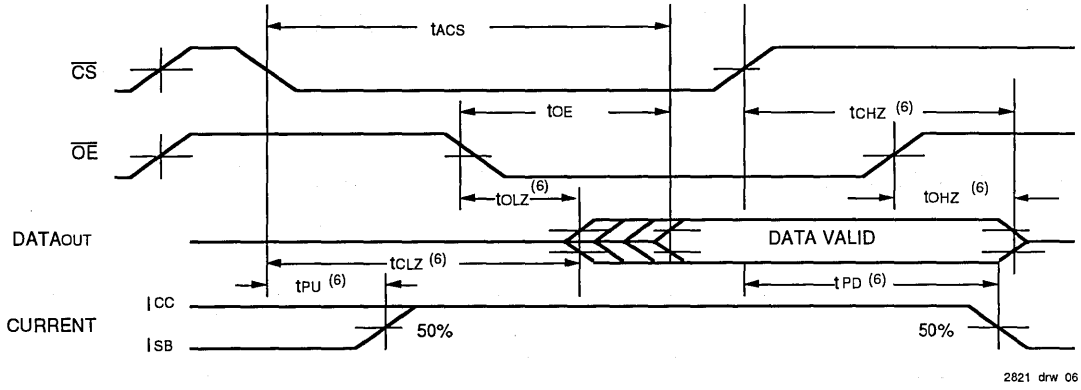
NOTES:
2821 tbl 09

1. This parameter is guaranteed by design but not tested.
2. Port-to-Port delay through the RAM cells from the writing port to the reading port.
3. Preliminary specification only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



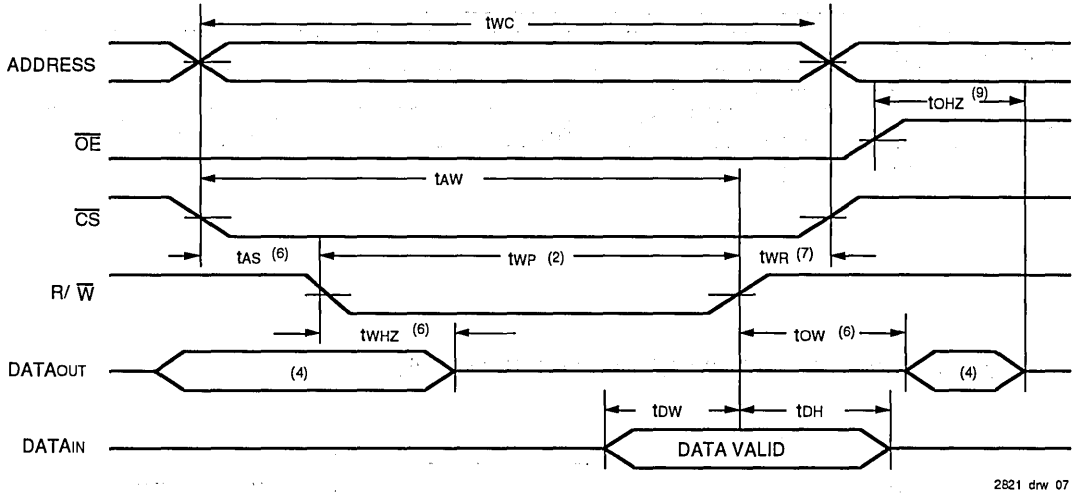
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



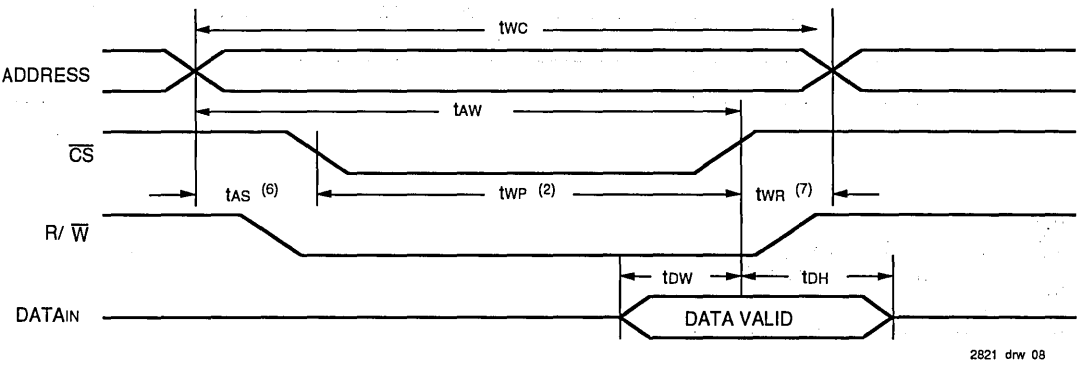
NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS} \leq V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS}$ = L.
6. This parameter is guaranteed by design but not tested.

7

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 3, 5, 8)

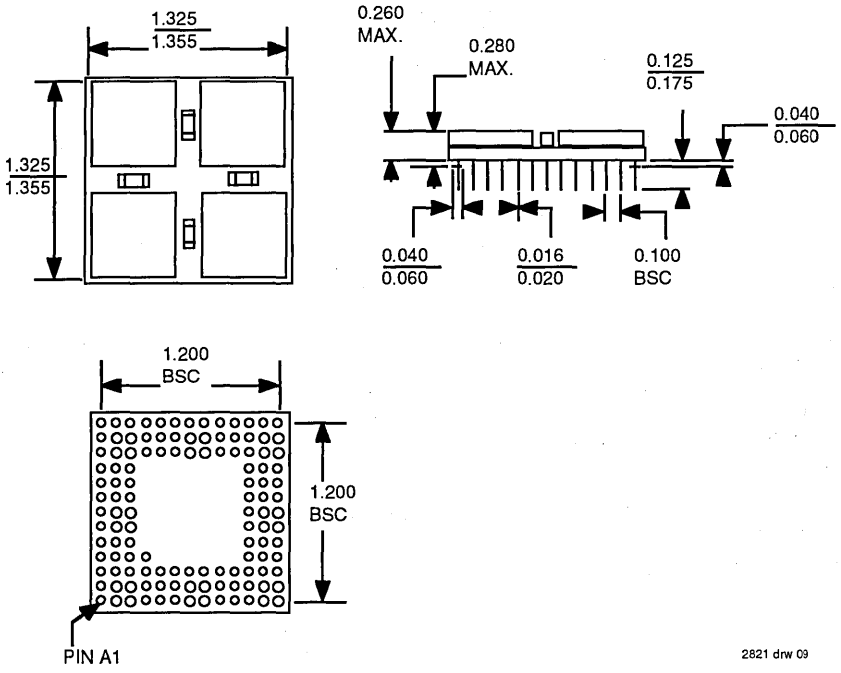


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 3, 5, 8)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply. and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

PACKAGE DIMENSIONS



2821 drw 09

7

Integrated Device Technology, Inc.

128K x 16
64K x 16
32K x 16
CMOS DUAL-PORT RAM
(SHARED MEMORY MODULE)

IDT7MB6036
IDT7MB6046
IDT7MB6056

FEATURES:

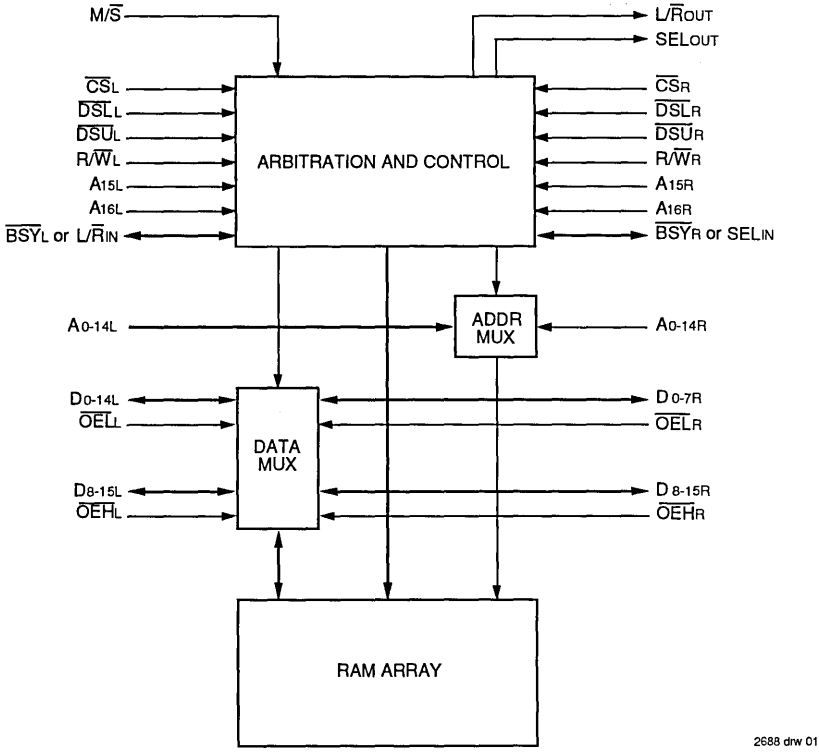
- High density 2 megabit/1 megabit/512K-bit CMOS Dual-Port static RAM (shared memory modules)
- Fully asynchronous read/write operation from either port
- Port arbitration/multiplexing logic by custom FCT chip set
- Memory array comprised of industry standard static RAM component
- Fast access time
  - 40ns (max.)
- Versatile controls: $\overline{BUSY}$ output flag and separate controls for lower and upper byte writes on each port
- Master/Slave control on-board for expanding word width
- Multiple GND and Vcc pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

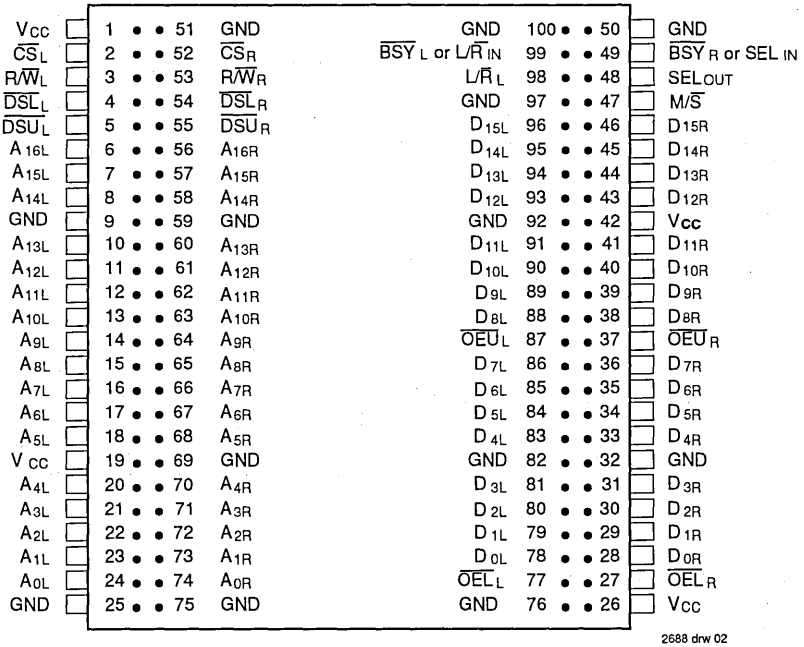
The Shared Memory Module provides two ports with separate control, address and Data I/O pins that permit independent access for read or writes to any location in the memory array. Using the on-board Master/Slave input allows these modules to be used as building blocks in 32-bit or more-bit systems requiring full speed operation without additional discrete logic.

In the Master Mode, the Shared Memory Module arbitrates asynchronously between the left and right ports $\overline{CS}$ inputs. The first to arrive is granted exclusive access to the entire RAM array for as long as its $\overline{CS}$ is asserted. If both ports attempt simultaneous access, the losing port will have its $\overline{BUSY}$ asserted until the winning port completes it access, at which time the second port will be granted its own exclusive access to the entire RAM array. See application note AN-74 for more details regarding proper module operating modes.

FUNCTIONAL BLOCK DIAGRAM[1]



PIN CONFIGURATION (1, 2)



2688 drw 02

NOTES:
1. Pins 7 and 57 must be grounded for proper operation of the 7MB6046 module.
2. Pins 6, 7, 56 and 57 must be grounded for proper operation of the 7MB6056 module.

PIN DESCRIPTION

Symbol	Description
V_{CC}	Power
GND	Ground
A_{0-16L}	Left Port Address
D_{0-15L}	Left Port Data
A_{0-16R}	Right Port Address
D_{0-15R}	Right Port Data
R/$\overline{W}$	Read/Write Control
$\overline{CS}$	Active Low Chip Select
$\overline{DSL}$	Data Strobe for Lower Byte
$\overline{DSU}$	Data Strobe for Upper Byte
$\overline{OEL}$	Output Enable for Lower Byte
$\overline{OEU}$	Output Enable for Upper Byte
$\overline{BSY}_L$ or L/$\overline{R}_{IN}$	Left Busy Output for Stand Alone or Master Mode. Left or Right Port Select Input for Slave Mode.
$\overline{BSY}_R$ or SEL_{IN}	Right Busy Output for Stand Alone or Master Mode. RAM Array Select Input for Slave Mode.
L/$\overline{R}_{OUT}$	Left or Right Port Select Output on Master to be Connected to L/$\overline{R}$_IN Input on One or More Slaves when Width Expansion is Required.
SEL_{OUT}	RAM Array Select Output on Master to be Connected to SEL_IN Input on One or More Slaves when Width Expansion is Required.
M/$\overline{S}$	Master/Slave signal for cascading master w/one or more slaves.

2688 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2688 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	20	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2688 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2688 tbl 04

1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2688 tbl 05

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

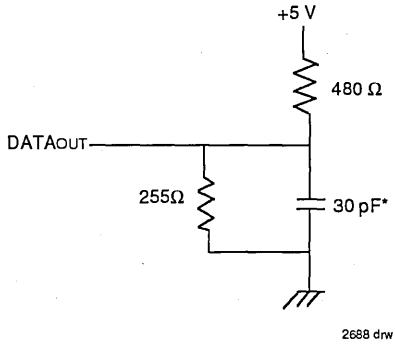
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage Current	VCC = Max. VIN = GND to VCC	—	15	µA
|ILO|	Output Leakage Current	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	—	15	µA
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL, f = fMAX, Output Open	—	520	mA
ISB	Standby Power Supply Current	$\overline{CS}$ ≥ VIH, VCC= MAX. Outputs Open, f = fMAX.	—	200	mA
VOH	Output High Voltage	VCC = Min. IOH = –8mA	2.4	—	V
VOL	Output Low Voltage	VCC = Min. IOL = 16mA		0.4	V

2688 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2688 tbl 07



*Including scope and jig.

Figure 1. Output Load

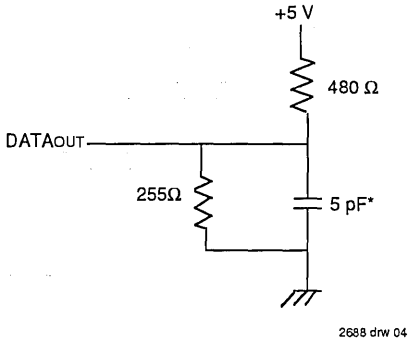


Figure 1. Output Load (for tOHZ and tOLZ)

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V + 10%, TA = 0°C to +70°C)

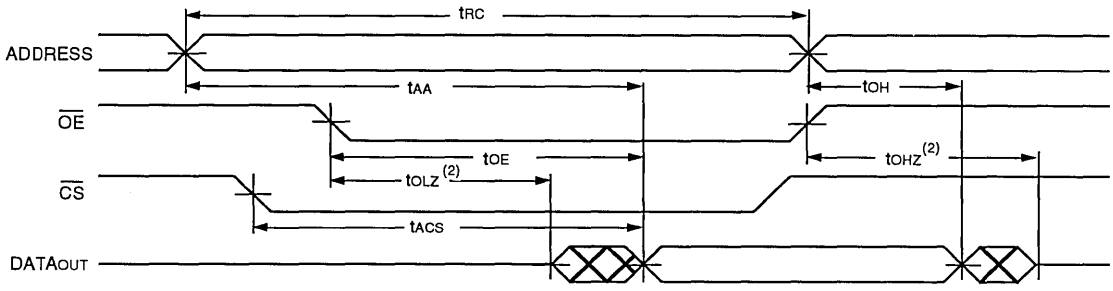
Symbol	Parameter	-40 Min.	-40 Max.	-50 Min.	-50 Max.	-60 Min.	-60 Max.	-70 Min.	-70 Max.	-85 Min.	-85 Max.	-100 Min.	-100 Max.	Unit
No Contention Read														
tRC	Read Cycle Time	40	—	50	—	60	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	40	—	50	—	60	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	40	—	50	—	60	—	70	—	85	—	100	ns
tOE	Output Enable to Data Valid	22	—	—	27	—	32	—	37	—	42	—	47	ns
tOH	O/P Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOLZ(1)	$\overline{OE}$ to Output in Low-Z	8	—	8	—	8	—	8	—	8	—	8	—	ns
tOHZ(1)	$\overline{OE}$ to Output in High-Z	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	—	7.5	ns
No Contention Write														
tWC	Write Cycle Time	40	—	50	—	60	—	70	—	85	—	100	—	ns
tAW	Address Valid to End of Write	35	—	45	—	50	—	60	—	75	—	90	—	ns
tCW	$\overline{CS}$ to End of Write	35	—	45	—	50	—	60	—	75	—	90	—	ns
tAS	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCDS	$\overline{CS}$ to Data Strobe	15	—	15	—	15	—	15	—	15	—	15	—	ns
tDS	Data Strobe Width	20	—	25	—	30	—	35	—	50	—	60	—	ns
tWR	Write Recovery Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
tDW	Data Valid to End of Write	22	—	22	—	25	—	30	—	45	—	50	—	ns
tDH	Data Hold from End of Write	5	—	5	—	5	—	5	—	10	—	10	—	ns
Contention Read														
tCB	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	15	—	20	—	20	ns
tBD	Busy Negate to Data Valid	—	40	—	50	—	60	—	70	—	85	—	100	ns
Contention Write														
tCB	$\overline{CS}$ to BUSY	—	12	—	12	—	12	—	15	—	20	—	20	ns
tBDS	Busy Negate to Data Strobe	7	—	7	—	7	—	10	—	15	—	15	—	ns
Slave Timing														
tLR	$\overline{CS}$ to L/R Output	—	11	—	11	—	11	—	15	—	20	—	20	ns
tSEL	$\overline{CS}$ to Select Output	—	14	—	14	—	14	—	15	—	20	—	20	ns
tAPS	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter guaranteed by design but not tested.

2688 tbl 08

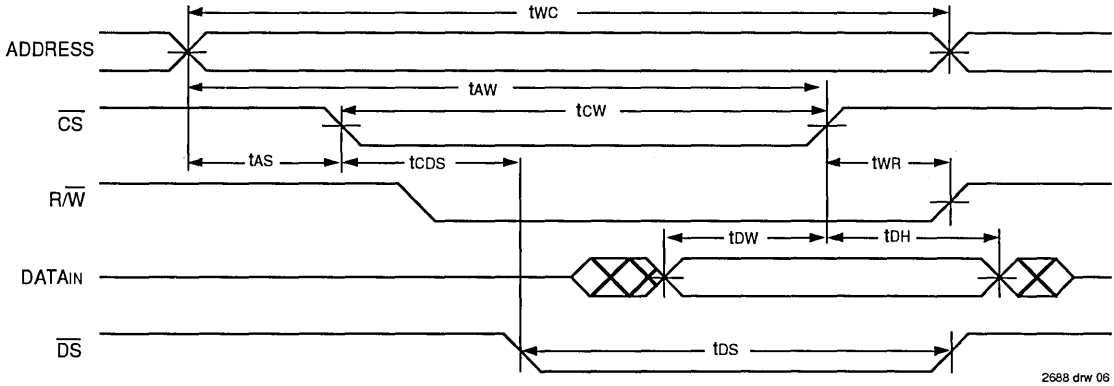
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



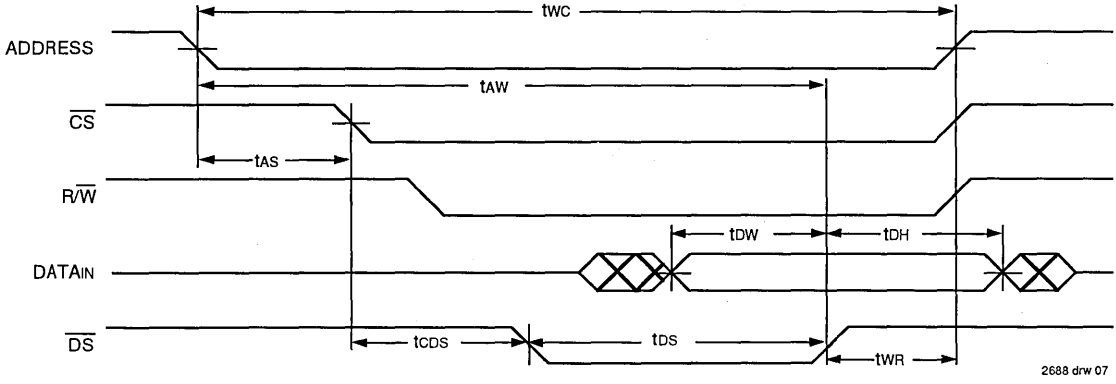
2688 drw 05

TIMING WAVEFORM OF WRITE CYCLE (CS CONTROLLED)



2688 drw 06

TIMING WAVEFORM OF WRITE CYCLE (DS CONTROLLED)

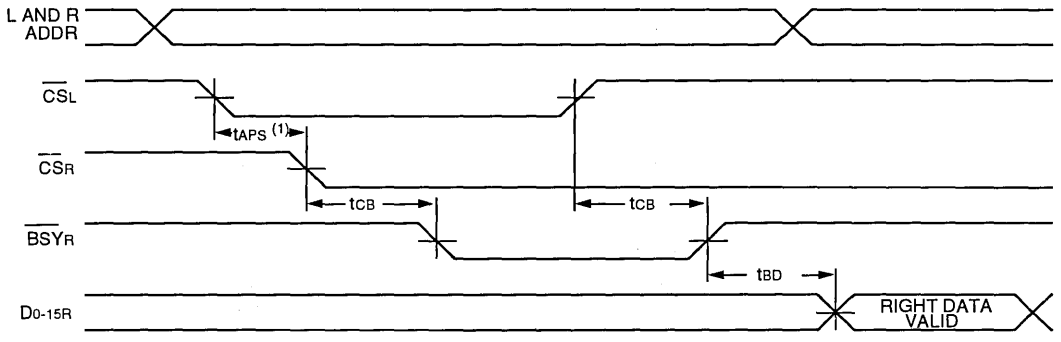


2688 drw 07

NOTES:
1. R/W = VIH.
2. Transition is measured +200mV from steady state with 5pF load (including scope and jig. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF CONTENTION READ, ($\overline{CS}$ ARBITRATION)

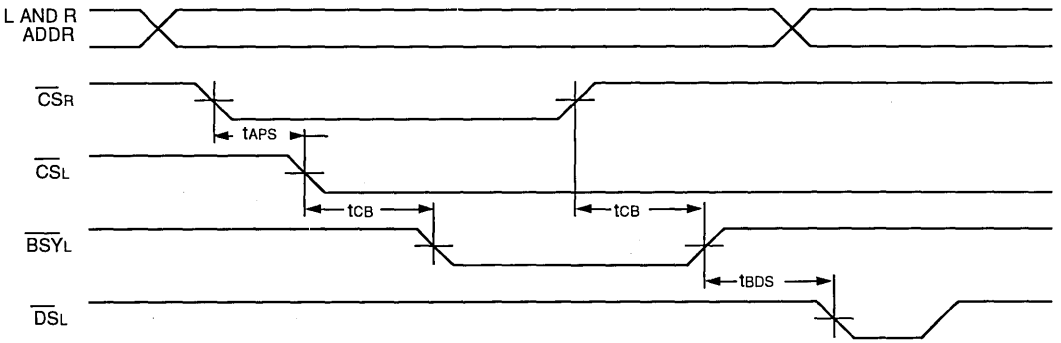
$\overline{CS_L}$ VALID FIRST:



2688 drw 08

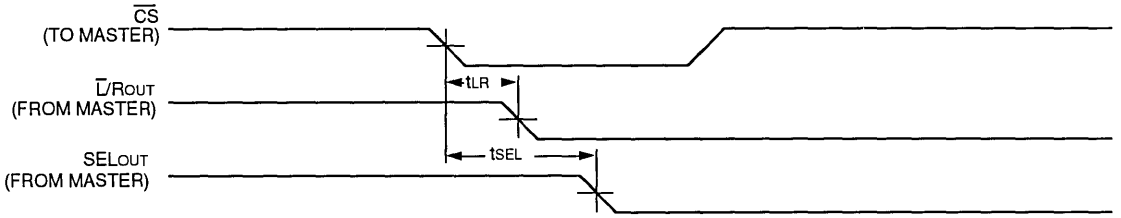
TIMING WAVEFORM OF CONTENTION WRITE, ($\overline{CS}$ ARBITRATION)

$\overline{CS_R}$ VALID FIRST:



2688 drw 09

TIMING WAVEFORM OF SLAVE(2)

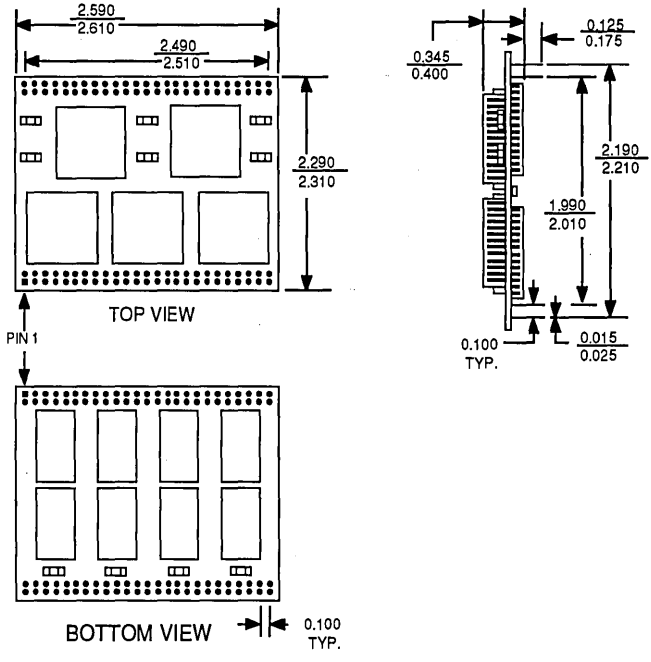


2688 drw 10

NOTES:
1. t_{APS} is only necessary to guarantee left side access. Within this set-up time, one side or the other will gain access, but neither will have priority.
2. $\overline{CS}$ inputs are ignored when configured as a Slave, allowing the Master to control port selection with L/R_OUT and SEL_OUT signals.

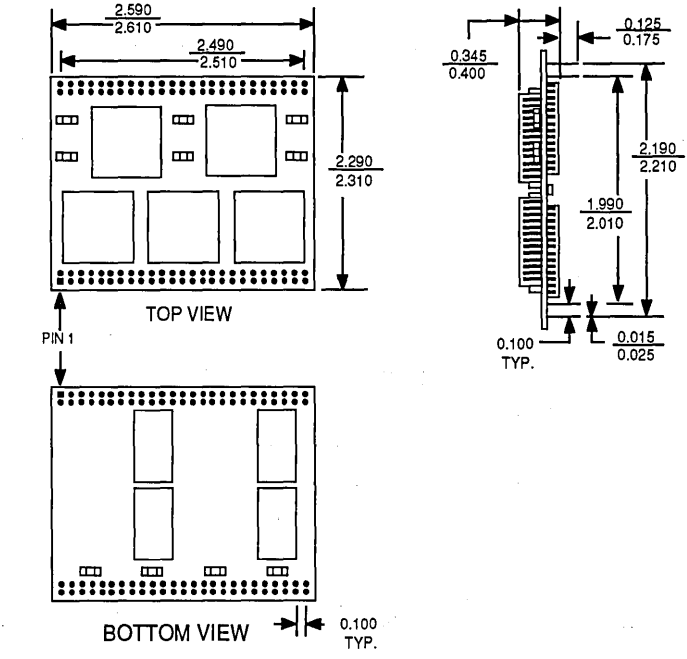
PACKAGE DIMENSIONS

7MB6036



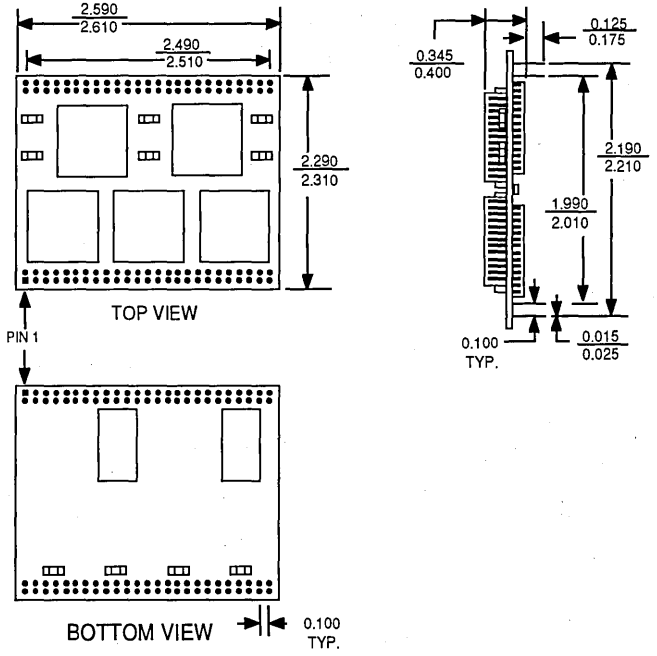
2688 drw 11

7MB6046



2688 drw 12

7MB6056



2688 drw 13

7

Integrated Device Technology, Inc.

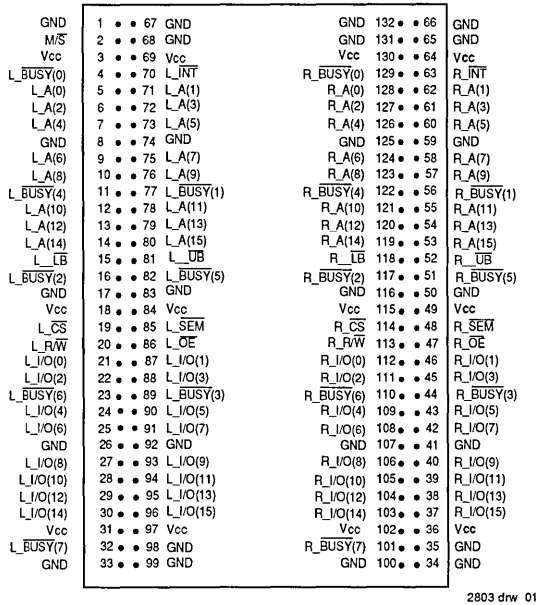
64K x 16
32K x 16
CMOS DUAL-PORT
STATIC RAM MODULE

PRELIMINARY
IDT7MB1006
IDT7MB1008

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times: 25ns (max.)
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 32 bits or more using the master/slave function
- Separate upper and lower byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication and $\overline{BUSY}$ flag for maintaining data coherency
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted PQFP (plastic quad flatpack) components on a 132-pin FR-4 QIP (Quad In-line Package)
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION (1)



2803 drw 01

QIP
TOP VIEW

NOTES:
1. For the IDT7MB1008 (32K x 16) version, Pins 53 & 80 must be connected to GND for proper operation of the module.

DESCRIPTION:

The IDT7MB1006/1008 is a 64K x 16/32K x 16 high-speed CMOS dual-port static RAM module constructed on a multi-layer epoxy laminate (FR-4) substrate using eight IDT7025 (8K x 16) dual-port RAMs or depopulated using only four IDT7025 dual-port RAMs. The IDT7MB1006/1008 module is designed to be used as stand-alone dual-port RAM or as a combination master/slave dual-port RAM for 32-bit or wide word systems. Using the IDT master/slave approach in such system applications results in full-speed, error-free operation without the need for additional discrete logic.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ and $\overline{INT}$. $\overline{BUSY}$ flags are provided to maintain data coherency between ports.

The IDT7MB1006/1008 module is packaged on a FR-4 132-pin QIP (Quad In-line Package) with dimensions of only 3.51" x 1.61" x 0.31". Maximum access times as fast as 25ns are available over the commercial temperature range.

All inputs and outputs of the IDT7MB1006/1008 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

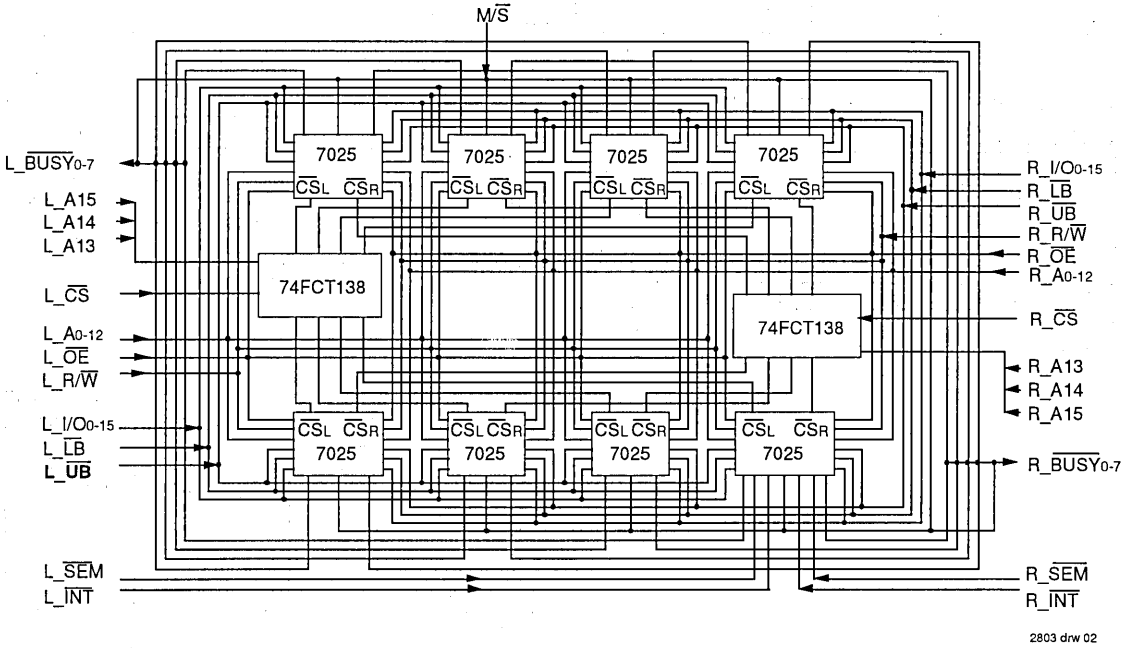
PIN NAMES

Left Port	Right Port	Description
L_A (0–15)	R_A (0–15)	Address Inputs
L_I/O (0–15)	R_I/O (0–15)	Data Inputs/Outputs
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{CS}$	R_$\overline{CS}$	Chip Select
L_$\overline{OE}$	R_$\overline{OE}$	Output Enable
L_$\overline{BUSY}$ (0–7)	R_$\overline{BUSY}$ (0–7)	Busy Flags
L_$\overline{INT}$	R_$\overline{INT}$	Interrupt Flag
L_$\overline{SEM}$	R_$\overline{SEM}$	Semaphore Control
M/$\overline{S}$		Master/Slave Control
Vcc		Power
GND		Ground

2803 tbl 01

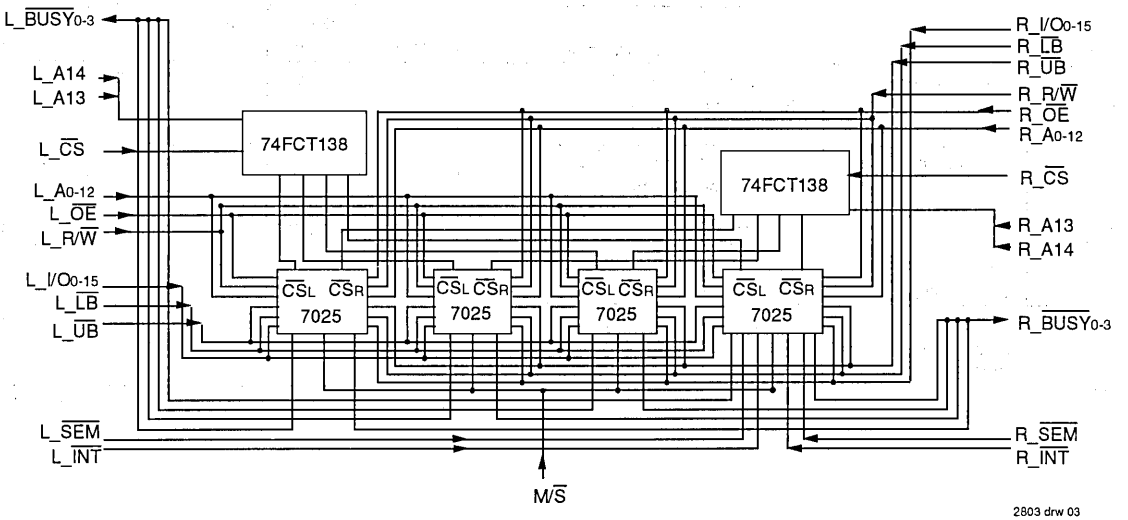
FUNCTIONAL BLOCK DIAGRAM

7MB1006



2803 drw 02

7MB1008



2803 drw 03

7

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	0V	5.0V± 10%

2803 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

NOTE: 2803 tbl 03

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2803 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	7MB1006/8 Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$, $\overline{BUSY}$, $\overline{SEM}$, $\overline{INT}$)	V_{IN} = 0V	15/15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100/60	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100/ 60	pF

NOTE: 2803 tbl 05

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \le V_{IL}$, $\overline{SEM} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	960	—	680	mA
I_{CC1}	Dynamic Operating Current (One Port Active)	V_{CC} = Max., L_$\overline{CS}$ or R_$\overline{CS} \ge V_{IH}$, Outputs Open, f = f_{MAX}	—	760	—	480	mA
I_{SB1}	Standby Supply Current (TTL Levels)	V_{CC} = Max., L_$\overline{CS}$ and R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM} \ge V_{CC}$ - 0.2V	—	565	—	285	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS} \ge V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \ge V_{CC}$ - 0.2V	—	125	—	65	mA

2803 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

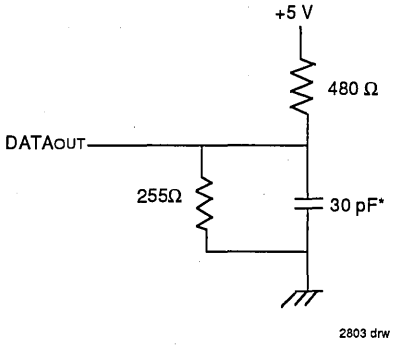
Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data,$\overline{CS}$,$\overline{BUSY}$,$\overline{SEM}$,$\overline{INT}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2803 tbl 07

AC TEST CONDITIONS

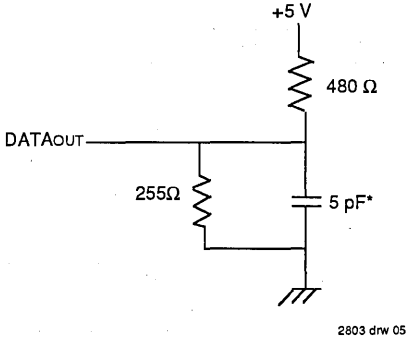
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2803 tbl 08



2803 drw 04

Figure 1. Output Load



2803 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MB1006SxxK or 7MB1008SxxK								
		-25[5]		-30[5]		-35		-40		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	ns

NOTES:

2803 tbl 09

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1} = 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB1006SxxK or 7MB1008SxxK						Unit
		-50		-65		-80		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	50	—	65	—	80	ns
t_{ACS}[2]	Chip Select Access Time	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t_{CW}[2]	Chip Select to End of Write	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	25	—	30	—	35	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns

2803 tbl 10

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1} = 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR} = 5ns, t_{DH} = 5ns, t_{OW} = 5ns.

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	-25[11] Min.	-25[11] Max.	-30[11] Min.	-30[11] Max.	-35 Min.	-35 Max.	-40 Min.	-40 Max.	Unit
$\overline{BUSY}$ Cycle - MASTER MODE[3]										
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	25	—	30	—	35	—	40	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	25	—	30	—	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	20	—	25	—	30	—	35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	20	—	25	—	30	—	30	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]										
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	0	—	ns
t_{WH}[6]	Write Hold After $\overline{BUSY}$	15	—	20	—	25	—	25	—	ns
Port-to-Port Delay Timing										
t_{WDD}[5]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns
Interrupt Timing										
t_{AS}[10]	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WR}[10]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	20	—	25	—	30	—	35	ns
t_{INR}	Interrupt Reset Time	—	20	—	25	—	30	—	35	ns

NOTES:

2803 tbl 11

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{DDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrupt, then t_{AS}=0 and t_{WR}= 5ns.
11. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	-50		-65		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Cycle - MASTER MODE(3)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	50	—	55	—	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	45	—	45	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	45	—	50	—	55	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	40	—	45	—	45	ns
t_{APS}(6)	Arbitration Priority Set-up Time	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode(4)								
t_{WB}(7)	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	ns
t_{WH}(8)	Write Hold After $\overline{BUSY}$	25	—	30	—	30	—	ns
Port-to-Port Delay Timing								
t_{WDD}(5)	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t_{DDD}(5)	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns
Interrupt Timing								
t_{AS}(10)	Address Set-up Time	5	—	5	—	5	—	ns
t_{WR}(10)	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	45	—	45	—	55	ns
t_{INR}	Interrupt Reset Time	—	45	—	45	—	55	ns

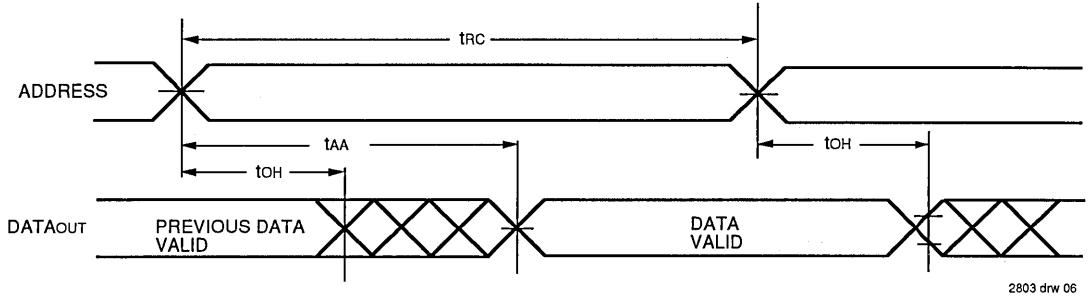
NOTES:

2803 tbl 12

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrupt, then t_{AS}=0 and t_{WR}= 5ns.

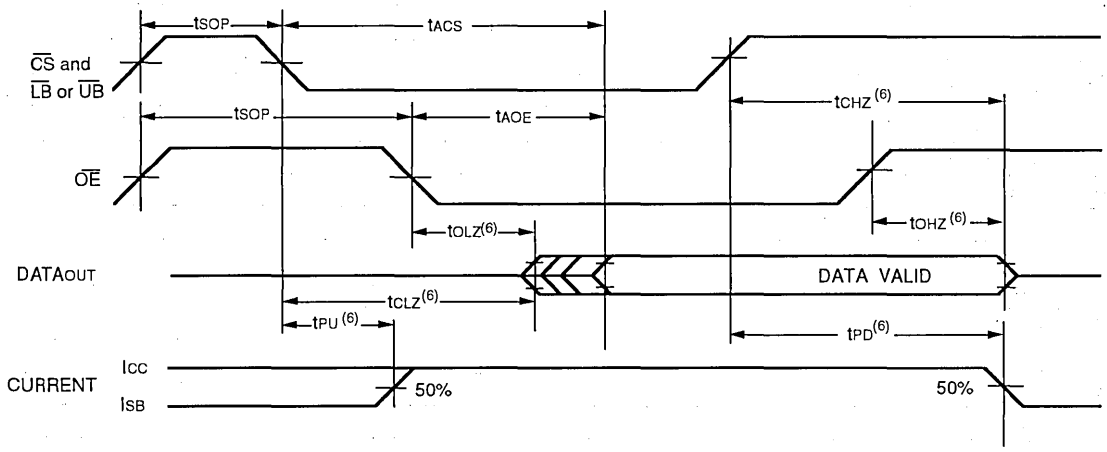
7

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



2803 drw 06

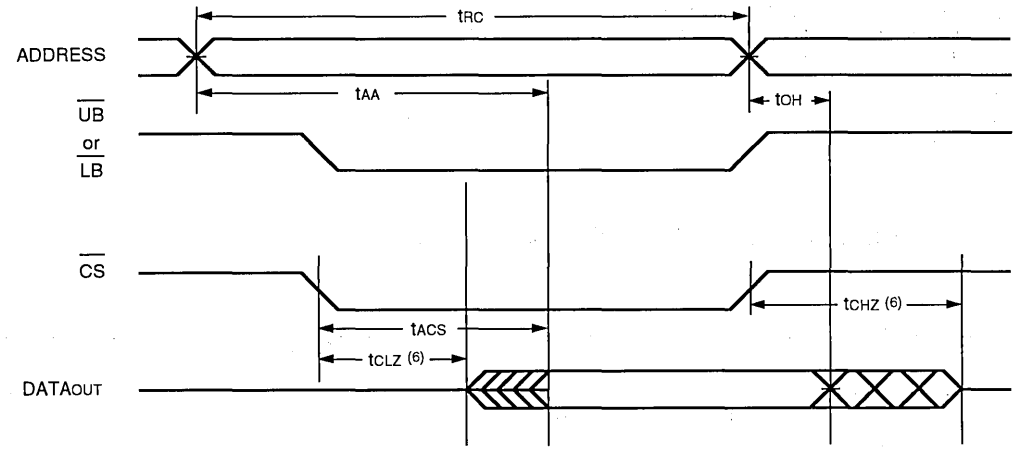
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



2803 drw 07

NOTES:
1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low. UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low, UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. This parameter is guaranteed by design but not tested.

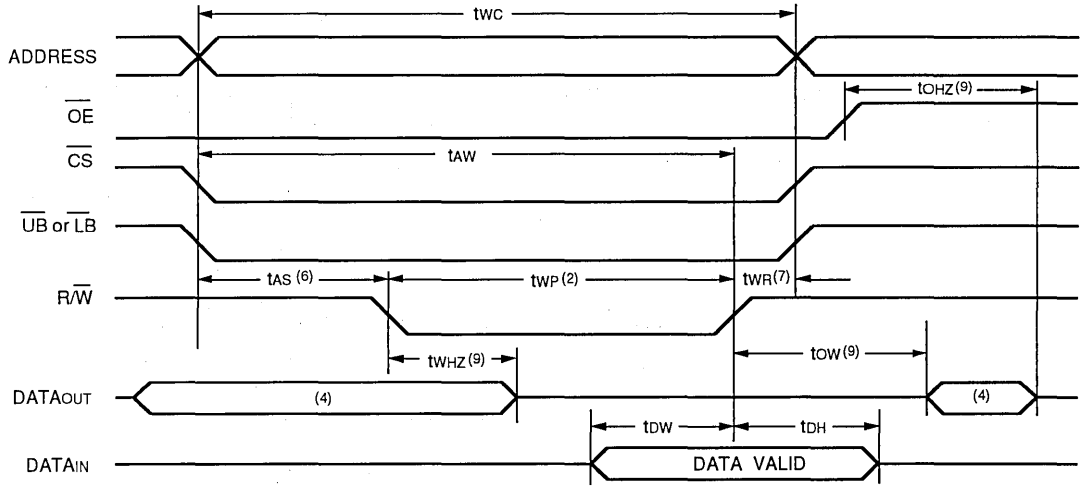
TIMING WAVEFORM OF READ CYCLE NO. 3 (UB OR LB CONTROLLED TIMING)(1,3,4,5)



2803 drw 08

NOTES:
1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low. UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. This parameter is guaranteed by design but not tested.

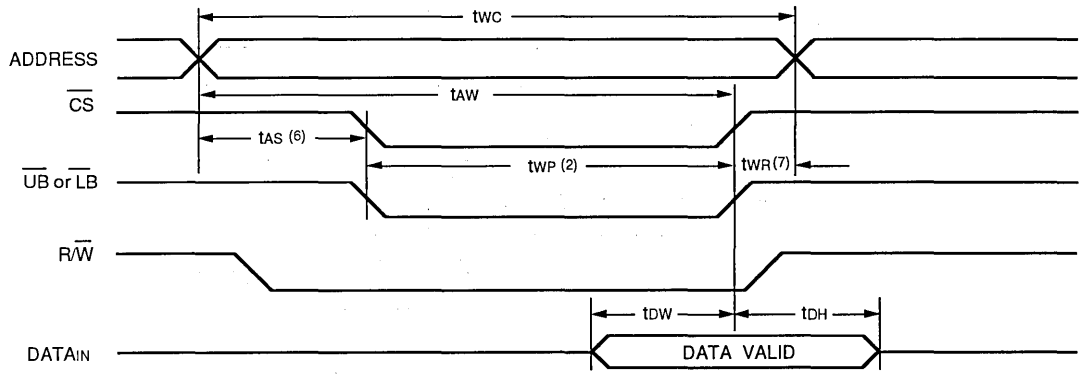
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 09

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING)(1,3,5,8)

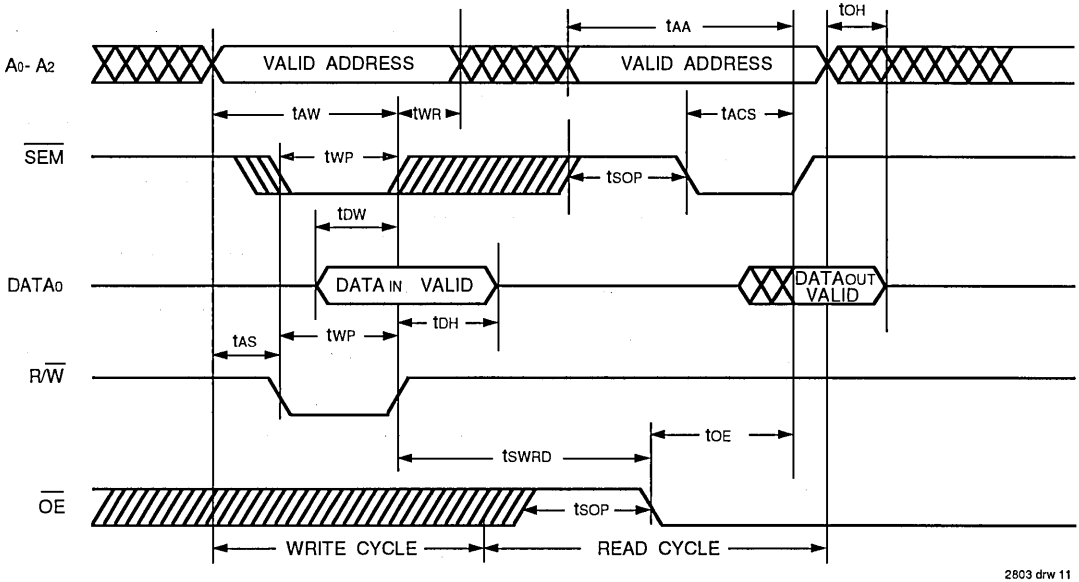


2803 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low $\overline{UB}$ or $\overline{LB}$ and a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

7

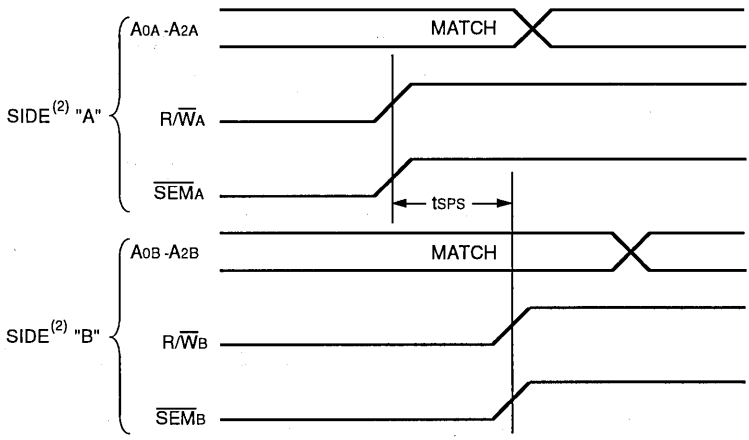
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)



2803 drw 11

NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

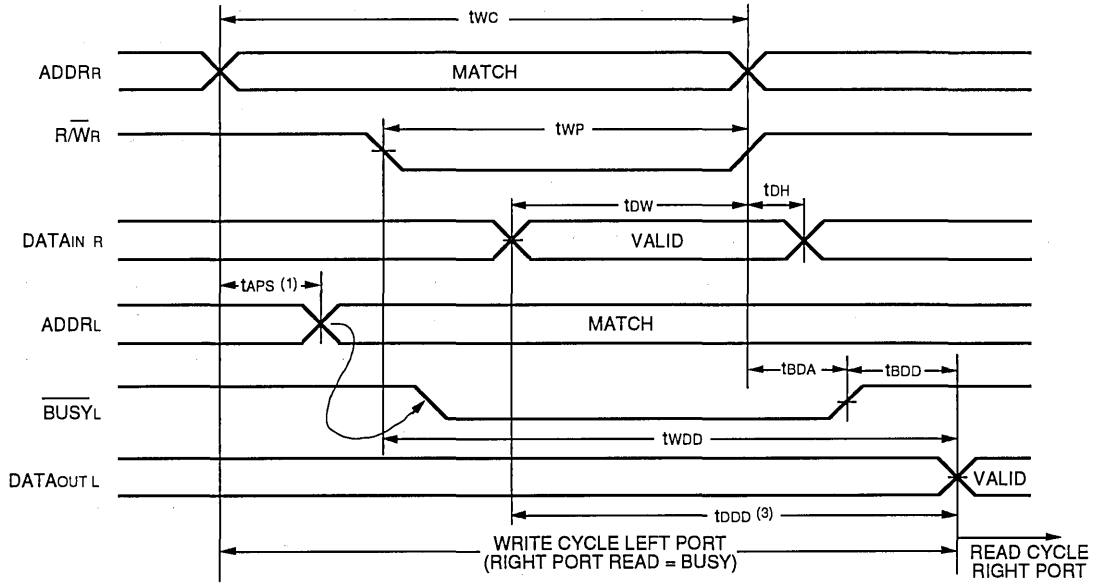
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



2803 drw 12

NOTES:
1. D_{0R} = D_{0L} = Low, $L\_\overline{CS}$ = $R\_\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going High to $R/\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

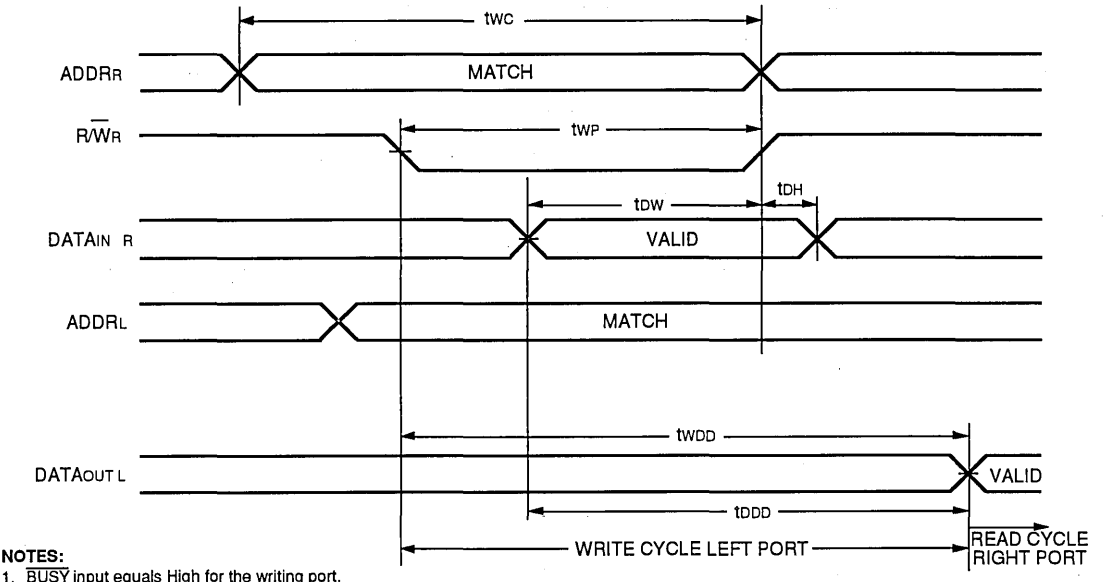
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ ($M/\overline{S} \geq V_{IH}$)(2)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. L_$\overline{CS}$ = R_$\overline{CS}$ = Low
3. $\overline{OE}$ = Low for the reading port.

2803 drw 13

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY ($M/\overline{S} \leq V_{IL}$)(1,2)

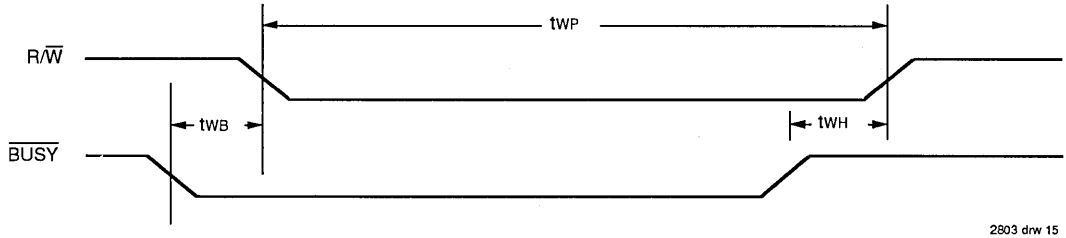


NOTES:
1. $\overline{BUSY}$ input equals High for the writing port.
2. L_$\overline{CS}$ = R_$\overline{CS}$ = Low

2803 drw 14

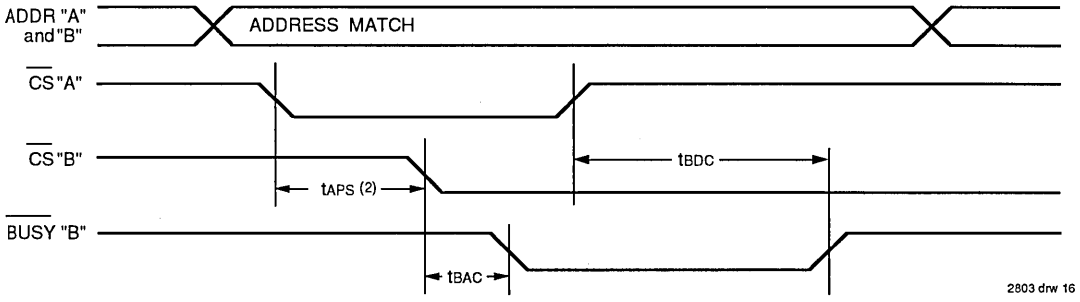
7

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (M/$\overline{S}$ ≤ VIL)



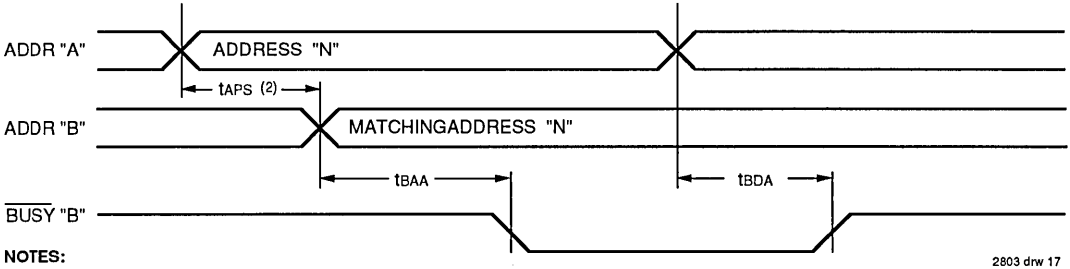
2803 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CS}$ TIMING(1)



2803 drw 16

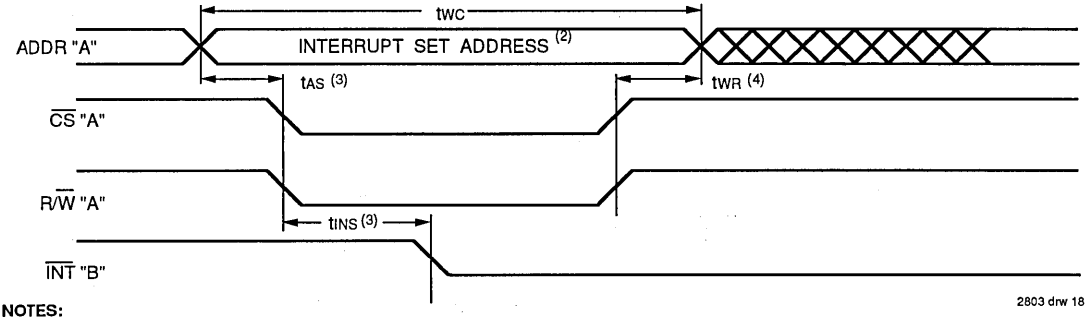
WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)



2803 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

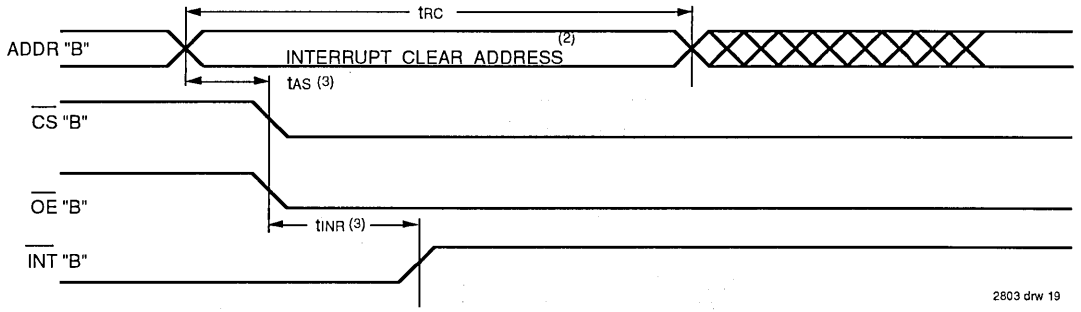
WAVEFORM OF INTERRUPT TIMING(1)



2803 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See InterruptTruth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable is de-asserted first.

WAVEFORM OF INTERRUPT TIMING[1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See InterruptTruth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable is de-asserted first.

TRUTH TABLE I: NON-CONTENTION READ/WRITE CONTROL[1, 2, 3]

Inputs[1]						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTES:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

2803 tbl 13

TRUTH TABLE II: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

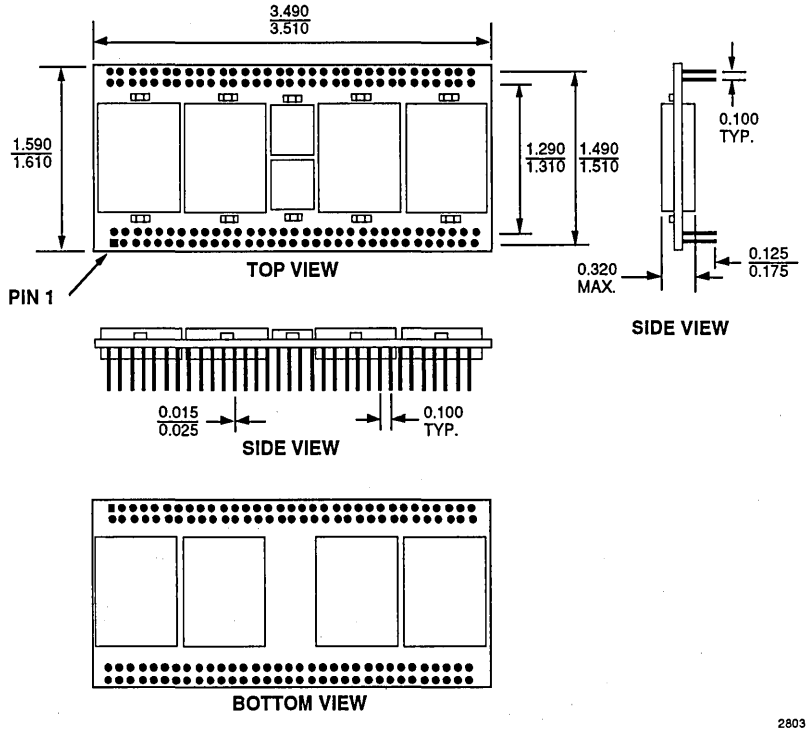
NOTES:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

2803 tbl 14

INTERRUPT/BUSY FLAGS, DEPTH/WIDTH EXPANSION, MASTER/SLAVE CONTROL, SEMPAHORES

For more details regarding Interrupt/Busy flags, depth/width expansion, master/slave control, or semaphore operations, please consult the IDT7025 datasheet.

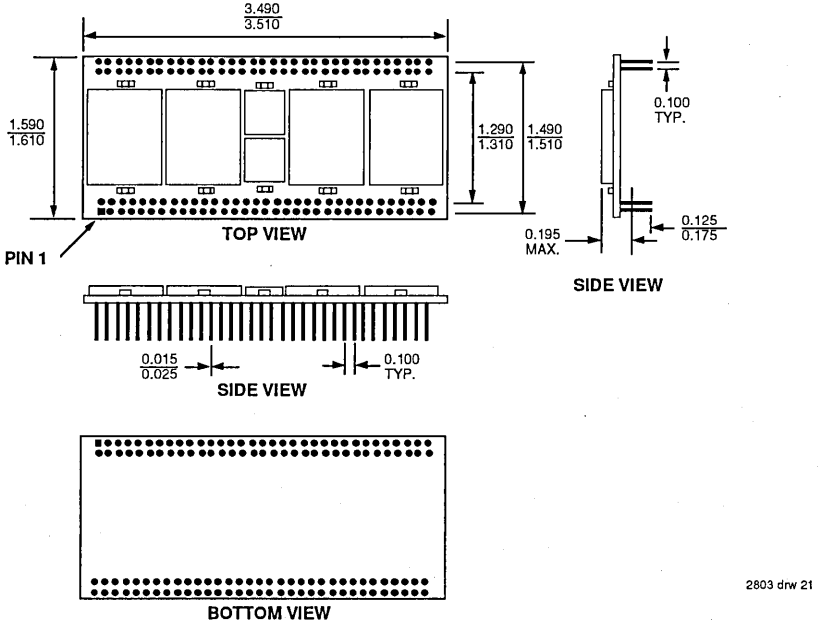
PACKAGE DIMENSIONS
7MB1006



2803 drw 20

PACKAGE DIMENSIONS

7MB1008



2803 drw 21

7

Integrated Device Technology, Inc.

8K/16K x 9 CMOS DUAL-PORT STATIC RAM MODULES

PRELIMINARY
IDT7M1004
IDT7M1005

FEATURES:

- High density 8K/16K x 9 CMOS Dual-Port Static RAM modules
- Fast access times
  —commercial: 30, 35, 45, 55, 65ns
  —military: 40, 45, 55, 65, 80, 100ns
- Fully asynchronous read/write operation from either port
- Expand data bus width to 18 bits or more using external arbitration
- Surface mounted LCC packages allow through-hole module to fit on a 60-pin sidebrazed DIP
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

The IDT7M1004/1005 are 8K/16K x 9 high speed CMOS Dual-Port static RAM modules constructed on a co-fired ceramic substrate using 8 IDT7012 (2K x 9) Dual-Port RAMs or depopulated using only 4 IDT7012 Dual-Port RAMs. The IDT7M1004/1005 modules are designed to be used for stand alone 9-bit word width systems where on-chip arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

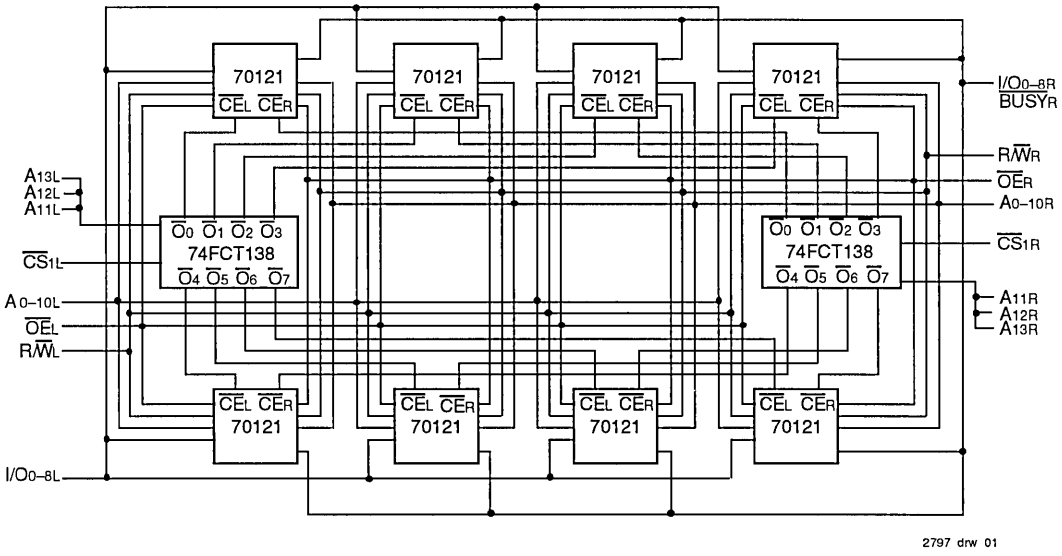
This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1004/1005 modules are packaged in a 60-pin ceramic sidebrazed DIP (Dual In-line Package). Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS

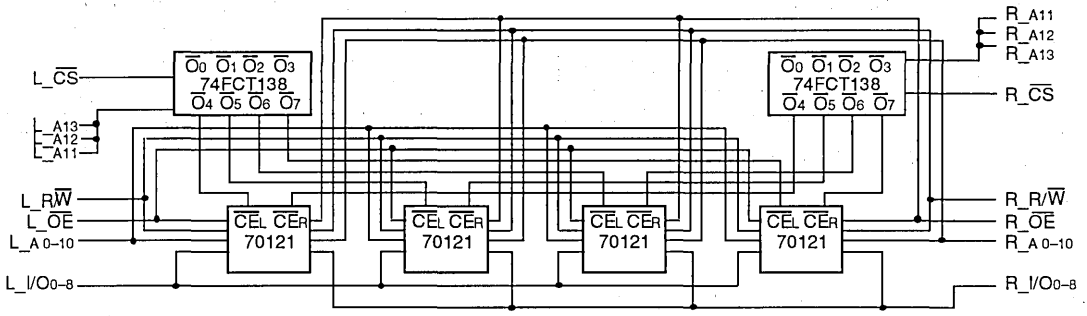
IDT7M1005 (16K x 9)



2797 drw 01

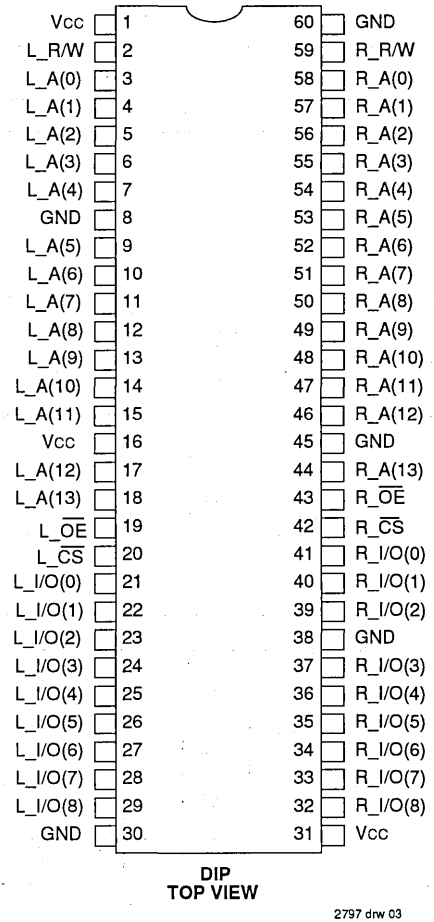
CEMOS is a trademark of Integrated Device Technology, Inc.

IDT7M1004 (8K x 9)



2797 drw 02

PIN CONFIGURATION



DIP
TOP VIEW

2797 drw 03

PIN NAMES(1)

Left Port	Right Port	Names
L_$\overline{CS}$	R_$\overline{CS}$	Chip Selects
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{OE}$	R_$\overline{OE}$	Output Enables
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–8)	R_I/O (0–8)	Data Input/Outputs
Vcc		Power
GND		Ground

2797 tbl 01

NOTE:
1. On the IDT7M1004 option (8K x 9) L_A13 and R_A13 need to be connected to GND for proper operation of the module.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2797 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2797 tbl 03

NOTE:
1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2797 tbl 04

CAPACITANCE TABLE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M1004 Max.	IDT7M1005 Max.	Unit
C_{IN}(1)	Input Capacitance (A0–10, $\overline{OE}$, R/$\overline{W}$)	V_{IN} = 0V	100	55	pF
C_{IN}(2)	Input Capacitance (Data)	V_{IN} = 0V	100	55	pF
C_{IN}(3)	Input Capacitance (A11–13, $\overline{CS}$)	V_{IN} = 0V	15	15	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100	55	pF

2797 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1004		IDT7M1005		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	—	80	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	40	—	80	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2797 tbl 06

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, Outputs Open, f = f_{MAX}	—	500	870	—	560	860	mA
I_{CC1}	Standby Supply Current (One Port Inactive)	V_{CC} = Max., $\overline{CS}$_L or $\overline{CS}$_R $\geq V_{IH}$ Outputs Open, f = f_{MAX}	—	370	650	—	430	750	mA
I_{SB1}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., $\overline{CS}$_L and $\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	280	560	—	280	560	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}$_L and $\overline{CS}$_R $\geq V_{CC}$ –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V, f=0	—	60	120	—	120	240	mA

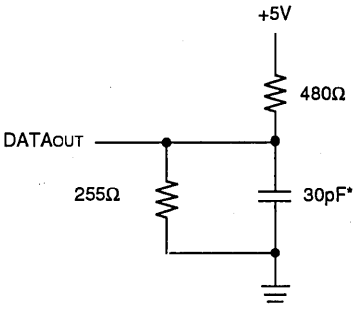
2797 tbl 07

NOTES:
1. IDT7M1004 (8K x 9) version only.
2. IDT7M1005 (16K x 9) version only.

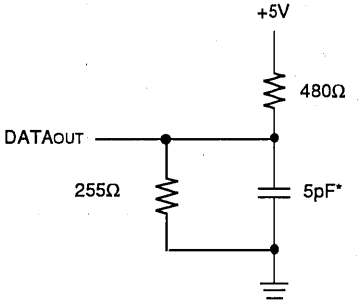
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2797 tbl 08



2797 drw 04



2797 drw 05

*Including scope and jig.

Figure 1. Output Load

Figure 2. Output Load (For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

7

AC ELECTRICAL CHARACTERISTICS

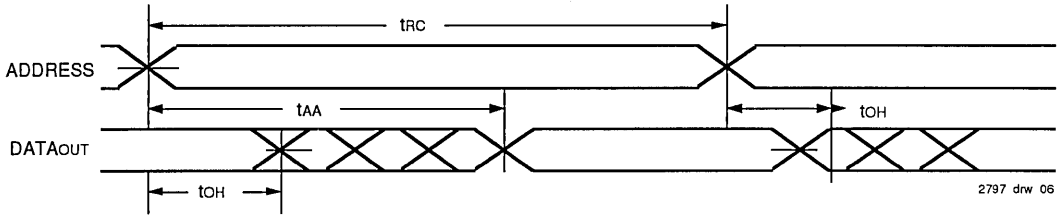
(V_{CC} = 5V ± 10%, T_A = −55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	-30[9]		-35[9]		-40		-45		-55		-65		-80[10]		-100[10]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																		
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{ACS}[2]	Chip Select Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{OE}	Output Enable Access Time	—	15	—	20	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle																		
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}[2]	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	40	—	50	—	55	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	25	—	25	—	30	—	40	—	45	—	50	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

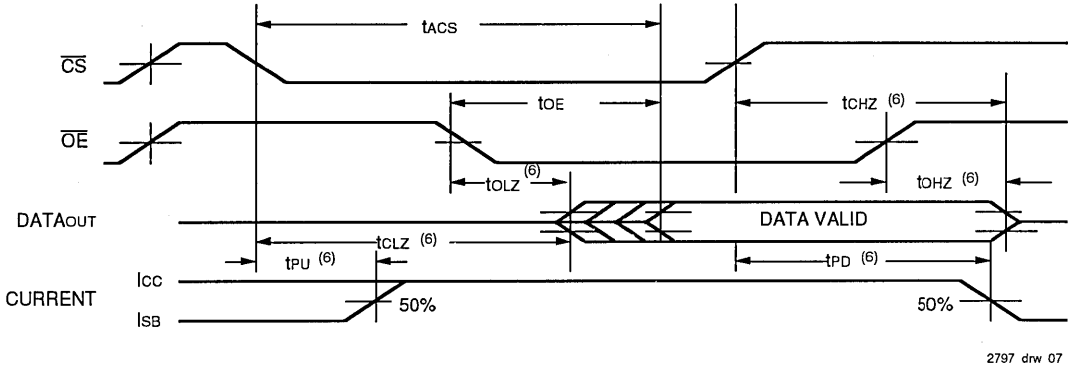
2797 tbl 09

NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM array, $\overline{CS} \leq V_{IL}$.
3. Master mode is not available on this module.
4. The module is always in the Slave Mode.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. This speed is currently available in commercial versions only.
10. This speed is currently available in military versions only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



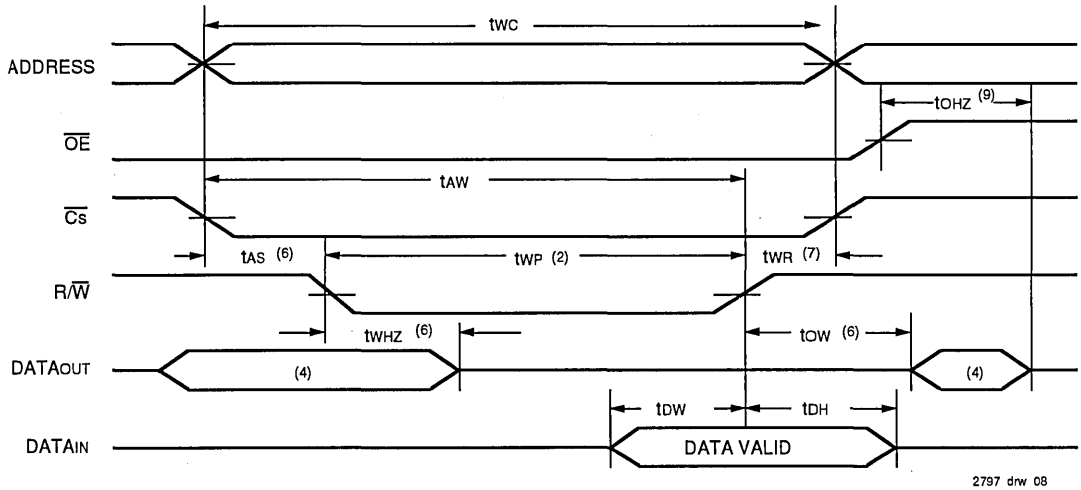
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



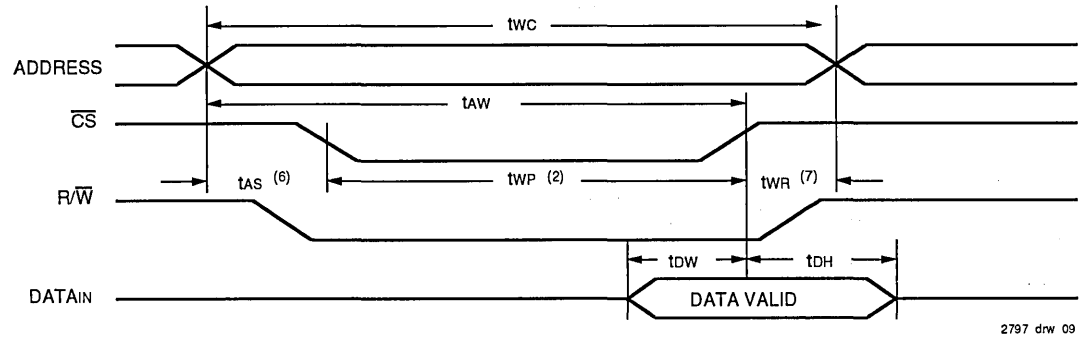
NOTES:
1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS}$ = L. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = L
5. To access RAM, $\overline{CS}$ = L. To access semaphore, $\overline{CS}$ = H.
6. This parameter is guaranteed by design but not tested.

7

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING) (1, 3, 5, 8)



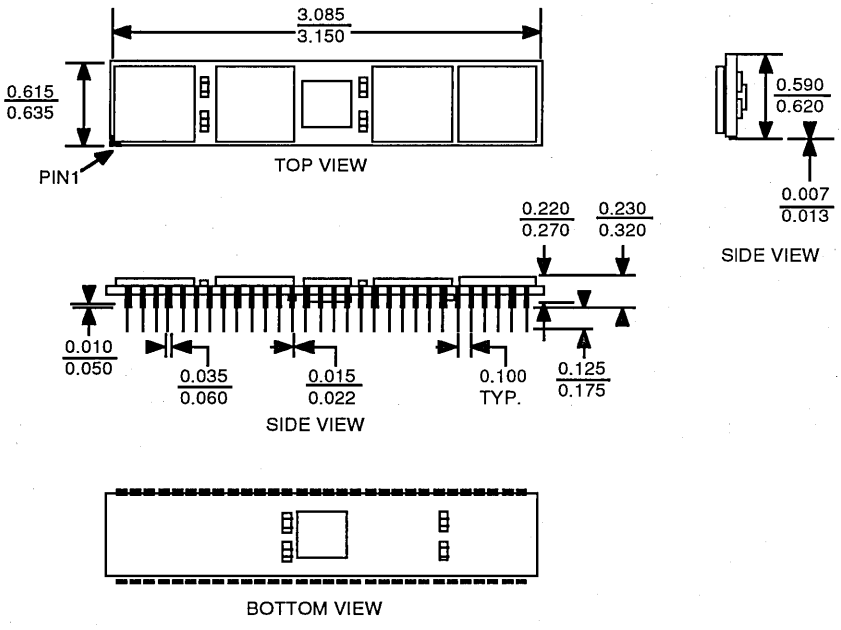
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 3, 5, 8)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

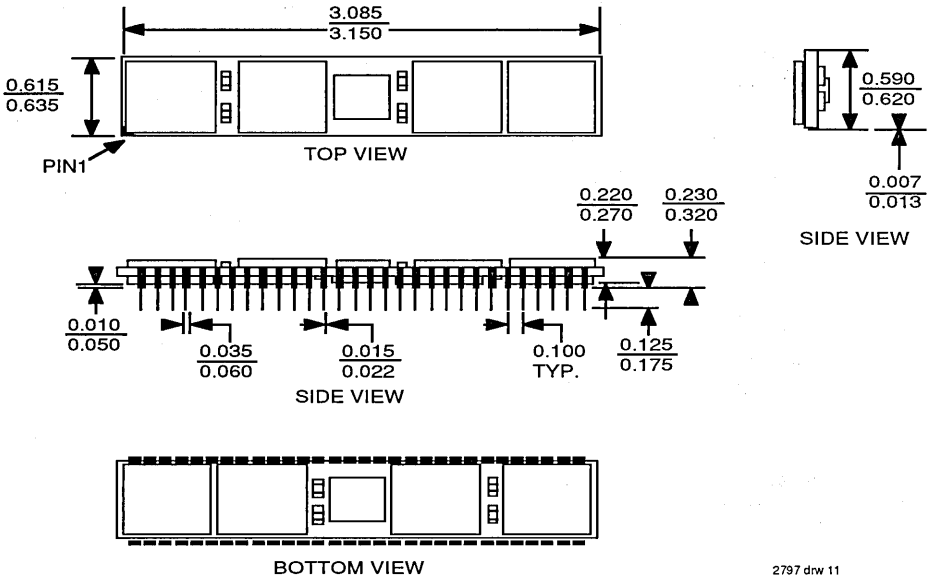
PACKAGE DIMENSIONS

7M1004



2797 drw 10

7M1005



2797 drw 11

7

Integrated Device Technology, Inc.

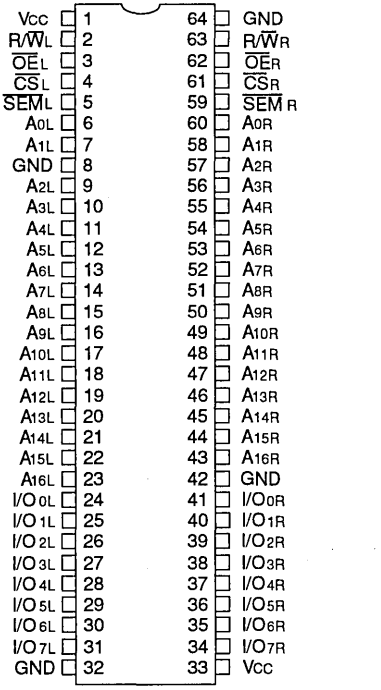
128K x 8
64K x 8
CMOS DUAL-PORT
STATIC RAM MODULE

PRELIMINARY
IDT7M1001
IDT7M1003

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times:
  - — commercial - 25, 30, 35, 40, 50, 65ns
  - — military - 35, 40, 50, 65, 80ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted LCC (leadless chip carriers) components on a 64-pin sidebraze DIP (Dual In-line Package)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION[1]



DIP
TOP VIEW

2804 drw 01

NOTE:
1. For the IDT7M1003 (64K x 8) version, Pins 23 & 43 must be connected to GND for proper operation of the module.

DESCRIPTION:

The IDT7M1001/IDT7M1003 is a 128K x 8 /64K x 8 high-speed CMOS dual-port static RAM module constructed on a multilayer ceramic substrate using eight IDT7006 (16K x 8) dual-port RAMs and two IDT FCT138 decoders or depopulated using only four IDT7006s and two decoders.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7M1001/1003 module is designed to be used as stand-alone dual-port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M1001/1003 module is packaged on a multilayer co-fired ceramic 64-pin DIP (Dual In-line Package) with dimensions of only 3.2" x 0.62" x 0.38". Maximum access times as fast as 25ns over the commercial temperature range and 35ns over the military temperature range are available.

All inputs and outputs of the IDT7M1001/1003 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

All IDT military module semiconductor components are manufacured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

Left Port	Right Port	Description
A (0–16)L	A (0–16)R	Address Inputs
I/O (0–7)L	I/O (0–7)R	Data Inputs/Outputs
R/$\overline{W}$L	R/$\overline{W}$R	Read/Write Enables
$\overline{CS}$L	$\overline{CS}$R	Chip Select
$\overline{OE}$L	$\overline{OE}$R	Output Enable
$\overline{SEM}$L	$\overline{SEM}$R	Semaphore Control
Vcc		Power
GND		Ground

2804 tbl 01

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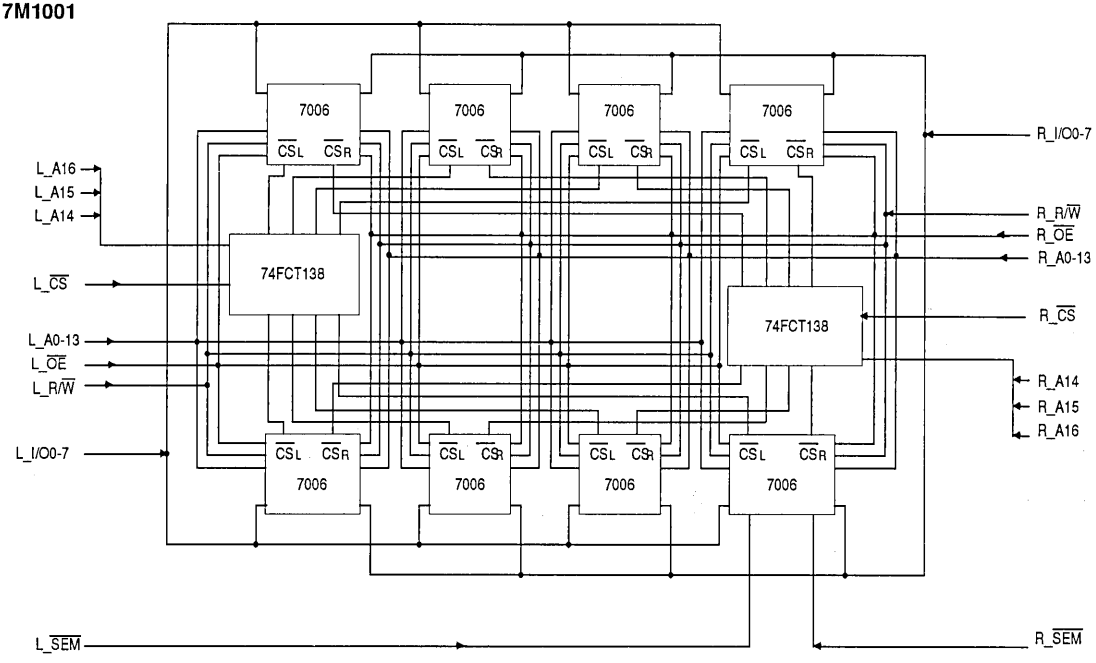
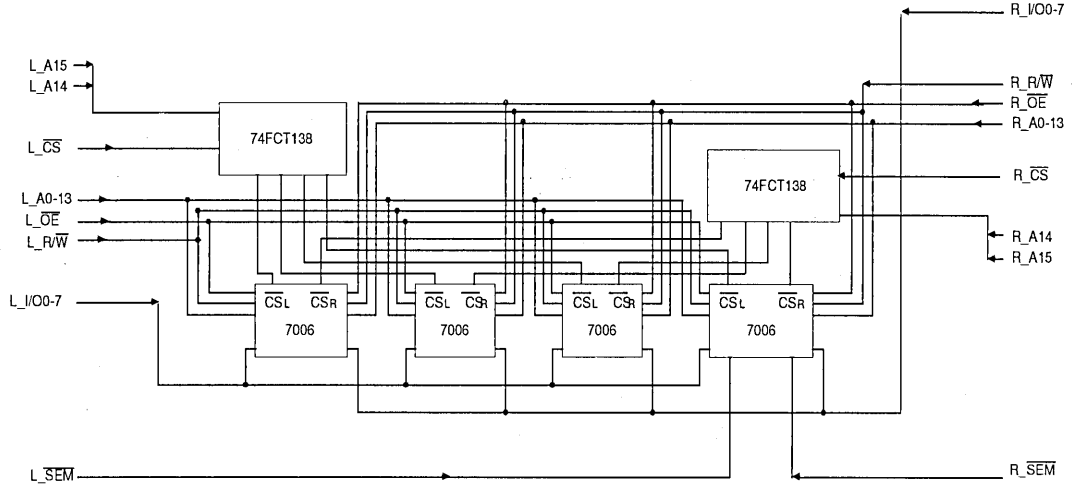
FUNCTIONAL BLOCK DIAGRAM

7M1001



2804 drw 02

7M1003



2804 drw 03

7

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2804 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100	pF

2804 tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2804 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

2804 tbl 05

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS} \le V_{IL}$, $\overline{SEM} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	940	660	—	1130	790	mA
I_{CC1}	Standby Supply Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	750	470	—	905	565	mA
I_{SB1}	Standby Supply Current (TTL Levels)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc –0.2V	—	565	285	—	685	345	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ Vcc –0.2V V_{IN} > Vcc 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc –0.2V	—	125	65	—	245	125	mA

2804 tbl 06

NOTES:
1. IDT7M1001 (128K x 8) version only.
2. IDT7M1003 (64K x 8) version only.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

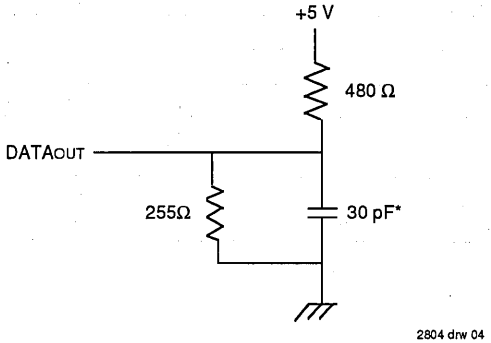
Symbol	Parameter	Test Conditions	IDT7M1001 Min.	IDT7M1001 Max.	IDT7M1003 Min.	IDT7M1003 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	Vcc = Max. VIN = GND to Vcc	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	Vcc = Max. VIN = GND to Vcc	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	Vcc = Max. $\overline{CS}$ ≥ VIH, VOUT = GND to Vcc	—	80	—	40	µA
VOL	Output Low Voltage	Vcc = Min. IOL = 4mA	—	0.4	—	0.4	V
VOH	Output High Voltage	Vcc = Min. IOH = -4mA	2.4	—	2.4	—	V

2804 tbl 07

AC TEST CONDITIONS

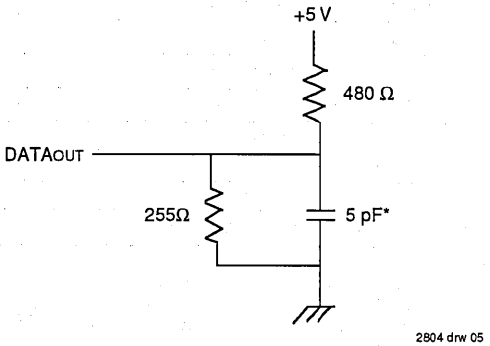
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2804 tbl 08



2804 drw 04

Figure 1. Output Load



2804 drw 05

Figure 2. Output Load
(for tCLZ, tCHZ, tOLZ, tOHZ, tWHZ, tOW)

*Including scope and jig.

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-25[5]		-30[5]		-35[5]		-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	ns
Port-to-Port Delay Timing										
t_{WDD}[6]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}[6]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns

2804 tbl 09

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-50		-65		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	50	—	65	—	80	ns
t_{ACS}[2]	Chip Select Access Time	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t_{CW}[2]	Chip Select to End of Write	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	25	—	30	—	35	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns
Port-to-Port Delay Timing								
t_{WDD}[5]	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns

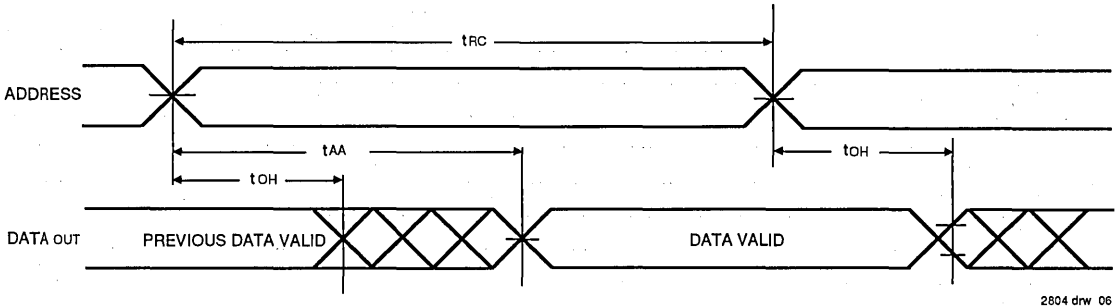
2804 tbl 10

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.

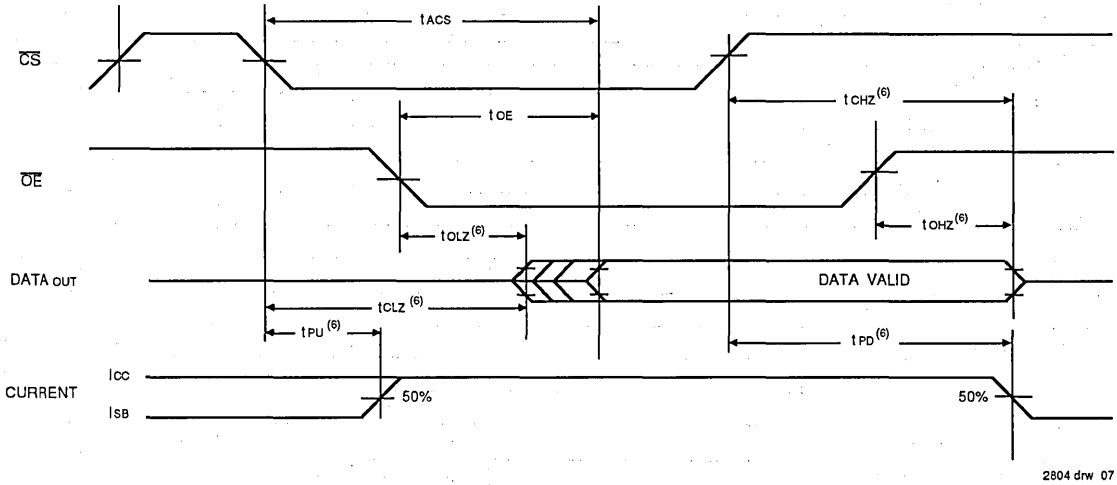
7

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



2804 drw 06

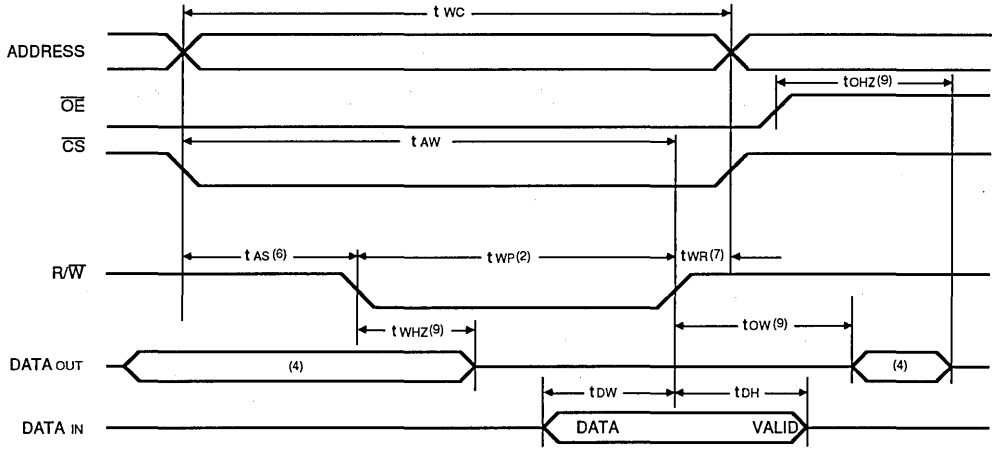
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



2804 drw 07

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. This parameter is guaranteed by design but not tested.

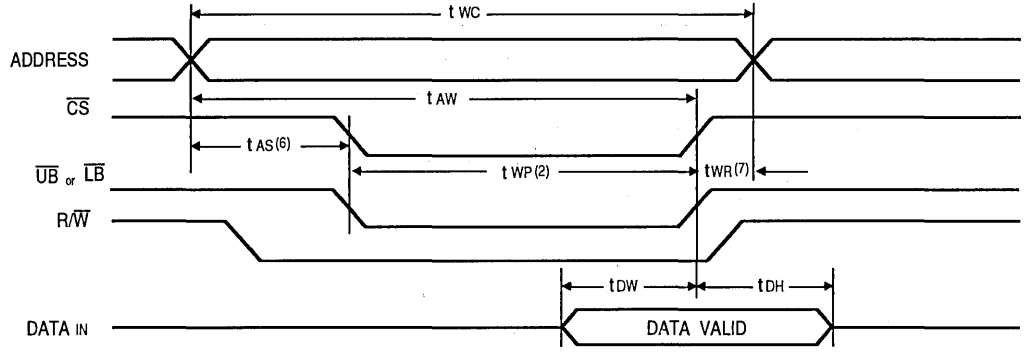
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2804 drw 08

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

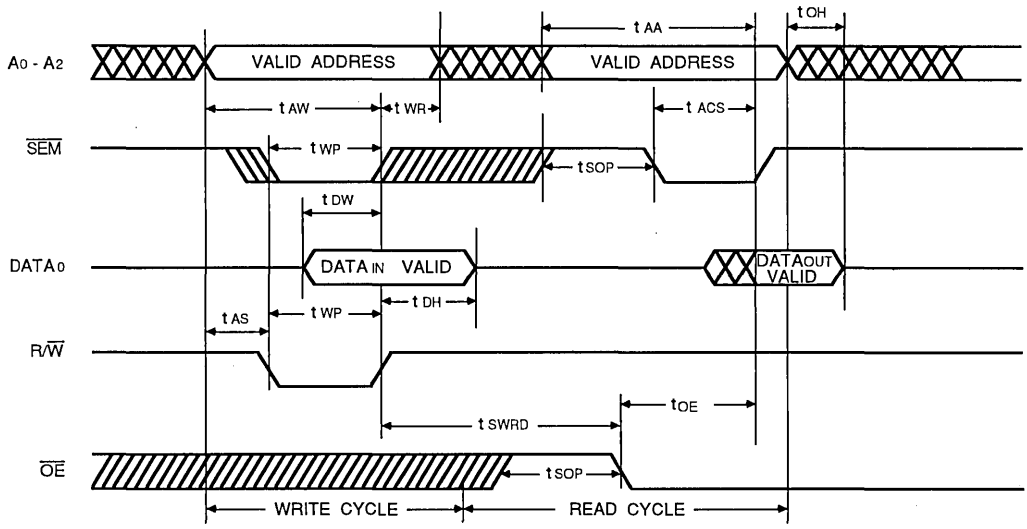
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,3,5,8)



2804 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (twp) of a Low $\overline{UB}$ or $\overline{LB}$ and a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. twr is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

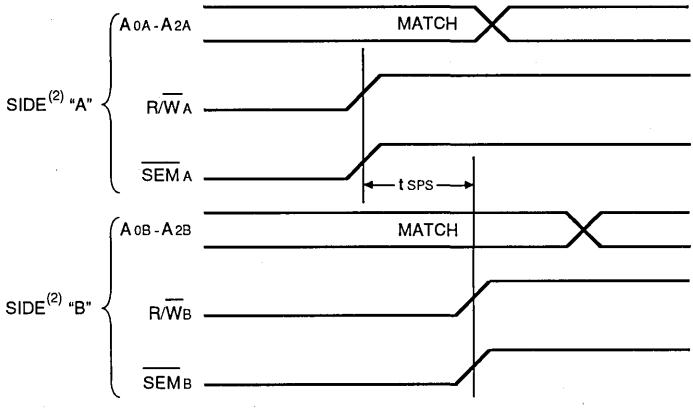
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)



2804 drw 10

NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

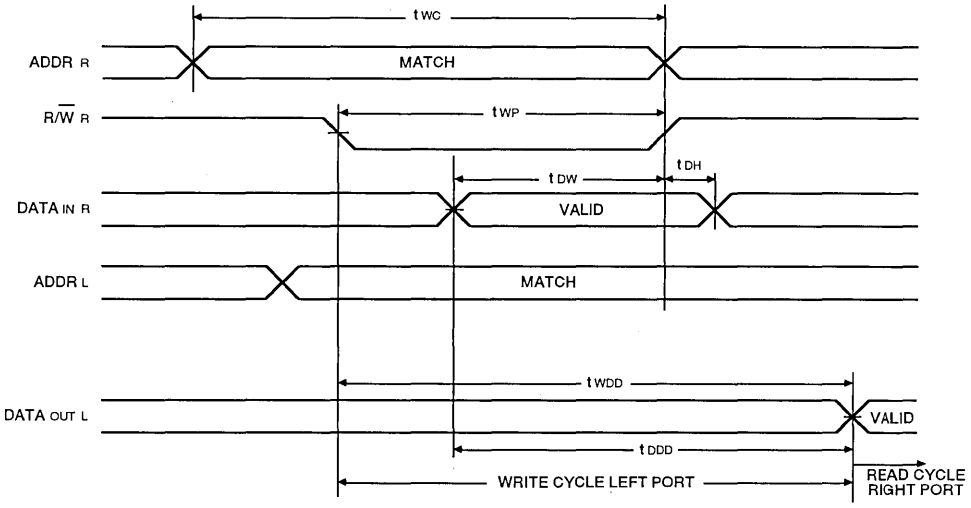
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



2804 drw 11

NOTES:
1. $D_{0R} = D_{0L}$ = Low, $L\_\overline{CS} = R\_\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going High to $R/\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1]



2804 drw 12

NOTE:
1. L_$\overline{CS}$ = R_$\overline{CS}$ = Low

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL[1]

Inputs[1]				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Both Bytes
L	H	L	H	DATAOUT	Read Both Bytes
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. AOL — A12 ≠ A0R — A12R

2804 tbl 11

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TABLE II: SEMAPHORE READ/WRITE CONTROL[1]

Inputs				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. AOL — A12 ≠ A0R — A12R

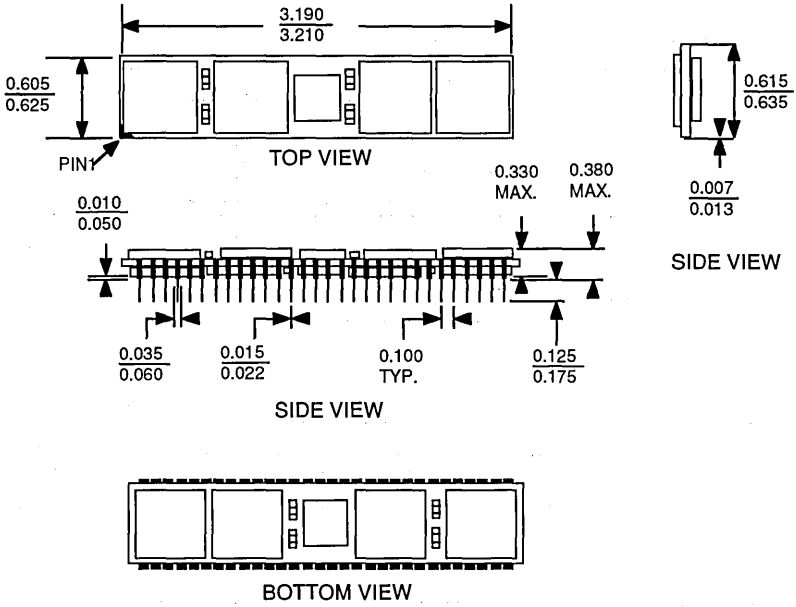
2804 tbl 12

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

PACKAGE DIMENSIONS

7M1001



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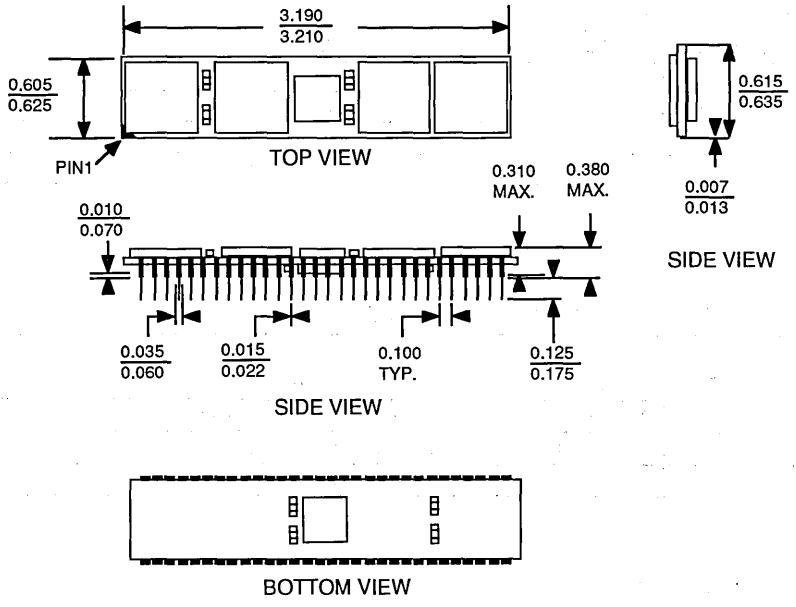
7M1003



2804 drw 14

Integrated Device Technology, Inc.

128K/64K x 8 CMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7MP1021
IDT7MP1023

FEATURES

- High density 1M/512K CMOS dual-port static RAM modules
- Fast access times: 25, 30, 35, 40, 50ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted plastic components on a 64-lead SIMM (Single In-line Memory Module)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION

		1	VCC
R_A(0)	2	3	L_A(0)
R_A(1)	4	5	L_A(1)
R_A(2)	6	7	L_A(2)
R_A(3)	8	9	L_A(3)
R_A(4)	10	11	L_A(4)
GND	12	13	L_A(5)
R_A(5)	14	15	L_A(6)
R_A(6)	16	17	L_A(7)
R_A(7)	18	19	L_A(8)
R_A(8)	20	21	L_A(9)
R_A(9)	22	23	L_A(10)
R_A(10)	24	25	GND
R_A(11)	26	27	L_$\overline{OE}$
R_$\overline{OE}$	28	29	L_R/$\overline{W}$
R_R/$\overline{W}$	30	31	L_$\overline{SEM}$
R_$\overline{SEM}$	32	33	L_$\overline{CS}$
R_$\overline{CS}$	34	35	L_A(11)
GND	36	37	L_A(12)
R_A(12)	38	39	L_A(13)
R_A(13)	40	41	L_A(14)
R_A(14)	42	43	L_A(15)
R_A(15)	44	45	N.C.
N.C.	46	47	L_I/O(0)
R_I/O(0)	48	49	L_I/O(1)
R_I/O(1)	50	51	GND
R_I/O(2)	52	53	L_I/O(2)
R_I/O(3)	54	55	L_I/O(3)
R_I/O(4)	56	57	L_I/O(4)
R_I/O(5)	58	59	L_I/O(5)
R_I/O(6)	60	61	L_I/O(6)
R_I/O(7)	62	63	L_I/O(7)
VCC	64		

SIMM TOP VIEW

2839 drw 01

DESCRIPTION:

The IDT7MP1021/1023 is a 128K/64K x 8 high-speed CMOS dual-port static RAM module constructed on a multi-layer FR-4 substrate using decode logic and either eight IDT7006 (16K x 8) dual-port RAMs for the 7MP1021 or four IDT7006s for the 7MP1023.

The IDT7MP1021/1023 provide two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7MP1021/1023 modules are designed to be used as stand-alone dual-port RAMs where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7MP1021/1023 modules are packaged on a 64-lead multilayer FR-4 SIMM (Single In-line Memory Module). Maximum access times as fast as 25ns over the commercial temperature range are available.

All inputs and outputs of the IDT7MP1021/1023 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
L_A (0–15)	R_A (0–15)	Address Inputs
L_I/O (0–7)	R_I/O (0–7)	Data Inputs/Outputs
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{CS}$	R_$\overline{CS}$	Chip Select
L_$\overline{OE}$	R_$\overline{OE}$	Output Enable
L_$\overline{SEM}$	R_$\overline{SEM}$	Semaphore Control
Vcc		Power
GND		Ground

2839 tbl 01

NOTE:

1. For the IDT7MP1023 (64K x 8) version, Pins 45 & 46 must be connected to GND for proper operation of the module. These pins become L_A(16) and R_A(16) respectively for the IDT7MP1021 (128K x 8) version.

7

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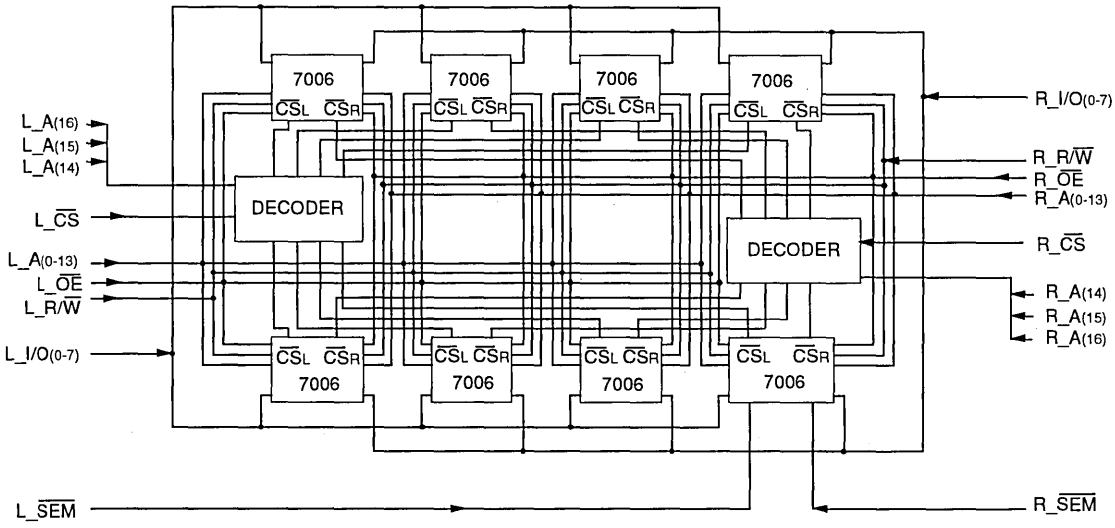
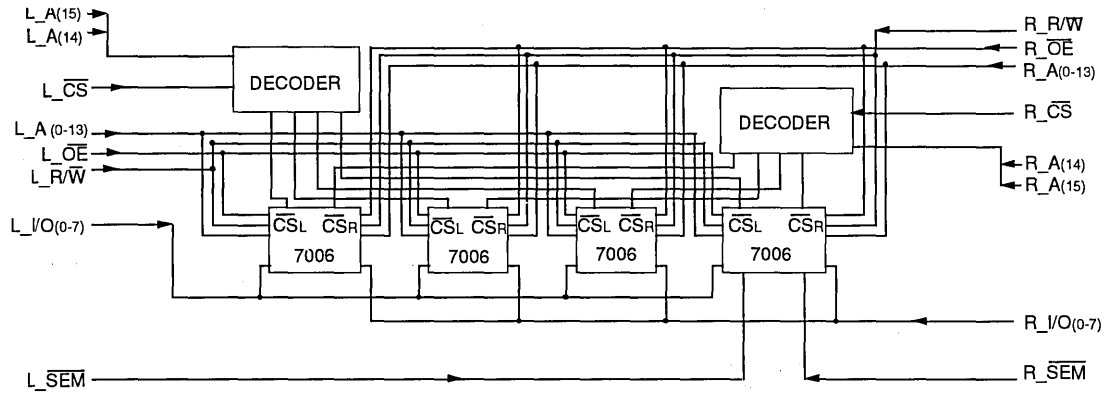
FUNCTIONAL BLOCK DIAGRAM

7MP1021



2839 drw 02

7MP1023



2839 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2839 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100	pF

NOTE:
2839 tbl 03
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2839 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

2839 tbl 05

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A =0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MP1021/1023 Min.	IDT7MP1021/1023 Max.[1]	IDT7MP1021/1023 Max.[2]	Unit
I_{CC2}	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS} \leq V_{IL}$, $\overline{SEM} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	940	660	mA
I_{CC1}	Standby Supply Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	750	470	mA
I_{SB1}	Standby Supply Current (TTL Levels)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM} \geq$ Vcc –0.2V	—	565	285	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS} \geq$ Vcc –0.2V $V_{IN} >$ Vcc 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \geq$ Vcc –0.2V	—	125	65	mA

NOTES:
2839 tbl 06
1. For IDT7MP1021 (128K x 8) version only.
2. For IDT7MP1023 (64K x 8) version only.

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

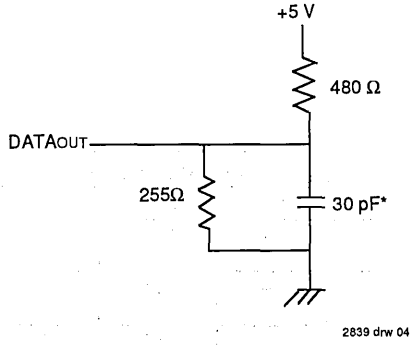
Symbol	Parameter	Test Conditions	IDT7MP1021		IDT7MP1023		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4		2.4	—	V

2839 tbl 07

AC TEST CONDITIONS

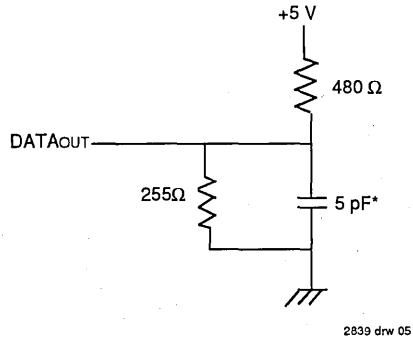
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2839 tbl 08



2839 drw 04

Figure 1. Output Load



2839 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP1023SxxM, 7MP1021SxxM										Unit
		-25[5]		-30[5]		-35[5]		-40		-50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	50	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	—	50	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	15	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	15	—	ns
Port-to-Port Delay Timing												
t_{WDD}[6]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	—	70	ns
t_{DDD}[6]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	—	55	ns

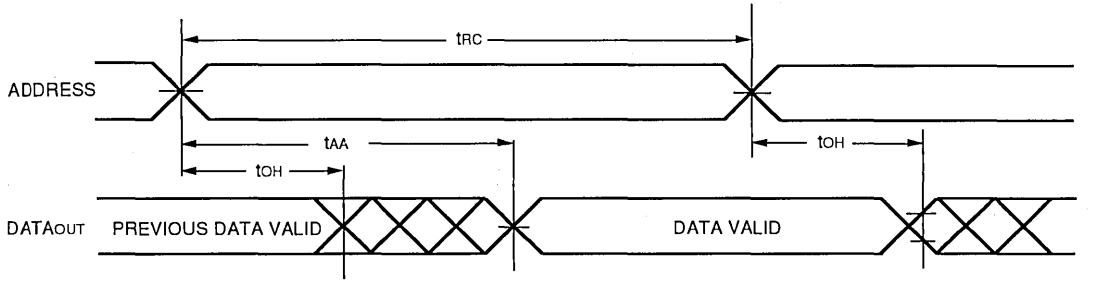
2839 tbl 09

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

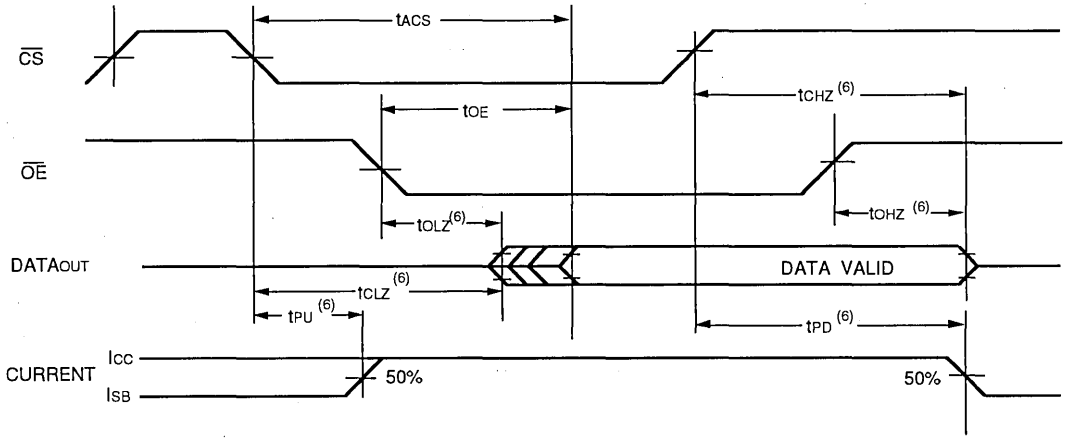
7

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



2839 drw 06

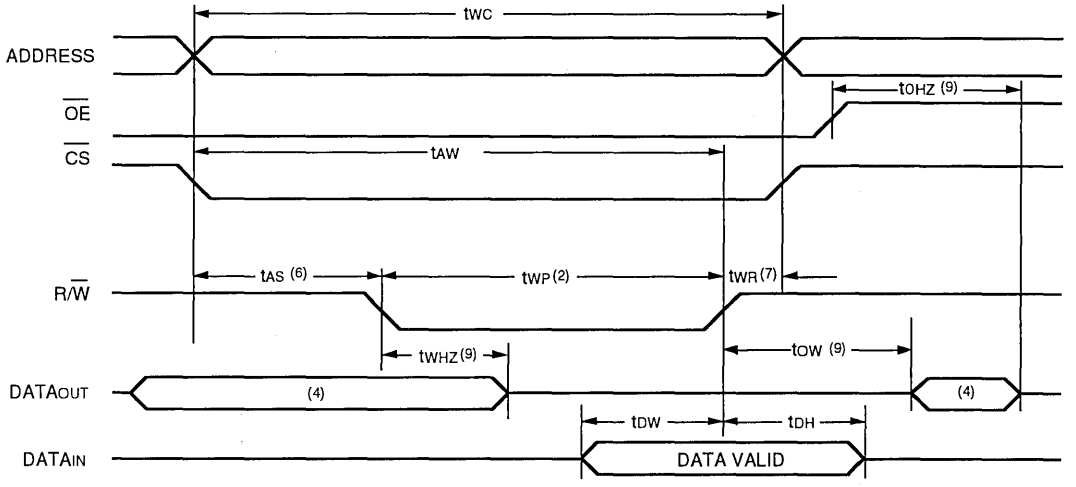
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



2839 drw 07

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. This parameter is guaranteed by design but not tested.

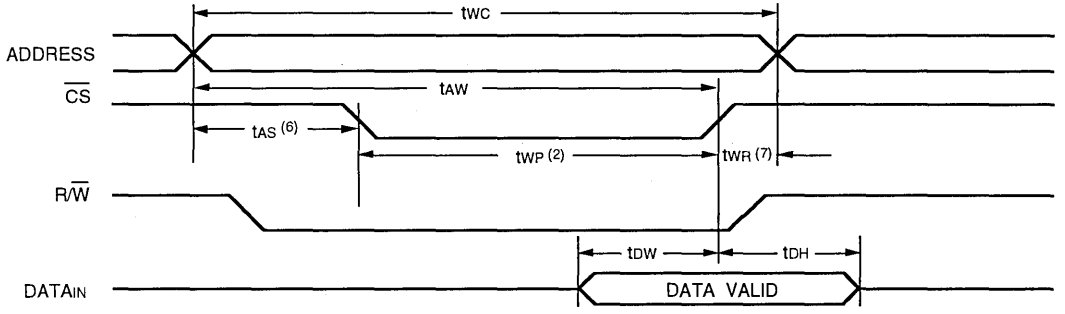
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2839 drw 08

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

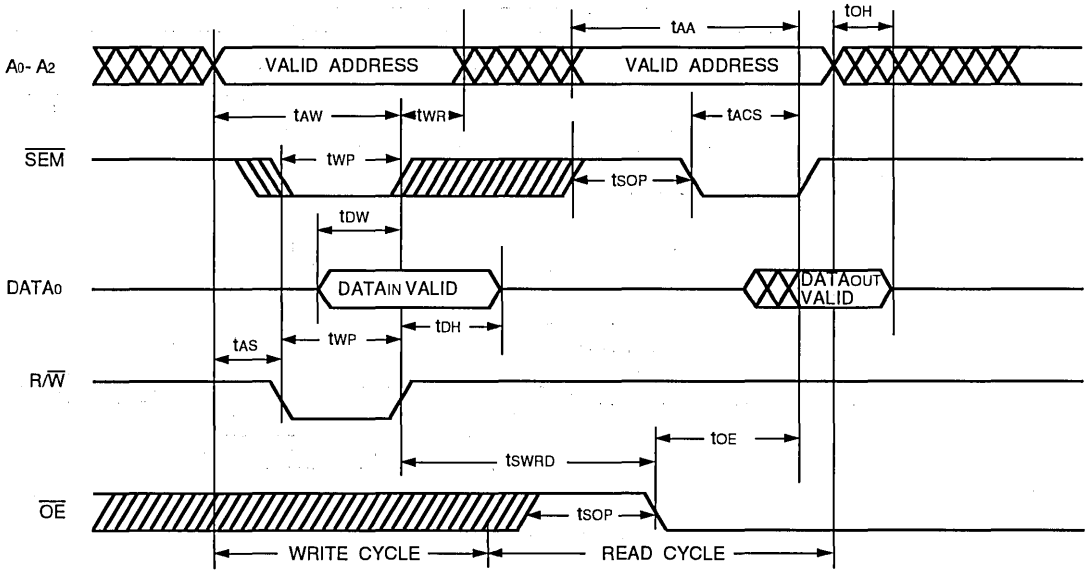
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,3,5,8)



2839 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

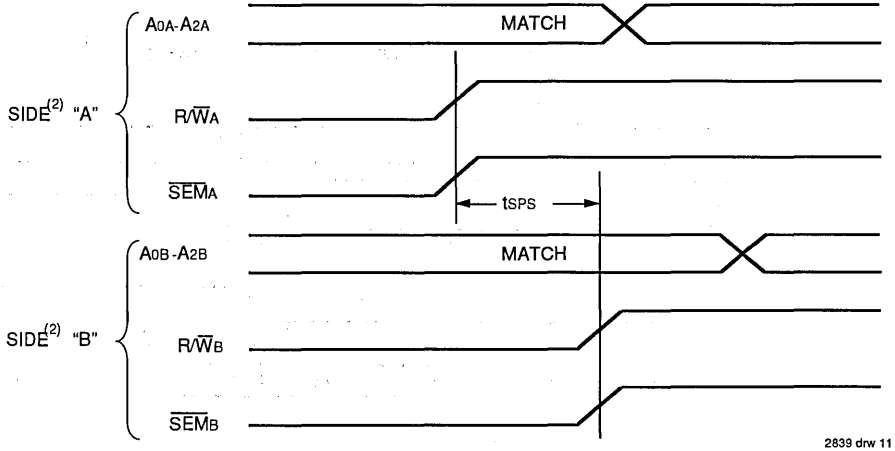
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)



2839 drw 10

NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

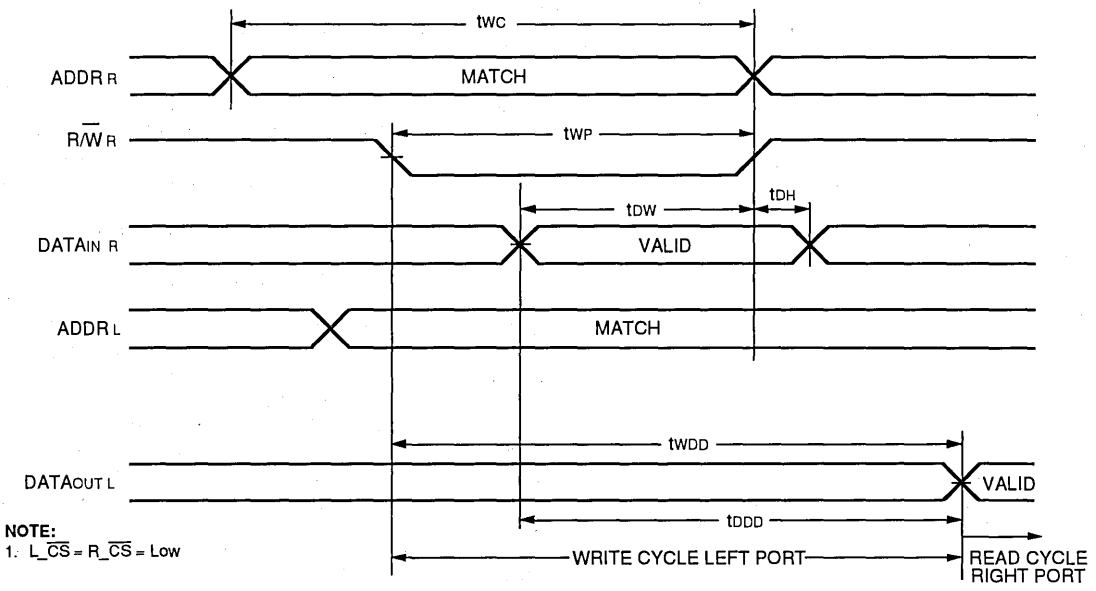
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



2839 drw 11

NOTES:
1. DOR = DOL = Low, L_$\overline{CS}$ = R_$\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}$A or $\overline{SEM}$A going High to R/$\overline{W}$B or $\overline{SEM}$B going High.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1)



NOTE:
1. L_CS = R_CS = Low

2839 drw 12

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL(1)

Inputs(1)				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read from Memory
X	X	H	X	Hi-Z	Outputs Disabled

NOTE:
1. AOL — A12 ≠ A0R — A12R

2839 tbl 10

TABLE II: SEMAPHORE READ/WRITE CONTROL(1)

Inputs				Outputs	
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. AOL — A12 ≠ A0R — A12R

2839 tbl 11

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

Integrated Device Technology, Inc.

32K x 18
16K x 18
CEMOS™ PARALLEL
IN-OUT FIFO MODULE

IDT7MP2009
IDT7MP2010

FEATURES:

- First-In/First-Out memory module
- 32K x 18 organization (IDT7MP2009)
- 16K x 18 organization (IDT7MP2010)
- High speed: 15ns (max.) access time
- Separate upper and lower 9-bit XI and XO
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

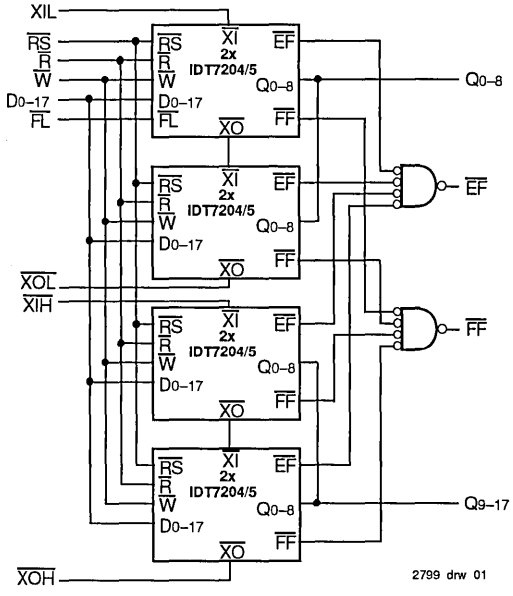
DESCRIPTION:

IDT7MP2009/7MP2010 are FIFO memory modules constructed on multi-layered epoxy laminate (FR-4) substrate by mounting eight IDT7205 (8K x 9) or IDT7204 (4K x 9) FIFOs in plastic leaded chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7205s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize a algorithm that loads and empties data on a first-In/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

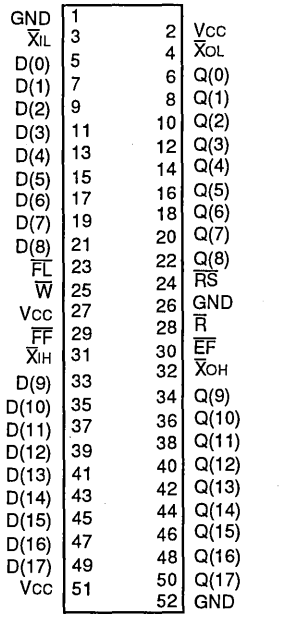
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE (W) and READ (R) pins. The devices have a read/write cycle time of 25ns (min.) for commercial temperature ranges.

The devices utilize a 18-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ZIP
TOP VIEW

2799 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL}$	First Load
D_{0-17}	$DATA_{IN}$
Q_{0-17}	$DATA_{OUT}$
$\overline{X}IH$, $\overline{X}IL$	Expansion In (High Bit, Low Bit)
$\overline{X}OH$, $\overline{X}OL$	Expansion Out (High Bit, Low Bit)
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}	Power
GND	Ground

2799 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} (1)	Input High Voltage Commercial	2.0	—	—	V
V_{IL} (1)	Input Low Voltage Commercial	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

2799 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	120	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

2799 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2799 tbl 01

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT7MP2010 Min.	IDT7MP2010 Max.	IDT7MP2009 Min.	IDT7MP2009 Max.	Unit
$\|I_{LI}\|$(1)	Input Leakage Current (Any Input)	—	20	—	20	µA
$\|I_{OL}\|$(2)	Output Leakage Current	—	80	—	80	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	0.4	—	0.4	V
I_{CC1}(3)	Operating Current	—	1280	—	1200	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/$\overline{RT}$ = V_{IH})	—	125	—	115	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	65	—	65	mA

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. R ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.

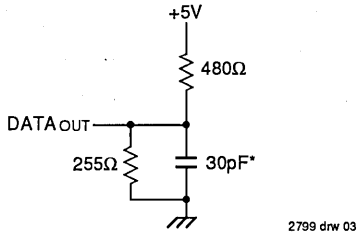
2799 tbl 05

7

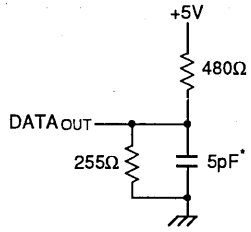
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2799 tbl 06



2799 drw 03



2799 drw 04

* Includes scope and jig capacitances.

Figure 1. Output Load
*** Includes scope and jig capacitances.**

Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP2009SxxZ, 7MP2010SxxZ										
		-15[3]		-20[3]		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}[1]	Read Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	5	—	5	—	5	—	10	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	15	—	13	—	20	—	20	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}[1]	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	15	—	18	—	18	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}[1]	Reset Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	17	—	20	—	25	—	30	—	35	ns
t_{RFF}	Read High to Full Flag High	—	20	—	23	—	25	—	30	—	35	ns
t_{WEF}	Write High to Empty Flag High	—	20	—	23	—	25	—	30	—	35	ns
t_{WFF}	Write Low to Full Flag Low	—	17	—	20	—	25	—	30	—	35	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.
3. Preliminary specifications only.

2799 tbl 07

AC ELECTRICAL CHARACTERISTICS

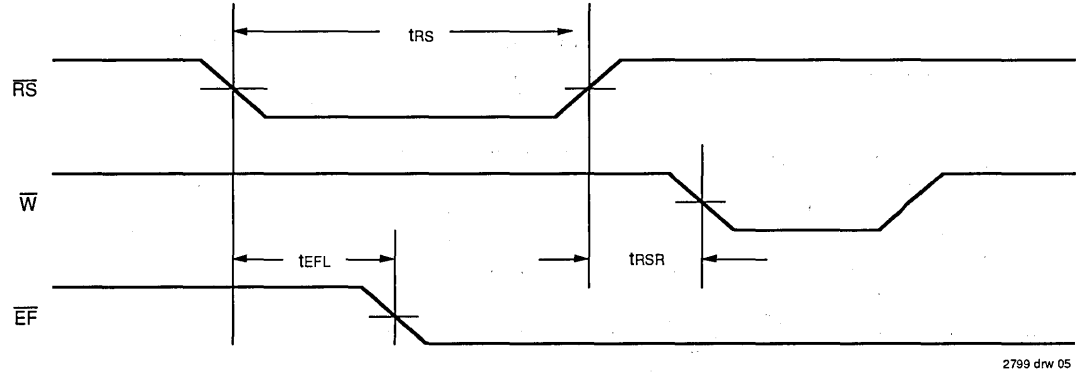
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP2009SxxZ, 7MP2010SxxZ								
		-40		-50		-60		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	ns
t_{RPW}[1]	Read Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	ns
t_{WPW}[1]	Write Pulse Width	40	—	50	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	ns
t_{RS}[1]	Reset Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	75	—	85	ns
t_{REF}	Read Low to Empty Flag Low	—	40	—	50	—	60	—	70	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	ns

2799 tbl 08

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF RESET CYCLE[1,2]

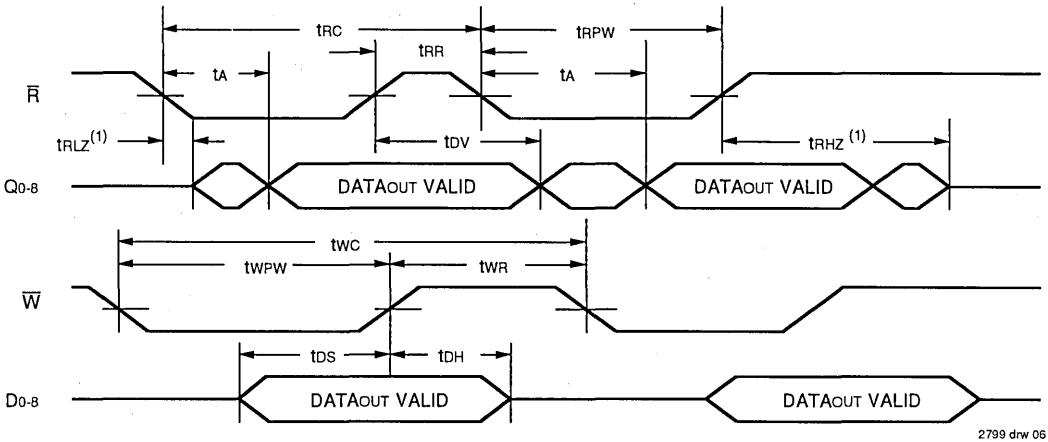


2799 drw 05

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

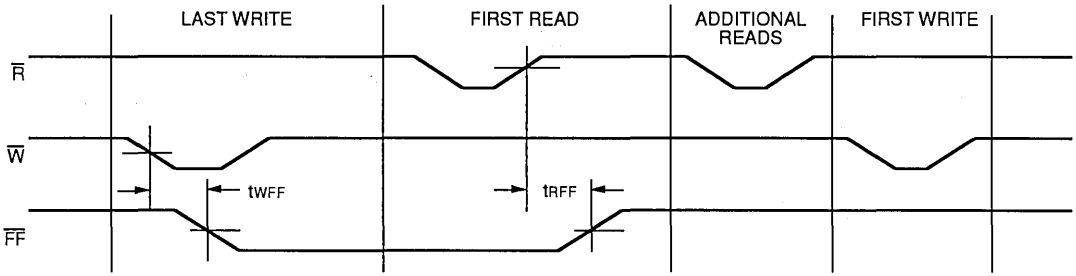
7

TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



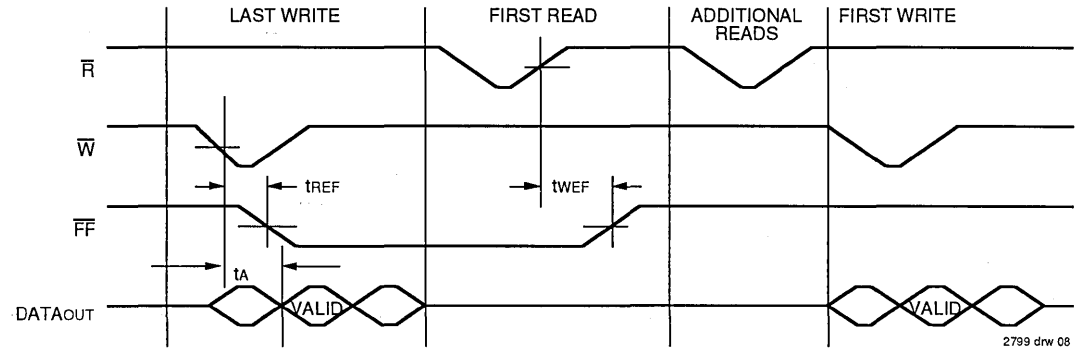
2799 drw 06

TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



2799 drw 07

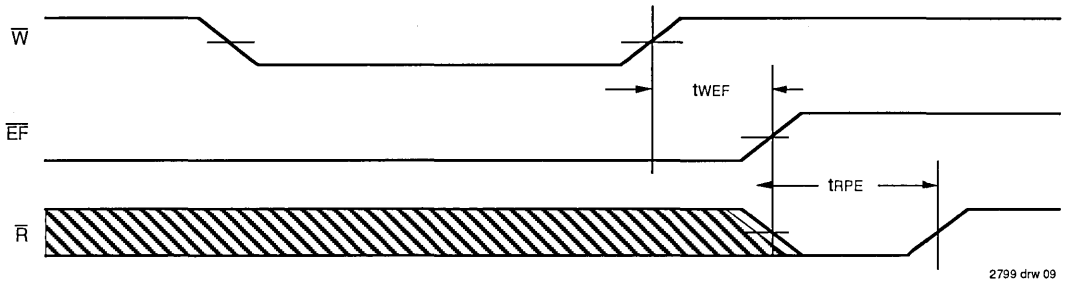
TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE(1)



2799 drw 08

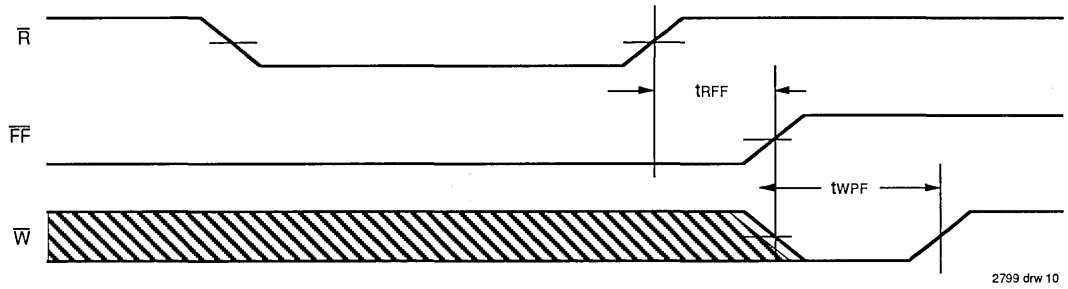
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF THE EMPTY FLAG CYCLE(1)



NOTE:
1. (t_{RPE} = t_{RPW})

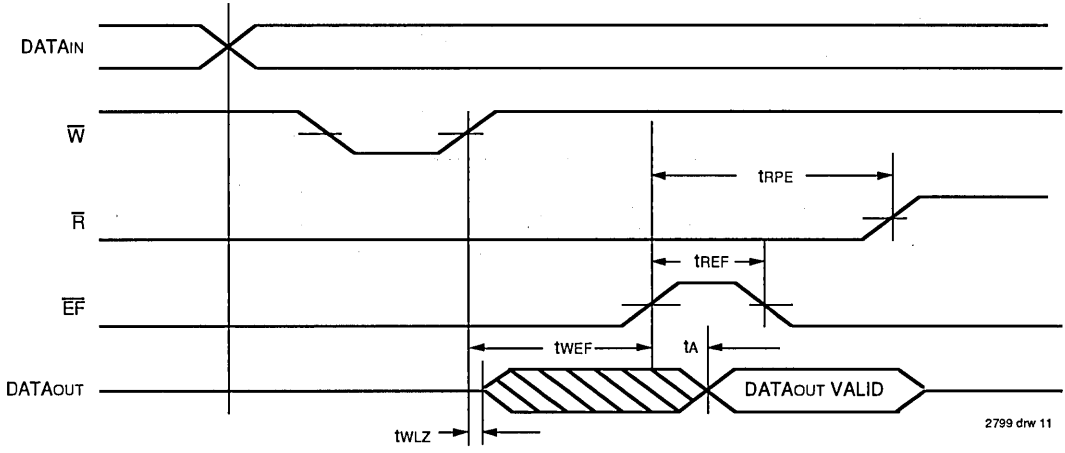
TIMING WAVEFORM OF THE FULL FLAG CYCLE



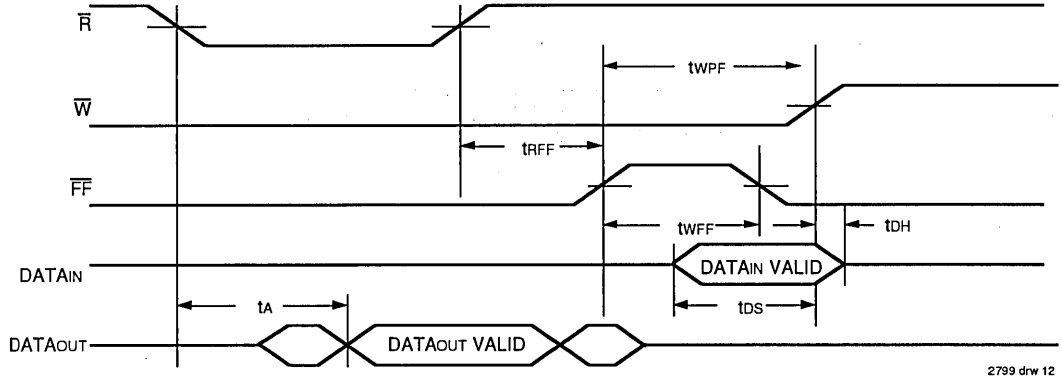
NOTE:
1. (t_{WPF} = t_{WPW})

7

TIMING WAVEFORM OF READ DATA FLOW-THROUGH MODE



TIMING WAVEFORM OF WRITE DATA FLOW-THROUGH MODE

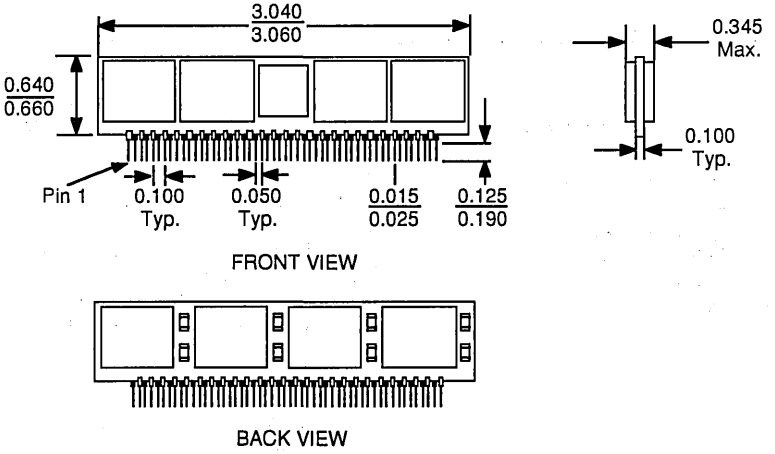


DEPTH/WIDTH EXPANSION & DATA FLOW-THROUGH MODES:

For more details on expanding FIFO modules in depth and/or width, please refer to the IDT7204 or IDT7205 data sheets.

For more details on data flow-through modes (read data fall-through and write data fall-through), please refer to the IDT7204 or IDT7205 data sheets.

PACKAGE DIMENSIONS



2799 drw 13

7

Integrated Device Technology, Inc.

32K/64K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

IDT7M207
IDT7M208

FEATURES:

- First-In/First-Out memory module
- 64K x 9 (IDT7M208) or 32K x 9 (IDT7M207)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable: depth and/or width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

DESCRIPTION:

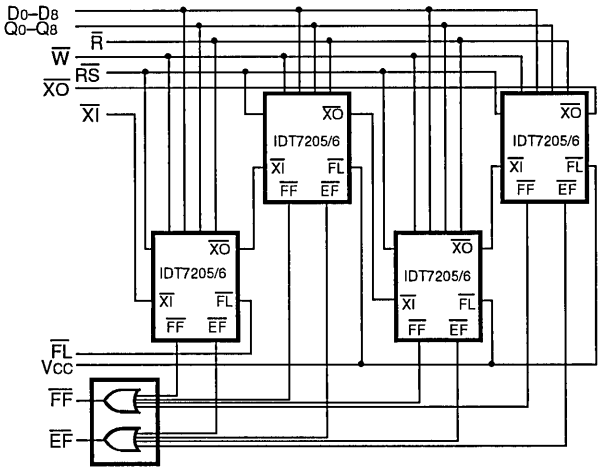
IDT7M207 and IDT7M208 are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7205 (8K x 9) or IDT7206 (16K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7205/6s fabricated in IDT's high performance CEMOS technology. These devices utilize an algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags as warnings for data overflow and underflow conditions and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 20ns (min.) for commercial and 30ns (min.) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's Military FIFO modules have semiconductor components manufactued in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

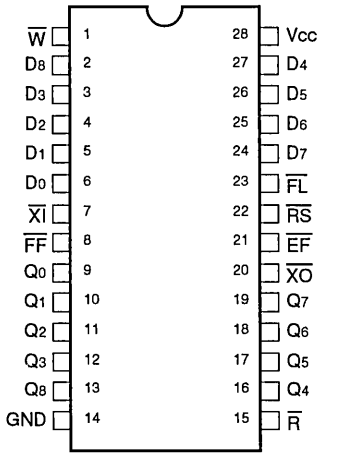
FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

2718 drw 01

PIN CONFIGURATION



DIP
TOP VIEW

2718 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATAIN	$\overline{XO}$ = EXPANSION OUT	V_{cc} = 5V
$\overline{RS}$ = RESET	Q = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

2718 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2718 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	50	pF

NOTE: 2718 tbl 03

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTES: 2718 tbl 04

1. VIH = 2.6V for $\overline{XI}$ input (commercial)
   VIH = 2.8V for $\overline{XI}$ input (military)
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V±10%, TA = 0°C to +70°C; and –55°C to +125°C)

Symbol	Parameter	Commercial Min.	Commercial Max.	Military Min.	Military Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–5	5	-40	40	µA
ILO(2)	Output Leakage Current	–40	40	-40	40	µA
VOH	Output Logic "1" Voltage IOUT = –2mA	2.4	—	2.4	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	0.4	—	0.4	V
ICC1(3)	Average VCC Power Supply Current	—	560	—	720	mA
ICC2(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/$\overline{RT}$ = VIH)	—	60	—	80	mA
ICC3(3)	Power Down Current (All Input = VCC – 0.2V)	—	32	—	48	mA

NOTES: 2718 tbl 05

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Icc measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2718 tbl 06

7

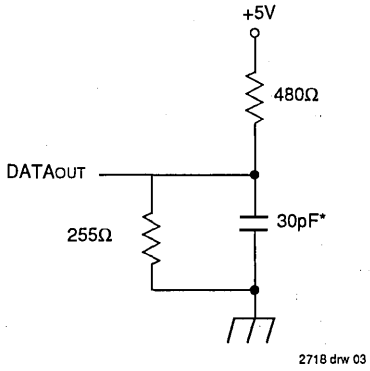


Figure 1. Output Load
*** Includes scope and jig capacitances.**

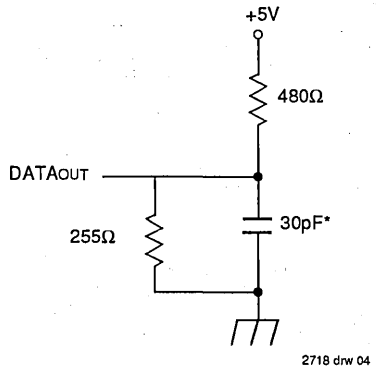


Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C and –55°C to +125°C)

		-20[3] (Com'l Only)		-25[3] (Com'l Only)		-30[3]		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fs	Shift Frequency	—	33.3	—	28.6	—	25	—	22.5	MHz
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW[1]	Read Pulse Width	20	—	25	—	30	—	35	—	ns
tRLZ[2]	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
tWLZ[2]	Write Pulse High to Data Bus at Low Z	5	—	5	—	5	—	10	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ[2]	Read Pulse High to Data Bus at High Z	—	16	—	20	—	20	—	20	ns
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tWPW[1]	Write Pulse Width	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
tRS[1]	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Emtpy Flag Low	—	30	—	35	—	40	—	45	ns
tREF	Read Low to Emtpy Flag Low	—	23	—	25	—	30	—	35	ns
tRFF	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
tWEF	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
tWFF	Write Low to Full Flag Low	—	23	—	25	—	30	—	35	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Preliminary specifications only.

2718 tbl 07

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C and –55°C to +125°C)

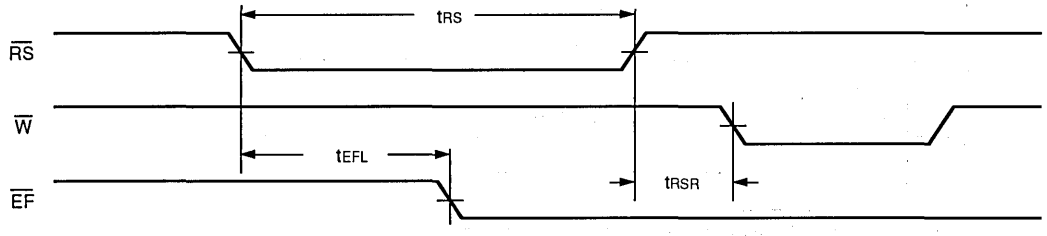
Symbol	Parameter	-40		-50		-60		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fs	Shift Frequency	—	20	—	15.4	—	13.3	—	11.6	MHz
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	ns
t_{RPW}[1]	Read Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	ns
t_{WPW}[1]	Write Pulse Width	40	—	50	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	ns
t_{RS}[1]	Reset Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	55	—	65	—	75	—	85	ns
t_{REF}	Read Low to Emtpy Flag Low	—	40	—	50	—	60	—	70	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	ns

NOTES:
1. Pulse widths less than minimum value are not allowed
2. Values guaranteed by design, not currently tested.

2718 tbl 08

7

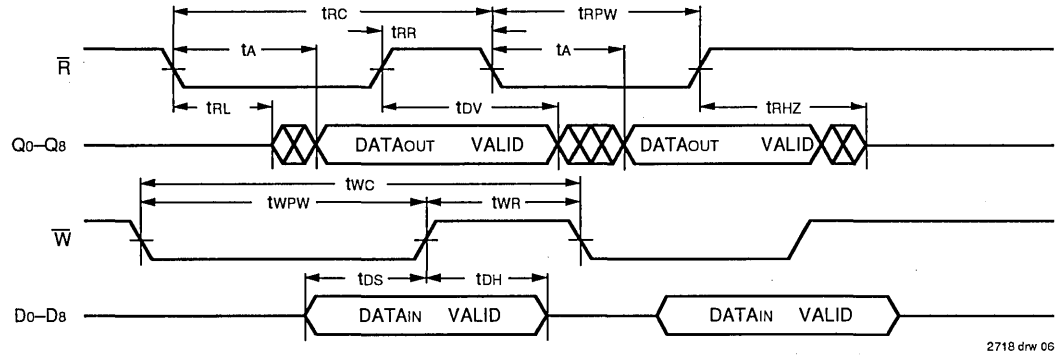
TIMING WAVEFORM OF RESET CYCLE[1,2]



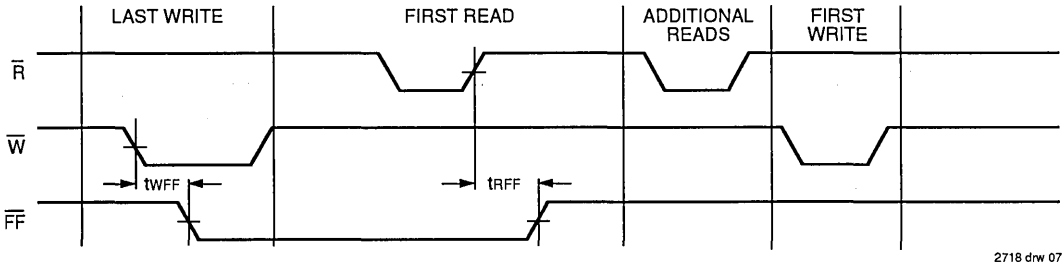
2718 drw 05

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

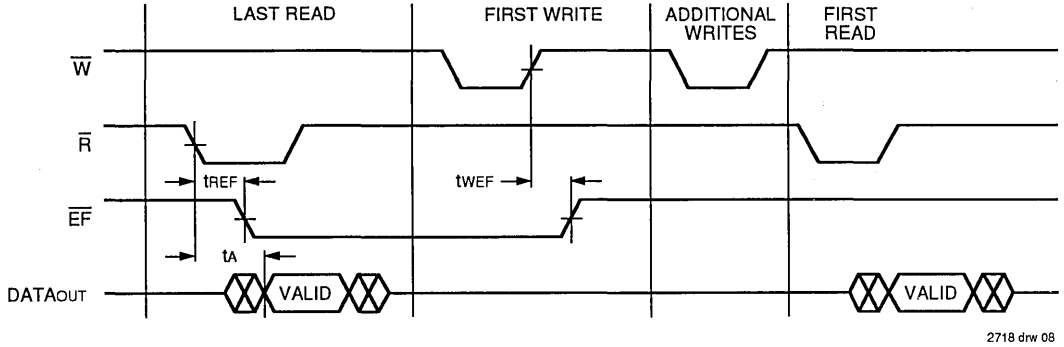
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ

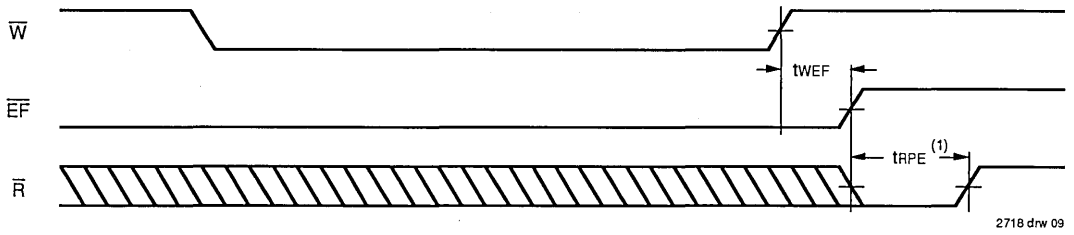


TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



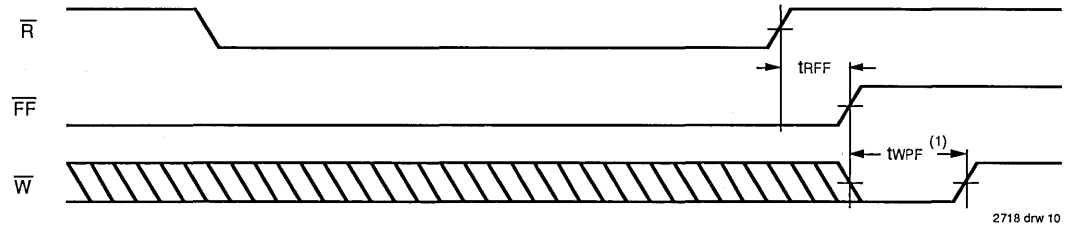
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM FOR THE EMPTY FLAG CYCLE



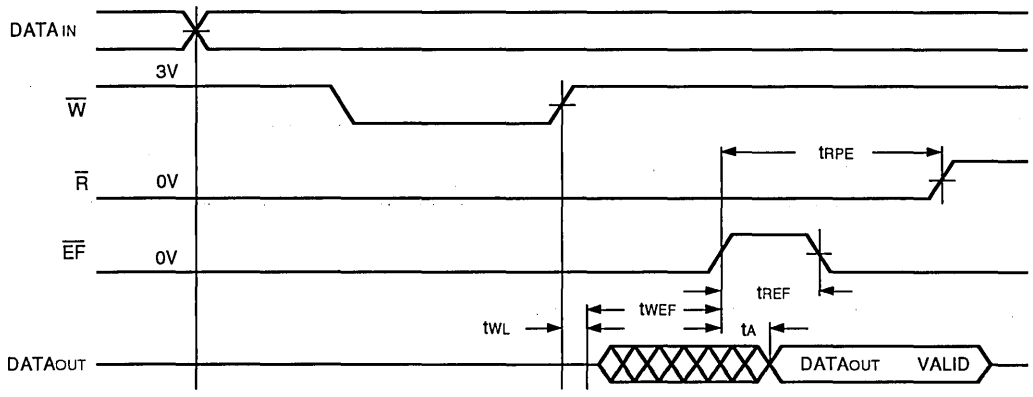
NOTE:
1. t_{RPE} must be ≥ $t_{RPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM FOR THE FULL FLAG CYCLE



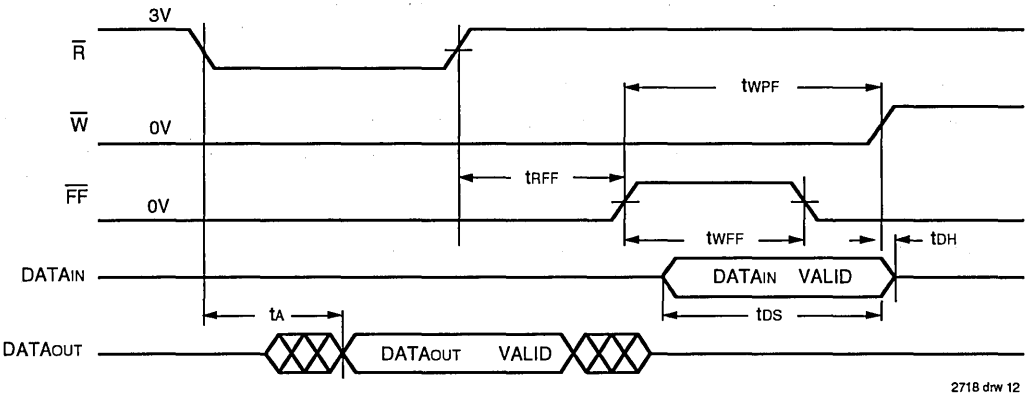
NOTE:
1. t_{WPF} must be ≥ $t_{WPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM OF READ DATA FLOW-THROUGH MODE



2718 drw 11

TIMING WAVEFORM OF WRITE DATA FLOW-THROUGH MODE



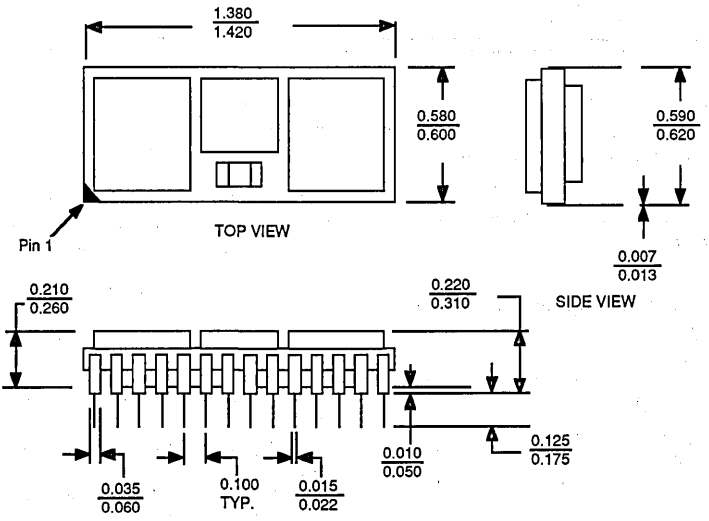
2718 drw 12

DEPTH/WIDTH EXPANSION & DATA FLOW-THROUGH MODES:

For more details on expanding FIFO modules in depth and/or width, please refer to the IDT7205 or IDT7206 data sheets.

For more details on data flow-through modes (read data fall through and write data fall-through), please refer to the IDT7205 or IDT7206 data sheets.

PACKAGE DIMENSIONS



2718 drw 13

7

Integrated Device Technology, Inc.

1M x 32 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4104

FEATURES:

- High density 4 megabyte static RAM module
- Low profile 80 pin ZIP (Zig-zag In-line vertical Package) or 80 pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION[1]

PD_0	2	1	GND	PD_0-NC
PD_2	4	3	PD_1	PD_1-GND
I/O_0	6	5	I/O_4	PD_2-NC
I/O_1	8	7	V_{CC}	
I/O_2	10	9	I/O_5	
I/O_3	12	11	I/O_6	
GND	14	13	I/O_7	
A_5	16	15	A_0	
A_6	18	17	A_1	
A_7	20	19	A_2	
A_8	22	21	A_3	
A_9	24	23	V_{CC}	
A_{10}	26	25	A_4	
I/O_8	28	27	GND	
I/O_9	30	29	I/O_{12}	
I/O_{10}	32	31	I/O_{13}	
I/O_{11}	34	33	I/O_{14}	
$\overline{WE_0}$	36	35	I/O_{15}	
$\overline{OE_0}$	38	37	$\overline{WE_1}$	
$\overline{CS}$	40	39	V_{CC}	
		41	GND	
NC	42	43	$\overline{OE_1}$	
$\overline{WE_2}$	44	45	$\overline{WE_3}$	
I/O_{16}	46	47	I/O_{20}	
I/O_{17}	48	49	I/O_{21}	
I/O_{18}	50	51	I/O_{22}	
I/O_{19}	52	53	I/O_{23}	
GND	54	55	A_{11}	
A_{17}	56	57	A_{12}	
A_{18}	58	59	A_{13}	
A_{19}	60	61	A_{14}	
NC	62	63	V_{CC}	
NC	64	65	A_{15}	
NC	66	67	GND	
NC	68	69	A_{16}	
NC	70	71	I/O_{28}	
I/O_{24}	72	73	V_{CC}	
I/O_{25}	74	75	I/O_{29}	
I/O_{26}	76	77	I/O_{30}	
I/O_{27}	78	79	I/O_{31}	
GND	80			

ZIP, SIMM
TOP VIEW

2769 drw 01

NOTE:

1. Pins 2, 3 and 4 (PD_0, PD_1 and PD_2) are read by the user to determine the density of the module. If PD_0 reads NC, PD_1 reads GND and PD_2 reads NC, then the module has a 1M depth.

DESCRIPTION:

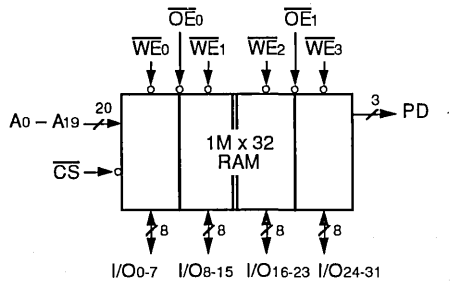
The IDT7MP4104 is a 1M x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 1M x 4 static RAMs in plastic packages. Availability of four write enable lines (one for each group of two RAMs) provides byte access. The IDT7MP4104 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MP4104 is packaged in a 80 pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 80 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 80 pins to be placed on a package 4.45 inches long and 0.35 inches wide. At only 0.60 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4104 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Three identification pins (PD0, PD1 and PD2) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0, PD1 and PD1 to determine a 1M depth.

FUNCTIONAL BLOCK DIAGRAM



2769 drw 02

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-19}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE_0}$-$\overline{WE_3}$	Write Enables
$\overline{OE_0}$	Output Enable for Lower Word
$\overline{OE_1}$	Output Enable for Upper Word
PD_0-PD_2	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

2769 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
C_{IN1}	Input Capacitance (Address, $\overline{CS}$)	$V_{(IN)}$ = 0V	60	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	$V_{(IN)}$ = 0V	15	pF
C_{IN3}	Input Capacitance ($\overline{OE}$)	$V_{(IN)}$ = 0V	30	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	15	pF

NOTE: 2769 tbl 02
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2769 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2769 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2769 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2769 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2769 tbl 07

Symbol	Parameter	Test Conditions	7MP4104 Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	80	mA

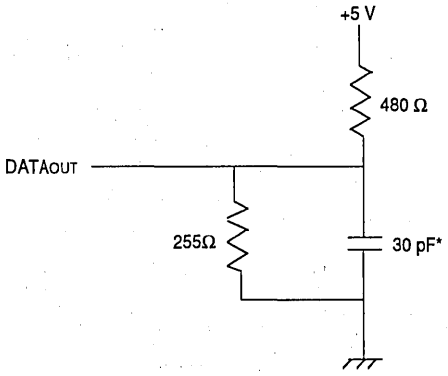
2769 tbl 08

7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

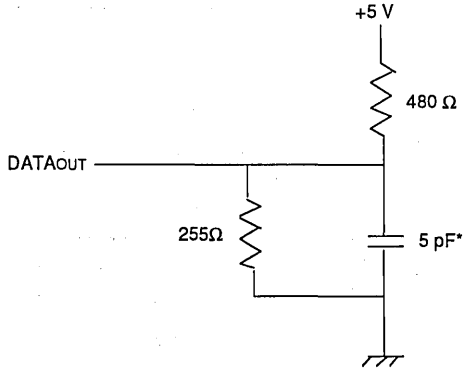
2769 tbl 09



2769 drw 03

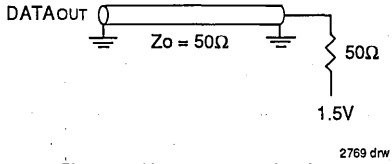
*Includes scope and jig.

Figure 1. Output Load



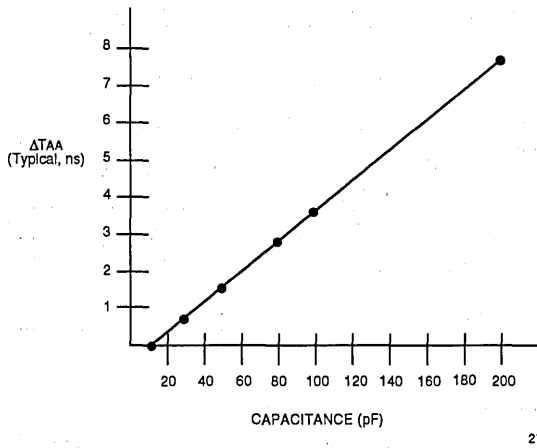
2769 drw 04

Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})



2769 drw 05

Figure 3. Alternate Output Load



2769 drw 06

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

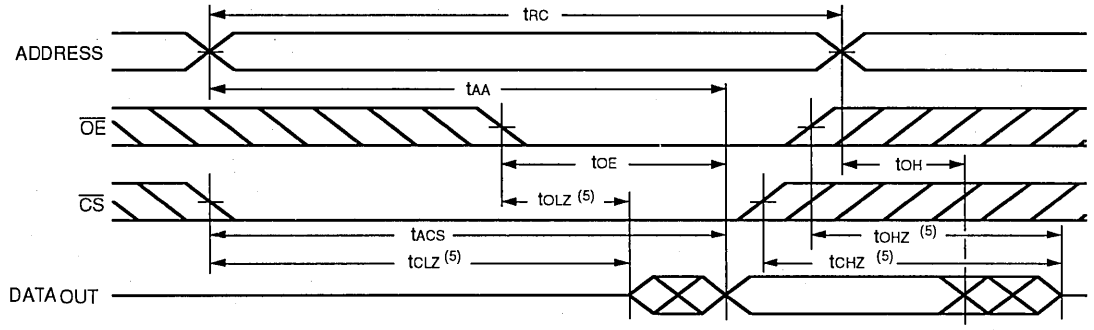
Symbol	Parameter	7MP4104SxxZ, 7MP4104SxxM						Unit
		-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	18	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	10	—	12	—	18	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	10	—	12	—	18	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	20	—	25	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	10	—	15	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2769 tbl 10

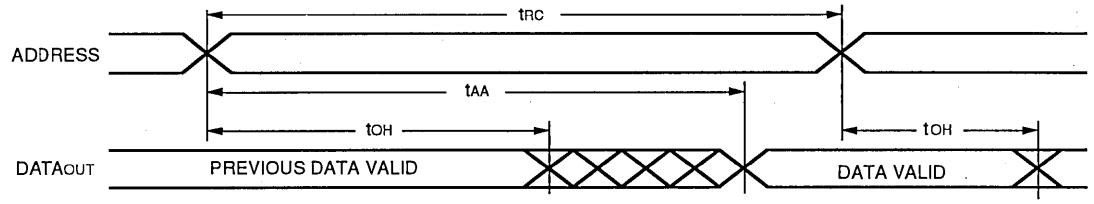
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



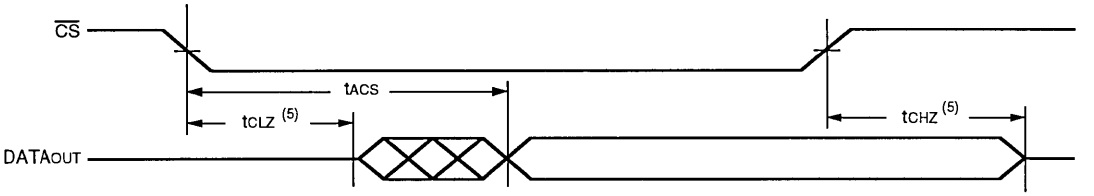
2769 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2769 drw 08

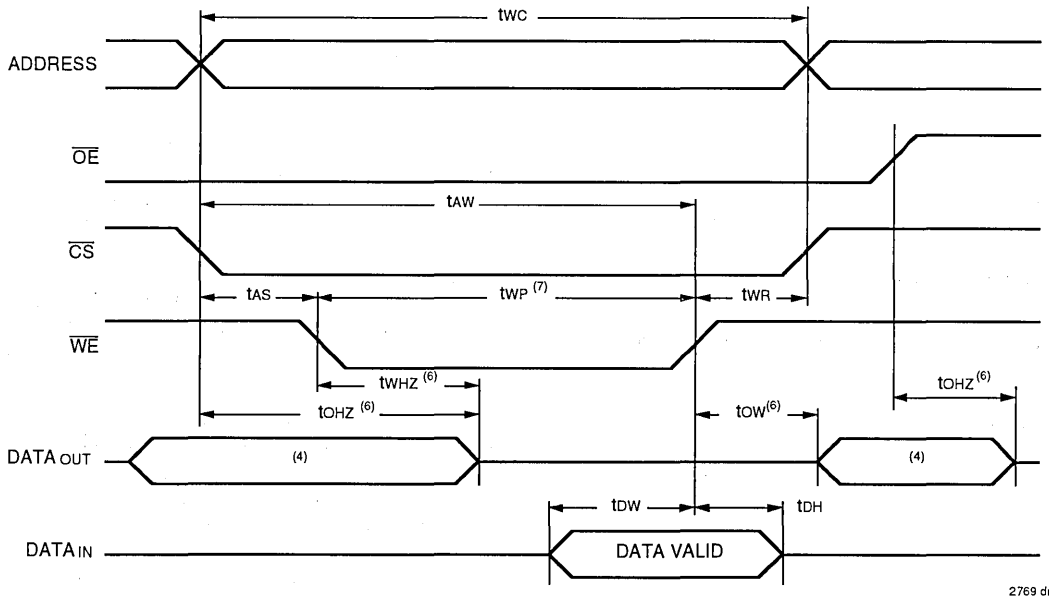
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



2769 drw 09

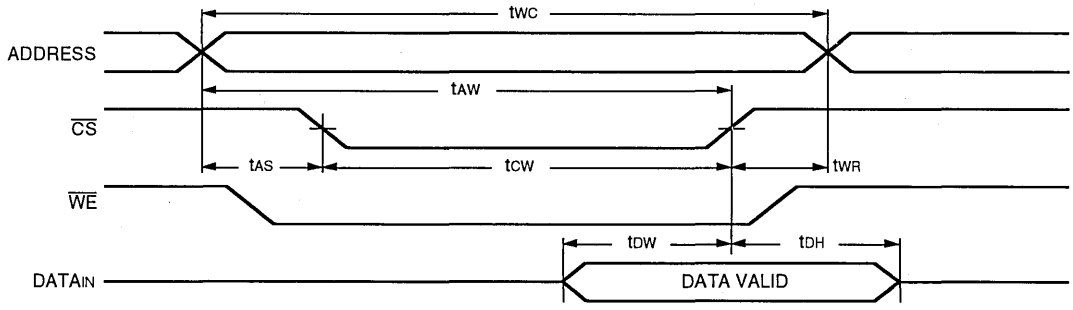
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



2769 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



2769 drw 11

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS - PLEASE CONSULT FACTORY FOR DETAILS

Integrated Device Technology, Inc.

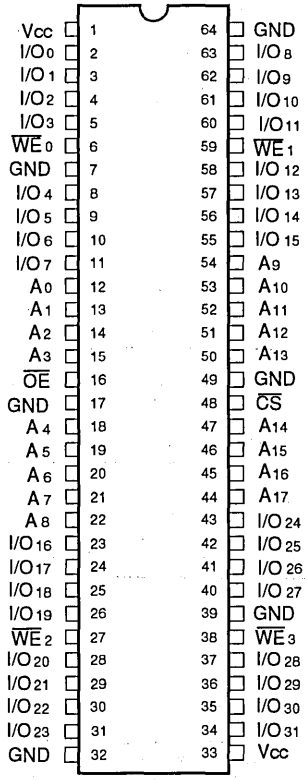
256K x 32 BiCMOS/CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4077

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin sidebraze DIP (Dual In-line Package)
- Very fast access time: 15ns (max.)
- Surface mounted leadless chip carrier (LCC) components on an multilayer ceramic substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

PIN CONFIGURATION



2814 drw 01

DIP
TOP VIEW

DESCRIPTION:

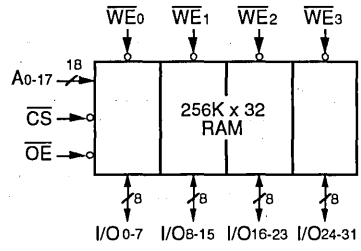
The IDT7M4077 is a 256K x 32 static RAM module constructed on a multilayer ceramic substrate using eight 256Kx4 static RAMs in leadless chip carrier (LCC) packages. Availability of four write enable lines (one for each group of two RAMs) provides byte write capability. The IDT7M4077 is available with access time as fast as 15ns with minimal power consumption.

The IDT7M4077 is packaged in a 64 pin sidebraze DIP (Dual In-line Package). The DIP configuration allows 64 pins to be placed on a package 3.5 inches long, 0.6 inches wide and 0.31 inches thick.

All inputs and outputs of the IDT7M4077 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2814 drw 02

PIN NAMES

I/O0–31	Data Inputs/Outputs
A0–17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$0–3	Write Enables
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2814 tbl 01

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2814 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2814 tbl 03

NOTE:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2814 tbl 04

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
$C_{I/O}$	I/O Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
C_{IN1}	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	90	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	$V_{(IN)}$ = 0V	35	pF

2814 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2814 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage ($\overline{WE}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2814 tbl 07

Symbol	Parameter	Test Conditions	7M4077(1, 2) Military Max.	7M4077(1, 2) Comm. Max.	7M4077(3) Military Max.	7M4077(3) Comm. Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1760	1600	1500	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	720	600	600	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	400	320	320	80	mA

2814 tbl 08

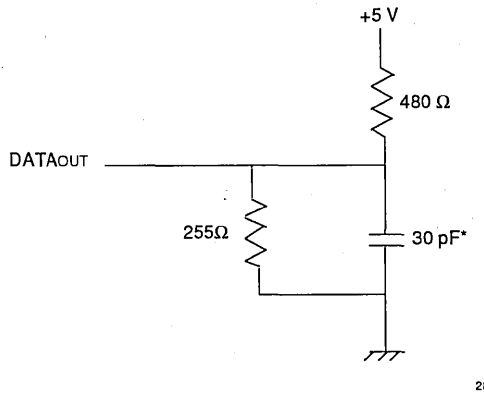
NOTES:
1. Preliminary specifications only.
2. 15-20ns versions only.
3. 25-55ns versions only.

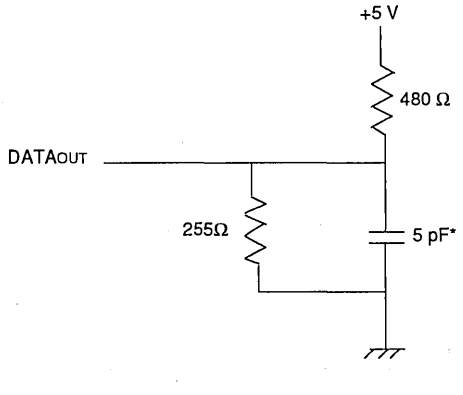
7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2814 tbl 09

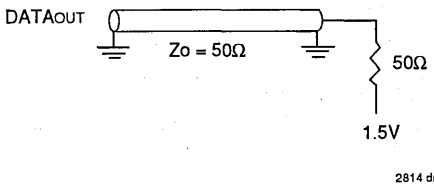




*Includes scope and jig.

Figure 1. Output Load

Figure 1. Output Load (for t_{OLZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})



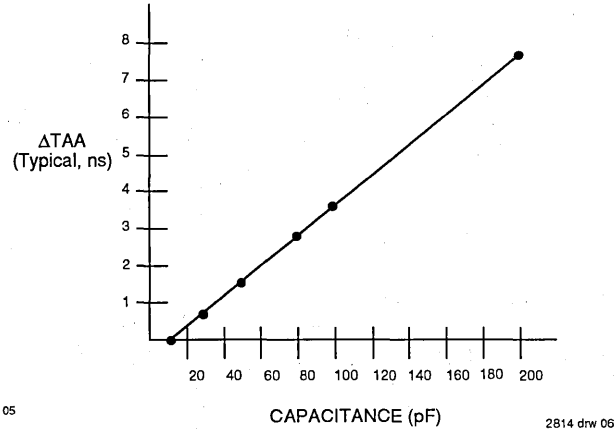


Figure 3. Alternate Output Load

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

		7M4077SxxC, 7M4077SxxCB						
		-15[2]		-17[2]		-20[2]		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	15	—	17	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	8	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	8	—	8	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	17	—	20	—	ns
t_{CW}	Chip Select to End of Write	12	—	15	—	17	—	ns
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	17	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	8	—	10	—	13	ns
t_{DW}	Data to Write Time Overlap	10	—	10	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2814 tbl 10

7

AC ELECTRICAL CHARACTERISTICS

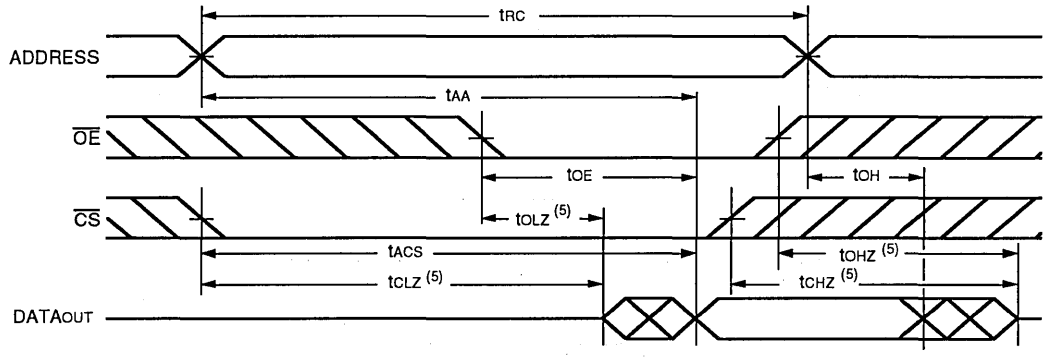
(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

		7M4077SxxC, 7M4077SxxCB										
		-25		-30		-35		-45		-55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	18	—	23	—	25	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	17	—	20	—	25	—	30	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	12	—	15	—	20	—	25	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	40	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	23	—	25	—	25	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	30	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

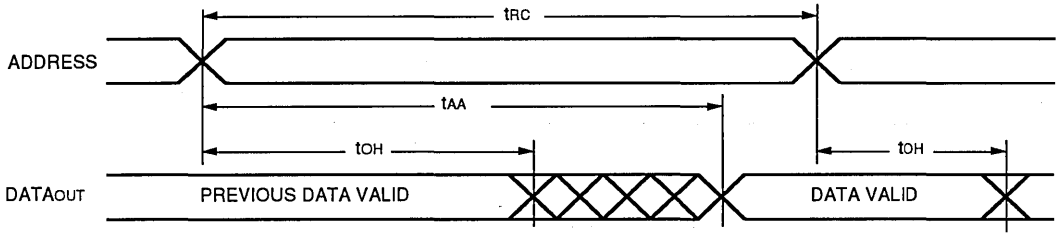
2814 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1(1,3,4)



2814 drw 07

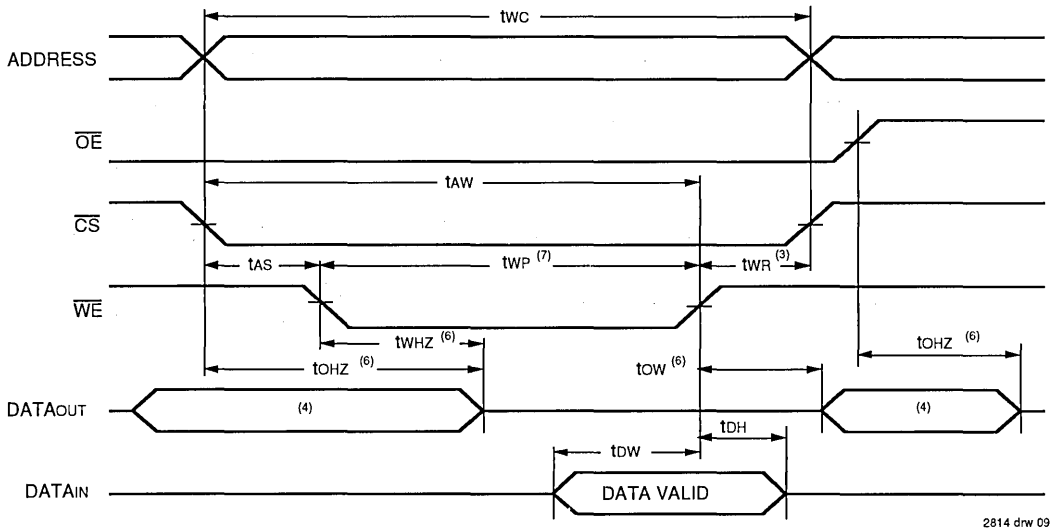
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



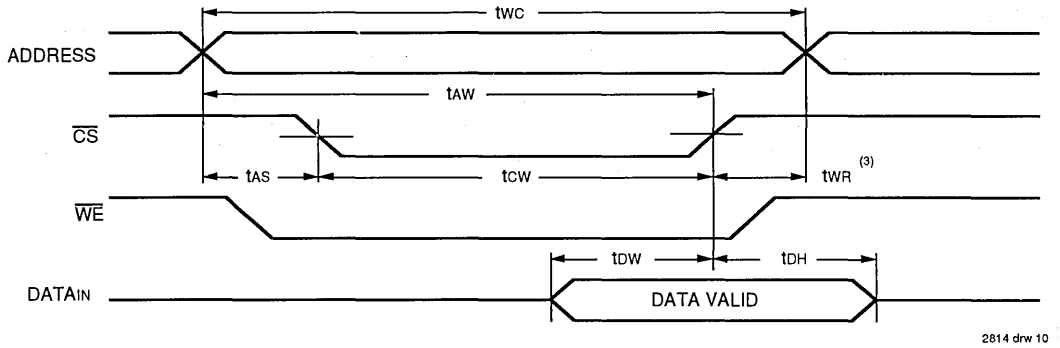
2814 drw 08

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1,2,3,7)

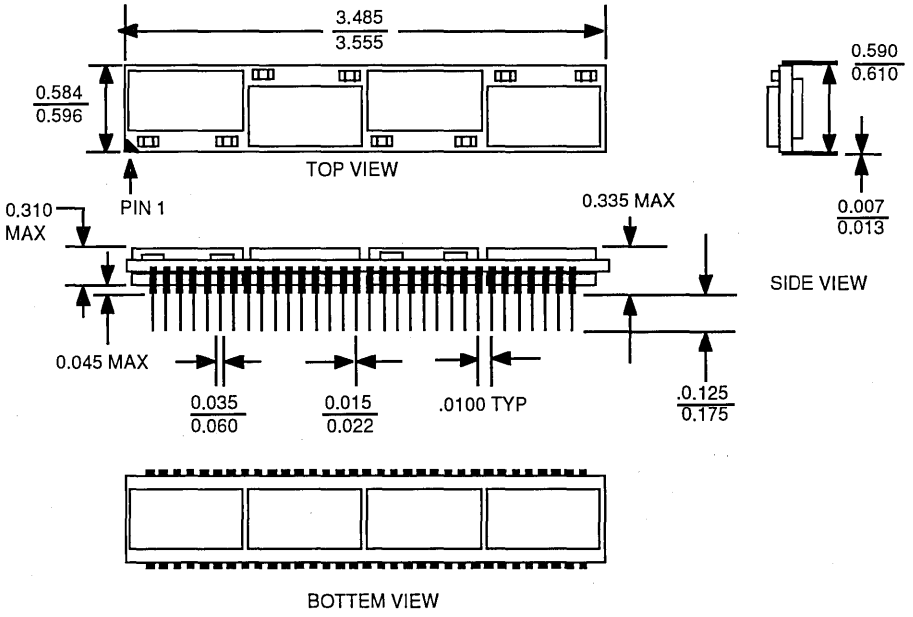


TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2814 drw 11

7

Integrated Device Technology, Inc.

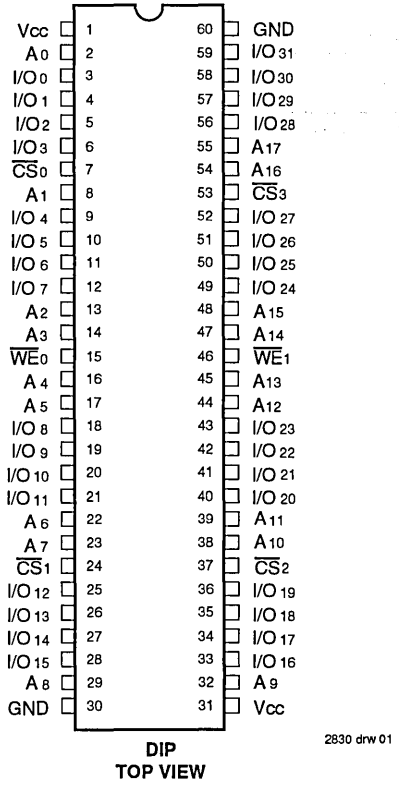
256K x 32 CMOS STATIC RAM MODULE

IDT7MB4067

FEATURES:

- High density 8 megabit static RAM module
- Low profile 60 pin DIP (Dual In-line Package)
- Very fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

PIN CONFIGURATION



DIP
TOP VIEW

2830 drw 01

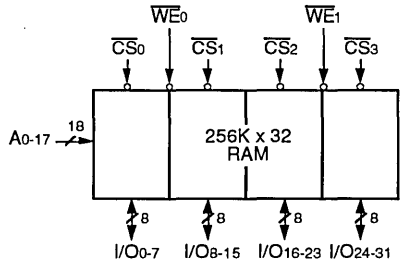
DESCRIPTION:

The IDT7MB4067 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MB4067 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MB4067 is packaged in a 60 pin DIP (Dual In-line Package). The DIP configuration allows 60 pins to be placed on a package 3.0 inches long and 0.6 inches wide and 0.365 inches tall.

All inputs and outputs of the IDT7MB4067 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



2830 drw 02

PIN NAMES

A_0-A_{17}	Addresses
I/O_{0-31}	Data Inputs/Outputs
$\overline{CS}_0$	Chip Select for I/O_{0-7}
$\overline{CS}_1$	Chip Select for I/O_{8-15}
$\overline{CS}_2$	Chip Select for I/O_{16-23}
$\overline{CS}_3$	Chip Select for I/O_{24-31}
$\overline{WE}_0$	Write Enable for I/O_{0-15}
$\overline{WE}_1$	Write Enable for I/O_{16-31}
GND	Ground
Vcc	Power

2830 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Data I/O Capacitance	$V_{(IN)}$ = 0V	15	pF
$C_{IN(W)}$	Input Capacitance ($\overline{WE}$)	$V_{(IN)}$ = 0V	40	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address)	$V_{(IN)}$ = 0V	75	pF

2830 tbl 02

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2830 tbl 03

NOTE:
1. V_{IL} (min) = –2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2830 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	Hi-Z	Standby
Read	L	H	Dout	Active
Write	L	L	Din	Active

2830 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2830 tbl 06

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4067 Min.	7MB4067 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2830 tbl 07

Symbol	Parameter	Test Conditions	7MB4067 Min.	7MB4067 Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	—	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	—	80	mA

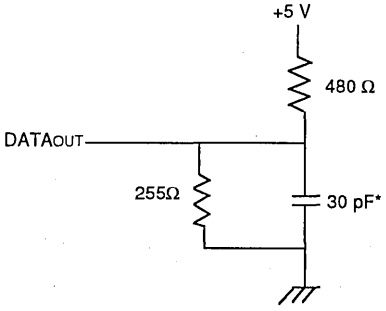
2830 tbl 08

7

AC TEST CONDITIONS

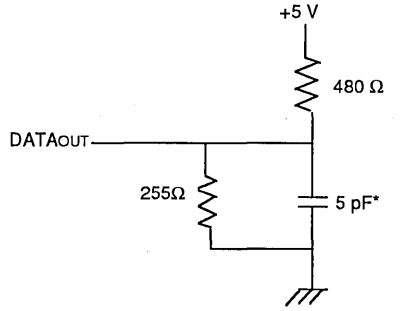
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2830 tbl 09



2830 drw 03 *Includes scope and jig

Figure 1. Output Load



2830 drw 04

Figure 1. Output Load (for tCHZ, tCLZ, tWHZ, tOW)

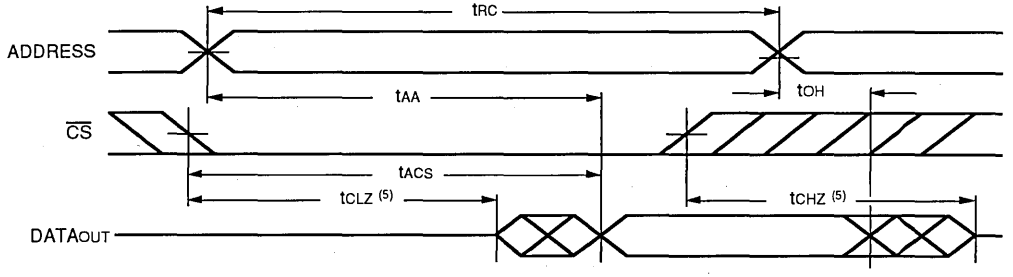
AC ELECTRICAL CHARACTERISTICS (VCC = 5V ±10%, TA = 0°C to +70°C)

		7MB4067SxxP										
		-20[2]		-25		-30		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

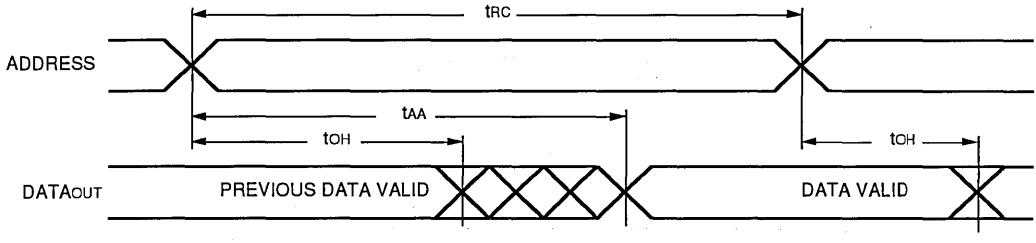
2830 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



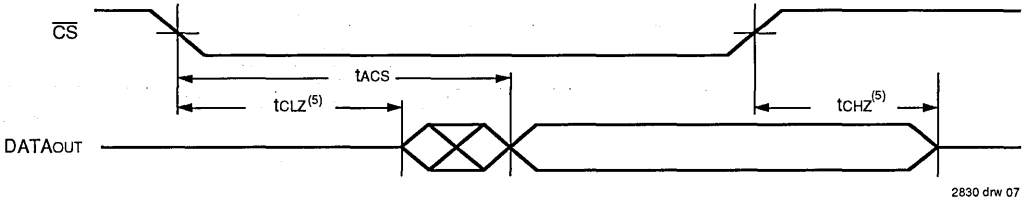
2830 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



2830 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)

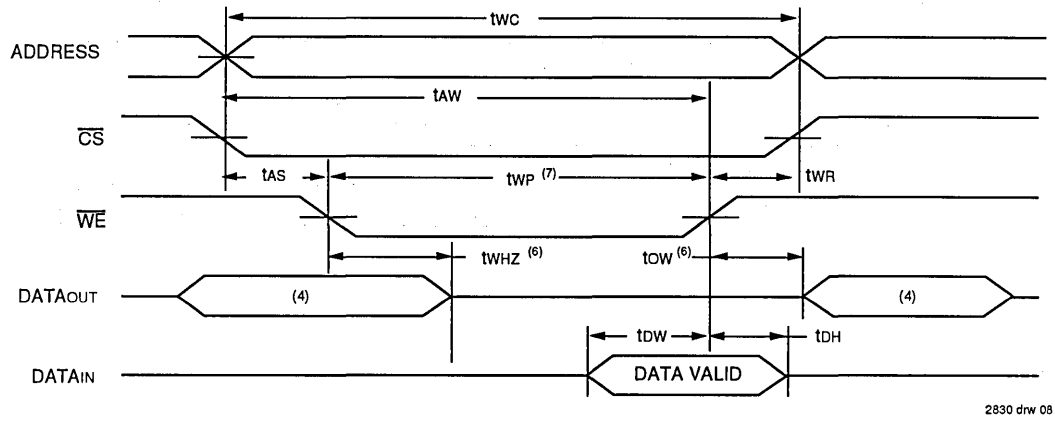


2830 drw 07

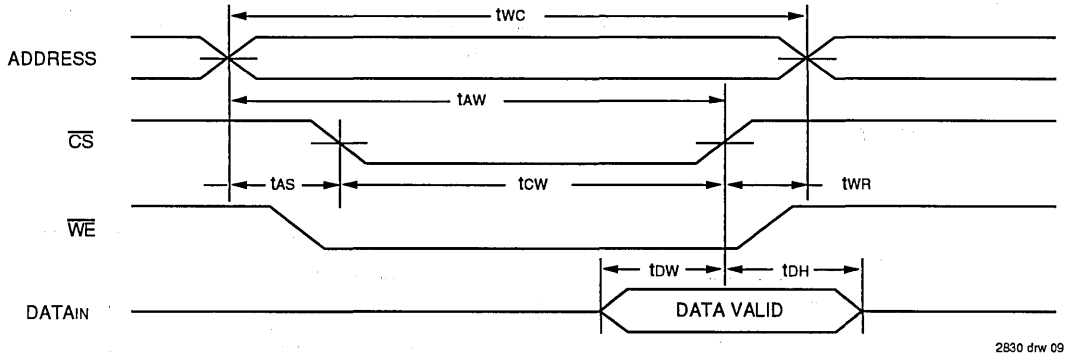
7

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



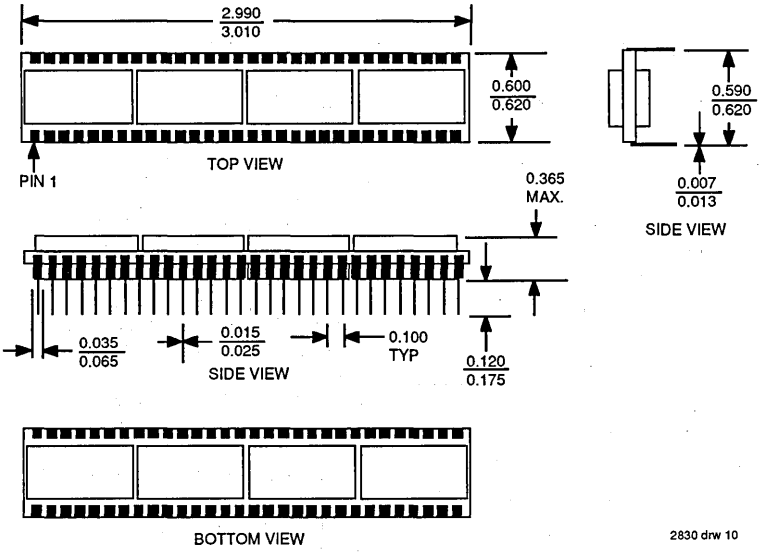
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. During a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}.

PACKAGE DIMENSIONS



7

Integrated Device Technology, Inc.

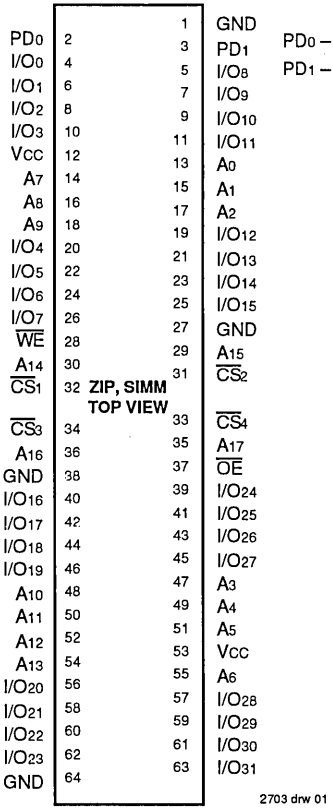
256K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4045

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION[1]



2703 drw 01

NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads GND and PD_1 reads GND, then the module had a 256K depth.

DESCRIPTION:

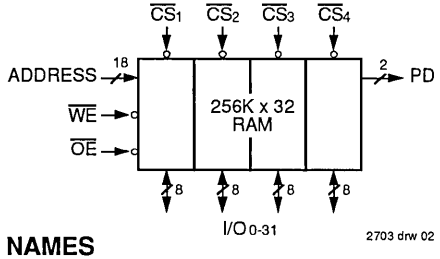
The IDT7MP4045 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 1 megabit static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ technology. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 64 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.60 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



2703 drw 02

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

2703 tbl 01

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CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE: 2703 tbl 02
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2703 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2703 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2703 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2703 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2703 tbl 07

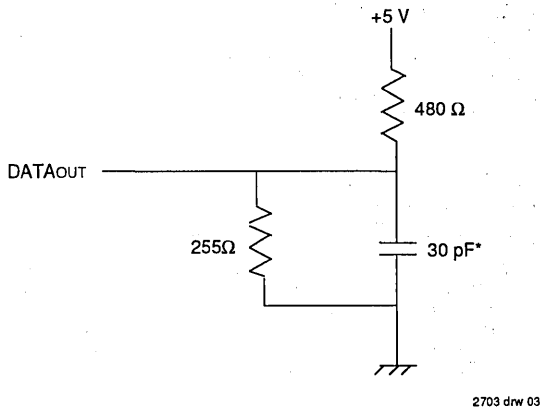
Symbol	Parameter	Test Conditions	10ns - 17ns[1] Max.	20ns - 45ns Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1600	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	320	80	mA

NOTE: 2703 tbl 08
1. Preliminary specifications only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2703 tbl 09



*Includes scope and jig.

Figure 1. Output Load

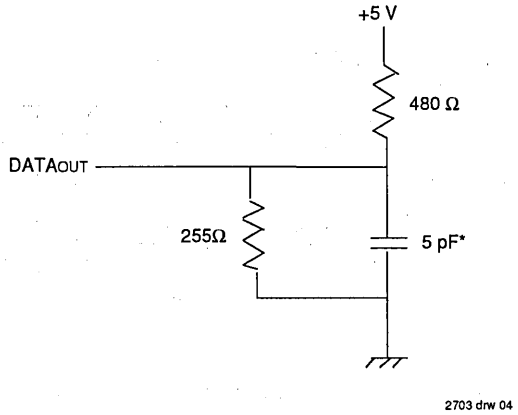


Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

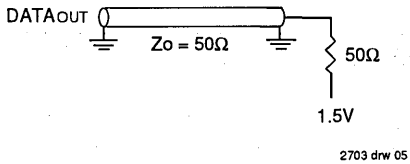


Figure 3. Alternate Output Load

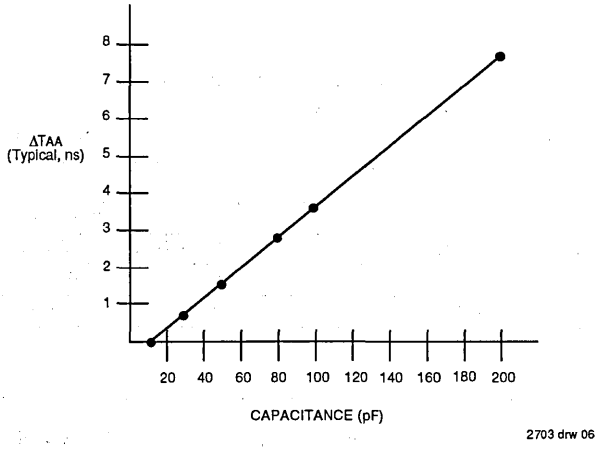


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM								Unit
		-10[2]		-12[2]		-15[2]		-17[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	7	—	8	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	5	—	6	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	5	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	5	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2703 tbl 10

7

AC ELECTRICAL CHARACTERISTICS

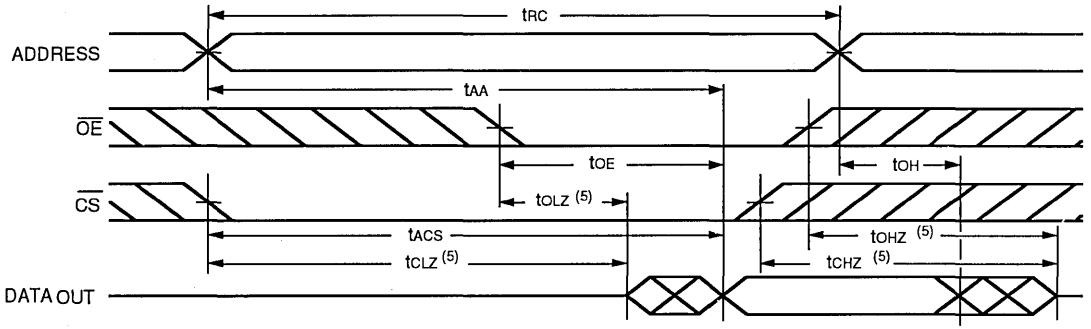
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MP4045SxxZ, 7MP4045SxxM										
		-20		-25		-30		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.

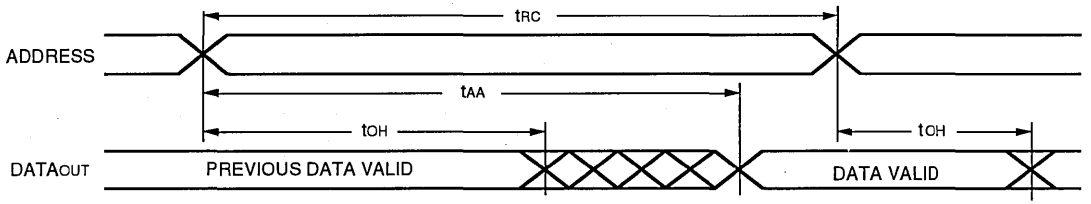
2703 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



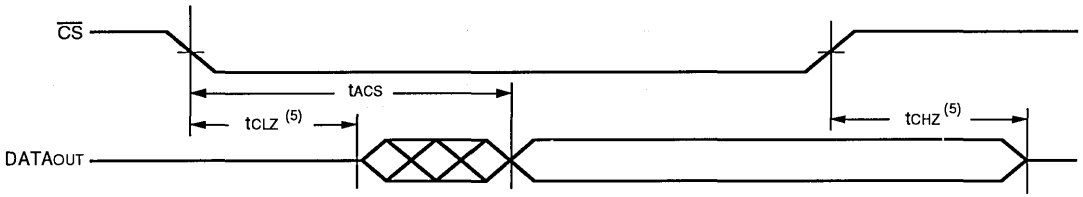
2703 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2703 drw 08

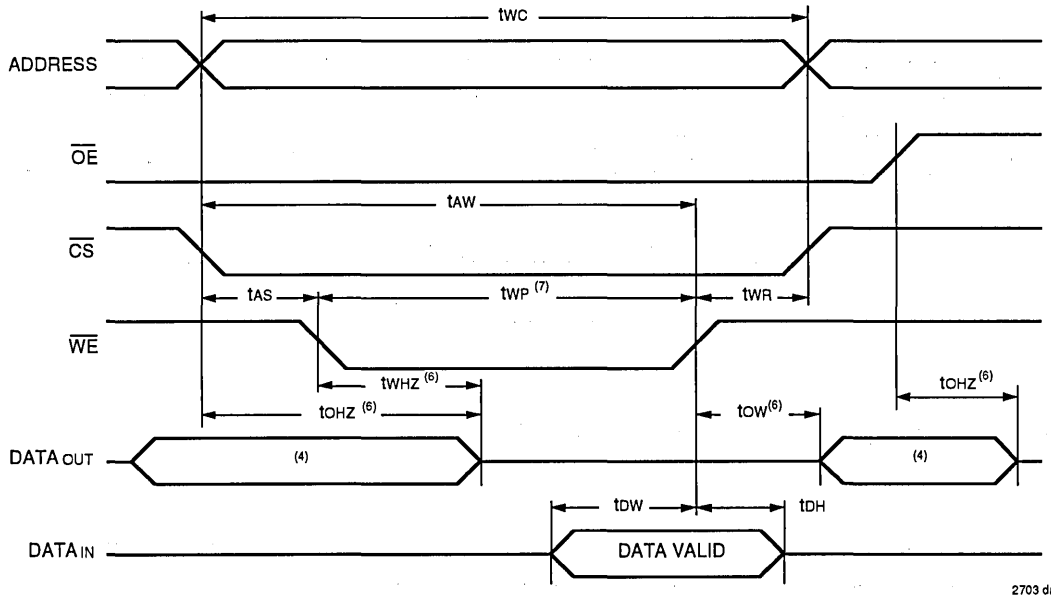
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



2703 drw 06

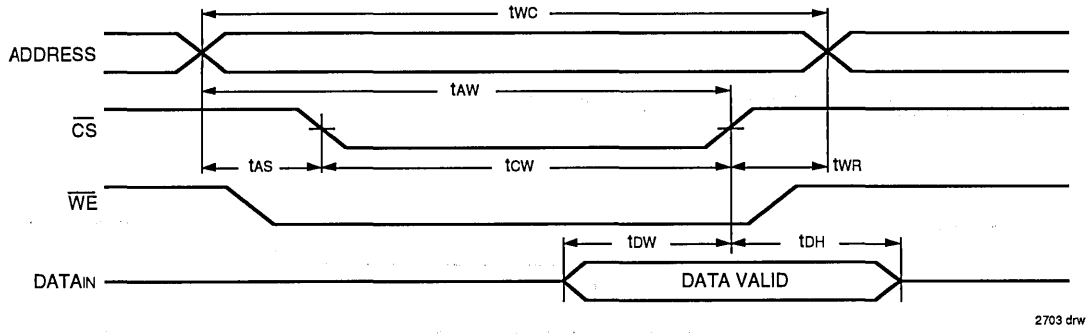
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



2703 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)

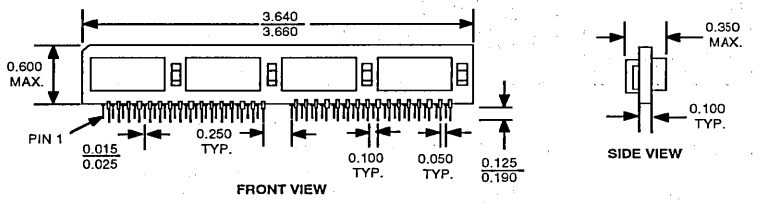


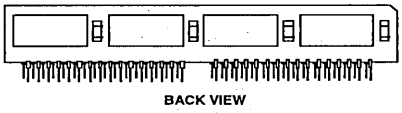
2703 drw 11

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS

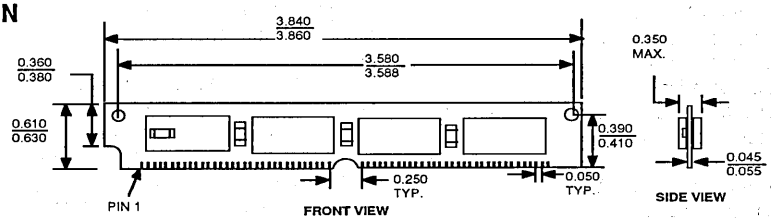
ZIP VERSION

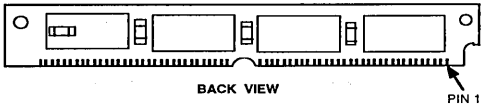




2703 drw 12

SIMM VERSION





2703 drw 13

7

Integrated Device Technology, Inc.

SUBSYSTEMS FLEXI-PAK™ FAMILY
32K x 32
128K x 32
CMOS STATIC RAM MODULES

IDT7M4003
IDT7M4013

FEATURES:

- High-density 1 megabit/4 megabit CEMOS™ static RAM modules
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules, with equivalent pin-outs, supporting a wide range of applications
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - 7M4003 - 15ns (max.) commercial
  - 7M4003 - 20ns (max.) military
  - 7M4013 - 15ns (max.) commercial
  - 7M4013 - 20ns (max.) military
- Low power CMOS operation
- Surface mounted LCC or SO components on a multi-layered co-fired ceramic substrate
- Offered in a 66-pin "PGA-type" HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M4003/4013 are high-speed, high-density 1megabit/4 megabit CMOS static RAM modules constructed on a multi-layer co-fired ceramic substrate using either 32K x 8 or 128K x 8 SRAM components.

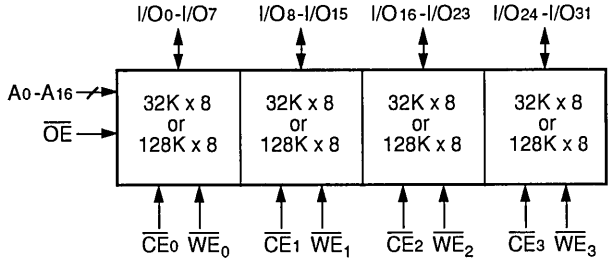
These modules are part of the IDT Subsytems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmable memory or those applications needing a combination of both. All three module configurations have equivalent pin-outs, making these "plug-in compatible" with each other (i.e. inter-changeable) suitable for a wide range of applications.

The IDT7M4003/4013 is available with access times as fast as 15ns over the commercial temperature range and 20ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit 1 megabit/4 megabit of memory into 1 sq. inch of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

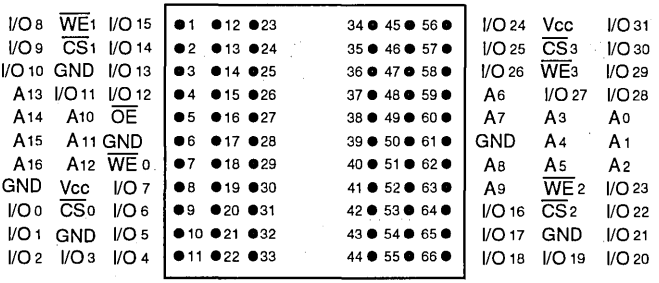
FUNCTIONAL BLOCK DIAGRAM



2711 drw 01

CMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



HIP
TOP VIEW

2711 drw 02

NOTE:
1. For the IDT7M4003 (32K x 32) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{0-3}$	Write Enables
$\overline{CS}_{0-3}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2711 tbl 01

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN(1)}$	Input Capacitance (DATA, $\overline{CS}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(2)}$	Input Capacitance (ADDRESS, $\overline{OE}$)	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2711 tbl 02
1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Read	L	H	H	High Z	Active
Write	L	X	L	$DATA_{IN}$	Active

2711 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2711 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2711 tbl 05
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2711 tbl 06

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.(1)	Max.(2)	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	10	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ f = f_{MAX}, Output Open	—	800	880	mA
I_{SB}	Standby Supply Curent	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ f = f_{MAX}, Output Open	—	80	280	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} > V_{CC}$ -0.2V or < 0.2V	—	80	80	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA(3)	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA(4)	2.4	—	—	V

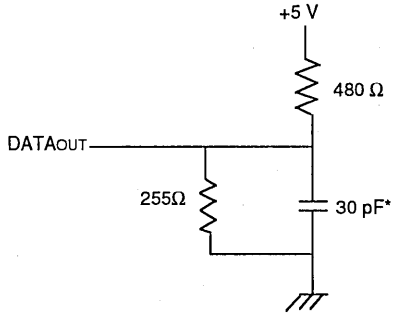
2711 tbl 07

NOTES:
1. For TA = 0°C to +70°C versions only.
2. For TA = -55°C to +125°C versions only.
3. I_{OL} = 2mA for 70ns – 100ns versions of the IDT7M4013.
4. I_{OH} = -1mA for 70ns – 100ns versions of the IDT7M4013.

AC TEST CONDITIONS

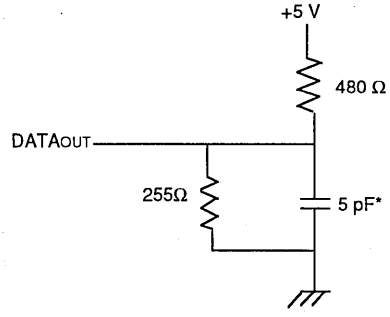
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2711 tbl 07



2711 drw 03

Figure 1. Output Load



2711 drw 04

Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15[2]		-17[2]		-20[2]		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE												
t_{RC}	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	12	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	6	—	7	—	7	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	12	—	13	—	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	6	—	8	—	9	—	12	—	13	ns
t_{DW}	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.

2711 tbl 09

7

AC ELECTRICAL CHARACTERISTICS

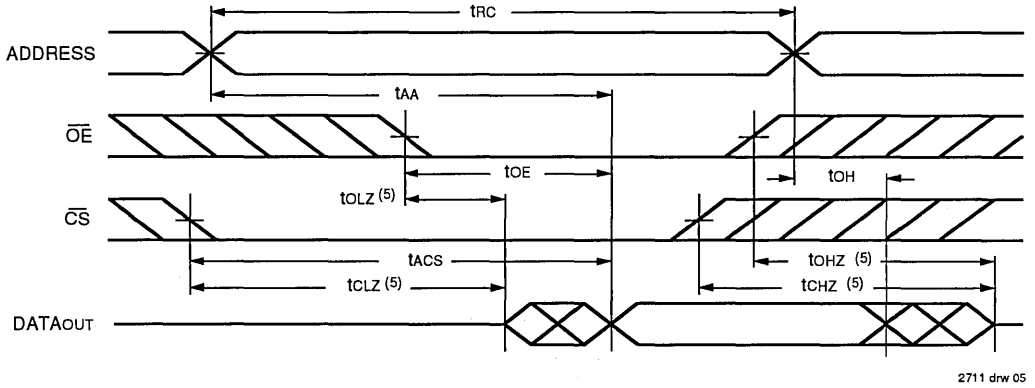
(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-35		-40		-50		-60 (Mil. Only)		-70 (Mil. Only)		-85 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	30	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	20	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	45	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	16	—	16	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

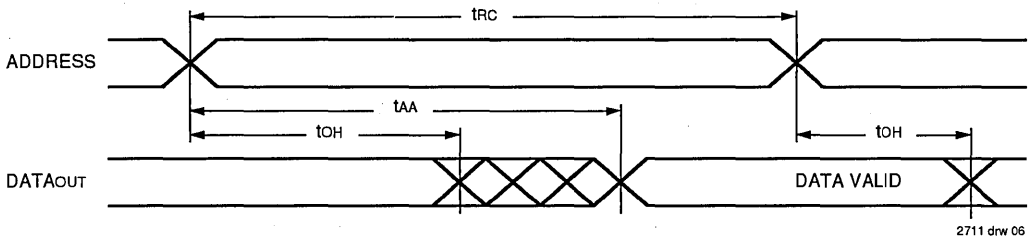
2711 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



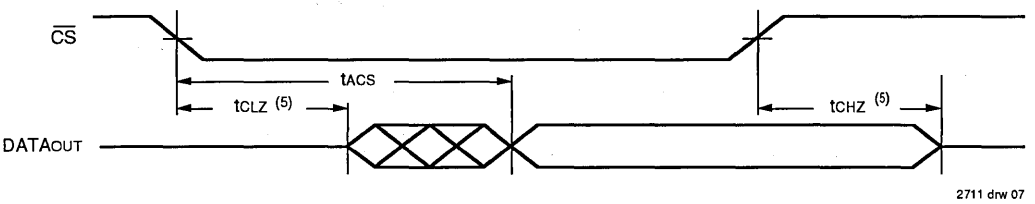
2711 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2711 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

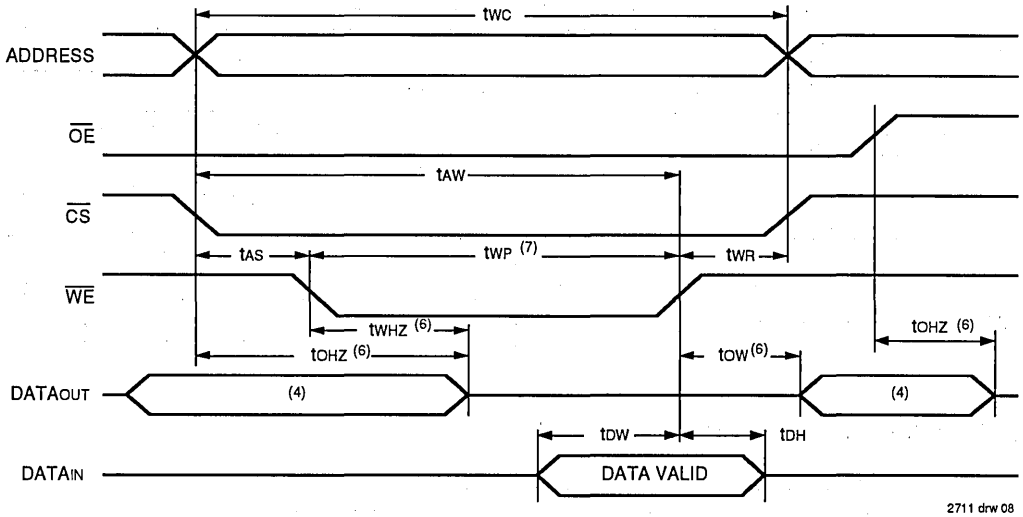


2711 drw 07

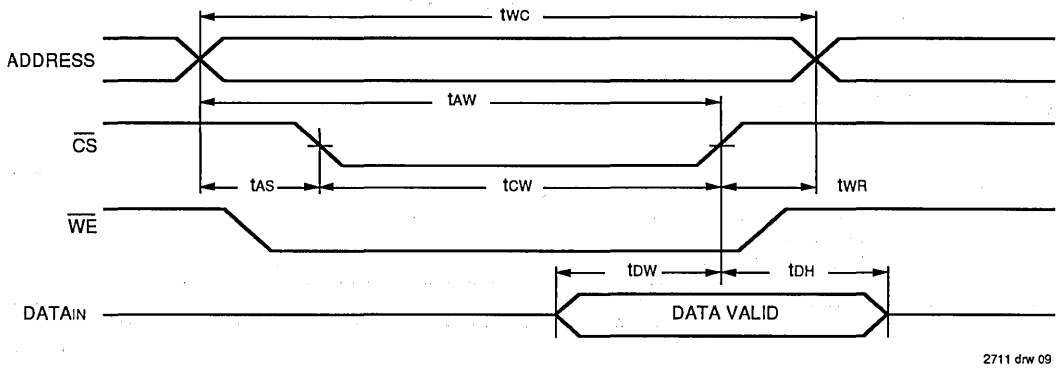
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

7

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



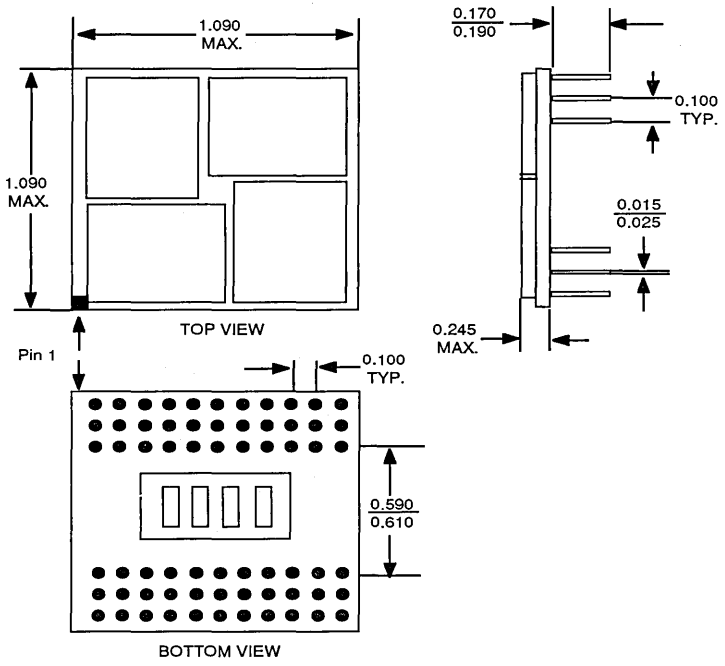
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

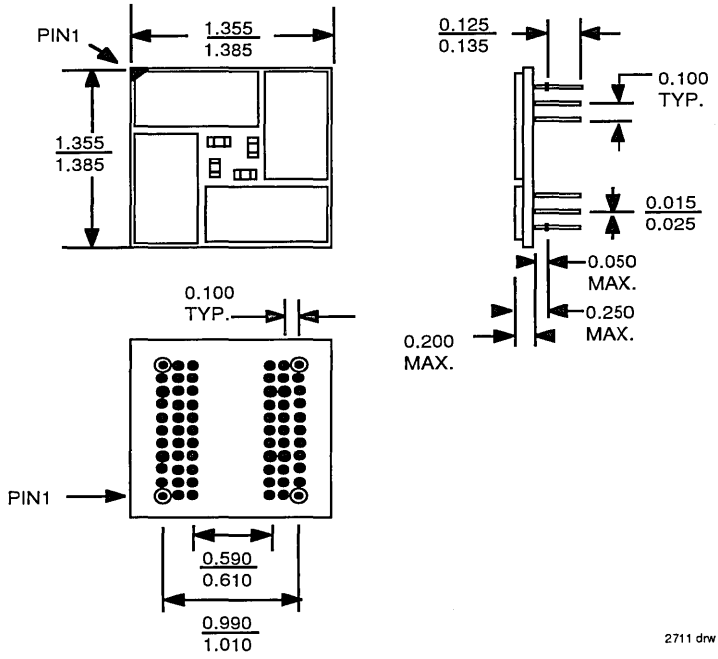
PACKAGE DIMENSIONS

7M4003SxxCHx



2711 drw 10

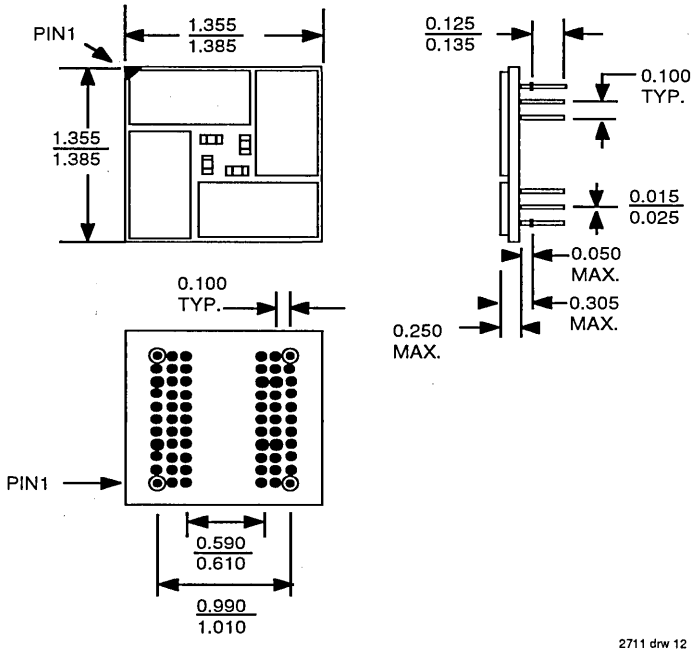
7M4013SxxCHx



2711 drw 11

7

7M4013SxxNH



2711 drw 12

Integrated Device Technology, Inc.

64K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4036

FEATURES:

- High density 2 megabit static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION[1]

		1	GND	
PD_0	2	3	PD_1	PD_0 –OPEN
I/O_0	4	5	I/O_8	PD_1 – GND
I/O_1	6	7	I/O_9	
I/O_2	8	9	I/O_{10}	
I/O_3	10	11	I/O_{11}	
V_{CC}	12	13	A_0	
A_7	14	15	A_1	
A_8	16	17	A_2	
A_9	18	19	I/O_{12}	
I/O_4	20	21	I/O_{13}	
I/O_5	22	23	I/O_{14}	
I/O_6	24	25	I/O_{15}	
I/O_7	26	27	GND	
$\overline{WE}$	28	29	A_{15}	
A_{14}	30	31	$\overline{CS_2}$	
$\overline{CS_1}$	32			
		33	$\overline{CS_4}$	
$\overline{CS_3}$	34	35	NC	
NC	36	37	$\overline{OE}$	
GND	38	39	I/O_{24}	
I/O_{16}	40	41	I/O_{25}	
I/O_{17}	42	43	I/O_{26}	
I/O_{18}	44	45	I/O_{27}	
I/O_{19}	46	47	A_3	
A_{10}	48	49	A_4	
A_{11}	50	51	A_5	
A_{12}	52	53	V_{CC}	
A_{13}	54	55	A_6	
I/O_{20}	56	57	I/O_{28}	
I/O_{21}	58	59	I/O_{29}	
I/O_{22}	60	61	I/O_{30}	
I/O_{23}	62	63	I/O_{31}	
GND	64			

2682 drw 02

ZIP, SIMM TOP VIEW

NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads Open and PD_1 reads GND, then the module had a 64K depth.

DESCRIPTION:

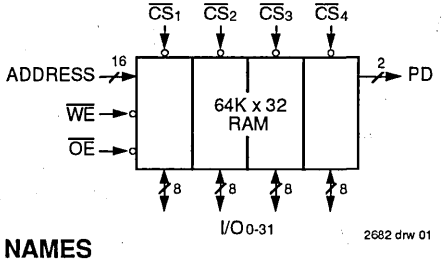
The IDT7MP4036 is a 64K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 64K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K static RAMs fabricated in IDT's high performance, high reliability CEMOS™ and BiCEMOS™ technology. The IDT7MP4036 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4036 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 64 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4036 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 64K depth.

FUNCTIONAL BLOCK DIAGRAM



2682 drw 01

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-15}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

2682 tbl 01

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COMMERCIAL TEMPERATURE RANGE **APRIL 1992**

DSC-7056/2

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	15	pF

NOTE: 2682 tbl 02
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}[2]	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES: 2682 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.
2. I/O pins must not exceed V_{CC} +0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2682 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2682 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2682 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed V_{CC} +0.5V.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2682 tbl 07

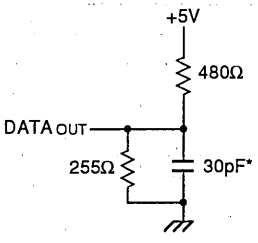
Symbol	Parameter	Test Conditions	7MP4036B 10, 12, 15, 17ns Max.	7MP4036S 20, 25, 35ns Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1520	1280	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	—	320	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	—	240	mA

2682 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2682 tbl 09



*incluces scope and jig.

Figure 1. Output Load

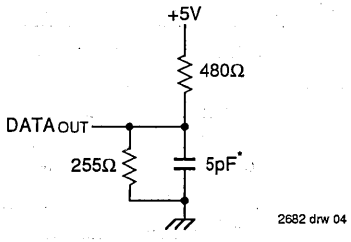


Figure 2. Output Load
(for t_{OLZ}, t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

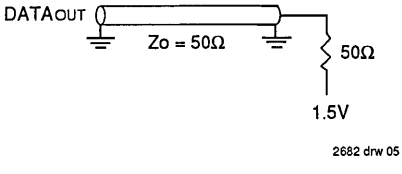


Figure 3. Alternate Output Load

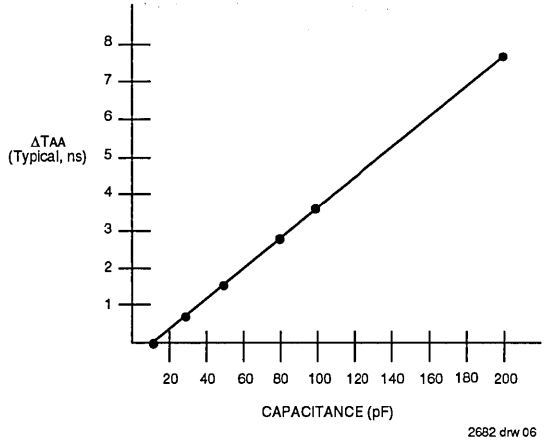


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MP4036BxxZ, 7MP4036BxxM								
		-10[2]		-12[2]		-15		-17		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	7	—	7	—	8	—	9	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	4	—	5	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	7	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	6	—	6	—	7	—	9	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:

2682 tbl 10

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

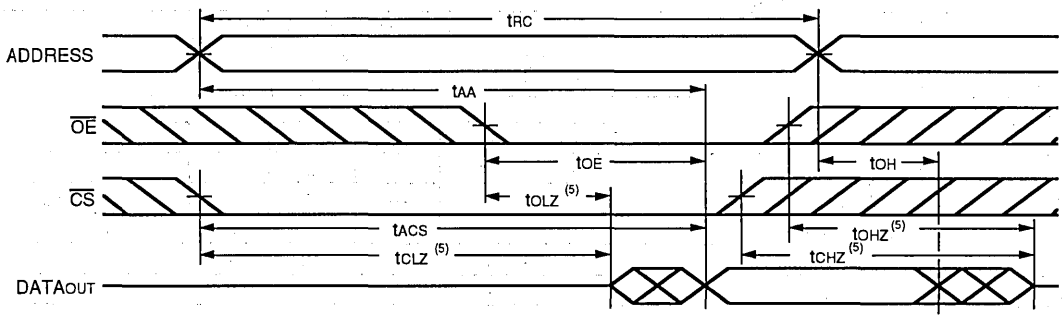
		7MP4036SxxZ, 7MP4036SxxM						
		-20		-25		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	25	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	10	—	15	—	22	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	10	—	15	—	22	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	20	—	25	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	12	—	15	—	18	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2682 tbl 11

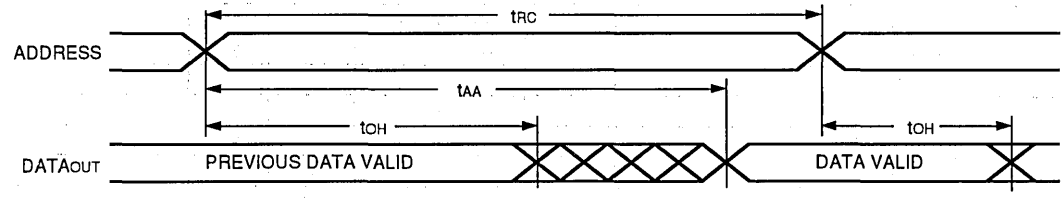
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



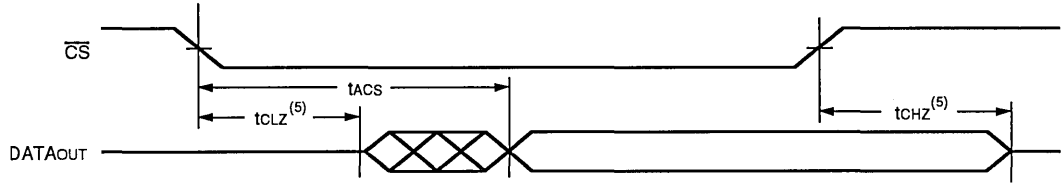
2682 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2682 drw 08

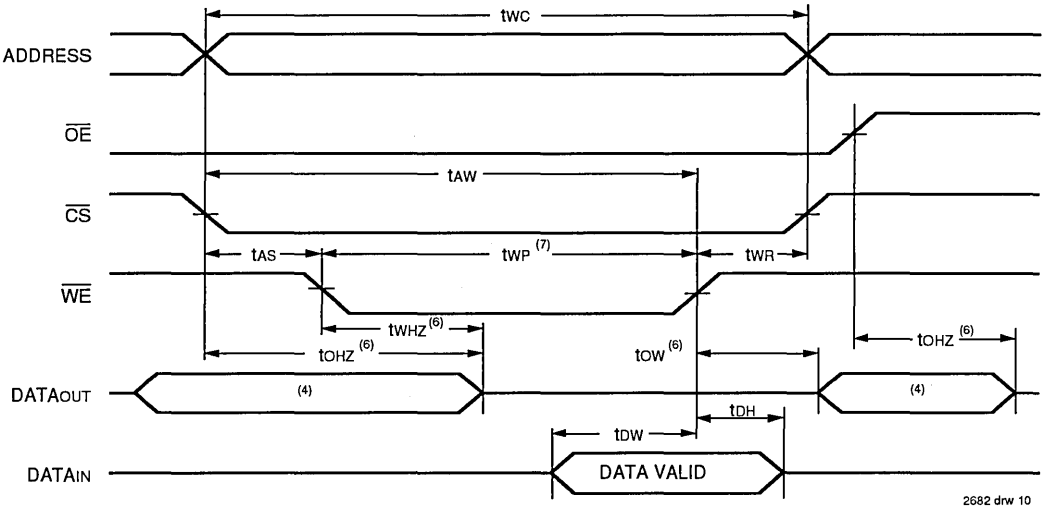
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



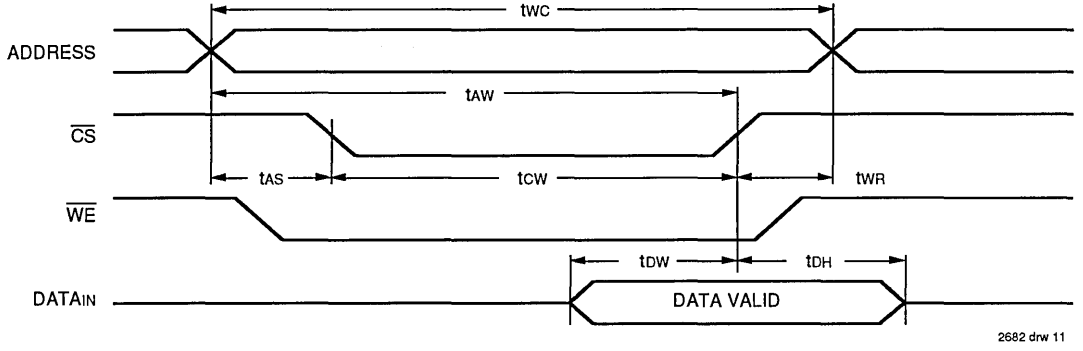
2682 drw 09

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLED TIMING)(1, 2, 3, 7)



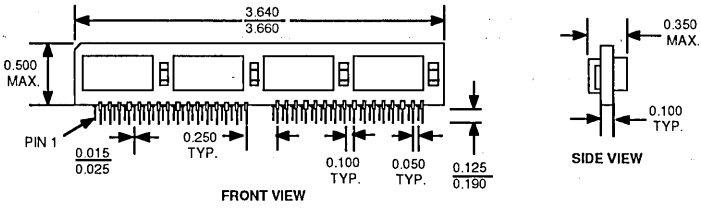
TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

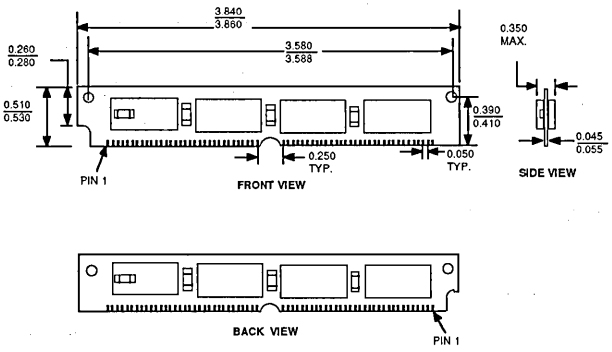
PACKAGE DIMENSIONS

ZIP VERSION



2682 drw 12

SIMM VERSION



2682 drw 13

Integrated Device Technology, Inc.

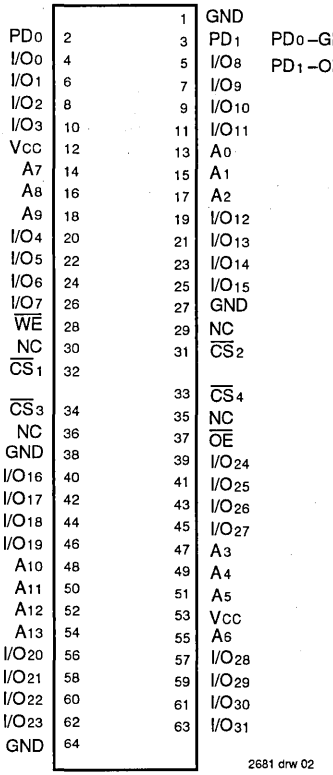
16K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4031

FEATURES:

- High density 512K static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line Package)
- Ultra-fast access time: 8ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

PIN CONFIGURATION[1]



2681 drw 02

ZIP
TOP VIEW

NOTE:
1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the depth of the module. If PD0 reads GND and PD1 reads Open, then the module has 16K depth.

DESCRIPTION:

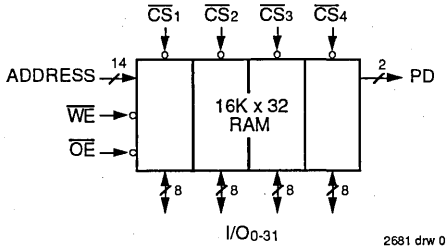
The IDT7MP4031 is a 16K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 16K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ or CEMOS™ technology. The IDT7MP4031 is available with access time as fast as 8ns with minimal power consumption.

The IDT7MP4031 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line Package). The dual row configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MP4031 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 16K depth.

FUNCTIONAL BLOCK DIAGRAM



2681 drw 01

PIN NAMES

I/O0–31	Data Input/Output
A0–13	Addresses
CS1–4	Chip Select
WE	Write Enable
OE	Output Enable
PD0–1	Depth Identification
VCC	Power
GND	Ground

2681 tbl 01

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CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	15	pF

2681 tbl 02

NOTE:
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}[2]	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2681 tbl 03

NOTES:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.
2. I/O pins must not exceed V_{CC} +0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2681 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2681 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2681 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed VCC +0.5V.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	7MP4031S Max.	7MP4031B Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	10	µA
I_{LO}	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	—	V

2681 tbl 07

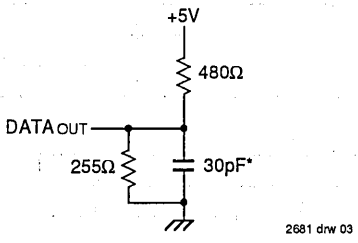
Symbol	Parameter	Test Conditions	7MP4031B 8 - 15ns Max.	7MP4031S 20 - 35ns Max.	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	1600	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max. f = f_{MAX}, Outputs Open	—	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V; f = 0, $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	—	160	mA

2681 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2681 tbl 09



*Including scope and jig.

Figure 1. Output Load

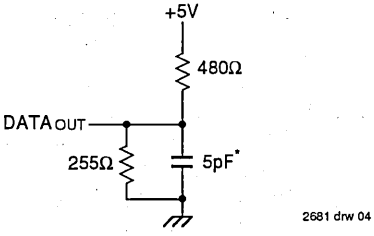


Figure 2. Output Load (for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ and tOW)

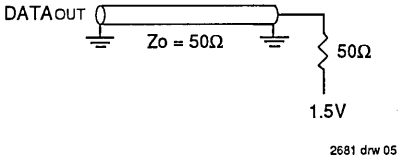


Figure 3. Alternate Output Load

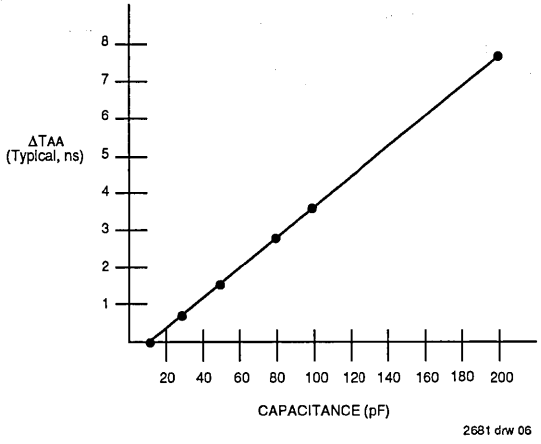


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7MP4031BxxZ						
		-8[2]		-10[2]		-12		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{ACS}	Chip Select Access Time	—	8	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	1	—	1	—	1	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	3	—	3	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	9	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	3	—	3	—	3	ns
t_{DW}	Data to Write Time Overlap	5	—	5	—	6	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns

NOTES:
1. This parameter is guaranteed, but not tested.
2. Preliminary specifications only.

2681 tbl 10

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MP4031BxxZ		7MP4031SxxZ						
		-15		-20		-25		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	7	—	8	—	10	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	14	—	17	—	20	—	30	—	ns
t_{CW}	Chip Select to End of Write	14	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	ns
t_{DW}	Data to Write Time Overlap	10	—	10	—	13	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed, but not tested.

2681 tbl 11

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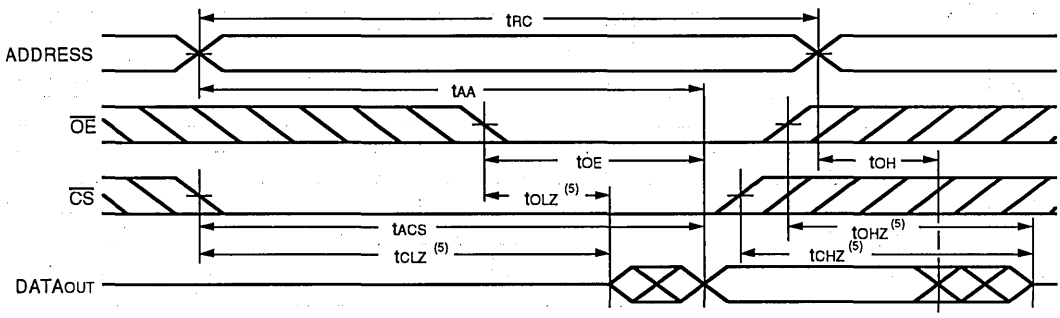
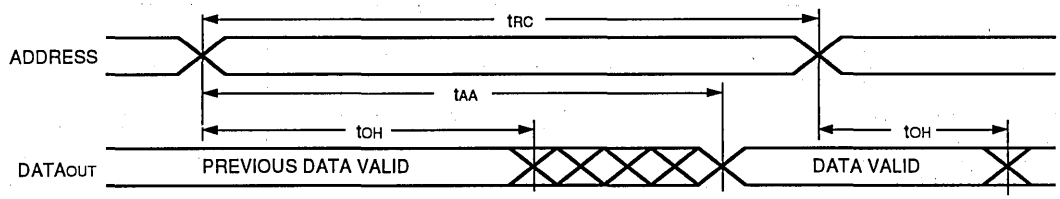
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



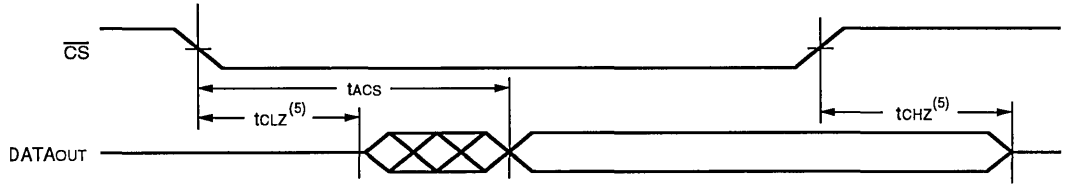
2681 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2681 drw 08

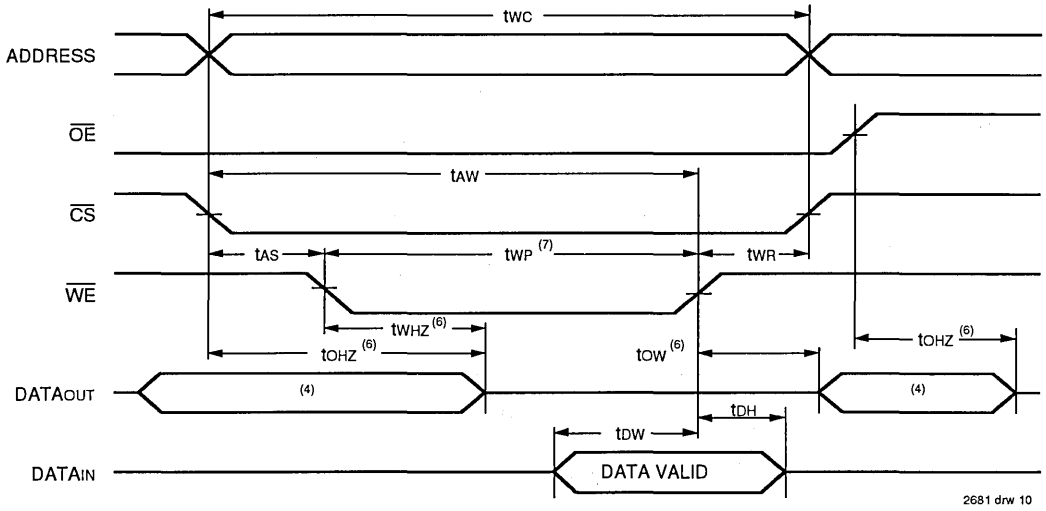
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



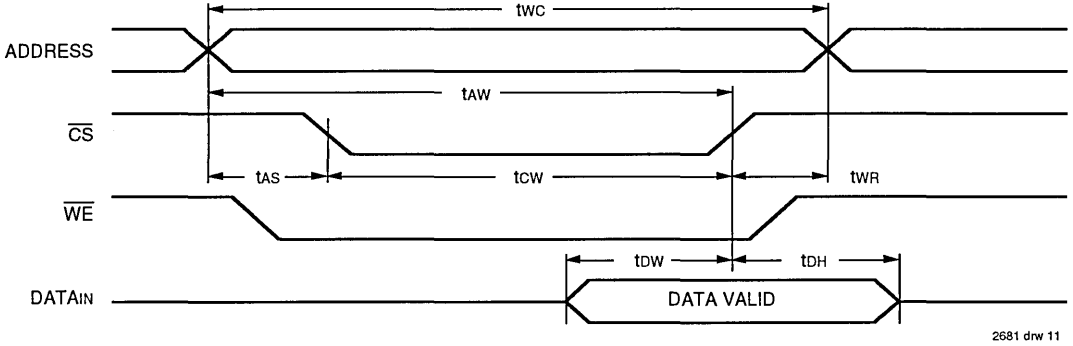
2681 drw 09

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

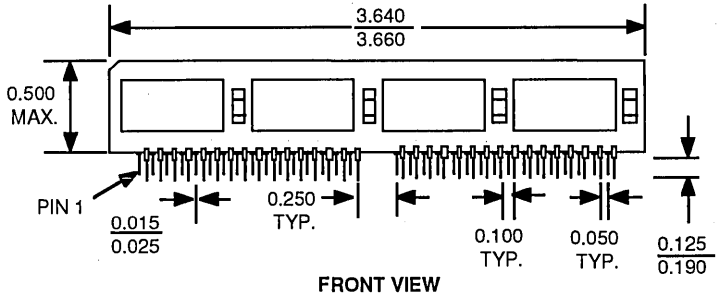


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)

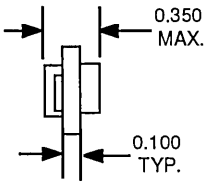


NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

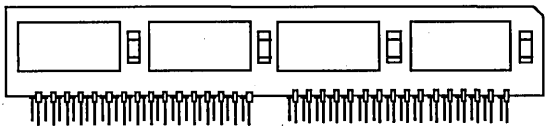
PACKAGE DIMENSIONS



FRONT VIEW



SIDE VIEW



BACK VIEW

2681 drw 12

Integrated Device Technology, Inc.

256K x 20/256K x 16 BiCMOS/CMOS STATIC RAM MODULES

PRELIMINARY
IDT7MB4065
IDT7MB4066

FEATURES:

- High density 256K x 20/256K x 16 BiCMOS/CMOS static RAM modules
- Low profile 48-pin FR-4 DIP (Dual In-line Package)
- Fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

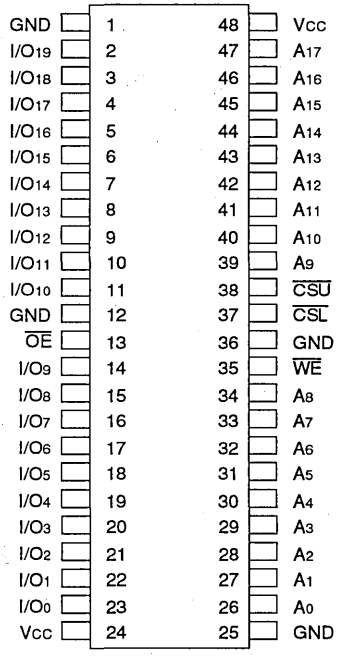
DESCRIPTION:

The IDT7MB4065/4066 are high-speed, high density 256K x 20/256K x 16 BiCMOS/CMOS static RAM modules constructed on an epoxy laminate (FR-4) substrate using either 5 256K x 4 or 4 256K x 4 static RAMs in plastic SOJ packages. The IDT7MB4065/4066 are available with access time as fast as 10ns with minimal power consumption.

The IDT7MB4065/4066 are packaged in a 48 pin FR-4 DIP (Dual In-line Package). The dual row configuration allows 48 pins to be placed on a package 2.4 inches long, 600 mils wide and 0.35 inches tall.

All inputs and outputs of the IDT7MB4065/4066 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

PIN CONFIGURATIONS[1]

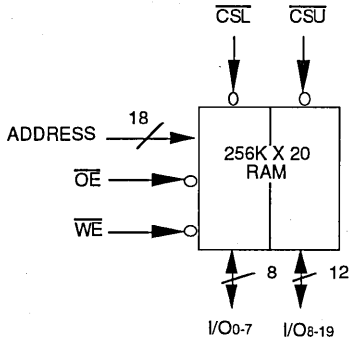


2808 drw 01

DIP
TOP VIEW

NOTE:
1. On the 7MB4066, pins 10,11,14, 15 are N.C. (No Connects).

FUNCTIONAL BLOCK DIAGRAM[1]



2808 drw 02

NOTE:
1. On the 7MB4066, there are 16 I/Os with byte access to I/Os(0-7)and I/Os(8-15).

PIN NAMES

I/O0-19	Data Inputs/Outputs
A0-17	Address
$\overline{CSL}$	Chip Select - Lower Byte
$\overline{CSU}$	Chip Select - Upper Byte
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connect
Vcc	Power
GND	Ground

2808 tbl 01

7

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Comm.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2808 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	Hi-Z	Standby
Read	L	L	H	Dout	Active
Write	L	X	L	Din	Active
Read	L	H	H	Hi-Z	Active

2808 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5 (1)	—	0.8	V

NOTE: 2808 tbl 04

1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2808 tbl 05

CAPACITANCE

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter (1)	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance	V_{IN} = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	42	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2808 tbl 06

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2808 tbl 07

Symbol	Parameter	Test Conditions	7MB4065		7MB4066		Unit
			10 - 17ns(1) Max.	20 - 45ns Max.	10 - 17ns(1) Max.	20 - 45ns Max.	
I_{CC}	Dymanic Operating Current	f = f_{MAX}(2); CS = V_{IL} V_{CC} = Max.; Output Open	1000	750	800	600	mA
I_{SB}	Standby Supply Current	CS ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}(2)	300	300	240	240	mA
I_{SB1}	Full Standby Supply Current	CS ≥ V_{CC} – 0.2V; F = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V, f = 0	200	50	160	40	mA

NOTES: 2808 tbl 08

1. Preliminary specifications only.
2. f_{MAX} = 1/t_{RC}

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2808 tbl 09

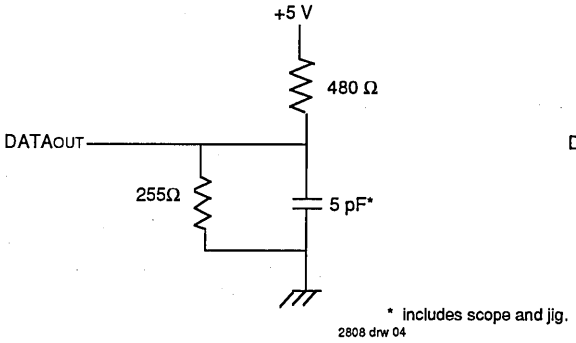


Figure 1. Output Load

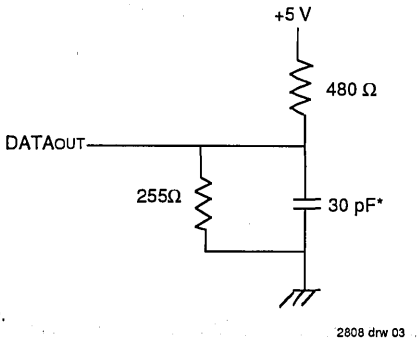


Figure 2. Output Load
(for t_{OLZ}, t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MB4065/4066SxxP								
		-10[2]		-12[2]		-15[2]		-17[2]		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	4	—	4	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	8	—	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	5	—	6	—	8	—	10	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2808 tbl 10

7

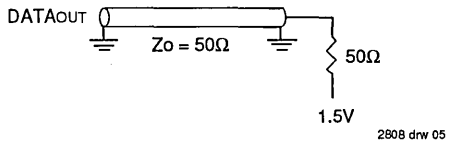


Figure 3. Alternate Output Load

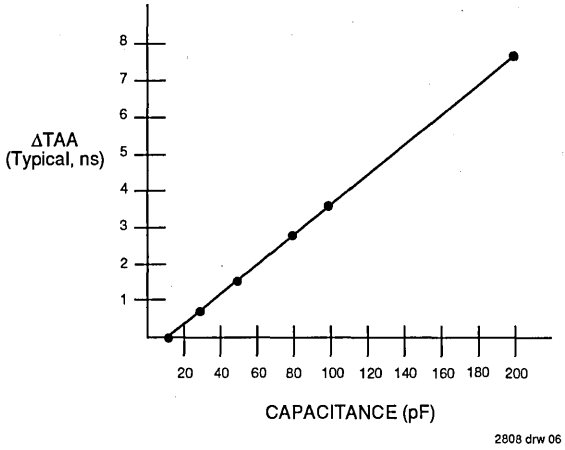


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

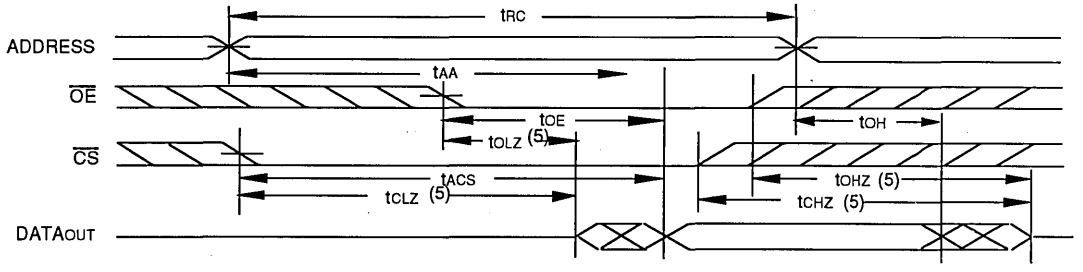
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4065/4066SxxP										
		-20		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{CW}	Chip Selection to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW} [1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

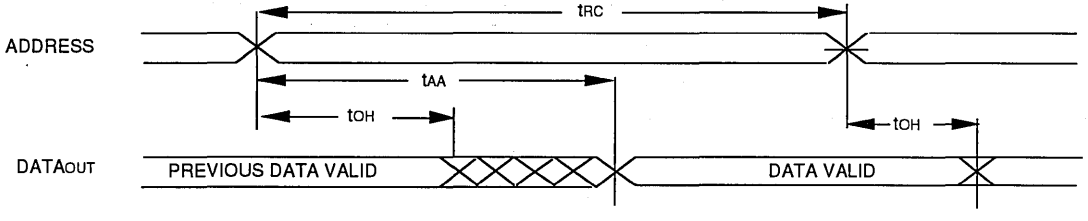
2808 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



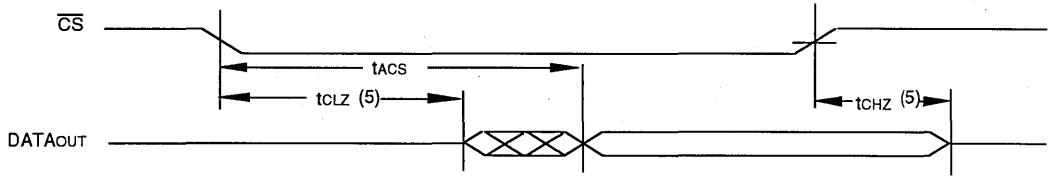
2808 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2,4)



2808 drw 08

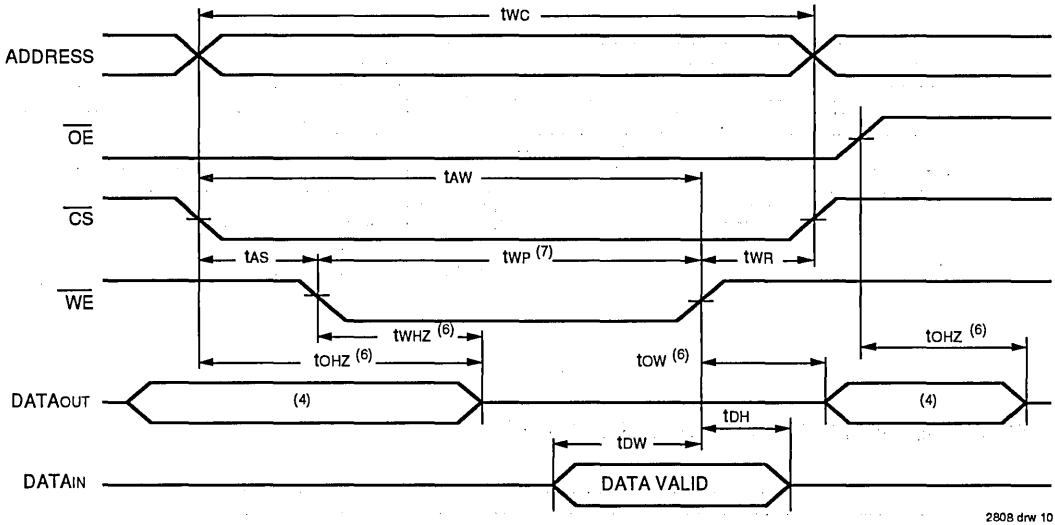
TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3,4)



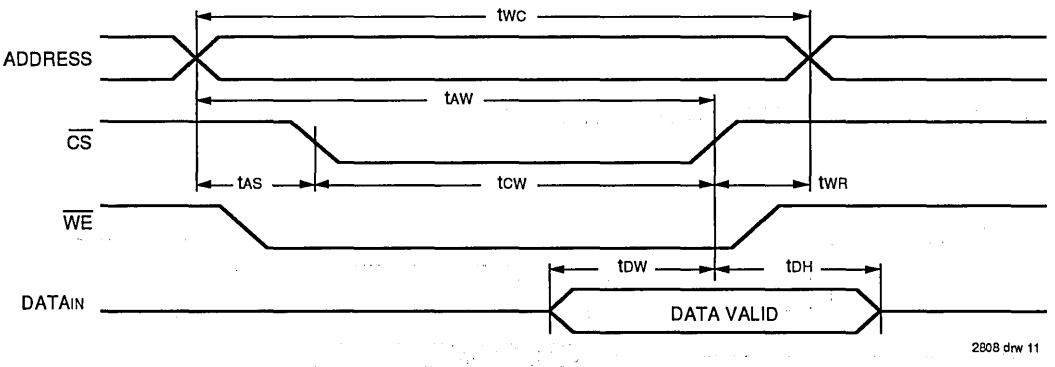
2808 drw 09

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



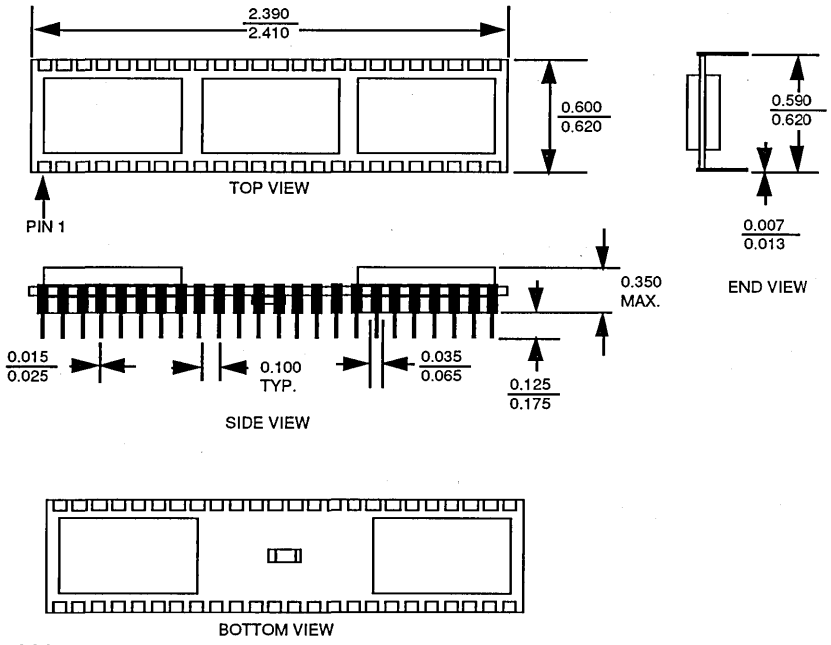
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must High during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twp is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, so input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. Transition is measured ±200 mV from steady state. This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the wirte pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

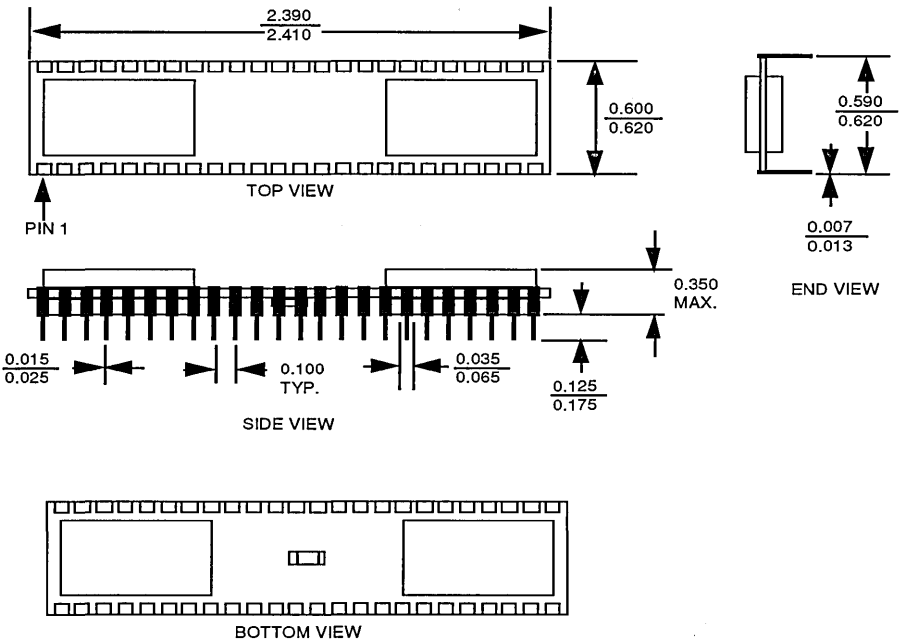
PACKAGE DIMENSIONS

7MB4065



2080 drw 12

7MB4066



2080 drw 13

7

Integrated Device Technology, Inc.

512K/256K x 16 CMOS STATIC RAM MODULE

IDT7MP4047
IDT7MP4046

FEATURES:

- High-speed 8/4 megabit (pin compatible) CMOS static RAM modules
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 220mA max.
  - — CMOS Standby: 850µA max.
  - — Data retention: 450µA max. (Vcc= 2V)
- Surface mounted small outline plastic packages on a 45 pin FR-4 SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

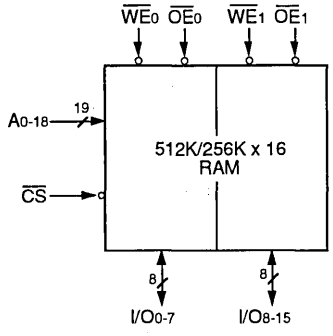
DESCRIPTION:

The IDT7MP4047/4046 is a 512K/256K x 16 CMOS static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using eight or four 128K x 8 static RAMs in small outline plastic packages and a one-of-four decoder. Availability of two Write Enables and two Output Enables provides byte access and output control flexibility. The IDT7MP4047/4046 is available with access times as fast as 70ns with a maximum operating current of 220mA. For battery backup applications, a very low data retention current is available.

The IDT7MP4047/4046 is packaged in a 45 pin FR-4 SIP (Single In-line Package). This results is a package 4.6 inches in length and less than 0.2 inches in thickness.

All inputs and outputs of the IDT7MP4047/4046 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

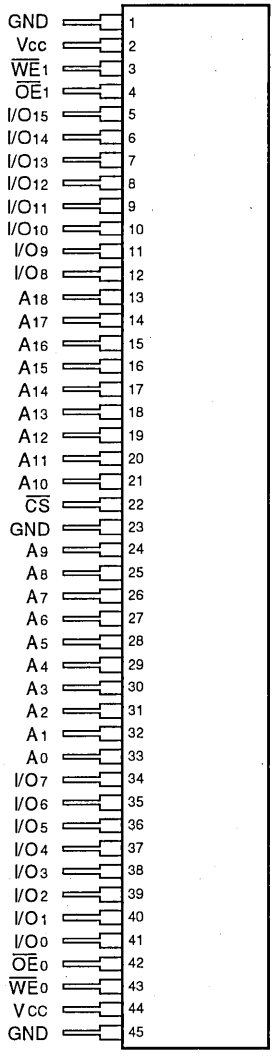
FUNCTIONAL BLOCK DIAGRAM



2754 drw 01

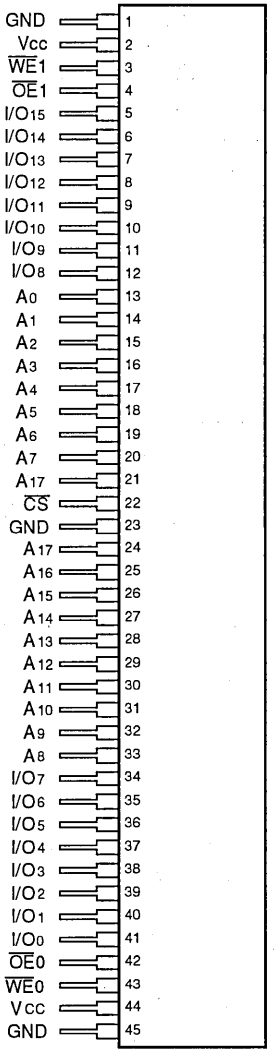
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION — 7MP4047



2754 drw 02

PIN CONFIGURATION[1] — 7MP4046



SIP
FRONT VIEW

2754 drw 03

NOTE:
1. For proper operation of the 7MP4046 module, pins 21 and 24 must be tied together.

PIN NAMES - 7MP4047

I/O_0–I/O_{15}	Data Inputs/Outputs
A_0–A_{18}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

2754 tbl 03

PIN NAMES - 7MP4046

I/O_0–I/O_{15}	Data Inputs/Outputs
A_0–A_{17}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}_{0-1}$	Write Enables
$\overline{OE}_{0-1}$	Output Enables
Vcc	Power
GND	Ground

2754 tbl 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
2754 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

2754 tbl 06

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
2754 tbl 07

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

2754 tbl 08

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	7MP4046 Max.	7MP4047 Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	220	220	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Ouput Open	—	12	24	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	—	450	850	µA

2754 tbl 09

DATA RETENTION CHARACTERISTICS

(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	7MP4046/4047 Max. @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} - 0.2V	—	250/450	µA
t_{CDR}(2)	Chip Deselect to Data Retention Time	V_{IN} ≤ V_{CC} - 0.2V	0	—	ns
t_R(2)	Operation Recovery Time	V_{IN} ≥ - 0.2V	t_{RC}(1)	—	ns

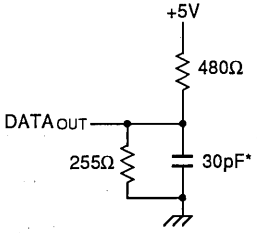
NOTES:
2754 tbl 10

1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.

AC TEST CONDITIONS

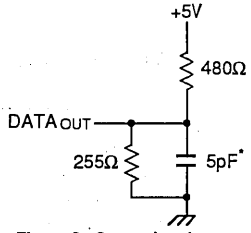
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2754 tbl 11



2754 drw 04

Figure 1. Output Load



2754 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP4046/4047LxxS								
		-70		-85		-100		-120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	85	—	100	—	ns
t_{DS}	Data Set-up Time	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	30	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2754 tbl 12

7

CAPACITANCE[1] - 7MP4047

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

2754 tbl 01

NOTE:
1. This parameter is guaranteed by design, but not tested.

CAPACITANCE[1] - 7MP4046

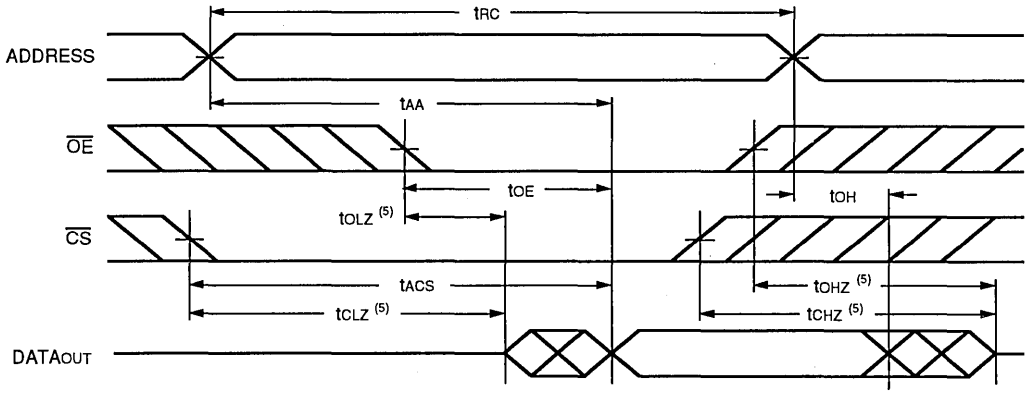
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	30	pF
$C_{IN(C)}$	Input Capacitance($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

2754 tbl 02

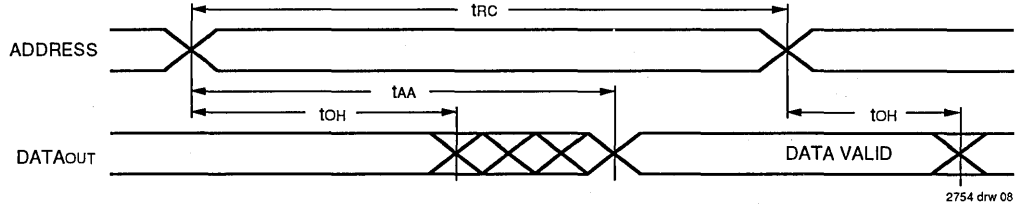
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



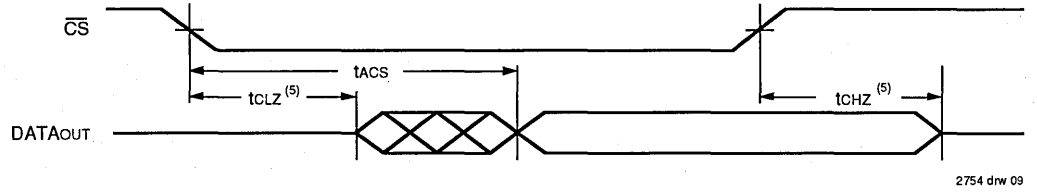
2754 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2754 drw 08

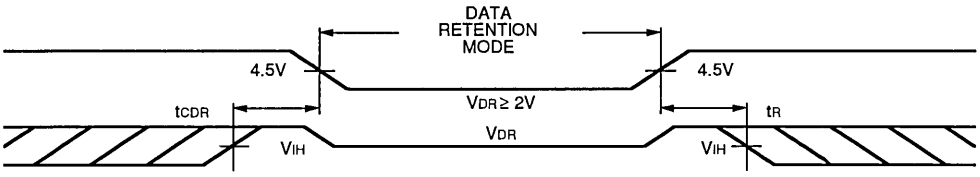
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



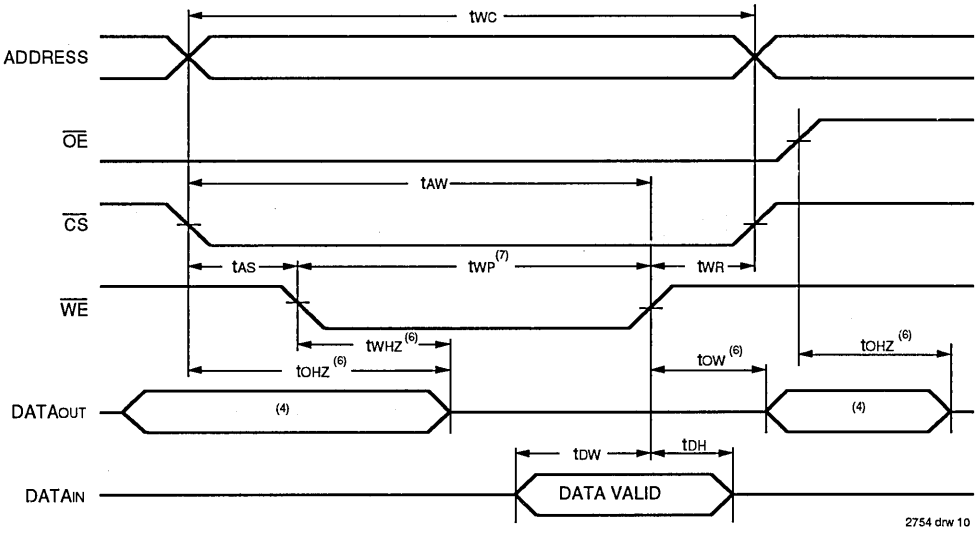
2754 drw 09

NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed, but not tested.

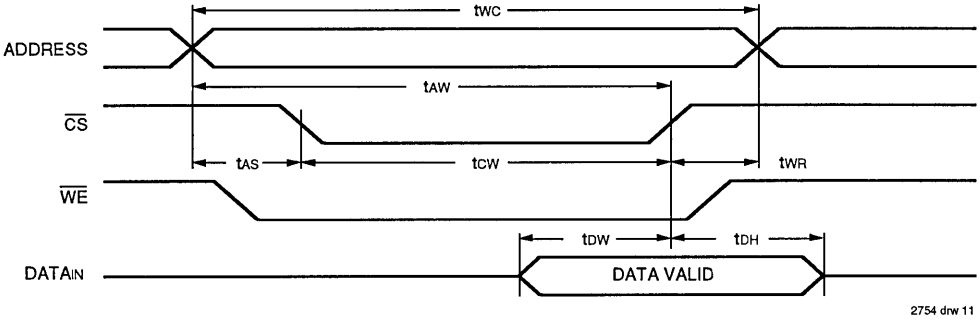
DATA RETENTION WAVEFORM



TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



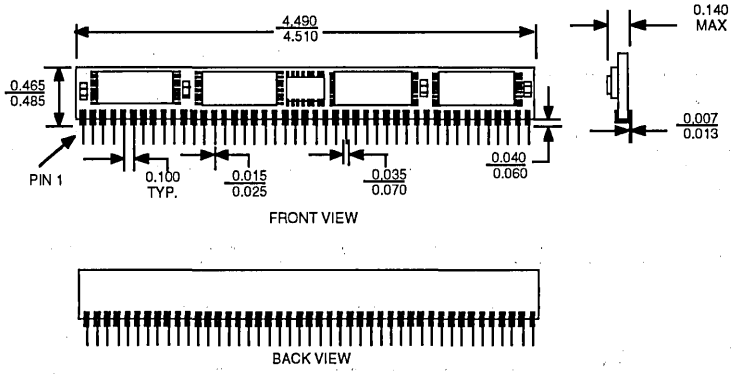
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).. This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tWD. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

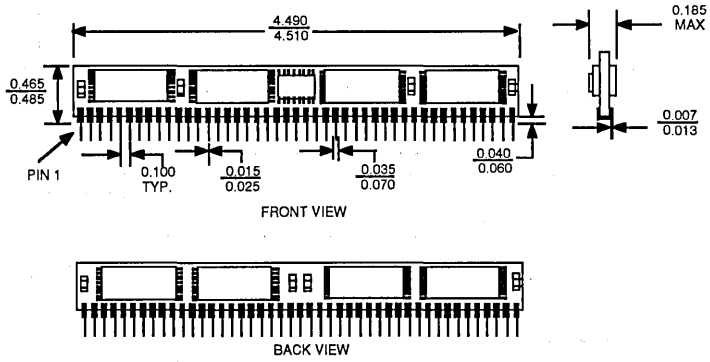
PACKAGE DIMENSIONS

7MP4046



2754 drw 12

7MP4047



2754 drw 13

Integrated Device Technology, Inc.

64K x 16 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4027

FEATURES:

- High density 1 megabit static RAM module
- Low profile 40 pin DSIP (Dual Single In-line vertical Package)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

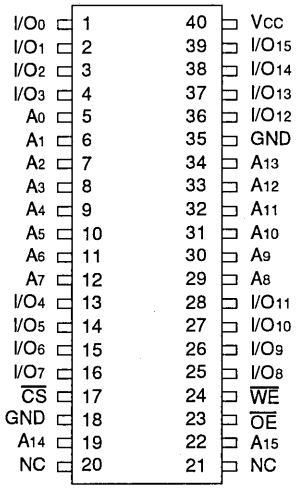
DESCRIPTION:

The IDT7MP4027 is a 64K x 16 static RAM module constructed on an epoxy laminate (FR-4) substrate using 4 64K x 4 static RAMs in plastic SOJ packages. The IDT7MP4027 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4027 is packaged in a 40 pin DSIP (Dual Single In-line vertical Package). This configuration allows 40 pins to be placed on a package 2 inches long, 0.35 inches thick and 0.5 inches tall.

All inputs and outputs of the IDT7MP4027 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

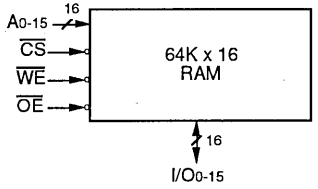
PIN CONFIGURATION



2843 drw 01

DSIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



2843 drw 02

PIN NAMES

A0-15	Addresses
I/O0-15	Data Inputs/Outputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
NC	No Connect
VCC	Power
GND	Ground

2843 tbl 01

7

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CAPACITANCE (T_A = +25°C, F = 1.0MHZ)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Data I/O Capacitance	$V_{(IN)}$ = 0V	15	pF
C_{IN}	Input Capacitance (Address and Control)	$V_{(IN)}$ = 0V	40	pF

2843 tbl 02

NOTE:
1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2843 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2843 tbl 03

NOTE:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2843 tbl 06

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2843 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max.; V_{IN} = GND to V_{CC} (Address and Control)	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2843 tbl 07

Symbol	Parameter	Test Conditions	7MP4027B Max.	7MP4027S Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; CS = V_{IL} V_{CC} = Max.; Output Open	720	640	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max. Outputs Open, f = f_{MAX}	—	160	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V; f = 0 $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	—	120	mA

2843 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2843 tbl 09

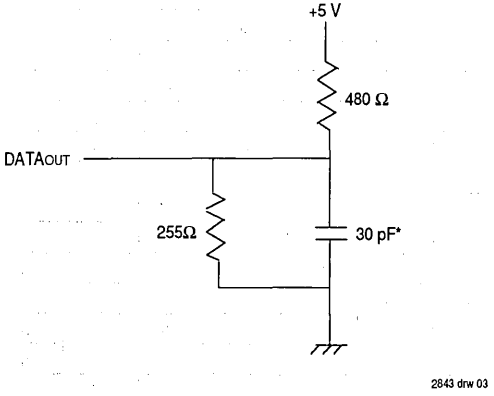


Figure 1. Output Load.

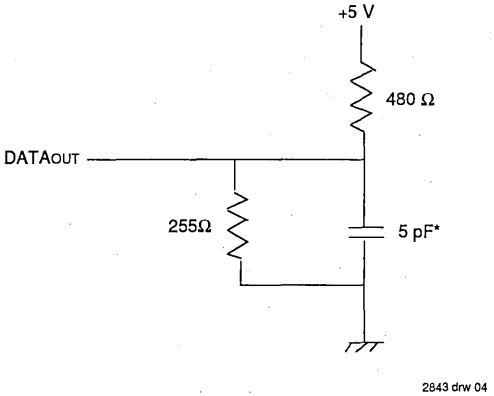


Figure 2. Output Load (for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW)

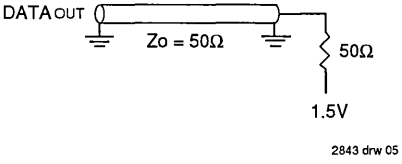


Figure 3. Alternate Output Load.

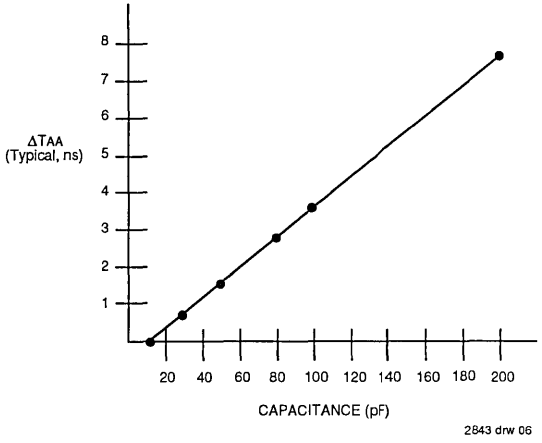


Figure 4. Alternate Lumped Capacitive Load, Typical Derating.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

		7MP4027BxxV								
		-10[2]		-12[2]		-15		-17		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	4	—	5	—	6	—	8	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	5	—	6	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	7	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	4	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	4	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:

2843 tbl 10

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

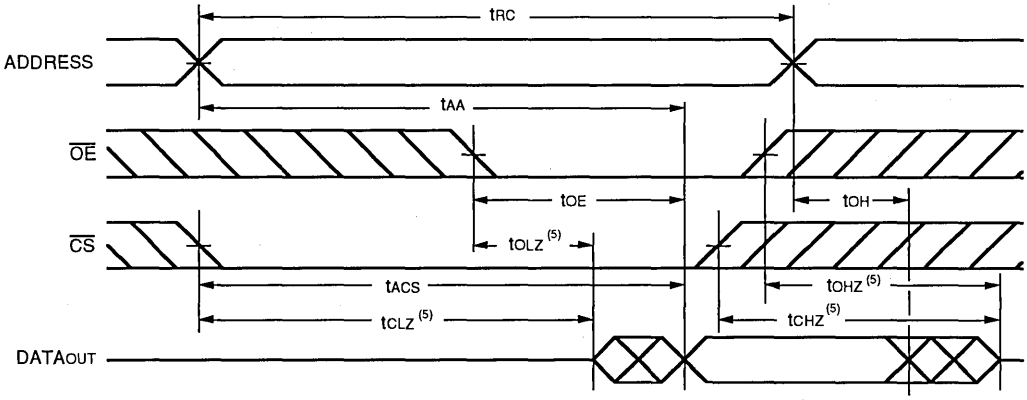
		7MP4027SxxV								
		-20		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	4	—	4	—	4	—	4	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	12	—	15	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	15	—	20	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	15	—	20	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	15	—	20	—	20	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2843 tbl 11

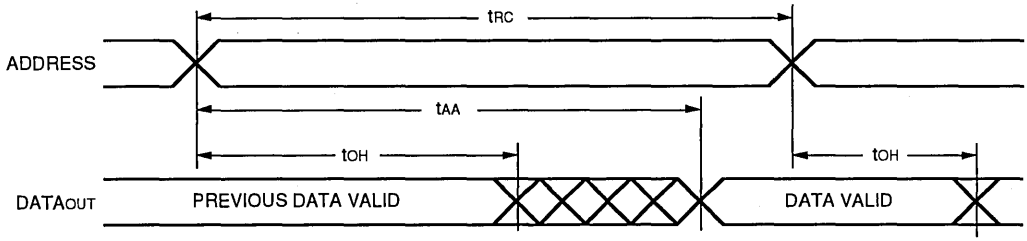
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



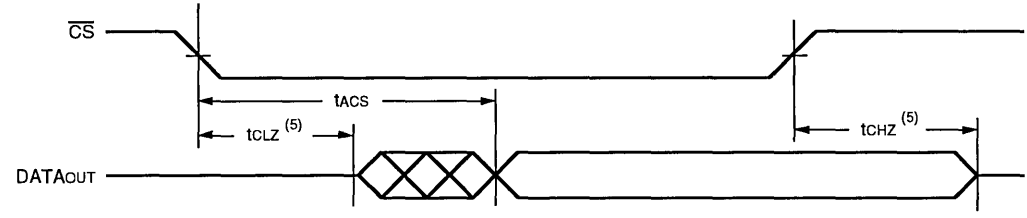
2843 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2843 drw 08

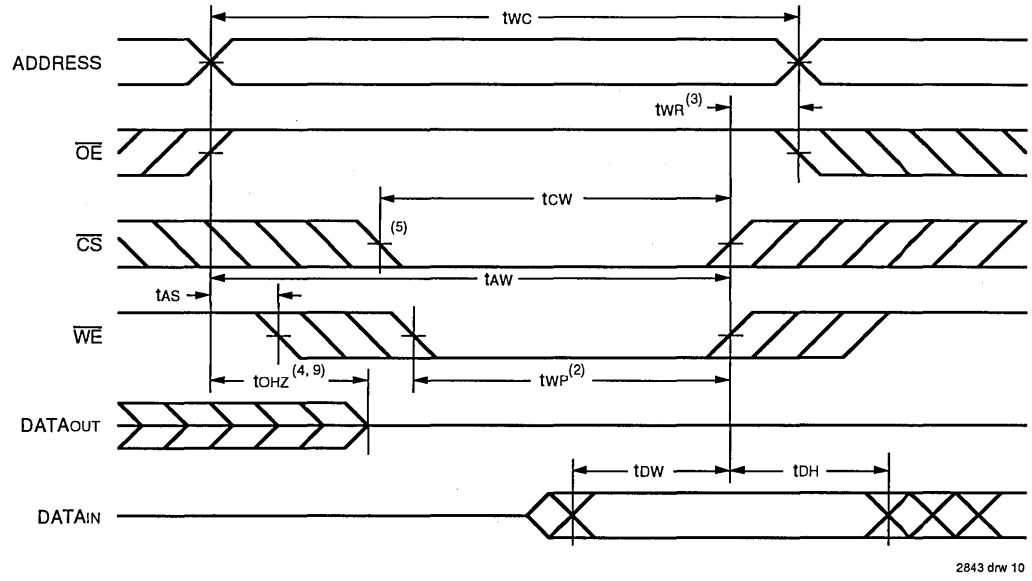
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



2843 drw 09

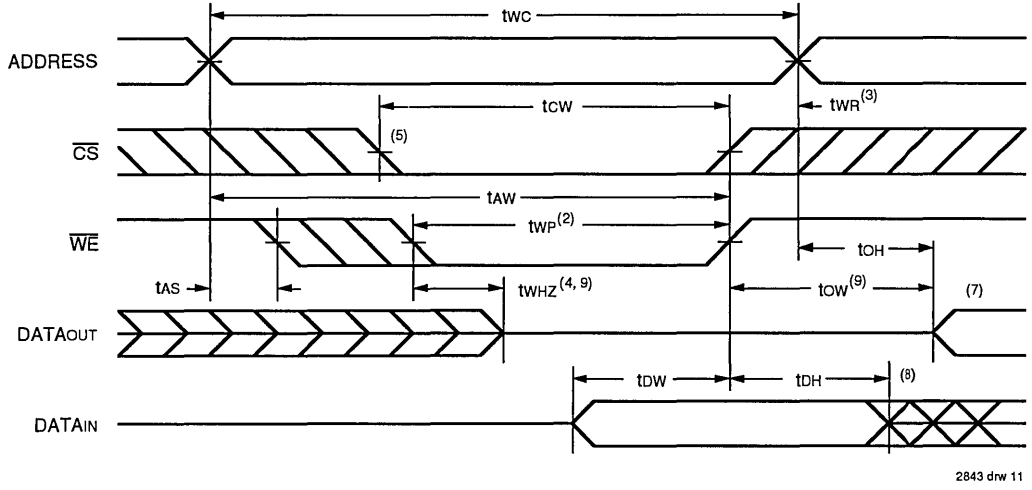
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2843 drw 10

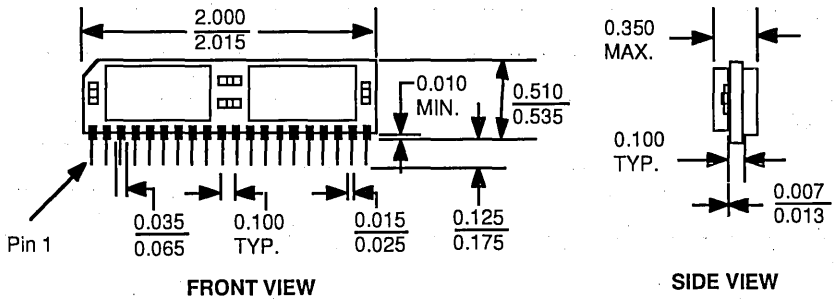
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2843 drw 11

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



FRONT VIEW

SIDE VIEW

2843 drw 12

Integrated Device Technology, Inc.

256K x 9 CMOS STATIC RAM MODULE

IDT7MB4040

FEATURES

- High density separate I/O, 2 megabit (256K x 9) static RAM module
- Low profile 44 pin, 600 mil DIP
- Fast access time: 10ns (max.)
- Surface mounted plastic SOJ packages on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins for maximum noise immunity
- Inputs/outputs directly TTL compatible

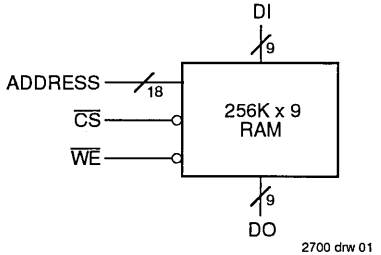
DESCRIPTION

The IDT7MB4040 is a separate I/O, 9 bit wide 2 megabit static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using 9 256K x 1 static RAMs in plastic SOJ packages. The IDT7MB4040 is available with access times as fast as 10ns with minimal power consumption.

The IDT7MB4040 is packaged in a 44 pin FR-4 DIP. The memory configuration results in a package 3.4 inches long, 600 mils wide, and only 350 mils in height. Provision of a ninth bit results in a optimal package for high reliability applications where parity is a must.

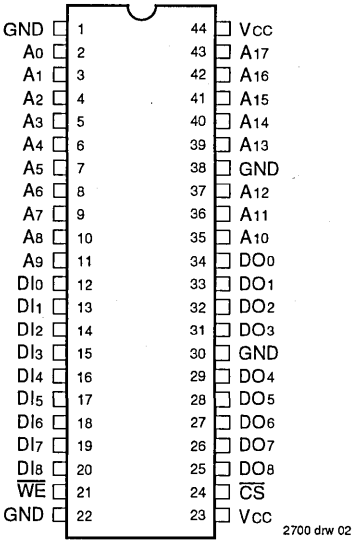
All inputs and outputs of the IDT7MB4040 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



2700 drw 01

PIN CONFIGURATION



2700 drw 02

DIP
TOP VIEW

7

PIN NAMES

DI_0–DI_8	Data Inputs
DO_0–DO_8	Data Outputs
A_0–A_{17}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

2700 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High-Z	Active

2700 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2700 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	75	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE: 2700 tbl 04

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	5.8	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2700 tbl 05

1. V_{IL} = -2.0V for pulse width less than 15ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2700 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	45	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2700 tbl 07

Symbol	Parameter	Test Conditions	10ns, 12ns Max.	15-35ns Max.	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ Outputs Open, f = f_{MAX}.	1710	1350	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}.	630	360	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V, f=0 $V_{IN} \geq V_{CC}$ – 0.2V or ≤ 0.2V	270	270	mA

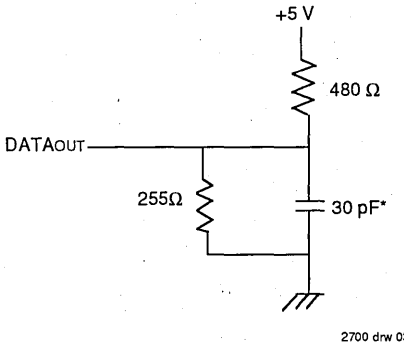
NOTE:
1. 10ns, 12ns are preliminary specifications.

2700 tbl 08

AC TEST CONDITIONS

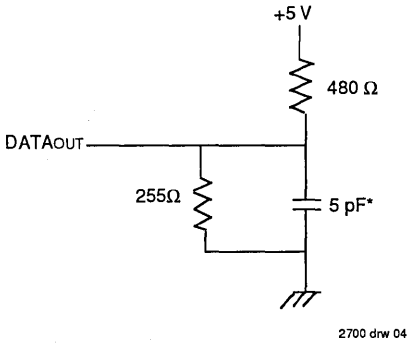
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2700 tbl 09



2700 drw 03

Figure 1. Output Load



2700 drw 04

Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OW})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS[2] (V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4040SxxP								Unit
		-10		-12		-15		-17		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	—	17	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Selection to End of Write	8	—	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	6	—	7	—	8	—	9	ns
t_{DW}	Data to Write Time Overlap	8	—	9	—	10	—	11	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. 10ns, 12ns are preliminary specifications.

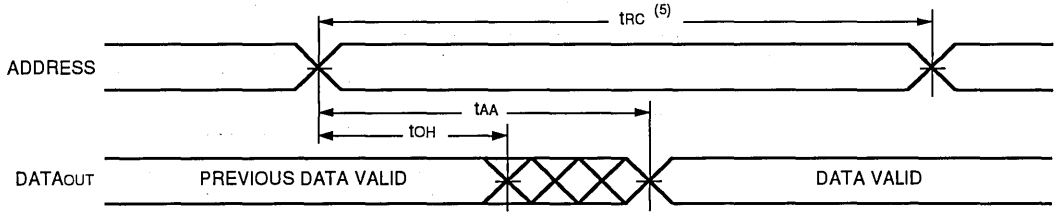
2700 tbl 10

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MB4040SxxP -20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	10	—	13	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	20	—	25	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{CW}	Chip Selection to End of Write	17	—	22	—	30	—	ns
t_{AW}	Address Valid to End of Write	17	—	22	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	17	—	22	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Ouput in High Z	—	10	—	13	—	20	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	0	—	5	—	5	—	ns

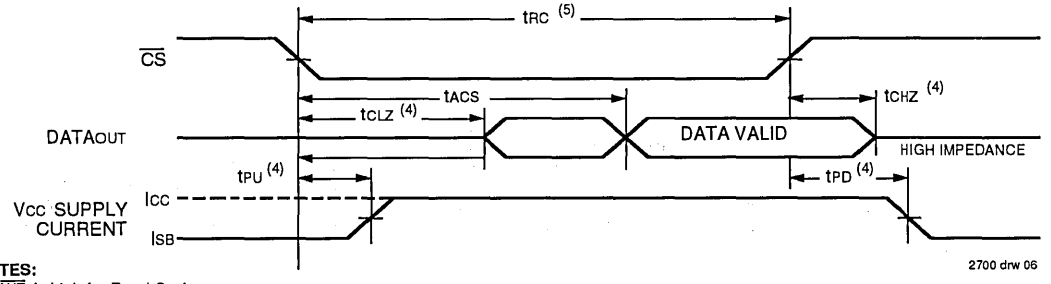
2700 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)

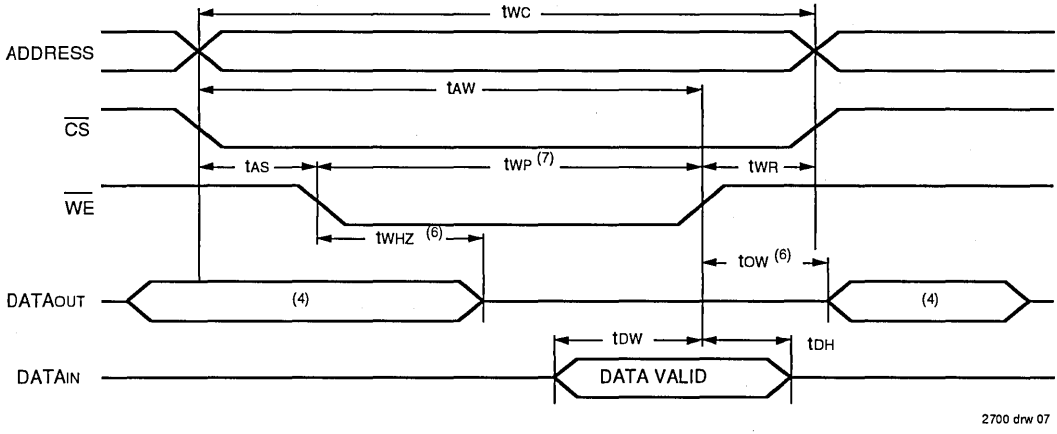
2700 drw 05



2700 drw 06

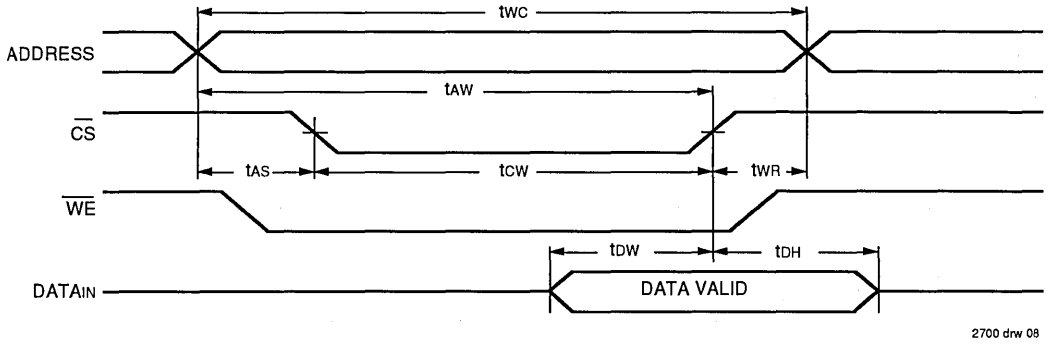
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. $\overline{CS}$ is low for Read Cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading on Figure 2. This parameter is guaranteed by design, but not tested.
5. All Read Cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



2700 drw 07

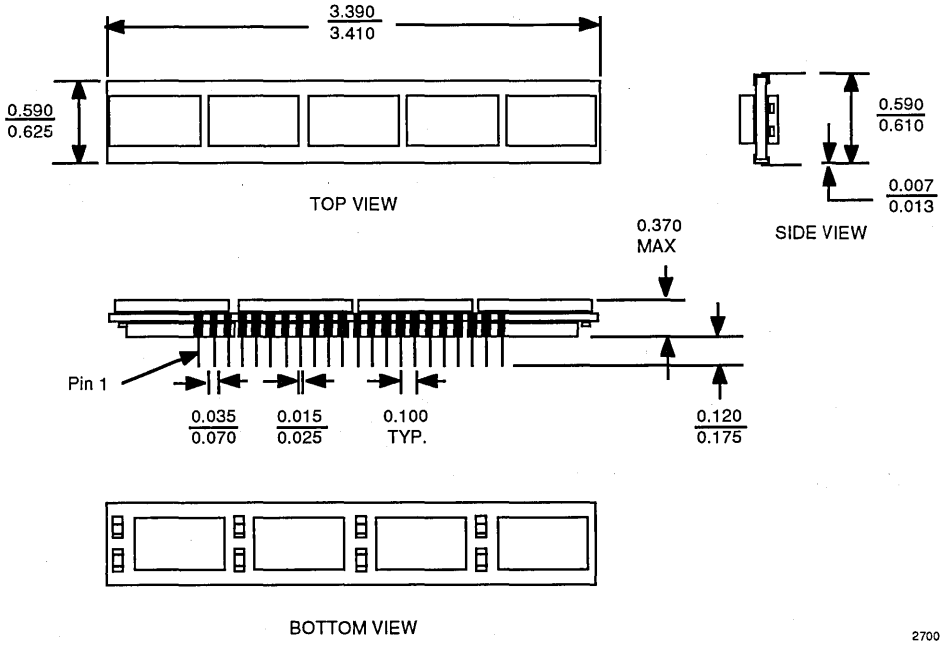
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



2700 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

PACKAGE DIMENSIONS



2700 drw 09

7

Integrated Device Technology, Inc.

2M x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MB4084

FEATURES:

- High density 16 megabit (2M x 8) static RAM module
- Equivalent to the JEDEC standard for future monolithic
- Fast access time: 55ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 36-pin, 600 mil FR-4 DIP (Dual-In-Line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

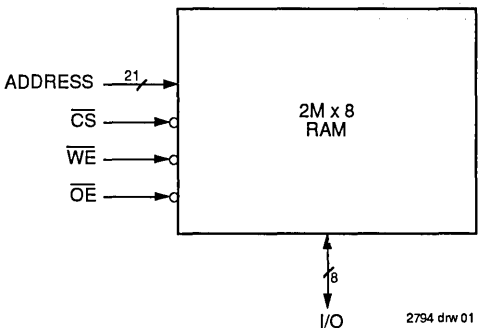
DESCRIPTION:

The IDT7MB4084 is a 16megabit (2M x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 512K x 8 static RAMs and a decoder. The IDT7MB4084 is available with access times as fast as 55ns, and a data retention current of 250µA and a standby current of 450µA.

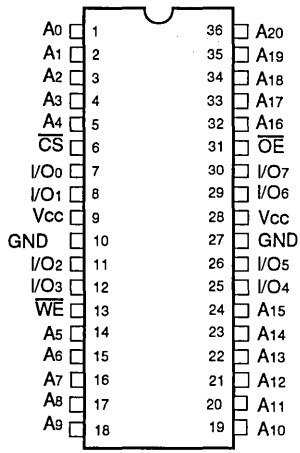
The IDT7MB4084 is packaged in a 36-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.8 inches long and 0.6 inches wide.

All inputs and outputs of the7MB4084 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP
TOP VIEW 2794 drw 02

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-20	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2794 tbl 01

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2794 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2794 tbl 03

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2794 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2794 tbl 04

1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2794 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4084LxxP		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V	—	450	µA

2794 tbl 07

7

DATA RETENTION CHARACTERISTICS

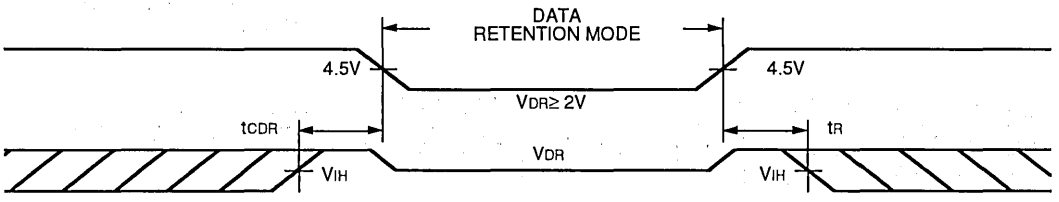
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. Vcc @ 2.0V	Unit
V_{DR}	Vcc for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}(2)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(2)	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}(1)	—	ns

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.

2794 tbl 08

DATA RETENTION WAVEFORM

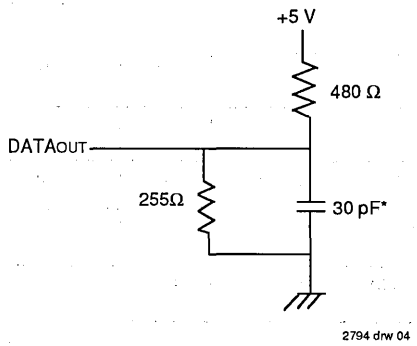


2794 drw 03

AC TEST CONDITIONS

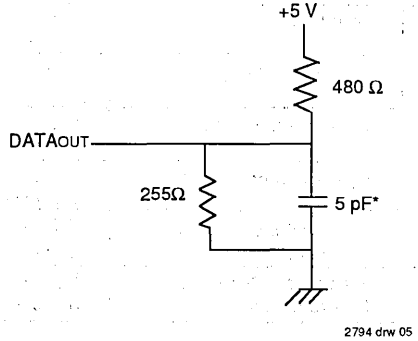
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2794 tbl 09



2794 drw 04

Figure 1. Output Load



2794 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS[2]

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4084LxxP										Unit
		-55		-70		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	30	—	45	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	30	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	55	—	70	—	85	—	100	—	120	ns
Write Cycle												
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	50	—	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	65	—	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	20	—	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	20	—	30	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	5	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2794 tbl 10

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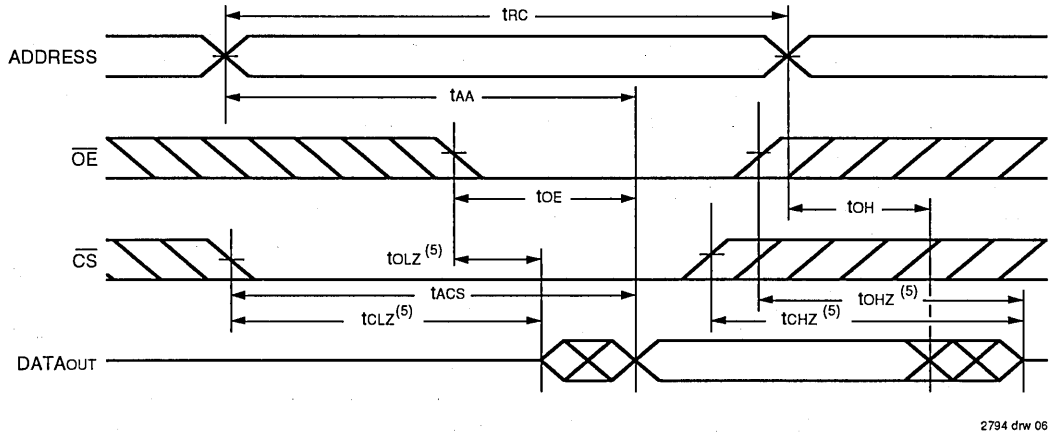
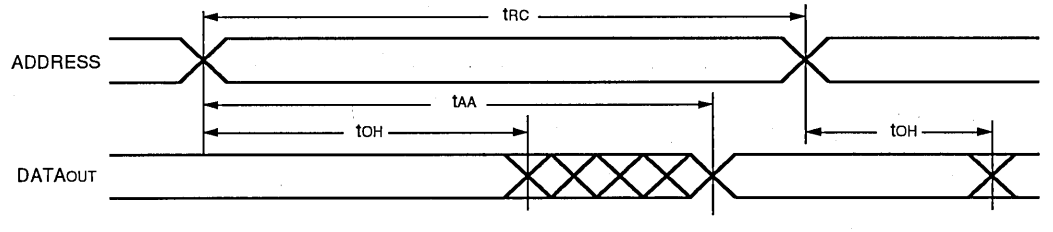
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



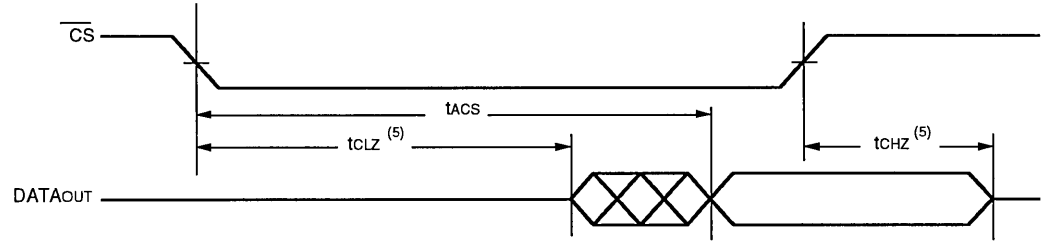
2794 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2794 drw 07

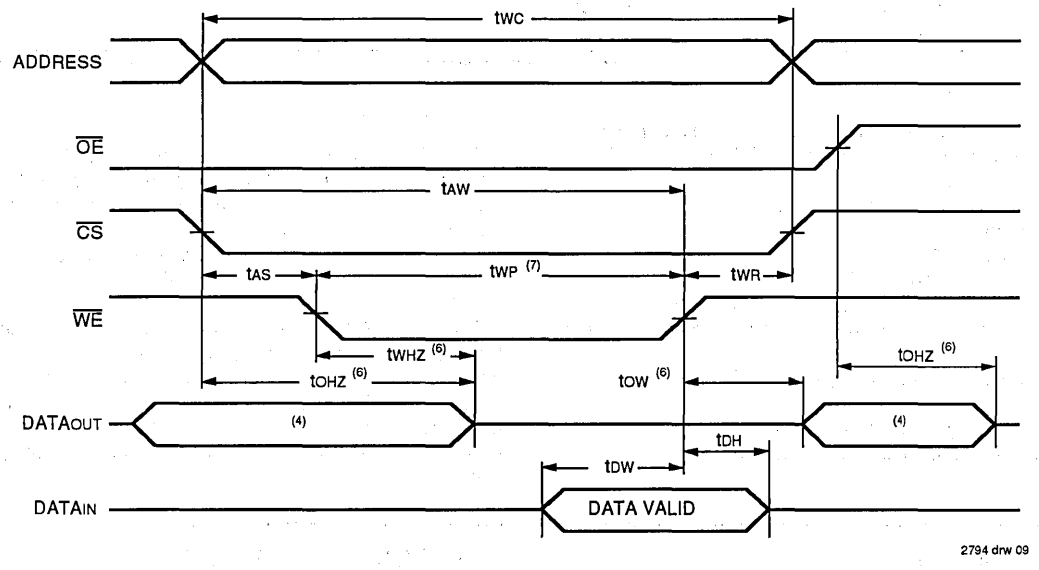
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2794 drw 08

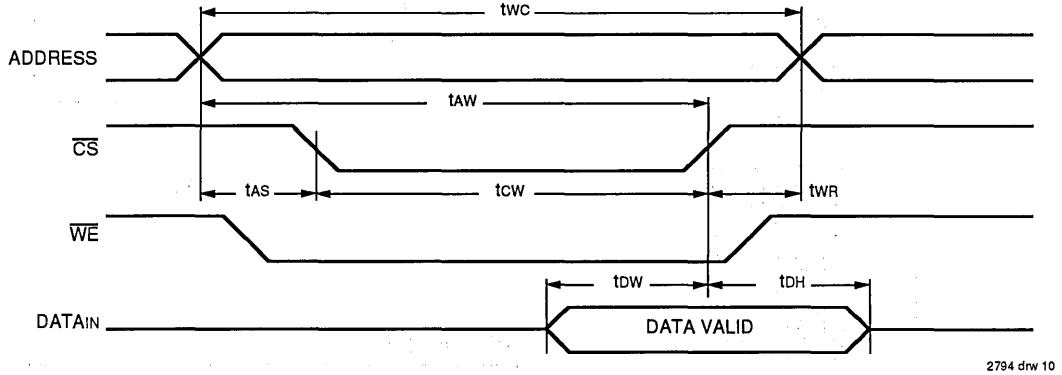
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2794 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2794 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of tWP or tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

Integrated Device Technology, Inc.

2M x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7MP4059

FEATURES:

- High-density 16 megabit CMOS static RAM module
- Pin-compatible upgrade from IDT7MP4058 (512K x 8) SRAM module
- Fast access time: 55ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.)V_{CC} = 2V
- Surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 36-pin SIP (Single In-line Package) for maximum space-saving
- Single 5V (±10%) power supply
- Inputs and outputs TTL-compatible

DESCRIPTION:

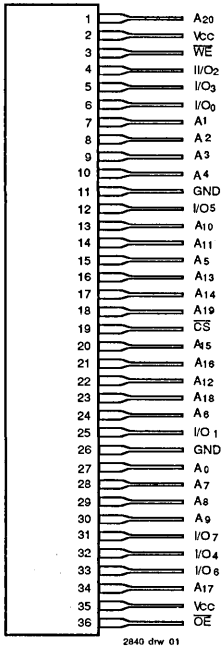
The IDT7MP4059 is a 2M x 8 high-speed CMOS static RAM module constructed on an epoxy laminate substrate (FR-4) using four 512K x 8 static RAMs and a one-of-four decoder in plastic surface mount packages.

The IDT7MP4059 is available with maximum access times as fast as 55ns, with maximum operating power consumption of 605mW.

The IDT7MP4059 is offered in a 36-pin SIP (Single In-line Package). This vertically mounted SIP module is a cost-effective solution allowing for very high packing density.

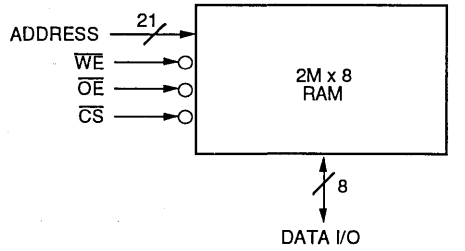
All inputs and outputs of the IDT7MP4059 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION



SIP
BACK VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_{0-20}	Address Inputs
I/O_{0-7}	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Power
GND	Ground

2840 tbl 01

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2840 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

2840 tbl 04

NOTE:
1. V_{IL} = –3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2840 tbl 05

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN\ (C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

2840 tbl 03

NOTE:
1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2840 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
I_{LO}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ 0.2V, $V_{IN} \geq V_{CC}$ –0.2V or ≤ 0.2V	—	450	µA

2840 tbl 07

7

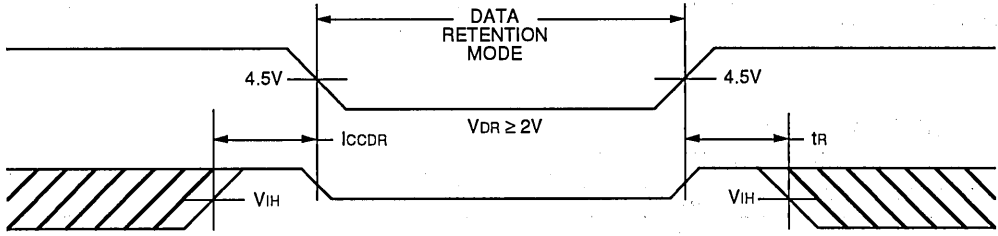
DATA RETENTION CHARACTERISTICS (T_A = 0°C TO +70°C)

Symbol	Parameter	Test Condition	Min.	Vcc @ 2.0V Max.	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}(1)	—	ns

NOTES:
1. t_{RC} = Read Cycle Time
2. This parameter is guaranteed by design, but not tested.

2840 tbl 08

DATA RETENTION WAVEFORM

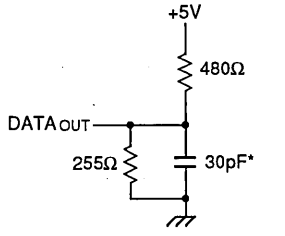


2840 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

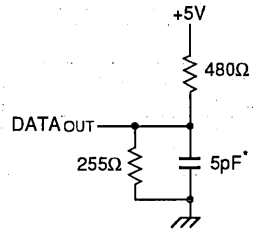
2840 tbl 09



2840 drw 04

*Including scope and jig.

Figure 1. Output Load



2840 drw 05

Figure 2. Output Load
(For t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

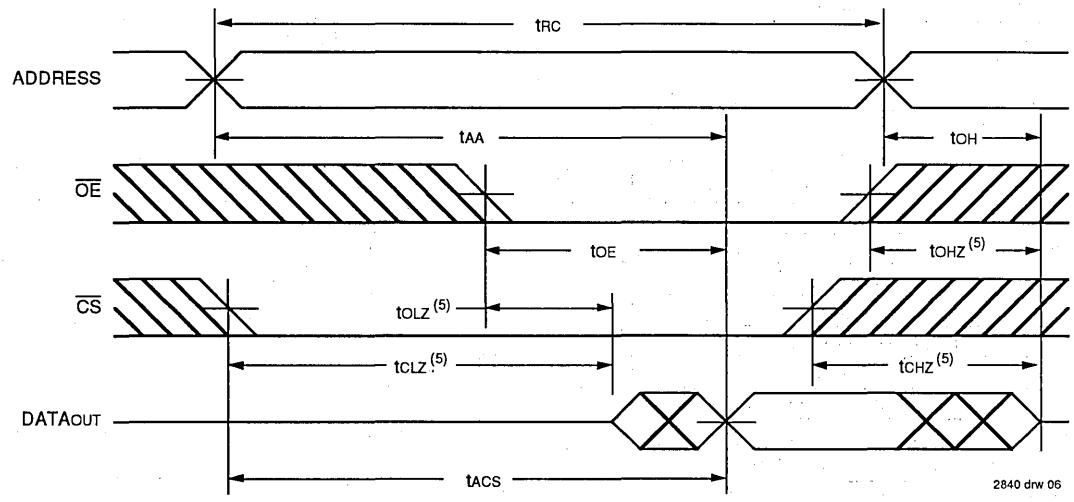
		7MP4059LxxS								
		-55		-70		-85		-100		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OE}	Output Enable to Output Valid	—	30	—	45	—	48	—	50	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	20	—	30	—	33	—	35	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	20	—	40	—	43	—	45	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	55	—	70	—	85	—	100	ns
Write Cycle										
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{WP}	Write Pulse Width	40	—	55	—	65	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	2	—	5	—	ns
t_{AW}	Address Valid to End of Write	45	—	65	—	82	—	90	—	ns
t_{CW}	Chip Select to End of Write	45	—	65	—	80	—	85	—	ns
t_{DW}	Data to Write Time Overlap	30	—	35	—	38	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	20	—	—	30	—	33	—	35	ns
t_{OW}(1)	Output Active from End of Write	5	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

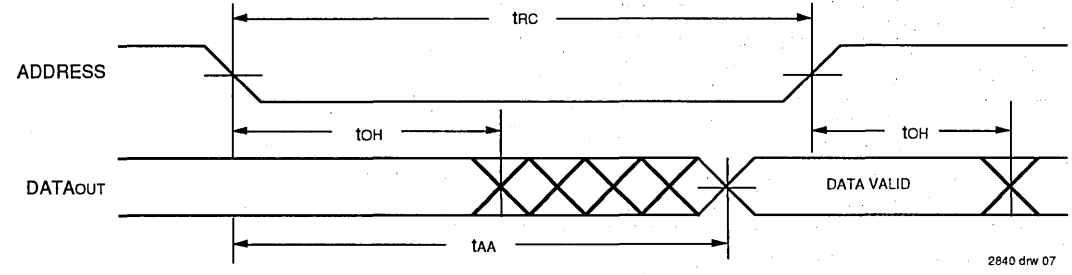
2840 tbl 10

7

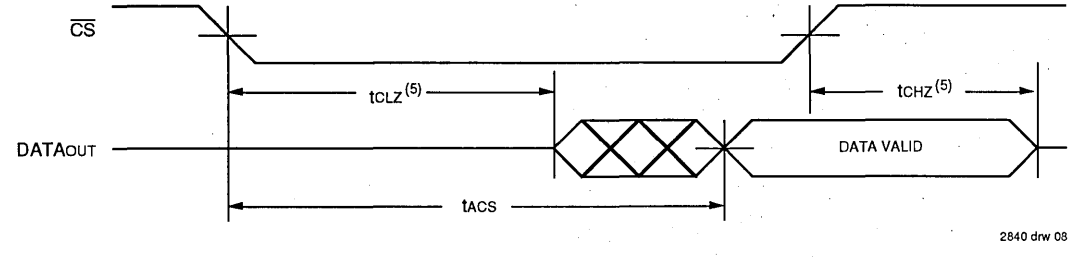
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)

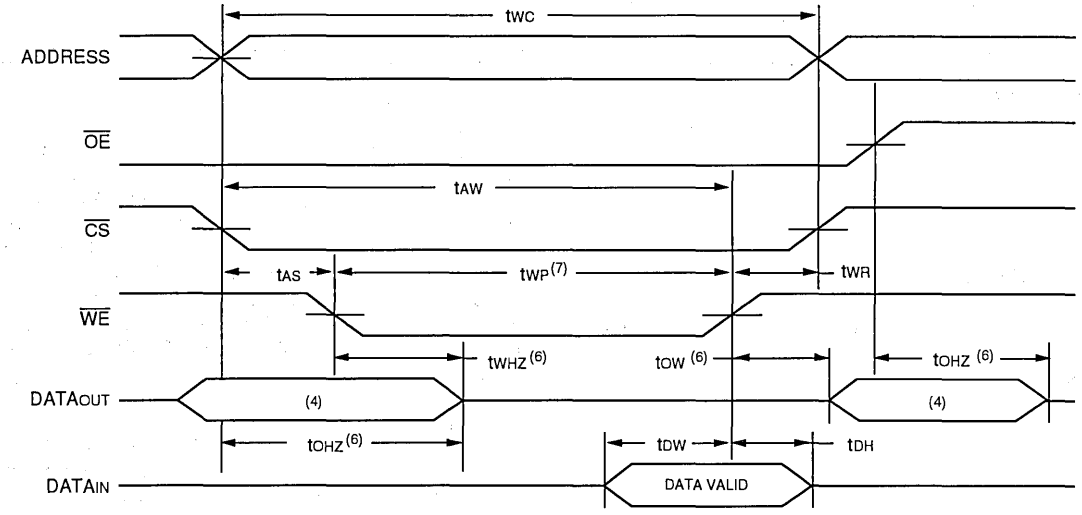


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



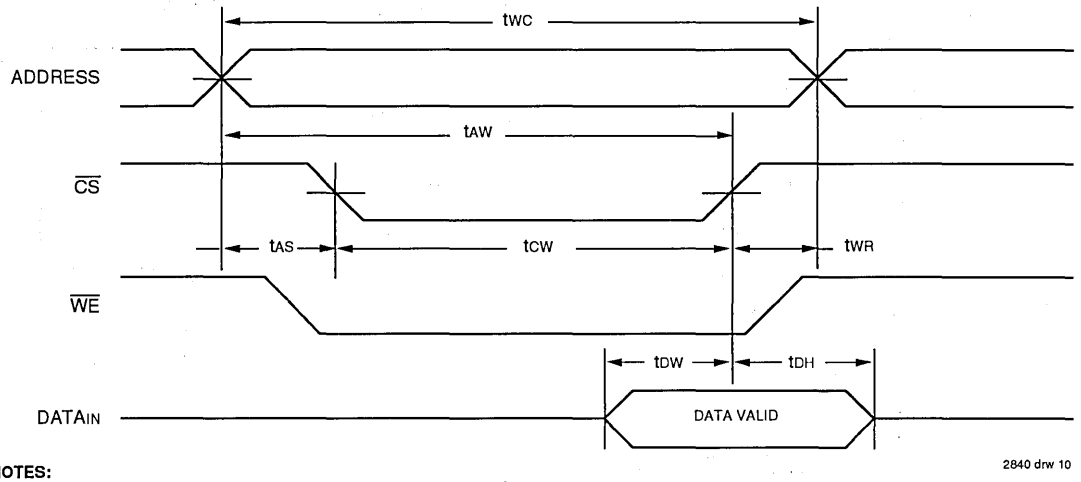
NOTES:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected $\overline{CS}$ = V_{IL}
3. Address valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = V_{IL}
5. Transition is measured = 200mV from steady state. This parameter is guaranateed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)(1, 2, 3, 7)



2840 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING)(1, 2, 3, 5)



2840 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlay (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

Integrated Device Technology, Inc.

512K x 8 BiCMOS/CMOS STATIC RAM MODULE

IDT7M4048
IDT7MB4048

FEATURES:

- High density 4 megabit (512K x 8) static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 15ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 400µA (max.)
  - — Data Retention: 250µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

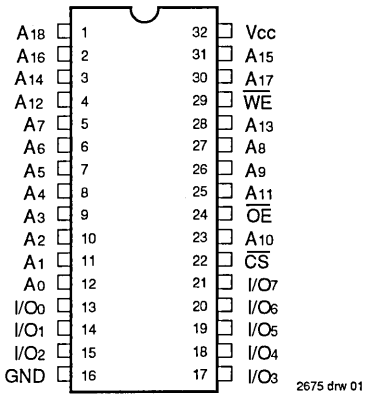
DESCRIPTION:

The IDT7M4048/7MB4048 is a 4 megabit (512K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 1 megabit static RAMs and a decoder. The IDT7MB4048 is available with access times as fast as 15ns. For low power applications, the IDT7M4048 version offers a data retention current of 200µA and a standby current of 400µA.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint. The IDT7MB4048 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4048 and 7MB4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

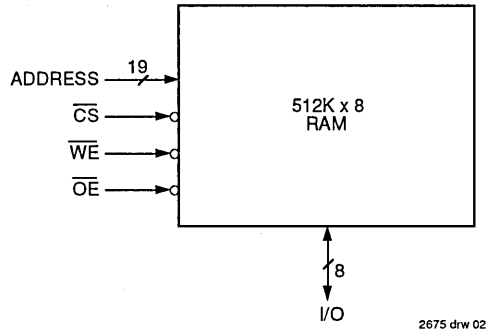
PIN CONFIGURATION



2675 drw 01

DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



2675 drw 02

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2675 tbl 3

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2675 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2675 tbl 04

1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2675 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7M4048LxxN		7MB4048SxxP 25 - 55ns		7MB4048SxxP 15 - 20ns[3]		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	—	8	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	—	8	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA[1], I_{OL} = 8mA[2]	—	0.4	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA[1], I_{OH} = –4mA[2]	2.4	—	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	—	480	—	520	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	—	250	—	250	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2	—	0.4	—	50	—	170	mA

NOTES: 2675 tbl 07

1. For 7M4048LxxN version only.
2. For 7MB4048SxxP version only.
3. Preliminary specifications only.

7

DATA RETENTION CHARACTERISTICS[3]

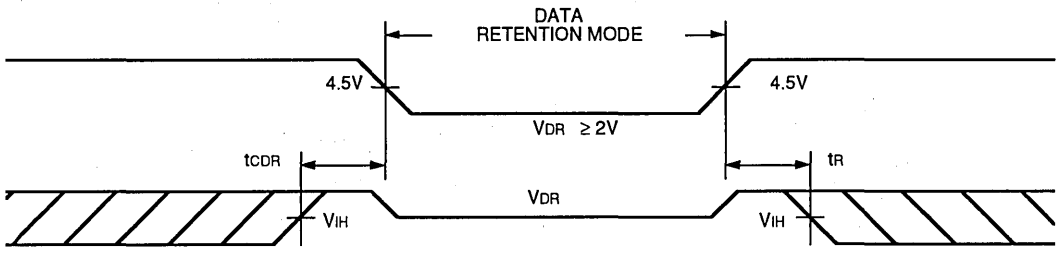
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}[2]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R[2]	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}[1]	—	ns

2675 tbl 08

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.
3. For 7M4048LxxN version only.

DATA RETENTION WAVEFORM

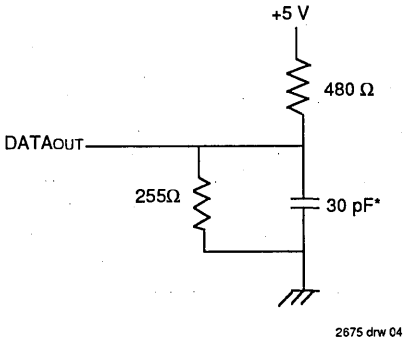


2675 drw 03

AC TEST CONDITIONS

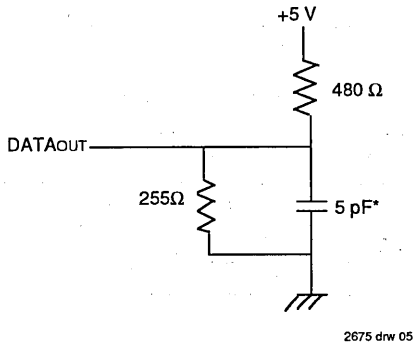
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

2675 tbl 09



2675 drw 04

Figure 1. Output Load



2675 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

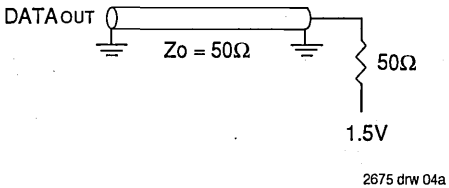


Figure 3. Alternate Output Load

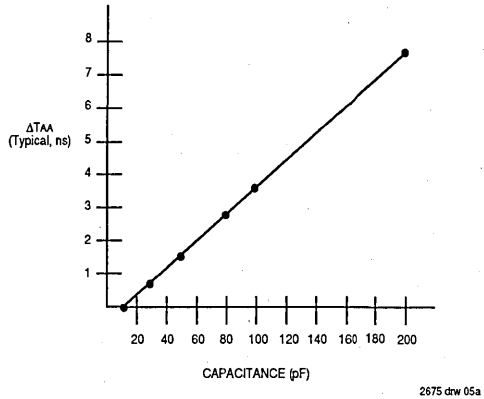


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MB4048SxxP												Unit
		-15(3)		-17(3)		-20(3)		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	35	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	30	—	35	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	—	35	ns
tOE	Output Enable to Output Valid	—	8	—	8	—	10	—	12	—	15	—	15	ns
tOHZ(1)	Output Disable to Output in High Z	—	7	—	7	—	8	—	12	—	12	—	15	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	12	—	12	—	13	—	14	—	16	—	20	ns
tOH	Output Hold from Address Change	1	—	1	—	3	—	3	—	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	15	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle														
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	35	—	ns
tWP	Write Pulse Width	15	—	14	—	15	—	17	—	20	—	25	—	ns
tAS(2)	Address Set-up Time	3	—	3	—	3	—	3	—	0	—	0	—	ns
tAW	Address Valid to End of Write	15(5)	—	17(4)	—	18	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	15	—	17	—	18	—	20	—	25	—	30	—	ns
tDW	Data to Write Time Overlap	10	—	10	—	12	—	15	—	17	—	20	—	ns
tDH(2)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWR(2)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	8	—	10	—	13	—	15	—	15	—	15	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	2	—	5	—	5	—	ns

2675 tbl 10

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 3ns for $\overline{CS}$ controlled write cycles.
3. Preliminary specifications only.
4. tAW=14ns for $\overline{CS}$ controlled write cycles.
5. tAW=12ns for $\overline{CS}$ controlled write cycles.

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7MB4048SxxP				7M4048LxxN						
		-45		-55		-60[3]		-65[3]		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES: 2675 tbl 11

1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 5ns for $\overline{CS}$ controlled write cycles.
3. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

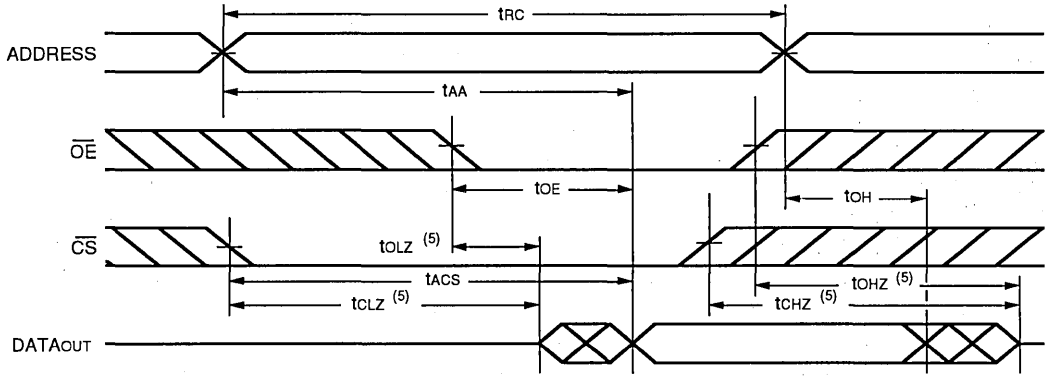
Symbol	Parameter	7M4048LxxN						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 12

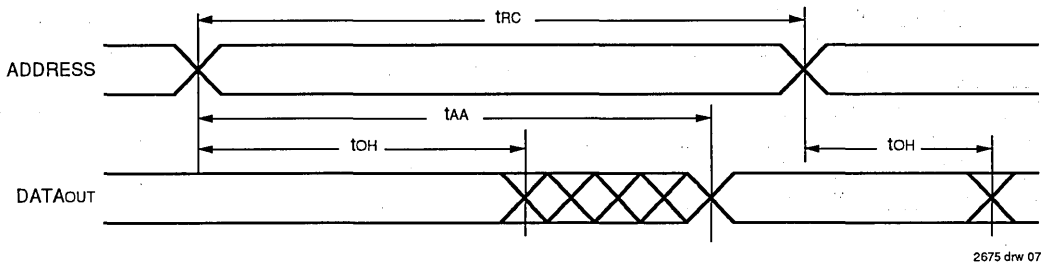
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



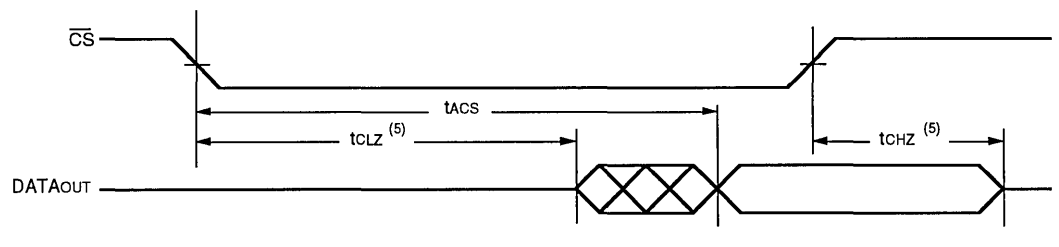
2675 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2675 drw 07

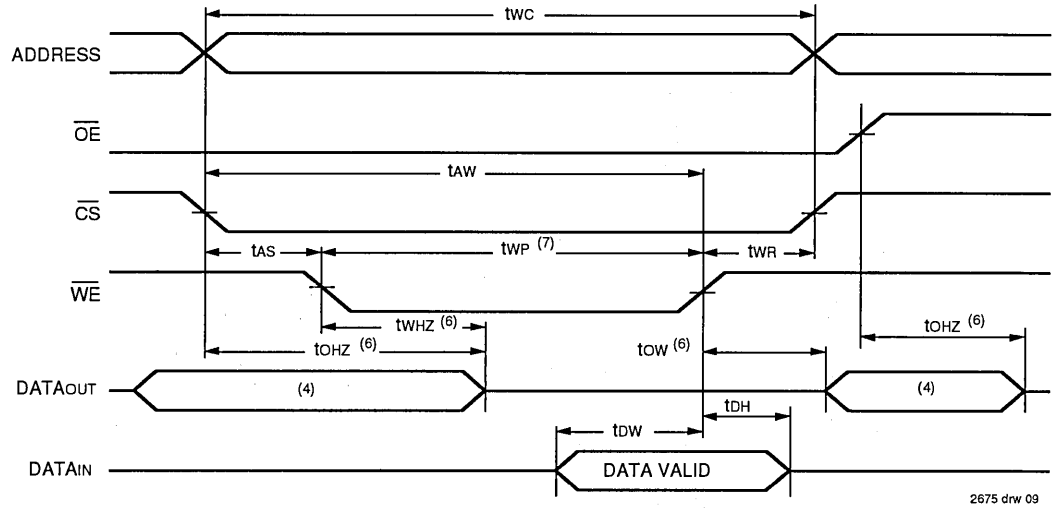
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



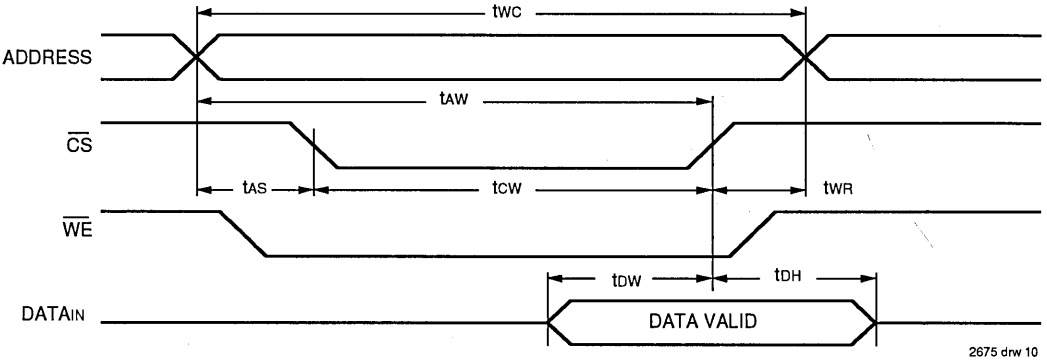
2675 drw 08

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



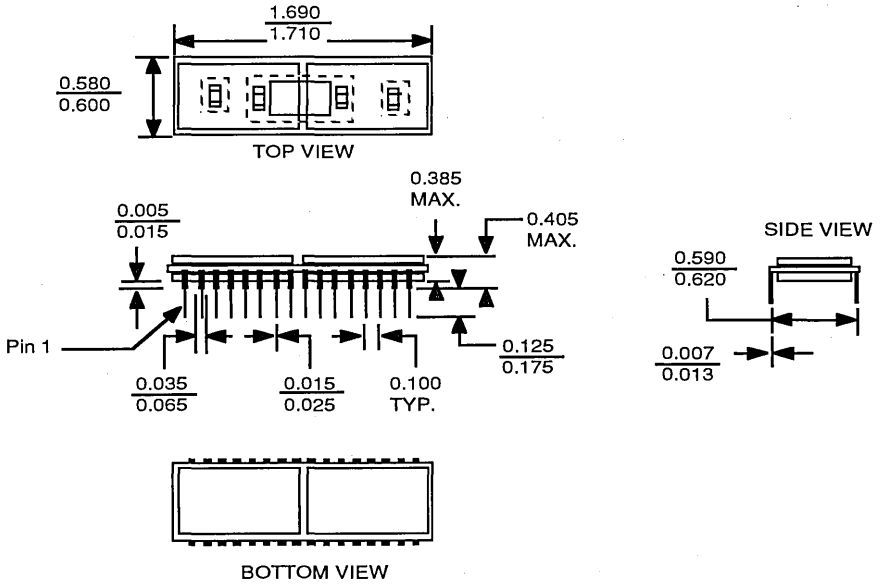
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

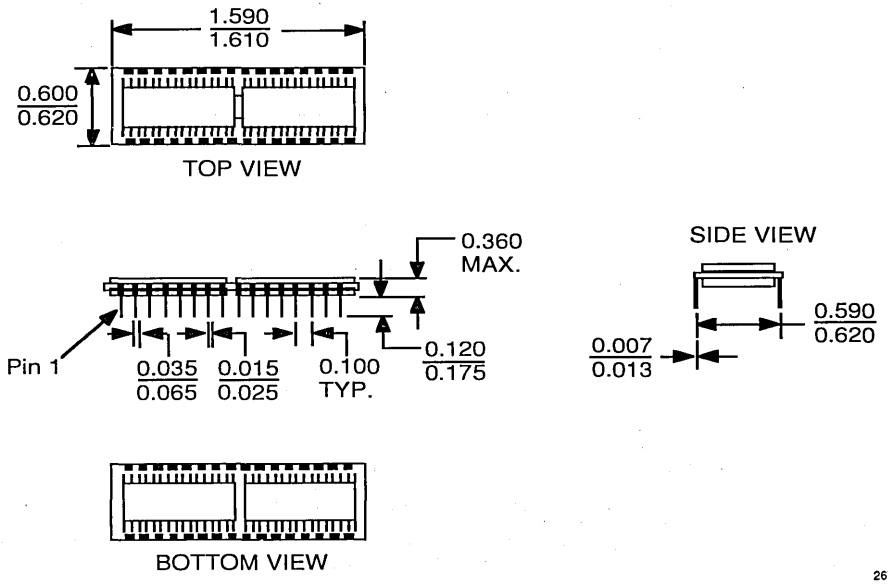
PACKAGE DIMENSIONS

7M4048LxxN



2675 drw 11

7MB4048SxxP



2675 drw 12

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048

FEATURES:

- High density 4 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 1.4mA (max.)
  - — Data Retention: 800µA (max.) Vcc = 2V
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

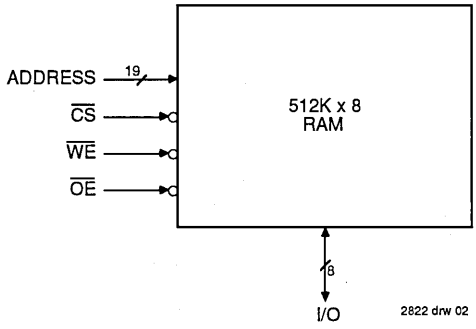
The IDT7M4048 is a 4 megabit (512K x 8) CMOS static RAM module constructed on a co-fired ceramic substrate using four 1 Megabit static RAMs and a decoder. The IDT7M4048 is available with access times as fast as 17ns. For low power applications, the IDT7M4048 version offers a data retention current of 800µA and a standby current of 1.4mA.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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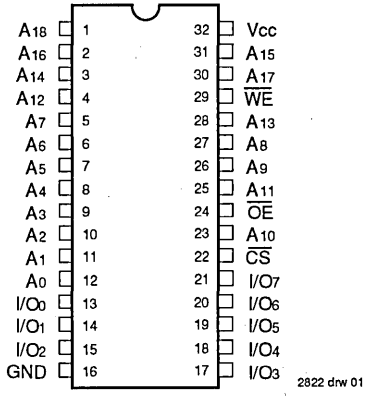
PIN CONFIGURATION



2822 drw 01

DIP
TOP VIEW

PIN NAMES

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

2822 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2822 tbl 09

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	50	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE: 2822 tbl 10

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +160	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2822 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2822 tbl 03

1. V_{IL} = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%

2822 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048SxxCB, 7M4048LxxCB				Unit
			17ns-55ns		60ns-120ns		
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA(1), I_{OL} = 8mA(2)	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA(1), I_{OH} = -4mA(2)	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$; f = f_{MAX}, Outputs Open	—	240	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	120	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or ≤ 0.2V	—	60	—	4	mA
		Very Low Power Version(3)	—	60	—	1.4	mA

NOTES:
1. For 17ns-55ns versions only.
2. For 60ns-120ns versions only.
3. L version only.

2822 tbl 05

DATA RETENTION CHARACTERISTICS(5)

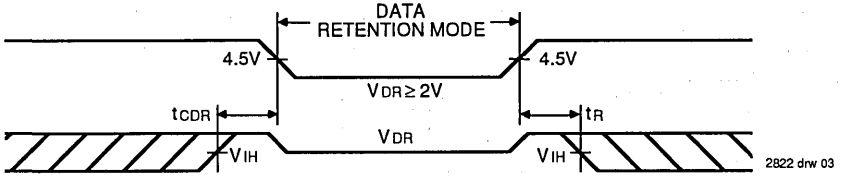
(T_A = -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \ge V_{CC}$ - 0.2V	—	2(4)	mA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \le V_{CC}$ - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	$V_{IN} \ge$ 0.2V	t_{RC}(2)	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 60ns-120ns versions, ICCDR=800µA.
5. L version only.

2822 tbl 09

DATA RETENTION WAVEFORM



2822 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2822 tbl 07

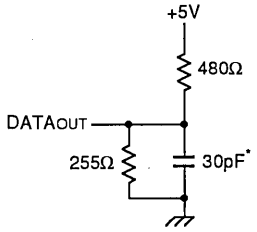


Figure 1. Output Load

* Including scope and jig

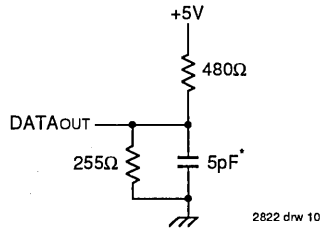


Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7M4048SxxCB, 7M4048LxxCB										
		-17(3)		-20(3)		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tAA	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
tACS	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
tOHZ(1)	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
tOH	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
tWC	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
tWP	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
tAS(2)	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
tAW	Address Valid to End of Write	17(4)	—	18	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
tDW	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
tDH(2)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWR(2)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

2822 tbl 06

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. tAW=14ns for $\overline{CS}$ controlled write cycles.

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB										Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
tAA	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
tACS	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
tOHZ[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
tOLZ[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
tWC	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
tWP	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
tAS	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
tAW	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
tCW	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
tDW	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
tDH	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
tOW[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES:

2822 tbl 06

1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for $\overline{CS}$ controlled write cycles. tDH, tWR= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

7

AC ELECTRICAL CHARACTERISTICS

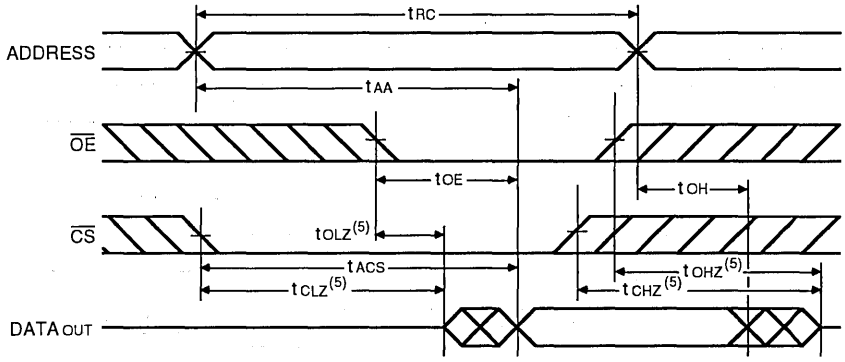
(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4048SxxCB, 7M4048LxxCB						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

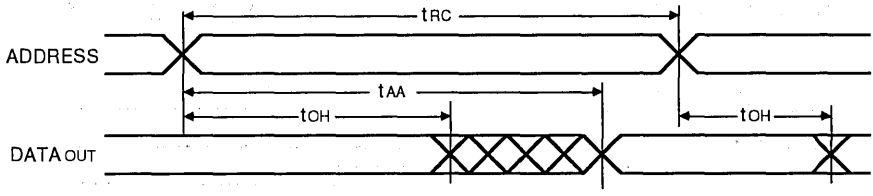
NOTE:
1. This parameter is guaranteed by design, but not tested.

2822 tbl 08

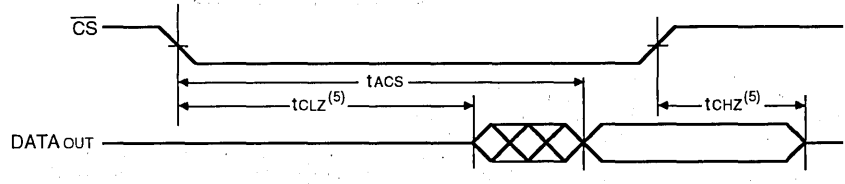
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

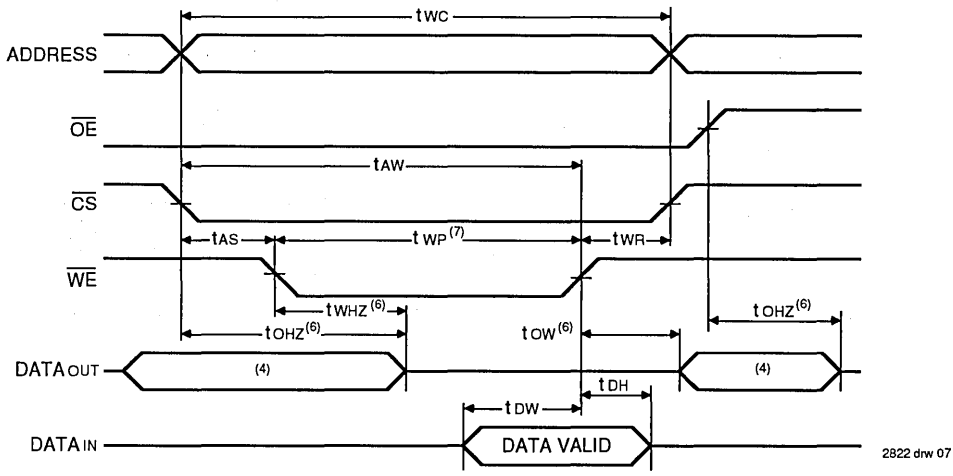


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

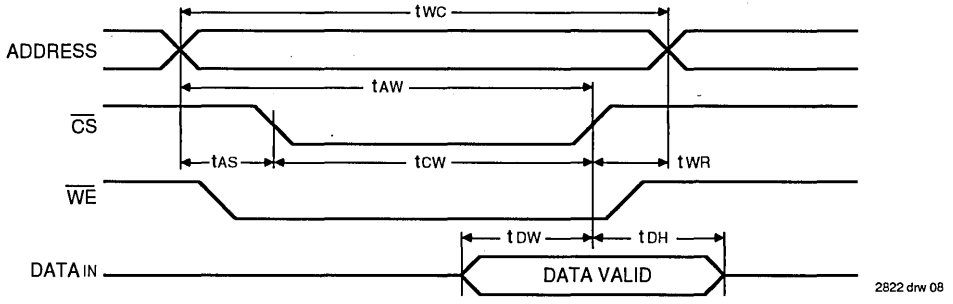


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

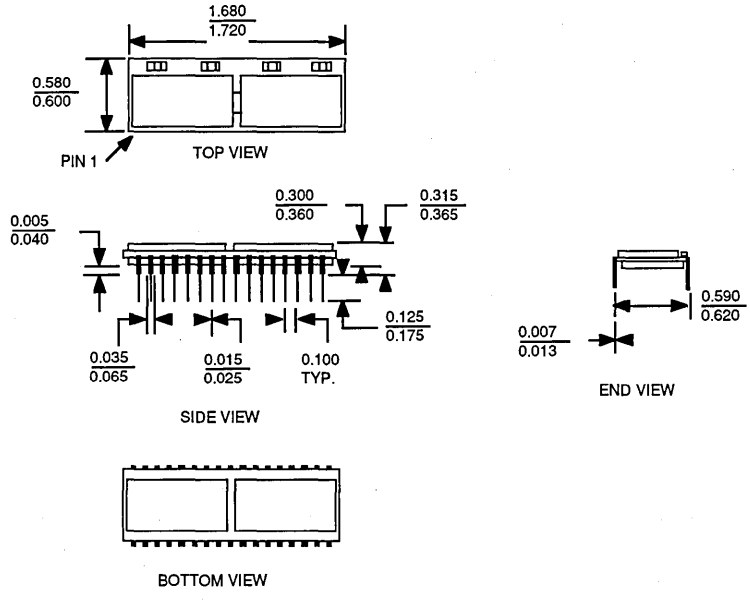


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((t_{WP}) > t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS



7

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

IDT7MP4058

FEATURES:

- High-density 4 megabit CMOS static RAM module
- Pin compatible with future 16 megabit upgrade (IDT7MP4059)
- Fast access time: 70ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.)Vcc = 2V
- Surface-mounted RAM packages on an epoxy laminate (FR-4) substrate
- Offered in a 36-pin SIP (Single In-line Package)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

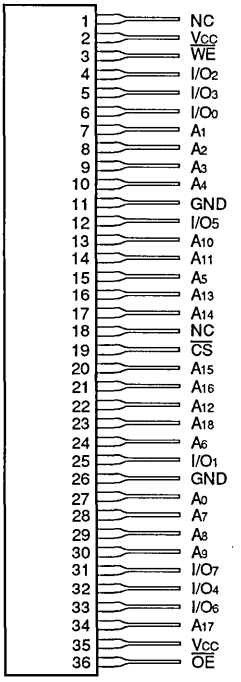
The IDT7MP4058L is a 512K x 8 high-speed CMOS static RAM module constructed on an epoxy laminate substrate (FR-4) using four 128K x 8 static RAMs and a one-of-four decoder in plastic surface mount packages.

The IDT7MP4058L is available with maximum access times as fast as 70ns, with maximum operating power consumption of 605mW.

The IDT7MP4058L is offered in a 36-pin SIP (Single In-line Package). This vertically mounted SIP module is a cost-effective solution allowing for very high packing density.

All inputs and outputs of the IDT7MP4058L are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

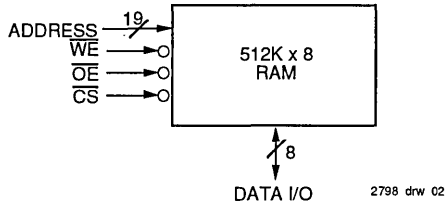
PIN CONFIGURATION



2798 drw 01

SIP
BACK VIEW

FUNCTIONAL BLOCK DIAGRAM



2798 drw 02

PIN NAMES

A0–18	Address Inputs
I/O0–7	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
Vcc	Power
GND	Ground
NC	No Connect

2798 tbl 01

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2798 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN\ (C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2798 tbl 06

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 2798 tbl 03

1. V_{IL} = –3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2798 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2798 tbl 07

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ 0.2V, $V_{IN} \geq V_{CC}$ –0.2V or ≤ 0.2V	—	450	µA

2798 tbl 05

DATA RETENTION CHARACTERISTICS (T_A = 0°C TO +70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ 0.2V	—	250	µA
t_{CDR}[2]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ 0.2V or	0	—	ns
t_R[2]	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}[1]	—	ns

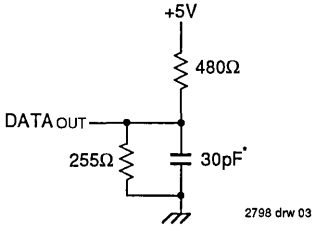
NOTES: 2798 tbl 10

1. t_{RC} = Read Cycle Time
2. This parameter is guaranteed by design, but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2798 tbl 08



*Including scope and jig.

Figure 1. Output Load

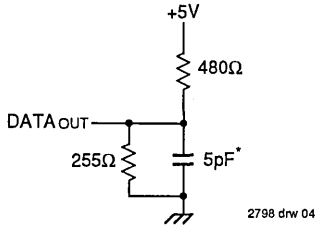


Figure 2. Output Load
(For t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

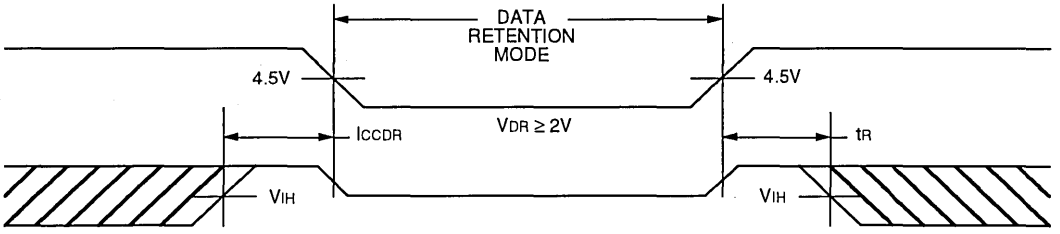
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7MP4058LxxS								
		-70		-85		-100		-120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	45	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	70	—	85	—	100	—	120	ns
Write Cycle										
t_{WC}	Write Cycle Time	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	65	—	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	30	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

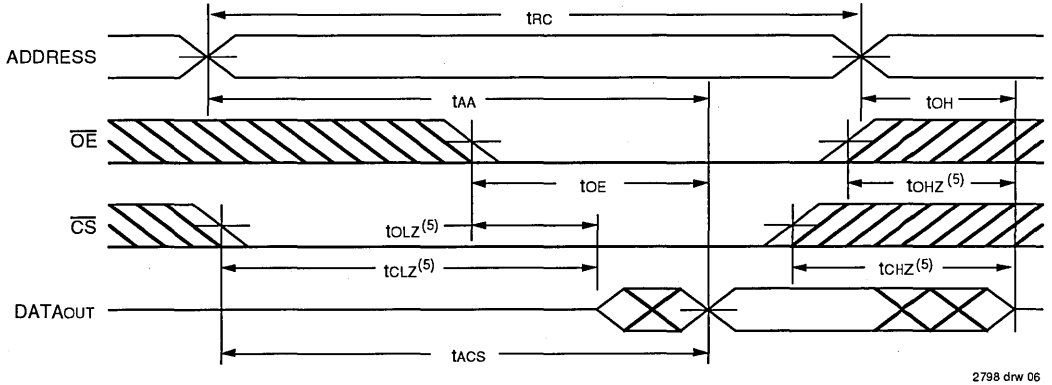
2798 tbl 09

DATA RETENTION WAVEFORM



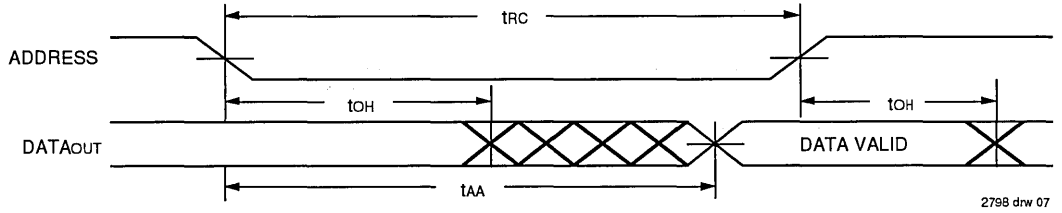
2798 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



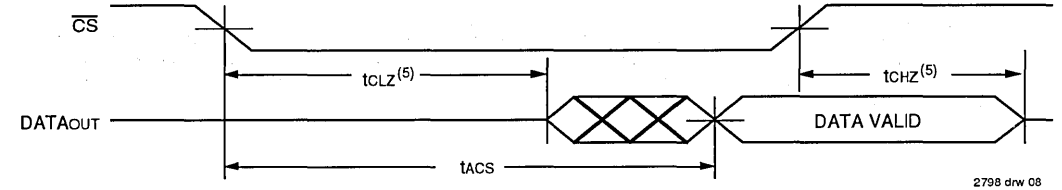
2798 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



2798 drw 07

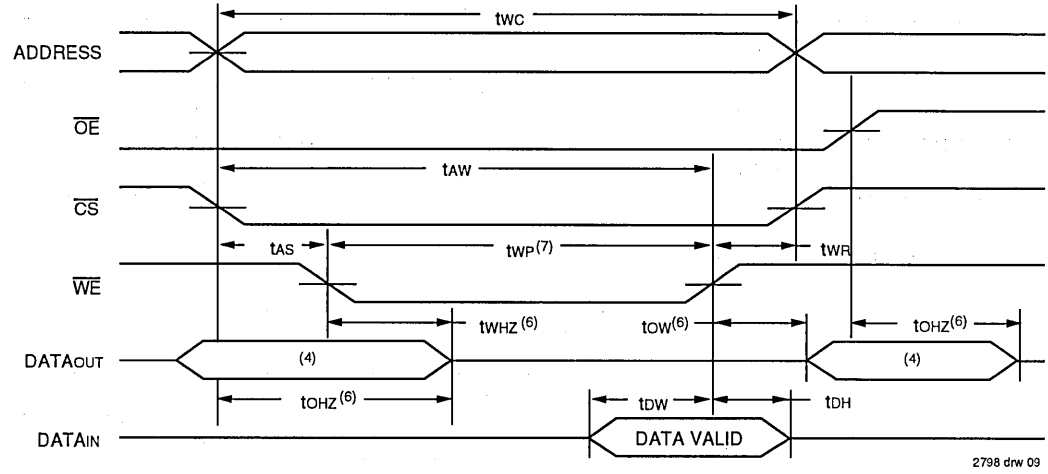
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



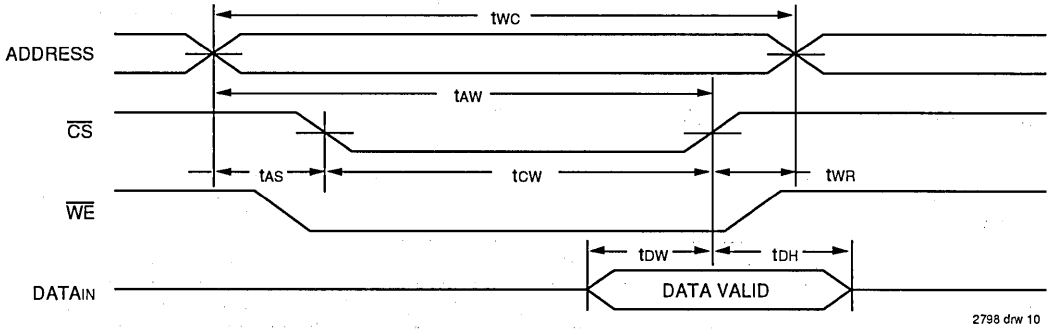
2798 drw 08

NOTES:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected $\overline{CS}$ = VIL
3. Address valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = VIL
5. Transition is measured = 200mV from steady state. This parameter is guaranateed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

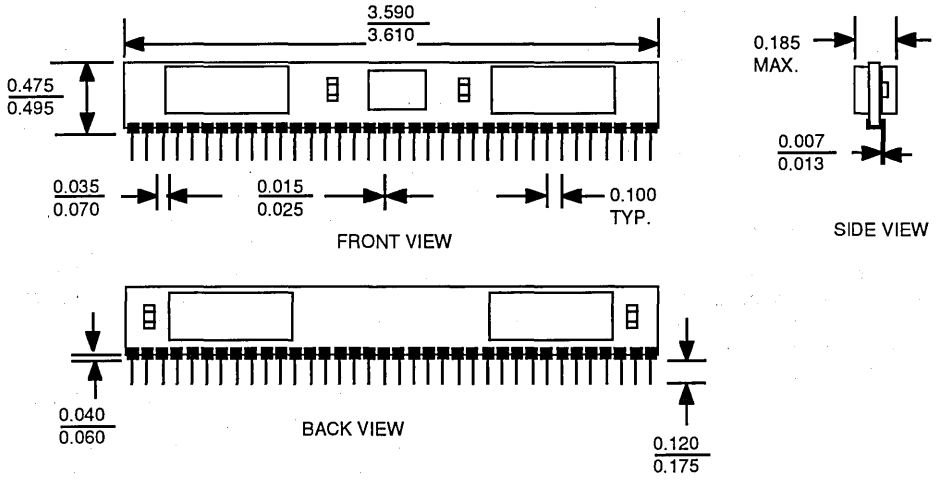


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlay (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2798 drw 11

7

Integrated Device Technology, Inc.

256K x 8 BiCMOS/CMOS STATIC RAM MODULE

IDT7M4068
IDT7MB4068

FEATURES:

- High density 2 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 8 static RAMs
- Fast access time: 10ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 250µA (max.)
  - — Data Retention: 150µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP (Dual In-line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

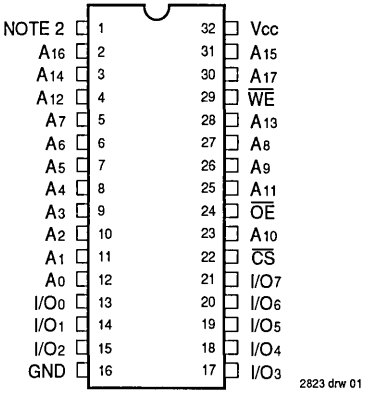
DESCRIPTION:

The IDT7M4068/7MB4068 is a 2 megabit (256K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using two 1 Megabit static RAMs and a decoder. The IDT7MB4068 is available with access times as fast as 10ns. For low power applications, the IDT7M4068 version offers a data retention current of 150µA and a standby current of 250µA.

The IDT7M4068 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 2 megabits into the JEDEC DIP footprint. The IDT7MB4068 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4068 and 7MB4068 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

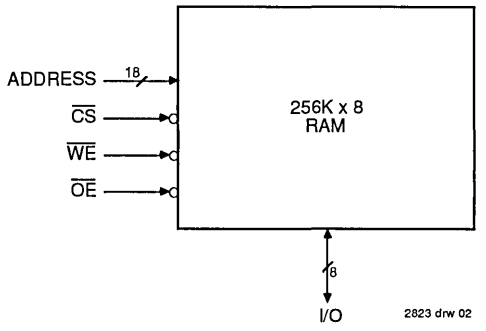
PIN CONFIGURATION[1]



DIP
TOP VIEW

NOTES:
1. For proper operation of the 7M4068LxxN module, Pin 1 must be connected to GND. For the 7MB4068xxP module, Pin 1 in a no connect.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2823 tbl 01

CEMOS is a trademark of Integrated Device Technology Inc.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2823 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	25	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE: 2823 tbl 03

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2823 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2823 tbl 04

1. VIL = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2823 tbl 06

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = 0°C to +70°C)

			7M4068LxxN		7MB4068SxxP				
					25 - 55ns		10 - 20ns[3]		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	2	—	10	—	10	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	2	—	10	—	10	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA[1], IOL = 8mA[2]	—	0.4	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA[1], IOH = –4mA[2]	2.4	—	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL; f = fMAX, Outputs Open	—	110	—	300	—	400	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Outputs Open	—	6	—	120	—	120	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2V	—	0.25	—	20	—	80	mA

NOTES: 2823 tbl 07

1. For 7M4068LxxN version only.
2. For 7MB4068SxxP, 7MB4068BxxP versions only.
3. Preliminary specifications only.

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DATA RETENTION CHARACTERISTICS[3]

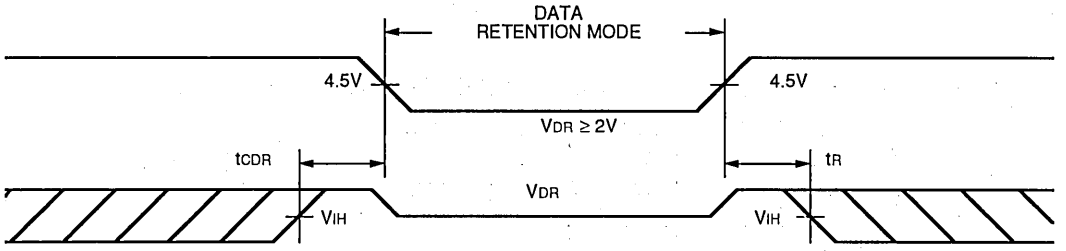
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	150	µA
t_{CDR}[2]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R[2]	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}[1]	—	ns

2823 tbl 08

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.
3. For 7M4068LxxN version only.

DATA RETENTION WAVEFORM

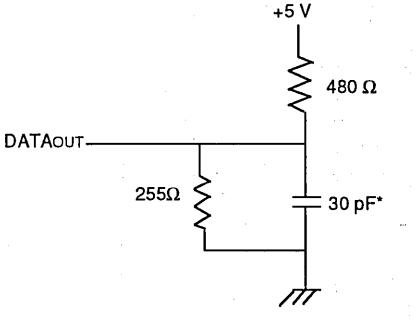


2823 drw 03

AC TEST CONDITIONS

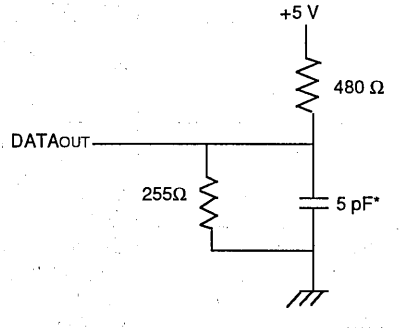
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2823 tbl 09



2823 drw 04

Figure 1. Output Load



2823 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

* Including scope and jig

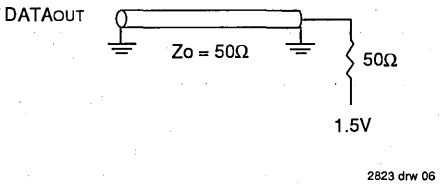


Figure 3. Alternate Output Load

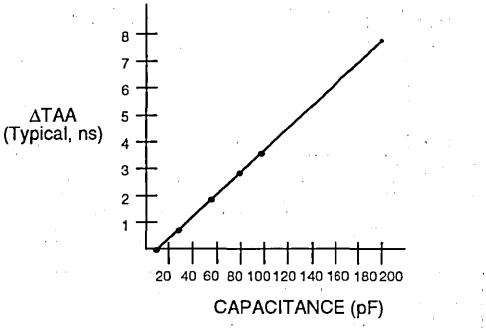


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP -10[2] Min.	-10[2] Max.	-12[2] Min.	-12[2] Max.	-15[2] Min.	-15[2] Max.	-17[2] Min.	-17[2] Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
t_{OE}	Output Enable to Output Valid	—	6	—	6	—	7	—	8	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	6	—	6	—	7	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	10	—	12	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{WP}	Write Pulse Width	10	—	10	—	12	—	14	—	ns
t_{AS}	Address Set-up Time	3	—	3	—	3	—	0	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	15	—	14	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	15	—	14	—	ns
t_{DW}	Data to Write Time Overlap	6	—	8	—	10	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	8	—	8	—	10	—	10	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

2823 tbl 10

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP								Unit
		-20		-25		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	12	—	25	—	30	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	15	—	17	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	16	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2823 tbl 11

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB4068SxxP				7M4068LxxN						Unit
		-45		-55		-60[2]		-65[2]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	25	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	25	—	25	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2823 tbl 12

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

7

AC ELECTRICAL CHARACTERISTICS

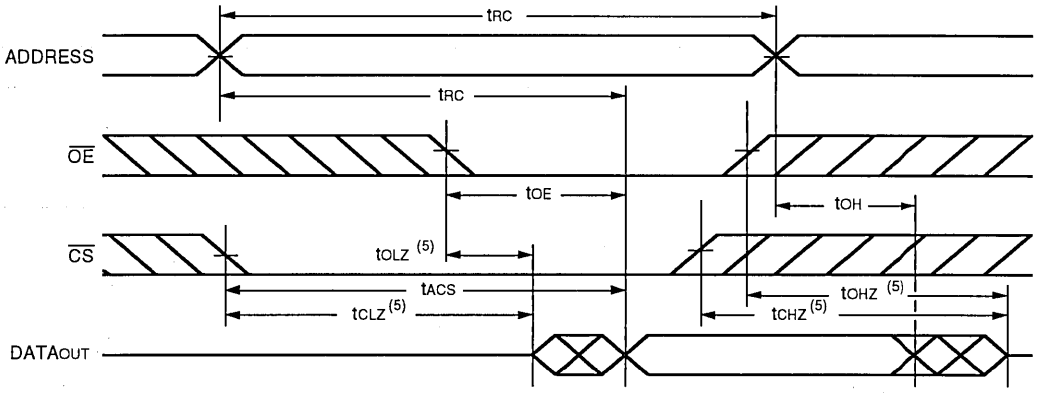
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4068LxxN						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

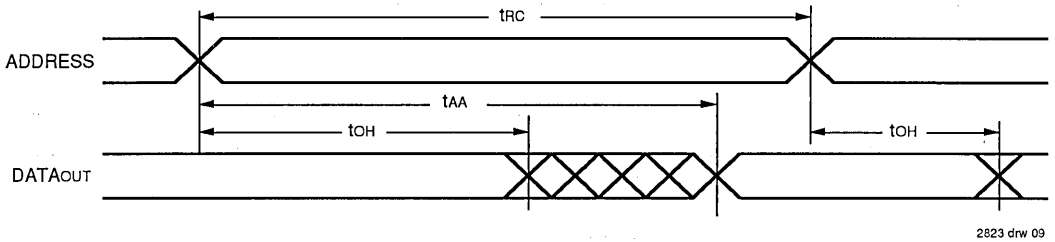
2823 tbl 13

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



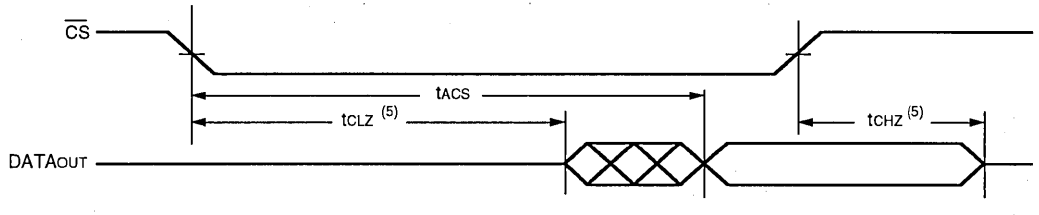
2823 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2823 drw 09

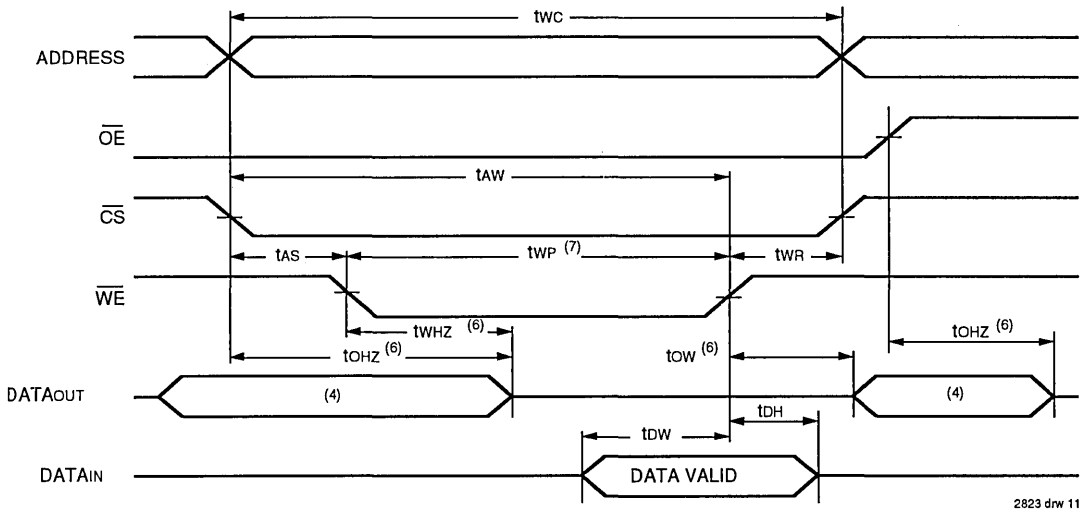
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



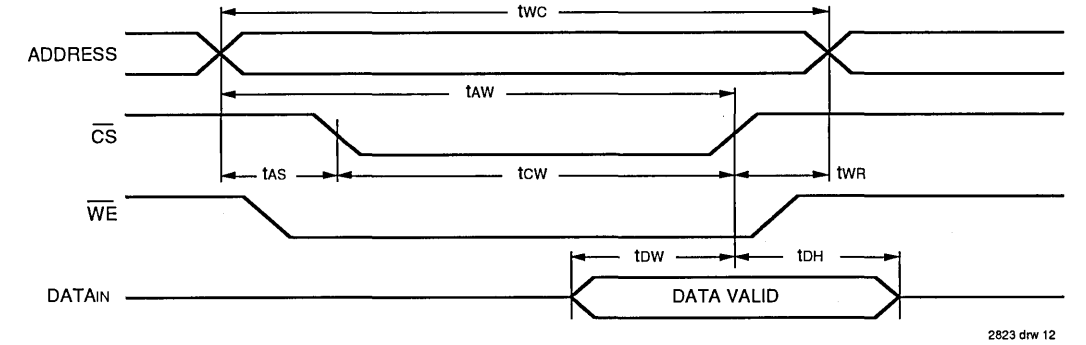
2823 drw 10

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



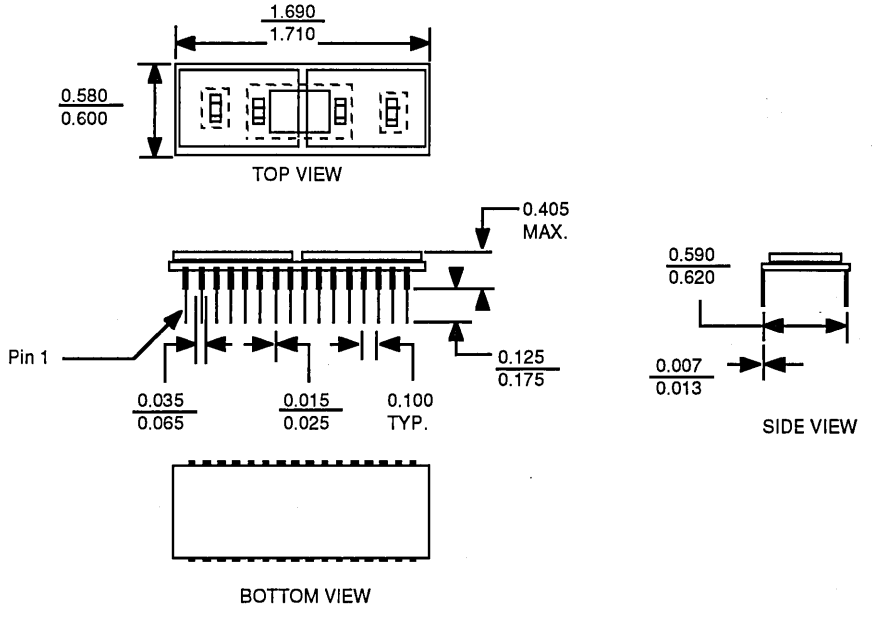
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

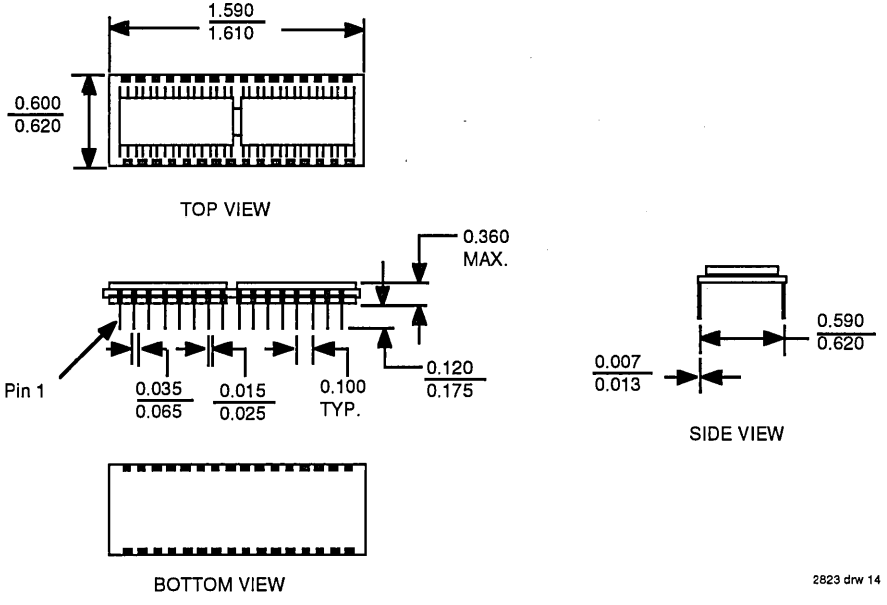
PACKAGE DIMENSIONS

7M4068LxxN



2823 drw 13

7MB4068SxxP



2823 drw 14

7

Integrated Device Technology, Inc.

256K x 8
CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4068

FEATURES:

- High density 2 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 8 static RAMs
- Fast access time: 17ns (max.)
- Low power consumption (L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 700µA (max.)
  - — Data Retention: 400µA (max.) Vcc = 2V
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

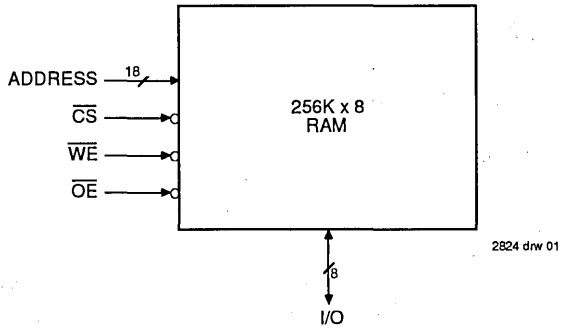
The IDT7M4068 is a 2 megabit (256K x 8) CMOS static RAM module constructed on a co-fired ceramic substrate using two 1 Megabit static RAMs and a decoder. The IDT7M4068 is available with access times as fast as 17ns. For low power applications, the IDT7M4068 version offers a data retention current of 400µA and a standby current of 700µA.

The IDT7M4068 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 2 megabits into the JEDEC DIP footprint.

All inputs and outputs of the IDT7M4068 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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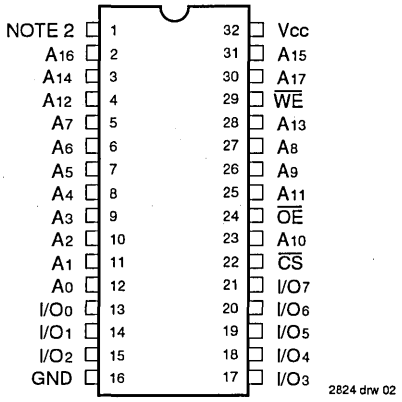
MILITARY TEMPERATURE RANGE **APRIL 1992**

PIN CONFIGURATION[1]



2824 drw 02

DIP
TOP VIEW

NOTE:
1. For proper operation of the module, Pin 1 must be connected to GND.

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2824 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2824 tbl 02

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	25	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE: 2824 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	-55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +160	°C
IOUT	DC Output Current	50	mA

NOTE: 2824 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2824 tbl 05
1. VIL = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%

2824 tbl 06

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4068SxxCB, 7M4068LxxCB				Unit
			17ns-55ns		60ns-120ns		
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA(1), I_{OL} = 8mA(2)	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA(1), I_{OH} = –4mA(2)	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ ≤ V_{IL}; f = f_{MAX}, Outputs Open	—	240	—	110	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	60	—	6	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	30	—	2	mA
		Very Low Power Version(3)	—	30	—	0.7	mA

NOTES:
1. For 60ns-120ns versions only.
2. For 17ns-55ns versions only.
3. L version only.

2824 tbl 07

DATA RETENTION CHARACTERISTICS(5)

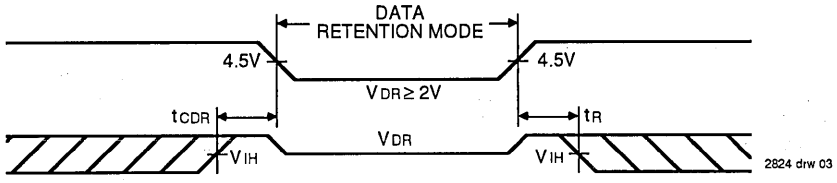
(T_A = -55°C to +125°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} - 0.2V	—	1(4)	mA
t_{CDR}(3)	Chip Deselect to Data Retention Time	V_{IN} ≤ V_{CC} - 0.2V or	0	—	ns
t_R(3)	Operation Recovery Time	V_{IN} ≥ 0.2V	t_{RC}(2)	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. For 60ns-120ns versions, ICCDR=400µA.
5. L version only.

2824 tbl 08

DATA RETENTION WAVEFORM

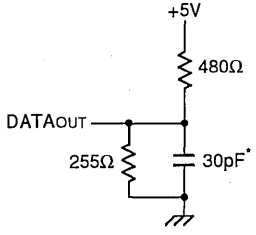


2824 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

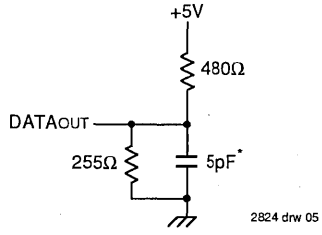
2824 tbl 09



2824 drw 04

Figure 1. Output Load

* Including scope and jig



2824 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		7M4068SxxCB, 7M4068LxxCB										
		-17[3]		-20[3]		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	17	—	20	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	7	—	8	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	12	—	13	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	1	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	17	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	17	—	20	—	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	17	—	20	—	25	—	ns
t_{AS}[2]	Address Set-up Time	3	—	3	—	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	17[4]	—	18	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	17	—	18	—	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	17	—	20	—	ns
t_{DH}[2]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}[2]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	10	—	13	—	15	—	15	—	15	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	5	—	5	—	ns

2824 tbl 10

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 3ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.
4. t_{AW}=14ns for $\overline{CS}$ controlled write cycles.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4068SxxCB, 7M4068LxxCB										Unit
		-45		-55		-60[3]		-65[3]		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	60	—	65	—	70	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	30	—	35	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	20	—	25	—	25	—	30	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	3	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	20	—	20	—	25	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	10	—	10	—	—	10	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	45	—	55	—	65	—	65	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	65	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	45	—	50	—	55	—	55	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{CW}	Chip Select to End of Write	40	—	50	—	60	—	65	—	65	—	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0[2]	—	0[2]	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	15	—	20	—	25	—	25	—	30	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	0	—	0	—	0	—	ns

NOTES:
2824 tbl 11

1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 5ns for $\overline{WE}$ controlled write cycles.
3. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

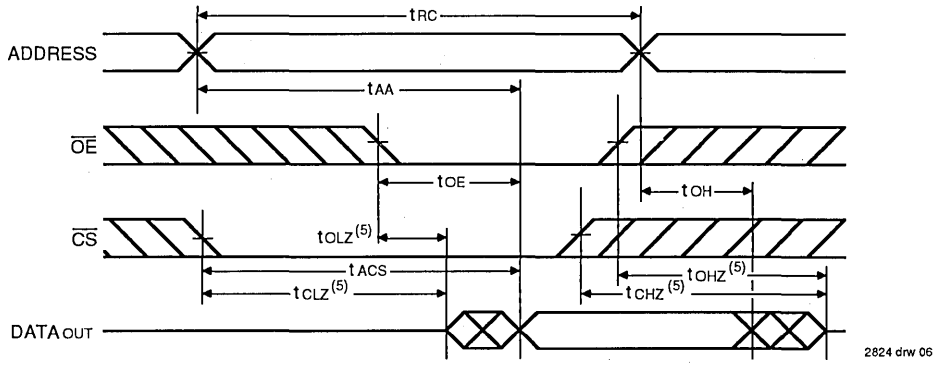
(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	7M4068SxxCB, 7M4068LxxCB						Unit
		-85		-100		-120		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Time Overlap	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

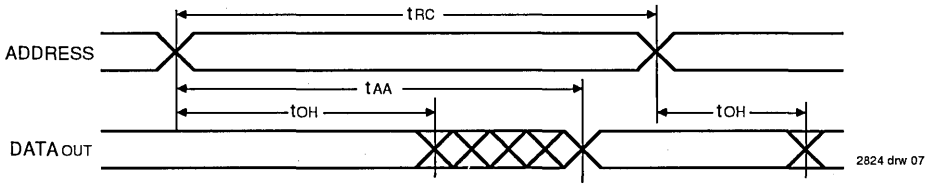
2824 tbl 12

NOTE:
1. This parameter is guaranteed by design, but not tested.

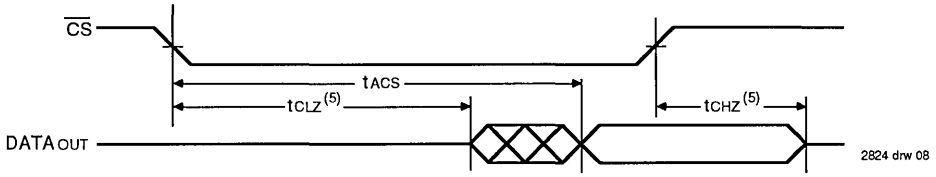
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

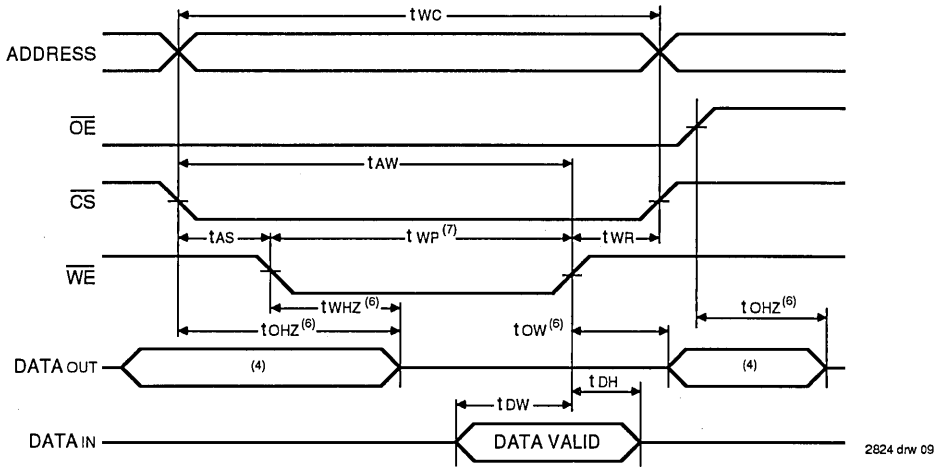


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

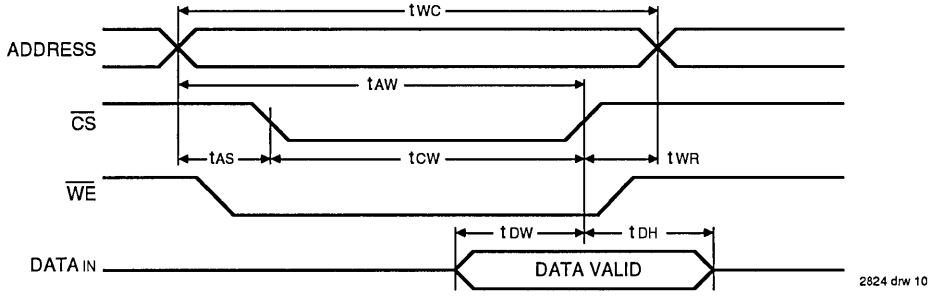


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

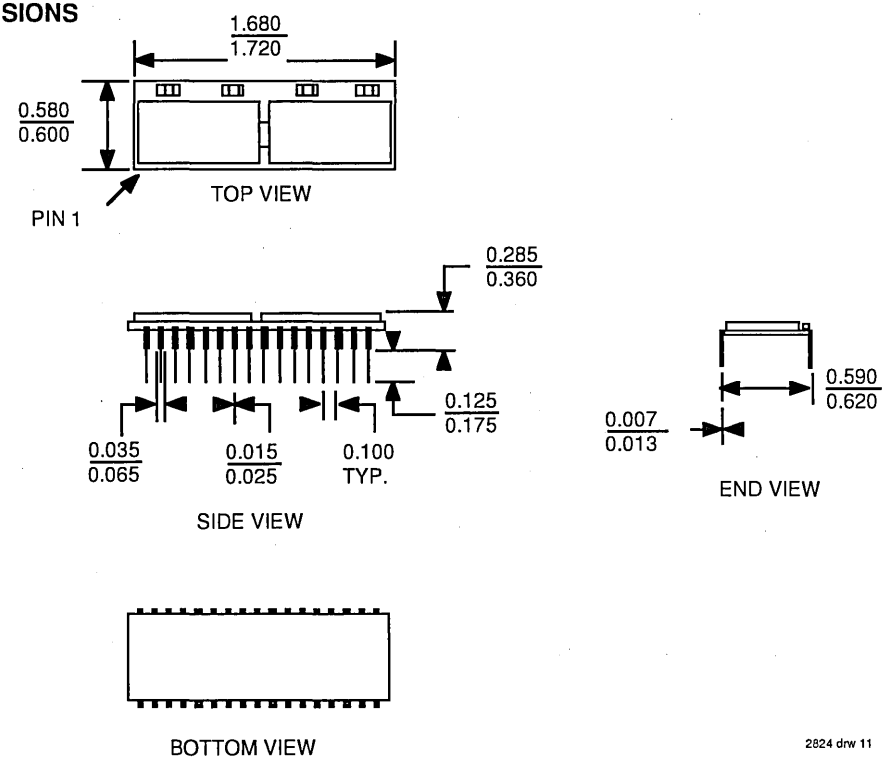


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2824 drw 11

Integrated Device Technology, Inc.

256K x 8 CMOS STATIC RAM MODULE

IDT7MP4034

FEATURES:

- High density separate I/O, 2 megabit CMOS static RAM module
- Fast access time: 10ns (max.)
- Low profile 42-pin ZIP (Zig-zag In-line vertical Package)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

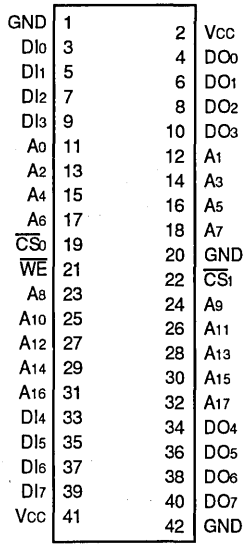
DESCRIPTION:

The IDT7MP4034 is a separate I/O, 256K x 8 CMOS static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 1 static RAMs in plastic SOJ packages. Availability of two chip select lines (one for each group of four RAMs) provides nibble access and allows the user to configure the memory into a 256K x 8 or a 512K x 4 organization. The IDT7MP4034 is available with access times as fast as 10ns with minimal power consumption.

The IDT7MP4034 is packaged in a 42-pin FR-4 ZIP (Zig-zag In-line vertical Package). The memory configuration results in a package 2.65 inches long and 0.35 inches wide. At only 0.5 inches high, this low profile package is ideal for high performance systems with minimum board spacing.

All inputs and outputs of the IDT7MP4034 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

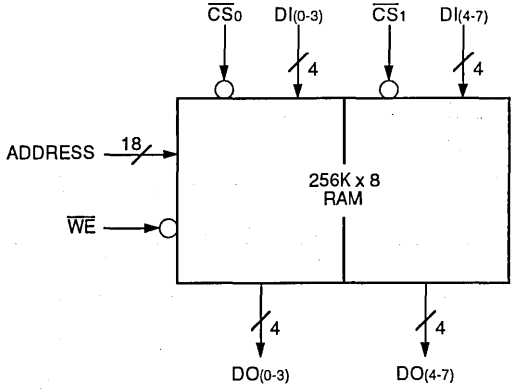
PIN CONFIGURATION



ZIP
TOP VIEW

2745 drw 01

FUNCTIONAL BLOCK DIAGRAM



2745 drw 02

PIN NAMES

DI0-7	Data Inputs
DO0-7	Data Outputs
A0-17	Address Inputs
CS0-1	Chip Selects
WE	Write Enable
VCC	Power
GND	Ground

2745 tbl 01

7

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2745 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2745 tbl 04
1. V_{IL} = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2745 tbl 05

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	$DATA_{IN}$	Active

2745 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address and Control)	V_{IN} = 0V	92	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE: 2745 tbl 06
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, T_A = 0°C TO +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2745 tbl 07

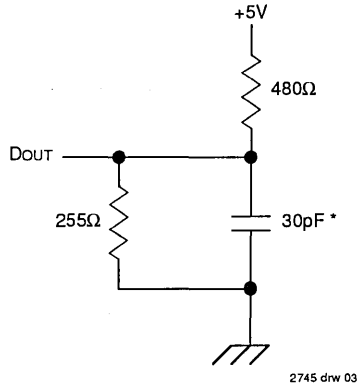
Symbol	Parameter	Test Conditions	10-12ns Max.	15-45ns Max.	Unit
I_{CC}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open V_{CC} = Max., f = f_{MAX}	1520	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	560	320	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, V_{IN} > V_{CC} - 0.2V or < 0.2V, f = 0	240	240	mA

NOTE: 2745 tbl 08
1. 10, 12, 15, and 17ns are preliminary specifications only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

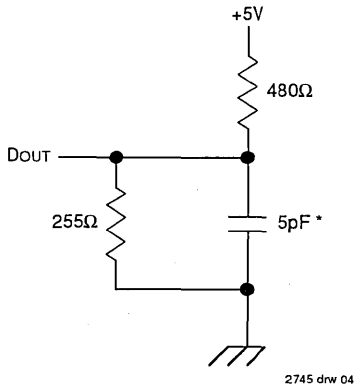
2745 tbl 09



2745 drw 03

Figure 1. Output Load

* Including scope and jig.



2745 drw 04

Figure 2. Output Load (for t_{CHZ}, t_{CLZ}, t_{OW} and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS(2)

(Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4034SxxZ -10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-17 Min.	-17 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	17	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ} (1)	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	10	—	12	—	15	—	17	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	13	—	15	—	ns
t_{AW}	Address Valid to End of Write	10	—	10	—	13	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	10	—	13	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	5	—	5	—	8	—	9	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	10	—	11	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

NOTES:

2745 tbl 10

1. This parameter is guaranteed by design but not tested.
2. 10,12,15, and 17ns are preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

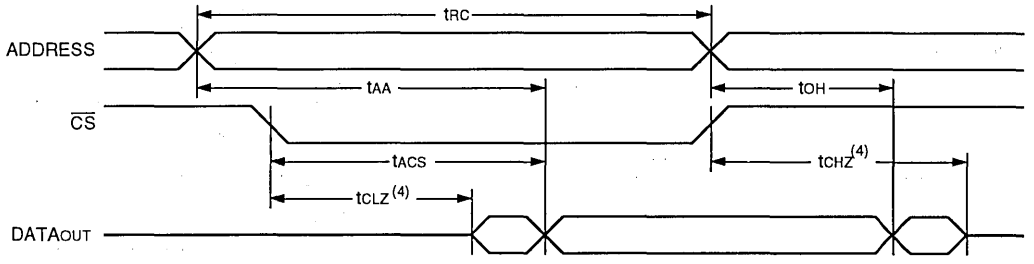
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP4034SxxZ								
		-20		-25		-35		-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Deselect to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{CW}	Chip Select to End of Write	17	—	22	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	17	—	22	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	17	—	22	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	10	—	13	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	—	0	—	0	—	0	—	0	ns

2745 tbl 11

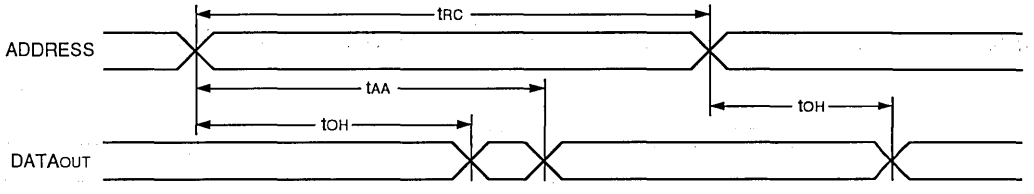
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



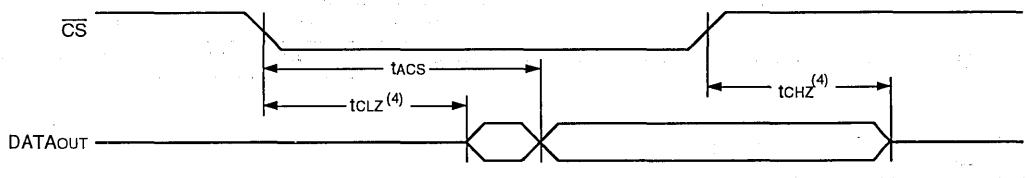
2745 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)



2745 drw 06

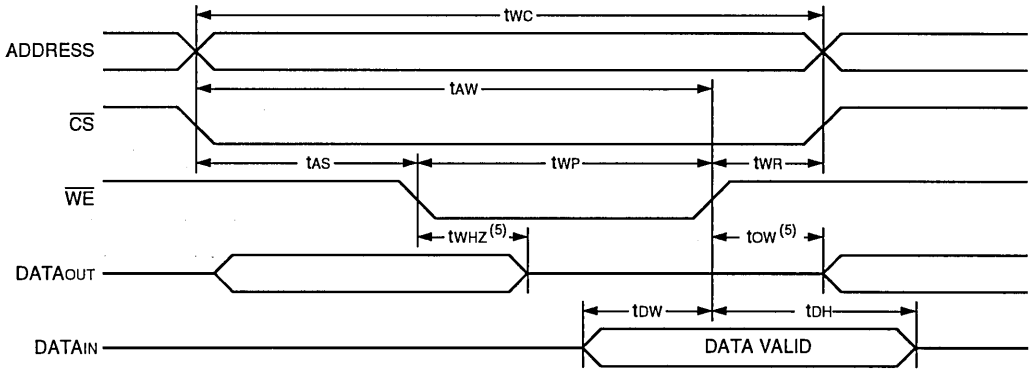
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)



2745 drw 07

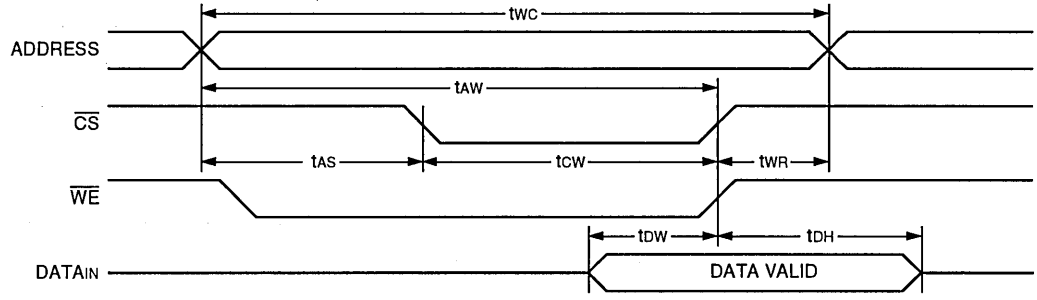
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1, 2, 3] ($\overline{WE}$ CONTROLLED TIMING)



2745 drw 08

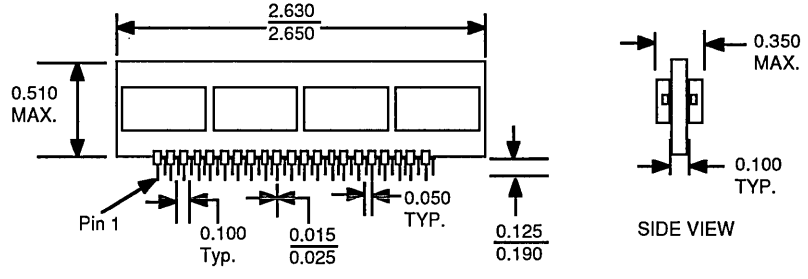
TIMING WAVEFORM OF WRITE CYCLE NO. 1[1, 2, 3, 4] ($\overline{CS}$ CONTROLLED TIMING)



2745 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneous with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

PACKAGE DIMENSIONS



2745 drw 10

Integrated Device Technology, Inc.

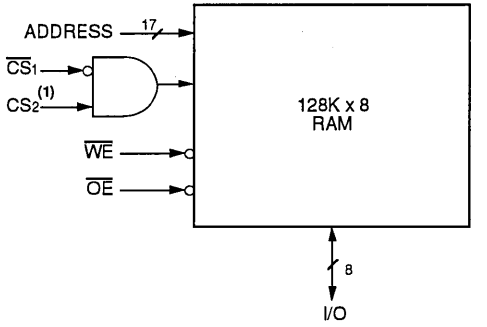
128K x 8 CMOS STATIC RAM

IDT71M024
IDT71M025

FEATURES:

- High density 1 megabit (128K x 8) static RAM
- Dual Chip Select Version (IDT71M024)
  Single Chip Select Version (IDT71M025)
- Fast access time:
  – commercial: 55ns (max.)
  – military: 60ns (max.)
- Low power consumption
  – active: 100mA (max.)
  – CMOS standby: 2mA (max.)
- Very low power version
  – data retention: 50µA (max.) Vcc = 3V
  – CMOS standby: 100µA (max.)
- 32-pin ceramic sidebrazed DIP or ceramic leadless chip carrier (LCC)
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

FUNCTIONAL BLOCK DIAGRAM



2820 drw 01

NOTE:
1. For the IDT71M024 version only.

PIN NAMES

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Addresses
$\overline{CS_1}$, CS_2	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
N.C.	No Connect
Vcc	Power
GND	Ground

2820 tbl 01

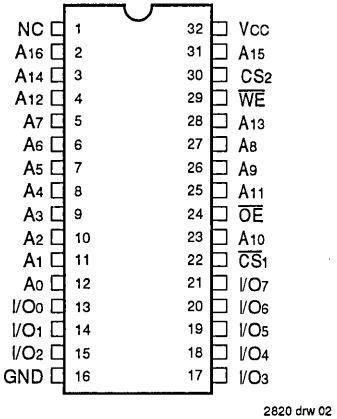
DESCRIPTION:

The IDT71M024/71M025 is a 1 megabit (128K x 8) static RAM packaged in a sidebrazed ceramic dual in-line package (DIP) and a ceramic leadless chip carrier (LCC). The IDT71M024/71M025 is available with access times as fast as 55ns. For battery backup applications, a very low power version is available, offering a commercial temperature data retention current of 50µA with Vcc = 3V.

The IDT71M024/71M025 are packaged in JEDEC standard 600 mil 32-pin ceramic DIPs. The IDT71M024 as comes in a hermetic 400 mil by 820 mil LCC. For surface mount applications, the proposed JEDEC standard 400 mil by 820 mil LCC is ideal.

All inputs and outputs of the IDT71M024/71M025 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use. All IDT military semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION(1)



2820 drw 02

DIP, LCC
TOP VIEW

NOTE:
1. For the IDT71M024 version Pin 30=CS_2. For the IDT71M025 version Pin 30=N.C.

7

TRUTH TABLE[1]

Mode	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	L	X	X	High-Z	Standby
Read	L	H	L	H	DOUT	Active
Read	L	H	H	H	High-Z	Active
Write	L	H	X	L	DIN	Active

NOTE: 2820 tbl 02
1. CS_2 is available for the IDT71M024 version only.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2820 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2820 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2820 tbl 04
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2820 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	2.5	—	5	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS_1}$ = VIH and CS_2= VIL, VOUT = GND to VCC	—	2.5	—	5	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA	—	0.4	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA,	2.4	—	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ 1≤ VIL and CS_2 ≥ VIH, f = fMAX, Outputs Open	—	100	—	100	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS_1}$ ≥ VIH and CS_2 ≤ VIL, VCC = Max., f = fMAX, Outputs Open	—	2.5	—	2.5	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS_1}$ ≥ VCC - 0.2V and CS_2 ≤ 0.2V VIN ≥ VCC - 0.2V or ≤ 0.2V	—	2	—	2	mA
		Very Low Power Version[1]	—	100	—	350	µA

NOTE: 2820 tbl 07
1. For data retention version, please specify L power when ordering.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2820 tbl 08

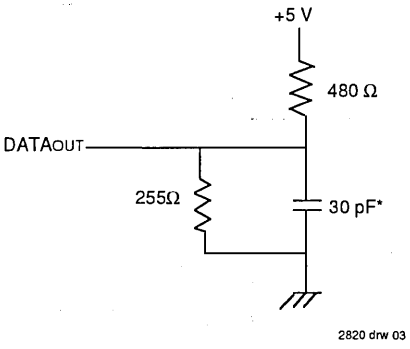


Figure 1. Output Load

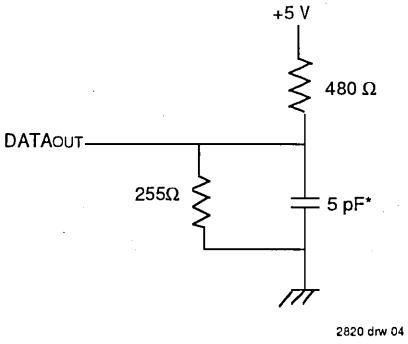


Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

* Including scope and jig

DATA RETENTION CHARACTERISTICS(1)

(T_A = 0°C to +70°C and -55°C to +125°C)

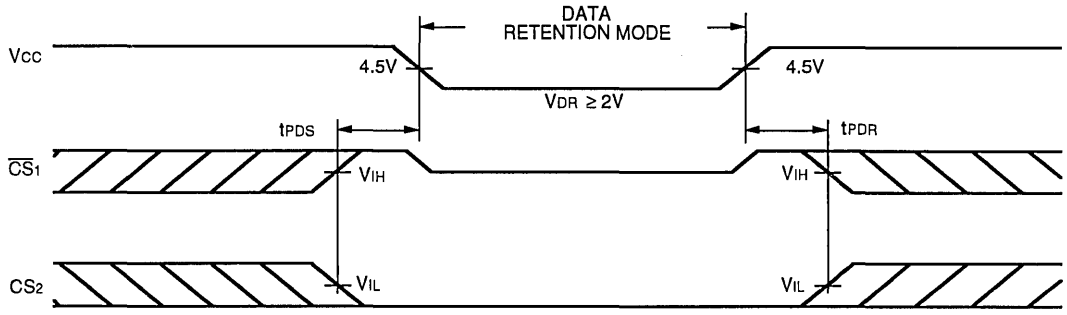
Symbol	Parameter	Test Condition	Min.	Comm. Max.	Military Max.	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	—	V
$V_{\overline{CS}_1}$	$\overline{CS}_1$ Input Voltage	$V_{DR} \geq 2.2V$	2.2	—	—	V
V_{CS_2}	CS_2 Input Voltage	$V_{DR} \geq 4.5V$	—	0.8	0.8	V
		$V_{DR} < 4.5V$	—	0.2	0.2	V
I_{CCDR1}	Data Retention Current	V_{CC} = 3.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	300	µA
I_{CCDR2}	Data Retention Current	V_{CC} = 2.0V, $CS_2 \leq 0.2V$ or $\overline{CS}_1$, $CS_2 \geq V_{CC}$ - 0.2V, $V_{IN} \leq V_{CC}$ - 0.2V or $V_{IN} \geq 0.2V$	—	50	200	µA
t_{PDS}(2)	Power Down Set Up Time		0	—	—	ns
t_{PDR}(2)	Power Down Recovery Time		t_{RC}(3)	—	—	ns

NOTES:
1. This option is only offered when ordering L power version.
2.. This parameter is guaranteed by design, but not tested.
3. t_{RC} = Read Cycle Time.

2820 tbl 09

7

DATA RETENTION WAVEFORM



2820 drw 05

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = 0°C to +70°C and -55°C to +125°C)

		71M024 or 71M025								
		-55[2,3]		-60[2]		-65[2]		-70		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	60	—	65	—	70	—	70	—	ns
tAA	Address Access Time	—	55	—	60	—	65	—	70	ns
tACS1	Chip Select ($\overline{CS_1}$) Access Time	—	55	—	60	—	65	—	70	ns
tACS2	Chip Select (CS_2) Access Time	—	60	—	65	—	70	—	70	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	35	—	35	ns
tOHZ[1]	Output Disable to Output in High Z	—	20	—	25	—	25	—	25	ns
tOLZ[1]	Output Enable to Output in Low Z	3	—	3	—	5	—	5	—	ns
tCLZ1,2[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	ns
tCHZ1,2[1]	Chip Deselect to Output in High Z	—	20	—	25	—	25	—	25	ns
tOH	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	60	—	65	—	70	—	70	ns
Write Cycle										
tWC	Write Cycle Time	60	—	65	—	70	—	70	—	ns
tWP	Write Pulse Width	45	—	50	—	55	—	55	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tAW	Address Valid to End of Write	55	—	60	—	65	—	65	—	ns
tCW1	Chip Select ($\overline{CS_1}$) to End of Write	55	—	60	—	65	—	65	—	ns
tCW2	Chip Select (CS_2) to End of Write	55	—	60	—	65	—	65	—	ns
tDW	Data to Write Time Overlap	25		30	—	30	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Output in High Z	—	20	—	25	—	25	—	25	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

2820 tbl 10

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.
3 Commercial temperature only.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

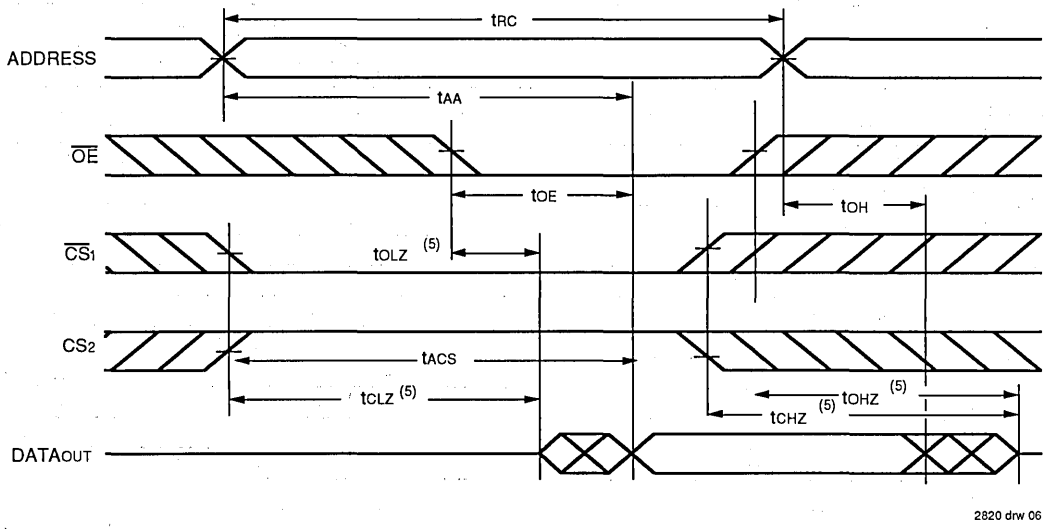
		71M024 or 71M025						
		-85		-100		-120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	85	—	100	—	120	ns
t_{ACS1}	Chip Select ($\overline{CS_1}$) Access Time	—	85	—	100	—	120	ns
t_{ACS2}	Chip Select (CS_2) Access Time	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	45	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	30	—	35	—	35	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
$t_{CLZ1,2}$[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	ns
$t_{CHZ1,2}$[1]	Chip Deselect to Output in High Z	—	30	—	35	—	35	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	85	—	100	—	120	ns
Write Cycle								
t_{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	60	—	65	—	65	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	70	—	75	—	75	—	ns
t_{CW1}	Chip Select ($\overline{CS_1}$) to End of Write	70	—	75	—	75	—	ns
t_{CW2}	Chip Select (CS_2) to End of Write	70	—	75	—	75	—	ns
t_{DW}	Data to Write Time Overlap	35	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	30	—	35	—	35	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2820 tbl 11

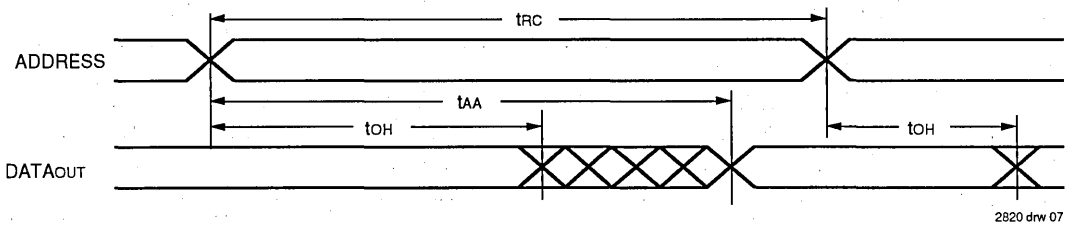
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



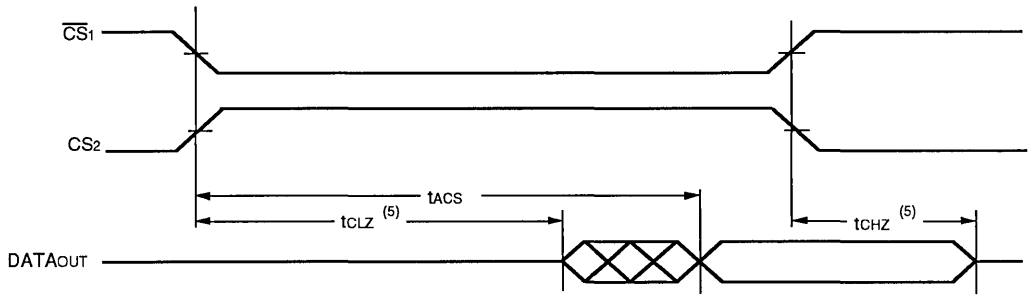
2820 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2820 drw 07

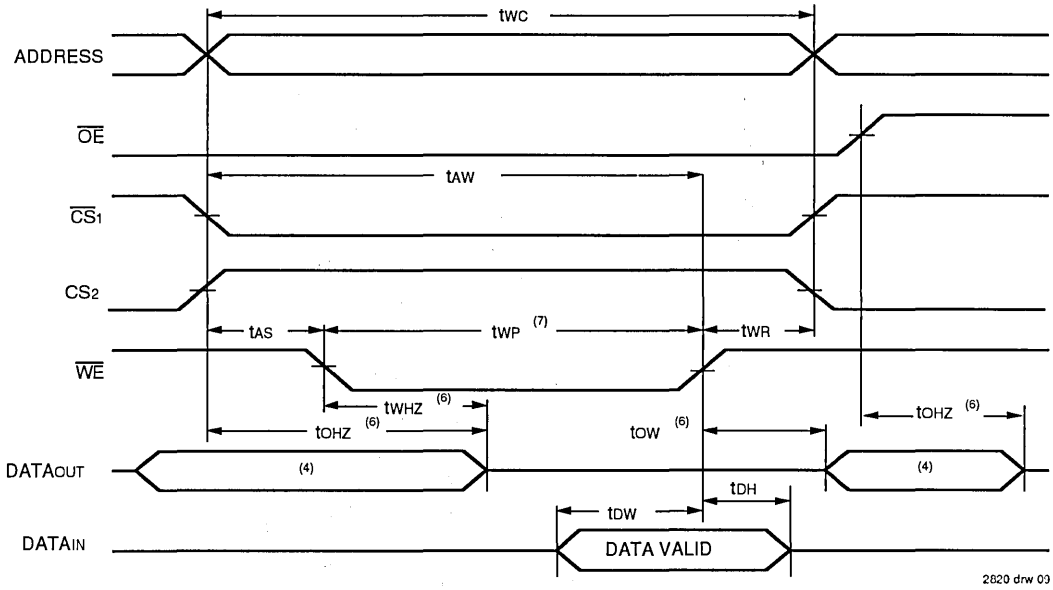
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



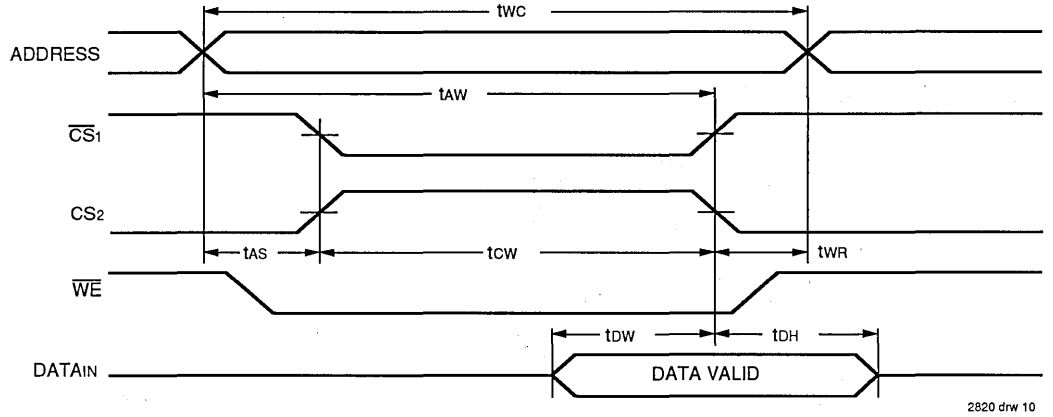
2820 drw 08

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} .
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low, CS_2 transition high.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

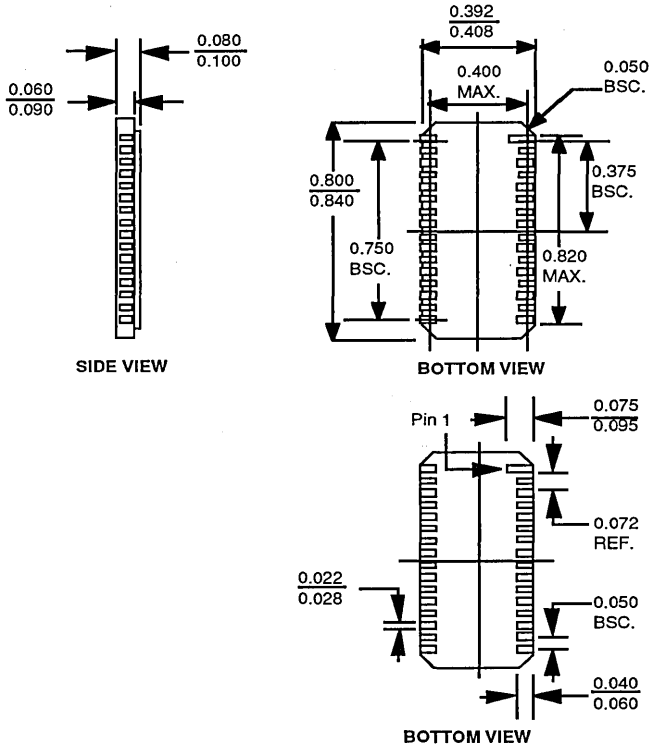


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS_1}$, CS_2 CONTROLLED TIMING)(1, 2, 3, 5)



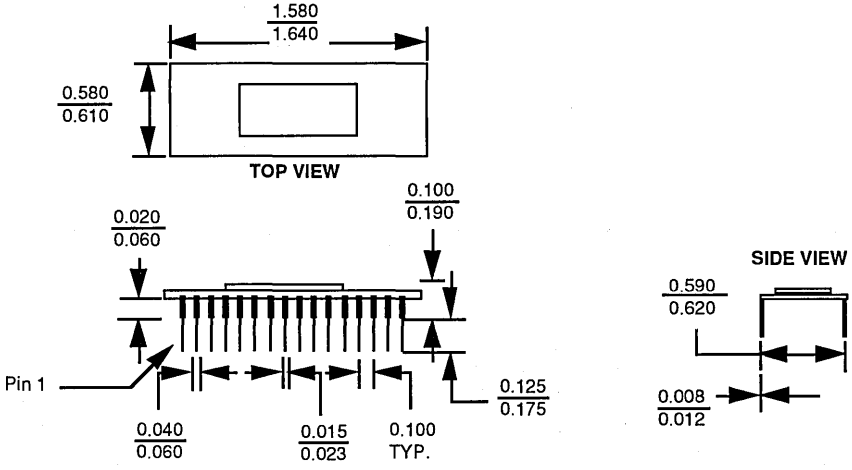
NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$ must be high, or CS_2 must be low during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, high CS_2, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS_1}$ low transition, CS_2 high transition occur simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS
400 MIL BY 820 MIL LCC PACKAGE



2820 drw 11

600 MIL DUAL IN-LINE PACKAGE



2820 drw 12

Integrated Device Technology, Inc.

256KB/ 1MB/ 4MB IDT79R4000 SECONDARY CACHE MODULE BLOCK FAMILY

PRELIMINARY
IDT7MP6074
IDT7MP6084
IDT7MP6094

FEATURES:

- High-speed BiCEMOS™/CEMOS™ secondary cache module block constructed to support the IDT79R4000 CPU
- Available as a pin compatible family to build 256 kilobyte (unified), 1 megabyte (unified) and 4 megabyte (unified or split) secondary caches
- Zero wait-state operation
- Four word line size
- Operating frequencies to support 50MHz and 75MHz IDT79R4000
- Available as a set of four identical high density 80 lead (gold-plated fingers) SIMMs (Single In-Line Memory Modules)
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

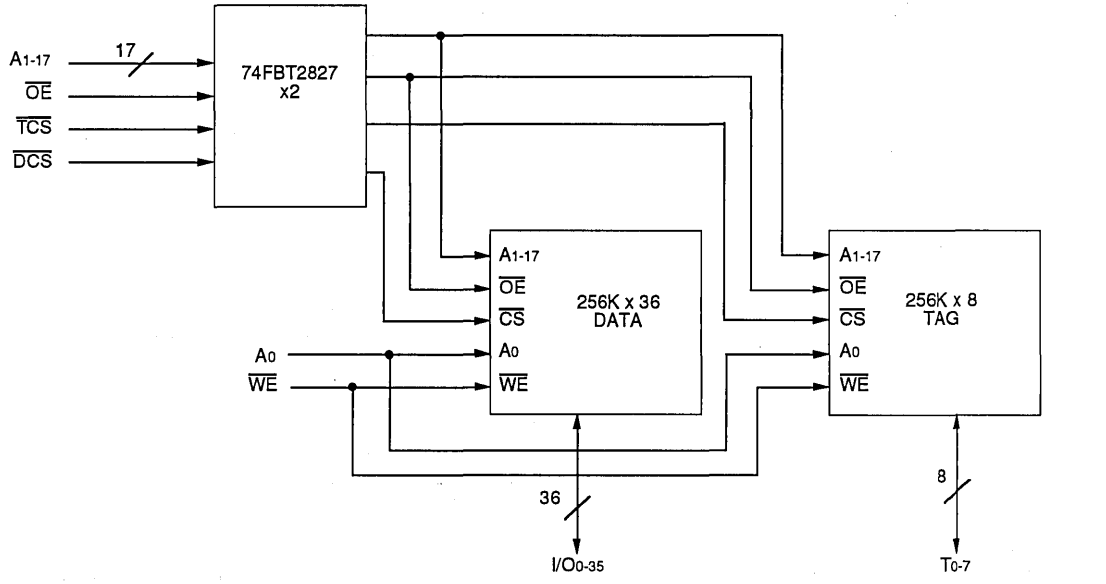
DESCRIPTION:

The IDT7MP6074 is a 256 kilobyte IDT79R4000 secondary cache module block constructed on a multilayer epoxy laminate substrate (FR-4), using 11 16K x 4 static RAMs and 2 IDT74FBT2827 drivers. The IDT7MP6084 is a 1 megabyte IDT79R4000 secondary cache module block using 11 64K x 4 static RAMs, and the IDT7MP6094 is a 4 megabyte IDT79R4000 secondary cache module block using 11 256K x 4 static RAMs. The IDT74FBT2827 has internal 25W series resistors and BiCEMOS™ I/Os resulting in the fastest propagation times with minimal overshoot and ringing. Four identical cache module blocks comprise a full secondary cache.

The IDT7MP6074/84/94 support use in an IDT79R4000-based system at speeds of 50MHz and 75MHz with zero wait-state operation. These Module support a four word line size. For other line sizes, please consult factory.

All inputs and outputs of the IDT7MP6074/84/94 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation.

FUNCTIONAL BLOCK DIAGRAM



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BiCEMOS and CEMOS are trademarks of Integrated Device Technology Inc.

PIN CONFIGURATION

Vcc	2	1	GND
I/O1	4	3	I/O0
I/O3	6	5	I/O2
I/O5	8	7	I/O4
GND	10	9	I/O6
I/O8	12	11	I/O7
I/O10	14	13	I/O9
I/O12	16	15	I/O11
I/O14	18	17	I/O13
I/O15	20	19	GND
I/O17	22	21	I/O16
I/O19	24	23	I/O18
I/O21	26	25	I/O20
GND	28	27	I/O22
I/O23	30	29	Vcc
I/O25	32	31	I/O24
I/O27	34	33	I/O26
I/O29	36	35	I/O28
I/O30	38	37	GND
I/O32	40	39	I/O31
I/O34	42	41	I/O33
GND	44	43	I/O35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
Vcc	54	53	GND
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
GND	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
T0	70	69	$\overline{TCS}$
T1	72	71	GND
T3	74	73	T2
T5	76	75	T4
T7	78	77	T6
GND	80	79	Vcc

2833 drw 02

SIMM
TOP VIEW

PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

2833 tbl 02

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	10	pF
CIN(A)	Input Capacitance (A1-15, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	VIN = 0V	10	pF
CIN(B)	Input Capacitance (A0, $\overline{WE}$)	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2833 tbl 03
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2833 tbl 04
1. VIL = -1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2833 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2833 tbl 01

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

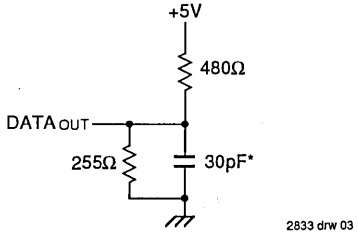
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2833 tbl 06

AC TEST CONDITIONS

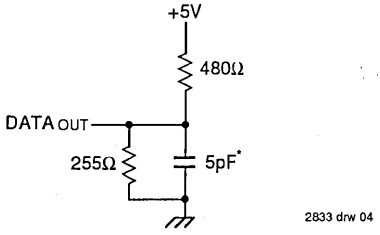
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

2833 tbl 07



2833 drw 03

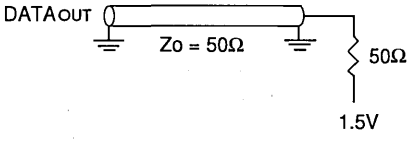
Figure 1. Output Load



2833 drw 04

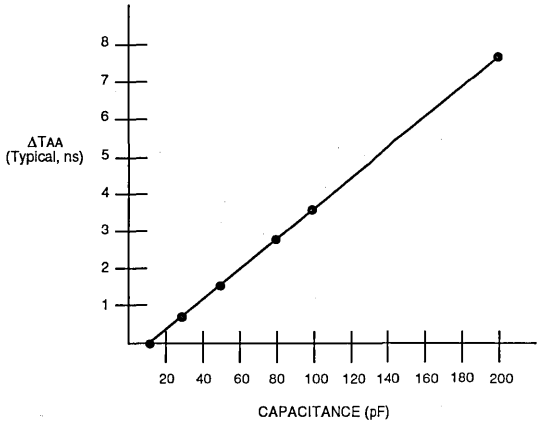
Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.



2833 drw 05

Figure 3. Alternate Output Load



2833 drw 06

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

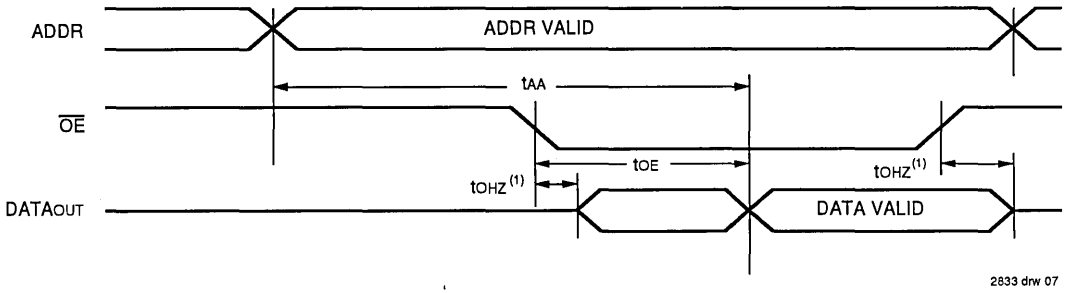
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6074/6084/6094SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{AOA}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{AOW}	A_0 Valid to End of Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End of Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2833 tbl 08

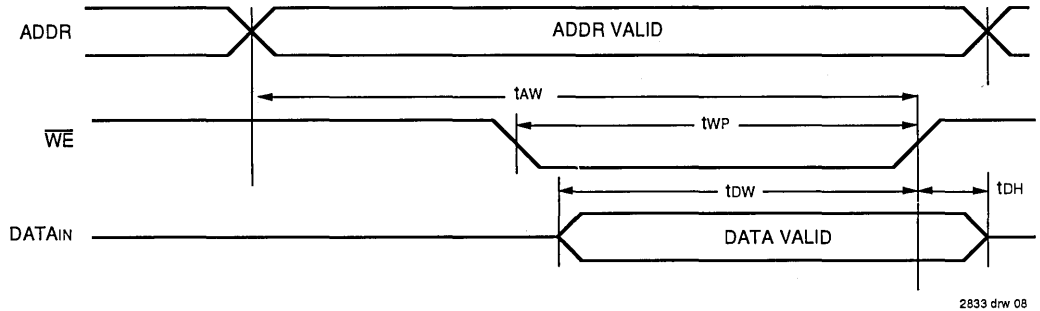
TIMING WAVEFORM OF READ CYCLE(1)



2833 drw 07

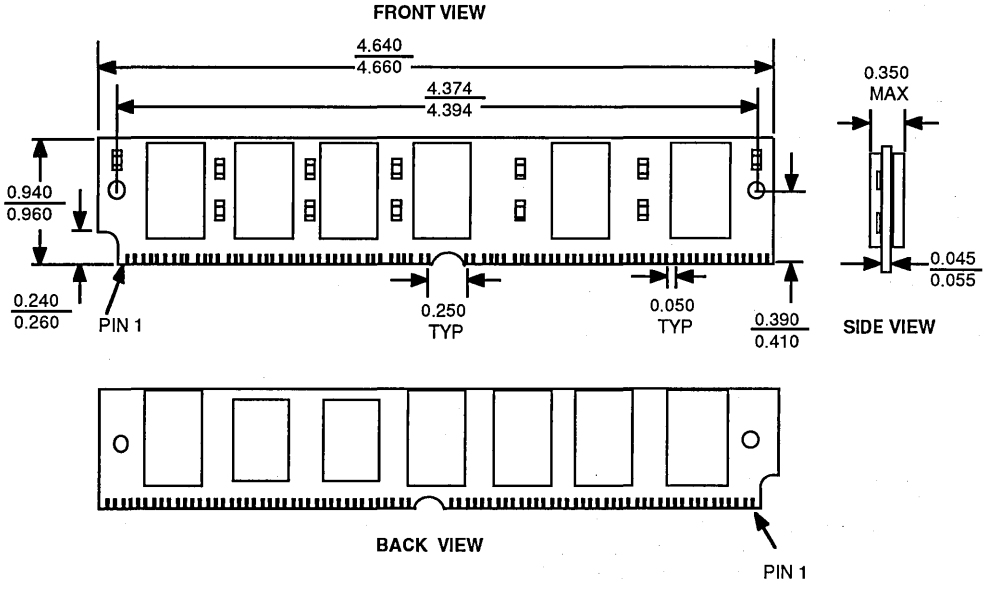
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE



2833 drw 08

PACKAGE DIMENSIONS



2833 drw 09

7

Integrated Device Technology, Inc.

128K/256K BYTE CMOS SECONDARY CACHE MODULE FOR THE INTEL™ i486™

IDT7MP6085
IDT7MP6087

FEATURES:

- 128K/256K byte pin compatible secondary cache modules
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 50MHz
- 80 lead FR-4 SIMM (Single In-line Memory Module)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

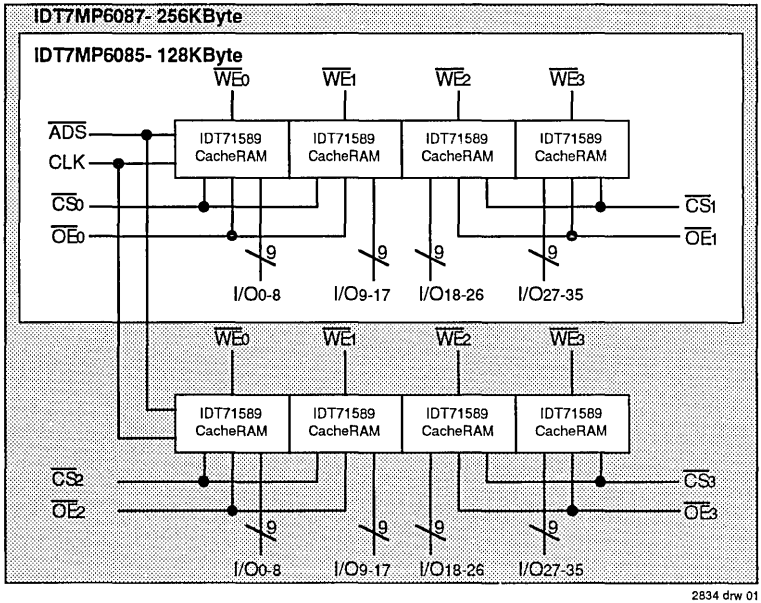
DESCRIPTION:

The IDT7MP6085/7MP6087 are pin compatible secondary cache modules. The IDT7MP6085 is a 128K byte cache and the IDT7MP6087 is a 256K byte cache. The IDT7MP6087 uses eight IDT71589 32K x 9 CacheRAMs in plastic SOJs mounted on two sides of a multilayer epoxy laminate (FR-4) substrate with gold-plated leads while the IDT7MP6085 uses four IDT71589s on one side of the same substrate. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486.

The IDT7MP6085/7MP6087 contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle. An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock. For more details, please consult the IDT71589 datasheet.

The SIMM package allows 80 leads to be placed on a package 4.65 inches long by 0.56 inches tall. The IDT7MP6085 is 0.21 inches thick and the IDT7MP6087 is 0.35 inches thick. The IDT7MP6085/7MP6087 are available to interface with a 50MHz i486. All inputs and outputs of the IDT7MP6085/7MP6087 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



2834 drw 01

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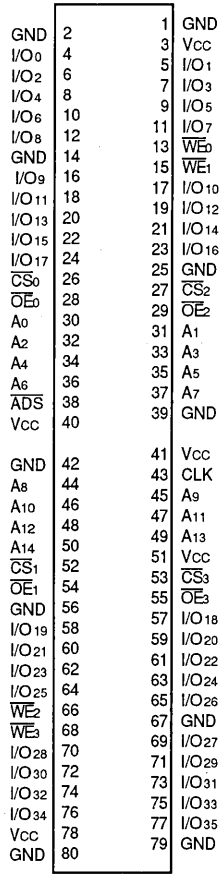
Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION



2834 drw 02

SIMM
TOP VIEW

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
$\overline{CS}_{0-3}$	Word Chip Select/Count Enable
$\overline{WE}_{0-3}$	Byte Write Enables
$\overline{OE}_{0-3}$	Word Output Enables
ADS	Address Status
CLK	System Clock
GND	Ground
VCC	Power

2834 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2834 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5.0V ± 5%

2834 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2834 tbl 04

1. VIL = –3.0V for pulse width less than 5ns.

CAPACITANCE(1)

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	7MP6085/7 Max.	Unit
CIN	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	20	pF
CIN	Input Capacitance (Address, CLK, $\overline{ADS}$)	VIN = 0V	42/70	pF
CI/O	I/O Capacitance	VOUT = 0V	13/20	pF

NOTE: 2834 tbl 05

1. This parameter is guaranteed by design but not tested.

7

TRUTH TABLE[1]

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	DATAOUT	Read
↑	X	H	—	L	L	H	DATAIN	Write
↑	L	X	—	L	L	H	DATAIN	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, "–" = Unrelated, Hi-Z = High Impedance.

2834 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	7MP6085/7 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, CLK, $\overline{ADS}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40/80	µA
$\|I_{LI}\|$	Input Leakage Current ($\overline{CS}$, $\overline{OE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{WE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10/20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10/20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

NOTE:
1. Specifications apply to both the IDT7MP6085 and IDT7MP6087 unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	IDT7MP6085		IDT7MP6087		Unit
			50MHz[1]	25,33,40MHz	50MHz[1]	25,33,40MHz	
I_{CC1}	Operating Power Supply Current	$\overline{CS} \le V_{IL}$ Outputs Open V_{CC} = Max., f = 0[2]	—	520	—	1040	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS} \le V_{IL}$ Outputs Open V_{CC} = Max., f = f_{MAX}[2]	1150	960	2300	1920	mA

NOTES:
1. Preliminary specification only.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

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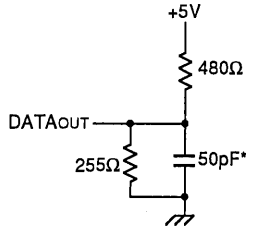
AC TEST CONDITIONS

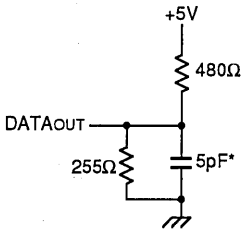
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2834 tbl 09



2834 drw 03

Figure 1. Output Load



2834 drw 04

Figure 1. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

*including scope and jig

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

		7MP6085/6087SxxM								
		50MHz[1]		40MHz		33MHz		25MHz		
Symbol	Name	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCYC	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
tCH	Clock Pulse High	8	—	10	—	11	—	14	—	ns
tCL	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
tS1	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	4	—	5	—	ns
tS2	Set-up Time (Address, Input Data)	5	—	5	—	5	—	6	—	ns
tH1	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	1	—	1	—	ns
tH2	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	2	—	2	—	ns
tADSH	Hold Time ($\overline{ADS}$)	3	—	3	—	3	—	3	—	ns
tCD	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
tDC	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
tOLZ	Output Enable to Output in Lo-Z[2,3]	2	—	2	—	2	—	2	—	ns
tOHZ	Output Disable to Output in Hi-Z[2,3]	—	7	—	8	—	9	—	10	ns

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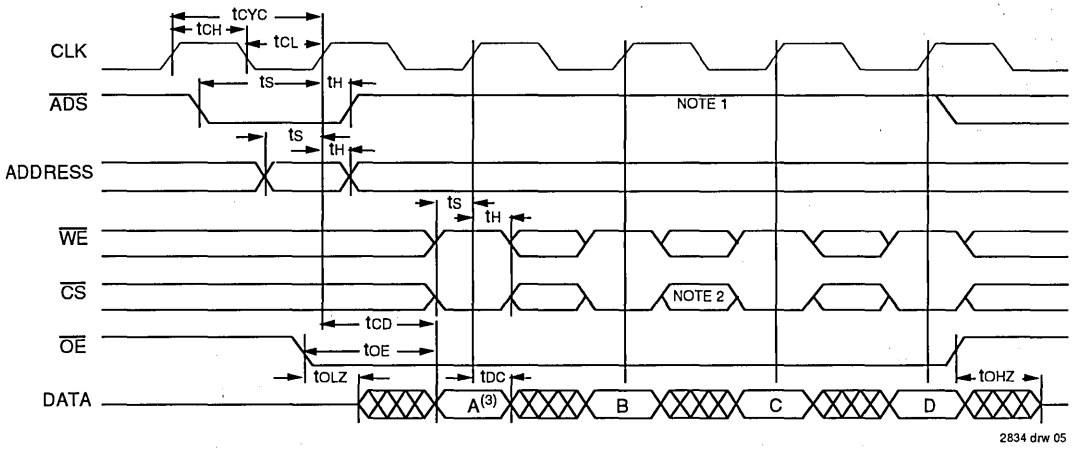
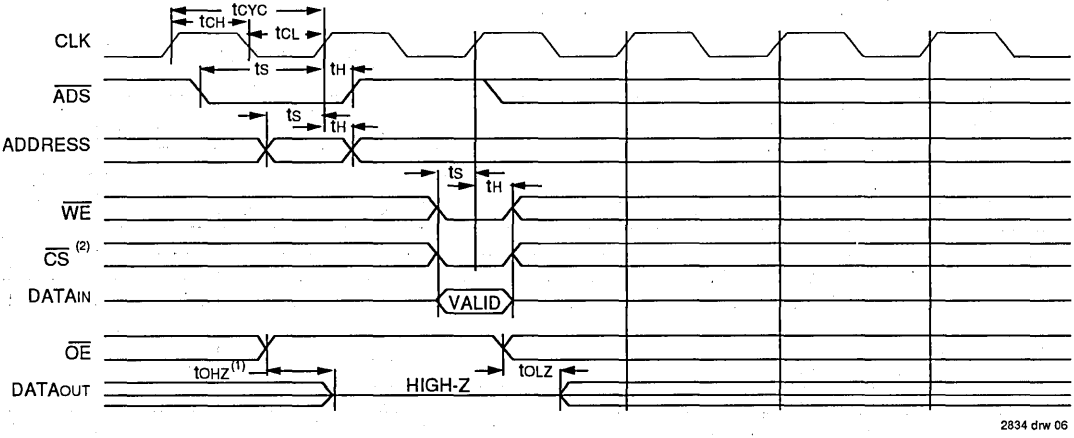
NOTES:
1. Preliminary specifications only.
2. Transition is measured ±200mV from low or high impedance voltage with load (See AC Test Conditions, Figure 2).
3. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF BURST READ CYCLE



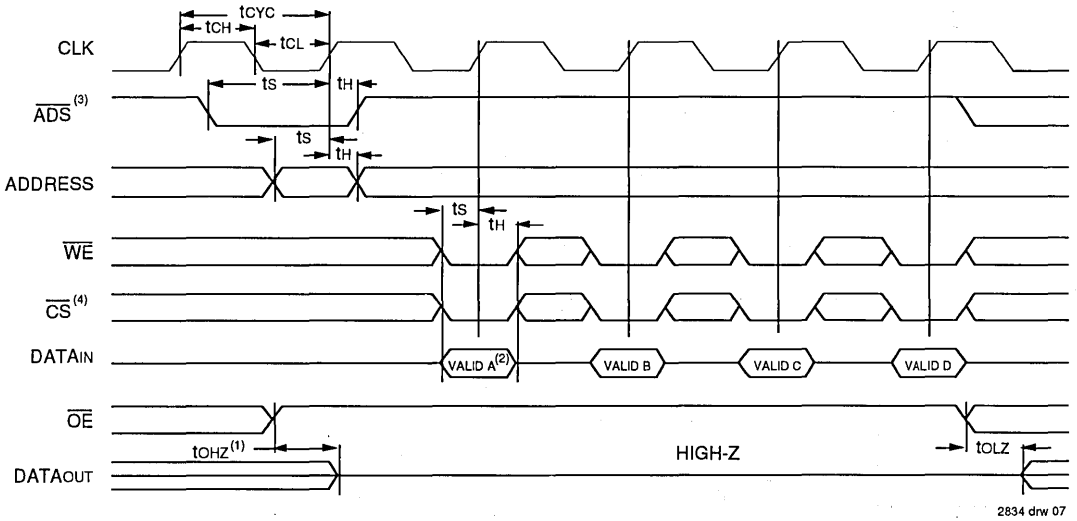
NOTES:
1. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and tH.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A_0}$. C-Data from input address except A_1 is now $\overline{A_1}$. D-Data from input address except A_0 and A_1 are now $\overline{A_0}$ and $\overline{A_1}$.

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as tOHZ + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TIMING WAVEFORM OF BURST WRITE CYCLE



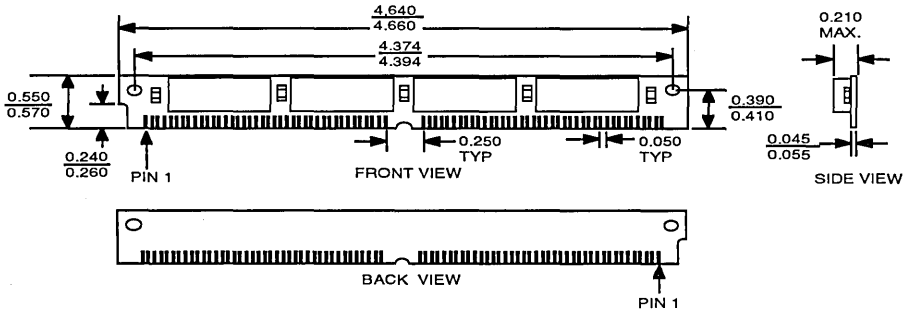
NOTES:

1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

7

PACKAGE DIMENSIONS

IDT7MP6085



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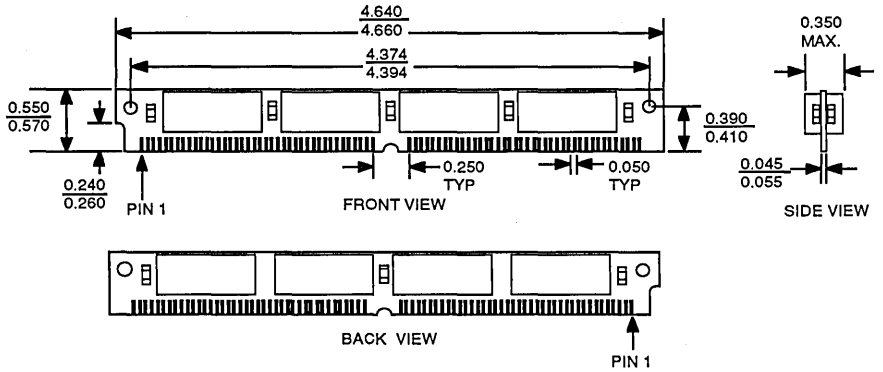
IDT7MP6087



2834 drw 09

Integrated Device Technology, Inc.

128KB SECONDARY CACHE MODULE FOR THE INTEL™ i486™

PRELIMINARY
IDT7MB6089

FEATURES:

- Pin compatible with the Intel 485Turbocache™ 82485MB
- 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache module
- Ideal for use with i486-based systems with an Intel 485Turbocache socket
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and the IDT71B74 cache-tag RAM
- Operates with external i486 speeds of up to 33MHz
- DMA snooping is supported
- 485Turbocache write protect strap, chip select and backoff features are not supported
- 113 lead FR-4 QIP (Quad in-Line Package)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

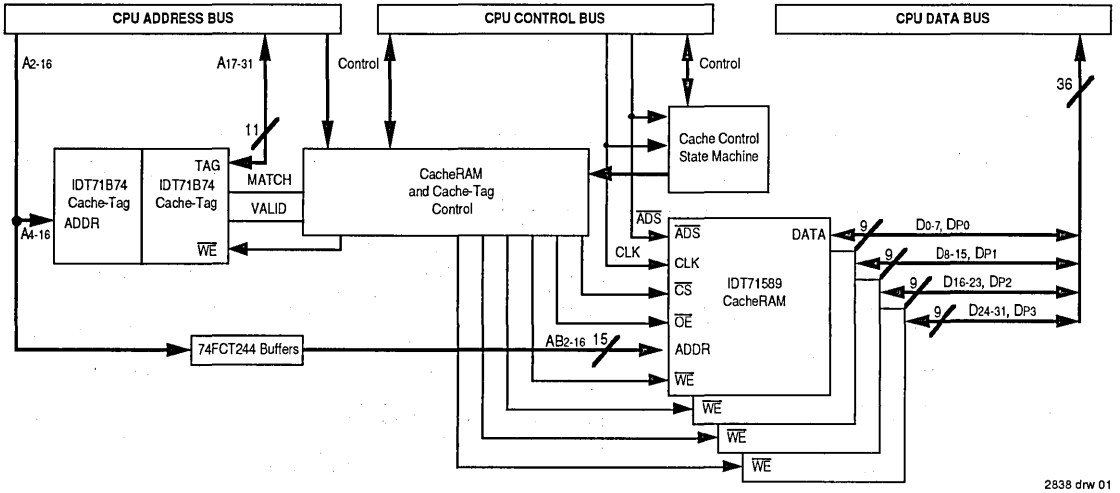
DESCRIPTION:

The IDT7MB6089 is a pin compatible replacement for the Intel 485Turbocache™ 82485MB. The module is a 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache and is ideal for use with many i486-based systems that have an Intel 485Turbocache socket. The IDT7MB6089 uses four IDT71589 32K x 9 CacheRAMs and two IDT71B74 8K x 8 cache-tag RAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board along with logic for cache control. Extremely high speeds are achieved using IDT's high performance, high reliability BiCEMOS™ and CEMOS™ technologies.

An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The quad in-line package (QIP) package configuration allows 113 leads to be placed on a package 2.8 inches long by 2.0 inches wide and 0.25 inches tall. All inputs and outputs of the IDT7MB6089 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



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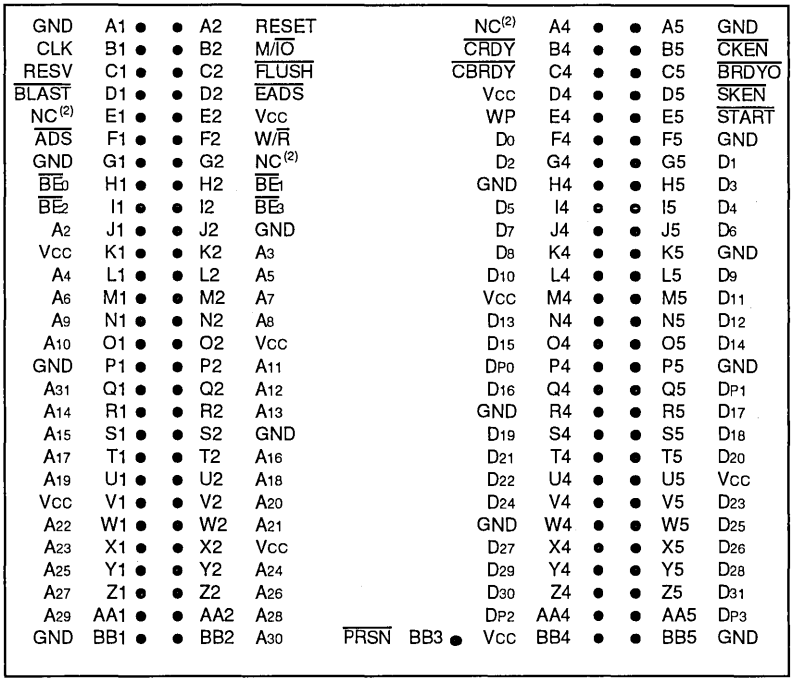
Intel, 485Turbocache and i486 are trademarks of Intel Corp.

PIN CONFIGURATION[1]



QIP
TOP VIEW

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NOTE:

1. Pins E1, G2, and A4 are $\overline{BOFF}$, $\overline{WPSTRP}$, and $\overline{CS}$ on the Intel 485Turbocache respectively. These signals are not used by the IDT7MB6089 and are N.C. (No Connect).

PIN NAMES

Symbol	Parameter	Type	Active	Description
CLK	CLOCK	Input	N/A	This input is the timing reference for all of the IDT7MB6089's functions. It is the same as the i486 CLK input.
RESET	RESET CACHE	Input	High	A synchronous positive-true reset input, which invalidates all cache locations and resets the cache control logic.
$\overline{ADS}$	ADDRESS STROBE	Input	Low	$\overline{ADS}$ is connected to the ADS# pin of the i486 CPU. It is used by the IDT7MB6089 to start any read or write cycle.
M/$\overline{IO}$	MEMORY/IO	Input	N/A	This pin is used by the i486 to indicate whether the current cycle is a memory or I/O cycle. I/O cycles are not cacheable by the IDT7MB6089.
W/$\overline{R}$	WRITE/READ	Input	N/A	Write cycles are indicated by a high level on this pin, and read cycles are indicated by a low level.
$\overline{START}$	MEMORY START	Output	Low	During a cache read miss cycle or a write cycle, the $\overline{START}$ pin signals that the main memory system should service the current access.
$\overline{BRDYO}$	BURST READY OUT	Output	Low	This the IDT7MB6089's means of signaling to the i486 that cache data is ready to be sampled.
$\overline{CBRDY}$	CACHE BURST READY IN	Input	Low	This is the system input to the IDT7MB6089 to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MB6089 during a burst access.
$\overline{CRDY}$	CACHE READY IN	Input	Low	$\overline{CRDY}$ signals to the IDT7MB6089 and the i486 that the main memory data is valid during a non-burst access. Another $\overline{ADS}$ must be generated by the CPU to fetch other words of that cache line from main memory.

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$\overline{BLAST}$	BURST LAST	Input	Low	This i486 output indicates to the IDT7MB6089 cache control logic that the current cycle is the last cycle of a cache burst.
$\overline{BOFF}$	BACKOFF	N/A	N/A	This signal is not used by the IDT7MB6089.
$\overline{PRSN}$	PRESENCE	Output	Low	This pin is hardwired to ground. It tells the system logic that the IDT7MB6089 is plugged into the system.
A_2-A_{31}	PROCESSOR ADDRESSES	Input	N/A	These are the address inputs to the IDT7MB6089. The IDT7MB6089 requires that these signals be valid for the duration of any cache cycle.
$\overline{BE_0}$-$\overline{BE_3}$	BYTE ENABLE	Input	Low	The byte enable inputs are sampled only during CPU write cycles and are only used to control byte writes to valid cache lines during write hit cycles. The timing is the same as for the address input pins.
$\overline{CS}$	CHIP SELECT	N/A	N/A	This signal is not used by the IDT7MB6089.
D_0-D_{31}	PROCESSOR DATA LINES	I/O	N/A	These are the data inputs from either the i486 or the system memory. D_0-D_7 define the least significant byte while D_{24}-D_{31} define the most significant byte.
DP_0-DP_3	DATA PARITY	I/O	N/A	These are the parity bits from either the i486 or the system memory. The timing requirements are the same as the data lines.
$\overline{CKEN}$	CACHE ENABLE TO CPU	Output	Low	This signal is the cache enable signal generated by the IDT7MB6089. The IDT7MB6089 will always assert $\overline{CKEN}$ during T1 cycles and during read hit cycles before the last $\overline{BRDYO}$. The IDT7MB6089 will not assert $\overline{CKEN}$ during read miss cycles.
$\overline{SKEN}$	SYSTEM CACHE ENABLE	Input	Low	This signal is generated by the system to indicate that a line is cacheable. The IDT7MB6089 will look for $\overline{SKEN}$ to be active during the cycle before the first word transfer and the cycle before the last word transfer of a line fill.
$\overline{FLUSH}$	FLUSH CACHE	Input	Low	This signal causes the IDT7MB6089 to invalidate its entire cache contents.
WP	WRITE PROTECT	Input	High	The write protect input is only sampled during write cycles. If this signal is asserted during a write hit cycle, the current cache data will not be overwritten.
$\overline{WPSTRP}$	WRITE PROTECT STRAP	N/A	N/A	This signal is not used by the IDT7MB6089.
$\overline{EADS}$	VALID EXTERNAL ADDRESS	Input	Low	This signal indicates that an invalidation address is present on the IDT7MB6089 address bus.

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FUNCTIONAL DESCRIPTION:

BASIC OPERATION

All operations of the IDT7MB6089 fall into the following cycles: reset, read hit, read miss, write hit, write miss and invalidation. For proper operation during any of the above cycles (except reset) the address to the IDT7MB6089 must be held valid for the duration of the cycle. For read or write cycles, the M/$\overline{IO}$ pin must be held high for the duration of the cycle, or the IDT7MB6089 will consider the cycle an I/O cycle (which is not cacheable by the IDT7MB6089). The W/$\overline{R}$ pin must also be held valid for the duration of the read or write cycle. For reset and invalidation cycles the state of the M/$\overline{IO}$ and W/$\overline{R}$ pins are not checked.

RESET

The IDT7MB6089 is reset when RESET is asserted. Asserting RESET will invalidate the entire contents of the cache, and reset the control logic of the cache. If RESET is asserted, no other control signals will be recognized.

READ MISS

A read cycle is initiated by the assertion of $\overline{ADS}$ with M/$\overline{IO}$ high and W/$\overline{R}$ low. At the initiation of the cycle, the IDT7MB6089 begins its tag look-up. If the input address is not contained in the cache, a miss has occurred. The IDT7MB6089 will then assert $\overline{START}$ and wait for the main memory system to service the current access. The IDT7MB6089 considers the data returned from the main memory system as cacheable if $\overline{SKEN}$ is asserted at least one cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is asserted.

After it is determined that the current line is cacheable, the IDT7MB6089 invalidates a line in the cache and waits for the main memory system to return data. With each $\overline{CBRDY}$ or $\overline{CRDY}$ assertion, a new data word is loaded into the cache.

READ HIT

A read hit cycle is initiated in the same manner described above for a read miss cycle. But in this case when the IDT7MB6089 does its tag look-up, the input address is contained in the cache indicating a read hit. The IDT7MB6089 will transfer a line of data with the first word being valid in the first T2 cycle. The IDT7MB6089 then transfers a new data word in each subsequent T2 cycle until $\overline{BLAST}$ is asserted to the module. The IDT7MB6089 also forces $\overline{START}$ high and $\overline{BRDYO}$ low starting in the first T2 cycle and will hold them at those levels for subsequent T2 cycles. $\overline{CKEN}$ is asserted during the T1 cycle and again in the second and subsequent T2 cycles.

WRITE MISS

Since the IDT7MB6089 is a write through cache, write misses are ignored.

WRITE HIT

A write cycle is initiated by the assertion of $\overline{ADS}$ with M/$\overline{IO}$ high and W/$\overline{R}$ high. At the initiation of the cycle, the IDT7MB6089 begins its tag look-up. If the input address is contained in the cache, the cache contents will be updated in the first T2 cycle if the WP input is low. If the WP input is high during a write hit the line is seen as write protected and the write is ignored.

INVALIDATION

An invalidation is initiated by the assertion of EADS in a Ti or T1 cycle. At the initiation of an invalidation, the IDT7MB6089 begins its tag look-up. If the line is found in the cache, the line will be invalidated. The IDT7MB6089 requires two cycles after the assertion of EADS to invalidate a line; therefore, invalidations can only occur every third cycle. Invalidations will be ignored by the IDT7MB6089 during T2 cycles.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2838 tbl 03

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2838 tbl 04

NOTE:
1. V_{IL} = –3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2838 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	30	µA
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	10	µA
$\|I_{LI}\|$	Input Leakage Current (CLK, $\overline{ADS}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{IH}\|$	Input High Current (Control)	V_{CC} = Max, V_{IN} = V_{CC}	—	1.0	mA
$\|I_{IL}\|$	Input Low Current (Control)	V_{CC} = Max, V_{IN} = GND	—	260	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OLD}	Output Low Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OLC}	Output Low Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min.	—	0.5	V
V_{OHD}	Output High Voltage (Data)	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output High Voltage (Control)	I_{OH} = –2mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1900	mA

2838 tbl 06

CAPACITANCE[1]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance (Address)	V_{IN} = 0V	25	pF
C_{IN}	Input Capacitance (Control)	V_{IN} = 0V	25	pF
C_{IN}	Input Capacitance (CLK)	V_{IN} = 0V	40	pF
C_{IN}	Input Capacitance ($\overline{ADS}$)	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance ($\overline{BRDYO}$)	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance (START, $\overline{SKEN}$)	V_{IN} = 0V	15	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	10	pF

2838 tbl 07

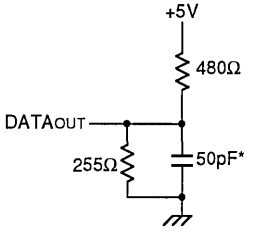
NOTE:
1. These parameters are guaranteed by design but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

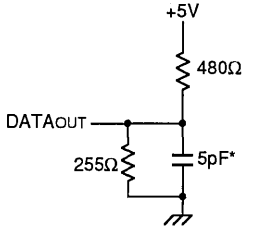
2838 tbl 08

7



2838 drw 03

Figure 1. Output Load



2838 drw 04

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

AC ELECTRICAL CHARACTERISTICS

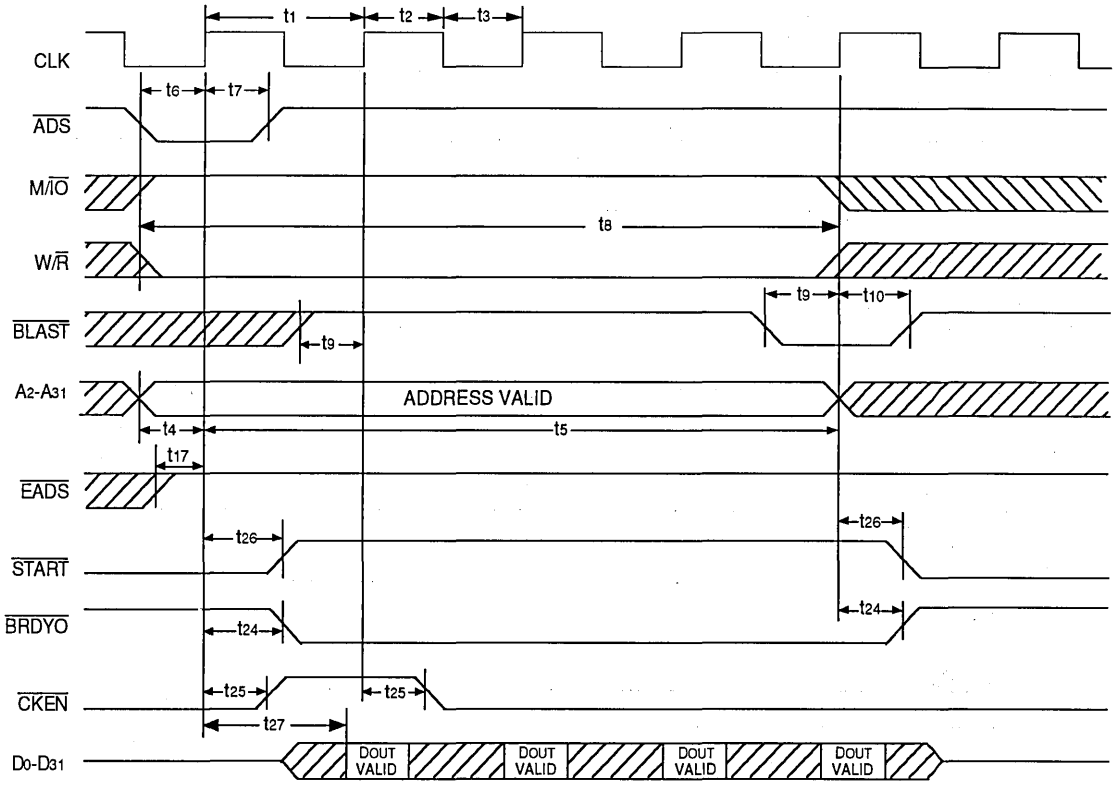
(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

		7MB6089SxxK				
		33MHz		25MHz		
Symbol	Name	Min.	Max.	Min.	Max.	Unit
t_1	Clock Period	30	—	40	—	ns
t_2	Clock High Time	11	—	14	—	ns
t_3	Clock Low Time	11	—	14	—	ns
t_4	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Setup Time	13	—	17	—	ns
t_5	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Hold Time	(see note 1)	—	(see note 1)	—	ns
t_6	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Setup Time	13	—	20	—	ns
t_7	$\overline{ADS}$ Hold Time	3	—	3	—	ns
t_8	M/$\overline{IO}$, W/$\overline{R}$ Hold Time	(see note 1)	—	(see note 1)	—	ns
t_9	$\overline{BLAST}$ Setup Time	9	—	10	—	ns
t_{10}	$\overline{BLAST}$ Hold Time	3	—	3	—	ns
t_{11}	$\overline{CRDY}$, $\overline{CBRDY}$ Setup Time	11	—	11	—	ns
t_{12}	$\overline{CRDY}$, $\overline{CBRDY}$ Hold Time	3	—	3	—	ns
t_{13}	$\overline{SKEN}$ Setup Time	9	—	9	—	ns
t_{14}	$\overline{SKEN}$ Hold Time	3	—	3	—	ns
t_{15}	D_0-D_{31}, DP_0-DP_3 Setup Time	5	—	5	—	ns
t_{16}	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	3	—	ns
t_{17}	$\overline{EADS}$ Setup Time	9	—	9	—	ns
t_{18}	$\overline{EADS}$ Hold Time	3	—	3	—	ns
t_{19}	A_4-A_{31} Setup Time (Snoop)	6	—	6	—	ns
t_{20}	A_4-A_{31} Hold Time (Snoop)	67	—	87	—	ns
t_{21}	RESET, $\overline{FLUSH}$ Setup Time	9	—	9	—	ns
t_{22}	RESET, $\overline{FLUSH}$ Hold Time	3	—	3	—	ns
t_{23}	RESET, $\overline{FLUSH}$ Pulse Width	80	—	80	—	ns
t_{24}	$\overline{BRDYO}$ Valid	—	16	—	22	ns
t_{25}	$\overline{CKEN}$ Valid	—	15	—	18	ns
t_{26}	$\overline{START}$ Valid	—	16	—	22	ns
t_{27}	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit)	—	24	—	30	ns
t_{28}	WP Setup Time	15	—	15	—	ns
t_{29}	WP Hold Time	—	3	—	3	ns

NOTE:
1. The address, M/$\overline{IO}$ and W/$\overline{R}$ inputs to the IDT7MB6089 must be held valid for the duration of the read, write or invalidation cycle.

2838 tbl 09

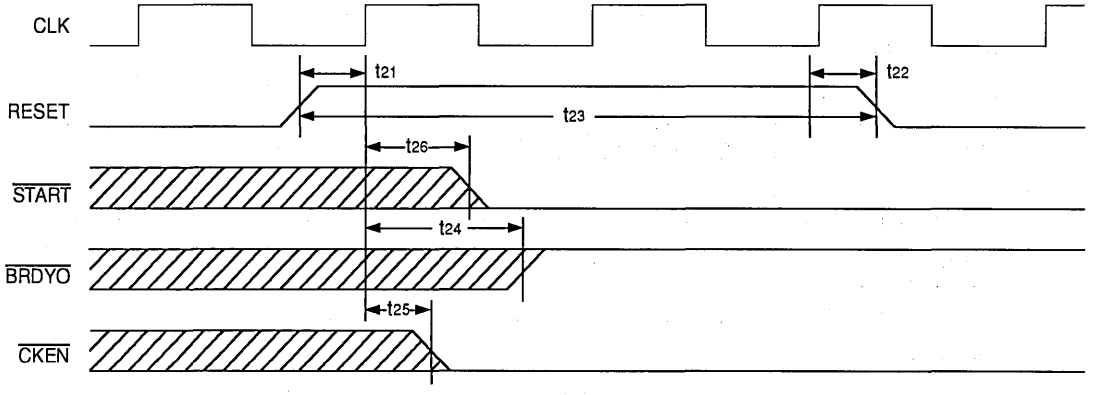
TIMING WAVEFORM OF A READ HIT CYCLE (READ LINE)(1)



NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH.

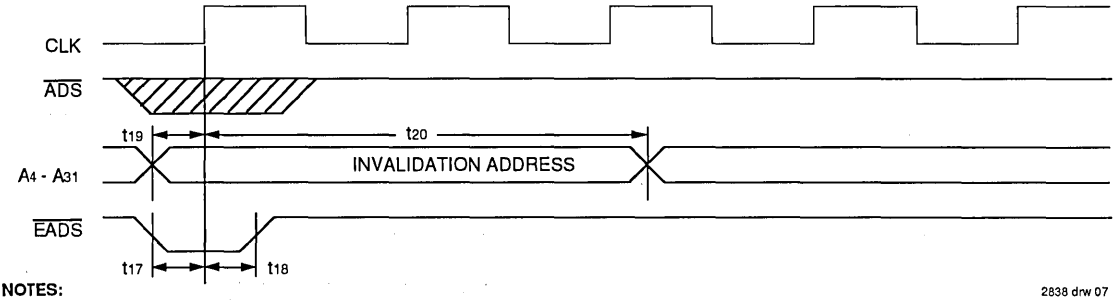
2838 drw 05

TIMING WAVEFORM OF A RESET OPERATION



2838 drw 06

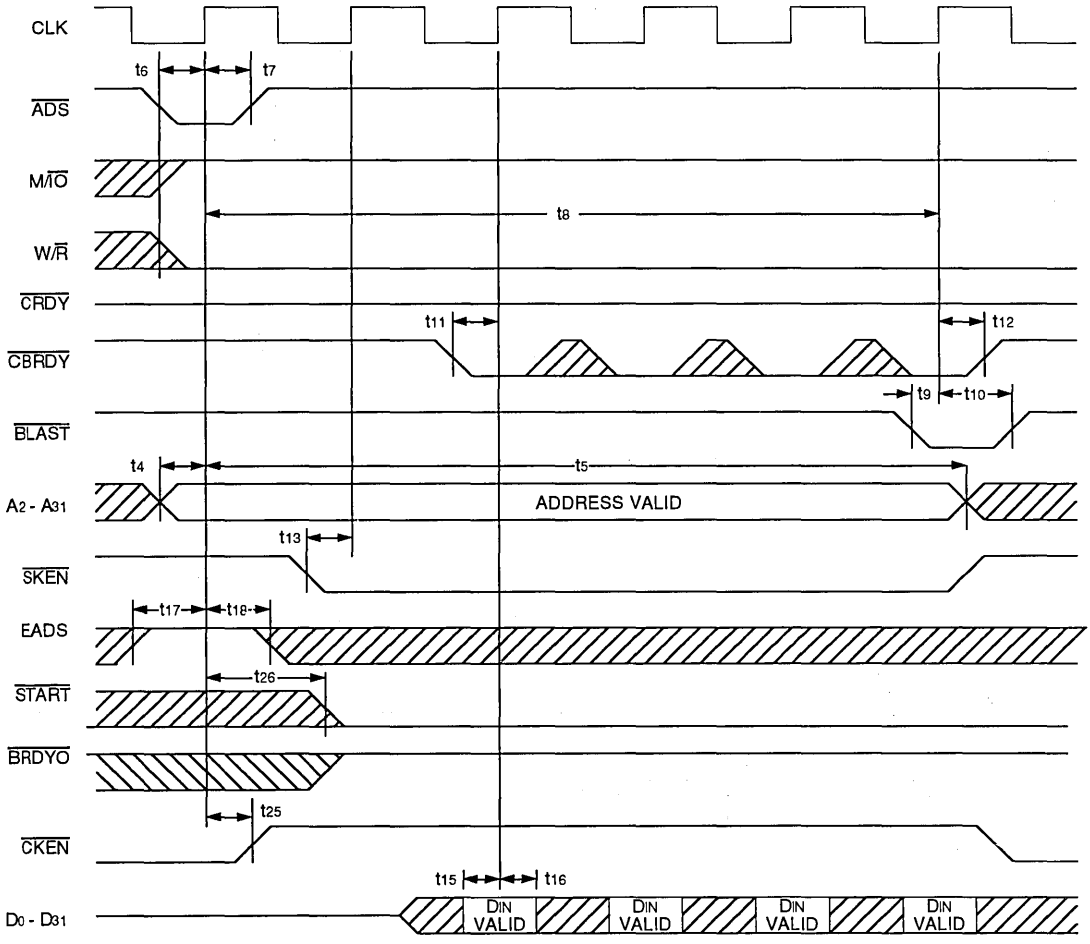
TIMING WAVEFORM OF A CACHE INVALIDATION(1,2)



2838 drw 07

NOTES:
1. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored.
2. $\overline{EADS}$ is only recognized when the cache is idle (Ti) or at the beginning of a CACHE cycle (T1). $\overline{EADS}$ is ignored while the cache is processing any other request.

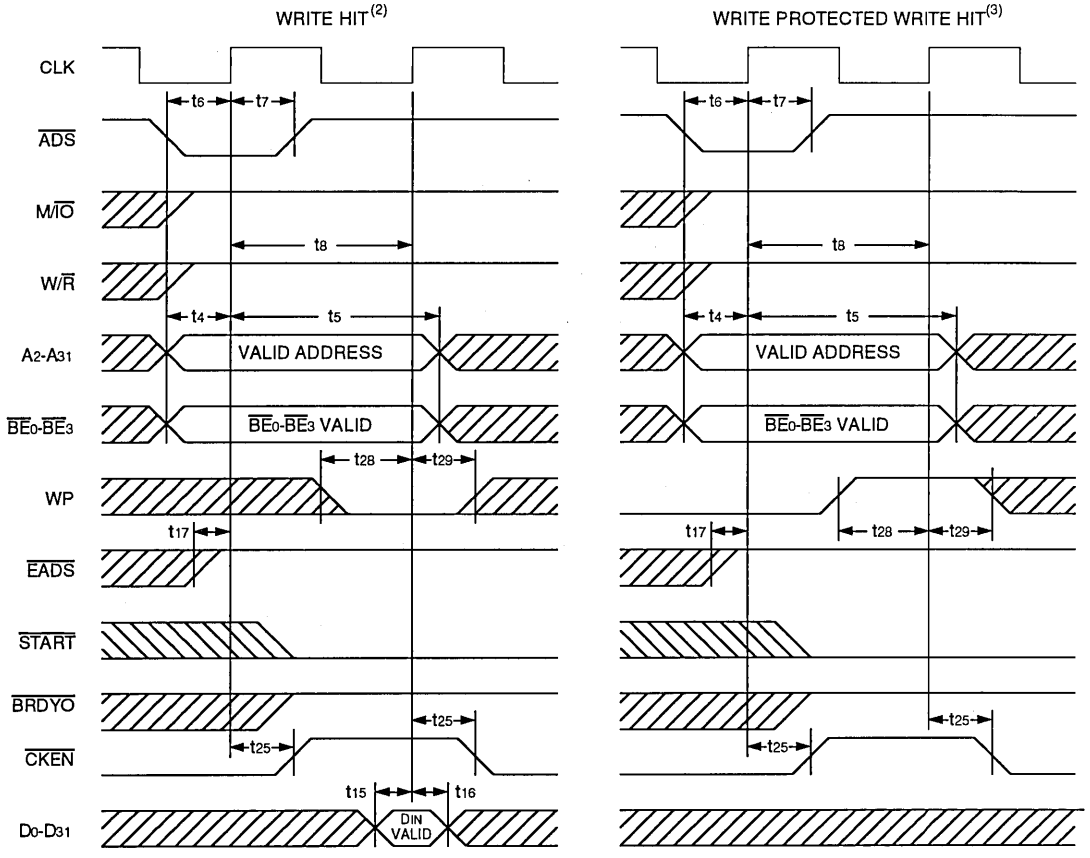
TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)(1)



2838 drw 08

NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH.

TIMING WAVEFORM OF A WRITE HIT(1)



NOTES:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH.
2. For a write hit, data in the IDT7MB6089 is updated.
3. For a write protected write hit, the data in the IDT7MB6089 is not updated.

2838 drw 09

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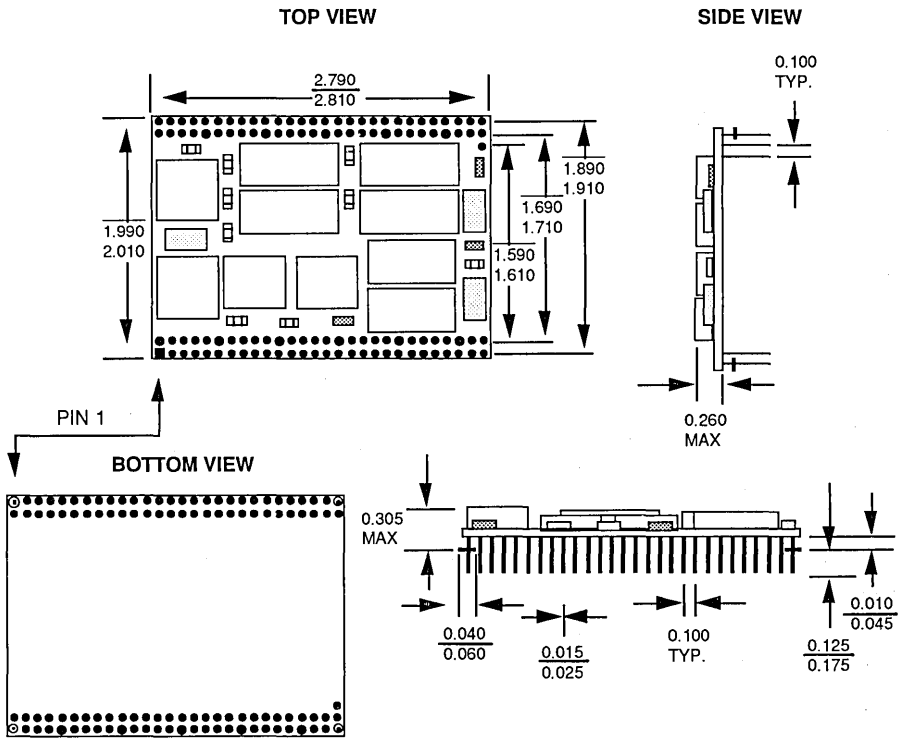
PACKAGE DIMENSIONS



2838 drw 10

Integrated Device Technology, Inc.

128KB SECONDARY CACHE MODULE FOR THE INTEL™ i486™

PRELIMINARY
IDT7MB6091

FEATURES:

- Pin compatible with the Intel 485Turbocache™ 82485MB
- 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache module
- Ideal for use with i486-based systems with an Intel 485Turbocache socket
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and the IDT71B74 cache-tag RAM
- Operates with external i486 speeds of up to 33MHz
- Concurrent snooping is supported
- 485Turbocache write protect strap feature is not supported
- 113 lead FR-4 QIP (Quad in-Line Package)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

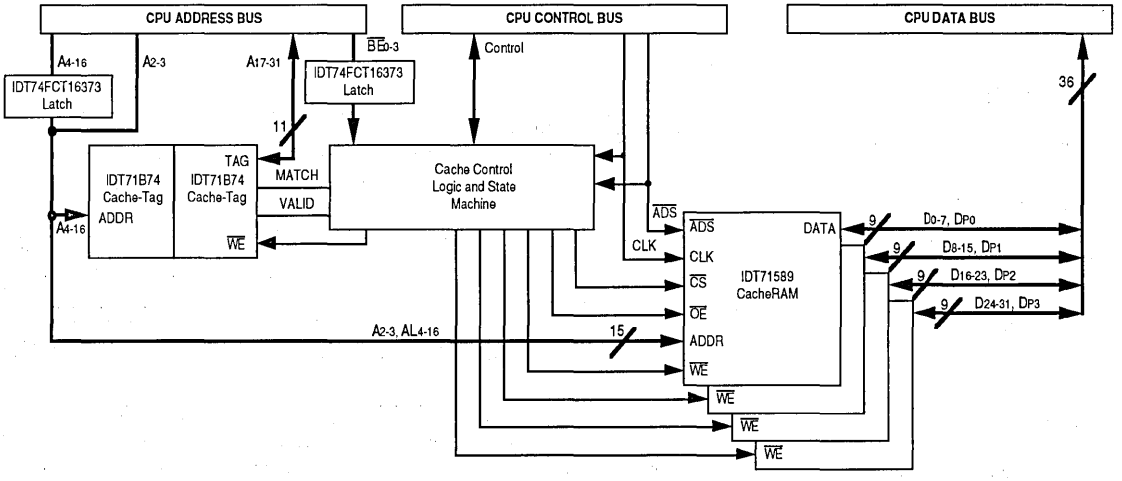
DESCRIPTION:

The IDT7MB6091 is a pin compatible replacement for the Intel 485Turbocache™ 82485MB. The module is a 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache and is ideal for use with many i486-based systems that have an Intel 485Turbocache socket. The IDT7MB6091 uses four IDT71589 32K x 9 CacheRAMs, two IDT71B74 8K x 8 cache-tag RAMs and two IDT74FCT16373 Double-Density™ 16-bit latches in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board along with logic for cache control. Extremely high speeds are achieved using IDT's high performance, high reliability BiCEMOS™ and CEMOS™ technologies.

An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The quad in-line package (QIP) package configuration allows 113 leads to be placed on a package 2.9 inches long by 2.0 inches wide and 0.25 inches tall. All inputs and outputs of the IDT7MB6091 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



2844 drw 01

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Intel, 485Turbocache and i486 are trademarks of Intel Corp.

PIN CONFIGURATION[1]

GND	A1	●	●	A2	RESET		$\overline{CS}$	A4	●	●	A5	GND
CLK	B1	●	●	B2	M/$\overline{IO}$		$\overline{CRDY}$	B4	●	●	B5	$\overline{CKEN}$
RESV	C1	●	●	C2	$\overline{FLUSH}$		$\overline{CBRDY}$	C4	●	●	C5	$\overline{BRDYO}$
$\overline{BLAST}$	D1	●	●	D2	$\overline{EADS}$		V_{CC}	D4	●	●	D5	$\overline{SKEN}$
$\overline{BOFF}$	E1	●	●	E2	V_{CC}		WP	E4	●	●	E5	$\overline{START}$
$\overline{ADS}$	F1	●	●	F2	W/$\overline{R}$		D_0	F4	●	●	F5	GND
GND	G1	●	●	G2	NC[2]		D_2	G4	●	●	G5	D_1
$\overline{BE_0}$	H1	●	●	H2	$\overline{BE_1}$		GND	H4	●	●	H5	D_3
$\overline{BE_2}$	I1	●	●	I2	$\overline{BE_3}$		D_5	I4	●	●	I5	D_4
A_2	J1	●	●	J2	GND		D_7	J4	●	●	J5	D_6
V_{CC}	K1	●	●	K2	A_3		D_8	K4	●	●	K5	GND
A_4	L1	●	●	L2	A_5		D_{10}	L4	●	●	L5	D_9
A_6	M1	●	●	M2	A_7		V_{CC}	M4	●	●	M5	D_{11}
A_9	N1	●	●	N2	A_8		D_{13}	N4	●	●	N5	D_{12}
A_{10}	O1	●	●	O2	V_{CC}		D_{15}	O4	●	●	O5	D_{14}
GND	P1	●	●	P2	A_{11}		D_{P0}	P4	●	●	P5	GND
A_{31}	Q1	●	●	Q2	A_{12}		D_{16}	Q4	●	●	Q5	D_{P1}
A_{14}	R1	●	●	R2	A_{13}		GND	R4	●	●	R5	D_{17}
A_{15}	S1	●	●	S2	GND		D_{19}	S4	●	●	S5	D_{18}
A_{17}	T1	●	●	T2	A_{16}		D_{21}	T4	●	●	T5	D_{20}
A_{19}	U1	●	●	U2	A_{18}		D_{22}	U4	●	●	U5	V_{CC}
V_{CC}	V1	●	●	V2	A_{20}		D_{24}	V4	●	●	V5	D_{23}
A_{22}	W1	●	●	W2	A_{21}		GND	W4	●	●	W5	D_{25}
A_{23}	X1	●	●	X2	V_{CC}		D_{27}	X4	●	●	X5	D_{26}
A_{25}	Y1	●	●	Y2	A_{24}		D_{29}	Y4	●	●	Y5	D_{28}
A_{27}	Z1	●	●	Z2	A_{26}		D_{30}	Z4	●	●	Z5	D_{31}
A_{29}	AA1	●	●	AA2	A_{28}		D_{P2}	AA4	●	●	AA5	D_{P3}
GND	BB1	●	●	BB2	A_{30}	$\overline{PRSN}$	BB3	●	V_{CC}	BB4	●	●	BB5	GND

QIP
TOP VIEW

2844 drw 02

NOTE:
1.Pin G2 is $\overline{WPSTRP}$ on the Intel 485Turbocache. This signal is not used by the IDT7MB6091 and is N.C. (No Connect).

PIN NAMES

Symbol	Parameter	Type	Active	Description
CLK	CLOCK	Input	N/A	This input is the timing reference for all of the IDT7MB6091's functions. It is the same as the i486 CLK input.
RESET	RESET CACHE	Input	High	A synchronous positive-true reset input, which invalidates all cache locations and resets the cache control logic.
$\overline{ADS}$	ADDRESS STROBE	Input	Low	$\overline{ADS}$ is connected to the ADS# pin of the i486 CPU. It is used by the IDT7MB6091 to start any read or write cycle. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	MEMORY/IO	Input	N/A	This pin is used by the i486 to indicate whether the current cycle is a memory or I/O cycle. I/O cycles are not cacheable by the IDT7MB6091.
W/$\overline{R}$	WRITE/READ	Input	N/A	Write cycles are indicated by a high level on this pin, and read cycles are indicated by a low level.
$\overline{START}$	MEMORY START	Output	Low	During a cache read miss cycle or a write cycle, the $\overline{START}$ pin signals that the main memory system should service the current access.
$\overline{BRDYO}$	BURST READY OUT	Output	Low	This the IDT7MB6091's means of signaling to the i486 that cache data is ready to be sampled.
$\overline{CBRDY}$	CACHE BURST READY IN	Input	Low	This is the system input to the IDT7MB6091 to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MB6091 during a burst access.
$\overline{CRDY}$	CACHE READY IN	Input	Low	$\overline{CRDY}$ signals to the IDT7MB6091 and the i486 that the main memory data is valid during a non-burst access. Another $\overline{ADS}$ must be generated by the CPU to fetch other words of that cache line from main memory.

2844 tbl 01

$\overline{BLAST}$	BURST LAST	Input	Low	This i486 output indicates to the IDT7MB6091 cache control logic that the current cycle is the last cycle of a cache burst.
$\overline{BOFF}$	BACKOFF	Input	Low	This signal is used to stall the IDT7MB6091. The IDT7MB6091 will also put its data bus into a high-impedance state. The IDT7MB6091 will only recognize invalidation cycles when $\overline{BOFF}$ is asserted.
$\overline{PRSN}$	PRESENCE	Output	Low	This pin is hardwired to ground. It tells the system logic that the IDT7MB6091 is plugged into the system.
A_{2}-A_{31}	PROCESSOR ADDRESSES	Input	N/A	These are the address inputs to the IDT7MB6091.
$\overline{BE_{0}}$-$\overline{BE_{3}}$	BYTE ENABLE	Input	Low	The byte enable inputs are sampled only during CPU write cycles and are only used to control byte writes to valid cache lines during write hit cycles. The timing is the same as for the address input pins.
$\overline{CS}$	CHIP SELECT	Input	Low	Chip select can be used for depth expansion. $\overline{CS}$ must be low for $\overline{EADS}$ or $\overline{ADS}$ to be recognized by the IDT7MB6091.
D_{0}-D_{31}	PROCESSOR DATA LINES	I/O	N/A	These are the data inputs from either the i486 or the system memory. D_{0}-D_{7} define the least significant byte while D_{24}-D_{31} define the most significant byte.
DP_{0}-DP_{3}	DATA PARITY	I/O	N/A	These are the parity bits from either the i486 or the system memory. The timing requirements are the same as the data lines.
$\overline{CKEN}$	CACHE ENABLE TO CPU	Output	Low	This signal is the cache enable signal generated by the IDT7MB6091. The IDT7MB6091 will always assert $\overline{CKEN}$ during T1 cycles and during read hit cycles before the last $\overline{BRDYO}$. The IDT7MB6091 will not assert $\overline{CKEN}$ during read miss cycles.
$\overline{SKEN}$	SYSTEM CACHE ENABLE	Input	Low	This signal is generated by the system to indicate that a line is cacheable. The IDT7MB6091 will look for $\overline{SKEN}$ to be active during the cycle before the first word transfer and the cycle before the last word transfer of a line fill.
$\overline{FLUSH}$	FLUSH CACHE	Input	Low	This signal causes the IDT7MB6091 to invalidate its entire cache contents.
WP	WRITE PROTECT	Input	High	The write protect input is only sampled during write cycles. If this signal is asserted during a write hit cycle, the current cache data will not be overwritten.
$\overline{WPSTRP}$	WRITE PROTECT STRAP	N/A	N/A	This signal is not used by the IDT7MB6091.
$\overline{EADS}$	VALID EXTERNAL ADDRESS	Input	Low	This signal indicates that an invalidation address is present on the IDT7MB6091 address bus. $\overline{CS}$ must be low for $\overline{EADS}$ to be recognized by the IDT7MB6091.

2844 tbl 02

FUNCTIONAL DESCRIPTION:

BASIC OPERATION

The IDT7MB6091 is a complete secondary cache subsystem designed to replace the Intel Turbocache485. The IDT7MB6091 is designed to support zero wait state line reads, i.e. four words of data in five clocks. The IDT7MB6091 supports all of the following bus cycles: read hit, read miss, write hit, write miss, invalidation and backoff. The IDT7MB6091 also features single pin reset and cache flush capabilities.

The IDT7MB6091 latches the address at the input of the module at the beginning of any read, write or invalidation cycle. The address remains latched for one cycle after the initiation of a read or write, and the address remains latched for two cycles after the initiation of an invalidation.

RESET

The IDT7MB6091 is reset when RESET is asserted. Asserting RESET will invalidate the entire contents of the cache, and reset the control logic of the cache. The cache will be reset regardless of the state of other control signals when RESET is asserted.

FLUSH

The entire cache contents of the IDT7MB6091 is invalidated when the $\overline{FLUSH}$ input is asserted. The cache will be invalidated regardless of the state of other control signals when $\overline{FLUSH}$ is asserted. $\overline{FLUSH}$ will not reset the state of the cache control logic.

READ

The IDT7MB6091 recognizes the initiation of a read cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled low with M/$\overline{IO}$ high and W/$\overline{R}$ low. As soon as the address is valid at the input of the module, the IDT7MB6091 begins its tag look-up. If the input address is not contained in the cache, then a miss has occurred and the IDT7MB6091 will wait for the main memory system to service the current access. If the input address is present in the cache, then a hit has occurred and the IDT7MB6091 will burst back a line of data to the CPU.

If a read miss occurs the IDT7MB6091 asserts $\overline{START}$ in the first T2 cycle and then waits for the memory system to provide data. The IDT7MB6091 will consider the data returned from the memory system as cacheable if $\overline{SKEN}$ is sampled low at least one cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first

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asserted. The IDT7MB6091 will load the data word returned from the memory system into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low. However, the IDT7MB6091 will only validate the line of data returned from the memory system if $\overline{SKEN}$ is sampled low the cycle before the last data word is transferred from the memory system, i.e. the fourth time that $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low. The line fill is aborted if $\overline{BLAST}$ is sampled low concurrent with $\overline{CBRDY}$ or $\overline{CRDY}$ being sampled low prior to the last data word transfer.

The IDT7MB6091 will consider the data returned as non-cacheable if $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low before or concurrently with $\overline{SKEN}$. Therefore, to avoid a potential performance penalty, $\overline{SKEN}$ should not be asserted prior to $\overline{CBRDY}$ or $\overline{CRDY}$ if the data is considered non-cacheable, since the IDT7MB6091 will invalidate a line of data if $\overline{SKEN}$ is sampled low before $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low during a read miss.

The IDT7MB6091 requires that the read miss address (i.e. the address that was valid at the beginning of the read cycle) is present when $\overline{SKEN}$ is sampled low at the beginning of a line fill and again when $\overline{SKEN}$ is sampled at the end of a line fill. The address must be valid because it is latched at these times to invalidate a line at the beginning of the fill and then to validate the line at the end of the line fill. When the address is latched at the end of the line fill, it will remain latched until the last data word of the line is written to the cache.

If the IDT7MB6091 detects that the input address is contained in the cache, the IDT7MB6091 will supply data to the CPU. The IDT7MB6091 starts bursting data back to the CPU in the first T2 cycle. The IDT7MB6091 then transfers a new data word in each subsequent T2 cycle until $\overline{BLAST}$ is asserted to the cache. The IDT7MB6091 also forces $\overline{START}$ high and $\overline{BRDYO}$ low in the first T2 cycle. $\overline{CKEN}$ is asserted during the T1 cycle and again in the second and subsequent T2 cycles during a read hit.

WRITE

The IDT7MB6091 recognizes the initiation of a write cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled low with M/$\overline{IO}$ high and W/$\overline{R}$ high. As soon as the address is valid at the input of the module, the IDT7MB6091 begins its tag look-up. If the input address is contained in the cache then a write hit has occurred, and the cache contents are updated in the first T2 cycle if the WP input is low. If the WP input is high during a write hit, the line is seen as write protected and the write is ignored. If the input address is not contained in the cache then a write miss has occurred, the IDT7MB6091 ignores the write and the cache contents are not updated.

INVALIDATION

An invalidation is initiated by the simultaneous assertion of $\overline{EADS}$ and $\overline{CS}$. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored since invalidations have priority. At the initiation of an invalidation, the IDT7MB6091 begins its tag look-up. If the line is found in the cache, the line will be invalidated. The IDT7MB6091 requires two cycles after the assertion of $\overline{EADS}$ to invalidate a line; therefore, invalidations can only occur every third cycle. The IDT7MB6091 ignores invalidations only if an address is currently latched in the address latch. Therefore, the IDT7MB6091 ignores invalidations at the following times: the cycle after the initiation of a read or write cycle, the cycle after $\overline{SKEN}$ is first sampled low during a line fill, the cycle(s) after sampling $\overline{SKEN}$ low concurrent with (or after) the third word transfer and prior to the fourth word transfer of a line fill, and the two cycles following a previous invalidation.

BACKOFF

A cache backoff is initiated by the assertion of $\overline{BOFF}$. $\overline{BOFF}$ interrupts any other cache cycle that the IDT7MB6091 is servicing. The cycle after $\overline{BOFF}$ is sampled low, the IDT7MB6091 will float its data bus, and the output control signals are driven to their idle levels, i.e. $\overline{CKEN}$ low, $\overline{START}$ high and $\overline{BRDYO}$ high. When $\overline{BOFF}$ is asserted, the IDT7MB6091 ignores all cache cycles except for invalidations; however, the IDT7MB6091 will still recognize the assertion of RESET or $\overline{FLUSH}$ when $\overline{BOFF}$ is asserted.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2844 tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2844 tbl 04

1. V_{IL} = –3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2844 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (A_2 - A_3)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	30	µA
$\|I_{LI}\|$	Input Leakage Current (Data, A_2 - A_3, $\overline{BE_0}$ - $\overline{BE_3}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage Current (CLK, $\overline{ADS}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{IH}\|$	Input High Current (Control)	V_{CC} = Max, V_{IN} = V_{CC}	—	1.0	mA
$\|I_{IL}\|$	Input Low Current (Control)	V_{CC} = Max, V_{IN} = GND	—	260	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OLD}	Output Low Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OLC}	Output Low Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min.	—	0.5	V
V_{OHD}	Output High Voltage (Data)	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output High Voltage (Control)	I_{OH} = –2mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	1900	mA

2844 tbl 06

CAPACITANCE[1]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance (A_2 - A_3)	V_{IN} = 0V	35	pF
C_{IN}	Input Capacitance (Data, A_{2-3}, $\overline{BE_{0-3}}$)	V_{IN} = 0V	15	pF
C_{IN}	Input Capacitance (Control)	V_{IN} = 0V	25	pF
C_{IN}	Input Capacitance ($\overline{ADS}$, CLK)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance ($\overline{BRDYO}$)	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance (START, $\overline{SKEN}$)	V_{IN} = 0V	15	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	10	pF

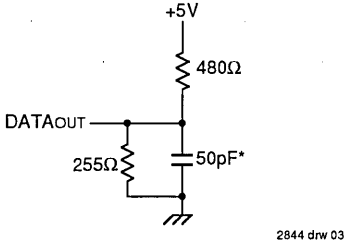
2844 tbl 07

NOTE:
1. These parameters are guaranteed by design but not tested.

AC TEST CONDITIONS

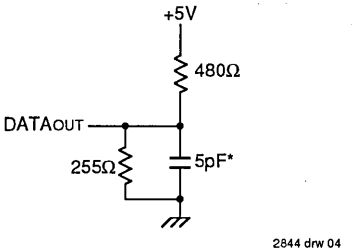
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2844 tbl 08



2844 drw 03

Figure 1. Output Load



2844 drw 04

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

AC ELECTRICAL CHARACTERISTICS

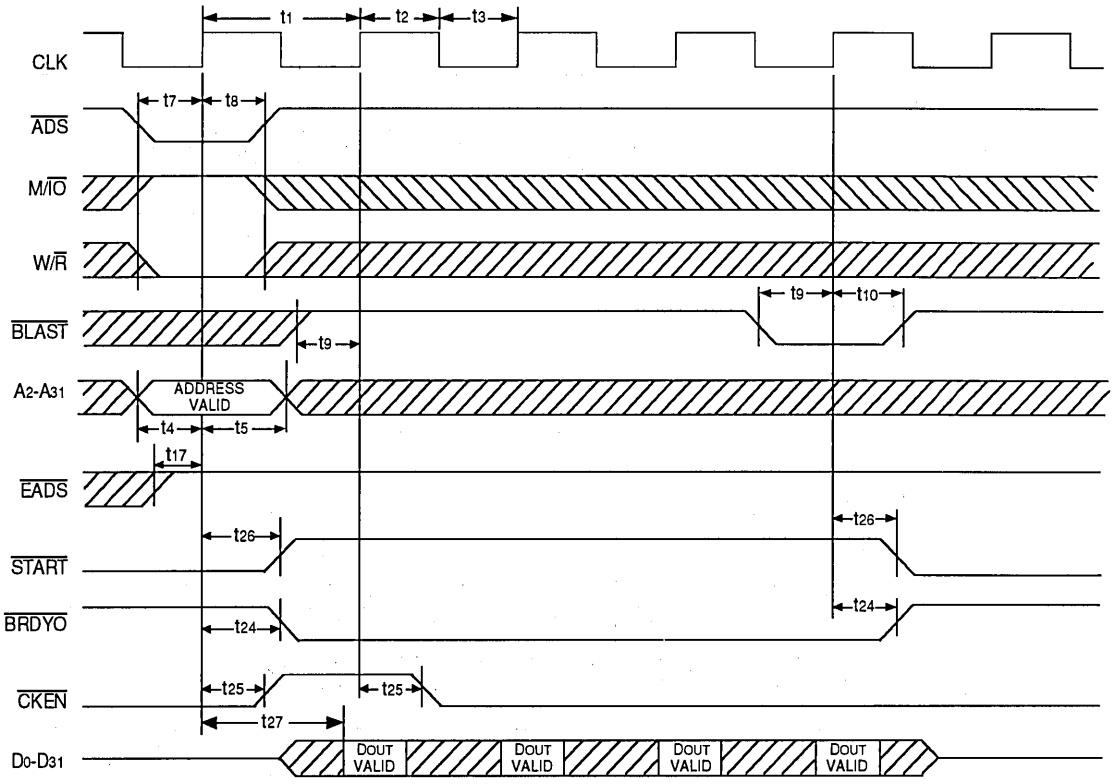
(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

		7MB6091SxxK				
		33MHz		25MHz		
Symbol	Name	Min.	Max.	Min.	Max.	Unit
t1	Clock Period	30	—	40	—	ns
t2	Clock High Time	11	—	14	—	ns
t3	Clock Low Time	11	—	14	—	ns
t4	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Setup Time	13	—	17	—	ns
t5	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Hold Time	10	—	10	—	ns
t6	A_4-A_{31} Line Fill Setup Time	5	—	5	—	ns
t7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Setup Time	13	—	20	—	ns
t8	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Hold Time	3	—	3	—	ns
t9	$\overline{BLAST}$ Setup Time	9	—	10	—	ns
t10	$\overline{BLAST}$ Hold Time	3	—	3	—	ns
t11	$\overline{CRDY}$, $\overline{CBRDY}$ Setup Time	11	—	11	—	ns
t12	$\overline{CRDY}$, $\overline{CBRDY}$ Hold Time	3	—	3	—	ns
t13	$\overline{SKEN}$ Setup Time	9	—	9	—	ns
t14	$\overline{SKEN}$ Hold Time	3	—	3	—	ns
t15	D_0-D_{31}, DP_0-DP_3 Setup Time	5	—	5	—	ns
t16	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	3	—	ns
t17	$\overline{EADS}$ Setup Time	9	—	9	—	ns
t18	$\overline{EADS}$ Hold Time	3	—	3	—	ns
t19	A_4-A_{31} Setup Time (Snoop)	6	—	6	—	ns
t20	A_4-A_{31} Hold Time (Snoop)	10	—	10	—	ns
t21	RESET, $\overline{FLUSH}$ Setup Time	9	—	9	—	ns
t22	RESET, $\overline{FLUSH}$ Hold Time	3	—	3	—	ns
t23	RESET, $\overline{FLUSH}$ Pulse Width	80	—	80	—	ns
t24	$\overline{BRDYO}$ Valid	—	16	—	22	ns
t25	$\overline{CKEN}$ Valid	—	15	—	18	ns
t26	$\overline{START}$ Valid	—	16	—	22	ns
t27	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit)	—	24	—	30	ns
t28	WP Setup Time	15	—	15	—	ns
t29	WP Hold Time	—	3	—	3	ns
t30	$\overline{BOFF}$ Setup Time	9	—	10	—	ns
t31	$\overline{BOFF}$ Hold Time	3	—	3	—	ns

NOTE:
1. The address, M/$\overline{IO}$ and W/$\overline{R}$ inputs to the IDT7MB6091 must be held valid for the duration of the read, write or invalidation cycle.

2844 tbl 09

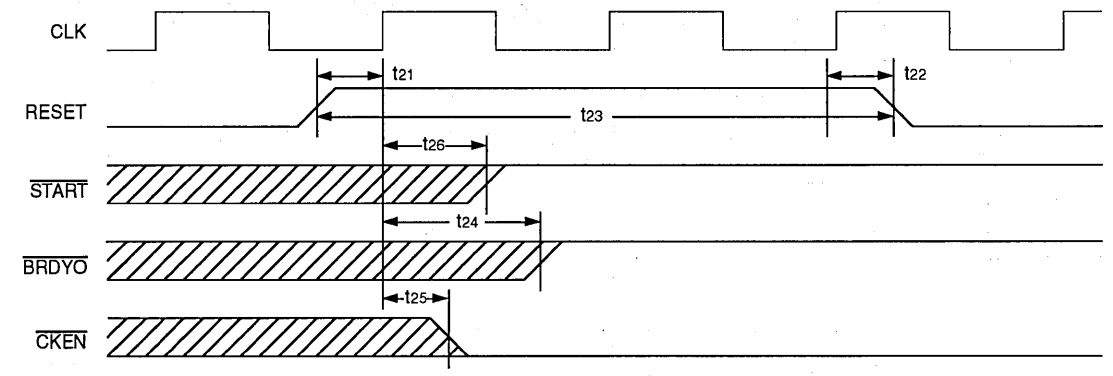
TIMING WAVEFORM OF A READ HIT CYCLE (READ LINE)(1)



NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

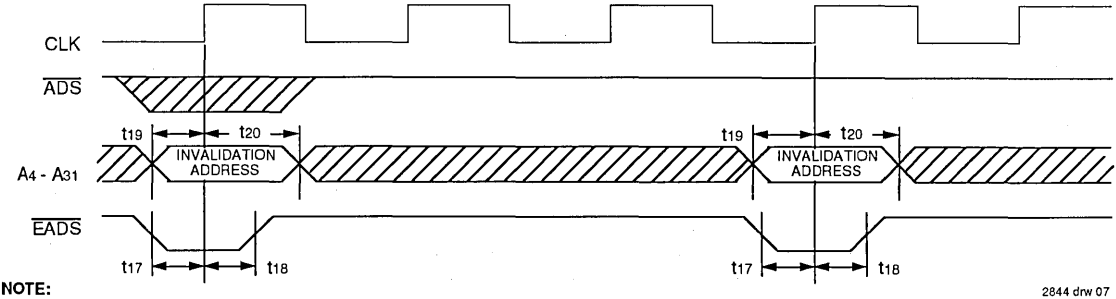
2844 drw 05

TIMING WAVEFORM OF A RESET OPERATION



2844 drw 06

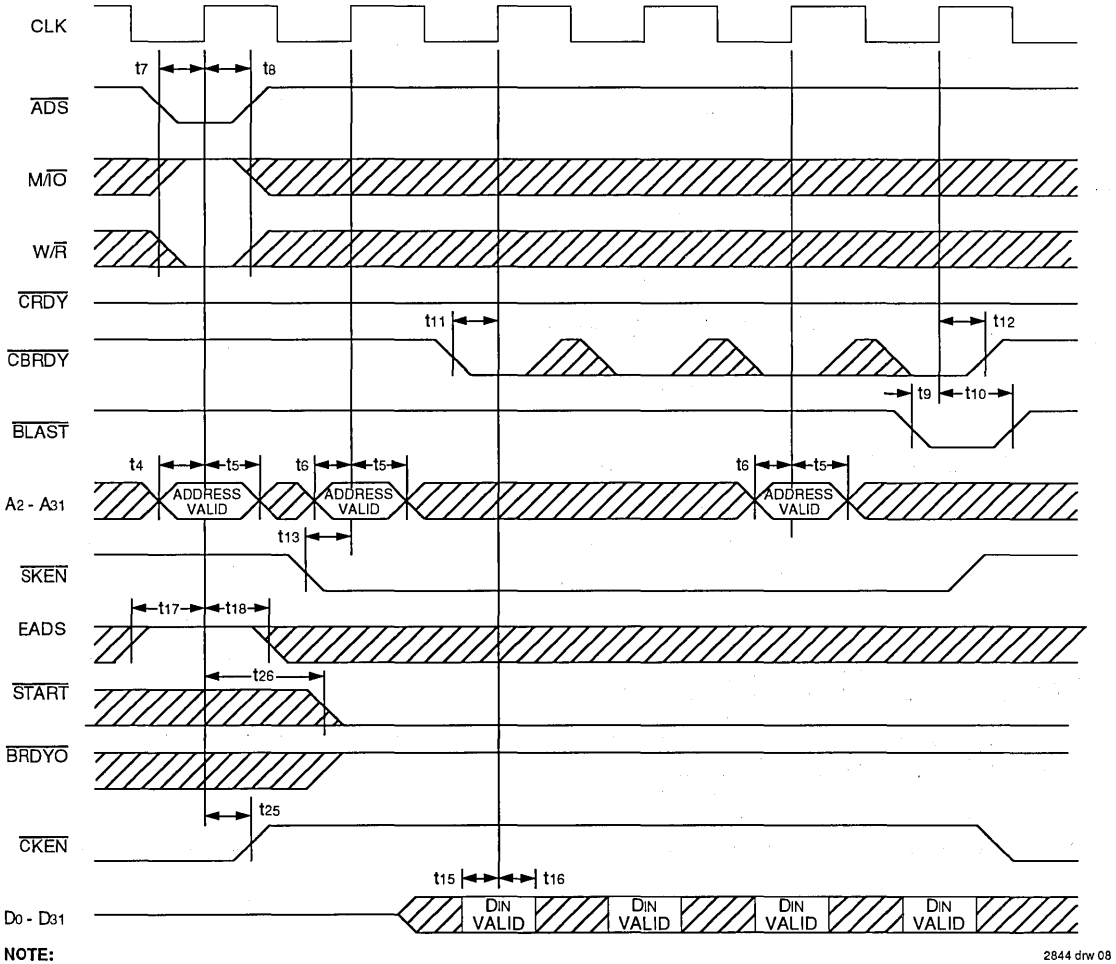
TIMING WAVEFORM OF A CACHE INVALIDATION(1)



NOTE:
1. If EADS and ADS are asserted simultaneously, ADS is ignored.

2844 drw 07

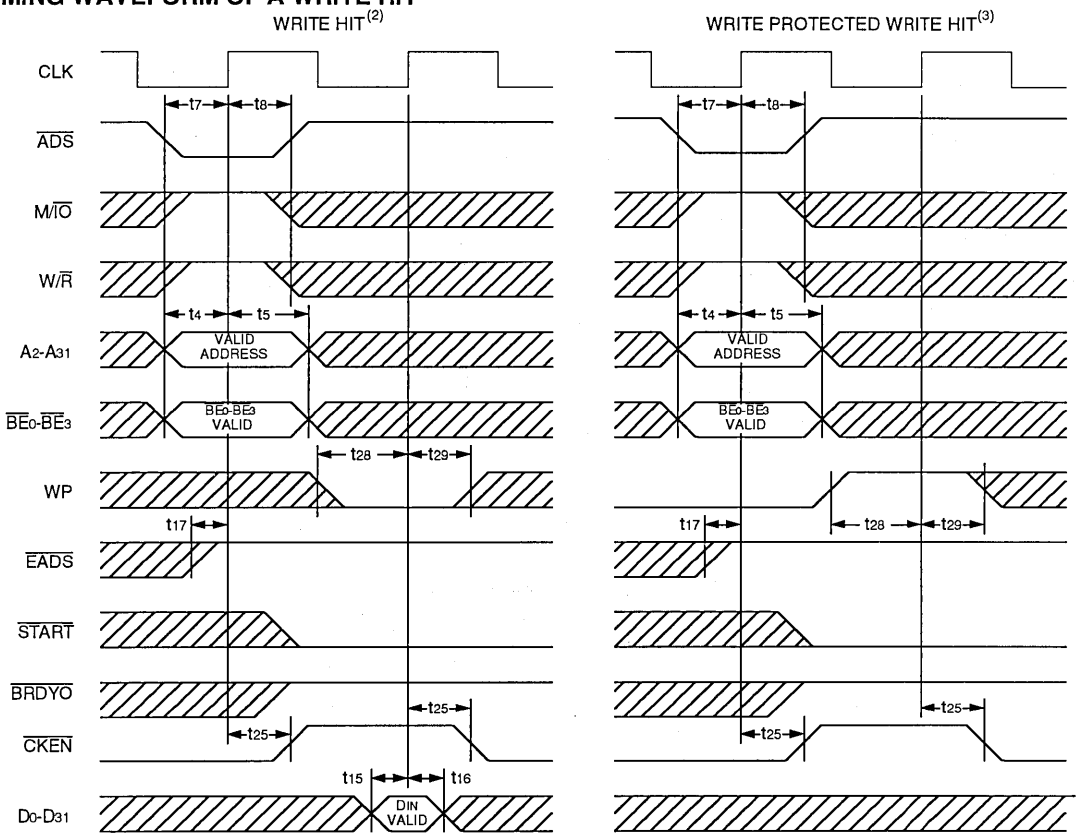
TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)(1)



NOTE:
1. RESET is held LOW, FLUSH is held HIGH, BOFF is held HIGH.

2844 drw 08

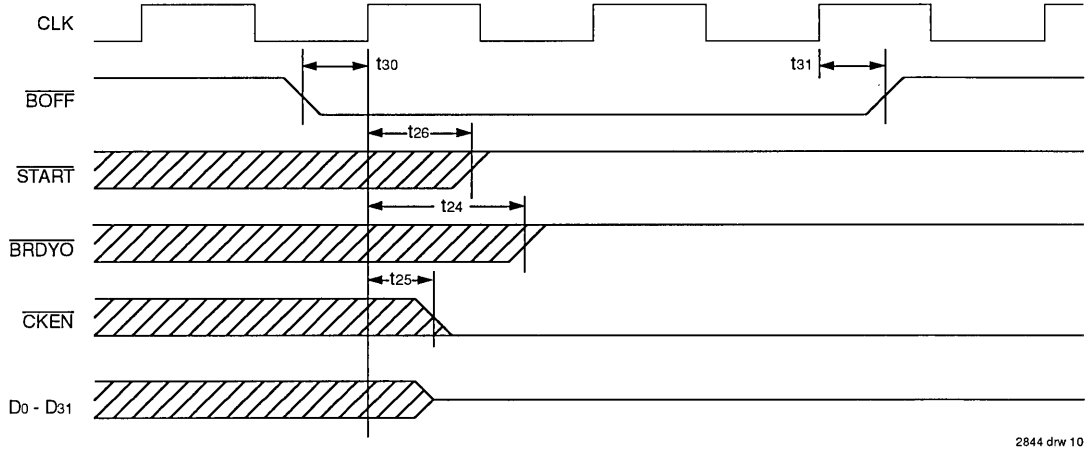
TIMING WAVEFORM OF A WRITE HIT[1]



2844 drw 09

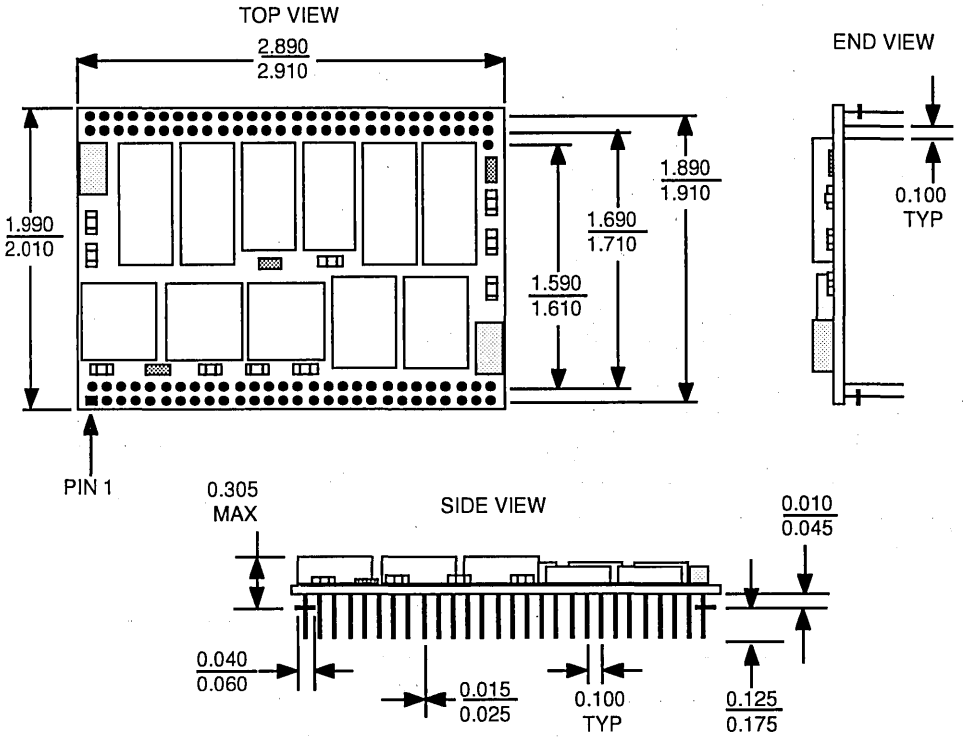
NOTES:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.
2. For a write hit, data in the IDT7MB6091 is updated.
3. For a write protected write hit, the data in the IDT7MB6091 is not updated.

TIMING WAVEFORM OF A BACKOFF OPERATION



2844 drw 10

PACKAGE DIMENSIONS



2844 drw 11

Integrated Device Technology, Inc.

128K BYTE CMOS SECONDARY CACHE MODULE FOR THE INTEL™ i486™

IDT7MP6086

FEATURES:

- 128K byte direct mapped secondary cache module
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486 processor
- Operates with i486 speeds of up to 50MHz
- 72 lead FR-4 SIMM (Single-in-Line Memory Module)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

DESCRIPTION:

The IDT7MP6086 is a 128K byte direct mapped secondary cache module, using four IDT71589 32K x 9 CacheRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) substrate with gold-plated leads. Extremely high speeds are achieved using IDT's high performance, high reliability CEMOS™ technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486 architecture while using low speed logic devices and consuming the minimum board space.

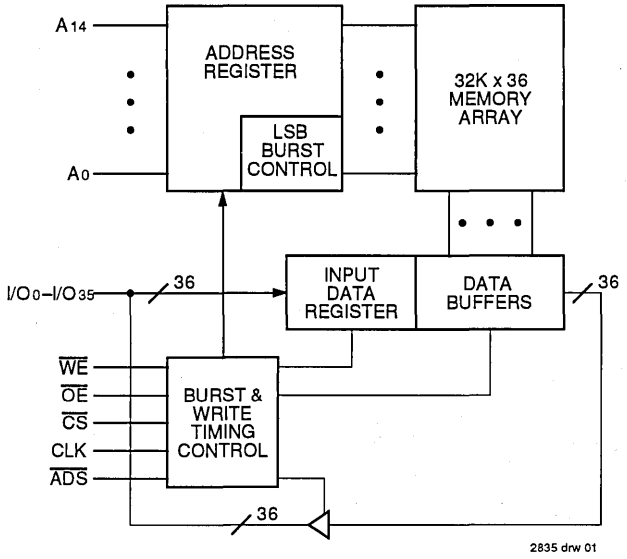
The IDT7MP6086 contains a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle. An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Three program identification pins are provided so that the system can uniquely identify the IDT7MP6086.

Note that individual parity bits are grouped with their respective bytes, not all at the end.

The SIMM package configuration allows 72 leads to be placed on a package 4.25 inches long, 0.55 inches tall and 0.25 inches thick. The IDT7MP6086 is available with speed matching a 50MHz i486. All inputs and outputs of the IDT7MP6086 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



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Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION[1]

		1	GND
GND	2	3	VCC
I/O0	4	5	I/O1
I/O2	6	7	I/O3
I/O4	8	9	I/O5
I/O6	10	11	I/O7
I/O8	12	13	$\overline{WE0}$
$\overline{WE1}$	14	15	I/O9
I/O10	16	17	I/O11
GND	18	19	I/O12
I/O13	20	21	I/O14
I/O15	22	23	I/O16
I/O17	24	25	A0
A1	26	27	A2
A3	28	29	A4
A5	30	31	A6
A7	32	33	A8
$\overline{ADS}$	34	35	CLK
VCC	36		
		37	GND
$\overline{CS}$	38	39	$\overline{OE}$
A9	40	41	A10
A11	42	43	A12
A13	44	45	A14
I/O18	46	47	I/O19
I/O20	48	49	I/O21
I/O22	50	51	I/O23
I/O24	52	53	I/O25
I/O26	54	55	GND
$\overline{WE2}$	56	57	$\overline{WE3}$
I/O27	58	59	I/O28
I/O29	60	61	I/O30
I/O31	62	63	I/O32
I/O33	64	65	I/O34
I/O35	66	67	PD0
PD1	68	69	PD2
VCC	70	71	GND
GND	72		

2835 drw 02

SIMM
TOP VIEW

NOTE:
1. Please consult the factory regarding program identification pins.

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE0\text{-}3}$	Byte Write Enables
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
PD0-2	Program Identification
GND	Ground
Vcc	Power

2835 tbl 01

CAPACITANCE

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
CIN	Input Capacitance (Data)	VIN = 0V	13	pF
CIN	Input Capacitance (Address & Control)	VIN = 0V	42	pF
CI/O	Output Capacitance	VOUT = 0V	13	pF

NOTE: 2835 tbl 02
1. This parameter is guaranteed by design but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2835 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2835 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2835 tbl 05
1. VIL = –3.0V for pulse width less than 5ns.

TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
Hi-Z = High Impedance

2835 tbl 06

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C TO + 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address & Contol)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2835 tbl 07

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	50MHz[1]	40MHz	33MHz	25MHz	Unit
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	—	520	520	520	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	1150	960	880	800	mA

NOTES:
1. Preliminary specification only.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

2835 tbl 08

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2835 tbl 09

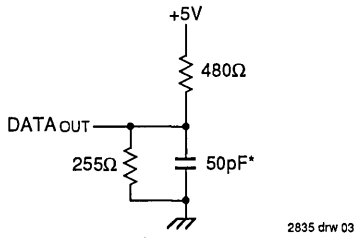


Figure 1. Output Load

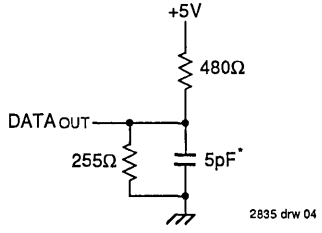


Figure 1. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

*including scope and jig

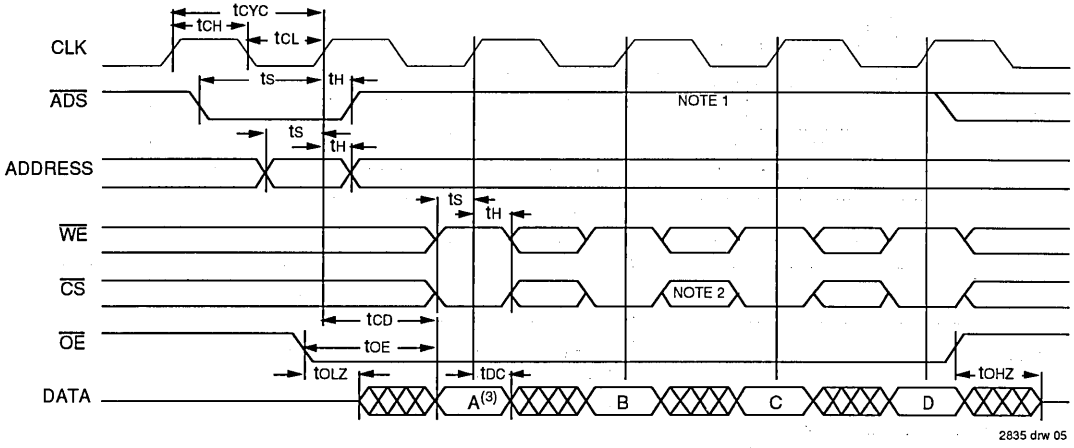
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, TA = 0° to +70°C)

		7MP6086SxxM								
		50 MHz[1]		40 MHz		33 MHz		25 MHz		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCYC	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
tCH	Clock Pulse High	8	—	10	—	11	—	14	—	ns
tCL	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
tS1	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	4	—	5	—	ns
tS2	Set-up Time (Address, Input Data)	5	—	5	—	5	—	6	—	ns
tH1	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	1	—	1	—	ns
tH2	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	2	—	2	—	ns
tADSH	Hold Time ($\overline{ADS}$)	3	—	3	—	3	—	3	—	ns
tCD	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
tDC	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
tOLZ	Output Enable to Output in Lo-Z[2,3]	2	—	2	—	2	—	2	—	ns
tOHZ	Output Disable to Output in Hi-Z[2,3]	—	7	—	8	—	9	—	10	ns

NOTES:
2835 tbl 10

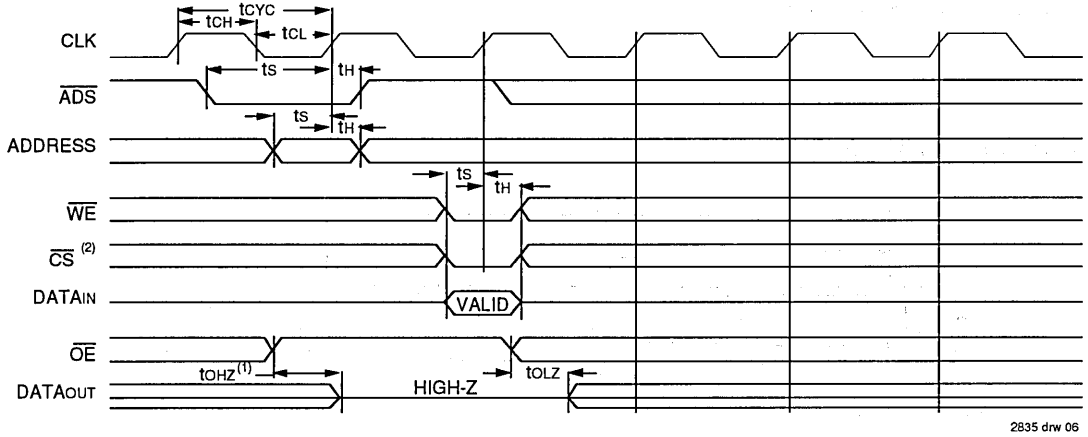
1. Preliminary specifications only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figure 2).
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF BURST READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and tH.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A}_0$. C-Data from input address except A_1 is now $\overline{A}_1$. D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as tOHZ + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

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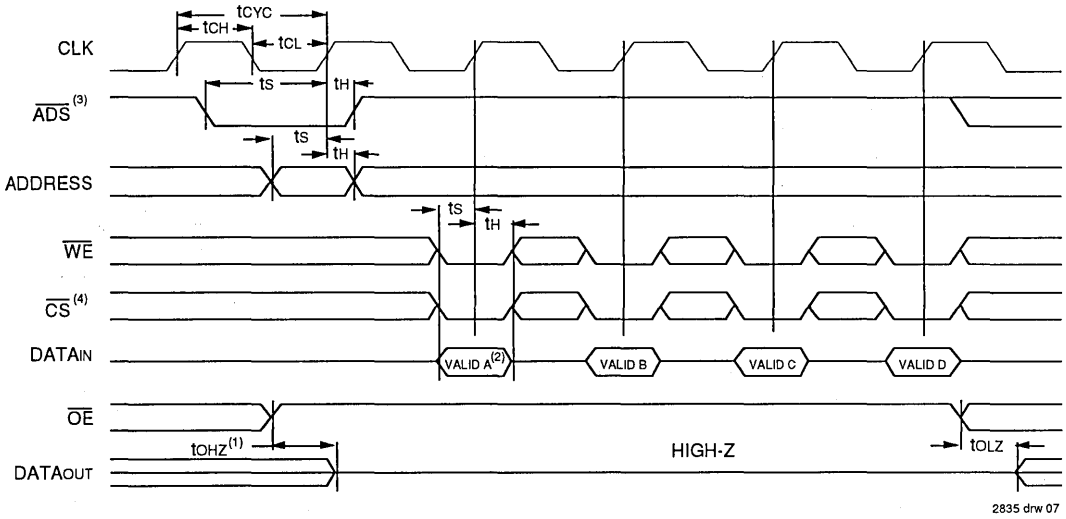
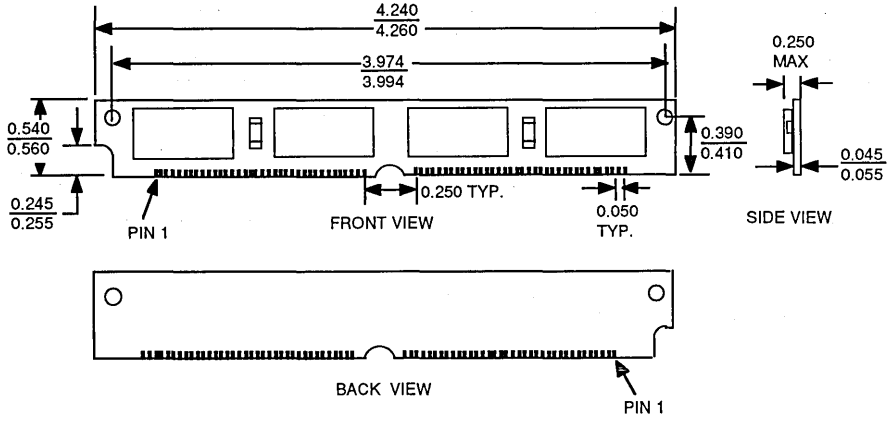
TIMING WAVEFORM OF BURST WRITE CYCLE



NOTES:

1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

PACKAGE DIMENSIONS



Integrated Device Technology, Inc.

IDT79R4000 FLEXI-CACHE™ DEVELOPMENT TOOL

PRELIMINARY
IDT7MP6048
IDT7MP6068

FEATURES:

- Hardware Development Tool for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU
- Configurable in various cache sizes, number of words per line size, and split vs. unified cache operation
- Move from prototype/development to production with no redesign by using pin compatible "production grade" IDT79R4000 secondary cache modules
- Development module operating frequencies to support zero wait-state 50MHz IDT79R4000 operation
- Four identical 80 lead gold-plated SIMMs (Single In-Line Memory Modules) support each IDT79R4000 CPU
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

DESCRIPTION:

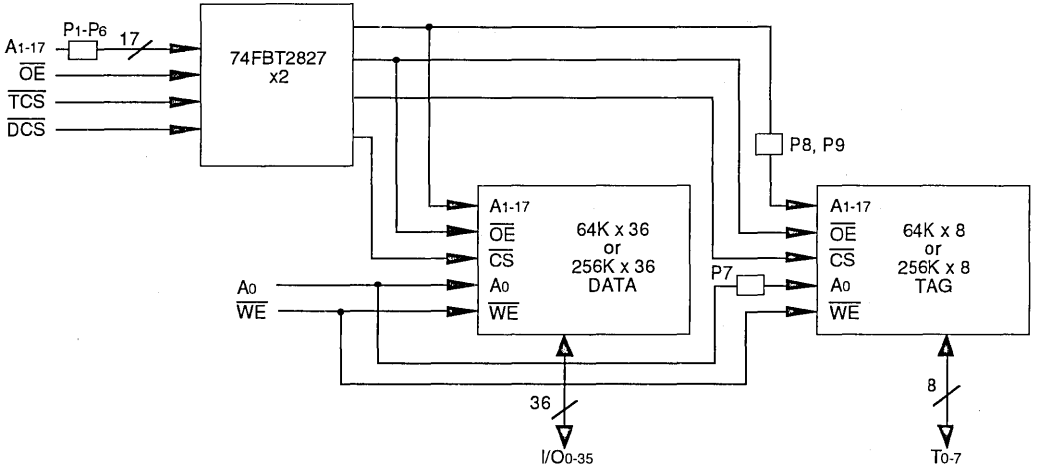
The IDT7MP6048/7MP6068 is a Hardware Development Tool used for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU. By changing jumpers on the modules, the designer can easily change certain characteristics (cache size, number of words per line, and split vs. unified operation) of the secondary cache in the lab. By running benchmarks on the actual system using these various cache configurations, the secondary cache which best optimizes system performance can be determined. This development tool gives you cache performance benchmarks which are superior to benchmarks derived via simulation.

Move from development to production without changing the secondary cache footprint by choosing pin compatible "production grade" IDT79R4000 secondary cache modules. These high performance, high density IDT modules are optimized to meet the customers' exact cache requirements required for volume production of the system (please consult the factory for more details).

The IDT7MP6048 is a 1 megabyte secondary cache module block (four identical modules builds a complete cache to support each IDT79R4000 CPU) constructed on a multilayer, epoxy laminate substrate (FR-4) using 11 64K x 4 static RAMs and FBT logic drivers while the IDT7MP6068 is a 4 megabyte secondary cache module block using 11 256K x 4 static RAMs and FBT logic drivers. Extremely high speeds can be achieved using high performance BiCEMOS™ IDT61B298 or

(continued on page 2)

FUNCTIONAL BLOCK DIAGRAM(1)



2841 drw 01

NOTE:

1. The Data and Tag sizes shown on the block diagram are only for the case when the jumpers are in the default positions for the respective modules. These sizes will change according to the jumper connections (see Jumper Connections on page 2).

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DESCRIPTION (continued from page 1)

IDT71B028 static RAMs and IDT74FBT2827 drivers. The FBT drivers have BiCEMOS™ I/Os and internal 25Ω series output resistors resulting in the fastest propagation times with minimal overshoots and ringing. Multiple GND pins and on-board decoupling capacitors provide maximum noise immunity for this performance critical part of the system. All inputs and outputs of the modules are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation of the module.

CACHE CONFIGURATIONS(1)

Memory Size
4MB (7MP6068 default)
2MB
1MB (7MP6048 default)
512KB
256KB
128KB

Words per line
4 (default)
8
16
32

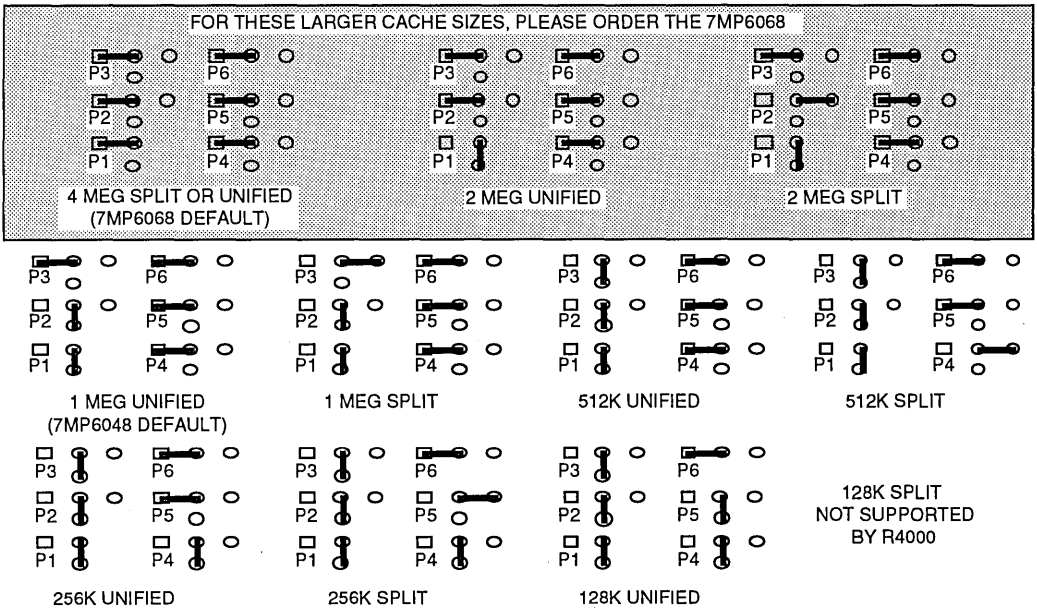
Cache Operation
unified cache (default)
split cache

NOTE: 2841 tbl 01

1. Please refer to the Jumper Connections for instructions on how to implement the Cache Configurations shown above.

JUMPER CONNECTIONS:

Cache depth and Split vs. Unified Operation are controlled by Jumpers P1-P6 as follows:



Cache line size is controlled by Jumpers P7-P9 as follows:

2841 drw 02

PIN CONFIGURATION[1]

VCC	2	1	GND
I/O1	4	3	I/O0
I/O3	6	5	I/O2
I/O5	8	7	I/O4
GND	10	9	I/O6
I/O8	12	11	I/O7
I/O10	14	13	I/O9
I/O12	16	15	I/O11
I/O14	18	17	I/O13
I/O15	20	19	GND
I/O17	22	21	I/O16
I/O19	24	23	I/O18
I/O21	26	25	I/O20
GND	28	27	I/O22
I/O23	30	29	VCC
I/O25	32	31	I/O24
I/O27	34	33	I/O26
I/O29	36	35	I/O28
I/O30	38	37	GND
I/O32	40	39	I/O31
I/O34	42	41	I/O33
GND	44	43	I/O35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
VCC	54	53	GND
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
GND	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
T0	70	69	$\overline{TCS}$
T1	72	71	GND
T3	74	73	T2
T5	76	75	T4
T7	78	77	T6
GND	80	79	VCC

2841 drw 03

SIMM
TOP VIEW

NOTE:
1. For proper operation of the module, please refer to the Jumper Connections for proper connections of the module pins. .

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2841 tbl 02

PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2841 tbl 03

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	10	pF
CIN(A)	Input Capacitance (A1-15, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	VIN = 0V	10	pF
CIN(B)	Input Capacitance (A0, $\overline{WE}$)	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE: 2841 tbl 04
1. This parameter is guaranteed by design, but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2841 tbl 05
1. VIL = -1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2841 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2841 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

2841 tbl 08

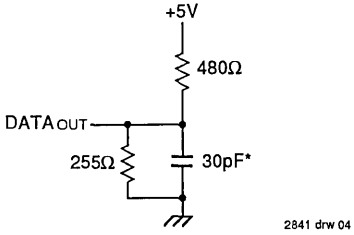


Figure 1. Output Load

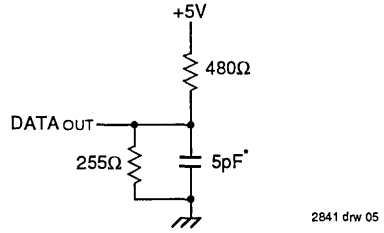


Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

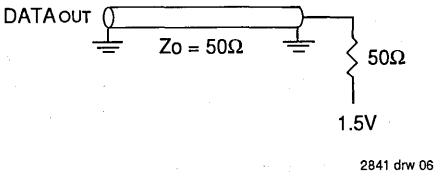


Figure 3. Alternate Output Load

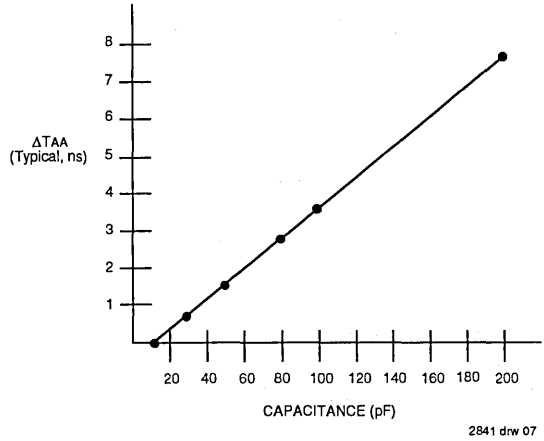


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

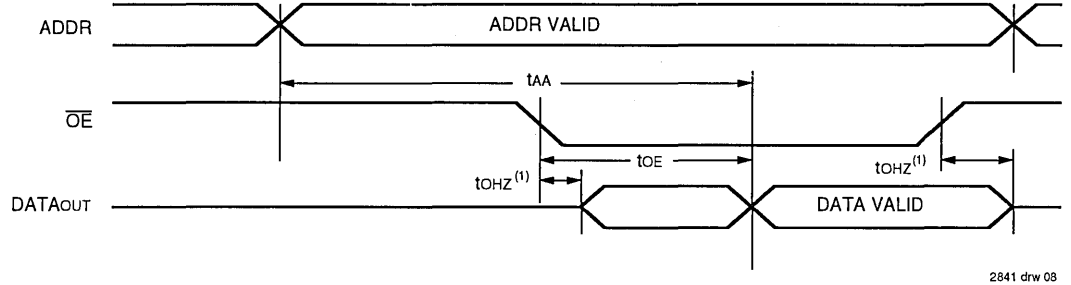
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6048/6068SxxM -12 Min.	-12 Max.	-15 Min.	-15 Max.	-17 Min.	-17 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-30 Min.	-30 Max.	Unit
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{AOA}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{AOW}	A_0 Valid to End of Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End of Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2841 tbl 08

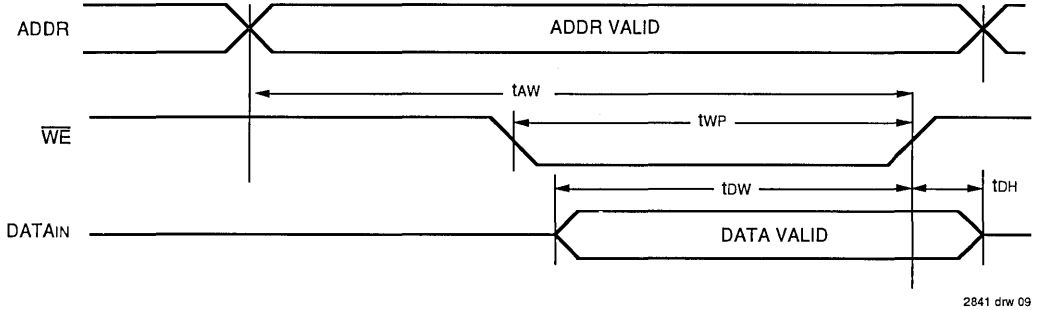
TIMING WAVEFORM OF READ CYCLE[1]



2841 drw 08

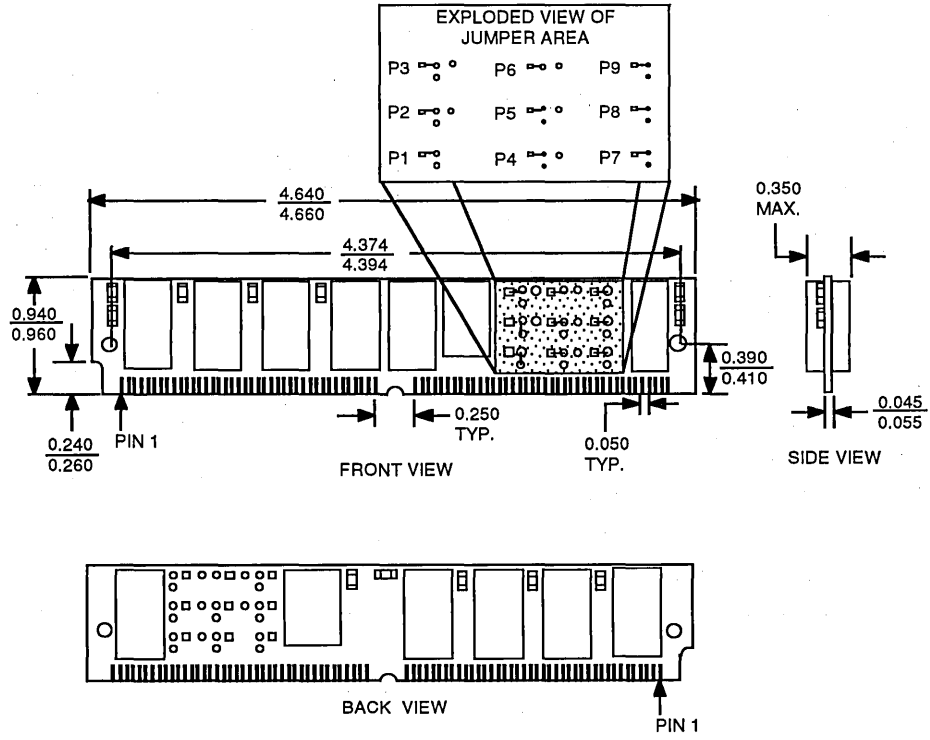
NOTE:
1. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE



2841 drw 09

PACKAGE DIMENSIONS



2841 drw 10

Integrated Device Technology, Inc.

THE SUBSYSTEMS "FLEXI-PAK™" CMOS MODULE FAMILY

GENERAL INFORMATION

SRAM, EPROM, & EEPROM MODULES

FEATURES:

- High-density modules using high-speed CMOS SRAM, EPROM, and EEPROM components.
- Inter-changeable modules with equivalent footprints
- Fast access times:
  - SRAM: 20ns (max.) - military
    15ns (max.) - commercial
  - EEPROM: 95ns (max.) - military
    75ns (max.) - commercial
  - EPROM: 95ns (max.) - military
    40ns (max.) - commercial
- Low power CMOS operation
- Surface mounted LCC components on a co-fired ceramic substrate
- Offered in a 66-pin, ceramic HIP (Hex In-line Package) occupying as small as1 sq. inch of board space
- Single 5V (± 10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The Flexi-Pak family of modules are high-speed, high-density CMOS memory modules constructed on a multilayer co-fired ceramic substrate using either SRAM, EPROM, or EEPROM components in leadless chip carriers.

This family of IDT modules supports applications requiring stand alone static or programmable memory or those applications needing a combination of both. All module configurations in this family have equivalent footprints, allowing "plug-in compatibility" with each other (i.e. interchangeable), ideal for a wide range of prototype and debugging applications.

The Flexi-Pak family utilizes the fastest commercial grade and MIL-STD-883 Class B military grade components, giving you the highest performance available anywhere. CMOS technology offers a low-cost, low-power alternative to bipolar and fast NMOS memories.

All versions of the Flexi-Pak Module Family are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit into 1 sq. inch of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

ORGANIZATIONS

SRAM: IDT7M4003 - 128K x 8, 64K x 16, 32K x 32
IDT7M4013 - 512K x 8, 256K x 16, 128K x 32

EEPROM: IDT7M7004 - 128K x 8, 64K x 16, 32K x 32
IDT7M7014*- 512K x 8, 256K x 16, 128K x 32

SRAM / EEPROM:

IDT7M7005 -	64K x 8 / 64K x 8
	64K x 8 / 32K x 16
	32K x 16 / 64K x 8
	32K x 16 / 32K x 16
IDT7M7025* -	64K x 8 / 256K x 8
	64K x 8 / 128K x 16
	32K x 16 / 256K x 8
	32K x 16 / 128K x 16
IDT7M7035* -	256K x 8 / 256K x 8
	256K x 8 / 128K x 16
	128K x 16 / 256K x 8
	128K x 16 / 128K x 16
IDT7M7045* -	256K x 8 / 64K x 8
	256K x 8 / 32K x 16
	128K x 16 / 64K x 8
	128K x 16 / 32K x 16

SRAM / EPROM:

IDT7M7012 -	64K x 8 / 64K x 8
	64K x 8 / 32K x 16
	32K x 16 / 64K x 8
	32K x 16 / 32K x 16
IDT7M7002 -	64K x 8 / 256K x 8
	64K x 8 / 128K x 16
	32K x 16 / 256K x 8
	32K x 16 / 128K x 16
IDT7M7022* -	256K x 8 / 256K x 8
	256K x 8 / 128K x 16
	128K x 16 / 256K x 8
	128K x 16 / 128K x 16
IDT7M7032* -	256K x 8 / 64K x 8
	256K x 8 / 32K x 16
	128K x 16 / 64K x 8
	128K x 16 / 32K x 16

*Please consult the factory for availability of these versions.

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Flexi-Pak is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY
32K x 32
CMOS EEPROM MODULE

IDT7M7004

FEATURES:

- High-density 1 megabit CMOS EEPROM module
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules with equivalent pin-outs
- Footprint compatible module upgrades to the next higher density with relative ease (IDT7M7014)
- Fast access time:
  - — 75ns (max.) 7M7004 commercial
  - — 95ns (max.) 7M7004 military
- Surface mounted LCC components on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the maximum number of Erase/Write Cycles per Byte

DESCRIPTION:

The IDT7M7004 is a high-speed, high-density 1 megabit CMOS EEPROM module constructed on a multi-layer, co-fired ceramic substrate using 4 32K x 8 EEPROM components in leadlesss chip carriers.

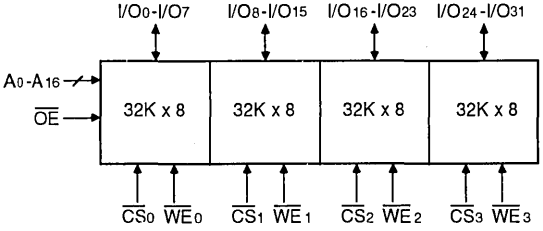
This module is part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making these "plug-in compatible" (i.e. inter-changeable), suitable for a wide range of applications.

The IDT7M7004 is available with access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits 1 megabit of 32-bit wide memory into 1 square inch of board space.

All military IDT modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



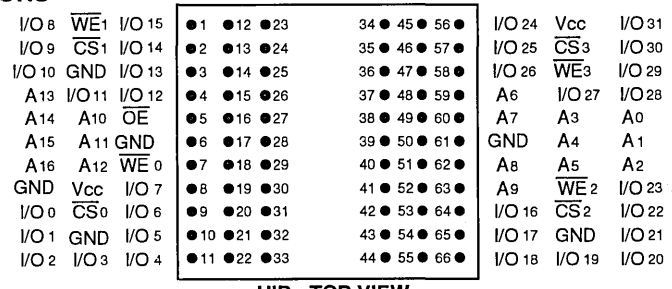
2825 drw 01

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$ 0-3	Write Enables
$\overline{CS}$ 0-3	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2825 tbl 01

PIN CONFIGURATIONS (1)



HIP - TOP VIEW

2825 drw 02

NOTE:

1. For the IDT7M7014 (128K x 32 version), pins 6 & 7 become A15 & A16 respectively. For the IDT7M7004 version, pins 6 & 7 are no connects..

Flexi-Pak is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2825 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE (1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Write	L	H	L	D_{IN}	Active
Read	L	H	H	High Z	Active

2825 tbl 03

NOTE:
1. For the proper operation of the module, $\overline{OE}$ must be High for all Write Cycles.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2825 tbl 04

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN} (1)	Input Capacitance (Data, $\overline{CS}$, $\overline{WE}$)	V_{IN} = 0V	12	pF
C_{IN} (2)	Input Capacitance (Address, $\overline{OE}$)	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2825 tbl 05

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2825 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A =-55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data, $\overline{WE}$, $\overline{CS}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 6mA	—	0.45	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
I_{CC}	Dynamic Operating Current	f = 5 MHz, I_{OUT} = 0 mA V_{CC} = Max.	—	320	mA
I_{SB}	Standby Supply Current (TTL)	$\overline{CS}$ ≥ 2V to V_{CC} + 1V	—	12	mA

2825 tbl 07

7

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2825 tbl 08

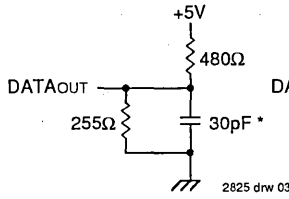


Figure 1. Output Load

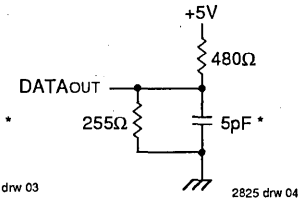


Figure 2. Output Load (for t_{CHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

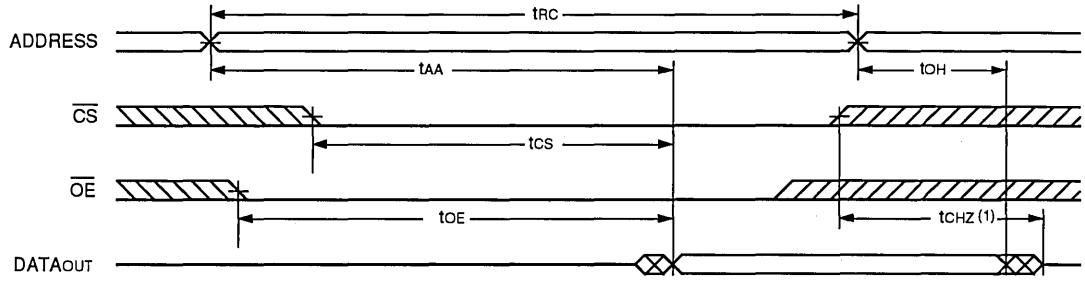
(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameters	7M7004SxxC/7M7004SxxCB										Unit
		-75		-95		-125		-150		-200		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
t_{AA}	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
t_{ACS}	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
t_{OE}	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
t_{CHZ} (1)	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t_{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t_{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t_{CS}	$\overline{CS}$ Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{CH}	$\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
t_{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t_{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t_{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t_{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t_{BLC}	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	µs
t_{WPH}	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
t_{DH} (1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
t_{OEH} (1)	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OE} (1)	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
t_{WR} (1)	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

2825 tbl 09

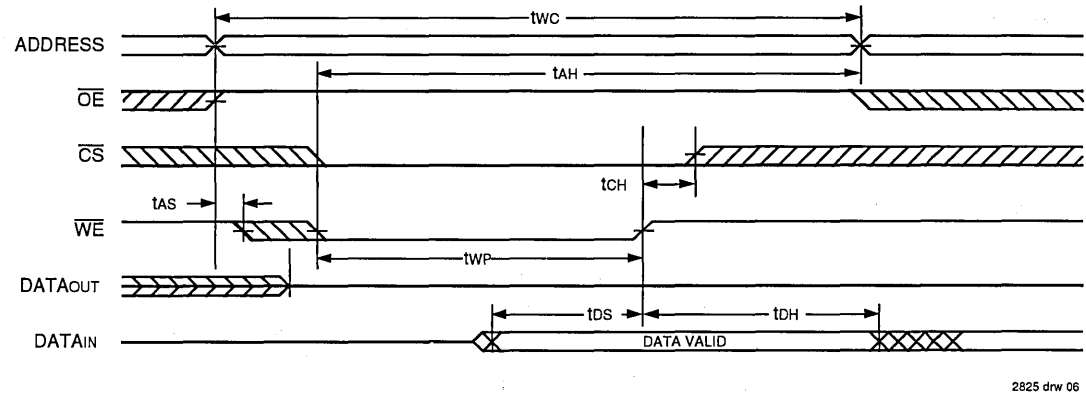
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE[1]

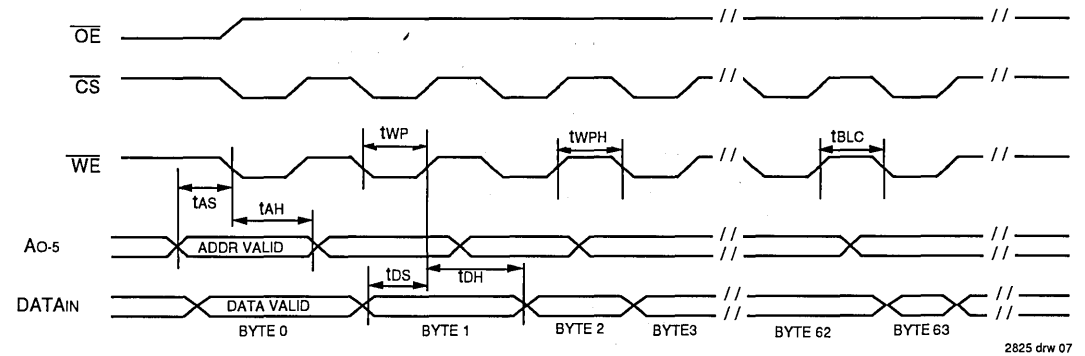


NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)

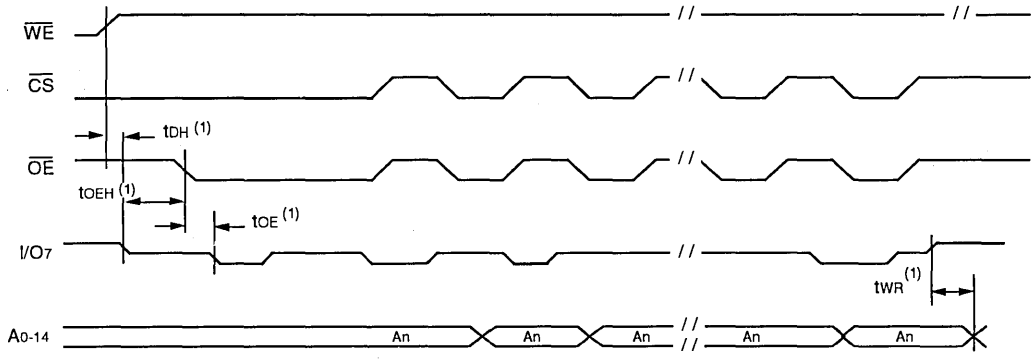


TIMING WAVEFORM OF PAGE MODE WRITE CYCLE [1]



NOTES:
1. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

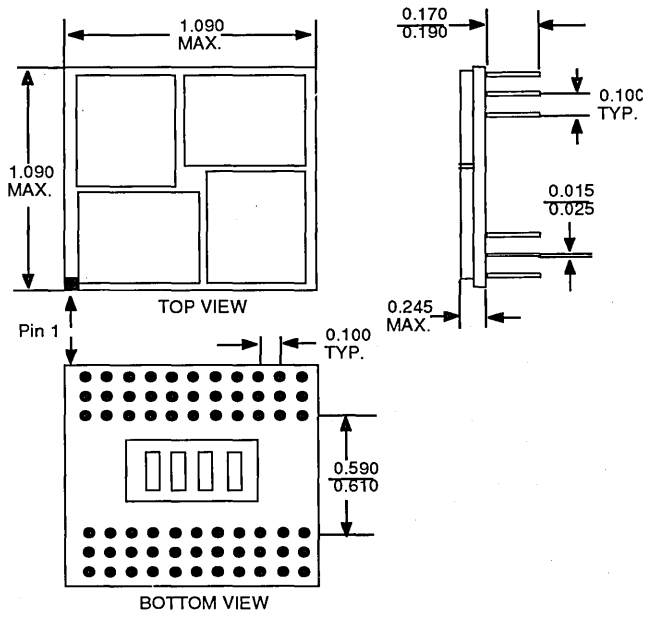
TIMING WAVEFORM OF $\overline{DATA}$ POLLING CYCLE



2825 drw 08

NOTES:
1. This parameter is guaranteed by design but not tested.
2. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

PACKAGE DIMENSIONS



2825 drw 09

Integrated Device Technology, Inc.

SUBSYSTEMS "FLEXI-PAK™" FAMILY 32K x 16/32K x 16 CMOS SRAM/EEPROM MODULE

PRELIMINARY
IDT7M7005

FEATURES:

- High-density CMOS module with SRAM and EEPROM memory on-board
- Member of the Subsystems "Flexi-Pak" Family of interchangeable modules with equivalent pin-outs
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - — 15ns (max.) commercial SRAM
  - — 20ns (max.) military SRAM
  - — 75ns (max.) commercial EEPROM
  - — 95ns (max.) military EEPROM
- Low power CMOS operation
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Offered in a 66-pin HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Please consult the factory regarding the number of Erase/Write Cycles per Byte Minimum available on the module

DESCRIPTION:

The IDT7M7005 is a high-speed, high-density CMOS module with both SRAM & EEPROM memory on-board. It is constructed on a multi-layer, co-fired ceramic substrate using 32K x 8 SRAM or EEPROM components in leadlesss chip carriers.

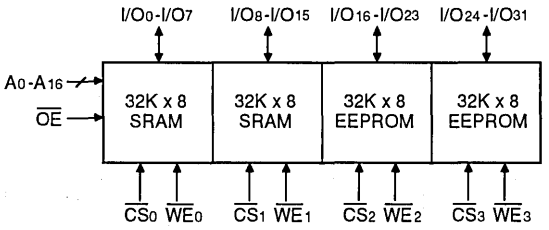
These modules are part of the IDT Subsystems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmmable memory or those applications needing a combination of both. All of these module configurations have equivalent pin-outs, making them "plug-in compatible" with each other, suitable for a wide range of applications.

The IDT7M7005 is available with SRAM access times as fast as 15ns over the commercial temperature range and 20ns over the military temperature range and EEPROM access times as fast as 75ns over the commercial temperature range and 95ns over the military temperature range.

These modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and fits the SRAM/EEPROM memory into 1 sq. inch of board space.

All military IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

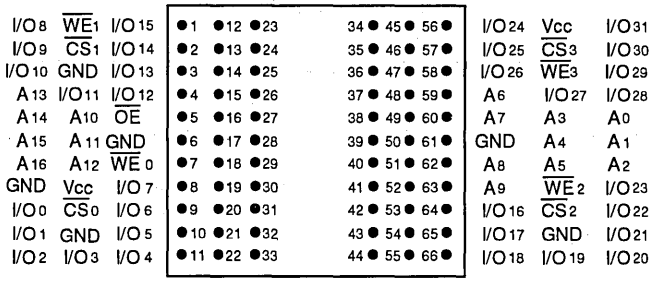


2826 drw 01

7

Flexi-Pak is a Trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS (1)



2826 drw 02

HIP
TOP VIEW

NOTE:
. For the IDT7M7005 (32K x 16/32K x 16) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$ 0-1	RAM Write Enables
$\overline{WE}$ 2-3	EEPROM Write Enables
$\overline{CS}$ 0-1	RAM Chip Selects
$\overline{CS}$ 2-3	EEPROM Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2826 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2826 tbl 03

TRUTH TABLE (1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	note 1	L	DIN	Active
Read	L	H	H	High Z	Active

2826 tbl 02

NOTE:
1. For the SRAM array $\overline{OE}$ = X (don't care); however, for the EEPROM array $\overline{OE}$ = H (high).

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN (1)	Input Capacitance (Data, $\overline{CS}$, $\overline{WE}$)	VIN = 0V	12	pF
CIN (2)	Input Capacitance (Address, $\overline{OE}$)	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	15	pF

2826 tbl 04

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2826 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2826 tbl 06

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.[1]	Max.[2]	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	30	40	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	10	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ f = f_{MAX}, Output Open	—	560	600	mA
I_{SB}	Standby Supply Curent	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ f = f_{MAX}, Output Open	—	46	146	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} > V_{CC}$ -0.2V or < 0.2V	—	46	46	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA (3)	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA (3)	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 6mA (4)	—	0.45	0.45	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA (4)	2.4	—	—	V

2826 tbl 07

NOTES:
1. For T_A = 0°C to +70°C versions only.
2. For T_A = -55°C to +125°C versions only.
3. For I/Os (0-15).
4. For I/Os (16-31).

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AC TEST CONDITIONS (EEPROM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2826 tbl 08

AC ELECTRICAL CHARACTERISTICS (EEPROM)

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C or 0°C to +70°C)

Symbol	Parameters	-75		-95		-125		-150		-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	75	—	95	—	125	—	150	—	200	—	ns
t_{AA}	Address Access Time	—	75	—	95	—	125	—	150	—	200	ns
t_{ACS}	Chip Select Access Time	—	75	—	95	—	125	—	150	—	200	ns
t_{OE}	Output Enable to Output Valid	—	40	—	50	—	55	—	70	—	80	ns
t_{CHZ} (1)	Chip Select to Output in High Z	0	40	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t_{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t_{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t_{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t_{CS}	$\overline{CS}$ Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{CH}	$\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
PAGE MODE WRITE CYCLE												
t_{WC}	Write Cycle Time	0.4	10	0.4	10	0.4	10	0.4	10	0.4	10	ms
t_{AH}	Address Hold Time	50	—	50	—	50	—	50	—	50	—	ns
t_{AS}	Address Setup Time	2	—	2	—	2	—	2	—	2	—	ns
t_{DS}	Data Set-up Time	55	—	55	—	55	—	55	—	55	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	105	—	105	—	105	—	105	—	105	—	ns
t_{BLC}	Byte Load Cycle Time	0.2	200	0.2	200	0.2	200	0.2	200	0.2	200	µs
t_{WPH}	Write Pulse Width High	55	—	55	—	55	—	55	—	55	—	ns
DATA POLLING CYCLE												
t_{DH} (1)	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ms
t_{OEH} (1)	Output Enable Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OE} (1)	Output Enable to Output Delay	—	100	—	100	—	100	—	100	—	100	ns
t_{WR} (1)	Write Recovery Time	2	—	2	—	2	—	2	—	2	—	ns

2826 tbl 09

NOTE:
1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS (SRAM)

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2826 tbl 10

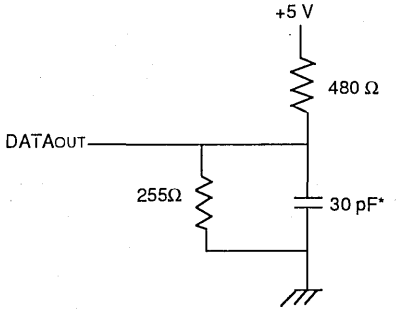


Figure 1. Output Load 2826 drw 03

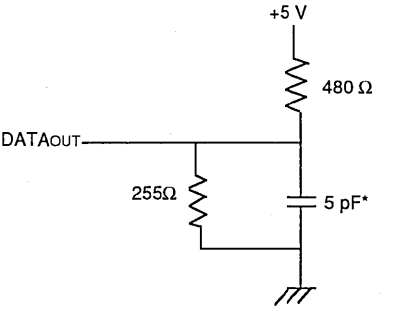


Figure 2. Output Load 2826 drw 04
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15[2] Min.	-15[2] Max.	-17[2] Min.	-17[2] Max.	-20[2] Min.	-20[2] Max.	-25 Min.	-25 Max.	-30 Min.	-30 Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	2	—	2	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	12	—	15	ns
tOHZ[1]	Output Disable to Output in High Z	—	6	—	7	—	7	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Ouput in High Z	—	6	—	8	—	9	—	12	—	13	ns
tDW	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.

2711 tbl 09

7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

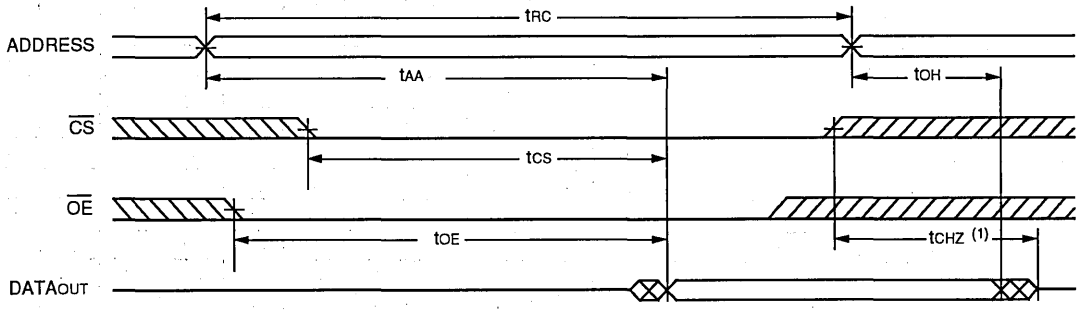
Symbol	Parameters	-35		-40		-50		-60 (Mil. Only)		-70 (Mil. Only)		-85 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	30	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	20	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	45	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	16	—	16	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

2711 tbl 10

NOTE:
1. This parameter is guaranteed by design, but not tested.

EEPROM TIMING WAVEFORMS

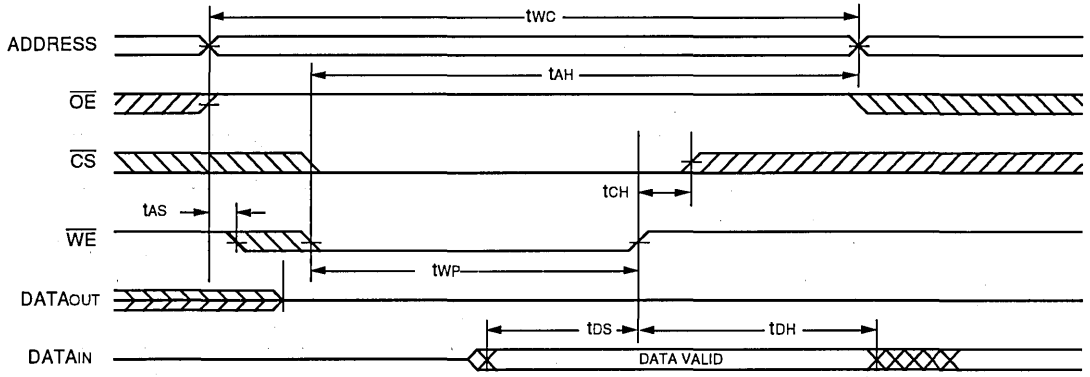
TIMING WAVEFORM OF READ CYCLE[1]



2826 drw 05

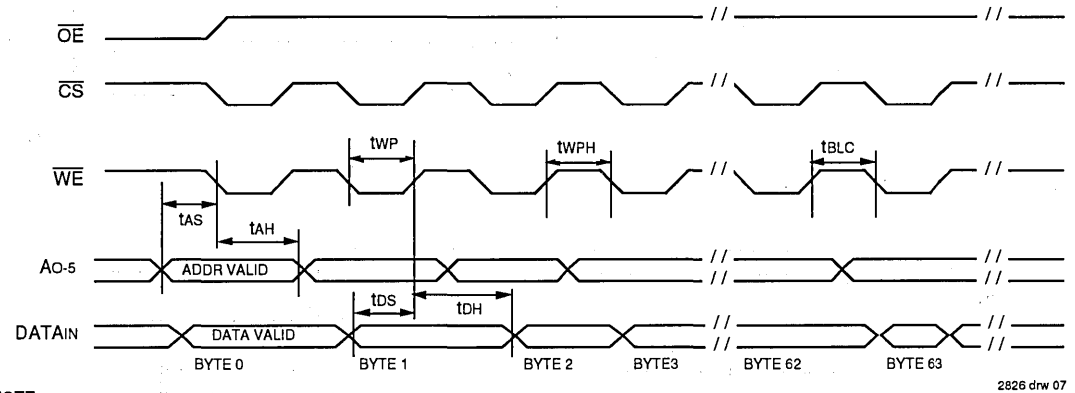
NOTES:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF PAGE MODE WRITE CYCLE (1)

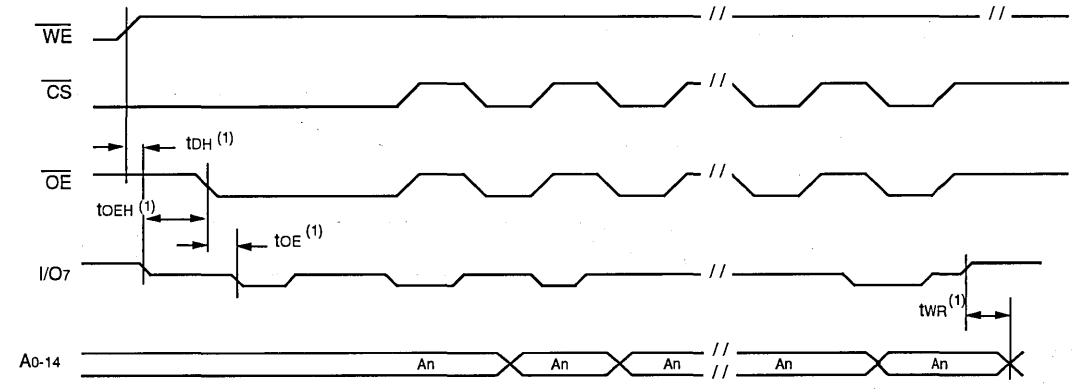
2826 drw 06



2826 drw 07

NOTE:
1. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

TIMING WAVEFORM OF $\overline{DATA}$ POLLING CYCLE

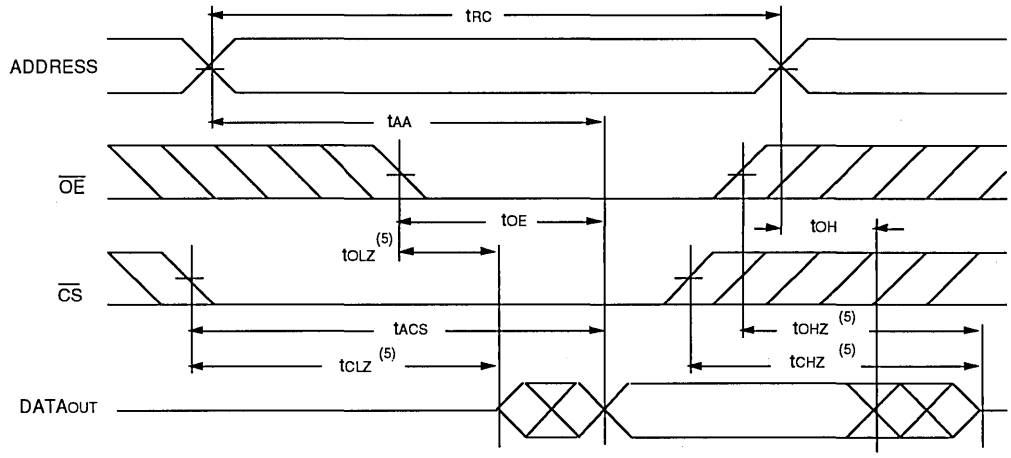


2826 drw 08

NOTES:
1. This parameter is guaranteed by design but not tested.
2. A6 through A14 must specify the page address during each High to Low transitions of $\overline{WE}$ (or $\overline{CS}$). $\overline{OE}$ must be High only when $\overline{WE}$ and $\overline{CS}$ are both Low.

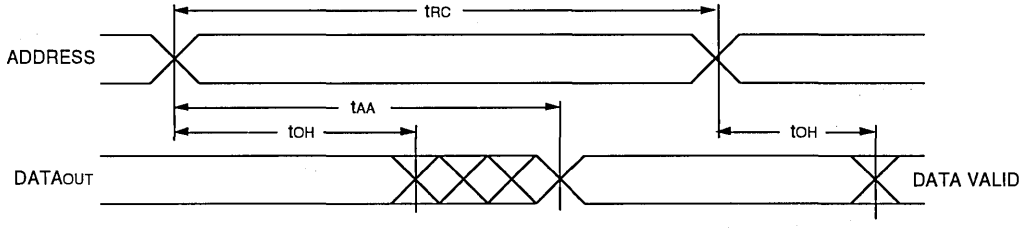
SRAM TIMING WAVEFORMS

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



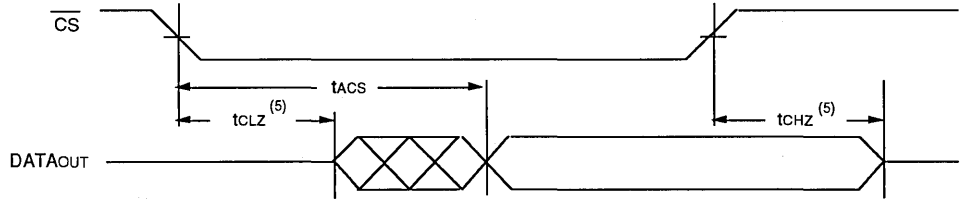
2826 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2826 drw 10

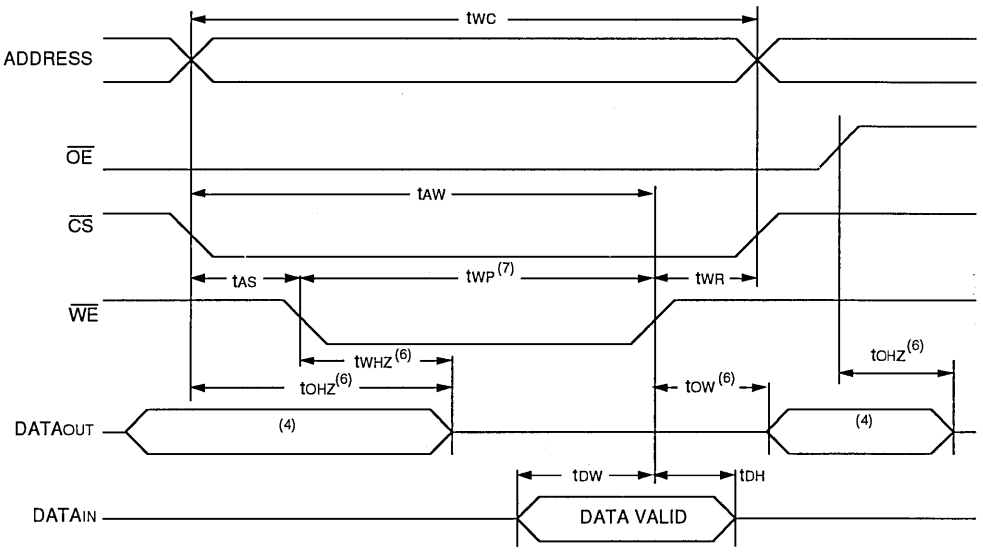
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2826 drw 11

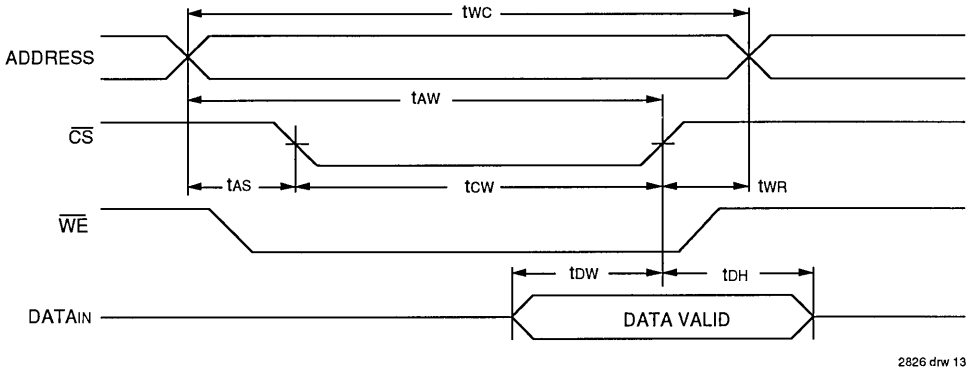
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)



2826 drw 12

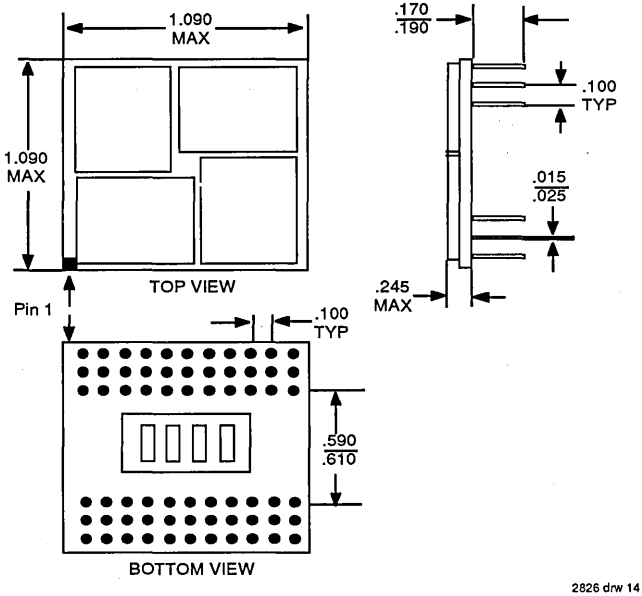
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



2826 drw 13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

PACKAGE DIMENSIONS



2826 drw 14

Integrated Device Technology, Inc.

FAST CMOS 32-BIT BUFFER/LINE DRIVER AND BIDIRECTIONAL TRANSCEIVER MODULES

IDT7MP9244T/AT/CT
IDT7MP9245T/AT/CT

FEATURES:

- High density 32-bit FCT Logic modules
- Equivalent to FAST™ speed and drive
- Low profile module 75-pin ZIP (Zig-zag In-line vertical Package)
- Uses 70 mil pitch leads for maximum density
- Surface mount components on a multilayer epoxy laminate (FR-4) substrate
- True TTL input and output compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
  - — I_{OL} = 64mA
- CMOS power levels (10mW typ. static)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION:

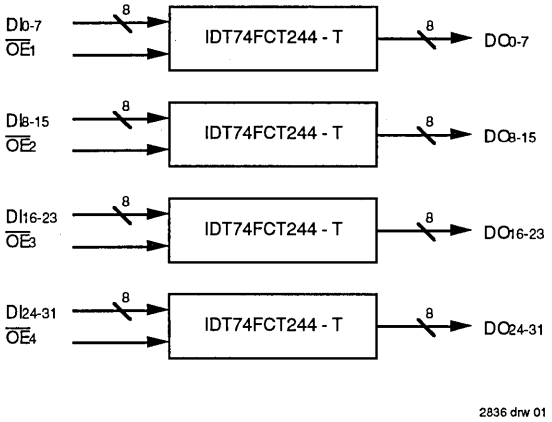
The IDT7MP9244T/AT/CT and IDT7MP9245T/AT/CT logic modules are designed to be employed as 32-bit memory and address drivers, clock drivers and bus-oriented transmitter/receivers which require maximum board packing density. The IDT FCT logic components are built using advanced CEMOS™, a dual metal CMOS technology.

The IDT7MP9244T/AT/CT has byte output enable control and the IDT7MP9245T/AT/CT has word output enable and transmit/receive control.

The IDT7MP9244T/AT/CT and IDT7MP9245T/AT/CT are packaged in a 75 pin ZIP (Zig-zag In-line vertical Package) module offering the optimum in packing density. The dual row (70 mil lead pitch) vertical configuration allows 75 pins to be placed on a package 2.65 inches long, 510 mils tall and only 180 mils thick, resulting in a three-fold density improvement over an equivalent monolithic though-hole implementation.

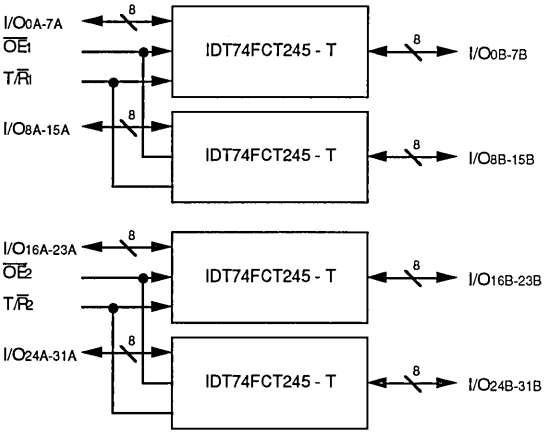
FUNCTIONAL BLOCK DIAGRAMS

IDT7MP9244



2836 drw 01

IDT7MP9245



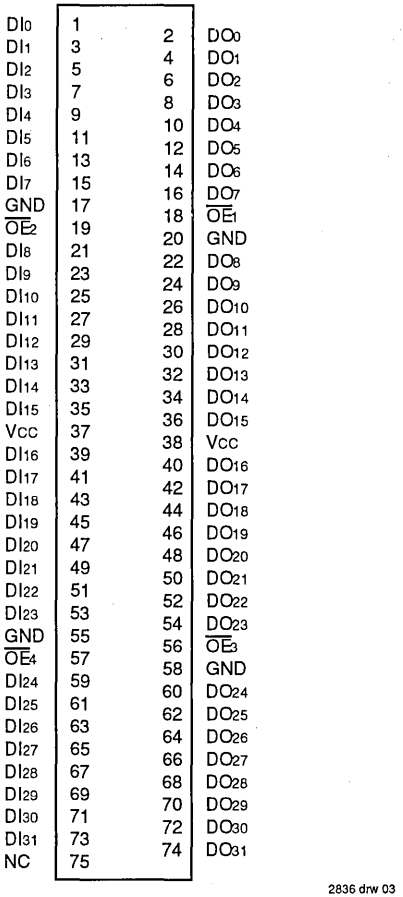
2836 drw 02

7

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATION

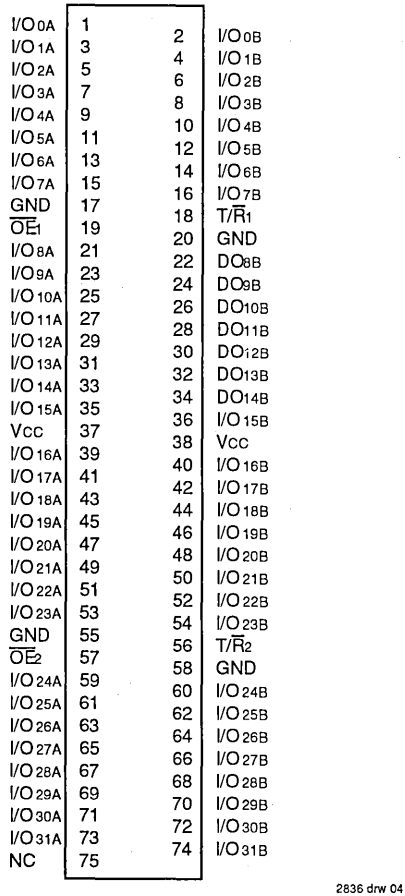
IDT7MP9244



2836 drw 03

ZIP
TOP VIEW

IDT7MP9245



2836 drw 04

ZIP
TOP VIEW

PIN DESCRIPTION - 7MP9244

Pin Names	Description
$\overline{OE}_1$- $\overline{OE}_4$	3–State Output Enable Inputs (Active LOW)
DI0-31	Inputs
DO0-31	Outputs

2836 tbl 01

PIN DESCRIPTION - 7MP9245

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3–State Output Enable Inputs (Active LOW)
T/$\overline{R}_1$, T/$\overline{R}_2$	Transmit/Receive Inputs
I/O0A-31A	Side A Inputs or 3-State Outputs
I/O0B-31B	Side BInputs or 3-State Outputs

2836 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTES: 2836 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1)

7MP9244			7MP9245		
Inputs		Outputs	Inputs		
$\overline{OE}$	D	O	$\overline{OE}$	T/$\overline{R}$	Outputs
L	L	L	L	L	Bus I/OB Data to Bus I/OA
L	H	H	L	H	Bus I/OB Data to Bus I/OA
H	X	Z	H	X	High-Z State

NOTE: 2836 tbl 04
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, F = 1.0MHZ)

Symbol	Parameter(1)	Conditions	Max.	Unit
$C_{I/O}$	Input Capacitance (I/O)	V_{IN} = 0V	15	pF
C_{CTRL}	Input Capacitance ($\overline{OE}$, T/$\overline{R}$)	V_{IN} = 0V	30	pF

NOTE: 2836 tbl 05
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS(4)

(T_A = 0°C TO +70°C, V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O= 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	2.0	6.0	mA

NOTES: 2836 tbl 06
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS[7]

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5, 6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.5	8.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.8	9.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND 32 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	12.8	26.0	
			V_{IN} = 3.4V V_{IN} = GND	—	20.8	58.0	

2836 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. Gross functional testing is performed on the IDT modules; power supply characteristics of the IDT modules are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9244[1]

Symbol	Parameter	Condition[2]	7MP9244T		7MP9244AT		7MP9244CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	5.6	1.5	5.2	ns

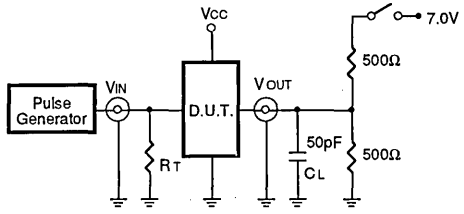
NOTES: 2836 tbl 08
1. Specifications given are for the IDT74FCT244-T components used on the IDT7MP9244. Functional testing is performed on the IDT7M9244 module; switching characteristics for this module is guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR IDT7MP9245[1]

Symbol	Parameter	Condition[2]	7MP9245T		7MP9245AT		7MP9245CT		Unit
			Min.[3]	Max.	Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay I/O_A to I/O_B, I/O_B to I/O_A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_A or I/O_B		1.5	9.5	1.5	6.2	1.5	5.8	ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}$ to I/O_A or I/O_B		1.5	7.5	1.5	5.0	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $T/\overline{R}$ to I/O_A or I/O_B		1.5	9.5	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $T/\overline{R}$ to I/O_A or I/O_B		1.5	7.5	1.5	5.0	1.5	4.8	ns

NOTES: 2836 tbl 09
1. Specifications given are for the IDT74FCT245-T components used on the IDT7MP9245. Functional testing is performed on the IDT7MP9245 module; switching characteristics for this module is guaranteed by design but not tested.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS (FOR ALL OUTPUTS)



2836 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

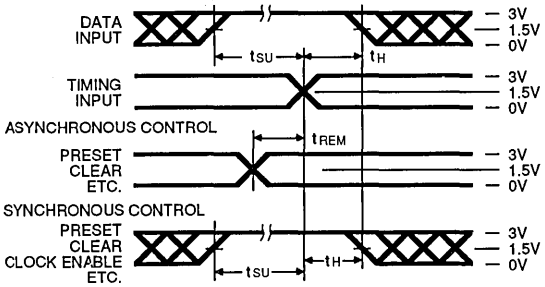
2836 tbl 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

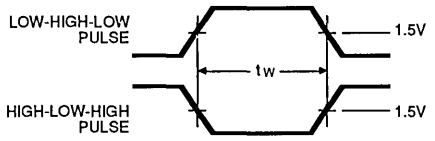
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



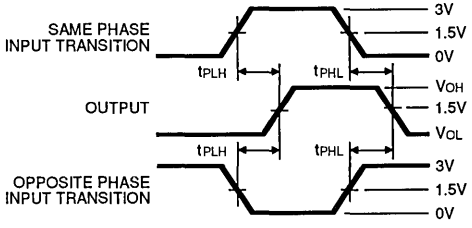
2836 drw 06

PULSE WIDTH



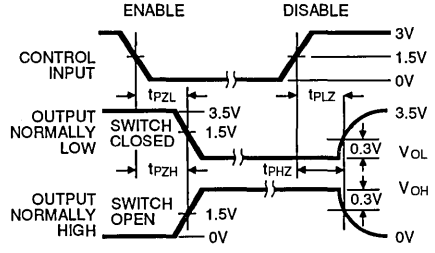
2836 drw 08

PROPAGATION DELAY



2836 drw 07

ENABLE AND DISABLE TIMES

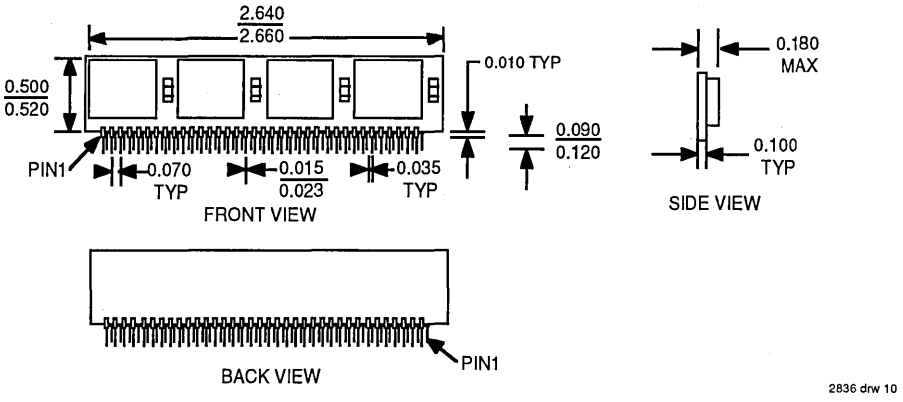


2836 drw 09

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

PACKAGE DIMENSIONS



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