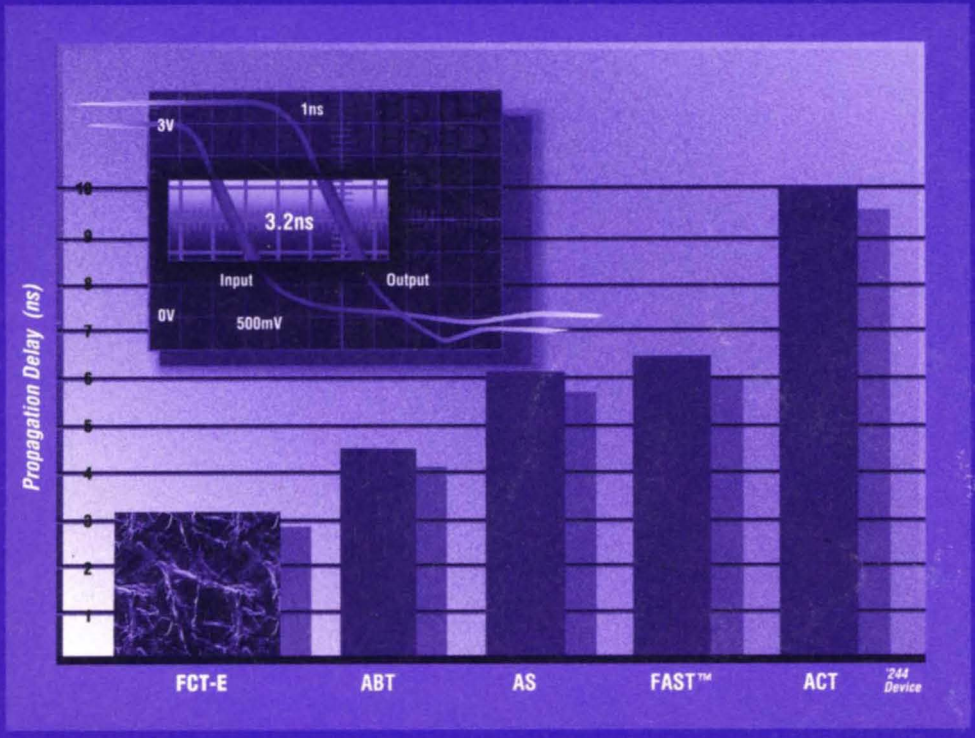
IDT
FCT-E Speed
Double-Density™ Logic
Product Information



Integrated Device Technology, Inc.

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LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

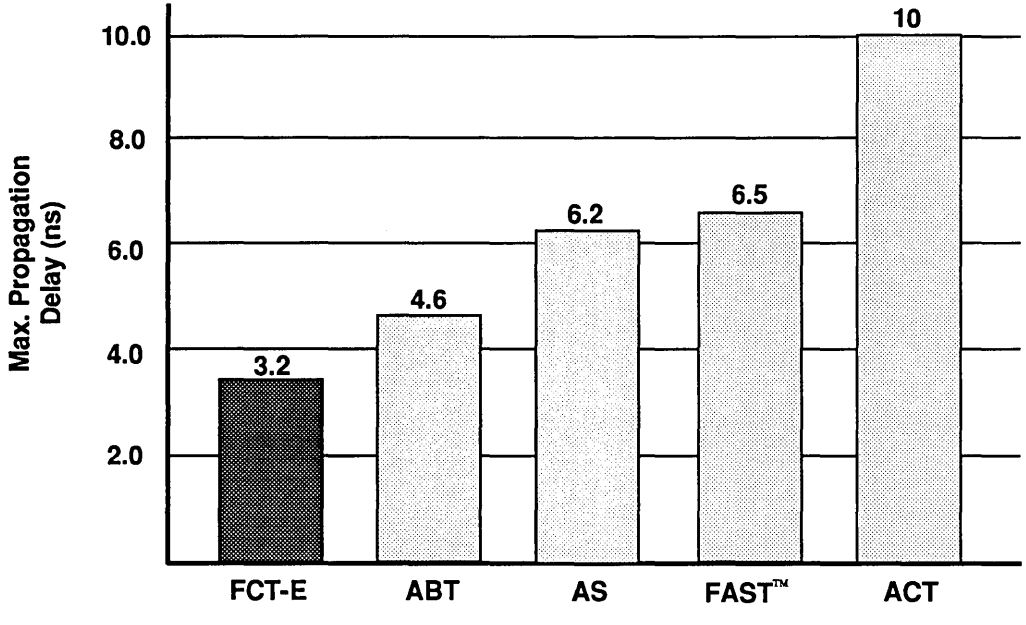
Integrated Device Technology, Inc.

INTRODUCTION

Increase performance and reduce board area with new Double-Density™ FCT-E Speed logic!

THE FASTEST LOGIC

IDT's FCT Double-Density logic is now available in "E-Speed" grade, making it the highest performing CMOS logic available. Propagation delays are as low as 3.2ns (tpd max.), making it 30% faster than alternative Widebus™ and other CMOS-based solutions. This is the ideal solution for 75MHz and 100MHz workstations, and 66MHz Pentium™ designs. And unlike those other logic families, you get increased performance without an increase in power dissipation. IDT's new Double-Density E-Speed devices use significantly less power than any other CMOS, BiCMOS, or Bipolar logic family, increasing system reliability and extending battery life.



TWICE THE LOGIC IN HALF THE SPACE

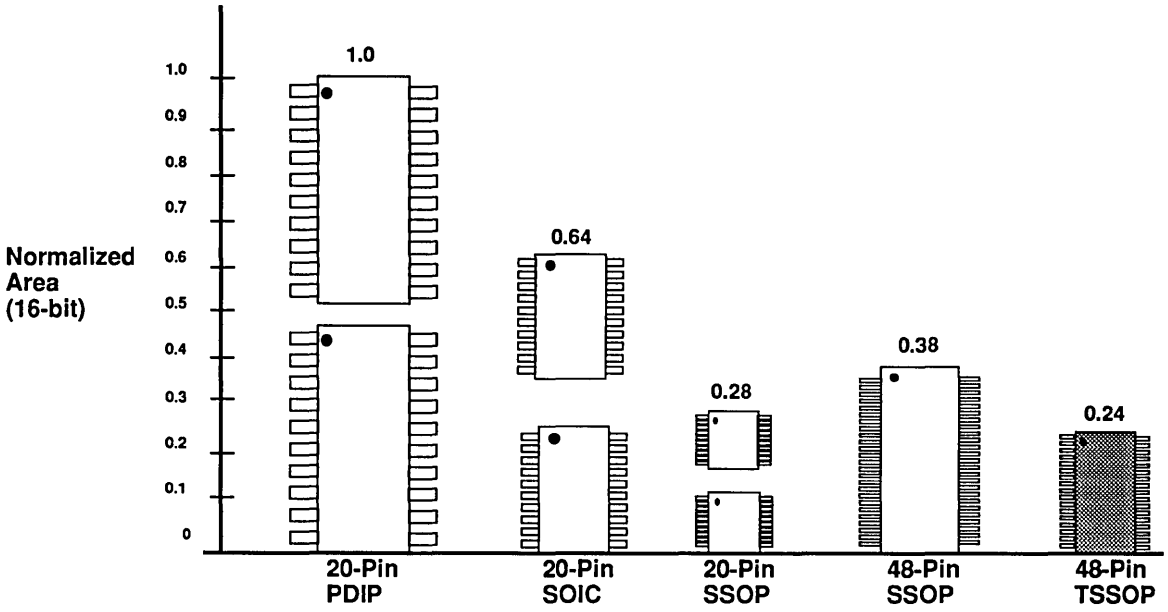
IDT's Double-Density logic is comprised of 16-, 18-, and 20-bit wide, extra quiet, very low power, high-performance CMOS bus interface logic products. Double-Density logic is an extension of IDT's earlier family of octal FCT-T devices, but with wider data paths to support present and future microprocessor architectures and bus requirements.

PCMCIA COMPATIBLE PACKAGING REDUCES BOARD AREA BY 62%

Applications such as PCMCIA cards demand small, low-profile packages. IDT Double-Density logic's Thin Shrink Small Outline Package (TSSOP) is 1.09mm thin, and is PCMCIA type I, II, III compliant. The TSSOP package is also an excellent choice for daughter boards or any application requiring high levels of integration where saving space is critical.

IDT's low-profile, compact 48- and 56-pin TSSOP packages reduce PC board area requirements and increase integration levels. TSSOP packages save over 62% board area compared to two SOICs, and over 35% board area compared to 48- or 56-pin SSOPs!

COMPACT IDT TSSOP PACKAGE SAVES SPACE



FCT-E SPEED DOUBLE-DENSITY LOGIC IS AVAILABLE IN TWO CONFIGURATIONS:

5V operation with High-Drive outputs and 5V operation with Balanced-Drive outputs.
The High-Drive version provides –32mA/+64mA (IOH/IOL) drive and has a power off disable feature that allows power to be applied to inputs, outputs, or I/Os, even when Vcc is not present, eliminating concerns about power sequencing or hot-board insertions. This makes the High-Drive configuration ideal for heavy capacitive loads, terminated lines, loaded backplanes, and applications requiring live insertion.

The Balanced-Drive version provides –24mA/+24mA (IOH/IOL) drive with integrated series terminating resistors for driving highly capacitive loads, such as memory. The resistors improve the quality of signals being transmitted by minimizing the imbalance between the internal source impedance and the external line impedance. Incorporating the resistors within the IC minimizes board space, and makes your PC board more compact. The Balanced-Drive outputs also help reduce the magnitude of simultaneous switching noise (ground bounce) to less than 600mV (typ.), improving system signal integrity and increasing system performance. This makes the Balanced-Drive configuration ideal for driving memory, on-board buses, low EMI situations, and general applications.

EASILY UPGRADE SYSTEM PERFORMANCE

The FCT-E Speed Double-Density Logic is an extension of IDT's presently available FCT, FCT-A, and FCT-C Speed Double-Density Logic and offers an easy upgrade path for increasing your system performance. Simply replace your present, lower speed logic with IDT's pin, function, and package compatible high-speed FCT-E Logic for an instant performance increase.

OTHER HIGH PERFORMANCE LOGIC PRODUCTS FROM IDT

Also available from IDT are 3.3V Double-Density Logic, 5V Octal Logic, 3.3V Octal Logic, Low Skew Clock Drivers and Clock Generators, and Complex Logic Products. For more information on these products, or any of IDT's other product lines, please contact your local IDT sales office.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16240T/AT/CT/ET
IDT54/74FCT162240T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16240T/AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162240T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

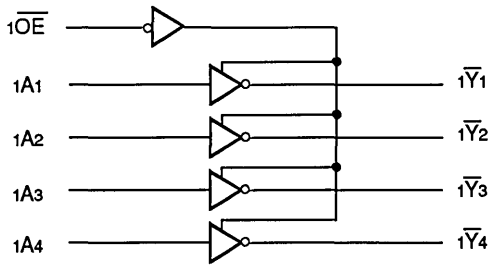
DESCRIPTION:

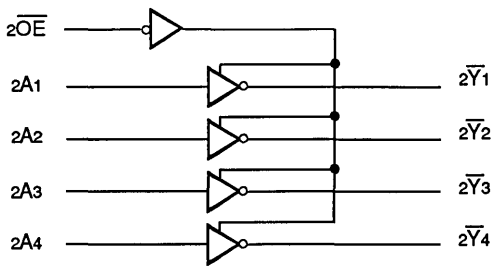
The IDT54/74FCT16240T/AT/CT/ET and IDT54/74FCT162240T/AT/CT/ET 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. The flow-through organization of signal pins simplifies layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16240T/AT/CT/ET are ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162240T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162240T/AT/CT/ET are plug-in replacements for IDT54/74FCT16240T/AT/CT/ET and 54/74ABT16240 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM





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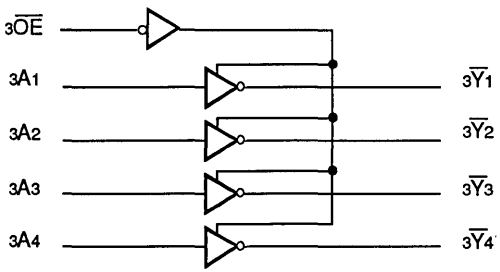

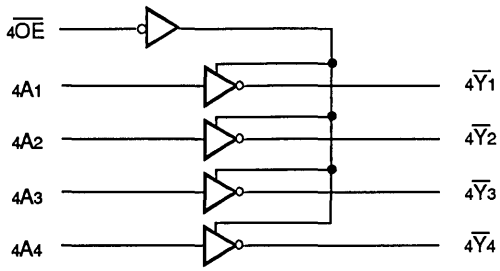

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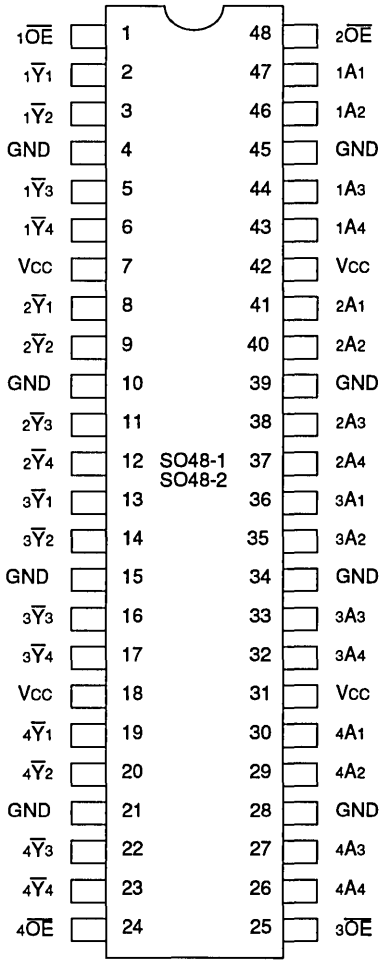
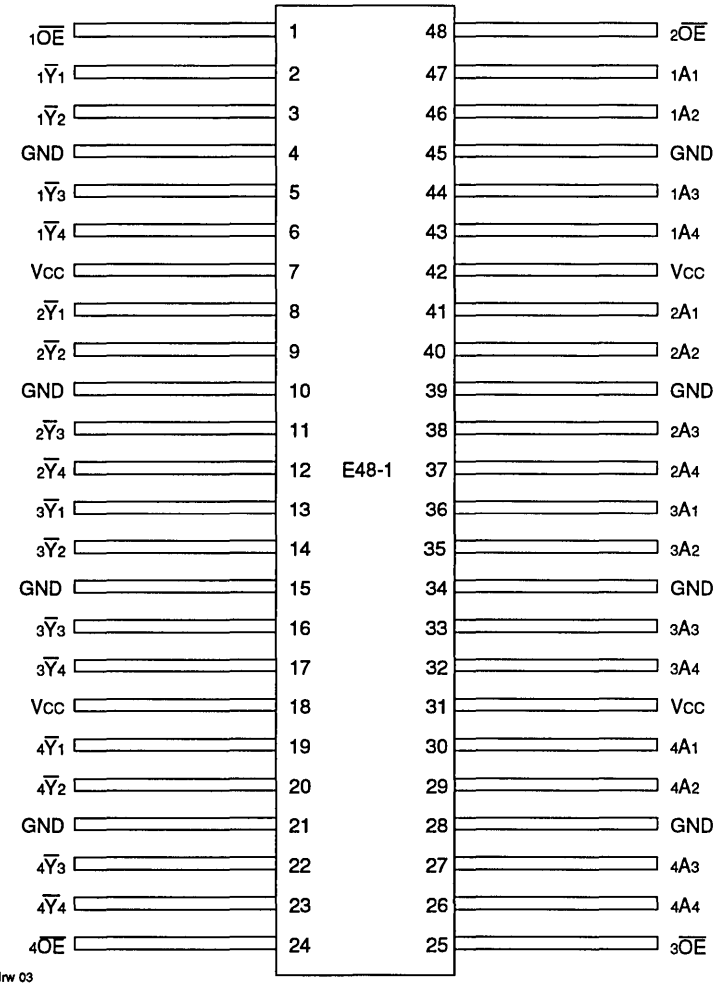
PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2541 drw 03



2541drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs
$x\overline{Y}x$	3-State Outputs

2541 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	$x\overline{Y}x$
L	L	H
L	H	L
H	X	Z

NOTE: 2541 tbl 02

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2541 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2541 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2541 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2541 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2541 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

NOTES:

2541 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16240T/162240T				FCT16240AT/162240AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16240CT/162240CT				FCT16240ET/162240ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	4.7	1.5	3.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

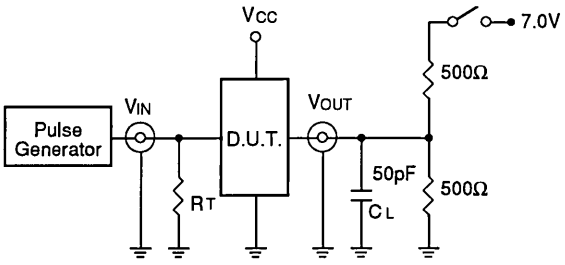
NOTES:

2541 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2541 drw 05

SWITCH POSITION

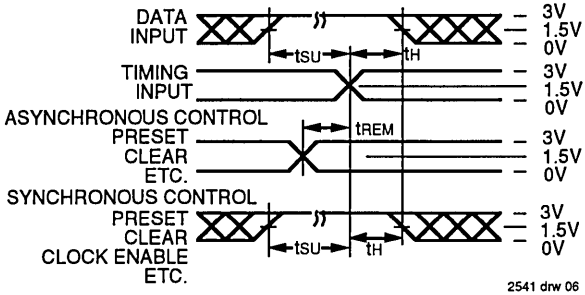
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2541 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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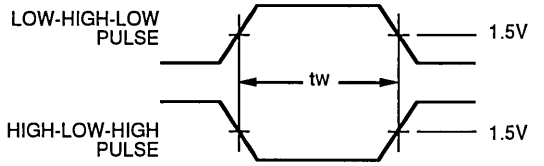
PULSE WIDTH



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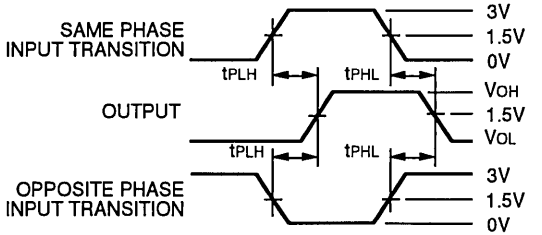
PROPAGATION DELAY



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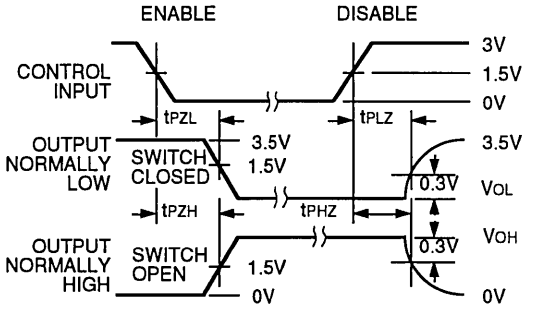
ENABLE AND DISABLE TIMES

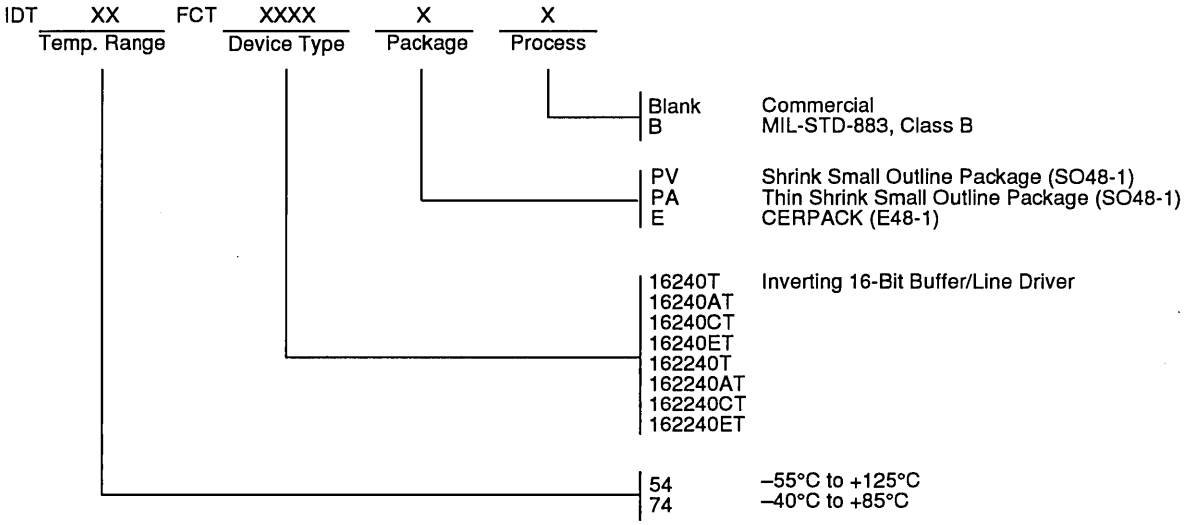


2541 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2541 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16244T/AT/CT/ET
IDT54/74FCT162244T/AT/CT/ET
IDT54/74FCT166244T/AT//CT
IDT54/74FCT16XH244T/AT/CT/ET
ADVANCE INFORMATION

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack packages and 19.6 mil pitch TSSOP package
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16244T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162244T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT166244T/AT/CT:**
  - Light Drive Balanced Output: ±8mA (commercial), ±6mA (military)
  - Minimal system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.4V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT16XH244AT/CT/ET:**
  - Bus Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors.

DESCRIPTION:

The 16-Bit Buffer/Line Driver is for bus interface or signal buffering applications requiring high speed and low power dissipation. These devices have a flow through pin organization, and shrink packaging to simplify board layout. All inputs are designed with hysteresis for improved noise margin. The three-state controls allow independent 4-bit, 8-bit or combined 16-bit operation. These parts are plug in replacements for 54/74ABT16244 where higher speed, lower noise or lower power dissipation levels are desired.

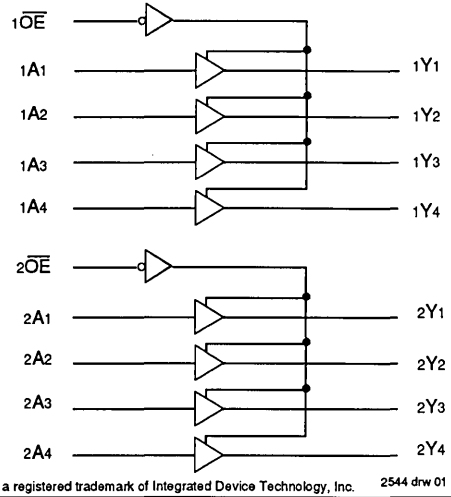
The IDT54/74FCT16244T/AT/CT/ET are ideally suited for driving high capacitance loads (>200pF) and low impedance backplanes. These "high drive" buffers are designed with power off disable capability to allow "live insertion" of boards when used in a backplane interface.

The IDT54/74FCT162244T/AT/CT/ET have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors while still providing very high speed operation for loads of less than 200pF.

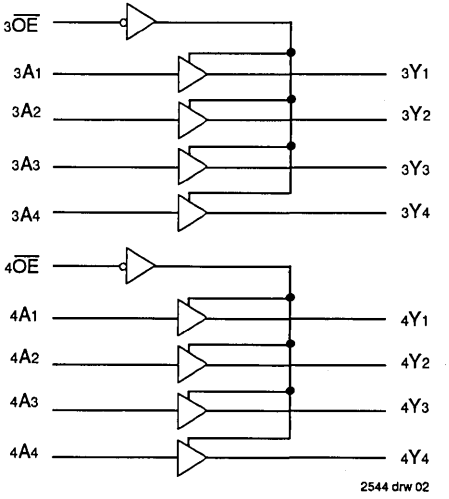
The IDT54/74FCT166244T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<50pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

The IDT54/74FCT16XH244T/AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull up resistors.

FUNCTIONAL BLOCK DIAGRAM

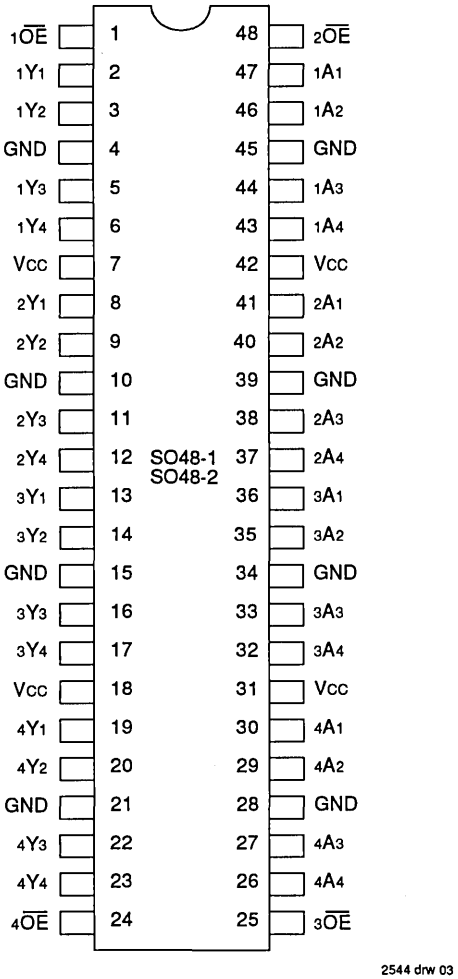


2544 drw 01



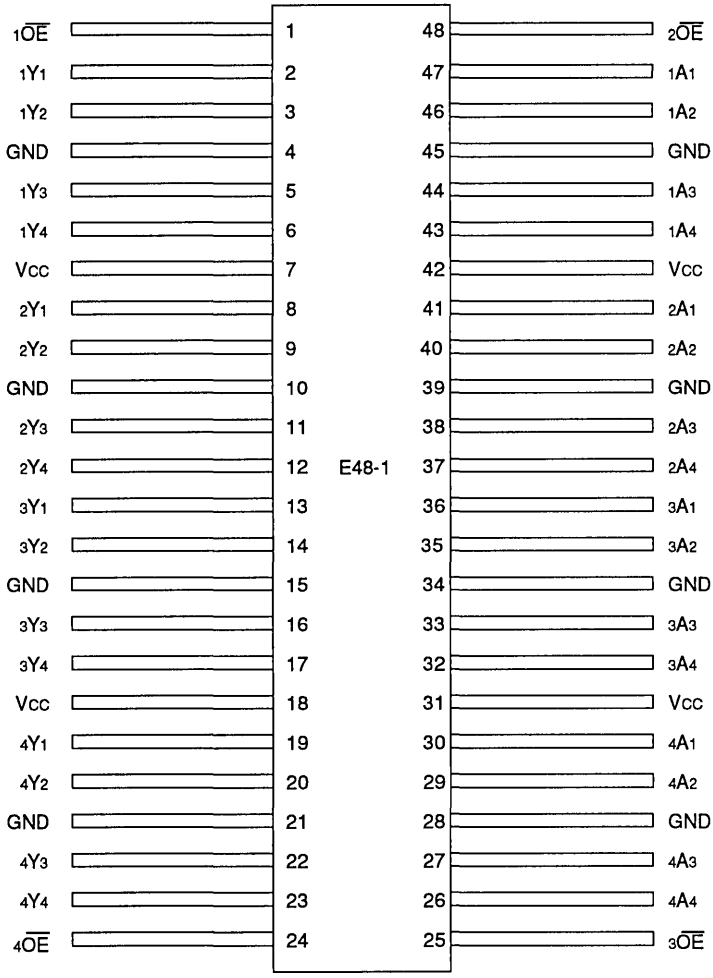
2544 drw 02

PIN CONFIGURATIONS



2544 drw 03

SSOP
TSSOP
TOP VIEW



2544 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs[1]
xYx	3-State Outputs

NOTE: 2544 tbl 01

1. On FCT16XH244T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

NOTE: 2544 tbl 02

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2544 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT and FCT166XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2544 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 lnk 05

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Symbol	Parameter		Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(6)	Standard Input(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O(5)			—	—	±1	
		Bus Hold Input			±100	—	—	
		Bus Hold I/O			±100	—	—	
I_{IL}	Input LOW Current(6)	Standard Input(5)		V_I = GND	—	—	±1	
		Standard I/O(5)			—	—	±1	
		Bus Hold Input			±100	—	—	
		Bus Hold I/O			±100	—	—	
$I_{I(HOLD)}$	Input Current(6)	Bus Hold Input	V_{CC} = Min.	V_I = 2.4V	–50	—	—	µA
				V_I = 0.4V	+50	—	—	
I_{OZH}	High Impedance Output Current		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)			V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current		V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Pins with Bus Hold are identified in the pin description.

OUTPUT DRIVE CHARACTERISTICS FOR FCT16244T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2544 lnk 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT162244T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2544 lnk 08

OUPUT DRIVE CHARACTERISTICS FOR FCT166244T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		24	48	72	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		–24	–48	–72	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA MIL. I_{OL} = 8mA COM'L.	—	0.3	0.55	V

2544 lnk 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

2544 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT16244T/FCT162244T

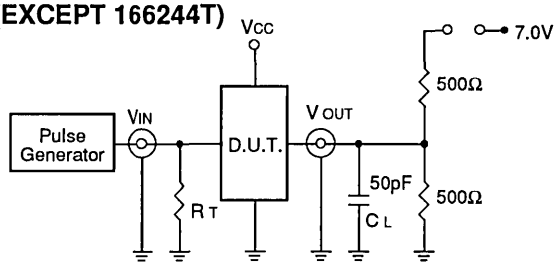
Symbol	Parameter	Condition[1]	FCT16244T/162244T/166244T[4]				FCT16244AT/162244AT/166244AT[4]				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16244CT/162244CT/166244CT[4]				FCT16244ET/162244ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	4.1	1.5	4.6	1.5	3.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. C_L = 20pF for FCT166244T/AT/CT.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS (EXCEPT 166244T)



2544 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

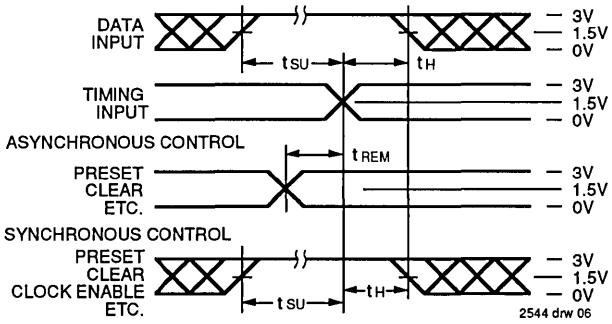
2544 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

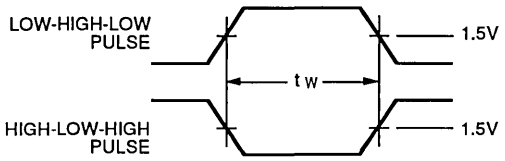
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



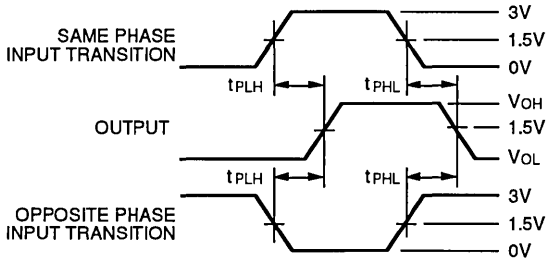
2544 drw 06

PULSE WIDTH



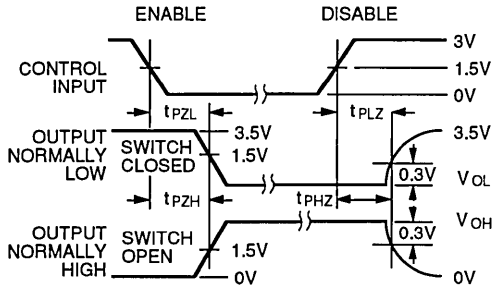
2544 drw 07

PROPAGATION DELAY



2544 drw 08

ENABLE AND DISABLE TIMES

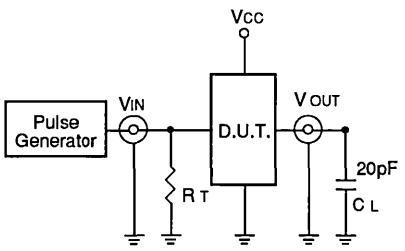


2544 drw 09

NOTES:

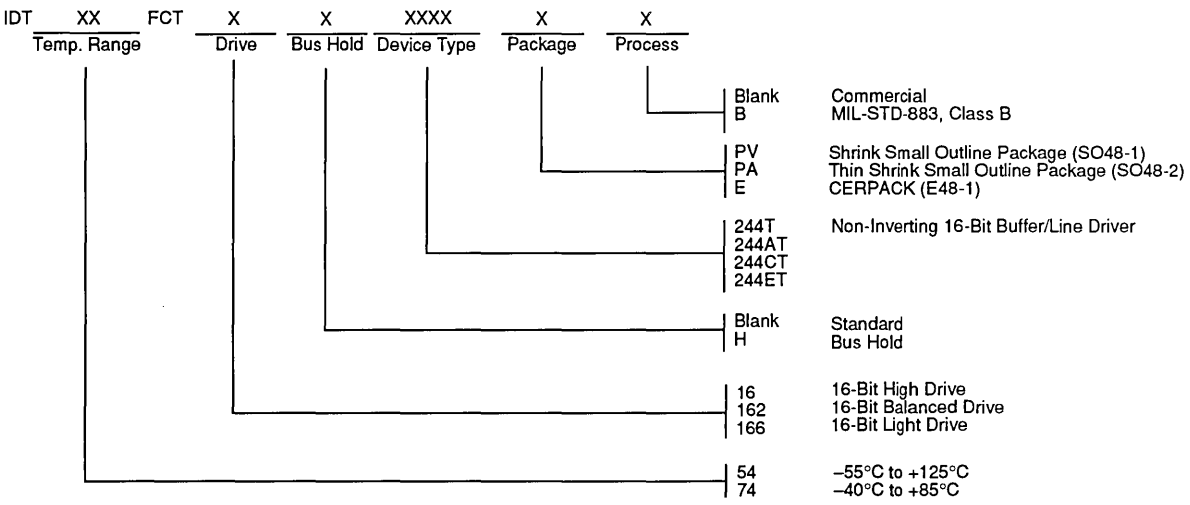
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

TEST CIRCUITS FOR 166244T OUTPUTS



2544 drw 10

ORDERING INFORMATION



2544 drw 11

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT16245T/AT/CT/ET
IDT54/74FCT162245T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16245T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162245T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

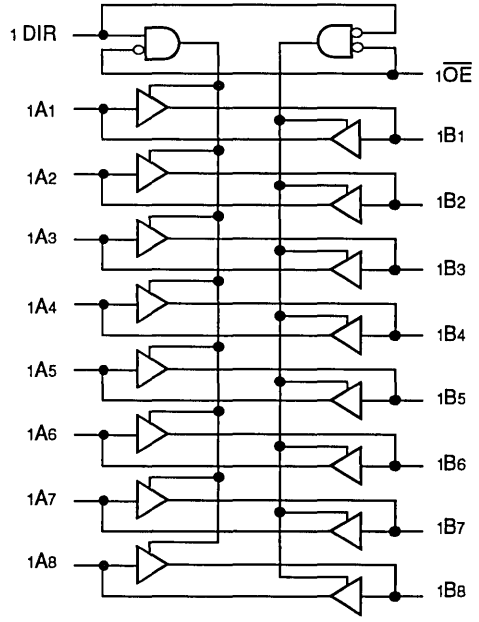
DESCRIPTION:

The IDT54/74FCT16245T/AT/CT/ET and IDT54/74FCT162245T/AT/CT/ET 16-bit transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($x\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

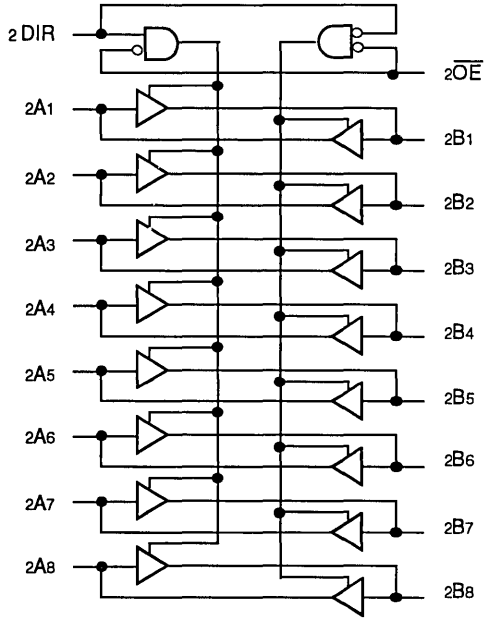
The IDT54/74FCT16245T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162245T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162245T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16245T/AT/CT/ET and 54/74ABT16245 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

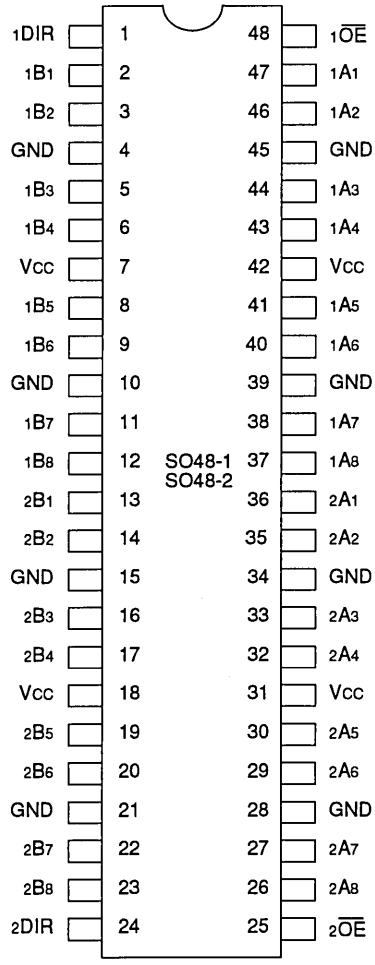


2545 drw 01



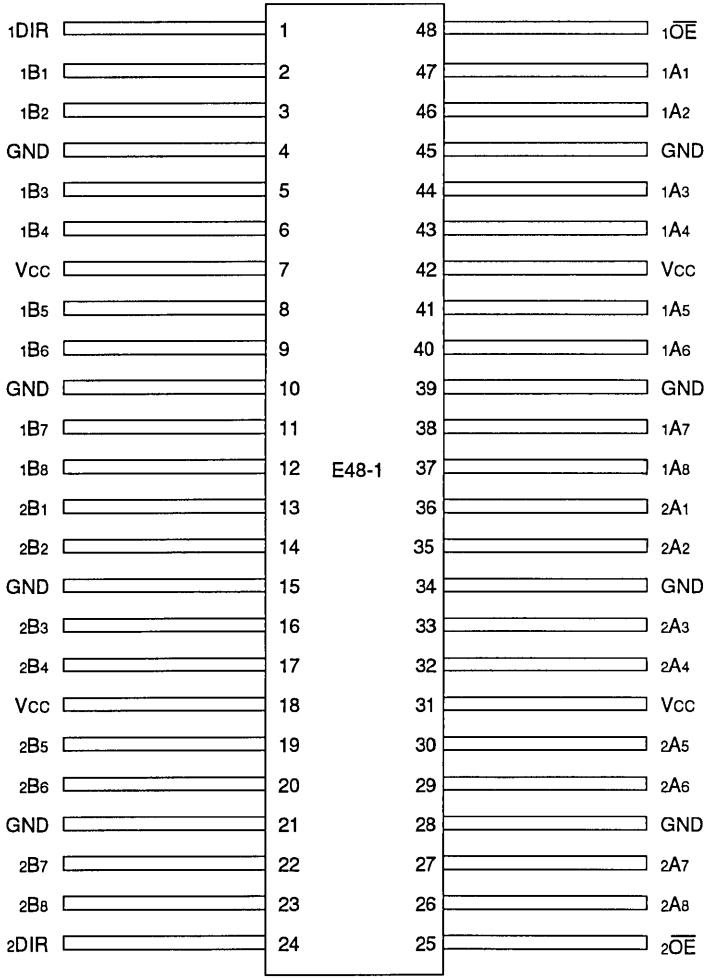
2545 drw 02

PIN CONFIGURATIONS



2545 drw 03

SSOP
TSSOP
TOP VIEW



2545 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

2545 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE: 2545 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2545 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2545 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2545 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16245T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2545 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162245T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2545 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

2345 tbl 08

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula.These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16245T/162245T				FCT16245AT/162245AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
tPZH tPZL	Output Enable Time x$\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
tPZH tPZL	Output Enable Time xDIR to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time xDIR to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16245CT/162245CT				FCT16245ET/162245ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50pF RL = 500Ω	1.5	4.1	1.5	4.5	1.5	3.2	—	—	ns
tPZH tPZL	Output Enable Time x$\overline{OE}$ to A or B		1.5	5.8	1.5	6.2	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to A or B		1.5	4.8	1.5	5.2	1.5	4.0	—	—	ns
tPZH tPZL	Output Enable Time xDIR to A or B[3]		1.5	5.8	1.5	6.2	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xDIR to A or B[3]		1.5	4.8	1.5	5.2	1.5	4.0	—	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

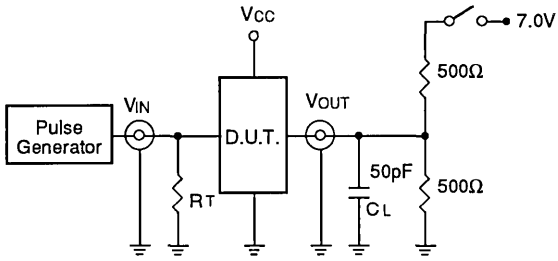
NOTES:

2545 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2545 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

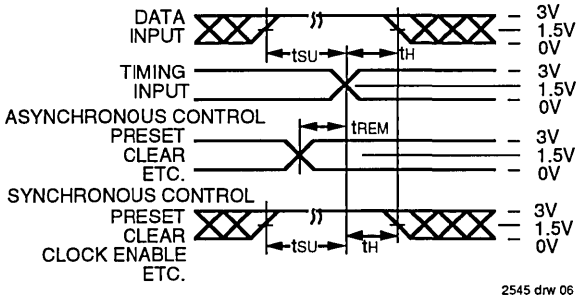
2545 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

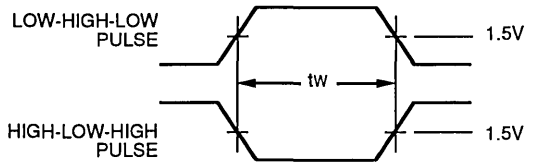
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



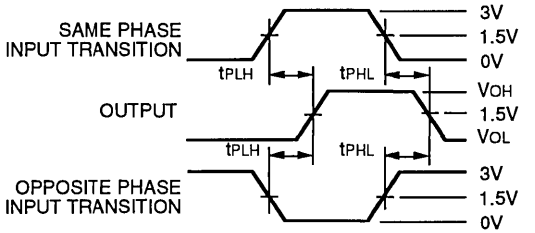
2545 drw 06

PULSE WIDTH



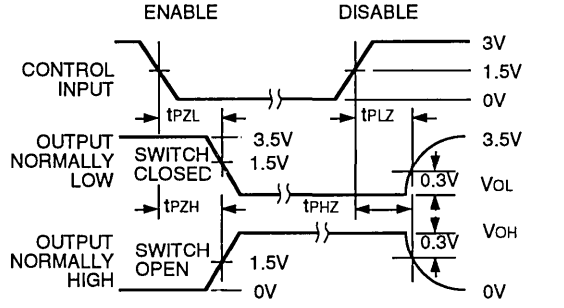
2545 drw 07

PROPAGATION DELAY



2545 drw 08

ENABLE AND DISABLE TIMES

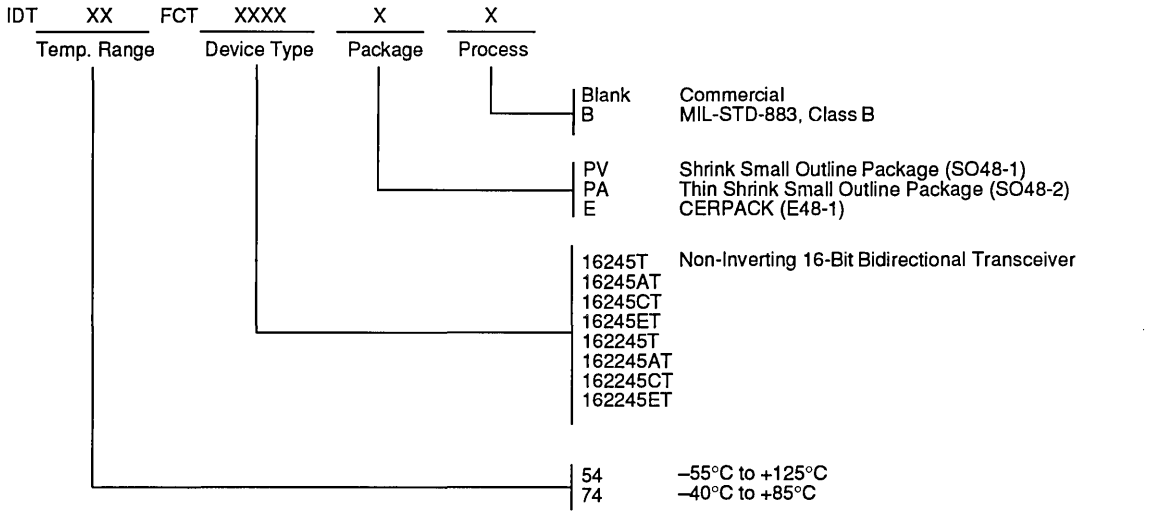


2545 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2545 drw 10

Integrated Device Technology, Inc.

FAST CMOS 12-BIT TRI-PORT BUS EXCHANGER

IDT54/74FCT16260AT/CT/ET
IDT54/74FCT162260AT/CT/ET
ADVANCE INFORMATION

FEATURES:

- **Common features:**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack packages and 19.6 mil pitch TSSOP package
  - Low power dissipation (significantly lower than BiCMOS technologies)
  - High-speed 12-bit bus exchanger for interbus communication:
    Multi-way interleaving memory
    Multiplexed address or data busses
  - Bidirectional operation
- **Features for FCT16260AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
  - Direct low-impedance backplane interface
- **Features for FCT162260AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

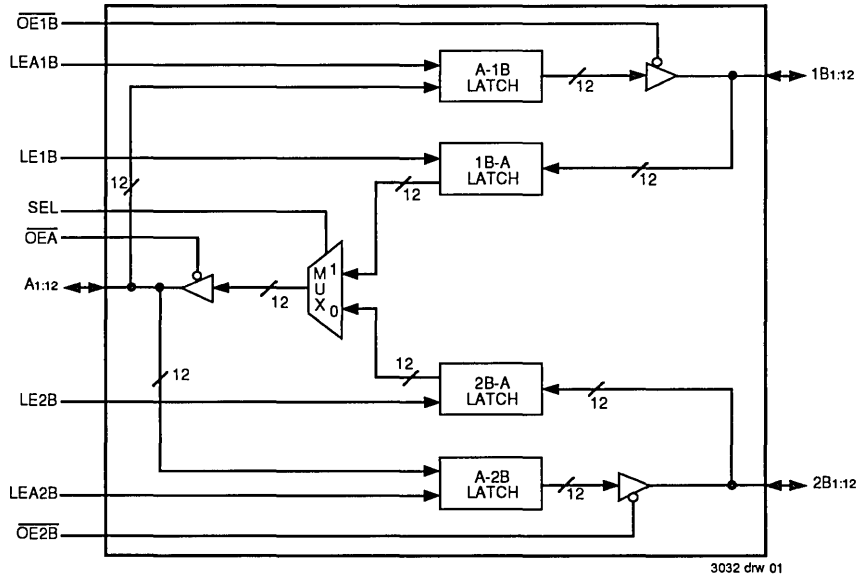
The IDT54/74FCT16260AT/CT/ET and the IDT54/74FCT162260AT/CT/ET Tri-Port Bus Exchangers are high-speed 12-bit latched bus multiplexers/transceivers for use in high-speed microprocessor applications. These Bus Exchangers support memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

The Tri-Port Bus Exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is HIGH, the latch is transparent. When a latch-enable input is LOW, the data at the input is latched and remains latched until the latch enable input is returned HIGH. Independent output enables ($\overline{OE1B}$ and $\overline{OE2B}$) allow reading from one port while writing to the other port.

The IDT54/74FCT16260AT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162260AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times - reducing the need for external series terminating resistors.

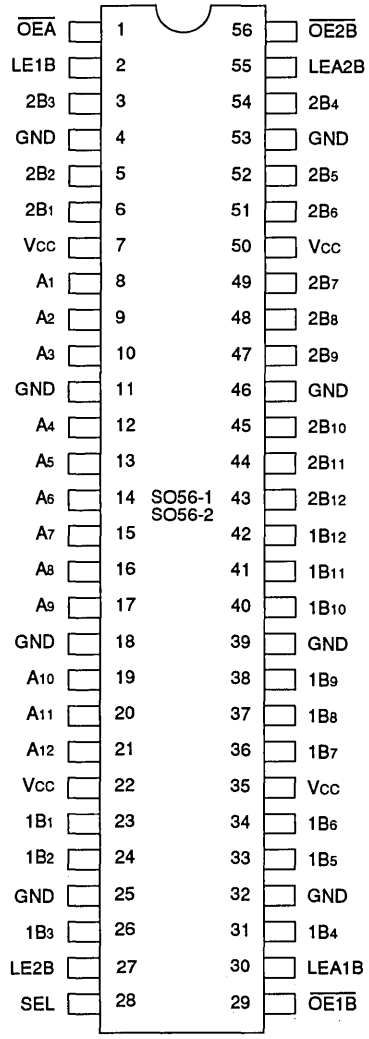
FUNCTIONAL BLOCK DIAGRAM



3032 drw 01

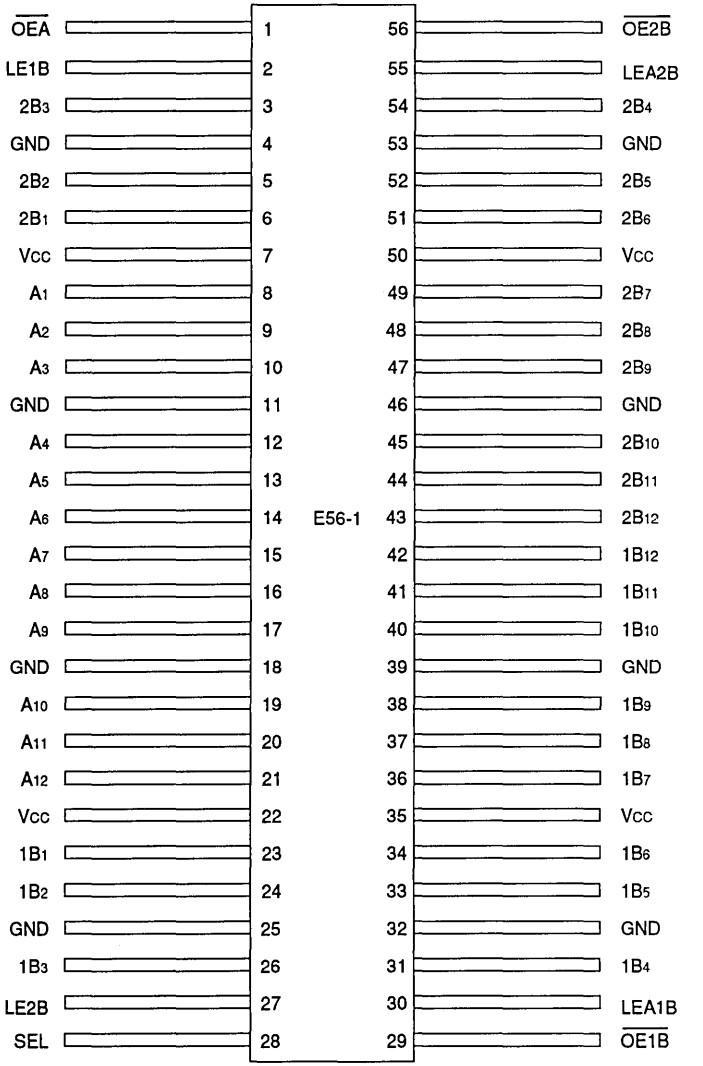
The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3032 drw 02



CERPACK
TOP VIEW

3032 drw 03

PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.
1B(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory.
2B(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-Port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for the 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for the 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OEA}$	I	Output Enable for A Port (Active LOW).
$\overline{OE1B}$	I	Output Enable for 1B Port (Active LOW).
$\overline{OE2B}$	I	Output Enable for 2B Port (Active LOW).

3032 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	-40 to +85	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES: 3032 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 3032 tbl 03

1. This parameter is measured at characterization but not tested.

FUNCTION TABLES(2)

Inputs						Output
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A(1)
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A(1)
X	X	X	X	X	H	Z

3032 tbl 04

Inputs					Outputs	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	B(1)
L	H	L	L	L	L	B(1)
H	L	H	L	L	B(1)	H
L	L	H	L	L	B(1)	L
X	L	L	L	L	B(1)	B(1)
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

3032 tbl 05

NOTES:

1. Output level before the indicated steady-state input conditions were established.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

3032 tbl 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT16260T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

3032 tbl 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT162260T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

3032 lnk 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Output Port Enabled LExx = Vcc One Input Bit Toggling One Output Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle One Output Port Enabled LExx = Vcc One Input Bit Toggling One Output Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.8	3.5[5]	
		50% Duty Cycle One Output Port Enabled LExx = Vcc Twelve Input Bits Toggling Twelve Output Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	4.8	12.5[5]	

3032 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16260AT/162260AT				FCT16260CT/162260CT				FCT16260ET/162260ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Ax to 1Bx or Ax to 2Bx	CL = 50pF RL = 500Ω	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1		TBD		TBD	ns
tPLH tPHL	Propagation Delay 1Bx to Ax or 2Bx to Ax		1.5	5.6	1.5	5.9	1.5	5.0	1.5	5.4		TBD		TBD	ns
tPLH tPHL	Propagation Delay LExB to Ax		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1		TBD		TBD	ns
tPLH tPHL	Propagation Delay LEA1B to 1Bx or LEA2B to 2Bx		1.5	4.7	1.5	5.2	1.5	4.4	1.5	4.8		TBD		TBD	ns
tPLH tPHL	Propagation Delay SEL to Ax		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1		TBD		TBD	ns
tPZH tPZL	Output Enable Time $\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1Bx, or $\overline{OE2B}$ to 2Bx		1.5	5.7	1.5	6.1	1.5	5.1	1.5	5.4		TBD		TBD	ns
tPHZ tPLZ	Output Disable Time $\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1Bx, or $\overline{OE2B}$ to 2Bx		1.5	4.4	1.5	4.8	1.5	4.0	1.5	4.4		TBD		TBD	ns
tSU	Set-Up Time, HIGH or LOW Data to Latch		1.5	—	1.5	—	1.0	—	1.0	—		TBD		TBD	ns
tH	Hold Time, Latch to Data		1.0	—	1.5	—	1.0	—	1.5	—		TBD		TBD	ns
tW	Pulse Width, Latch HIGH[3]		3.0	—	3.0	—	3.0	—	3.0	—		TBD		TBD	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

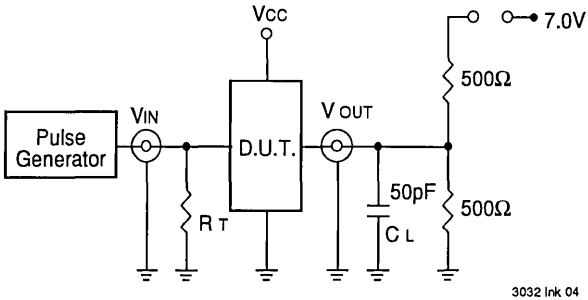
3032 tbl 10

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3032 lnk 04

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Outputs	Open

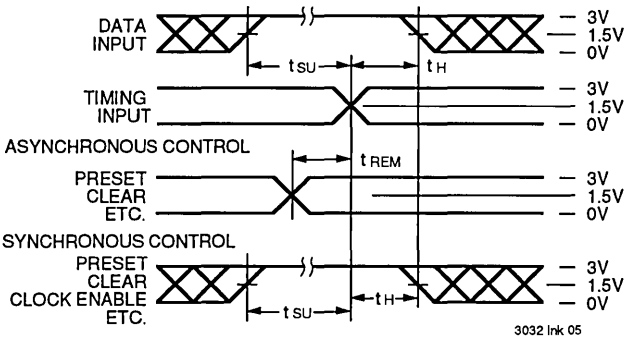
3032 tbl 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

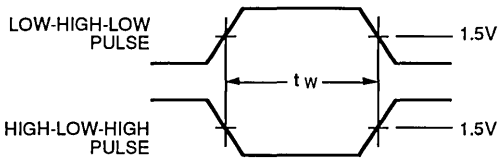
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



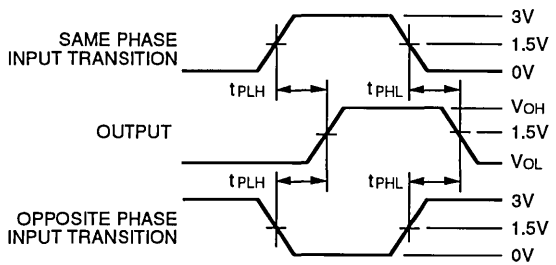
3032 lnk 05

PULSE WIDTH



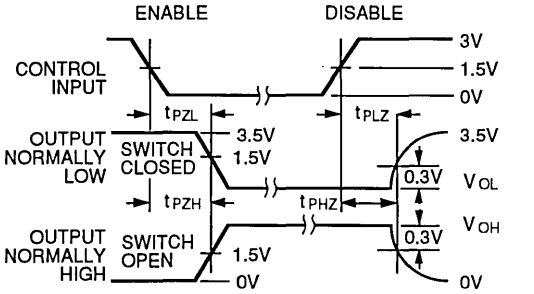
3032 lnk 06

PROPAGATION DELAY



3032 lnk 07

ENABLE AND DISABLE TIMES

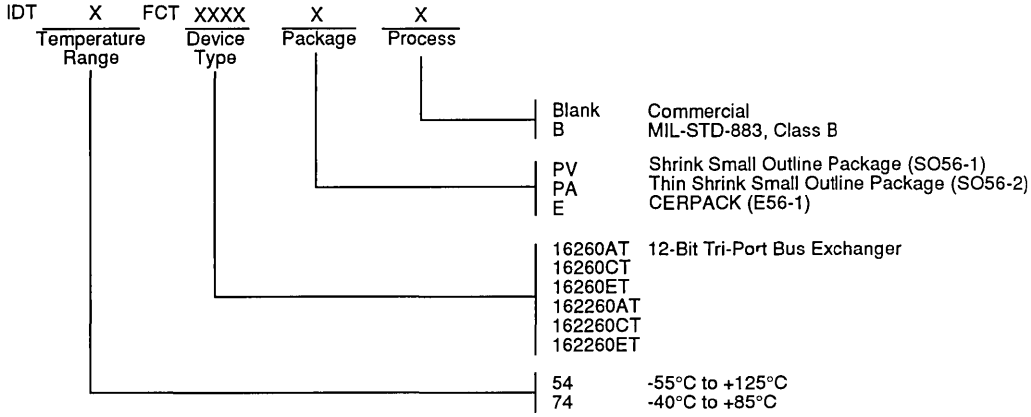


3032 lnk 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



drw 09

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

Integrated Device Technology, Inc.

FAST CMOS 16-BIT TRANSPARENT LATCHES

IDT54/74FCT16373T/AT/CT/ET
IDT54/74FCT162373T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16373T/AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162373T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

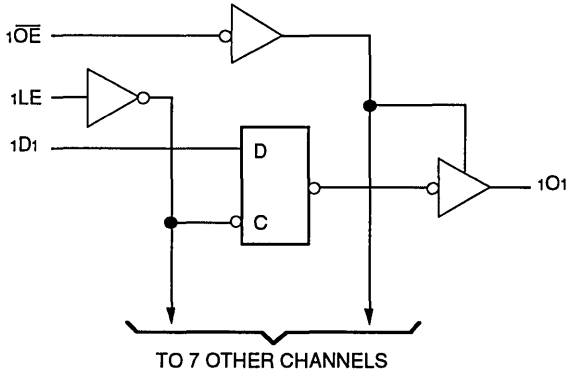
DESCRIPTION:

The IDT54/74FCT16373T/AT/CT/ET and IDT54/74FCT162373T/AT/CT/ET 16-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches, or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

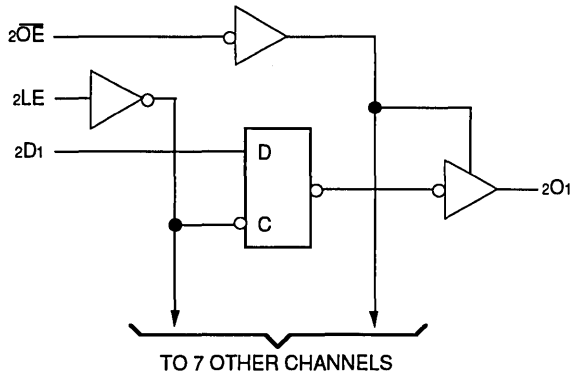
The IDT54/74FCT16373T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162373T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162373T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16373T/AT/CT/ET and 54/74ABT16373 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

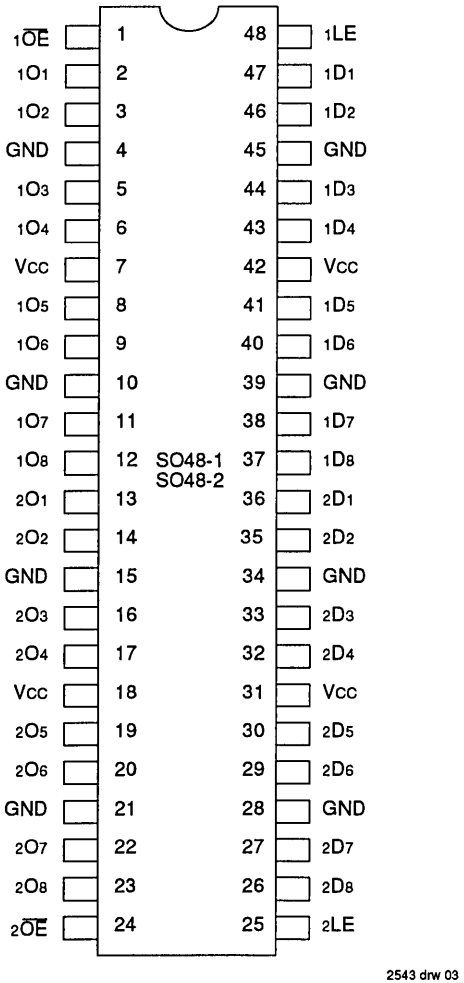


2543 drw 01



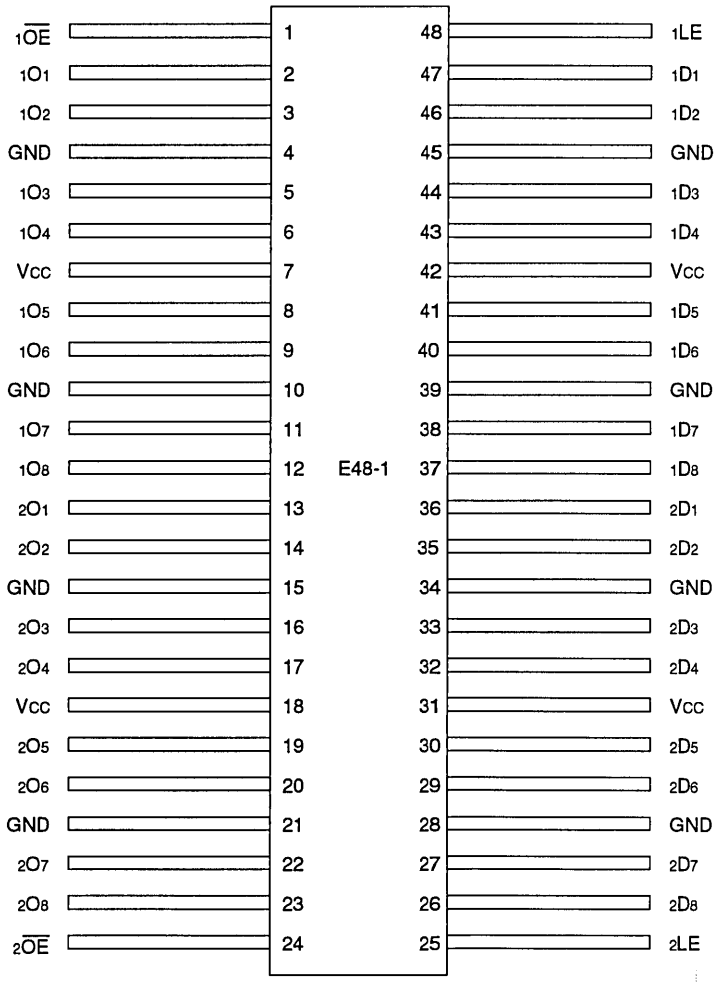
2543 drw 02

PIN CONFIGURATIONS



2543 drw 03

SSOP
TSSOP
TOP VIEW



2543 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Inputs (Active HIGH)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xOx	3-State Outputs

2543 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:
1. H = HIGH voltage level
   L = LOW voltage level
   X = Don't care
   Z = High-impedance

2543 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2543 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2543 lnk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2543 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16373T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2543 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162373T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2543 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Sixteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

2543 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16373T/162373T				FCT16373AT/162373AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	xLE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

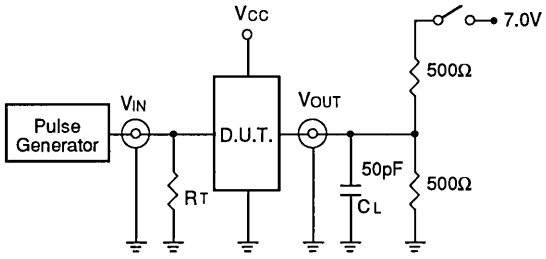
Symbol	Parameter	Condition[1]	FCT16373CT/162373CT				FCT16373ET/162373ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	4.2	1.5	5.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	5.5	2.0	8.0	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.9	1.5	3.6	—	—	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	1.0	—	—	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.0	—	—	—	ns
tW	xLE Pulse Width HIGH		5.0	—	6.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2543 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2543 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

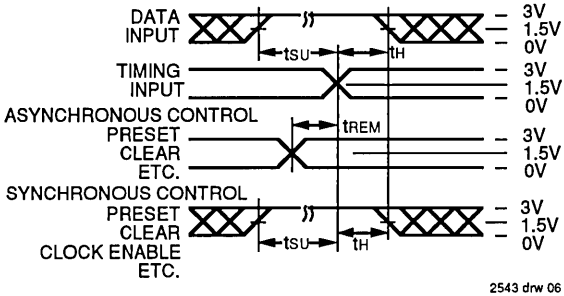
2543 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

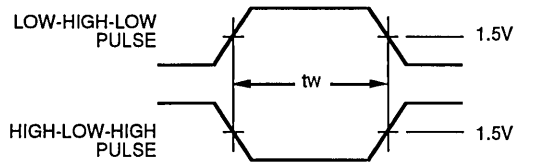
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



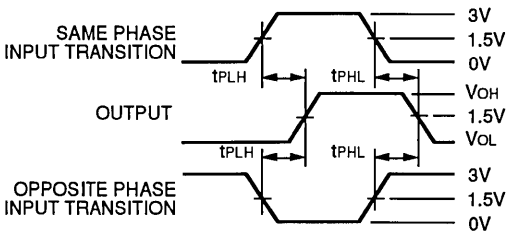
2543 drw 06

PULSE WIDTH



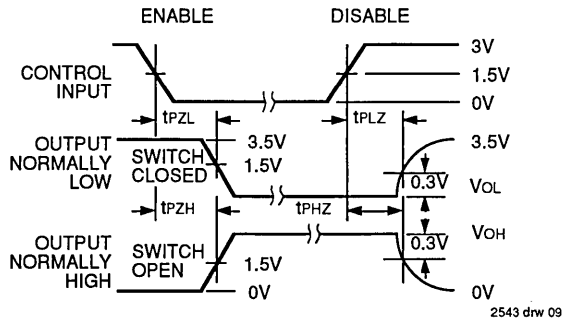
2543 drw 07

PROPAGATION DELAY



2543 drw 08

ENABLE AND DISABLE TIMES

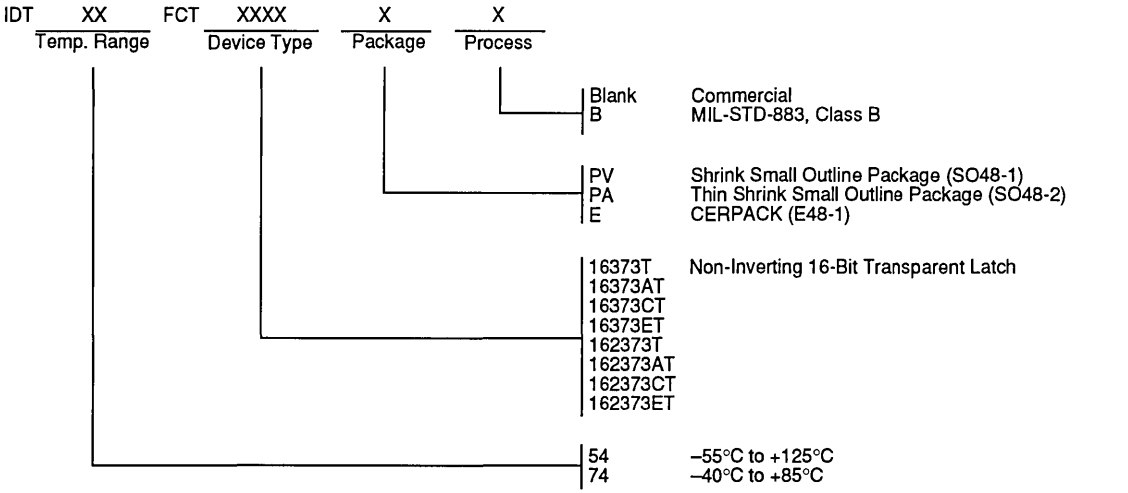


2543 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2543 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT16374T/AT/CT/ET
IDT54/74FCT162374T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16374T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162374T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

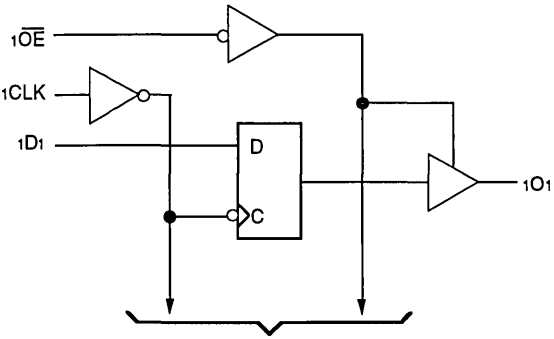
DESCRIPTION:

The IDT54/74FCT16374T/AT/CT/ET and IDT54/74FCT162374T/AT/CT/ET 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ($x\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

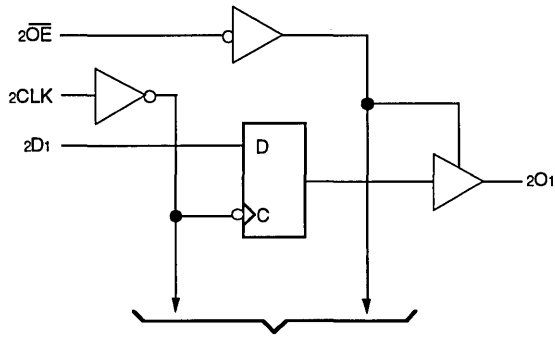
The IDT54/74FCT16374T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162374T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162374T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16374T/AT/CT/ET and 54/74ABT16374 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM

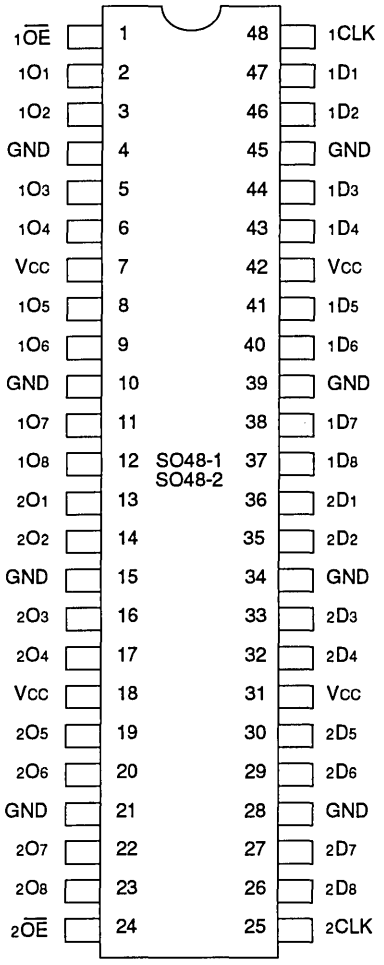


2542 drw 01



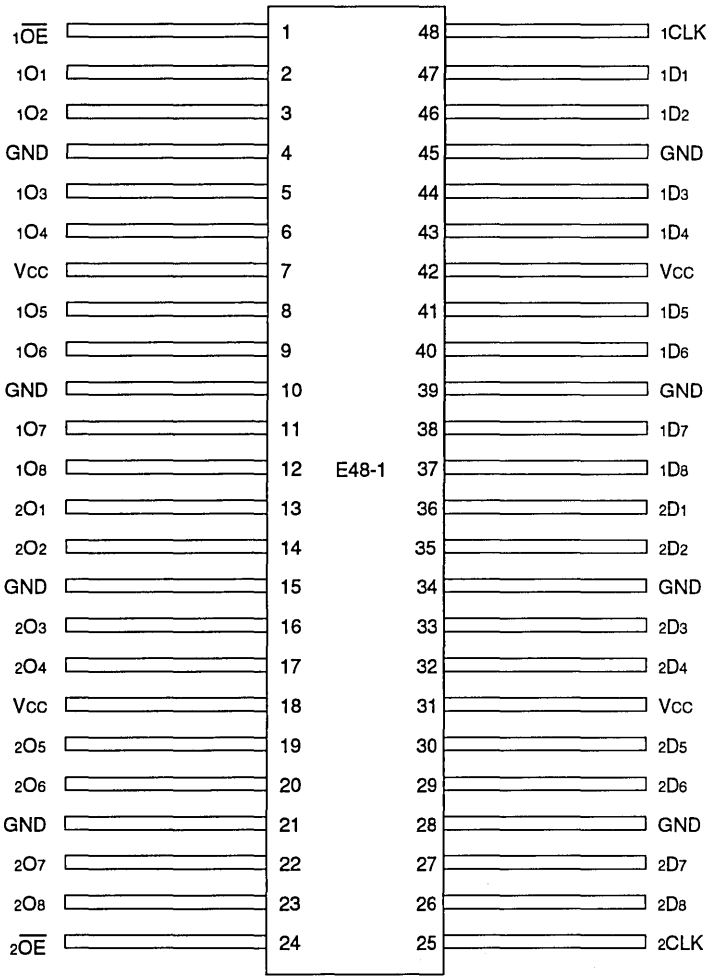
2542 drw 01

PIN CONFIGURATIONS



2542 drw 03

SSOP
TSSOP
TOP VIEW



2542 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs.
$x\overline{OE}$	3-State Output Enable Input (Active LOW)

2542 tbl 01

FUNCTION TABLE[1]

Function	Inputs			Outputs
	xDx	xCLK	$x\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE: 2542 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2542 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2542 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2542 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2542 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2542 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.1	3.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	7.5	19.0[5]	

2542 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16374T/162374T				FCT16374AT/162374AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
tPZH tPZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16374CT/162374CT				FCT16374ET/162374ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	5.2	2.0	6.2	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.7	1.5	3.6	—	—	ns
tSU	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
tW	xCLK Pulse Width HIGH or LOW		5.0	—	6.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

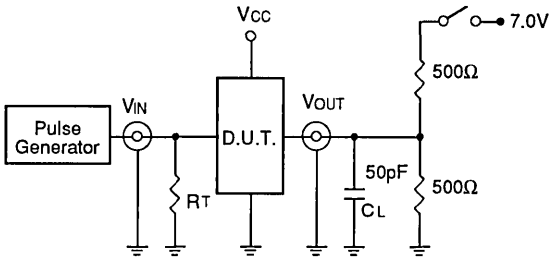
NOTES:

2542 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2542 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

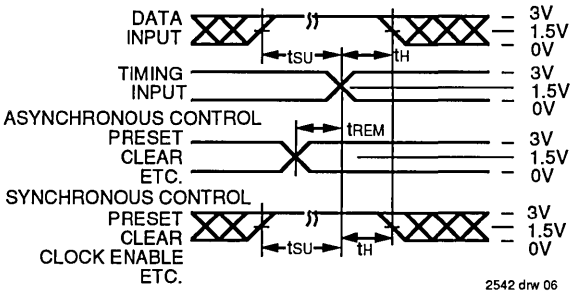
2542 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

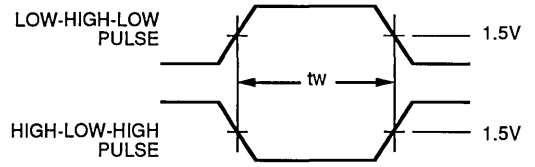
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



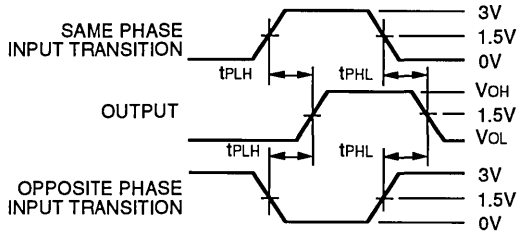
2542 drw 06

PULSE WIDTH



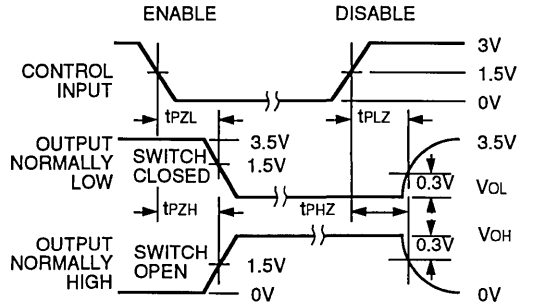
2542 drw 07

PROPAGATION DELAY



2542 drw 08

ENABLE AND DISABLE TIMES

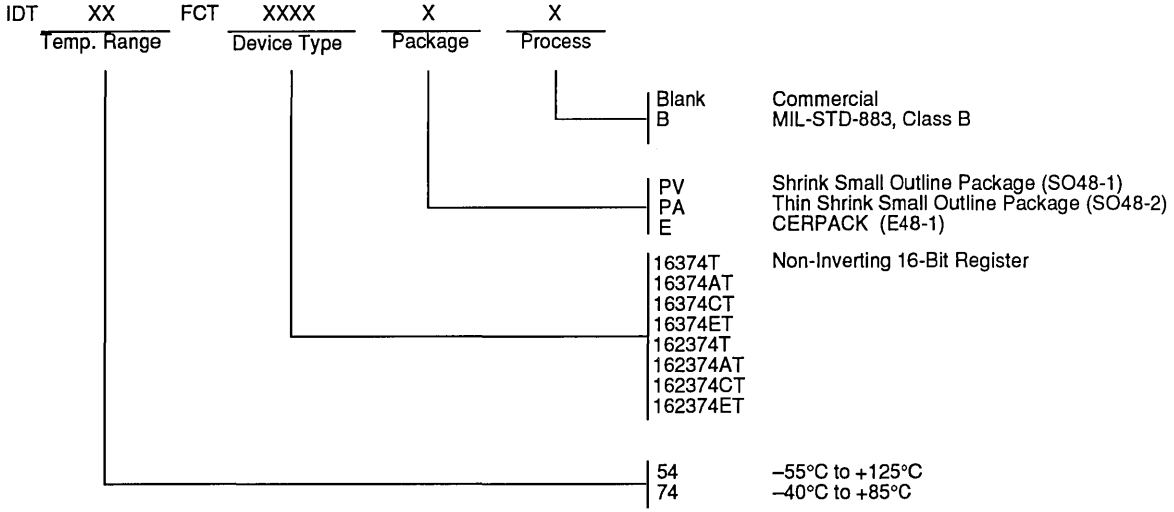


2542 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2542 drw 10

Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16500AT/CT/ET
IDT54/74FCT162500AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16500AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162500AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

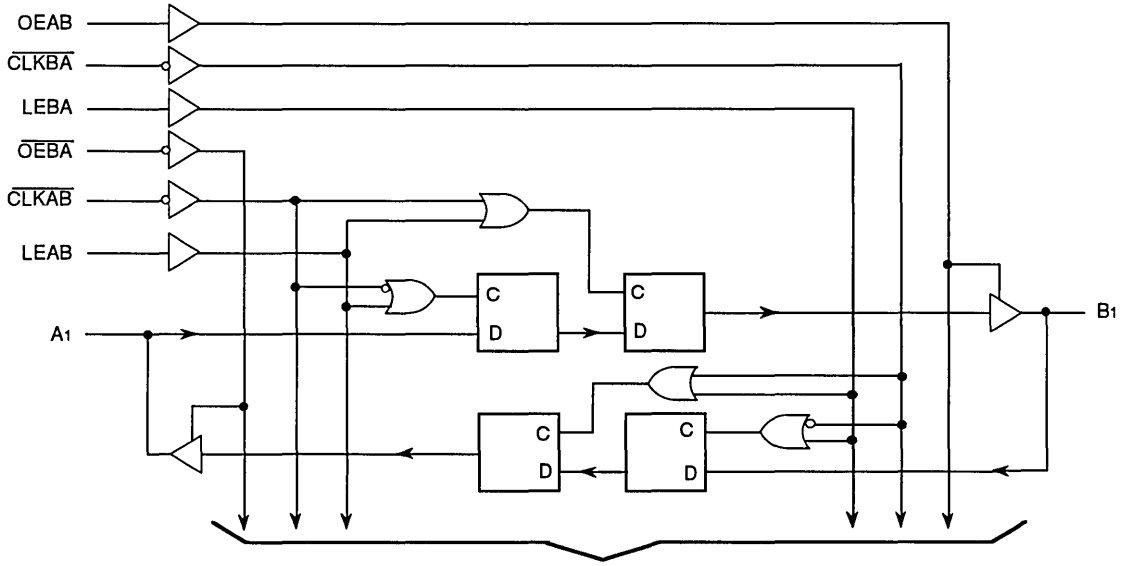
DESCRIPTION:

The IDT54/74FCT16500AT/CT/ET and IDT54/74FCT162500AT/CT/ET 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but uses $\overline{OEBA}$, LEBA and $\overline{CLKBA}$. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16500AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

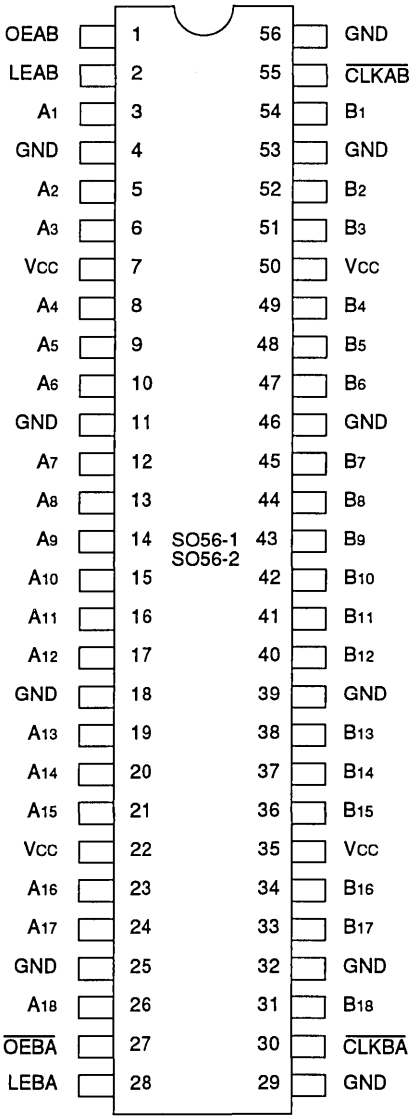
The IDT54/74FCT162500AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162500AT/CT/ET are plug-in replacements for the IDT54/74FCT16500AT/CT/ET and 54/74ABT16500 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



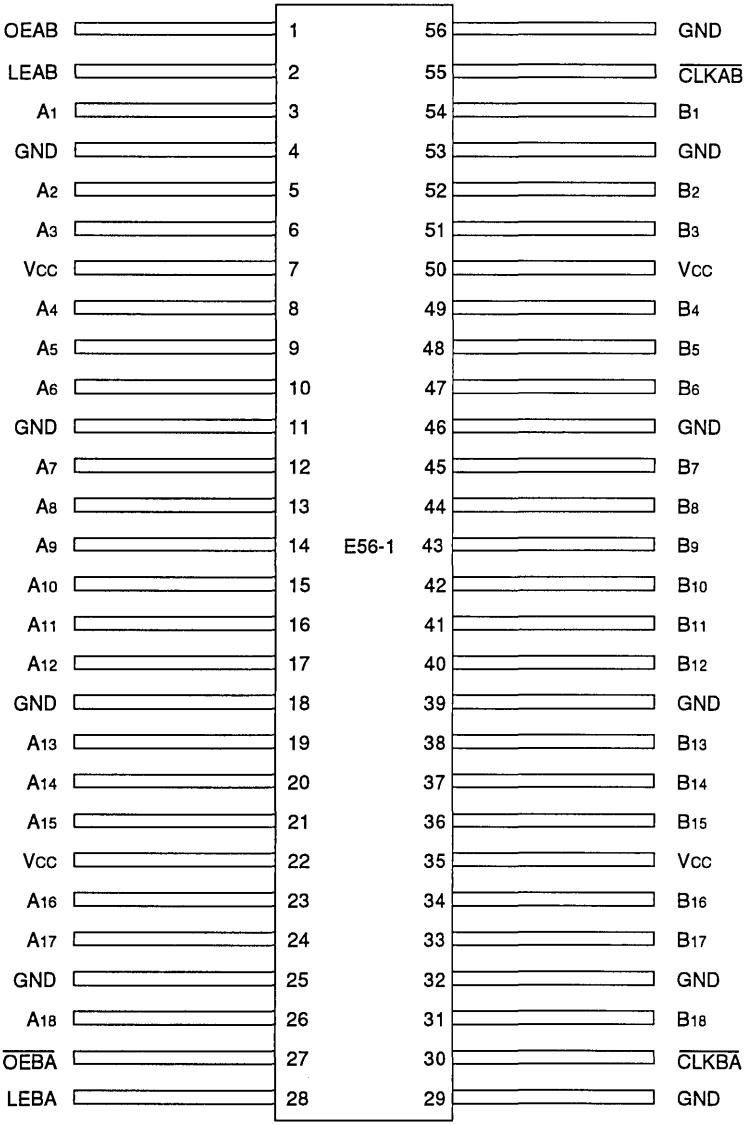
2548 drw 01

PIN CONFIGURATIONS



2548 drw 02

SSOP
TSSOP
TOP VIEW



2548 drw 03

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2548 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B[2]
H	L	L	X	B[3]

2548 tbl 02

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↓ = HIGH-to-LOW Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2548 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2548 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2548 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16500T

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2548 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162500T

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2548 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.5	20.8[5]	

2548 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT16500AT/162500AT				FCT16500CT/162500CT				FCT16500ET/162500ET				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency[3]		C_L = 50pF	—	150	—	150	—	150	—	150	—	150	—	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax		R_L = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	—	3.8	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	—	4.2	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLKBA}$ to Ax, $\overline{CLKAB}$ to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	—	4.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	—	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	—	4.0	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW Ax to $\overline{CLKAB}$, Bx to $\overline{CLKBA}$			3.0	—	3.0	—	3.0	—	3.0	—	2.4	—	—	—	ns
t_H	Hold Time, HIGH or LOW Ax to $\overline{CLKAB}$, Bx to $\overline{CLKBA}$			0	—	0	—	0	—	0	—	0	—	—	—	ns
t_{SU}	Set-up Time HIGH or LOW	Clock HIGH		3.0	—	3.0	—	3.0	—	3.0	—	2.0	—	—	—	ns
	Ax to LEAB, Bx to LEBA	Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
t_W	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

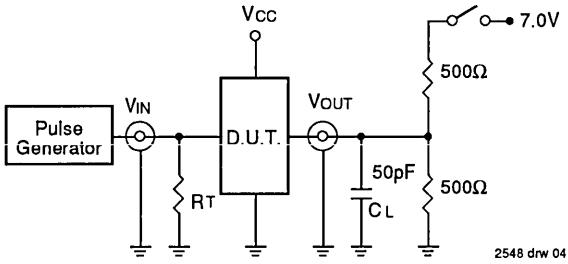
NOTES:

2548 tbl 09

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2548 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

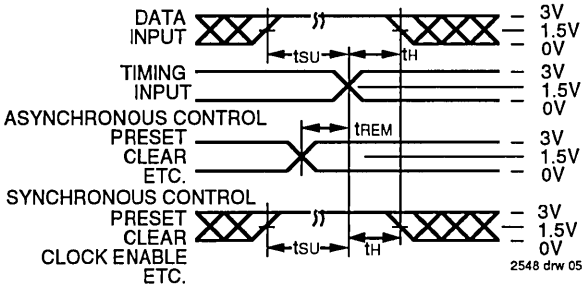
2548 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

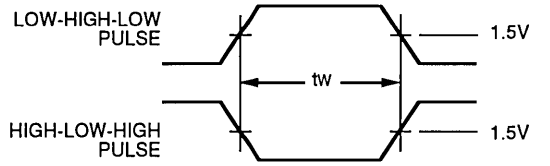
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



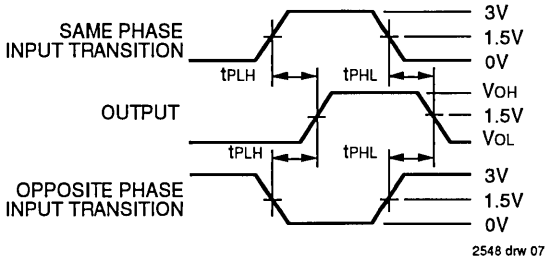
2548 drw 05

PULSE WIDTH



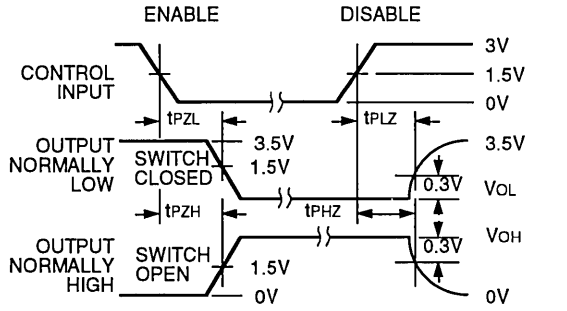
2548 drw 06

PROPAGATION DELAY



2548 drw 07

ENABLE AND DISABLE TIMES

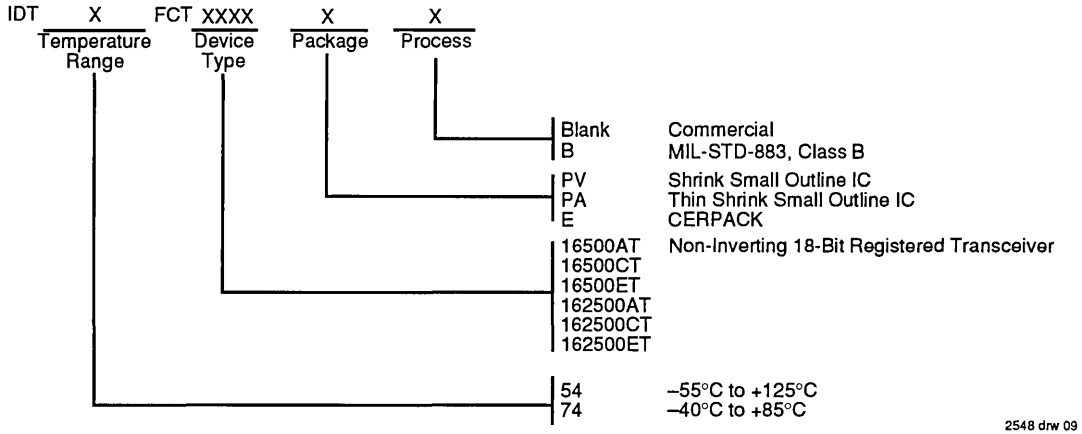


2548 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16501AT/CT/ET
IDT54/74FCT162501AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16501AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162501AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

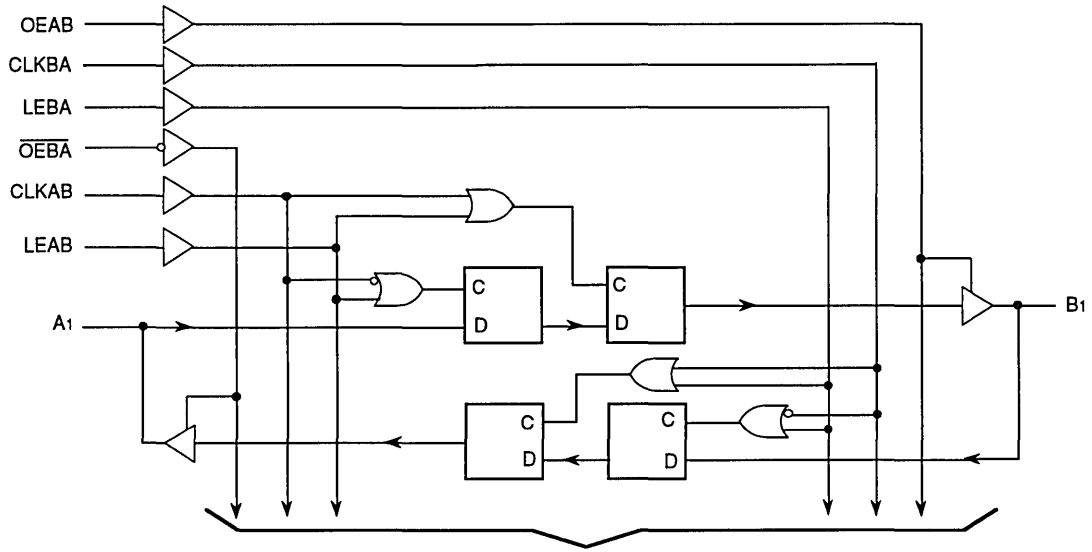
DESCRIPTION:

The IDT54/74FCT16501AT/CT/ET and IDT54/74FCT162501AT/CT/ET 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from the B port to the A port is similar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16501AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

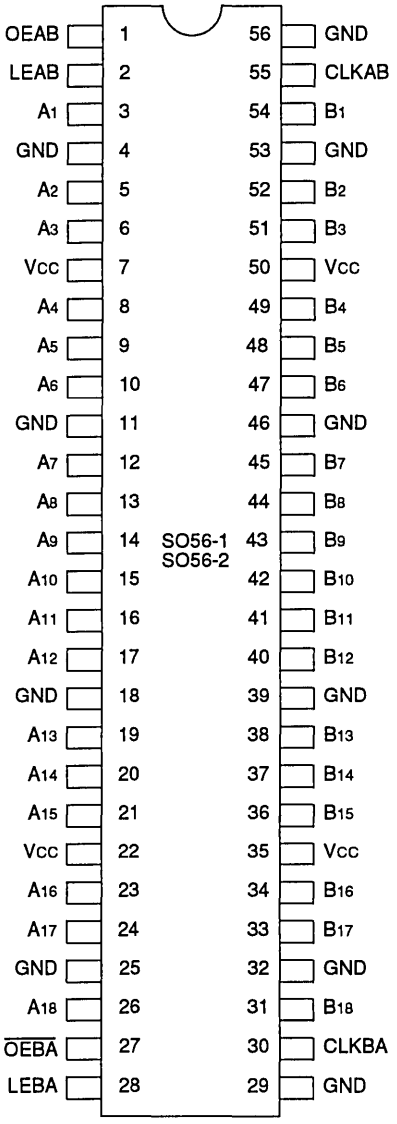
The IDT54/74FCT162501AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162501AT/CT/ET are plug-in replacements for the IDT54/74FCT16501AT/CT/ET and 54/74ABT16501 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



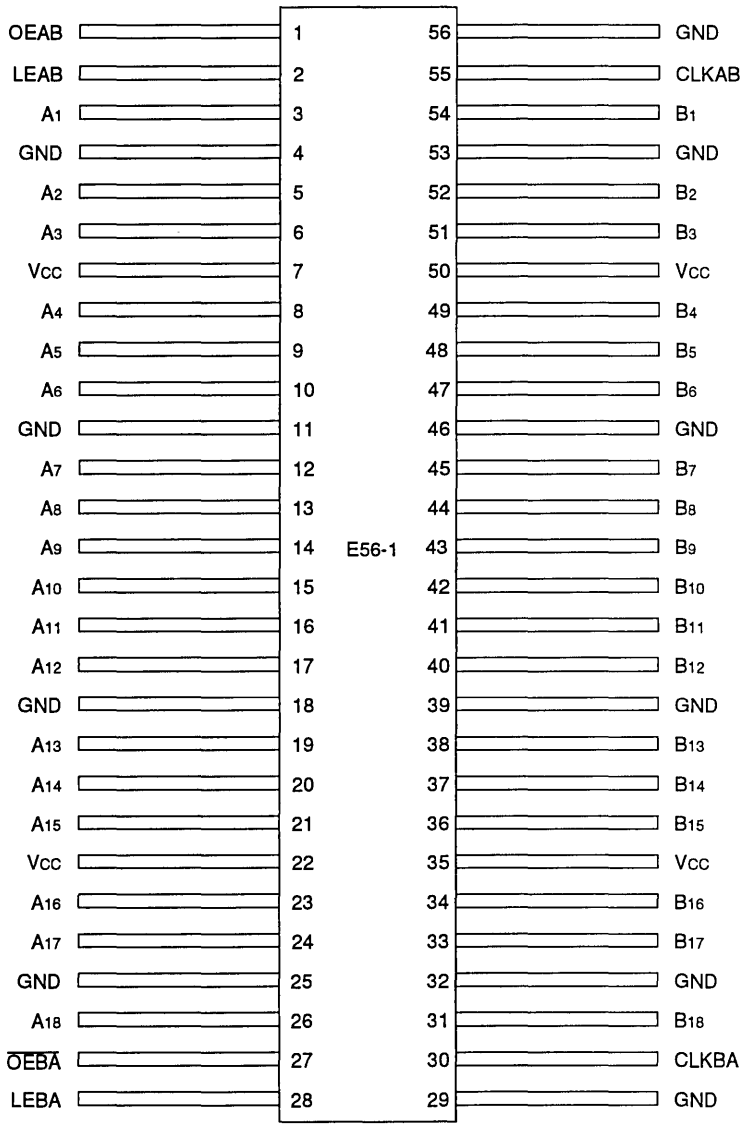
2547 drw 01

PIN CONFIGURATIONS



2547 drw 02

SSOP
TSSOP
TOP VIEW



2547 drw 03

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2547 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[2]
H	L	H	X	B[3]

NOTES: 2547 tbl 02

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2547 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2547 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2547 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16501T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2547 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162501T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2547 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.5	20.8[5]	

2547 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT16501AT/162501AT				FCT16501CT/162501CT				FCT16501ET/162501ET				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
fMAX	CLKAB or CLKBA frequency[3]		CL = 50pF	—	150	—	150	—	150	—	150	—	150	—	—	MHz
tPLH tPHL	Propagation Delay Ax to Bx or Bx to Ax		RL = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	1.5	4.2	—	—	ns
tPLH tPHL	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	1.5	4.2	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	1.5	4.0	—	—	ns
tSU	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			3.0	—	3.0	—	3.0	—	3.0	—	2.4	—	—	—	ns
tH	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	0	—	—	—	ns
tSU	Set-up Time HIGH or LOW	Clock LOW		3.0	—	3.0	—	3.0	—	3.0	—	2.0	—	—	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns
tW	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
tW	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
tSK(o)	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

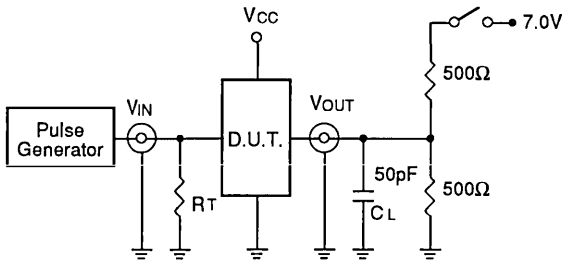
NOTES:

2547 tbl 09

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2547 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

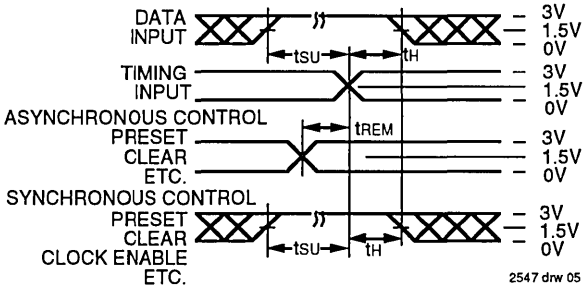
2547 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

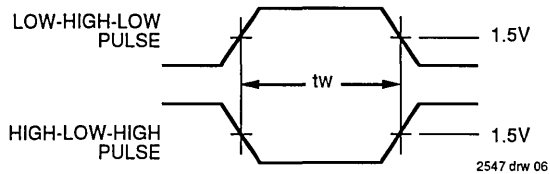
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



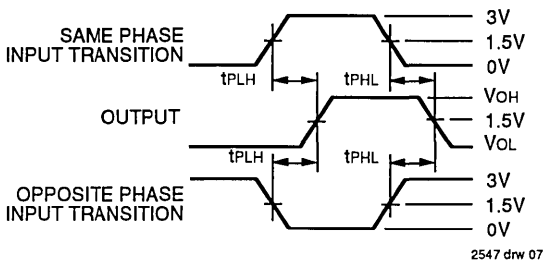
2547 drw 05

PULSE WIDTH



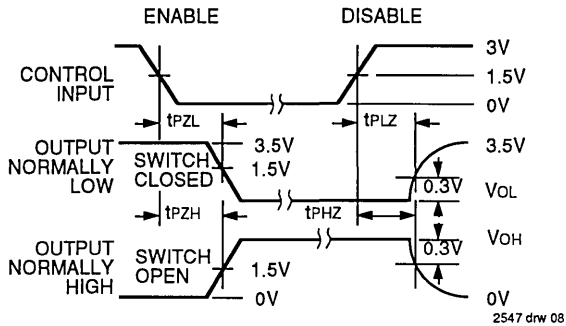
2547 drw 06

PROPAGATION DELAY



2547 drw 07

ENABLE AND DISABLE TIMES

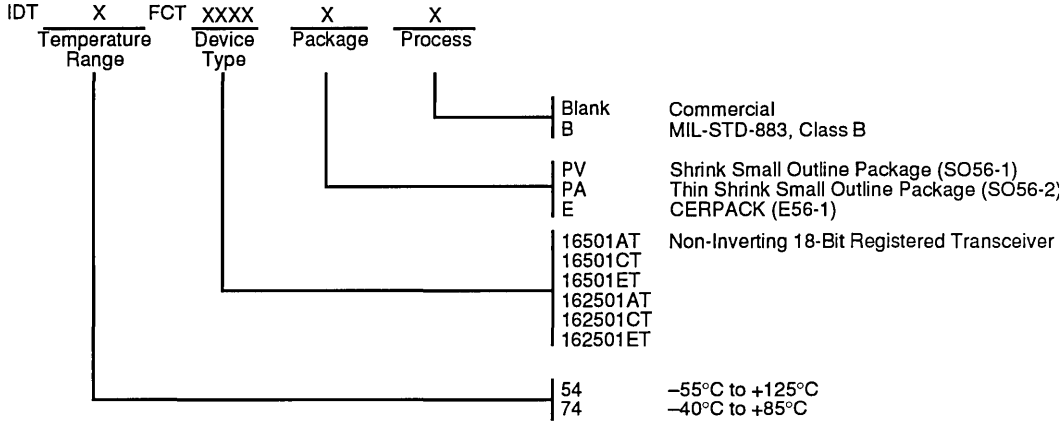


2547 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2547 drw 09

Integrated Device Technology, Inc.

FAST CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT16543T/AT/CT/ET
IDT54/74FCT162543T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16543T/AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162543T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

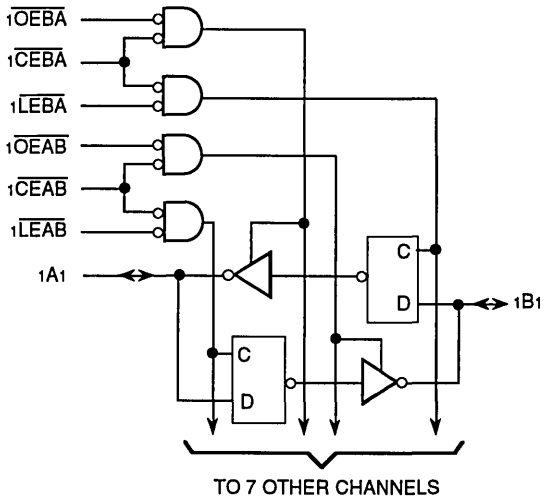
DESCRIPTION:

The IDT54/74FCT16543T/AT/CT/ET and IDT54/74FCT162543T/AT/CT/ET 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW in order to enter data from the A port or to output data from the B port. $x\overline{LEAB}$ controls the latch function. When $x\overline{LEAB}$ is LOW, the latches are transparent. A subsequent LOW-to-HIGH transition of $x\overline{LEAB}$ signal puts the A latches in the storage mode. $x\overline{OEAB}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $x\overline{CEBA}$, $x\overline{LEBA}$, and $x\overline{OEBA}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

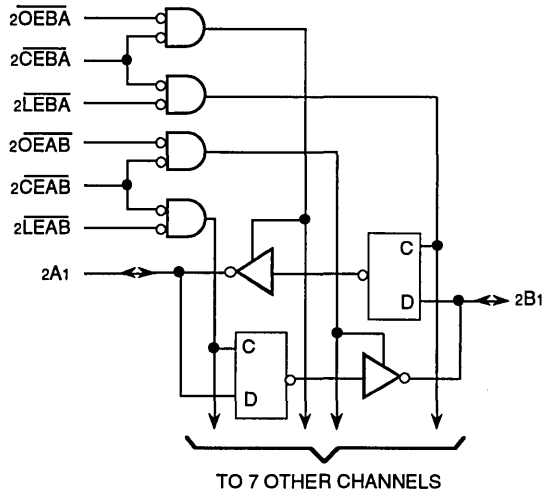
The IDT54/74FCT16543T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162543T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162543T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16543T/AT/CT/ET and 54/74ABT16543 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM

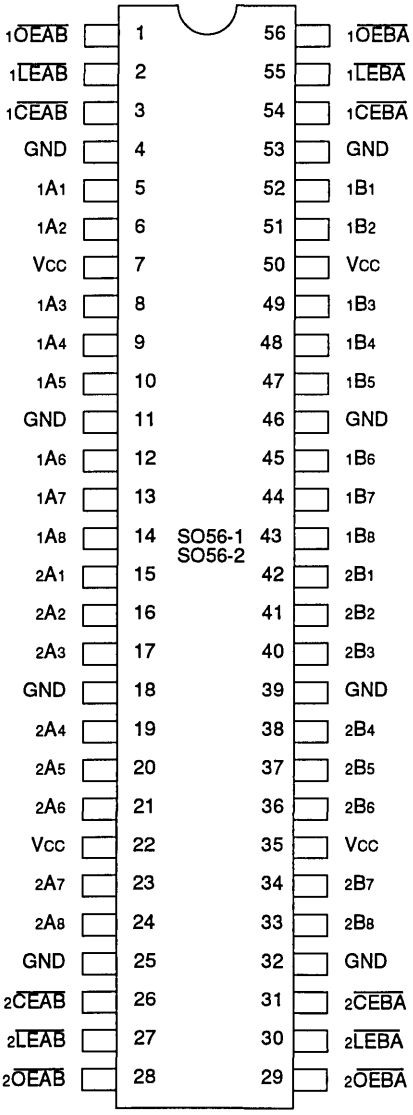


2618 drw 01



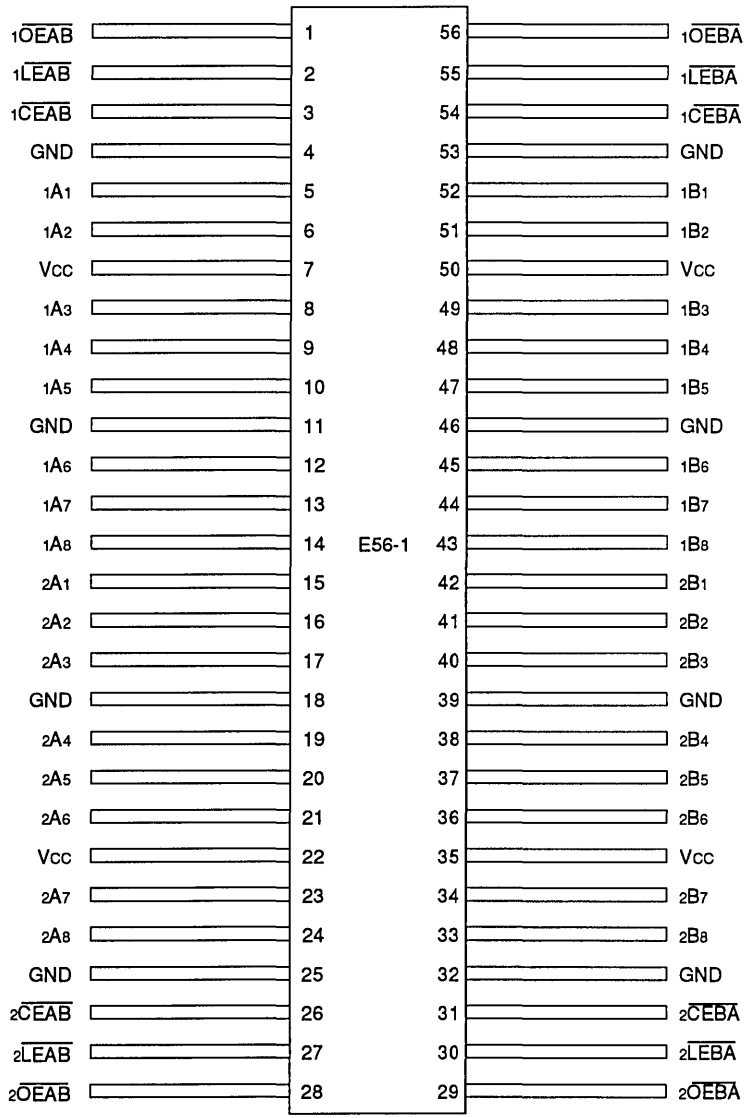
2618 drw 02

PIN CONFIGURATIONS



2618 drw 03

SSOP
TSSOP
TOP VIEW



2618 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$x\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$x\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

2618 tbl 01

FUNCTION TABLE[1, 2]

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$x\overline{CEAB}$	$x\overline{LEAB}$	$x\overline{OEAB}$	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES: 2618 tbl 02

1. * Before $x\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown; B-to-A flow control is the same, except using $x\overline{CEBA}$, $x\overline{LEBA}$ and $x\overline{OEBA}$.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2618 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2618 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2618 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2618 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2618 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = Vcc One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = Vcc Sixteen Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

NOTES:

2618 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16543T/162543T				FCT16543AT/162543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2618 tbl 09

Symbol	Parameter	Condition[1]	FCT16543CT/162543CT				FCT16543ET/162543ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		1.5	7.0	1.5	8.0	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	8.0	1.5	9.0	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	6.5	1.5	7.5	1.5	4.0	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.0	—	—	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.0	—	—	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

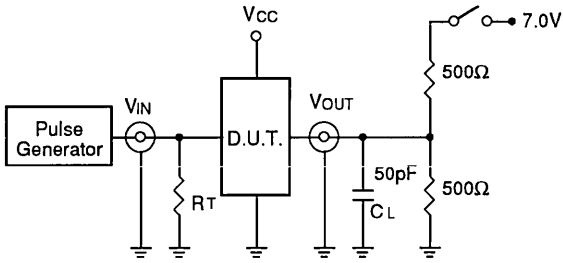
NOTES:

2618 tbl 10

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2618 drw 05

SWITCH POSITION

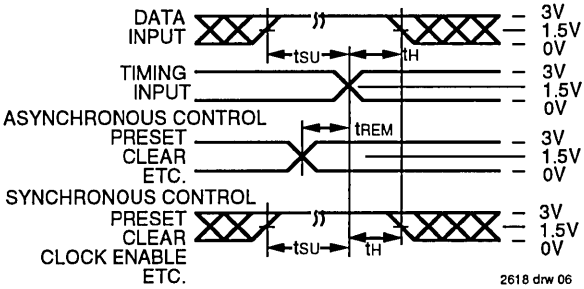
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 2618 lnk 10

C_L = Load capacitance: includes jig and probe capacitance.

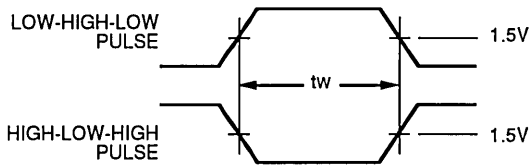
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



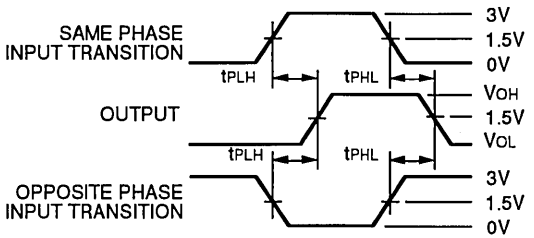
2618 drw 06

PULSE WIDTH



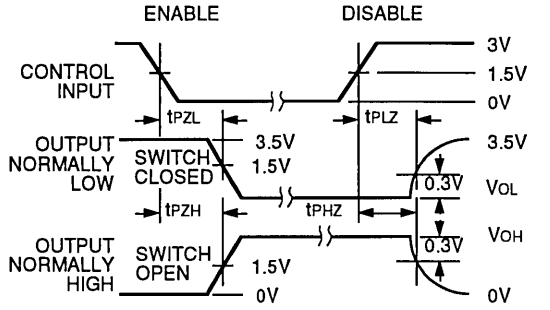
2618 drw 07

PROPAGATION DELAY



2618 drw 08

ENABLE AND DISABLE TIMES

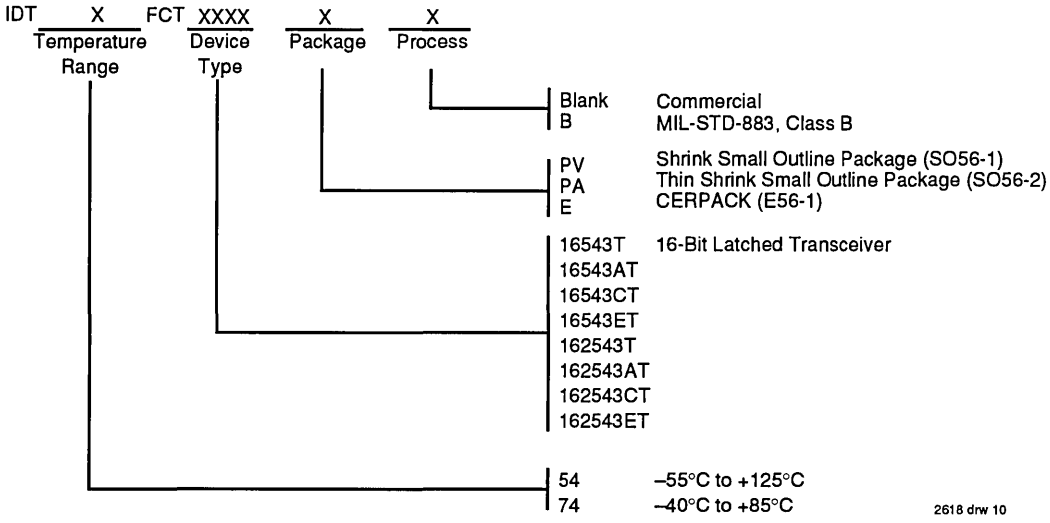


2618 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT16646T/AT/CT/ET
IDT54/74FCT162646T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16646T/AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162646T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

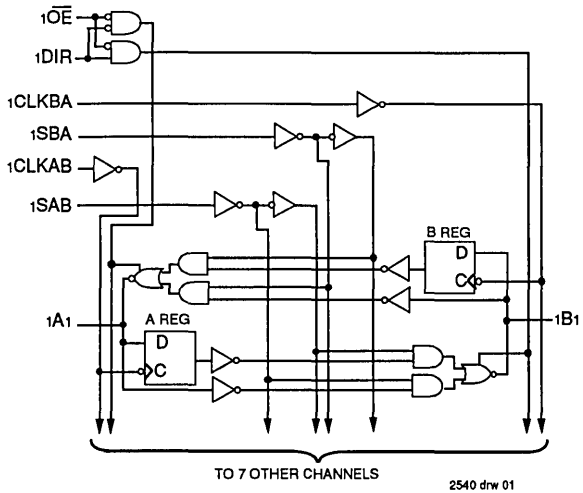
DESCRIPTION:

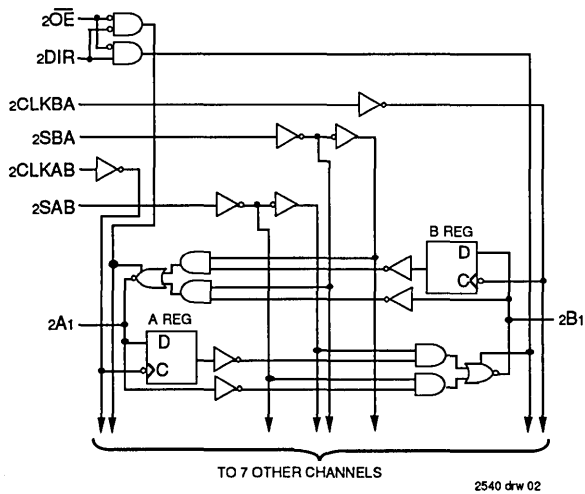
The IDT54/74FCT16646T/AT/CT/ET and IDT54/74FCT162646T/AT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control ($x\overline{OE}$) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16646T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

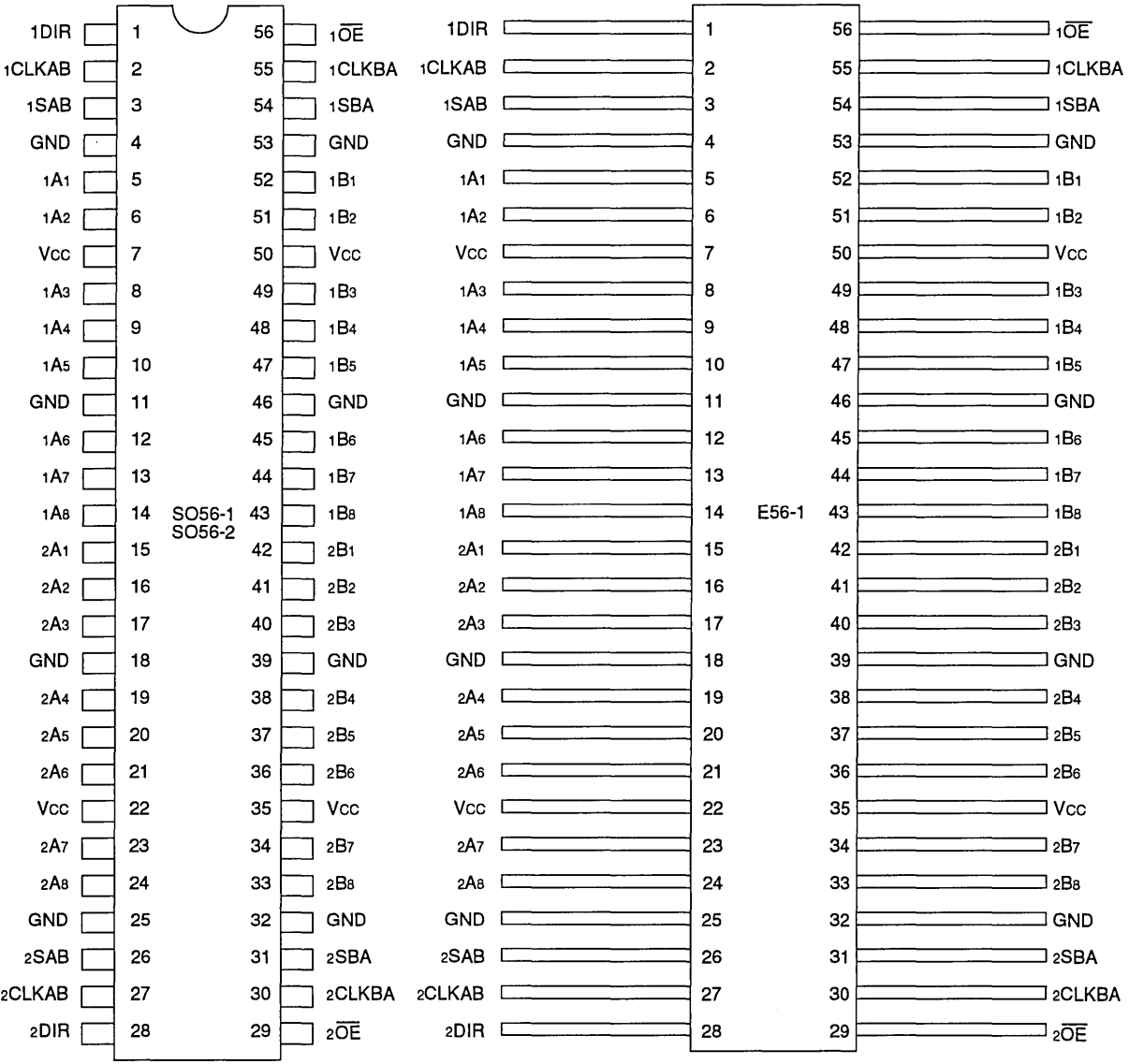
The IDT54/74FCT162646T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162646T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16646T/AT/CT/ET and 54/74ABT16646 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATIONS



2540 drw 03

SSOP
TSSOP
TOP VIEW

2540 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
$x\overline{DIR}$, $x\overline{OE}$	Output Enable Inputs

2540 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2540 tbl 02

FUNCTION TABLE[2]

Inputs						Data I/O[1]		Operation or Function
$x\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the $x\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

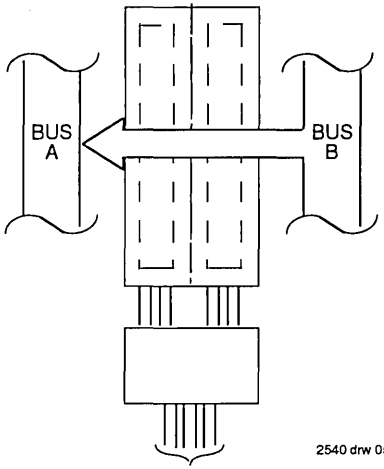
2634 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

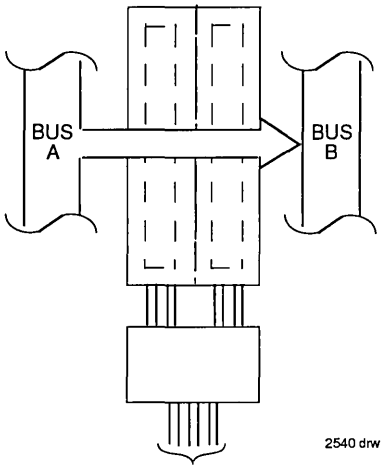
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

2540 tbl 04



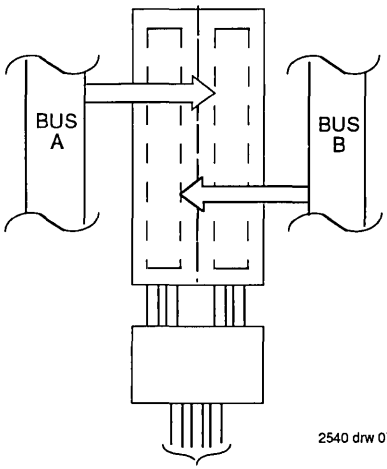
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



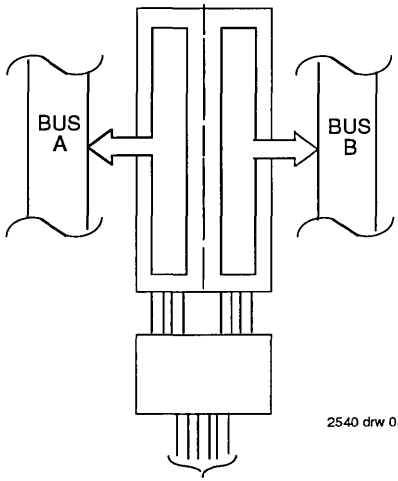
xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xDIR (1)	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2540 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16646T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2540 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162646T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2540 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = $\overline{xOE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $\overline{xOE}$ = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $\overline{xOE}$ = GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2540 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16646T/162646T				FCT16646AT/162646AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2540 tbl 09

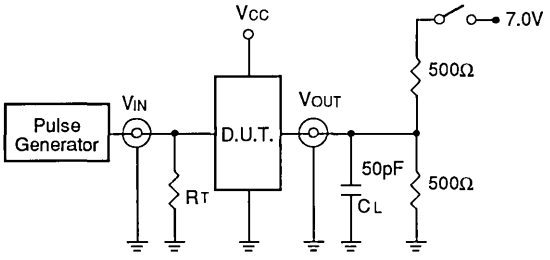
			FCT16646CT/162646CT				FCT16646ET/162646ET				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]		—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2540 tbl10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

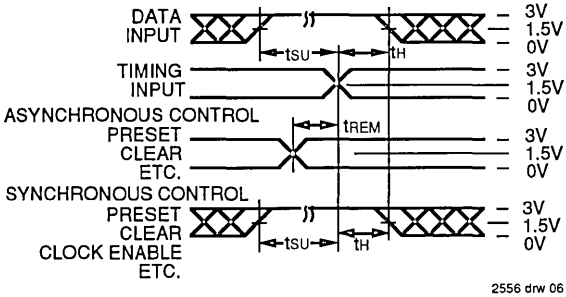
2556 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

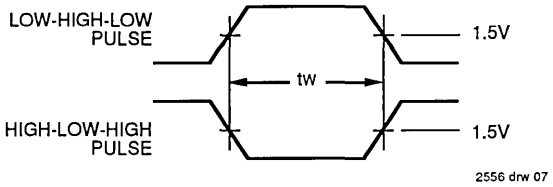
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



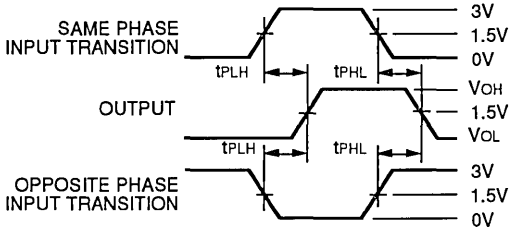
2556 drw 06

PULSE WIDTH



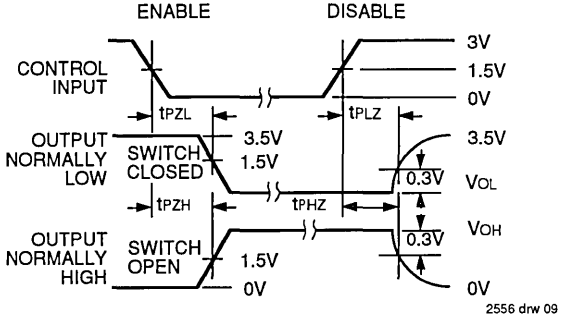
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

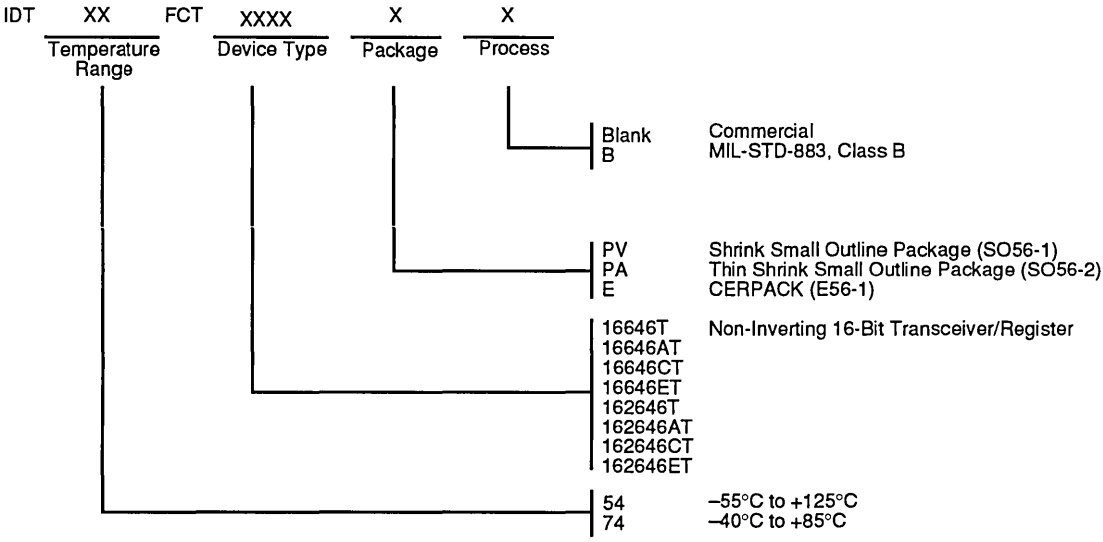


2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2540 drw 14

Integrated Device Technology, Inc.

FAST CMOS 16-BIT INVERTING BUS TRANSCEIVER/REGISTER

IDT54/74FCT16651T/AT/CT/ET

FEATURES:

- 0.5 MICRON CMOS Technology
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤ 1μA max.**
- High drive outputs (–32mA I_{OH}, 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of –40°C to +85°C V_{CC} = 5V ±10%

DESCRIPTION:

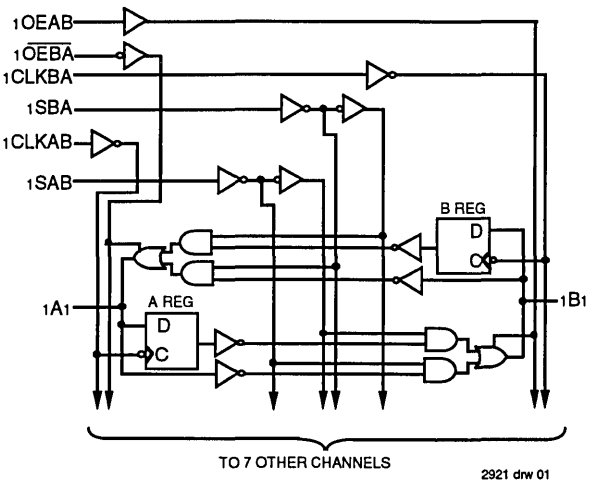
The IDT54/74FCT16651T/AT/CT/ET 16-bit inverting registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit inverting bus transceivers with 3-state D-type registers. For example, the xOEAB and $x\overline{OEBA}$ signals control the transceiver functions. The xSAB and xSBA control pins select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

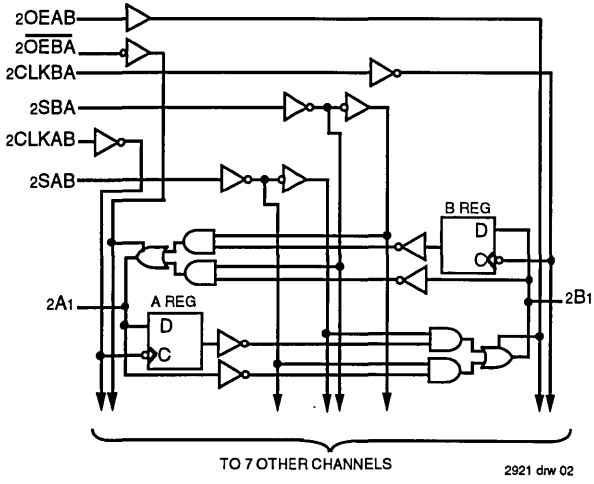
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16651T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

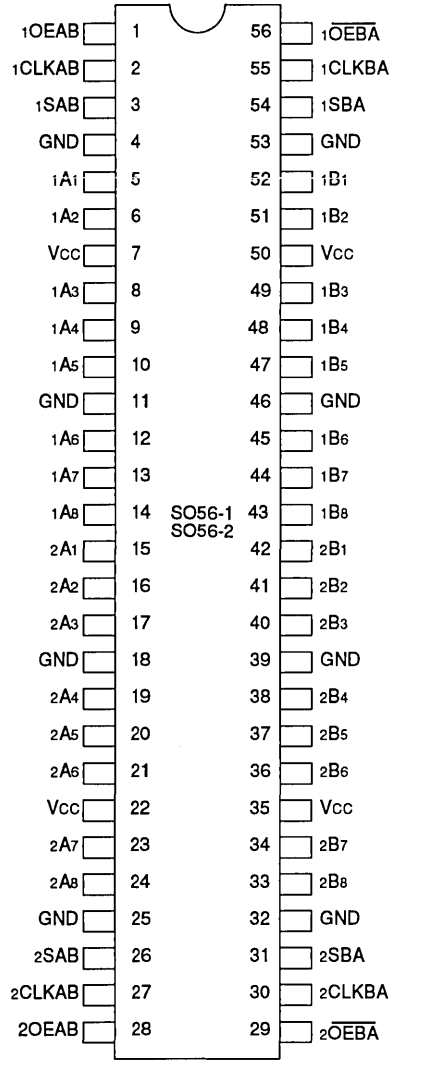
The IDT54/74FCT16651T/AT/CT/ET are plug-in replacements for the 54/74ABT16651 in bus and backplane interface applications.

FUNCTIONAL BLOCK DIAGRAM



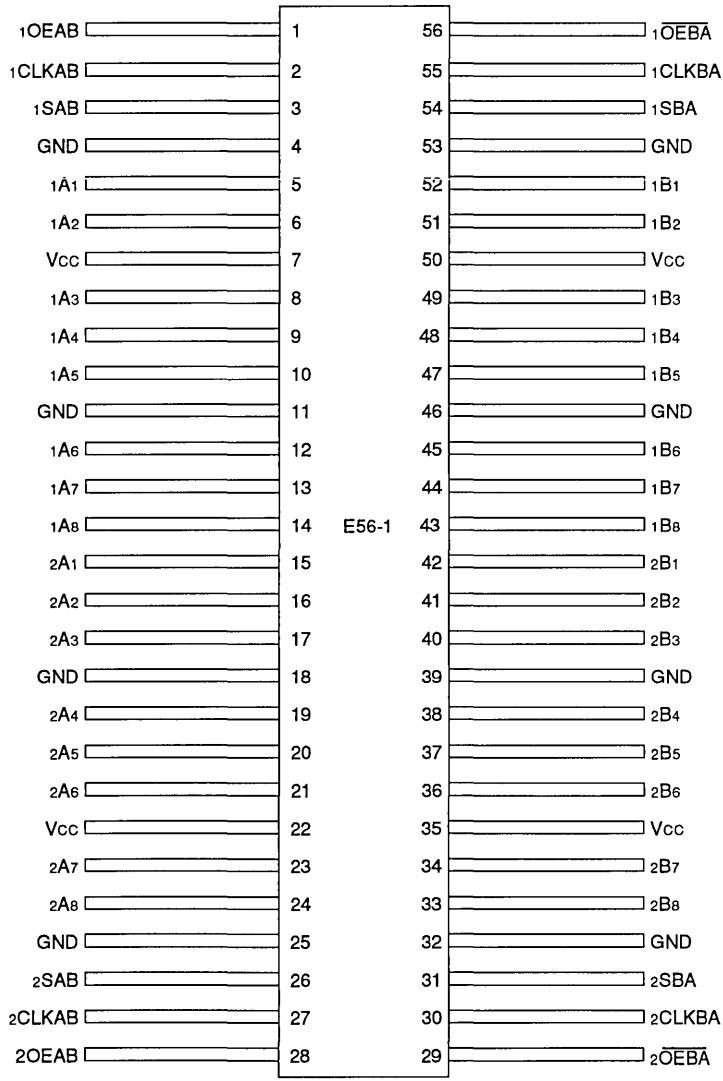


PIN CONFIGURATIONS



2921 drw 03

**SSOP
TSSOP
TOP VIEW**



2921 drw 04

**CERPACK
TOP VIEW**

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, $x\overline{OEBA}$	Output Enable Inputs

2921 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2921 lnk 02
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(3)

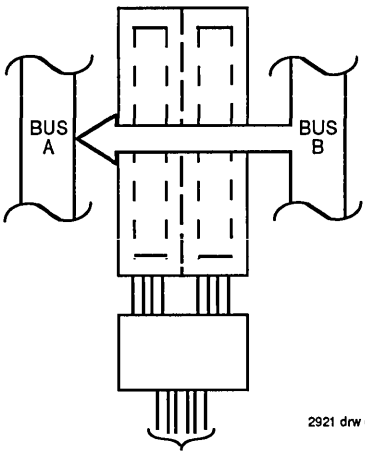
Inputs						Data I/O(1)		Operation or Function
xOEAB	$x\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified(1)	Store A, Hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in Both Registers(4)
L	X	H or L	↑	X	X	Unspecified(1)	Input	Hold A, Store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in both Registers(5)
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and
								Stored $\overline{B}$ Data to A Bus

NOTES: 2921 tbl 03
1. The data output functions may be enabled or disabled by various signals at the xOEAB or $x\overline{OEBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L, clocks can occur simultaneously.
   Select control = H, clocks must be staggered in order to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
4. $\overline{A}$ in B register
5. $\overline{B}$ in A register

ABSOLUTE MAXIMUM RATINGS(1)

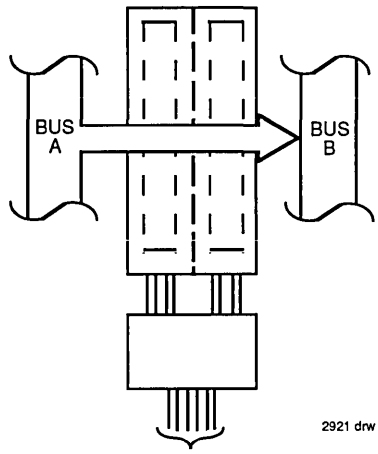
Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2921 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



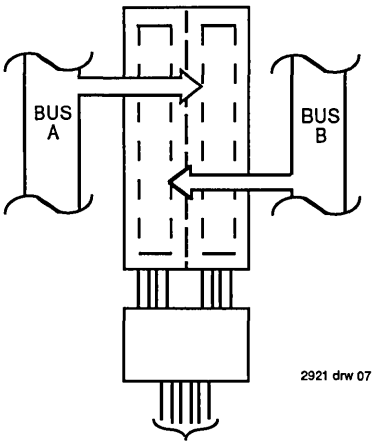
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



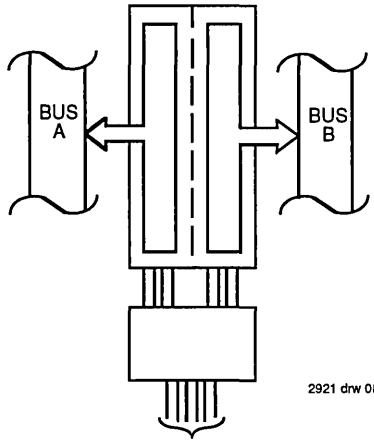
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, Vcc = 5.0V ± 10%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	Vcc = Max.	V_I = Vcc	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	Vcc = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc		—	5	500	µA

2921 lnk 05

DC OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	Vcc = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2921 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = $x\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.8	1.7	mA
		xOEAB = $x\overline{OEBA}$=GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	3.8	6.5[5]	
		xOEAB = $x\overline{OEBA}$=GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2921 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16651T				FCT16651AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time, HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2921 tbl 08

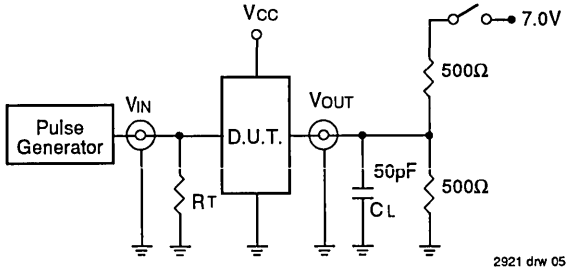
Symbol	Parameter	Condition[1]	FCT16651CT				FCT16651ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time, HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2921 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2921 drw 05

SWITCH POSITION

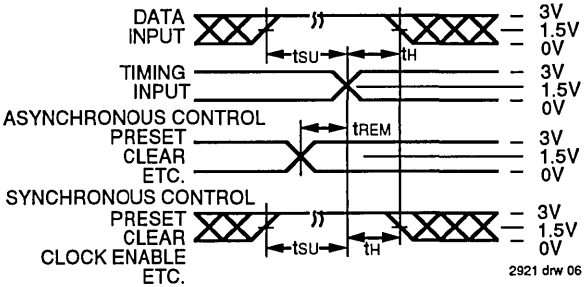
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2921 lnk 09

DEFINITIONS:

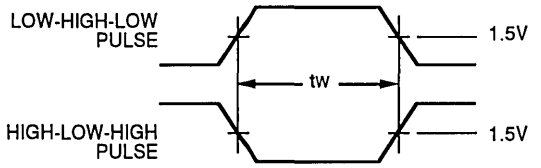
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



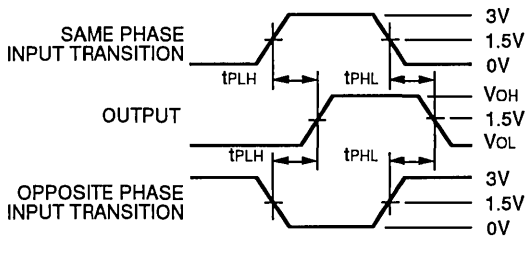
2921 drw 06

PULSE WIDTH



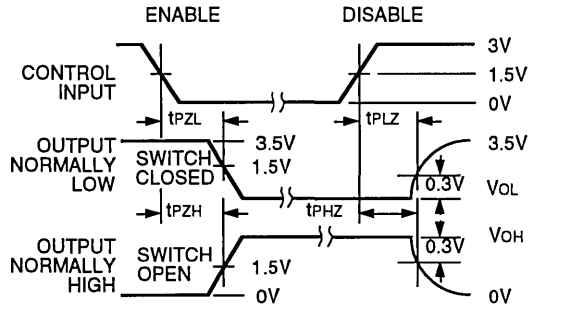
2921 drw 07

PROPAGATION DELAY



2921 drw 08

ENABLE AND DISABLE TIMES

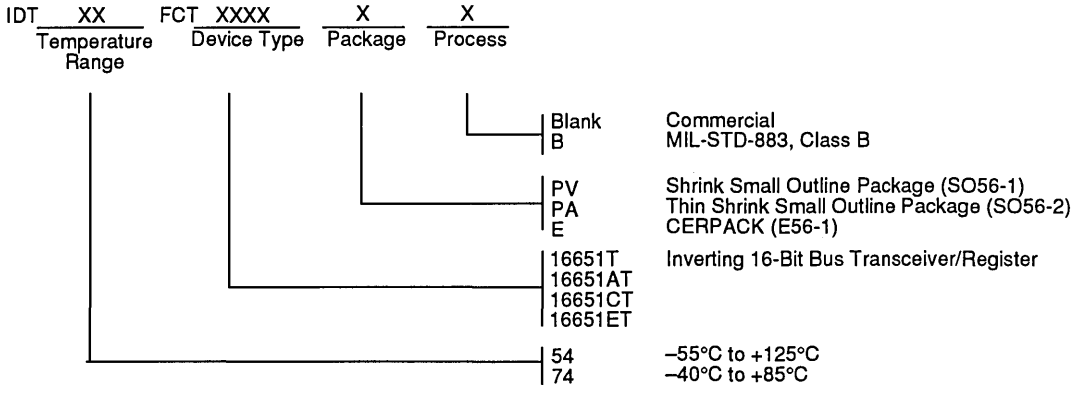


2921 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2921 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTER

IDT54/74FCT16652T/AT/CT/ET
IDT54/74FCT162652T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16652T/AT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162652T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

The IDT54/74FCT16652T/AT/CT/ET and IDT54/74FCT162652T/AT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the xOEAB and $x\overline{OEBA}$ signals control the transceiver functions.

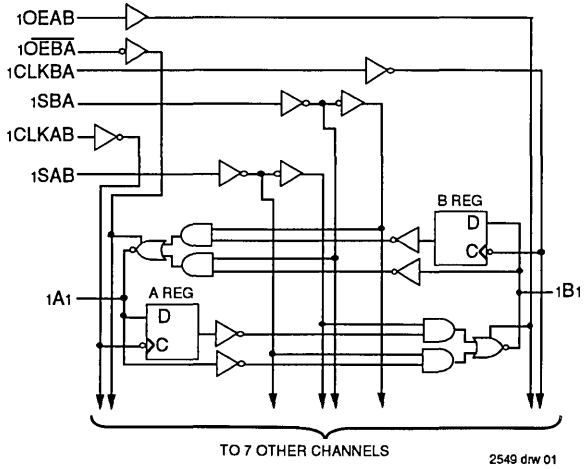
The xSAB and xSBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

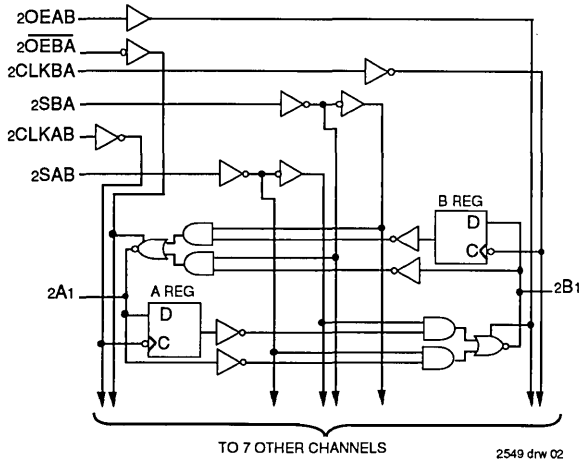
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16652T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

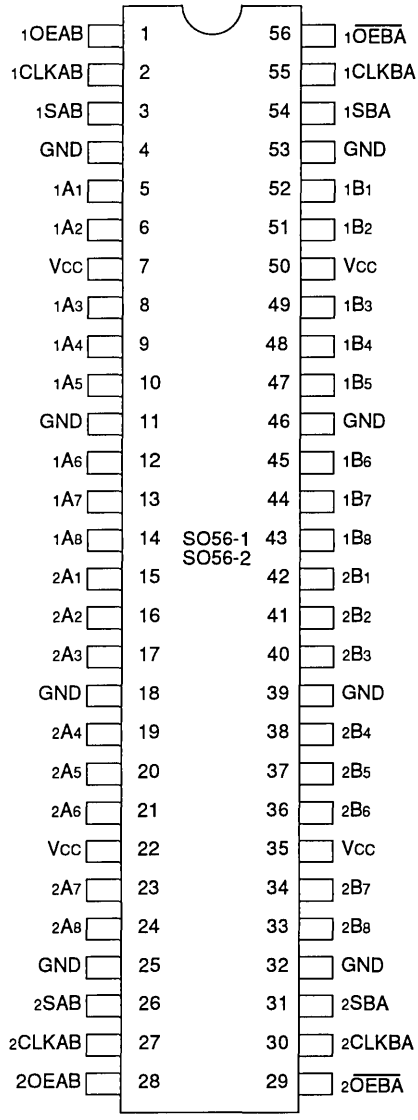
The IDT54/74FCT162652T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162652T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16652T/AT/CT/ET and 54/74ABT16652 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



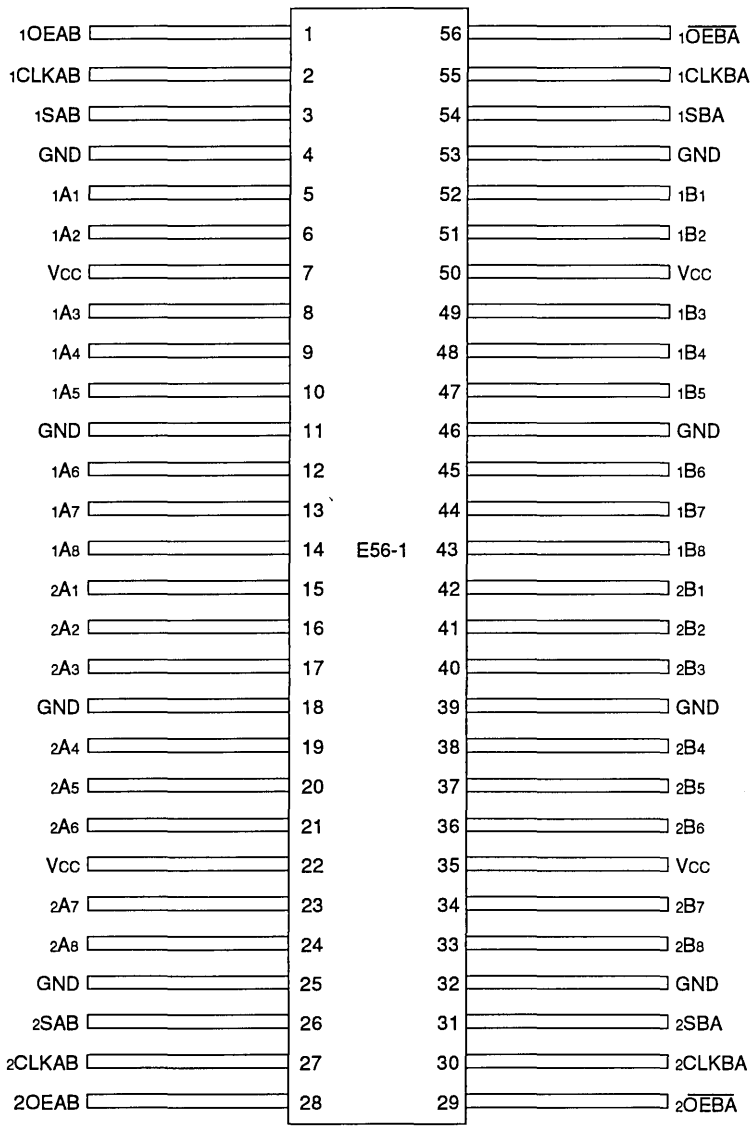


PIN CONFIGURATIONS



SSOP/
TSSOP
TOP VIEW

2549 drw 03



CERPACK
TOP VIEW

2549 drw 04

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, $x\overline{OEBA}$	Output Enable Inputs

2549 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2549 lnk 02
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(3)

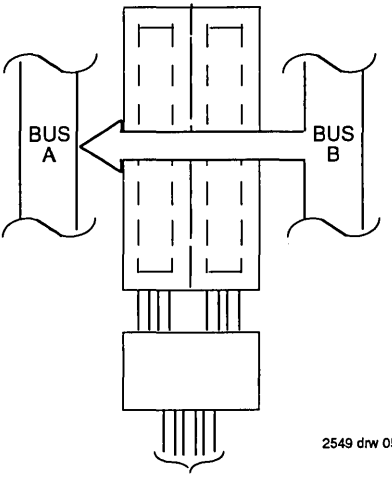
Inputs						Data I/O(1)		Operation or Function
xOEAB	$x\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified(1)	Store A, Hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified(1)	Input	Hold A, Store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

NOTES: 2549 tbl 03
1. The data output functions may be enabled or disabled by various signals at the xOEAB or $x\overline{OEBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ≠ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

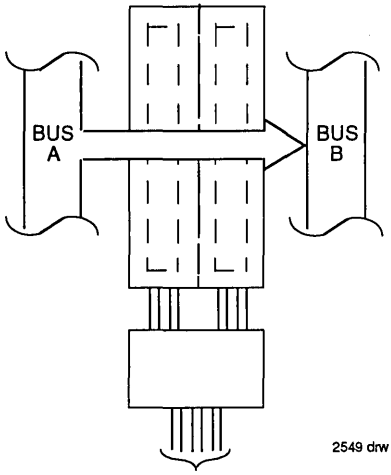
Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2549 lnk 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.



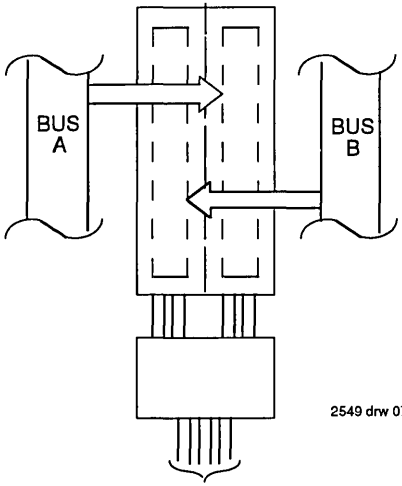
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



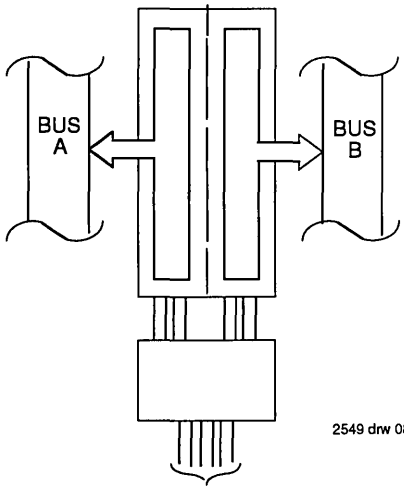
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2549 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16652T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2549 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162652T

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2549 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = $x\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xOEAB = $x\overline{OEBA}$=GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xOEAB = $x\overline{OEBA}$=GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2549 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16652T/162652T				FCT16652AT/162652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2549 tbl 09

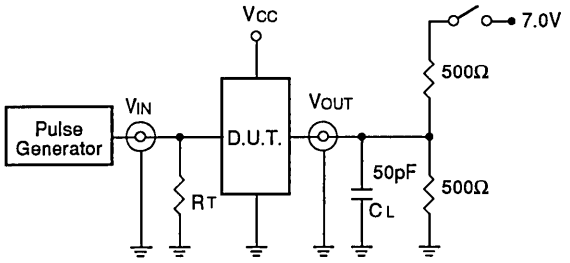
Symbol	Parameter	Condition[1]	FCT16652CT/162652CT				FCT16652ET/162652ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2549 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2549 drw 09

SWITCH POSITION

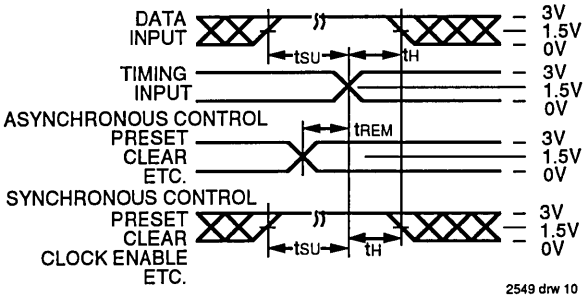
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2549 lnk 10

DEFINITIONS:

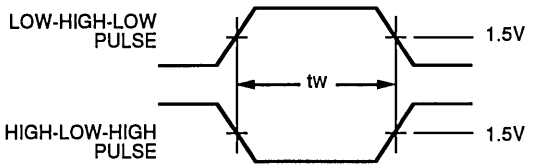
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



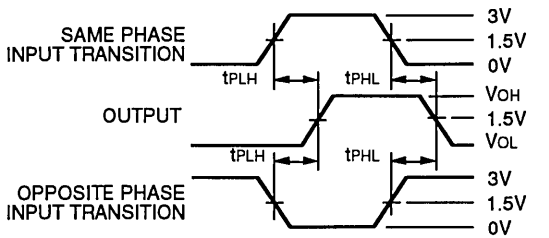
2549 drw 10

PULSE WIDTH



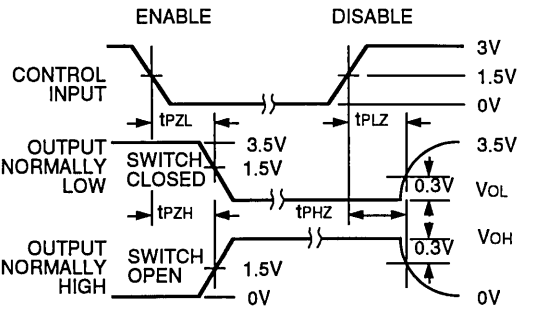
2549 drw 11

PROPAGATION DELAY



2549 drw 12

ENABLE AND DISABLE TIMES

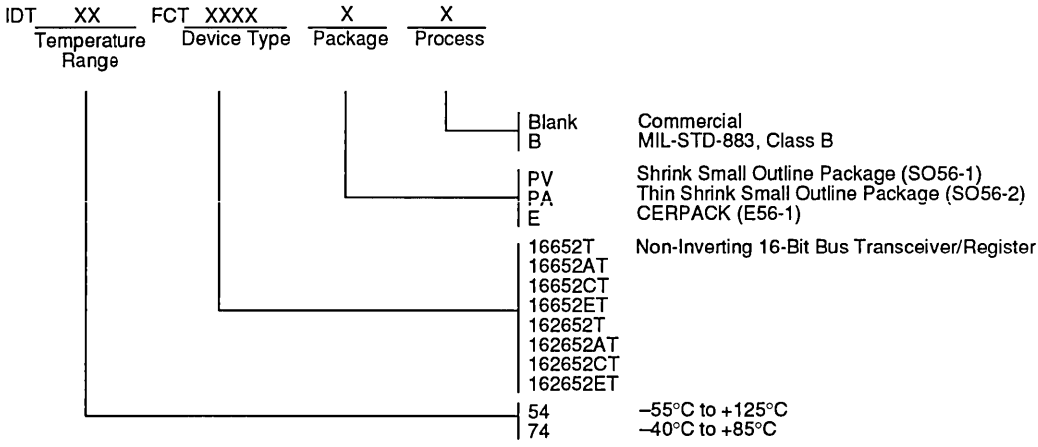


2549 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2549 drw 14

Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTER

IDT54/74FCT16823AT/BT/CT/ET
IDT54/74FCT162823AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16823AT/BT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162823AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

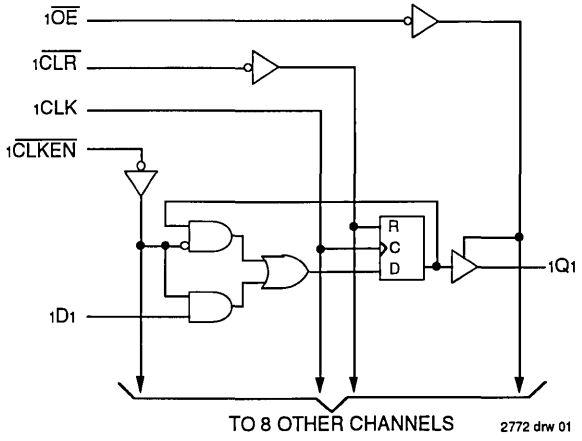
DESCRIPTION:

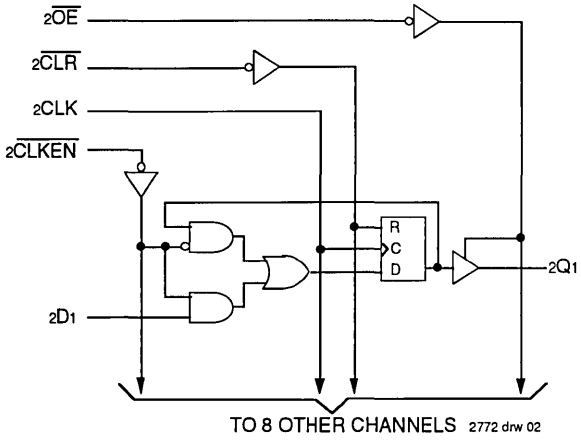
The IDT54/74FCT16823AT/BT/CT/ET and IDT54/74FCT162823AT/BT/CT/ET 18-bit bus interface registers are built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16823AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

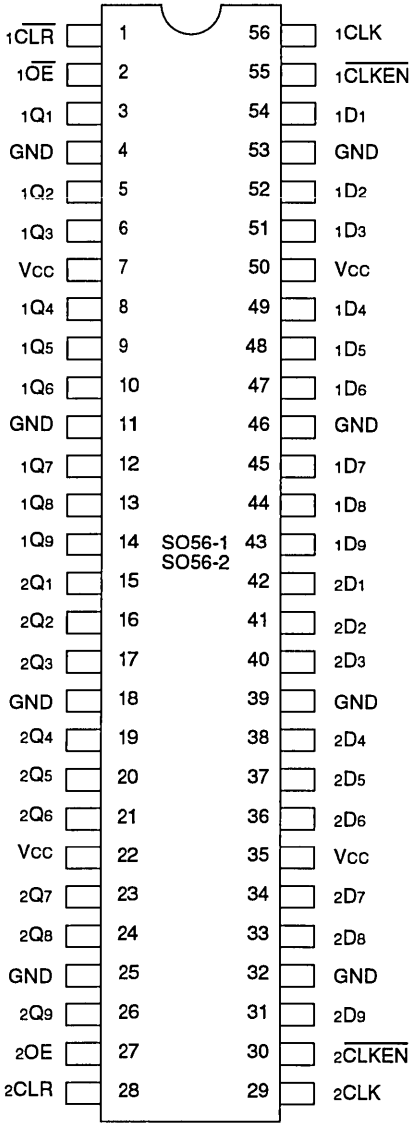
The IDT54/74FCT162823AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The IDT54/74FCT162823AT/BT/CT/ET are plug-in replacements for the IDT54/74FCT16823AT/BT/CT/ET and 54/74ABT16823 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



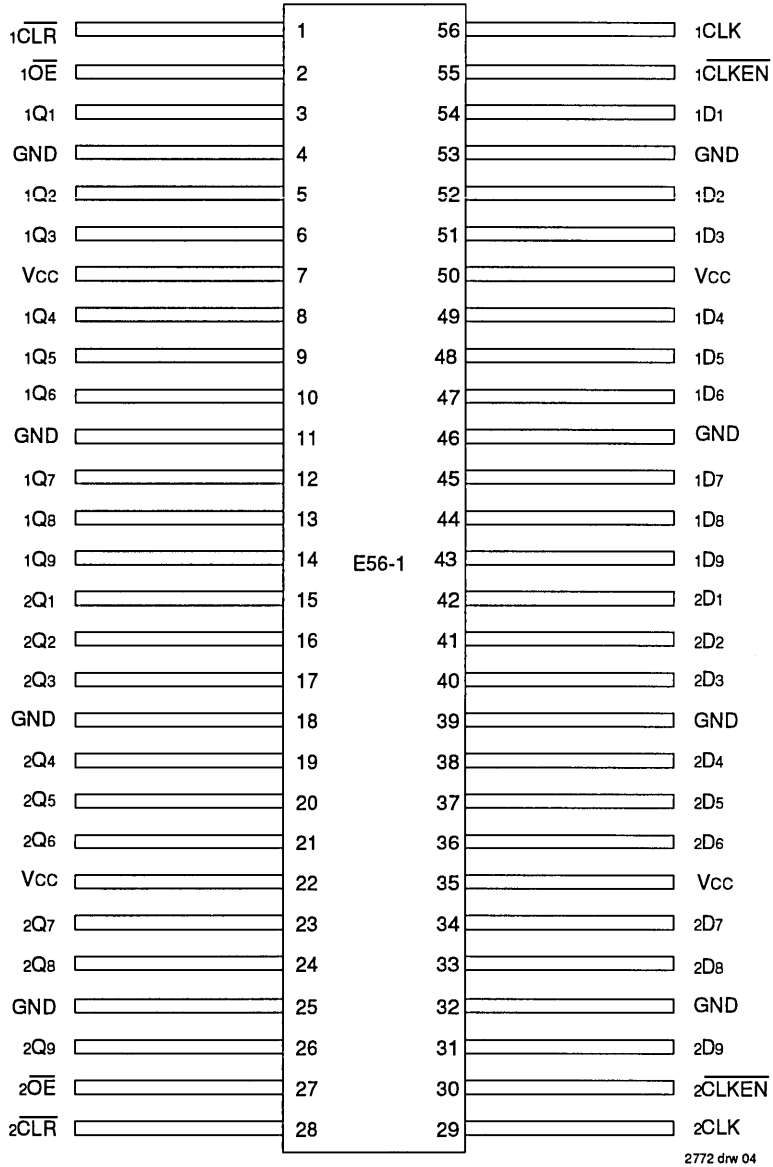


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2772 drw 03



CERPACK
TOP VIEW

2772 drw 04

PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
$x\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$x\overline{CLR}$	Asynchronous clear Inputs (Active LOW)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

2772 tbl 01

FUNCTION TABLE[1]

Inputs					Outputs	
$x\overline{OE}$	$x\overline{CLR}$	$x\overline{CLKEN}$	xCLK	xDx	xQx	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q[2]	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES:
2772 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
2772 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
2772 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2772 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.5	3.5	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2772 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2772 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.2	7.1[5]	
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	9.2	22.1[5]	

NOTES:

2772 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16823AT/162823AT				FCT16823BT/162823BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF[3] RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tPHL	Propagation Delay x$\overline{CLR}$ to xQx	CL = 50pF RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tPZH tPZL	Output Enable Time x$\overline{OE}$ to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to xQx	CL = 5pF[3] RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	
tSU	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW xDx to xCLK		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		2.0	—	2.0	—	0	—	0	—	ns
tW	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tW	x$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	7.0	—	6.0	—	6.0	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2772 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These limits are guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

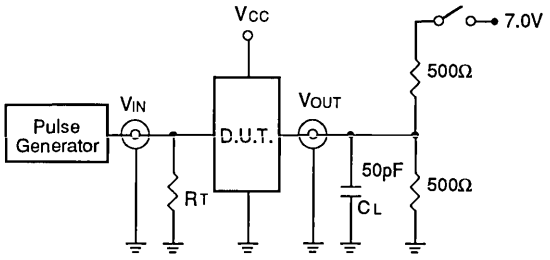
Symbol	Parameter	Condition[1]	FCT16823CT/162823CT				FCT16823ET/162823ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.4	—	—	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	—	—	
t_{PHL}	Propagation Delay $x\overline{CLR}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	4.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xQx	C_L = 5pF[3] R_L = 500Ω	1.5	6.2	1.5	6.2	1.5	3.6	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	6.5	1.5	3.6	—	—	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
t_{SU}	Set-up Time HIGH or LOW $x\overline{CLKEN}$ to xCLK		3.0	—	3.0	—	2.5	—	—	—	ns
t_H	Hold Time HIGH or LOW $x\overline{CLKEN}$ to xCLK		0	—	0	—	0.0	—	—	—	ns
t_W	xCLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.0[3]	—	—	—	ns
t_W	$x\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	3.0[3]	—	—	—	ns
t_{REM}	Recovery Time $x\overline{CLR}$ to xCLK		6.0	—	6.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

2772 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These limits are guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2773 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

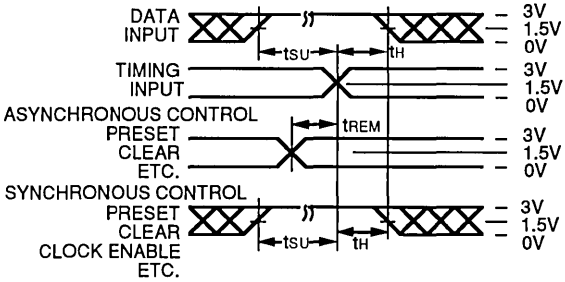
2773 tbl 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

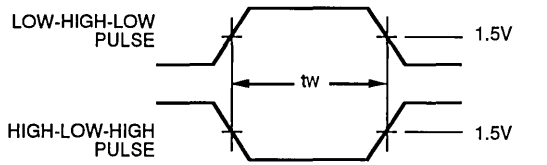
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



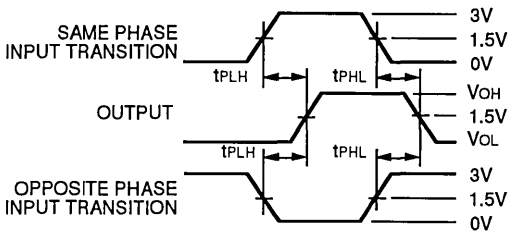
2773 drw 06

PULSE WIDTH



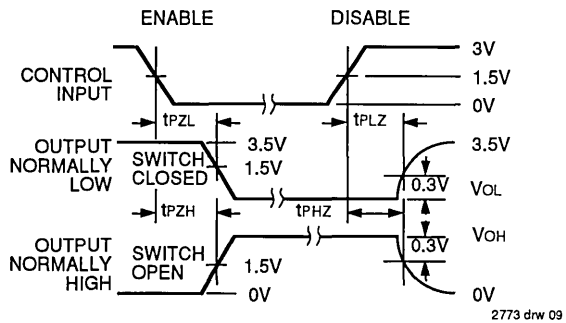
2773 drw 07

PROPAGATION DELAY



2773 drw 08

ENABLE AND DISABLE TIMES

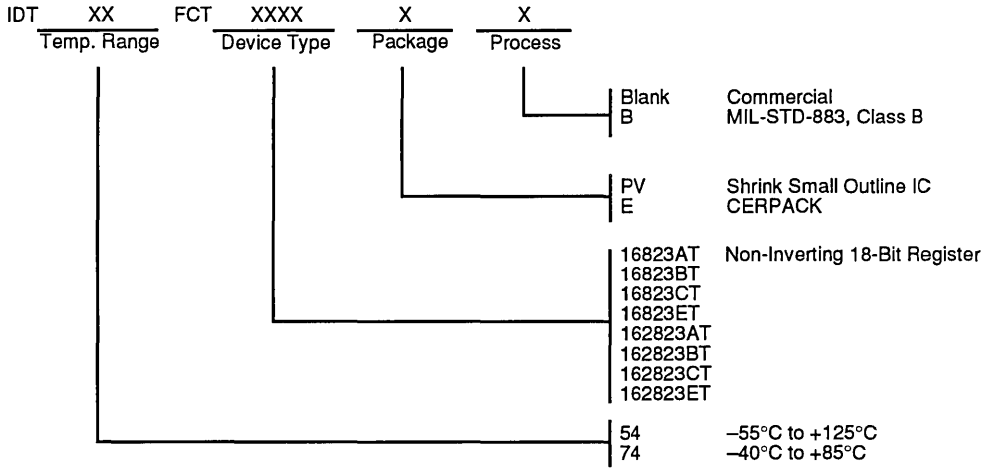


2773 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2772 drw 10

Integrated Device Technology, Inc.

FAST CMOS 20-BIT BUFFERS

IDT54/74FCT16827AT/BT/CT/ET
IDT54/74FCT162827AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16827AT/BT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162827AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

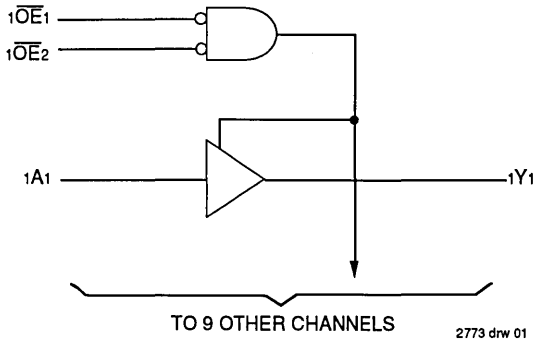
DESCRIPTION:

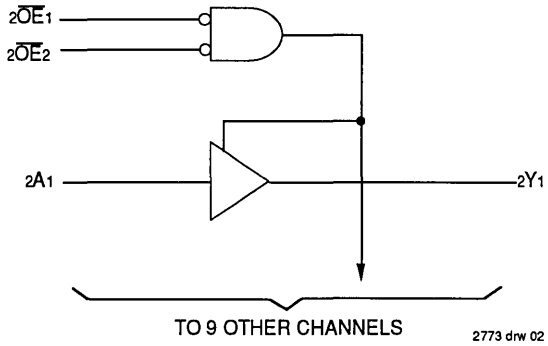
The IDT54/74FCT16827AT/BT/CT/ET and IDT54/74FCT162827AT/BT/CT/ET 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16827AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

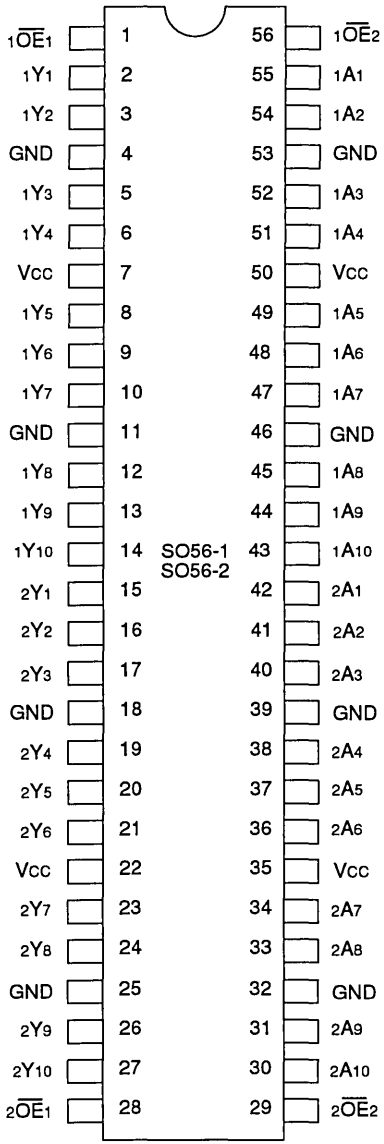
The IDT54/74FCT162827AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162827AT/BT/CT/ET are plug-in replacements for the IDT54/74FCT16827AT/BT/CT/ET and 54/74ABT16827 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



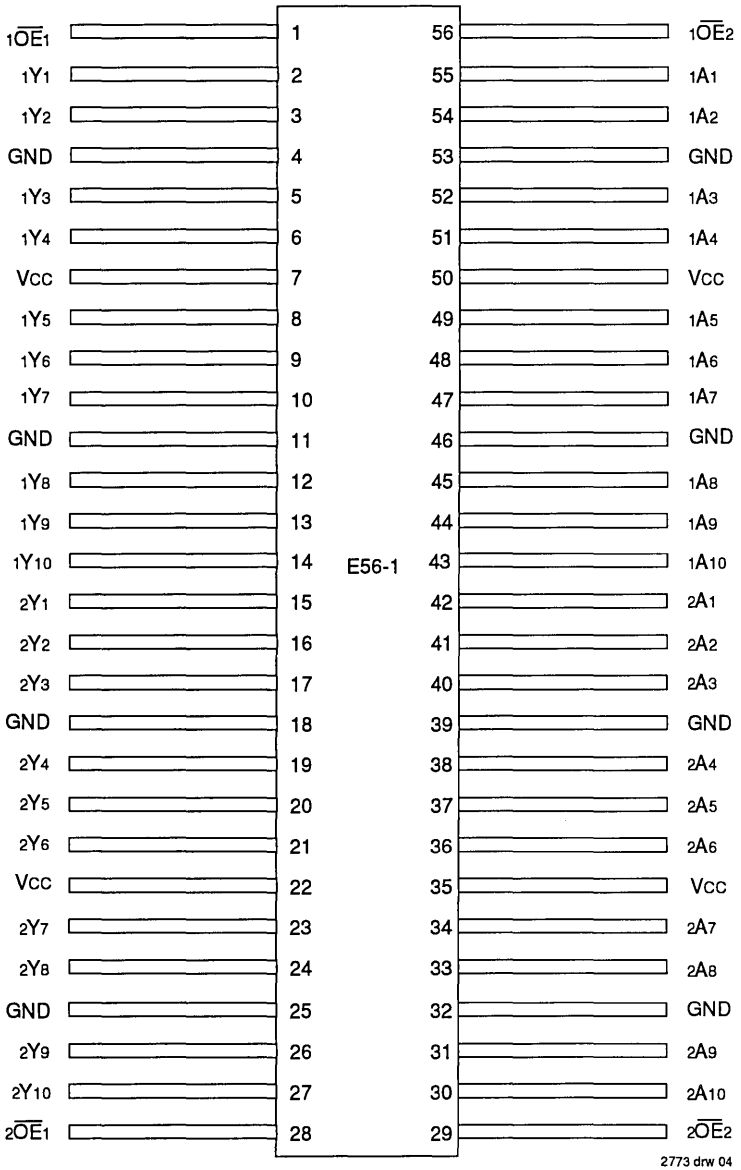


PIN CONFIGURATIONS



2773 drw 03

SSOP
TSSOP
TOP VIEW



2773 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xOE_x	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2773 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xOE_1	xOE_2	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

2773 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2773 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2773 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2773 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16827T

Symbol	Parameter	Test Conditions [1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2773 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2773 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2773 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16827AT/162827AT				FCT16827BT/162827BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $x\overline{OE}x$ to xYx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $x\overline{OE}x$ to xYx	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

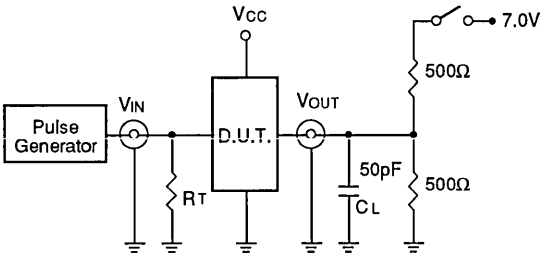
Symbol	Parameter	Condition[1]	FCT16827CT/162827CT				FCT16827ET/162827ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xAx to xYx	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.2	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.0	—	—	
tPZH tPZL	Output Enable Time $x\overline{OE}x$ to xYx	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $x\overline{OE}x$ to xYx	CL = 5pF[3] RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.0	—	—	
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

2773 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2773 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

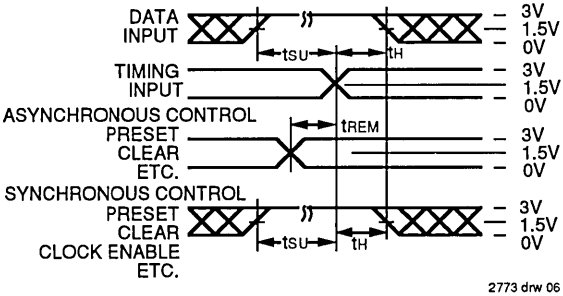
2773 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

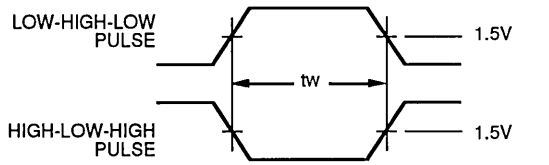
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



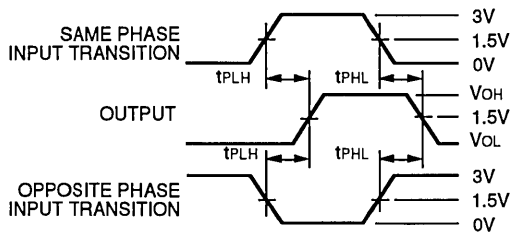
2773 drw 06

PULSE WIDTH



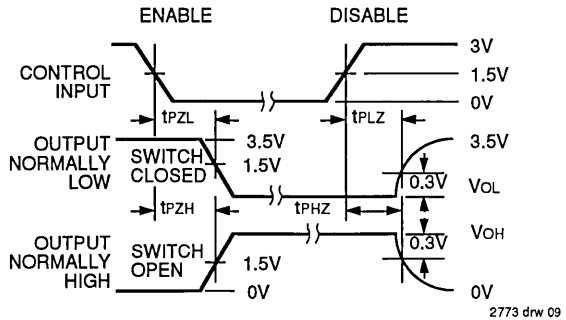
2773 drw 07

PROPAGATION DELAY



2773 drw 08

ENABLE AND DISABLE TIMES

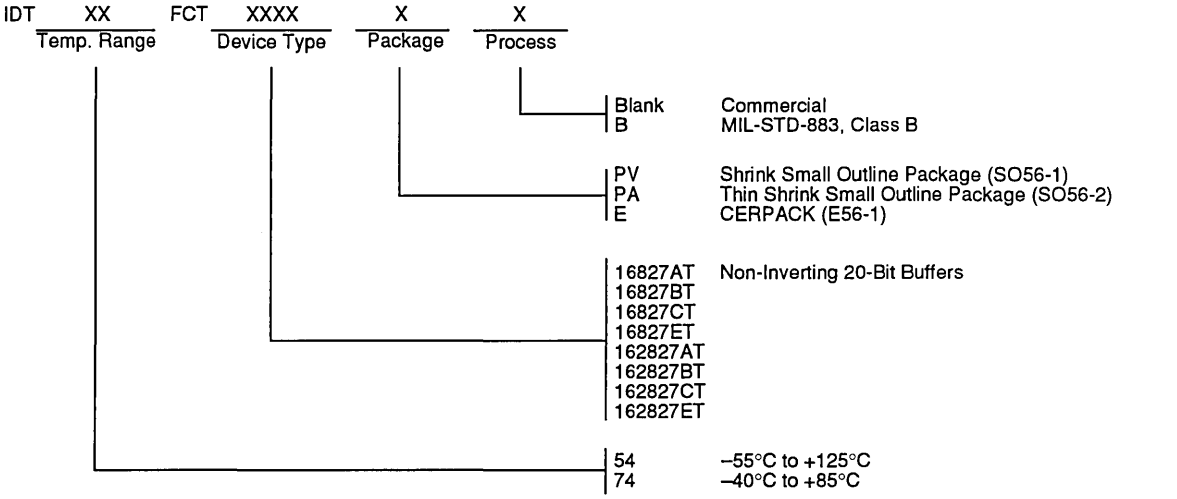


2773 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2773 drw 10

Integrated Device Technology, Inc.

FAST CMOS 20-BIT TRANSPARENT LATCHES

IDT54/74FCT16841AT/BT/CT/ET
IDT54/74FCT162841AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16841AT/BT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162841AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

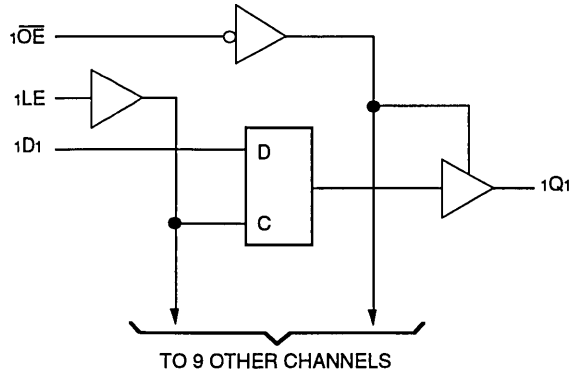
DESCRIPTION:

The IDT54/74FCT16841AT/BT/CT/ET and IDT54/74FCT162841AT/BT/CT/ET 20-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

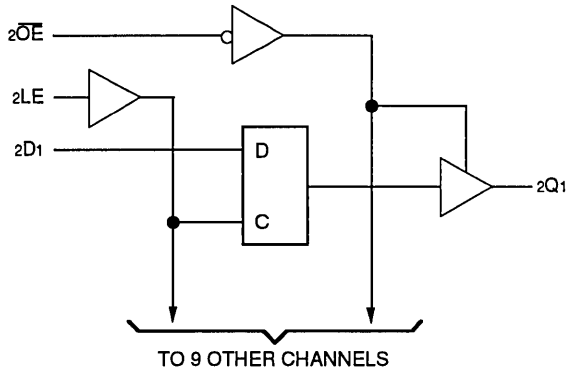
The IDT54/74FCT16841AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162841AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162841AT/BT/CT/ET are plug-in replacements for the IDT54/74FCT16841AT/BT/CT/ET and 54/74ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

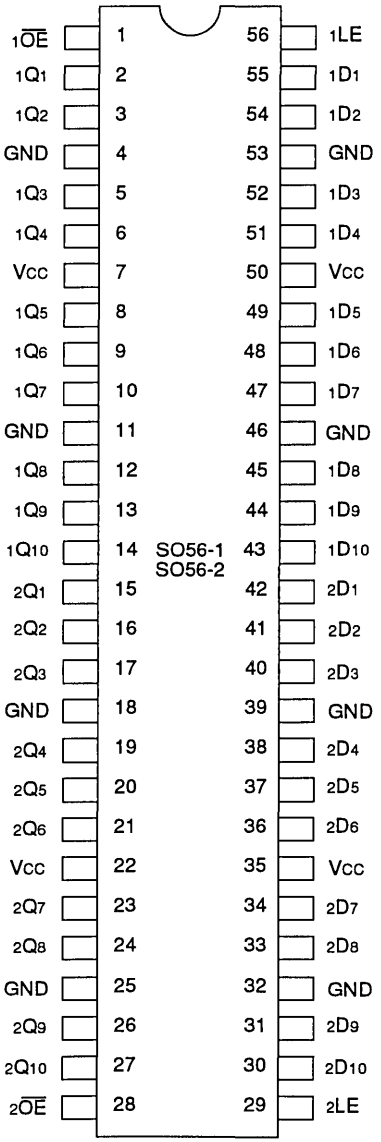


2556 drw 01



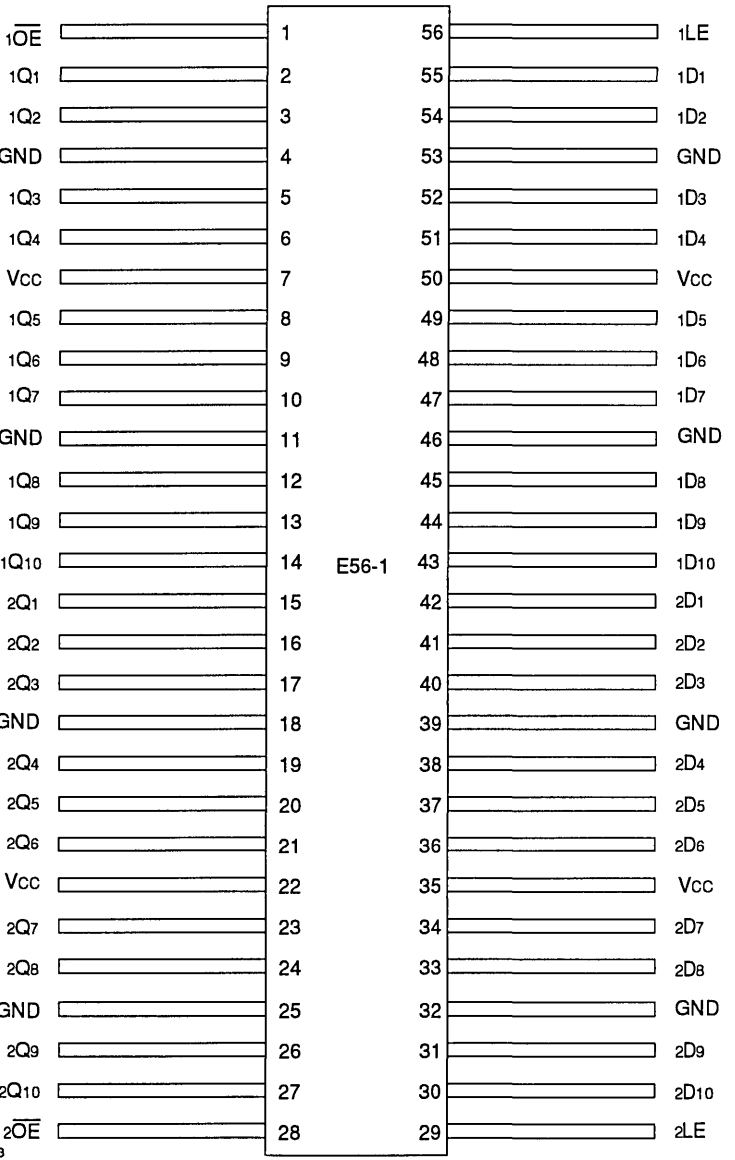
2556 drw 02

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2556 drw 03



2556 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
$x\overline{OE}$	Output Enable Input (Active LOW)
xQx	3-State Outputs

2556 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

2556 tbl 02

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2556 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2556 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2556 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16841T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2556 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162841T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2556 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Twenty Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2556 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16841AT/162841AT				FCT16841BT/162841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time x$\overline{OE}$ to xQx	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to xQx	CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	xLE Pulse Width HIGH		4.0[3]	—	5.0	—	4.0[3]	—	4.0[3]	—	ns
tSK(o)	Output skew[5]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2556 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These limits are guaranteed but not tested.
4. These conditions are guaranteed but not tested.
5. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

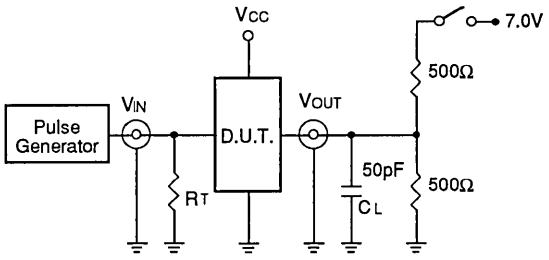
Symbol	Parameter	Condition[1]	FCT16841CT/162841CT				FCT16841ET/162841ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	5.5	1.5	6.3	1.5	3.4	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	13.0	1.5	15.0	1.5	7.5	—	—	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	6.4	1.5	6.8	1.5	3.7	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	15.0	1.5	16.0	1.5	7.5	—	—	
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.3	1.5	4.4	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xQx	C_L = 5pF[4] R_L = 500Ω	1.5	5.7	1.5	6.0	1.5	3.6	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	6.3	1.5	3.6	—	—	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	1.0	—	—	—	ns
t_W	xLE Pulse Width HIGH		4.0[3]	—	4.0[3]	—	3.0[3]	—	—	—	ns
$t_{SK(o)}$	Output skew[5]		—	0.5	—	0.5	—	0.5	—	—	ns

2556 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These limits are guaranteed but not tested.
4. These conditions are guaranteed but not tested.
5. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

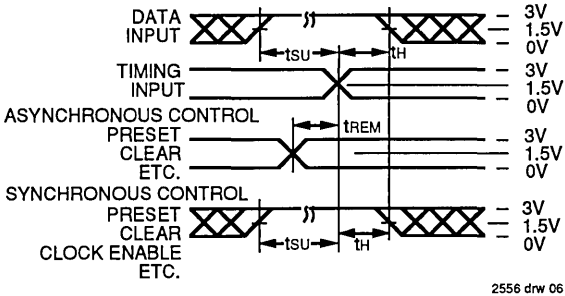
2556 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

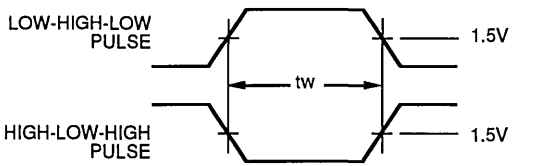
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



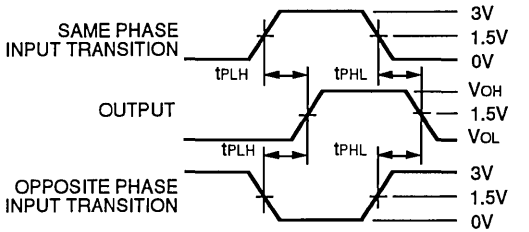
2556 drw 06

PULSE WIDTH



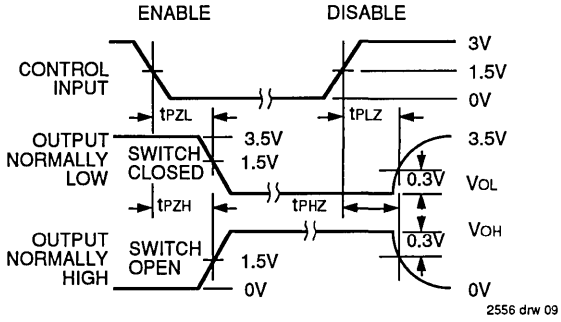
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

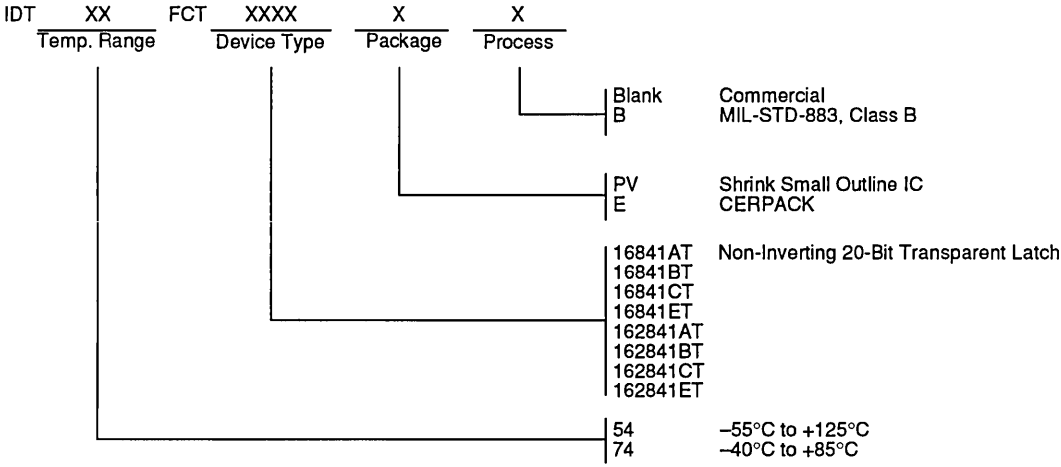


2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2556 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/ET
IDT54/74FCT162952AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of –40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16952AT/BT/CT/ET:**
  - High drive outputs (–32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162952AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

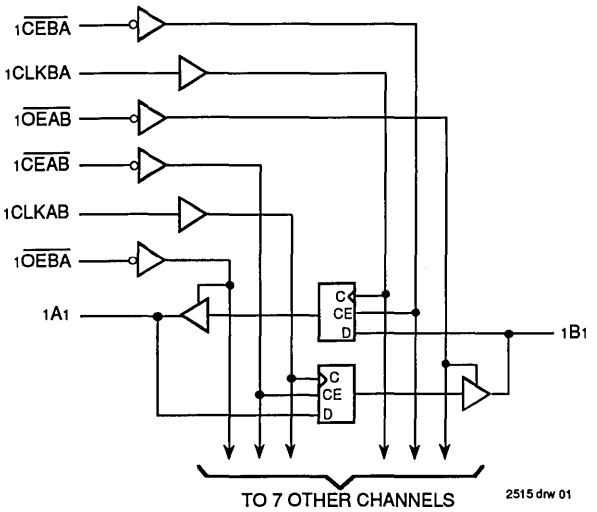
DESCRIPTION:

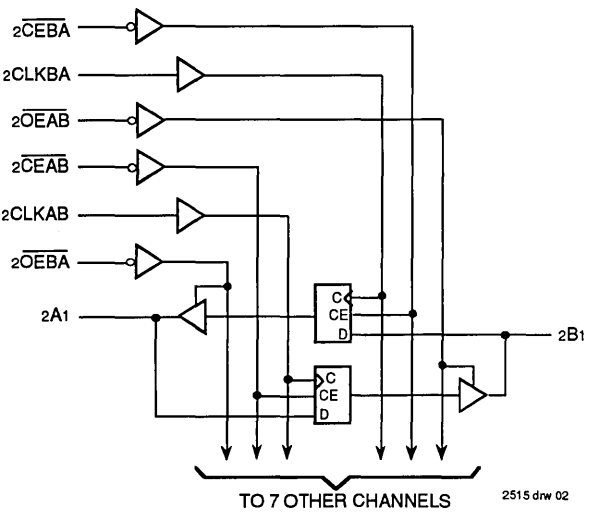
The IDT54/74FCT16952AT/BT/CT/ET and IDT54/74FCT162952AT/BT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for each set to permit independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW in order to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $xOEAB$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $xCEBA$, xCLKBA, and $xOEBA$ inputs. The flow-through organization of signal pins simplifies layout. Full 16-bit operation can be achieved by tying the control pins of the independent transceivers together. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16952AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability allowing "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162952AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162952AT/BT/CT/ET are plug-in replacements for the IDT54/74FCT16952AT/BT/CT/ET and 54/74ABT16952 for on-board bus interface applications.

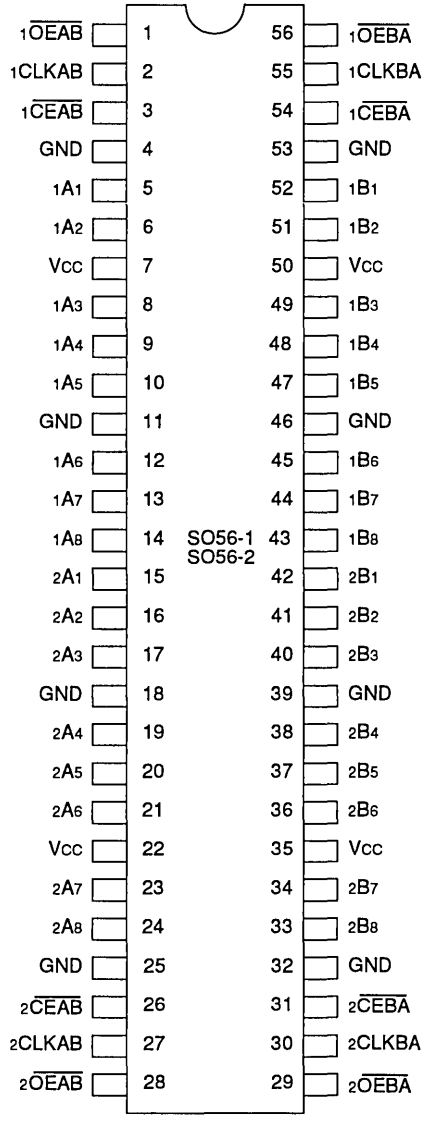
FUNCTIONAL BLOCK DIAGRAM





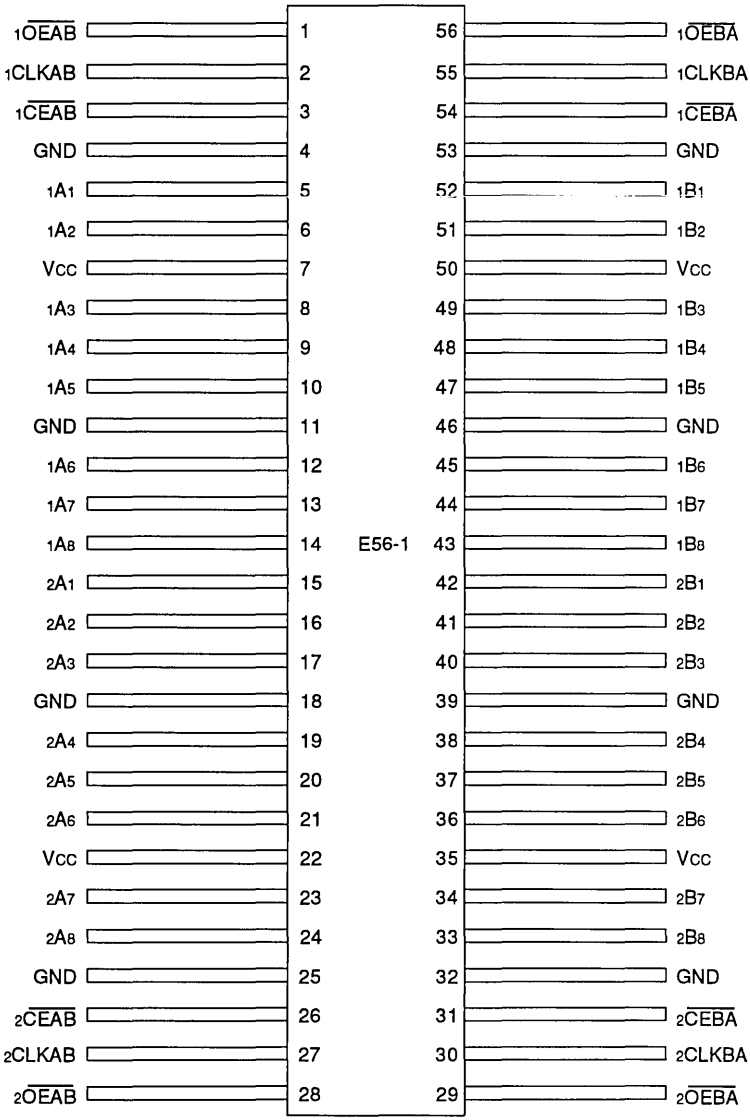
DSC-4633/3

PIN CONFIGURATIONS



2515 drw 03

SSOP
TSSOP
TOP VIEW



2515 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

2515 tbl 01

FUNCTION TABLE[1,3]

Inputs				Outputs
$x\overline{CEAB}$	xCLKAB	$x\overline{OEAB}$	xAx	xBx
H	X	L	X	B[2]
X	L	L	X	B[2]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES: 2515 tbl 02

1. A-to-B data flow is shown: B-to-A data flow is similar but uses, $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2515 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2515 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2515 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2515 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V(3)		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V(3)		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2613 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2515 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs HIGH
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16952AT/162952AT				FCT16952BT/162952BT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2515 tbl 09

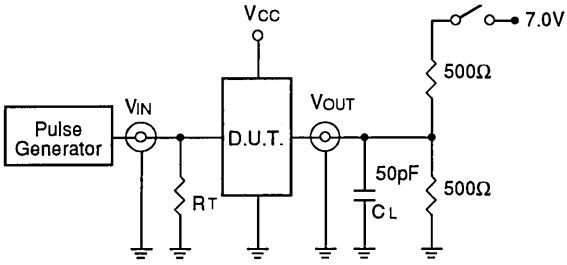
			FCT16952CT/162952CT				FCT16952ET/162952ET				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2.0	6.3	2.0	7.3	1.5	3.7	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	6.5	1.5	7.5	1.5	3.6	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	0	—	—	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
2515 tbl 10

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2515 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

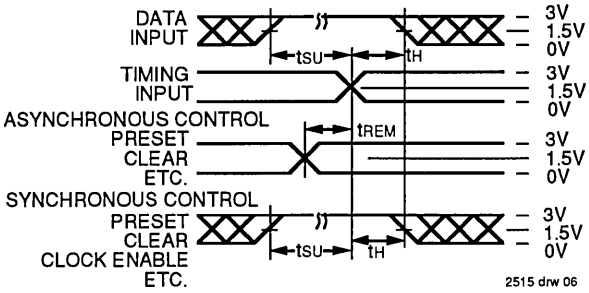
2515 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

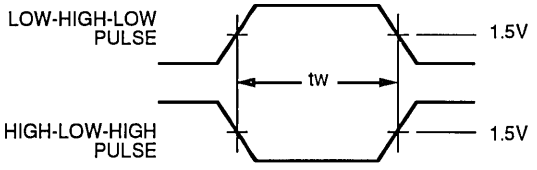
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



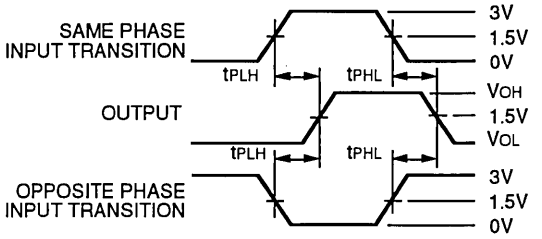
2515 drw 06

PULSE WIDTH



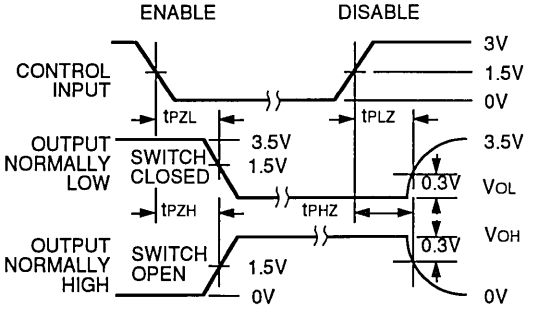
2515 drw 07

PROPAGATION DELAY



2515 drw 08

ENABLE AND DISABLE TIMES

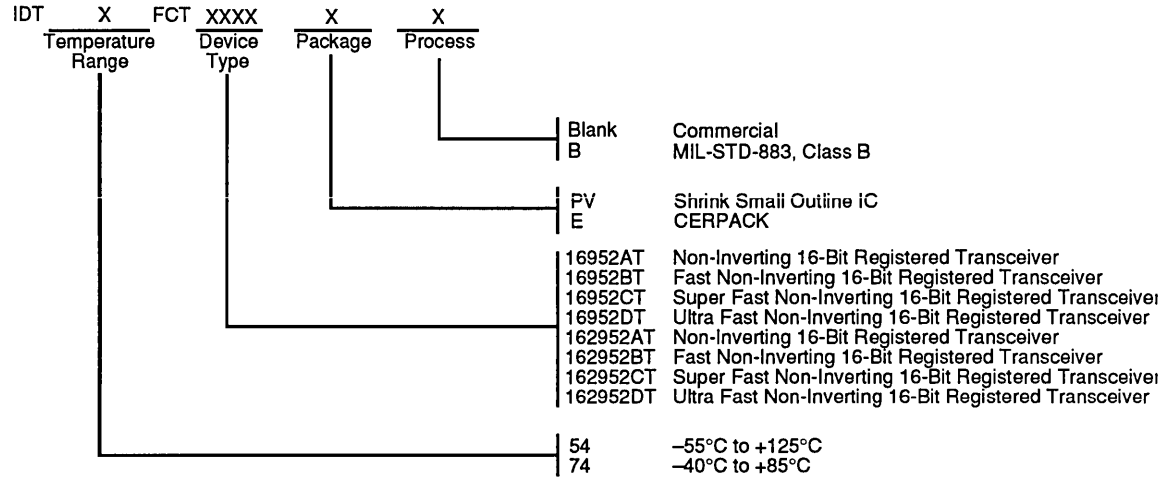


2515 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

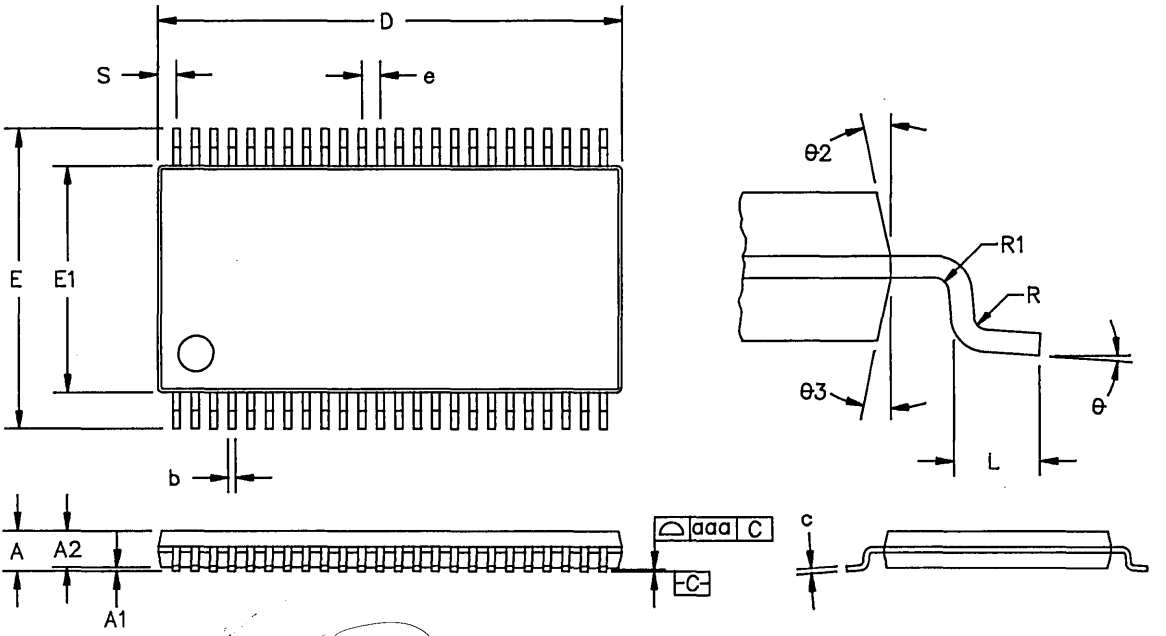
ORDERING INFORMATION



2515 drw 10

SMALL OUTLINE IC

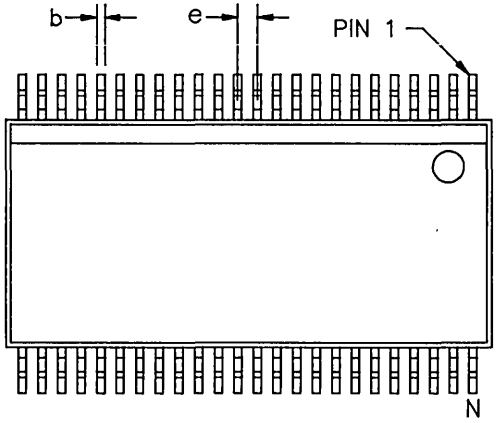
48 & 56 LEAD TSSOP



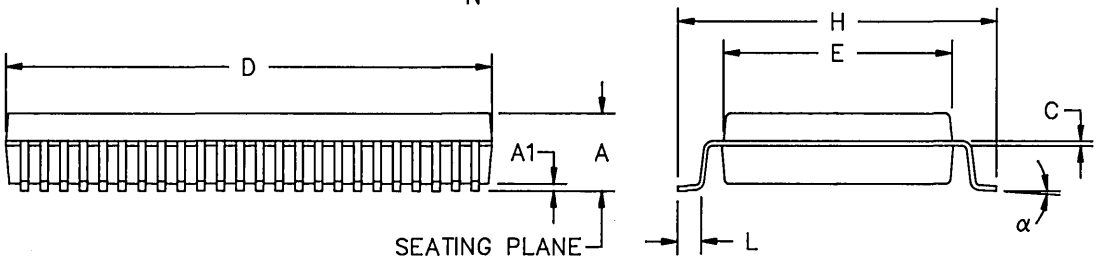
DWG #	SO48-2		SO56-2	
SYMBOL	MIN	MAX	MIN	MAX
A	–	1.10	–	1.10
A1	.00	.10	.00	.10
A2	.95	1.05	.95	1.05
D	12.40	12.80	13.90	14.30
E1	6.00	6.40	6.00	6.40
E	7.80	8.40	7.80	8.40
L	.50	.75	.50	.75
R	.09	–	.09	–
R1	.09	–	.09	–
e	.50 BSC		.50 BSC	
aaa	–	.10	–	.10
b	.15	.30	.15	.30
c	.10	.20	.10	.20
θ	0°	10°	0°	10°
θ1	10°	20°	10°	20°
θ2	10°	20°	10°	20°
S	–	.65	–	.40

SMALL OUTLINE IC

48 & 56 LEAD SSOP (JEDEC)



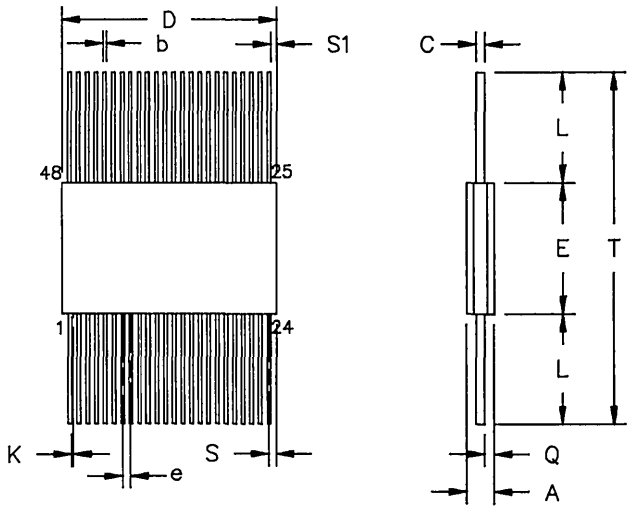
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



DWG #	SO48–1		SO56–1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
L	.020	.040	.020	.040
α	0°	8°	0°	8°

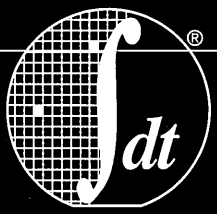
CERPACKS

48–56 LEAD CERPACK (.025" LEAD PITCH)



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.
4. THIS DWG REPRESENTS A 48 LEAD CERPACK.

DWG #	E48–1		E56–1	
# OF LDS (N)	48		56	
SYMBOL	MIN	MAX	MIN	MAX
A	.065	.086	.065	.086
b	.008	.013	.008	.013
C	.0045	.006	.0045	.006
D	.614	.626	.713	.727
E	.370	.390	.370	.390
e	.025 BSC		.025 BSC	
K	.003	.007	.003	.007
L	.312	.405	.312	.405
Q	.035	.045	.035	.045
S	–	.045	–	.045
S1	.005	–	.005	–
T	.995	1.200	.995	1.200



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