



**FUTURE ELECTRONICS 1994 DATA BOOK**

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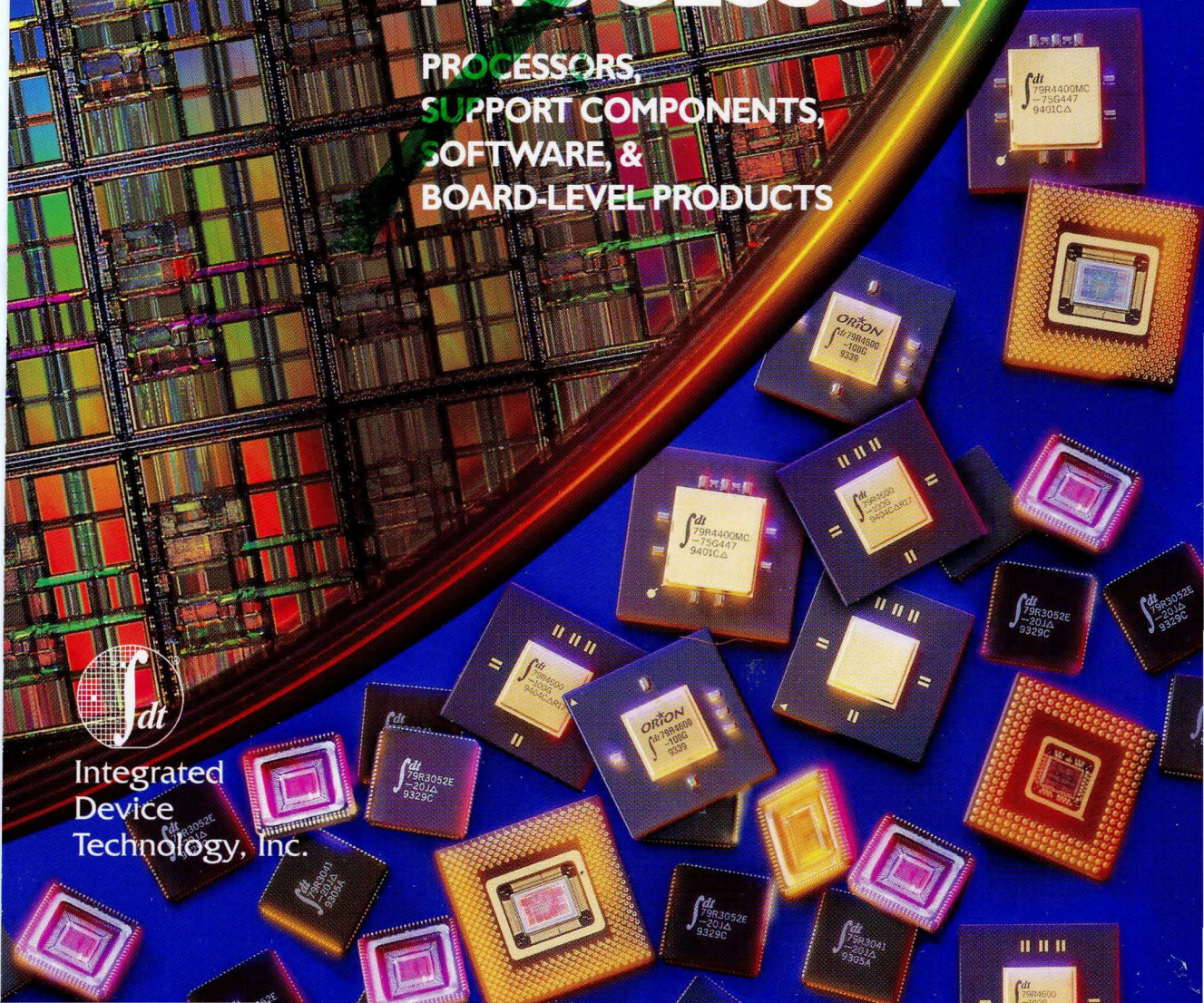
**FUTURE IS UNIQUE**

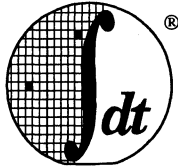
# RISC MICRO- PROCESSOR

PROCESSORS,  
SUPPORT COMPONENTS,  
SOFTWARE, &  
BOARD-LEVEL PRODUCTS



Integrated  
Device  
Technology, Inc.





**Integrated Device Technology, Inc.**

**1994**  
**RISC MICROPROCESSOR**  
**COMPONENTS & SUBSYSTEMS**  
**DATA BOOK**

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## CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books — Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1994 RISC Data Book is comprised of new and revised data sheets for the RISC and RISC Subsystems product groups. Also included is a current packaging section for the products included in this book. This section will be updated in each subsequent data book to reflect packages offered for products included in that book.

The 1994 RISC Data Book's Table of Contents contains a listing of the products contained in that data book only. In the past we have included products that appeared in other IDT data books. The numbering scheme for the book is as follows: the number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speed, lower power, and package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

**To find ordering information:** Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, and Cross Reference Guides. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

**To find product data:** Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

**ADVANCE INFORMATION** — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

**PRELIMINARY** — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

**FINAL** — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

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## **LIFE SUPPORT POLICY**

**Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.**

- 1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

Note: Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

The IDT logo is a registered trademark, and BUSMUX, Flexi-pak, BiCEMOS, CacheRAM, CEMOS, FASTX, Flow-thruEDC, IDT/c, IDT/envY, IDT/sae, IDT/sim, IDT/ux, MacStation, REAL8, RISC SubSystem, RISController, RISCORE, SmartLogic, SyncFIFO, TargetSystem, Orion, R3041, R3051, and R3081 are trademarks of Integrated Device Technology, Inc.

All other trademarks are trademarks of their respective companies.

# 1994 RISC DATA BOOK

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## ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

- A. Complete Bill To.
- B. Complete Ship To.
- C. Purchase Order Number.
- D. Certificate of Conformance. Y or N.
- E. Customer Source Inspection. Y or N.
- F. Government Source Inspection. Y or N
- G. Government Contract Number and Rating.
- H. Requested Routing.
- I. IDT Part Number —  
Each item ordered must use the complete part number exactly as listed in the price book.
- J. SCD Number — Specification Control Document (Internal Traveller).
- K. Customer Part Number/Drawing Number/Revision Level —  
Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
- L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
- M. Request Date With Exact Quantity.
- N. Unit Price.
- O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772

Dun & Bradstreet Number — 03-814-2600

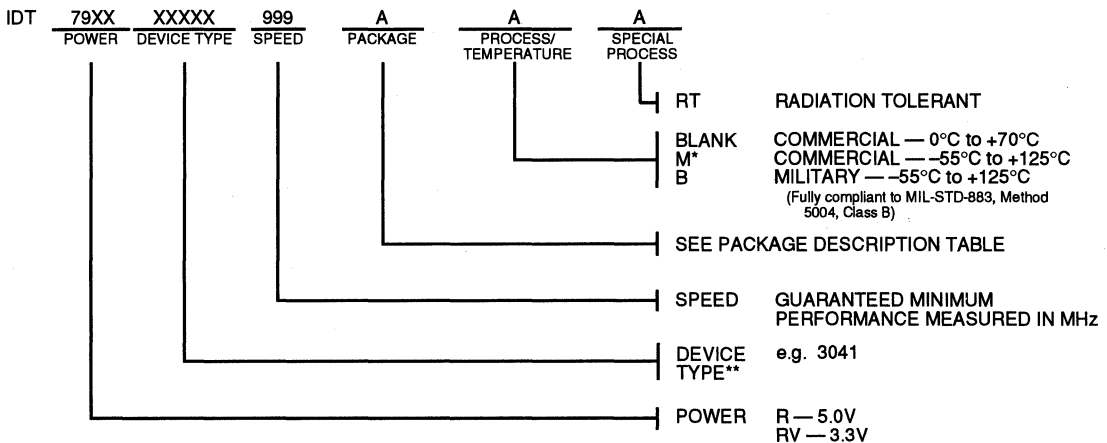
Federal Tax I.D. — 94-2669985

TLX# — 887766

FAX# — 408-727-3468

## PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character



### PACKAGE DESCRIPTION TABLE

C	CERAMIC SIDEBRAZE	PF	PLASTIC FLATPACK
D	CERDIP	SO	PLASTIC SMALL OUTLINE IC
F	FLATPACK	TC	SIDEBRAZE THINDIP (300 MIL)
G	PIN GRID ARRAY	TP	PLASTIC THIN DUAL IN-LINE
J	PLASTIC LEADED CHIP CARRIER	QE	CERQUAD GULL WING
L	LEADLESS CHIP CARRIER	XE	CERPACK (F11 CONFIG. ONLY)
P	PLASTIC DIP	XL	FINE-PITCH LCC
Y	SOJ		

\*Consult Factory

\*\*For Logic, the "54" series (e.g. IDT54FCT138) — -55°C to +125°C  
the "74" series (e.g. IDT74FCT138) — 0°C to +70°C

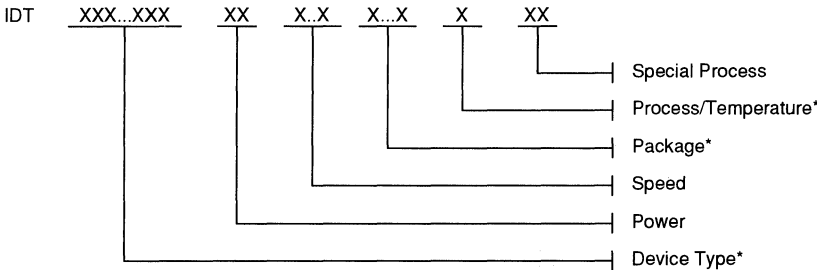
# IDT PACKAGE MARKING DESCRIPTION

## PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used: "S" or "SA" is used for the standard power product. "L" or "LA" is used for lower power than the standard power product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



\* Field Identifier Applicable To All Products

2507 drw 01

## ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

- A = Anam, Korea
- I = USA
- P = Penang, Malaysia

## MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.



Integrated Device Technology, Inc.

## HIGH-SPEED CMOS MICROPROCESSOR FAMILY PRODUCT SELECTOR GUIDE

### High-Speed CMOS Microprocessor Family

- Broadest range of high-performance to low-cost, code-compatible RISC processors: R3000A, R4000 CPUs, R3001, R3051/52/81/41 RISCControllers, R3010A FPA, R3500 RISCCore
- R4000—third-generation high-performance 64-bit CPU and FPA with on-chip cache
- R3001 and R3051/52/81/41 RISCController Family—designed for low-cost embedded systems, all code-compatible with original R3000
- R3500 RISCCore—combines CPU and FPA, pin- and SW-compatible with the R3000A
- Support chips designed for RISC systems: R3020 Write Buffer, 73720 Bus Exchanger, R3721 DRAM Controller
- Applications range from real-time control to multiprocessing systems
- Optimizing compilers for C, Pascal, FORTRAN, Ada, PL/1 and Cobol
- R3000, R3001, R3051/52/81/41 and R3500 are 100% code-compatible
- R3010A Floating Point Accelerator—conforms with IEEE 754 1985 Standard
- R3020 Write Buffer enhances CPU performance by allowing memory "write-through" during run cycles
- Low-cost Evaluation Boards available
- In the Data Book Page column, "G" references the 1992/3 RISC Microprocessor Components and Subsystems Data Book, while "J" references the 1994 RISC Microprocessor Components and Subsystems Data Book.

Part Number	Description	Pkgs.	Avail.	Data Book Page
<b>RISC CMOS MICROPROCESSORS</b>				
IDT79R4000/4400	Very high-performance, highly integrated 64-bit CPU, fully binary compatible with the R3000A. Combines CPU, floating-point and 16/32KB of cache, capable of over 50 VAX mips sustained performance	447PGA 179PGA	NOW	J 5.6
IDT79R4600	Very high-performance, highly integrated 64-bit CPU, fully binary compatible with the R3000A optimized for low-cost systems. Combines CPU, floating-point and 32KB of cache, capable of over 50 VAX mips sustained performance	179 PGA	NOW	J 5.7
IDT79R3000A	RISC CPU Processor, 20–40MHz, on-chip Cache Control, Memory Management Unit, 64-Entry Translation Lookaside Buffer, thirty-two 32-bit general-purpose registers	144PGA 175PGA 160 Mquad	NOW	J 5.1
IDT79R3500	RISCCore integrates R3000A CPU and R3010A FPA using the R3000A pinout.	161PGA 160Mquad	NOW	G 5.3
IDT79R3010A	RISC Floating-Point Accelerator, 20–40MHz	84PGA	NOW	J 6.1
IDT79R3041	RISCController, 2.5KB cache, R3000A core, 4-deep read/write buffers, low-cost packaging, pin-compatible with R3051/52/81	84PLCC 84PF	NOW	J 5.2
IDT79R3051/52	RISCControllers, 6KB or 10KB on-chip cache, R3000A CPU core, and 4-deep read/write buffers, low-cost 84-pin plastic packaging	84PLCC 84MJ	NOW	J 5.3
IDT79R3081	RISCController, 20KB on-chip cache, R3000 CPU core, R3010A Floating Point Accelerator, 4-deep read/write buffers, pin-compatible with R3051/52/41	84MJ	NOW	J 5.5
<b>RISC SUPPORT DEVICES</b>				
IDT73720	16-Bit Tri-Port Bus Exchanger	68PLCC 80PQFP	NOW	J 6.4
IDT79R3020	RISC CPU Write Buffer	68PLCC	NOW	J 6.3

## High-Speed CMOS RISC Microprocessor Family (Cont'd)

Part Number	Description	Avail.	Data Book Page
<b>R3000 FAMILY EVALUATION KITS</b>			
IDT79S341	R3041 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3041 CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	J 7.5
IDT79S385A	R305X Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3052E CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports. Supplied with all schematics, PAL equations and user's manual. Also includes DOS version of the IDT/c compiler (see 7RS903) and a sample of the R3081.	NOW	J 7.4
IDT79S381	R3081 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3081 CPU, 2MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	J 7.6
IDT79S460	R4600 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R4600 CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	J 7.7
IDT79S389	R3051 Family Laser Printer Controller Reference Platform for PostScript Level 2 Software from Adobe. Board uses R305x, IDT79R3721 DRAM Controller and IDT73720 Bus Exchanger. Kit contains 3051 and 3081. Board configured with 8MB DRAM (up to 64MB possible), 4MB EPROM and 512 bytes EEROM. Programmable DUART (85C30), SCSI Controller, Appletalk and Centronics port. Also contains IDT/sim initialization and monitor debug softwar. Expansion connector for custom engine interface, additional I/O or additional font ROM space.	NOW	J 7.3
<b>R3000 FAMILY SOFTWARE DEVELOPMENT TOOLS</b>			
IDT79S901	IDT/sim System Integration Manager (see RISC SubSystems for description)	NOW	J 7.8
IDT79S903	IDT/c C-Compiler (see RISC SubSystems for description)	NOW	J 7.9
IDT79S909	IDT/kit Kernel Integration Toolkit (see RISC SubSystems for description)	NOW	J 7.10
<b>R3000/R4000 FAMILY MIPS SOFTWARE</b>			
79SXCC-3A-BU1-200	RISCCross C-Compiler, R3000 & R4000 Binary Single-user Sun Host	NOW	CALL
79SXCC-3A-BU3-200	RISCCross C-Compiler, R3000 & R4000 Binary Multi-user Sun Host	NOW	CALL
79SXPE-3A-BU1-110	RISCCross SPP/e, R3000 Binary Single-user Sun Host	NOW	CALL
79SXPE-3A-BU3-110	RISCCross SPP/e, R3000 Binary Multi-user Sun Host	NOW	CALL
79SXPE-4A-BU1-110	RISCCross SPP/e, R4000 Binary Single-user Sun Host	NOW	CALL
79SXPE-4A-BU3-110	RISCCross SPP/e, R4000 Binary Multi-user Sun Host	NOW	CALL
79SXPC-31A-BU1	RISCCross Cache, R3000 Binary Single-user Sun Host	NOW	CALL
79SXPC-31A-BU3	RISCCross Cache, R3000 Binary Multi-user Sun Host	NOW	CALL
79SXPC-4A-BU1-120	RISCCross Cache, R4000 Binary Single-user Sun Host	NOW	CALL
79SXPC-4A-BU3-120	RISCCross Cache, R4000 Binary Multi-user Sun Host	NOW	CALL

### Integrated RISC Design Solutions

IDT is committed to providing complete integrated RISC solutions by combining expertise in silicon process technology with leadership products in development systems and software. Long an industry leader in producing the fastest static RAMs for cache memory and high-speed logic for memory interface, IDT offers:

- Dedicated RISC support chips
- MIPS compilers and cross-software for PC and Sun
- CPU and cache modules
- RISC evaluation and prototyping vehicles
- Monitors and debuggers



# RISC SubSystems—RISC Without Risk ..... IDT Provides Total RISC System Solutions!

## FASTER SYSTEMS: FASTER DESIGN CYCLES

Using RISC technology, you can build systems that will run rings around an old x86 or 680x0 design. IDT's RISC SubSystems Division can help you get your design completed in record time. IDT has proven RISC design and manufacturing experience that you can rely on. Exploit our expertise by having IDT design AND manufacture your board. Or integrate one of our pre-built, fully-tested modules into your design.

### Architectural Expertise

IDT brings together a unique combination of component knowledge, software skills, and board design experience as the foundation for developing a board-level product that meets your needs. As experienced system architects, we understand that component knowledge alone is not enough—that the interface between hardware and software is critical to a successful design. We have spent years honing our architectural expertise to include an in-depth understanding of both the hardware and software issues so our designs produce the performance you expect.

### Fast Development Cycle

IDT uses the most advanced engineering tools in our hardware development lab. We have qualified quick-turn PCB fab houses and our own fully-equipped advanced manufacturing area, so new fabs can be assembled and sent into debug in a matter of days. In addition, IDT has developed the best software diagnostic tools available for MIPS RISC debug. Spotting behavioral patterns in malfunctioning systems and quickly identifying and fixing the hardware or software problem is key to maintaining a time-critical development cycle—and we want you to be first to market!

### Optimized Designs

IDT is a premier supplier of RISC assemblies. Our expertise in handling layout, termination, and component selection issues is unmatched, and we use the latest tools for PCB layout, routing and design simulation. Our design team is fast and experienced, coordinating component selection with availability of the latest technology, and using ASICs where appropriate to improve performance and reduce space and cost. To date, we have designed and produced more different MIPS RISC assemblies than anyone else, optimizing every design for the highest possible performance per dollar.

### Total Support

On-going support means on-time deliveries. IDT has on-going vendor TQM programs with suppliers of critical components to ensure on-time delivery of in-spec material. Our manufacturing organization is experienced in building very high-speed boards with tight tolerances and high-pin-count surface-mount components. And our design team is on-call to solve problems quickly if difficulties arise during production. We provide total support—from board design and software porting through production and test—because our success depends on your success!

### Modules

Our modules contain the RISC CPU, Floating Point Accelerator, and all the cache memory. Most include clock control, interrupt and initialization logic, and read and write buffers, as well. All the components are surface-mounted on small, plug-in PC boards, burned-in and tested at the rated speed. All the tricky timing, and high-speed design is done and tested for you. The modules can be plugged into motherboards containing main memory, I/O, and the rest of the system, all of which is relatively low-speed and is easy to lay out using conventional design techniques.

### Custom Subsystems

For custom boards that meet your unique requirements, we can develop a complete product specification, design the boards, deliver prototypes, and provide production units in any quantities. Many customers have found this to be a cost-effective way to augment their own engineering resources, and to procure material that exactly meets their needs without all the headaches of purchasing, material control, and on-going product and manufacturing engineering.

### Printer Controllers

IDT has designed and produced a number of printer controllers, using both custom and standard hardware solutions. IDT's board-level products have been used to run Adobe PostScript™, PCL5 emulation, and Pipeline Associates' color PostScript emulation. IDT is a licensee for Adobe's CPSI interpreter, and can develop a flexible true Adobe solution in a variety of hardware and software environments.

Model	Description
<b>R3000-BASED CPU MODULES</b>	
	<ul style="list-style-type: none"><li>• R3000 Speeds to 40MHz</li><li>• Complete Prototyping and Porting systems available</li><li>• Cache Memory on board up to 256KB each of I and D</li><li>• Multiple CPU Modules</li></ul>
<b>Custom Designs</b>	
	<ul style="list-style-type: none"><li>• Plotter Controllers</li><li>• Add-In Cards to EISA/ISA Bus</li><li>• Add-in Cards for Macintosh</li><li>• Laser Printer Controllers</li></ul>
<b>Software</b>	
	<ul style="list-style-type: none"><li>• Adobe CPSI PostScript Application Development</li><li>• UNIX™ Porting, and Driver Development</li><li>• C-EXECUTIVE™ Real Time OS</li><li>• Interprocessor Communication between RISC Subsystem and Mac or PC</li></ul>

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**TECHNOLOGY AND CAPABILITIES**

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**RISC DEVELOPMENT SUPPORT  
PRODUCTS**

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## IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM, FCT logic, high-density modules, FIFOs, multi-port memories, BiCEMOS™ ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

In 1993, IDT introduced its newest RISC microprocessor based on the MIPS architecture for the desktop PC, and embedded control markets. The R4600 Orion microprocessor, is the first RISC processor offering Pentium performance at a cost lower than most of Intel's 486DX line.

The R4600 is a full 64-bit implementation of the MIPS III instruction set architecture found in the popular R4000PC and R4400PC, but uses a shorter pipeline resulting in fewer stalls and, therefore, higher performance.

When compared against other processors targeted at the Windows NT market, the R4600 possesses clear advantages. The R4600 has the best performance per dollar, the best performance per watt consumed, and the most efficient use of silicon for the performance attained.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

2

## IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant

devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD		SMD		SMD	
<b>SRAM</b>	<b>IDT</b>	5962-93177	7206L	5962-88654	54FCT640/A
84036	6116	5962-92069	72141L	5962-88655	54FCT534/A
5962-88740	6116LA	5962-92101	72215LB	5962-89767	54FCT540/A
84132	6167	5962-93138	72220L	5962-89766	54FCT541/A
5962-86015	7187	5962-92057	72225LB	5962-89733	54FCT191/A
5962-86859	6198/7198/7188	5962-93189	72245LB	5962-89732	54FCT241/A
5962-86705	6168	5962-91757	72200L	5962-89652	54FCT399/A
5962-85525	7164	<b>CLP</b>		5962-89513	54FCT574/A
5962-88552	71256L	<b>IDT</b>		5962-89731	54FCT833A/B
5962-88662	71256S	5962-87708	39C10B & C	5962-89730	54FCT543/A
5962-88611	71682L	5962-88533	49C460A/B/C	5962-90901	29FCT52A/B/C
5962-89891	7198	5962-88613	39C60/A	5962-92205	29FCT520AT/BT/CT
5962-89892	6198	5962-88643	49C410	5962-92157	49FCT805/A/806/A
5962-89690	6116	5962-88673	7216L	5962-92233	54FCT138T/AT/CT
5962-38294	7164	5962-87686	7217L	5962-92208	54FCT157T/AT/CT
5962-89692	7188	5962-88733	7210	5962-92209	54FCT161T/AT/CT
5962-89712	71982	5962-92122	49C465/A	5962-92210	54FCT163T/AT/CT
5962-89790	71682	<b>LOGIC</b>		5962-90669	54FCT193/A
<b>SMP</b>	<b>IDT</b>	<b>IDT</b>		5962-92213	54FCT240T/AT/CT
5962-86875	7130/7140	5962-87630	54FCT244/A	5962-92232	54FCT241T/AT/CT
5962-87002	7132/7142	5962-87629	54FCT245/A	5962-92203	54FCT244T/AT/CT
5962-88610	7133SA/7143SA	5962-88662	54FCT299/A	5962-92214	54FCT245T/AT/CT
5962-88665	7133LA/7143LA	5962-87644	54FCT373/A	5962-92211	54FCT257T/AT/CT
5962-89764	7134	5962-87628	54FCT374/A	5962-92215	54FCT273T/AT/CT
5962-91508	7006	5962-87627	54FCT377/A	5962-92216	54FCT299T/AT/CT
5962-91617	7025	5962-87654	54FCT377/A	5962-92217	54FCT373T/AT/CT
5962-91662	7024	5962-87655	54FCT138/A	5962-92218	54FCT374T/AT/CT
5962-93153	7014S	5962-87656	54FCT240/A	5962-92219	54FCT377T/AT/CT
<b>FIFO</b>	<b>IDT</b>	5962-87656	54FCT273/A	5962-92212	54FCT399T/AT/CT
5962-87531	7201LA	5962-89533	54FCT861A/B	5962-92234	54FCT521T/AT/BT/CT
5962-86846	72404L	5962-89506	54FCT827A/B	5962-92236	54FCT534T/AT/CT
5962-88669	7203S	5962-88575	54FCT841A/B	5962-92220	54FCT540T/AT/CT
5962-89568	7204L	5962-88608	54FCT821A/B	5962-92237	54FCT541T/AT/CT
5962-89536	7202LA	5962-88543	54FCT521/A	5962-92221	54FCT543T/AT/CT
5962-89863	7201SA	5962-88640	54FCT161/A	5962-92238	54FCT573T/AT/CT
5962-89523	72403L	5962-88639	54FCT573/A	5962-92222	54FCT574T/AT/CT
5962-89666	7200L	5962-88656	54FCT823A/B	5962-92244	54FCT645T/AT/CT
5962-89942	72103L	5962-88657	54FCT163/A	5962-92223	54FCT646T/AT/CT
5962-89943	72104L	5962-88674	54FCT825A/B	5962-92246	54FCT652T/AT/CT
5962-89567	7203L	5962-88661	54FCT863A/B	5962-92225	54FCT821AT/BT/CT
5962-90715	7204S	5962-88736	29FCT520A/B	5962-92229	54FCT823AT/BT/CT
5962-91677	7205L	5962-88775	54FCT646/A	5962-92230	54FCT825AT/BT/CT
		5962-89508	54FCT139/A	5962-92247	54FCT827AT/BT/CT
		5962-89665	54FCT824A/B		
		5962-88651	54FCT533/A		
		5962-88653	54FCT645/A		

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## RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house

on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

2

# IDT LEADING EDGE CEMOS TECHNOLOGY

## HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity

and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective ( $L_{eff}$ ) gate lengths by more than 60 percent from 1.3 microns (millionths of a meter) in 1981 to 0.45 microns in 1993.

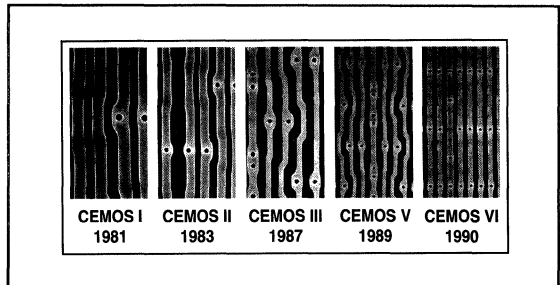
	CEMOS I	CEMOS II		CEMOS III	CEMOS V	CEMOS VI	CEMOS VII	
		A	C				V <sub>CC</sub> = 5V	V <sub>CC</sub> = 3.3V
Calendar Year	1981	1983	1985	1987	1989	1990	1992	1993
Drawn Feature Size	2.5 $\mu$	1.7 $\mu$	1.3 $\mu$	1.2 $\mu$	1.0 $\mu$	0.8 $\mu$	0.65 $\mu$	0.65 $\mu$
$L_{eff}$	1.3 $\mu$	1.1 $\mu$	0.9 $\mu$	0.8 $\mu$	0.6 $\mu$	0.45 $\mu$	0.45 $\mu$	0.25 $\mu$
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III	BiCEMOS IV V <sub>CC</sub> = 5V	BiCEMOS IV V <sub>CC</sub> = 3.3V

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization)

2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

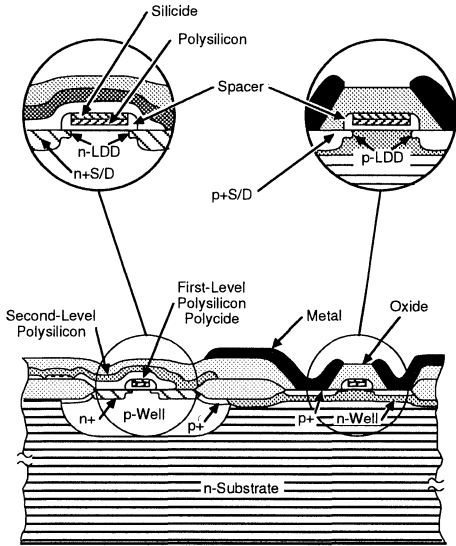


Figure 3. IDT CEMOS Device Cross Section

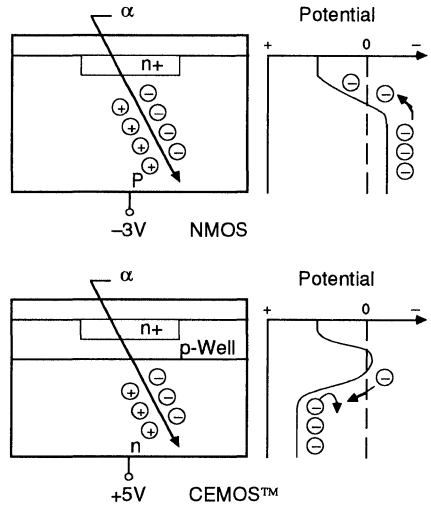


Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

**ALPHA PARTICLES**

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

**LATCHUP IMMUNITY**

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

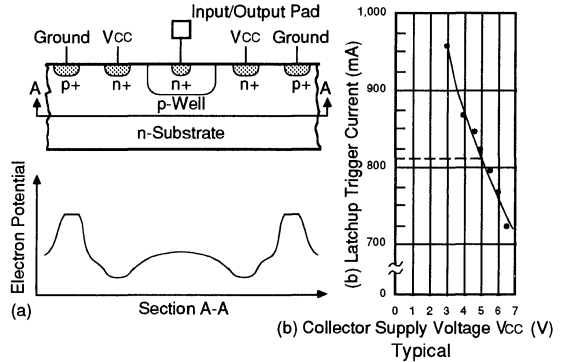


Figure 5. IDT CEMOS Latchup Suppression

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## SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20-60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high performance modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output .

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

- 1) the low power characteristics of IDT's CMOS and BiCMOS products,
- 2) the density advantages of first class SMD components including those from IDT's components divisions, and
- 3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

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## STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of “Silicon Valley.” The company’s operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products’ test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT’s Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of “innovation,” these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseat operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface-mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT’s largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT’s second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT’s leadership family of CMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT’s facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

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## SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883, paragraph 1.2.1.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC,

functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

### SPECIAL PROGRAMS

**Class S.** IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

**Radiation Hardened.** IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

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**GENERAL INFORMATION**

**1**

**TECHNOLOGY AND CAPABILITIES**

**2**

**QUALITY AND RELIABILITY**

**3**

**PACKAGE DIAGRAM OUTLINES**

**4**

**RISC PROCESSING COMPONENTS**

**5**

**RISC SUPPORT COMPONENTS**

**6**

**RISC DEVELOPMENT SUPPORT  
PRODUCTS**

**7**

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## QSP—QUALITY, SERVICE AND PERFORMANCE

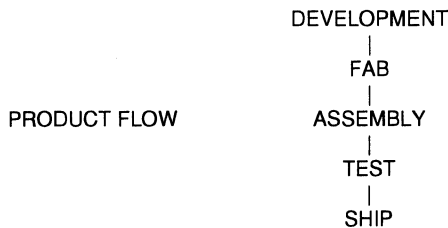
Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Total Quality Commitment (TQC) process. Everyone who influences the quality of the product—from the designer to the shipping clerk—is committed to constantly improving the quality of their actions.

### IDT QUALITY PHILOSOPHY

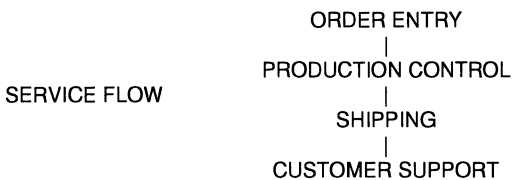
*"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."*

### IDT's ASSURANCE STRATEGY FOR TQC

Measurable standards are essential to the success of TQC. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.



These systems and controls concentrate on TQC by focusing on the following key elements:

### Statistical Techniques

Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/processes are under control.

### Standardization

Implementing policies, procedures and measurement techniques that are common across different operational areas.

### Documentation

Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

### Productivity Improvement

Using constant improvement teams made up from employees at all levels of the organization.

### Leadership

Focusing on quality as a key business parameter and strategic strength.

### Total Employee Participation

Incorporating the TQC process into the IDT Corporate Culture.

### Customer Service

Supporting the customer, as a partner, through performance review and pro-active problem solving.

### People Excellence

Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

### PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

### Manufacturing

To accomplish continuous improvement during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

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In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

### **Inventory and Shipping**

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

### **SERVICE FLOW**

Quality not only applies to the product but to the quality -of-service we give our customers. Services is also constantly monitored for improvement.

### **Order Procedures**

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the TQC process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

### **Production Control**

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

- Quotation response and accuracy.
- Scheduling response and accuracy.
- Response and accuracy of Expedites.
- Inventory, management, and effectiveness.
- On time delivery.

### **Customer Support**

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to continuous improvement is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle—full support of our customers and their designs with high-quality products.

### **SUMMARY**

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our customers will be successful in the coming decade. With the implementation of the TQC strategy within the company, we will satisfy our goal...

*"Leadership through Quality, Service and Performance Products"*.

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## IDT QUALITY CONFORMANCE PROGRAM

### A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

### SUMMARY

#### Monolithic Hermetic Package Processing Flow<sup>(1)</sup>

Refer to the *Monolithic Hermetic Package Processing Flow diagram*. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.
3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.
5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.
6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.
7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.
8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.
10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.
11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.
12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

#### NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

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## SUMMARY

### Monolithic Plastic Package Processing Flow

*Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.*

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.
3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.
4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.
5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.
7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.
9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.
10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.
11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

**TABLE 1**

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

**Monolithic Hermetic Package Final Processing Flow**

OPERATION	CLASS-S		CLASS-B		CLASS-C <sup>(1)</sup>	
	TEST METHOD	RQMT	TEST METHOD	RQMT	TEST METHOD	RQMT
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min. or equivalent	100%	Per applicable device specification	100%
PORT BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable <sup>(2)</sup> device specification	100%
Group A ELECTRICAL: Static (DC, Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable <sup>(2)</sup> device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D	Sample	5005 Group B, C, D	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

**NOTES:**

1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

**3**



# RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

## INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

## THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

*Total Dose Accumulation* refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (Si) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

*Burst Radiation or Dose Rate* refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

*Single Event Upset (SEU)* is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

*Neutron Irradiation* will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

## DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

## RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant (RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each RE or RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level

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tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan. Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

## CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications. Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.



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GENERAL INFORMATION

1

TECHNOLOGY AND CAPABILITIES

2

QUALITY AND RELIABILITY

3

**PACKAGE DIAGRAM OUTLINES**

4

RISC PROCESSING COMPONENTS

5

RISC SUPPORT COMPONENTS

6

RISC DEVELOPMENT SUPPORT  
PRODUCTS

7

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## THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T<sub>J</sub>), it becomes increasingly important to maintain a low (T<sub>J</sub>).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_0 \exp \left[ \frac{E_a}{k} \left( \frac{1}{T_0} - \frac{1}{T_J} \right) \right]$$

where

t<sub>A</sub> = lifetime at elevated junction (T<sub>J</sub>) temperature  
 t<sub>0</sub> = normal lifetime at normal junction (T<sub>0</sub>) temperature  
 E<sub>a</sub> = activation energy (ev)  
 k = Boltzmann's constant (8.617 x 10<sup>-5</sup>ev/k)  
 i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.

4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883<sub>C</sub> to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T<sub>J</sub>), it is necessary to know the thermal resistance of the package (θ<sub>JA</sub>) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$

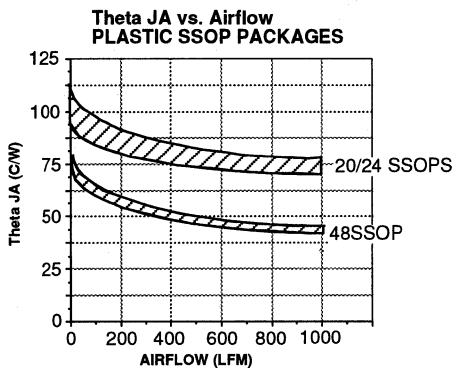
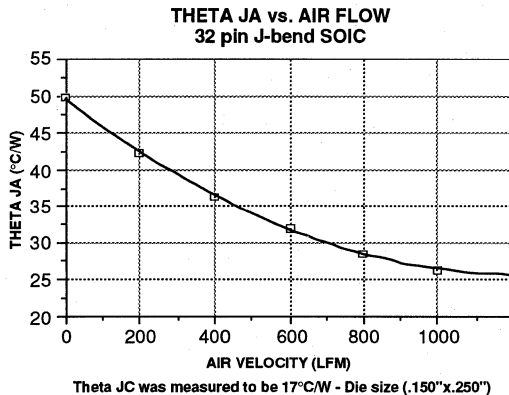
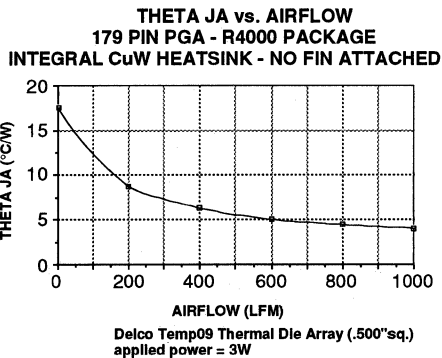
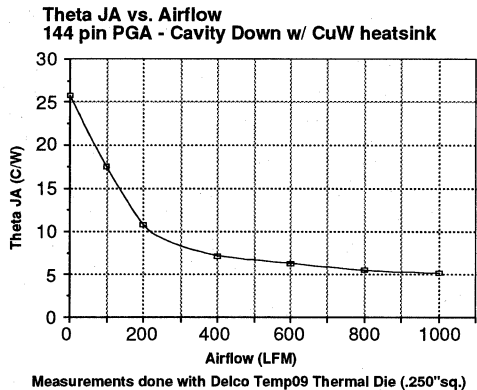
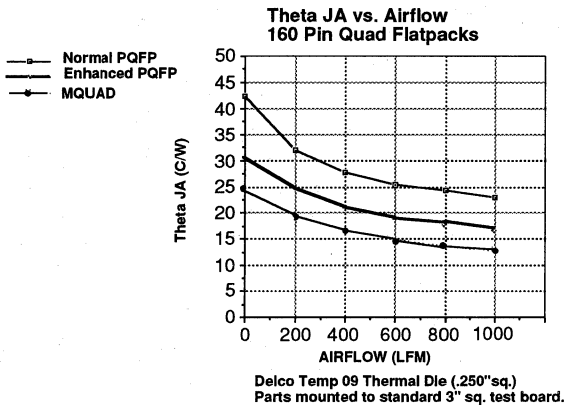
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

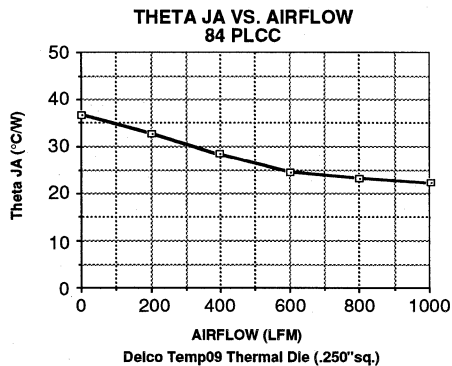
$$\theta_{JC} = \frac{T_J - T_C}{P}$$

$$\theta_{CA} = \frac{T_C - T_A}{P}$$

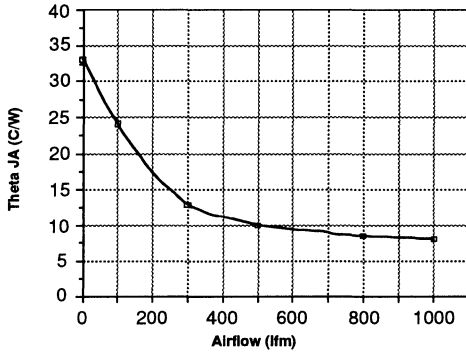
θ = Thermal resistance  
 J = Junction  
 P = Operational power of device (dissipated)  
 T<sub>A</sub> = Ambient temperature in degree celsius  
 T<sub>J</sub> = Temperature of the junction  
 T<sub>C</sub> = Temperature of case/package  
 θ<sub>CA</sub> = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.  
 θ<sub>JC</sub> = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)  
 θ<sub>JA</sub> = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ<sub>JC</sub> + θ<sub>JA</sub> which includes the influence of area and environmental condition.)



THETA JC : 20/24 PIN = 35-40 °C/W  
48 PIN = 16-20 °C/W

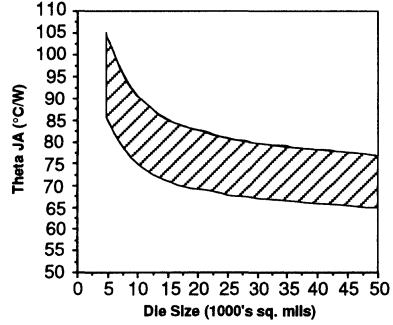


**Theta JA vs. Airflow**  
**84 pin PGA - Cavity Down w/CuW heatsink**

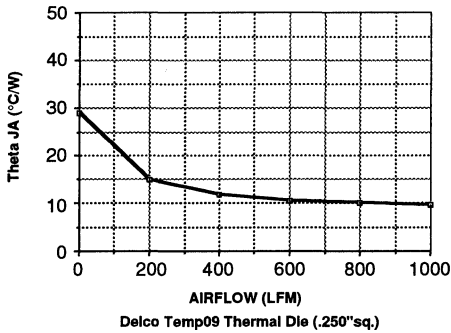


Measurements were done using Temp09 Delco Thermal Die (.250sq.)

**Theta JA - Still Air 16-20 Lead Ceramic Dips**

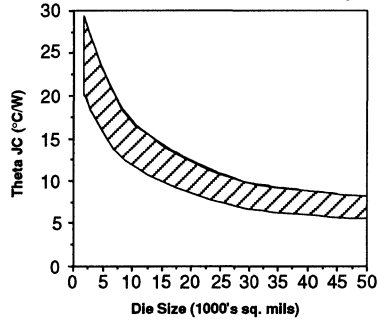


**GD 208 THETA JA VS. AIRFLOW**

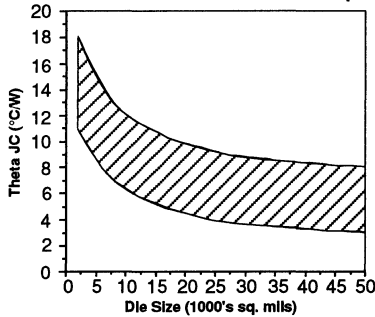


Delco Temp09 Thermal Die (.250"sq.)

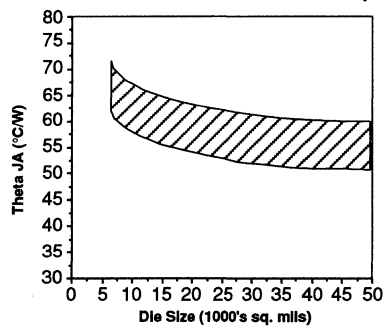
**Theta JC 16-20 Lead Ceramic Dip**



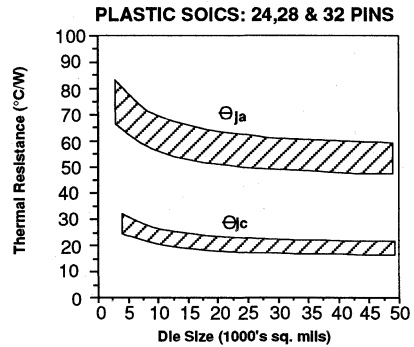
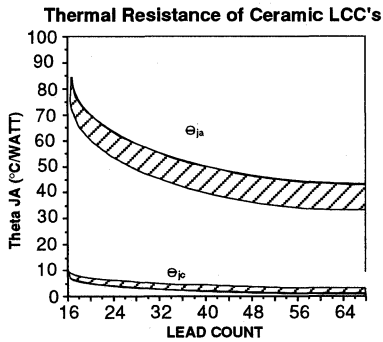
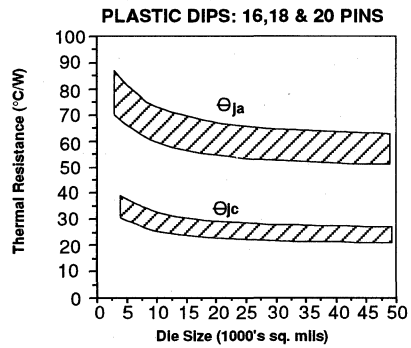
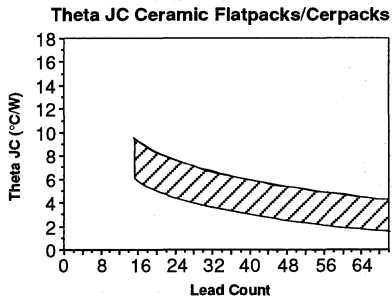
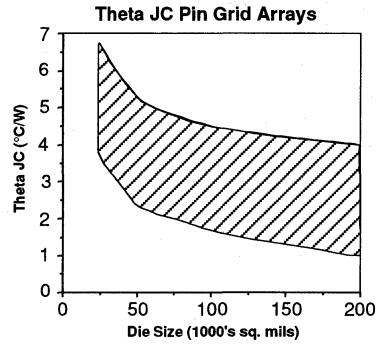
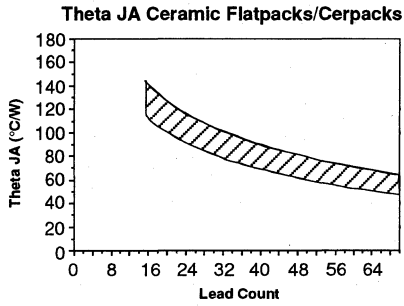
**Theta JC 22-40 Lead Ceramic Dips**

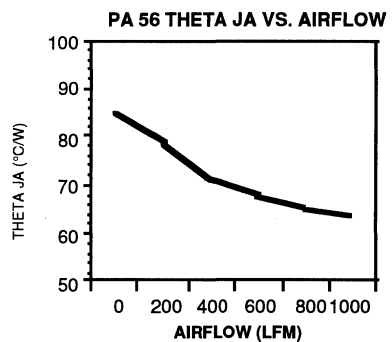
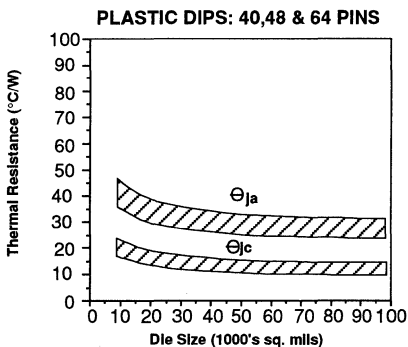
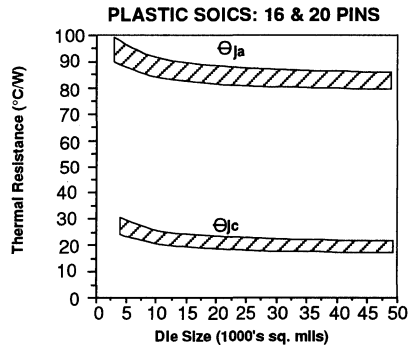
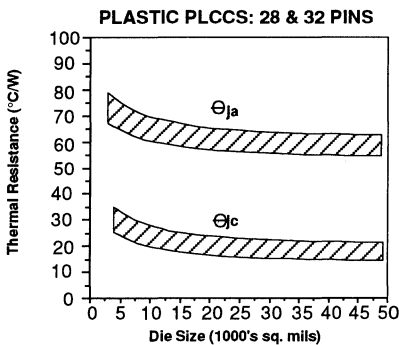
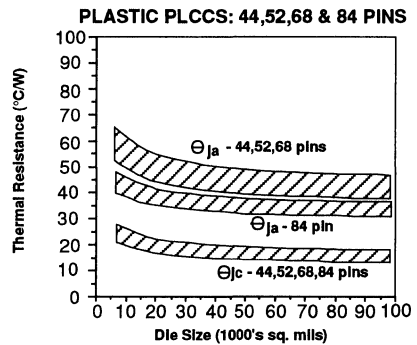
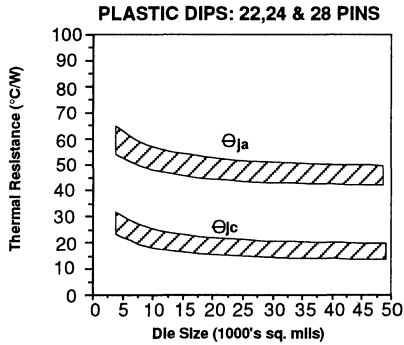


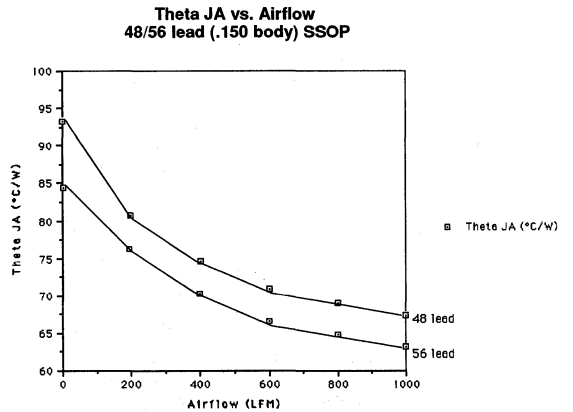
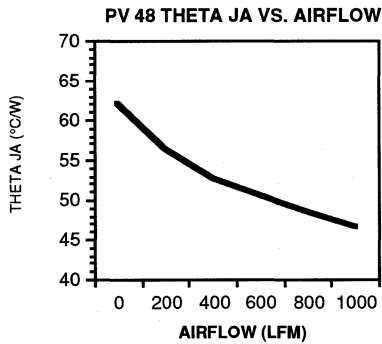
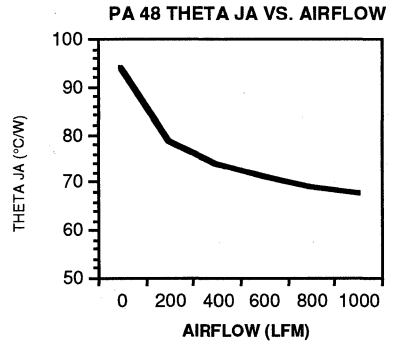
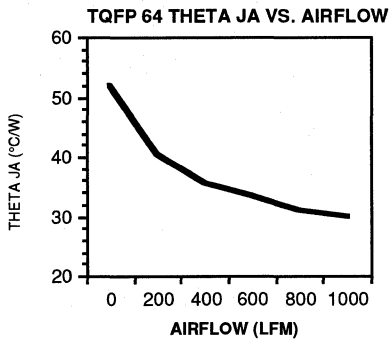
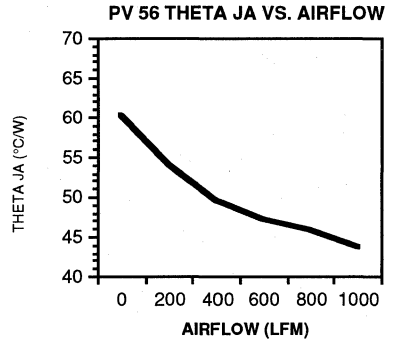
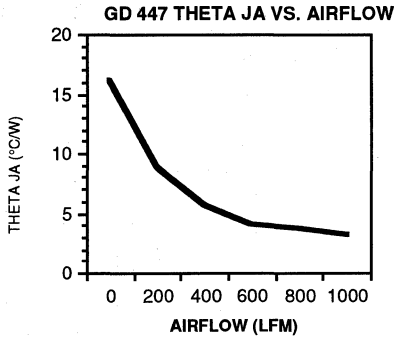
**Theta JA - Still Air 22-40 Ceramic Dips**



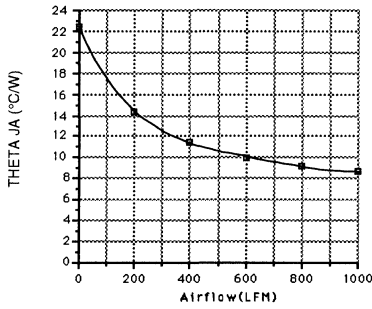






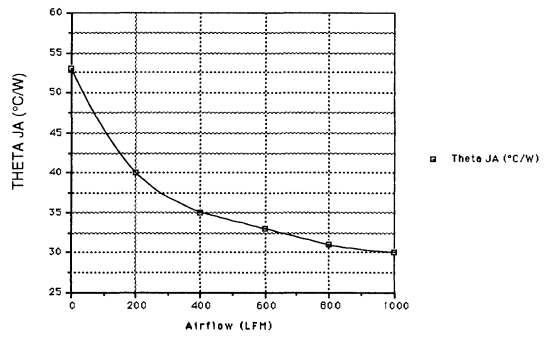


**Theta JA vs. Airflow**  
**84/160/208 lead MQUAD flatpack**  
**28mm body**

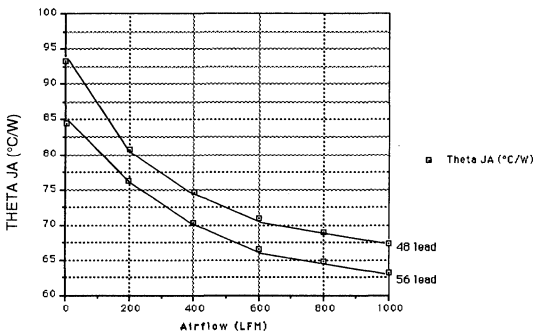


This data is with all leads soldered. .250"sq. Delco Temp09 thermal die.

**Theta JA vs. Airflow**  
**64/80/100 lead Thin Quad Flatpack**  
**(14mm body)**



**Theta JA vs. Airflow**  
**48/56 lead (.150 body) SSOP**



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## PACKAGE DIAGRAM OUTLINE INDEX

SECTION PAGE

### MONOLITHIC PACKAGE DIAGRAM OUTLINES .....4.3

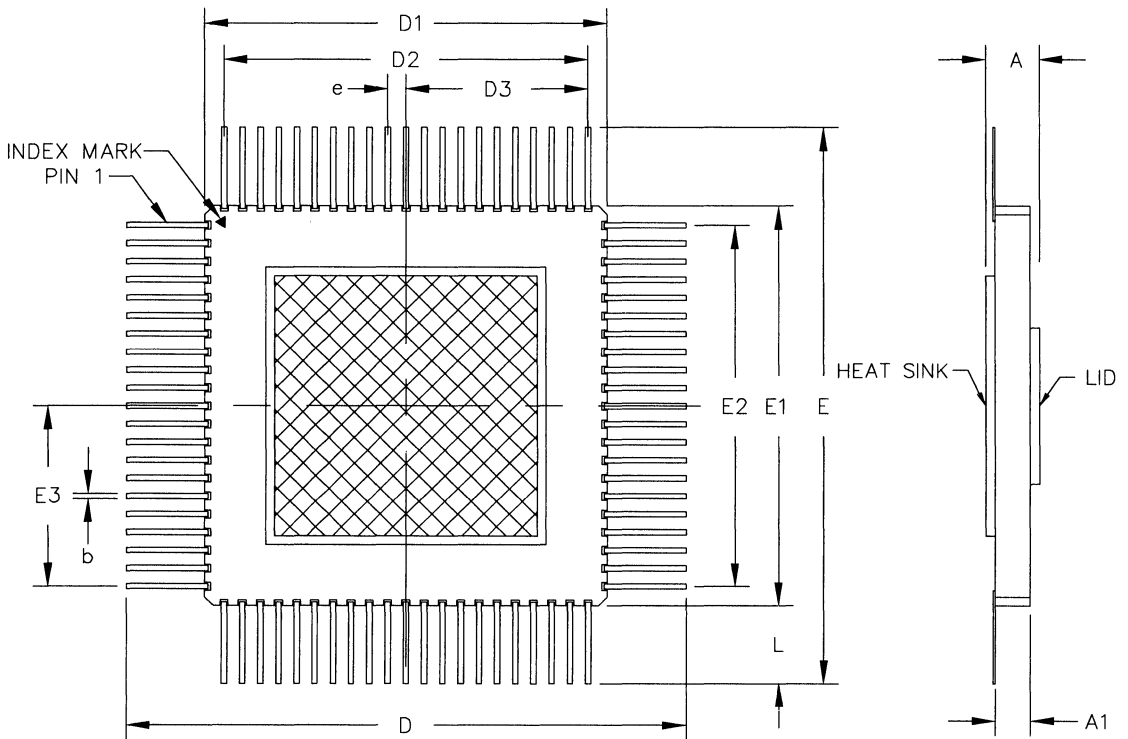
PKG.	DESCRIPTION	
F84-1	84-Lead Quad Flatpack (cavity down) .....	1
F84-2	84-Lead Quad Flatpack (cavity up) .....	2
CQ84-1	84-Lead CERQUAD .....	3
G84-4	84-Lead Pin Grid Array (cavity down—R3010A) .....	4
G179-1	179-Lead Pin Grid Array (cavity down) .....	5
G447-1	447-Lead Pin Grid Array (cavity down) .....	6
G447-2	447-Lead Pin Grid Array (cavity down) .....	7
PN100-1	100 Lead Thin Quad Flatpack .....	8
M84-1	84-Lead MQUAD™ (J-bend, cavity down) .....	9
M160-1	160-Lead MQUAD™ (cavity down) .....	10
M208-1	208-LeadMQUAD™ (cavity down) .....	11
J68-1	68-Pin Plastic Leaded Chip Carrier (square) .....	12
J84-1	84-Pin Plastic Leaded Chip Carrier (square) .....	12

### MODULE PACKAGE DIAGRAM OUTLINES

Module package diagrams are located at the back of each Subsystems data sheet.

FLATPACKS

84 LEAD QUAD FLATPACK (CAVITY DOWN)



4

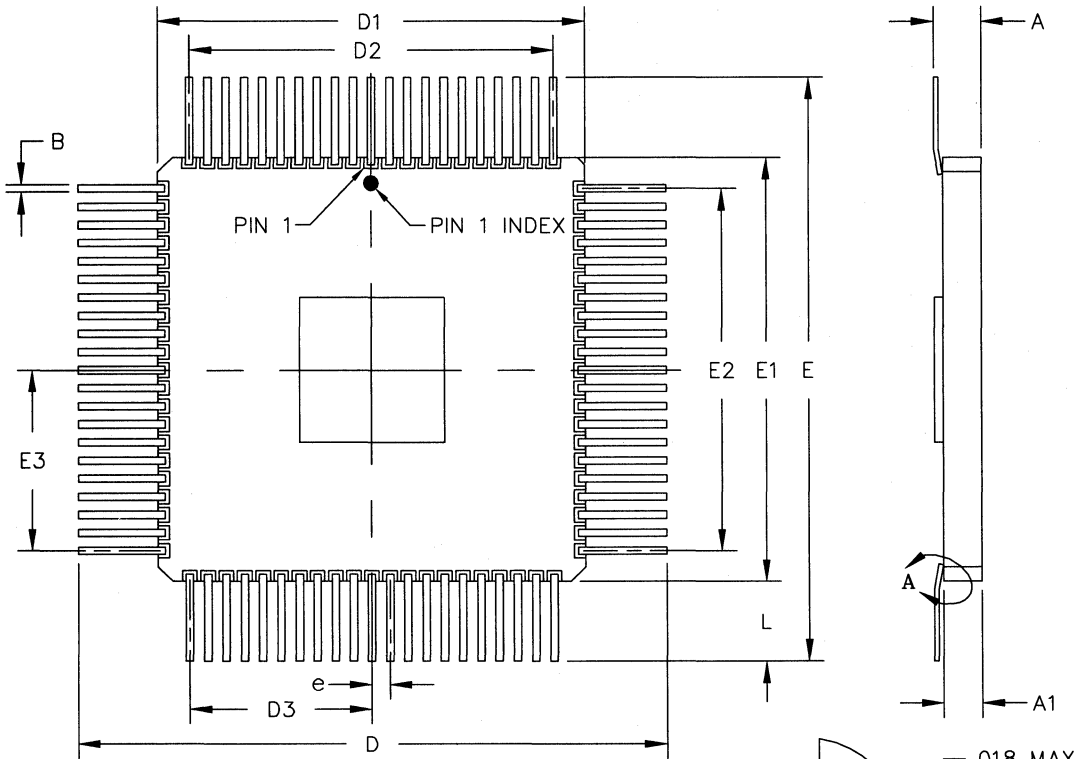
DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	-	.135
A1	-	.105
b	.014	.020
C	.007	.011
D/E	1.940	1.960
D1/E1	1.140	1.160
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.390	.410
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY UP)



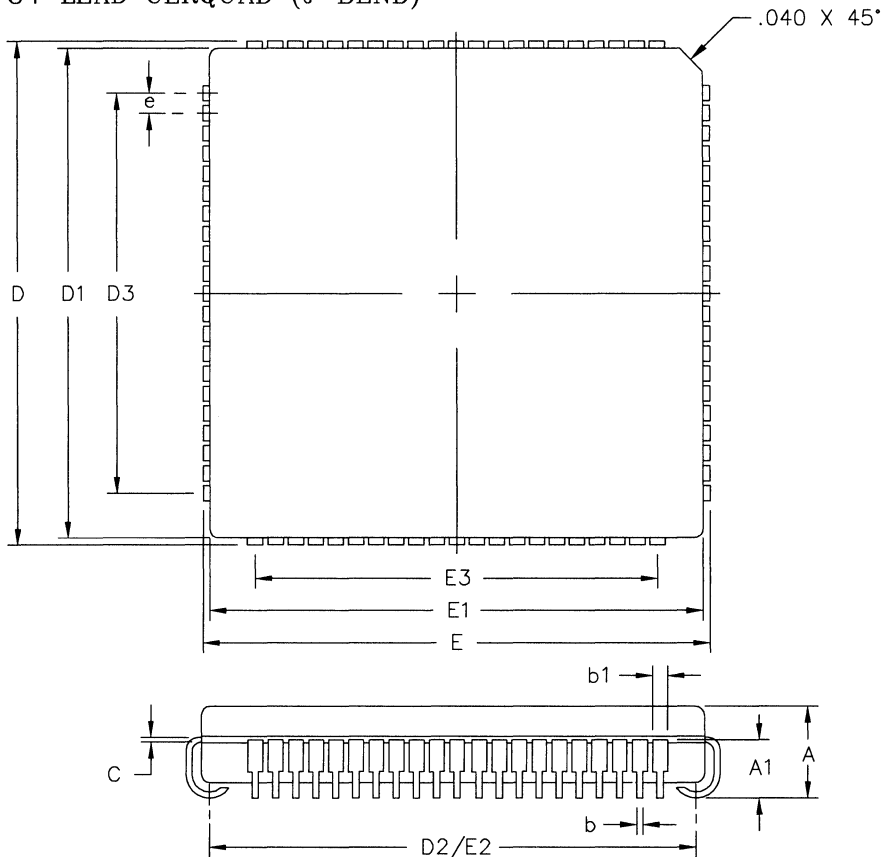
DWG #	F84-2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	-	.140
A1	-	.105
b	.014	.020
C	.007	.013
D/E	1.940	1.960
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.

CERQUADS

84 LEAD CERQUAD (J-BEND)



DWG #	CQ84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	.1.150
D3/.E3	1.000 BSC	
e	.050 BSC	
ND/NE	21	

NOTES:

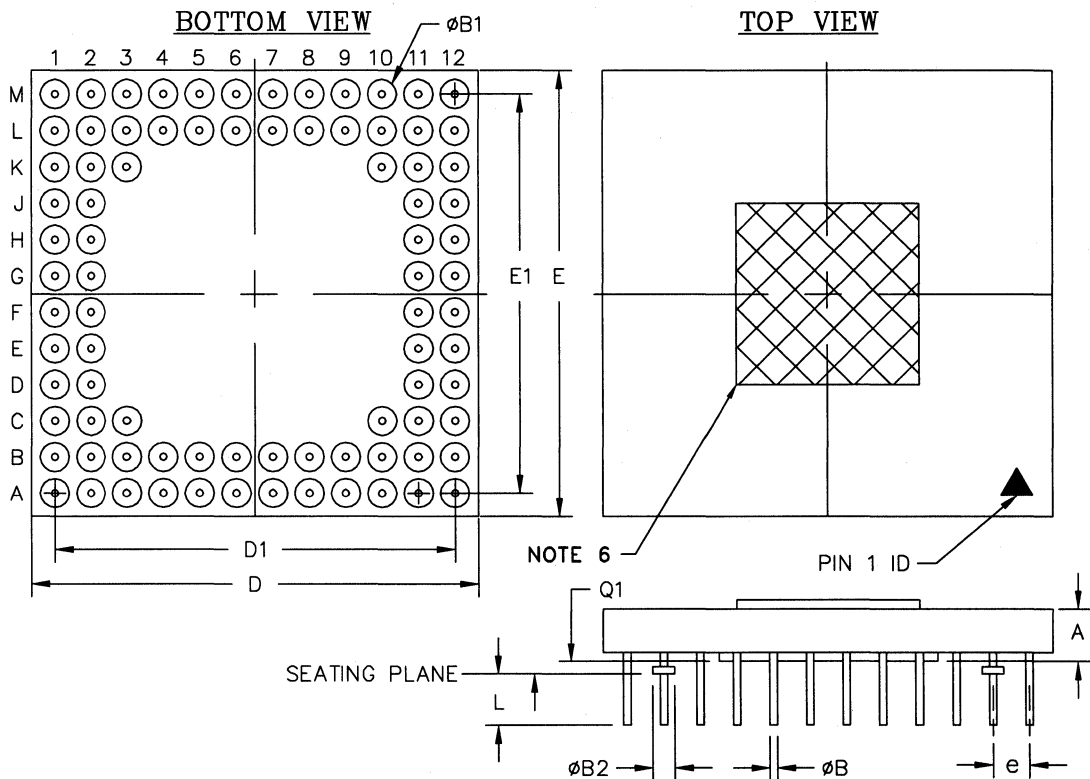
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.

4



PIN GRID ARRAYS

84 PIN PGA (CAVITY DOWN - R3010A)



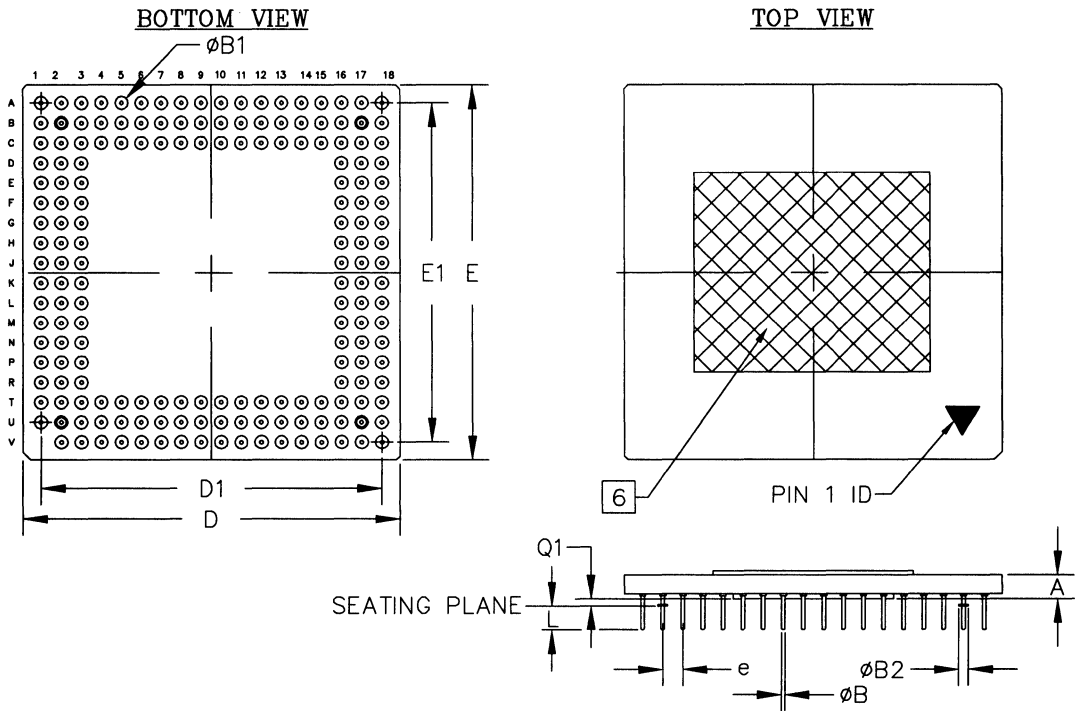
DWG #	G84-4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
$\phi B$	.016	.020
$\phi B1$	.060	.080
$\phi B2$	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

179 PIN PGA (CAVITY DOWN)



DWG #	G179-1	
# OF PINS (N)	179	
SYMBOL	MIN	MAX
A	.082	.145
$\phi B$	.016	.020
$\phi B1$	.060	.080
$\phi B2$	.040	.060
D/E	1.840	1.880
D1/E1	1.700 BSC	
e	.100 BSC	
L	.120	.140
M	18	
Q1	.025	.060

NOTES: (UNLESS OTHERWISE SPECIFIED)

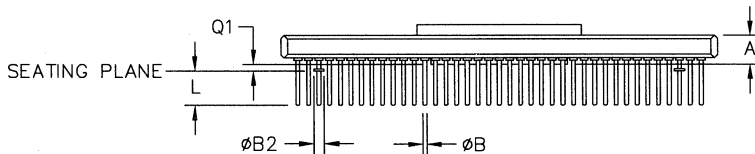
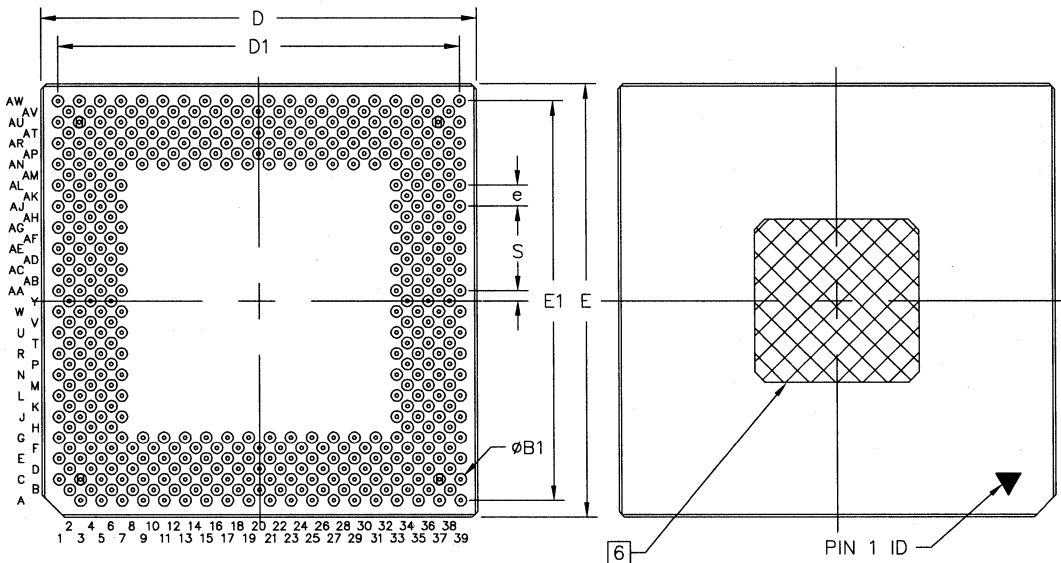
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERED CORNERS ARE IDT'S OPTION.
- [6] CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

PIN GRID ARRAYS (Continued)

447 PIN PGA (CAVITY DOWN)

BOTTOM VIEW

TOP VIEW



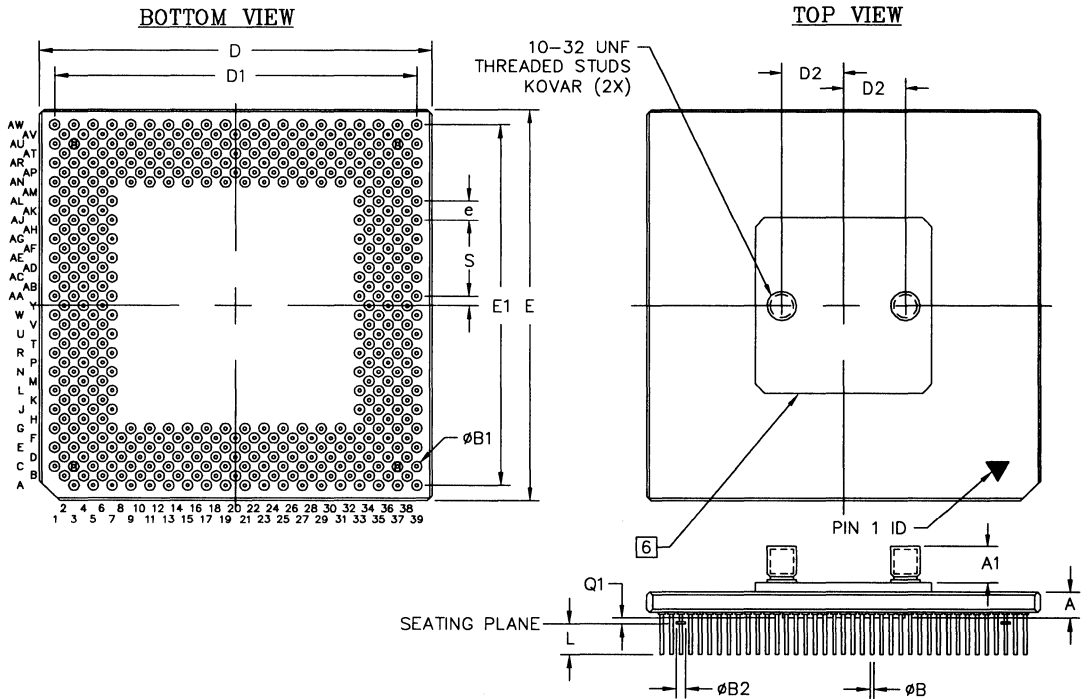
DWG #	G447-1	
# OF PINS (N)	447	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	.050	.060
ØB2	.045	.055
D/E	2.040	2.080
D1/E1	1.900 BSC	
e	.100 BSC	
L	.120	.140
M	39	
Q1	.025	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.
- 6 CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

PIN GRID ARRAYS (Continued)

447 PIN PGA WITH STUDS (CAVITY DOWN)



4

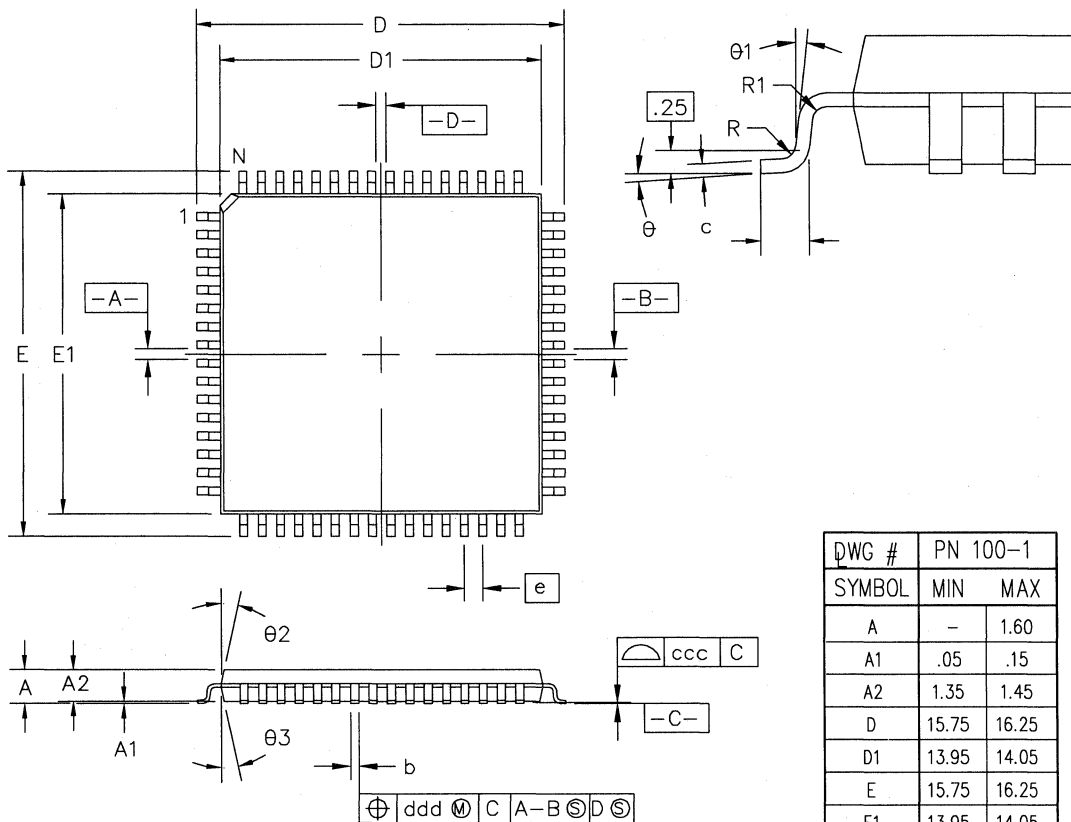
DWG #	G447-2	
# OF PINS (N)	447	
SYMBOL	MIN	MAX
A	.070	.145
A1	.245	.255
$\phi B$	.016	.020
$\phi B1$	.050	.060
$\phi B2$	.045	.055
D/E	2.040	2.080
D1/E1	1.900 BSC	
D2	.420	.430
e	.100 BSC	
L	.120	.140
M	39	
Q1	.025	.060
S	.050 BSC	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
  2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
  3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
  4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
  5. CHAMFERRED CORNERS ARE IDT'S OPTION.
- [6] THIS AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PLASTIC QUAD FLATPACKS

100 LEAD TQFP



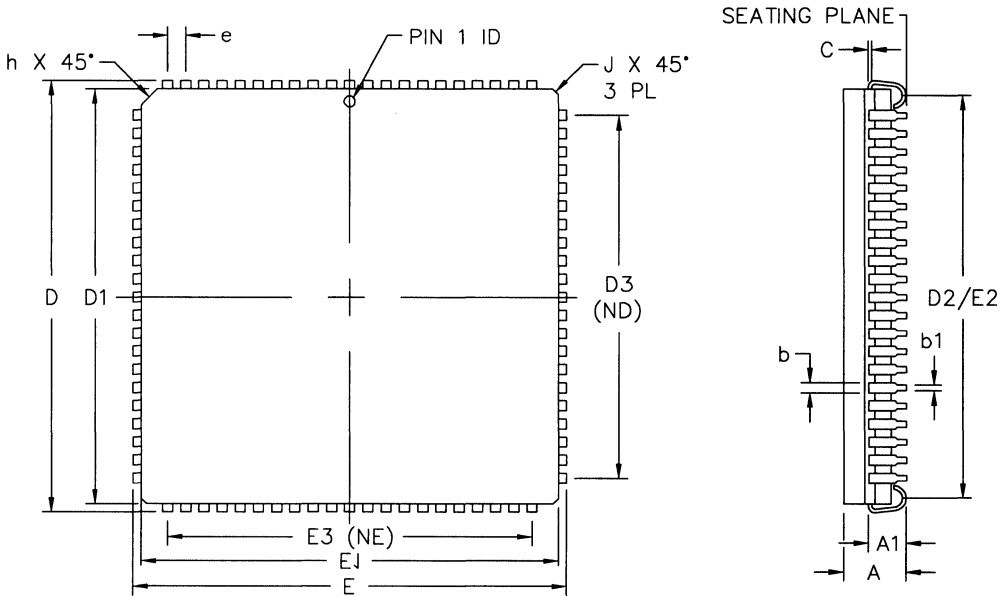
DWG #	PN 100-1	
SYMBOL	MIN	MAX
A	-	1.60
A1	.05	.15
A2	1.35	1.45
D	15.75	16.25
D1	13.95	14.05
E	15.75	16.25
E1	13.95	14.05
L	.45	.70
N	100	
e	.50 BSC	
b	.17	.27
ccc	-	.08
ddd	-	.08
R	.08	.20
R1	.08	-
$\theta$	0°	7°
$\theta_1$	2°	10°
$\theta_2$	11°	13°
$\theta_3$	11°	13°
c	.09	.16

NOTES:

1. ALL DIMENSIONS ARE IN MELLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PACKAGE. ALLOWABLE PROTRUSION TO BE .254 PER SIDE.

MQUADS <sup>®</sup>

84 LEAD MQUAD (J-BEND, CAVITY DOWN)



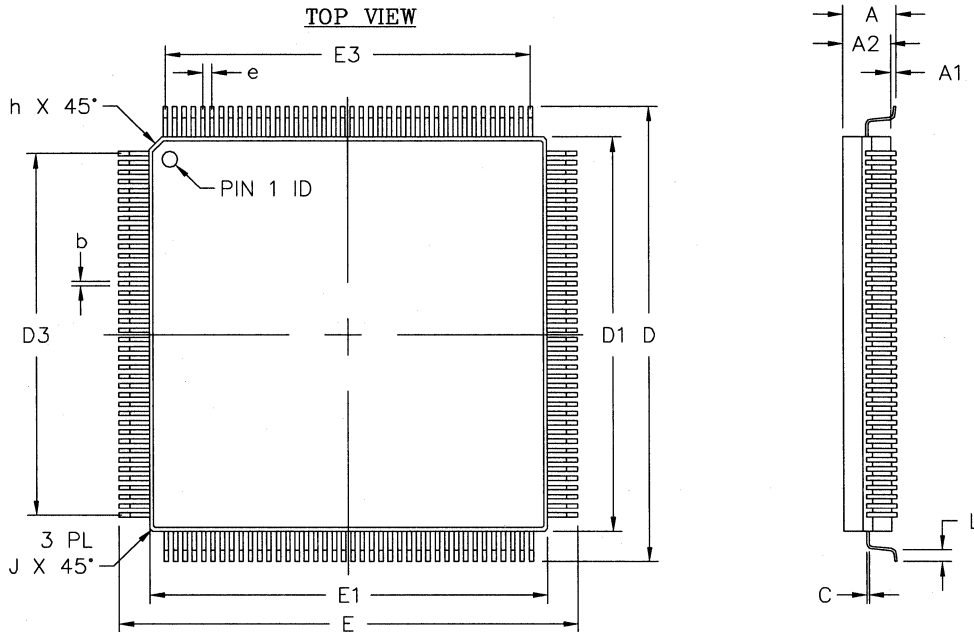
DWG #	M84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.165	.180
A1	.094	.114
b	.026	.032
b1	.013	.021
C	.008	.012
D/E	1.185	1.195
D1/E1	1.140	1.150
D2/E2	1.090	1.130
D3/E3	1.000 BSC	
e	.050 BSC	
h	.045 REF	
J	.015 REF	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
4. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

MQUADS<sup>®</sup> (Continued)

160 LEAD MQUAD (CAVITY DOWN)



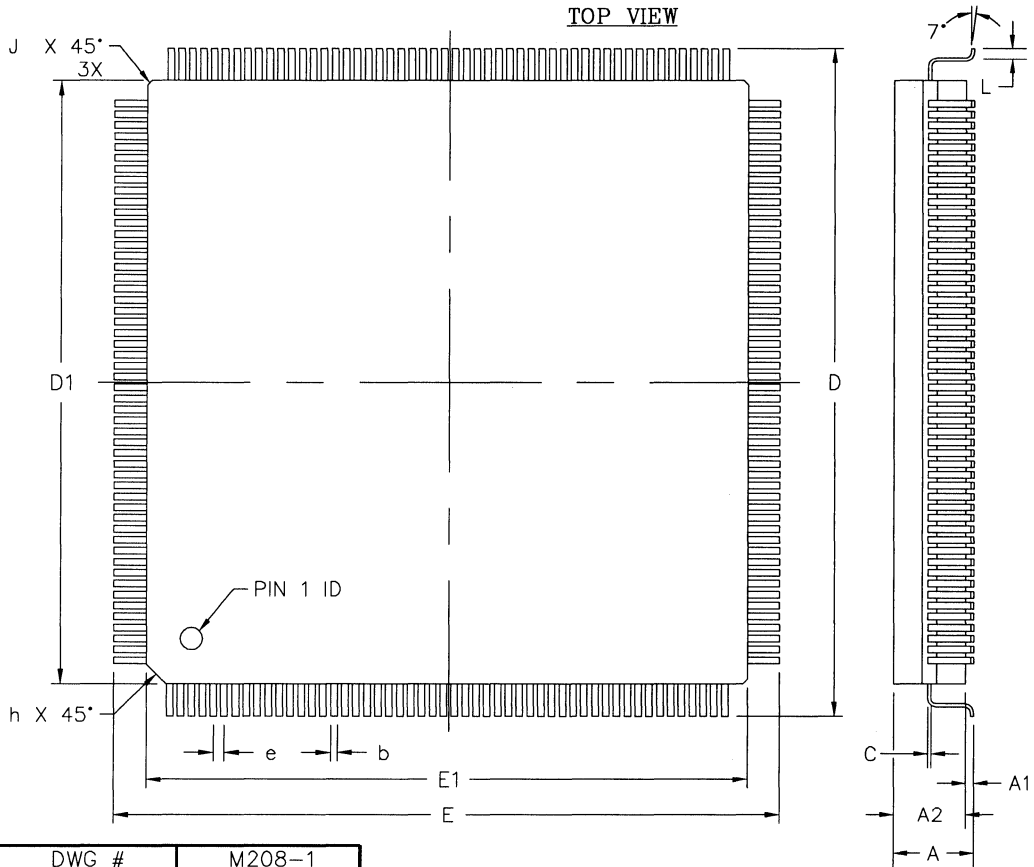
DWG #	M160-1	
# OF LDS (N)	160	
SYMBOL	MIN	MAX
A	3.50	3.86
A1	.25	.51
A2	3.17	3.43
b	.22	.35
C	.13	.20
D/E	31.70	32.10
D1/E1	27.56	27.72
D3/.E3	25.35 BSC	
e	.65 BSC	
h	.89 REF	
J	.20 REF	
L	.67	.93
ND/NE	40	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 SHOULD BE MEASURED FORM THE BOTTOM OF THE PACKAGE.
4. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

MQUADS <sup>®</sup> (Continued)

208 LEAD MQUAD (CAVITY DOWN)



DWG #	M208-1	
# OF LDS (N)	208	
SYMBOL	MIN	MAX
A	3.50	3.86
A1	.25	.51
A2	3.17	3.43
b	.22	.35
C	.13	.20
D/E	30.50	30.70
D1/E1	27.59	27.79
e	.50 BSC	
h	.89 REF	
J	.20 REF	
L	.40	.60
ND/NE	52	

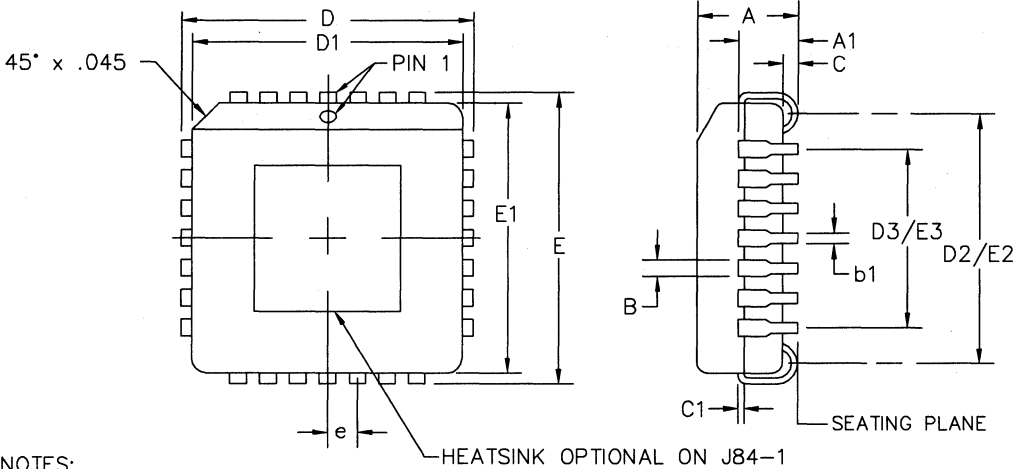
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 SHOULD BE MEASURED FORM THE BOTTOM OF THE PACKAGE.
4. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.



PLASTIC LEADED CHIP CARRIERS

20-84 LEAD PLCC (SQUARE)



NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J68-1		J84-1	
# OF LDS	68		84	
SYMBOL	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180
A1	.095	.115	.095	.115
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	.985	.995	1.185	1.195
D1	.950	.956	1.150	1.156
D2/E2	.890	.930	1.090	1.130
D3/E3	.800	REF	1.000	REF
E	.985	.995	1.185	1.195
E1	.950	.956	1.150	1.156
e	.050	BSC	.050	BSC
ND/NE	17		21	

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GENERAL INFORMATION

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IDT79R3051™/79R3052™	IDT79R3051/79R3052 Integrated RISCControllers .....	5.3
IDT79R3071™	IDT79R3071 RISCController .....	5.4
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Integrated Device Technology, Inc.

# RISC CPU CORE

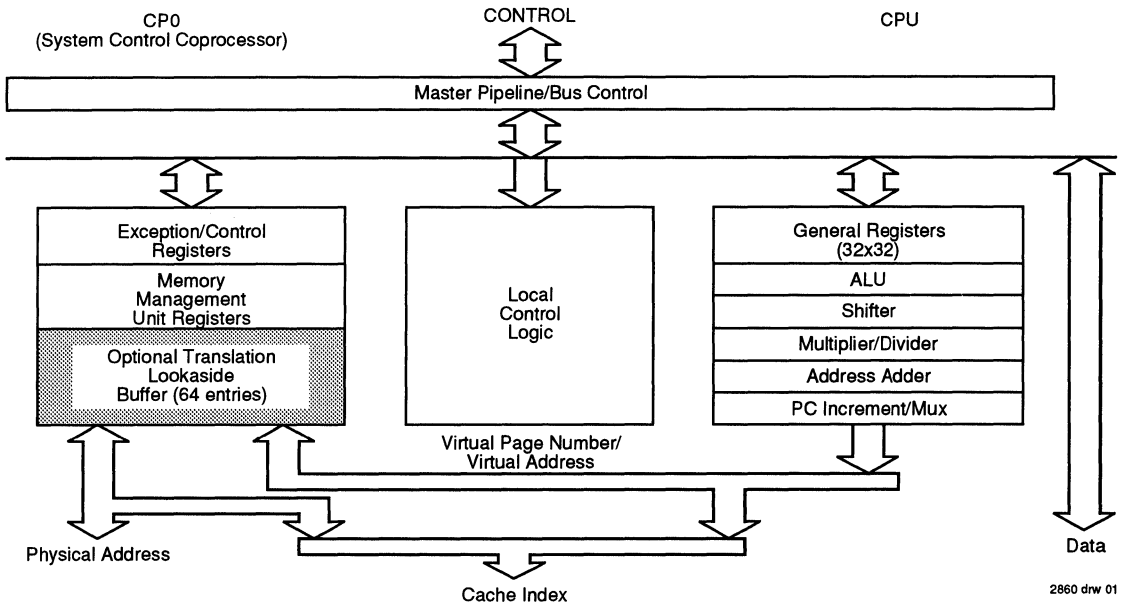
## R3000A Core for RISController Devices

### FEATURES:

- Enhanced instruction set compatible R3000A Core for integrated RISControllers
- Integrates well with R3010A Core Hardware Floating Point Accelerator
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- Integrated Cache Control for On-Chip Caches—The CPU core contains a high-bandwidth memory interface that handles separate Instruction and Data Caches. Both caches are accessed during a single CPU cycle. All cache control is integrated into the core, allowing high-speed execution.
- "E" versions feature Memory Management Unit, including a fully-associative, 64-entry Translation Look-aside Buffer (TLB). This provides fast address translation for virtual-to-physical memory mapping of the 4GB virtual address space.
- Dynamically able to switch between Big- and Little-Endian byte ordering conventions.
- Software compatible with all R3000 devices. This insures a wide range of development support, including compilers, operating systems, libraries, and applications software.
- High-speed 0.6µ CMOS technology.
- 50MHz clock rates yield up to 40VUPS sustained throughput.
- Supports independent multi-word block refill of both the instruction and data caches.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs, 2 software interrupts, with single cycle latency to exception handler routine.

5

### R3000A CORE BLOCK DIAGRAM



2860 drw 01

The IDT logo is a registered trademark and Orion, R3041, R3051, R3052, R3081, R3721, R4600, RISCCompiler, RISController, RISCCore, RISC Subsystem, and RISC Windows are trademarks of Integrated Device Technology, Inc.

**DESCRIPTION**

The R3000A RISC Microprocessor Core consists of two tightly-coupled processors. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor price/performance. The second processor is a system control coprocessor, called CP0, containing an optional fully-associative 64-entry TLB (Translation Look-aside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4GB virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 400MB/second using integrated cache memory.

**This data sheet provides an overview of the features and architecture of the R3000A core. This core is integrated into various members of the IDT RISController family, such as the R3041, R3051, and R3081. Detail on those specific devices is found in separate data sheets and user's manuals.**

**R3000A CPU Registers**

The R3000A CPU provides 32 general-purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers which hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hard-wired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the Status and Cause registers incorporated within the System Control Coprocessor (CP0).

**Instruction Set Overview**

All R3000A instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction

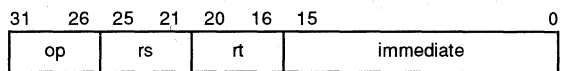
decoding, thus minimizing instruction execution time. The R3000A core initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions.

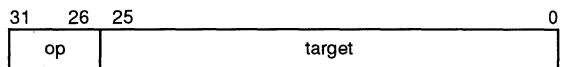
The R3000A instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

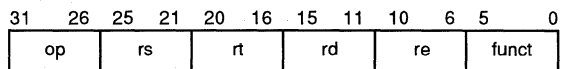
I-Type (Immediate)



J-Type (Jump)



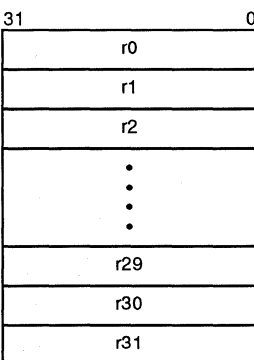
R-Type (Register)



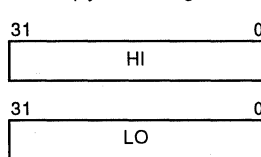
2860 drw 03

**Figure 3. R3000A Instruction Formats**

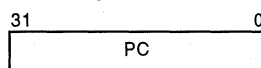
General Purpose Registers



Multiply/Divide Registers



Program Counter



2860 drw 02

**Figure 2. R3000A CPU Registers**

The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

Loads and Stores can be performed on byte, half-word, word, or non-aligned word data (32-bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.

- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats. Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two

operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The R3000A instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.
- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.



## R3000A INSTRUCTION SUMMARY

OP	Description	OP	Description
	<b>Load/Store Instructions</b>		<b>Multiply/Divide Instructions</b>
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HIGH
LWL	Load Word Left	MTHI	Move To HIGH
LWR	Load Word Right	MFLO	Move From LOW
SB	Store Byte	MTLO	Move To LOW
SH	Store Halfword		
SW	Store Word		
SWL	Store Word Left	J	<b>Jump and Branch Instructions</b> Jump
SWR	Store Word Right	JAL	Jump and Link
		JR	Jump to Register
	<b>Arithmetic Instructions (ALU Immediate)</b>	JALR	Jump and Link Register
ADDI	Add Immediate	BEQ	Branch on Equal
ADDIU	Add Immediate Unsigned	BNE	Branch on Not Equal
SLTI	Set on Less Than Immediate	BLEZ	Branch on Less than or Equal to Zero
SLTIU	Set on Less Than Immediate Unsigned	BGTZ	Branch on Greater Than Zero
ANDI	AND Immediate	BLTZ	Branch on Less Than Zero
ORI	OR Immediate	BGEZ	Branch on Greater than or Equal to Zero
XORI	Exclusive OR Immediate	BLTZAL	Branch on Less Than Zero and Link
LUI	Load Upper Immediate	BGEZAL	Branch on Greater than or Equal to Zero and Link
			<b>Special Instructions</b>
	<b>Arithmetic Instructions (3-operand, register-type)</b>	SYSCALL	System Call
ADD	Add	BREAK	Break
ADDU	Add Unsigned		
SUB	Subtract		<b>Coprocessor Instructions</b>
SUBU	Subtract Unsigned	LWCz	Load Word from Coprocessor
SLT	Set on Less Than	SWCz	Store Word to Coprocessor
MFCz	Move From Coprocessor	MTCz	Move To Coprocessor
SLTU	Set on Less Than Unsigned		
AND	AND	CTCz	Move Control to Coprocessor
OR	OR	CFCz	Move Control From Coprocessor
XOR	Exclusive OR	COPz	Coprocessor Operation
NOR	NOR	BCzT	Branch on Coprocessor z True
		BCzF	Branch on Coprocessor z False
	<b>Shift Instructions</b>		<b>System Control Coprocessor (CPO) Instructions</b>
SLL	Shift Left Logical	MTC0	Move To CP0
SRL	Shift Right Logical	MFC0	Move From CP0
SRA	Shift Right Arithmetic	TLBR	Read indexed TLB entry
SLLV	Shift Left Logical Variable	TLBWI	Write Indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWR	Write Random TLB entry
SRAV	Shift Right Arithmetic Variable	TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

Table 1 lists the instruction set of the R3000A processor core.

**R3000A System Control Coprocessor (CP0)**

The R3000A core can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the R3000A core and supports the virtual memory system and exception handling functions of the processor. The virtual memory system is implemented using a Translation Look-aside Buffer and a group of programmable registers as shown in Figure 3.

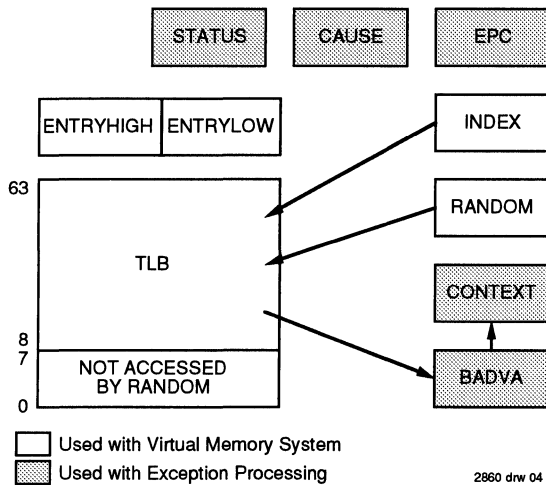
**SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS**

The CP0 registers shown in Figure 3 are used to control the memory management and exception handling capabilities of the R3000A. Table 2 provides a brief description of the registers common to most devices using the core. Note, however, that certain devices (e.g. non-E versions, the R3081, and R3041) implement slightly different sets of these registers, as described in their user's manuals.

**SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS**

Register	Description
EntryHIGH	HIGH half of a TLB entry
EntryLOW	LOW half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

2860 tbl 02



2860 drw 04

**Figure 4. The System Coprocessor Registers**

**Memory Management System**

The R3000A has an addressing range of 4gB. However, since most R3000A systems implement a physical memory smaller than 4gB, the R3000A provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4gB address space is divided into 2gB which can be accessed by both the users and the kernel, and 2gB for the kernel only.

The actual virtual to physical translation mechanism is either through an on-chip translation lookaside buffer (TLB), or through a fixed translation mechanism, depending on the device ("E" vs. non-"E" devices). These mechanisms are explained in the data sheets and user's manuals for those devices.

**R3000A Operating Modes**

The R3000A has two operating modes: User mode and Kernel mode. The R3000A normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception (RFE) instruction is executed. The manner in which memory addresses are translated or mapped depends on the operating mode of the R3000A, and whether the device implements an on-chip TLB.

**User Mode**—in this mode, a single, uniform virtual address space (kuseg) of 2gB is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. The actual virtual to physical address mapping is either done via a fixed translation, or through the TLB, depending on the device.

**Kernel Mode**—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512mB segment use cache memory but are not mapped through the optional TLB. Instead, they always map to the first 0.5gB of physical address space, whether or not the device contains an on-chip TLB.
- *kseg1*—references to this 512mB segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5gB segment of physical address space as *kseg0*.
- *kseg2*—references to this 1gB segment are either mapped through the TLB (with use of the cache determined by bit settings within the TLB entries) or through a predetermined mapping (non-E versions; all references go through the cache).

**R3000A Pipeline Architecture**

The execution of a single R3000A instruction consists of five primary steps:

- 1) **IF** — Fetch the instruction (I-Cache).
- 2) **RD** — Read any required operands from CPU registers while decoding the instruction.
- 3) **ALU** — Perform the required operation on instruction operands.
- 4) **MEM** — Access memory (D-Cache).
- 5) **WB** — Write back results to register file.

Each of these steps requires approximately one CPU cycle, as shown in Figure 4 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

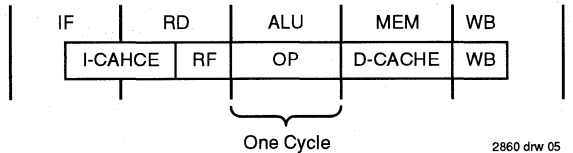


Figure 5. R3000A Instruction Pipeline

**INSTRUCTION EXECUTION**

The R3000A uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 5.

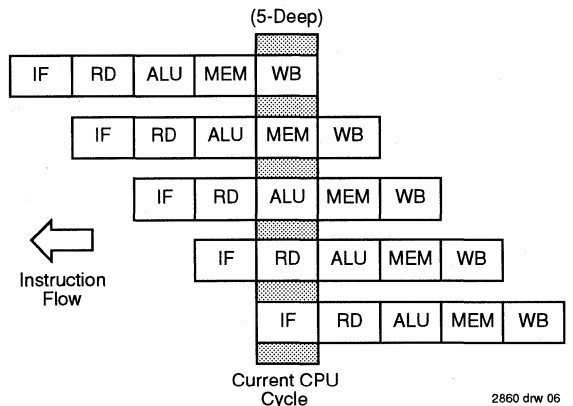


Figure 6. R3000A Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

## Memory System Hierarchy

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques, including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers.

Figure 6 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the R3000A's performance capabilities. The key features of this system are:

- **On-chip Cache Memory**—Local, high-speed memory (called cache memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The R3000A supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU.
- **Write Buffer**—in order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the R3000A is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the R3000A supports an interface to an on-chip write buffer. Thus, the R3000A core continues execution at high-speed, while the store data is retired at the slower memory rate.
- **Read Buffer**—The IDT RISController family typically incorporates an on-chip read buffer. This enables the system interface to match the speed of the high-speed execution core with the slower speed of a low-cost memory system, while still optimizing performance. This small on-chip FIFO enables the CPU to refill the cache and execute instructions even while additional instructions are being read from memory. This process is called instruction streaming.

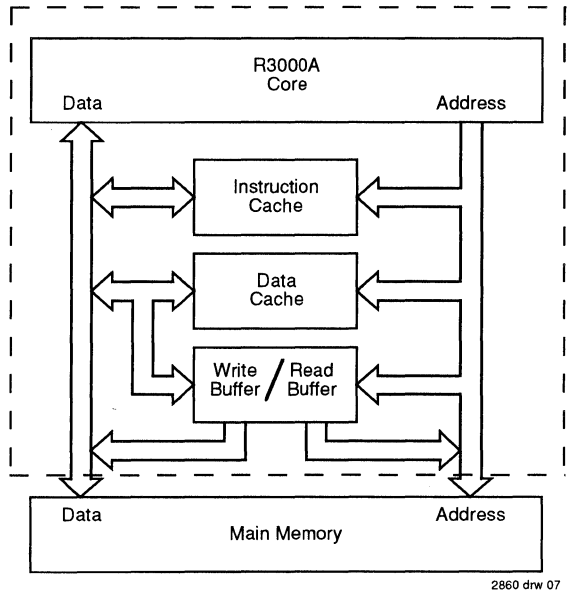


Figure 7. An R3000A System with a High-Performance Memory System

## ADVANCED FEATURES

The R3000A offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields. The R3000A allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, and further allows parity checking to be disabled. More details on these features can be found in the various devices' Hardware User's Manuals.

Further features of the R3000A are configured by the user, in a device dependent fashion. These functions include whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, particulars of the memory interface, etc.



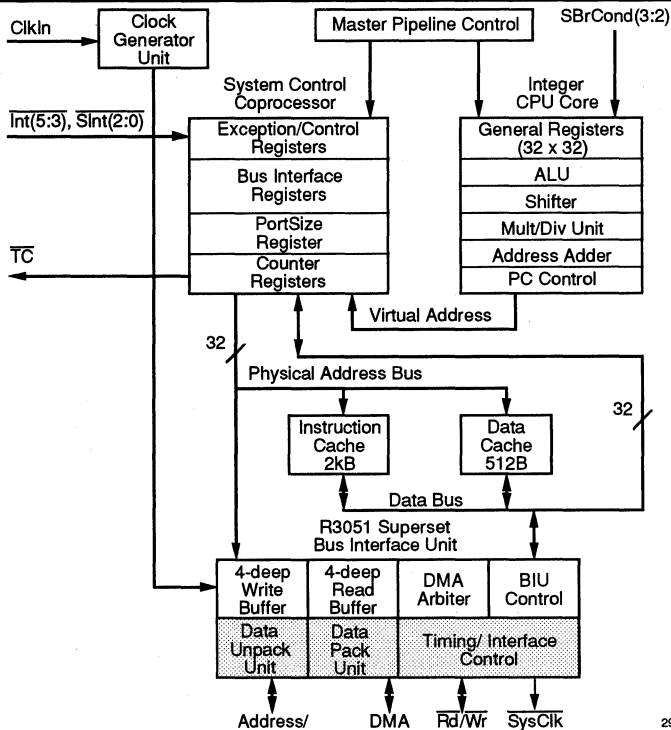
Integrated Device Technology, Inc.

# IDT79R3041™ INTEGRATED RISController™ FOR LOW-COST SYSTEMS

IDT79R3041  
IDT79RV3041

## FEATURES:

- Instruction set compatible with IDT79R3000A and R3051™ Family MIPS RISC CPUs
- High level of integration minimizes system cost
  - RISC CPU
  - Multiply/divide unit
  - Instruction Cache
  - Data Cache
  - Programmable bus interface
  - Programmable port width support
- On-chip instruction and data caches
  - 2KB of Instruction Cache
  - 512B of Data Cache
- Flexible bus interface allows simple, low-cost designs
  - Superset pin-compatible with R3051
  - Adds programmable port width interface (8-, 16-, and 32-bit memory sub-regions)
  - Adds programmable bus interface timing support (Extended address hold, Bus turn around time, Read/write masks)
- Single, double-frequency clock input
- 16.67MHz, 20MHz, 25MHz and 33MHz operation
- 16MIPS at 20MHz
- Low cost 84-pin PLCC packaging
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-word read buffer supports burst or simple block reads
- On-chip DMA arbiter
- On-chip 24-bit timer
- Boot from 8-bit, 16-bit, or 32-bit wide PROMs
- Pin- and software-compatible family includes R3041, R3051, R3052™, and R3081™
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point emulation software
  - Page Description Languages



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All others are trademarks of their respective companies

Figure 1. R3041 Block Diagram

COMMERCIAL TEMPERATURE RANGE

MARCH 1994

**INTRODUCTION**

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging. Thus, the R3051 family allows customer applications to bring maximum performance at minimum cost.

The R3041 extends the range of price/performance achievable with the R3051 family, by dramatically lowering the cost

of using the MIPS architecture. The R3041 is designed to achieve minimal system and components cost, yet maintain the high-performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the R3051 and R3081.

The R3051 family offers a variety of price/performance features in a pin-compatible, software compatible family. Table 1 provides an overview of the current members of the R3051 family. Note that the R3051, R3052, and R3081 are also available in pin-compatible versions that include a full-function memory management unit, including 64-entry TLB. The R3051/2 and R3081 are described in separate manuals and data sheets.

Figure 1 shows a block level representation of the functional units within the R3041. The R3041 can be viewed as the embodiment of a discrete solution built around the R3000A. By integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

An overview of these blocks is presented here, followed with detailed information on each block.

Device Name	Instruction Cache	Data Cache	Floating Point	Bus Options
R3051	4kB	2kB	Software Emulation	Mux'ed A/D
R3052	8kB	2kB	Software Emulation	Mux'ed A/D
R3081 or 8kB	16kB or 8kB	4kB	On-chip Hardware	1/2 frequency bus option
R3041	2kB	512B	Software Emulation Programmable timing support	8-, 16-, and 32-bit port width support

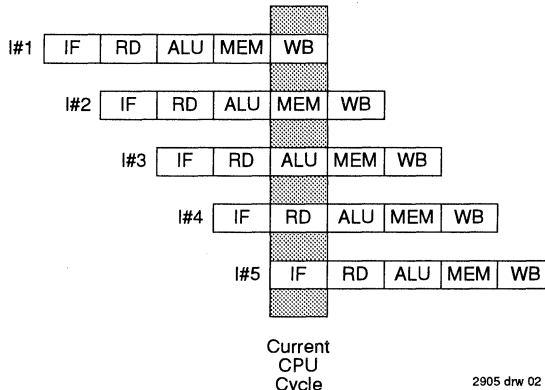
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**Table 1. Pin compatible R3051 Family**

**CPU Core**

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to a single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS-I Instruction Set Architecture (ISA). In fact, the execution engine of the R3041 is the same as the execution engine of the R3000A. Thus, the R3041 is binary compatible with those CPU engines, as well as compatible with other members of the R3051 family.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). The five parts of the pipeline are the Instruction Fetch, Read register, ALU execution, Memory, and Write Back stages. Figure 2 shows the concurrency achieved by the R3051 family pipeline.



**Figure 2. R3051 Family 5-Stage Pipeline**

**System Control Co-Processor**

The R3041 also integrates on-chip a System Control Co-processor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the R3051 family, but instead performs the same virtual to physical address mapping of the base version of the R3051 family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

The memory mapping used by these devices is illustrated in Figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by ad-

dress decoding, or in other system specific forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- **Cache Configuration Register:** This register controls the data cache block size and miss refill algorithm.
- **Bus Control Register:** This register controls the behavior of the various bus interface signals.
- **Count and Compare Registers:** Together, these two registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **Port Size Control Register:** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring additional external logic.

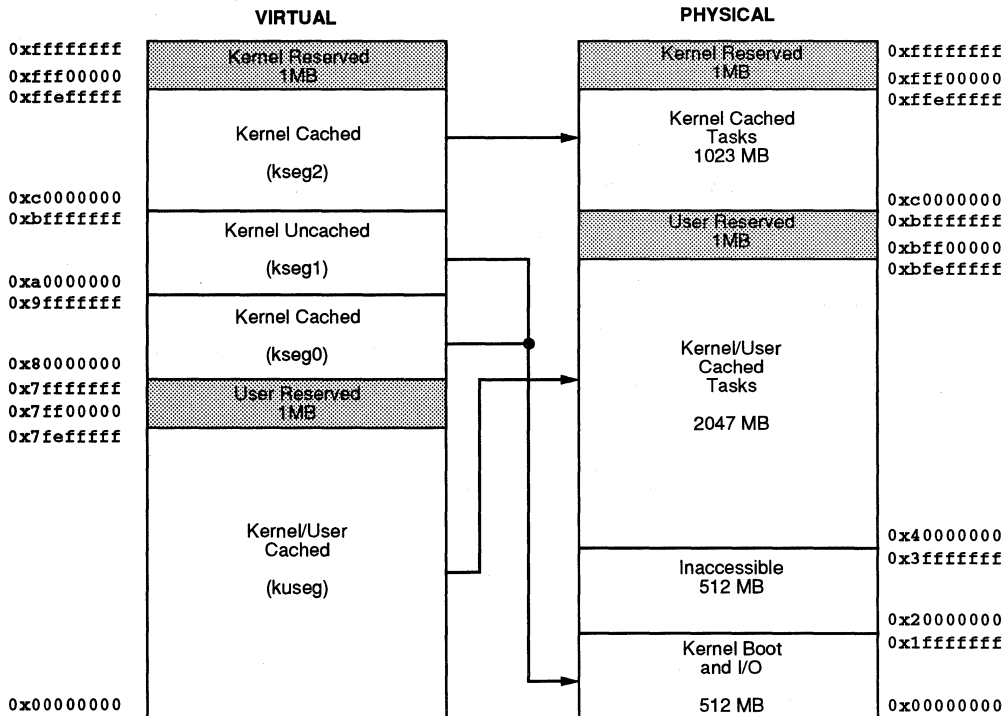


Figure 3. Virtual to Physical Mapping of Base Architecture Versions

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### Clock Generation Unit

The R3041 is driven from a single 2x frequency input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A based applications.

### Instruction Cache

The R3041 integrates 2kB of on-chip Instruction Cache, organized with a line size of 16 bytes (four 32-bit entries) and is direct mapped. This relatively large cache substantially contributes to the performance inherent in the R3041, and allows systems based on the R3041 to achieve high-performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switch.

### Data Cache

The R3041 incorporates an on-chip data cache of 512B, organized as a line size of 4 bytes (one word) and is direct mapped. This relatively large data cache contributes substantially to the performance inherent in the R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

### Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3041 incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3041 augments the basic R3051 bus interface capability by adding the ability to directly interface with varying memory port widths, for instructions or data. For example, the R3041 can be used in a system with an 8-bit boot PROM, 16-bit font/program cartridges, and 32-bit main memory, transparently to software, and without requiring external data packing, rotation, and unpacking.

In addition, the R3041 incorporates the ability to change some of the interface timing of the bus. These features can be used to eliminate external data buffers and take advantage of lower speed and lower cost interface components.

One of the bus interface options is the Extended Address Hold mode which adds 1/2 clock of extra address hold time from ALE falling. This allows easier interfacing to FPGAs and ASICs.

The R3041 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate. During main memory writes, the R3041 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software which initiated the store, insuring that the same software can run in true 32-bit memory systems.

The R3051 family read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to use page or static column mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or even to use simpler SRAM techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R3041 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, using 8-, 16-, or 32-bit boot PROMs is easily supported by the R3041.



**SYSTEM USAGE**

The IDT R3051 family is specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems use inexpensive EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. An embedded system can optionally use an 8-bit boot PROM instead. A 16-bit font/program cartridge interface is provided for add-in cards. A 16-bit DRAM interface is used

for a low-cost page frame buffer. In this system example, a field or manufacturing upgrade to a 32-bit page frame buffer is supported by the boot software and DRAM controller. Embedded systems may optionally substitute SRAMs for the DRAMs. Finally various 8/16/32-bit I/O ports such as RS-232/422, SCSI, and LAN as well as the laser printer engine interface are supported. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the R3051 family.

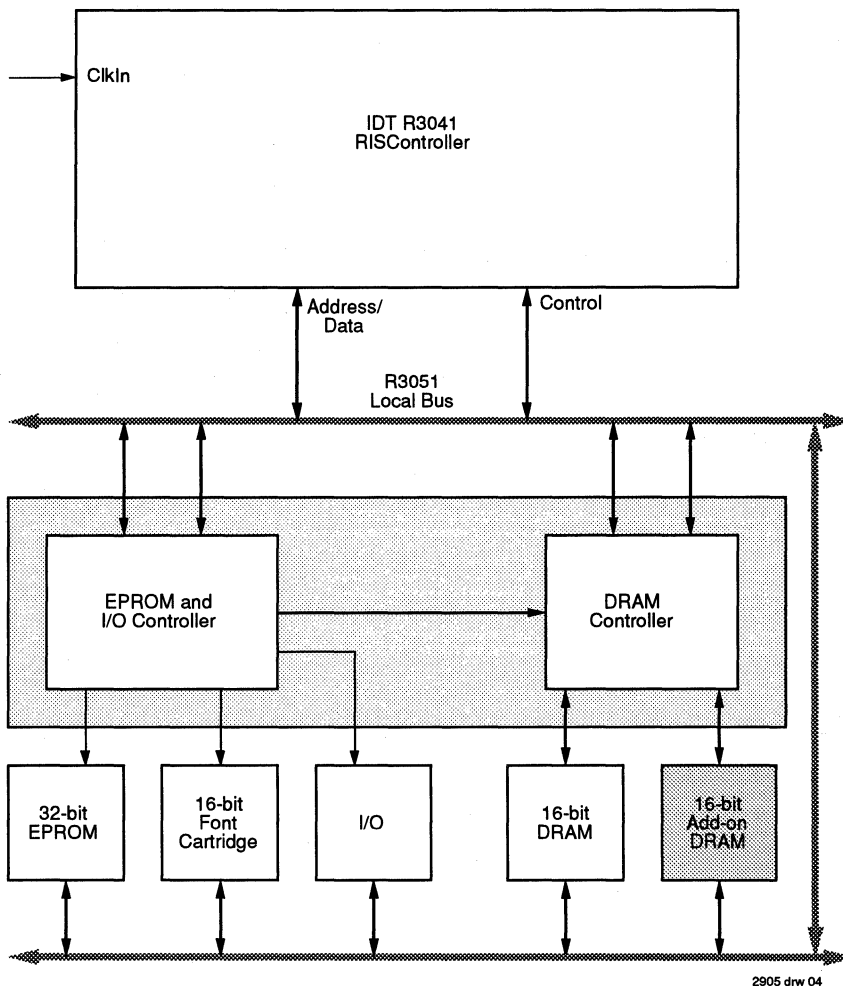


Figure 4. Typical R3041-Based Application

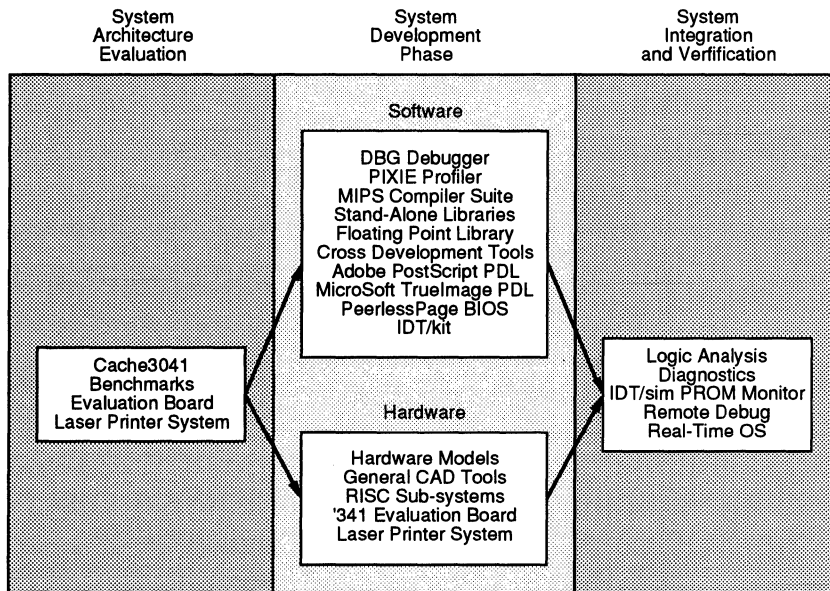
**DEVELOPMENT SUPPORT**

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family based applications, and include tools such as:

- Optimizing compilers from MIPS Technology, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.

- The high-performance IDT floating point emulation library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT Laser Printer System boards, which directly drive a low-cost print engine, and runs Adobe PostScript™ Page Description Language
- Adobe PostScript Page Description Language running on the IDT R3051 family.
- The IDT/sim™ PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™ (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.



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Figure 5. R3041 Development Environment

## PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine:** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves over 16 MIPS performance when operating out of cache.
- **Large on-chip caches:** The R3051 family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- **Autonomous multiply and divide operations:** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- **Integrated write buffer:** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support:** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various R3051 family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these devices in their application.

## SELECTABLE FEATURES

The R3051 family uses two methods to allow the system designer to configure bus interface operation options.

The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communication between various types of processors and databases.
- **Data Cache Refill of one or four words:** The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed:** The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time:** The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals:** The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.
- **Programmable memory Port Widths:** The R3041 allows the kernel to partition the physical memory space into various sub-regions, and to individually indicate the port width of these sub-regions. Thus, the bus interface unit can perform data packing and unpacking when communicating with narrow memory sub-regions. For example, these features, can be used to allow the R3041 to interface with narrow 8-bit boot PROMs, or to implement 16-bit only memory systems.

## THERMAL CONSIDERATIONS

The R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package is used for all speeds of the R3041 family.

Higher speed and higher performance members of the R3051 family utilize more advanced packaging techniques to dissipate power while remaining both low-cost and pin- and socket-compatible with the PLCC package. Thus, these members of the R3051 family are available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

The members of the R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I<sub>CC</sub> specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 2 for the PLCC package.

$\theta_{CA}$	Airflow (ft/min)					
	0	200	400	600	800	1000
"J" Package	29	26	21	18	16	15
TQFP	55	40	35	33	31	30

2905 tbl 02

**Table 2. Thermal Resistance ( $\theta_{CA}$ ) at Various Airflows**

## NOTES ON SYSTEM DESIGN

The R3041 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

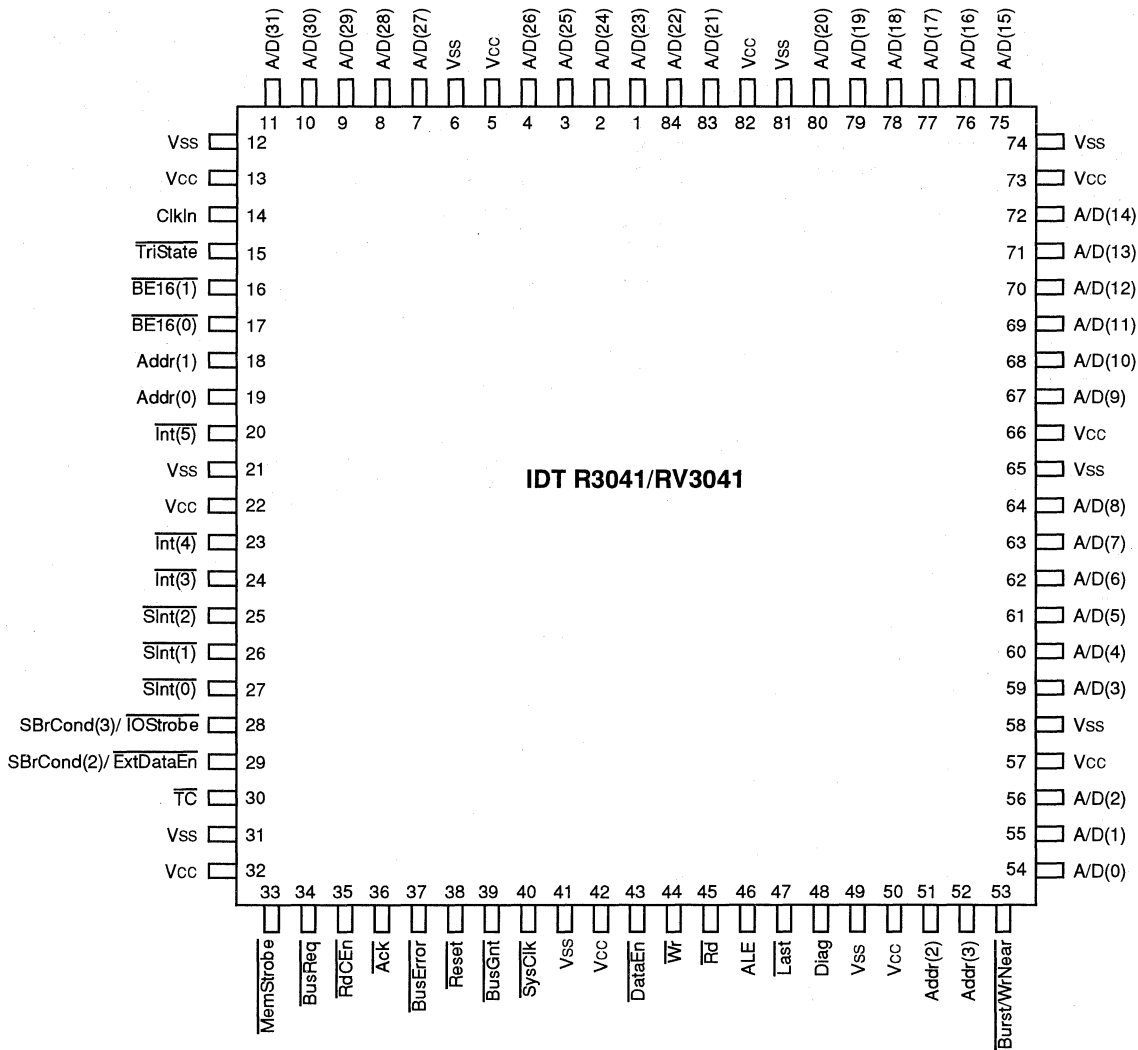
To minimize these AC parameters, the R3041 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3041 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3041 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

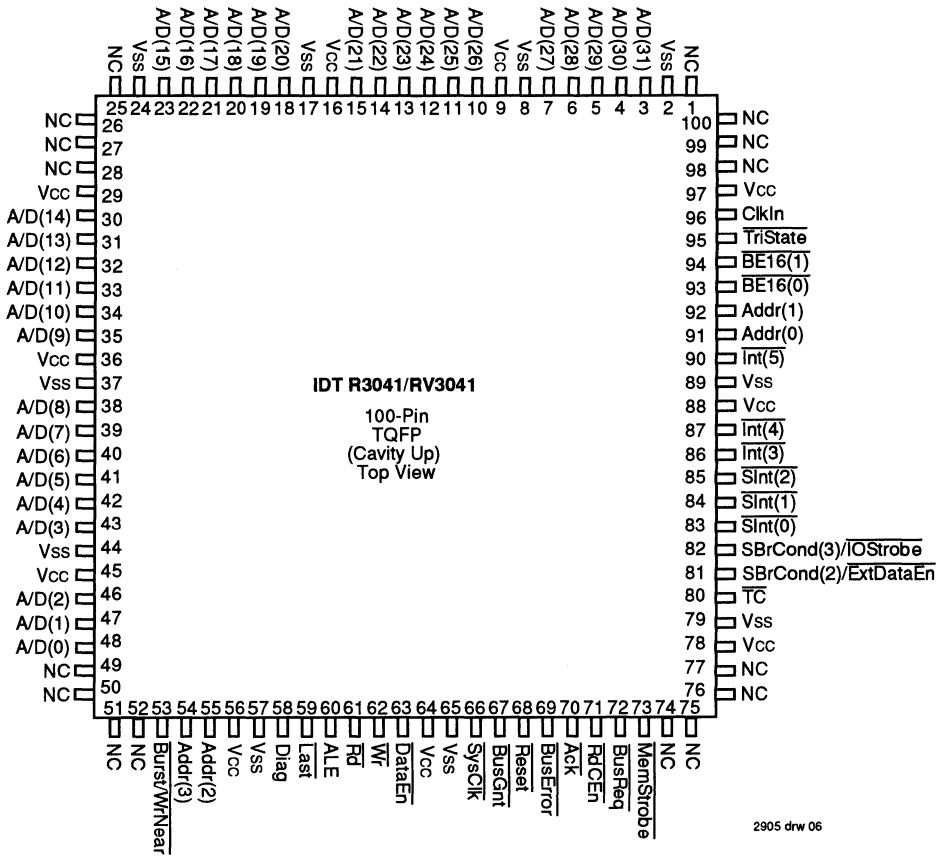
**PIN CONFIGURATIONS**



2905 drw 06

**84-Pin PLCC/  
Top View  
(Cavity Down)**

**PIN CONFIGURATIONS**



2905 drw 06

5



**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Burst/}}\overline{\text{WrNear}}$	O	<p><b>Burst Transfer/Write Near:</b> On read transactions, the <math>\overline{\text{Burst}}</math> signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if the 4-word data block refill option is selected in the CP0 Cache Config Register.</p> <p>On write transactions, the <math>\overline{\text{WrNear}}</math> output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.</p>
$\overline{\text{Rd}}$	O	<b>Read:</b> An output which indicates that the current bus transaction is a read.
$\overline{\text{Wr}}$	O	<b>Write:</b> An output which indicates that the current bus transaction is a write.
$\overline{\text{Ack}}$	I	<b>Acknowledge:</b> An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
$\overline{\text{RdCEn}}$	I	<b>Read Buffer Clock Enable:</b> An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{\text{SysClk}}$	O	<b>System Reference Clock:</b> An output from the CPU which reflects the timing of the internal processor "System" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
$\overline{\text{BusReq}}$	I	<b>DMA Arbiter Bus Request:</b> An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
$\overline{\text{BusGnt}}$	O	<p><b>DMA Arbiter Bus Grant.</b> An output from the CPU used to acknowledge that a <math>\overline{\text{BusReq}}</math> has been detected, and that the bus is relinquished to the external master.</p> <p>The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the <math>\overline{\text{BusGnt}}</math> output early, and waiting for the <math>\overline{\text{BusReq}}</math> input to be negated.</p>
$\overline{\text{SBrCond(3)/}}\overline{\text{IOStrobe}}$	I/O	<p><b>Branch Condition Port/IO Strobe:</b> The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.</p> <p>If this pin is selected to function as <math>\overline{\text{IOStrobe}}</math>, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals on the bus interface.</p>
$\overline{\text{SBrCond(2)/}}\overline{\text{ExtDataEn}}$	I/O	<p><b>Branch Condition Port/Extended Data Enable:</b> The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.</p> <p>If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of <math>\overline{\text{Rd}}</math> or <math>\overline{\text{Wr}}</math>. This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.</p>
$\overline{\text{MemStrobe}}$	O	<p><b>Memory Strobe:</b> This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices.</p> <p>The R3041 <math>\overline{\text{MemStrobe}}</math> output pin is designated as the BrCond(0) input pin in the R3051 and R3081.</p>

2305 tbl 04





**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup> R3041**

Symbol	Rating	Commercial	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>c</sub>	Operating Case Temperature	0 to +85	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
V <sub>IN</sub>	Input Voltage	-0.5 to +7.0	V

**NOTES:**

2905 tbl 06

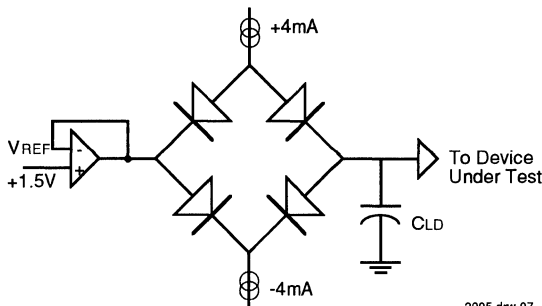
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -3.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> + 0.5 Volts.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2905 tbl 07

**OUTPUT LOADING FOR AC TESTING**



2905 drw 07

**AC TEST CONDITIONS R3041**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.0	—	V
V <sub>IL</sub>	Input LOW Voltage	—	0.4	V
V <sub>IHS</sub>	Input HIGH Voltage	3.5	—	V
V <sub>ILS</sub>	Input LOW Voltage	—	0.4	V

2905 tbl 08

Signal	C <sub>ld</sub>
All Signals	25 pF

2905 tbl 09



**DC ELECTRICAL CHARACTERISTICS R3041 — (T<sub>c</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)**

Symbol	Parameter	Test Conditions	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V <sub>IHS</sub>	Input HIGH Voltage <sup>(2,3)</sup>	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V <sub>ILS</sub>	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C <sub>IN</sub>	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
C <sub>OUT</sub>	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = 5V, T <sub>c</sub> = 25°C	—	350	—	400	—	300	—	370	mA
I <sub>IH</sub>	Input HIGH Leakage	V <sub>IH</sub> = V <sub>CC</sub>	—	100	—	100	—	100	—	100	mA
I <sub>IL</sub>	Input LOW Leakage	V <sub>IL</sub> = GND	-100	—	-100	—	-100	—	-100	—	mA
I <sub>OZ</sub>	Output Tri-state Leakage	V <sub>OH</sub> = 2.4V, V <sub>OL</sub> = 0.5V	-100	100	-100	100	-100	100	-100	100	mA

**NOTES:**

2905 tbl 10

- V<sub>IL</sub> Min. = -3.0V for pulse width less than 15ns. V<sub>IL</sub> should not fall below -0.5 volts for larger periods.
- V<sub>IHS</sub> and V<sub>ILS</sub> apply to Clkin and Reset.
- V<sub>IH</sub> should not be held above V<sub>CC</sub> + 0.5 volts.
- Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS R3041 (1, 2, 3) — (T<sub>c</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to SysClk falling	12	—	9	—	7	—	7	—	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	4	—	3	—	2.5	—	2.5	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	10	—	8	—	7	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	10	—	8	—	7	—	7	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from SysClk rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from SysClk falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5	—	ns
t11	DataEn	Asserted from SysClk	—	19	—	15	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from SysClk	—	15	—	12	—	11	—	11	ns
t18	A/D	Tri-state from SysClk	—	13	—	10	—	10	—	10	ns
t19	A/D	SysClk to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	μs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	Reset	Set-up to SysClk falling	6	—	6	—	5	—	5	—	ns
t26	Int	Mode set-up to Reset rising	6	—	6	—	5	—	5	—	ns
t27	Int	Mode hold from Reset rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	6	—	5	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	6	—	5	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

2905 tbl 11

**AC ELECTRICAL CHARACTERISTICS R3041 (CONT.)**

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t45	ExtDataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	ExtDataEn	Driven from SysClk falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	IOStrobe	Valid from SysClk falling	—	10	—	8	—	7	—	7	ns
t48	ExtDataEn, DataEn	Asserted from SysClk rising	—	15	—	12	—	9	—	9	ns
t49	ExtDataEn	Negated from SysClk rising	—	9	—	7	—	6	—	6	ns
t50	MemStrobe	Asserted from SysClk rising	—	19	—	15	—	15	—	15	ns
t51	MemStrobe	Negated from SysClk falling	—	19	—	15	—	15	—	15	ns
t52	MemStrobe	Asserted from Addr(3:0) valid <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF <sup>(4, 5)</sup>	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

**NOTES:**

2905 tbl 12

1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other R3051 family members.

**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup> RV3041**

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
Tc	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
VIN	Input Voltage	-0.5 to +7.0	V

**NOTES:**

2905 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed Vcc +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**AC TEST CONDITIONS RV3041**

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.0	—	V
VILS	Input LOW Voltage	—	0.4	V

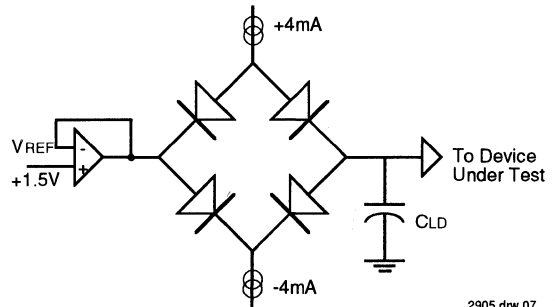
2905 tbl 08

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature	GND	Vcc
Commercial RV3041	0°C to +85°C (Case)	0V	3.3 ±5%

2905 tbl 07

**OUTPUT LOADING FOR AC TESTING**



2905 drw 07

Signal	Cld
All Signals	25 pF

2905 tbl 09

**DC ELECTRICAL CHARACTERISTICS RV3041** — ( $T_C = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +3.3\text{V} \pm 5\%$ )

Symbol	Parameter	Test Conditions	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	2.4	—	2.4	—	2.4	—	V
VOL	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	—	0.4	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage <sup>(2,3)</sup>	—	2.5	—	2.5	—	2.5	—	2.5	—	V
VILS	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	—	0.4	V
CIN	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
COU	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
ICC	Operating Current	$V_{CC} = 3.3\text{V}, T_C = 25^\circ\text{C}$	—	130	—	150	—	180	—	225	mA
IiH	Input HIGH Leakage	$V_{IH} = V_{CC}$	—	100	—	100	—	100	—	100	mA
IiL	Input LOW Leakage	$V_{IL} = \text{GND}$	-100	—	-100	—	-100	—	-100	—	mA
IOZ	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-100	100	-100	100	-100	100	-100	100	mA

**NOTES:**

1.  $V_{IL}$  Min. =  $-3.0\text{V}$  for pulse width less than 15ns.  $V_{IL}$  should not fall below  $-0.5$  volts for larger periods.
2.  $V_{IHS}$  and  $V_{ILS}$  apply to  $\text{ClkIn}$  and  $\text{Reset}$ .
3.  $V_{IH}$  should not be held above  $V_{CC} + 0.5$  volts.
4. Guaranteed by design.

2905 tbl 10

**AC ELECTRICAL CHARACTERISTICS RV3041** (1, 2, 3) — ( $T_C = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +3.3\text{V} \pm 5\%$ )

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to SysClk falling	12	—	9	—	7	—	7	—	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	2	—	2	—	2	—	2	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	10	—	8	—	7	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	10	—	8	—	7	—	7	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from SysClk rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from SysClk falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5	—	ns
t11	DataEn	Asserted from SysClk	—	19	—	15	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from SysClk	—	15	—	12	—	11	—	11	ns

2905 tbl 11

**AC ELECTRICAL CHARACTERISTICS RV3041 (CONT.)**

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t18	A/D	Tri-state from SysClk	—	13	—	10	—	10	—	10	ns
t19	A/D	SysClk to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	Reset	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t26	Int	Mode set-up to Reset rising	8	—	6	—	5	—	5	—	ns
t27	Int	Mode hold from Reset rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	t22 + 2	ns
t45	ExtDataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	ExtDataEn	Driven from SysClk falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	IOStrobe	Valid from SysClk falling	—	10	—	8	—	7	—	7	ns
t48	ExtDataEn,	Asserted from SysClk rising	—	15	—	12	—	9	—	9	ns
t49	ExtDataEn DataEn	Negated from SysClk rising	—	9	—	7	—	6	—	6	ns
t50	MemStrobe	Asserted from SysClk rising	—	19	—	15	—	15	—	15	ns
t51	MemStrobe	Negated from SysClk falling	—	19	—	15	—	15	—	15	ns
t52	MemStrobe	Asserted from Addr(3:0) valid <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF <sup>(4,5)</sup>	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

**NOTES:**

1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other R3051 family members.

2905 tbl 12



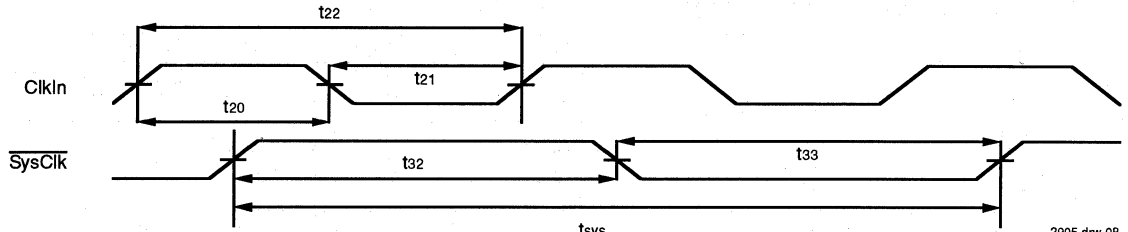


Figure 8. R3051 Family Clocking

2905 drw 08

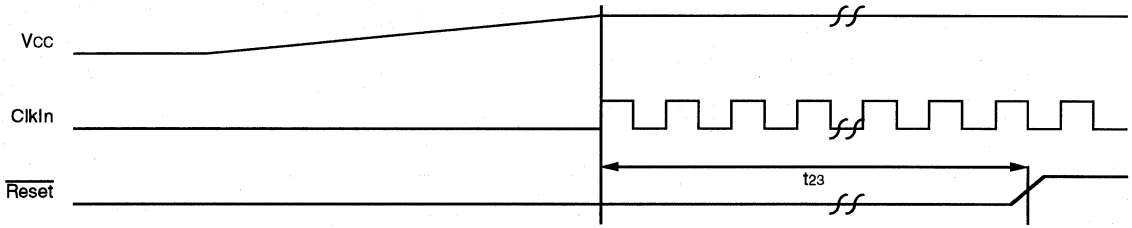


Figure 9. Power-On Reset Sequence

2905 drw 09

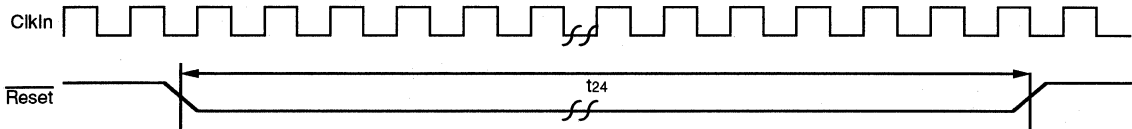


Figure 10(a). Warm Reset Sequence

2905 drw 10

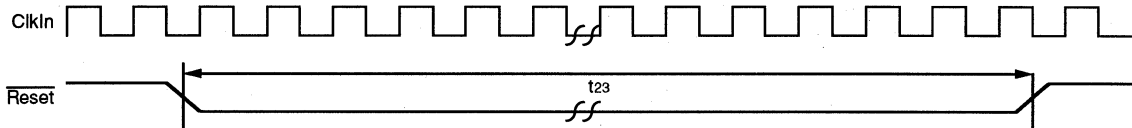


Figure 10(b). Warm Reset Sequence (Internal Pull-Ups Used)

2905 drw 11

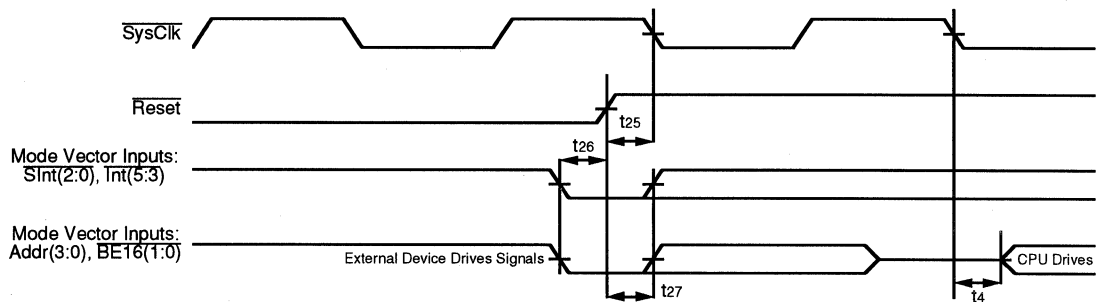


Figure 11. Mode Selection and Negation of Reset

2905 drw 12

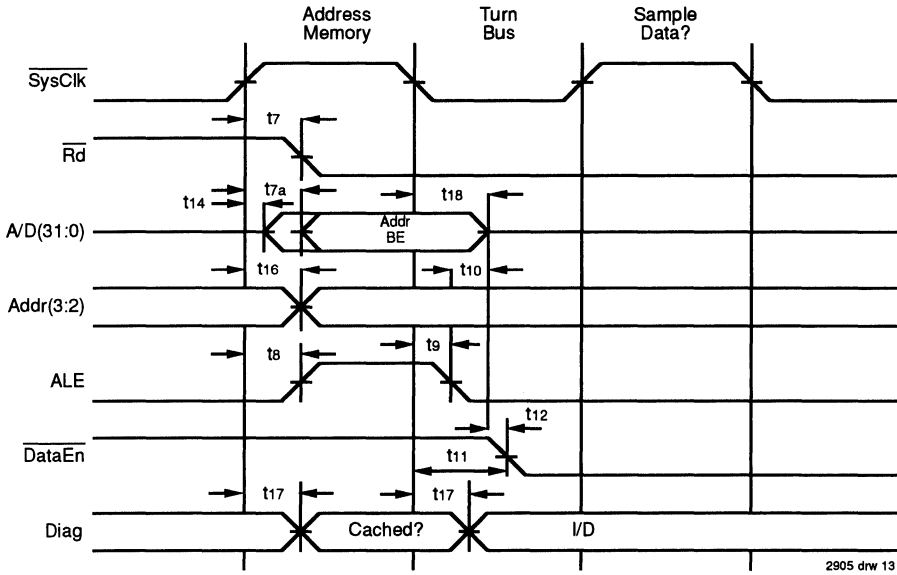


Figure 12(a). Start of Read Timing with Non-Extended Address Hold Option

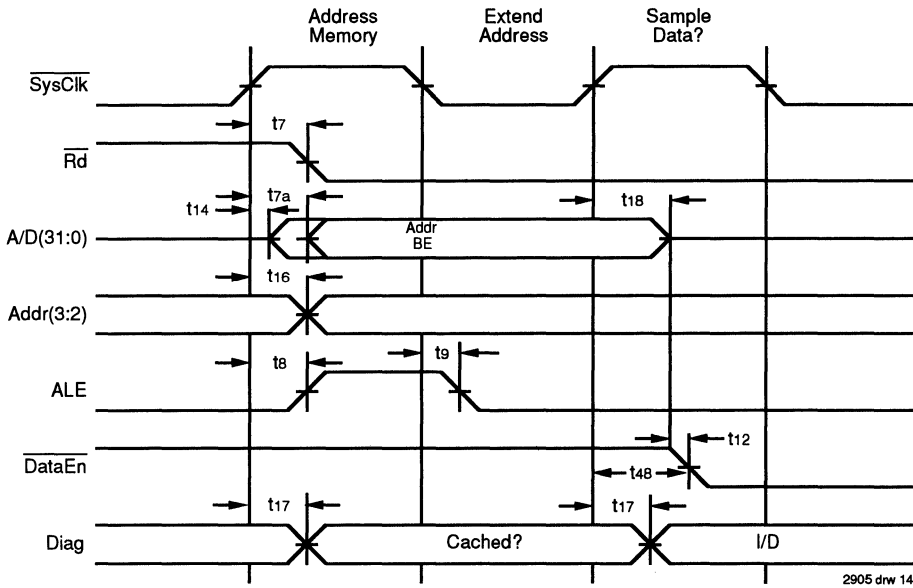
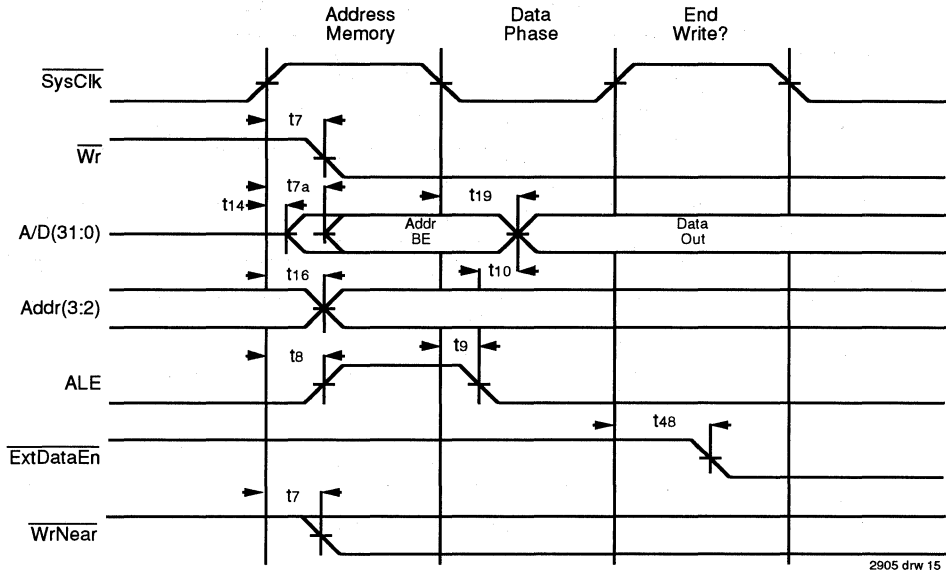


Figure 12(b). Start of Read Timing with Extended Address Hold Option

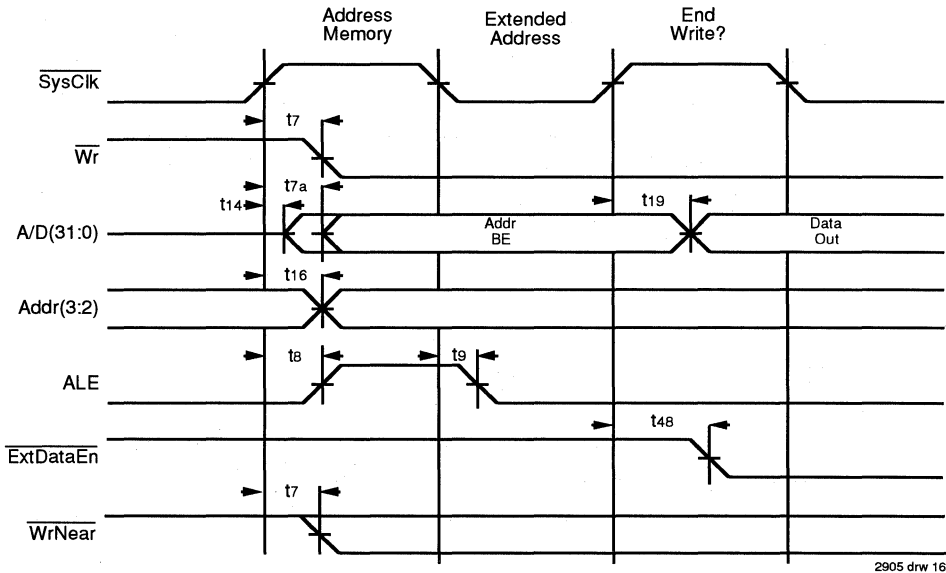
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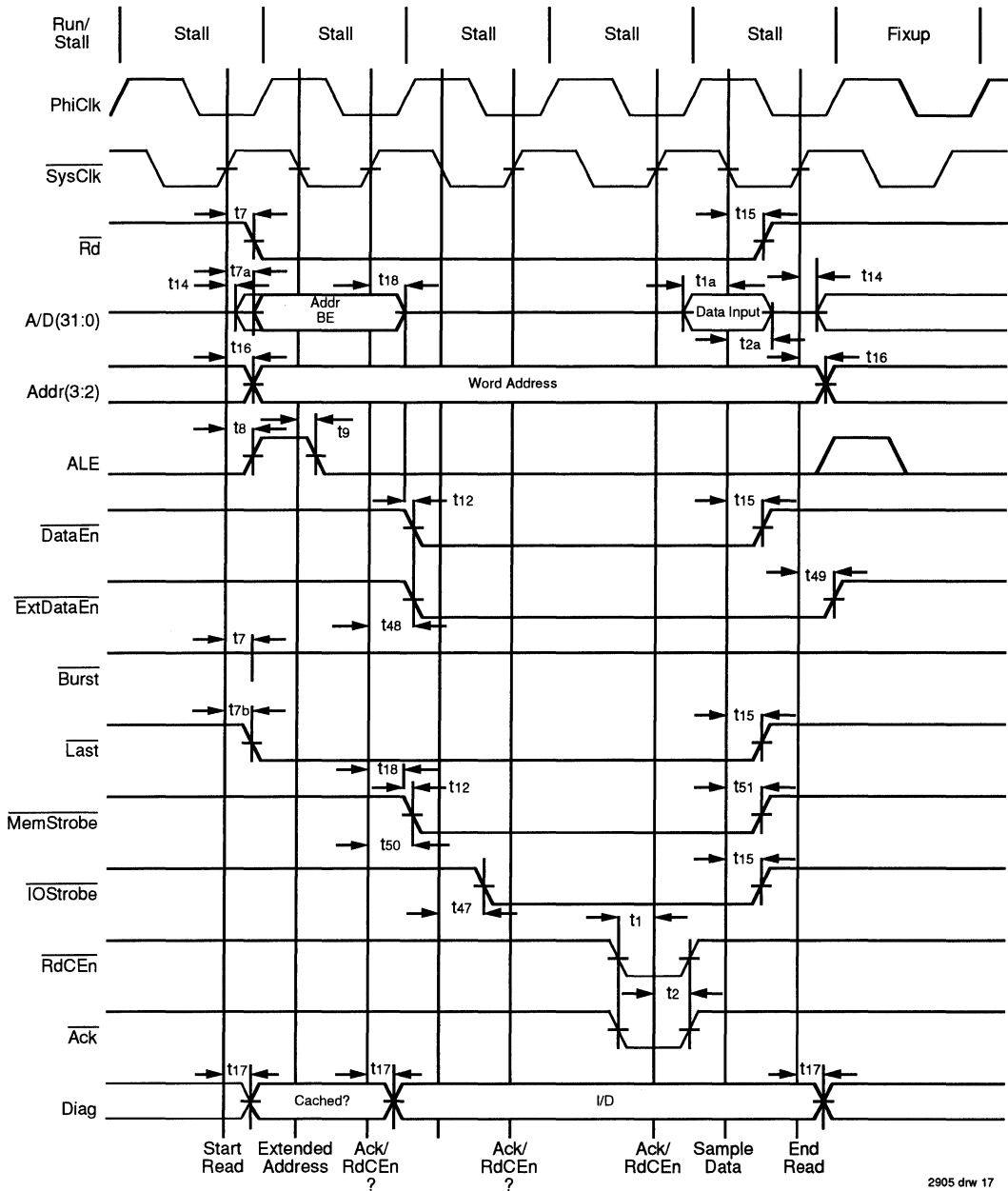
2905 drw 15

Figure 12(c). Start of Write Timing with Non-Extended Address Hold Option



2905 drw 16

Figure 12(d). Start of Write Timing with Extended Address Hold Option



2905 drw 17

Figure 13. Single Datum Read

5

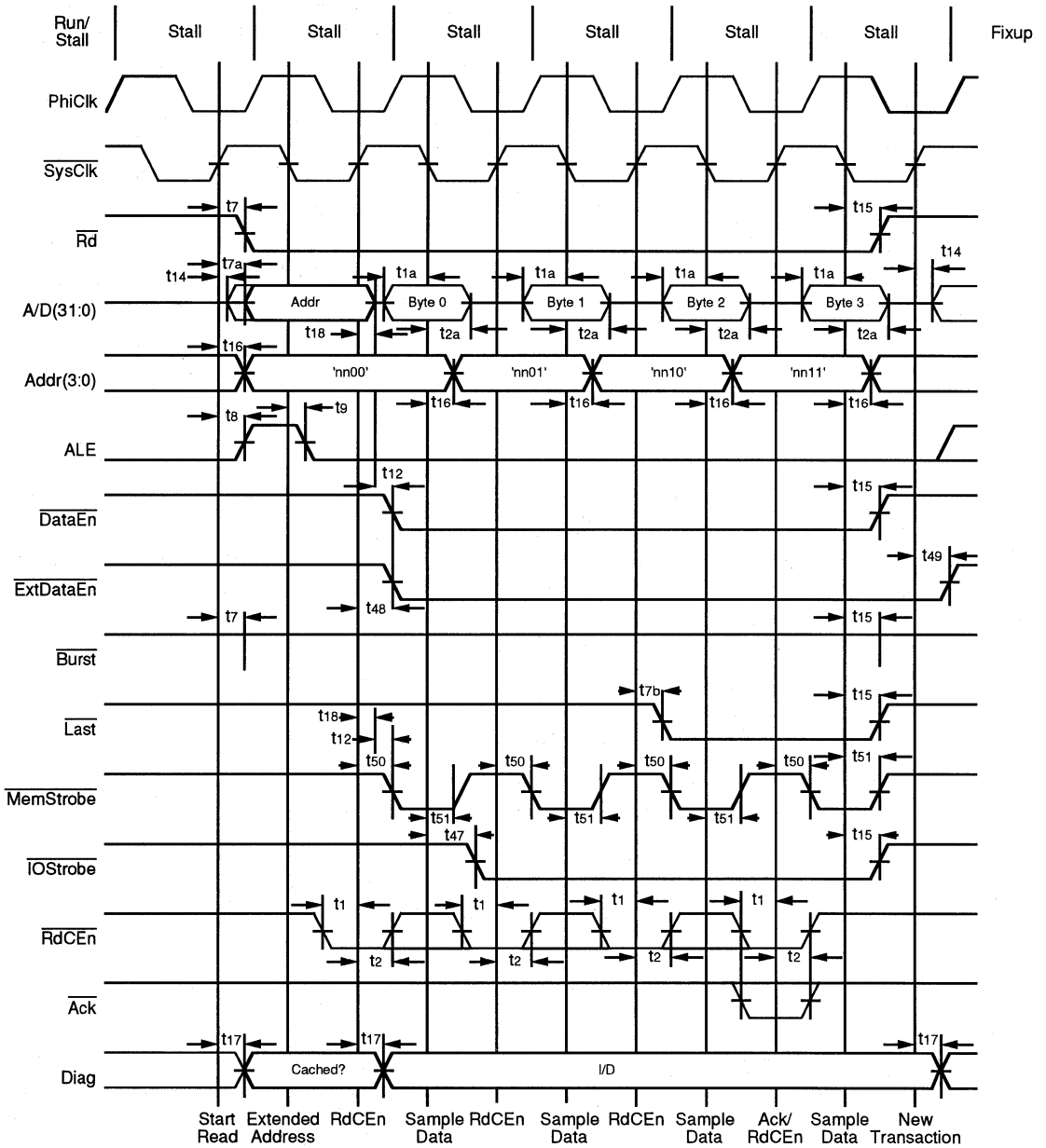
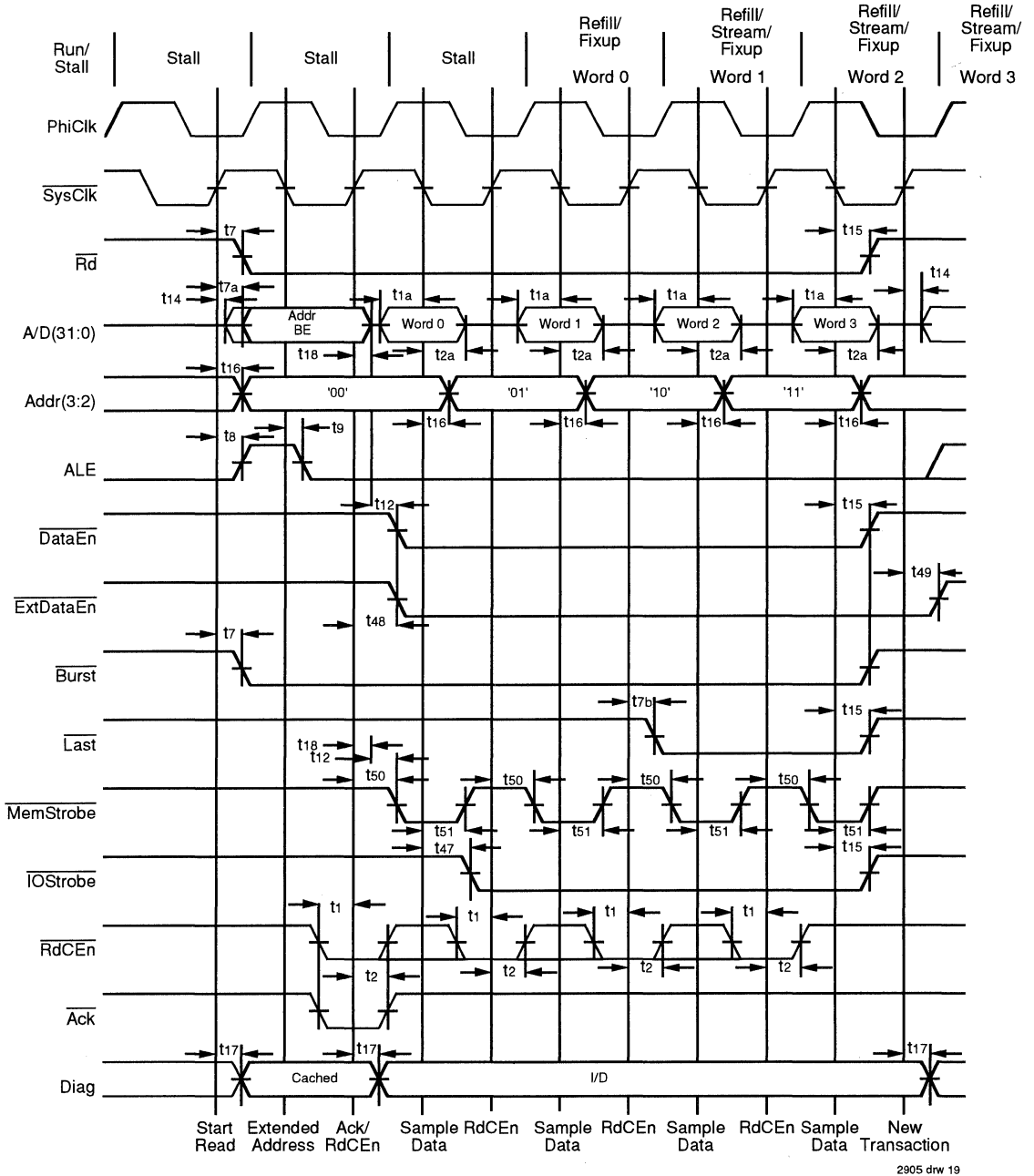


Figure 14. Mini-burst read of 32-bit datum from 8-bit wide memory port



5

Figure 15. R3041 Quad Word Read

2905 drw 19

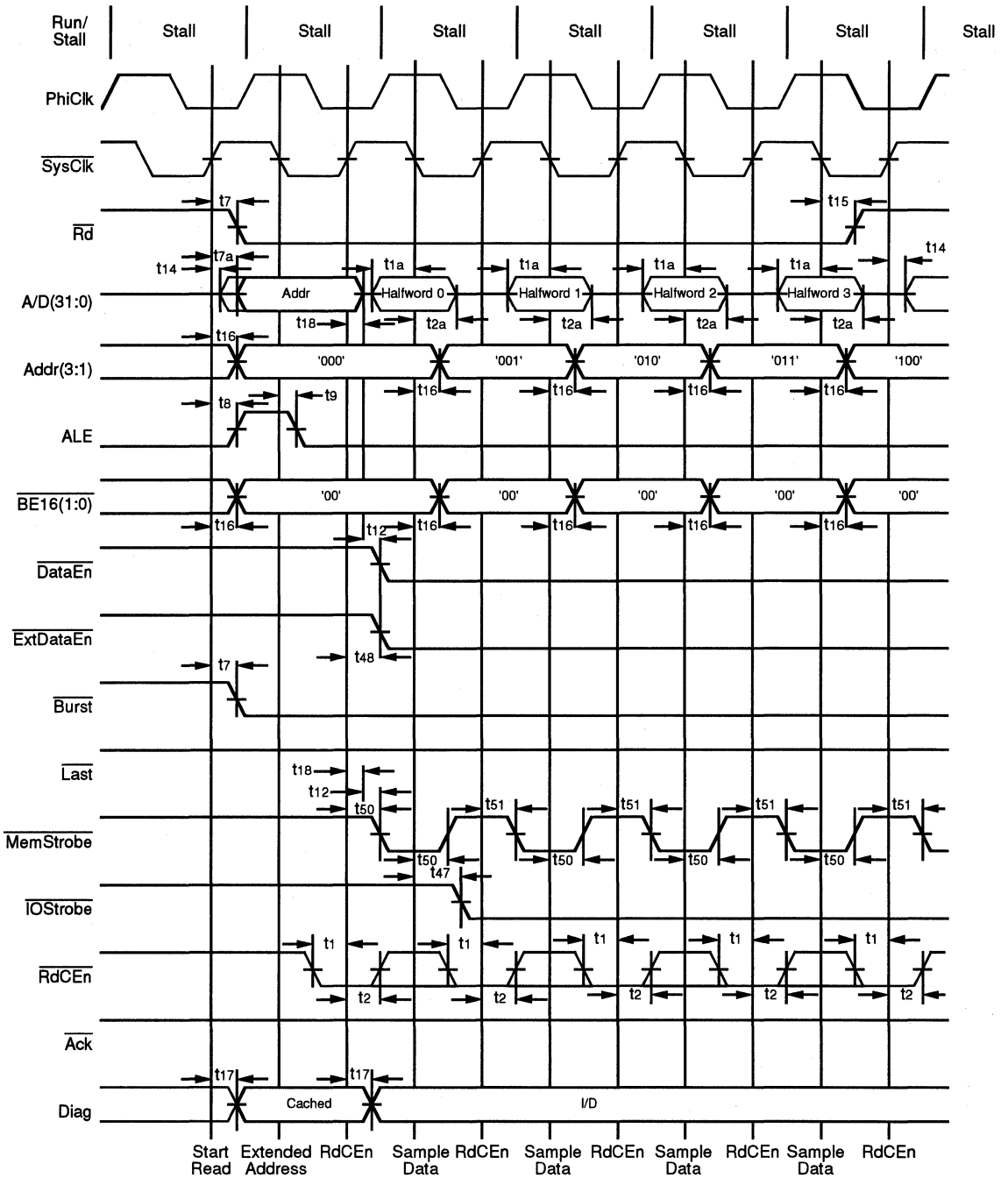


Figure 16(a). Quad Word Read to 16-bit wide Memory Port

2905 drw 20

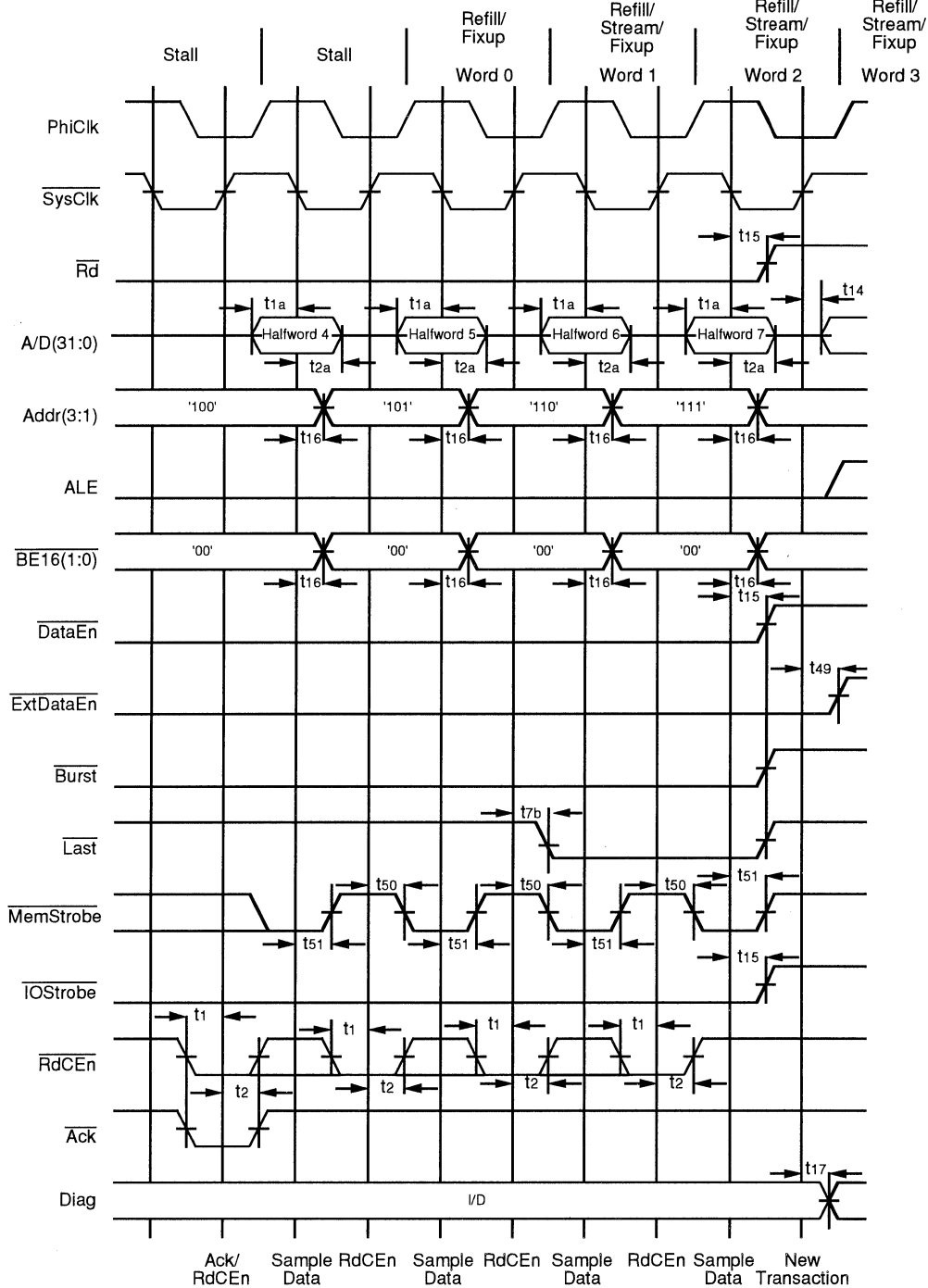
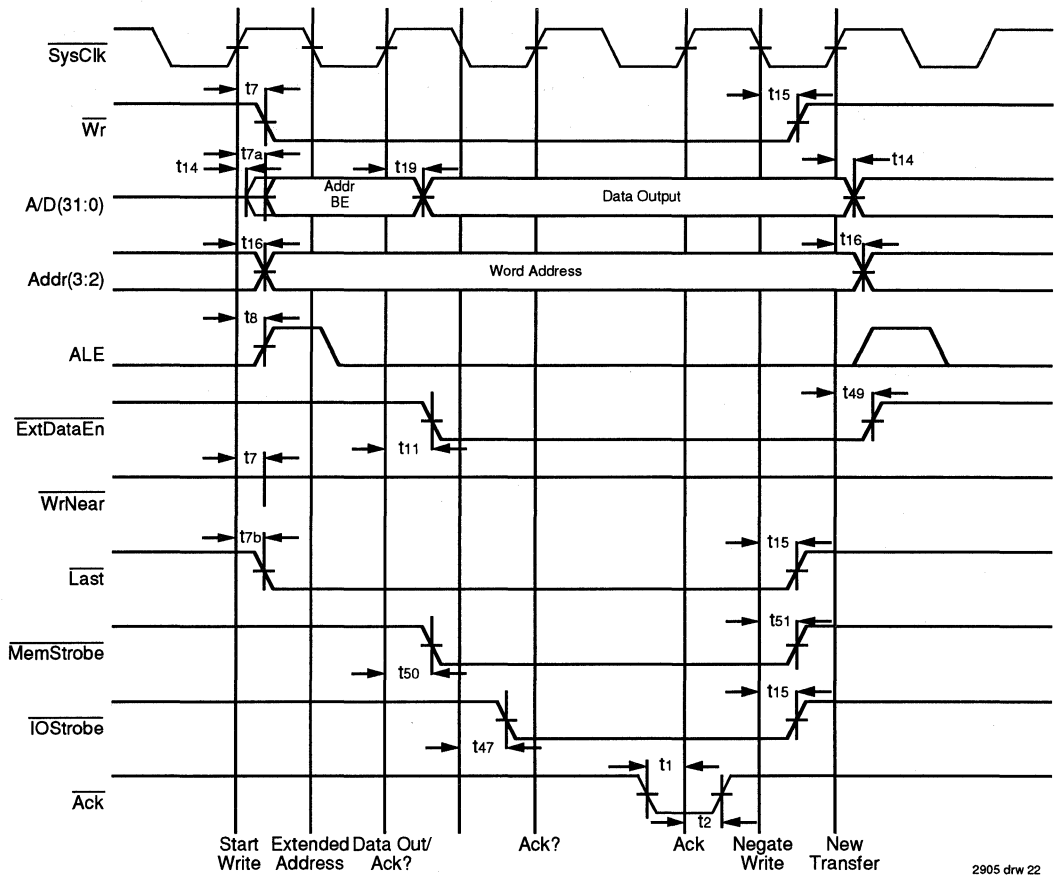


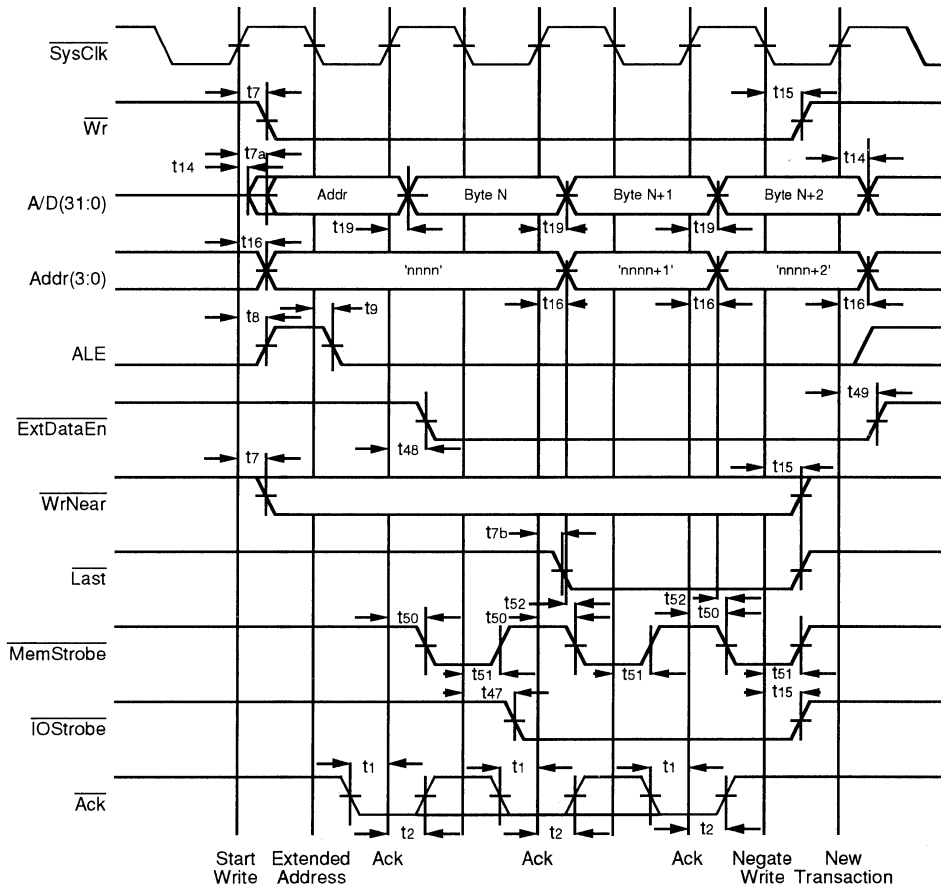
Figure 16(b). End of Quad Word read from 16-bit Wide Memory Port

5



2905 drw 22

Figure 17. Basic Write to 32-bit Memory Port



2905 drw 23

Figure 18. Tri-Byte Mini-burst Write to 8-bit Port

5



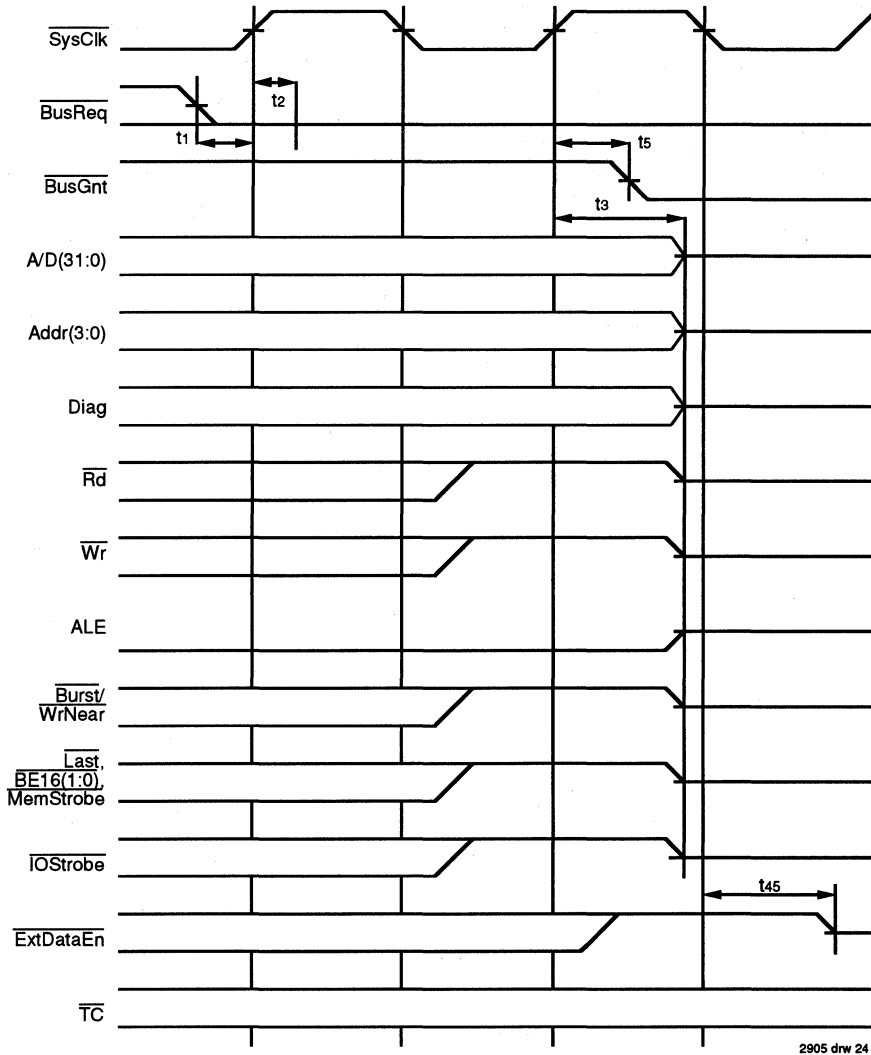


Figure 19. Request and Relinquish of R3041 Bus to External Master

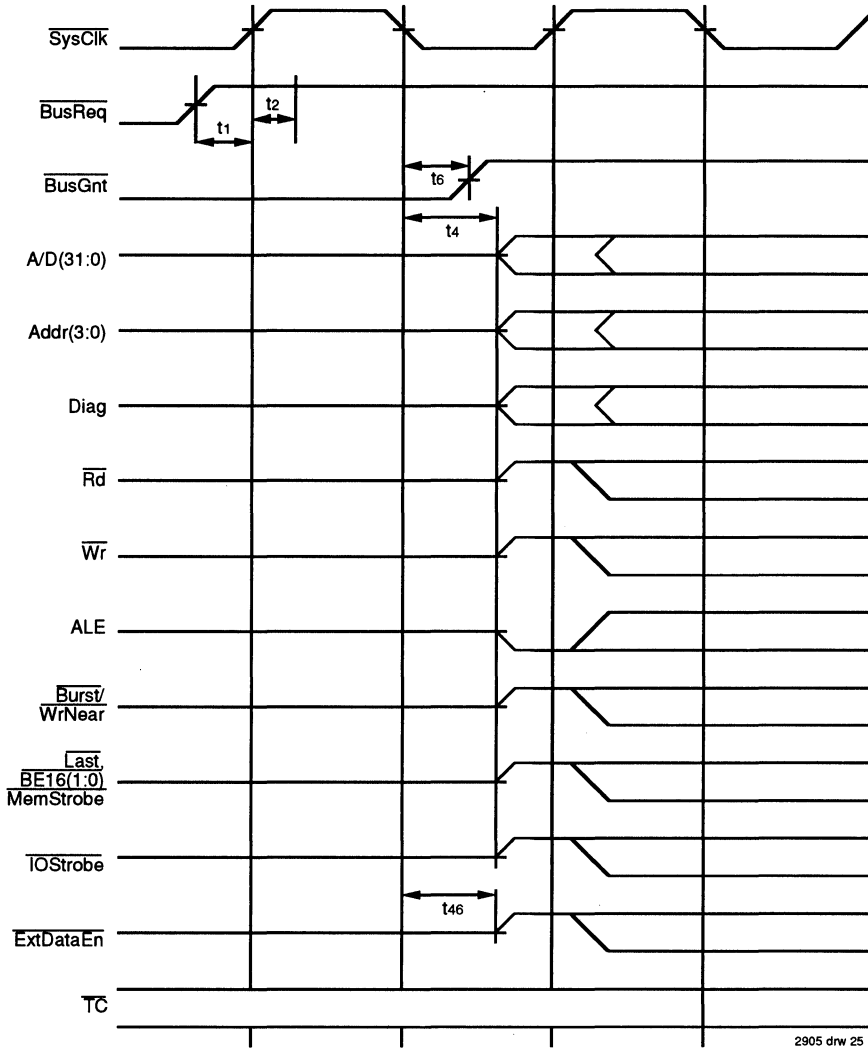


Figure 20. R3041 Regaining Bus Mastership

5

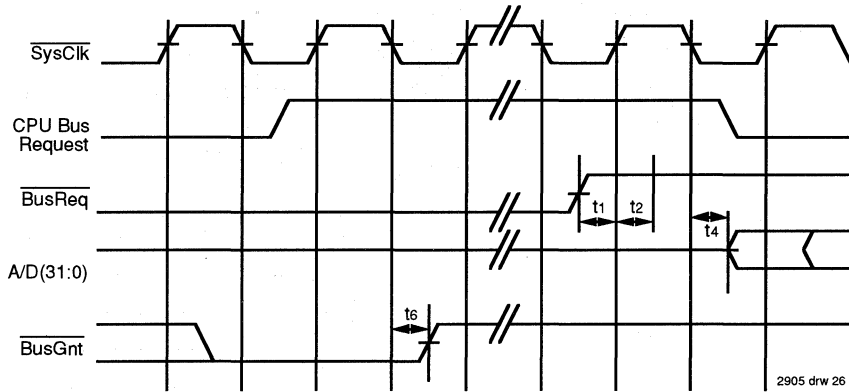


Figure 21. R3041 DMA Pulse Protocol

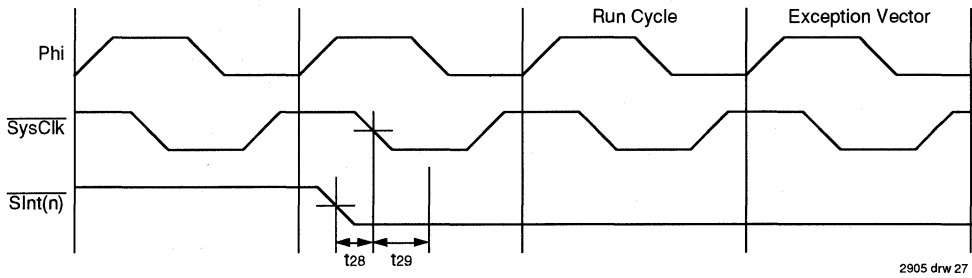


Figure 22. Synchronized Interrupt Input Timing

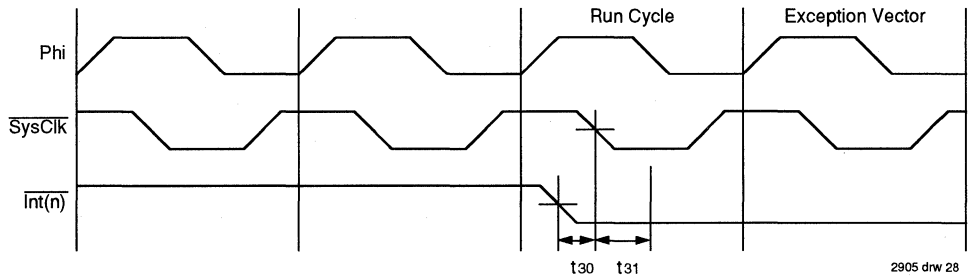


Figure 23. Direct Interrupt Input Timing

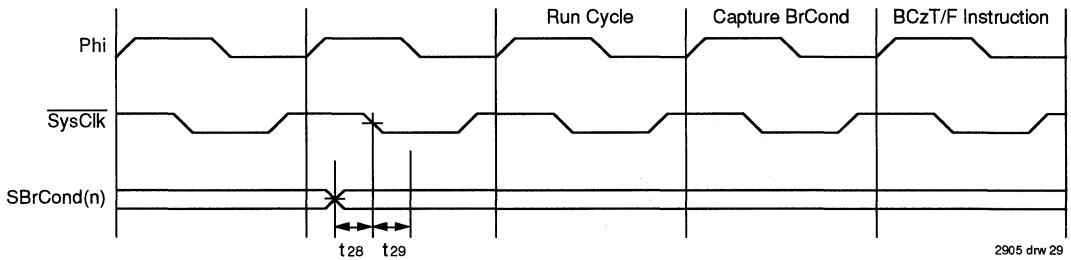


Figure 24. Synchronized Branch Condition Input Timing

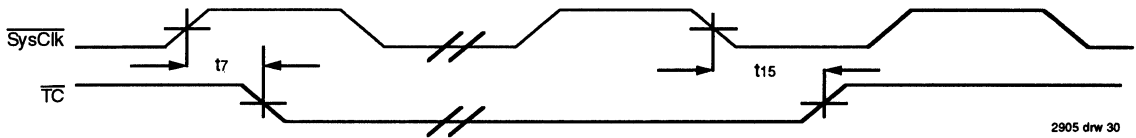
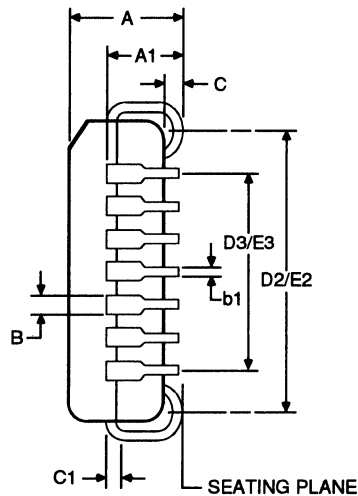
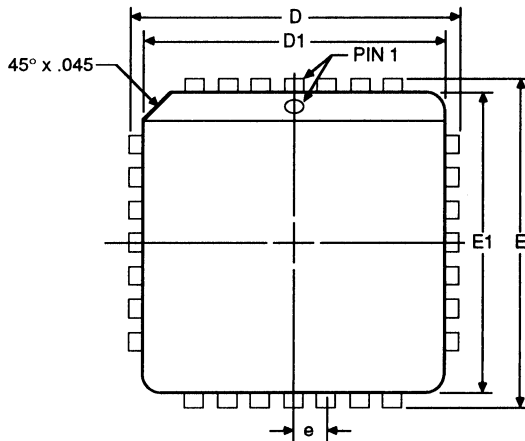


Figure 25. T-bar Output

2905 drw 30

84 LEAD PLCC (SQUARE)



2905 drw 31

5

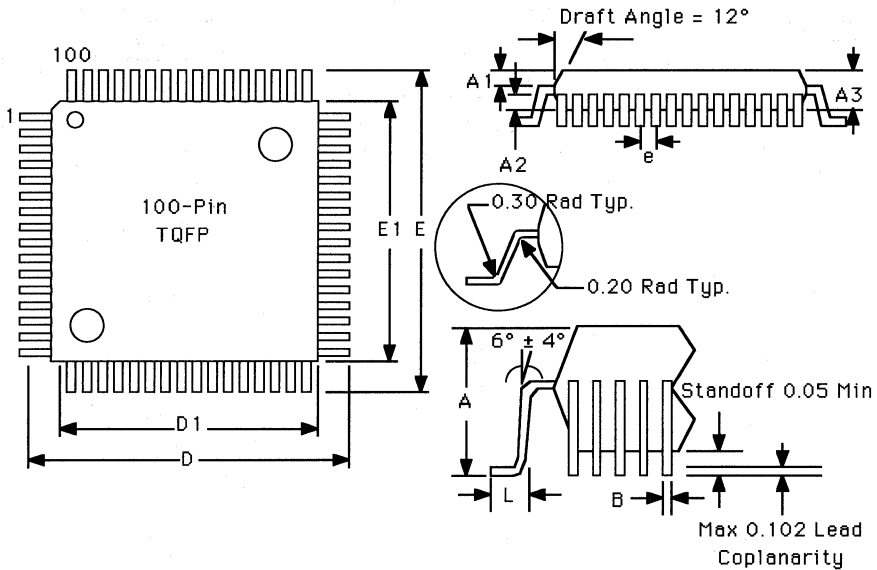
DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

2905 tbl 13

NOTES:

1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protrusions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. PLCC is pin & form compatible with MQUAD; the MQUAD package is used in other R3051 family members.

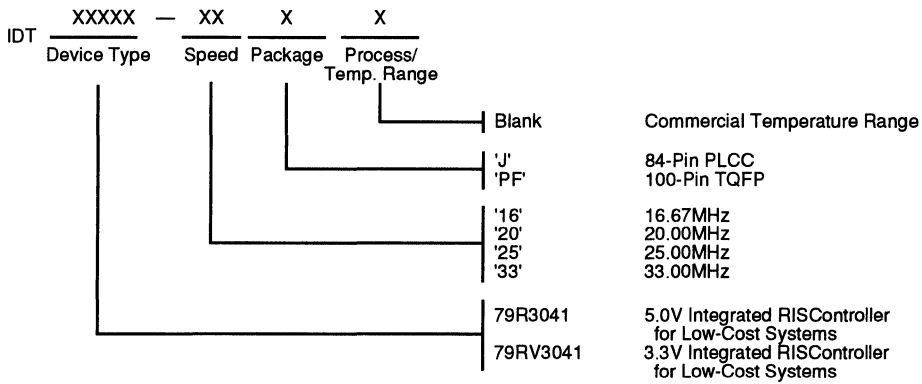
100-PIN TQFP



DWG #	TQFP	
# of Leads	100	
Symbol	Min.	Max.
A	—	1.60
A1	0.5	0.15
A2	1.35	1.45
D	15.75	16.25
D1	13.95	14.05
E	15.75	16.25
E1	13.95	14.05
L	0.45	0.70
N	100	
e	0.50BSC	
b	0.17	0.27
ccc	—	0.08
ddd	—	0.08
R	0.08	0.20
R1	0.08	—
θ	0	7.0
θ1	11.0	13.0
θ2	11.0	13.0
c	0.09	0.16

2905 tbl 14

**ORDERING INFORMATION**



2905 drw 32

**VALID COMBINATIONS**

IDT 79R3041 - 16J, 20J, 25J, 33J  
79RV3041 - 16J, 20J, 25J, 33J

5.0V, PLCC Package, Commercial Temperature Range  
3.3V, PLCC Package, Commercial Temperature Range

IDT 79R3041 - 16PF, 20PF, 25PF  
79RV3041 - 16PF, 20PF, 25PF

5.0V, TQFP Package, Commercial Temperature Range  
3.3V, TQFP Package, Commercial Temperature Range



Integrated Device Technology, Inc.

# IDT79R3051/79R3052 INTEGRATED RISControllers™

IDT79R3051™, 79R3051E  
IDT79R3052™, 79R3052E

## FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - IDT79R3000A /IDT79R3001 RISC Integer CPU
  - R3051 features 4KB of Instruction Cache
  - R3052 features 8KB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill from slow memory devices
- On-chip DMA arbiter
- Bus Interface minimizes design complexity
- Single clock input with 40%-60% duty cycle
- 35 MIPS, over 64,000 Dhrystones at 40MHz
- Low-cost 84-pin PLCC packaging that's pin-/package-compatible with thermally enhanced 84-pin MQUAD.
- Flexible bus interface allows simple, low-cost designs
- 20, 25, 33, and 40MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

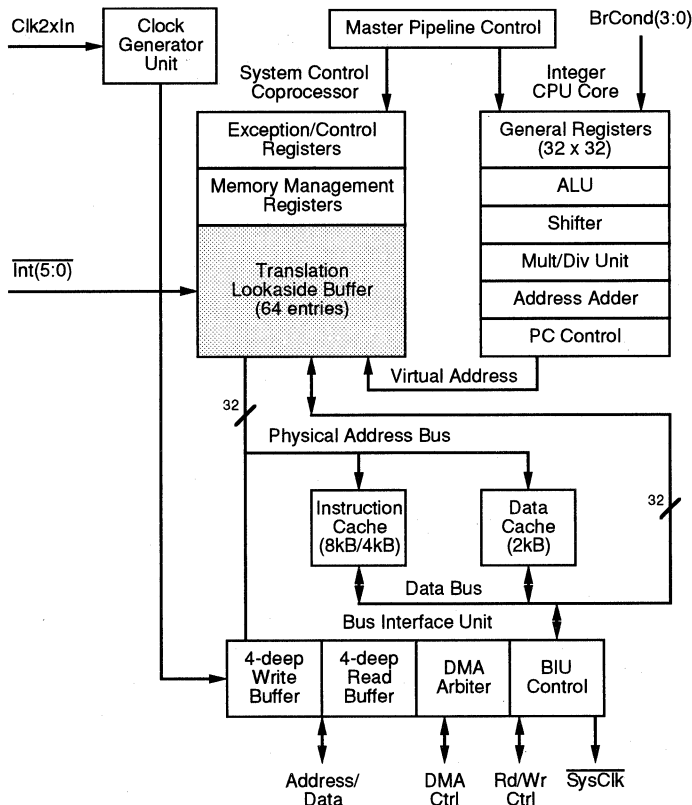


Figure 1. R3051 Family Block Diagram

2874 drw 01

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COMMERCIAL TEMPERATURE RANGE

MARCH 1994

## INTRODUCTION

The IDT IDT79R3051 family is a series of high-performance 32-bit microprocessors featuring a high level of integration which are targeted to high-performance, but cost-sensitive embedded processing applications. The IDT79R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, without significantly degrading system performance. Thus, the IDT79R3051 family is able to offer 35MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Furthermore, the IDT79R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The IDT79R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block-level representation of the functional units within the IDT79R3051 family. The IDT79R3051 family could be viewed as the embodiment of a discrete solution built around the IDT79R3000A or IDT79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the IDT79R3051 family. All devices are pin- and software-compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The IDT79R3052"E" incorporates 8kB of Instruction Cache, and features a full-function Memory Management Unit (MMU), including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same MMU incorporated into the IDT79R3000A and IDT79R3001.
- The IDT79R3052 also incorporates 8kB of Instruction Cache. However, the MMU is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The IDT79R3051 "E" incorporates 4KB of Instruction Cache. Additionally, this device features the same full-function MMU (including TLB file) as the IDT79R3052"E", and IDT79R3000A.
- The IDT79R3051 incorporates 4KB of Instruction Cache, and uses the simpler memory management model of the IDT79R3052.

An overview of the functional blocks incorporated in these devices follows.

### CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close-to single cycle execution rate. The CPU core contains a five stage pipeline and 32 orthogonal 32-bit registers. The IDT79R3051 family implements the MIPS ISA. In fact, the execution engine of the IDT79R3051 family is the same as the execution engine of the IDT79R3000A (and IDT79R3001). Thus the IDT79R3051 family is binary-compatible with those CPU engines.

The execution engine of the IDT79R3051 family uses a five-stage pipeline to achieve close-to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the IDT79R3051 family pipeline.

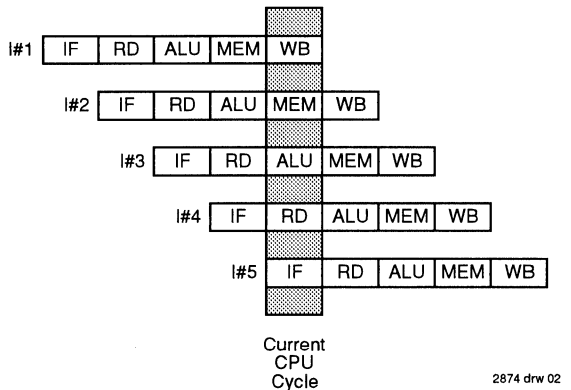


Figure 2. R3051 Family 5-Stage Pipeline

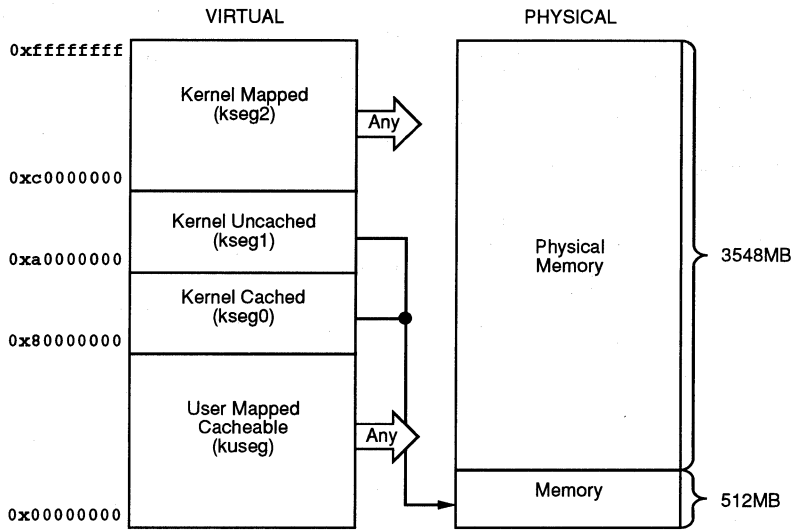
### System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the IDT79R3051 family, as well as the virtual to physical mapping of the IDT79R3051 family.

There are two versions of the IDT79R3051 family architecture: the Extended Architecture Versions (the IDT79R3051E and IDT79R3052E) contain a fully associative 64-entry TLB which maps 4KB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4GB physical address space. In this TLB, 8-page translations can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT79R3000A and IDT79R3001. Figure 3 shows the virtual-to-physical address mapping found in the Extended Architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important), and can also be used to simplify system debugging.



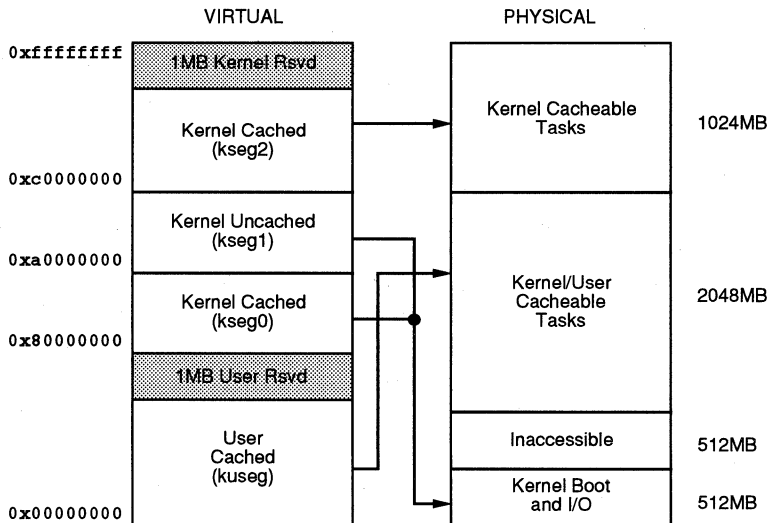


2874 drw 03

Figure 3. Virtual-to-Physical Mapping of Extended Architecture Versions

The base versions of the architecture (the IDT79R3051 and IDT79R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in Figure 4. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.



2874 drw 04

Figure 4. Virtual-to-Physical Mapping of Base Architecture Versions

### Clock Generation Unit

The IDT79R3051 family is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in IDT79R3000A and IDT79R3001 based applications.

### Instruction Cache

The current family includes two different instruction cache sizes: the IDT79R3051 family (the IDT79R3051 and IDT79R3051E) feature 4KB of instruction cache, and the IDT79R3052 and IDT79R3052E each incorporate 8KB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the IDT79R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

### Data Cache

All four devices incorporate an on-chip data cache of 2KB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the IDT79R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

### Bus Interface Unit

The IDT79R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The IDT79R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to demultiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the IDT79R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The IDT79R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed

of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate.

The IDT79R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity.

In order to accommodate slower quad-word reads, the IDT79R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

## SYSTEM USAGE

The IDT79R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application-specific peripherals. These systems may also typically contain large, slow Static RAMs, although the IDT79R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 5 shows a typical system block diagram. Transparent latches are used to de-multiplex the IDT79R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051 family A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

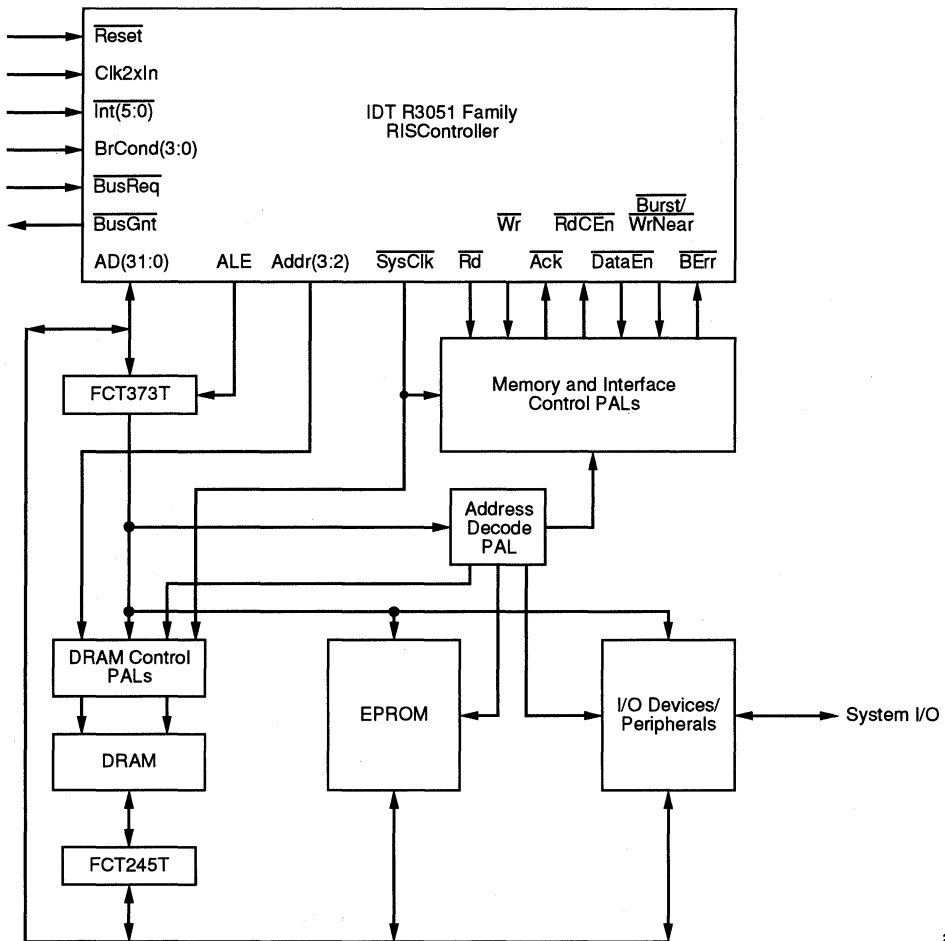
## DEVELOPMENT SUPPORT

The IDT79R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and sub-system modules.

Figure 7 is an overview of the system development process typically used when developing IDT79R3051 family-based applications. The IDT79R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for IDT79R3051/52 based applications, and include tools such as:

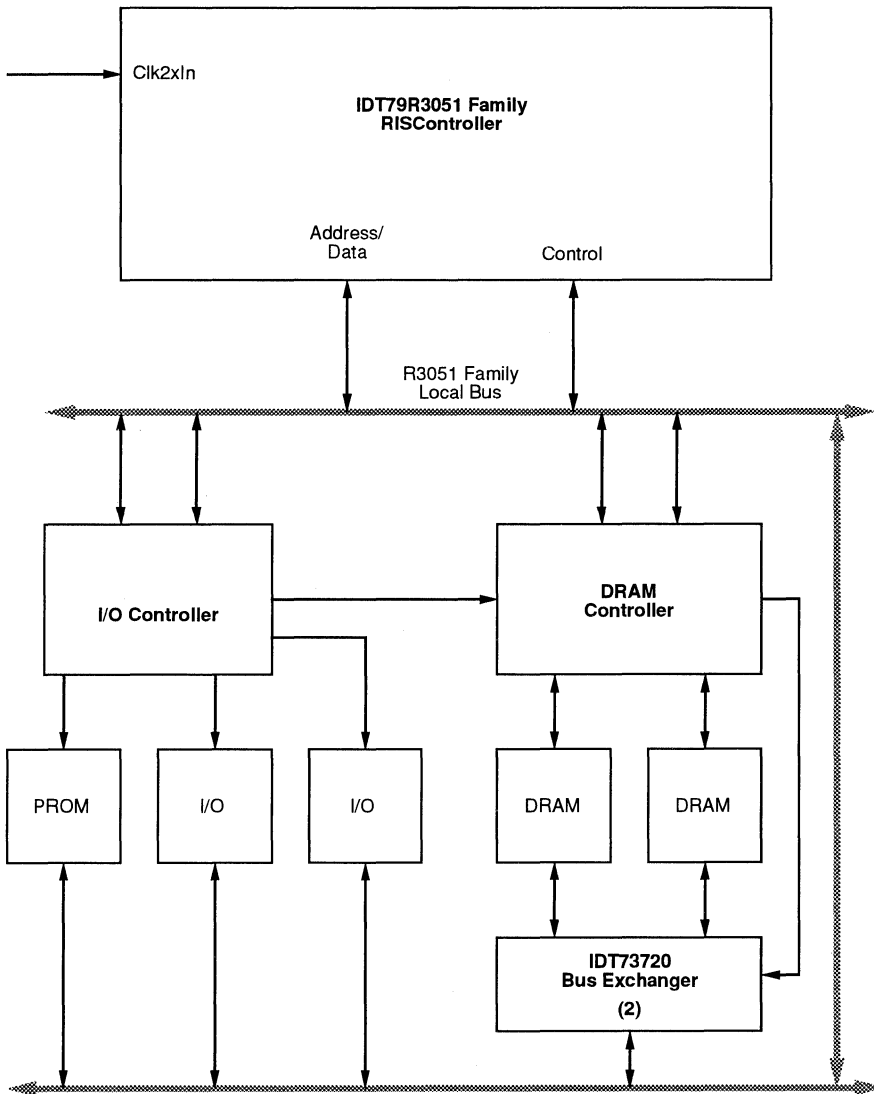
- A program, Cache-3051, which allows the performance of an IDT79R3051 family based system to be modeled and understood without requiring actual hardware.

- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, which has been integrated into the compiler toolchain to allow software floating point to replace hardware floating point without modifying the original source code.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT79R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- An In-Circuit Emulator, developed and sold by Embedded Performance, Inc.



2874 drw 05

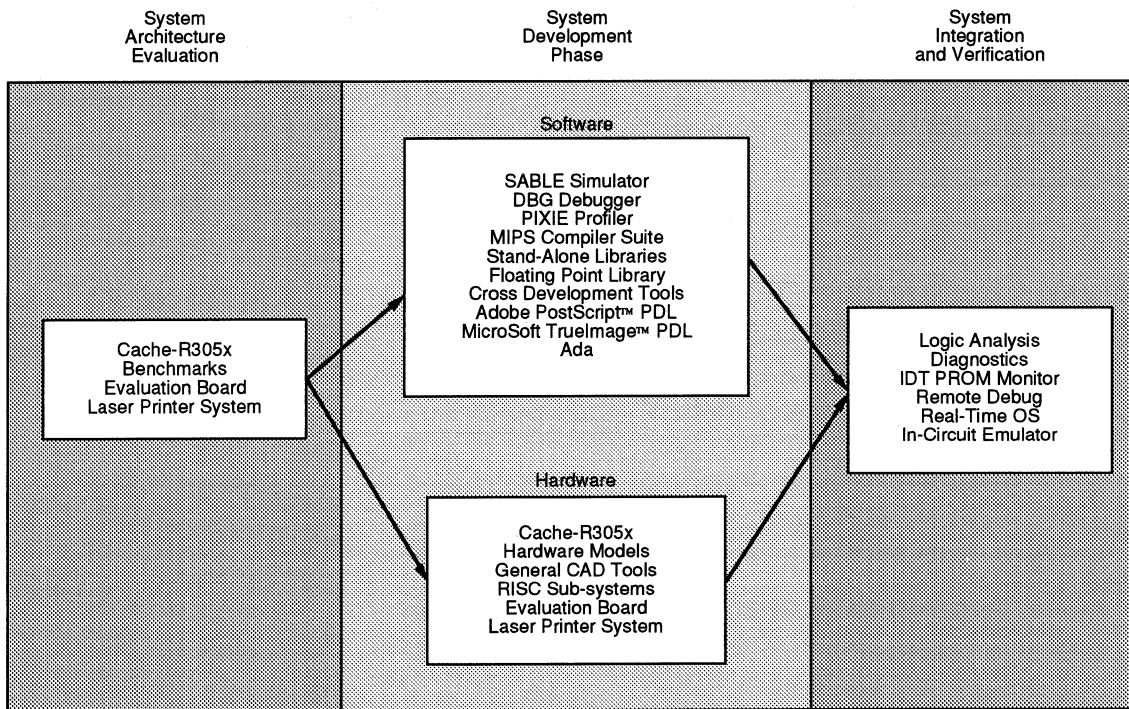
Figure 5. Typical R3051 Family Based System



2874 drw 06

Figure 6. R3051 Family Chip Set Based System

5



2874 drw 07

Figure 7. R3051 Family Development Toolchain

## PERFORMANCE OVERVIEW

The IDT79R3051 family achieves a very high level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and a branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35MIPS performance when operating out of cache.
- **Large on-chip caches.** The IDT79R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance, very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The IDT79R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the IDT79R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The IDT79R3051 family features a four-deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The IDT79R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35MIPS integer performance, and over 64,000 dhrystones at 40MHz without the use of external caches or zero wait-state memory devices.

## SELECTABLE FEATURES

The IDT79R3051 family allows the system designer to configure some aspects of operation. These aspects are established when the device is reset and include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communications between various types of processors and databases.
- **Data cache refill of one or four words:** The memory system must be capable of performing 4-word transfers to satisfy cache misses. This option allows the system designer to choose between one- and four-word refill on data cache misses, depending on the performance each option brings to his application.

## THERMAL CONSIDERATIONS

The IDT79R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the IDT79R3051 family are packaged in cavity-down packaging.

The lowest cost members of the family use a standard cavity-down, injection molded PLCC package (the "J" package). This package, coupled with the power reduction techniques employed in the design of the IDT79R3051 family, allows operation at speeds to 25MHz. However, at higher speeds, additional thermal care must be taken.

For this reason, the IDT79R3051 family is also available in the MQUAD package (the "MJ" package), which is an all-aluminum package with the die attached to a normal copper lead-frame, mounted to the aluminum casing. The MQUAD allows for more efficient thermal transfer between the die and the case of the part due to the heat-spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, which reduces the temperature gradient across the package, and, therefore, presents a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin- and form-compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

The members of the IDT79R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 1 for the various packages.

$\theta_{CA}$	Airflow (ft/min)					
	0	200	400	600	800	1000
"J" Package	29	26	21	18	16	15
"MJ" Package*	22	14	12	11	9	8

2874 tbl 01

Table 1. Thermal Resistance ( $\theta_{CA}$ ) at Various Airflows  
(\*estimated; final values tbd)



## PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	<p><b>Address/Data:</b> A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer.</p> <p>Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of:</p> <p><b>Address(31:4):</b> The high-order address for the transfer is presented on A/D(31:4).</p> <p><b><math>\overline{BE}</math>(3:0):</b> These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are represented on A/D(3:0).</p> <p>During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.</p>
Addr(3:2)	O	<p><b>Low Address (3:2)</b> A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.</p>
Diag(1)	O	<p><b>Diagnostic Pin 1.</b> This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed:</p> <p><b>Cached:</b> During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss. The value of this pin at this time in other than read cycles is undefined.</p> <p><b>Miss Address (3):</b> During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p>
Diag(0)	O	<p><b>Diagnostic Pin 0.</b> This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed:</p> <p><b><math>\overline{ID}</math>:</b> If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase.</p> <p><b>Miss Address (2):</b> During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p>
ALE	O	<p><b>Address Latch Enable:</b> Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.</p>
$\overline{DataEn}$	O	<p><b>External Data Enable:</b> This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.</p>

**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Burst}}$ $\overline{\text{WrNear}}$	O	<p><b>Burst Transfer/Write Near:</b> On read transactions, the <math>\overline{\text{Burst}}</math> signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time.</p> <p>On write transactions, the <math>\overline{\text{WrNear}}</math> output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.</p>
$\overline{\text{Rd}}$	O	<b>Read:</b> An output which indicates that the current bus transaction is a read.
$\overline{\text{Wr}}$	O	<b>Write:</b> An output which indicates that the current bus transaction is a write.
$\overline{\text{Ack}}$	I	<b>Acknowledge:</b> An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
$\overline{\text{RdCEn}}$	I	<b>Read Buffer Clock Enable:</b> An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{\text{SysClk}}$	O	<b>System Reference Clock:</b> An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
$\overline{\text{BusReq}}$	I	<b>DMA Arbiter Bus Request:</b> An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{\text{BusGnt}}$	O	<b>DMA Arbiter Bus Grant.</b> An output from the CPU used to acknowledge that a $\overline{\text{BusReq}}$ has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	<b>Branch Condition Port:</b> These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
$\overline{\text{BErr}}$	I	<b>Bus Error:</b> Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{\text{Int}}(5:3)$ $\overline{\text{SInt}}(2:0)$	I	<p><b>Processor Interrupt:</b> During normal operation, these signals are logically the same as the <math>\overline{\text{Int}}(5:0)</math> signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000.</p> <p>There are two types of interrupt inputs: the <math>\overline{\text{SInt}}</math> inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.</p>
$\overline{\text{Clk2xIn}}$	I	<b>Master Clock Input:</b> This is a double frequency input used to control the timing of the CPU.
$\overline{\text{Reset}}$	I	<b>Master Processor Reset:</b> This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{\text{Reset}}$ .
Rsvd(4:0)	I/O	<b>Reserved:</b> These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

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**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>C</sub>	Operating Case Temperature	0 to +85	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +155	°C
V <sub>IN</sub>	Input Voltage	-0.5 to +7.0	-0.5 to +7.0	V

**NOTES:**

2874 tbl 04

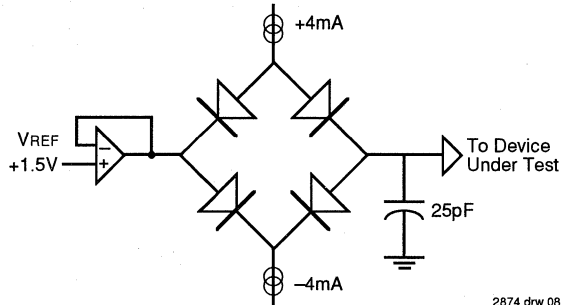
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -3.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> + 0.5V.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2874 tbl 06

**OUTPUT LOADING FOR AC TESTING**



2874 drw 08

**AC TEST CONDITIONS**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.0	—	V
V <sub>IL</sub>	Input LOW Voltage	—	0.4	V
V <sub>IHS</sub>	Input HIGH Voltage	3.5	—	V
V <sub>ILS</sub>	Input LOW Voltage	—	0.4	V

2874 tbl 05

**DC ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)**

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V <sub>IHS</sub>	Input HIGH Voltage <sup>(2,3)</sup>	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V <sub>ILS</sub>	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C <sub>IN</sub>	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
C <sub>OUT</sub>	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	pF
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = 5V, T <sub>C</sub> = 25°C	—	400	—	450	—	600	—	700	mA
I <sub>IH</sub>	Input HIGH Leakage	V <sub>IH</sub> = V <sub>CC</sub>	—	100	—	100	—	100	—	100	µA
I <sub>IL</sub>	Input LOW Leakage	V <sub>IL</sub> = GND	-100	—	-100	—	-100	—	-100	—	µA
I <sub>OZ</sub>	Output Tri-state Leakage	V <sub>OH</sub> = 2.4V, V <sub>OL</sub> = 0.5V	-100	100	-100	100	-100	100	-100	100	µA

**NOTES:**

2874 tbl 07

- V<sub>IL</sub> Min. = -3.0V for pulse width less than 15ns. V<sub>IL</sub> should not fall below -0.5V for larger periods.
- V<sub>IHS</sub> and V<sub>ILS</sub> apply to Clk2xIn and Reset.
- V<sub>IH</sub> should not be held above V<sub>CC</sub> + 0.5V.
- Guaranteed by design.

**AC ELECTRICAL CHARACTERISTICS (1, 2, 3)** ( $T_C = 0^\circ\text{C}$  to  $+95^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 5\%$ )

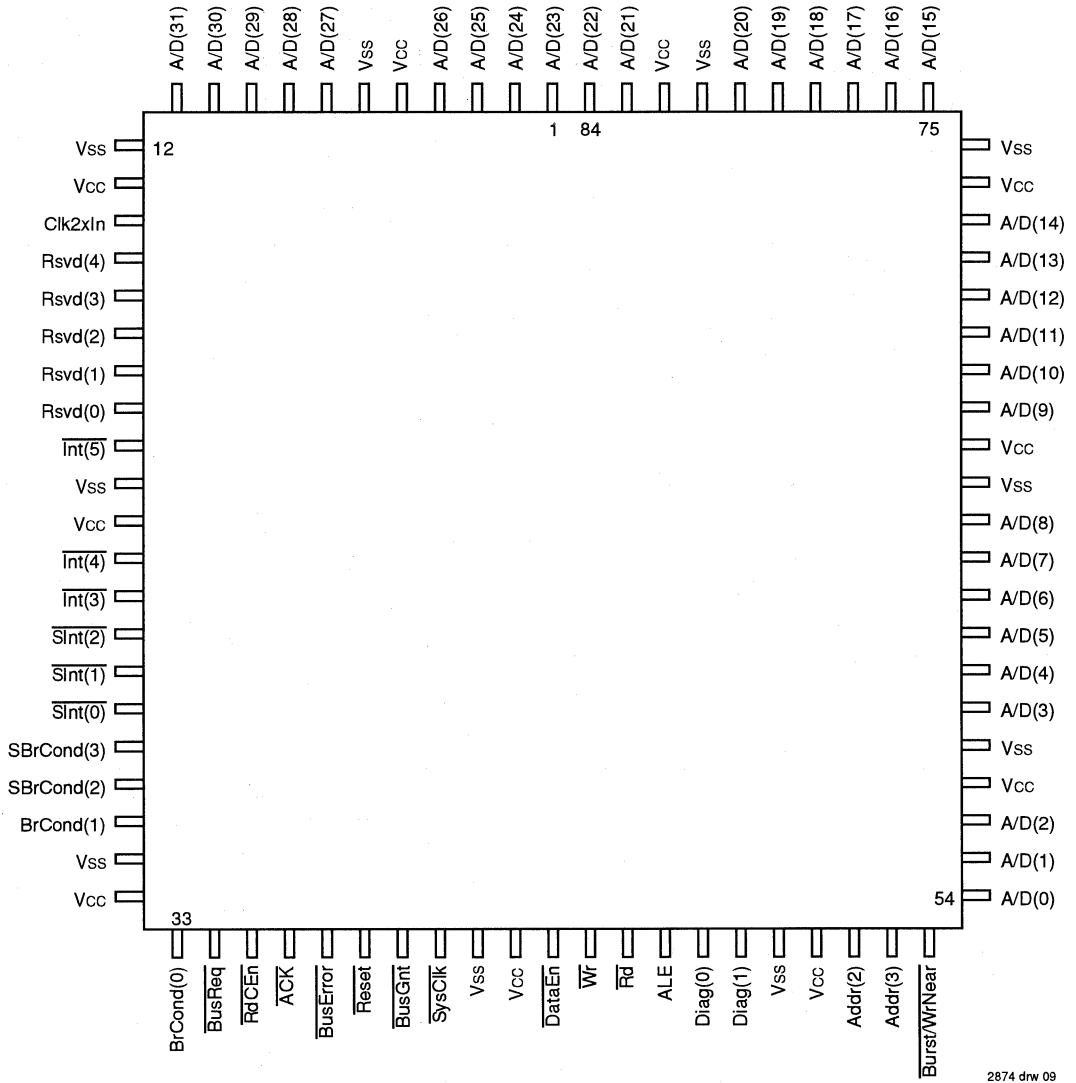
Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn,	Set-up to $\overline{\text{SysClk}}$ rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	5	—	4.5	—	ns
t2	BusReq, Ack, BusError, RdCEn,	Hold from $\overline{\text{SysClk}}$ rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ Burst/ $\overline{\text{WrNear}}$ , Rd, DataEn	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ Burst/ $\overline{\text{WrNear}}$ , Rd, DataEn	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	8	—	7	—	6	—	5	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	8	—	7	—	6	—	5	ns
t7	$\overline{\text{Wr}}$ , Rd, Burst/ $\overline{\text{WrNear}}$ , A/D	Valid from $\overline{\text{SysClk}}$ rising	—	5	—	5	—	4	—	3.5	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	4	—	4	—	3	—	3	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	4	—	4	—	3	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from $\overline{\text{SysClk}}$ falling	—	15	—	15	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising <sup>(4)</sup>	0	—	0	—	0	—	0	—	ns
t15	$\overline{\text{Wr}}$ , Rd, DataEn, Burst/ $\overline{\text{WrNear}}$	Negated from $\overline{\text{SysClk}}$ falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from $\overline{\text{SysClk}}$	—	6	—	6	—	5	—	4.5	ns
t17	Diag	Valid from $\overline{\text{SysClk}}$	—	12	—	11	—	10	—	9	ns
t18	A/D	Tri-state from $\overline{\text{SysClk}}$ falling	—	10	—	10	—	9	—	8	ns
t19	A/D	$\overline{\text{SysClk}}$ falling to data out	—	12	—	11	—	10	—	9	ns
t20	Clk2xIn	Pulse Width HIGH	10	—	8	—	6.5	—	5.6	—	ns
t21	Clk2xIn	Pulse Width LOW	10	—	8	—	6.5	—	5.6	—	ns
t22	Clk2xIn	Clock Period	25	250	20	250	15	250	12.5	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	$\mu\text{s}$
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	6	—	5	—	4	—	3	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{\text{SInt}}$ , SBrCond	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t29	$\overline{\text{SInt}}$ , SBrCond	Hold from $\overline{\text{SysClk}}$ falling	3	—	3	—	2	—	2	—	ns
t30	$\overline{\text{Int}}$ , BrCond	Set-up to $\overline{\text{SysClk}}$ falling	6	—	5	—	4	—	3	—	ns
t31	$\overline{\text{Int}}$ , BrCond	Hold from $\overline{\text{SysClk}}$ falling	3	—	3	—	2	—	2	—	ns
tsys	$\overline{\text{SysClk}}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	$\overline{\text{SysClk}}$	Clock HIGH Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
t33	$\overline{\text{SysClk}}$	Clock LOW Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 1	t22 + 1	t22 - 1	t22 + 1	ns
tderate	All outputs	Timing deration for loading over 25pF <sup>(4, 5)</sup>	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

**NOTES:**

- All timings referenced to 1.5V, with a rise and fall time of less than 2.5ns.
- All outputs tested with 25pF loading.
- The AC values listed here reference timing diagrams contained in the R3051 Family Hardware User's Manual.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.

2874 tbl 08

**PIN CONFIGURATIONS**



2874 drw 09

**84-Pin PLCC/MQUAD**  
**Top View**

**NOTE:**  
Reserved Pins must not be connected.

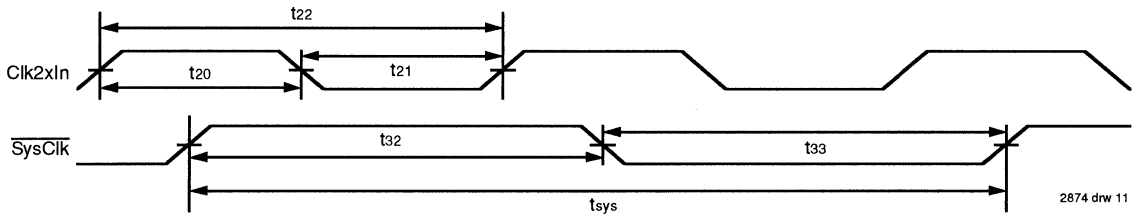


Figure 8. R3051 Family Clocking

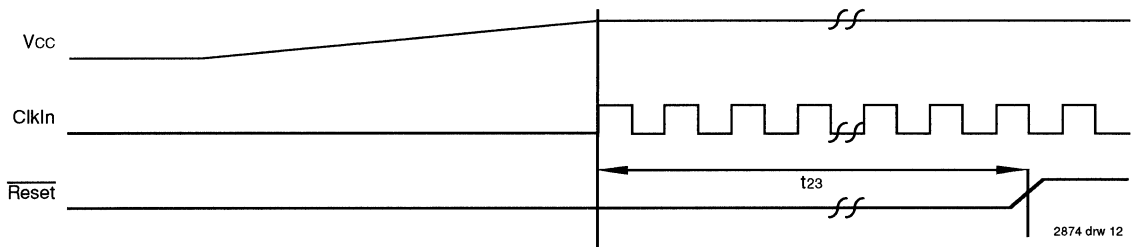


Figure 9. Power-On Reset Sequence

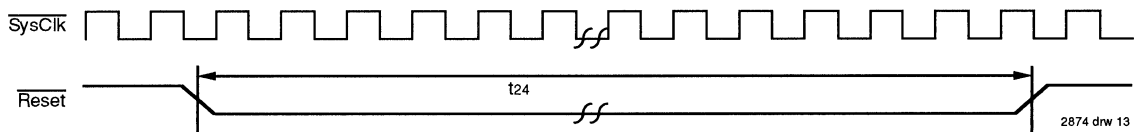


Figure 10. Warm Reset Sequence

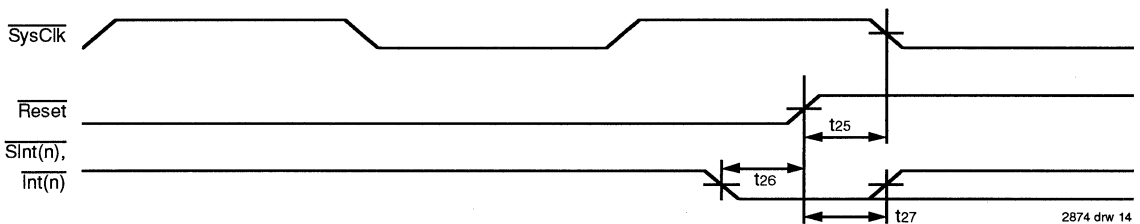


Figure 11. Mode Selection and Negation of Reset

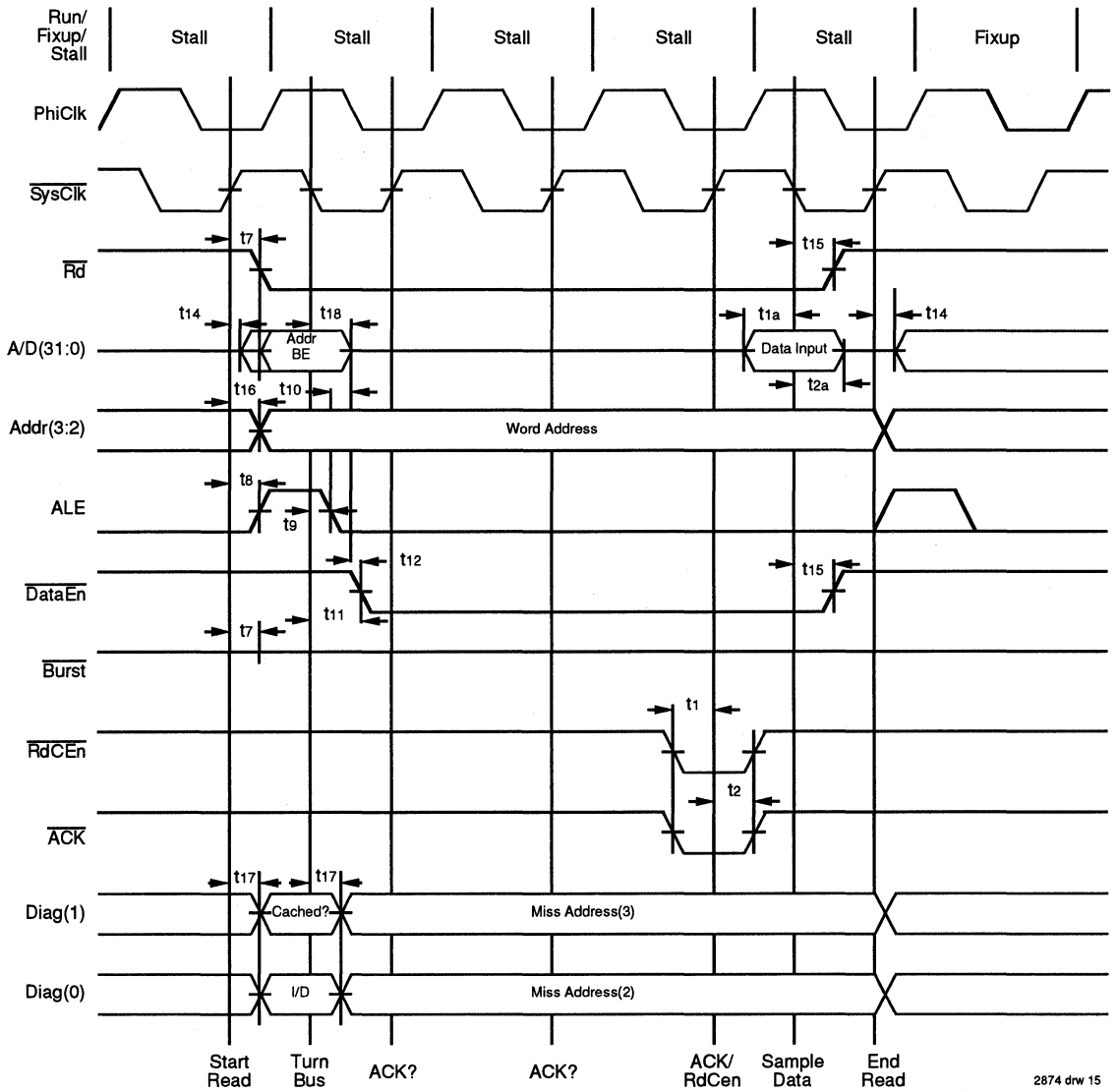


Figure 12. Single Datum Read in R3051 Family

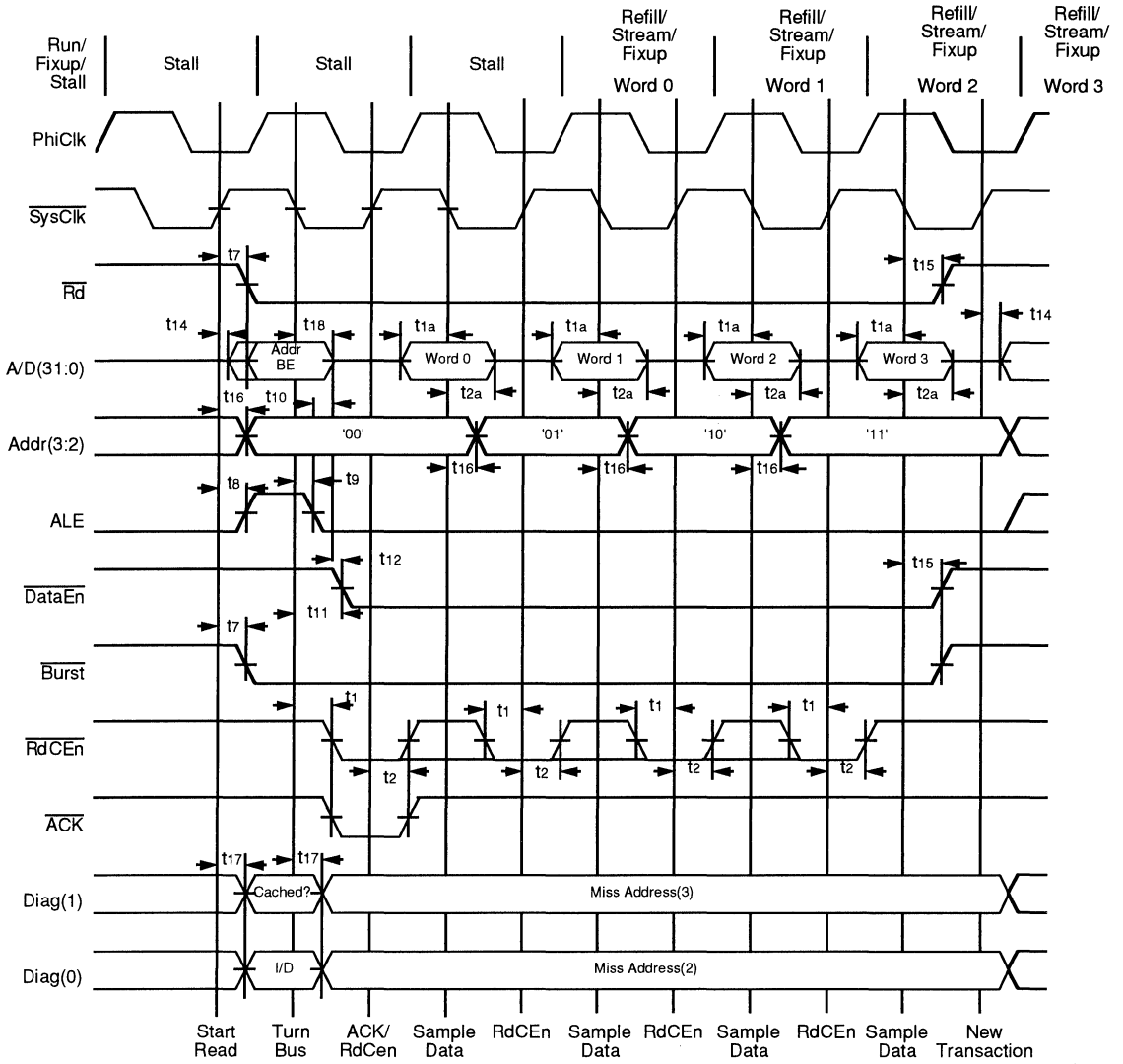


Figure 13. R3051 Family Burst Read

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2874 drw 16

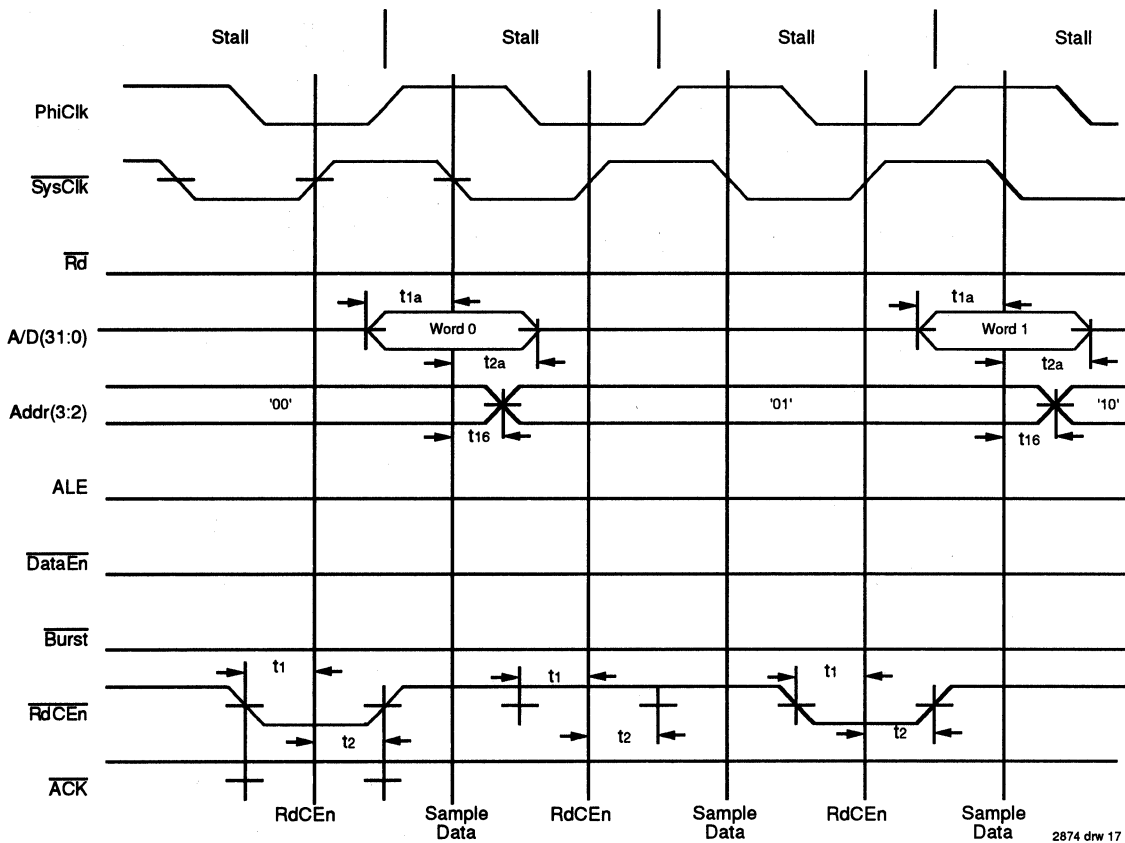
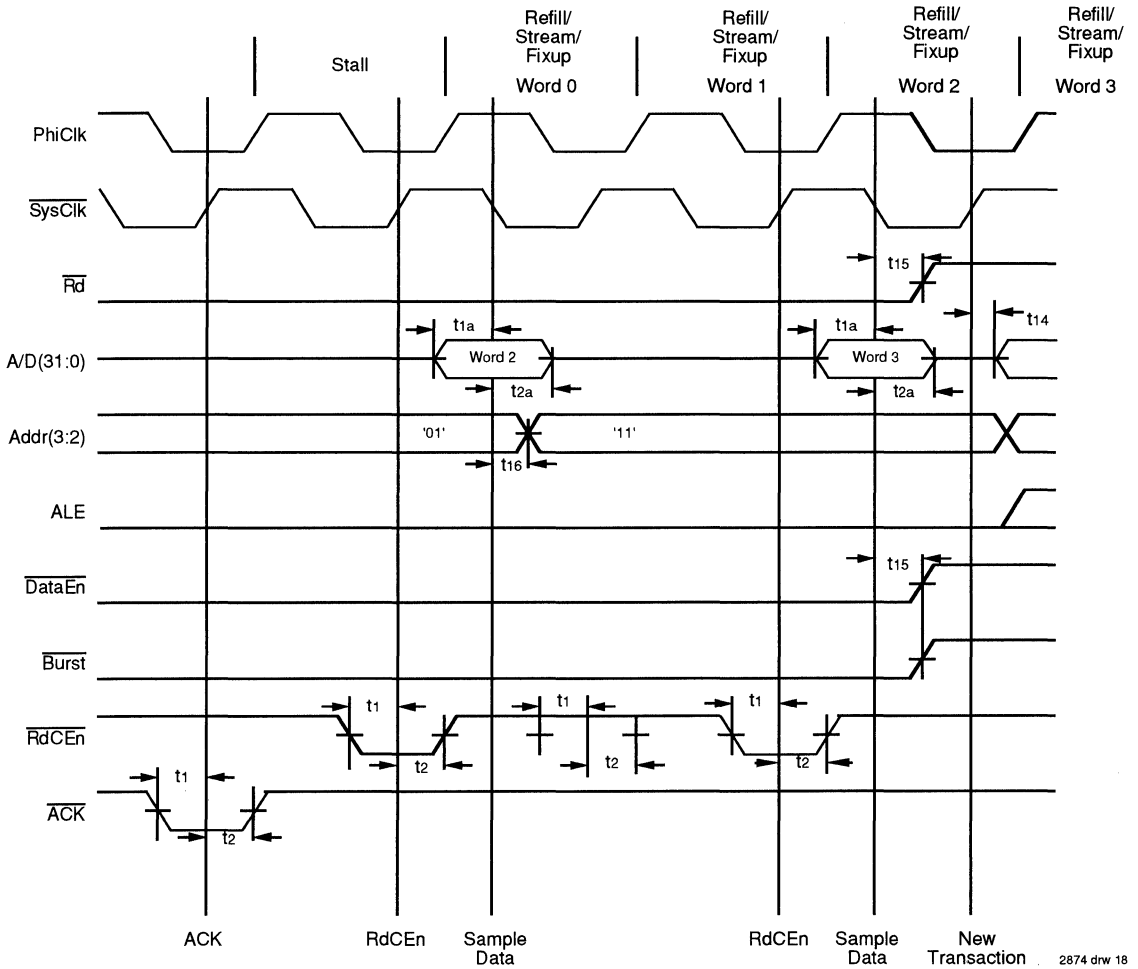


Figure 14 (a). Start of Throttled Quad Read

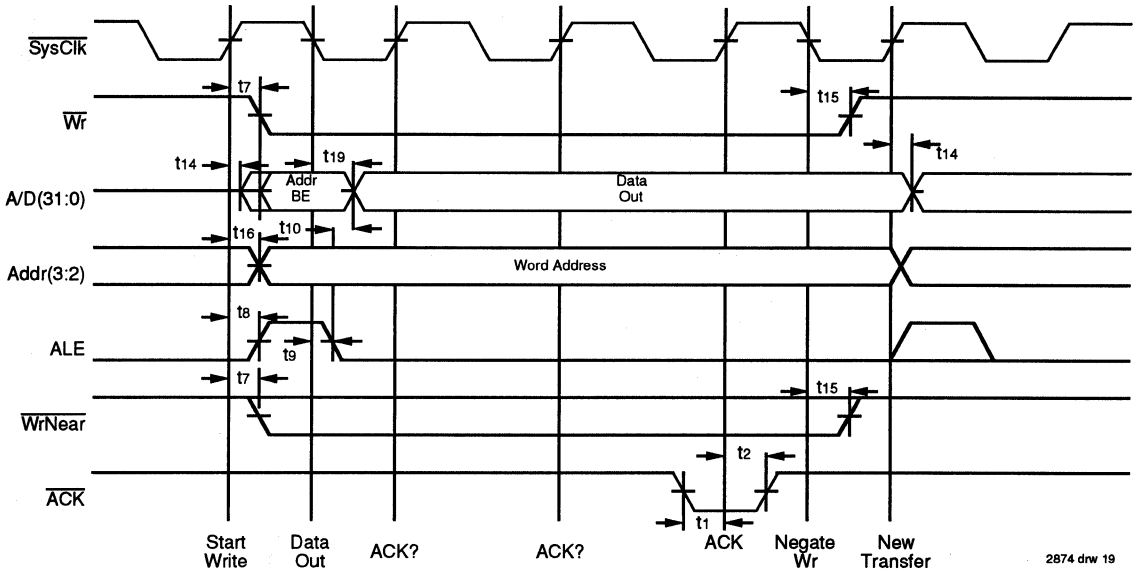


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Figure 14 (b). End of Throttled Quad Read

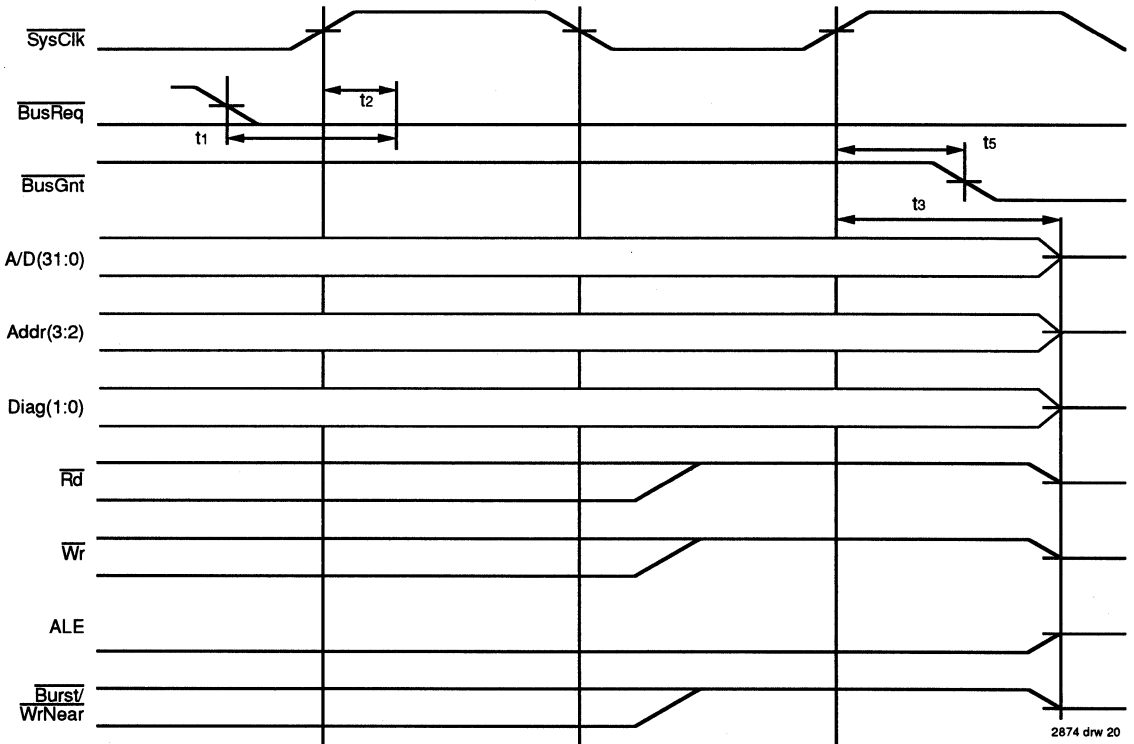
2874 drw 18





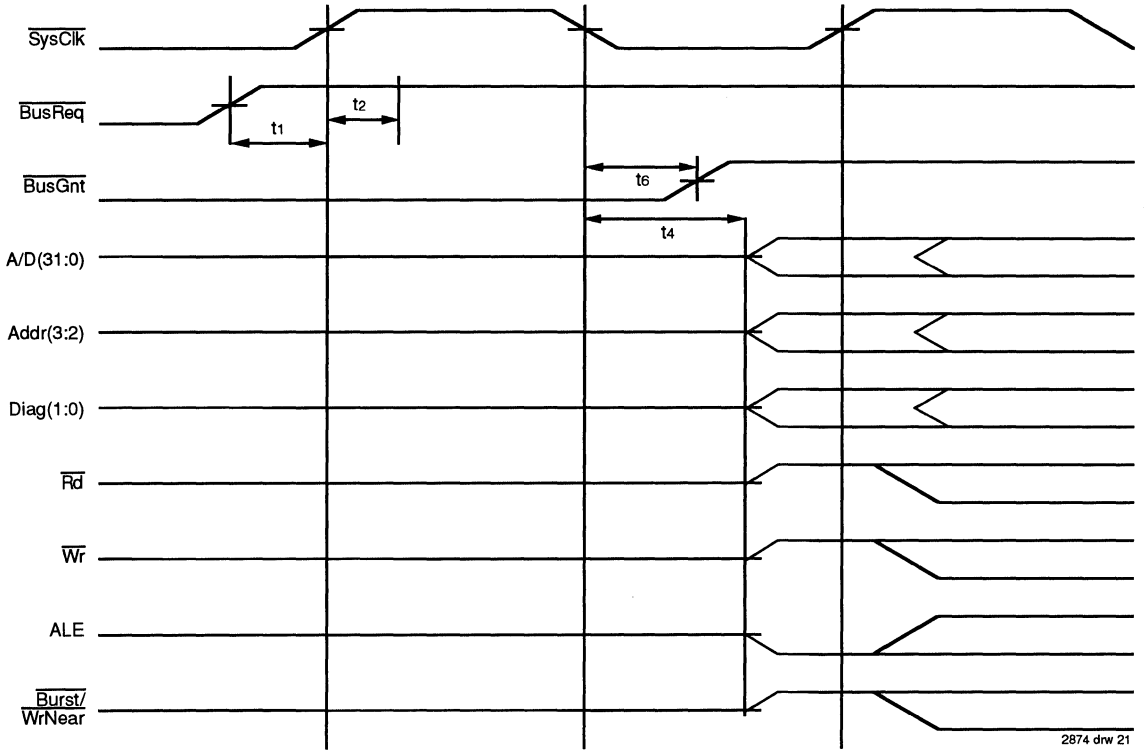
2874 drw 19

Figure 15. R3051 Family Write Cycle



2874 drw 20

Figure 16. Request and Relinquish of R3051 Family Bus to External Master



2874 drw 21

Figure 17. R3051 Family Regaining Bus Mastership

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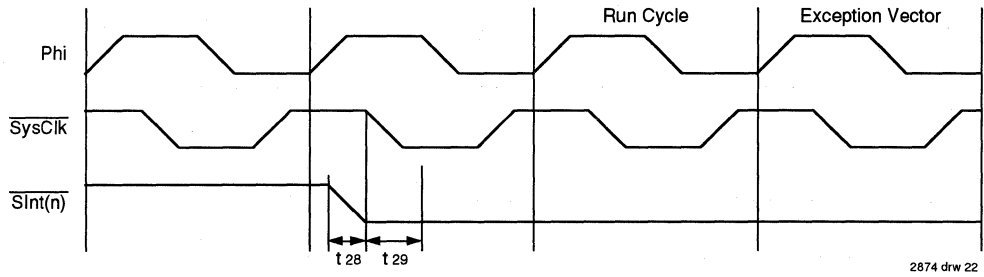


Figure 18. Synchronized Interrupt Input Timing

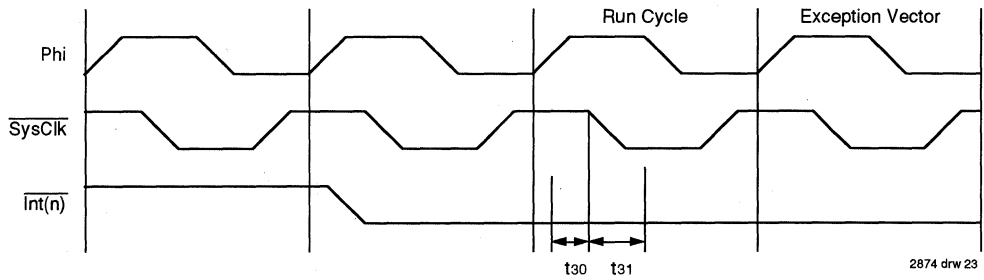


Figure 19. Direct Interrupt Input Timing

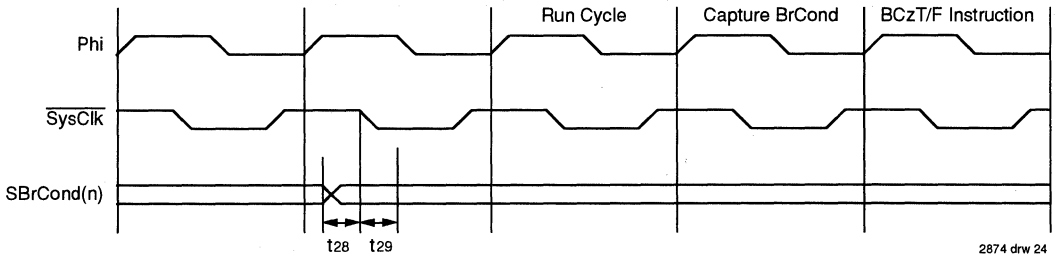


Figure 20. Synchronized Branch Condition Input Timing

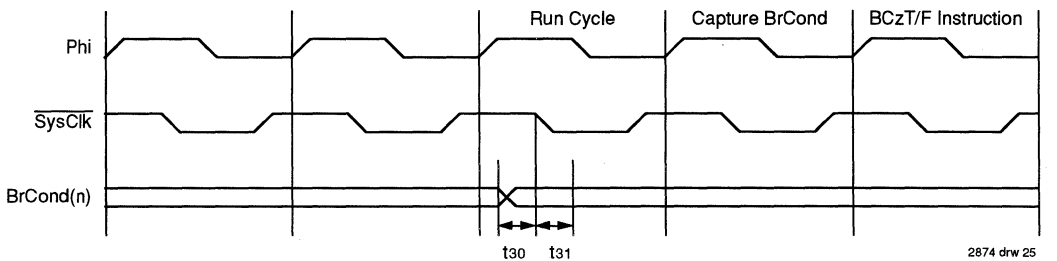
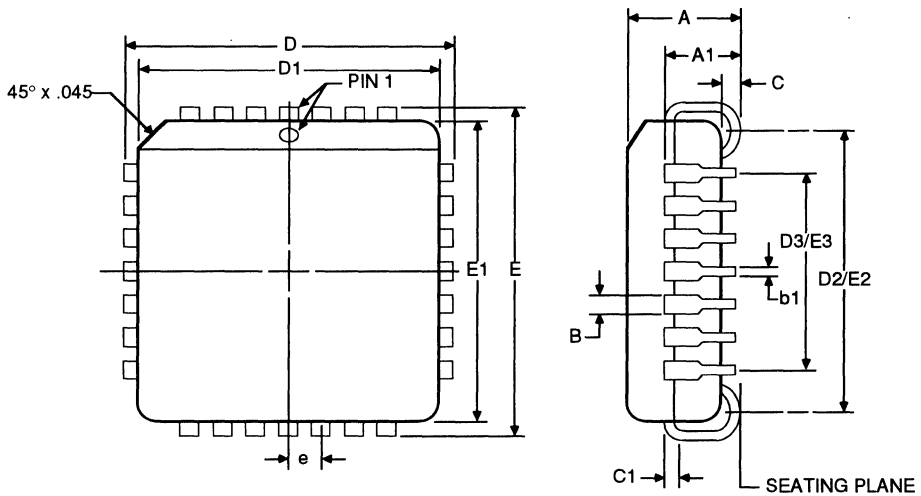


Figure 21. Direct Branch Condition Input Timing

84 LEAD PLCC/MQUAD<sup>(7)</sup> (SQUARE)



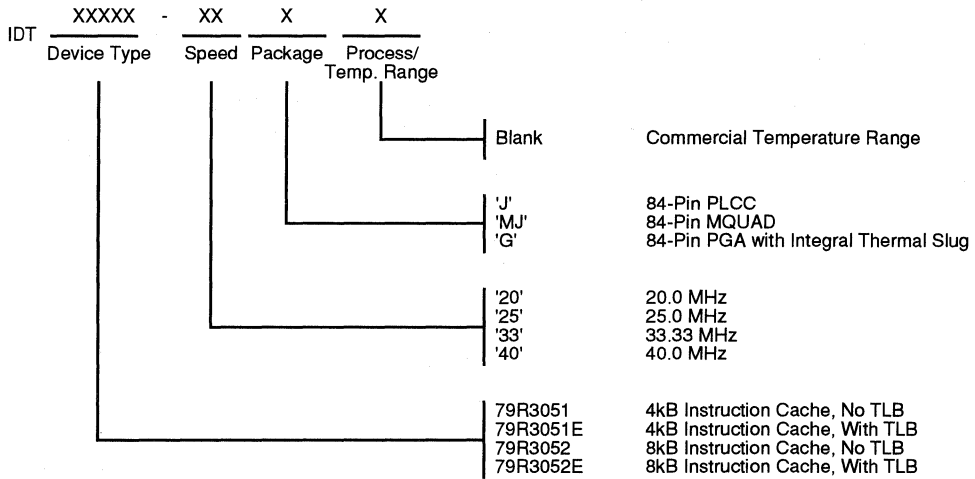
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NOTES:

1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protrusions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. MQUAD is pin & form compatible with PLCC.

DWG #	J84-1		MJ84-1	
# of Leads	84		84	
Symbol	Min.	Max.	Min.	Max.
A	165	.180	165	.180
A1	.095	.115	.094	.114
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	1.185	1.195	1.185	1.195
D1	1.150	1.156	1.140	1.150
D2/E2	1.090	1.130	1.090	1.130
D3/E3	1.000 REF		1.000 REF	
E	1.185	1.195	1.185	1.195
E1	1.150	1.156	1.140	1.150
e	.050 BSC		.050 BSC	
ND/NE	21		21	

**ORDERING INFORMATION**



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**VALID COMBINATIONS**

IDT 79R3051 - 20, 25	All packages
79R3051E - 20, 25	All packages
79R3052 - 20, 25	All packages
79R3052E - 20, 25	All packages
79R3051 - 33, 40	PGA, MJ Packages Only
79R3051E - 33, 40	PGA, MJ Packages Only
79R3052 - 33, 40	PGA, MJ Packages Only
79R3052E - 33, 40	PGA, MJ Packages Only



Integrated Device Technology, Inc.

# IDT79R3071™ RISController™

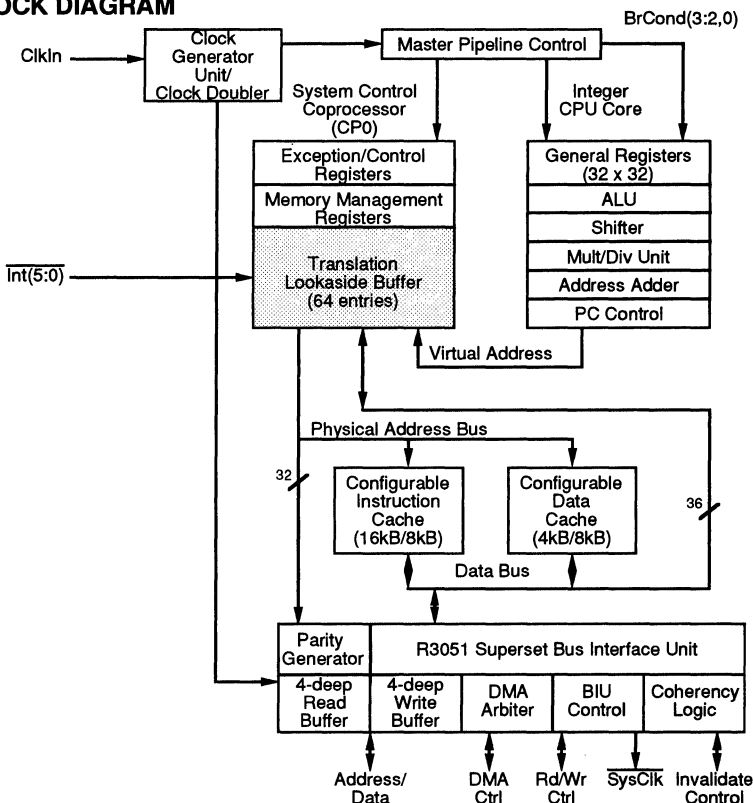
IDT79R3071  
IDT79R3071E

## FEATURES

- Instruction set compatible with IDT79R3000A, R3051™, and R3500 RISC CPUs
- High level of integration minimizes system cost
  - R3000A Compatible CPU
  - Optional R3000A compatible MMU
  - Large Instruction Cache
  - Large Data Cache
  - Read/Write Buffers
- 35VUPS at 40MHz
  - 320MB/sec on-chip bandwidth
  - 160MB/sec bus bandwidth
- Flexible bus interface allows simple, low-cost designs
- 1x clock input
- 33- through 50MHz operation
- 50MHz at 1x clock input and 1/2 bus frequency
- Superset pin- and software-compatible with R3041™, R3051, R3052™, and R3081™

- Large on-chip caches with user configurability
  - 16kB Instruction Cache, 4kB Data Cache
  - Dynamically configurable to 8kB Instruction Cache, 8kB Data Cache
  - Parity protection over data and tag fields
- Low cost 84-pin packaging
- Multiplexed bus interface with support for low-cost, low-speed memory systems with a high-speed CPU
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-deep read buffer supports burst or simple block reads
- On-chip DMA arbiter
- Hardware-based Cache Coherency Support
- Programmable power reduction mode
- Bus Interface operates only at half-processor frequency

## R3071 BLOCK DIAGRAM



3045 drw 01

The IDT logo is a registered trademark, and RISController, R3041, R3051, R3052, R3071, R3081, R4400, R4600, IDT/sim, and IDT/kit are trademarks of Integrated Device Technology, Inc. All others are trademarks of their respective companies.

COMMERCIAL TEMPERATURE RANGE

MARCH 1994

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## INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, which is targeted to high-performance but cost-sensitive processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35VUPS performance at 40MHz without requiring external SRAM or caches.

The R3071 extends the capabilities of the R3051 family, by integrating additional resources into the same pin-out. The R3071 thus extends the range of applications addressed by the R3051 family, and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs, according to the price/performance goals of the end system.

An overview of this device, and quantitative electrical parameters and mechanical data, is found in this data sheet; consult the *R3071 Family Hardware User's Guide* for a complete description of this processor.

## DEVICE OVERVIEW

As part of the R3051 family, the R3071 extends the offering of a wide range of functionality in a compatible interface. The R3051 family allows the system designer to implement a single base system, and utilize interface-compatible processors of various complexity to achieve the price-performance goals of the particular end system.

Differences among the various family members pertain to the on-chip resources of the processor. Current family members are shown in Table 1, below.

Figure 1 shows a block-level representation of the functional units within the R3071E. The R3071E could be viewed as the embodiment of a discrete solution built around the R3000A and R3010A. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Device Name	Instruction Cache	Data Cache	MMU Option	FPA	Bus Options
R3041	2kB	512B	No	Software	Programmable Options Variable Port width interface
R3051	4kB	2kB	"E" version	Software	32-bit mux'ed
R3052	8kB	2kB	"E" version	Software	32-bit mux'ed
R3071	16kB	4kB or 8kB	"E" version or 8kB	Software	1/2 frequency bus only
R3081	16kB or 8kB	4kB or 8kB	"E" version	On-chip hardware	1/2 frequency bus

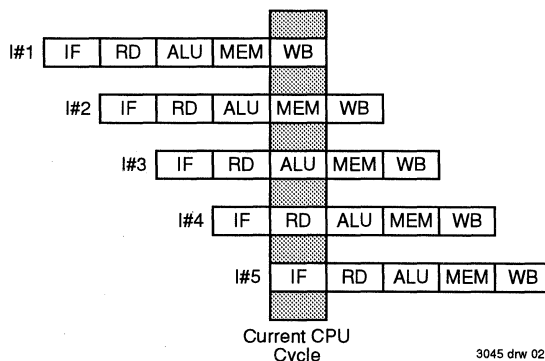
3045 tbl 01

Table 1. R3051 Family Members

### CPU Core

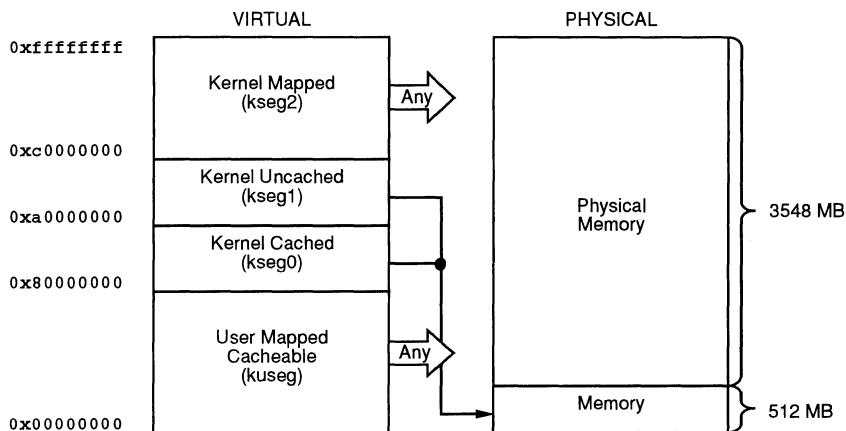
The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3071 uses the same basic integer execution core as the entire R3051 family, which is the R3000A implementation of the MIPS instruction set. Thus, the R3071 family is binary compatible with the R3051, R3052, R3000A, R3001, and R3500 CPUs. In addition, the R4000 and Orion represent an upwardly software compatible migration path to still higher levels of performance.

The execution engine in the R3071 uses a five-stage pipeline to achieve near single-cycle instruction execution rates. A new instruction can be initiated in each clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved in the R3071 execution pipeline.



3045 drw 02

Figure 2. R3071 5-Stage Pipeline



3045 drw 03

Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

**System Control Co-Processor**

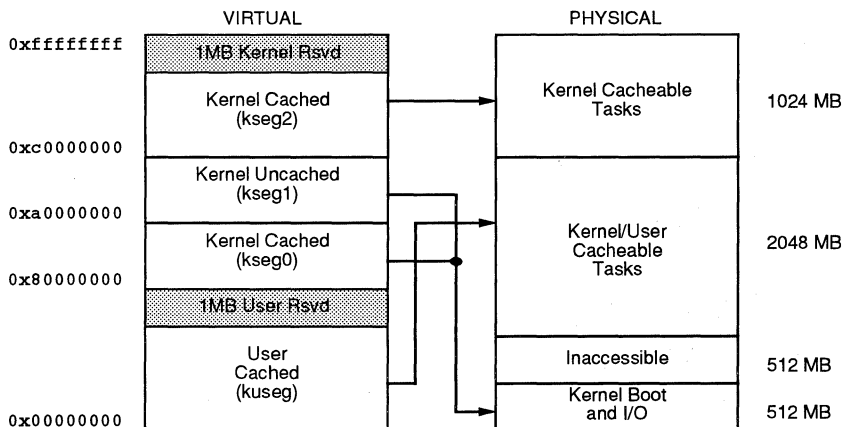
The R3071 family also integrates the System Control Co-processor, CP0, on-chip. CP0 manages both the exception handling capability of the R3071, as well as the virtual-to-physical address mapping.

As with the R3051 and R3052, the R3071 offers two versions of memory management and virtual-to-physical address mapping: the extended architecture versions, the R3051E, R3052E, and R3071E, incorporate the same MMU as the R3000A. These versions contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard-mapped to physical addresses, and kernel and user segments which are mapped page by page by the TLB into anywhere in the 4GB physical address space. In this TLB, 8 pages can be "locked" by the kernel to insure deterministic response in real-time applications. Figure 3 illustrates the virtual to physical mapping found in the R3071E.

The Extended architecture versions of the R3051 family (the R3051E, R3052E, and R3071E) allow the system designer to implement kernel software which dynamically manages User task utilization of system resources, and also allows the Kernel to protect certain resources from User tasks. These capabilities are important in general computing applications such as ARC computers, and are also important in a variety of embedded applications, from process control (where protection may be important) to X-Window display systems (where virtual memory management can be used). The MMU can also be used to simplify system debug.

R3051 family base versions (the R3051, R3052, and R3071) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. These devices still support distinct kernel and user mode operation, but do not require page management software, leading to a simpler software model. The memory mapping used by these devices is shown in Figure 4. Note that the reserved spaces are for compatibility with future family members, which may map on-

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3045 drw 04

Figure 4. Virtual to Physical Mapping of Base Architecture Versions



chip resources to these addresses. References to these addresses in the R3071 will be translated in the same fashion as the rest of their respective segments, with no traps or exceptions signalled.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to implement page management software. This distinction can be implemented by decoding the output physical address. In systems which do not need memory protection, and wish to have the kernel and user tasks operate out of the same memory space, high-order address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

### Clock Generator Unit

The R3071 is driven from a single input clock at the processor rated speed. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The R3071 includes an on-chip clock doubler to provide higher frequency signals to the internal execution core. The clock generator unit replaces the external delay line required in R3000A based applications.

### Instruction Cache

The R3071 implements a 16kB Instruction Cache. The system may choose to repartition the on-chip caches, so that the instruction cache is reduced to 8kB but the data cache is increased to 8kB. The instruction cache is organized with a line size of 16 bytes (four entries). This large cache achieves hit rates in excess of 98% in most applications, and substantially contributes to the performance inherent in the R3071. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

The instruction cache is parity protected over the instruction word and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

### Data Cache

The R3071 incorporates an on-chip data cache of 4kB, organized as a line size of 4 bytes (one word). The R3071 allows the system to reconfigure the on-chip cache from the default 16kB I-Cache/4kB D-Cache to 8kB of Instruction and 8kB of Data caches.

The relatively large data cache achieves hit rates in excess of 95% in most applications, and contributes substantially to the performance inherent in the R3071. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write-through cache, to insure that main memory is always consistent with the

internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance. Further, support has been provided to allow hardware based data cache coherency in a multi-master environment, such as one utilizing DMA from I/O to memory.

The data cache is parity protected over the data and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

### Bus Interface Unit

The R3071 uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slower memory devices. Alternately, a high-performance, low-cost secondary cache can be implemented, allowing the processor to increase performance in systems where bus bandwidth is a performance limitation.

As part of the R3051 family, the R3071 bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3071 also supports hardware based cache coherency during DMA writes. The R3071 can invalidate a specified line of data cache, or in fact can perform burst invalidations during burst DMA writes.

The R3071 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3071 read interface performs both single datum reads and quad word reads. Single reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3071 incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

The R3071 is R3051 superset compatible in its bus interface. Specifically, the R3071 has additional support to simplify the design of very high frequency systems. This support includes the ability to run the bus interface at one-half the processor execution rate, as well as the ability to slow the transitions

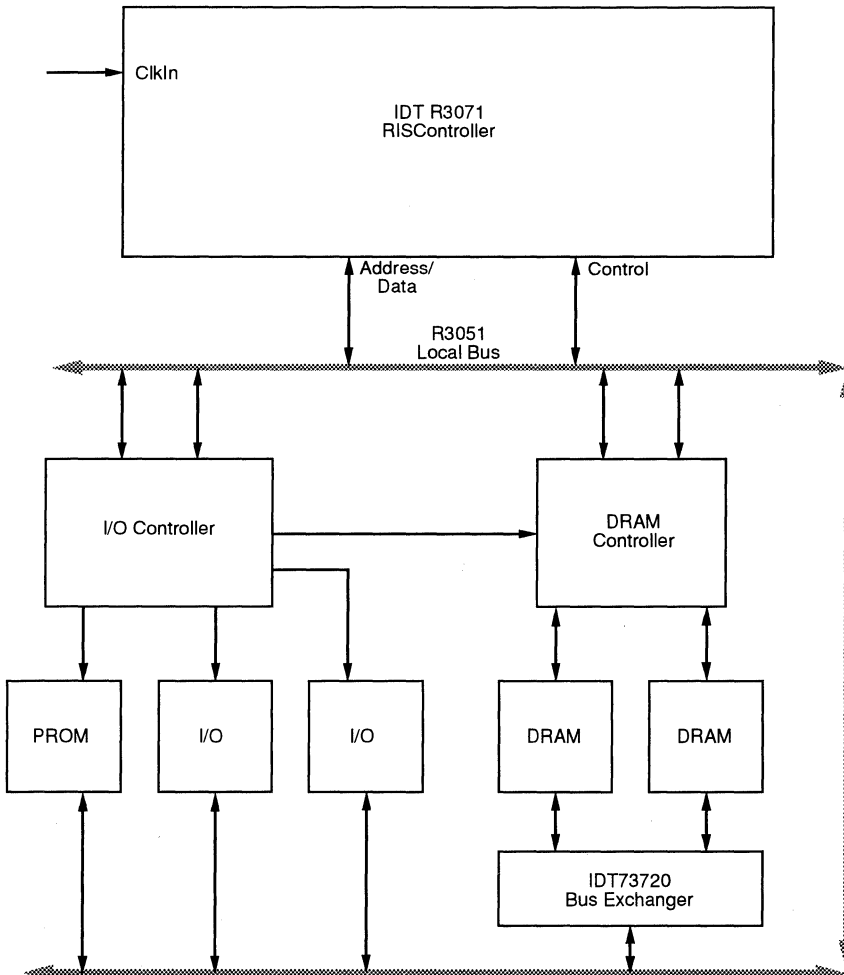
between reads and writes to provide extra buffer disable time for the memory interface. However, it is still possible to design a system which, with no modification to the PC Board or software, can accept either an R3051, R3052, or R3071.

**SYSTEM USAGE**

The IDT R3051 family has been specifically designed to allow a wide variety of memory systems. Low-cost systems can use slow speed memories and simple controllers, while other designers may choose to incorporate higher frequencies, faster memories, and techniques such as DMA to achieve maximum performance. The R3071 includes specific support for high performance systems, including signals necessary to implement external secondary caches, and the ability to perform hardware based cache coherency in multi-master systems.

Figure 5 shows a typical system implementation. Transparent latches are used to de-multiplex the R3071 address and data busses from the A/D bus. The data paths between the memory system elements and the A/D bus is managed by simple octal devices. A small set of simple PALs is used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize a simpler, lower performance memory system to reduce cost and simplify the design. Similarly, the system designer could choose to implement techniques, such as external secondary cache, or DMA, to further improve system performance.



3045 drw 05

Figure 5. R3071-Based System

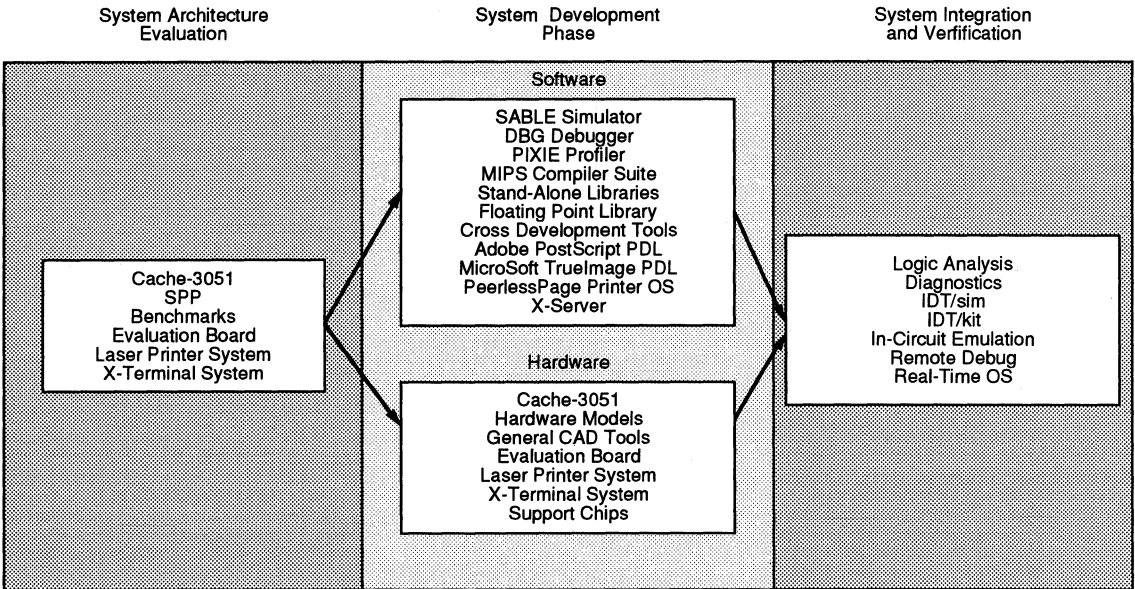
**DEVELOPMENT SUPPORT**

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, sub-system modules, and shrink wrap operating systems. The R3071, which is pin and software compatible with the R3051, can directly utilize these existing tools to reduce time to market.

Figure 6 is an overview of the system development process typically used when developing R3051 family applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family applications, and include tools such as:

- A program, Cache-R3051, which allows the performance of an R3051 family system to be modeled and understood without requiring actual hardware.

- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, including transcendental functions and IEEE compliant exception handlers.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- Adobe PostScript™ Page Description Language, ported to the IDT 79S389 Centaurus reference board.
- IDT/sim™, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™, which implements a run-time support package for R3051 family systems.



3045 drw 06

Figure 6. R3051 Family Development Toolchain

## PERFORMANCE OVERVIEW

The R3071 achieves a very high-level of performance. This performance is based on:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35VUPS performance when operating out of cache.
- Large on-chip caches. The R3051 family contains caches which are substantially larger than those on the majority of today's microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate. The R3071 doubles the cache available on the R3052.
- Autonomous multiply and divide operations. The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the CPU to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R3071 features a four-deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve over 35VUPS integer performance and 64,000 dhrystones without the use of external caches or zero wait-state memory devices.

The performance differences between the various family members depends on the application software and the design of the memory system. The impact of the various cache sizes, and the hardware floating point, can be accurately modeled using Cache-3051. Since the R3051, R3052, and R3071 are all pin and software compatible, the system designer has maximum freedom in trading between performance and cost. A system can be designed, and later the appropriate CPU inserted into the board, depending on the desired system performance.

## SELECTABLE FEATURES

The R3071 allows the system designer to configure certain aspects of operation. Some of these options are established when the device is reset, while others are enabled via the Config registers:

- BigEndian vs. LittleEndian Byte Ordering. The part can be configured to operate with either byte ordering. ACE/ARC systems typically use Little Endian byte ordering. However, various embedded applications, written originally for a Big Endian processor such as the MC680x0, are easier to port to a Big Endian system.
- Data Cache Refill of one or four words. The memory system must be capable of performing four word refills of instruction cache misses. The R3071 allows the system designer to enable D-Cache refill of one or four words dynamically. Thus, specialized algorithms can choose one refill size, while the rest of the system can operate with the other.
- Half-frequency bus mode. The processor can be configured such that the external bus interface is at one-half the frequency of the processor core. This simplifies system design; however, the large on-chip caches mitigate the performance impact of using a slower system bus clock.
- Slow bus turn-around. The R3071 allows the system designer to space processor operations, so that more time is allowed for transitions between memory and the processor on the multiplexed address/data bus.
- Configurable cache. The R3071 allows the system designer to use software to select either a 16kB Instruction Cache/4kB Data Cache organization, or an 8kB Instruction/8kB Data Cache organization.
- Cache Coherent Interface. The R3071 has an optional hardware based cache coherency interface intended to support multi-master systems such as those utilizing DMA between memory and I/O.

**THERMAL CONSIDERATIONS**

The R3071 utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, the R3071 is packaged using cavity-down packaging, utilizing techniques to improve thermal transfer to the surrounding air.

The R3071 utilizes the 84-pin MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package allows for an efficient thermal transfer between the die and the case due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin and form compatible with the PLCC used for the R3051. Thus, designers can inter-change R3071s and R3051s in a particular design, without changing their PC Board.

The R3071 is guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient temperature conditions which will meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 2.

Note that the R3071 allows the operational frequency to be turned down during idle periods to reduce power consumption. This operation is described in the *R3071 Hardware User's Guide*. Reducing the operation frequency dramatically reduces power consumption.

$\theta_{CA}$						
Airflow (ft/min)	0	200	400	600	800	1000
"MJ" Package*	22	14	12	11	9	8

Table 2. Thermal Resistance ( $\theta_{CA}$ ) at Various Airflows  
 (\*estimated: final values tbd)

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**NOTES ON SYSTEM DESIGN**

The R3071 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

To minimize these AC parameters, the R3071 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3071 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall ( 10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading ( due to devices connected on the signal net and the routing of the net self) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3071 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

## PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	<p><b>Address/Data:</b> A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer.</p> <p>Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of:</p> <p><b>Address(31:4):</b> The high-order address for the transfer is presented on A/D(31:4).</p> <p><b><math>\overline{BE}</math>(3:0):</b> These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0).</p> <p>During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.</p> <p>During cache coherency operations, the R3071 monitors the A/D bus at the start of a DMA write to capture the write target address for potential data cache invalidates.</p>
Addr(3:2)	O	<p><b>Low Address (3:2)</b> A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.</p> <p>During cache coherency operations, the R3071 monitors the Addr bus at the start of a DMA write to capture the write target address for potential data cache invalidates.</p>
Diag(1)	O	<p><b>Diagnostic Pin 1.</b> This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed:</p> <p><b>Cached:</b> During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss.</p> <p><b>Miss Address (3):</b> During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p> <p>On write cycles, this output signals whether the data being written is retained in the on-chip data cache. The value of this pin is time multiplexed during writes:</p> <p><b>Cached:</b> During the address phase of write transactions, this signal is an active high output which indicates that the store data was retained in the on-chip data cache.</p> <p><b>Reserved:</b> The value of this pin during the data phase of writes is reserved.</p>
Diag(0)	O	<p><b>Diagnostic Pin 0.</b> This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed:</p> <p><b><math>I/\overline{D}</math>:</b> If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase.</p> <p><b>Miss Address (2):</b> During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p> <p>During write cycles, the value of this pin during both the address and data phases is reserved.</p>

**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
ALE	I/O	<b>Address Latch Enable:</b> Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.  During cache coherency operations, the R3071 monitors ALE at the start of a DMA write, to capture the write target address for potential data cache invalidates.
$\overline{Rd}$	O	<b>Read:</b> An output which indicates that the current bus transaction is a read.
$\overline{Wr}$	I/O	<b>Write:</b> An output which indicates that the current bus transaction is a write.  During coherent DMA, this input indicates that the current transfer is a write.
$\overline{DataEn}$	O	<b>External Data Enable:</b> This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers
$\overline{Burst/}$ $\overline{WrNear}$	O	<b>Burst Transfer/Write Near:</b> On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if quad word refill is currently selected.  On write transactions, the $\overline{WrNear}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 512 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{Ack}$	I	<b>Acknowledge:</b> An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.  During Coherent DMA, this input indicates that the current write transfer is completed, and that the internal invalidation address counter should be incremented.
$\overline{RdCEn}$	I	<b>Read Buffer Clock Enable:</b> An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	<b>System Reference Clock:</b> An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit. This clock will either be at the same frequency as the CPU execution rate clock, or at one-half that frequency, as selected during reset.
$\overline{BusReq}$	I	<b>DMA Arbiter Bus Request:</b> An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	O	<b>DMA Arbiter Bus Grant.</b> An output from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{IvdReq}$	I	<b>Invalidate Request.</b> An input provided by an external DMA controller to request that the CPU invalidate the Data Cache line corresponding to the current DMA write target address. This signal is the same pin as Diag(0)
$\overline{CohReq}$	I	<b>Coherent DMA Request.</b> An input used by the external DMA controller to indicate that the requested DMA operations could involve hardware cache coherency. This signal is the Rsvd(0) of the R3051.
SBrCond(3:2) BrCond(0) BrCond(1)	I	<b>Branch Condition Port:</b> These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously. Note that BrCond(1) is reserved for use by the R3081 internal FPA, and must be pulled-up externally.
$\overline{BusError}$	I	<b>Bus Error:</b> Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.

3045 tbi 04

**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Int}}(5:3)$ $\overline{\text{SInt}}(2:0)$	I	<p><b>Processor Interrupt:</b> During normal operation, these signals are logically the same as the <math>\overline{\text{Int}}(5:0)</math> signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000.</p> <p>There are two types of interrupt inputs: the <math>\overline{\text{SInt}}</math> inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts. Note that one interrupt, reserved for use by the R3081 on-chip FPA, will not be monitored externally.</p>
ClkIn	I	<b>Master Clock Input:</b> This input clock is provided at the execution frequency of the CPU.
Reset	I	<b>Master Processor Reset:</b> This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{\text{Reset}}$ .
Rsvd(4:1)	I/O	<b>Reserved:</b> These four signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins. Note that Rsvd(0) of the R3051 is now used for the $\overline{\text{CohReq}}$ input pin.

3045 tbl 05



**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup>**

Symbol	Rating	Commercial	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>C</sub>	Operating Case Temperature	0 to +85	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
V <sub>IN</sub>	Input Voltage	-0.5 to +7.0	V

**NOTES:** 3045 tbl 06

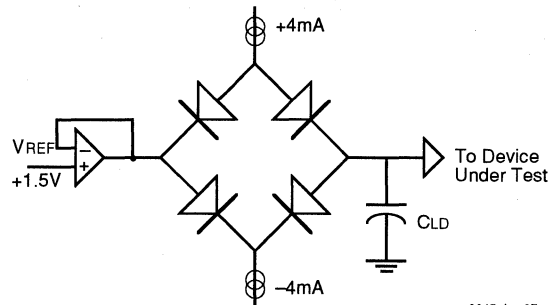
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -3.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> + 0.5V.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +85°C	0V (Case)	5.0 ±5%
Commercial	0°C to +85°C	0V (Case)	3.3 ±5%

3045 tbl 07

**OUTPUT LOADING FOR AC TESTING**



3045 drw 07

**AC TEST CONDITIONS—R3071**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.0	—	V
V <sub>IL</sub>	Input LOW Voltage	—	0.4	V
V <sub>IHS</sub>	Input HIGH Voltage	3.5	—	V
V <sub>ILS</sub>	Input LOW Voltage	—	0.4	V

3045 tbl 08

Signal	CLD
SysClk	50 pf
All Others	25 pf

3045 tbl 09

**DC ELECTRICAL CHARACTERISTICS R3071—** (T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)

Symbol	Parameter	Test Conditions	33.33MHz		40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	3.5	—	3.5	—	3.5	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(9)</sup>	—	2.0	—	2.0	—	2.0	—	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	V
V <sub>IHS</sub>	Input HIGH Voltage <sup>(2,3)</sup>	—	3.0	—	3.0	—	3.0	—	V
V <sub>ILS</sub>	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	V
C <sub>IN</sub>	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	pF
C <sub>OUT</sub>	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	pF
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = 5V, T <sub>C</sub> = 25°C	—	1050	—	1200	—	1400	mA
I <sub>IH</sub>	Input HIGH Leakage	V <sub>IH</sub> = V <sub>CC</sub>	—	100	—	100	—	100	µA
I <sub>IL</sub>	Input LOW Leakage	V <sub>IL</sub> = GND	-100	—	-100	—	-100	—	µA
I <sub>OZ</sub>	Output Tri-state Leakage	V <sub>OH</sub> = 2.4V, V <sub>OL</sub> = 0.5V	-100	100	-100	100	-100	-100	µA

**NOTES:**

- V<sub>IL</sub> Min. = -3.0V for pulse width less than 15ns. V<sub>IL</sub> should not fall below -0.5V for larger periods.
- V<sub>IHS</sub> and V<sub>ILS</sub> apply to ClkIn and Reset.
- V<sub>IH</sub> should not be held above V<sub>CC</sub> + 0.5V.
- Guaranteed by design.

3045 tbl 10

**AC ELECTRICAL CHARACTERISTICS R3071** <sup>(1, 2)</sup> (T<sub>c</sub> = 0°C to +85°C, V<sub>cc</sub> = +5.0V ±5%)

Symbol	Signals	Description	33.33MHz		40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{\text{BusReq}}$ , $\overline{\text{Ack}}$ , $\overline{\text{BusError}}$ , $\overline{\text{RdCEn}}$ , $\overline{\text{CohReq}}$	Set-up to $\overline{\text{SysClk}}$ rising	4	—	3	—	2.5	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	5	—	4.5	—	4.0	—	ns
t2	$\overline{\text{BusReq}}$ , $\overline{\text{Ack}}$ , $\overline{\text{BusError}}$ , $\overline{\text{RdCEn}}$ , $\overline{\text{CohReq}}$	Hold from $\overline{\text{SysClk}}$ rising	3	—	3	—	2	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	1	—	1	—	.5	—	
t3	A/D, $\overline{\text{Addr}}$ , $\overline{\text{Diag}}$ , $\overline{\text{ALE}}$ , $\overline{\text{Wr}}$ , $\overline{\text{BurstWrNear}}$ , $\overline{\text{Rd}}$ , $\overline{\text{DataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	—	10	ns
t4	A/D, $\overline{\text{Addr}}$ , $\overline{\text{Diag}}$ , $\overline{\text{ALE}}$ , $\overline{\text{Wr}}$ , $\overline{\text{BurstWrNear}}$ , $\overline{\text{Rd}}$ , $\overline{\text{DataEn}}$	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	6	—	5	—	4	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	6	—	5	—	3.5	ns
t7	$\overline{\text{Wr}}$ , $\overline{\text{Rd}}$ , $\overline{\text{BurstWrNear}}$ , A/D	Valid from $\overline{\text{SysClk}}$ rising	—	4	—	3.5	—	3.0	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	3	—	3	—	2	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	3	—	3	—	2	ns
t10	A/D	Hold from ALE negated	1.5	—	1.5	—	1.5	—	ns
t11	$\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$ falling	—	13	—	12	—	11	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state <sup>(3)</sup>	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising <sup>(3)</sup>	0	—	0	—	0	—	ns
t15	$\overline{\text{Wr}}$ , $\overline{\text{Rd}}$ , $\overline{\text{DataEn}}$ , $\overline{\text{BurstWrNear}}$	Negated from $\overline{\text{SysClk}}$ falling	—	5	—	4	—	3.5	ns
t16	$\overline{\text{Addr}}(3:2)$	Valid from $\overline{\text{SysClk}}$	—	5	—	4.5	—	4.0	ns
t17	$\overline{\text{Diag}}$	Valid from $\overline{\text{SysClk}}$	—	10	—	9	—	7	ns
t18	A/D	Tri-state from $\overline{\text{SysClk}}$ falling	—	9	—	8	—	8	ns
t19	A/D	$\overline{\text{SysClk}}$ falling to data out	—	11	—	10	—	8	ns
t20	$\overline{\text{ClkIn}}$ (2x clock mode)	Pulse Width HIGH	6.5	—	5.6	—	N/A <sup>(6)</sup>	—	ns
t21	$\overline{\text{ClkIn}}$ (2x clock mode)	Pulse Width LOW	6.5	—	5.6	—	N/A <sup>(6)</sup>	—	ns
t22	$\overline{\text{ClkIn}}$ (2x clock mode)	Clock Period	15	250	12.5	250	N/A <sup>(6)</sup>	—	ns
t23	$\overline{\text{Reset}}$	Pulse Width from V <sub>cc</sub> valid	200	—	200	—	32	—	μs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	2	—	t <sub>sys</sub>
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	8	—	7	—	2	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	0	—	0	—	2.5	—	ns
t28	$\overline{\text{SInt}}$ , $\overline{\text{SBrCond}}$	Set-up to $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	ns
t29	$\overline{\text{SInt}}$ , $\overline{\text{SBrCond}}$	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	1.5	—	ns
t30	$\overline{\text{Int}}$ , $\overline{\text{BrCond}}$	Set-up to $\overline{\text{SysClk}}$ falling	4	—	3	—	2	—	ns
t31	$\overline{\text{Int}}$ , $\overline{\text{BrCond}}$	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	1.5	—	ns

## NOTES:

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- All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
- The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
- The design guarantees that the input clock rise and fall times can be as long as 5ns.
- 1x clock mode only.

**AC ELECTRICAL CHARACTERISTICS R3071 (continued)<sup>(1, 2)</sup>** — (T<sub>c</sub> = 0°C to +85°C, V<sub>cc</sub> = +5.0V ±5%)

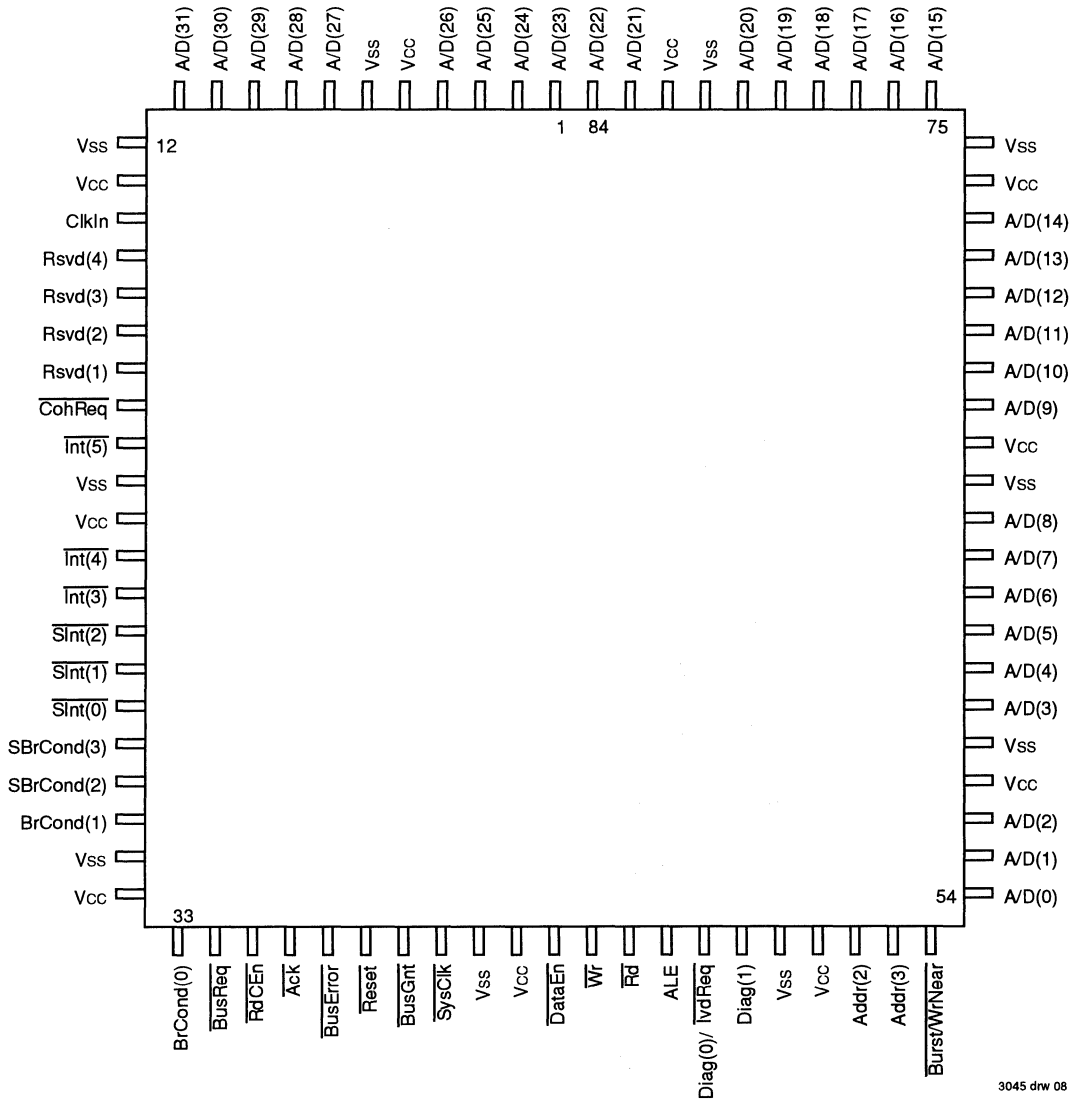
Symbol	Signals	Description	33.33MHz		40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>sys</sub>	$\overline{\text{SysClk}}$ (full frequency mode)	Pulse Width	2*t <sub>22</sub>	2*t <sub>22</sub>	2*t <sub>22</sub>	2*t <sub>22</sub>	t <sub>44</sub>	t <sub>44</sub>	ns
t <sub>32</sub>	$\overline{\text{SysClk}}$ (full frequency mode)	Clock HIGH time <sup>(6)</sup>	t <sub>22-1</sub>	t <sub>22+1</sub>	t <sub>22-1</sub>	t <sub>22+1</sub>	t <sub>44/2-1</sub>	t <sub>44/2+1</sub>	ns
t <sub>33</sub>	$\overline{\text{SysClk}}$ (full frequency mode)	Clock LOW time <sup>(6)</sup>	t <sub>22-1</sub>	t <sub>22+1</sub>	t <sub>22-1</sub>	t <sub>22+1</sub>	t <sub>44/2-1</sub>	t <sub>44/2+1</sub>	ns
t <sub>sys/2</sub>	$\overline{\text{SysClk}}$ (half frequency mode)	Pulse Width	2*t <sub>44</sub>	2*t <sub>44</sub>	2*t <sub>44</sub>	2*t <sub>44</sub>	2*t <sub>44</sub>	2*t <sub>44</sub>	ns
t <sub>34</sub>	$\overline{\text{SysClk}}$ (half frequency mode)	Clock HIGH Time	t <sub>44-1</sub>	t <sub>44+1</sub>	t <sub>44-1</sub>	t <sub>44+1</sub>	t <sub>44-1</sub>	t <sub>44+1</sub>	ns
t <sub>35</sub>	$\overline{\text{SysClk}}$ (half frequency mode)	Clock LOW Time	t <sub>44-1</sub>	t <sub>44+1</sub>	t <sub>44-1</sub>	t <sub>44+1</sub>	t <sub>44-1</sub>	t <sub>44+1</sub>	ns
t <sub>36</sub>	ALE	Set-up to $\overline{\text{SysClk}}$ falling	7	—	6	—	5	—	ns
t <sub>37</sub>	ALE	Hold from $\overline{\text{SysClk}}$ falling	1	—	1	—	0	—	ns
t <sub>38</sub>	A/D	Set-up to ALE falling	8	—	8	—	7	—	ns
t <sub>39</sub>	A/D	Hold from ALE falling	1	—	1	—	0	—	ns
t <sub>40</sub>	$\overline{\text{Wr}}$	Set-up to $\overline{\text{SysClk}}$ rising	8	—	7	—	6	—	ns
t <sub>41</sub>	$\overline{\text{Wr}}$	Hold from $\overline{\text{SysClk}}$ rising	3	—	3	—	1	—	ns
t <sub>42</sub>	ClkIn (1x clock mode)	Pulse Width HIGH <sup>(5)</sup>	13	—	11	—	8.5	—	ns
t <sub>43</sub>	ClkIn (1x clock mode)	Pulse Width LOW <sup>(5)</sup>	13	—	11	—	8.5	—	ns
t <sub>44</sub>	ClkIn (1x clock mode)	Clock Period <sup>(5)</sup>	30	50	25	50	20	50	ns
t <sub>derate</sub>	All outputs	Timing deration for loading over C <sub>LD</sub> <sup>(3, 4)</sup>	—	0.5	—	0.5	—	0.5	ns/ 25pF

**NOTES:**

3045 tbl 12

- All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
- The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
- The design guarantees that the input clock rise and fall times can be as long as 5ns.
- In 1x clock mode, t<sub>22</sub> is replaced by t<sub>44/2</sub>.

**PIN CONFIGURATIONS**



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**84-Pin MQAD  
Top View**

**NOTE:**

1. Reserved Pins must not be connected.
2. BrCond(1) is reserved in the R3071, and must be pulled-up externally.

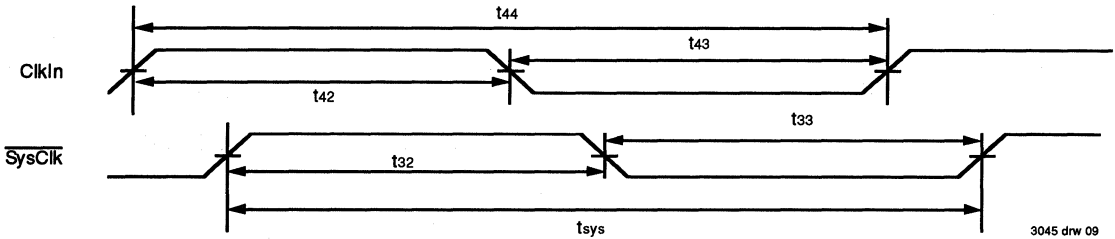


Figure 7 (a). R3071 Clcking (1x clock input mode, full frequency bus)

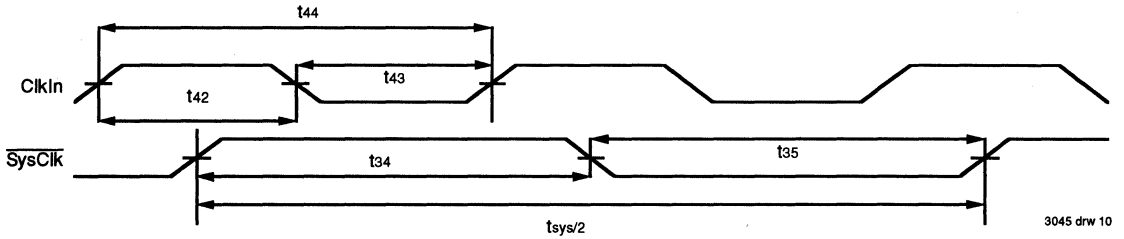


Figure 7 (b). R3071 Clcking (1x clock input mode, half-frequency bus)

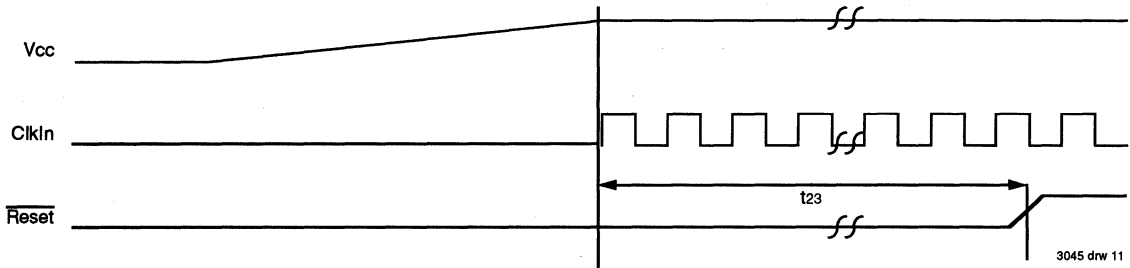


Figure 8. Power-On Reset Sequence

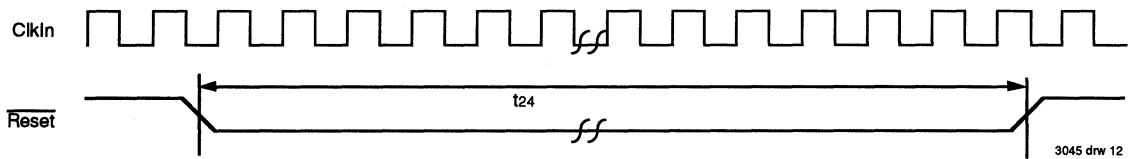


Figure 9. Warm Reset Sequence

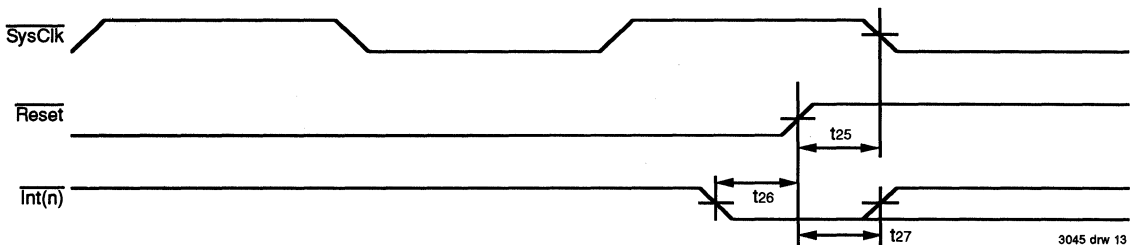
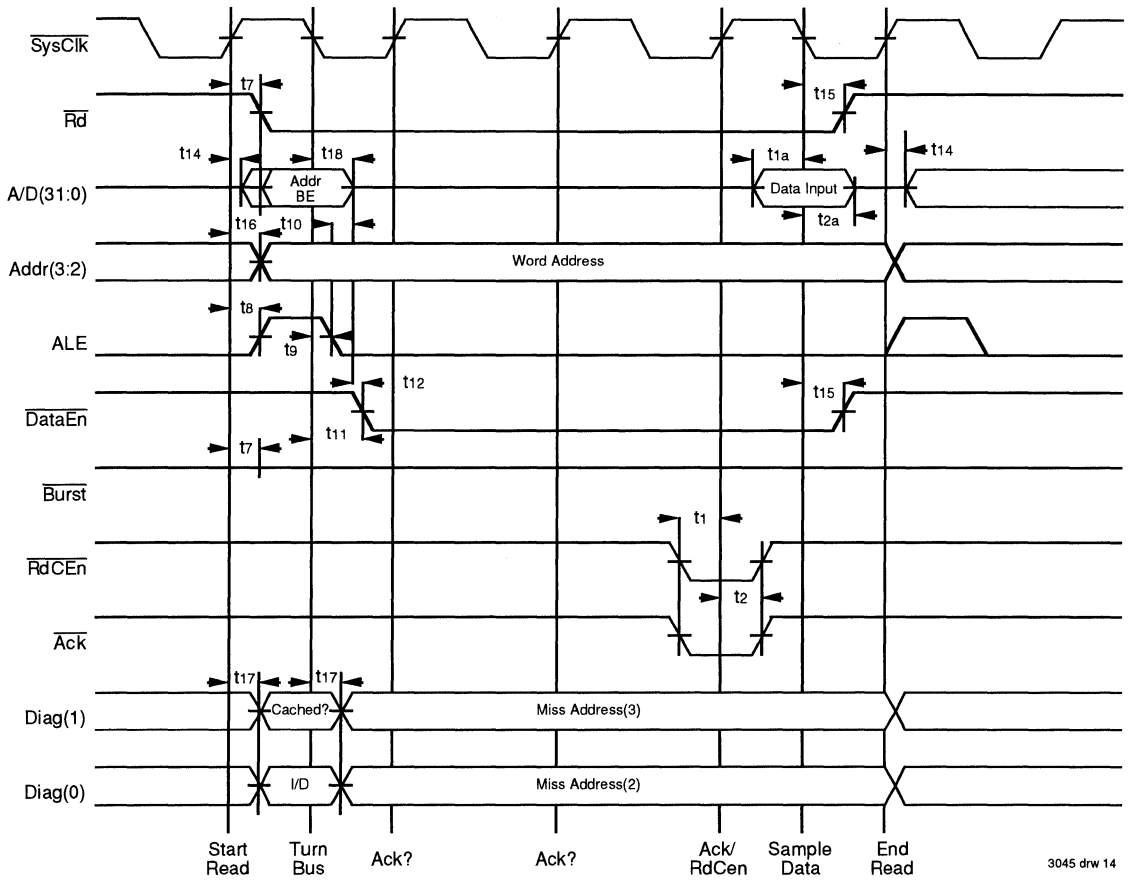


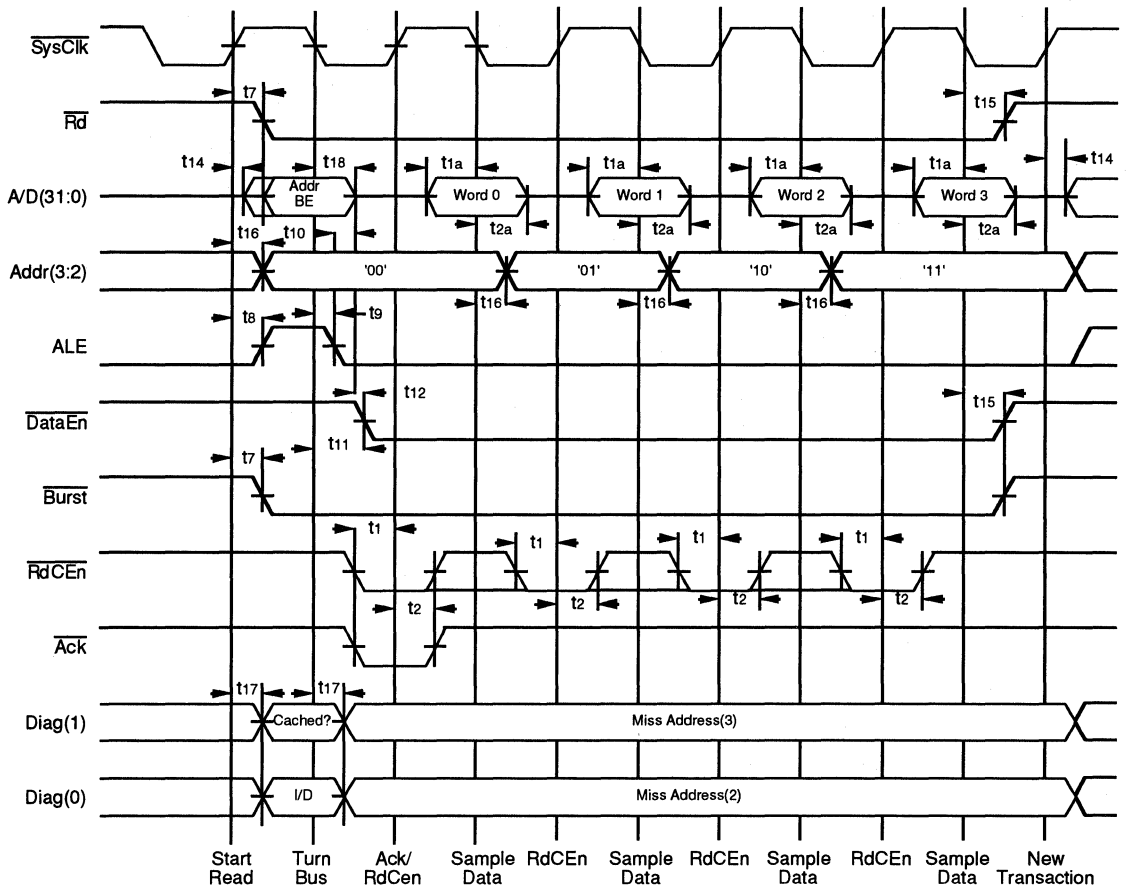
Figure 10. Mode Selection and Negation of Reset



3045 drw 14

Figure 11. Single Datum Read in R3071

5



3045 drw 15

Figure 12. R3071 Burst Read

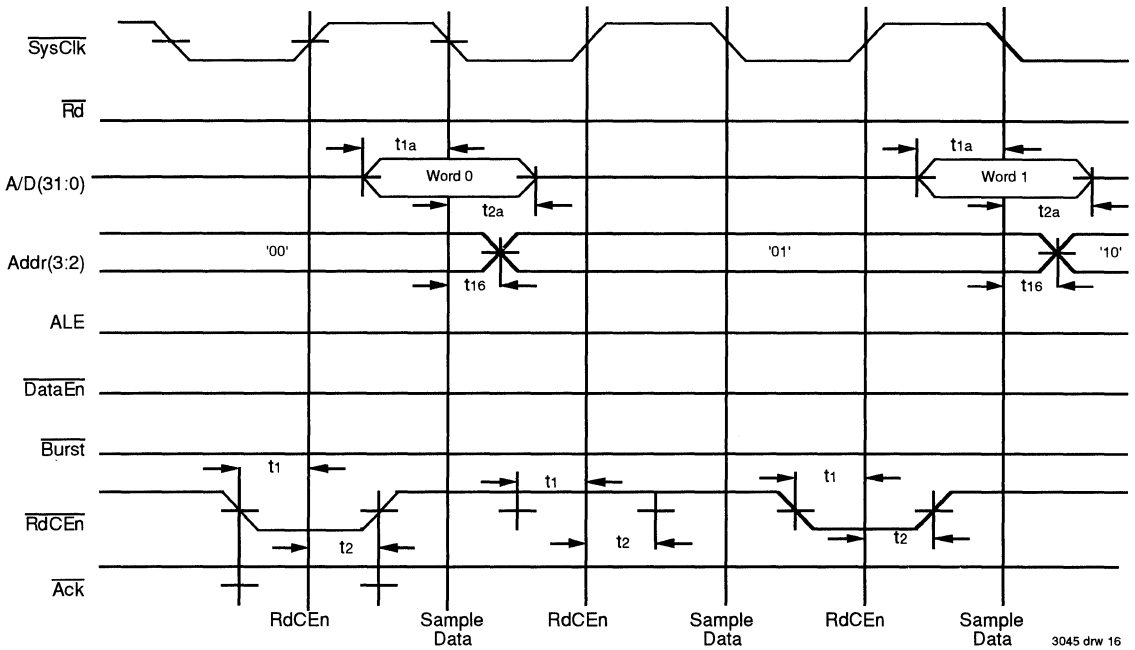


Figure 13 (a). Start of Throttled Quad Read

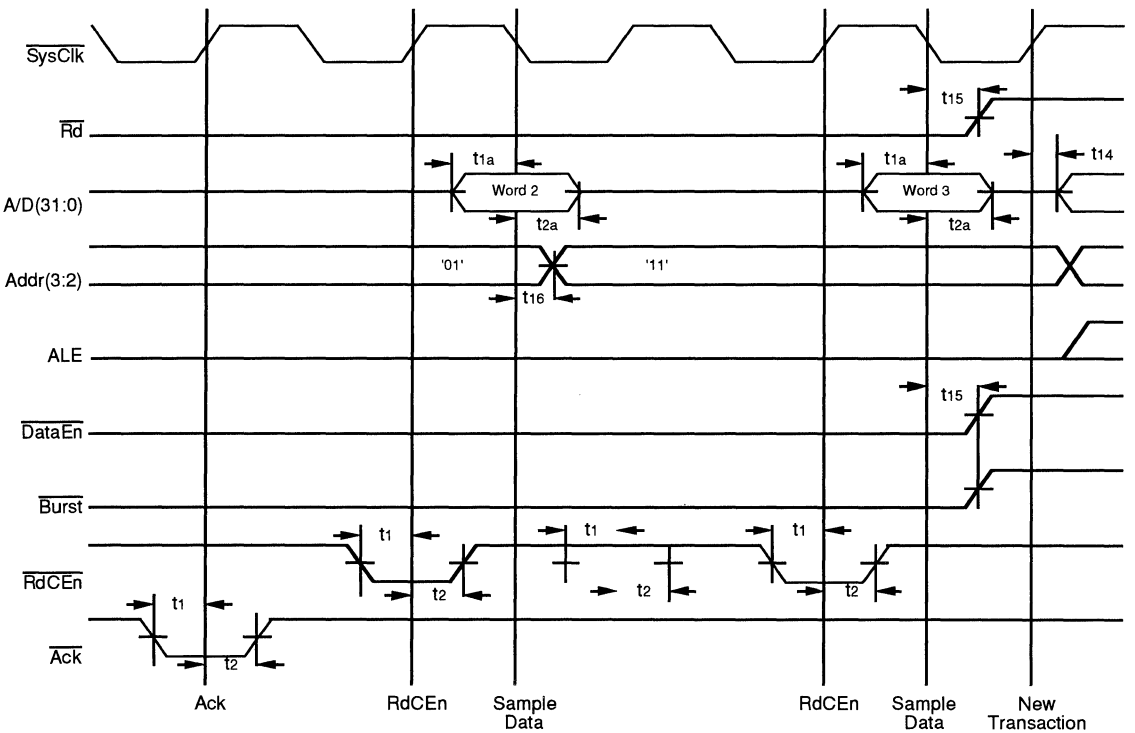


Figure 13 (b). End of Throttled Quad Read

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3045 drw 16

3045 drw 17



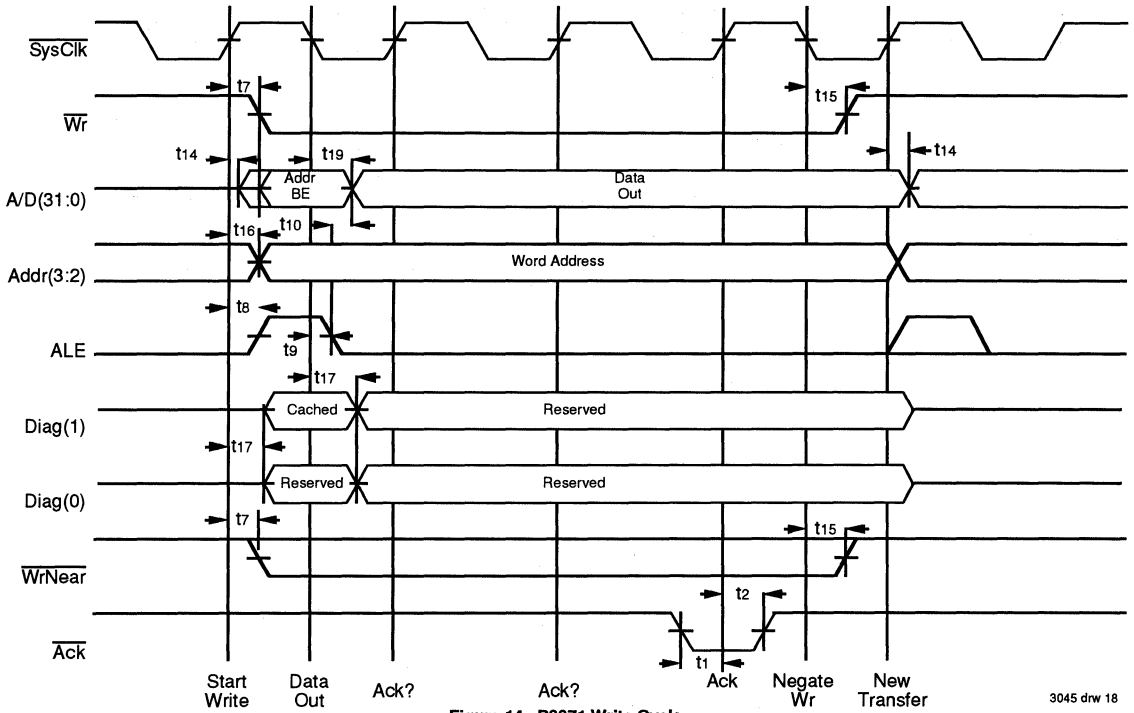


Figure 14. R3071 Write Cycle

3045 drw 18

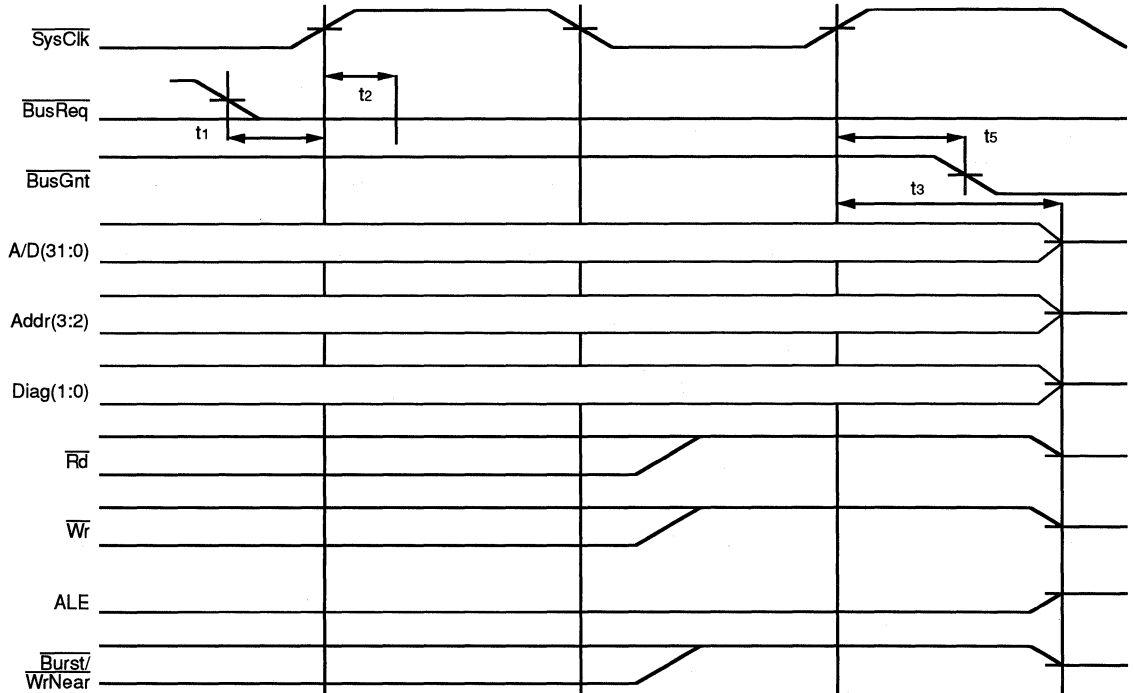
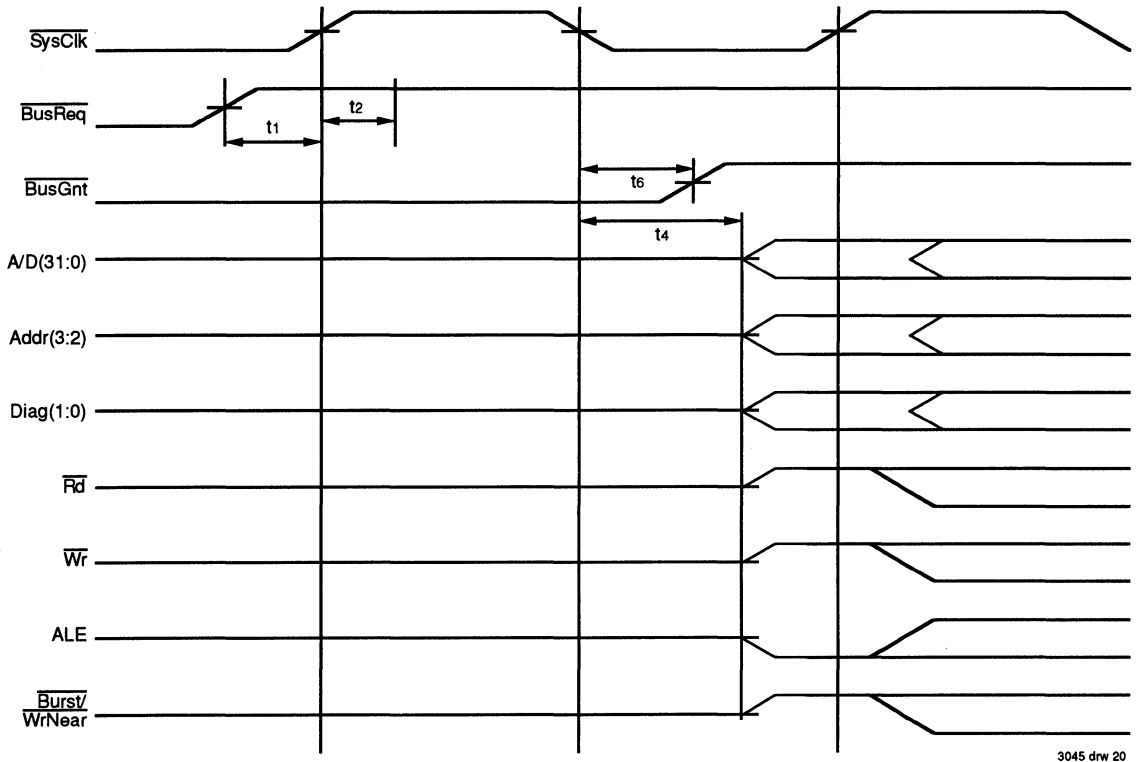


Figure 15. Request and Relinquish of R3071 Bus to External Master

3045 drw 19



3045 drw 20

Figure 16. R3071 Regaining Bus Mastership

5

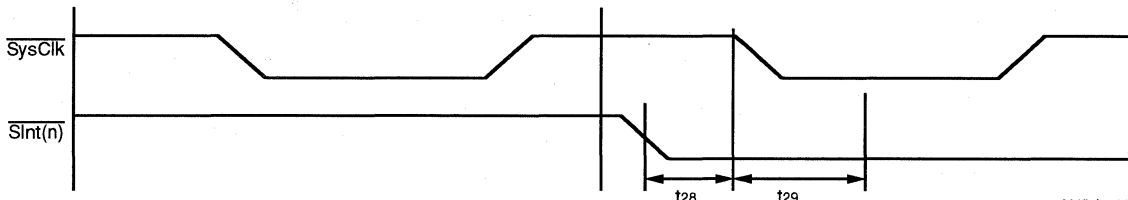


Figure 17. Synchronized Interrupt Input Timing

3045 drw 21

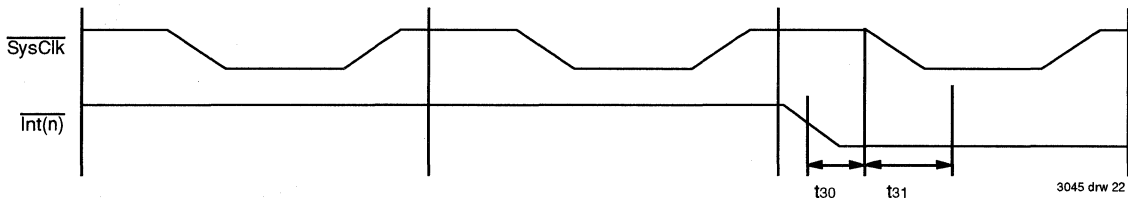


Figure 18. Direct Interrupt Input Timing

3045 drw 22

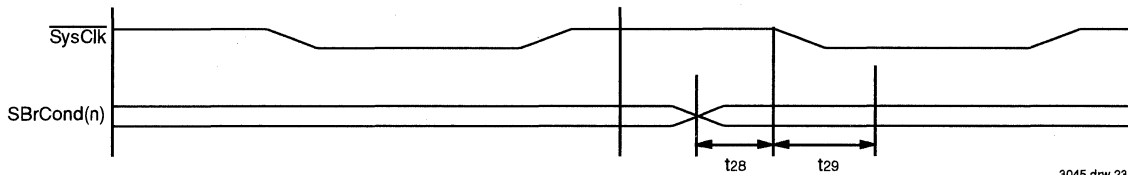


Figure 19. Synchronized Branch Condition Input Timing

3045 drw 23

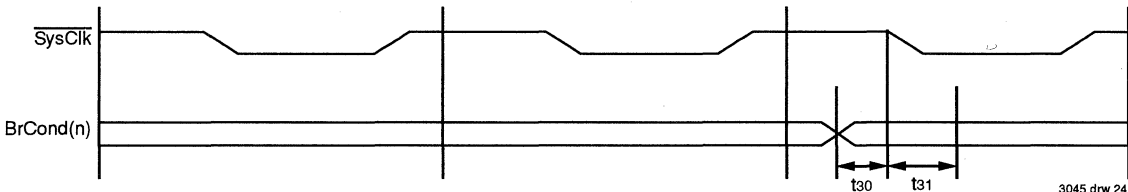


Figure 20. Direct Branch Condition Input Timing

3045 drw 24

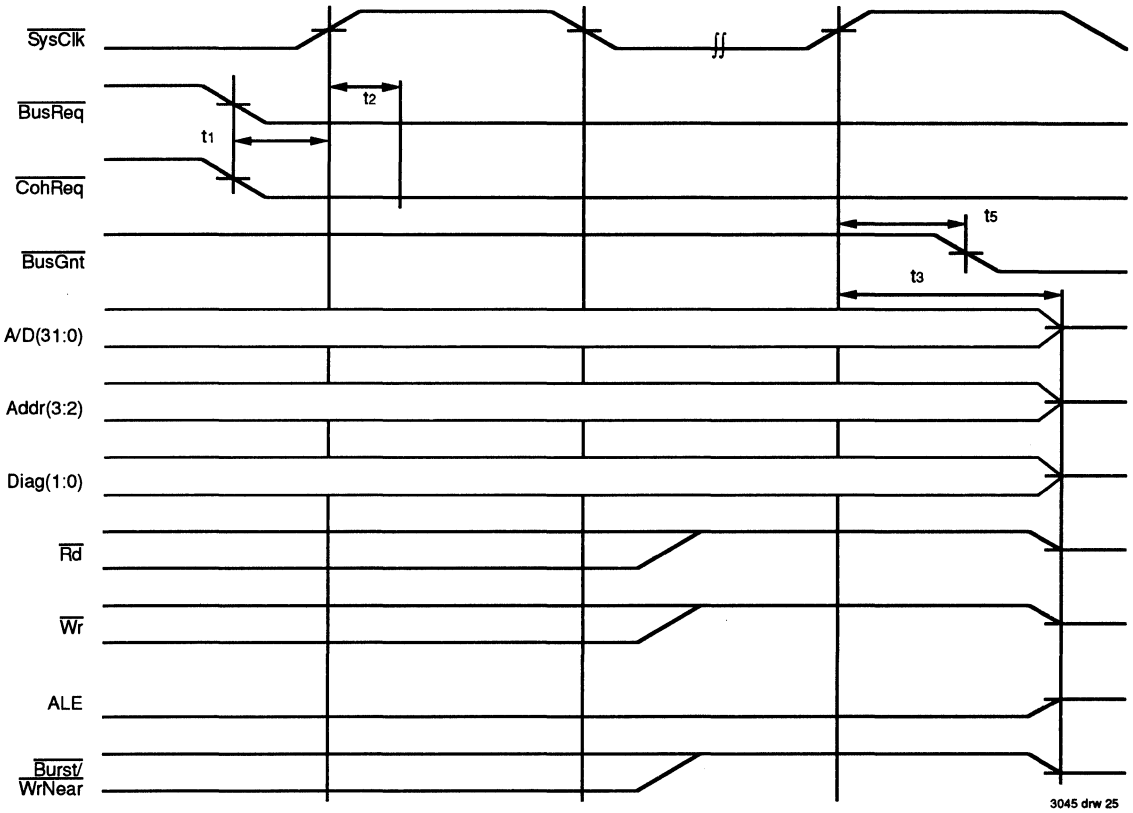


Figure 21. Coherent DMA Request

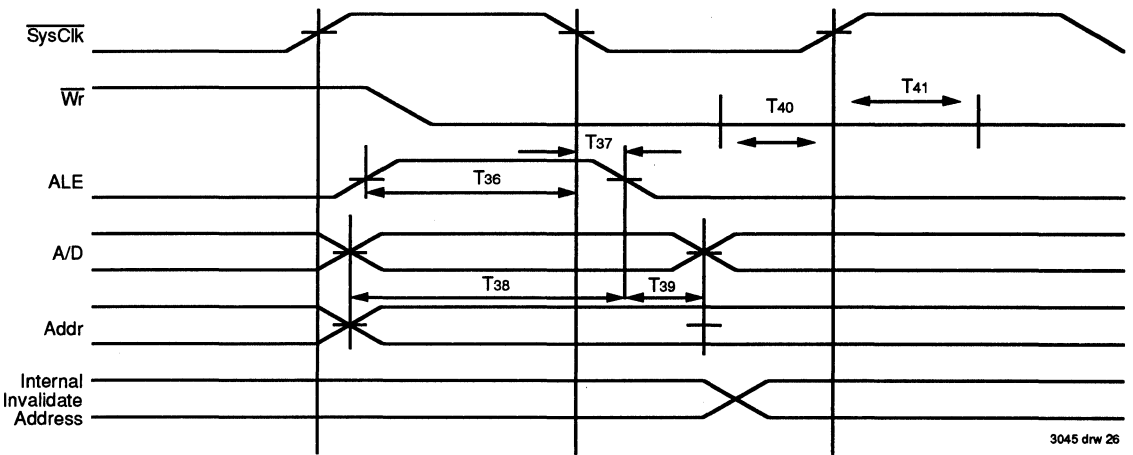


Figure 22. Beginning of Coherent DMA Write

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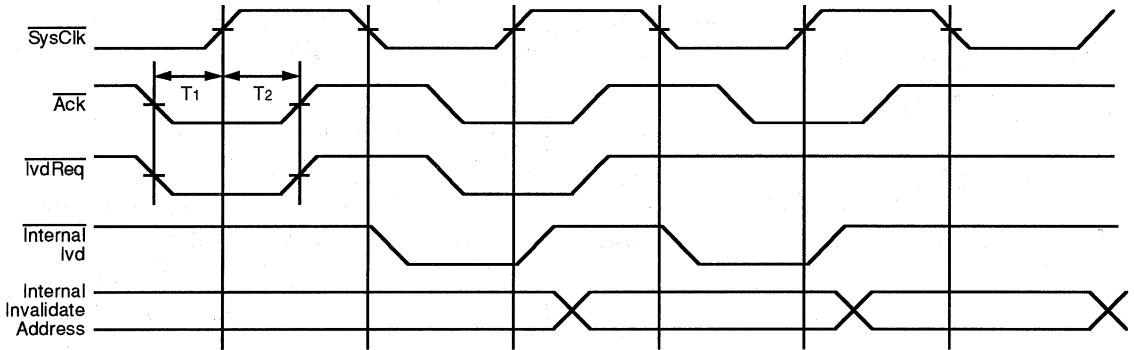


Figure 23. Cache Word Invalidation

3045 drw 27

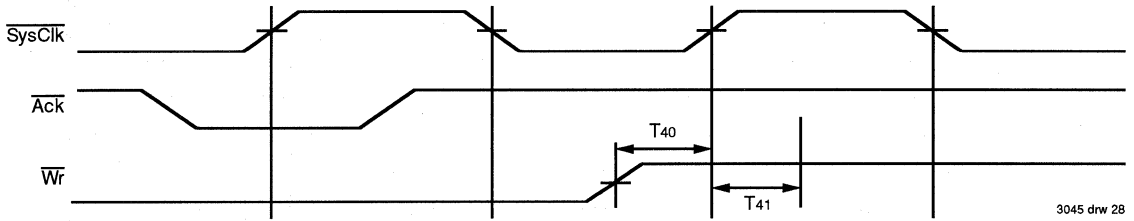


Figure 24. End of Coherent Write

3045 drw 28

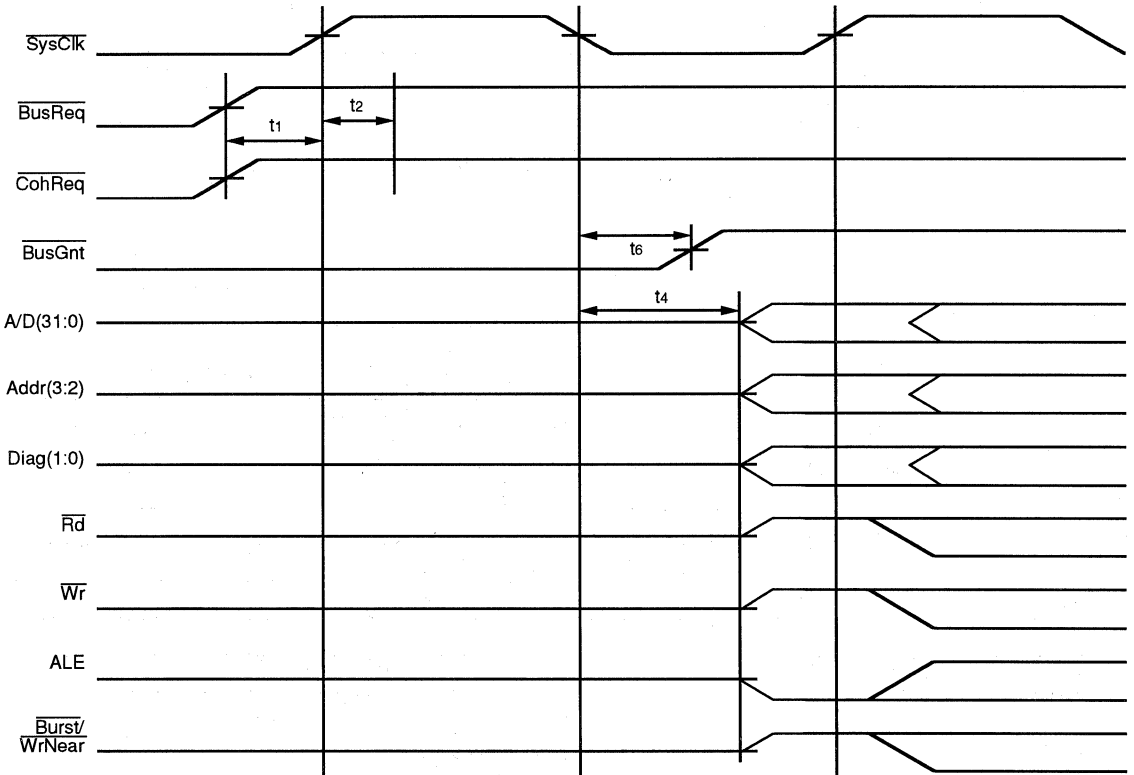
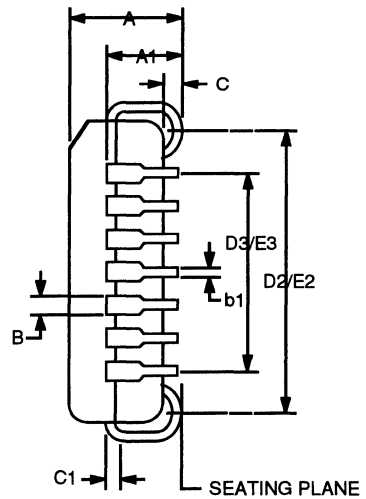
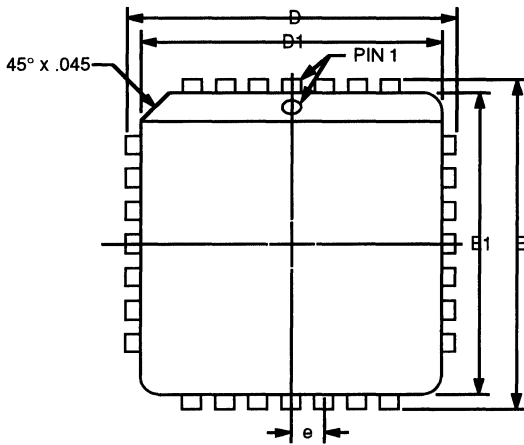


Figure 25. End of Coherent DMA Request

3045 drw 29

84 LEAD MQUAD<sup>(7)</sup>



3045 drw 30

NOTES:

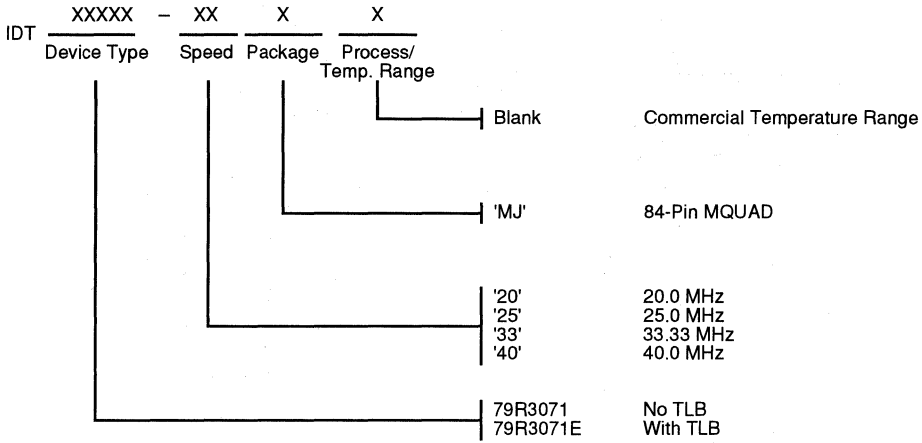
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protusions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. 84-pin MQUAD is pin & form compatible with 84-pin PLCC of R3051/2

5

DWG #	MJ84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.094	.114
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.140	1.150
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.140	1.150
e	.050 BSC	
ND/NE	21	

3045 tbl 13

**ORDERING INFORMATION**



3045 drw 31

**VALID COMBINATIONS**

IDT 79R3071 – 33, 40, 50 MJ	MQUAD Package
79R3071E – 33, 40, 50 MJ	MQUAD Package



Integrated Device Technology, Inc.

# IDT79R3081 RISController™

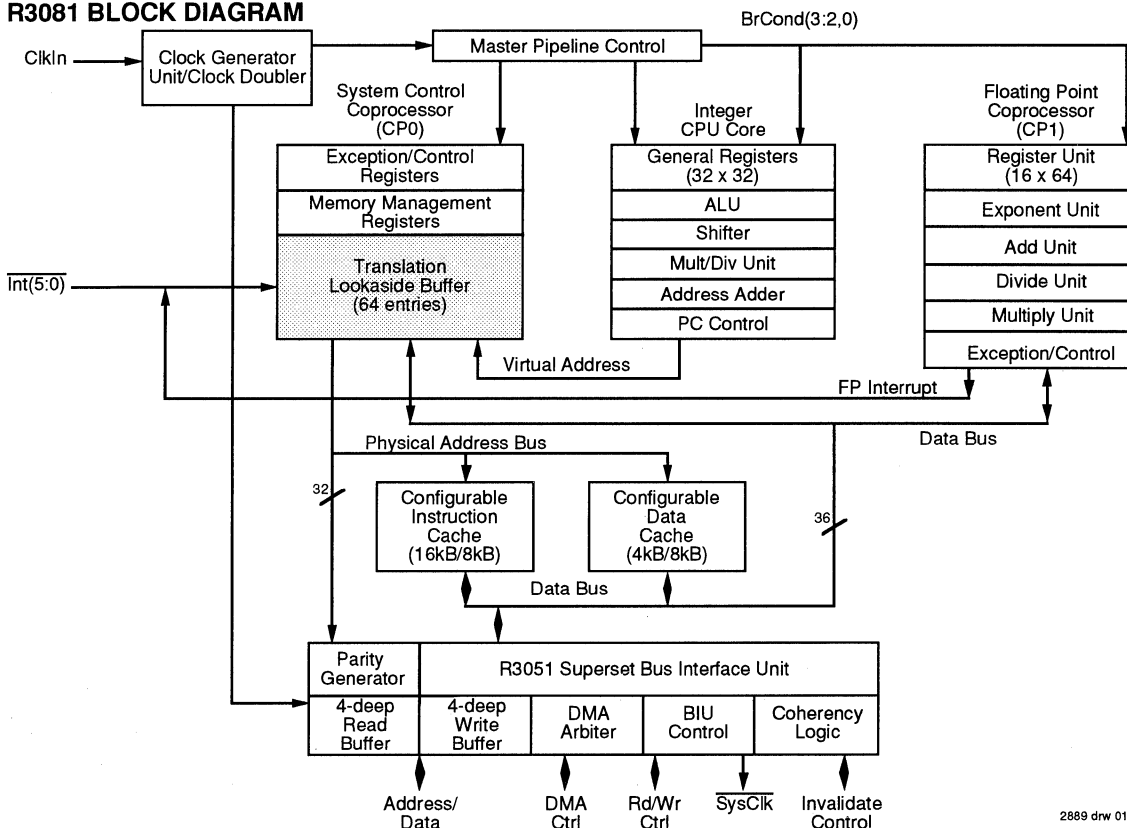
IDT 79R3081™, 79R3081E  
IDT 79RV3081, 79RV3081E

## FEATURES

- Instruction set compatible with IDT79R3000A, R3051, and R3500 RISC CPUs
- High level of integration minimizes system cost
  - R3000A Compatible CPU
  - R3010A Compatible Floating Point Accelerator
  - Optional R3000A compatible MMU
  - Large Instruction Cache
  - Large Data Cache
  - Read/Write Buffers
- 43VUPS at 40MHz
  - 13MFlops
- Flexible bus interface allows simple, low cost designs
- Optional 1x or 2x clock input
- 20 through 50MHz operation
- "V" version operates at 3.3V
- 50MHz at 1x clock input and 1/2 bus frequency only

- Large on-chip caches with user configurability
  - 16kB Instruction Cache, 4kB Data Cache
  - Dynamically configurable to 8kB Instruction Cache, 8kB Data Cache
  - Parity protection over data and tag fields
- Low cost 84-pin packaging
- Superset pin- and software-compatible with R3051
- Multiplexed bus interface with support for low-cost, low-speed memory systems with a high-speed CPU
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-deep read buffer supports burst or simple block reads
- On-chip DMA arbiter
- Hardware-based Cache Coherency Support
- Programmable power reduction mode
- Bus Interface can operate at half-processor frequency

## R3081 BLOCK DIAGRAM



2889 drw 01

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**MARCH 1994**

5



## INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35VUPS performance at 40MHz without requiring external SRAM or caches.

The R3081 extends the capabilities of the R3051 family, by integrating additional resources into the same pin-out. The R3081 thus extends the range of applications addressed by the R3051 family, and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs, according to the price/performance goals of the end system.

In addition to the embedded applications served by the R3051 family, the R3081 allows low-cost, entry level computer systems to be constructed. These systems will offer many times the performance of traditional PC systems, yet cost approximately the same. The R3081 is able to run any standard R3000A operation system, including ACE UNIX. Thus, the R3081 can be used to build a low-cost ARC compliant system, further widening the range of performance solutions of the ACE Initiative.

An overview of this device, and quantitative electrical parameters and mechanical data, is found in this data sheet; consult the *"R3081 Family Hardware User's Guide"* for a complete description of this processor.

## DEVICE OVERVIEW

As part of the R3051 family, the R3081 extends the offering of a wide range of functionality in a compatible interface. The R3051 family allows the system designer to implement a single base system, and utilize interface-compatible processors of various complexity to achieve the price-performance goals of the particular end system.

Differences among the various family members pertain to the on-chip resources of the processor. Current family members include:

- The R3052E, which incorporates an 8kB instruction cache, a 2kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB).
- The R3052, which also incorporates an 8kB instruction cache and 2kB data cache, but does not include the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3051E, which incorporates 4kB of instruction cache and 2kB of data cache, along with the full function MMU/

TLB of the R3000A.

- The R3051, which incorporates 4kB of instruction cache and 2kB of data cache, but omits the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3081E, which incorporates a 16kB instruction cache, a 4kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB). The cache on the R3081E is user configurable to an 8kB Instruction Cache and 8kB Data Cache.
- The R3081, which incorporates a 16kB instruction cache, a 4kB data cache, but uses the simpler memory mapping of the R3051/52, and thus omits the TLB. The cache on the R3081 is user configurable to an 8kB Instruction Cache and 8kB Data Cache.

Figure 1 shows a block level representation of the functional units within the R3081E. The R3081E could be viewed as the embodiment of a discrete solution built around the R3000A and R3010A. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

### CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3081 uses the same basic integer execution core as the entire R3051 family, which is the R3000A implementation of the MIPS instruction set. Thus, the R3081 family is binary compatible with the R3051, R3052, R3000A, R3001, and R3500 CPUs. In addition, the R4000 represents an upwardly software compatible migration path to still higher levels of performance.

The execution engine in the R3081 uses a five-stage pipeline to achieve near single-cycle instruction execution rates. A new instruction can be initiated in each clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved in the R3081 execution pipeline.

### System Control Co-Processor

The R3081 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3081, as well as the virtual to physical address mapping.

As with the R3051 and R3052, the R3081 offers two versions of memory management and virtual to physical address mapping: the extended architecture versions, the R3051E, R3052E, and R3081E, incorporate the same MMU as the R3000A. These versions contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard-mapped to physical addresses, and kernel and user segments which are mapped page by page by the TLB into anywhere in the 4GB physical address space. In this TLB, 8 pages can be "locked" by the kernel to insure deterministic response in real-time applications. Figure 3 illustrates the virtual to physical mapping found in the

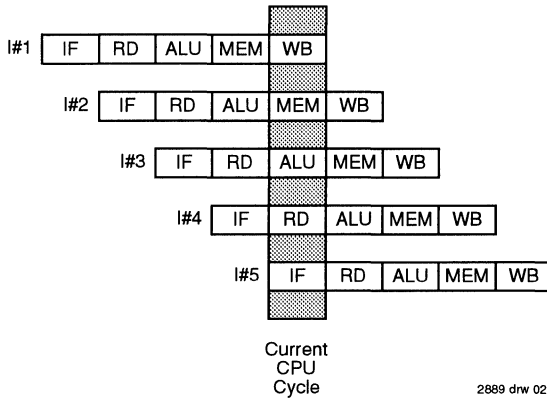


Figure 2. R3081 5-Stage Pipeline

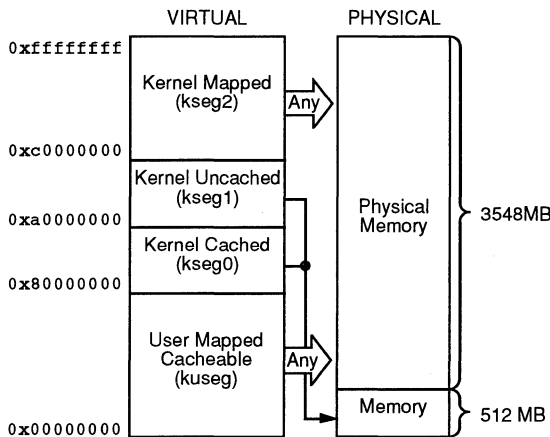


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

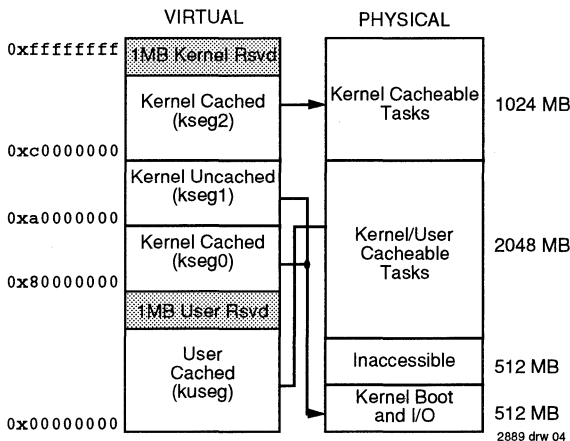


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

R3081E.

The extended architecture versions of the R3051 family (the R3051E, R3052E, and R3081E) allow the system designer to implement kernel software which dynamically manages user task utilization of system resources, and also allows the Kernel to protect certain resources from user tasks. These capabilities are important in general computing applications such as ARC computers, and are also important in a variety of embedded applications, from process control (where protection may be important) to X-Window display systems (where virtual memory management can be used). The MMU can also be used to simplify system debug.

R3051 family base versions (the R3051, R3052, and R3081) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. These devices still support distinct kernel and user mode operation, but do not require page management software, leading to a simpler software model. The memory mapping used by these devices is shown in Figure 4. Note that the reserved spaces are for compatibility with future family members, which may map on-chip resources to these addresses. References to these addresses in the R3081 will be translated in the same fashion as the rest of their respective segments, with no traps or exceptions signaled.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to implement page management software. This distinction can be implemented by decoding the output physical address. In systems which do not need memory protection, and wish to have the kernel and user tasks operate out of the same memory space, high-order address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

**Floating Point Co-Processor**

The R3081 also integrates an R3010A compatible floating point accelerator on-chip. The FPA is a high-performance co-processor (co-processor 1 to the CPU) providing separate add, multiply, and divide functional units for single and double precision floating point arithmetic. The floating point accelerator features low latency operations, and autonomous functional units which allow differing types of floating point operations to function concurrently with integer operations. The R3010A appears to the software programmer as a simple extension of the integer execution unit, with 16 dedicated 64-bit floating point registers (software references these as 32 32-bit registers when performing loads or stores). Figure 5 illustrates the functional block diagram of the on-chip FPA.

**Clock Generator Unit**

The R3081 is driven from a single input clock which can be either at the processor rated speed, or at twice that speed. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The R3081 includes an on-chip clock doubler to provide higher frequency signals to the internal execution core; if 1x clock

mode is selected, the clock doubler will internally convert it to a double frequency clock. The 2x clock mode is provided for compatibility with the R3051. The clock generator unit replaces the external delay line required in R3000A based applications.

**Instruction Cache**

The R3081 implements a 16kB Instruction Cache. The system may choose to repartition the on-chip caches, so that the instruction cache is reduced to 8kB but the data cache is increased to 8kB. The instruction cache is organized with a line size of 16bytes (four entries). This large cache achieves hit rates in excess of 98% in most applications, and substantially contributes to the performance inherent in the R3081. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

The instruction cache is parity protected over the instruction word and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

**Data Cache**

The R3081 incorporates an on-chip data cache of 4kB, organized as a line size of 4 bytes (one word). The R3081 allows the system to reconfigure the on-chip cache from the default 16kB I-Cache/4kB D-Cache to 8kB of Instruction and 8kB of Data caches.

The relatively large data cache achieves hit rates in excess

of 95% in most applications, and contributes substantially to the performance inherent in the R3081. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

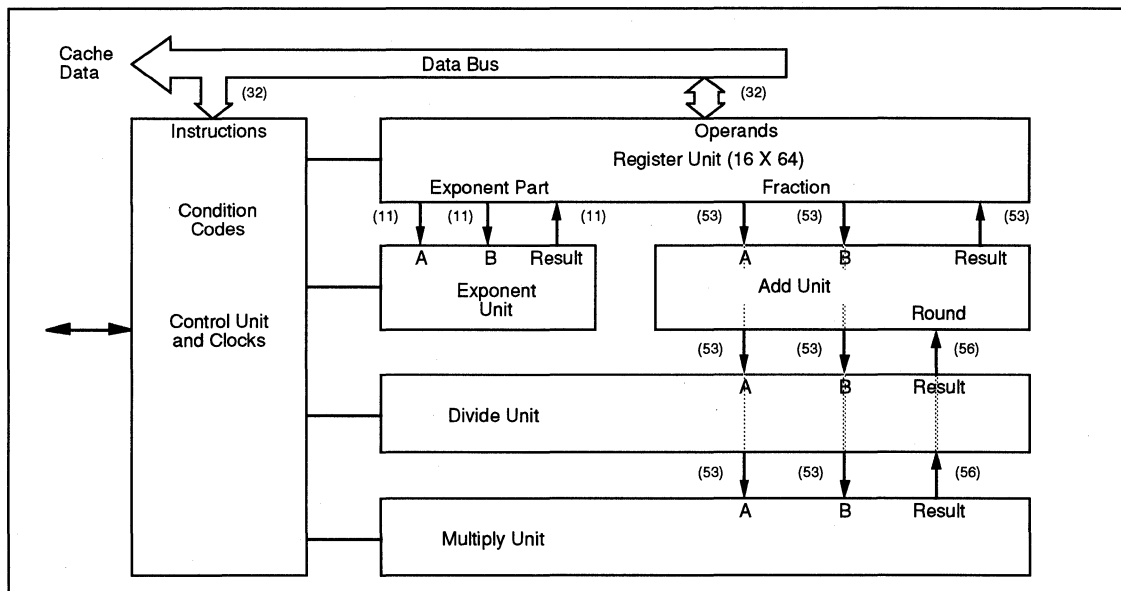
The data cache is implemented as a write-through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance. Further, support has been provided to allow hardware based data cache coherency in a multi-master environment, such as one utilizing DMA from I/O to memory.

The data cache is parity protected over the data and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

**Bus Interface Unit**

The R3081 uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slower memory devices. Alternately, a high-performance, low-cost secondary cache can be implemented, allowing the processor to increase performance in systems where bus bandwidth is a performance limitation.

As part of the R3051 family, the R3081 bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address



2889 drw 05

Figure 5. FPA Functional Block Diagram

Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3081 also supports hardware based cache coherency during DMA writes. The R3081 can invalidate a specified line of data cache, or in fact can perform burst invalidations during burst DMA writes.

The R3081 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3081 read interface performs both single datum reads and quad word reads. Single reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3081 incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

The R3081 is R3051 superset compatible in its bus interface. Specifically, the R3081 has additional support to simplify the design of very high frequency systems. This support includes the ability to run the bus interface at one-half the processor execution rate, as well as the ability to slow the transitions between reads and writes to provide extra buffer disable time for the memory interface. However, it is still possible to design a system which, with no modification to the PC Board or software, can accept either an R3051, R3052, or R3081.

## SYSTEM USAGE

The IDT R3051 family has been specifically designed to allow a wide variety of memory systems. Low-cost systems can use slow speed memories and simple controllers, while other designers may choose to incorporate higher frequencies, faster memories, and techniques such as DMA to achieve maximum performance. The R3081 includes specific support for high performance systems, including signals necessary to implement external secondary caches, and the ability to perform hardware based cache coherency in multi-master systems.

Figure 6 shows a typical system implementation. Transparent latches are used to de-multiplex the R3081 address and data busses from the A/D bus. The data paths between the memory system elements and the A/D bus is managed by simple octal devices. A small set of simple PALs is used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Depending on the cost vs. performance tradeoffs appropriate

to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize a simpler, lower performance memory system to reduce cost and simplify the design. Similarly, the system designer could choose to implement techniques such as external secondary cache, or DMA, to further improve system performance.

## DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, sub-system modules, and shrink wrap operating systems. The R3081, which is pin and software compatible with the R3051, can directly utilize these existing tools to reduce time to market.

Figure 7 is an overview of the system development process typically used when developing R3051 family applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family applications, and include tools such as:

- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT/sim™, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™, which implements a run-time support package for R3051 family systems.

## PERFORMANCE OVERVIEW

The R3081 achieves a very high-level of performance. This performance is based on:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 VUPS performance when operating out of cache.
- A full featured floating point accelerator/co-processor. The R3081 incorporates an R3010A compatible floating point accelerator on-chip, with independent ALUs for floating point add, multiply, and divide. The floating point unit is fully hardware interlocked, and features overlapped operation and precise exceptions. The FPA allows floating point adds, multiplies, and divides to occur concurrently with each other, as well as concurrently with integer operations.
- Large on-chip caches. The R3051 family contains caches which are substantially larger than those on the majority of today's microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate. The R3081 doubles the cache available on the R3052, making it a suitable engine for

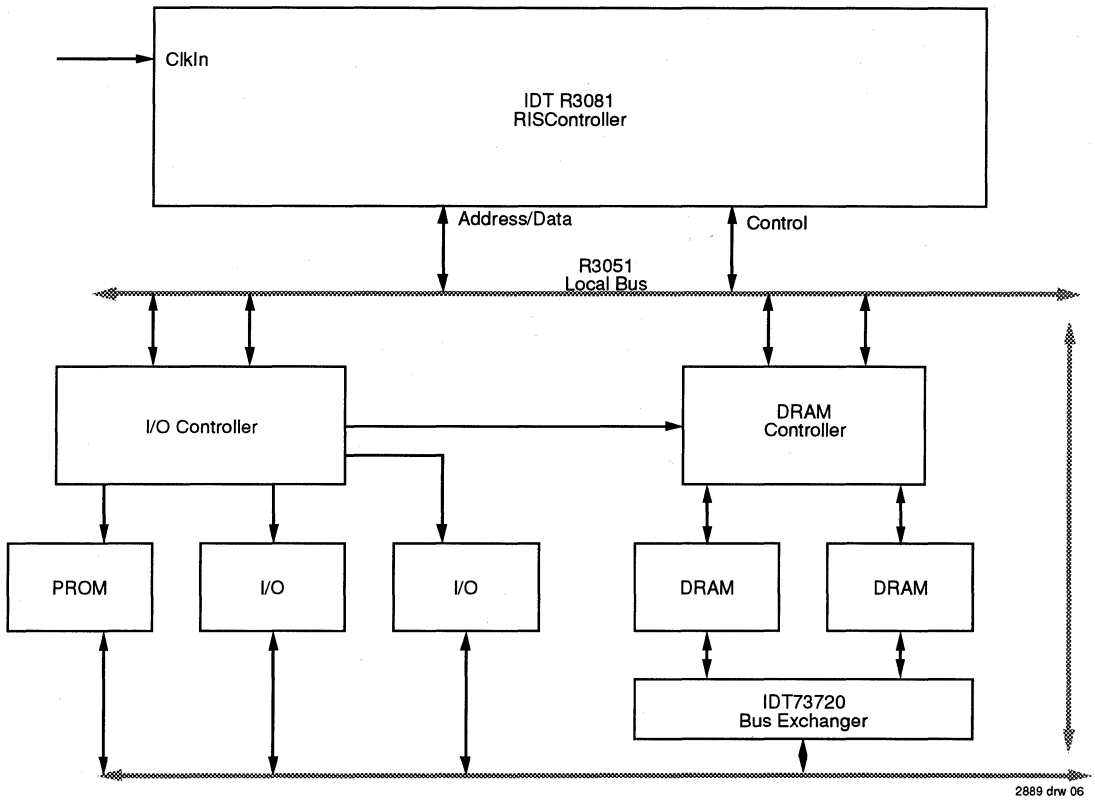


Figure 6. R3081 RISChipset Based System

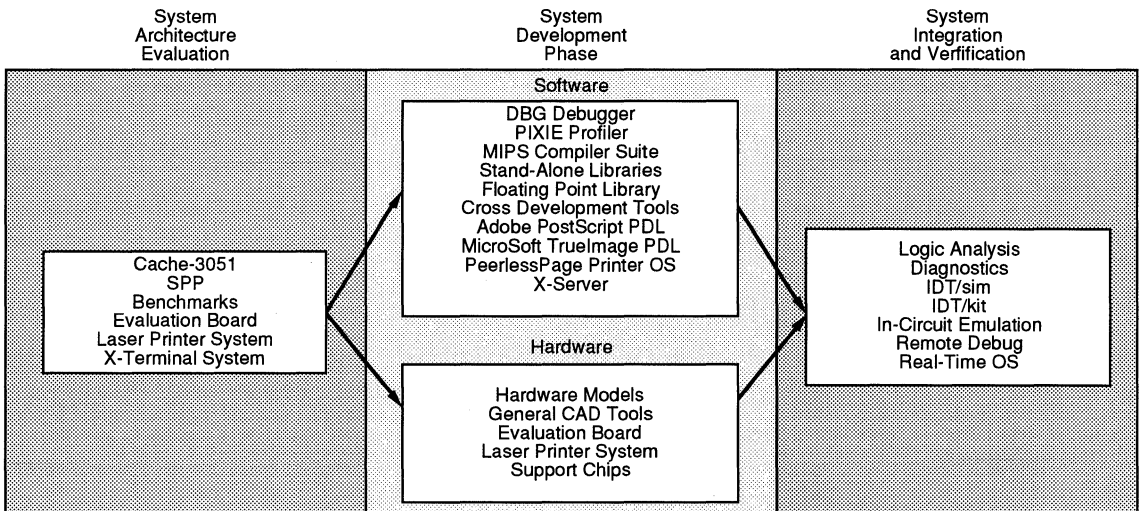


Figure 7. R3051 Family Development Toolchain

many general purpose computing applications, such as ARC compliant systems.

- Autonomous multiply and divide operations. The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the CPU to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R3081 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve over 35 VUPS integer performance, 11MFlops of Linpack performance, and 64,000 dhrystones without the use of external caches or zero wait-state memory devices.

The performance differences between the various family members depends on the application software and the design of the memory system. The impact of the various cache sizes, and the hardware floating point, can be accurately modeled using Cache-3051. Since the R3051, R3052, and R3081 are all pin and software compatible, the system designer has maximum freedom in trading between performance and cost. A system can be designed, and later the appropriate CPU inserted into the board, depending on the desired system performance.

## SELECTABLE FEATURES

The R3081 allows the system designer to configure certain aspects of operation. Some of these options are established when the device is reset, while others are enabled via the Config registers:

- BigEndian vs. LittleEndian Byte Ordering. The part can be configured to operate with either byte ordering. ACE/ARC systems typically use Little Endian byte ordering. However, various embedded applications, written originally for a Big Endian processor such as the MC680x0, are easier to port to a Big Endian system.
- Data Cache Refill of one or four words. The memory system must be capable of performing four word refills of instruction cache misses. The R3081 allows the system designer to enable D-Cache refill of one or four words dynamically. Thus, specialized algorithms can choose one refill size, while the rest of the system can operate with the other.
- Half-frequency bus mode. The processor can be configured such that the external bus interface is at one-half the frequency of the processor core. This simplifies system design; however, the large on-chip caches mitigate the performance impact of using a slower system bus clock.
- Slow bus turn-around. The R3081 allows the system designer to space processor operations, so that more time

is allowed for transitions between memory and the processor on the multiplexed address/data bus.

- Configurable cache. The R3081 allows the system designer to use software to select either a 16kB Instruction Cache/4kB Data Cache organization, or an 8kB Instruction/8kB Data Cache organization.
- Cache Coherent Interface. The R3081 has an optional hardware based cache coherency interface intended to support multi-master systems such as those utilizing DMA between memory and I/O.
- Optional 1x or 2x clock input. The R3081 can be driven with an R3051 compatible 2x clock input, or a lower frequency 1x clock input.

## THERMAL CONSIDERATIONS

The R3081 utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, the R3081 is packaged using cavity down packaging, with an embedded thermal slug to improve thermal transfer to the surrounding air.

The R3081 utilizes the 84-pin MQAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQAD package allows for an efficient thermal transfer between the die and the case due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQAD package is available at all frequencies, and is pin and form compatible with the PLCC used for the R3051. Thus, designers can inter-change R3081s and R3051s in a particular design, without changing their PC Board.

The R3081 is guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient temperature conditions which will meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 1.

Note that the R3081 allows the operational frequency to be turned down during idle periods to reduce power consumption. This operation is described in the *R3081 Hardware User's Guide*. Reducing the operation frequency dramatically reduces power consumption.

Airflow (ft/min)	ØCA					
	0	200	400	600	800	1000
"MJ" Package*	22	14	12	11	9	8
PLCC Package	29	26	21	18	16	15

2889 tbl 01

**Table 1. Thermal Resistance (ØCA) at Various Airflows**  
(\*estimated: final values tbd)

## NOTES ON SYSTEM DESIGN

The R3081 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

To minimize these AC parameters, the R3081 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3081 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to

minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3081 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

## PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	<p><b>Address/Data:</b> A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer.</p> <p>Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of:</p> <p><b>Address(31:4):</b> The high-order address for the transfer is presented on A/D(31:4).</p> <p><b><math>\overline{BE}</math>(3:0):</b> These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0).</p> <p>During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.</p> <p>During cache coherency operations, the R3081 monitors the A/D bus at the start of a DMA write to capture the write target address for potential data cache invalidates.</p>
Addr(3:2)	O	<p><b>Low Address (3:2)</b> A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.</p> <p>During cache coherency operations, the R3081 monitors the Addr bus at the start of a DMA write to capture the write target address for potential data cache invalidates.</p>
Diag(1)	O	<p><b>Diagnostic Pin 1.</b> This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed:</p> <p><b>Cached:</b> During the phase in which the A/D bus presents address information, this pin is an active HIGH output which indicates whether the current read is a result of a cache miss.</p> <p><b>Miss Address (3):</b> During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p> <p>On write cycles, this output signals whether the data being written as retained in the on-chip data cache. The value of this pin is time multiplexed during writes:</p> <p><b>Cached:</b> During the address phase of write transactions, this signal is an active high output which indicates that the store data was retained in the on-chip data cache.</p> <p><b>Reserved:</b> The value of this pin during the data phase of writes is reserved.</p>
Diag(0)	O	<p><b>Diagnostic Pin 0.</b> This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed:</p> <p><b><math>\overline{ID}</math>:</b> If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase.</p> <p><b>Miss Address (2):</b> During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.</p> <p>During write cycles, the value of this pin during both the address and data phases is reserved.</p>

2889 tbl 02



**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
ALE	I/O	<b>Address Latch Enable:</b> Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.  During cache coherency operations, the R3081 monitors ALE at the start of a DMA write, to capture the write target address for potential data cache invalidates.
$\overline{Rd}$	O	<b>Read:</b> An output which indicates that the current bus transaction is a read.
$\overline{Wr}$	I/O	<b>Write:</b> An output which indicates that the current bus transaction is a write. During coherent DMA, this input indicates that the current transfer is a write.
$\overline{DataEn}$	O	<b>External Data Enable:</b> This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers
$\overline{Burst}/\overline{WrNear}$	O	<b>Burst Transfer/Write Near:</b> On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if quad word refill is currently selected.  On write transactions, the $\overline{WrNear}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 512 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{Ack}$	I	<b>Acknowledge:</b> An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.  During Coherent DMA, this input indicates that the current write transfer is completed, and that the internal invalidation address counter should be incremented.
$\overline{RdCEn}$	I	<b>Read Buffer Clock Enable:</b> An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	<b>System Reference Clock:</b> An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit. This clock will either be at the same frequency as the CPU execution rate clock, or at one-half that frequency, as selected during reset.
$\overline{BusReq}$	I	<b>DMA Arbiter Bus Request:</b> An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	O	<b>DMA Arbiter Bus Grant.</b> An output from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{IvdReq}$	I	<b>Invalidate Request.</b> An input provided by an external DMA controller to request that the CPU invalidate the Data Cache line corresponding to the current DMA write target address. This signal is the same pin as Diag(0)
$\overline{CohReq}$	I	<b>Coherent DMA Request.</b> An input used by the external DMA controller to indicate that the requested DMA operations could involve hardware cache coherency. This signal is the Rsvd(0) of the R3051.
SBrCond(3:2) BrCond(0)	I	<b>Branch Condition Port:</b> These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously. Note that BrCond(1) is used by the internal FPA, and thus is not available on an external pin.
$\overline{BusError}$	I	<b>Bus Error:</b> Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.

2889 tbl 03

**PIN DESCRIPTION (Continued):**

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Int}}(5:3)$	I	<b>Processor Interrupt:</b> During normal operation, these signals are logically the same as the $\overline{\text{Int}}(5:0)$ $\overline{\text{SInt}}(2:0)$ signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000.  There are two types of interrupt inputs: the $\overline{\text{SInt}}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts. Note that the interrupt used by the on-chip FPA will not be monitored externally.
CkIn	I	<b>Master Clock Input:</b> This input clock can be provided at the execution frequency of the CPU (1x clock mode) or at twice that frequency (2x clock mode), as selected at reset..
$\overline{\text{Reset}}$	I	<b>Master Processor Reset:</b> This signal initializes the CPU. Mode selection is performed during the last cycle of Reset.
Rsvd(4:1)	I/O	<b>Reserved:</b> These four signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins. Note that Rsvd(0) of the R3051 is now used for the $\overline{\text{CohReq}}$ input pin.

2889 tbl 04

**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
Tc	Operating Case Temperature	0 to +85	-55 to +125	°C
TBIAS	Case Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
VIN	Input Voltage	-0.5 to +7.0	-0.5 to +7.0	V

2889 tbl 05

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed Vcc +0.5V.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature(Case)	GND	Vcc
Military	-55°C to +125°C	0V	5.0 ±10%
Commercial	0°C to +85°C	0V	5.0 ±5%
Commercial	0°C to +85°C	0V	3.3 ±5%

2889 tbl 07

**AC TEST CONDITIONS—R3081**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.0	—	V
V <sub>IL</sub>	Input LOW Voltage	—	0.4	V
V <sub>IHS</sub>	Input HIGH Voltage	3.5	—	V
V <sub>ILS</sub>	Input LOW Voltage	—	0.4	V

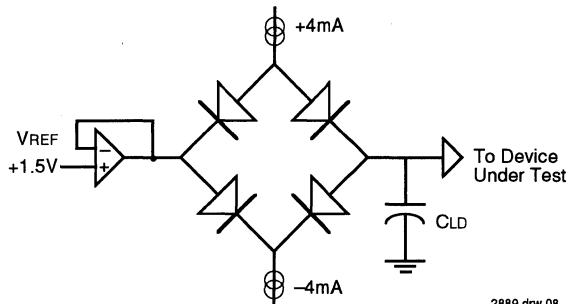
2889 tbl 06

**AC TEST CONDITIONS—RV3081**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.0	—	V
V <sub>IL</sub>	Input LOW Voltage	—	0.4	V
V <sub>IHS</sub>	Input HIGH Voltage	3.0	—	V
V <sub>ILS</sub>	Input LOW Voltage	—	0.4	V

2889 tbl 06

**OUTPUT LOADING FOR AC TESTING**



2889 drw 08

Signal	CLD
SysCLK	50 pf
All Others	25 pf

2889 tbl 08

**DC ELECTRICAL CHARACTERISTICS R3081****COMMERCIAL TEMPERATURE RANGE** — ( $T_C = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 5\%$ )

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		50MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
VOL	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage <sup>(2,3)</sup>	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	V
VILS	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
CIN	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	—	10	pF
COU	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	—	10	—	10	pF
ICC	Operating Current	$V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$	—	850	—	950	—	1050	—	1200	—	825	mA
I <sub>IH</sub>	Input HIGH Leakage	$V_{IH} = V_{CC}$	—	100	—	100	—	100	—	100	—	100	μA
I <sub>IL</sub>	Input LOW Leakage	$V_{IL} = \text{GND}$	-100	—	-100	—	-100	—	-100	—	-100	—	μA
I <sub>OZ</sub>	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-100	100	-100	100	-100	100	-100	100	-100	100	μA

**NOTES:**

2889 tbi 09

1.  $V_{IL}$  Min. =  $-3.0\text{V}$  for pulse width less than 15ns.  $V_{IL}$  should not fall below  $-0.5\text{V}$  for larger periods.
2.  $V_{IHS}$  and  $V_{ILS}$  apply to  $\text{ClkIn}$  and  $\text{Reset}$ .
3.  $V_{IH}$  should not be held above  $V_{CC} + 0.5\text{V}$ .
4. Guaranteed by design.

## AC ELECTRICAL CHARACTERISTICS R3081

COMMERCIAL TEMPERATURE RANGE <sup>(1, 2)</sup> (20, 25, 33MHz)—(T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, $\overline{\text{Ack}}$ , BusError, RdCEn, CohReq	Set-up to SysClk rising	6	—	5	—	4	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	ns
t2	BusReq, $\overline{\text{Ack}}$ , BusError, RdCEn, CohReq	Hold from SysClk rising	4	—	4	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ Burst/ $\overline{\text{WrNear}}$ , Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ Burst/ $\overline{\text{WrNear}}$ , Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	ns
t7	$\overline{\text{Wr}}$ , Rd, Burst/ $\overline{\text{WrNear}}$ , A/D	Valid from SysClk rising	—	5	—	5	—	4	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	ns
t11	$\overline{\text{DataEn}}$	Asserted from SysClk falling	—	15	—	15	—	13	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state <sup>(3)</sup>	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(3)</sup>	0	—	0	—	0	—	ns
t15	$\overline{\text{Wr}}$ , Rd, DataEn, Burst/ $\overline{\text{WrNear}}$	Negated from SysClk falling	—	7	—	6	—	5	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	ns
t17	Diag	Valid from SysClk	—	12	—	11	—	10	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	ns
t19	A/D	SysClk falling to data out	—	13	—	12	—	11	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	10	—	8	—	6.5	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	10	—	8	—	6.5	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	15	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	200	—	μs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	32	—	tsys
t25	$\overline{\text{Reset}}$	Set-up to SysClk falling	6	—	5	—	4	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	10	—	9	—	8	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	0	—	0	—	0	—	ns
t28	$\overline{\text{SInt}}$ , SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	ns
t29	$\overline{\text{SInt}}$ , SBrCond	Hold from SysClk falling	3	—	3	—	2	—	ns
t30	$\overline{\text{Int}}$ , BrCond	Set-up to SysClk falling	6	—	5	—	4	—	ns
t31	$\overline{\text{Int}}$ , BrCond	Hold from SysClk falling	3	—	3	—	2	—	ns
tsys	SysClk (full frequency mode)	Pulse Width <sup>(5)</sup>	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	SysClk (full frequency mode)	Clock HIGH Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	ns

## NOTES:

2889 tbl 10

- All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
- The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
- In 1x clock mode, t22 is replaced by t44/2.
- In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.

**AC ELECTRICAL CHARACTERISTICS R3081 (cont.)**

**COMMERCIAL TEMPERATURE RANGE<sup>(1, 2)</sup> — (T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)**

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t33	SysClk (full frequency mode)	Clock LOW Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	ns
tsys/2	SysClk (half frequency mode)	Pulse Width <sup>(5)</sup>	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	
t34	SysClk (half frequency mode)	Clock HIGH Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	ns
t35	SysClk (half frequency mode)	Clock LOW Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	ns
t36	ALE	Set-up to SysClk falling	9	—	8	—	7	—	ns
t37	ALE	Hold from SysClk falling	2	—	2	—	1	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	8	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	1	—	ns
t40	W <sub>r</sub>	Set-up to SysClk rising	10	—	9	—	8	—	ns
t41	W <sub>r</sub>	Hold from SysClk rising	3	—	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH <sup>(6)</sup>	20	—	16	—	13	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW <sup>(6)</sup>	20	—	16	—	13	—	ns
t44	ClkIn (1x clock mode)	Clock Period <sup>(6)</sup>	50	50	40	50	30	50	ns
tderate	All outputs	Timing deration for loading over CLD <sup>(3, 4)</sup>	—	0.5	—	0.5	—	0.5	ns/ 25pF

**NOTES:**

2889 tbl 11

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.

**AC ELECTRICAL CHARACTERISTICS R3081**

**COMMERCIAL TEMPERATURE RANGE<sup>(1, 2)</sup> (40, 50MHz) — (T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +5.0V ±5%)**

Symbol	Signals	Description	40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	
t1	BusReq, AcK, BusError, RdCEn, CohReq	Set-up to SysClk rising	3	—	2.5	—	ns
t1a	A/D	Set-up to SysClk falling	4.5	—	4.0	—	ns
t2	BusReq, AcK, BusError, RdCEn, CohReq	Hold from SysClk rising	3	—	2	—	ns
t2a	A/D	Hold from SysClk falling	1	—	1.5	—	ns
t3	A/D, Addr, Diag, ALE, W <sub>r</sub> Burst/W <sub>r</sub> Near, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, W <sub>r</sub> Burst/W <sub>r</sub> Near, Rd, DataEn	Driven from SysClk falling	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	5	—	4	ns
t6	BusGnt	Negated from SysClk falling	—	5	—	3.5	ns
t7	W <sub>r</sub> , Rd, Burst/W <sub>r</sub> Near, A/D	Valid from SysClk rising	—	3.5	—	3.0	ns
t8	ALE	Asserted from SysClk rising	—	3	—	2	ns
t9	ALE	Negated from SysClk falling	—	3	—	2	ns
t10	A/D	Hold from ALE negated	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	12	—	11	ns
t12	DataEn	Asserted from A/D tri-state <sup>(3)</sup>	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(3)</sup>	0	—	0	—	ns
t15	W <sub>r</sub> , Rd, DataEn, Burst/W <sub>r</sub> Near	Negated from SysClk falling	—	4	—	3.5	ns
t16	Addr(3:2)	Valid from SysClk	—	4.5	—	4.0	ns
t17	Diag	Valid from SysClk	—	9	—	7	ns

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## AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

COMERCIAL TEMPERATURE RANGE <sup>(1, 2)</sup> (40, 50MHz)— (T<sub>c</sub> = 0°C to +85°C, V<sub>cc</sub> = +5.0V ±5%)

Symbol	Signals	Description	40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	
t18	A/D	Tri-state from SysClk falling	—	8	—	8	ns
t19	A/D	SysClk falling to data out	—	10	—	8	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	5.6	—	N/A <sup>(1)</sup>	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	5.6	—	N/A <sup>(1)</sup>	—	ns
t22	ClkIn (2x clock mode)	Clock Period	12.5	250	N/A <sup>(1)</sup>	—	ns
t23	Reset	Pulse Width from Vcc valid	200	—	32	—	μs
t24	Reset	Minimum Pulse Width	32	—	2	—	tsys
t25	Reset	Set-up to SysClk falling	3	—	3	—	ns
t26	In̄	Mode set-up to Reset rising	7	—	2	—	ns
t27	In̄	Mode hold from Reset rising	0	—	2.5	—	ns
t28	SIn̄, SBrCond	Set-up to SysClk falling	3	—	3	—	ns
t29	SIn̄, SBrCond	Hold from SysClk falling	2	—	1.5	—	ns
t30	In̄, BrCond	Set-up to SysClk falling	3	—	2	—	ns
t31	In̄, BrCond	Hold from SysClk falling	2	—	1.5	—	ns
tsys	SysClk (full frequency mode)	Pulse Width <sup>(5)</sup>	2*t22	2*t22	t44	t44	ns
t32	SysClk (full frequency mode)	Clock HIGH Time <sup>(5)</sup>	t22-1	t22+1	t44/2-1	t44/2+1	ns
t33	SysClk (full frequency mode)	Clock LOW Time <sup>(5)</sup>	t22-1	t22+1	t44/2-1	t44/2+1	ns
tsys/2	SysClk (half frequency mode)	Pulse Width <sup>(5)</sup>	4*t22	4*t22	2*t44	2*t44	ns
t34	SysClk (half frequency mode)	Clock HIGH Time <sup>(5)</sup>	2*t22-1	2*t22+1	t44-1	t44+1	ns
t35	SysClk (half frequency mode)	Clock LOW Time <sup>(5)</sup>	2*t22-1	2*t22+1	t44-1	t44+1	ns
t36	ALE	Set-up to SysClk falling	6	—	5	—	ns
t37	ALE	Hold from SysClk falling	1	—	0	—	ns
t38	A/D	Set-up to ALE falling	8	—	7	—	ns
t39	A/D	Hold from ALE falling	1	—	0	—	ns
t40	Wr	Set-up to SysClk rising	7	—	6	—	ns
t41	Wr	Hold from SysClk rising	3	—	1	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH <sup>(6)</sup>	11	—	8.5	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW <sup>(6)</sup>	11	—	8.5	—	ns
t44	ClkIn (1x clock mode)	Clock Period <sup>(6)</sup>	25	50	20	50	ns
tderate	All outputs	Timing deration for loading over CLD <sup>(3, 4)</sup>	—	0.5	—	0.5	ns/ 25pF

## NOTE:

1. 1X Clock mode only.

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**DC ELECTRICAL CHARACTERISTICS RV3081****COMERCIAL TEMPERATURE RANGE** — ( $T_c = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{cc} = +3.3\text{V} \pm 5\%$ )

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	2.4	—	2.4	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	—	0.4	—	0.4	—	0.4	V
$V_{IH}$	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	2.0	—	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	—	0.8	V
$V_{IHS}$	Input HIGH Voltage <sup>(2,3)</sup>	—	2.8	—	2.8	—	2.8	—	V
$V_{ILS}$	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	—	0.4	V
$C_{IN}$	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	pF
$C_{OUT}$	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	—	10	pF
$I_{CC}$	Operating Current	$V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$	—	500	—	550	—	650	mA
$I_{IH}$	Input HIGH Leakage	$V_{IH} = V_{CC}$	—	100	—	100	—	100	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage	$V_{IL} = \text{GND}$	-100	—	-100	—	-100	—	$\mu\text{A}$
$I_{OZ}$	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-100	100	-100	100	-100	100	$\mu\text{A}$

**NOTES:**

- $V_{IL}$  Min. =  $-3.0\text{V}$  for pulse width less than 15ns.  $V_{IL}$  should not fall below  $-0.5\text{V}$  for larger periods.
- $V_{IHS}$  and  $V_{ILS}$  apply to  $CiIn$  and  $Reset$ .
- $V_{IH}$  should not be held above  $V_{CC} + 0.5\text{V}$ .
- Guaranteed by design.

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## AC ELECTRICAL CHARACTERISTICS RV3081

COMMERCIAL TEMPERATURE RANGE (1, 2) (T<sub>C</sub> = 0°C to +85°C, V<sub>CC</sub> = +3.3V ±5%)

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	6	—	5	—	4	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	4	—	4	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	—	4	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	—	13	ns
t12	DataEn	Asserted from A/D tri-state <sup>(3)</sup>	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(3)</sup>	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	—	5	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	ns
t17	Diag	Valid from SysClk	—	12	—	11	—	10	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	ns
t19	A/D	SysClk falling to data out	—	13	—	12	—	11	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	10	—	8	—	6.5	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	10	—	8	—	6.5	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	μs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	4	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	8	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3	—	3	—	2	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	4	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	3	—	2	—	ns
tsys	SysClk (full frequency mode)	Pulse Width <sup>(5)</sup>	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk (full frequency mode)	Clock HIGH Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	ns

## NOTES:

- All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
- The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
- In 1x clock mode, t22 is replaced by t44/2.
- In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.

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## AC ELECTRICAL CHARACTERISTICS RV3081 (cont.)

COMMERCIAL TEMPERATURE RANGE<sup>(1, 2)</sup> — ( $T_C = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +3.3\text{V} \pm 5\%$ )

Symbol	Signals	Description	20MHz		25MHz		33.33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t33	SysClk (full frequency mode)	Clock Low Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	t22-1	t22+1	ns
t <sub>sys/2</sub>	SysClk (half frequency mode)	Pulse Width <sup>(5)</sup>	4*t22	4*t22	4*t22	4*t22	4*t22	4*t22	
t34	SysClk (half frequency mode)	Clock HIGH Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	ns
t35	SysClk (half frequency mode)	Clock LOW Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	2*t22-1	2*t22+1	ns
t36	ALE	Set-up to SysClk falling	9	—	8	—	7	—	ns
t37	ALE	Hold from SysClk falling	2	—	2	—	1	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	8	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	1	—	ns
t40	Wr	Set-up to SysClk rising	10	—	9	—	8	—	ns
t41	Wr	Hold from SysClk rising	3	—	3	—	3	—	ns
t42	Clkin (1x clock mode)	Pulse Width HIGH <sup>(6)</sup>	20	—	16	—	13	—	ns
t43	Clkin (1x clock mode)	Pulse Width LOW <sup>(6)</sup>	20	—	16	—	13	—	ns
t44	Clkin (1x clock mode)	Clock Period <sup>(6)</sup>	50	50	40	50	30	50	ns
t <sub>derate</sub>	All outputs	Timing deration for loading over $C_{LD}$ <sup>(3, 4)</sup>	—	0.5	—	0.5	—	0.5	ns/ 25pF

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## NOTES:

- All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
- The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
- Guaranteed by design.
- This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
- In 1x clock mode, t22 is replaced by t44/2.
- In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.

## DC ELECTRICAL CHARACTERISTICS R3081

MILITARY TEMPERATURE RANGE — ( $T_C$ <sup>(5)</sup> =  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 10\%$ )

Symbol	Parameter	Test Conditions	20MHz		25MHz		Units
			Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	2.4	—	V
VOL	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(3)</sup>	—	2.0	—	2.0	—	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	—	—	0.8	—	0.8	V
V <sub>IHS</sub>	Input HIGH Voltage <sup>(2,3)</sup>	—	2.8	—	2.8	—	V
V <sub>ILS</sub>	Input LOW Voltage <sup>(1,2)</sup>	—	—	0.4	—	0.4	V
C <sub>IN</sub>	Input Capacitance <sup>(4)</sup>	—	—	10	—	10	pF
C <sub>OUT</sub>	Output Capacitance <sup>(4)</sup>	—	—	10	—	10	pF
I <sub>CC</sub>	Operating Current	$V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$	—	850	—	950	mA
I <sub>IH</sub>	Input HIGH Leakage	$V_{IH} = V_{CC}$	—	100	—	100	μA
I <sub>IL</sub>	Input LOW Leakage	$V_{IL} = \text{GND}$	-100	—	-100	—	μA
I <sub>OZ</sub>	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-100	100	-100	100	μA

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## NOTES:

- V<sub>IL</sub> Min. = -3.0V for pulse width less than 15ns. V<sub>IL</sub> should not fall below -0.5V for larger periods.
- V<sub>IHS</sub> and V<sub>ILS</sub> apply to Clkin and Reset.
- V<sub>IH</sub> should not be held above  $V_{CC} + 0.5\text{V}$ .
- Guaranteed by design.
- Case Temperatures are "instant on."

## AC ELECTRICAL CHARACTERISTICS R3081

MILITARY TEMPERATURE RANGE <sup>(1, 2)</sup> — ( $T_C^{(7)}$  = -55°C to +125°C,  $V_{CC}$  = +5.0V ±10%)

Symbol	Signals	Description	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	6	—	5	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	4	—	4	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	ns
t8	ALE	Asserted from SysClk rising	—	4.5	—	4.5	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	ns
t10	A/D	Hold from ALE negated <sup>(3)</sup>	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state <sup>(3)</sup>	0	—	0	—	ns
t14	A/D	Driven from SysClk rising <sup>(3)</sup>	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	ns
t17	Diag	Valid from SysClk	—	12	—	11	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	ns
t19	A/D	SysClk falling to data out	—	13	—	12	ns
t20	Clkin (2x clock mode)	Pulse Width HIGH	10	—	8	—	ns
t21	Clkin (2x clock mode)	Pulse Width LOW	10	—	8	—	ns
t22	Clkin (2x clock mode)	Clock Period	25	250	20	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	μs
t24	Reset	Minimum Pulse Width	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3.5	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	3.5	—	3	—	ns
tsys	SysClk (full frequency mode)	Pulse Width <sup>(5)</sup>	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk (full frequency mode)	Clock High Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	ns

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## NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.
7. Case Temperatures are "instant on."

## AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

MILITARY TEMPERATURE RANGE<sup>(1, 2)</sup> (T<sub>C</sub><sup>(7)</sup> = -55°C to +125°C, V<sub>CC</sub> = +5.0V ±10%)

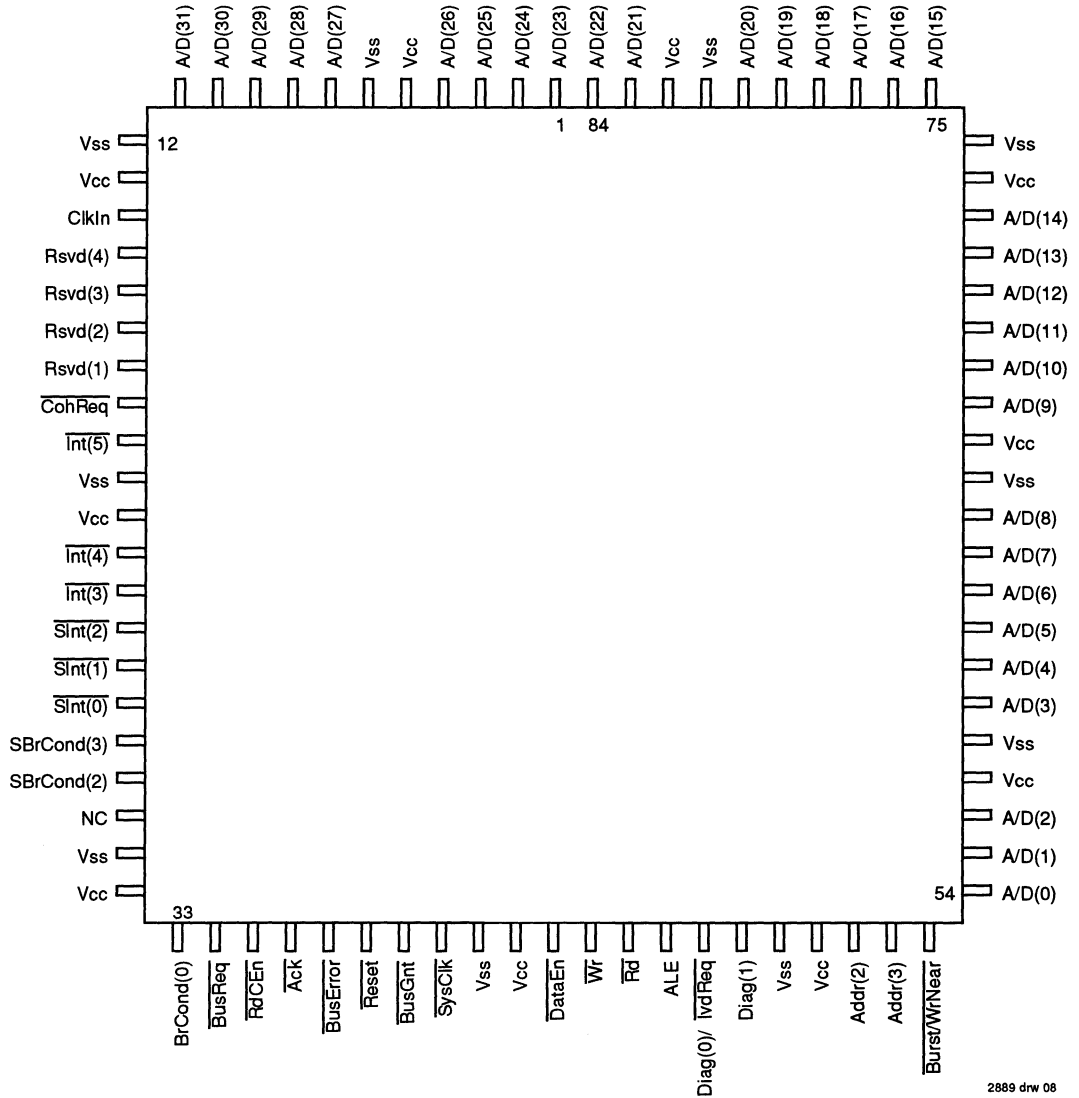
Symbol	Signals	Description	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t33	$\overline{\text{SysClk}}$ (full frequency mode)	Clock LOW Time <sup>(5)</sup>	t22-2	t22+2	t22-2	t22+2	ns
tsys/2	$\overline{\text{SysClk}}$ (half frequency mode)	Pulse Width <sup>(5)</sup>	4*t22	4*t22	4*t22	4*t22	ns
t34	$\overline{\text{SysClk}}$ (half frequency mode)	Clock HIGH Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t35	$\overline{\text{SysClk}}$ (half frequency mode)	Clock LOW Time <sup>(5)</sup>	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t36	ALE	Set-up to $\overline{\text{SysClk}}$ falling	9	—	8	—	ns
t37	ALE	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	ns
t40	$\overline{\text{Wr}}$	Set-up to $\overline{\text{SysClk}}$ rising	10	—	9	—	ns
t41	$\overline{\text{Wr}}$	Hold from $\overline{\text{SysClk}}$ rising	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH <sup>(6)</sup>	20	—	16	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW <sup>(6)</sup>	20	—	16	—	ns
t44	ClkIn (1x clock mode)	Clock Period <sup>(6)</sup>	50	50	40	50	ns
tderate	All outputs	Timing deration for loading over CLD <sup>(3, 4)</sup>	—	0.5	—	0.5	ns/ 25pF

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## NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual*.
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.
7. Case Temperatures are "instant on."

PIN CONFIGURATIONS



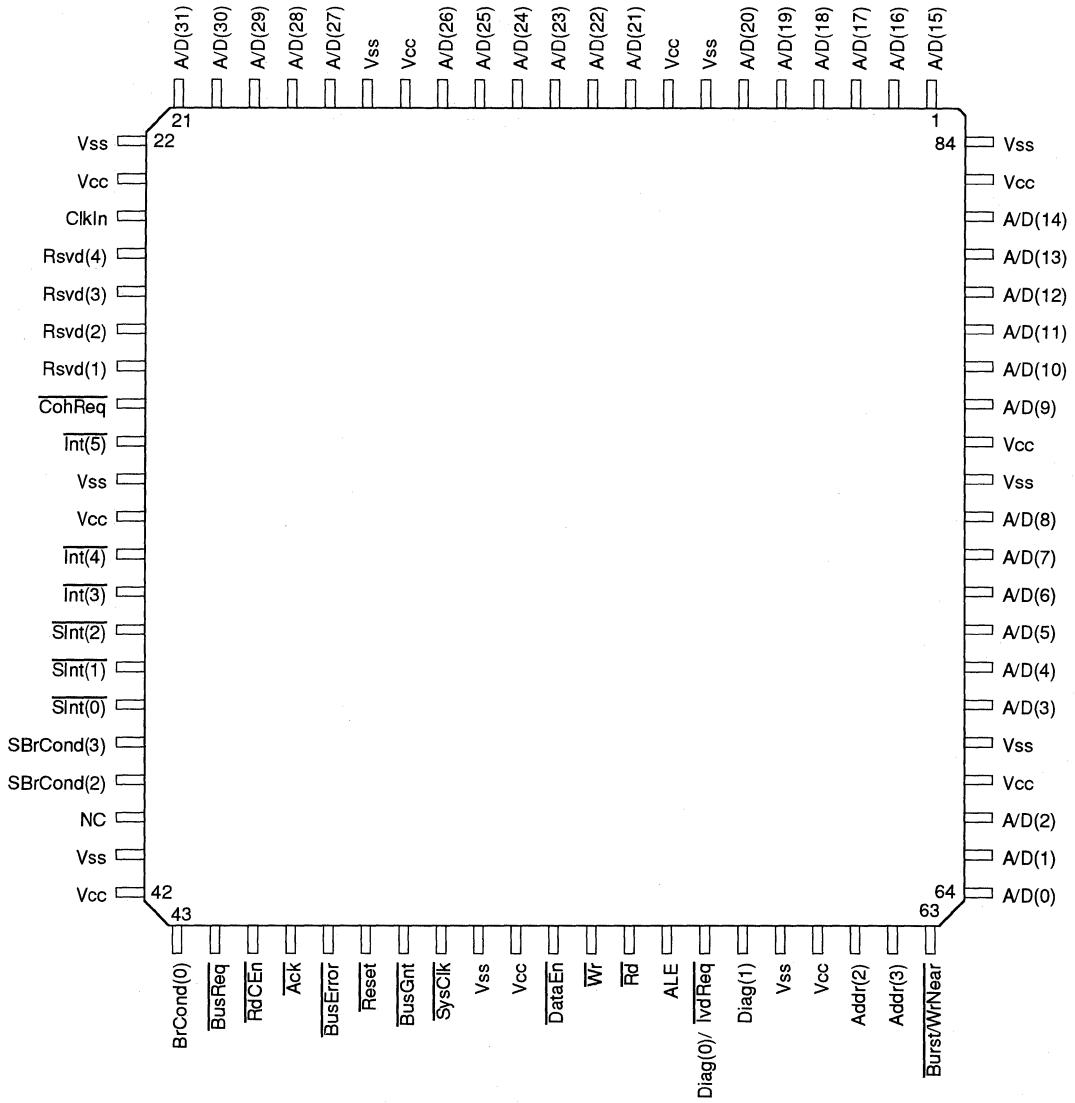
84-Pin MQAD/PLCC  
 Top View

2889 drw 08

**NOTE:**  
 Reserved Pins must not be connected.

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**PIN CONFIGURATIONS**



**84-Pin FD  
Top View**

**NOTE:**  
Reserved Pins must not be connected.

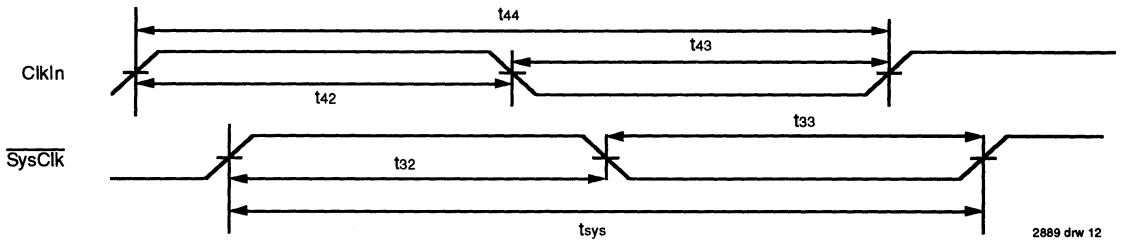


Figure 8 (a). R3081 Clcking (1x clock input mode, full frequency bus)

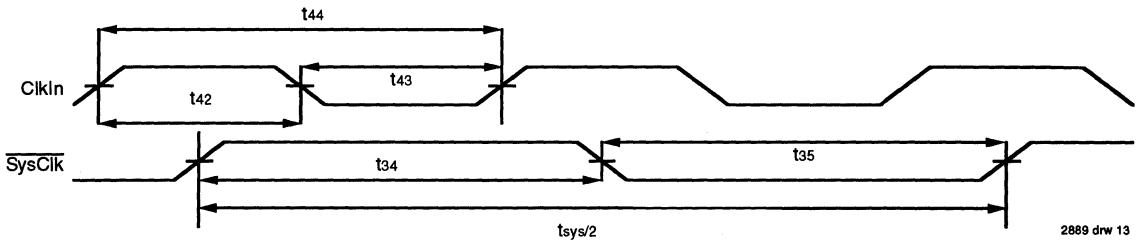


Figure 8 (b). R3081 Clcking (1x clock input mode, half-frequency bus)

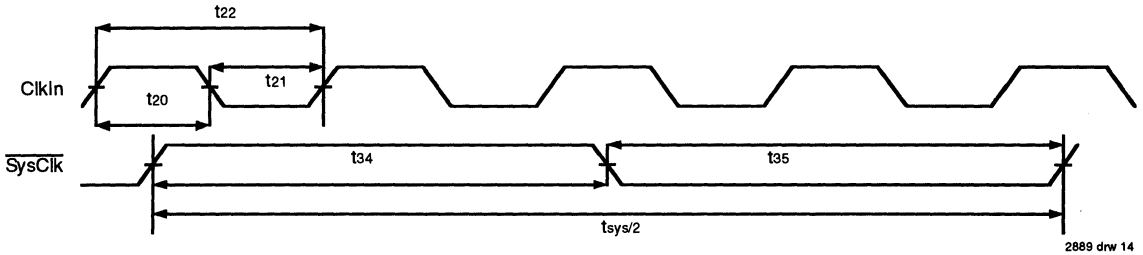


Figure 8 (c). R3081 Clcking (2x clock input mode, half-frequency bus)

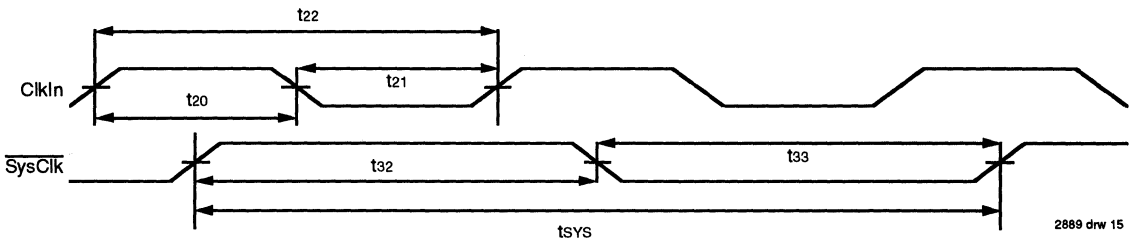


Figure 8 (d). R3081 Clcking (2x clock input mode, full-frequency bus)

5

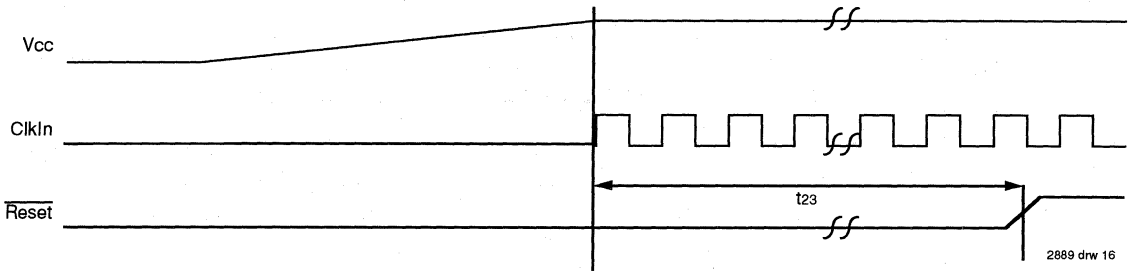


Figure 9. Power-On Reset Sequence

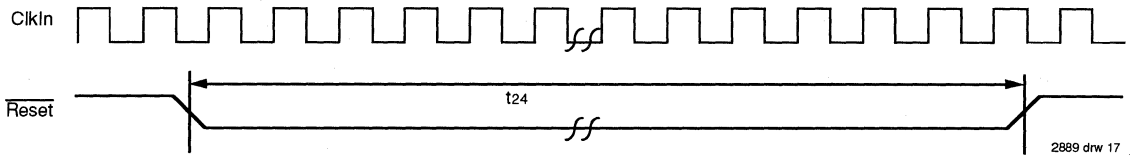


Figure 10. Warm Reset Sequence

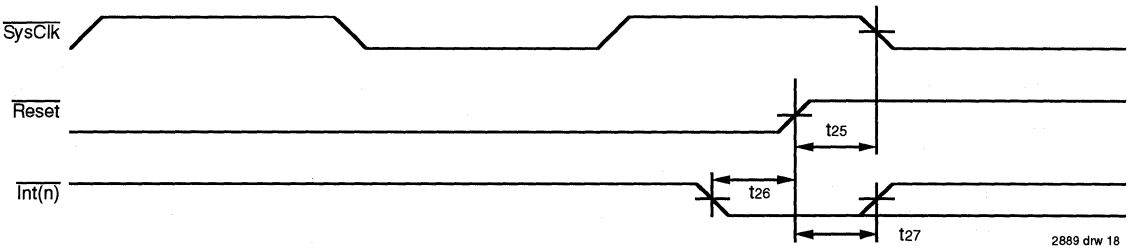
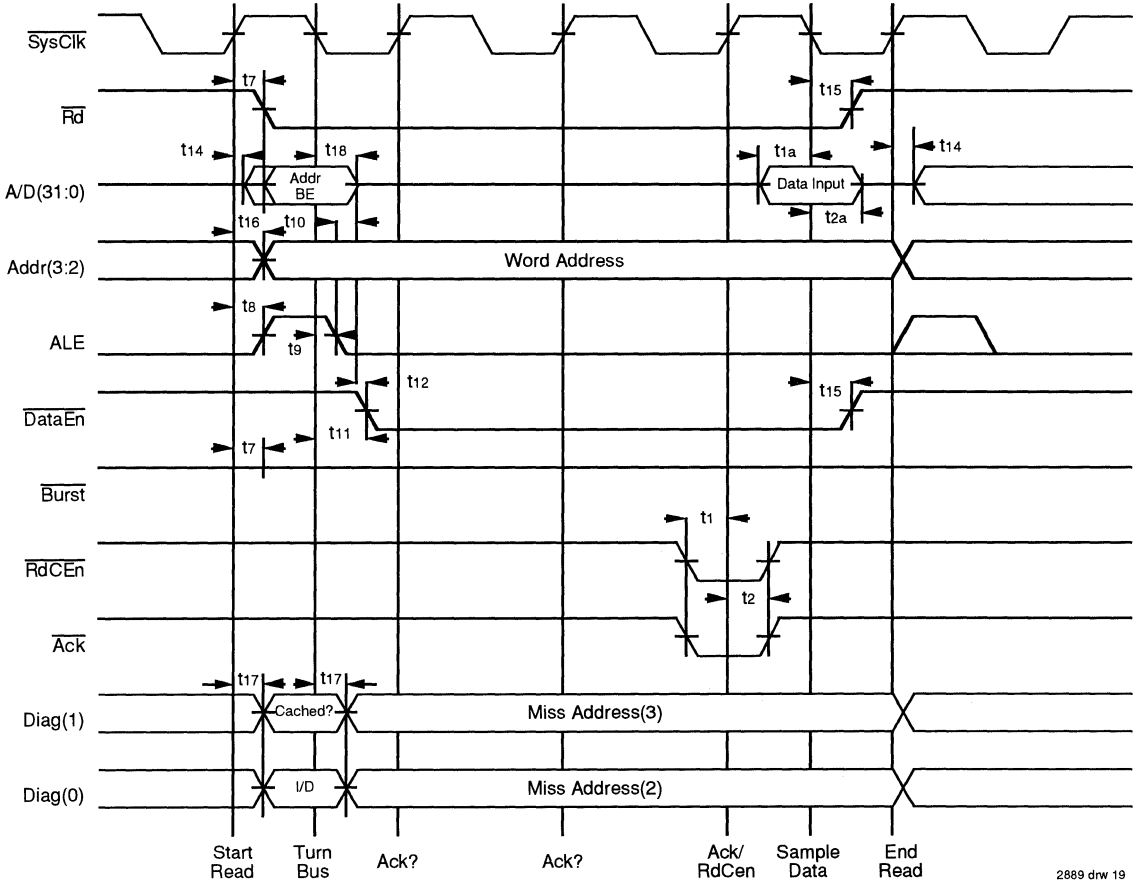


Figure 11. Mode Selection and Negation of Reset

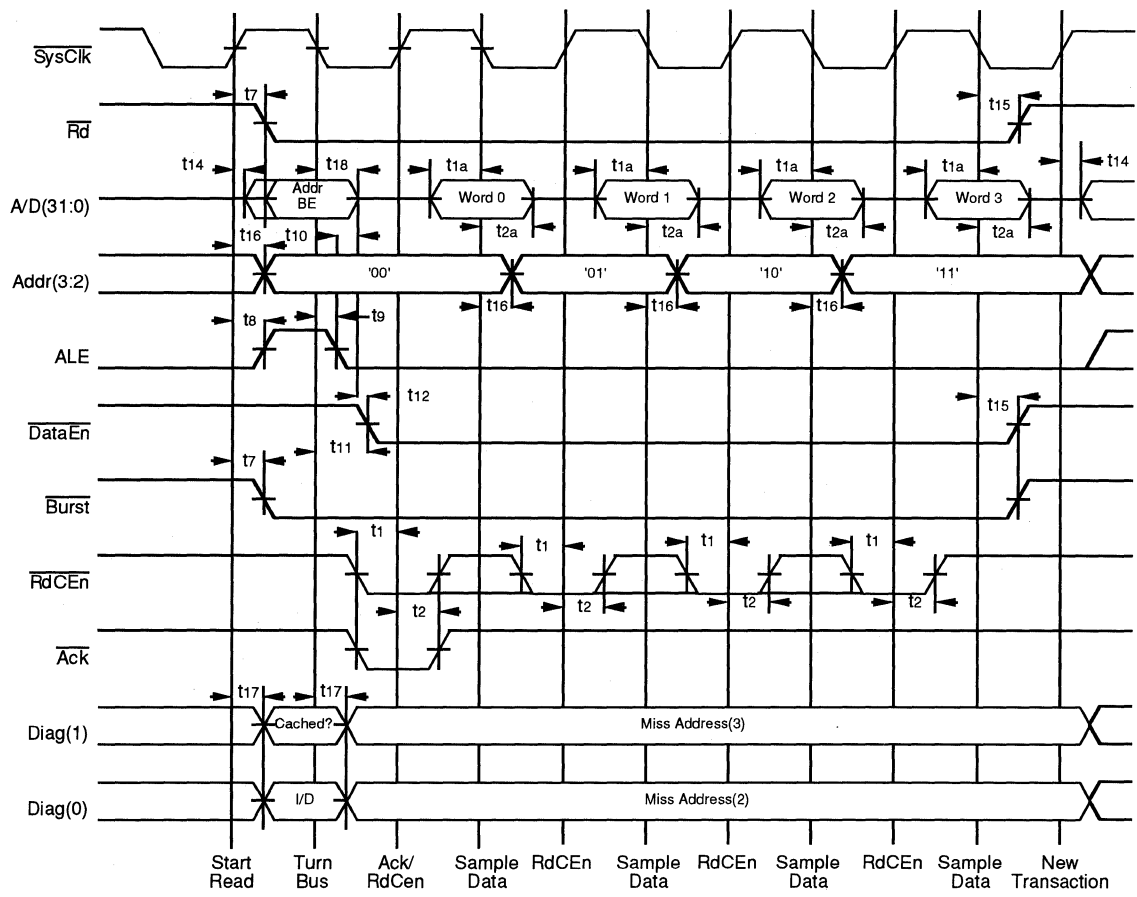


2889 drw 19

Figure 12. Single Datum Read in R3081

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2889 drw 20

Figure 13. R3081 Burst Read

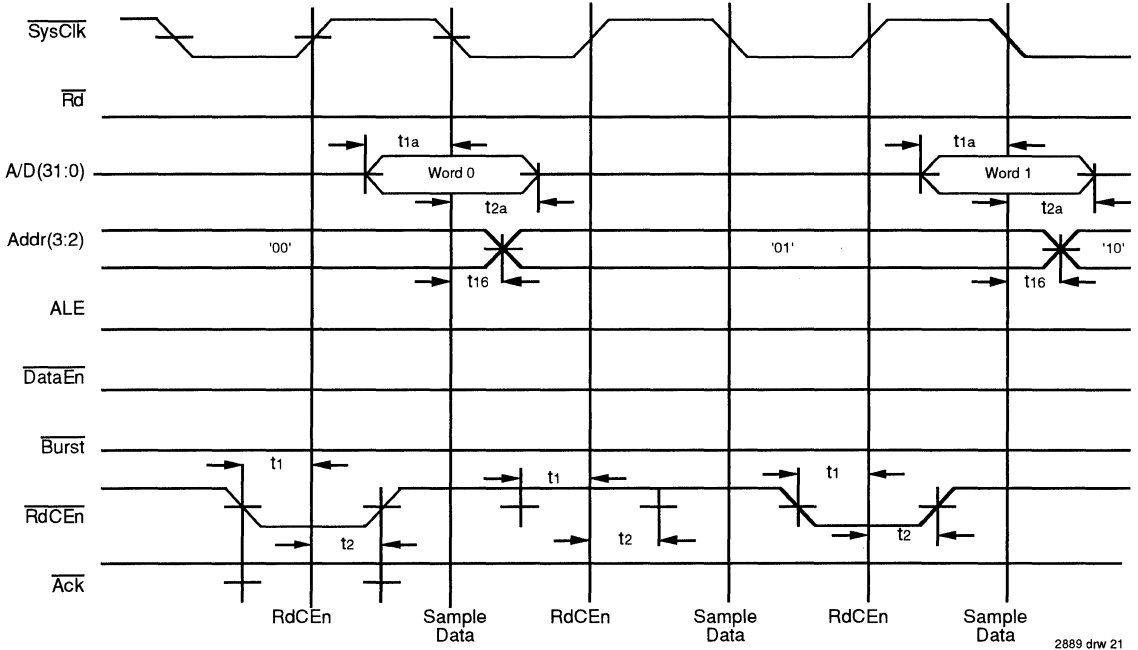


Figure 14 (a). Start of Throttled Quad Read

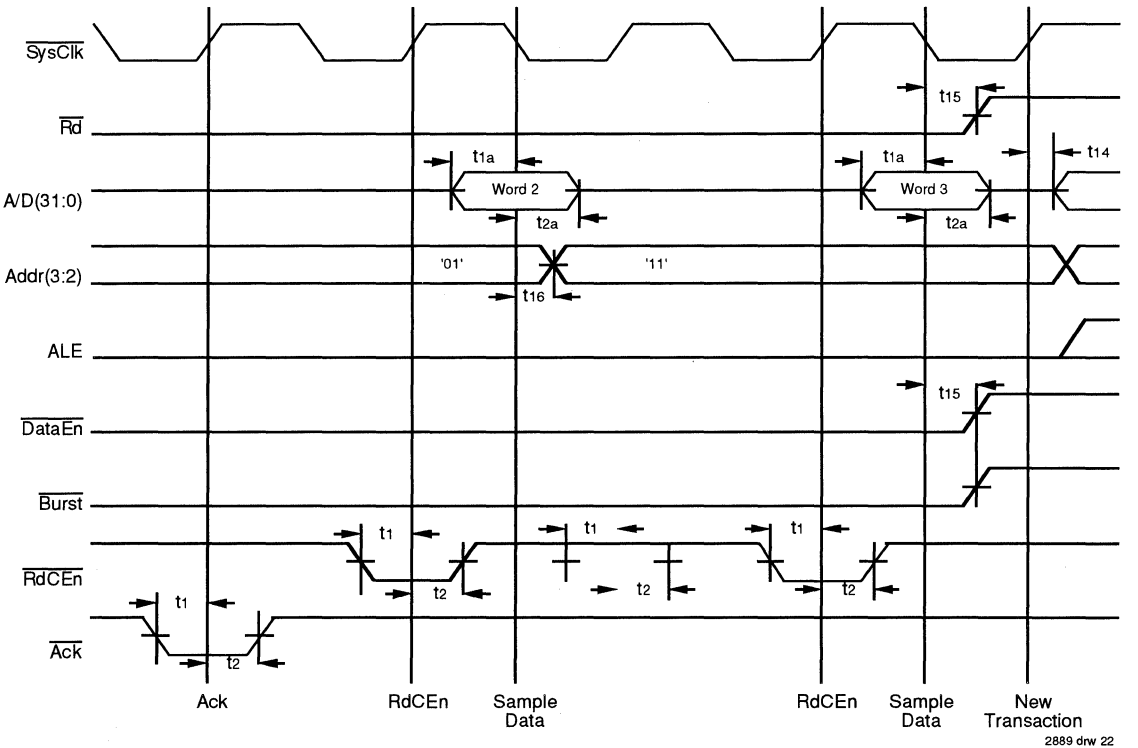


Figure 14 (b). End of Throttled Quad Read

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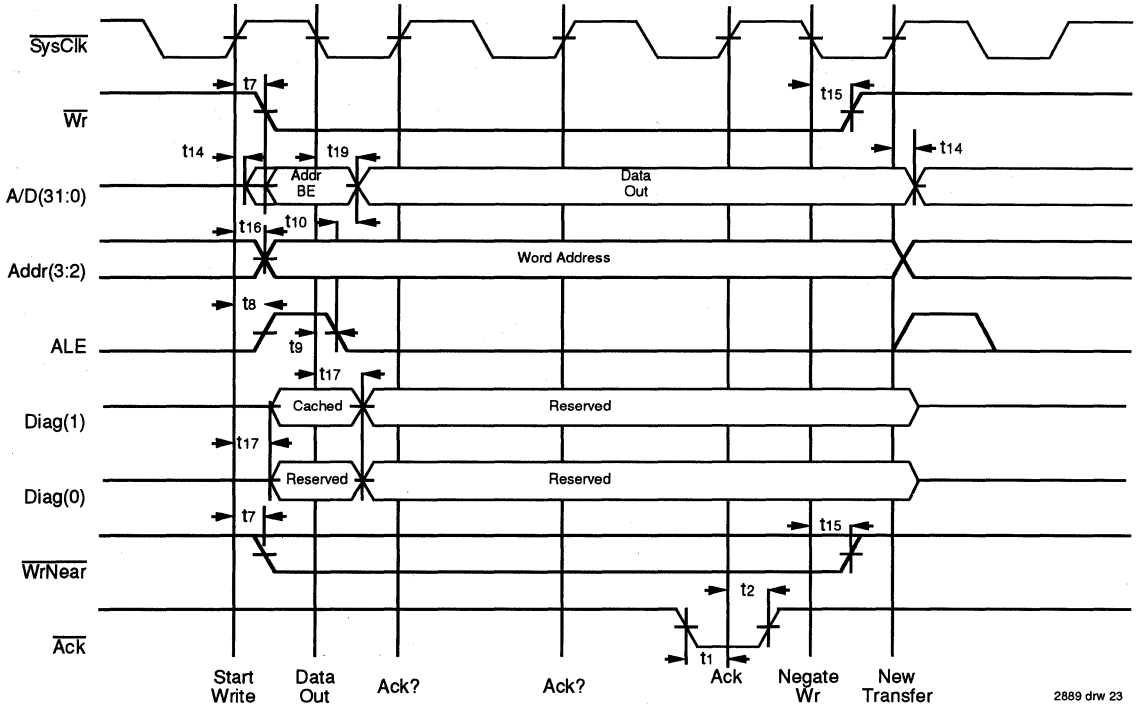


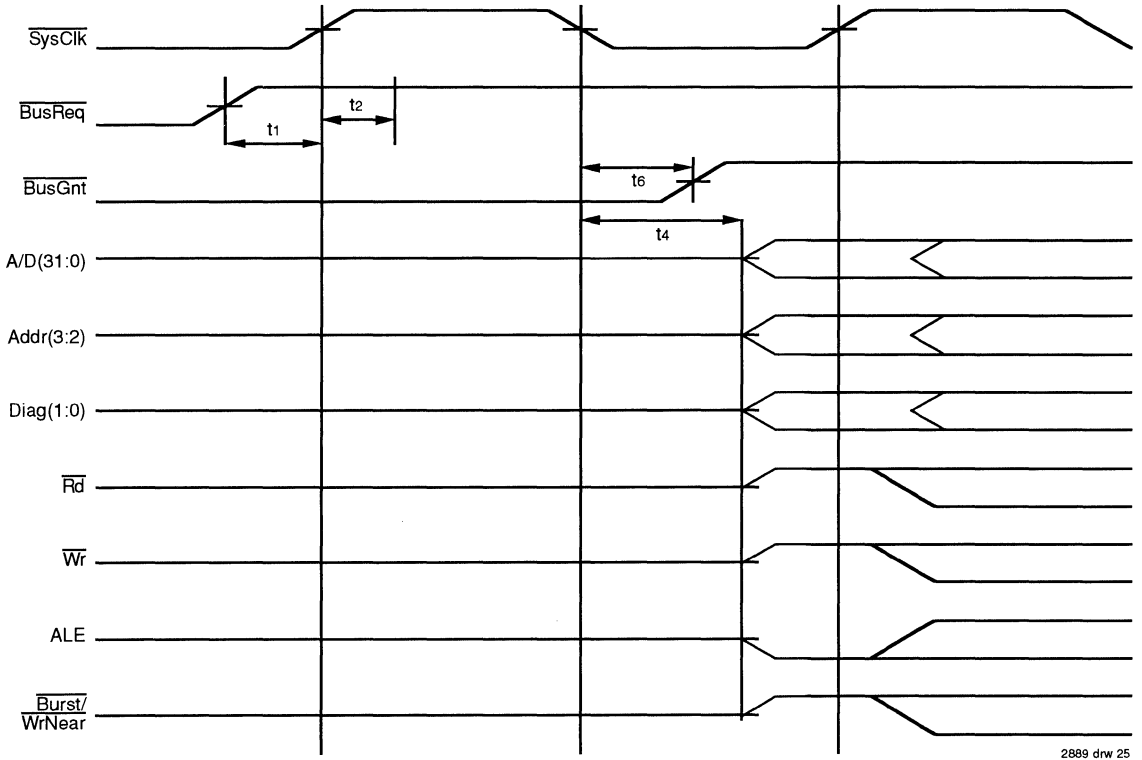
Figure 15. R3081 Write Cycle

2889 drw 23



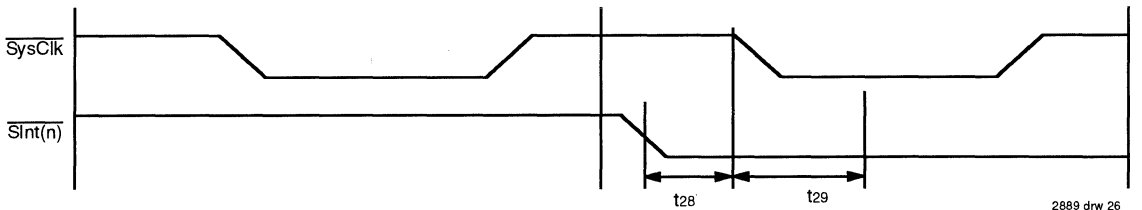
Figure 16. Request and Relinquish of R3081 Bus to External Master

2889 drw 24



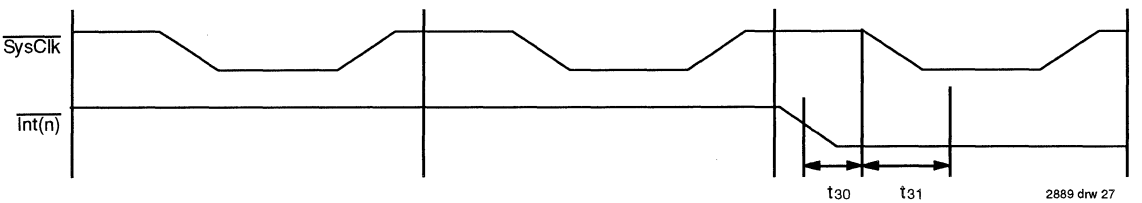
2889 drw 25

Figure 17. R3081 Regaining Bus Mastership



2889 drw 26

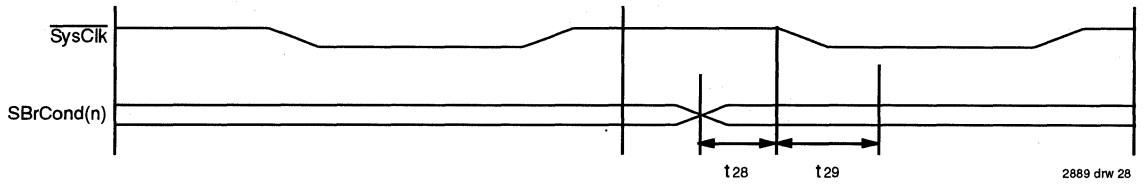
Figure 18. Synchronized Interrupt Input Timing



2889 drw 27

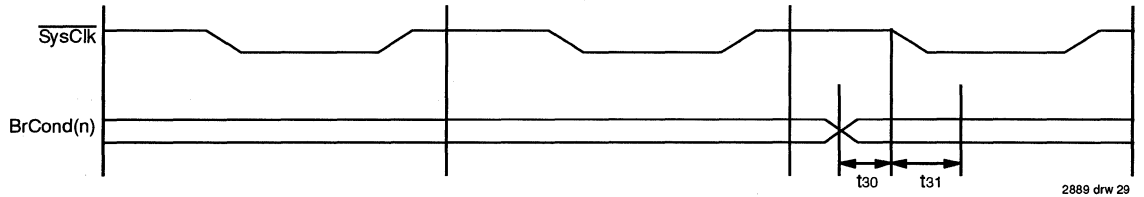
Figure 19. Direct Interrupt Input Timing

5



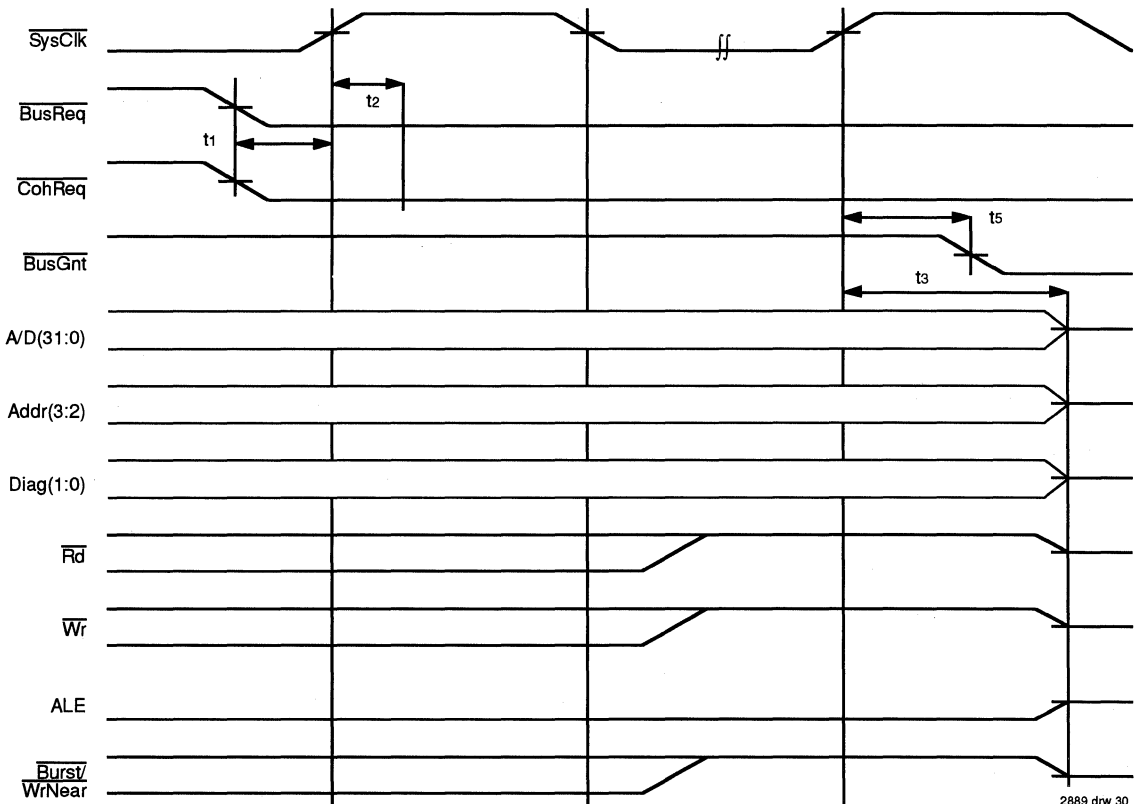
2889 drw 28

Figure 20. Synchronized Branch Condition Input Timing



2889 drw 29

Figure 21. Direct Branch Condition Input Timing



2889 drw 30

Figure 22. Coherent DMA Request

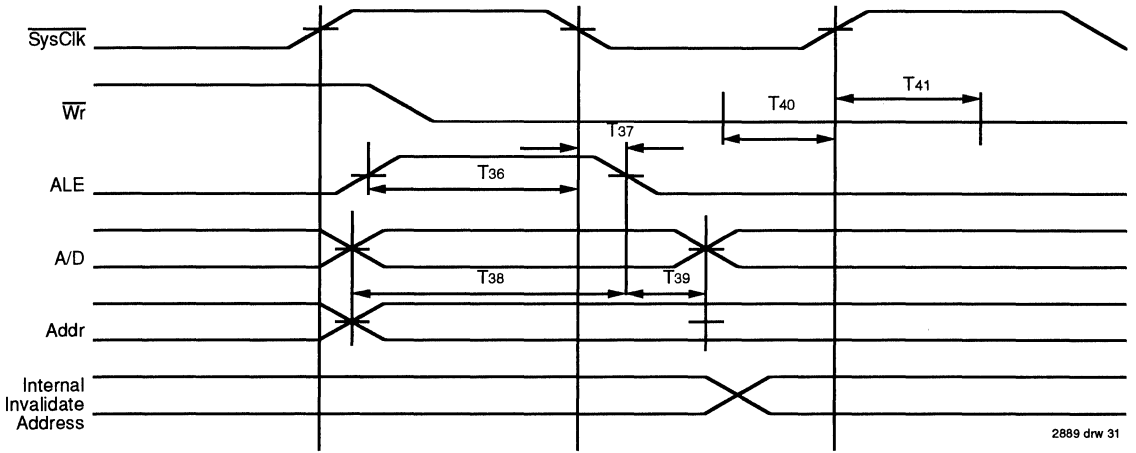


Figure 23. Beginning of Coherent DMA Write

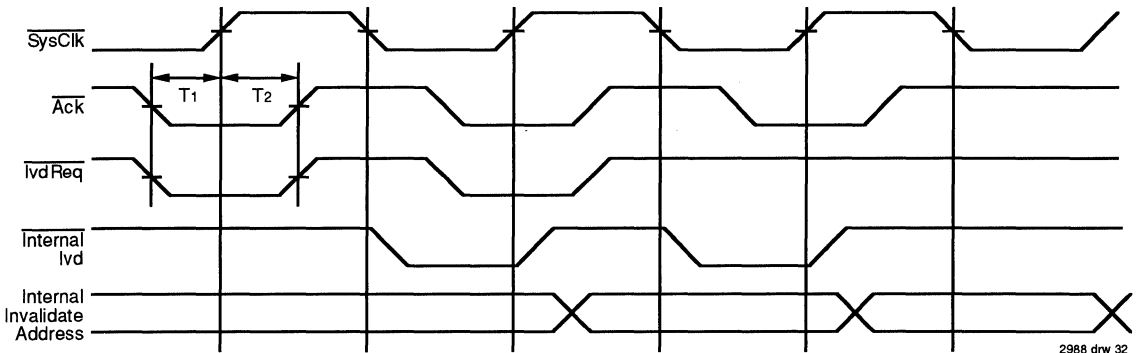


Figure 24. Cache Word Invalidation

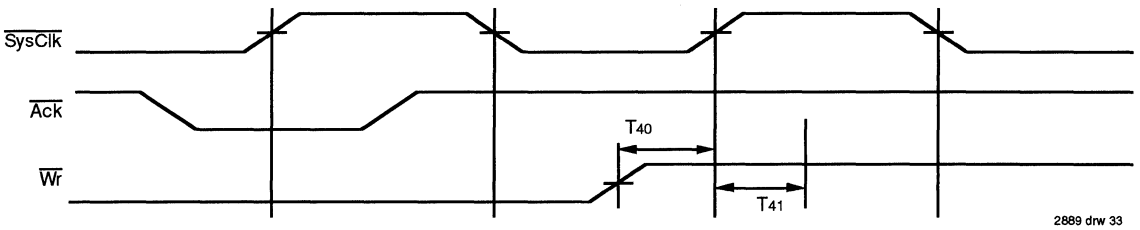


Figure 25. End of Coherent Write

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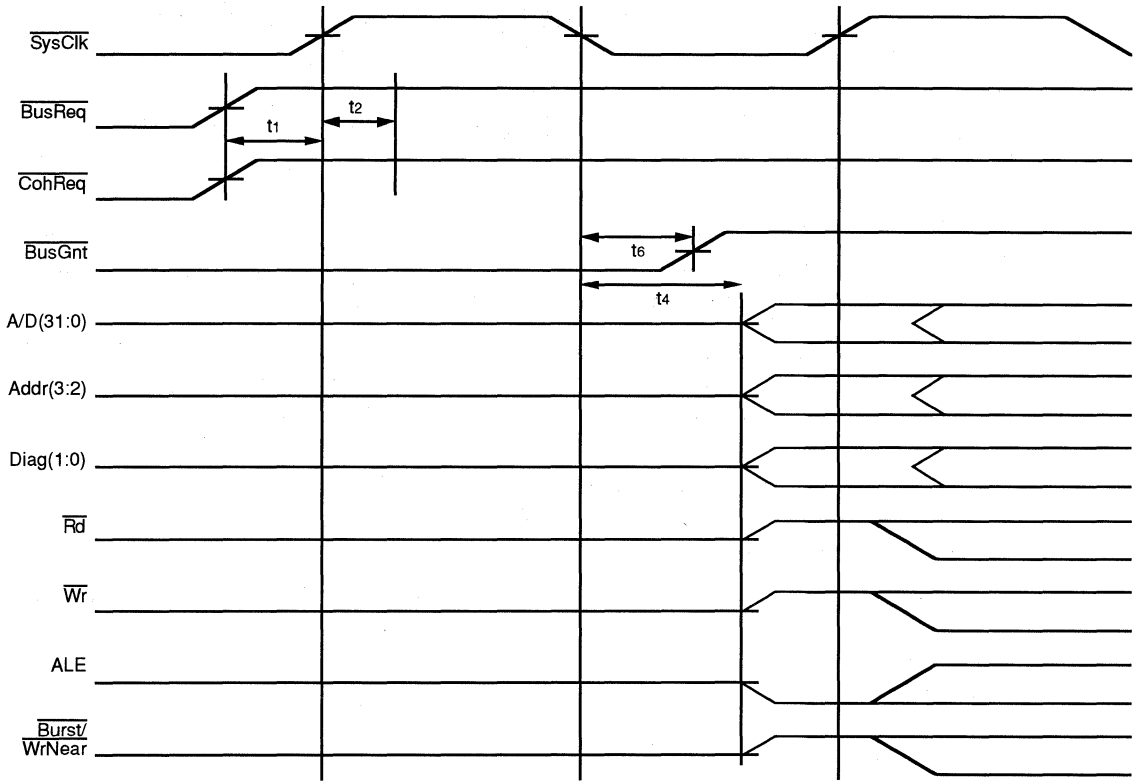
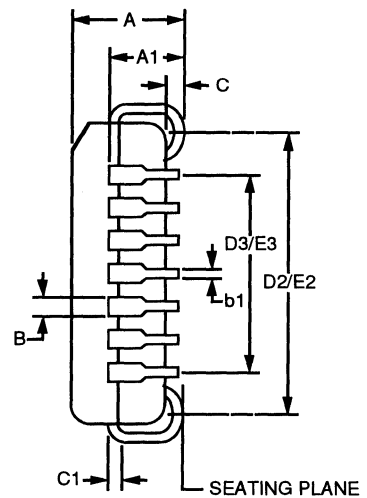
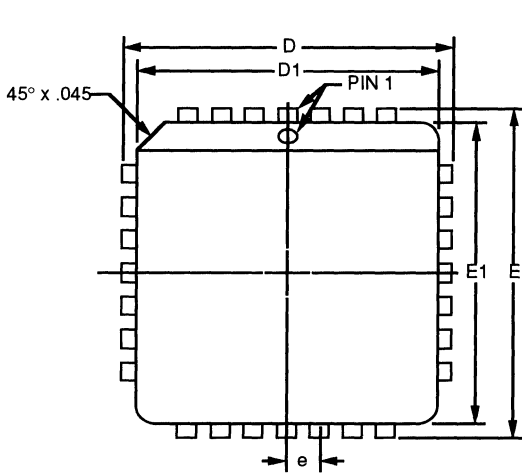


Figure 26. End of Coherent DMA Request

2889 drw 34

84 LEAD PLCC/MQUAD<sup>(7)</sup> (SQUARE)



2874 drw 27

NOTES:

1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protrusions.
4. Formed leads shall be planar with respect to one another and within .004 inches at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. MQUAD is pin & form compatible with PLCC.

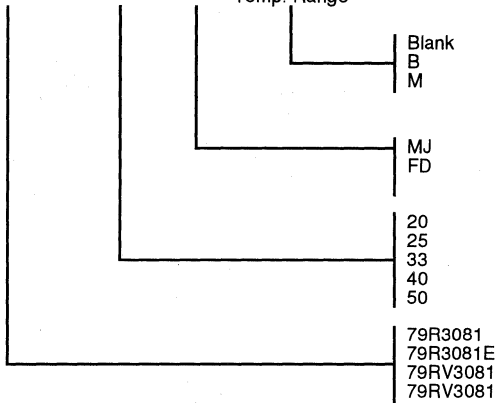
DWG #	J84-1		MJ84-1	
# of Leads	84		84	
Symbol	Min.	Max.	Min.	Max.
A	165	.180	165	.180
A1	.095	.115	.094	.114
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	1.185	1.195	1.185	1.195
D1	1.150	1.156	1.140	1.150
D2/E2	1.090	1.130	1.090	1.130
D3/E3	1.000 REF		1.000 REF	
E	1.185	1.195	1.185	1.195
E1	1.150	1.156	1.140	1.150
e	.050 BSC		.050 BSC	
ND/NE	21		21	

5



**ORDERING INFORMATION**

IDT XXXXX - XX X X  
 Device Type Speed Package Process/  
 Temp. Range



Commercial Temperature Range  
 Compliant to MIL-STD-883, Class B  
 Military Temperature Range Only

84-Pin MQUAD  
 84-lead Cavity-down Flatpack with  
 Integral Thermal Slug

20.0MHz  
 25.0MHz  
 33.33MHz  
 40.0MHz } 5V Only  
 50.0MHz

No TLB; Vcc = 5V  
 With TLB; Vcc = 5V  
 No TLB; Vcc = 3.3V  
 With TLB; Vcc = 3.3V

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**VALID COMBINATIONS**

IDT 79R3081 – 20, 25, 33, 40, 50  
 79R3081E – 20, 25, 33, 40, 50  
 79RV3081 – 20, 25, 33  
 79RV3081E – 20, 25, 33

MJ Package  
 MJ Package  
 MJ Package  
 MJ Package

79R3081M, B – 20, 25, 33  
 79R3081EM, B – 20, 25, 33

FD Package Only  
 FD Package Only



Integrated Device Technology, Inc.

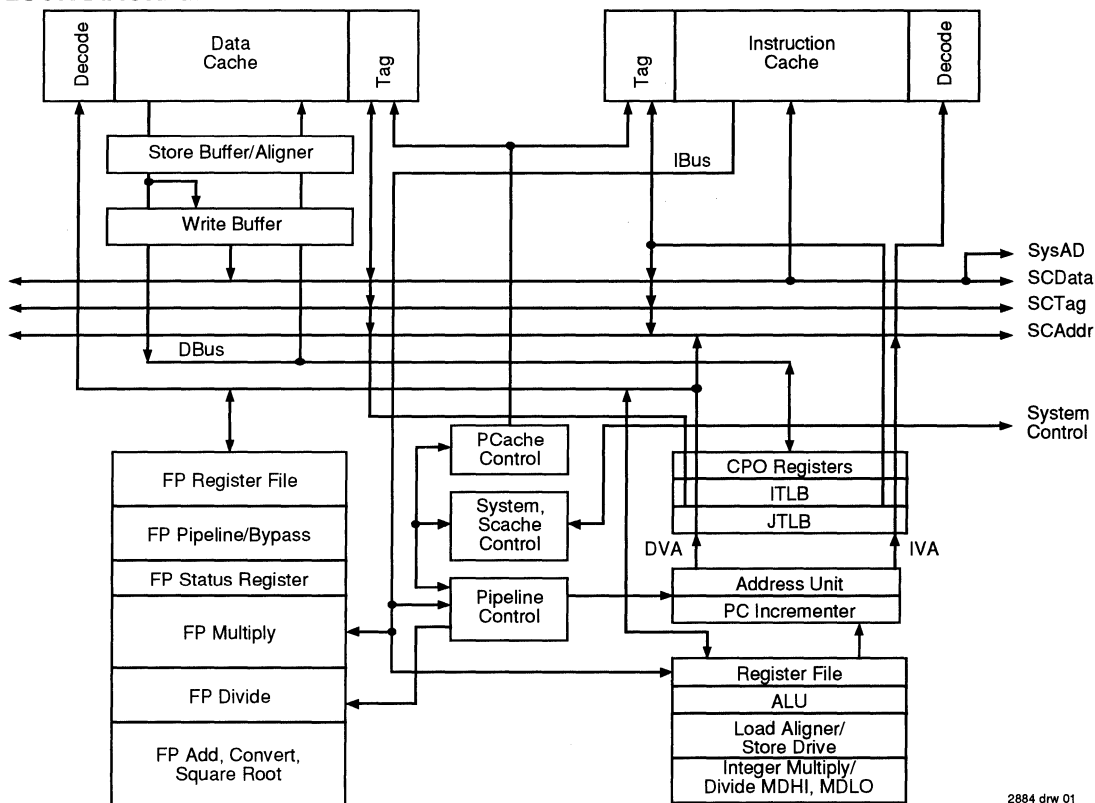
# THIRD GENERATION 64-BIT SUPER-PIPELINED RISC MICROPROCESSOR

IDT79R4400™  
IDT79RV4400

## FEATURES:

- True 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit floating-point operations
  - 64-bit registers
  - 64-bit virtual address space
- High-performance microprocessor
  - Super-pipelined architecture supports 150MIPS at 75MHz
  - No issue restrictions for dual instruction issue
  - Over 80 VUPs performance at 75MHz clock frequency
- High level of integration
  - 64-bit integer CPU
  - 64-bit floating-point accelerator
- 16KB instruction; 16KB data cache
- Flexible MMU with large TLB
- Standard operating system support includes:
  - Microsoft Windows™ NT
  - UNISOFT UNIX™ System V.4
- Fully software compatible with R3000A 32-bit RISC Processor Family
- 50, 67 and 75MHz clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - Desktop workstations
  - Deskside or departmental servers
  - High-performance embedded applications
  - Tightly coupled multi-processing systems
  - Fault tolerant systems
- R4400 for 5V operation and RV4400 for 3.3V operation

## BLOCK DIAGRAM



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COMMERCIAL TEMPERATURE RANGE

MARCH 1994

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## DESCRIPTION:

The IDT79R4400 family supports a wide variety of processor-based applications, from 32-bit ARC compliant desktop systems through high-performance, 64-bit OLTP systems manipulating large data bases in a multi-processor-based system. The IDT79R4400 products offer a broad range of price-performance options for high-performance systems, allowing the system architect unprecedented degrees of freedom in making price-performance tradeoffs.

The IDT R4400 products provide complete upward application-software compatibility with the IDT79R3000 family of microprocessors, including the IDT79R3000A and the IDT RISController™ family (IDT79R3051™ family). Microsoft Windows NT and UNISOFT UNIX V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4400-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The R4400 family achieves a unique balance between high-integer and high-floating-point performance. The key to this balance is the super-pipelined architecture of the processor, which brings performance gains to both integer and floating-point intensive programs without requiring recompilation to take advantage of the architectural advancement. The high-performance execution engine is assured of a rapid and continual supply of instructions and data through the use of large on-chip caches, and a high-performance on-chip TLB. The result is consistently high-performance; over 80 VUPS at 75MHz over a wide variety of realistic applications programs.

The R4400 family also provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4400 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit operating systems and applications.

The 64-bit computing and addressing capability of the R4400 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the IDT79R4400 CPU family. A more detailed description of the processor is available in the *"R4400 Hardware User's Manual"*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

## IDT79R4400 FAMILY MEMBERS

The IDT79R4400 processor is available in three different configurations: the IDT79R4400MC and IDT79R4400SC, which include a 128-bit wide secondary cache bus; and the IDT79R4400PC, with no secondary cache interface. All references to R4400 apply to R4400 (5V) and RV4400 (3.3V) operation.

### PC CONFIGURATION

The IDT79R4400PC is available in a 179-pin Pin Grid Array (PGA). This configuration does not support secondary cache or cache coherency, and is ideal for applications such as high-performance embedded control and low-cost desktop systems, where the on-chip caches provide enough performance and where cost, power, and board space must be kept to a minimum. By eliminating a secondary cache, a system can be designed with fewer parts and lower power consumption.

### SC CONFIGURATION

The 79R4400SC is available in a 447-pin Pin Grid Array (PGA). This processor supports a secondary cache interface and is ideal in systems where high performance is desired. This component supports a 128kB to 4mB secondary cache made from standard SRAMs. This flexibility allows system designers to make price/performance tradeoffs in cache subsystem designs.

### MC CONFIGURATION

The IDT79R4400MC is also available in the 447-pin Pin Grid Array (PGA). This processor supports a secondary cache and configurable multiprocessor cache coherency protocols. Like the "SC" configuration, this processor also supports a 128kB to 4mB secondary cache made from standard SRAMs. The IDT79R4400MC is well suited for a range of designs from high performance desktop systems to fault tolerant multiprocessor servers.

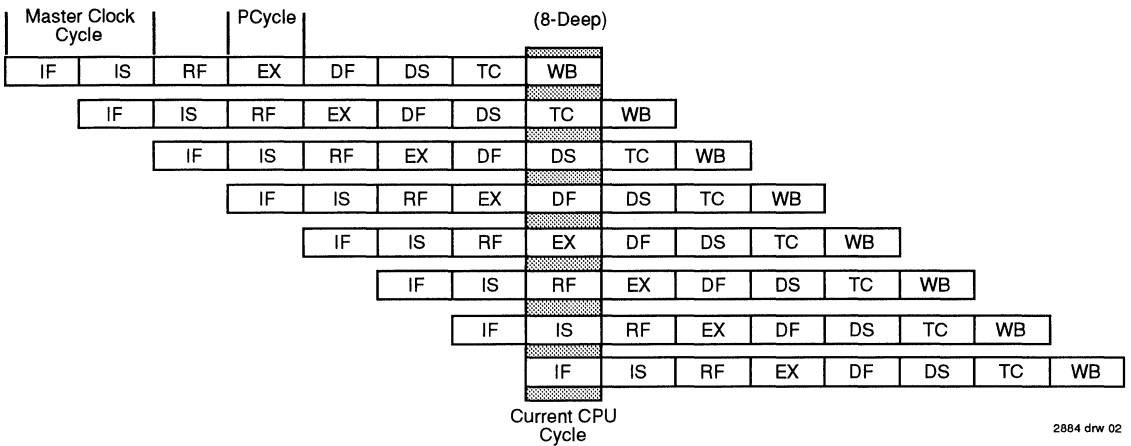


Figure 1. R4400 8-Stage Super-Pipeline

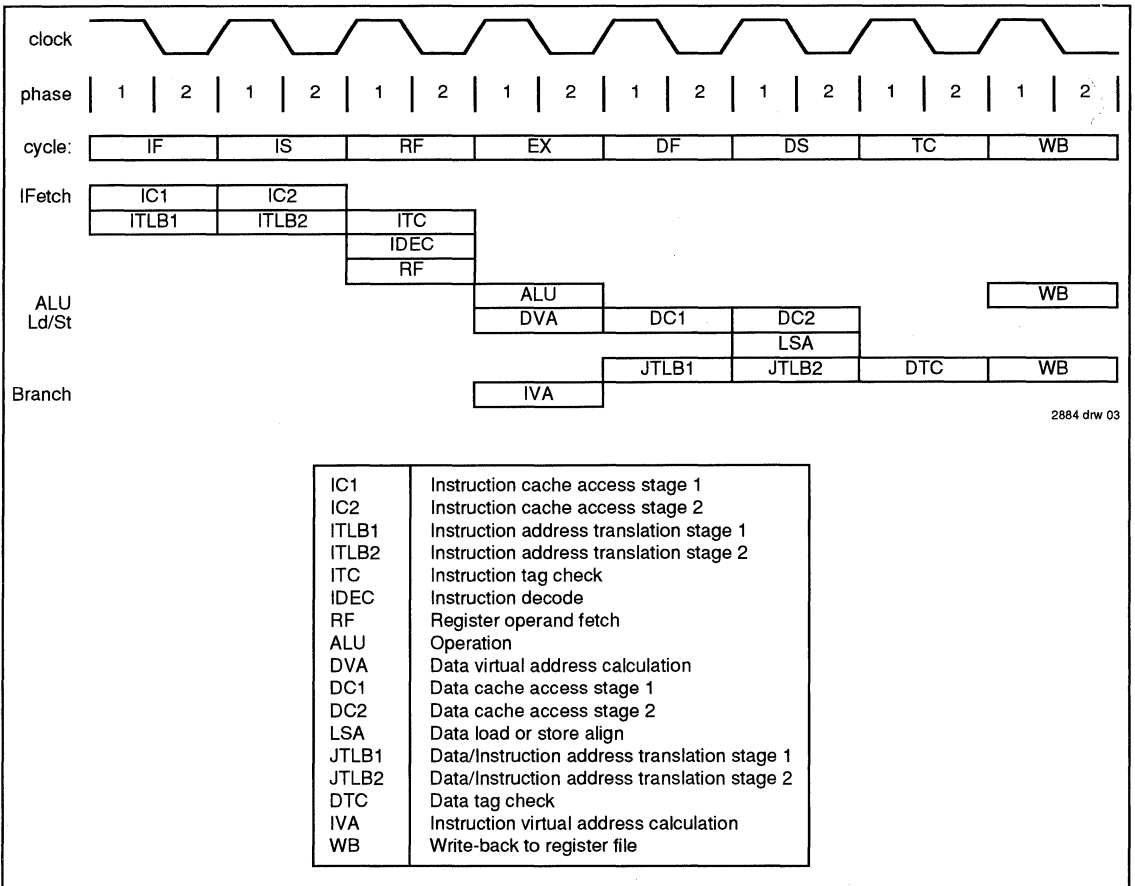


Figure 2. Pipeline Activities

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## HARDWARE OVERVIEW

The IDT R4400 processor brings a high-level of integration designed for high-performance computing. The key elements of the IDT R4400 are briefly described below. A more detailed description of each of these subsystems is available in other literature.

### Superpipelined Implementation

In order to achieve the high-performance desired for today's applications and user's interfaces, the R4400 exploits instruction level parallelism using a superpipelined micro-architecture.

The R4400 uses an 8-stage superpipeline which places no issue restrictions on instruction issue. Thus, any two instructions can be issued each master clock cycle under normal circumstances, leading to 150MIPS performance at 75MHz. One key advantage of this architecture is that all existing applications can gain from the architectural advancement represented by the R4400, without requiring recompilation to reorder the software.

In order to support dual instruction issue, the internal pipeline of the R4400 operates at twice the external clock frequency. Instruction execution stages such as cache accesses are pipelined (thus the chip itself is super-pipelined) to eliminate bottlenecks associated with long-latency functional units. Other stages, such as the ALU stage, completely process one operation per pipeline clock cycle, allowing the results of one operation to be immediately used by the instruction which follows, with no pipeline interlocks.

High clock frequency results from careful construction of the various resources of the processor: pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline stages.

After extensive simulation of many methods of exploiting instruction level parallelism, superpipelining was chosen because it improves integer performance commensurate with floating-point performance. Thus, the R4400 provides performance benefits both to technical computing applications, and also to a wide variety of commercial applications as well. In

today's technology, superpipelining results in less complex logic, faster cycle times, quicker design cycles, and lower cost. The pipeline of the IDT79R4400 is illustrated in Figure 1.

## THE R4400 PIPELINE

The R4400 processor has an eight-stage execution pipeline. That is, each instruction takes eight Pclock (Pipeline clocks, at twice the frequency of the input clock) cycles to execute, but a new instruction is started on each Pclock cycle. Another way of viewing the process is that, at any point in time, eight separate instructions are being executed at once. Figure 1 shows the R4400 pipeline in both views: a horizontal slice shows the execution process of individual instructions, and a vertical slice shows the processing of eight instructions at once.

Each box shown in Figure 1 corresponds to a part of the execution process.

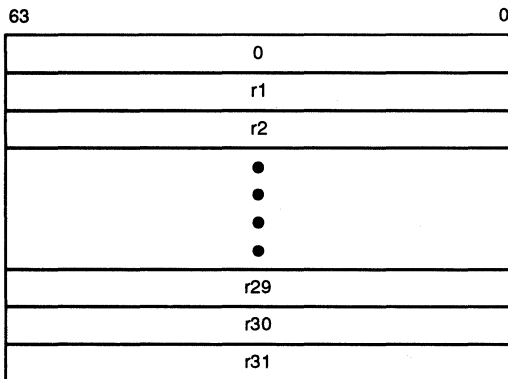
Figure 2 illustrates the activities occurring within each pipelined stage as a function of the instruction type. First, in the IF stage, an instruction address is selected by the program counter logic and the first half of both the instruction cache fetch (IC1) and the instruction virtual to physical address translation (ITLB1) is performed. The instruction address translation is done through a two entry subset of the main or joint translation lookaside buffer (JTLB) called the ITLB. In the IS stage, the second half of both the instruction cache fetch (IC2) and instruction translation (ITLB2) is done.

During the RF stage, three activities occur in parallel. The instruction decoder (IDEC) decodes the instruction and checks for interlock conditions. Meanwhile, the instruction tag check (ITC) is performed between the instruction cache tag and the page frame number (PFN) from the ITLB's translation. In parallel with both of the above, the operands are fetched from the register file (RF).

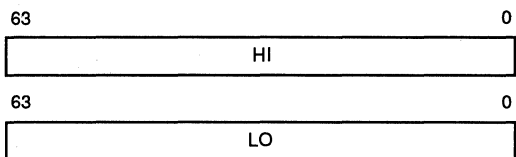
In the EX stage, if the instruction is a register-to-register operation, the arithmetic or logical operation is performed (ALU). If the instruction is a load/store, a data virtual address is calculated (DVA). If the instruction is a branch, a virtual branch target address is calculated (IVA).

For load/stores, the DF stage is used to do the first half of

### General Purpose Registers



### Multiply/Divide Registers



### Program Counter

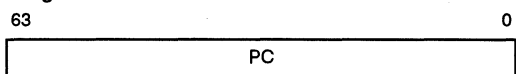


Figure 3. CPU Registers

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both the data cache fetch (DC1) and the data virtual to physical address translation (JTLB1). Similarly, the DS stage does the second half of both the data fetch (DC2) and the data translation (JTLB2) as well as the load align or store align (LSA), as appropriate. If the instruction is a branch, the JTLB is used during DF and DS to translate the branch address and refill the ITLB if necessary.

The TC stage is used to perform the tag check for load/stores. During the WB stage the instruction result is written to the register file.

Smooth pipeline flow is interrupted when cache accesses miss, data dependencies are detected, or when exceptions occur. Interruptions that are handled by hardware, such as cache misses, are referred to as *interlocks*, while those that are handled using software are *exceptions*. Collectively, the cases of all interlock and exception conditions are referred to as *faults*.

Interlocks come in two varieties. Those interlocks which are resolved by simply stopping the pipeline are referred to as *stalls*, while those which require part of the pipeline to advance while holding up another part are *slips*.

At each cycle, exception and interlock conditions are checked for all active instructions. The conditions can be referred back to particular instructions, as each exception or interlock condition corresponds to a particular pipeline stage.

When an exception condition occurs, the relevant instruction and all that follow it in the pipeline are cancelled. Accordingly, any stall conditions and any later exception conditions

that are referenced to the same instruction are inhibited; there is no value in servicing stalls for a cancelled instruction. A new instruction stream is begun, starting execution at a predefined exception vector. System control coprocessor registers are loaded with information that will identify the type of exception and any necessary auxiliary information, such as the virtual address at which translation exceptions occur.

When a stall condition is detected, all eight instructions, each in a different stage of the pipeline, are frozen at once. Often, the stall condition is only detected after parts of the pipeline have advanced using incorrect data; this occurrence is referred to as *pipeline overrun*. When in the stalled state, parts of the pipeline that are immune to overrun are frozen and the remainder is permitted to continue clocking. Just before resuming execution, the pipeline overrun is reversed by inserting corrected information into the pipeline.

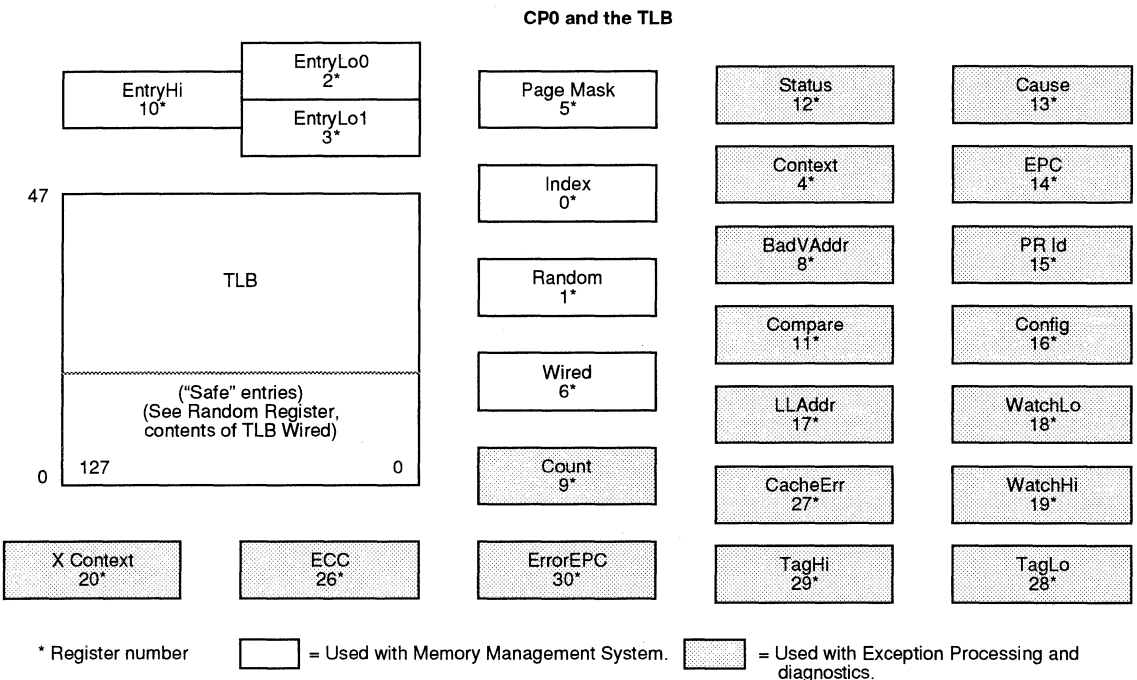
When a slip condition is detected, the pipeline stages which must advance in order to resolve the dependency continue to be retired while the dependent stages are held until the necessary data is available.

Another class of interlocks exists which, since they originate external to the processor, are not referenced to a particular pipeline stage. These interlocks are referred to as *external stalls* and are unaffected by the occurrence of exceptions.

### Integer Execution Engine

The R4400 implements the extended MIPS Instruction Set

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Figure 4. The R4400 CP0 Registers

architecture, and thus is fully upwards compatible with applications running on the earlier generation parts. The R4400 includes additions to the instruction set, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, as well as faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability amongst implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4400 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The programmer model for the R4400 includes the register set illustrated in Figure 3. The register resources include: 32 general purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

**System Control Co-processor (CP0)**

The system control co-processor in the MIPS architecture is responsible for the virtual memory subsystem, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4400 CP0 is a superset extension of the MMU found in the R3000A.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction translation buffer (the ITLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

**System Control Co-Processor Registers**

The R4400 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined, changed (the operating modes, kernel vs. user mode, interrupts enabled or disabled, cache features) and controlled. Also, these registers control exception handling. In addition, the R4400 includes registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

Figure 4 illustrates the System Control Co-Processor registers.

**Virtual to Physical Address Mapping**

The R4400 provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4400 provides a single, uniform virtual address space of 2GB.

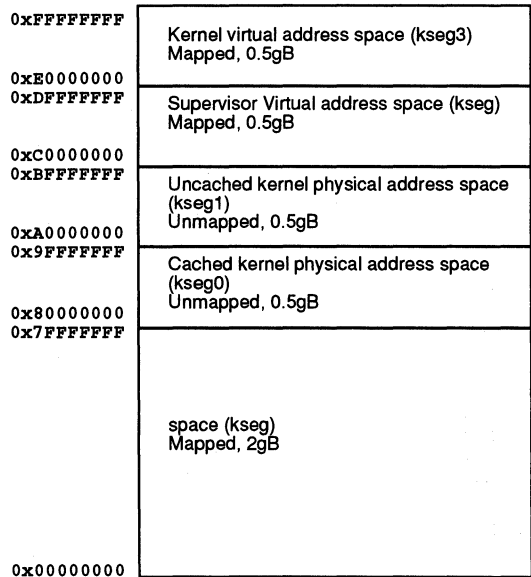
When operating in the kernel mode, four distinct virtual address spaces, totalling 4GB, are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4400 processor also support a supervisor mode in which the virtual address space is 2.5GB, divided into two regions based on the high-order bits of the virtual address. The three different modes of virtual addressing are shown in Figure 5. When the R4400 is configured as a 64-bit microprocessor, the virtual address space layout is a compatible extension of the 32-bit virtual address space layout.

**Joint TLB**

For fast virtual-to-physical address decoding, the R4400 uses a large, fully associative TLB which maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteris-



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**Figure 5. Kernel Mode Virtual Addressing (32-bit mode)**

tics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can treat various regions of memory distinctly from applications programs and data files. For example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4400 uses a Random Replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing

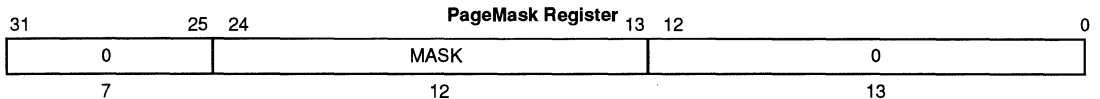
deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, noncoherent, sharable, exclusive, or update. The use of these attributes, coupled with state information in the processor caches, enables a wide variety of multiprocessing strategies to be easily implemented.

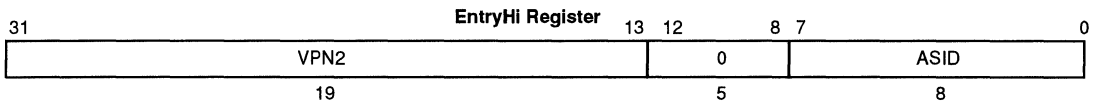
Figure 6 shows the format of the TLB entry and registers used to control the TLB.

**Instruction TLB**

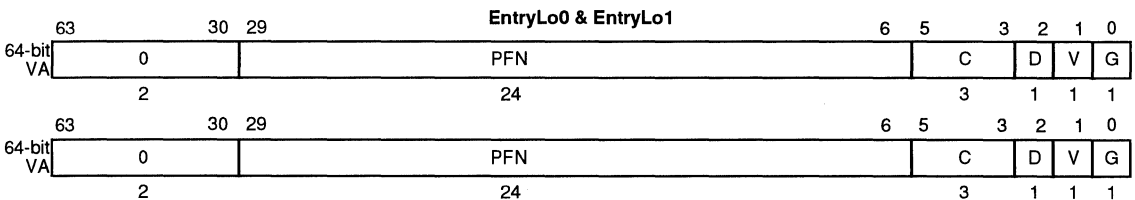
The R4400 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to



*MASK* = Page comparison mask  
 0 = Reserved. Must be written as zero; returns zero when read.



*VPN2* = Virtual Page Number divided by two (maps to two pages)  
*ASID* = Address Space ID field. An 8-bit field which lets multiple processes share the TLB while each process has a distinct mapping of otherwise identical virtual page numbers. This is the same ASID described at the beginning of this chapter.  
 0 = Reserved. Must be written as zero; returns zero when read.



*PFN* = Page Frame Number. Upper bits of the physical address.  
*C* = Specifies the cache algorithm to be used.  
*D* = Dirty. If this bit is set, the page is marked as dirty and, therefore, writable. This bit is actually a write-protect bit that software can use to prevent alteration of data.  
*V* = Valid. If this bit is set, it indicates that the TLB entry is valid; otherwise, a TLBL or TLBS Miss occurs.  
*G* = Global. If this bit is set in both Lo0 and Lo1, then ignore the ASID.  
 0 = Reserved. Must be written as zero; returns zero when read.

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Figure 6. Fields of an R4400 TLB Entry



occur in parallel with data address translation. When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

### Register File

The R4400 has thirty-two general purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same register twice per cycle as well as to minimize the operation latency in the pipeline.

### ALU

The R4400 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle.

### Integer Multiplier/Divider

The R4400 integer multiplier and divider units perform signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the *MDHI* and *MDLO* registers. The values can then be transferred to the general purpose register file using the *MFHI*/*MFLO* instructions. The following table shows the number of processor internal cycles required between a 32-bit integer multiply or divide and a subsequent *MFHI* or *MFLO* operation, in order that no interlock or stall occurs.

Operation	Single Word	Double Word
MULT	10	20
DIV	69	133

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### FLOATING-POINT UNIT

The R4400 incorporates an entire floating-point unit on chip, including a floating-point register file and execution unit. The floating-point unit forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

### Floating-point Co-Processor

The R4400 floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allow for overlapped operations. The multiplier is pipelined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R3010, the R4400 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely im-

portant in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with the IEEE Standard 754.

The following table gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	7	8
DIV	23	36
SQRT	54	112
CMP	3	3
FIX	4	4
ROUND	4	4
TRUNC	4	4
FLOAT	5	5
ABS	2	2
MOV	1	1
NEG	2	2
LWC1,LDC1	3	3
SWC1,SDC1	1	1

### Floating-Point General Register File

The floating-point register file is made up of sixteen <sup>2884 tbi 02</sup>64-bit registers which can also be viewed as thirty-two 32-bit floating-point registers. The MIPS architecture supports a coprocessor load and store double so, when configured as 64-bit registers, the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store a doubleword instruction in every cycle.

### Floating-Point Control Register File

The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

### CACHE MEMORY

In order to keep the high-performance superpipeline full and operating efficiently, the R4400 incorporates on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice a cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined, single

master clock cycle access of each cache, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2GB per second at a system clock frequency of 75MHz.

**Instruction Cache**

The IDT79R4400 incorporates a direct-mapped on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with byte parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed twice per master clock cycle, although the current IDT79R4400 CPU fetches on 32-bit unit/master cycle for a peak instruction bandwidth of 400MB/sec. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

**Data Cache**

For fast, single cycle data access, the IDT79R4400 includes an 16KB on-chip data cache.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The Data Cache is direct mapped, and its line size can be configured as four or eight words. The write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation.

Associated with the Data Cache is the store buffer. When the R4400 executes a store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the Data Cache in the next cycle that the Data Cache is not

accessed. The store buffer allows the R4400 to execute two stores per master cycle and to perform back-to-back stores without penalty. Likewise, the R4400 can perform two loads or a load and store per master cycle without penalty, yielding 1.2GB/sec bandwidth without restrictions on instruction combinations.

When the Data Cache line does need to be written back to slower memory (either secondary cache or main memory), the processor writes the data to an internal write buffer which can hold a line (4 or 8 words) of data. By writing the data to the fast write buffer, the processor can continue executing instructions without having to wait until the write completes to the slower memory.

The IDT79R4400 caches are designed for easy and flexible integration in many types of multiprocessor systems. The Data Cache contains all the necessary state bits to allow the R4400 to maintain cache coherency across all R4400 processors in a system.

**SECONDARY CACHE INTERFACE**

The R4400SC and R4400MC support a secondary cache that can range in size from 128KBs to 4MBs. The cache can be configured as a unified cache or split into an instruction cache and a data cache, and it can be designed using industry standard SRAMs. The IDT R4400 provides all of the secondary cache control circuitry on chip, including ECC.

The secondary cache interface consists of a 128-bit data bus, a 25-bit tag bus, and 18-bit address bus, and SRAM control signals. The wide data bus improves performance by providing a high bandwidth data path to fill the primary caches. ECC check bits are added to both the data and tag buses to improve data integrity. All double-bit errors can be detected and all single bit-errors can be detected and all single bit-errors can be corrected on both buses.

The secondary cache access time is configurable, providing system designers with the flexibility to tailor the cache design to specific applications. The line size of the secondary cache is also configurable and can be 4-, 8-, 16-, or 32-words. The line size of the primary cache must always be less than or equal to the line size of the secondary cache.

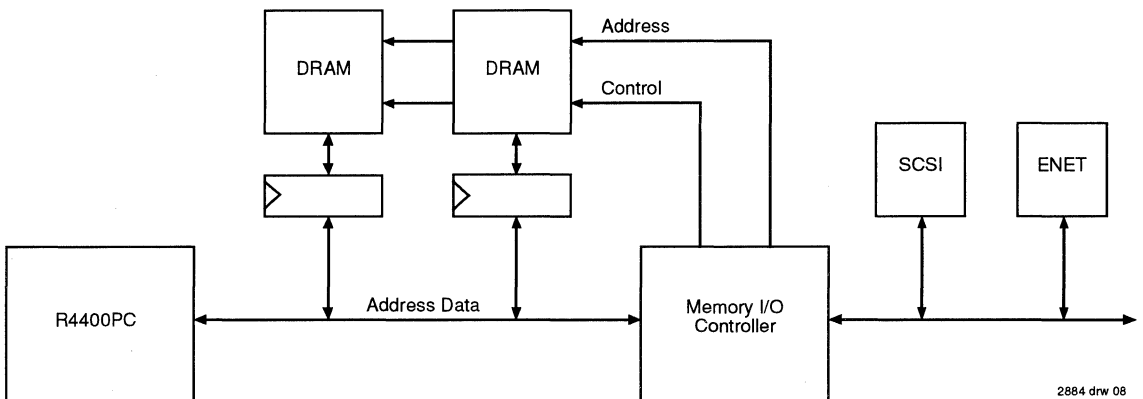


Figure 7. Typical Desktop System Block Diagram

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The secondary cache is physically tagged and physically indexed. The physical cache prevents problems that could arise due to virtual address aliasing. Also, a physical cache makes multiprocessing cache coherency protocols easier to implement. The R4400MC provides a set of cache states and a mechanism for manipulating the contents and state of the cache, which are sufficient to implement a variety of cache coherency protocols, using either bus snooping or directory based schemes.

**SYSTEM INTERFACE**

The R4400 supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sophisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 75MHz.

Figure 7 shows a typical desktop system using the R4400PC. Similarly, a high-performance desktop workstation/server system can be built using the IDT79R4400SC and adding a secondary cache.

The system interface allows the processor to access external resources in order to satisfy cache misses and uncached operations. The IDT79R4400MC, in addition to handling simple memory and I/O transactions, supports a number of cache coherency transactions of sufficient generality to support a variety of cache coherent multiprocessing models. In particular, the interface is designed to support both bus snooping and directory based multiprocessor models and supports both write-update and write-invalidate coherency protocols.

Figure 8 shows a typical multiprocessor system using the IDT79R4400MC, an interface agent, and a secondary cache.

**System Address/Data Bus**

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4400 and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4400 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no write buffering or a fast, high performance interface can be designed to communicate with the R4400. Again, the system designer has the flexibility to make these price/performance tradeoffs.

**System Command Bus**

The R4400 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this line of data is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4400. Processor requests are initiated by the R4400 and responded to by an external device. External requests are issued by an external device and require the R4400 to respond.

The R4400 supports byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

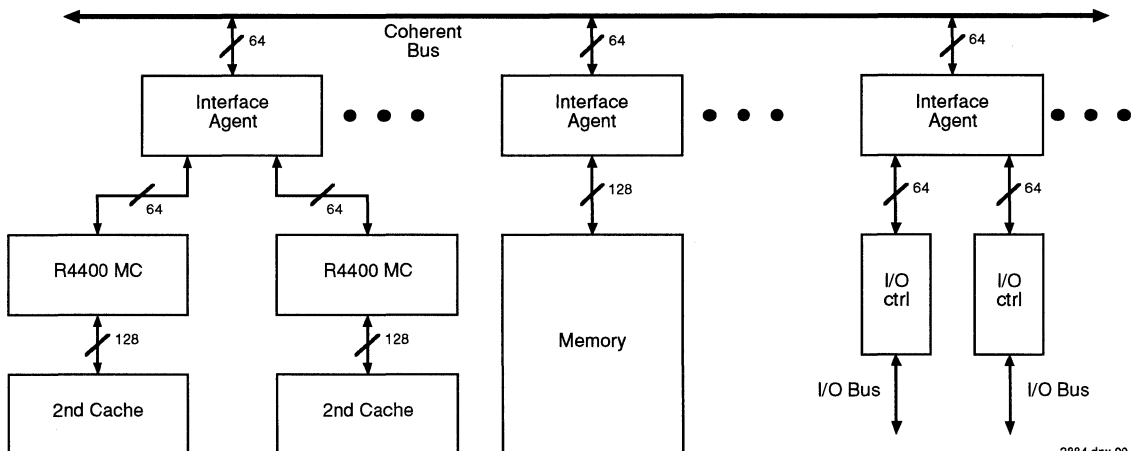


Figure 8. Multiprocessor System Using the R4400 MC

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**Handshake Signals**

There are eight handshake signals on the system interface. Two of these,  $\overline{\text{RdRdy}}$  and  $\overline{\text{WrRdy}}$  are used by an external device to indicate to the IDT79R4400 whether it can accept a new read or write transaction. The IDT79R4400 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$  and  $\overline{\text{Release}}$  are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts  $\overline{\text{ExtRqst}}$ . The IDT79R4400 responds by asserting  $\overline{\text{Release}}$  to release the system interface to slave state.

$\overline{\text{ValidOut}}$  and  $\overline{\text{ValidIn}}$  are used by the IDT79R4400 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4400 asserts  $\overline{\text{ValidOut}}$  when it is driving these buses with a valid command or data, and the external device drives  $\overline{\text{ValidIn}}$  when it has control of the buses and is driving a valid command or data.

Finally, there are two signals that are available on the MC version only and are used in multiprocessing systems. They are  $\overline{\text{IvdAck}}$  and  $\overline{\text{IvdErr}}$ , and they are driven by an external device to indicate the completion status of the current processor invalidate or update request.

**R4400 Requests**

The R4400 is capable of issuing requests to a memory and

I/O subsystem. The system interface supports two modes of operation:

- Secondary Cache mode
- No Secondary Cache mode

**No Secondary Cache Mode**

The R4400 without a secondary cache requires a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4400 issues another request. The R4400PC can issue read and write requests to an external device, and an external device can issue read and write requests to the R4400.

Figure 9 shows a processor read request. The R4400 asserts  $\overline{\text{ValidOut}}$  and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has  $\overline{\text{RdRdy}}$  asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting  $\overline{\text{Release}}$ . The external device can then begin sending the data to the IDT79R4400.

**Secondary Cache Mode**

The R4400 with a secondary cache operates in an overlapping bus transfer mode in which multiple system interface transactions may be issued in parallel. The processor may issue a combination of read request, an update or invalidate request, and a write request. For instance, when a dirty cache line needs to be replaced, the processor issues a read request

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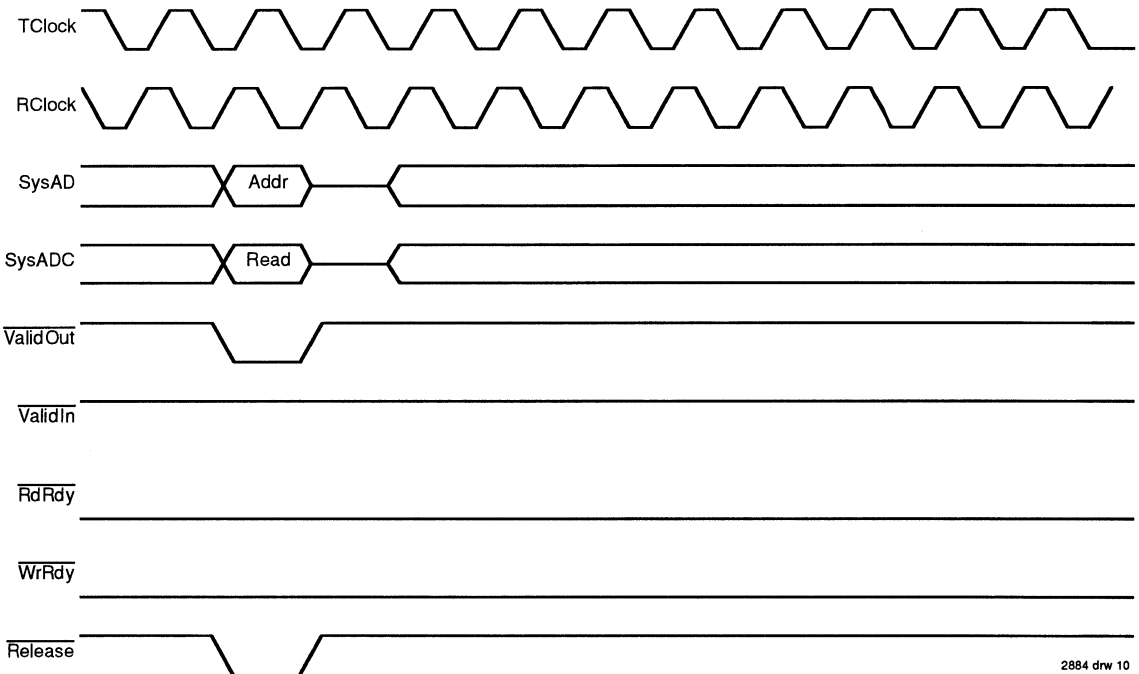


Figure 9. Processor Read Request

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immediately followed by a write request, without waiting for the read data to return. This has the advantage of "hiding" the write transaction between the read request and read response, thus increasing overall system performance. This mode of operation is not necessary or useful in R4400 systems without secondary cache since the processor contains a write buffer capable of accepting an entire primary cache line of data. Overlapping is a superset of non-overlapping system operation.

Figure 10 illustrates a processor request in overlap mode. This request is made up of a read, invalidate, and write request. Note that the protocol for the read, the invalidate, and the write are all similar to each other, with the exception that the processor also sends out valid data during the write request. In Figure 10 the processor write transaction not only occurs before the read response from the external device, but it also illustrates how an external device can hold off a write request through the deassertion of WrRdy.

**External Requests**

The R4400 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4400 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue cache coherency requests to the processor, such as a request for the R4400 to update, invalidate, or snoop upon its caches, or to supply a cache line of data. Additionally, an external device may need to write to the

R4400 interrupt register.

The following is a list of the supported external requests:

- Read
- Write
- Invalidate
- Update
- Snoop
- Intervention
- Null

Figure 11 shows an example of an external snoop request. The process by which the external device issues the request is very similar to the way the R4400 issues a request. The external device first gains ownership of the system interface by asserting ExtRqst and waiting for the R4400 to assert Release. The external device then sends in a valid command by asserting ValidIn and driving the SysCmd and SysAD buses with the snoop command and address. The R4400 responds to the request by asserting ValidOut and driving the SysCmd bus with the cache state of the snooped upon line.

**CACHE COHERENCY CAPABILITY**

With the IDT79R4400MC, cache coherence is maintained in hardware. The system control coprocessor permits the specification of different caching protocols on a per-page basis. A page may be:

- uncached
- cached but non-coherent
- cached and coherent exclusive (only one processor cache contains the data on loads and stores).

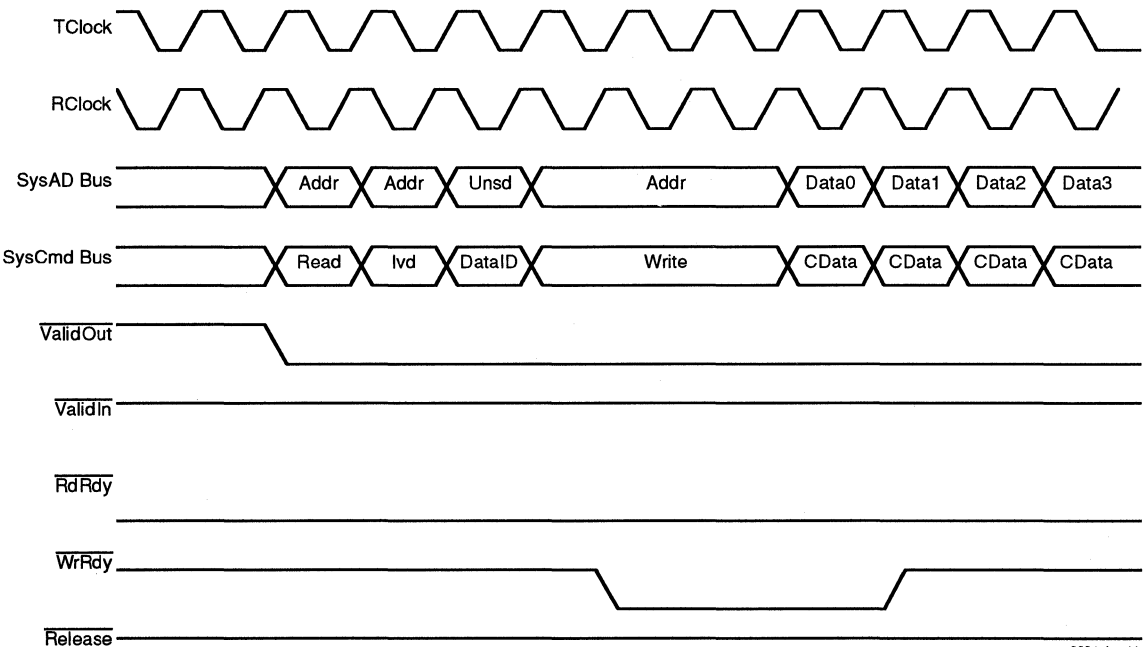


Figure 10. Processor Read, Invalidate, Write Request

- cached and coherent exclusive on writes (write invalidate scheme—only one processor cache contains the data when that datum is written to).
- cached and coherent with updates on writes (write-update scheme).

Depending upon the amount and type of data sharing in an application, the operating system can choose the most appropriate caching strategy.

Support for processor synchronization is provided by the Load Linked and Store Conditional instructions. The Load Linked and Store Conditional instructions:

1. Provide a simple mechanism for generating all of the common synchronization primitives including test-and-set, bit-level locks, semaphores, counters, sequencers, etc. with no additional hardware overhead.
2. Operate in such a fashion that bus traffic is only generated when the state of the cache line changes.
3. Need not lock a system bus—a very important feature for larger systems.

**ADVANCED FEATURES**

The R4400 supports a number of other capabilities in addition to the standard processor model described above. Many of these capabilities are selected by the system designer during the processor reset sequence, via the boot time mode control interface. Features are included to support fault tolerance, system test, or other system environments.

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (Master clock divided by 256). The low frequency operation allows the initialization information to be kept in a low cost EPROM.

Immediately after the VCCOk Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

**JTAG INTERFACE**

The JTAG boundary scan mechanism provides a capability for testing the interconnect between the IDT79R4400 processor, the printed circuit board to which it is attached, and the other components on the board. In addition the JTAG boundary scan mechanism provides a rudimentary capability for low-speed logical testing of the secondary cache RAMs. The JTAG boundary scan mechanism does not provide any capability for testing the R4400 processor itself.

In accordance with the JTAG specification the R4400 processor contains a TAP controller, JTAG instruction register, JTAG boundary scan register, JTAG identification register, and JTAG bypass register. However, the R4400 JTAG implementation provides only the *external test* functionality of the boundary scan register.



**Boot Time Options**

**FAULT TOLERANT SUPPORT**

The R4400 has been designed to support varying models

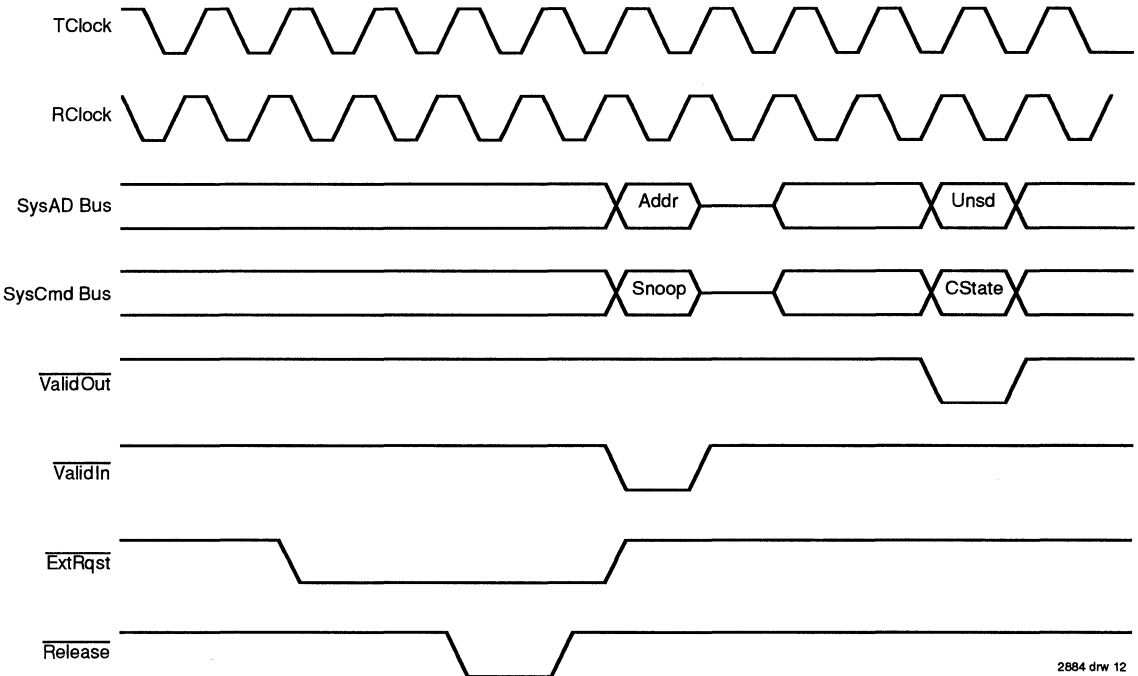


Figure 11. External Snoop Request

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## BOOT-TIME MODES

Serial Bit	Value	Mode Setting
0	0 1	<b>BlkOrder:</b> Block read response ordering. Sequential ordering. Sub-block ordering.
1	0 1	<b>EIBParMode:</b> System interface check bus checking. SECEDED error checking and correcting mode. Byte parity.
2	0 1	<b>EndBit:</b> Byte ordering. Little Endian. Big Endian.
3	0 1	<b>DShMdDis:</b> Dirty shared mode, enables transition to dirty shared state on processor update successful. Dirty Shared Enabled. Dirty Shared Disabled.
4	0 1	<b>NoSCMode:</b> Specifies presence of secondary cache. Present. Not Present.
5:6	0 1-3	<b>SysPort:</b> System Interface port width (Bit 6 Most Significant). 64 bits. Reserved <sup>(1)</sup>
7	0 1	<b>SC64BitMd:</b> Secondary cache interface port width. 128 bits. Reserved <sup>(1)</sup>
8	0 1	<b>EISpltMd:</b> Secondary cache organization Unified Reserved <sup>(1)</sup>
9:10	0 1 2 3	<b>SCBlkSz:</b> Secondary cache line size (Bit 10 Most Significant). 4 words. 8 words. 16 words. 32 words.
11:14	0 1 2 3 4 5 6 7 8 9-15	<b>XmitDatPat:</b> System Interface Data Rate (Bit 14 Most Significant). D DDx DDxx DxDx DDxxx DDxxxx DxxDxx DDxxxxx DxxxDxxx Reserved <sup>(1)</sup>
15:17	0 1 2 3-7	<b>SysCkRatio:</b> PClock to SClock divisor: frequency relationship between SClock, RClock, and TClock and PClock (Bit 17 Most Significant). Divide by 2 Divide by 3 Divide by 4 Reserved <sup>(1)</sup>
18	0	Reserved (Required value)
19	0 1	<b>TimIntDis:</b> Timer Interrupt enable allows timer interrupts, otherwise the interrupt used by the timer becomes a general-purpose interrupt. Enabled Disabled
20	0 1	<b>PotUpdDis:</b> Potential invalidate enable (allows potential invalidates to be issued. Otherwise only normal invalidates are issued). Enabled Disabled

Serial Bit	Value	Mode Setting
21:24	0-2 3-15	<b>TWrSup:</b> Secondary cache write deassertion delay, TWrSup in PCycles (Bit 24 Most Significant). Undefined Number of PCLK cycles (Min 3; Max 15)
25:26	0 1-3	<b>TWr2Dly:</b> Secondary cache write assertion delay 2, TWr2Dly in PCycles (Bit 26 Most Significant). Undefined Number of PCLK cycles (Min 1; Max 3)
27:28	0 1-3	<b>TWr1Dly:</b> Secondary cache write assertion delay 1, TWr1Dly in PCycles (Bit 28 Most Significant). Undefined Number of PCLK cycles (Min 1; Max 3)
29	0 1	<b>TWrRc:</b> Secondary cache write recovery time, TWrRc in PCycles either 0 or 1 cycles. 0 cycle 1 cycle
30:32	0 1	<b>TDIs:</b> Secondary cache disable time, TDIs in PCycles (Bit 32 Most Significant). Undefined Number of PCLK cycles (Min 2; Max 7)
33:36	0-2 3-15	<b>TRd2Cyc:</b> Secondary cache read cycle time 2, TRdCyc2 in PCycles (Bit 36 Most Significant). Undefined Number of PCLK cycles (Min 3; Max 15)
37:40	0-3 4-15	<b>TRd2Cyc:</b> Secondary cache read cycle time 1, TRdCyc1 in PCycles, (Bit 40 Most Significant). Undefined Number of PCLK cycles (Min 4; Max 15)
41:45 <sup>(2)</sup>	0	Reserved.
46	0 1	<b>Pkg179:</b> R4400 type. Large (447 pin). SC/MC Small (179). PC
47:49	0 1 2 3 4-7	<b>CycDivisor:</b> This mode determines the clock divisor for the reduced power mode. When the RP bit in the Status Register is set to one, the pipeline clock is divided by one of the following values (Bit 49 is Most Significant). Divide by 2 Divide by 4 Divide by 8 Divide by 16 Reserved <sup>(1)</sup>
50:52	0-1 2-3 4-7	<b>Drv0_50, Drv0_75, Drv1_00:</b> Drive the outputs in N x MasterClock period (Bit 52 Most Significant). Drive at 0.5 x MasterClock period. Drive at 0.75 x MasterClock period. Drive at 1.0 x MasterClock period.
53:56	0 1-14 15	<b>InitP:</b> Initial values for the state bits that determine the pull-down di/dt and switching speed of the output buffers (Bit 53 Most Significant). Fastest pull-down rate. Intermediate pull-down rate. Slowest pull-down rate.
57:60	0 1-14 15	<b>InitN:</b> Initial values for the state bits that determine the pull-up di/dt and switching speed of the output buffers (Bit 57 Most Significant). Slowest pull-up rate. Intermediate pull-up rates. Fastest pull-up rate.
61	0 1	<b>EnbIDPLLR:</b> Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers only during ColdReset. Disable di/dt control mechanism. Enable di/dt control mechanism.



Serial Bit	Value	Mode Setting
62	0 1	<b>EnbIDPLL:</b> Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers during ColdReset and during normal operation. Disable di/dt control mechanism. Enable di/dt control mechanism.
63	0 1	<b>DsbIDPLL:</b> Enables PLLs that match MasterIn and produce RClock, TClock, SClock and the internal clocks. Enable PLLs. Disable PLLs.
64	0 1	<b>SRTristate:</b> Controls when output-only pins are tristated Only when ColdReset is asserted. When Reset or ColdReset are asserted
65-255	0 <sup>(2)</sup>	Reserved (must be scanned in as zeros).

**NOTES:**

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1. Selecting a Reserved value results in undefined processor behavior.
2. 0's must be presented for these reserved values.

**PIN DESCRIPTION**

The following is a list of interface, interrupt and maintenance pins available on the different package configurations.

Pin Name	Type	Description
Secondary cache interface pins available <i>only</i> on the SC and MC configuration:		
SCAddr(17:1)	Output	Secondary cache address bus A 17-bit address bus for the secondary cache.
SCAddr0(W:Z)	Output	Secondary cache address lsb To minimize loading effect, there are 4 identical copies of this signal.
SCAPar(2:0)	Output	Secondary cache address parity bus A 3-bit bus that carries the parity of the SCAddr bus and the cache control lines $\overline{SCOE}$ , $\overline{SCWR}$ , $\overline{SCDCS}$ and $\overline{SCTCS}$ .
SCData(127:0)	Input/Output	Secondary cache data bus A 128-bit bus used to read or write cache data from/to the secondary cache.
SCDChk(15:0)	Input/Output	Secondary cache data ECC bus A 16-bit bus that carries two 8-bit ECC fields that covers the 128 bits of the SCData from/to the secondary cache. SCDChk(15:8) corresponds to SCData(127:64) and SCDChk(7:0) corresponds to SCData(63:0).
$\overline{SCDCS}$	Output	Secondary cache data chip select Chip select enable signal for the secondary cache Ram associated with SCData and SCDChk.
$\overline{SCOE}$	Output	Secondary cache output enable Output enable for the secondary cache RAM.
SCTag(24:0)	Input/Output	Secondary cache tag bus A 25-bit bus used to read or write cache tags from/to the secondary cache.
SCTChk(6:0)	Input/Output	Secondary cache tag ECC bus A 7-bit bus that carries an ECC field covering the SCTag from/to the secondary cache.
$\overline{SCTCS}$	Output	Secondary cache tag chip select Chip select enable signal for the secondary cache tag RAM associated with SCTag and SCTChk.
$\overline{SCWr}(W:Z)$	Output	Secondary Cache write enable Write enable for the secondary cache RAM.
System interface pins available on all parts:		
$\overline{ExtRqst}$	Input	External request Signals that the system interface needs to submit an external request.
$\overline{Release}$	Output	Release interface Signals that the processor is releasing the system interface to slave state

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**PIN DESCRIPTION (Cont.)**

Pin Name	Type	Description
$\overline{\text{RdRdy}}$	Input	Read Ready Signals that an external agent can now accept a processor read, invalidate, or update request in both secondary cache and no secondary cache mode or can accept a read followed by a write request in secondary cache mode.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System command/data identifier bus parity A single, even-parity bit for the SysCmd bus.
$\overline{\text{ValidIn}}$	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{\text{ValidOut}}$	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{\text{WrRdy}}$	Input	Write Ready Signals that an external agent can now accept a processor write request in both non-overlap and overlap mode.
System interface pins available only on the MC configuration.		
$\overline{\text{IvdAck}}$	Input	Invalidate acknowledge Signals successful completion of a processor invalidate or update request.
$\overline{\text{IvdErr}}$	Input	Invalidate error Signals unsuccessful completion of a processor invalidate or update request.
Interrupt pins available only on the PC configuration:		
$\overline{\text{Int}}(5:1)$	Input	Interrupt Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Interrupt pin available on all devices:		
$\overline{\text{Int}}(0)$	Input	Interrupt One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
Non-maskable interrupt pin available on all devices:		
$\overline{\text{NMI}}$	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Boot-time mode control interface pins available on all devices:		
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.
JTAG interface pins available on all devices:		
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.

## PIN DESCRIPTION (Cont.)

Pin Name	Type	Description
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.
Maintenance pins available on all devices:		
IOOut	Output	I/O output Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the R4000 to an external agent.
IOIn	Input	I/O input Output slew rate control feedback loop input (see IOOut).
MasterClock	Input	Master clock Master clock input at the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
VCCOk	Input	VCC is OK When asserted, this signal indicates to the R4000 that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the reading of the boot-time mode control serial stream.
$\overline{\text{ColdReset}}$	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of $\overline{\text{ColdReset}}$ . $\overline{\text{ColdReset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Reset}}$	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. $\overline{\text{Reset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Fault}}$	Output	Fault Mismatch output of boundary comparators.
VccP	Input	Quiet VCC for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet VSS for PLL Quiet Vss for the internal phase locked loop.
Maintenance pins available only on the SC and MC configurations:		
Status(7:0)	Status	Output An 8-bit bus that indicates the current operation status of the processor.

2884 tbl 07

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
Tc	Operating Temperature	0 to +85 (Case)	°C
TBIAS	Case Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

**RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Temperature	GND	Vcc
R4400 Com.	0°C to +85°C (Case)	0V	5.0 ±5%
RV4400 Com.	0°C to +85°C (Case)	0V	3.3 ±5%

2884 tbl 10

**NOTES:**

2884 tbl 09

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -3.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> +0.5 Volts.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**DC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE**(V<sub>CC</sub> = 5.0V ± 5%; T<sub>case</sub> = 0°C to +85°C)

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	I <sub>OH</sub> = -4mA	3.5	—	3.5	—	3.5	—	V
VOHC	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut) <sup>(3)</sup>	I <sub>OH</sub> = -4mA	4.0	—	4.0	—	4.0	—	V
VOL	Output LOW Voltage	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage		2.0	V <sub>CC</sub> + .5	2.0	V <sub>CC</sub> + .5	2.0	V <sub>CC</sub> + .5	V
VIL	Input LOW Voltage <sup>(1,2)</sup>		-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
VIHC	Input HIGH Voltage (MasterClock, SyncIn)		0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	V
VILC	Input LOW Voltage (MasterClock, SyncIn)		-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	V
C <sub>in</sub>	Input Capacitance		—	10	—	10	—	10	pF
C <sub>Out</sub>	Output Capacitance		—	10	—	10	—	10	pF
I <sub>Leak</sub>	Input Leakage		—	10	—	10	—	10	μA
I <sub>OLeak</sub>	Input/Output Leakage		—	20	—	20	—	20	μA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = 5V, T <sub>C</sub> = 25°C	—	2.8	—	3.2	—	3.6	A

2884 tbl 11

**NOTES:**

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 15ns.
- Except for MasterClock input.
- Applies to TClock, RClock, MasterOut, and ModeClock outputs.

**AC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE**

(Vcc=5.0V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters<sup>(2)</sup>

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCKHigh	MasterClock High	<sup>(3)</sup>	4	—	3	—	3	—	ns
TMCKLow	MasterClock Low	<sup>(3)</sup>	4	—	3	—	3	—	ns
	MasterClock Freq <sup>(1)</sup>		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCIJitter	Clock Jitter (on RClk, TClk, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

**NOTES:**

1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

2884 tbl 12

**SYSTEM INTERFACE PARAMETERS—R4400**

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TDO <sup>1,2,3</sup>	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TDS	Data Setup		5	—	5	—	3.5	—	ns
TDH	Data Hold		1.5	—	1.5	—	1	—	ns

**NOTES:**

1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

2884 tbl 13a

**BOOT MODE INTERFACE PARAMETERS—R4400**

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMDS	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
TMDH	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

## SECONDARY CACHE INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TSCO <sup>1,2,3</sup>	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TSCDS	Data Setup		5	—	5	—	3.5	—	ns
TSCDH	Data Hold		2	—	1.5	—	1	—	ns
TRd1Cyc <sup>4</sup>	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
TDis <sup>4</sup>	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
TRd2Cyc <sup>4</sup>	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
TWr1Dly <sup>4</sup>	Cycles bet. Addr & SCWr		1	3	1	3	1	3	Pcycles
TWrRc <sup>4</sup>	Cycles bet. deassertion of SCWr to start of next cycle		0	1	0	1	0	1	Pcycles
TWrSup <sup>4</sup>	Cycles from second doubleword to SCWr		2	15	2	15	3	15	Pcycles
TWr2Dly <sup>4</sup>	Cycles between 1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

## NOTES:

- When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
- Timings are measured from 1.5V of the Pclock to 1.5V of signal.
- Capacitive load for all output timings is 50pF. Deration is per CLD specification.
- Number of cycles is configured through the boot time mode control.

## CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

## DC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V<sub>CC</sub> = 3.3V ± 5%; T<sub>case</sub> = 0°C to +85°C)

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	2.4	—	V
V <sub>OHc</sub>	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut) <sup>(3)</sup>	I <sub>OH</sub> = -4mA	2.7	—	2.7	—	2.7	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + .5	2.0	V <sub>CC</sub> + .5	2.0	V <sub>CC</sub> + .5	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1,2)</sup>		-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
V <sub>IHC</sub>	Input HIGH Voltage (MasterClock, Syncln)		0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	0.8 V <sub>CC</sub>	V <sub>CC</sub> + .5	V
V <sub>ILc</sub>	Input LOW Voltage (MasterClock, Syncln)		-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	-0.5 <sup>(1)</sup>	0.2 V <sub>CC</sub>	V
C <sub>in</sub>	Input Capacitance		—	10	—	10	—	10	pF
C <sub>out</sub>	Output Capacitance		—	10	—	10	—	10	pF
I <sub>Leak</sub>	Input Leakage		—	10	—	10	—	10	μA
I <sub>OLeak</sub>	Input/Output Leakage		—	20	—	20	—	20	μA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = 3.3V, T <sub>C</sub> = 25°C	—	2.0	—	2.4	—	2.8	A

## NOTES:

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 15ns.
- Except for MasterClock input.
- Applies to TClock, RClock, MasterOut, and ModeClock outputs.

2884 tbl 11

## AC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V<sub>CC</sub> = 3.3V ± 5%; T<sub>case</sub> = 0°C to +85°C) MasterClock and Clock Parameters<sup>(2)</sup>

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T <sub>MCKHigh</sub>	MasterClock High	<sup>(3)</sup>	4	—	3	—	3	—	ns
T <sub>MCKLow</sub>	MasterClock Low	<sup>(3)</sup>	4	—	3	—	3	—	ns
	MasterClock Freq <sup>(1)</sup>		25	50	25	67	25	75	MHz
T <sub>MCP</sub>	MasterClock Period		20	40	15	40	13.3	40	ns
T <sub>MCKjitter</sub>	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
T <sub>MCRise</sub>	MasterClock Rise Time		—	5	—	4	—	3.5	ns
T <sub>MCFall</sub>	MasterClock Fall Time		—	5	—	4	—	3.5	ns
T <sub>ModeCKP</sub>	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
T <sub>JTAGCKP</sub>	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

## NOTES:

- Operation of the R4400 is only guaranteed with the phase lock loop enabled.
- Capacitive load for all output timings is 50pF. Deration is per CLD specification.
- Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

2884 tbl 12

## SYSTEM INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TDO <sup>1,2,3</sup>	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TDS	Data Setup		5	—	5	—	3.5	—	ns
TDH	Data Hold		1.5	—	1.5	—	1	—	ns

## NOTES:

2884 tbl 13a

- When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
- Timings are measured from 1.5V of the clock to 1.5V of signal.
- Capacitive load for all output timings is 50pF. Deration is per CLD specification.
- Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

## BOOT MODE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMDS	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
TMDH	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

## SECONDARY CACHE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TSCO <sup>1,2,3</sup>	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TSCDS	Data Setup		5	—	5	—	3.5	—	ns
TSCDH	Data Hold		2	—	1.5	—	1	—	ns
TRd1Cyc <sup>4</sup>	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
TDis <sup>4</sup>	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
TRd2Cyc <sup>4</sup>	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
TWr1Dly <sup>4</sup>	Cycles bet. Addr & SCWr		1	3	1	3	1	3	Pcycles
TWrRc <sup>4</sup>	Cycles bet. deassertion of SCWr to start of next cycle		0	1	0	1	0	1	Pcycles
TWrSUP <sup>4</sup>	Cycles from second doubleword to SCWr		2	15	2	15	3	15	Pcycles
TWr2Dly <sup>4</sup>	Cycles between 1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

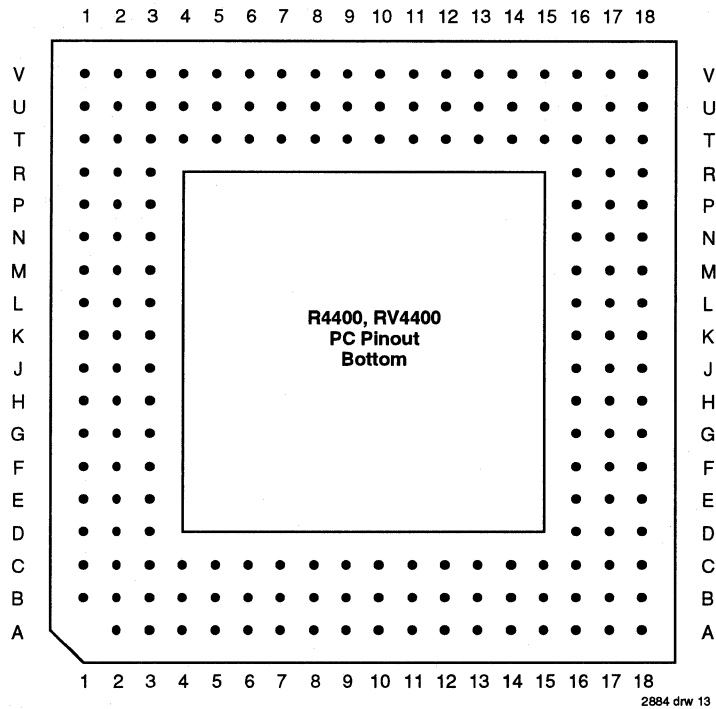
2884 tbl 14

## NOTES:

- When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
- Timings are measured from 1.5V of the Pclock to 1.5V of signal.
- Capacitive load for all output timings is 50pF. Deration is per CLD specification.
- Number of cycles is configured through the boot time mode control.



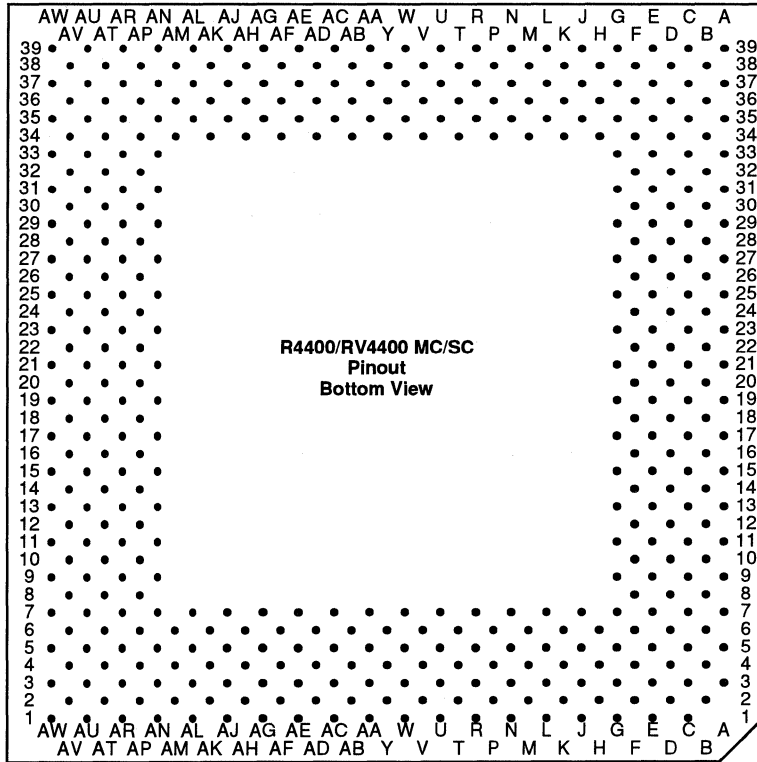
### PHYSICAL SPECIFICATIONS



## IDT79R4400/RV4400 PC PACKAGE PINOUT

R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin
ColdReset	T14	SysAD29	T16	VssP	K16
ExtRqst	U2	SysAD30	R17	Vcc	A2
Fault	B16	SysAD31	M16	Vcc	A4
Reserved (NC)	U10	SysAD32	H2	Vcc	A9
Vcc	T9	SysAD33	G3	Vcc	A11
IOIn	T13	SysAD34	F3	Vcc	A13
IOOut	U12	SysAD35	D2	Vcc	A16
Int0	N2	SysAD36	C3	Vcc	B18
Int1	L3	SysAD37	B3	Vcc	C1
Int2	K3	SysAD38	C6	Vcc	D18
Int3	J3	SysAD39	C7	Vcc	F1
Int4	H3	SysAD40	C10	Vcc	G18
Int5	F2	SysAD41	C11	Vcc	H1
JTCK	H17	SysAD42	B13	Vcc	J18
JTDI	G16	SysAD43	A15	Vcc	K1
JTDO	F16	SysAD44	C15	Vcc	L18
JTMS	E16	SysAD45	B17	Vcc	M1
MasterClock	J17	SysAD46	E17	Vcc	N18
MasterOut	P17	SysAD47	F17	Vcc	R1
ModeClock	B4	SysAD48	L2	Vcc	T18
Modeln	U4	SysAD49	M3	Vcc	U1
NMI	U7	SysAD50	N3	Vcc	V3
PLLCap0	****	SysAD51	R2	Vcc	V6
PLLCap1	****	SysAD52	T3	Vcc	V8
RClock0	T17	SysAD53	U3	Vcc	V10
RClock1	R16	SysAD54	T6	Vcc	V12
RdRdy	T5	SysAD55	T7	Vcc	V14
Release	V5	SysAD56	T10	Vcc	V17
Reset	U16	SysAD57	T11	Vss	A3
SyncIn	J16	SysAD58	U13	Vss	A6
SyncOut	P16	SysAD59	V15	Vss	A8
SysAD0	J2	SysAD60	T15	Vss	A10
SysAD1	G2	SysAD61	U17	Vss	A12
SysAD2	E1	SysAD62	N16	Vss	A14
SysAD3	E3	SysAD63	N17	Vss	A17
SysAD4	C2	SysADC0	C8	Vss	A18
SysAD5	C4	SysADC1	G17	Vss	B1
SysAD6	B5	SysADC2	T8	Vss	C18
SysAD7	B6	SysADC3	L16	Vss	D1
SysAD8	B9	SysADC4	B8	Vss	F18
SysAD9	B11	SysADC5	H16	Vss	G1
SysAD10	C12	SysADC6	U8	Vss	H18
SysAD11	B14	SysADC7	L17	Vss	J1
SysAD12	B15	SysCmd0	E2	Vss	K18
SysAD13	C16	SysCmd1	D3	Vss	L1
SysAD14	D17	SysCmd2	B2	Vss	M18
SysAD15	E18	SysCmd3	A5	Vss	N1
SysAD16	K2	SysCmd4	B7	Vss	P18
SysAD17	M2	SysCmd5	C9	Vss	R18
SysAD18	P1	SysCmd6	B10	Vss	T1
SysAD19	P3	SysCmd7	B12	Vss	U18
SysAD20	T2	SysCmd8	C13	Vss	V1
SysAD21	T4	SysCmdP	C14	Vss	V2
SysAD22	U5	TClock0	C17	Vss	V4
SysAD23	U6	TClock1	D16	Vss	V7
SysAD24	U9	VCCOK	M17	Vss	V9
SysAD25	U11	ValidIn	P2	Vss	V11
SysAD26	T12	ValidOut	R3	Vss	V13
SysAD27	U14	WrRdy	C5	Vss	V16
SysAD28	U15	VccP	K17	Vss	V18

### PHYSICAL SPECIFICATIONS



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## IDT79R4400/RV4400 MC/SC PACKAGE PINOUT

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
ColdReset	AW37	SCDChk9	N37	SCData53	AR13
ExtRqst	AV2	SCDChk10	AU17	SCData54	AR15
Fault	C39	SCDChk11	AG37	SCData55	AT18
Reserved (NC)	AV24	SCDChk12	E19	SCData56	AU23
IOIn	AV32	SCDChk13	R35	SCData57	AT26
IOOut	AV28	SCDChk14	AR19	SCData58	AR27
Int0	AL1	SCDChk15	AE35	SCData59	AN29
IvdAck <sup>(1)</sup>	AA35	SCData0	R3	SCData60	AP32
IvdErr <sup>(1)</sup>	AA39	SCData1	R7	SCData61	AN35
JTCK	U39	SCData2	L5	SCData62	AJ35
JTDI	N39	SCData3	F8	SCData63	AE33
JTDO	J39	SCData4	C9	SCData64	V4
JTMS	G37	SCData5	F12	SCData65	R5
MasterClock	AA37	SCData6	G15	SCData66	N5
MasterOut	AJ39	SCData7	E17	SCData67	E5
ModeClock	B8	SCData8	G21	SCData68	G9
ModeIn	AV8	SCData9	C25	SCData69	E11
NMI	AV16	SCData10	G25	SCData70	G13
PLLCap0	****	SCData11	E29	SCData71	D14
PLLCap1	****	SCData12	G31	SCData72	C21
RClock0	AM34	SCData13	C35	SCData73	D22
RClock1	AL33	SCData14	K36	SCData74	E25
RdRdy	AW7	SCData15	N35	SCData75	G27
Release	AV12	SCData16	AE3	SCData76	C31
Reset	AU39	SCData17	AG5	SCData77	F32
Reserved (NC)	Y2	SCData18	AK4	SCData78	J35
SCAPar0	U5	SCData19	AN9	SCData79	M34
SCAPar1	U1	SCData20	AU9	SCData80	AC7
SCAPar2	P4	SCData21	AN13	SCData81	AE5
SCAddr1	AL5	SCData22	AT14	SCData82	AG7
SCAddr2	AG1	SCData23	AR17	SCData83	AR5
SCAddr3	AE7	SCData24	AT22	SCData84	AR9
SCAddr4	AC1	SCData25	AU25	SCData85	AR11
SCAddr5	AC5	SCData26	AN27	SCData86	AN15
SCAddr6	AC3	SCData27	AR29	SCData87	AP16
SCAddr7	AA1	SCData28	AN31	SCData88	AU21
SCAddr8	AB4	SCData29	AR35	SCData89	AN23
SCAddr9	AA5	SCData30	AK36	SCData90	AR25
SCAddr10	AA7	SCData31	AG35	SCData91	AP28
SCAddr11	AA3	SCData32	T6	SCData92	AU31
SCAddr12	W3	SCData33	L3	SCData93	AR33
SCAddr13	Y6	SCData34	L7	SCData94	AL35
SCAddr14	W5	SCData35	E7	SCData95	AH34
SCAddr15	W7	SCData36	G11	SCData96	U7
SCAddr16	W1	SCData37	E13	SCData97	N3
SCAddr17	U3	SCData38	E15	SCData98	N7
SCAddr0W	AN7	SCData39	G17	SCData99	C5
SCAddr0X	AN5	SCData40	C23	SCData100	E9
SCAddr0Y	AM6	SCData41	F24	SCData101	C11
SCAddr0Z	AL7	SCData42	E27	SCData102	C13
SCDCS	M6	SCData43	D30	SCData103	F16
SCDChk0	G19	SCData44	C33	SCData104	E21
SCDChk1	T34	SCData45	E35	SCData105	G23
SCDChk2	AP20	SCData46	L35	SCData106	C27
SCDChk3	AD34	SCData47	R33	SCData107	F28
SCDChk4	C19	SCData48	AF4	SCData108	E31
SCDChk5	R37	SCData49	AJ3	SCData109	G33
SCDChk6	AU19	SCData50	AJ7	SCData110	J37
SCDChk7	AE37	SCData51	AP8	SCData111	N33
SCDChk8	C17	SCData52	AT10	SCData112	AD6

## IDT79R4400/RV4400 MC/SC PACKAGE PINOUT (continued)

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
SCData113	AG3	Status7	AC33	SysAD57	AW27
SCData114	AJ5	SyncIn	W39	SysAD58	AW31
SCData115	AU5	SyncOut	AN39	SysAd59	AW35
SCData116	AN11	SysAD0	T2	SysAD60	AU37
SCData117	AU11	SysAD1	M2	SysAD61	AR39
SCData118	AU13	SysAD2	J3	SysAD62	AL39
SCData119	AN17	SysAD3	G3	SysAD63	AG39
SCData120	AR21	SysAD4	C1	SysADC0	A17
SCData121	AP24	SysAD5	A3	SysADC1	R39
SCData122	AU27	SysAD6	A9	SysADC2	AW17
SCData123	AT30	SysAD7	A13	SysADC3	AD38
SCData124	AU33	SysAD8	A21	SysADC4	A19
SCData125	AN33	SysAD9	A25	SysADC5	T38
SCData126	AL37	SysAD10	A29	SysADC6	AW19
SCData127	AG33	SysAD11	A33	SysADC7	AC39
SCOE	N1	SysAd12	B38	SysCmd0	G1
SCTCS	J1	SysAD13	E37	SysCmd1	E3
SCTChk0	AN21	SysAD14	G39	SysCmd2	B2
SCTChk1	AN19	SysAD15	L39	SysCmd3	B12
SCTChk2	AU15	SysAD16	AD2	SysCmd4	B16
SCTChk3	AP12	SysAD17	AH2	SysCmd5	B20
SCTChk4	AU7	SysAD18	AL3	SysCmd6	B24
SCTChk5	AR7	SysAD19	AN3	SysCmd7	B28
SCTChk6	AH6	SysAD20	AU1	SysCmd8	B32
SCTag0	K4	SysAD21	AW3	SysCmdP	A37
SCTag1	G7	SysAD22	AW9	TClock0	H34
SCTag2	C7	SysAD23	AW13	TClock1	J33
SCTag3	D10	SysAD24	AW21	VCCOk	AE39
SCTag4	C15	SysAD25	AW25	ValidIn	AN1
SCTag5	D18	SysAD26	AW29	ValidOut	AR3
SCTag6	F20	SysAD27	AW33	WrRdy	A7
SCTag7	E23	SysAD28	AV38	VccSense	W33
SCTag8	D26	SysAD29	AR37	VssSense	U37
SCTag9	C29	SysAD30	AM38	VccP	AA33
SCTag10	G29	SysAD31	AH38	VssP	Y34
SCTag11	E33	SysAD32	R1	Vcc	A39
SCTag12	G35	SysAD33	L1	Vcc	B6
SCTag13	L33	SysAD34	H2	Vcc	B10
SCTag14	L37	SysAD35	E1	Vcc	B18
SCTag15	P36	SysAD36	C3	Vcc	B26
SCTag16	AF36	SysAD37	A5	Vcc	B34
SCTag17	AJ37	SysAD38	A11	Vcc	D4
SCTag18	AJ33	SysAd39	A15	Vcc	D8
SCTag19	AN37	SysAD40	A23	Vcc	D16
SCTag20	AU35	SysAD41	A27	Vcc	D24
SCTag21	AR31	SysAd42	A31	Vcc	D32
SCTag22	AU29	SysAD43	A35	Vcc	D36
SCTag23	AN25	SysAd44	C37	Vcc	F2
SCTag24	AR23	SysAD45	E39	Vcc	F14
SCWrW	J5	SysAD46	H38	Vcc	F22
SCWrX	J7	SysAD47	M38	Vcc	F30
SCWrY	H6	SysAD48	AE1	Vcc	F38
SCWrZ	G5	SysAD49	AJ1	Vcc	H4
Status0	U33	SysAD50	AM2	Vcc	H36
Status1	U35	SysAD51	AR1	Vcc	K6
Status2	V36	SysAD52	AU3	Vcc	K38
Status3	W35	SysAD53	AW5	Vcc	P2
Status4	W37	SysAD54	AW11	Vcc	P34
Status5	AC37	SysAD55	AW15	Vcc	T4
Status6	AC35	SysAD56	AW23		

**IDT79R4400 MC/SC PACKAGE PINOUT (continued)**

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
Vcc	T36	Vcc	AV34	Vss	Y4
Vcc	V6	Vcc	AW1	Vss	Y36
Vcc	V38	Vcc	AW39	Vss	AB6
Vcc	Y38	Vss	B4	Vss	AB36
Vcc	AB2	Vss	B14	Vss	AB38
Vcc	AB34	Vss	B22	Vss	AF2
Vcc	AD4	Vss	B30	Vss	AF34
Vcc	AD36	Vss	B36	Vss	AH4
Vcc	AF6	Vss	D2	Vss	AH36
Vcc	AF38	Vss	D6	Vss	AK6
Vcc	AK2	Vss	D12	Vss	AK38
Vcc	AK34	Vss	D20	Vss	AP4
Vcc	AM4	Vss	D28	Vss	AP6
Vcc	AM36	Vss	D34	Vss	AP14
Vcc	AP2	Vss	D38	Vss	AP22
Vcc	AP10	Vss	F4	Vss	AP30
Vcc	AP18	Vss	F6	Vss	AP34
Vcc	AP26	Vss	F10	Vss	AP36
Vcc	AP38	Vss	F18	Vss	AT2
Vcc	AT4	Vss	F26	Vss	AT6
Vcc	AT8	Vss	F34	Vss	AT12
Vcc	AT16	Vss	F36	Vss	AT20
Vcc	AT24	Vss	K2	Vss	AT28
Vcc	AT32	Vss	K34	Vss	AT34
Vcc	AT36	Vss	M4	Vss	AT38
Vcc	AV6	Vss	M36	Vss	AV4
Vcc	AV14	Vss	P6	Vss	AV10
Vcc	AV20	Vss	P38	Vss	AV18
Vcc	AV22	Vss	V2	Vss	AV26
Vcc	AV30	Vss	V34	Vss	AV36

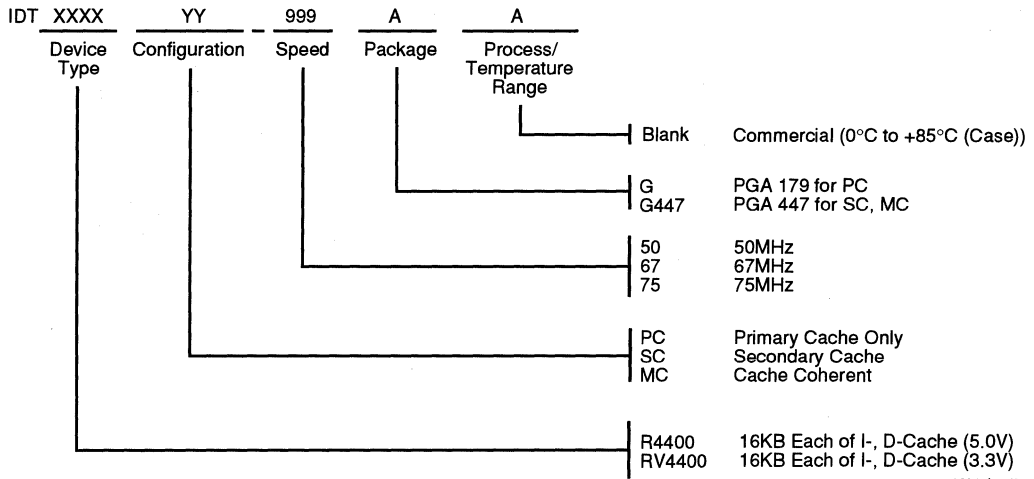
**NOTE:**

1. Available in IDT79R4400MC only. For IDT79R4400SC, these inputs must be pulled to Vcc.

2884 tbl 19

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**ORDERING INFORMATION**



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**VALID COMBINATIONS**

- R4400 PC — 50, 67, 75      G
- R4400 SC — 50, 67, 75    G447
- R4400 MC — 50, 67, 75    G447
- RV4400 PC — 50, 67, 75    G
- RV4400 SC — 50, 67, 75    G447
- RV4400 MC — 50, 67, 75    G447



Integrated Device Technology, Inc.

# FOURTH GENERATION 64-BIT RISC MICROPROCESSOR

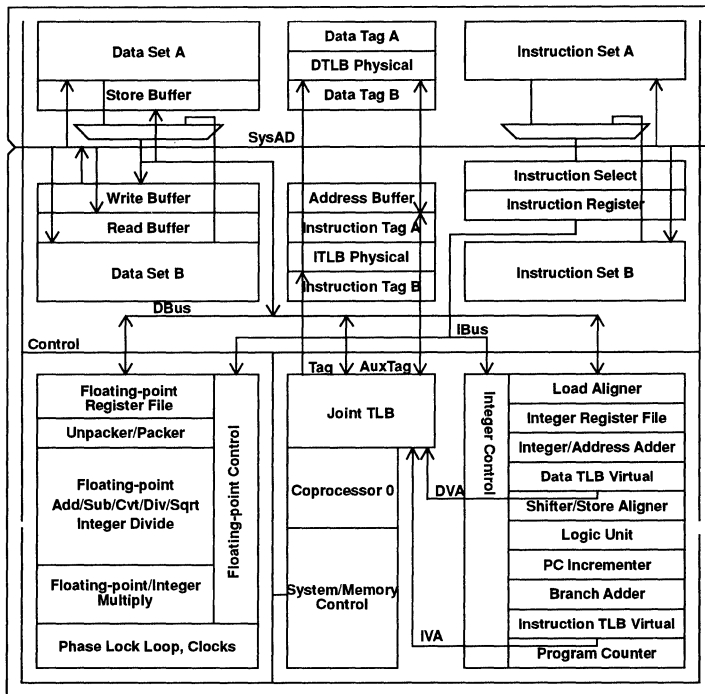
**ORION™**  
IDT79R4600™

## FEATURES:

- True 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit floating-point operations
  - 64-bit registers
  - 64-bit virtual address space
- High-performance microprocessor
  - 150 peak MIPS at 150MHz
  - 50peak MFLOP/s at 150MHz
  - 96 SPECint92 at 150Mz
  - Two-way set associative caches
- High level of integration
  - 64-bit integer CPU
  - 64-bit floating-point unit
  - 16KB instruction cache; 16KB data cache
  - Flexible MMU with large TLB
- Low-power operation
  - 3.3V or 5V power supply options
  - 21mW/MHZ typical internal power dissipation (2.1W @ 100MHz, 3.3V)
- Standby mode reduces internal power to 400mW @ 3.3V
- Standard operating system support includes:
  - Microsoft Windows™ NT
  - UNISOFT Unix™ System V.4
- Fully software compatible with R4000 RISC Processor Family
- Available in R4000PC/R4000PC pin-compatible 179-pin PGA or 208-pin MQUAD
- 50MHz, 67MHz, 75MHz input frequencies with mode bit dependent output clock frequencies
  - On-chip clock doubler for 150MHz pipeline
- 64GB physical address space
- Processor family for a wide variety of applications
  - Desktop workstations and PCs
  - Deskside or departmental servers
  - High-performance embedded applications (e.g. color printers, multi-media and internetworking.)
  - Notebooks

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## BLOCK DIAGRAM:



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COMMERCIAL TEMPERATURE RANGE

March 1994



**DESCRIPTION:**

The IDT79R4600 supports a wide variety of processor-based applications, from 32-bit Windows NT desktop or notebook systems through high-performance, 64-bit OLTP systems. Compatible with the IDT79R4000PC family for both hardware and software, the R4600 will serve in many of the same applications, but, in addition supports low-power operation for applications such as "green" desktops and notebook computers. It does not provide integrated secondary cache and multiprocessor support as found in the R4000SC and R4000MC, but an external secondary cache can lastly be designed around it. The large on-chip two-way set associative caches make this unnecessary in most embedded control applications.

The R4600 brings R4000SC performance levels to the R4000PC package, while at the same time providing lower cost and lower power. It does this by providing larger on-chip caches that are two-way set associative, fewer pipeline stalls, and early restart for data cache misses. The result is 96 SPECint92 and >90SPECfp92 (exact figures are system-dependent).

The R4600 provides complete upward application-software compatibility with the IDT79R3000™ family of microprocessors, including the IDT RISController™ 79R3051™/R3052™/R3041™/R3071™/R3081™ as well as the IDT79R4000 family of microprocessors. Microsoft Windows NT and UNISOFT Unix V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4600-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

Together with the R4000 family, the R4600 provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4000 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit

operating systems and applications.

The 64-bit computing and addressing capability of the R4600 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the R4600 CPU. A more detailed description of the processor is available in the "IDT79R4600 Processor Hardware User's Manual", available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

**HARDWARE OVERVIEW**

The R4600 family brings a high-level of integration designed for high-performance computing. The key elements of the R4600 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

**Pipeline**

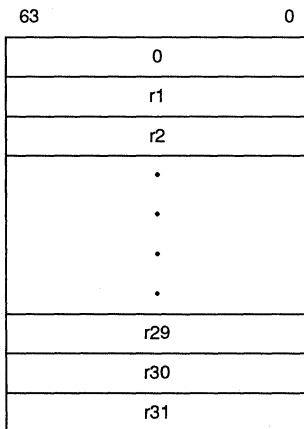
The R4600 uses a 5-stage pipeline similar to the IDT79R3000. The simplicity of this pipeline allows the R4600 to be lower cost and lower power than super-scalar or super-pipelined processors. Unlike the R3000, the R4600 does virtual-to-physical translation in parallel with cache access. This allows the R4600 to operate at twice the frequency of the R3000 and to support a larger TLB for address translation.

Compared to the 8-stage R4000 pipeline, the R4600 is more efficient (requires fewer stalls).

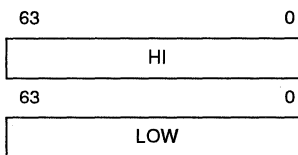
Figure 2 shows the R4600 pipeline.

Figure 1. CPU Registers

**General Purpose Registers**



**Multiply/Divide Registers**



**Program Counter**

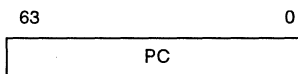
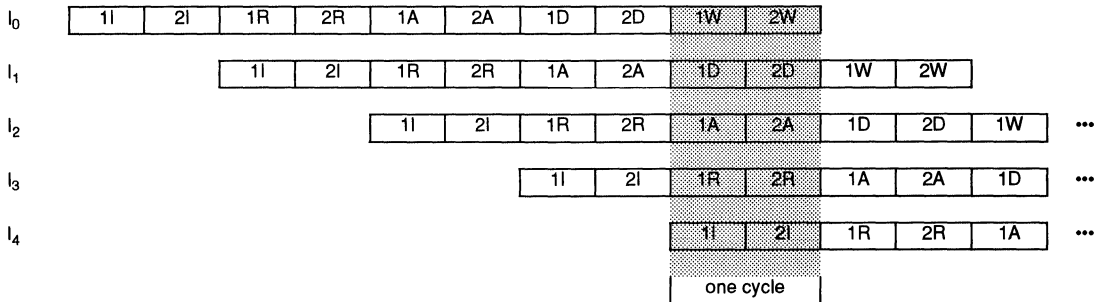


Figure 2. R4600 Pipeline



- 1I-1R Instruction cache access
- 2I Instruction virtual to physical address translation in ITLB
- 2A-2D Data cache access and load align
- 1D Data virtual to physical address translation in DTLB
- 1D-2D Virtual to physical address translation in JTLB
- 2R Register file read
- 2R Bypass calculation
- 2R Instruction decode
- 2R Branch address calculation
- 1A Issue or slip decision
- 1A-2A Integer add, logical, shift
- 1A Data virtual address calculation
- 2A Store align
- 1A Branch decision
- 2W Register file write

**Integer Execution Engine**

The R4600 implements the MIPS Instruction Set architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4600 includes the same additions to the instruction set as found in the R4000 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4600 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point reg-

isters, and a floating-point control/status register.

**Register File**

The R4600 has thirty-two general-purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

**ALU**

The R4600 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

**Integer Multiply/Divide**

The R4600 uses the floating-point unit to perform integer multiply and divide. The results of the operation are placed in the HI and LO registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. Table 1 below shows the number of processor internal cycles required between an integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs.

**Table 1: Integer multiply/divide cycles**

	32-bit	64-bit
MULT	10	12
DIV	42	74

**Floating-Point Co-Processor**

The R4600 incorporates an entire floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

**Floating-Point Units**

The R4600 floating-point execution units supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 6 cycles.

As in the IDT79R3010A and IDT79R4000, the R4600 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with the IEEE Standard 754.

Table 2 below gives the latencies of some of the floating-point instructions in internal processor cycles.

**Table 2: Floating-Point Cycles**

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	8	8
DIV	32	61
SQRT	31	60
CMP	3	3
FIX	4	4
FLOAT	6	6
ABS	1	1

**Table 2: Floating-Point Cycles**

Operation	Single Precision	Double Precision
MOV	1	1
NEG	1	1
LWC1, LDC1	2	2
SWC1, SDC1	1	1

**Floating-Point General Register File**

The floating-point register file is made up of thirty-two 64-bit registers. With the LDC1 and SDC1 instructions the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store double-word instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

**System Control Co-processor (CP0)**

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4600 CP0 is essentially identical to that of the R4000PC, except that the WatchLo and WatchHi registers are no longer present and the Index CACHE ops use an extra address bit to select one of the two sets (the R4000 caches are direct mapped, instead of two-way set associative).

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer (the ITLB), a data address translation buffer (the DTLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

**System Control Co-Processor Registers**

The R4600 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4600 includes registers to implement a real-time cycle counting facility, to aid in cache diagnostic testing, and to assist in data error detection.

Figure 5 shows the CP0 registers.

**Virtual to Physical Address Mapping**

The R4600 provides three modes of virtual addressing:

- user mode
- supervisor mode
- kernel mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4600 provides a single, uniform virtual address space of 256GB (2GB for 32-bit mode).

When operating in the kernel mode, four distinct virtual address spaces, totalling 1024GB (4GB in 32-bit mode), are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4600 processors also support a supervisor mode in which the virtual address space is 256.5GB (2.5GB in 32-bit mode), divided into three regions based on the high-order bits of the virtual address.

Figure 4 shows the address space layout for 32-bit operation.

When the R4600 is configured as a 64-bit microprocessor, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout.

**Joint TLB**

For fast virtual-to-physical address decoding, the R4600 uses a large, fully associative TLB which maps 96 Virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the

amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory mapped using only one TLB entry.

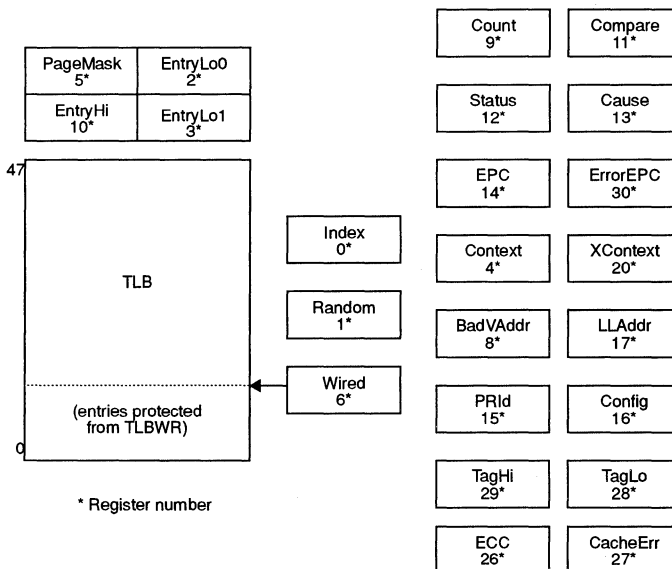
The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4600 provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, non-coherent write-back, non-coherent write-through write-allocate, non-coherent write-through no write-allocate. Non-coherent write-back is typically used for both code and data on the R4600; the write-through modes support more efficient frame buffer accesses than the R4000 family, cache coherency is not supported, however.

**Instruction TLB**

The R4600 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address

Figure 3. The R4600 CP0 Registers



translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is invisible to the user.

### Data TLB

The R4600 also incorporates a 4-entry data TLB. Each entry maps a 4KB page. The data TLB improves performance by allowing data address translation to occur in parallel with data address translation. When a miss occurs on an data address translation, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used half is filled. The operation of the DTLB is invisible to the user.

Furthermore, the large 2-way set-associative caches increase emulation performance of DOS and Windows 3.1 applications when running under Windows NT.

**Figure 4. Kernel Mode Virtual Addressing (32-bit mode)**

0xFFFFFFFF	Kernel virtual address space (kseg3) Mapped, 0.5GB
0xE0000000	
0xDFFFFFFF	Supervisor virtual address space (sseg) Mapped, 0.5GB
0xC0000000	
0xBFFFFFFF	Uncached kernel physical address space (kseg1) Unmapped, 0.5GB
0xA0000000	
0x9FFFFFFF	Cached kernel physical address space (kseg0) Unmapped, 0.5GB
0x80000000	
0x7FFFFFFF	
	User virtual address space (useg) Mapped, 2.0GB
0x00000000	

### Cache Memory

In order to keep the R4600's high-performance pipeline full and operating efficiently, the R4600 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2.4GB per second at a pipeline-clock frequency of 150MHz.

### Instruction Cache

The R4600 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 600MB/sec at 150MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill writes 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

### Data Cache

For fast, single cycle data access, the R4600 includes a 16KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through on a per-page basis when it is appropriate, such as for frame buffers.

Associated with the Data Cache is the store buffer. When the R4600 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4600 to execute a store every processor cycle and to perform back-to-back stores without penalty.

### Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses,

use the on-chip write buffer. The write buffer holds up to four 64-bit address and data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

**System Interface**

The R4600 supports a 64-bit system interface that is compatible with the R4000PC system interface. This interface operates from two clocks provided by the R4600, TClock[1:0] and RClock[1:0], at some division of the internal clock.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 150MHz.

Figure 5 on page 7 shows a typical system using the R4600. In this example two banks of DRAMs are used to supply and accept data with a DDxxDD data pattern.

**System Address/Data Bus**

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4600 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4600 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4600. Again, the system designer has the flexibility to make these price/performance trade-offs.

**System Command Bus**

The R4600 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4600. Processor requests are initiated by the R4600 and responded to by an external device. External requests are issued by an external device and require the R4600 to respond.

The R4600 supports one to eight byte and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

**Handshake Signals**

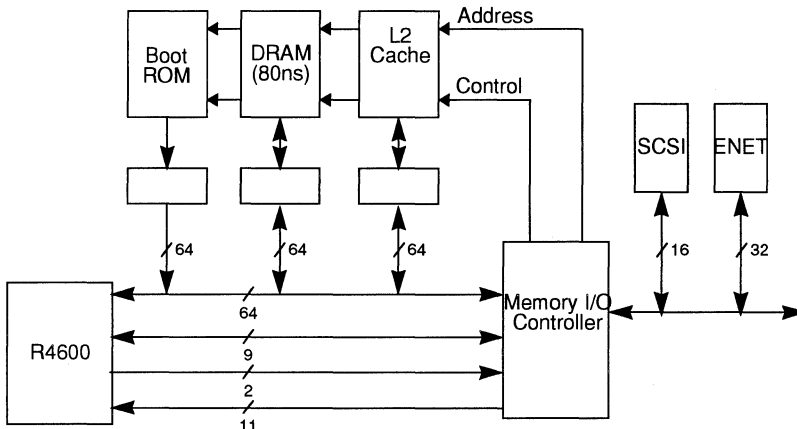
There are six handshake signals on the system interface. Two of these,  $\overline{\text{RdRdy}}$  and  $\overline{\text{WrRdy}}$  are used by an external device to indicate to the R4600 whether it can accept a new read or write transaction. The R4600 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$  and  $\overline{\text{Release}}$  are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts  $\overline{\text{ExtRqst}}$ . The R4600 responds by asserting  $\overline{\text{Release}}$  to release the system interface to slave state.

$\overline{\text{ValidOut}}$  and  $\overline{\text{ValidIn}}$  are used by the R4600 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4600 asserts  $\overline{\text{ValidOut}}$  when it is driving these buses with a valid command or data, and the external device drives

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Figure 5. Typical Desktop System Block Diagram



ValidIn when it has control of the buses and is driving a valid command or data.

**Non-overlapping System Interface**

The R4600 requires a non-overlapping system interface, compatible with the R4000PC. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4600 issues another request. The R4600 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4600.

The R4600 asserts ValidOut and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release. The external device can then begin sending the data to the R4600.

Figure 6 on page 8 shows a processor block read request and the external agent read response. The read latency is 4 cycles (ValidOut to ValidIn), and the response data pattern is DDxxDD. Figure 6 on page 8 shows a processor block write.

**External Requests**

The R4600 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4600 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue requests to the processor, such as a request for the R4600 to write to the R4600 interrupt register.

The following is a list of the supported external requests:

- Write
- Null

**Boot Time Options**

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the Vccok Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

**JTAG Interface**

For compatibility with the R4000PC, the R4600 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

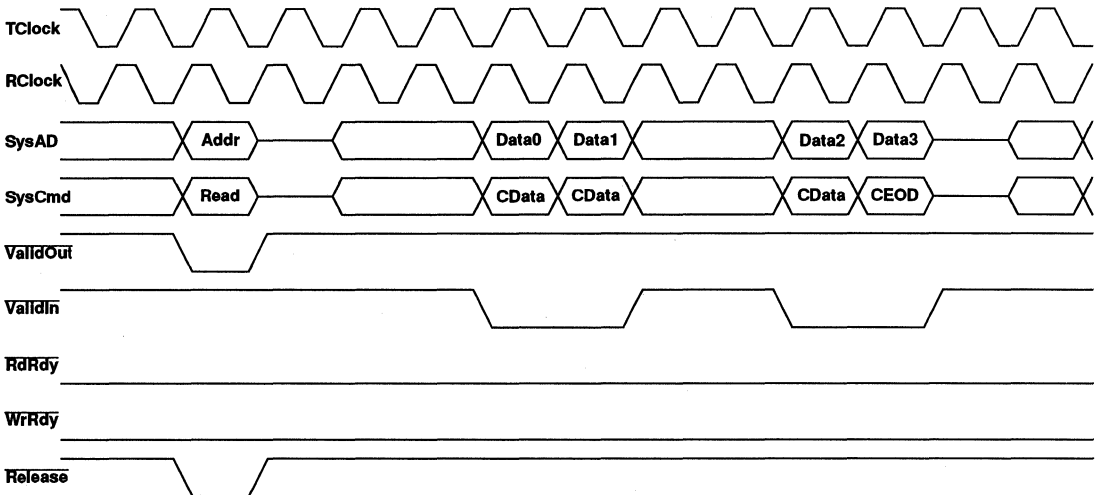
**Boot-Time Modes**

The boot-time serial mode stream is defined in Table 3 below. Bit 0 is the bit presented to the processor when Vccok is asserted; bit 255 is the last.

**Power Management**

CP0 is also used to control the power management for the R4600. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU. The standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by any interrupt.

Figure 6. Processor Block Read



**Table 3: Boot time mode stream**

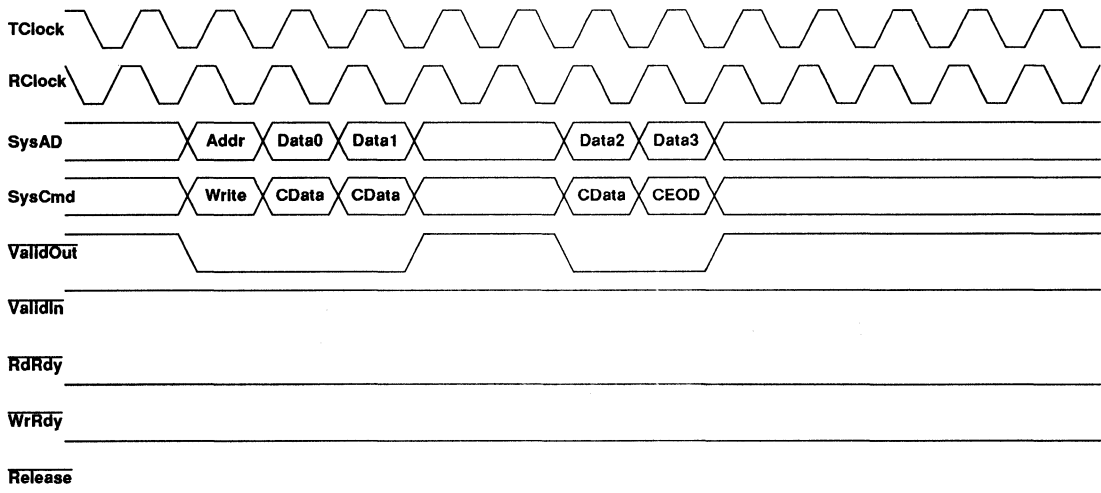
**Table 3: Boot time mode stream**

Mode bit	Description
0	reserved (must be zero)
4..1	Writeback data rate 0 → D, 1 → DDx, 2 → DDxx, 3 → Dx Dx, 4 → DDxxx, 5 → DDxxxx, 6 → DxxDxx, 7 → DDxxxxxx, 8 → DxxxDxxx, 9-15 reserved
7..5	Clock divisor 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved
8	0 → Little endian, 1 → Big endian
10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue
11	Disable the timer interrupt on Int[5].

Mode bit	Description
12	reserved (must be zero)
14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)  Reserved
bit 15*	0 -> TClock[0] enabled 1 -> TClock[0] disabled
bit 16*	0 -> TClock[1] enabled 1 -> TClock[1] disabled
bit 17*	0 -> TClock[0] enabled 1 -> TClock[0] disabled
bit 18*	0 -> TClock[1] enabled 1 -> TClock[1] disabled
255..19	must be zero  * valid for rev 2.0 only, otherwise must be zero

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**Figure 7. Processor Block Write**





**Differences from the R4000PC**

Tables 4 to 10 highlight some of the differences between the R4600 and the R4000PC. This list is not exhaustive.

**Table 4: System interface comparison between R4000PC and R4600**

	R4000PC	R4600
I/O	TTL compatible	IDT 3V standard R4600: TTL-compatible (5V±0.5V)
Package	179-pin ceramic PGA	same and 208-pin MQUAD
JTAG	yes	no (serial out connected directly to serial in)
Block transfer sizes	16B or 32B	32B
Sclock divisor	2, 3, or 4	2, 3, 4, 5, 6, 7, 8
Non-block writes	max throughput of 4 sclock cycles	two new system interface protocol options that support 2 sclock cycle throughput (remains 4 in compatibility mode)
Serial configuration	as described in <i>R4000 User's Guide</i>	different, as described in Table 3
Address bits 63..56 on reads and writes	zero	bits 19..12 of virtual address
Uncached and write-through stores	uncached stores stall until sent on system interface	uncached and write-through stores buffered in 4-entry write buffer
SysADC	parity only	same
SysADC for non-data cycles	zero on R4000, parity on R4000	zero
SysCmdP	zero on R4000, parity on R4000	zero
Parity error during writeback	use Cache Error exception	output bad parity
Error bit in data identifier of read responses	Bus Error if error bit set for any doubleword	Only check error bit of first doubleword; all other error bits ignored
Parity error on read data	Bus Error if parity error in any doubleword	bad parity written to cache; take Cache Error exception if bad parity occurs on doublewords that the processor is waiting for
Block writes	1-2 null cycles between address and data	0 cycles between address and data
Release after Read Request	variable latency	0 latency
SysAD value for x cycles of writeback data pattern	data bus undefined	data bus maintains last D cycle value
SysAD bus use after last D cycle of writeback	?	unused for trailing x cycles (e.g. DDxxDDxx, not DDxxDD)
Output slew rate	dynamic feedback control	simple CMOS output buffers with 2-bit static strength control
IOOut output	output slew rate control feedback loop output	driven HI, do not connect (reserved for future output)
IOIn input	output slew rate control input	should be driven HI (reserved for future input)
GrpRunB output	do not connect	same (reserved for future output)
GrpStallB input	should be connected to Vcc	same (reserved for future input)
FaultB output pin	indicates compare mismatch	driven HI, do not connect (reserved for future output)

**Table 5: Cache comparison between R4000PC and R4600**

	R4000PC	R4600
Cache Sizes	8KB Instruction cache, 8KB Data cache	16KB Instruction cache, 16KB Data cache
Cache Line Sizes	software selectable between 16B and 32B	fixed at 32B
Cache Index	vAddr <sub>12..0</sub>	same
Cache Tag	pAddr <sub>35..12</sub>	same
Cache Organization	direct mapped	2-way set associative
Data cache write policy	write-allocate and write-back	write-allocate or not based on TLB entry, write-through or not based on TLB entry
Data cache miss	stall, output address, copy dirty data to write-back buffer, refill cache, output writeback data	same, with FIFO to select the set to refill
Data order for block reads	sub-block ordering	same
Data order for block writes	sequential	same
Instruction cache miss restart	restart after all data received and written to cache	same
Data cache miss restart	restart after all data received and written to cache	restart on first doubleword, send subsequent doublewords to response buffer
Instruction Tag	2-bit cache state	1-bit cache state
Cache miss overhead	5-8? cycles	3 cycles
Instruction cache parity	1 parity bit per 8 data bits	1 parity bit per 32 data bits
Data cache parity	1 parity bit per 8 data bits	same

**Table 6: TLB comparison between R4000PC and R4600**

	R4000PC	R4600
Instruction virtual address translation	2-entry ITLB	same
ITLB miss	1 cycle penalty, refilled from JTLB, LRU replacement	1 cycle on branch, jump, and ERET, 2 cycles otherwise, refilled from JTLB, LRU replacement
Data virtual address translation	done directly in JTLB	4-entry DTLB
DTLB miss	n.a.	1 cycle penalty, refilled from JTLB, pseudo-LRU replacement
JTLB	48 entries of even/odd page pairs, fully associative	same
Page size	4KB, 16KB, ..., 16MB	same
Multiple entry match in JTLB	sets TS in Status and disables TLB until Reset to prevent damage	no damage for multiple match; no detection or shutdown implemented
Virtual address size	VSIZE = 40	same
Physical address size	PSIZE = 36	same

**Table 7: Pipeline comparison between R4000PC and R4600**

	R4000PC	R4600
ALU latency	1 cycle	1 cycle
Load latency	3 cycles	2 cycles
Branch latency	4 cycles (2 cycle penalty for taken branches)	2 cycles (no penalty for taken branches)
Store buffer (not write buffer)	2 doublewords	1 doubleword
Integer multiply	integer multiply hardware, 1 cycle to issue	done in floating-point multiplier, 4 cycles to issue
Integer divide	done in integer datapath adder, slips until done	done in floating-point adder, 4 cycles to issue
Integer multiply	HI and LO available at the same time	LO available one cycle before HI
Integer divide	HI and LO available at the same time	HI available one cycle before LO
HI and LO hazards	yes, HI and LO written early in pipeline	no, HI and LO written after w
MFHI/MFLO latency	1 cycle	2 cycles
SLLV, SRLV, SRAV	2 cycles to issue	1 cycle to issue
DSLL, DSRL, DSRA, DSLL32, DSRL32, DSRA32, DSLLV, DSRLV, DSRAV	2 cycles to issue	1 cycle to issue

**Table 8: Coprocessor 0 comparison between R4000PC and R4600**

	R4000PC	R4600
WatchLo, WatchHi	implemented	unimplemented
Config	as described in <i>MIPS R-Series Architecture</i>	subset
Status	as described in <i>MIPS R-Series Architecture</i> , but RP not functional	no TS or RP
Low-power standby mode	no	WAIT instruction disables internal clock, freezing pipeline and other state; resume on interrupt
MFC0/MTC0 hazard	only hazardous for certain cp0 register combinations	always hazardous -- detected and 1-cycle slip inserted
EntryLo0, EntryLo1	as described in <i>MIPS R-Series Architecture</i>	two new cache algorithms added to C field for non-coherent write-through
TagLo, TagHi, ECC, CacheErr	R4000SC bits implemented but meaningless	Only bits meaningful on R4000PC implemented
TagLo	as described in <i>MIPS R-Series Architecture</i>	bits 5..3 read/write, but otherwise unused, bit 2 used for F bit
Exceptions	as described in <i>MIPS R-Series Architecture</i> (VCEI and VCED not possible in R4000PC)	VCEI, VCED, and WATCH exceptions not implemented
Index CACHE ops I Fill CACHE op	use vAddr <sub>12..4</sub> to select line	use vAddr <sub>13</sub> to select set, vAddr <sub>12..5</sub> to select line of set
Index Store Tag CACHE op	Status.CE ignored	TagLo.P stored if Status.CE set
PRId	Imp = 0x04	Imp = 0x20

**Table 9: Coprocessor 1 comparison between R4000PC and R4600**

	R4000PC	R4600
Possible exception stall	only for operands that can cause exceptions	some simplifications in detection hardware
Floating-point divide	separate divide unit	done in floating-point adder
Floating-point square root	done in floating-point adder	same
Converts to/from 64-bit integer	uses unimplemented for integer operands/ results with more than 53 bits of precision	handles full 64-bit operands and results
Floating-point registers	Status.FR enables all 32 floating point registers	same
FCR0	Imp = 0x05	Imp = 0x20

**Table 10: R4000PC Errata comparison with R4600**

	R4000PC errata	R4600
COPz rs field illegal	FPE unimplemented exception for COP1 (incorrect)	reserved instruction exception, as described in <i>MIPS R-Series Architecture</i>
BCz rt field illegal	FPE unimplemented exception for COP1 (incorrect)	reserved instruction exception, as described in <i>MIPS R-Series Architecture</i>
Address error check for xkseg	C00000FFFFFFFF (incorrect)	C00000FF7FFFFFFFF (correct)
PTEBase field of Context and XContext	same bits (incorrect)	same for rev 1.x separate for rev 2.0
TLB vs. XTLB refill vector selection	based on current mode (incorrect)	based on address (correct)

**PIN DESCRIPTION**

The following is a list of interface, interrupt, and miscellaneous pins available on the R4600.

Pin Name	Type	Description
System interface:		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity for the R4600 unused on input and zero on output.
Clock/control interface:		
MasterClock	Input	Master clock Master clock input at one half the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
IOOut	Output	Reserved for future output Always HIGH.
IOIn	Input	Reserved for future input Should be driven HIGH.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.

Pin Name	Type	Description
Fault*	Output	Fault Always HIGH.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.
Interrupt interface:		
Int* (5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
JTAG interface:		
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.
Initialization interface:		
Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4600 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset. ColdReset must be de-asserted synchronously with MasterOut.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterOut.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

## Standby Mode Operations

The R4600 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as "Standby Mode".

### Entering Standby Mode

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, some of the input pin clocks (Int[5:0]\*, NMI\*, ExtReq\*, Reset\*, and ColdReset\*) and the output clocks (TClock[1:0], RClock[1:0], SyncOut, Modeclock and MasterOut) will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (i.e. the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	RV4600 3.3V±5%	R4600 5.0V±5%	Unit
		Commercial	Commercial	
V <sub>TERM</sub>	Terminal Voltage with respect to GND	-0.5 <sup>(2)</sup> to +4.6	-0.5 <sup>(2)</sup> to +7.0	V
T <sub>C</sub>	Operating Temperature (case)	0 to +85	0 to +85	°C
T <sub>BIAS</sub>	Case Temperature Under Bias	-55 to +125	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-55 to +125	°C
I <sub>IN</sub>	DC Input Current	20 <sup>(3)</sup>	20 <sup>(3)</sup>	mA
I <sub>OUT</sub>	DC Output Current	50	50	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -2.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub>+0.5 Volts.
- When V<sub>IN</sub> < 0V or V<sub>IN</sub> > V<sub>CC</sub>
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

## RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V <sub>CC</sub>	
			RV4600	R4600
Commercial	0°C to +85°C (Case)	0V	3.3V±5%	5.0V±5%

**DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE RV4600**

( $V_{CC} = 3.3 \pm 5\%$ ,  $T_{CASE} = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	RV4600 100MHz		RV4600 133MHz		RV4600 150MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
$V_{OL}$	—	0.1V	—	0.1V	—	0.1V	$I_{OUT} = 20\mu\text{A}$
$V_{OH}$	$V_{CC} - 0.1V$	—	$V_{CC} - 0.1V$	—	$V_{CC} - 0.1V$	—	
$V_{OL}$	—	0.4V	—	0.4V	—	0.4V	$I_{OUT} = 4\text{mA}$
$V_{OH}$	2.4V	—	2.4V	—	2.4V	—	
$V_{IL}$	-0.5V	$0.2V_{CC}$	-0.5V	$0.2V_{CC}$	-0.5V	$0.2V_{CC}$	—
$V_{IH}$	$0.7V_{CC}$	$V_{CC} + 0.5V$	$0.7V_{CC}$	$V_{CC} + 0.5V$	$0.7V_{CC}$	$V_{CC} + 0.5V$	—
$V_{OHC}$	—	—	—	—	—	—	—
$V_{ILC}$	—	—	—	—	—	—	—
$V_{IHC}$	—	—	—	—	—	—	—
$C_{IN}$	—	10pF	—	10pF	—	10pF	—
$C_{OUT}$	—	10pF	—	10pF	—	10pF	—
$I_{O\text{LEAK}}$	—	20 $\mu\text{A}$	—	20 $\mu\text{A}$	—	20 $\mu\text{A}$	Input/Output Leakage

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Parameter		RV4600 100MHz		RV4600 133MHz		RV4600 150MHz		Conditions
		Typical <sup>(12)</sup>	Maximum	Typical <sup>(12)</sup>	Maximum	Typical <sup>(12)</sup>	Maximum	
System Condition:		100/50MHz		133/44MHz		150/50MHz		—
$I_{CC}$	standby	—	125mA	—	175mA	—	200mA	$C_L = 0\text{pF}^{(11)}$
		—	175mA	—	225mA	—	250mA	$C_L = 50\text{pF}$
	active	575mA	975mA	775mA	1150mA	875mA	1300mA	$C_L = 0\text{pF}$ , No SysAd activity <sup>(11)</sup>
		650mA	1100mA	850mA	1375mA	950mA	1550mA	$C_L = 50\text{pF}$ R4x00 compatible writes $T_C = 25^\circ\text{C}$
		650mA	1275mA	850mA	1525mA	950mA	1725mA	$C_L = 50\text{pF}$ Pipelined writes or Write re-issue, $T_C = 25^\circ\text{C}$



**AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE RV4600** $(V_{CC}=3.3V \pm 5\%; T_{CASE} = 0^{\circ}C \text{ to } +85^{\circ}C)$ **Clock Parameters**

Parameter	Symbol	Test Conditions	RV4600 100MHz		RV4600 133MHz		RV4600 150MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	$t_{MCHIGH}$	Transition $\leq 5ns$	4	—	3	—	3	—	ns
MasterClock LOW	$t_{MLOW}$	Transition $\leq 5ns$	4	—	3	—	3	—	ns
MasterClock Frequency <sup>(5)</sup>	—	—	25	50	25	67	25	75	MHz
MasterClock Period	$t_{MCP}$	—	20	40	15	40	13.3	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}^{(11)}$	—	—	$\pm 250$	—	$\pm 250$	—	$\pm 250$	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}^{(11)}$	—	—	$\pm 500$	—	$\pm 500$	—	$\pm 500$	ps
MasterClock Rise Time	$t_{MCRise}^{(11)}$	—	—	5	—	4	—	3.5	ns
MasterClock Fall Time	$t_{MCFall}^{(11)}$	—	—	5	—	4	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	$256^*$ $t_{MCP}$	—	$256^*$ $t_{MCP}$	—	$256^*$ $t_{MCP}$	ns

**NOTES:**

5. Operation of the R4600 is only guaranteed with the Phase Lock Loop enabled.

**System Interface Parameters<sup>(6)</sup>**

Parameter	Symbol	Test Conditions	RV4600 100MHz ( $V_{CC}=3.3\pm 5\%$ )		RV4600 133MHz ( $V_{CC}=3.3\pm 5\%$ )		RV4600 150MHz ( $V_{CC}=3.3\pm 5\%$ )		Units
			Min	Max	Min	Max	Min	Max	
Data Output <sup>(7)</sup>	$t_{DM} = \text{Min}$ $t_{DO} = \text{Max}$	mode <sub>14..13</sub> = 10 (fastest)	1.0	9	1.0	9	1.0	8	ns
		mode <sub>14..13</sub> = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Setup	$t_{DS}$	$t_{rise} = 5ns$ $t_{fall} = 5ns$	3.5	—	3.5	—	3.5	—	ns
Data Hold	$t_{DH}$		1.5	—	1.5	—	1.5	—	ns

**Boot Time Interface Parameters**

Parameter	Symbol	Test Conditions	RV4600 100MHz		RV4600 133MHz		RV4600 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	$t_{DS}$	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	$t_{DH}$	—	0	—	0	—	0	—	Master Clock Cycle

## Capacitive Load Deration

Parameter	Symbol	RV4600 100MHz		RV4600 133MHz		RV4600 150MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	C <sub>LD</sub>	0.2	0.2	0.2	0.2	0.2	0.2	ns/25pF

## DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE R4600

(V<sub>CC</sub> = 5.0±5%, T<sub>CASE</sub> = 0°C to +85°C)

Parameter	R4600 100MHz		R4600 133MHz		R4600 150MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V <sub>OL</sub>	—	0.1V	—	0.1V	—	0.1V	I <sub>OUT</sub>   = 20μA
V <sub>OH</sub>	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	V <sub>CC</sub> - 0.1V	—	
V <sub>OL</sub>	—	0.4V	—	0.4V	—	0.4V	I <sub>OUT</sub>   = 4mA
V <sub>OH</sub>	3.5V	—	3.5V	—	3.5V	—	
V <sub>IL</sub>	-0.5V	0.8V	-0.5V	0.8V	-0.5V	0.8V	—
V <sub>IH</sub>	2.0V	V <sub>CC</sub> + 0.5V	2.0V	V <sub>CC</sub> + 0.5V	2.0V	V <sub>CC</sub> + 0.5V	—
I <sub>IN</sub>	—	±10μA	—	±10μA	—	±10μA	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
C <sub>IN</sub>	—	10pF	—	10pF	—	10pF	—
C <sub>OUT</sub>	—	10pF	—	10pF	—	10pF	—
I/O <sub>LEAK</sub>	—	20μA	—	20μA	—	20μA	Input/Output Leakage

Parameter		R4600 100MHz		R4600 133MHz		R4600 150MHz		Conditions
		Typical <sup>(12)</sup>	Maximum	Typical <sup>(12)</sup>	Maximum	Typical <sup>(12)</sup>	Maximum	
System Condition:		100/50MHz		133/44MHz		150/50MHz		—
I <sub>CC</sub>	standby	—	175mA	—	225mA	—	260mA	C <sub>L</sub> = 0pF <sup>(11)</sup>
		—	250mA	—	325mA	—	370mA	C <sub>L</sub> = 50pF
	active	875mA	1250mA	1175mA	1675mA	875mA	1875mA	C <sub>L</sub> = 0pF, No SysAd activity <sup>(11)</sup>
		975mA	1650mA	1275mA	2075mA	1450mA <sup>(9)</sup>	2325mA	C <sub>L</sub> = 50pF R4x00 compatible writes T <sub>C</sub> = 25°C
		975mA	1925mA	1275mA	2300mA	1450mA	2600mA	C <sub>L</sub> = 50pF Pipelined writes or Write re-issue, T <sub>C</sub> = 25°C

**AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE R4600** $(V_{CC}=5.0V \pm 5\%; T_{CASE} = 0^{\circ}C \text{ to } +85^{\circ}C)$ **Clock Parameters**

Parameter	Symbol	Test Conditions	R4600 100MHz		R4600 133MHz		R4600 150MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	$t_{MCHIGH}$	Transition $\leq 5ns$	4	—	3	—	3	—	ns
MasterClock LOW	$t_{MCLow}$	Transition $\leq 5ns$	4	—	3	—	3	—	ns
MasterClock Frequency <sup>(5)</sup>	—	—	25	50	25	67	25	75	MHz
MasterClock Period	$t_{MCP}$	—	20	40	15	40	13.3	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}^{(11)}$	—	—	$\pm 250$	—	$\pm 250$	—	$\pm 250$	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}^{(11)}$	—	—	$\pm 500$	—	$\pm 500$	—	$\pm 500$	ps
MasterClock Rise Time	$t_{MCRise}^{(11)}$	—	—	5	—	4	—	3.5	ns
MasterClock Fall Time	$t_{MCFall}^{(11)}$	—	—	5	—	4	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	$256^* t_{MCP}$	—	$256^* t_{MCP}$	—	$256^* t_{MCP}$	ns
JTAG Clock Period	$t_{JTAGCKP}$	—	—	$4^* t_{MCP}$	—	$4^* t_{MCP}$	—	$4^* t_{MCP}$	ns

**NOTES:**

6. Operation of the R4600 is only guaranteed with the Phase Lock Loop enabled.

**AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE R4600** $(V_{CC} = 5.0V \pm 5\%; T_{CASE} = 0^{\circ}C \text{ to } +85^{\circ}C)$ **System Interface Parameters<sup>(6)</sup>**

Parameter	Symbol	Test Conditions	R4600 100MHz		R4600 133MHz		R4600 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output <sup>(7)</sup>	$t_{DO}$	mode <sub>14..13</sub> = 10 (fastest)	1.0	9	1.0	9	1.0	8	ns
		mode <sub>14..13</sub> = 11	1.5	11	1.5	10	1.3	9.3	ns
		mode <sub>14..13</sub> = 00	1.5	3	1.6	1	1.6	10.6	ns
		mode <sub>14..13</sub> = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Setup	$t_{DS}$	$t_{rise} = 5ns$ $t_{fall} = 5ns$	3.5	—	3.5	—	3.5	—	ns
Data Hold	$t_{DH}$		1.5	—	1.5	—	1.0	—	ns

**NOTES:**

7. Timings are measured from 1.5V of the clock to 1.5V of the signal.

8. Capacitive load for all output timings is 50pF.

9. Timings are measured from 1.5V of the clock to 1.5V of the signal.

10. Capacitive load for all output timings is 50pF.

11. Guaranteed by Design.

12. Typical integer instruction mix and cache miss rates.

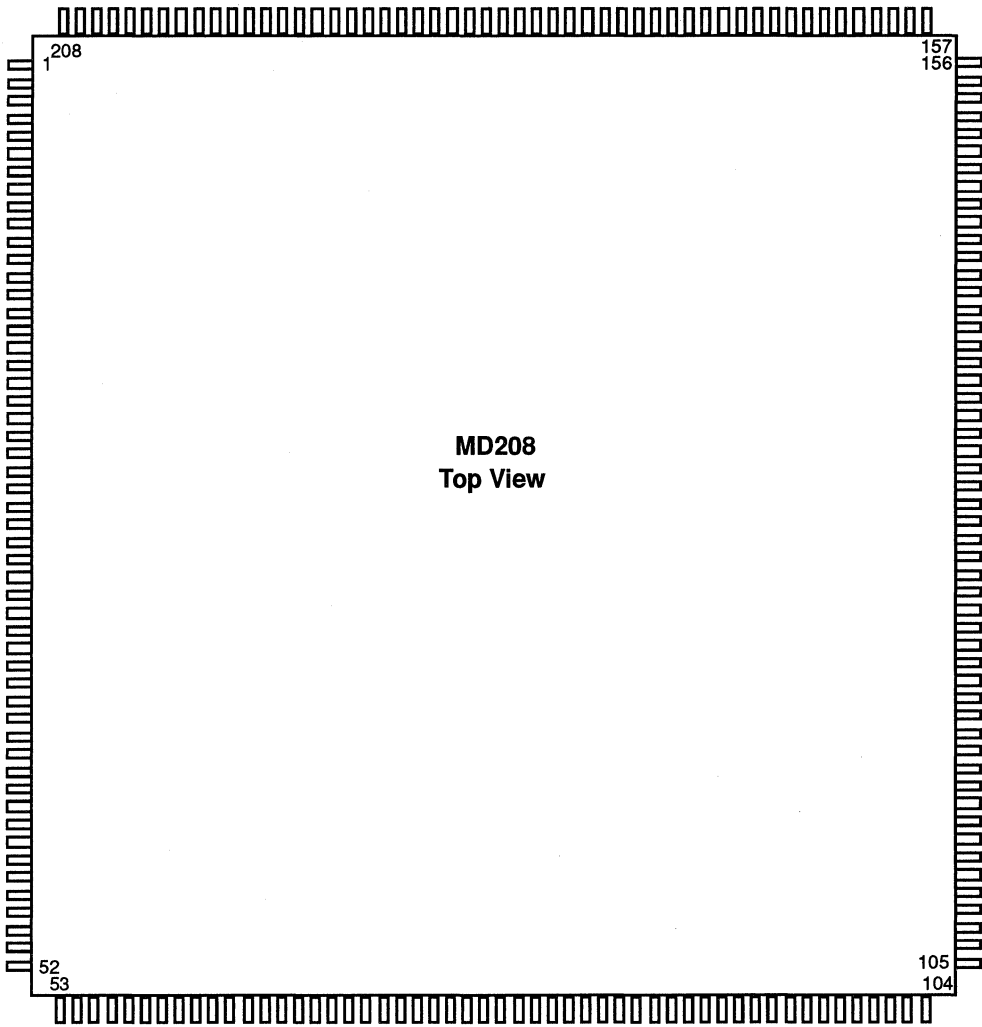
**Boot Time Interface Parameters**

Parameter	Symbol	Test Conditions	R4600 100MHz		R4600 133MHz		R4600 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	$t_{DS}$	—	3	—	3	—	3	—	MasterClock cycles
Mode Data Hold	$t_{DH}$	—	0	—	0	—	0	—	MasterClock cycles

**CAPACITIVE LOAD DERATION**

Parameter	Symbol	R4600 100MHz		R4600 133MHz		R4600 150MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	$C_{LD}$	0	2	0	2	0	2	ns/25pF

PHYSICAL SPECIFICATIONS — MQUAD



## RV4600 MQUAD package pin-out

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	Vss	55	SysCmd2	107	N.C.	159	RClock0
4	Vcc	56	SysAD36	108	N.C.	160	RClock1
5	SysAD45	57	SysAD4	109	Vcc	161	SyncOut
6	SysAD13	58	SysCmd1	110	Vss	162	SysAD30
7	FaultB	59	Vss	111	SysAD21	163	Vcc
8	SysAD44	60	Vcc	112	SysAD53	164	Vss
9	Vss	61	SysAD35	113	RdRdyB	165	SysAD62
10	Vcc	62	SysAD3	114	ModeIn	166	MasterOut
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	Vss	117	Vcc	169	Vcc
14	SysAD11	66	Vcc	118	Vss	170	Vss
15	Vss	67	N.C.	119	ReleaseB	171	VccOK
16	Vcc	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	IntB5	122	NMIB	174	Vcc
19	SysAD10	71	SysAD33	123	Vcc	175	Vss
20	SysCmd7	72	SysAD1	124	Vss	176	N.C.
21	Vss	73	Vss	125	SysADC2	177	N.C.
22	Vcc	74	Vcc	126	SysADC6	178	N.C.
23	SysAD41	75	IntB4	127	Vcc	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	Vcc	181	VccP
26	SysAD40	78	IntB3	130	Vss	182	VssP
27	N.C.	79	Vss	131	SysAD56	183	N.C.
28	N.C.	80	Vcc	132	N.C.	184	N.C.
29	Vss	81	IntB2	133	SysAD25	185	MasterClock
30	Vcc	82	SysAD16	134	SysAD57	186	Vcc
31	SysAD8	83	SysAD48	135	Vcc	187	Vss
32	SysCmd5	84	IntB1	136	Vss	188	SyncIn
33	SysADC4	85	Vss	137	IOOut	189	Vcc
34	SysADC0	86	Vcc	138	SysAD26	190	Vss
35	Vss	87	SysAD17	139	SysAD58	191	JTCK
36	Vcc	88	SysAD49	140	IOIn	192	SysADC5
37	SysCmd4	89	IntB0	141	Vcc	193	SysADC1
38	SysAD39	90	SysAD18	142	Vss	194	JTDI
39	SysAD7	91	Vss	143	SysAD27	195	Vcc
40	SysCMD3	92	Vcc	144	SysAD59	196	Vss
41	Vss	93	SysAD50	145	ColdResetB	197	SysAD47
42	Vcc	94	ValidInB	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	Vcc	199	JTD0
44	SysAD6	96	SysAD51	148	Vss	200	SysAD46
45	ModeClock	97	Vss	149	SysAD60	201	Vcc
46	WrRdyB	98	Vcc	150	ResetB	202	Vss
47	SysAD37	99	ValidOutB	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	JTMS
49	Vss	101	SysAD52	153	Vcc	205	TClock1
50	Vcc	102	ExtRqstB	154	Vss	206	TClock0
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.C.

N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

## R4600/RV4600 PGA Pin-out

Function	Pin
ColdReset	T14
ExtRqst	U2
Fault	B16
Reserved O (NC)	U10
Reserved I (Vcc)	T9
IOIn	T13
IOOut	U12
Int0	N2
Int1	L3
Int2	K3
Int3	J3
Int4	H3
Int5	F2
JTCK	H17
JTDI	G16
JTDO	F16
JTMS	E16
MasterClock	J17
MasterOut	P17
ModeClock	B4
ModeIn	U4
NMI	U7
RClock0	T17
RClock1	R16
RdRdy	T5
Release	V5
Reset	U16
SyncIn	J16
SyncOut	P16
SysAD0	J2
SysAD1	G2
SysAD2	E1
SysAD3	E3
SysAD4	C2

Function	Pin
SysAD5	C4
SysAD6	B5
SysAD7	B6
SysAD8	B9
SysAD9	B11
SysAD10	C12
SysAD11	B14
SysAD12	B15
SysAD13	C16
SysAD14	D17
SysAD15	E18
SysAD16	K2
SysAD17	M2
SysAD18	P1
SysAD19	P3
SysAD20	T2
SysAD21	T4
SysAD22	U5
SysAD23	U6
SysAD24	U9
SysAD25	U11
SysAD26	T12
SysAD27	U14
SysAD28	U15
SysAD29	T16
SysAD30	R17
SysAD31	M16
SysAD32	H2
SysAD33	G3
SysAD34	F3
SysAD35	D2
SysAD36	C3
SysAD37	B3
SysAD38	C6
SysAD39	C7

Function	Pin
SysAD40	C10
SysAD41	C11
SysAD42	B13
SysAD43	A15
SysAD44	C15
SysAD45	B17
SysAD46	E17
SysAD47	F17
SysAD48	L2
SysAD49	M3
SysAD50	N3
SysAD51	R2
SysAD52	T3
SysAD53	U3
SysAD54	T6
SysAD55	T7
SysAD56	T10
SysAD57	T11
SysAD58	U13
SysAD59	V15
SysAD60	T15
SysAD61	U17
SysAD62	N16
SysAD63	N17
SysADC0	C8
SysADC1	G17
SysADC2	T8
SysADC3	L16
SysADC4	B8
SysADC5	H16
SysADC6	U8
SysADC7	L17
SysCmd0	E2
SysCmd1	D3
SysCmd2	B2

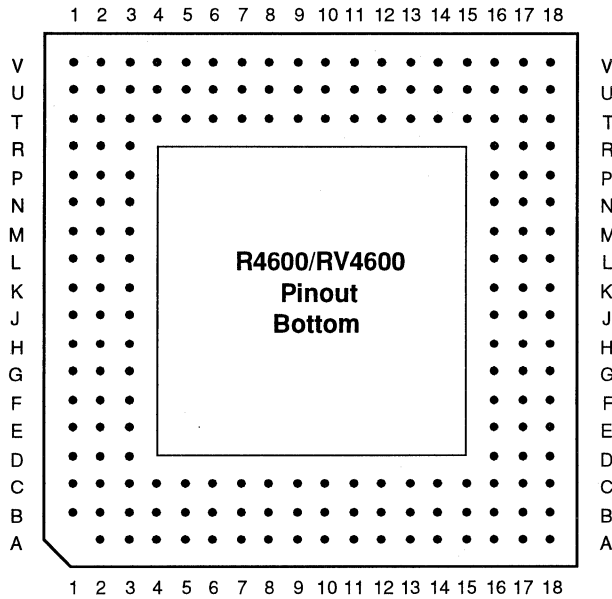
Function	Pin
SysCmd3	A5
SysCmd4	B7
SysCmd5	C9
SysCmd6	B10
SysCmd7	B12
SysCmd8	C13
SysCmdP	C14
TClock0	C17
TClock1	D16
VCCOk	M17
ValidIn	P2
ValidOut	R3
WrRdy	C5
VccP	K17
VssP	K16
Vcc	A2
Vcc	A4
Reserved I (NC)	A7
Vcc	A9
Vcc	A11
Vcc	A13
Vcc	A16
Vcc	B18
Vcc	C1
Vcc	D18
Vcc	F1
Vcc	G18
Vcc	H1
Vcc	J18
Vcc	K1
Vcc	L18
Vcc	M1
Vcc	N18
Vcc	R1
Vcc	T18

Function	Pin
Vcc	U1
Vcc	V3
Vcc	V6
Vcc	V8
Vcc	V10
Vcc	V12
Vcc	V14
Vcc	V17
Vss	A3
Vss	A6
Vss	A8
Vss	A10
Vss	A12
Vss	A14
Vss	A17
Vss	A18
Vss	B1
Vss	C18
Vss	D1
Vss	F18
Vss	G1
Vss	H18
Vss	J1
Vss	K18
Vss	L1
Vss	M18
Vss	N1
Vss	P18
Vss	R18
Vss	T1
Vss	U18
Vss	V1
Vss	V2
Vss	V4
Vss	V7

Function	Pin
Vss	V9
Vss	V11
Vss	V13
Vss	V16
Vss	V18

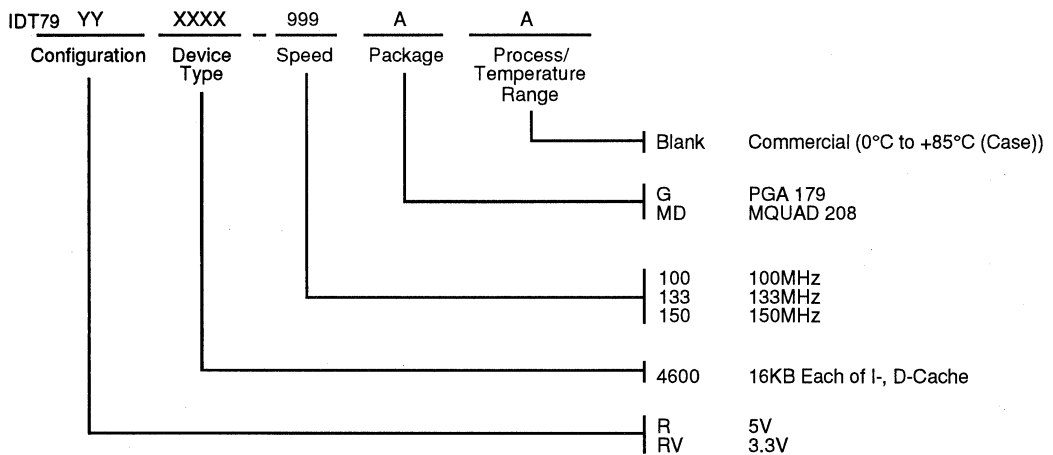


**PHYSICAL SPECIFICATIONS — PGA**



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**ORDERING INFORMATION**



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GENERAL INFORMATION

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TECHNOLOGY AND CAPABILITIES

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QUALITY AND RELIABILITY

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PACKAGE DIAGRAM OUTLINES

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RISC PROCESSING COMPONENTS

5

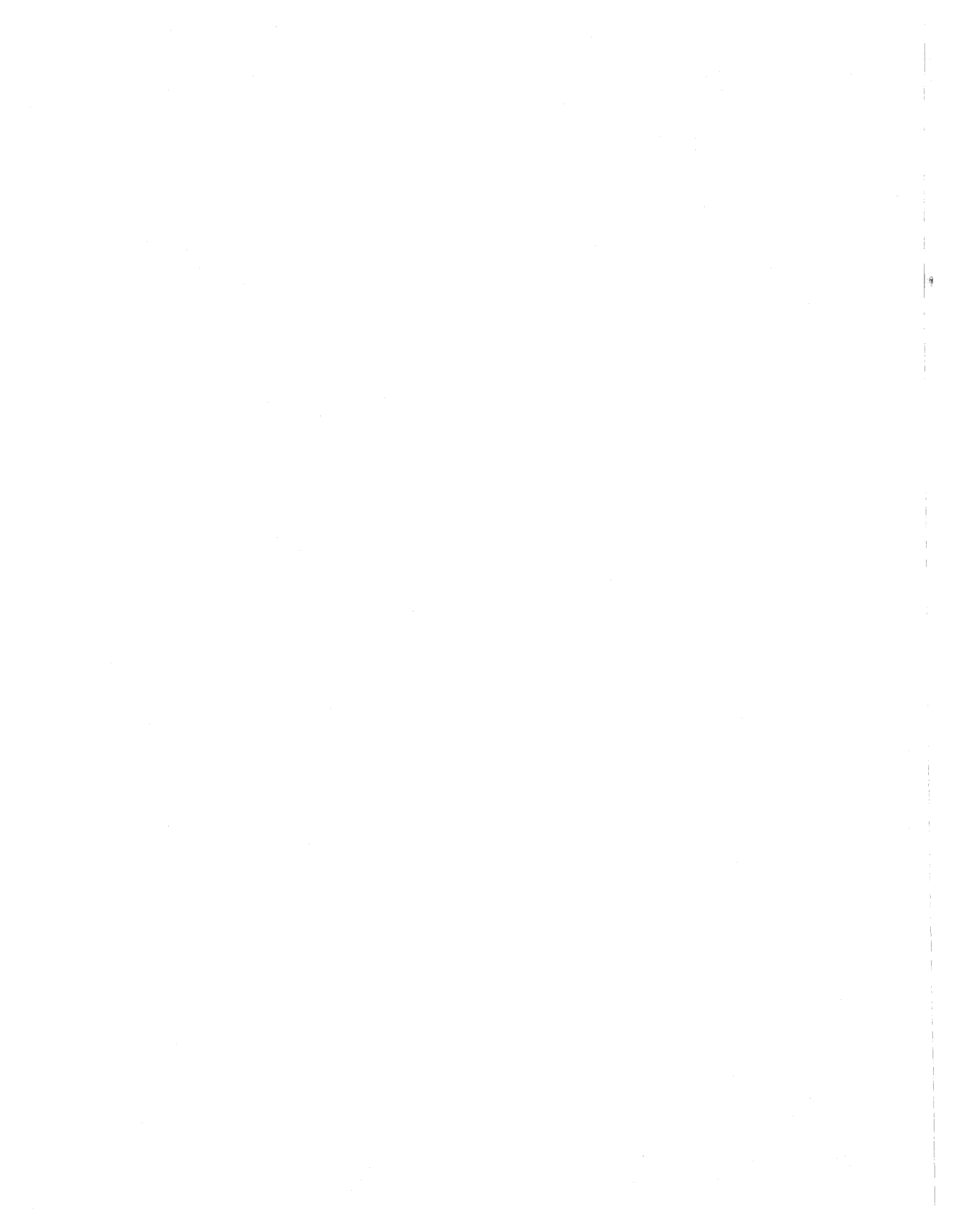
**RISC SUPPORT COMPONENTS**

6

RISC DEVELOPMENT SUPPORT  
PRODUCTS

7

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## RISC SUPPORT COMPONENTS

A RISC microprocessor is an important, but not self-sufficient, element of a high-performance general or embedded computing system. Equally important is the memory system (both cache and main memory) and the I/O interface to the execution core.

To simplify the task of building these high-performance subsystems, IDT produces a wide variety of support chips and building block devices. These chips range from general purpose devices such as fast static RAM and high-performance logic (used with many processor families), to specialized devices used in only certain types of applications (such as the IDT LaserFIFO, used in laser printer systems) and devices designed to work with only a specific processor family.

Generic building block devices include SRAMs, with densities from 16KB to 1MB and access times as low as 7ns, as well as high-speed logic devices such as the FCT-T family.

By providing these system solutions as building blocks, IDT allows its customers the maximum flexibility in achieving their price/performance goals while minimizing time-to-market, real estate and complexity of the end system.

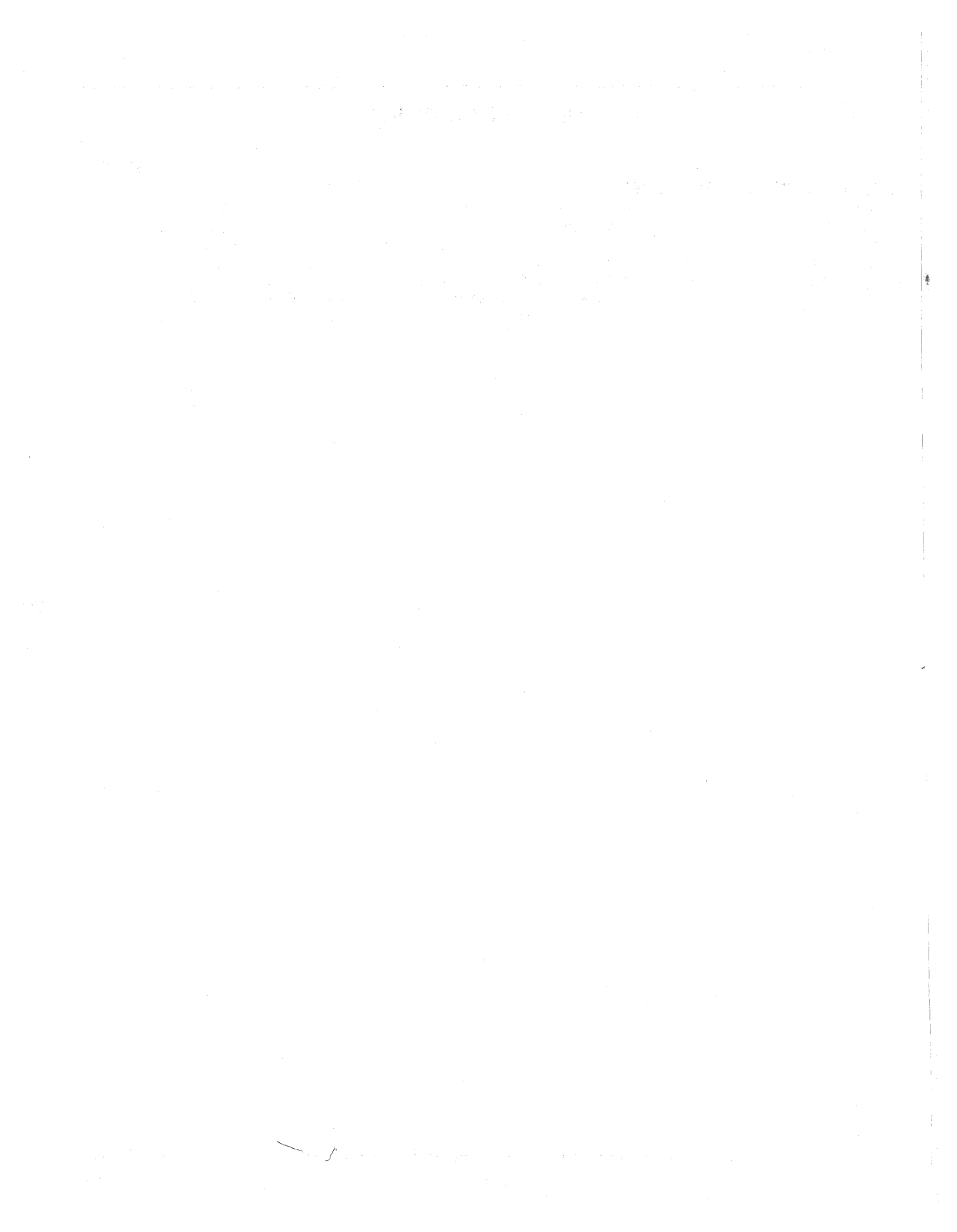
This section of the data book contains some selected devices which have either been specifically designed for particular RISC processors or found to be exceptionally useful in these high-performance systems.



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Integrated Device Technology, Inc.

# RISC FLOATING POINT ACCELERATOR (FPA) CORE

## R3010A Core

### FEATURES:

- Hardware support of single- and double-precision operations:
  - Floating-Point Add
  - Floating-Point Subtract
  - Floating-Point Multiply
  - Floating-Point Divide
  - Floating-Point Comparisons
  - Floating-Point Conversions
- 50MHz operation
- Direct, high-speed interface with R3000A processor core
- Supports full conformance with IEEE 754-1985 Floating-Point specification
- Full 64-bit operation using sixteen 64-bit data registers
- High-speed 0.6μ CMOS technology
- 32-bit status/control register providing access to all IEEE-Standard exception handling
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA
- Overlapped operation of independent floating point ALUs

### DESCRIPTION:

The R3010A Floating-Point Accelerator (FPA) operates in conjunction with the R3000A processor, and extends the R3000A instruction set to perform arithmetic operations on values in floating-point representations. The R3010A FPA with associated system software fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recommendations.

This data sheet provides an overview of the features and architecture of the R3010A FPA core. This core is incorporated in devices such as the IDT79R3081™. Further information on this device can be found in the IDT79R3081 data sheet and hardware user's manual.

### R3010A FPA REGISTERS

The R3010A FPA provides 32 general-purpose, 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the system's programmers as an extension of the CPU internal registers.

### FUNCTIONAL BLOCK DIAGRAM

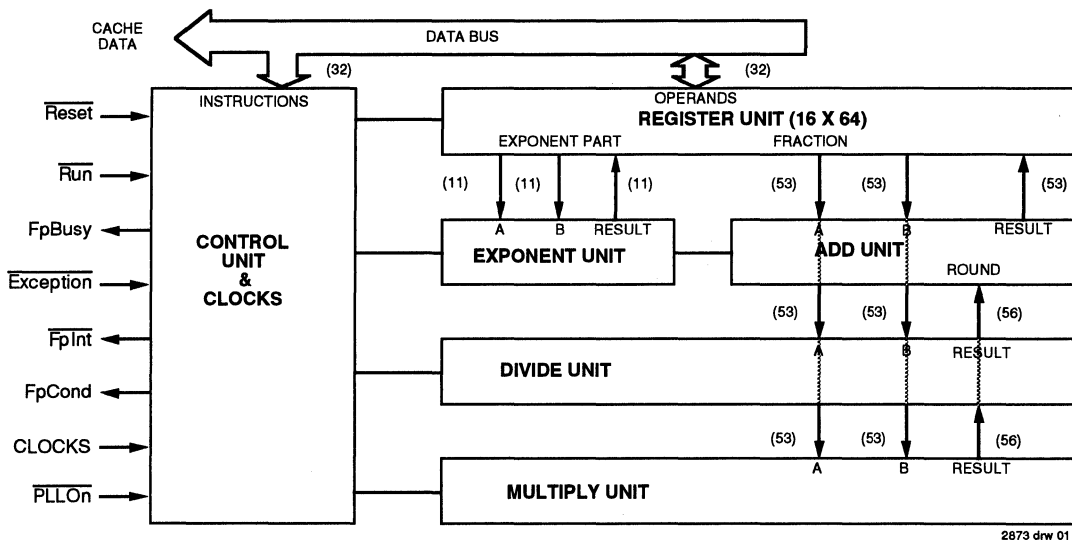


Figure 1. R3010A Functional Block Diagram

The IDT logo is a registered trademark and R3081 is a trademark of Integrated Device Technology, Inc.



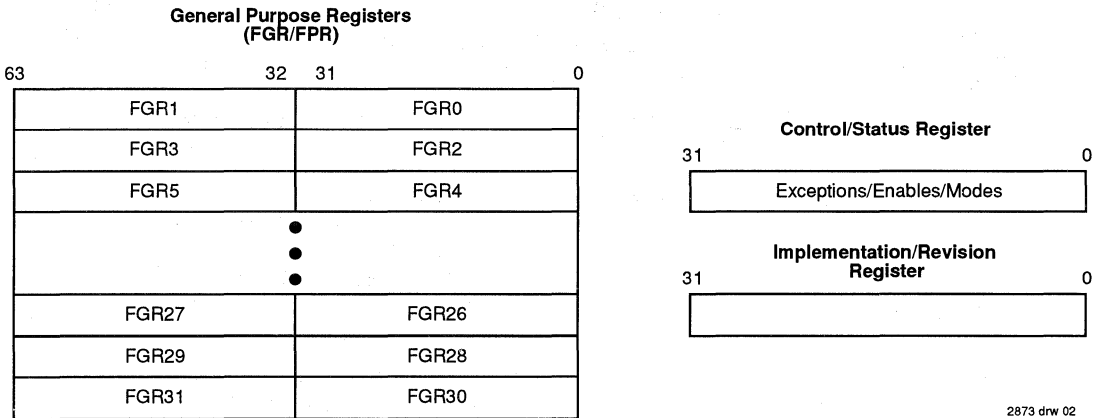


Figure 2. R3010A FPA Registers

The FPA registers are shown in Figure 2.

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

**Floating-Point General Registers (FGR)**

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

**Floating-Point Registers (FPR)**

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

**Floating-Point Control Registers (FCR)**

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

**COPROCESSOR OPERATION**

The FPA continually monitors the R3000A processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the R3000A main processor.

- The FPA performs three types of operations:
- Loads and Stores
  - Moves
  - Two- and three-register floating-point operations

**Load, Store, and Move Operations**

Load, Store, and Move operations move data between memory or the R3000A Processor registers and the R3010A FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

**Floating-Point Operations**

The FPA supports the following single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

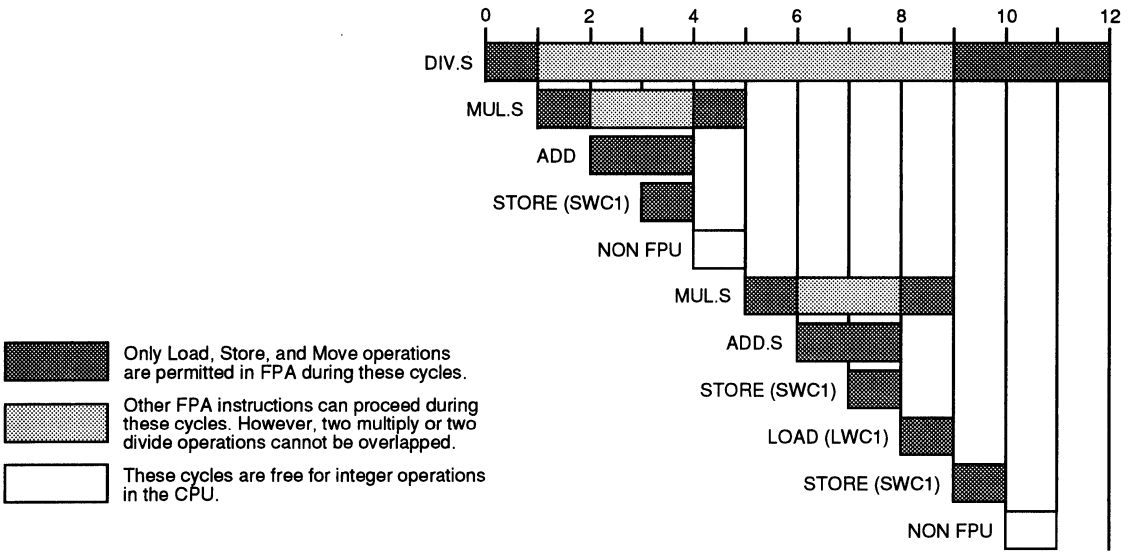


Figure 3. Examples of Overlapping Floating Point Operation

2873 drw 03

**Exceptions**

The R3010A FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

**INSTRUCTION SET OVERVIEW**

All R3010A instructions are 32 bits long and they can be divided into the following groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA core, which is used as CpCond1 in the CPU core for use in coprocessor branch operations.

Table 1 lists the instruction set of the R3010A FPA.

OP	Description	OP	Description
<b>LWC1</b>	<b>Load/Store/Move Instructions</b> Load Word to FPA Store Word from FPA Move Word to FPA Move Word from FPA Move Control word to FPA Move Control word from FPA	<b>ADD.fmt</b>	<b>Computational Instructions</b> Floating-point Add Floating-point Subtract Floating-point Multiply Floating-point Divide Floating-point Absolute value Floating-point Move Floating-point Negate <b>Compare Instructions</b> Floating-point Compare
<b>SWC1</b>		<b>SUB.fmt</b>	
<b>MTC1</b>		<b>MUL.fmt</b>	
<b>MFC1</b>		<b>DIV.fmt</b>	
<b>CTC1</b>		<b>ABS.fmt</b>	
<b>CFC1</b>		<b>MOV.fmt</b>	
	<b>NEG.fmt</b>		
<b>CVT.S.fmt</b>	<b>Conversion Instructions</b> Floating-point Convert to Single FP Floating-point Convert to Double FP Floating-point Convert to fixed-point	<b>C.cond.fmt</b>	
<b>CVT.D.fmt</b>			
<b>CVT.W.fmt</b>			

Table 1. R3010A Instruction Summary

2873 tbl 01

### ID79R3010 PIPELINE ARCHITECTURE

The R3010A FPA provides an instruction pipeline that parallels that of the R3000A processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the 3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single R3010A instruction consists of six primary steps:

- 1) **IF**—Instruction Fetch. The main processor calculates the instruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
- 2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the instruction on the bus to determine if it is an instruction for the FPA.
- 3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.

4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.

5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.

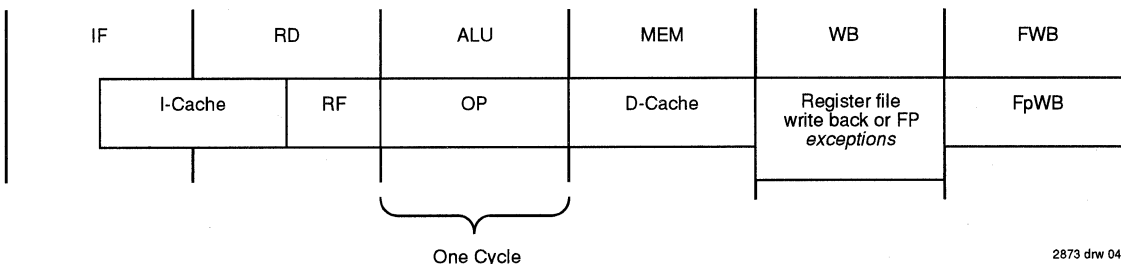
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the R3000A main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

The R3010A uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

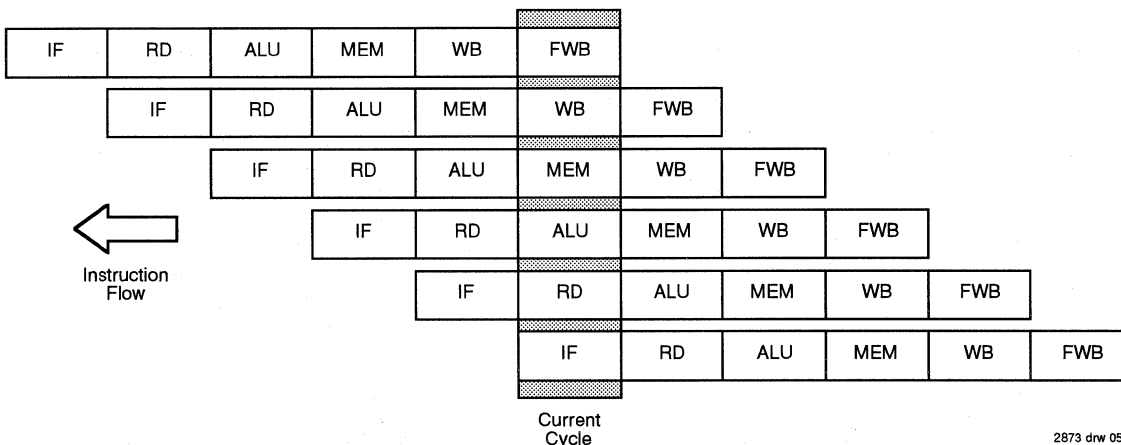
This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

### INSTRUCTION EXECUTION



2873 drw 04

Figure 4. R3010A Instruction Summary



2873 drw 05

Figure 5. R3010A Instruction Pipeline



Integrated Device Technology, Inc.

# BiCameral™ CacheRAM™ 288K (16K x 9 x 2) FOR RISC CACHES

PRELIMINARY  
IDT71B229S

### FEATURES:

- Supports the R3000, R3500 and R3001 to 40MHz
- BiCameral organization:
  - Split instruction/data cache support
  - No bank-switching timing contention
- Single address bus
- Single data bus
- Separate write enable and output enable for each bank
- Standard read and write control interface
- Internal address latches
- 32-pin 300 mil SOJ package

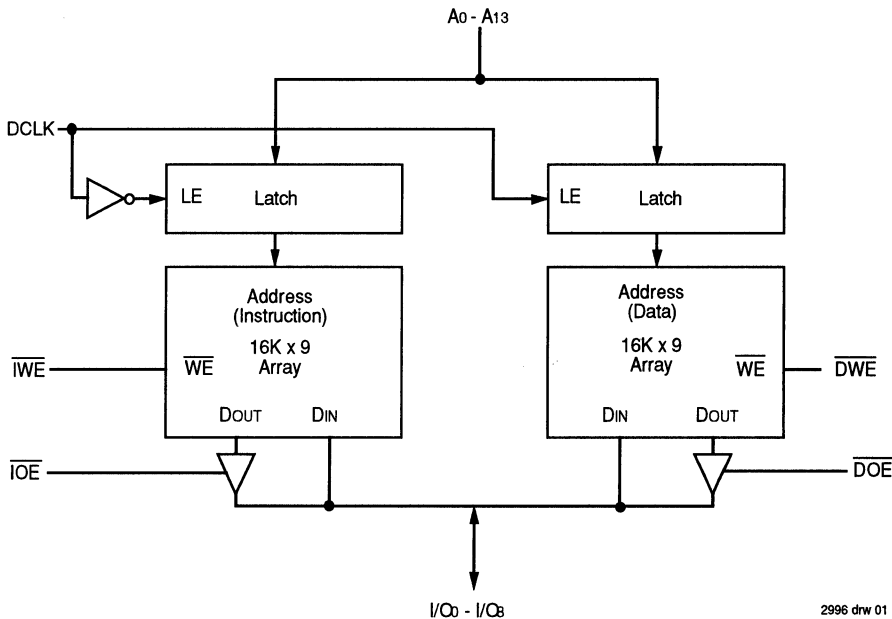
### DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT 79R3000 microprocessor. A complete 128KByte cache for the R3000 or the R3500 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system), while an R3001 cache can be built with five to six parts. CPU clock frequencies up to 40MHz are supported. The small 300 mil package allows a 128KByte cache to fit in a circuit board area of approximately two square inches.

Internal address latches eliminate the need for external latches. The BiCameral (two bank) organization reduces the number of devices required to support the R3000's split-cache architecture and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 clock speeds, simplifying R3000 cache design.

Made with BiCMOS, IDT's advanced high-speed process, the IDT71B229 provides dense caches in low board space while consuming minimum power.

### FUNCTIONAL BLOCK DIAGRAM



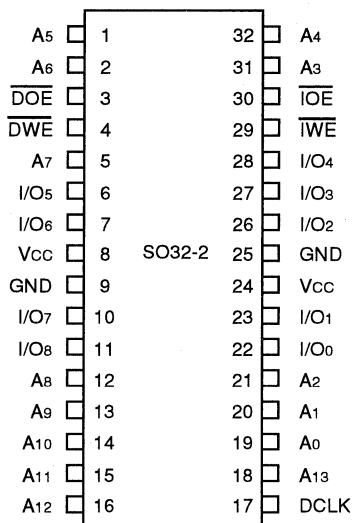
6

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COMMERCIAL TEMPERATURE RANGE

MARCH 1994

## PIN CONFIGURATIONS

SOJ  
TOP VIEW

2996 drw 02

## TRUTH TABLE 1

IOE	IWE	DOE	DWE	I/O(0:8)	Function
H	H	L	H	DATA OUT	Read D Bank data
H	H	H	L	DATA IN, HIGH-Z	Write data to D Bank
L	H	H	H	DATA OUT	Read I Bank data
H	L	H	H	DATA IN, HIGH-Z	Write data to I Bank
H	H	H	H	High-Z	No Activity
L	L	X	X	High-Z	Not Allowed
L	X	L	X	High-Z	Not Allowed
L	X	X	L	High-Z	Not Allowed
X	L	L	X	High-Z	Not Allowed
X	L	X	L	High-Z	Not Allowed
X	X	L	L	High-Z	Not Allowed

2996 tbl 01

TRUTH TABLE 2<sup>(1)</sup>

DCLK	I Address Latch	D Address Latch
L	Transparent	Latched
H	Latched	Transparent

## NOTE:

2996 tbl 02

1. L = Low, H = High, X = Don't Care and High-Z = High Impedance

**PIN DESCRIPTION**

Name	Description
DCLK	DCLK, when high, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a high input on DCLK. Taking DCLK low freezes data in the D bank's address latch and allows addresses to flow through the I bank's address latch.
$\overline{IOE}$	I Output Enable enables the data outputs from the I bank onto the data input/output pins. $\overline{IOE}$ must not be asserted simultaneously with the $\overline{DOE}$ , DWE or IWE pins.
$\overline{DOE}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{DOE}$ must not be asserted simultaneously with the $\overline{IOE}$ , IWE or DWE pins.
IWE	I Write Enable, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither DOE nor IOE should be enabled during a write operation.
DWE	D Write Enable is an input which is taken low to gate data from the input/output pins onto the RAM at the address being output from the D bank address latch. Neither DOE or IOE should be asserted during a write operation.
Addr(0:13)	The fourteen address inputs are used to access any of the 16,384 locations in either the D or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O0:8	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{IOE}$ , IWE, $\overline{DOE}$ and DWE pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{IOE}$ , IWE, $\overline{DOE}$ and DWE are all inactive, the input/output pins are floated in a high-impedance state.

2996 tbi 03



**CAPACITANCE** (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1,2)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
COUT	Output Capacitance	VOUT = 3dV	7	pF

- NOTES:** 2996 tbi 04
- This parameter is determined by device characterization, but is not production tested.
  - Capacitance is measured between 0V and 3V during switching.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

- NOTE:** 2996 tbi 05
- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

- NOTES:** 2996 tbi 06
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  - VIN must not exceed VCC+0.5V.

**DC ELECTRICAL CHARACTERISTICS**<sup>(1, 2)</sup> ( $V_{CC} = 5.0V \pm 5\%$ )

Symbol	Parameter	71B229S12 Com'l.	71B229S16 Com'l.	71B229S22 Com'l.	71B229S28 Com'l.	Unit	
I <sub>CC1</sub>	Operating Power Supply Current Outputs Open, $V_{CC} = \text{Max.}$ , $f = 0$	145	145	145	145	mA	
I <sub>CC2</sub>	Dynamic Operating Current Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{\text{MAX}}$	$WE \leq V_{IL}$	250	230	200	190	mA
		$WE \geq V_{IH}$	200	190	180	170	mA

**NOTES:**

2996 tbl 07

- All values are maximum guaranteed values.
- $f_{\text{MAX}} = 1/t_{\text{CYC}}$ , all Address input pins are cycling at  $f_{\text{MAX}}$ . For Reads and Writes both ports are cycling at  $f_{\text{MAX}}$ .  
 $f = 0$  means no Address inputs change.

**DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE** ( $V_{CC} = 5.0V \pm 5\%$ )

Symbol	Parameter	Test Condition	IDT71B229S		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	$V_{CC} = \text{Max.}$ , $V_{IN} = \text{GND to } V_{CC}$	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$V_{CC} = \text{Max.}$ , $V_{OUT} = \text{GND to } V_{CC}$	—	5	μA
V <sub>OL</sub>	Output Low Voltage	$I_{OL} = 8\text{mA}$ , $V_{CC} = \text{Min.}$	—	0.4	V
V <sub>OH</sub>	Output High Voltage	$I_{OH} = -4\text{mA}$ , $V_{CC} = \text{Min.}$	2.4	—	V

2996 tbl 08

**ACCESS TIME AND CLOCK FREQUENCY EQUIVALENTS**

R3000/1 Clock Frequency	71B229 Access Time
40 MHz	12 ns
33 MHz	16 ns
25 MHz	22 ns
20 MHz	28 ns

2996 tbl 09

**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2996 tbl 11

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5V ± 5%

2996 tbl 10

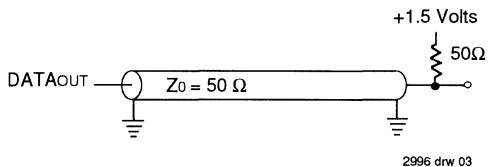
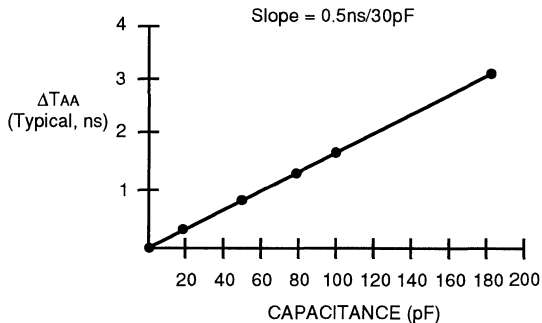
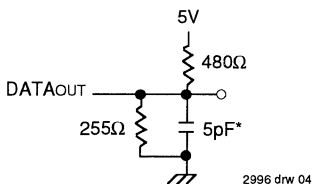


Figure 1. AC Test Load



2996 drw 05

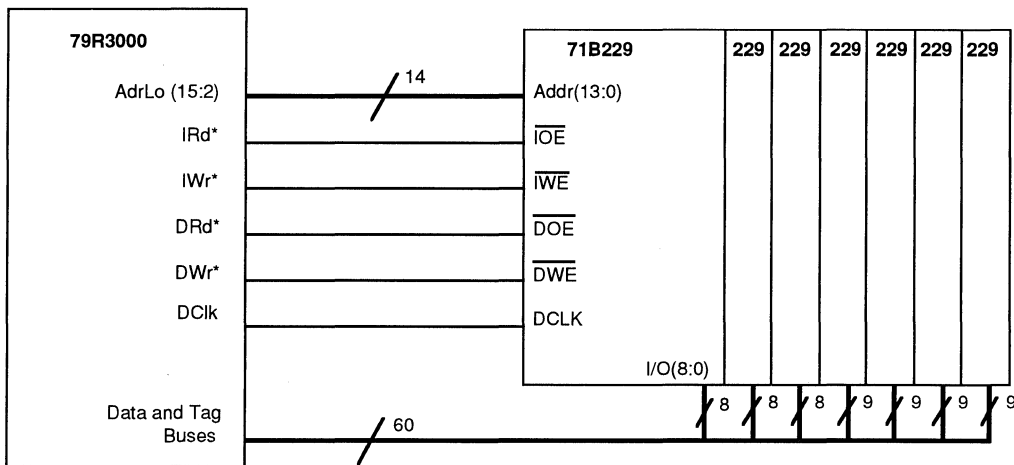
Figure 3. Lumped Capacitive Load, Typical Derating Curve



\*Includes scope and jig.

Figure 2. AC Test Load (for tolZ & toHz)

6



2996 drw 06

**NOTE:**

1. Loading of the IRd, IWr, DRd and DWr signals should be split evenly between the pair of R3000 pins dedicated to each of these functions.

Figure 2. Example of Cache Memory System Block Diagram



**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ )

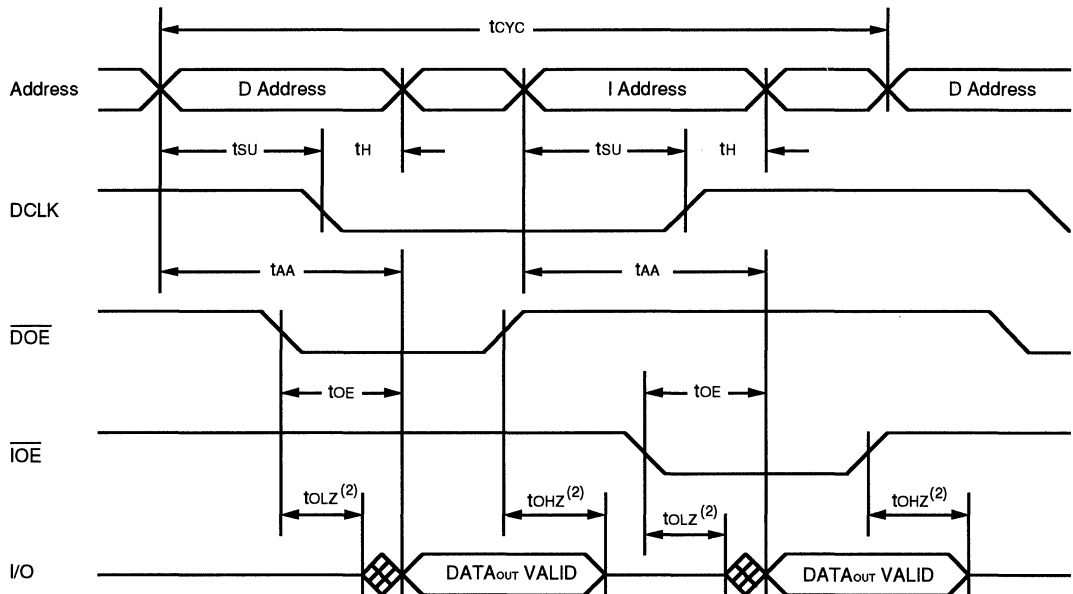
Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>CYC</sub>	Read Cycle Time <sup>(1)</sup>	25	—	30	—	40	—	50	—	ns
t <sub>SU</sub>	Address Setup Time	4	—	4	—	5	—	5	—	ns
t <sub>H</sub>	Address Hold Time	3	—	3	—	4	—	6	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	16	—	22	—	28	ns
t <sub>OE</sub>	Output Enable Time	—	5	—	7	—	10	—	13	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Disable to Output in High-Z	2	5	2	6	2	8	2	10	ns

**NOTES:**

2996 tbl 12

1. One cycle includes both a D bank read or write and an I bank read or write.
2. This parameter is guaranteed with the AC test load (Figure 2) due to device characterization, but is not production tested.

**TIMING WAVEFORM OF READ CYCLES<sup>(1)</sup>**



2996 drw 07

**NOTES:**

1. DWE and TWE must be high during read cycles.
2. The transition is measured  $\pm 200mV$  from steady state.

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ )

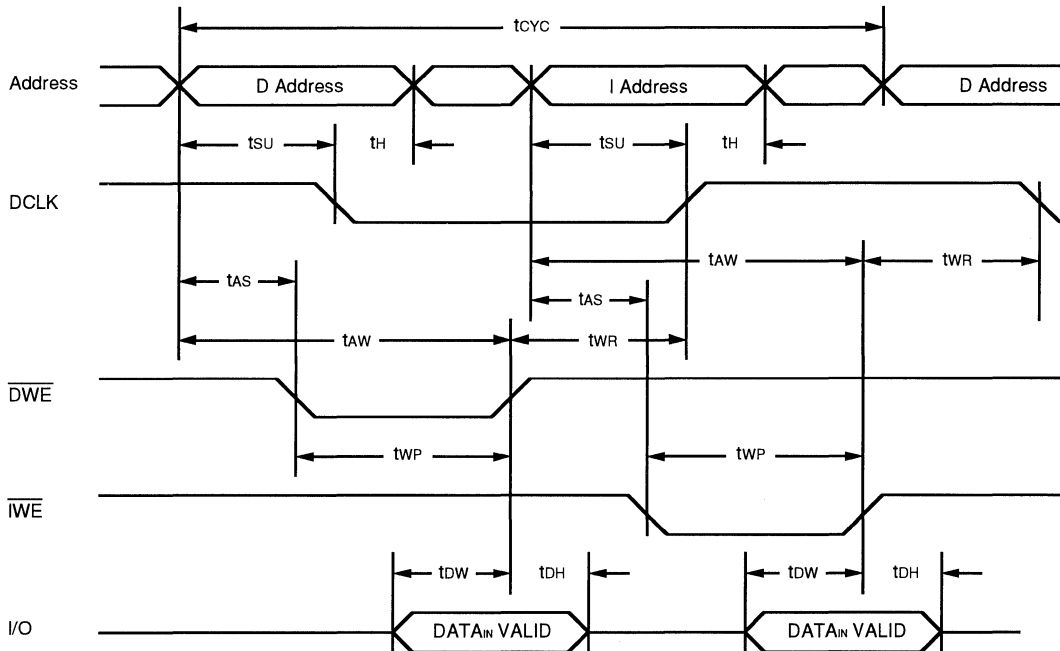
Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Cycle</b>										
t <sub>CYC</sub>	Write Cycle Time <sup>(1)</sup>	25	—	30	—	40	—	50	—	ns
t <sub>SU</sub>	Address Setup Time	4	—	4	—	5	—	5	—	ns
t <sub>H</sub>	Address Hold Time	3	—	3	—	4	—	6	—	ns
t <sub>AW</sub>	Address to End of Write	10	—	13	—	16	—	20	—	ns
t <sub>AS</sub>	Address to Start of Write	0	—	0	—	0	—	0	—	ns
t <sub>WR</sub>	Write Recovery Time	-0.5	—	-0.5	—	-0.5	—	-0.5	—	ns
t <sub>WP</sub>	Write Pulse Width	10	—	13	—	16	—	20	—	ns
t <sub>DW</sub>	Data to Write Time Overlap	5	—	6	—	7	—	8	—	ns
t <sub>DH</sub>	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns

**NOTE:**

1. One cycle includes both a D bank read or write and an I bank read or write.

2996 tbl 13

**TIMING WAVEFORM OF WRITE CYCLES<sup>(1, 2)</sup>**

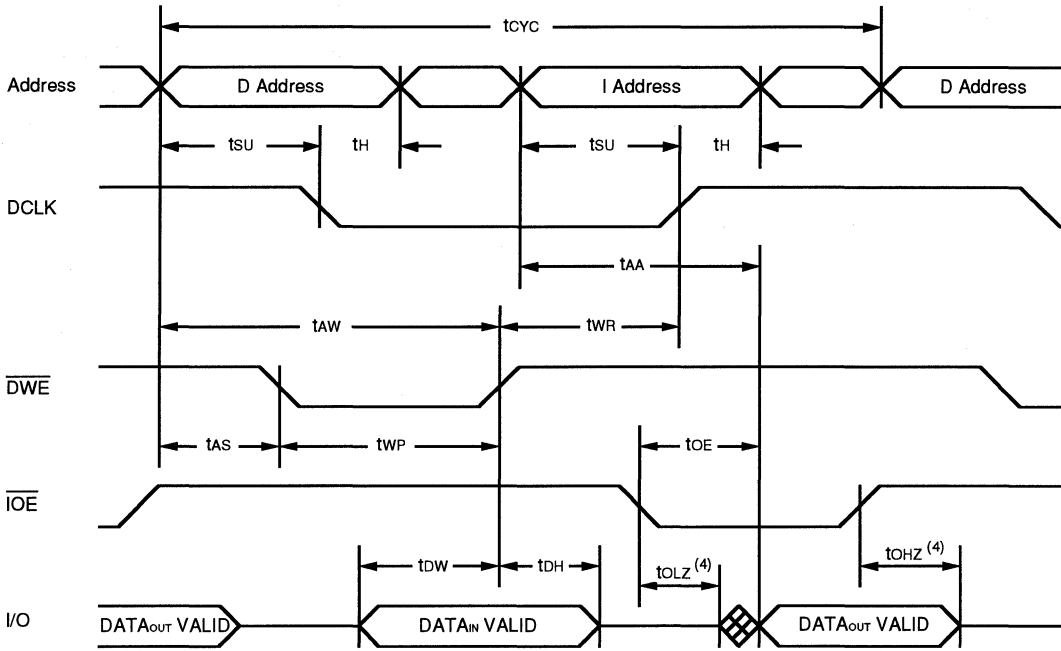


**NOTES:**

1.  $\overline{DOE}$  and  $\overline{TOE}$  are HIGH during write cycles.
2.  $\overline{DWE}$  must be HIGH or DCLK must be low during all address transitions. Likewise,  $\overline{IWE}$  or DCLK must be HIGH during all address transitions.

2996 drw 08

**TIMING WAVEFORM OF MIXED READ AND WRITE CYCLES(1, 2, 3)**



2996 drw 09

**NOTES:**

1.  $\overline{DOE}$  and  $\overline{IOE}$  are HIGH during write cycles.
2.  $\overline{DWE}$  must be HIGH or DCLK must be low during all address transitions. Likewise,  $\overline{IWE}$  or DCLK must be HIGH during all address transitions.
3.  $\overline{DWE}$  and  $\overline{IWE}$  must be HIGH during read cycles.
4. The transition is measured  $\pm 200mV$  from steady state.

**ORDERING INFORMATION**

IDT	71B229	S	XX	X	
	Device Type	Power	Speed	Package	
				Y	300-mil SOJ (SO32-2)
				12 16 22 28	} Access Time in nanoseconds

2996 drw 10



Integrated Device Technology, Inc.

# RISC CPU WRITE BUFFER

IDT79R3020

## FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R3000 RISC CPU processor
- Allows for write operations by the RISC CPU processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CMOS technology
- Pin, functionally and software compatible with the MIPS Computer Systems R2020 Write Buffer
- Speeds from 16.7 to 40MHz
- Also works with Intel i486™ for Writeback secondary cache

## DESCRIPTION:

The IDT79R3020 Write Buffer enhances the performance of IDT79R3000 systems by allowing the processor to perform write operations during Run cycles instead of resorting to time-consuming stall cycles. Each IDT79R3020 device handles an 8-bit slice of address, and a 9-bit slice of data (one parity bit per byte); thus, four IDT79R3020s provide 4-deep buffering of 32 bits of address and 36 bits of data and parity. Figure 1 illustrates the functional position of the Write Buffer in an IDT79R3000 system.

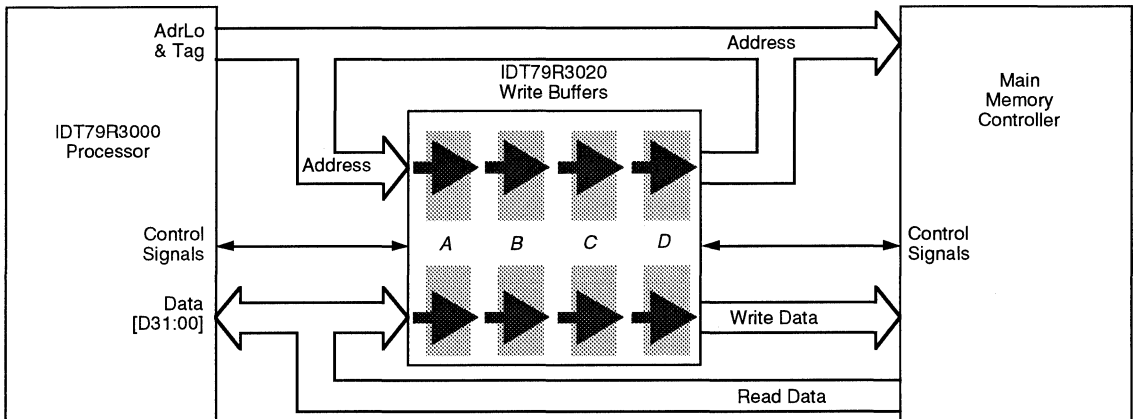
Whenever the processor performs a write operation, the Write Buffer captures the output data and its address (including the access type bits). The Write Buffer can hold up to four data-address sets while it waits to pass the data on to main memory. Transfers from the processor to the write buffers occur synchronously at the cycle rate of the processor and the write buffer signals the processor if it is unable to accept data. The write buffer also provides a set of handshake signals to communicate with a main memory controller and coordinate the transfer of write data to main memory.

The sections that follow describe these IDT79R3020 Write Buffer interfaces:

- the processor-Write Buffer interface
- the Write Buffer-main memory interface
- a miscellaneous, Write Buffer-board control interface.

6

## WRITE BUFFER



5002 drw 01

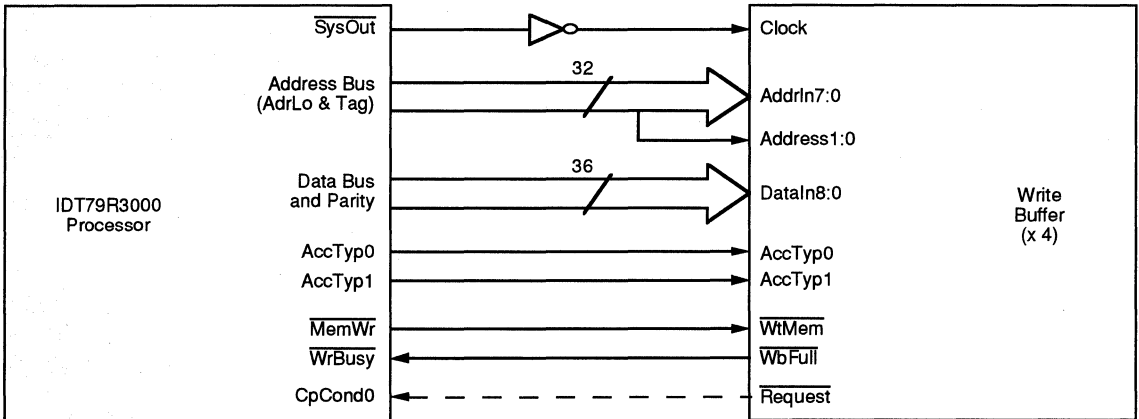
Figure 1. The IDT79R3020 Write Buffer in an IDT79R3000 System

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 i486 is a trademark of Intel Corporation.

## WRITE BUFFER - IDT79R3000 PROCESSOR INTERFACE

Figure 2 shows the signals comprising the Write Buffer interface to the IDT79R3000 (all descriptions assume that four IDT79R3020 Write Buffers are used to implement a 32-bit, buffered interface). The *AdrLo* bus and *Tag* bus bits from the processor are both connected to the Write Buffer to form a 32-

bit physical address that is captured by the buffers. Thirty-two bits of data, four bits of parity, and two access type bits are also captured by the Write Buffer. The paragraphs that follow describe the Write Buffer-processor interface signals and the timing of processor-to-Write Buffer data transfers.



5002 drw 02

Figure 2. Write Buffer — IDT79R3000 Processor Interface

## WRITE BUFFER-PROCESSOR INTERFACE SIGNALS

### Clock

An inverted version of the R3000s *SysOut* signal from the R3000 processor that synchronizes data transfers. The Write Buffer uses the trailing edge of *Clock* to latch the contents of the *AdrLo* bus and uses the leading *Clock* edge to latch the contents of the Data and *Tag* buses.

### DataIn8:0

Nine input data lines from the IDT79R3000 processor's Data bus (eight bits of data and one bit of parity).

### AddrIn7:0

Eight input address lines from the IDT79R3000 processor. The address lines are taken from the *AdrLo* and *Tag* buses.

### Address1:0

The two least significant address bits from the IDT79R3000 processor. These two address bits must be connected to all four Write Buffers and are used in conjunction with the access type (*AccTyp1:0*) signals, the *Position1:0* signals, and the *BigEndian* signal to determine which byte(s) in a word are being written into a particular Write Buffer.

### AccTypIn1:0

The access type signals from the IDT79R3000 processor specifying the size of a data access: word, tri-byte, half-word, or byte.

### WtMem

This input is connected to the *MemWr* signal from the IDT79R3000 processor that is asserted whenever the processor is performing a store (write) operation.

### Request

The primary purpose of this signal is to request access to memory and is described later when the Write Buffer-Main Memory Interface is discussed. The *Request* signal can also be connected to the *CpCond0* input of the IDT79R3000 and can then be tested by software to determine if there is any data in the Write Buffer. Since *Request* is deasserted if there is no data in the Write Buffer, software can determine if a previous write operation (for example, to an I/O device) has been completed before initiating a read or read status operation from that device.

### WbFull

The Write Buffer asserts this signal to the IDT79R3000s *WrBusy* input whenever it cannot accept any more data; that is, when the current write will fill the buffer or the buffer has all address-data pairs occupied. The IDT79R3000 processor performs a write-busy stall if it needs to store data while the *WbFull*/*WrBusy* signal is asserted.

### Data & Address Connections

Figure 3 illustrates how four Write Buffers are connected to the address and data outputs of the IDT79R3000 processor.

**Address Inputs**

Each Write Buffer device has eight address inputs (AdrIn7:0). The four low-order bits (AdrIn3:0) are clocked into the device on the trailing edge of the Clock signal and are taken from the IDT79R3000s AdrLo bus. The four high-order bits (AdrIn7:4) are clocked into the device on the rising edge of the Clock signal and are taken from the IDT79R3000s Tag bus.

Each device also has separate inputs (Address1, Address0) for the two low-order bits from the AdrLo bus. These bits must be input to each device since they comprise the byte pointer. Note in Figure 3 that the two low-order AdrIn inputs (AdrIn1:0) to Write Buffer device 0 are connected to ground since the Address1, Address0 inputs already supply these bits to the device.

**Data Inputs**

Each Write Buffer device has nine data inputs that are clocked into the device on the leading edge of the Clock signal and are taken from the IDT79R3000s Data bus. In Figure 3, each device captures eight bits of data and one bit of parity. Also note that the data bits assigned to each device correspond to the address bits connected to the device. This arrangement is required since data selection is dependent on a combination of the AccType signals and the two low order address bits. The arrangement also simplifies system utilization of the "Read Error Address" feature described later.

The *Position1* and *Position0* signals shown in Figure 3 specify the nibble position within a halfword that each write buffer device comprises.

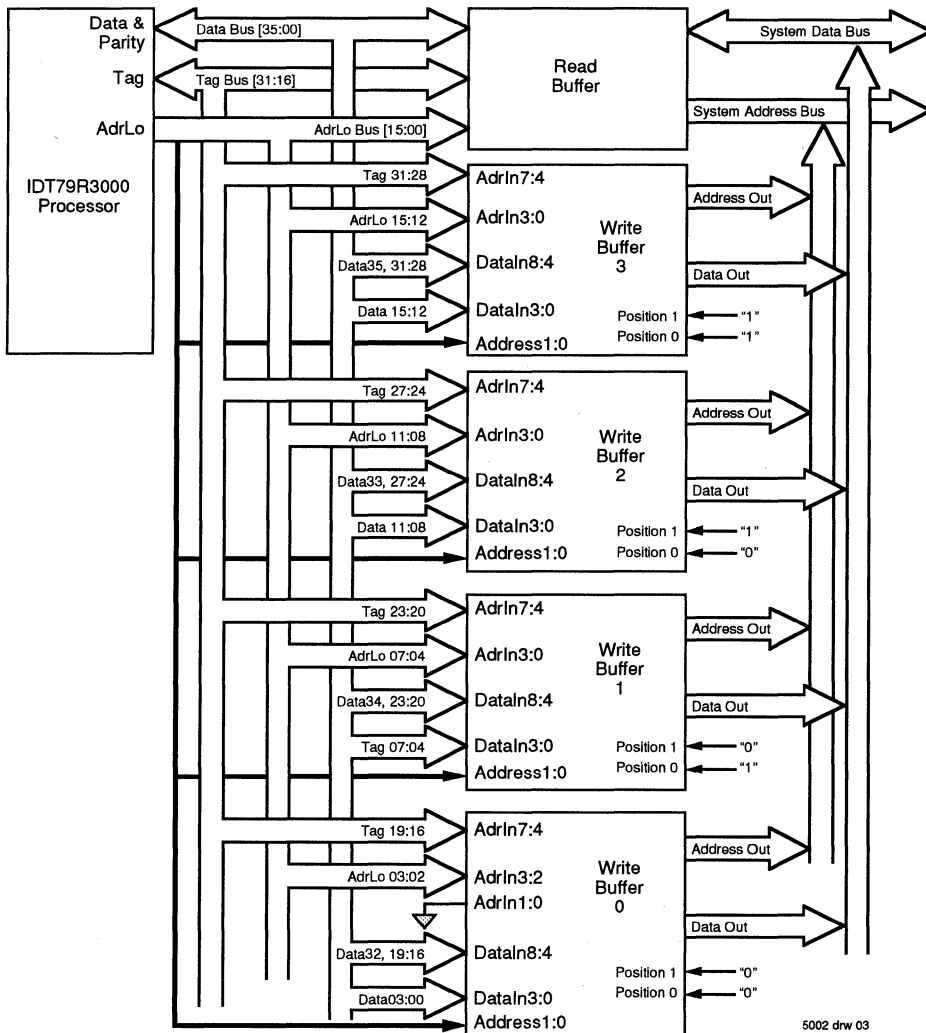
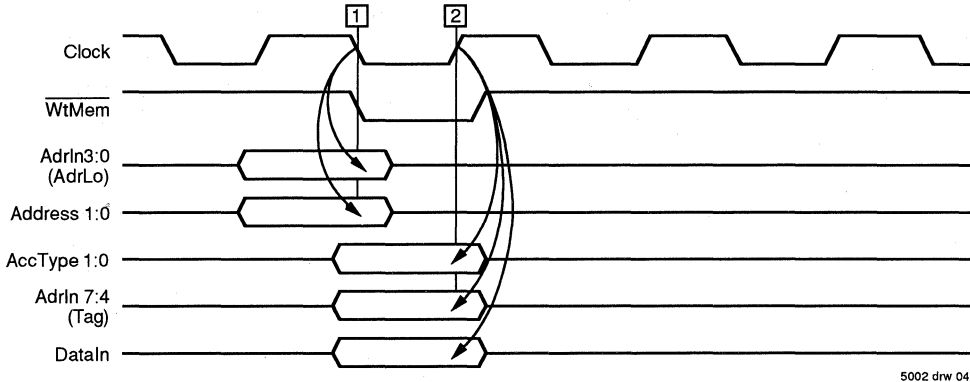


Figure 3. Write Buffer Data and Address Line Connections

**Write Buffer - Processor Timing**

Transfers between the processor and the Write Buffers occur synchronously: the Clock signal from the processor is input to the Write Buffers and used to clock the address and data information into the Write Buffers' latches. Figure 4 illustrates the timing for the processor-Write Buffer interface.

When the  $\overline{WrtMem}$  signal is asserted, the low-order address bits, and the Address 1:0 inputs, are latched on the trailing edge of the Clock signal (1). The rising edge of Clock (2) is used to latch the high-order address bits, the access type inputs and the contents of the data bus.



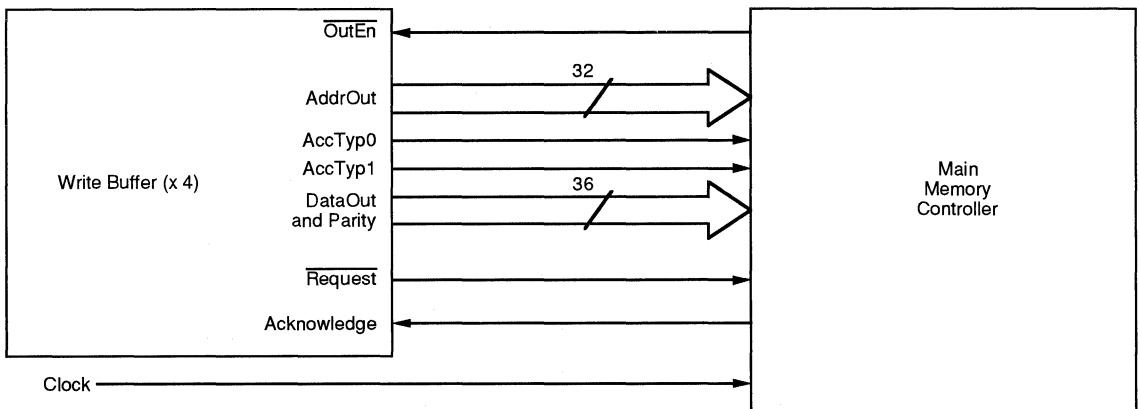
5002 drw 04

Figure 4. Processor — Write Buffer Interface Timing

**WRITE BUFFER - MAIN MEMORY INTERFACE**

Figure 5 shows the signals comprising the Write Buffer interface to main memory. This interface is essentially decoupled from the Write Buffer-processor interface: although some synchronization of the memory interface signals and the

Clock signal is required, the handshaking signals in this interface have no direct connection to the operation of the Write Buffer-processor interface.



5002 drw 05

Figure 5. Write Buffer — Main Memory Interface





by the preceding rule.

The Write Buffers present address-data pairs to the main memory controller in the sequence in which they were received from the processor except in the case of gathered data, where bytes or half words can be collected and written to main memory in a single write operation. If the address-data pair buffer is scheduled to be output, then gathering is inhibited and the buffer contents are presented to the main memory controller. Subsequent writes are then placed in another buffer. No reliance should be placed in any aspect of gathering (except that it only involves sequential writes to the same word address) as it is not readily deterministic. Non-sequential writes to the same word address are not gathered.

Note that gathering can require that two main memory controller references be used to empty a single Write Buffer entry. For example, this can occur if Bytes 0 and 3 of a word are sequentially written. Where order in writing is important, such as in I/O controllers, software should avoid sequential accesses to the same word. In cases where write-read access ordering is important but reading of the write location is not desired, such as during I/O, then a write followed by a write to a dummy location followed by a read of the dummy location will insure the first write has occurred before continuing. Alternatively, the Request signal can be tested to determine that the Write Buffer is empty.

## CONFIGURATION LOGIC CONNECTIONS

Because of their byte gathering capability, each buffer device internally maintains a record of each valid byte in an address/data pair. To do this, each device must have a way of determining which data bits within a word it is handling. The following signals determine how the write buffers handle data that is written to the devices:

- **Position 1, Position 0** - these signals (in conjunction with Big Endian) determine how each Write Buffer decodes the Address 1/0 and AccType 1/0 to determine if it should store the data inputs. Refer to Figure 3 for an illustration of how data bits are assigned to Write Buffer devices based on their *position*.
- **Big Endian** - When asserted, byte 0 is the leftmost, most significant byte (big-endian); when deasserted, byte 0 is the rightmost, least-significant byte (little-endian).
- **Address 1, Address 0** - these signals (taken from the AdrLo bus) must be connected to all buffer devices since they determine which byte within a word is being accessed.
- **AccType 1, AccType 0** - these inputs signals specify the data size of a write operation as shown in Table 1.

Table 1 shows how these signals operate to specify how bytes are saved within the Write Buffers.

Access Type 1 0	Address 1 0	Bytes Accessed							
		Big-Endian				Little-Endian			
1 1 (word)	0 0	0	1	2	3	3	2	1	0
1 0 (triple-byte)	0 0	0	1	2			2	1	0
	0 1		1	2	3	3	2	1	
0 1 (halfword)	0 0	0	1					1	0
	1 0			2	3	3	2		
0 0 (byte)	0 0	0							0
	0 1		1					1	
	1 0			2			2		
	1 1				3	3			

5002 drw 07

Table 1. Byte Specifications for Write Operations

The lower two address bits of the device in position zero (as determined by the two POSITION inputs) are inhibited; that is, they are not stored directly as they are output on the AdrLo bus. Instead, on output, the lower two address bits are generated from the indication of the positions of the valid data bytes as determined by above table.

## MATCHOUT/MATCHIN LOGIC AND READ CONFLICTS

Whenever the processor references main memory (either a write or a read reference), the Write Buffers compare the

word address from the CPU with the word addresses stored in the buffers. If any word address matches, the buffers assert signals that can be used by the main memory controller to ensure that the Write Buffer is emptied before the read access with the conflicting address has been performed.

Figure 7 illustrates the Write Buffer signals involved in address comparison logic. Each write buffer provides four output signals (MatchOut A, B, C, and D) which correspond to the four buffer ranks (A, B, C, D) in each device as shown in Figure 1. These MatchOut signals can be externally NANDed as shown in Figure 7 to determine if the address being input

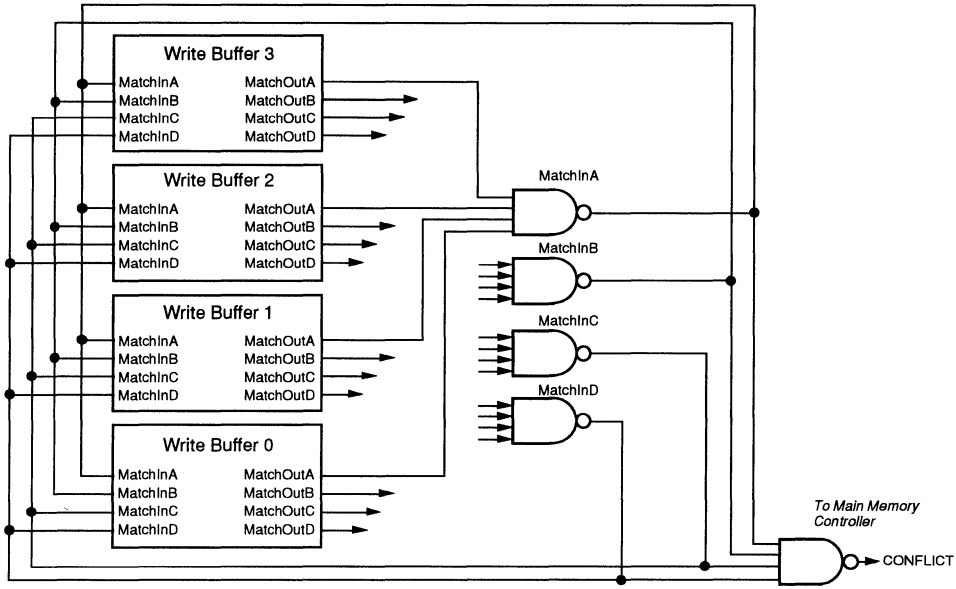


Figure 7. Write Buffer MatchOut/MatchIn Logic

5002 drw 08

matches those in any rank of the Write Buffer.

The outputs of the NAND gates are fed into Write Buffers via the MatchIn A, B, C, and D signals and are used within each device as part of the byte gathering logic. The NAND gate outputs can be NANDed together as shown in Figure 7 with the resultant signal used (in conjunction with the processor's MEMRD signal) to alert the main memory controller logic that there is a pending buffered write that conflicts with a just-issued read. The main memory controller can then delay the read access until the Request signal is deasserted indicating that the Write Buffer has been emptied.

### ERROR ADDRESS LATCH

The write buffer incorporates an internal latch that can be loaded with one of the buffered addresses and subsequently enabled out onto the data lines. This feature can be used by error handling routines to read an address back from the Write Buffer and analyze or recover from certain bus errors. Figure 8 shows the signals involved in operation of this latch.

When the LatchErrAddr signal is asserted, the address currently available to the address outputs of the Write Buffer is latched into the internal latch. This address can then be output on the DataOut lines by asserting the EnErrAdr signal so that the processor can read the address in as data. Refer to the AC specifications for timing parameters of the signals associated with the error address latch.

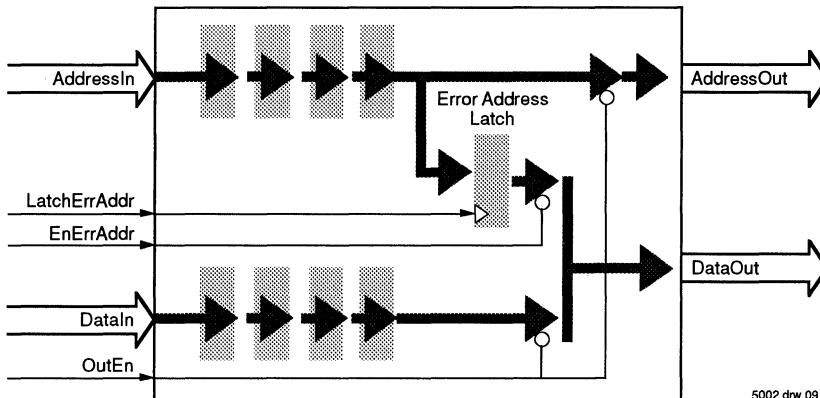


Figure 8. The Write Buffer Error Address Latch

5002 drw 09

**ABSOLUTE MAXIMUM RATINGS<sup>(1, 3)</sup>**

SYMBOL	RATING	COM.	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature <sup>(2)</sup>	-55 to +125	°C
V <sub>IN</sub>	Input Voltage	-0.5 to +7.0	V

**NOTES:**

5002 tbl 01

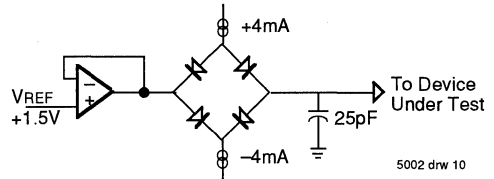
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>IN</sub> minimum = -3.0V for pulse width less than 15ns. V<sub>IN</sub> should not exceed V<sub>CC</sub> + 0.5V.
- Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

GRADE	AMBIENT TEMPERATURE	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0 ± 5%

5002 tbl 02

**OUTPUT LOADING FOR AC TESTING**



5002 drw 10

**DC ELECTRICAL CHARACTERISTICS —**

**COMMERCIAL TEMPERATURE RANGE (T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5.0 V ± 5%)**

SYMBOL	PARAMETER	TEST CONDITIONS	16.67MHz		20.0MHz		25.0MHz		33.33MHz		40MHz		UNIT
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4mA	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	—	2.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>		2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V <sub>IL</sub>	Input LOW Voltage <sup>(2)</sup>		—	0.8	—	0.8	—	0.8	=	0.8	—	0.8	V
C <sub>IN</sub>	Input Capacitance <sup>(3)</sup>		10	—	10	—	10	—	10	—	10	—	pF
C <sub>OUT</sub>	Output Capacitance <sup>(3)</sup>		10	—	10	—	10	—	10	—	10	—	pF
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = Max.	—	50	—	60	—	70	—	80	—	90	mA
I <sub>IH</sub>	Input HIGH Leakage	V <sub>IH</sub> = V <sub>CC</sub>	—	10	—	10	—	10	—	10	—	10	µA
I <sub>IL</sub>	Input LOW Leakage	V <sub>IL</sub> = GND	-10	—	-10	—	-10	—	-10	—	-10	—	µA
I <sub>OZ</sub>	Output Tri-state Leakage	V <sub>OH</sub> = 2.4V, V <sub>OL</sub> = 0.5V	-40	40	-40	40	-40	40	-40	40	-40	40	µA

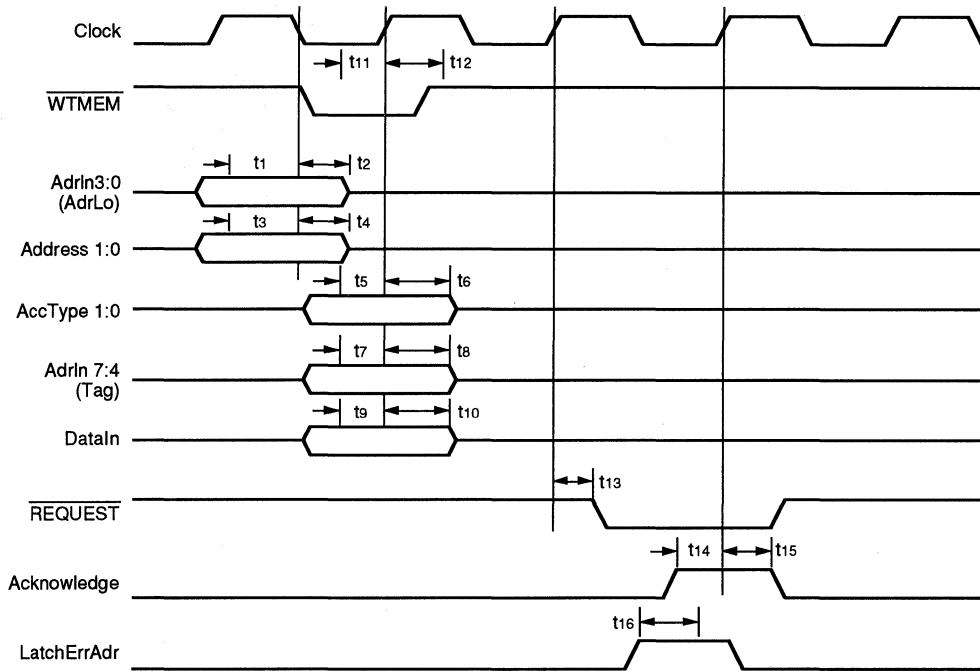
**NOTES:**

5002 tbl 03

- V<sub>IH</sub> should be held above V<sub>CC</sub> + 0.5V.
- V<sub>IL</sub> Min. = -3.0V for pulse width less than 15ns. V<sub>IL</sub> should not fall below -0.5V for longer periods.
- Tested only initially, and after design changes which may affect capacitance.

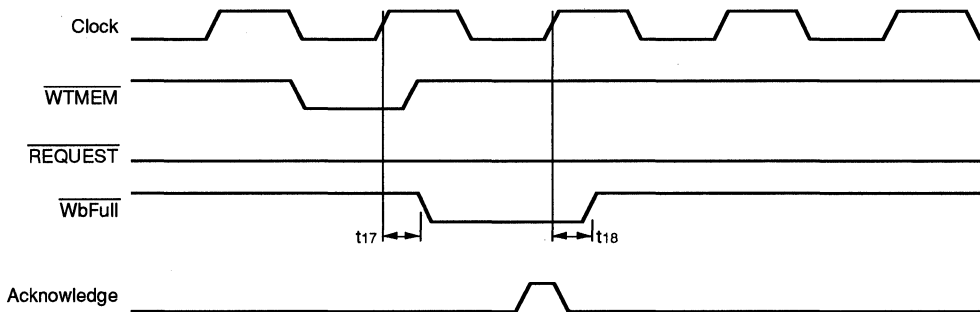
**AC ELECTRICAL CHARACTERISTICS —**  
**COMMERCIAL TEMPERATURE RANGE** (TA = 0°C to +70°C, VCC = +5.0V ± 5%)

SYMBOL	PARAMETER	16.67MHz		20.0MHz		25.0MHz		33.33MHz		40MHz		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	AddrIn (3:0) to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t2	AddrIn (3:0) from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t3	Address 1:0 to Clock falling setup	8	—	7	—	6	—	3	—	3	—	ns
t4	Address 1:0 from Clock falling hold	4	—	4	—	4	—	3	—	3	—	ns
t5	Access Type 1:0 to Clock rising setup	7	—	6	—	5	—	4	—	4	—	ns
t6	Access Type 1:0 from Clock rising hold	3	—	3	—	2	—	2	—	2	—	ns
t7	AddrIn (7:4) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t8	AddrIn (7:4) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t9	DataIn (8:0) to Clock rising setup	7	—	5	—	4	—	4	—	4	—	ns
t10	DataIn (8:0) from Clock rising hold	3	—	3	—	2	—	1	—	1	—	ns
t11	WrtMem to Clock rising setup	10	—	8	—	7	—	6	—	6	—	ns
t12	WrtMem from Clock rising hold	6	—	5	—	4	—	3	—	3	—	ns
t13	Request from Clock rising	—	32	—	30	—	22	—	16	—	16	ns
t14	Acknowledge to Clock rising setup	12	—	11	—	6	—	4	—	4	—	ns
t15	Acknowledge from Clock rising hold	7	—	6	—	5	—	3	—	3	—	ns
t16	LatchErrAdr to Acknowledge rising	5	—	5	—	5	—	3	—	3	—	ns
t17	WbFull active from Clock rising	—	21	—	19	—	17	—	9	—	9	ns
t18	WbFull inactive from Clock rising	—	21	—	19	—	11	—	9	—	9	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	2	15	2	15	2	15	2	12	2	12	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	2	15	2	15	2	15	2	12	2	12	ns
t21	MatchOut (ABCD) from Clock rising	—	24	—	22	—	20	—	15	—	12	ns
t22	MatchIn (ABCD) to Clock rising setup	10	—	9	—	8	—	5	—	5	—	ns
t23	MatchIn (ABCD) from Clock rising hold	3	—	3	—	3	—	3	—	3	—	ns
t24	EnErrAdr to Data (error latch) valid	2	15	2	15	2	15	2	15	2	15	ns
t25	EnErrAdr to Data (error latch) tri-state	2	15	2	15	2	15	2	15	2	15	ns
t26	Address/Data out from Clock rising	—	30	—	27	—	24	—	16	—	16	ns
t27	Reset to Clock rising, set-up	10	—	10	—	10	—	8	—	8	—	ns
t28	Reset from Clock rising, hold	3	—	2	—	1	—	1	—	1	—	ns
t29	Reset LOW pulse width	8	—	8	—	8	—	8	—	8	—	cycles
t30	WbFull HIGH from Clock rising (after Reset)	—	22	—	21	—	20	—	11	—	11	ns
t31	Request HIGH from Reset LOW	—	20	—	19	—	18	—	16	—	16	ns
t32	Access TypOut 1:0 from Reset LOW OutEn Asserted	—	28	—	26	—	25	—	23	—	23	ns
t33	MatchOut (ABCD) LOW from Reset LOW	—	21	—	20	—	20	—	15	—	15	ns
t34	Address/Data out tri-state from Reset LOW (OutEn negated)	—	32	—	30	—	27	—	23	—	23	ns
t35	Access TypeOut from Clock rising	—	32	—	30	—	27	—	23	—	23	ns
tcyc	Clock Pulse Width	60	2000	50	2000	40	2000	30	2000	25	2000	ns
tckhigh	Clock HIGH Pulse Width	24	—	20	—	16	—	12	—	10	—	ns
tcklow	Clock LOW Pulse Width	24	—	20	—	16	—	12	—	10	—	ns



5002 drw 11

Figure 9. Write Buffer Timing Specifications



5002 drw 12

Figure 10. WBFULL Signal Timing Specifications

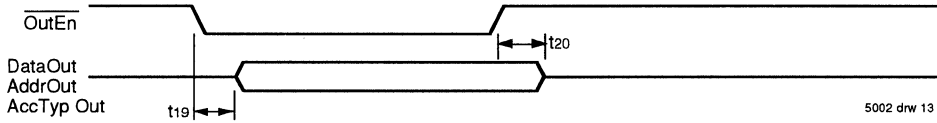


Figure 11.  $\overline{\text{OUTEN}}$  Timing Specifications

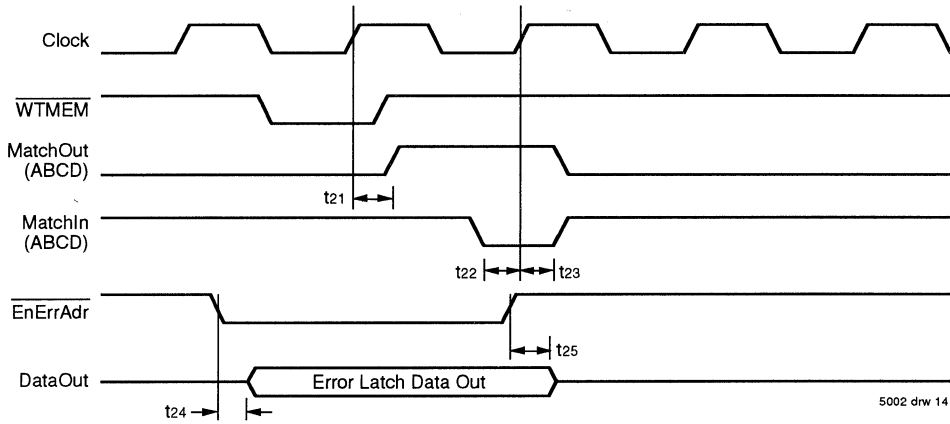


Figure 12. Match and Error Latch Timing Specifications

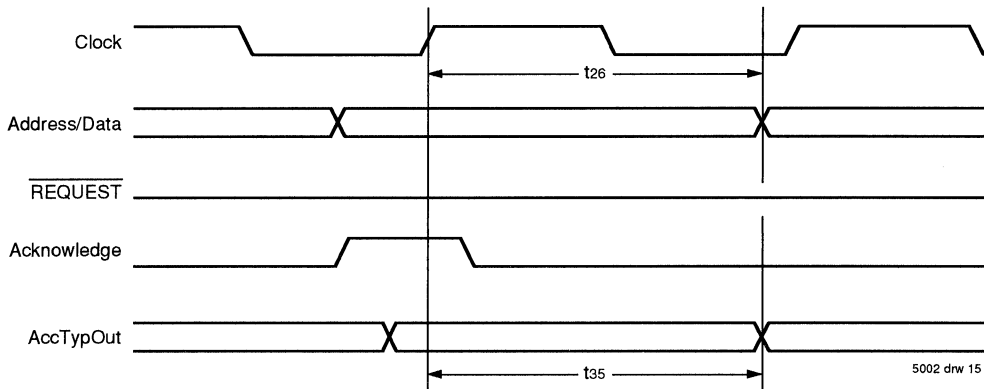


Figure 13. Address/Data Out, Access Type Out

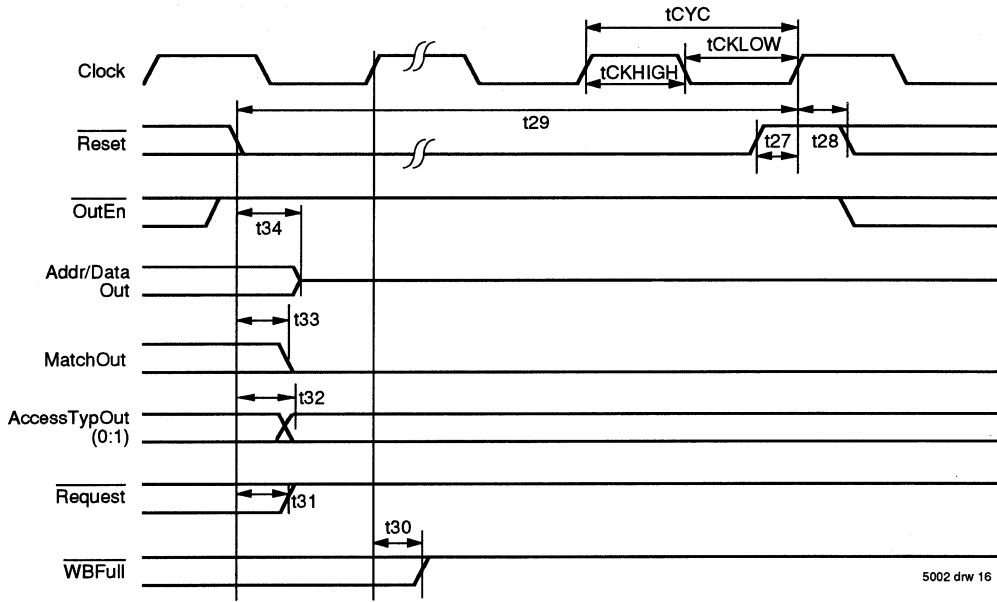


Figure 14. Reset Timing

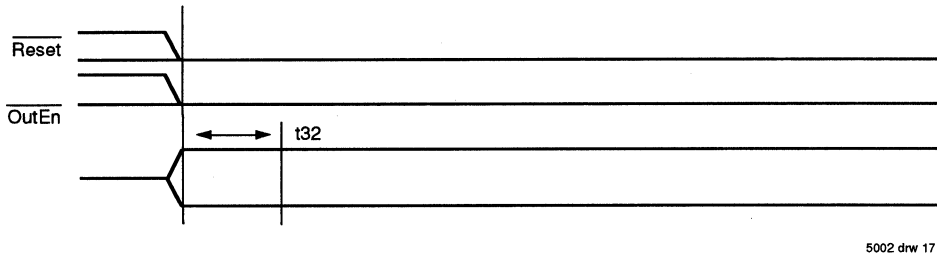


Figure 15. Reset Timing for Access Type Out

**68-PIN CPGA FOR 3020  
PIN GRID ARRAY (CERAMIC) – BOTTOM VIEW**

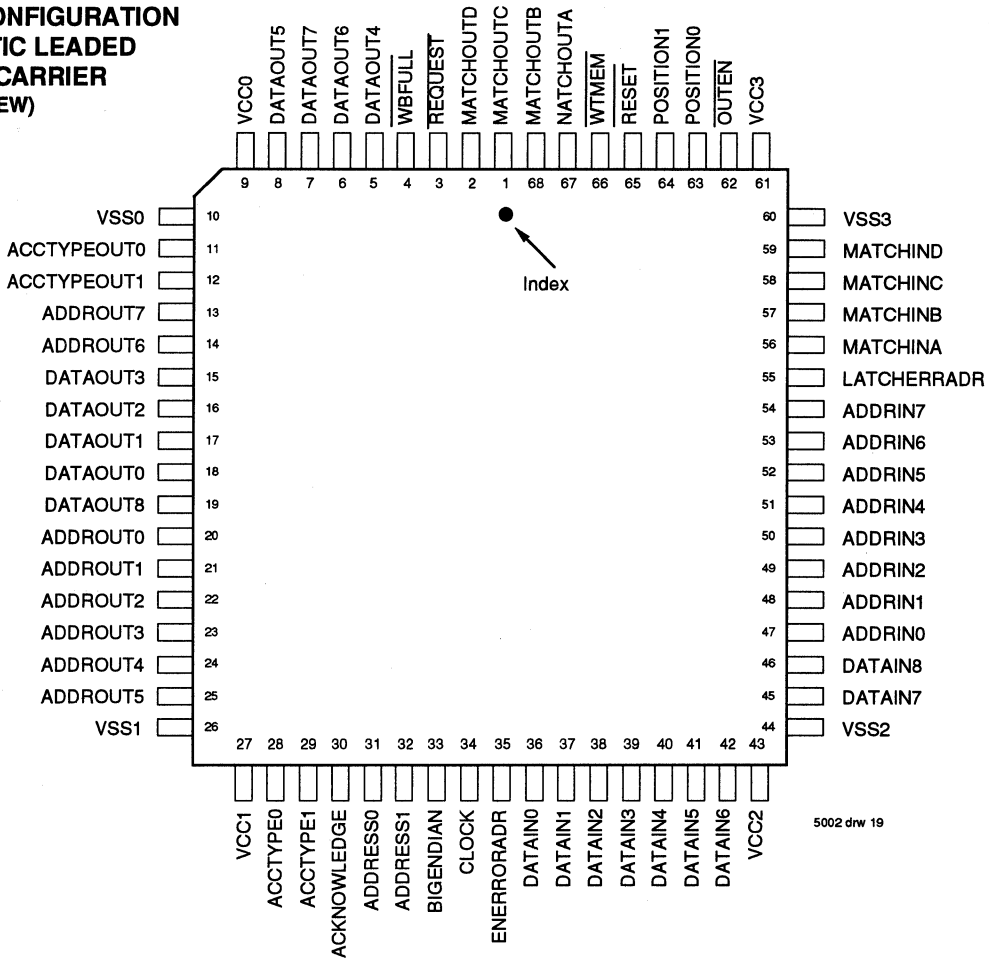
L		ACC-TYP0	AC-KNOWLEDGE	ADD-RESS1	CLOCK	DATA-IN0	DATA-IN2	DATA-IN4	DATA-IN6	VCC2	
K	GND1	VCC1	ACC-TYPE1	ADD-RESS0	$\overline{\text{BIG-ENDIAN}}$	$\overline{\text{EN-ERROR-ADR}}$	DATA-IN1	DATA-IN3	DATA-IN5	GND2	DATA-IN7
J	ADDR-OUT5	ADDR-OUT4								DATA-IN8	ADDR-IN0
H	ADDR-OUT3	ADDR-OUT2								ADDR-IN1	ADDR-IN2
G	ADDR-OUT1	ADDR-OUT0								ADDR-IN3	ADDR-IN4
F	DATA-OUT8	DATA-OUT0								ADDR-IN5	ADDR-IN6
E	DATA-OUT1	DATA-OUT2								ADDR-IN7	LATCH-ERR-ADR
D	DATA-OUT3	ADDR-OUT6								MATCH-INA	MATCH-INB
C	ADDR-OUT7	ACC-TYPE OUT1								MATCH-INC	MATCH-IND
B	ACC-TYPE OUT0	GND0	DATA-OUT7	DATA-OUT4	$\overline{\text{RE-QUEST}}$	MATCH-OUTC	MATCH-OUTA	$\overline{\text{RESET}}$	POSITION0	VCC3	GND3
A		VCC0	DATA-OUT5	DATA-OUT6	$\overline{\text{WB-FULL}}$	MATCH-OUTD	MATCH-OUTB	$\overline{\text{WTMEM}}$	POSITION1	OUTEN	
	1	2	3	4	5	6	7	8	9	10	11

5002 drw 18

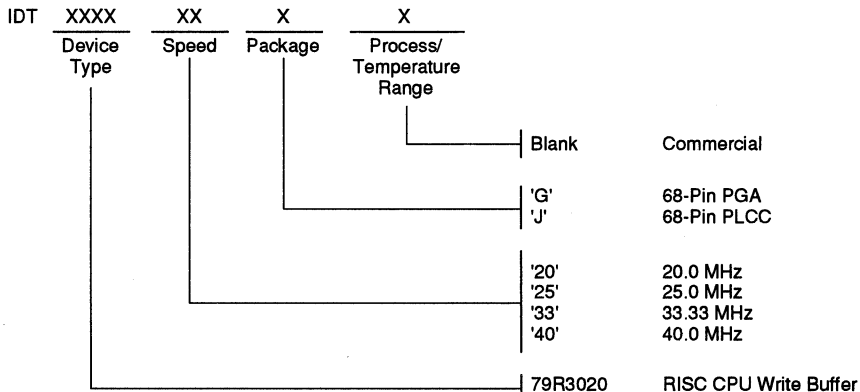
**6**



**PIN CONFIGURATION  
PLASTIC LEADED  
CHIP CARRIER  
(TOP VIEW)**



**ORDERING INFORMATION**





Integrated Device Technology, Inc.

# 16-BIT TRI-PORT BUS EXCHANGER

IDT73720/A

## FEATURES:

- High-speed 16-bit bus exchange for interbus communication in the following environments:
  - Multi-way interleaving memory
  - Multiplexed address and data busses
- Direct interface to R3051 family RISChipSet™
  - R3051™ family of integrated RISController™ CPUs
  - R3721 DRAM controller
- Data path for read and write operations
- Low noise 12mA TTL level outputs
- Bidirectional 3-bus architecture: X, Y, Z
  - One CPU bus: X
  - Two (interleaved or banked) memory busses: Y & Z
  - Each bus can be independently latched
- Byte control on all three busses
- Source terminated outputs for low noise and undershoot control
- 68-pin PLCC and 80-pin PQFP package
- High-performance CMOS technology.

## DESCRIPTION:

The IDT73720/A Bus Exchanger is a high speed 16-bit bus exchange device intended for inter-bus communication in interleaved memory systems and high performance multiplexed address and data busses.

The Bus Exchanger is responsible for interfacing between the CPU A/D bus (CPU address/data bus) and multiple memory data busses.

The 73720/A uses a three bus architecture (X, Y, Z), with control signals suitable for simple transfer between the CPU bus (X) and either memory bus (Y or Z). The Bus Exchanger features independent read and write latches for each memory bus, thus supporting a variety of memory strategies. All three ports support byte enable to independently enable upper and lower bytes.

## FUNCTIONAL BLOCK DIAGRAM

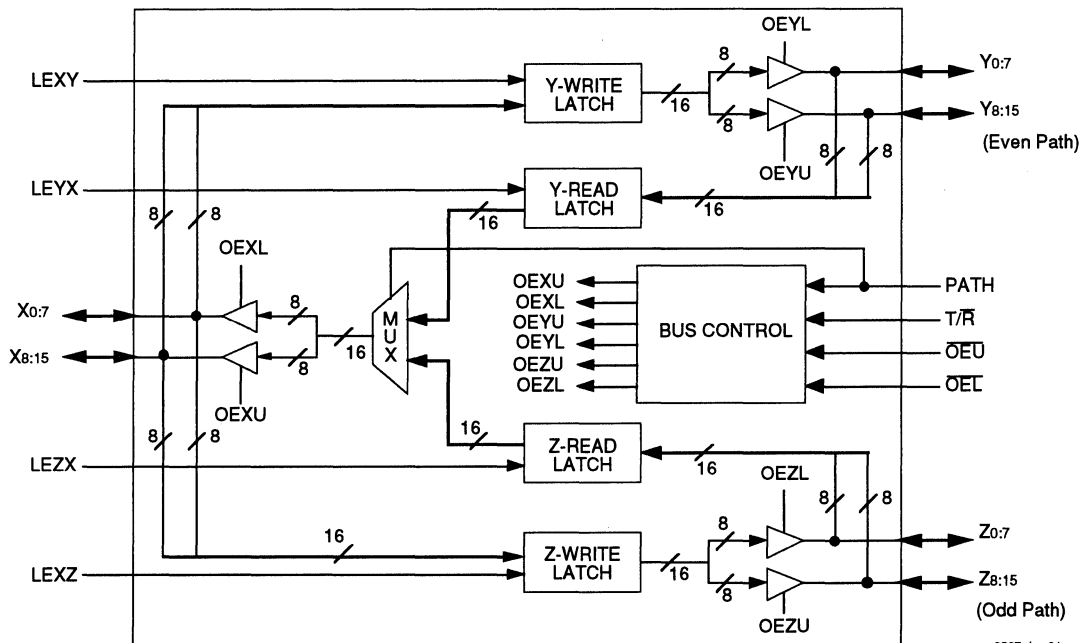


Figure 1. 73720 Block Diagram

2527 drw 01

### NOTE:

1. Logic equations for bus control:

$$OEXU = T/R^* \cdot OEU^*; OEXL = T/R^* \cdot OEL^*; OEYU = T/R \cdot PATH \cdot OEU^*$$

$$OEYL = T/R \cdot PATH \cdot OEL^*; OEZU = T/R \cdot PATH^* \cdot OEU^*; OEZL = T/R \cdot PATH^* \cdot OEL^*$$

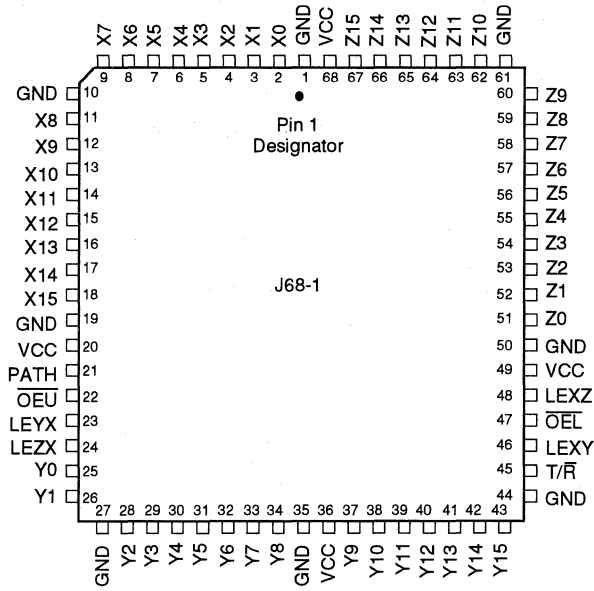
RISChipSet, RISController, R305x, R3051, R3052, R3041, R3081, R4400 and R4600 are trademarks and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

MARCH 1994

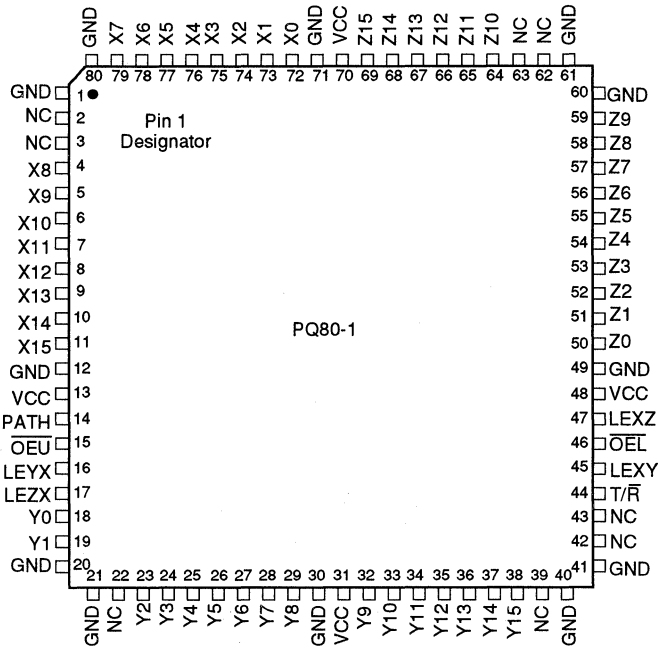
6

**PIN CONFIGURATIONS**



**PLCC  
TOP VIEW**

2527 drw 02



**PQFP  
TOP VIEW**

2527 drw 03

## PIN DESCRIPTION

Signal	I/O	Description
X(0:15)	I/O	Bidirectional Data Port X. Usually connected to the CPU's A/D (Address/Data) bus.
Y(0:15)	I/O	Bidirectional Data port Y. Connected to the even path or even bank of memory.
Z(0:15)	I/O	Bidirectional Data port Z. Connected to the odd path or odd bank of memory.
LEXY	I	Latch Enable input for Y-Write Latch. The Y-Write Latch is open when LEXY is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXY
LEXZ	I	Latch Enable input for Z-Write Latch. The Z-Write Latch is open when LEXZ is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXZ.
LEYX	I	Latch Enable input for the Y-Read Latch. The Y-Read Latch is open when LEYX is HIGH. Data from the even path Y is latched on the HIGH-to-LOW transition of LEYX.
LEZX	I	Latch Enable input for the Z-Read Latch. The Z-Read Latch is open when LEZX is HIGH. Data from the odd path Z is latched on the HIGH-to-LOW transition of LEZX
PATH	I	Even/Odd Path Selection. When high, PATH enables data transfer between the X-Port and the Y-port (even path). When LOW, PATH enables data transfer between the X-Port and the Z-Port (odd path).
T/R Port	I	Transmit/Receive Data. When high, Port X is an input Port and either Port Y or Z is an output Port. When LOW X is an output Port while Ports Y & Z are input Ports
OE <sub>U</sub>	I	Output Enable for Upper byte. When LOW, the Upper byte of data is transferred to the port specified by PATH in the direction specified by T/R .
OE <sub>L</sub>	I	Output Enable for Lower byte. When LOW, the Lower byte of data is transferred to the port specified by PATH in the direction specified by T/R .

2527 tbi 02

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +125	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

## NOTE:

2527 tbi 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COU	Output Capacitance	VOU = 0V	12	pF

## NOTE:

2527 tbi 04

- This parameter is guaranteed by device characterization, but is not production tested.

## TRUTH TABLE

Path	T/R	OE <sub>U</sub>	OE <sub>L</sub>	Functionality
L	L	L	L	Z→X (16-bits)–Read Z <sup>(1)</sup>
L	H	L	L	X→Z (16 bits)–Write Z <sup>(1)</sup>
H	L	L	L	Y→X (16-bits)–Read Y <sup>(2)</sup>
H	H	L	L	X→Y (16 bits)–Write Y <sup>(2)</sup>
X	X	H	H	All output buffers are disabled
X	X	H	L	Transfer of lower 8 bits (0:7) as per PATH & T/R
X	X	L	H	Transfer of upper 8 bits (8:15) as per PATH & T/R

## NOTES:

2527 tbi 01

- For Z→X and X→Z transfers, Y-port output buffers are tristated.
- For Y→X and X→Y transfers, Z-port output buffers are tristated.

## ARCHITECTURE OVERVIEW

The Bus Exchanger is used to service both read and write operations between the CPU and the dual memory busses. It includes independent data path elements for reads from and writes to each of the memory banks (Y and Z). Data flow control is managed by a simple set of control signals, analogous to a simple transceiver. In short, the Bus Exchanger allows bidirectional communication between ports X and Y and ports X and Z as illustrated in figure 1.

The data path elements for each port include:

**Read Latch:** Each of the memory ports Y and Z contains a transparent latch to capture the contents of the memory bus. Each latch features an independent latch enable.

**Write Latch:** Each memory port Y and Z contains an independent latch to capture data from the CPU bus during writes. Each memory port write latch features an independent latch enable, allowing write data to be directed to a specific memory port without disrupting the other memory port.

### Data Flow Control Signals

**T/R** (Transmit/Receive). This signal controls the direction of data transfer. A transmit is used for CPU writes, and a receive is used for read operations.

**OEU, OEL** are the output enable control signals to select upper or lower bytes of all three ports.

**Path:** The path control signal is used to select between the even memory path Y and the odd memory path Z during read or write operations. Path selects the memory port to be connected to the CPU bus (X-port), and is independent of the latch enable signals. Thus, it is possible to transfer data from one memory port to the CPU bus (X) while capturing data from the other memory port.

## MEMORY READ OPERATIONS

### Latch Mode

In this mode the read operation consists of two stages. During the first stage, the data present at the memory port is captured by the read latch for that memory port. During a subsequent stage, data is brought from a selected memory port to the CPU A/D port X by using output enable control.

The read operation is selected by driving T/R LOW. The read is managed using the Path input to select the memory port (Y or Z); the LEYX/LEZX enable the data capture into the corresponding Read Latch.

In this way, memory interleaving can be performed. While data from one bank is output onto the CPU bus, data on the other bank is captured in the other memory port. In the next cycle, the Path input is changed, enabling the next data

element onto the CPU bus, while the first bank is presented with a new data element.

### Transparent Mode

The Bus Exchanger may be used as a data transceiver by leaving all latches open or transparent.

### Memory Write Operations

Memory write operations also consist of two distinct stages. During one stage, the write data is captured into the selected memory port write latch. During a later stage, the memory is presented on the memory port bus.

The write operation is selected by driving T/R HIGH. Writes are thus performed using the Path input to select the memory port (Y or Z). The LEXY/LEXZ capture data in the corresponding Write Latch.

Note that it is possible to utilize the bus exchanger's write resources as an additional write buffer, if desired; the CPU A/D bus can be freed up once the data has been captured by the Bus Exchanger.

## APPLICATIONS

### Use as Part of the R3051 Family ChipSet

Figure 2 shows the use of the Bus Exchanger in a typical R3051 based system.

In write transactions, the R3051 drives data on the CPU bus. The latch enables are held open through the entire write; thus, the bus exchanger is used like a transceiver. The appropriate LEXY/LEXZ signal is derived from ALE (Logic LOW - indicating that the processor is driving data) and the low order address bit. The rising edge of W<sub>r</sub> from the CPU, ends the write operation.

During read transactions, the memory system is responsible for generating the input control signals to cause data to be captured at the memory ports. The memory controller is also responsible for acknowledging back to the CPU that the data is available, and causing the appropriate path to be selected.

The R3721 DRAM controller for the R3051 family uses the transparent latches of the read ports. The R3721 directly controls the inputs of the bus exchanger, during both reads and writes. Consult the R3721 data sheet for more information on these control signals.

### Use in a general 32-bit System

Figures 3 and 4 illustrate the use of the Bus Exchanger in a 32-bit microprocessor based system. Note the reduced pin count achieved with the Bus Exchanger.

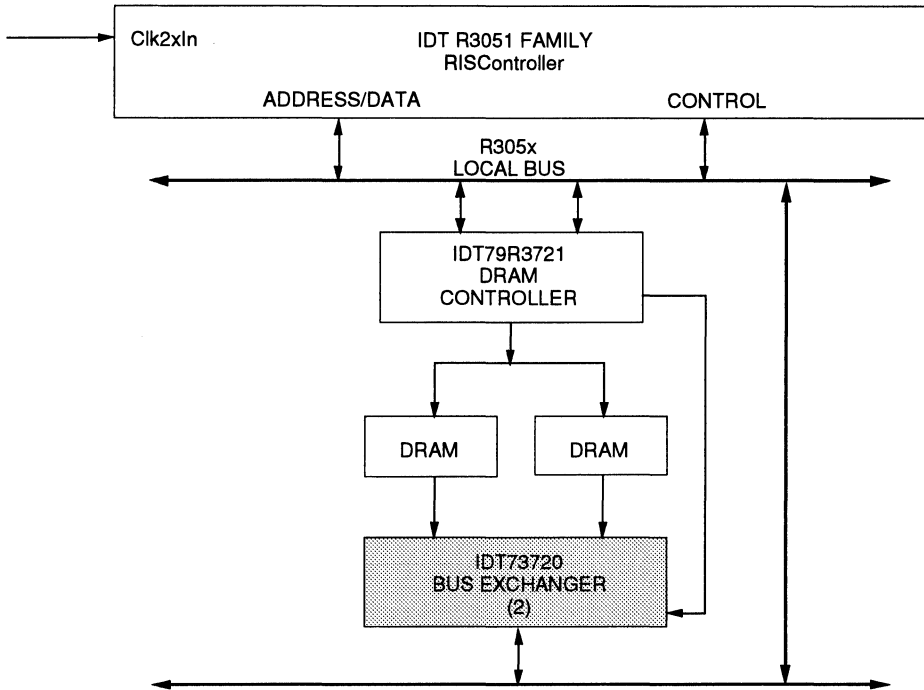
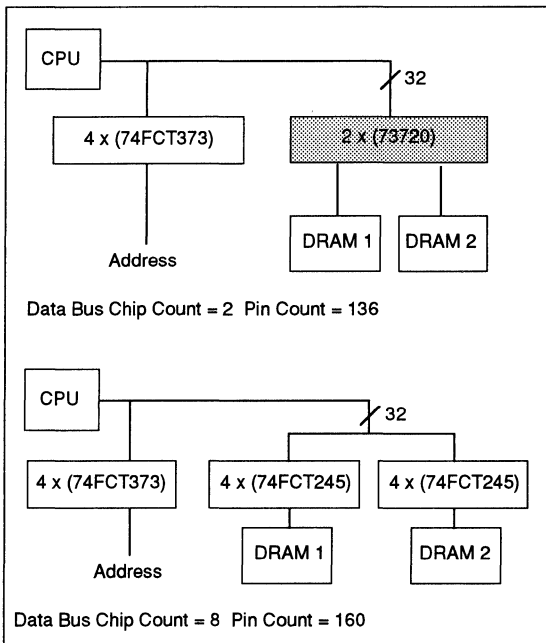


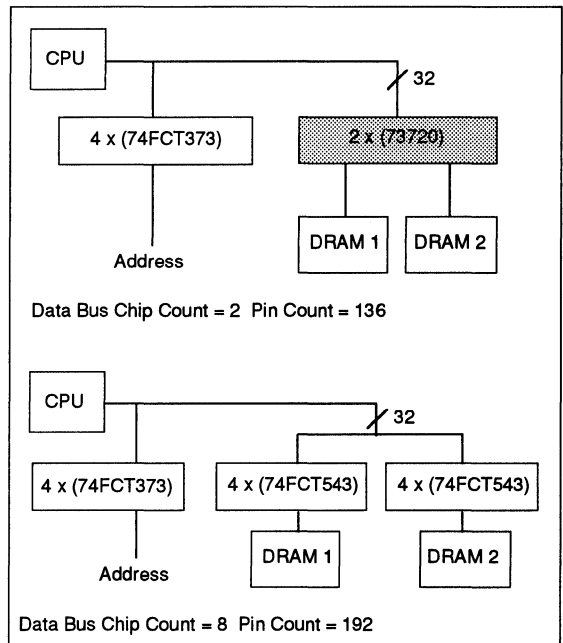
Figure 2. Bus Exchanger Used in R3051 Family System

2527 drw 04



2527 drw 05

Figure 3. CPU System with Transparent Data Path (2-way Interleaving)



2527 drw 06

Figure 4. CPU System with Latched Data Path (2-way Interleaving)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level		2.0	—	—	V	
$V_{IL}$	Input LOW Level		—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}, V_{IH} = 2.7V$	Inputs only	—	—	5.0	$\mu A$
			I/O pins	—	—	5.0	
$I_{IL}$	Input LOW Current	$V_{CC} = \text{Max.}, V_{IL} = 0.5V$	Inputs only	—	—	-5.0	$\mu A$
			I/O pins	—	—	-5.0	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18mA$	—	-0.7	-1.2	V	
$I_{OS}^{(3)}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}$	-60	—	-200	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$ or $V_{IL}, I_{OH} = -12mA$	2.4	3.3	—	V	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, V_{IN} = V_{IH}$ or $V_{IL}, I_{OL} = 12mA$	—	0.3	0.5	V	
$V_H$	Input Hysteresis All inputs	$V_{CC} = 5V$	—	200	—	mV	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$	—	0.2	1.5	mA	
$\Delta I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(4)}$	—	0.5	2.0	mA/ Input	
$I_{CCD}$	Dynamic Power Supply Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$ or $\text{GND}$ Outputs Disabled $\overline{OE} = V_{CC}$ One Input Toggling 50 % Duty Cycle	—	0.25	0.5	mA/ MHz	
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC}$ or $\text{GND}$ Outputs Disabled 50 % Duty Cycle $\overline{OE} = V_{CC}$ $f_i = 10\text{MHz}$ One Bit Toggling	—	2.7	6.5	mA	

**NOTES:**

2527 tbl 05

- For conditions shown as max. or min., use appropriate  $V_{CC}$  value.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient.
- Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $\text{NT} = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
All currents are in milliamps and all frequencies are in megahertz.

**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 5

2527 tbl 06

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ$  to  $+70^\circ C$ )

Symbol	Parameter	Test Conditions <sup>(1)</sup>	73720A		73720		Units
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	X to Y & X to Z Latches enabled	$C_L = 50pF$ $R_L = 500\text{ Ohms}$	2.0	6.0	2.0	7.5	ns
tPLH tPHL	Y to X & Z to X Latches enabled		2.0	6.0	2.0	7.5	ns
tPLH tPHL	Latch Enable to Y & Z Port LEXY to Y LEZX to Z		2.0	7.0	2.0	8.5	ns
tPLH tPHL	Latch Enable to X LEYX to X LEZX to X		2.0	7.0	2.0	8.5	ns
tPLH tPHL	Path to X Port Propagation Delay		2.0	7.0	2.0	8.5	ns
tHZ tLZ	Y & Z Port Disable Time ( $T/\bar{R}$ , PATH, $\bar{O}E_U$ , $\bar{O}E_L$ ) <sup>(3)</sup>		2.0	8.5	2.0	9.5	ns
tZH tZL	Y & Z Port Enable Time ( $T/\bar{R}$ , PATH, $\bar{O}E_U$ , $\bar{O}E_L$ ) <sup>(3)</sup>		2.0	9.5	2.0	10.5	ns
tHZ tLZ	X-Port DisableTime ( $T/\bar{R}$ , $\bar{O}E_U$ , $\bar{O}E_L$ ) <sup>(3)</sup>		2.0	8.5	2.0	9.5	ns
tZH tZL	X-Port Enable Time ( $T/\bar{R}$ , $\bar{O}E_U$ , $\bar{O}E_L$ ) <sup>(3)</sup>		2.0	9.5	2.0	10.5	ns
tSU	Port to LE Set-up time		2.0	—	2.0	—	ns
tH	Port to LE Hold time		1.5	—	1.5	—	ns
tW	LE Pulse Width, HIGH or LOW <sup>(2)</sup>		3	—	4	—	ns

**NOTES:**

1. All timings are referenced to 1.5 V.
2. Minimum Delay Times, Enable Times, Disable Times and Pulse Width are guaranteed by design, but not tested.
3. Bus turnaround times are guaranteed by design, but not tested. ( $T/\bar{R}$  enable/disable times).

2527 tbl 07

**TEST CIRCUITS AND WAVEFORMS**

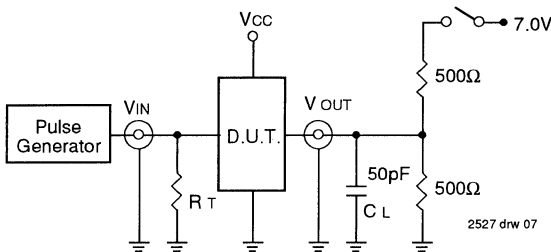


Figure 5. Test Circuit for all outputs

**SWITCH POSITION**

Test	Switch
Disable LOW	Closed
Enable LOW	Closed
All Other Tests	Open

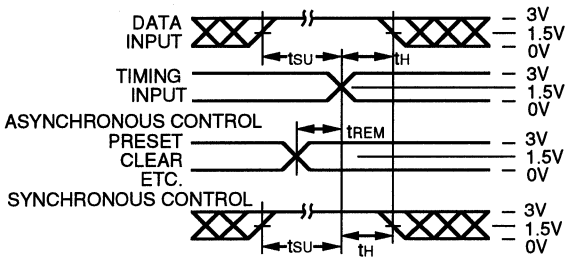
**DEFINITIONS:**

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

2527 tbl 08

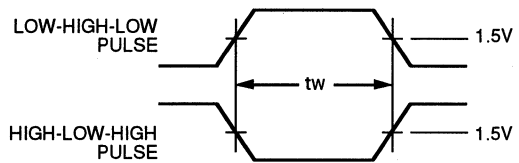


**SET-UP, HOLD AND RELEASE TIMES**



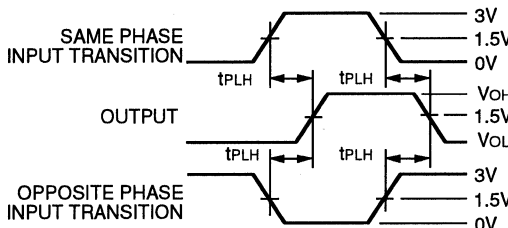
2527 drw 08

**PULSE WIDTH**



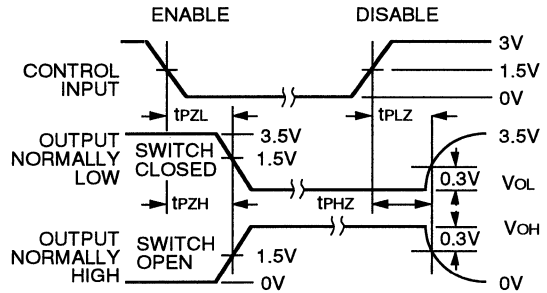
2527 drw 09

**PROPAGATION DELAY**



2527 drw 10

**ENABLE AND DISABLE TIMES**



2527 drw 11

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_0 \leq 50\Omega$ ;  $t_F \leq 2.5$ ns;  $t_r \leq 2.5$ ns.

**ORDERING INFORMATION**

IDT	XXXXX	X	X	X	
	Device Type	Speed	Package	Process/ Temperature Range	
				Blank	Commercial Temperature Range
				J	68-Pin PLCC
				PQF	80-Pin PQFP
				Blank	Standard Speed
				A	High Speed
				73720	Bus Exchanger

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Integrated Device Technology, Inc.

# IDT79R4000 FLEXI-CACHE™ DEVELOPMENT TOOL

**PRELIMINARY**  
**IDT7MP6048**  
**IDT7MP6068**

## FEATURES

- Hardware Development Tool for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU
- Configurable in various cache sizes, number of words per line size, and split vs. unified cache operation
- Move from prototype/development to production with no redesign by using pin-compatible "production grade" IDT79R4000 secondary cache modules
- Four identical 80-lead gold-plated SIMMs (Single In-Line Memory Modules) support each IDT79R4000 CPU
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL-compatible I/Os
- Single 5V (±10%) power supply

## DESCRIPTION

The IDT7MP6048/7MP6068 is a Hardware Development Tool used for implementing various configurations of the secondary cache requirement for the IDT79R4000 CPU. By changing jumpers on the modules, the designer can easily

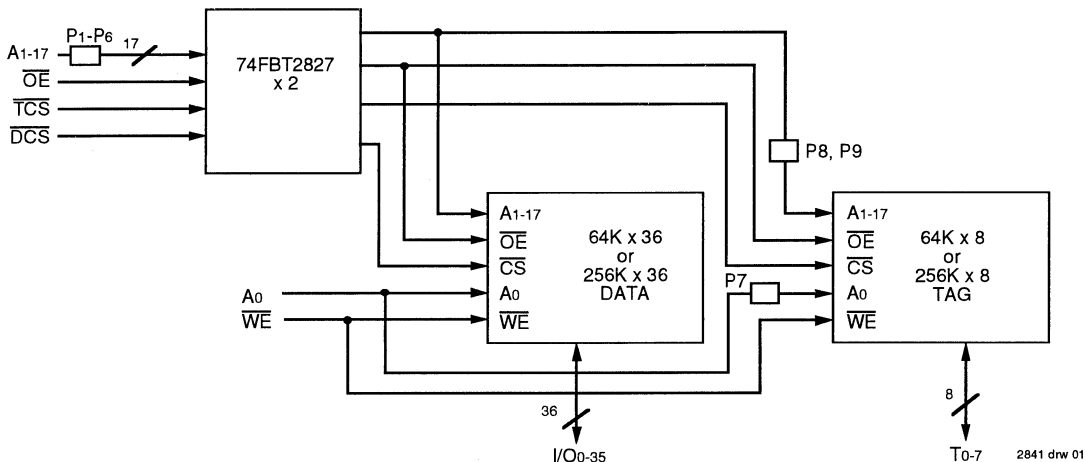
change certain characteristics (cache size, number of words per line, and split vs. unified operation) of the secondary cache in the lab. By running benchmarks on the actual system using these various cache configurations, the secondary cache which best optimizes system performance can be determined. This development tool gives you cache performance benchmarks which are superior to benchmarks derived via simulation.

Move from development to production without changing the secondary cache footprint by choosing pin-compatible "production grade" IDT79R4000 secondary cache modules. These high-performance, high-density IDT modules are optimized to meet the customers' exact cache requirements required for volume production of the system (please consult the factory for more details).

The IDT7MP6048 is a 1 MB secondary cache module block (four identical modules builds a complete cache to support each IDT79R4000 CPU) constructed on a multilayer, epoxy laminate substrate (FR-4) using 11 64K x 4 Static RAMs and FBT logic drivers while the IDT7MP6068 is a 4MB secondary cache module block using eleven 256K x 4 Static RAMs and FBT logic drivers. The FBT drivers have BiCMOS I/Os and internal 25Ω series output resistors resulting in the fastest propagation times with minimal overshoots and ringing. Mul-

6

## FUNCTIONAL BLOCK DIAGRAM<sup>(1)</sup>



### NOTE:

1. The Data and Tag sizes shown on the block diagram are only for the case when the jumpers are in the default positions for the respective modules. These sizes will change according to the jumper connections (see Jumper Connections on page 2).

The IDT logo is a registered trademark and FLEXI-CACHE is a trademark of Integrated Device Technology, Inc.

multiple GND pins and on-board decoupling capacitors provide maximum noise immunity for this performance critical part of the system. All inputs and outputs of the modules are TTL-

compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation of the module.

### CACHE CONFIGURATIONS<sup>(1)</sup>

Memory Size	Words per line	Cache Operation
4MB (7MP6068 default)	4 (default)	unified cache (default)
2MB	8	split cache
1MB (7MP6048 default)	16	
512KB	32	
256KB		
128KB		

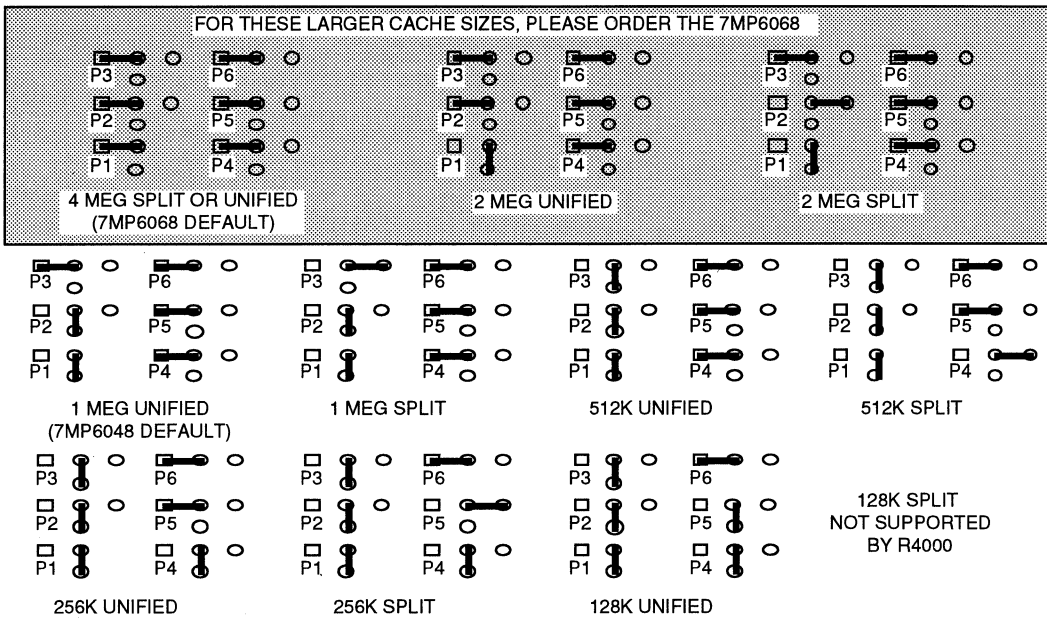
**NOTE:**

2841 tbl 01

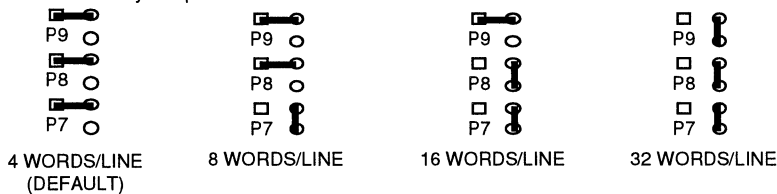
1. Please refer to the Jumper Connections for instructions on how to implement the Cache Configurations shown above.

### JUMPER CONNECTIONS

Cache depth and Split vs. Unified Operation are controlled by Jumpers P1-P6 as follows:



Cache line size is controlled by Jumpers P7-P9 as follows:



2841 drw 02

## PIN CONFIGURATION<sup>(1)</sup>

V <sub>CC</sub>	2	1	GND
I/O <sub>1</sub>	4	3	I/O <sub>0</sub>
I/O <sub>3</sub>	6	5	I/O <sub>2</sub>
I/O <sub>5</sub>	8	7	I/O <sub>4</sub>
GND	10	9	I/O <sub>6</sub>
I/O <sub>8</sub>	12	11	I/O <sub>7</sub>
I/O <sub>10</sub>	14	13	I/O <sub>9</sub>
I/O <sub>12</sub>	16	15	I/O <sub>11</sub>
I/O <sub>14</sub>	18	17	I/O <sub>13</sub>
I/O <sub>15</sub>	20	19	GND
I/O <sub>17</sub>	22	21	I/O <sub>16</sub>
I/O <sub>19</sub>	24	23	I/O <sub>18</sub>
I/O <sub>21</sub>	26	25	I/O <sub>20</sub>
GND	28	27	I/O <sub>22</sub>
I/O <sub>23</sub>	30	29	V <sub>CC</sub>
I/O <sub>25</sub>	32	31	I/O <sub>24</sub>
I/O <sub>27</sub>	34	33	I/O <sub>26</sub>
I/O <sub>29</sub>	36	35	I/O <sub>28</sub>
I/O <sub>30</sub>	38	37	GND
I/O <sub>32</sub>	40	39	I/O <sub>31</sub>
I/O <sub>34</sub>	42	41	I/O <sub>33</sub>
GND	44	43	I/O <sub>35</sub>
A <sub>0</sub>	46	45	$\overline{WE}$
A <sub>2</sub>	48	47	A <sub>1</sub>
A <sub>4</sub>	50	49	A <sub>3</sub>
A <sub>6</sub>	52	51	A <sub>5</sub>
V <sub>CC</sub>	54	53	GND
$\overline{OE}$	56	55	$\overline{DCS}$
A <sub>8</sub>	58	57	A <sub>7</sub>
A <sub>10</sub>	60	59	A <sub>9</sub>
GND	62	61	A <sub>11</sub>
A <sub>13</sub>	64	63	A <sub>12</sub>
A <sub>15</sub>	66	65	A <sub>14</sub>
A <sub>17</sub>	68	67	A <sub>16</sub>
T <sub>0</sub>	70	69	TCS
T <sub>1</sub>	72	71	GND
T <sub>3</sub>	74	73	T <sub>2</sub>
T <sub>5</sub>	76	75	T <sub>4</sub>
T <sub>7</sub>	78	77	T <sub>6</sub>
GND	80	79	V <sub>CC</sub>

SIMM  
TOP VIEW

2841 drw 03

### NOTE:

- For proper operation of the module, please refer to the Jumper Connections for proper connections of the module pins.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5V ± 10%

2841 tbl 02

## PIN NAMES

I/O <sub>0-35</sub>	Data Inputs/Outputs
T <sub>0-7</sub>	Tag Inputs/Outputs
A <sub>0-17</sub>	Address Inputs
$\overline{DCS}$	Data Chip Select
TCS	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground

2841 tbl 03

## CAPACITANCE

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN(D)</sub>	Input Capacitance (Data)	V <sub>IN</sub> = 0V	10	pF
C <sub>IN(A)</sub>	Input Capacitance (A <sub>1-15</sub> , $\overline{OE}$ , TCS, DCS)	V <sub>IN</sub> = 0V	10	pF
C <sub>IN(B)</sub>	Input Capacitance (A <sub>0</sub> , $\overline{WE}$ )	V <sub>IN</sub> = 0V	100	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

### NOTE:

- This parameter is guaranteed by design, but not tested.

2841 tbl 04

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

- V<sub>IL</sub> = -1.5V for pulse width less than 10ns.

2841 tbl 05

## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating <sup>(1)</sup>	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2841 tbl 06

### DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

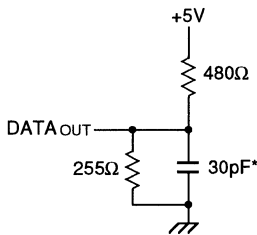
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{L1} $	Input Leakage (except $A_0, \overline{WE}$ )	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	10	$\mu A$
$ I_{L2} $	Input Leakage ( $A_0, \overline{WE}$ )	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	110	$\mu A$
$ I_{LO} $	Output Leakage	$V_{CC} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	10	$\mu A$
$I_{CC}$	Operating Current	$\overline{CS} = V_{IL}; V_{CC} = \text{Max.}, \text{Outputs Open}$	—	2200	mA
$V_{OH}$	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	V
$V_{OL}$	Output Low Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	0.4	V

2841 tbl 07

### AC TEST CONDITIONS

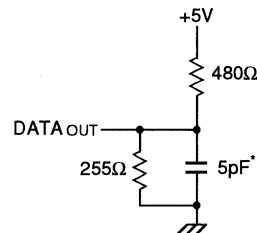
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 – 4

2841 tbl 08



2841 drw 04

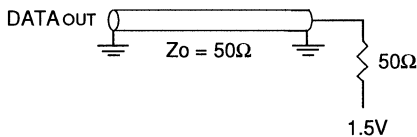
Figure 1. Output Load



2841 drw 05

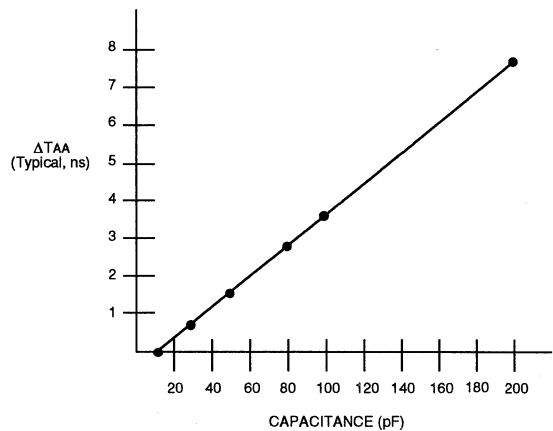
Figure 2. Output Load  
(for tolz and tohz)

\* Including scope and jig.



2841 drw 06

Figure 3. Alternate Output Load



2841 drw 07

Figure 4. Alternate Lumped Capacitive Load,  
Typical Derating

## AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0°C to +70°C)

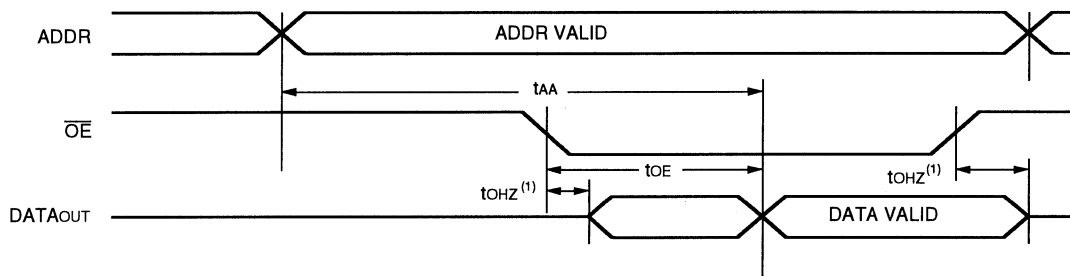
Symbol	Parameter	7MP6048/6068SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>														
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t <sub>A0A</sub>	A <sub>0</sub> Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
<b>WRITE CYCLE</b>														
t <sub>AW</sub>	Address Valid to End of Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t <sub>A0W</sub>	A <sub>0</sub> Valid to End of Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t <sub>WP</sub>	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t <sub>DW</sub>	Data Valid to End of Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

**NOTE:**

1. This parameter is guaranteed by design but not tested.

2833 tbl 08

### TIMING WAVEFORM OF READ CYCLE<sup>(1)</sup>

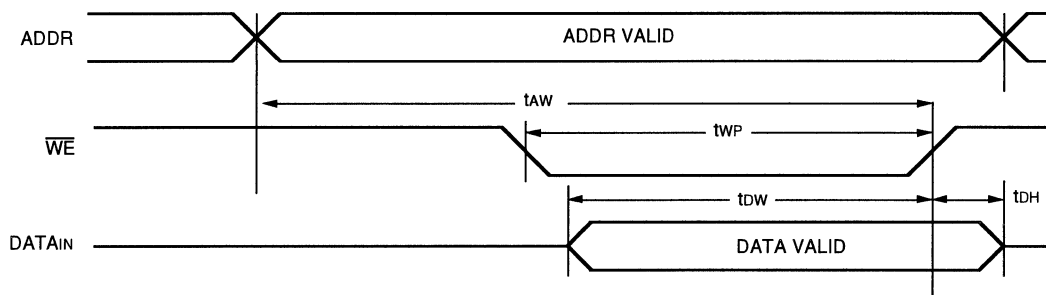


2841 drw 08

**NOTE:**

1. This parameter is guaranteed by design, but not tested.

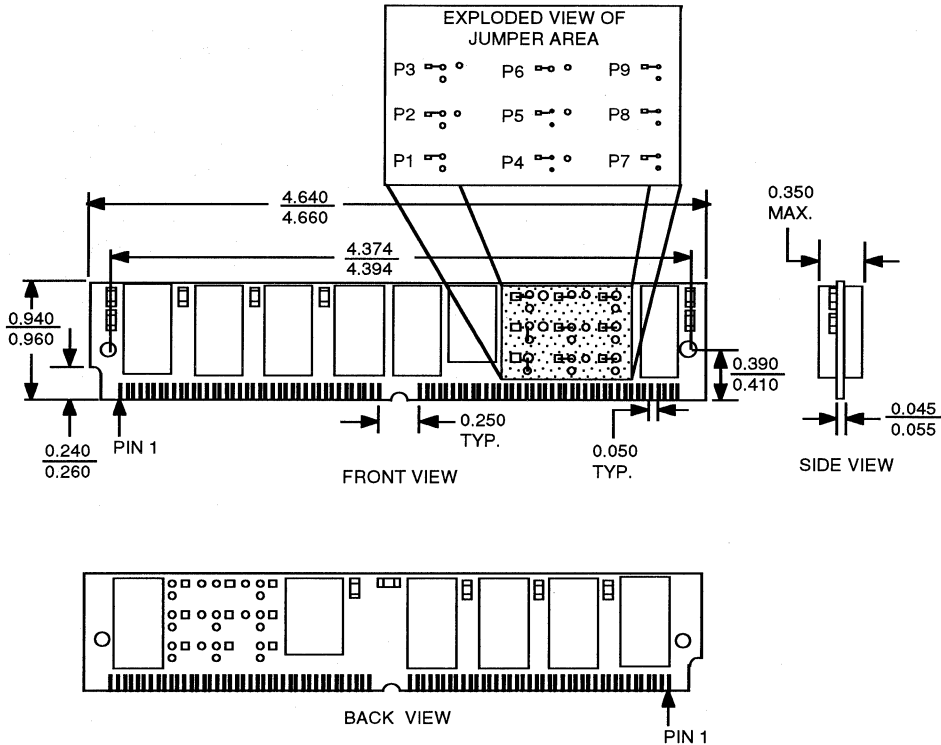
### TIMING WAVEFORM OF WRITE CYCLE



2841 drw 09

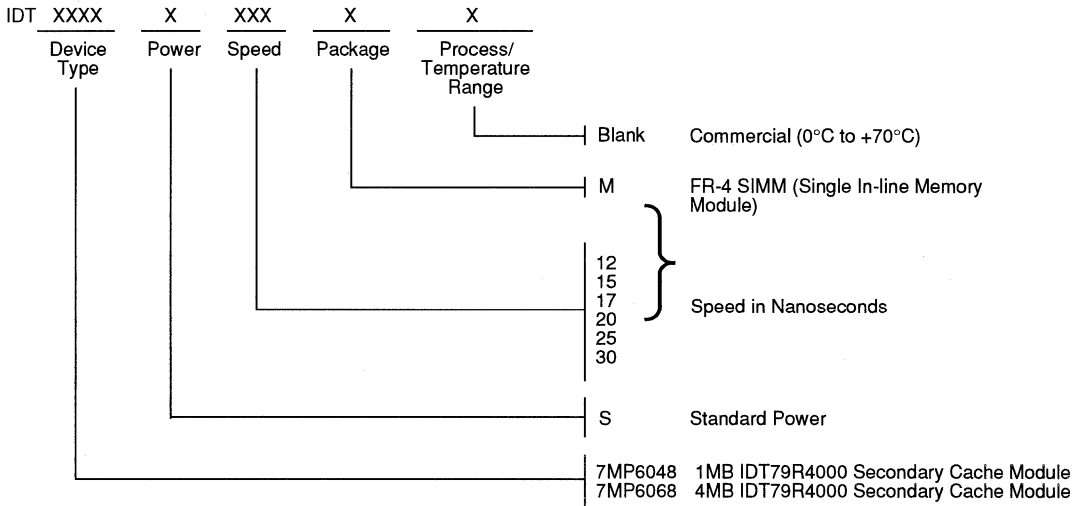
6

**PACKAGE DIMENSIONS**



2841 drw 10

**ORDERING INFORMATION**



2841 drw 11



Integrated Device Technology, Inc.

# LASER PRINTER Integrated System Controller for IDT R30xx RISController™ Family with Adobe Frame Buffer Compression

**IDT79R3740  
ADVANCE  
DATA**

## FEATURES:

- Integrated system controller for low cost, high resolution, high performance, laser printer controllers
  - Direct interface to IDT R3041™, R3051™, R3052™, R3071™ and R3081™ pin-compatible RISControllers™
  - Supports bus interface frequencies from 16 to 33MHz
- Incorporates Adobe Frame Buffer Compression
  - Achieves greater than 4:1 lossless compression for most pages of reasonable complexity, lowering DRAM cost up to 4MB for 600 dpi, 8 1/2" x 11" printers
  - Supports range of printer strategies, from "print all pages" with minimum memory cost (by switching to 300 dpi for page complexities that require more DRAM), to requiring more memory to print fully compressed, high quality pages at maximum performance
  - Supports printer page rates up to 20 ppm
- On-chip DRAM controller for up to 40MB of non-interleaved DRAM (up to 3 banks)
  - Direct DRAM drive
  - Supports base plus extension DRAM implementation (supports two device sizes in same system)
- On-chip ROM controller for up to 20MB of ROM (up to 3 banks)
  - Two-way interleaved or non-interleaved
- Supports burst ROMs
- Programmable I/O ports provide glue-less interface to integrated low cost peripherals
  - Burst DMA interface (permits inclusion of 8530 based AppleTalk as standard feature, at lower cost than option card approach)
  - Two DMA I/O ports with on-chip 4-byte FIFO with data packing and unpacking
  - Six programmable PIO pins for peripheral interrupts
  - 8-bit and 16-bit I/O ports
- IEEE P1284 bidirectional Centronics interface supports Compatible, Nibble, Byte, ECP and EPP modes
- Coprocessor bus master DMA interface for coprocessors (e.g. Adobe's Typhoon font rasterizer)
- High performance video interface
  - Video DMA support
  - Serializer can shift right or left to support duplexing
  - On-chip 4-word x 32-bit video FIFO
  - Programmable margin counters
  - PLL with optional bypass mode
  - Video bit rates to 10 megabits per second
- General purpose functions
  - 24-bit general purpose counter/timer
- 160-pin quad plastic flatpack (PQFP)

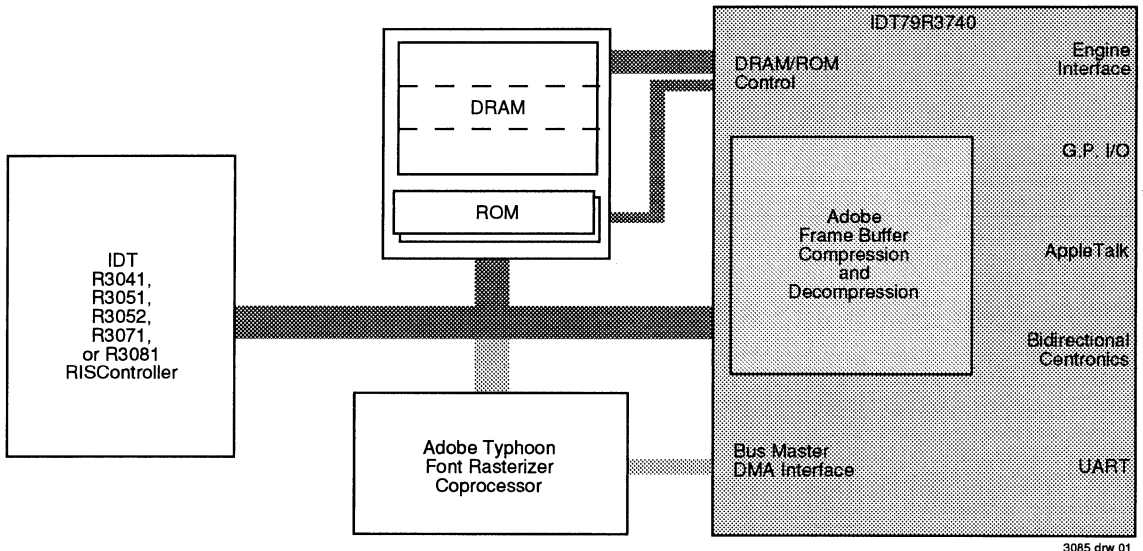


Figure 1. IDT79R3740 system organization.

The IDT logo is a registered trademark, and RISController, R3041, R3051, R3052, R3071, R3081, R4400 and R4600 are trademarks of Integrated Device Technology, Inc. Adobe, PostScript are trademarks of Adobe Systems Incorporated



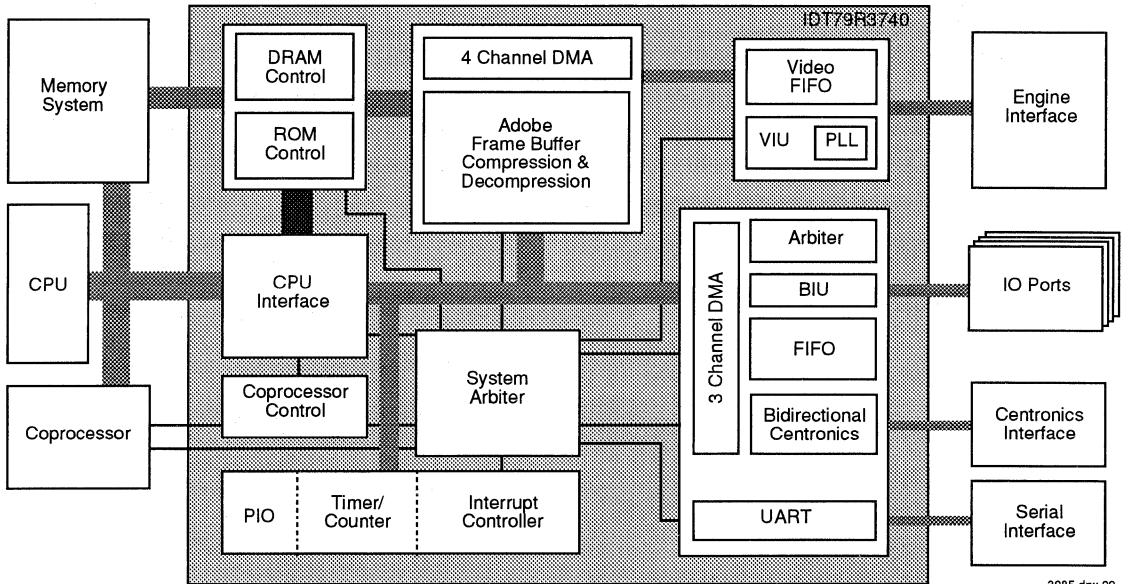


Figure 2. IDT79R3740 Block Diagram

**GENERAL DESCRIPTION**

The IDT79R3740 system controller is a highly integrated and programmable controller for low cost, high performance raster image systems. It utilizes Adobe Frame Buffer Compression (Adobe software accelerated by integrated hardware compression and decompression engines) to facilitate 600 dpi resolution using only 2MB of DRAM (600 dpi, 8 1/2 x 11" printers without compression are typically implemented with 6MB of DRAM), or 3MB for implementations including both PCL5e and PostScript Level 2.

The IDT79R3740 provides direct interfaces for the R3051 family of RISControllers, a high performance, flexible memory system controller, an interface for an optional coprocessor/accelerator interface (Adobe Typhoon), a '186-like interface for industry standard I/O peripherals, and a high performance engine interface. The IDT79R3740 definition assumes that most printer OEMs want a low base unit price, with a wide range of productization options, for various cost/performance points and printing strategies.

**ADOBE FRAME BUFFER COMPRESSION**

Adobe provides a comprehensive solution for memory cost reduction, supporting a complex set of system goals. Two underlying printer implementation strategies are supported.

First and foremost, the compression scheme must provide greater than four-to-one compression for most of the pages printed, across a broad range of page styles, using a lossless compression algorithm to maintain high page quality, regardless of data type (fonts, graphics or scanned halftone images). This affords the opportunity to significantly lower frame buffer memory cost (by up to 4MB for a 600 dpi, 8 1/2 x 11" page). In this model, the performance, quality and range of pages printed with full compression can be increased by adding more memory.

Secondly, Adobe Frame Buffer Compression can support a printer strategy of "printing all pages," avoiding the all-or-nothing extreme of full compression or the "page not printed because" error message. To implement this strategy, Adobe Frame Buffer Compression utilizes a two-step process, beginning with a lossless compression algorithm to provide full compression in a minimum memory system. If this cannot be achieved in the available memory space, because of overflow of the compressed buffer space, a lossy algorithm then attempts to achieve a higher compression ratio.

**CPU INTERFACE**

IDT79R3740 communicates with the IDT R3051 family CPUs via a multiplexed address/data bus and control interface that is a pin-for-pin, glueless match with the control signal and timing standards for IDT's RISController family, including R3041, R3051, R3052, R3071 and R3081.

A key *system* goal of IDT79R3740 is to integrate most general purpose logic to lower system cost, while preserving

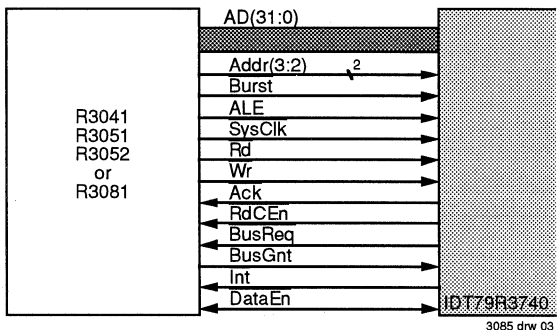


Figure 3. IDT RISController to IDT79R3740 Interface

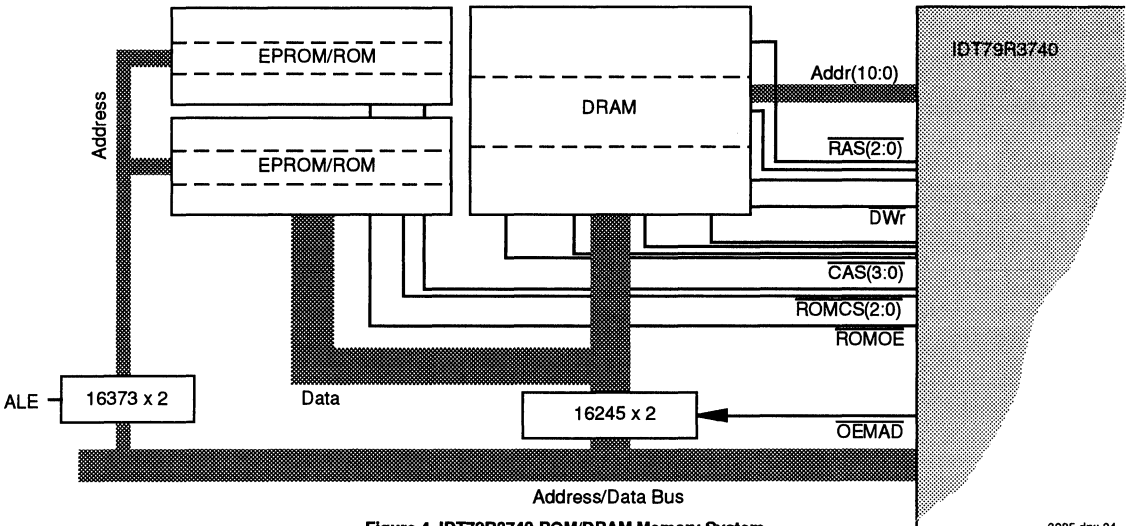


Figure 4. IDT79R3740 ROM/DRAM Memory System

3085 drw 04

OEM flexibility for product differentiation through CPU and clock frequency choices, memory timing/tuning and the addition of coprocessors.

A primary performance goal is to run the CPU bus at maximum utilization and frequency, with a minimum of stalls caused by memory system latencies or I/O device bandwidth limitations. IDT79R3740's on-chip FIFOs, arbitration logic and DMA capability allow I/O transfers to burst in and out of system memory at maximum memory system bandwidth. The CPU bus remains at minimum loading with only the CPU, IDT79R3740, an address latch, memory system buffers/transceivers and a system coprocessor, if used.

The IDT79R3740 provides unique system flexibility by providing programmability of the system interface functions and timing parameters. These include controls for memory configuration and device size, edge timing for DRAM and I/O peripheral control signals, and controls for the format and timing of engine interface signals. Each system interface is defined based on specific system goals for that interface. The IDT79R3740 contains Configuration Registers written during initialization, to configure the various modes, features and timing parameters.

**DRAM CONTROLLER**

Given the low-cost goals for IDT79R3740-based systems, and the relatively low performance gain for interleaving DRAM, the R3740 provides control signals for non-interleaved DRAM. DRAM control signals support base-plus-extension 32-bit memory organizations, where the minimum DRAM configuration can be installed in the board and optional memory is added by the end user (typically standard SIMMs). Various DRAM depths are supported, and the address space is continuous for the selected configuration. The base bank (RAS0) is typically different device sizes than the extension banks (RAS1 and RAS2).

For 33MHz systems there is an option to extend CAS by one additional cycle (also recommended for Typhoon ac-

cesses since Typhoon samples data on the rising edge of SysClk, while the CPU samples data on the falling edge). The DRAM controller supports single transfer reads and writes and burst reads. DRAM device attributes supported include page mode, early write and CAS-before-RAS refresh.

**ROM CONTROL**

The ROM controller supports up to 20MB of interleaved or non-interleaved memory. To support different system and device options, the assertion time of RdCEn and Ack can be programmed. There are three chip select lines to control up to three banks of ROM. Each bank can be either interleaved or non-interleaved. ROMCS2 controls the boot bank, and has a fixed space of 4MB. The address space for ROMCS1 and ROMCS2 is programmable for 1, 2, 4 or 8MB. To support interleaving, a ROMOE signal is provided to control the OE of the interleave multiplexer.

The ROM controller supports burst ROMs and the capability to write to the ROM space (for flash devices or debug).

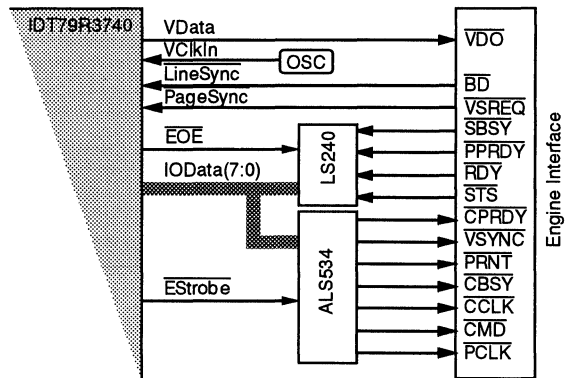


Figure 5. IDT79R3740 Engine Interface

3085 drw 05

## PROGRAMMABLE ENGINE INTERFACE

The IDT79R3740 moves data from the frame buffer memory (compressed data in DRAM) to the print engine by DMA through the decompression logic for compressed bands and through decompressor bypass logic for uncompressed bands. 32-bit words are buffered in a 4-word, 32-bit wide video FIFO and serialized for output to the print engine video input. A video PLL is provided for synchronization of the video to LineSync. A PLL bypass option is provided for engines that supply the video clock.

The serializer can shift video data in either direction to support duplex printing. Also, horizontal and vertical margin counters are provided, appropriately synchronized to PageSync and LineSync.

## PIO PORT AND INTERRUPT CONTROLLER

The IDT79R3740 has PIO[5:0] pins that can be individually programmed to be an input or an output. Each pin is synchronized and pulled up internally. Input pins can act as an active low interrupt. PIO(5:4) can be programmed to function as RI (Ring Indicator) and DCD (Data Carrier Detect) for the UART.

The interrupt controller serves internal resources and six external interrupts. Internal sources send a one cycle pulse that is latched by the cause register. External interrupt lines are sampled every cycle and latched by the cause register. The CPU reads the cause register to find the interrupt source. Each source is maskable via a mask register.

## GLUELESS I/O CHANNELS

The IDT79R3740 supports two 8-bit and two 16-bit devices on the separate I/O Bus. CPU and Typhoon accesses are supported to I/O devices and font cartridges, as well as DMA operation between I/O devices and DRAM.

I/O channels 0-2 have 16MB address spaces and channel 3 has a 256MB address space. For 16-bit devices, the CPU can read or write to any byte or half word. CPU or Typhoon access to the 16-bit bus with all byte enables active will be

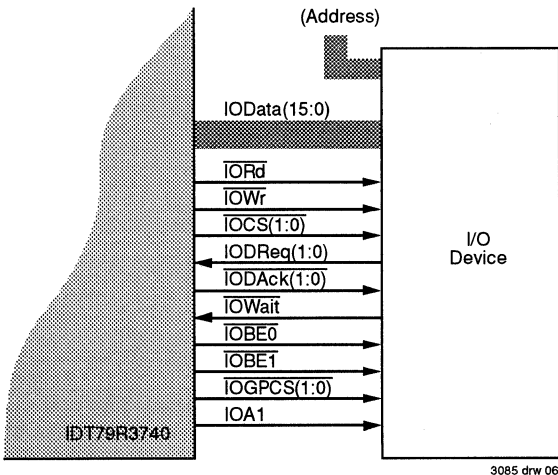


Figure 6. General Purpose I/O Device Interface

performed in two successive I/O cycles. In the two cycles data will be packed or unpacked from a 32-bit register for an I/O read or write, respectively. Conversion between big and little endian is supported for 16-bit devices.

The I/O channel unit operates as a DMA controller only for slave 8-bit devices with DMA capability. 8-bit data is packed or unpacked during DMA access into a 32-bit register for I/O read and write, respectively.

The timing of control signals to an I/O device are programmable. The length of  $\overline{Rd}$  and  $\overline{Wr}$  can be specified.  $\overline{CS}$  or  $\overline{DMAAck}$  are asserted one cycle before  $\overline{Rd}$  and  $\overline{Wr}$  become active and remain active for one cycle after  $\overline{Rd}$  and  $\overline{Wr}$  are deasserted.  $\overline{RdCEN}$  and  $\overline{Ack}$  will be asserted by the IDT79R3740 to end a CPU or coprocessor I/O cycle.

## DMA APPLETALK

One of the DMA supported I/O channels can directly support AppleTalk with only the addition of the 8530 or 85230 and the I/O interface devices it requires. The IDT79R3740's I/O FIFO and burst DMA capabilities aid in the separation of the real-time demands of the AppleTalk protocol from the real-time demands of the engine interface, without the system cost implications of "buffered AppleTalk."

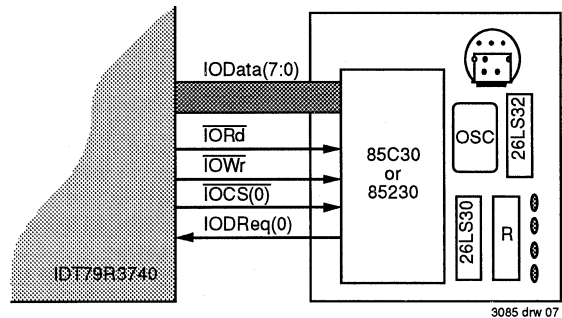


Figure 7. DMA Supported AppleTalk I/O Port

## IEEE P1284 COMMUNICATION

The Centronics interface meets the IEEE P1284 definition for a compliant device.

The modes supported include: Compatible, Nibble, Byte, ECP and EPP, including the negotiating necessary for transition between different modes. Compatible mode support includes the variations: Standard, IBM Epson and Classic.

Data transfer in Compatible mode can be DMA or interrupt driven. Byte and Nibble modes are interrupt driven.

There is support for special character detection in the incoming data path. Control characters like ^C and ^T can be detected to provide a CPU interrupt.

## PROGRAMMABLE TIMER/COUNTER

An internal general purpose 24-bit timer/counter is provided. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will restart the counter if the Enable bit is active.

As a timer, terminal count will cause an interrupt, reload with the value stored in the T/C Value Register and continue counting.

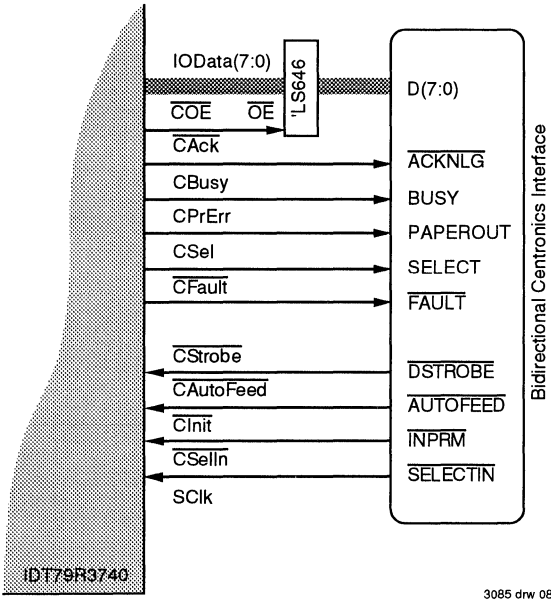


Figure 8. IEEE P1284 Bidirectional Centronics I/O Port

### COPROCESSOR (TYPHOON) CONTROLLER

The IDT79R3740 provides a DMA control interface to Adobe's Typhoon coprocessor, supporting both master or slave modes. As a slave it supports CPU read and write accesses to Typhoon. As a master, Typhoon access to DRAM, ROM and I/O (for font cartridges) is enabled.

### UART SERIAL INTERFACE

The UART in the IDT79R3740 is compatible with the 16550.

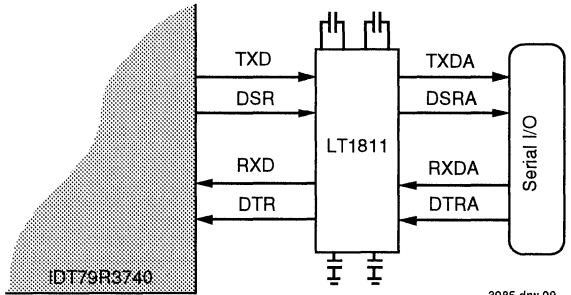


Figure 9. UART Serial Interface Implementation

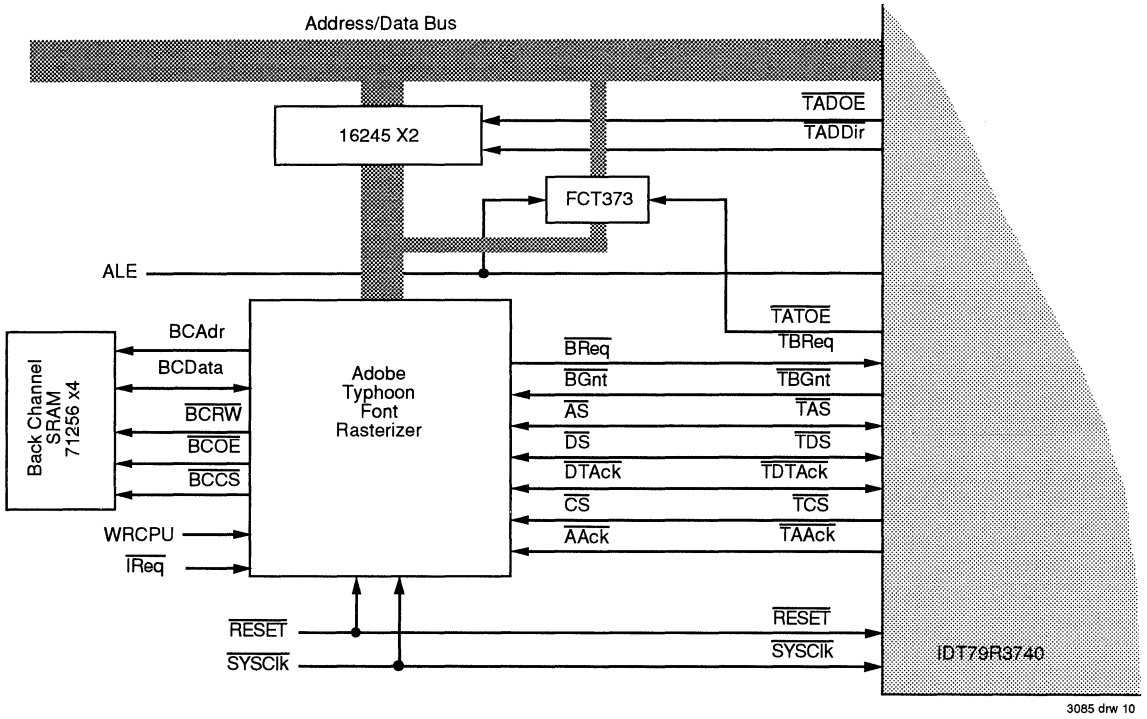


Figure 10. Adobe Typhoon Coprocessor Implementation



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**RISC DEVELOPMENT SUPPORT  
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Integrated Device Technology, Inc.

## RISC DEVELOPMENT SUPPORT PRODUCTS

### INTRODUCTION

For engineers developing software and hardware products around the IDT79R3000 Instruction Set Architecture (ISA), which includes the IDT79R3000A and IDT79R30xx families of RISCControllers, IDT offers three software products and several prototyping and evaluation systems. This catalog primarily focuses on products manufactured and sold directly by Integrated Device Technology.

### SOFTWARE PRODUCTS

**IDT/c**—IDT's optimizing ANSI C-compiler. This compiler, which uses the Gnu C front end, includes full ANSI C compatibility and highly efficient floating point emulation libraries for IDT79R30xx-based systems (without hardware floating point). A unique debug control scripting language makes it easy to locate hardware problems that occur only under rare conditions. IDT/c includes the compiler, optimizer, assembler, linker, librarian, C libraries, Floating Point Libraries, and symbolic debugger.

**IDT/sim**—IDT/sim is IDT's System Integration Manager, used to bring up new hardware and to support the symbolic debug in both the MIPS and IDT C compilers. IDT/sim is a ROMable debug kernel with extensive diagnostics built-in. It is supplied in EPROM on all IDT prototyping boards, and is available in source code for use with either the MIPS or IDT C Compilers.

**IDT/kit**—IDT/kit is our newest software development product: The Kernel Integration ToolKit. It contains source code and compiled versions of a complete set of routines for initializing systems, servicing interrupts, handling floating point exceptions, and so forth. Also included is source code for ANSI libraries, for the Floating Point Emulation Libraries and for transcendental functions.

### PROTOTYPING SYSTEMS

Completely assembled and tested hardware systems are available for prototyping and initial software porting. All include a CPU, serial I/O, EPROM containing the IDT/sim monitor, and some amount of RAM. All have provision for simple addition of user-defined hardware. Units are available with the R3041, R3051/2, and R3081 RISCControllers.

For laser printer controllers, the IDT79S389A Reference Platform provides a ready prototyping target for R30xx Family laser printer controllers using PostScript Level 2 software from Adobe.

### THIRD PARTY DEVELOPMENT TOOLS

The increasing popularity of IDT's RISCController family has resulted in a dramatic increase in the number of third party tools available. For information on these products, contact your local IDT sales representative.

- Real-Time Operating Systems from Lynx, Ready Systems, and Wind River
- Compilers from MIPS, Green Hills, BSO Tasking, and Cygnus
- VME Boards from CES, RISQ Modular Systems, Omnibyte, and Sanders Associates
- Device Simulation Models from LMSI, Zycad and HDL Systems
- Peripheral Support Circuits from V3 and National Semiconductor
- Page Description Language interpreters from Peerless and Adobe Systems
- In-Circuit Emulators from Embedded Performance, Inc.
- Logic Analyzer support from Hewlett-Packard, Fluke Instruments, and Tektronix



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Integrated Device Technology, Inc.

## THIRD-PARTY DEVELOPMENT TOOLS AND APPLICATIONS SOFTWARE FOR IDT RISC PROCESSORS

### OVERVIEW

The MIPS/IDT RISC Microprocessor family is supported by a wide variety of third-party development tools and applications software. Many of these tools are software products, useful across the entire line of processors; others of these are hardware development tools, appropriate for one or two members to the family.

As the MIPS architecture is increasingly popular and successful, many new tools are constantly being announced. IDT encourages our customers to work closely with their local sales representative for a current list of third party support. This listing is current as of the date of this document.

Product Name	Vendor	Phone	FAX
<b>Software Development Tools</b>			
SDE-MIPS	Algorithmics, Ltd.	071-700-3301	44-71-700-3400
ANSI C-Cross Compiler	BSO/Tasking	617-320-9400	617-320-9212
Source Level Debugger	Case Tools	408-685-0336	408-685-0312
GNU C and C++ Cross Dev. System	Cygnus Support	415-903-1405	415-903-0122
C and C++ Cross Dev. System	Green Hills Software	805-965-6044	805-965-6343
C-Cross Development System	Metaware/Embedded	408-429-6382	408-429-9273
RISCCross C-Compiler System	MIPS Technologies, Inc.	415-390-4134	415-390-6170
<b>Ada Development Tools</b>			
RISC/Ada Cross Development System	Alslys	619-457-2700	619-452-2117
DACS MIPS Ada Cross Development	DDC-I	602-275-7172	602-275-7502
Ada Development System	Verdix Corporation	416-285-9188	416-285-9585
<b>Software Libraries</b>			
VDS Video Compression	Performance Computing, Inc.	503-297-2292	503-297-0878
GOFAST Floating Point Emulation Library	U.S. Software	503-641-8446	503-644-2413
<b>Real-Time Operating Systems</b>			
Nucleus Plus™	Accelerated Technology	205-450-0707	205-450-0404
C-Executive™	JMI Software Consultants	215-628-0840	215-628-0353
LynxOS™	Lynx Real Time Systems	408-354-7770	408-354-7085
VRTX-32	Ready Systems (VRTX)	408-736-2600	408-982-8266
SVR4	Unisoft	510-420-6400	510-420-6499
VxWorks™ 5.1 Real Time OS	Wind River Systems, Inc.	800-545-WIND	510-814-2010
Chorus Nucleus	Chorus Systems	503-690-2300	503-690-2320
<b>Logic Analyzers</b>			
ML-4400 Logic Analyzer	American Arium	714-731-1661	714-731-6344
CLAS 4000 Logic Analyzer	Biomation	408-988-6800	408-988-1647
Logic Analyzer Preprocessors (30xx)	Corelis	310-926-6727	310-404-6196
HP-16500 Logic Analysis System	Hewlett-Packard Co.	719-590-2825	719-590-3505
DAS 9200 and Prism 3000 Logic Analysis	Tektronix, Inc.	503-629-1964	503-645-8986

**THIRD PARTY DEVELOPMENT TOOLS AND APPLICATIONS SOFTWARE**

<b>Product Name</b>	<b>Vendor</b>	<b>Phone</b>	<b>FAX</b>
<b><i>In-Circuit Emulators</i></b>			
Sys-R3051 In-Circuit Emulator	Embedded Performance, Inc.	408-980-8833	408-980-9686
NetROM ROM Emulator	XLNT Designs, Inc.	619-487-9320	619-487-9768
<b><i>Evaluation Boards</i></b>			
79S460 Orion Evaluation Board	Algorhythmics, Ltd.	071-700-3301	44-71-700-3400
R30xx and R4x00 Single-Board Computers	Heurikon	800-356-9602	608-831-4249
Single-Board Computers	Omnibyte Corporation	800-638-5022	708-231-7042
R30xx Single-Board Computers	RISQ Modular Systems	510-490-0732	510-490-7225
R30xx Single-Board Computers	AEON	505-828-9120	505-828-9115
EISA Multifunction I/O Board	VigilantTechnologies, Inc.	305-741-4478	305-741-7655
<b><i>Simulation Tools/Models</i></b>			
Timing Designer	Chronology Corporation		
Smart Model and Logic Model Libraries	Logic Modelling Corporation	503-690-6900	503-690-6906
IdeaStation and Quicksim II	Mentor Graphics	800-547-3000	503-685-1214
ASIC Emulation Systems	PIE Design Systems	408-738-8899	408-738-8853
Model Bank	Protocol (Zycad)	201-347-7900	201-347-8525
ASIC Emulation Systems	Quickturn Systems	415-967-3300	415-967-3199
	ViewLogic Systems	508-480-0881	508-480-0882
Soft RISC Simulator	HDL Systems	408-522-2600	408-522-2626
<b><i>Support Components</i></b>			
PICA Chipset	Acer America Corporation	408-433-4950	408-434-8517
LogiCore Chipset	DeskStation Technology	913-599-1900	913-599-4024
	Spacelabs	206-882-3700	206-885-3619
	V3 Corporation	416-285-9188	416-285-9585
R30xx Support Chipset	Visual Technology	508-836-4400	508-336-4337
R4xxx Support Chipset	Mentor Arc	510-656-0100	510-656-3246
<b><i>Consulting/Design Services</i></b>			
Hardware/Software Design Services	IDT RISC Subsystems	408-492-5627	408-988-5600
Hardware/Software Design Services	RISQ Modular Systems	510-490-0732	510-490-7225
<b><i>Page Description Languages</i></b>			
Postscript™	Adobe Systems, Inc	415-961-4400	415-961-3769
Peerless Page™	Peerless Systems Corporation	310-536-0908	310-536-0058
Phoenix Page™	Phoenix Technologies, Ltd.	617-551-5030	617-661-4802
	Pipeline Associates	201-267-3840	201-267-3715



Integrated Device Technology, Inc.

## TRAINING CLASS APPLICATIONS DEVELOPMENT WITH THE IDT R3041™/R3051™/R3081™ RISControllers™

### OVERVIEW

IDT offers a training class intended to provide in-depth knowledge on the use and capabilities of the R3041™/R3051™/R3081™ family of processors. The class is intended to provide an accurate basis for device evaluation, as well as to provide a design engineer with the ability to rapidly bring an R3041/51/81-based application to production.

The class is thus intended for engineers who are designing with the processor family, and who wish to minimize time to market. It is also appropriate for customers performing a detailed processor survey prior to device selection.

### COURSE CONTENTS

The course provides a detailed discussion, including hands-on workshops, of both the hardware and software considerations appropriate to applications development. While the

course does assume basic familiarity with hardware and software development, the course does not assume previous RISC training or experience.

The course prepares the participant to create designs around the R3051 family through detailed lecture and workshops. The programming environment is reviewed, as are various hardware price-performance trade-offs.

A detailed outline of the course is contained on the next page.

### COURSE LOCATION AND SCHEDULE

The course is held on three consecutive days at our Santa Clara, California facility. Directions, accommodations, and schedule information is available from your local sales representative.

## DAY 1

### Device Overview

- CPU Integer Unit
- Floating Point Accelerator
- System Control Co-Processor
- On-chip Caches
- System Interface

### Instruction Set Architecture

- Overview
- Register Model
- Instruction Set Details
- Co-processor Operations
- Native and Synthetic Instructions
- Pipeline Dependencies

### IDT/sim Prom Monitor

- Overview
- Commands
- Instruction decoding
- Program Assembly

### Cache Architecture

- Cache Architecture
- Operation
- Flushing
- Performance

### Memory Management

- Overview
- Virtual to Physical Address Translation
- TLB Operation

### Exception Handling

- Precise Exception Model
- Exception Processing
- Software Techniques
- Exception Latency
- Special Techniques

## DAY 2

### System Interface

- Operations Priority
- Execution Engine Fundamentals
- Read Interface
- Write Interface
- DMA Interface
- Reset Interface

### Using IDT/umonitor for System Bring-up

### 7RS385 Evaluation Board Design Review

- Board Overview
- Memory Timing
- I/O Timing

### System Design Topics

- Address Map Considerations
- Input Clock Considerations
- Reset Timing
- Output Loading
- System Clock State Machines
- Multiple Master Systems
- 0 Wait State Systems
- Bus Turn Around
- Using Ack and RdCEn
- Designing with DRAM Controllers
- R3041/51/81 Compatibility

## DAY 3

### High-Level Language Program Development

- Compiler Optimization overview
- Tool chain usage and example
- Host to Target Connections
- HLL to ASM Interface

### Source Level Debugging

### Software Development and Integration

- Getting a Prototype Running
- R3081 Utility Program Example
- IDT/kit

### Floating Point Options

- Software Emulation
- Hardware Floating Point



Integrated Device Technology, Inc.

# CENTAURUS LASER PRINTER CONTROLLER R3051™ FAMILY REFERENCE PLATFORM FOR PostScript™ Level 2 SOFTWARE FROM ADOBE®

PRELIMINARY  
IDT79S389

## FEATURES

- Software-ready laser printer controller suitable for Adobe OEMs developing PostScript Level 2 products
- IDT/Adobe demonstration platform for PostScript Level 2 software running on IDT's R3051 RISCController™ family
- IDT/OEM R3041™/R3051/R3081™ based prototyping target and reference design (25MHz)
- Uses IDT79R3721 DRAM Controller and IDT73720 Bus Exchangers
- Options for two-way interleaved or non-interleaved (jumpers) DRAM memory system
  - Up to 16MB DRAM (four 72-pin sockets; 1MB or 4MB SIMMs)
  - 4 non-interleaved banks or 2 two-way interleaved banks
- Options for two-way interleaved or non-interleaved EPROM/ROM memory system
  - Up to 4MB ROM (8 32-pin sockets; 1, 2 or 4Mb EPROM/ROMs)
  - 2 non-interleaved banks or 1 two-way interleaved bank
- 512 bytes serial EEROM
- Programmable DUART (85C30) with RS232C and Apple-Talk® ports
- SCSI Controller (53C80) with one SCSI port (2 connector locations)
- Centronics parallel input port
- Adobe reference front panel interface (based on Canon LBP-8 MARKIIIR 6-button/LCD/LED front panel)
- IDT FIFO-based Canon video interface to LBP-SX/RX engines
- Clock, reset and interrupt generation logic
- Expansion bus connector for:
  - Custom engine interfaces (600dpi, color, etc.)
  - Additional I/O (Ethernet, Adobe FAX, etc.)
  - Additional font ROM space
- Shipped with IDT/sim™ initialization and monitor debug software (PostScript EPROMs available from Adobe)
- Executes various Adobe software (provided only under license from Adobe Systems Incorporated), including:
  - Adobe's high-level and low-level monitors
  - Adobe Print Architecture
  - Adobe's PostScript Level 2 Interpreter

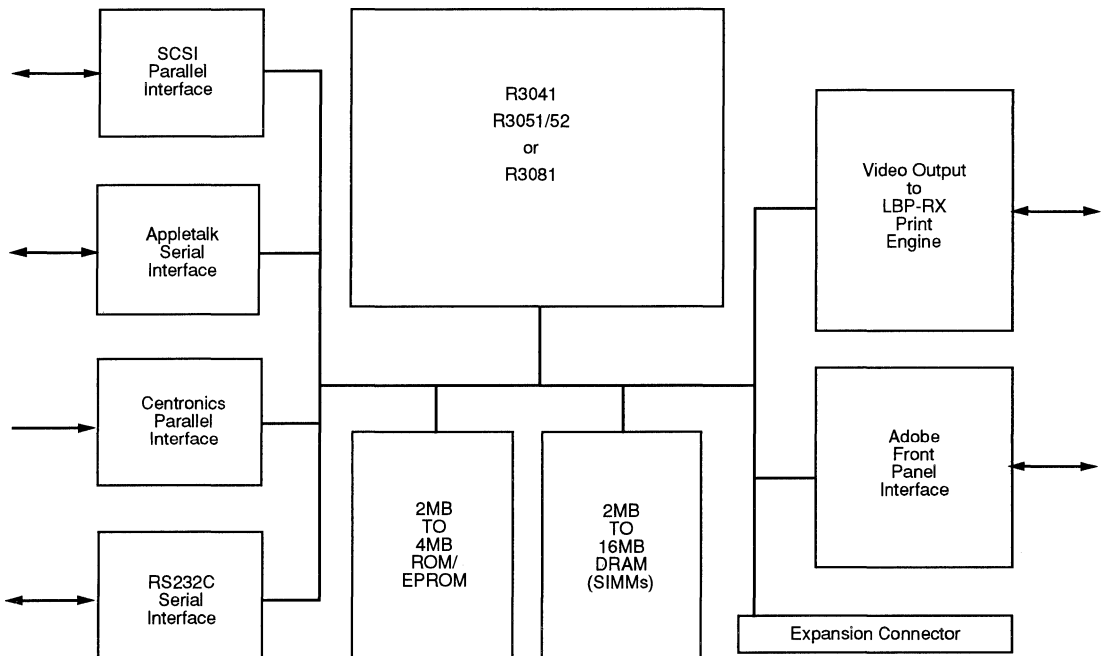


Figure 1. IDT79S389 Block Diagram

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MARCH 1994



## INTRODUCTION

The IDT79S389 provides an R3051 family laser printer controller reference platform for rapid adaptation into OEM differentiated products using PostScript Level 2 software from Adobe. "Reference platform" means that IDT and Adobe engineers have jointly developed both hardware and software modules for the specified configuration. This provides a baseline hardware and software design to accelerate time-to-market where changes can be limited to one or two areas (form factor, engine interface or I/O options), without having to start at the beginning.

Since the IDT R3051 family includes pin-compatible members with and without floating point accelerator hardware on chip, Adobe software licensees will be able to obtain "core PostScript" binaries in two versions: one compiled with the MIPS C-compiler assuming the presence of the FPA (for IDT79R3081), and another version based on IDT's floating point emulation libraries (for IDT79R3041, R3051 and R3052).

The IDT79S389 is completely self contained, and is intended for use either on the desktop, or installed inside a variety of Canon print engines; e.g. Canon OEM engines LBP-SX and LBP-RX, Canon LBP-8 MARKIII R and HP LaserJet III. The IDT79S389 fits into any of the above engine mounting locations, including the standard power supply and video interface connections. For evaluation on the desktop, a PC-style 4-pin power supply connector is also provided. Figure 1 illustrates the simplified block diagram of the IDT79S389 Reference Platform.

The IDT79S389 Reference Platform is designed around the R3051 RISController family, including the IDT79R3081 and the R3041. All devices in the R3051 family are pin- and software-compatible. As a consequence, R3041, R3051E, R3052, R3052E, R3081 and R3081E can be substituted for the R3051 throughout this manual. For details on the R3051 family refer to the data sheets and hardware user manuals.

## SYSTEM OVERVIEW

Figure 2 illustrates a high-level schematic of the data paths and various subsystems of the board. The user's manual that ships with the board provides extensive detail on the board, including complete schematics, PAL equations, and theory of operation.

### Address and Data Path

The R3051 family uses a time multiplexed address and data bus. The IDT79S389 demultiplexes this bus into an address bus and two data buses. The use of two data buses both minimizes the loading of the buses, and allows either or both of the EPROM and DRAM subsystems to be interleaved.

The address path is constructed using IDT 74FCT162373 16-bit wide transparent latches, and is de-multiplexed off the A/D bus using the processor supplied ALE output signal.

The data paths are provided by a pair of IDT 73720 Bus Exchangers. The 73720 in general is a 3-port, 16-bit wide transceiver, used to multiplex a common CPU port between two data ports (typically found in two way interleaved sys-

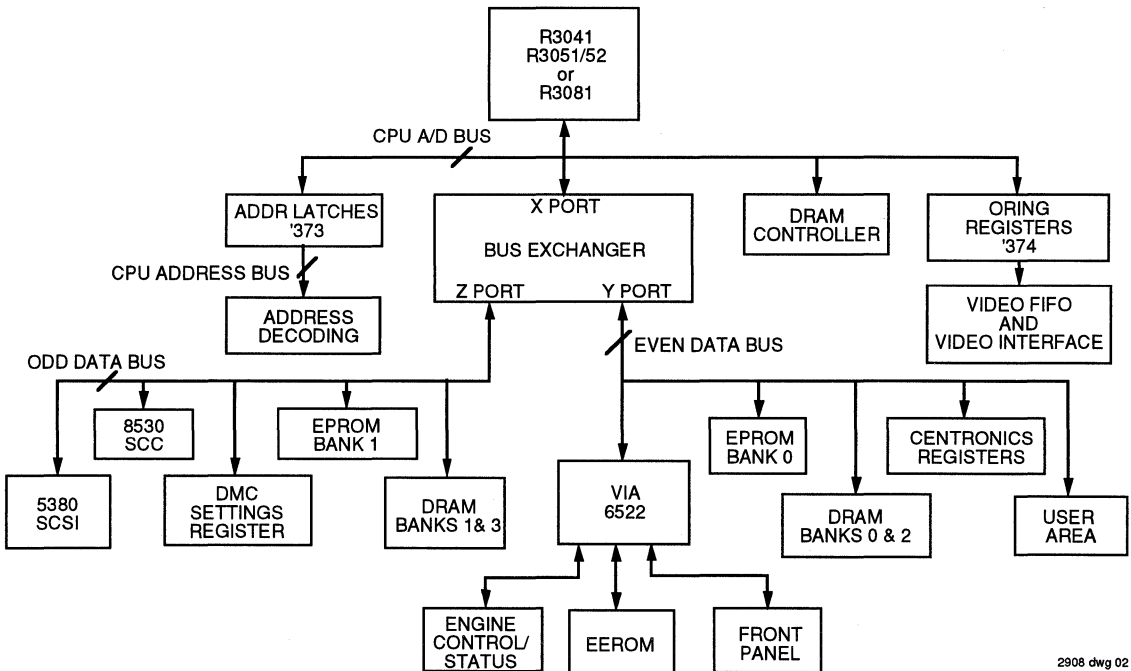


Figure 2. IDT79S389 High Level Schematics

	1MB SIMM non-interleaved	1MB SIMM interleaved	4MB SIMM non-interleaved	4MB SIMM interleaved
<b>Bank 0</b>	0x0080_0000 -> 0x008F_FFFF	0x0080_0000 -> 0x009F_FFFF (even)	0x0080_0000 -> 0x00BF_FFFF	0x0080_0000 -> 0x00FF_FFFF (even)
<b>Bank 1</b>	0x0090_0000 -> 0x009F_FFFF	0x0080_0000 -> 0x009F_FFFF (odd)	0x00C0_0000 -> 0x00FF_FFFF	0x0080_0000 -> 0x00FF_FFFF (odd)
<b>Bank 2</b>	0x00A0_0000 -> 0x00AF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (even)	0x0100_0000 -> 0x013F_FFFF	0x0100_0000 -> 0x017F_FFFF (even)
<b>Bank 3</b>	0x00B0_0000 -> 0x00BF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (odd)	0x0140_0000 -> 0x017F_FFFF	0x0100_0000 -> 0x017F_FFFF (odd)

Table 1. DRAM Memory Map

tems). The control of the 73720 Bus Exchangers is performed by a dedicated PAL, which directs transfers between the CPU and the appropriate data bus, and insures that bus conflicts are avoided.

**State Machines**

The IDT79S389 uses a distributed state machine structure to implement control of the various peripheral subsystems. In this structure, each peripheral subsystem has dedicated control PALs associated with it. These PALs monitor the start of a transaction, and either ignore the transaction (if intended for other subsystems), or provide the appropriate control responses back to the processor at the appropriate times, according to the latency of the targeted subsystem. A master PAL generates a common "Cycle End" indicator to all state machines, indicating that they can await another transaction.

The advantage of this distributed state machine structure is that memory subsystems can be independently added, removed, or modified, without impacting the rest of the system. This simplifies end user customizing and system debug.

The disadvantage of this structure is that the number of PALs required is larger than if the state machines were centralized. It is expected that customers using this as a reference design would customize and/or cost reduce the state machines and I/O subsystems, using interface ASICs, ASSPs, or condensed PALs.

In addition to the distributed state machines, the IDT79S389 contains a number of PALs providing common functions to all state machines. These functions include address decoding, Cycle End generation, data path steering logic, bus timeout, and CPU input/response synchronization.

**CPU Subsystem**

The IDT79S389 board incorporates the standard R3051 family PLCC footprint. It is targeted to run at 25MHz, although its frequency may be scaled up or down, as appropriate. Note that when scaling frequency, the user should reprogram the wait states associated with the various memory and peripheral subsystems, and may need or choose to use faster or slower control and memory devices. The board and software do not require the use of a TLB.

**DRAM Subsystem**

The DRAM subsystem of the IDT79S389 board supports the use of 256K x 32 or 1M x 32 72-pin SIMM memories. Up to 4 SIMMs may be used, for a maximum of 16MB of DRAM memory. The memory can be interleaved or non-interleaved, according to a set of DIP switches.

The DRAM system is controlled by the IDT79R3721 DRAM controller. This device features an R3051 family bus interface, and implements direct control of the DRAM devices. The timing and configuration of the DRAMs is programmable in the R3721, according to the settings of an internal mode register.

To maximize user flexibility without requiring PROM changes, the IDT79S389 memory maps a set of DIP switches, called the MSEL switches. At system startup, the value of these switches is read by the CPU and then written to the IDT79R3721 DRAM controller, to configure the system timing model. Thus, in order to change the memory configuration or timing, the user merely needs to set the DIP switches and reset the board.

The DRAM memory is memory mapped to the address space 0x0080\_0000 to 0x017F\_FFFF, depending on the size of SIMM, number of SIMMs, and interleaving chosen. Table 1 illustrates the address map, depending on configuration. Table 2 illustrates the read and write latency (measured in clock cycles) of the various memory configurations, assuming 80ns SIMMs and a 25MHz system.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	1	2
Non-page Write	4	4
Page Write	3	3

Table 2. Number of Clock Cycles for Various DRAM Transfers

The IDT79S389 board is shipped with two 1MB 80ns SIMMs in a non-interleaved configuration. Additional SIMMs can be added by the user, and interleaving can easily be selected.

	1Mb EPROM	2Mb EPROM	4Mb EPROM
<b>Bank 0</b> (non-interleaved)	0x1FC0_0000 -> 0x1FC7_FFFF	0x1FC0_0000 -> 0x1FCF_FFFF	0x1FC0_0000 -> 0x1FDF_FFFF
<b>Bank 1</b> (non-interleaved)	0x1FC8_0000 -> 0x1FCF_FFFF	0x1FD0_0000 -> 0x1FDF_FFFF	0x1FE0_0000 -> 0x1FFF_FFFF
<b>Bank 0</b> (Interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (even)	0x1FC0_0000 -> 0x1FDF_FFFF (even)	0x1FC0_0000 -> 0x1FFF_FFFF (even)
<b>Bank 1</b> (Interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (odd)	0x1FC0_0000 -> 0x1FDF_FFFF (odd)	0x1FC0_0000 -> 0x1FFF_FFFF (odd)

Table 3. EPROM Address Map

**EPROM Subsystem**

The EPROM subsystem contains 8 sockets, capable of accepting 1Mb, 2Mb, or 4Mb devices. The sockets accept 8-bit wide EPROMs in the DIP package.

The board can be used with either 4 or 8 EPROM devices; if 8 devices are used, Interleaved or non-interleaved operation can be selected. The density of EPROM, and the interleaving factor, are selected via jumpers and PALs for the board. The board ships with 512KB of 120ns EPROM installed in a single bank; the EPROMs contain the IDT/sim monitor program ported to this board.

The EPROMs reside in the physical address range 0x1FC0\_0000 through 0x1FFF\_FFFF. This address space includes the system exception vectors, as well as the bootup code, and can be accessed either through or around the on-chip processor cache, according to the virtual address used. Table 3 shows the physical address map for the EPROMs. Table 4 shows the memory latency of the EPROM subsystem, for 120ns EPROMs and a 25MHz system.

**SCSI Subsystem**

The IDT79S389 board contains a single SCSI channel, implemented using the 53C80 SCSI controller. Although there is only one channel, there are two SCSI connectors on the board, to support the differences in the form factor of the various laser engines supported.

The SCSI device resides in the address range 0x0074\_0000 through 0x0074\_FFFF.

**Serial Channels Subsystem**

The IDT79S389 board implements two serial channels. One is a traditional RS-232 channel, and is accessed by a DB-25 connector. The other channel supports AppleTalk, and uses the standard AppleTalk connector. The board includes voltage translators and transceivers to implement the electrical protocols required by these standards.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	4	1.6 (1-3-1)

Table 4. Number of Clock Cycles for Various EPROM Transfers

The serial channels are implemented using a single 85C30 SCC serial controller. The address space for the serial controller is 0x0073\_0000 through 0x0073\_FFFF.

**EEROM Interface**

The IDT79S389 board includes a 512B EEROM to store various configuration data. The EEROM is accessed by the 65C22 VIA device, which is memory mapped to 0x0071\_0000 through 0x0071\_FFFF.

**Centronics Interface**

The board also includes a unidirectional Centronics port. Centronics data is read from address space 0x0075\_0000 through 0x0075\_FFFF; Centronics status is written in the address space 0x0076\_0000 through 0x0076\_FFFF.

**Front Panel Interface**

The front panel interface corresponds to a Canon LBP-8 Mark IIIR, and uses a series of switches, LEDs, and LCDs to implement front panel control. Front panel is accessed by the 65C22 VIA device, which is memory mapped to 0x0071\_0000 through 0x0071\_FFFF.

**Video Interface**

The video interface corresponds to the interface requires for the Canon LBP-8 Mark IIIR, based on the Canon LBP-RX print engine. The video interface is implemented using discrete logic, with status taken from the 65C22.

Video data is sent to the video interface by performing an aliased read of the DRAM memory. If a processor read of the 16MB region starting at 0x0880\_0000 is detected, the access will be processed as a DRAM read. However, the read data returned from the DRAM will be captured by the video interface, and later shifted out to the print engine. This technique eliminates overhead by not requiring the processor to explicitly write the data to the video channel.

**User Expansion Area**

In addition to the memory systems described above, the IDT79S389 board contains a user expansion connector. The user expansion connector allows users to add custom features to the board for software development. Features which could be added might include an Ethernet channel, additional font ROM, or a different engine and front panel interface.

The IDT79S389 board provides a User Chip Select, mapped to address 0x0078\_0000 through 0x0078\_FFFF, for use with the expansion connector.

**Board Form Factor**

The form factor and hole placement of the board allows it to be directly mounted into either a Canon LBP-8 Mark IIIR laser printer, the HP LaserJet III, or the Canon OEM print engines LBP-SX or LBP-RX engines. The placement of the video, front panel, and power connectors, are compatible with these form factors.

In addition, the board can be run on a benchtop using a standard PC compatible power supply. If the board is used in this fashion to drive an engine, it is recommended that a common ground between the board and the engine be provided.

**Summary: Address Map and Interrupt Assignment**

Table 5 is a summary of the address map of the IDT79S389 board. Table 6 shows the interrupt assignments of the CPU.

Memory Subsystem	Start Address	End Address
VIA	0x0071_0000	0x0071_FFFF
SCC	0x0073_0000	0x0073_FFFF
SCSI	0x0074_0000	0x0074_FFFF
Centronics Data	0x0075_0000	0x0075_FFFF
Centronics Status	0x0076_0000	0x0076_FFFF
User Chip Select	0x0078_0000	0x0078_FFFF
MSEL Switches	0x0079_0000	0x0079_FFFF
R3721 Mode Register	0x007A_0000	0x007A_FFFF
DRAM	0x0080_0000	0x017F_FFFF
Aliased Video DRAM	0x0880_0000	0x097F_FFFF
EPROM	0x1FC0_0000	0x1FFF_FFFF

Table 5. IDT79S389 Memory Map Summary

Device	CPU Interrupt
Reserved	Int(0)
R3081 Floating Point	Int(1)
VIA	Int(2)
HFull/Video Reset	Int(3)
SCSI	Int(4)
SCC	Int(5)

Table 6. IDT79S389 Interrupt Assignment

**SPECIFICATION SUMMARY**

**Order Number:** IDT79S389

**Maximum on board memory capacity:**

**DRAM** Four 72-pin SIMM sockets for 256K x 32 or 1M x 32 (1 to 16MB)  
**EPROM** Eight 32-pin sockets for 128K x 8 to 512K x 8 (to 4MB)  
**Serial EEROM** One 8-pin socket for serial EEROM (512bytes)

**Debug Monitor EPROM:**

IDT/sim Version 4.0 ported to IDT79S389

**Serial Ports:**

**Serial** Controlled by 85C30 DUART. CRT terminal connector or for downloading J3 (25-pin AMP 748133-1,DB25S, right angle female).  
**Appletalk** AppleTalk connector J2 (8-pin AMP 749179-1, D8 8, right angle female).

**Parallel port:**

**Centronics** 36-pin, female, right angle, standard Centronics parallel connector (R.Nugent RPM-C36SB-SR-TG).

**SCSI port:**

Controlled by 53C80 SCSI controller. SCSI connector J5 or J10 (50-pin, female, right angle, (R.Nugent RPM-C50SB-SR-TG).

**Video:**

Standard 20-pin, male Canon LBP-RX video interface connector (HIROSE PCN-10-20P 2.54DSA).

**Front Panel:**

J7, 34-pin male, right angle connector (AMP 1-103149-7).

**Expansion:**

Four 40-pin male, four wall headers, J11-14 (MOLEX 39-26-7404).

**Physical:**

Compatible with Canon RX, SX engine form factors.

**Operating Temp:**

0–50°C.

**Power Supply:**

5.0V ± 5%, 3 Amps typical (estimate).



## PHYSICAL LAYOUT

The physical layout of the IDT79S389 Reference Platform reflects the board's primary objectives:

1. Software delivery vehicle for PostScript Level 2 software from Adobe
  - Memory space appropriate for PostScript Level 2 software typical implementations,
  - Various memory configurations (interleaved vs non-interleaved, code running out of DRAM or out of ROM) to easily evaluate cost and performance alternatives.
2. Cost-Effective design model for IDT79R3051 RiSController family
  - NO zero-wait-state memory,
  - Minimum complexity board configuration (6 layers),
  - Fits industry standard Canon LBP-RX print engine.
3. Advanced hardware starting point for rapid evaluation, cost-performance point analysis and development of OEM finished products.
4. Advanced software-ready controller, suitable for immediate development with PostScript Level 2 software from Adobe, and adaptation to other print engines and communications ports (Adobe software available only under license from Adobe Systems Incorporated).

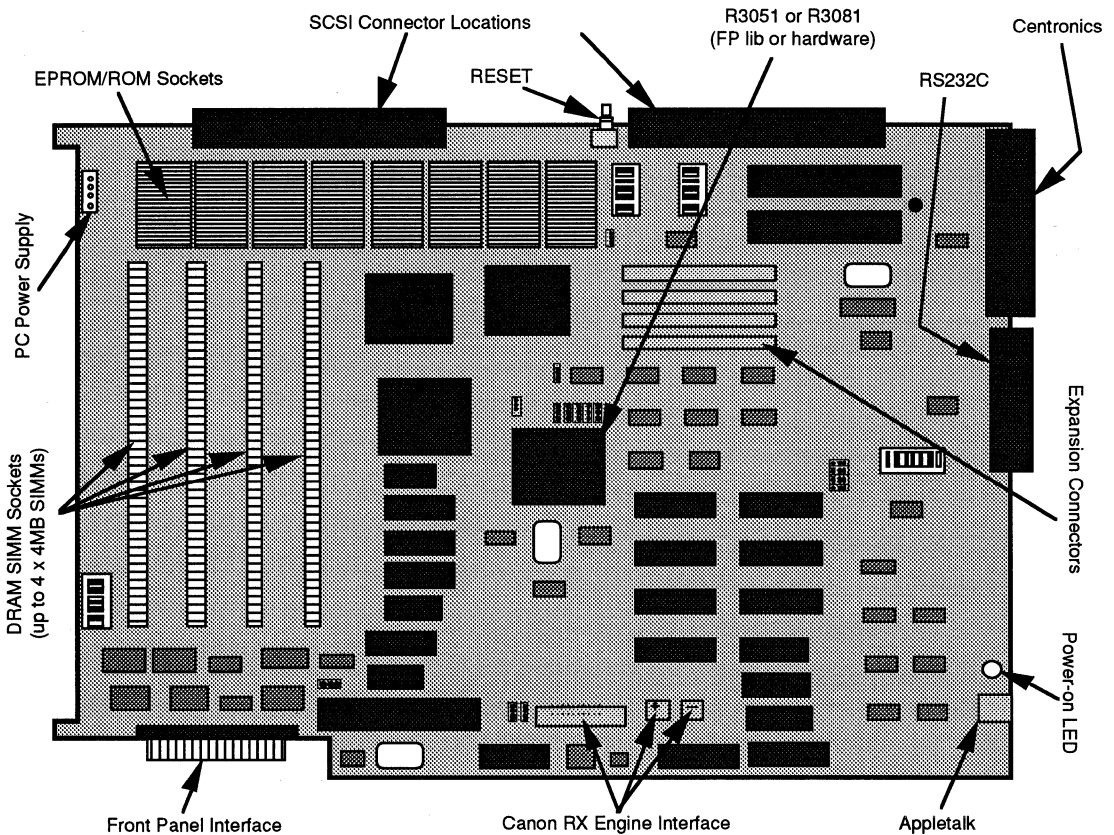


Figure 3. IDT79S389 Board Layout

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## ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's guide includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R3081 CPU plugged in, but samples of the R3052 and R3041 are provided. The R3051 can also be ordered to allow user upgrades.

### Evaluation Boards

**R30XX Evaluation Kit .....79S389**



Integrated Device Technology, Inc.

## R3051™ FAMILY EVALUATION KIT

IDT79S385A

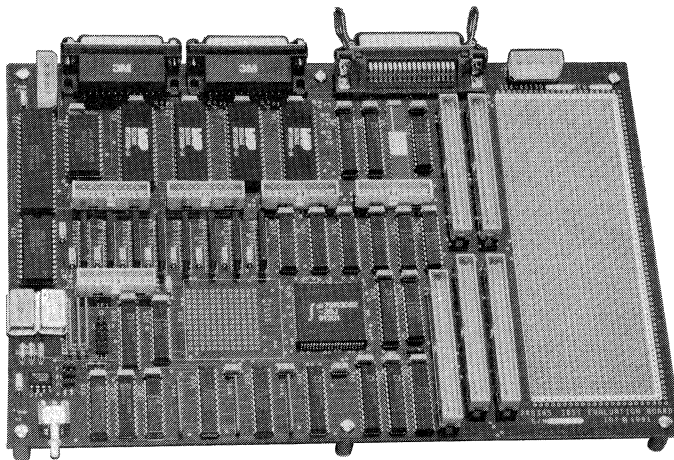
### FEATURES:

- Complete 25MHz RISC System Board
  - Requires only 5V supply and terminal to operate
  - Supports R3041™, R3051, R3052™, or R3081™ highly integrated RISC CPUs
  - Board contains an IDT79R3052E
  - 1MB of non-interleaved DRAM, expandable to 4MB
  - 128KB of EPROM, expandable to 2MB
  - Serial and Parallel Ports
  - Connectors provided for easy connection to HP Logic Analyzer
  - Wire-wrap area on the board
- IDT/c™ for IBM PC compatibles included in kit
  - Hardware or software floating point
  - Remote symbolic debug
- IDT's System Integration Manager (IDT/sim™) included in EPROM
  - High capability debug monitor
  - Simplifies software development

- Complete set of documentation included
  - Supplied with complete set of board schematics
  - PAL equations supplied on IBM PC 3.5" disks
  - User's manuals for R3051 family, IDT/sim, and IDT/c
- Utility programs also included
  - Program utility disk
  - HP16500A Logic Analyzer disassembly software
- R3081 sample also included for board upgrade

### DESCRIPTION:

The IDT79S385A Evaluation Kit is a complete kit for evaluating the R3051 hardware and software environment. The kit contains a working system, including all schematics and theory of operation, an R3081 sample to allow the user to upgrade the system capabilities, and a complete software development environment, including debug monitor and "C" compiler/assembler toolchain. Finally, the kit is complemented by documentation, logic analyzer software, and utility programs.



IDT79S385 RISC System Board. Actual Size 8.5" x 11"

The IDT logo is a registered trademark and R3051, R3041, and R3081 are trademarks of Integrated Device Technology, Inc.

MARCH 1994

## COMPLETE SINGLE BOARD COMPUTER

The 79S385 board is a complete working RISC system intended as a complete design example using the R3051 family of highly integrated RISC CPUs. The board requires only a simple CRT terminal and a 5V power supply for operation. Figure 2 shows a block diagram of the 79S385 board.

The board is designed around IDT's R3051 family of highly integrated RISC CPUs. An R3052E CPU chip (8KB I-cache and 2KB D-cache, with on-chip TLB) is included in a socket, but any member of the family can be substituted. The 79S385A kit includes a sample of a 25MHz R3081 in a PGA pinout, to allow the user to upgrade the system. A large wire-wrap area is available on the board for adding additional hardware. All the schematics and details of the designs are supplied with the board, including all PAL equations on an IBM format 3.5" disk.

The 79S385 board is supplied with 1MB of DRAM in socketed 256K x 4 ZIPs; the ZIPs can be replaced with 4MB devices to obtain 4MB of DRAM on the board (an applications brief on upgrading memory is included in the kit). Other hardware on board includes a 2681 DUART and an 8254 counter/timer; both these devices are supported with drivers in IDT/sim. A parallel Centronics port is available for higher speed download of code into the board.

The board contains 128KB of EPROM expandable to 2MB by replacing the EPROMs with higher density devices. The EPROMs contain IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing, and I/O.

There are two serial ports, a free-running programmable timer, and a parallel Centronics port for high-speed down-

load of software. A set of expansion connectors permits external hardware to be connected to the board, and a wire-wrap area on the board can be used to build additional hardware without using a second board.

The board is designed to be placed on a flat table-top surface. Standoffs are provided for physical support.

The 3051 Bus, along with other control signals, is connected to a set of pins in the center of the board next to the wire wrap area. These signals can be used to connect additional hardware on either the wire-wrap area or on another board via a ribbon cable. DMA control is provided. Table 1 shows the signal description for the expansion connector.

## IDT/SIM DEBUG MONITOR SOFTWARE

IDT's System Integration Manager (IDT/sim) is included in EPROMs on the board. This software permits downloading of code from a host system, execution control with breakpoints, in-line assembly and disassembly, and a variety of commands to control main memory, cache memory, and the internal TLB. It provides all the resources needed to bring up new hardware and software.

The evaluation kit also includes a complete set of user documentation for the IDT/sim software tool. The capabilities of IDT/sim are described in a separate data sheet.

## IDT/C "C" COMPILER FOR IBM PC COMPATIBLES

In addition, the evaluation kit contains a complete copy of the IDT/c software development toolchain, hosted on IBM PC compatible computers. IDT/c, described in a separate data sheet, includes:

- The ability to generate big- or little-endian code

Signal Name	I or O	Description
EA00-EA31	I/O	32-bit buffered address bus
ED00-ED31	I/O	32-bit buffered data bus
SYSOUT	O	Buffered SYSCLK Clock from CPU; used to synchronize data transfers
MRES#	O	Copy of the Reset signal to the CPU
MREQ	O	Memory Request output (handshaking signal for data transfers)
EXACK#	I	Acknowledge input (handshaking for data transfers)
IP4-IP5	I	Auxillary input pin to the 2681 UART
WEA-WED	O	Write Enables for the four bytes of the data word
UCS	O	Chip select signal decoded from the high order address bits for external hardware
INT0:INT5	I	Interrupt inputs to the R3052
RD#	O	Memory Read output signal from the 3052
WR#	O	Memory Write output signal from the 3052
BREQ#	I	Bus Request input to the 3052
BUSGNT#	O	Bus Grant output from the 3052

Table 1. Signals Supplied on Expansion Connector

2885 tbl 01





## BOARD SPECIFICATIONS

### CPU

25MHz R3052E on board  
25MHz R3081 sample included

### Cache Ram

8KB I-cache, 2KB D-cache (in 3052 chip)  
16KB I-Cache, 4KB D-Cache configurable to  
8KB I-Cache, 8KB-DCache (in R3081 chip)

### Cacheable Address Space

4GB

### DMA Support

Bi-directional tri-stateable buffers can be used to  
write to DRAM from external logic

### Block Refill

4 word instruction block size  
1 or 4 word data block size programmable via jumper

### Endianness (Byte Ordering)

User programmable via jumper

### Read/Write Buffers

Both are 4 words deep (inside R3052 chip)

### Interrupts

6 User Interrupts, three synchronized with SYSCLK

### I/O characteristics

TTL levels from FCT logic devices, PALs and R3052

### Power Supply

2 amps (typical) at 5V, 25°C, at rated speed

### Environmental Conditions

Ambient temperature 0°C to +50°C  
Relative Humidity 5% to 95%

### Clock Frequency

25MHz

### Interconnection

Five 50-pin connectors, containing Address, Data, and  
Control signals and R3052 signals  
Five 20-pin plugs for use with HP logic analyzer  
Two RS-232 serial ports on DB-25 connectors  
One parallel Centronics port for input

### User Selectable Options

Endianness, data block refill size  
Tri-State mode of 3052

## ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R3052E CPU plugged in, but any member of the 3051 family can be used. An additional sample of the R3081 is included to allow user upgrades.

### Evaluation Boards

R3051 Family Evaluation Kit ..... 79S385A

### EPROM Upgrades

The following part numbers update the evaluation board hardware to the latest version of the IDT/sim monitor.

Evaluation boards ..... 7RS901BGP

*Use with 79S385 only*

### Auxillary Download Programs

For downloading code from a MIPS machine into an evaluation board. This software includes programs to convert MIPS object code into S-records and to download either ASCII or binary S-records to a remote target. This software is only needed if you are running the MIPS C-compiler and do not have SPP. If you are using IDT/c or you have IDT/sim or MIPS SPP you already have these utilities.

MIPS download utility ..... 7RS950BUU

*Supplied on QIC-24 TAR tape*



Integrated Device Technology, Inc.

## R3041™ EVALUATION KIT

IDT79S341

### FEATURES:

- Complete low-cost 20MHz RISC system
  - Plug-in AT-style card or stand alone mode
  - Supports the R3041™ highly-integrated, low-cost RISCController™ CPU
  - DRAM/memory controller logic implemented with a single low-cost PLA chip
  - Capability to test different hardware wait-state and clocking options
  - 128KBytes of boot EPROM expandable to 512KB
  - 1MByte DRAM expandable to 4MB
  - 8/16/32-bit wide DRAM array
  - Two Serial Ports
  - 16-bit external Counter/Timer
  - PC ISA interface logic
  - Connector provided for easy connection to a logic analyzer
- IDT/c™ for PC included in kit:
  - Software floating point emulation
  - Remote symbolic debug
- IDT's System Integration Manager (IDT/sim™) included in EPROM
  - On-board debug monitor
  - Simplifies software development
- IDT's PCIO16 Terminal Emulation Program (IDT/pcio16™) included in kit
  - Allows communication and downloading between the board and PC
- Complete set of documentation included
  - User's Manual for R3041 Evaluation board
  - Installation and operation guide for standalone and PC configurations
  - Design and theory of operation documentation
  - Includes complete set of board schematics and PLA equations
  - User's Manual for R3041, IDT/c, and IDT/sim
  - Application Guide for the R3051 Family

### FUNCTIONAL BLOCK DIAGRAM

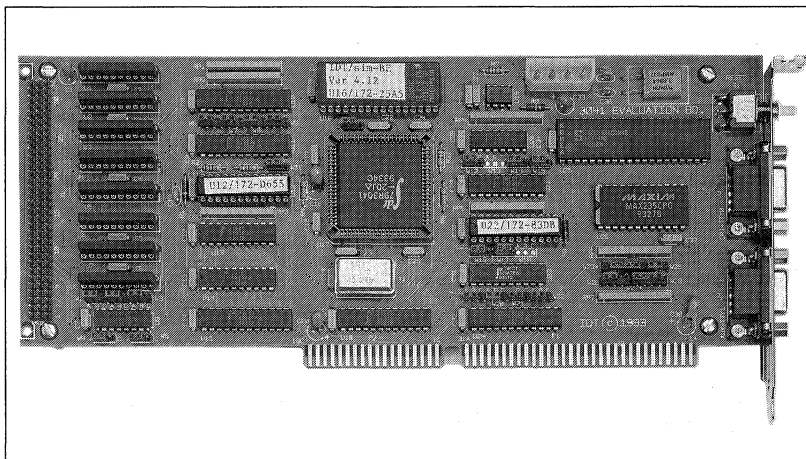


Figure 1. R3041 System Evaluation Board. Actual Size 4.2" x 10.0"

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## DESCRIPTION

The IDT79S341 Evaluation Kit is a complete kit for evaluating the R3041 hardware and software environment. The kit contains a working system, including a User's Manual with installation guide, schematics, PLA equations, theory of operation, and design notes. A complete software development environment, including debug monitor and "C" compiler/assembler toolchain for the PC is included. The kit also includes the R3041 User's Manual and the R3051 Family Applications Guide.

## COMPLETE SINGLE BOARD COMPUTER

The 79S341 Evaluation Board is an example of a complete working MIPS R3000-based RISC System. The board is a low-cost and parts-count design example using the highly integrated R3041 RISController CPU. Primary uses of the board include:

1. Evaluating the R3041 architecture.
2. Prototyping and running software.

The board is highly configurable and contains hardware options for state machine experiments as well as for setting different DRAM sizes, speeds and 32/16/8-bit memory widths.

The 79S341 Evaluation Board is designed around the IDT79R3041 RISController. The R3041 is a highly integrated low-cost version of the R3051 family of RISControllers and includes 2KB of on chip instruction and 512B of on chip data cache. The R3041 also contains memory controller support circuitry including programmable bus width, a refresh timer, read and write strobes, and address multiplexer controls. Thus on the 'S341 board, the DRAM controller, memory controller, and I/O controller are implemented externally within a single low-cost 24-pin PLA.

Although the R3041 can run in an R3051 family bus-compatible mode, on the 79S341 Evaluation Board, specific superset bus features of the R3041 are taken advantage of; for instance the 8-bit boot PROM capability, to reduce chip count and cost. Other boards, such as the IDT79S385A R3051 evaluation board kit, as described in a separate data sheet, can be used to demonstrate the R3041 using its R3051 bus-compatible mode.

The 79S341 Evaluation Board can be operated in one of two ways. In the default configuration as a standalone board, the 79S341 board requires only a standard RS232-C CRT video terminal and a 5V power supply for operation. The board can be placed on a flat table-top surface by using the remov-

able standoffs which are provided for physical support. The standoffs can be removed for the alternate configuration as a PC/AT ISA backplane add-in board. In this second configuration, the 79S341 Board only requires a PC/AT compatible personal computer. Using the IDT/pci16 PC/AT software program included in the kit provides a terminal emulator and downloader directly over the PC/AT backplane.

The 79S341 board contains a single 128K x 8 EPROM and can be upgraded to a user supplied 256K x 8 or 512K x 8 EPROM. Main memory consists of eight 256K x 4 (1Mb) DRAM ZIPs. There are two serial ports, one external timer in addition to the internal timer on the R3041, and a PC/AT backplane 16-bit I/O interface for downloading software. A logic analyzer connector permits external observation and evaluation of key CPU signals.

The boot EPROM contains IDT's System Integration Manager (IDT/sim), a debug monitor kernel that supports download of code from host systems, remote debug interface, execution control commands including single stepping and instruction tracing, memory probing, register probing, line-based assembly, and disassembly of code.

The board supports the use of 32/16/8-bit wide DRAM array configurations through the use of hardware jumper options. The board can be populated with either the default 1Mb DRAM ZIPs or with user supplied 4Mb DRAM ZIPs. Thus the board supports anywhere from 256KB to 4MB of main memory.

An IDT MacStation, SPARCstation, (or PC/AT) can be connected to the 79S341 via one of the serial ports and user developed code (generated using a cross-compiler such as GNU-C, MIPS-C, or the IDT/c compiler) can be downloaded to the board. In the add-in board mode, the 79S341 can be installed on the backplane of a PC/AT personal computer. Development can done completely from the PC/AT or downloads can be transferred from a workstation to the PC (via user supplied ethernet) and then through the PC/AT backplane of the 79S341. When used on the PC/AT backplane, additional server software which runs under MS-DOS is included, which allows CRT video emulation and program downloading via the PC/AT ISA backplane.

In addition, a logic analyzer connector is provided allowing additional hardware observability.

The 79S341 is constructed using through-hole devices on a 4-layer 4.2" x 10.0" PC/AT form factor compatible epoxy laminate board with standoffs and is intended either as a standalone bench top device or as a backplane add-in card.

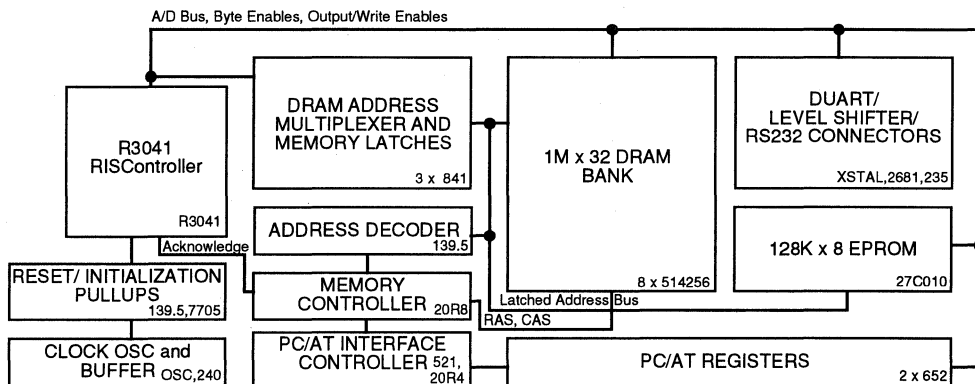


Figure 2. 79S341 Board Block Diagram

## IDT/C C-COMPILER FOR IBM PC COMPATIBLES

The evaluation kit contains a complete copy of the IDT/c software development toolchain, hosted on IBM PC-386/486 compatible computers. IDT/c, described in a separate data sheet, includes:

- ANSI-C optimizing compiler, assembler, linker, and librarian
- ANSI-C library support (source libraries available separately)
- Supports multiple memory segments for embedded system code
- Software floating point support
- Remote symbolic debug

## IDT/SIM DEBUG MONITOR SOFTWARE

IDT's System Integration Manager (IDT/sim) is included in an EPROM on the board. This software permits downloading of code from a host system, execution control with breakpoints, in-line assembly and disassembly, and a variety of commands to control registers, cache memory, and main memory. IDT/sim provides all the resources needed to bring up new hardware and software.

The evaluation kit also includes a complete set of user documentation for the IDT/sim software tool. The capabilities of IDT/sim are described in a separate data sheet.

## IDT/PCIO16 TERMINAL EMULATION AND DOWNLOAD UTILITY SOFTWARE

IDT's PC 16-bit I/O Terminal Emulation and Download Utility Software (IDT/pcio16) is included on an IBM PC compatible disk for use with an IBM PC AT-Bus compatible (ISA) machine. IDT/pcio16 allows the evaluation board to be operated from the PC/AT ISA backplane. The PC/AT acts as a video screen and keyboard terminal for the board by communicating through the backplane. IDT/pcio16 also includes download utilities to move s-record files from the PC/AT to the evaluation board.

## KIT SUMMARY

The IDT79S341 evaluation kit is a complete, low-cost package for evaluation of the R3041 RISC Controller and its software environment. The kit allows users to develop and execute high-level language "C" programs, to look at a software development toolchain for the IDT R3051 family, and to evaluate a low-cost hardware design using the R3041 RISC Controller.

## KIT CONTENTS

- 79S341 RISC Evaluation Board
- IDT/c Multi-Host compiler toolchain (IBM PC-compatible version)
- IDT/sim debug monitor included in board EPROM User's Manuals for:
  - 79S341 board
  - R3041
  - IDT/c
  - IDT/sim
  - Applications Guide for R3051 family
- IDT/pcio16 software on IBM PC compatible 3.5" disk format
- 6' cable for serial port from board for connection with 9-pin male or 25-pin male connector

**BOARD SPECIFICATIONS**

CPU 20MHZ R3041  
 On-chip 2KB l-cache, 512B D-cache

**On-Board Memory Capacity:**

As shipped (Minimum): DRAM — 256K x 32 (1MB)  
 EPROM — 128K x 8 (128KB)  
 Maximum: DRAM — 1M x 32 (4MB)  
 EPROM — 512K x 8 (512KB)  
 Debug Monitor EPROM: 128K x 8 (128KB) containing  
 IDT/sim.  
 Serial Ports: Controlled by SCN2681 DUART.  
 CRT Terminal connects to J3.

**Software configurable features.**

Default state: 9600 Baud, 8 bits, no parity,  
 1 stop bit.  
 AUX Download port connects to J4.

**Software configurable features:**

Default state: 9600 Baud, 8 bits, no parity,  
 1 stop bit.  
 Serial Port Connectors: Two DTE DB9s (right angle  
 female) connectors.

Timers: 1. Programmable counter/timer  
 16-bit timer on 2681 DUART.  
 2. On-chip R3041 24-bit timer used  
 for DRAM refresh timer.

Interrupts: 3 synchronized, 3 unsynchronized  
 (4 used on-board with 2 spares).

Expansion Connector: One 96p-pin Right angle (male)  
 DIN compatible. Connects with  
 96-PIN reverse DIN (female). Con-  
 tains R3052 A/D bus, control sig-  
 nals, and Buffered SysClk.

**User Selectable Options:**

Standalone vs. PC/AT ISA configuration, PC/AT ISA I/O  
 address, interrupt number, DRAM size, 32/16/8 DRAM width,  
 Boot PROM size, Endianess, cache vs. debug mode, Data  
 Block Refill size

**Physical Dimensions:**

PC/AT ISA Form Factor compatible: 4.2" x 10.0".  
 Operating Temperature: 0°C to 50°C  
 Relative Humidity: 5% - 95%  
 Power Supply: 5.0V ± 5%, 0.75Amps typical  
 Power Supply Connection (if used):  
 One 4-pin power supply  
 connector (4p-pin PC disk drive)

PC/AT Compatibility (if used): PC/AT 8.33MHz ISA Bus  
 backplane slot

PC/AT System Requirements (if used):  
 DOS 3.0 or higher, 640K memory,  
 3.5" floppy disk drive

**ORDERING INFORMATION**

Each kit is shipped with an evaluation board, complete  
 schematics and PLA equations, as well as a complete soft-  
 ware development toolchain for "C" language programming.  
 User's Manuals include instructions on compiling "C" pro-  
 grams, downloading code, and operating the Software Inte-  
 gration Manager.

Evaluation Board  
 R3041 Evaluation Kit.....79S341



Integrated Device Technology, Inc.

# R3081™ EVALUATION KIT

IDT79S381

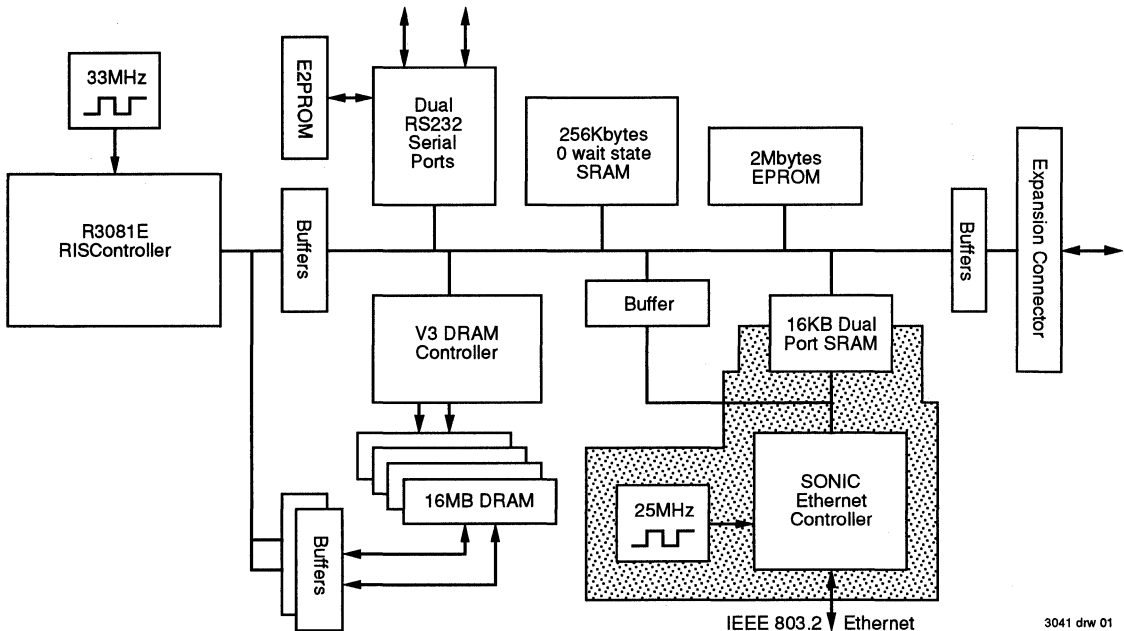
## FEATURES:

- Complete 33MHz RISC System Board
- Supports R3081™, R3051™, R3041™ CPUs
- Includes:
  - R3081 CPU, with R3041 and R3052™ samples
  - 2MB interleaved DRAM, expandable to 4MB, 8MB, or 16MB
  - 256KB zero-wait-state SRAM
  - 512KB of EPROM expandable to 1MB or 2MB
  - 1024-bit serial EEPROM
  - 2 serial ports
  - IEEE 802.3 Ethernet subsystem with 8KB dual-port SRAM expandable to 16KB
  - Expansion connector

## DESCRIPTION:

IDT's R3081 Evaluation Kit is a complete evaluation and development kit for IDT's R3051 family of RISControllers™. Designed to demonstrate the optimal performance of these RISControllers, zero-wait state memories allow one to see the true performance of IDT's R3041, R3051/2, and R3081 devices. For those developing large segments of code, the IEEE ethernet interface allows for quick downloading of large code blocks. The system supports up to 16MBytes of DRAM. On top of the system board with an on-board monitor, IDT's System Integration Manager (IDT/sim™), the complete package includes IDT's IDT/c compiler (IDT/c™), samples of our R3041 & R3052 devices, and a complete documentation package including a user's guide, board schematics, and PAL equations.

## FUNCTIONAL BLOCK DIAGRAM



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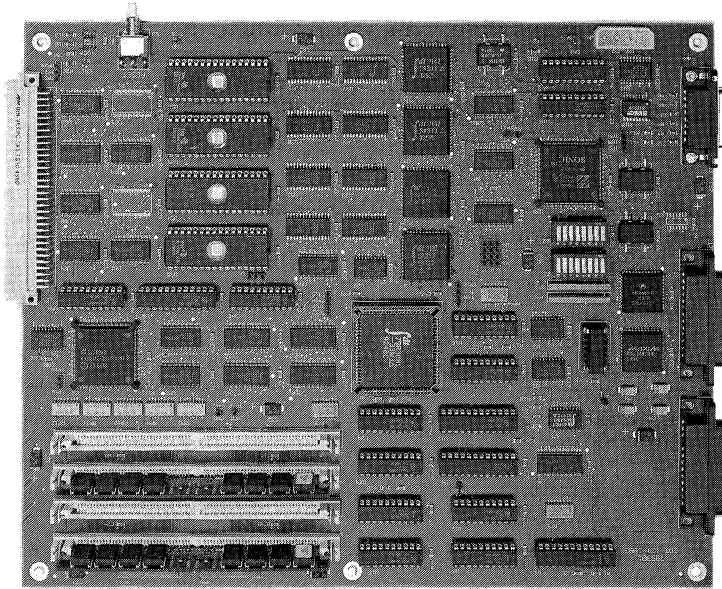
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MARCH 1994

**ORDERING INFORMATION**

Each kit is shipped with an evaluation board, complete schematics and PLA equations, as well as a complete software development toolchain for "C" language programming, downloading code, and operating the Software Integration Manager.

Evaluation Board  
R3081 Evaluation Kit.....79S381







Integrated Device Technology, Inc.

## Orion™ R4600™ EVALUATION and DEVELOPMENT PLATFORM

Preliminary  
79S460

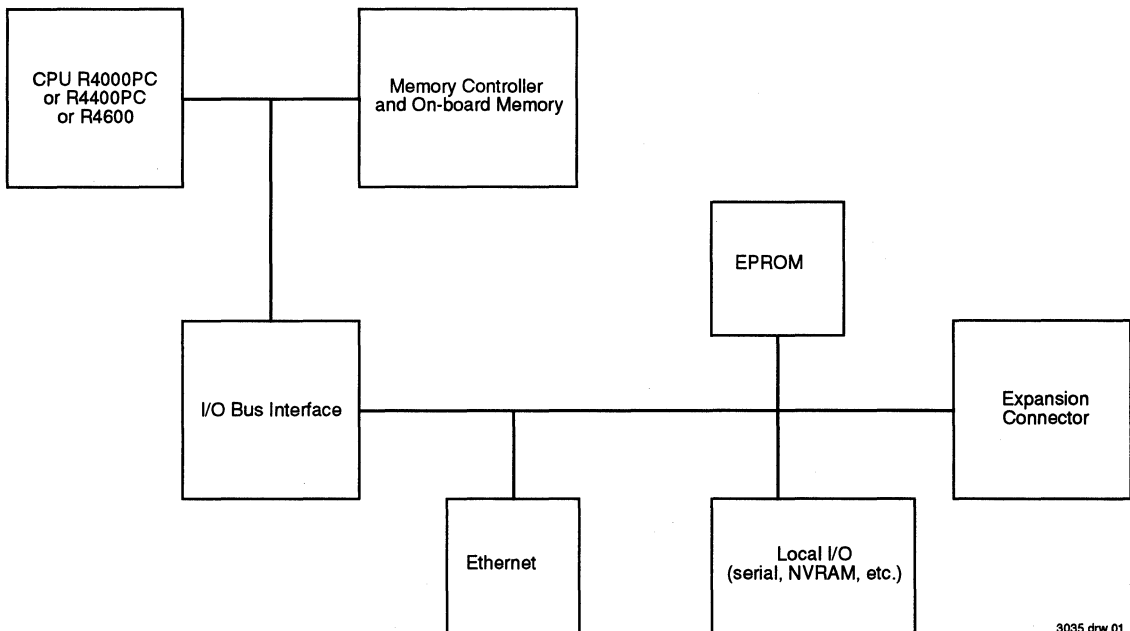
### FEATURES:

- Complete RISC System Development Board
    - Supports R4600 at speeds of 50 to 75MHz
  - Uses a 12 pin PC-style power connector with +12V, -12V and +5V
  - System interface and memory system runs at 50MHz
  - 2MB minimum of non-interleaved DRAM, expandable to 96MB in 4 SIMMs
    - 2 SIMMs for base memory and 2 SIMMs for expansion memory
    - Tuned for 60ns DRAMs but can use 70 or 80ns DRAMs
  - 256KB of EPROM, expandable to 1MB
  - Ethernet connection (thick net) via the DP83932 SONIC Controller
  - Dual serial ports through NEC 72001 DUART
  - Daughter board expansion area
  - Provides for logic analyzer connection
- Shipped with IDT/sim™ (System Integration Manager) in EPROM
    - High capability debug monitor
    - Simplifies software development
  - Complete set of documentation included
    - Complete set of board schematics
    - Complete PAL sources
    - Board specifications manual
    - Design manual with the theory of operations
    - User's manual for IDT/sim

### DESCRIPTION:

The 79S460 Evaluation Board is a complete design for evaluating the R4600 hardware and software environment. The package contains a working system, including schematics and theory of operations, complete documentation, and a debug monitor for software development.

### FUNCTIONAL BLOCK DIAGRAM



3055 drw 01

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MARCH 1994

## **COMPLETE SINGLE BOARD COMPUTER**

The 79S460 is a complete working RISC system intended as a design example using the R4600 highly integrated CPU. The board requires only a simple CRT terminal and a PC-style power supply for operations. While intended to use the R4600, the board also supports the pin compatible R4400™ PC.

The R4600 Evaluation Board is supplied with 2MB of DRAM in the base memory SIMM sockets. This can be upgraded to 32MB for base memory (4Mx36 SIMMs). The expansion memory SIMMs can provide an additional 64MB of DRAM. Other hardware on the board includes a NEC 72001 DUART and a DP83932 SONIC Ethernet Controller; both devices are supported with drivers in IDT/sim. The Ethernet connections is provided for higher speed download of code to the board.

The board contains 256KB of EPROM expandable to 1MB by replacing the given EPROM with a higher density device and adding the second EPROM. The enclosed EPROM contains IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing and I/O. The capabilities of IDT/sim are described in a separate data sheet.

The R4600 Evaluation Board also contains a daughter-board expansion bus. This is controlled by logic similar to a simplified i486 local bus but is expanded to 64-bits and operates at 33MHz. Daughter-boards provide slave memory or registers accessible to the R4600 CPU and can also be DMA masters capable of reading and writing to memory.

## **ORDERING INFORMATION**

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R4600 CPU plugged-in, but the R4400PC can also be used. The R4400PC can also be ordered to allow user upgrades.

## **EVALUATION BOARD**

R4600 Evaluation Kit.....79S460



Integrated Device Technology, Inc.

# IDT/SIM™ SYSTEM INTEGRATION MANAGER ROMABLE DEBUGGING KERNEL

IDT79S901

## FEATURES:

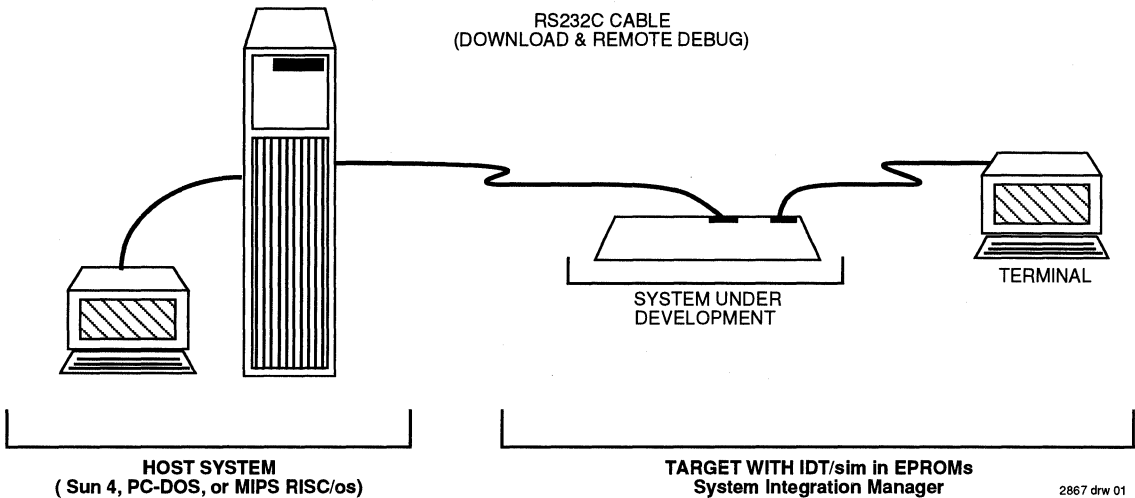
- Complete source code provided
- Robust debug monitor
- Supports remote source-level debug
  - GDB—IDT/c™ tool chain (new)
  - DBX—MIPS tool chain (old)
- Remote file access—connects target and remote host via a 19200 baud serial connection
- Ethernet (UDP/IP) support
- Diagnostic tests for memory, cache, MMU, FPU, and system
- Adaptable to systems with or without hardware floating point accelerator
- Includes a variety of device drivers
- Easy to add new commands and I/O drivers

## POWERFUL TOOL FOR INTEGRATION OF SYSTEMS BASED ON R3000 ISA CPUS

The IDT79S901 System Integration Manager (IDT/sim) is a ROMable software product that permits convenient control and debug of RISC systems built around R3000 ISA (RISController™), R4400™, and R4600™ CPUs. Facilities are included to operate the CPU under controlled conditions, examining and altering the contents of memory, manipulating and controlling R30XX, R4400 and R4600 resources (such as cache, TLB and coprocessors), loading programs from host machines, and controlling the path of execution of loaded programs.

IDT/sim source code includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware.

IDT/sim requires approximately 115KB of EPROM space for code and data, and 71KB of RAM space for uninitialized variable data and stack.



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MARCH 1994

## IDT/SIM FEATURES

IDT/sim is a software tool to help system designers debug hardware designs and port software to systems based on one of the R3000 ISA CPUs, R4400 and R4600. The software is supplied in EPROMs on most IDT RISC Development products, and may be purchased in source-code form so it can be compiled and installed on your system.

IDT/sim provides all the basic functions needed to get a new hardware design debugged and to port and debug software on it. Typically, the monitor is compiled and burned into EPROMs that are plugged into the target system. Approximately 115KB of EPROM is needed for the binary code, and 71KB of RAM is needed for storing variables. Once installed, the designer communicates with the monitor via a simple terminal connected to an RS-232 port on the target system. Source code is included to support a variety of UARTs for this port. On start-up, the monitor will determine the cache and main memory sizes automatically.

## DIAGNOSTICS

The monitor includes a set of diagnostic routines for testing the integrity of the hardware.

**Main Memory Test:** Finds opens, shorts and stuck-at faults on data and address lines. A cache memory test runs memory tests on both caches, checks tag memory, and verifies that instructions can be executed from cache.

**System Test:** Checks the ability to read and store full words, half-words, and bytes. Checks the cache operation for valid, hit/miss, and invalidation.

**MMU Test:** Check the operation of the TLB inside the R3000

**Floating Point Test:** Tests the functionality of the R3010 FPU, including exception interrupts.

## DOWNLOAD SUPPORT

Object code created on a software development system can be downloaded in either ASCII S-records or binary formats to the target system's memory. The code can be produced with the MIPS development tools, or with IDT/c on any number of development platforms: MIPS, Sun and 386/486 PCs under DOS.

IDT/sim source code includes utilities to convert object code from the MIPS compiler to S-records, to convert S-records to binary format (which is more compressed and downloads faster), and to download the binary records to the target. Similar utilities for use with the IDT/c multi-host C-compiler are supplied with IDT/c.

A terminal emulation feature allows the terminal, used as the IDT/sim console, to also be used as a terminal to a software development system accessed through a second serial port. This mode supports remote file download.

## DEBUG COMMANDS

A variety of commands are included in IDT/sim to support software/hardware debug.

**Execution Control:** Breakpoint, call, continue, go, gotill, next, step, unbreak.

**Memory Commands:** Assemble, cache flush, compare, disassemble, dump, dump cache, dump registers, fill, fill registers, move read/write cache, search and substitute.

**TLB commands:** Dump, flush, map, pid and probe.

**Remote Debug:** Source-level debug with DBX on a MIPS RISC/0's system and with IDT cross-development c-compiler tools.

**Communications:** Remote file access, terminal emulator and set baud rate.

## RUN-TIME SUPPORT

IDT/sim includes over 40 functions that can be called by user's programs to perform common I/O and R30XX, R4400 and R4600 control operations. A complete list of commands is listed later in this document.

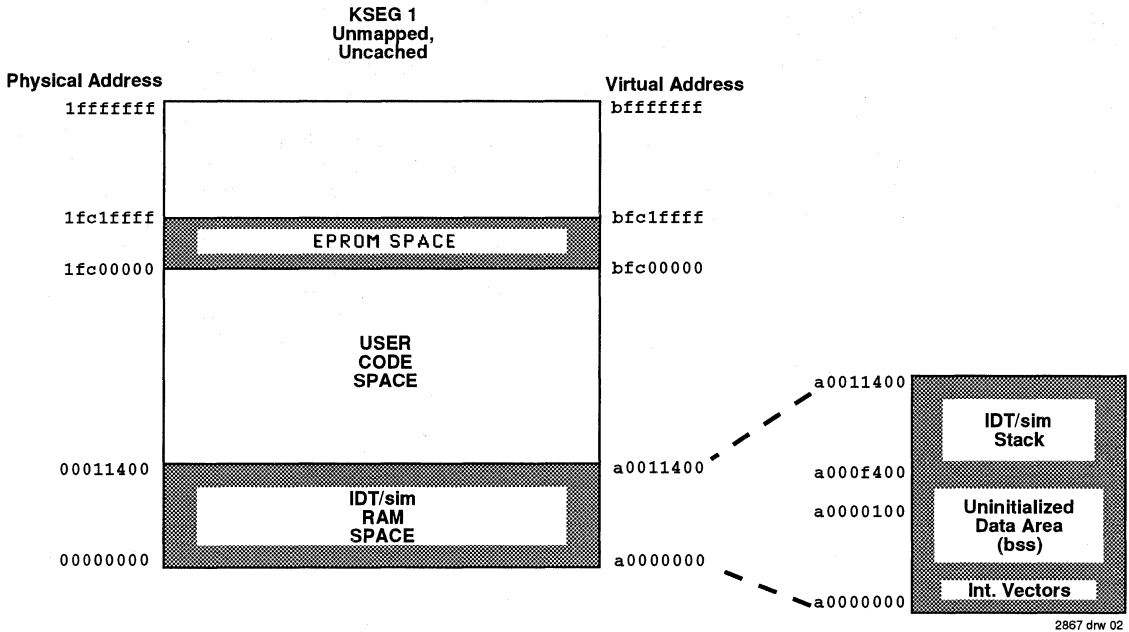
## NEW FEATURES IN VERSION 5.0

**IDT MicroMonitor:** IDT/sim includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware. The only necessary functioning hardware to run the MicroMonitor is the CPU, EPROM, and a serial port. This allows for immediate debugging of hardware, even when the DRAM is not functioning.

**Source-level Debug:** Supports source-level debug using either IDT/c or the MIPS tool chain.

**Remote File Access:** Connects target with remote host file system allowing file transfer between target and host.

**Trace Facility:** Traces the memory accesses of a user program. Provides for tracing the path of execution reads-from, writes-to memory. Trace qualifiers allow the tracing of a specific instruction or class of instructions. Also, specific memory ranges can be specified. The user may stop tracing on the following conditions: trace buffer full, hitting a breakpoint, executing a specific instruction, or accessing a specific memory range. The trace buffer contents may be displayed using standard R30XX, R4400 and R4600 family mnemonics.



**Figure 2 IDT/sim Memory Map**

Figure 2 shows the memory utilized by IDT/sim. The EPROM space starts at virtual address bfc00000, which is the R3000's start-up address. The compiled version of IDT/sim with all features included occupies about 115KB of EPROM

space, and is normally placed in 128KB of EPROM. IDT/sim uses main memory to store interrupt vectors, variables, and a stack. Approximately 71KB of RAM space is reserved for this data.

## IDT/sim COMMANDS

**asm** <addr> examine and change memory interactively  
 using standard assembler mnemonics

**benchmark/bm**  
 Facilitates benchmarking

**brk|b** [addresslist]  
 Set/display breakpoints

**cacheflush/cf** [-i|-d]  
 Flush the I-cache and/or the D-cache

**call/ca** <address> [arg1 arg2 ... arg8]  
 Call subroutine with up-to 8 arguments

**checksum/cs**  
 Display the checksums for an address range

**compare/cp** [-w|-b|-h] <RANGE> <destination>  
 Compare the block of memory specified by RANGE  
 to the block of memory that starts at destination

**cont/c**  
 Continues execution of the client process from  
 where it last halted execution.

**dbgint/di** [<-e|-d DEV>]  
 Debug interrupt enable/disable - allows 'break key'  
 to generate external interrupt

**debug/db** [DEV]  
 Enter remote debug mode

**dis** <RANGE>  
 Disassemble target memory specified by RANGE

**disptag/dt** [-i] RANGE  
 Displays the instruction or data cache tag values and  
 data contents

**dr** [reg#|name|reg\_group]  
 Print out the current contents of register(s)

**dt**  
 Dump the trace buffer

**dump/d** [-w|-h] <RANGE>  
 Dump the memory specified by RANGE to the  
 display

**enable DEVICE**  
 Connect to remote hosfor file access

**fill/f** [-w|-h|-b|-l|-r] <RANGE> [value\_list]  
 Fills memory specified by range with value\_list

**fr** [-s|-d] <reg#|name> <value>  
 Fill <reg#|name> with <value>

**go/g** [-n] <address>  
 Start execution at address <address>

**gotill/gt** <address>  
 Continue execution until address <address>

**help/?** [commandlist]  
 This command will print out a list of the commands  
 available in the monitor. If a command list is sup-  
 plied, only the syntax for the commands in the list is  
 displayed

**history/h**  
 Displays the last 16 commands entered

**idb** [DEVICE] Connect to remote host source level  
**debugger.init/i**

Initialize prom monitor (warm reset)

**load/l** [options] DEV  
 Download code to target

**move/m** [-w|-b|-h] <RANGE> <destination>  
 Move the block of memory specified by RANGE to  
 the address specified by destination

**next/n** [count]  
 Step over subroutine calls

**rad** [-o|-d|-h]  
 Set the default radix to the requested base.

**rc** [-i] <-w|-b|-h> <RANGE>  
 Isolate and read from cache

**regsel/rs** [-c|-h]  
 Select either the compiler names or the hardware  
 names for registers

**search/sr** [-w|-b|-h] <RANGE> <value> [mask]  
 Search area of memory for value.

**seg** [-0|-1|-2|-u]  
 Set the default segment to the requested k-segment.

**setbaud/sb** DEV  
 Set the baud rate on a serial channel

**step/s** [<count>]  
 Single step count times

**sub** [-w|-h|-b|-l|-r] <address>  
 Examine and change memory interactively.

**t** {-a/-o/-e/-d/-r RANGE/-w RANGE/-c RANGE/-i INS/-m  
 MSK}  
 Trace command

**tc** [-e BPNUM] [-d BPNUM]  
 Trace conditionally command

**te** [DEV]  
 Connects the console port straight though to a  
 second serial port

**tex** [RANGE]  
 Exclude tracing calls to RANGE

**tlbdump/td** [RANGE]  
 Dumps the contents of the TLB

**tlbflush/tf** [RANGE]  
 Displays the current process identifier ( pid )

**tlbmap/tm** [-i index] [-ndgv] <vaddress> <paddress>  
 Virtual-to-physical mapping of the TLB

**tlbpid/ti** [pid]  
 Set/display TLB PID

**tlbptov/tp/tm** <physaddr>  
 Probe the TLB

**ts** [-b/-f/-o/-r RANGE/-w RANGE/-i INS/-m MSK]  
 Stop trace command

**unbrk/ub** <bplist>  
 Clear breakpoints

**wc** [-i] [-w|-b|-h] <RANGE> [value\_list]  
 Isolate and write to I or D cache

**wtfle** <filename> [value\_list]  
 Write file to remote host file system

## RUN TIME SUPPORT ENTRY POINTS

*\_exit*  
*atob*  
*clear\_cache*  
*cli*  
*close*  
*exc\_utlb\_code*  
*flush\_cache*  
*get\_mem\_conf*  
*get\_range*  
*getchar*  
*gets*  
*install\_command*  
*install\_immediate\_int*  
*install\_new\_dev*  
*install\_normal\_int*  
*ioctl*  
*longjmp*  
*open*  
*printf*  
*putchar*  
*puts*  
*rclose*  
*read*  
*reinit*  
*reset*  
*restart*  
*rfileinit*  
*rgets*  
*rlseek*  
*ropen*  
*rprintf*  
*rread*  
*rwrite*  
*set\_mem-conf*  
*setjmp*  
*showcar*  
*sprintf*  
*strcat*  
*strcmp*  
*strcpy*  
*strlen*  
*tokenize*  
*timer\_start*  
*timer\_stop*  
*write*

## DEVICE DRIVERS (INCLUDED IN SOURCE CODE)

68681/2681 DUART  
8530 SCC  
SCSI  
Centronics Parallel  
8254 Timer/Counter  
8251 UART

## ORDERING INFORMATION

To order an IDT board-level product, see EPROM order codes below. To order IDT/sim in source code, order the Internal Use License AND order the software on the appropriate source media. You may also order binary distribution rights for the run-time version of the monitor. Ask your IDT sales office for information.

## LICENSES

- Internal Source License** .....79S901SL  
*Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product. Also purchase one or more of the Source Media listed below.*
- Limited Binary Distribution Rights** .....79S901BDR-L  
*Extension to Internal Source License to permit inclusion of binary code into end product. Internal Source License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. For additional copies, purchase Unlimited Binary Distribution Rights.*
- Unlimited Binary Distribution Sublicense** .....79S901BDR-U  
*Extension to Limited Binary Distribution Rights to allow unlimited distribution of binary code. Internal Source License and Limited Binary Distribution Rights must be referenced on order or ordered simultaneously.*
- Maintenance Agreement** .....79S901UP  
*Free updates for one year.*

## SOURCE MEDIA

IDT/sim source code can be compiled with either the MIPS C-compiler, or with IDT/c version 4.1 or later. Earlier versions of IDT/c cannot compile this code. The products listed below are media only and must be purchased with license 79S901SL, listed above.

- Source for 386/486PC, MS-DOS** .....79S901DOS  
*Compile with IDT/c C-Compiler. Shipped with 1.2MB 5.25" and 1.44MB 3.5" diskettes.*
- Source for MIPS/SUN Machines, on DC6150 QIC TAR Tape** .....79S901SUN-MIPS  
*Use with MIPS C-Compiler or with IDT/c. Developmental Use License number must be referenced on order, or must be ordered simultaneously.*







Integrated Device Technology, Inc.

# IDT/c™ Multi-Host GNU C-Compiler System

IDT7S903

## FEATURES:

- ANSI C-Compliant GNU Compiler, Assembler, Linker, Librarian, and ANSI Libraries
- Full Development Environment Including start-up code, cache management routines, etc.
- Efficient Software Floating Point Emulation Library for systems without hardware FPU. Includes Transcendentals
- GDB Provides full source and assembly level debug through IDT/sim™ interface
- Sun 4 (Sparc™), PC-DOS™, MIPS RISC/os™ and SGI Irix 4.0™ Host Platforms
- Fully object code compatible with MIPS RISCross Compilers™
- Supports entire IDT family of MIPS ISA Processors (R3000/R3500™, R3041™, R3051™, R3052™, R3081™, R4400™, and R4600™)

## OPTIMIZING C-COMPILER SYSTEM:

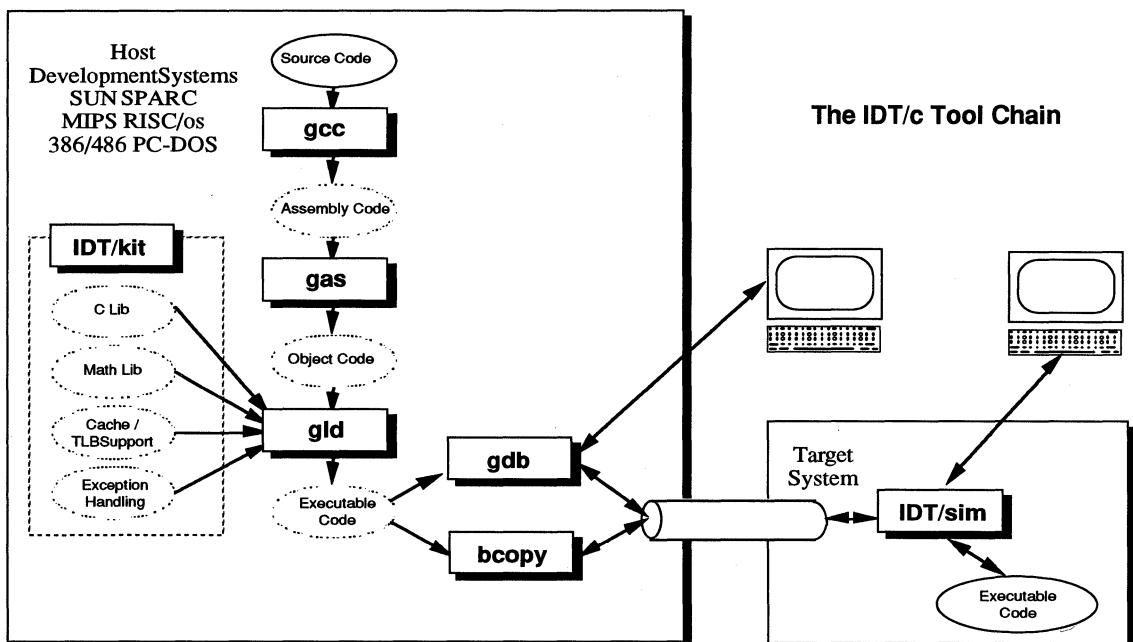
IDT/c is a C-compiler system for the IDT RISController™ family of embedded microprocessors. It supports development for any of the MIPS R3000 and R4000 family of microprocessors and their derivatives, including the IDT R4600.

The toolchain has been specifically designed for developing and debugging code that runs on a remote target. The compiler system includes the GNU C-compiler, assembler, linker, librarian, and source level debugger. The full GNU suite of libraries is included and it is supplemented by the IDT/kit™ libraries in binary form.

IDT/kit is a complete set of architecture-specific code (including start-up code, cache and exception management code, etc.) optimized for RISController family development. A complete assembly language floating point emulation library is also included for use in systems without a hardware FPU. IDT/kit is also available in source form.

IDT/c is available for execution on SunOS™, MIPS RISC/os and SGI Irix 4.0 (Avail. Q294) workstations as well as PC-DOS hosts. Other host ports are available from 3rd parties.

New features in release 5.0 of IDT/c include an upgrade to the current release of the GNU compiler suite, full implementation of gdb support and an improved floating point emulation library.



The IDT logo is a registered trademark, and R3041, R3051, R3052, R3081, R4400, R4600, IDT/c, IDT/kit, IDT/sim, RISCos, and RISController are trademarks of Integrated Device Technology, Inc. All others are trademarks of their respective companies.

MARCH 1994

## OVERVIEW

The IDT/c compiler system is a complete development package for CPUs based on the R3000 and R4000 architecture. It contains an optimizing cross compiler, assembler, linker, and download utilities. The 'C'-compiler is compliant with ANSI 'C' standard and generates optimized code equal in performance to the best available C-compilers. The assembler supports the R3000 machine instructions and architecture described in the book *MIPS RISC Architecture*, by Gerry Kane, including both native and synthetic instructions. The complete IDT/c package runs on a variety of host machines and operating systems, and is fully compatible with other IDT development software, such as IDT/sim and IDT/kit.

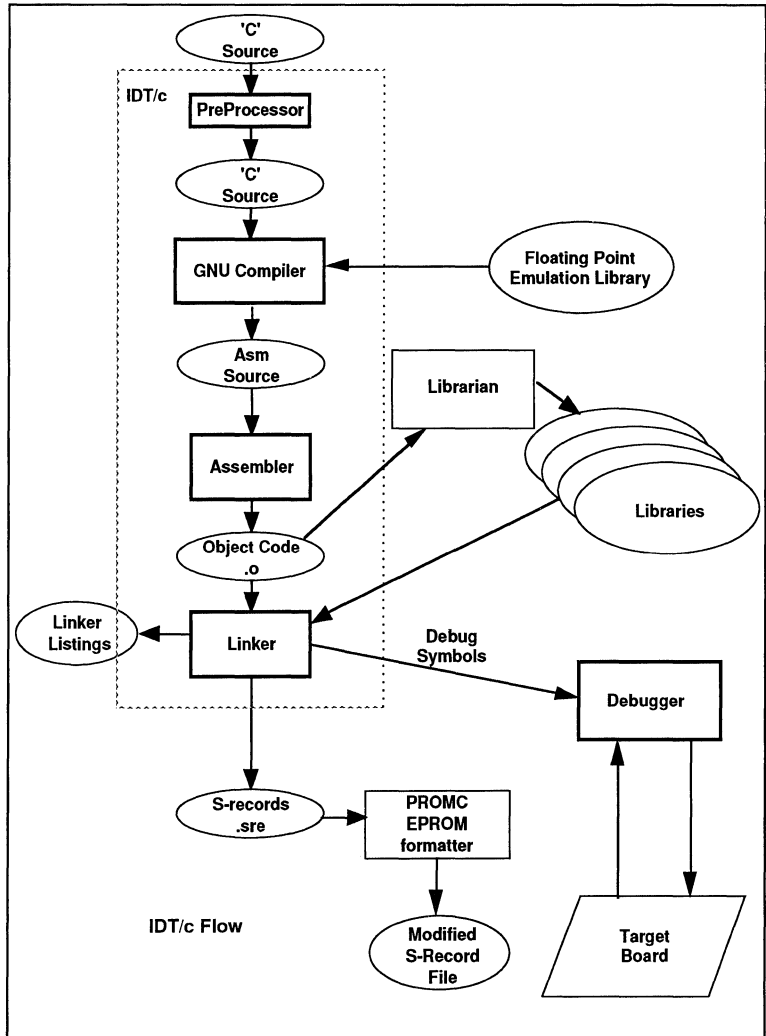
### Compiler

The C pre-processor is GNU cpp and the compiler itself is the GNU C Compiler gcc. All C-preprocessing features are supported. The entire toolchain included in IDT/c has been tested for compliance to the ANSI C standard using the Plum Hall test suite. The C-compiler performs extensive optimization in multiple passes through the code. Switches can be used to select particular optimizations.

The output of the compiler is an assembly language file. Modules compiled by IDT/c can be assembled and linked in the MIPS environment with modules compiled by the MIPS compiler. It is also possible to use IDT/c to compile, assemble and link modules which have been generated for the MIPS toolchain.

### Optimizing Assembler

The IDT/c assembler implements the R3000 native and synthetic instruction set. The assembler first expands the synthetic instructions into the native instruction set. It then rearranges code taking into account the R3000 pipeline architecture. The assembler also analyzes loads of static constants and tries to make use of previously loaded constants. The assembler produces object (".o") files which can be linked together with other object files or libraries to produce an executable file. All object files produced by IDT/c are in MIPS ECOFF format and are compatible with the MIPS RISCross™ compilers. This



allows a user to link code generated by IDT/c with objects or libraries generated by MIPS compilers. This is essential when using a real-time operating system or code libraries which are provided in binary and have been compiled using MIPS' compilers.

### Linker

The linker combines separately assembled program files into one object module. Command line switches or script files may be used to define the placement in memory of program segments.

There are several types of output file formats supported, including S-Records, Intel hex, and binary image. The S-Record files are useful in downloading to target boards. The hex format file is useful for EPROM programming because the code can be divided into multiple files under this format. S-Records can be downloaded to a target containing the IDT/sim monitor using a supplied download utility.

### Endianess

By default, IDT/c supports development of code for Big-endian targets. For support of Little-endian targets, contact IDT's RISC Marketing.

### Floating Point Library

IDT/c includes a floating point emulation library. A switch in the compiler is set at compile time to determine how the compiler should handle floating point instructions. In the normal mode, it will produce R3010 Floating Point Accelerator (FPA)-compatible instructions in the object code. This mode results in the highest performance for targets, which include the R3010, or for systems based on the R3500 or R3081, which include a R3010 compatible hardware floating point accelerator on-chip. If the switch is set the other way, the compiler will insert calls to the floating point emulation library instead, and the floating point emulation library must be available at link time. Because the compiler knows about the library during compile time, it can perform optimizations not otherwise possible and minimize the execution penalty for using software instead of hardware. This mode allows systems without a R3010 (such as those based on an R3041, R3051, or R3052) to implement efficient floating point arithmetic while using a lower cost CPU.

### Librarian

IDT/c supports object code libraries to reduce the number of files that must be dealt with explicitly during program development. Many compiled routines may be stored in a single library file by using the Librarian utility. At link time, the linker extracts only the routines actually used.

### Gdb—Remote Source Level Debugger

Remote debugging differs from the 'conventional' in several ways. The control of a target program relies on a communication line and debugging agent on the target instead of using operating system signals and related services.

Gdb has been enhanced to work with IDT/sim to provide full control of the target program. The distinguishing features are: a program mode in which gdb executes scripts that contain debugging and flow control commands; and host file services which provide the target program with full access to the host file system. The required physical link between host and target is a single RS232 line, though IDT/sim can be modified to use whatever interface is available in hardware.

It is also possible to use direct low-level IDT/sim debugging commands from a gdb session.

### Remote file services

IDB supports file open, close, read, write, seek; printf; and gets commands in the standard C library format.

## FLOATING POINT EMULATION MODE

When floating point and double length variables are used in C programs, compilers usually produce assembly instructions that directly operate on floating point arguments and use a designated register set to hold floating point operands. The C-compiler is aware of underlying hardware and attempts to produce optimal code by using all available resources.

The R3000 architecture has the floating point coprocessor in separate chip (R3010). There are numerous floating point instructions that operate on the 32 floating point

registers inside the R3010. When floating point hardware is not present—for example, an R3000 without the R3010, or a R3041, R3051 or R3052 controller chip—executing programs that use floating point arithmetic requires software that can compensate for the missing hardware. There are two basic solutions to this problem: trapping on the floating point instructions at execution time and relying on the trap handler simulating the FPU in software; or modifying the compiler so that it does not produce any instructions for the FPU in its output.

Using the operating environment to trap all attempts to execute instructions on (non-existent) floating point hardware offers the advantage of using a single object code version of the application whether hardware FPU is present or not. The disadvantage is that the complete FPU state machine must be emulated since the code produced by the C-compiler assumes the real hardware is present. The code that must be executed for each FP instruction is substantial: the trapping overhead for each FP instruction, the maintenance of the FP state machine, and the instructions to execute the required FP operation on integer hardware.

For example, the sequence below requires 3 traps, each of which involves saving all the registers used in the particular trap routine, maintaining the state of the 'virtual' FP register set somewhere in memory, performing the actual FP arithmetic (double addition), and updating the 'virtual' FPU status register bits.

```
lwc1      $f14, ($9)
lwc1      $f15, 4($9)
add.d    $f8, $f14, $f6
```

The solution implemented in IDT/c is to switch the compiler to a different mode for the two environments. In emulation mode, the compiler does not assume presence of any additional hardware, so only R3000 instructions are produced, and FP operations are performed by calls to special routines. The calls are compiler-generated and there is absolutely no difference on the C source level. The same C program that generated the example above would generate the following code in IDT/c emulation mode.

```
lw        $4, ($9)
lw        $5, 4($9)
jal      __adddf3
```

The only overhead is that of performing FP operations on the R3000 integer hardware. On floating point intensive applications, IDT/c typically yields execution times four to five times slower than R3010 execution times, but eight to twelve time faster than the trap-based hardware floating point emulation method described above.

## IDT/C PERFORMANCE

IDT/c Version 5.0 was developed with the goal of improving several aspects of the usefulness of the toolchain, and to provide a solid base upon which to build further perfor-

mance improvements and feature enhancements. The main areas of interest were reliability, maintainability, debugger functionality, and floating point emulation performance. In addition, it was hoped that some integer performance improvements could be realized.

The performance of IDT/c Version 5.0 has been measured against the MIPS RISCross™ C-compiler and previous versions of IDT/c using an array of industry standard benchmarks. These benchmarks include "The Intel Benchmark Suite" (Intel introduced them to measure the performance of various embedded processors when they announced the i960CA) and the "Stanford Benchmark Suite." The results of individual benchmark files vary widely for all of the toolchains, but some general performance comparisons can be drawn.

**Floating Point Emulation Comparisons**

A primary objective of the IDT/c Version 5.0 project was to provide a floating point emulation solution with the reliability of the MIPS "trap" based approach while significantly improving on the performance attainable with the MIPS/IDT "Mix and Match" approach. The Stanford Benchmark suite includes some floating point intensive routines (specifically MatrixMultiply and FFT) which provide a good indication of relative floating point performance. The results of these benchmarks indicated that IDT/c Version 5.0 achieved a

significant (just under 10%) advantage in floating point execution performance versus the "mix & match" approach while maintaining equivalent integer performance. This indicates an order of magnitude performance improvement versus existing "trap" based emulation approaches.

**Integer Comparisons**

One of the objectives of IDT/c Version 5.0 was to provide integer performance on a par with the existing MIPS RISCross compilers (hosted on a Sun4 workstation). The execution of the Stanford and Intel Benchmark suites indicated that IDT/c Version 5.0 achieved a slight (less than 2%) advantage in total execution performance for these two suites.

**General Performance Comparisons**

The benchmark results indicate a variety of performance differences between MIPS C, IDT/c Version 4.1.1 and IDT/c Version 5.0 across these benchmarks. The performance of one compiler versus another on a given benchmark may vary by as much as 20%. Note, however, that these benchmarks may not be fully representative of a particular target application as they are extremely small programs which, for the most part, fit into the large on chip caches found on the IDT RISControllers. Systems with differing cache sizes and/or memory latency may show different results for each compiler. Therefore, the best recommendation is to evaluate the compilers in the context of the intended application to gauge their relative performance.

**ORDERING INFORMATION**

The IDT/c C-Compiler is an efficient R3000 C-compiler system based on the popular GNU C and hosted on a variety of computers. The IDT/c system includes the compiler, assembler and linker, as well as the full GNU library suite and the IDT/kit libraries. All PC versions of the software are shipped with both 1.2MB floppy discs and 1.44MB 3.5" diskettes. A single user license is included with the product. Contact your IDT sales office for multiple user licensing.

**IDT/c Cross Compiler Package and Embedded Development Libraries**

The IDT/c package listed below includes the GNU C Cross Compiler for MIPS and the entire IDT/kit library suite in binary form, including the IDT software floating point emulation library. For developers who wish to customize the code to fit their hardware environment, the source to IDT/sim and IDT/kit is available, as is a binary distribution license for each product.

**IDT/c Cross Compiler Package—Version 5.0**

Single User Binary, 386/486 machine, MS-DOS .....	79S903DOS
Single User Binary, MIPS RISC/os, on DC6150 QIC TAR Tape .....	79S903MIPS
Single User Binary, SUN SunOS 4.x, on DC6150 QIC TAR tape .....	79S903SUN

**IDT/kit Kernel Integration Toolkit—Version 1.0**

Source License .....	79S909SL
Media, 386/486 PC-DOS .....	79S909DOS
Media, Sun SunOS 4.x or MIPS RISC/os, on DC6150 QIC TAR tape .....	79S909SUN/MIPS

**IDT/sim System Integration Manager—Version 4.0**

Source License .....	79S901SL
Media, 386/486 PC-DOS .....	79S901DOS
Media, Sun SunOS 4.x or MIPS RISC/os, on DC6150 QIC TAR tape .....	79S901SUN/MIPS





Integrated Device Technology, Inc.

# IDT/kit™ KERNEL INTEGRATION TOOLKIT

IDT79S909

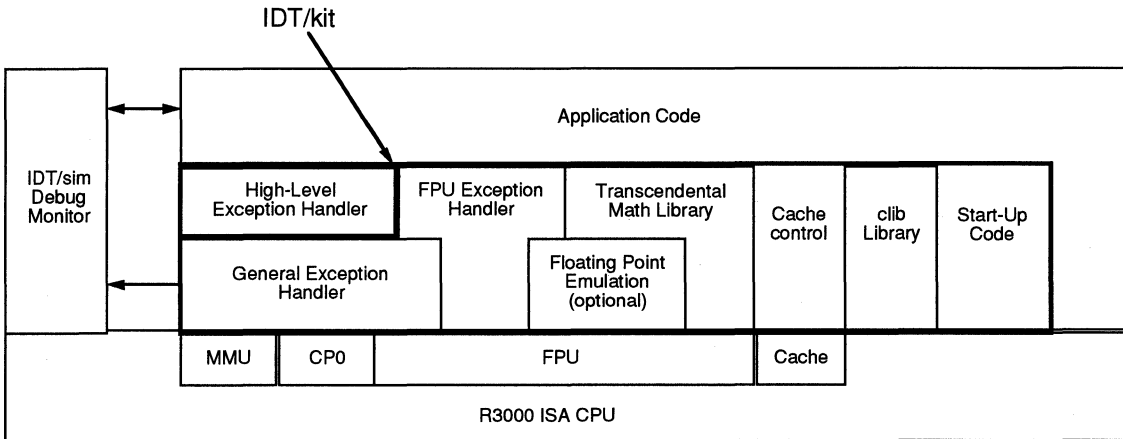
## FEATURES:

- Source code and object code versions of commonly used routines for an R3000 ISA CPU
- Start-Up Code to initialize CPU, MMU, and C runtime environment
- Cache control code to size, initialize, flush, and clear for DMA
- Re-entrant Exception Handler
- Floating Point Emulation Library and Transcendental Math Functions
- ANSI Standard C Library
- Time Support Functions
- MicroMonitor for initial hardware debug
- Interface Library to IDT/sim™ monitor

## ESSENTIAL CODE FOR R30XX SYSTEMS

IDT/kit (Kernal Integration Toolkit) consists of libraries and routines for important system software operations for R3000-based CPUs (R3041™/R3051™/R3052™/R3071™/R3081™). Modules are provided for initializing systems, handling interrupts, servicing floating point exceptions, and many other other common operations. Libraries are included for floating point emulation, transcendental arithmetic routines, and ANSI standard C functions. All IDT/kit libraries are supplied in source code (C and assembly) and in object modules compiled for both little- and big-endian systems and for both hardware and software emulation floating point.

IDT's MicroMonitor is also included in the IDT/kit package. The MicroMonitor is a very simple monitor for initial debug of new hardware. It requires only that the CPU, EPROM, and a serial port be operational. The MicroMonitor can be an invaluable aid for detecting state machine problems in first article hardware.



3018 drw 01

Figure 1. Schematic Representation of the modules in IDT/kit, showing how they control parts of the R3000 CPU and connect to IDT/sim, IDT's debug monitor.

## IDT/KIT™ FEATURES

The IDT Kernel Integration Toolkit (IDT/kit) consists of a set of libraries ready to be linked with user developed code. IDT/kit contains functions that would normally be furnished by an operating system like UNIX but without the overhead. Functions are provided for initializing the system, memory management, exception handling and time support; an ANSI standard 'C' library and a math library with transcendental functions are supplied.

This environment can be compiled with IDT/c or MIPS compilers, Big or Little Endian, Cached or Uncached and with an optional Emulation Mode if no Floating Point Accelerator is installed. With IDT/kit, floating point emulation support is transparent to the user application.

IDT/kit typically would co-exist with IDT/sim and become part of a total development and debug environment. On a system where IDT/sim is installed, all the commands, entry points and debugging facilities of IDT/sim are available to the Kernel Integration Toolkit. When using IDT/sim, IDT/kit filters exceptions first. If IDT/kit does not handle an exception, then it is passed to IDT/sim.

Default exception handlers intercept exceptions, save the environment, preserve the Exception Registers for later analysis, restore the environment and return to continue program execution. The default handlers can easily be replaced or extended with more robust handlers written by the user.

IDT/kit relieves the application from the low-level tweaking necessary to get started, but leaves easy hooks into the system for expansion and polishing as the development progresses. All code is supplied in source code (C and assembly), to allow easy access for modifications needed to tailor the system to specific needs. This allows the programmer to shorten the project development time by the 2-to-3 months required to understand and service the R3000 ISA resources like cache, MMU and exception handling.

IDT/kit includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware. The only hardware which must be functioning to run the MicroMonitor is the CPU, EPROM and a serial port function. This allows for immediate debugging of hardware even when the DRAM memory is *not* functioning.

## IDT/KIT COMPONENTS

### 1. MICROMONITOR:

A small assembly language monitor to aid in debugging the hardware design. The MicroMonitor requires only that three hardware resources are functional: the CPU can execute instructions, the EPROM can provide instructions and the UART can send and receive characters.

### 2. IDT\_CSU.S, THE START UP MODULE

Supplies the initialization and set up code necessary for operation of the system.

- initialize the Status Register
  - a) clear parity error bit
  - b) set Coprocessor 1 usable bit correctly
  - c) clear all IntMasks enabled
  - d) set kernel/user mode
- set Cause Register
  - a) clear software Interrupts Pending
- clear bss area
- establish temporary uncached user stack
- determine memory and cache sizes
- establish permanent stack at Top of Memory
- flush I and D-Caches
- if there is a Translation Lookaside Buffer invalidate it
- initialize library if IDT's standard C Library is used
- initialize exception handlers
- jmp to users' main()

### 3. LIBIKIL.A, KERNEL INTEGRATION LIBRARY:

The IDT Kernel Integration Library (libikil.a) is a library which can be linked to user programs to supply functions required to support the environment of the R3000 ISA family. This library is divided into four sections: Memory Handling, General Exception Handling, Floating Point Exception Handling and Time Support Functions.

- a. memory handling — the full range of functions necessary to manage main memory, cached memory and the Translate Lookaside Buffers
- b. general exception handling — the functions used in enabling and handling any interrupt exceptions, hardware or software, asserted by the CPU
- c. floating point exception handling — provides the support for the Floating Point Unit, the R3010, or for Emulation Software for floating point arithmetic, "strongly recommended" by the IEEE Standard 754-1985. It is transparent to the application code calling this interface whether hardware or software emulation is being employed.
- d. Time support functions using the 8254 timer as a prototype

### 4. LIBILNK.A, THE IDT/SIM INTERFACE LIBRARY:

The IDT/sim linking module which interfaces with all the functions available with IDT/sim not defined with IDT/kit or by the user

### 5. LIBIC.A, ANSI STANDARD C LIBRARY:

The IDT Standard C Library (**libic.a**) is a standard archive library which, when linked with the users' filename.o files, provides the functions defined by the ANSI standard including standard I/O, String and Character functions, Utility functions, and memory allocation functions.

## 6. LIBMATH.A, MATHEMATICS LIBRARY:

The IDT Math Library (**libmath.a**) is a standard archive library which, when linked with the users' filename.o files, provides the transcendental functions required for standard math processing. Whether hardware floating point or software emulation is used is transparent to the application code calling this library.

## 7. UTILITIES:

Three utilities that execute under MIPS RISC/os are supplied to convert from compiler output from the MIPS coff file format to an S-record format and to downloading the S-records to a target board in either ASCII or binary forms. These utilities are needed only for users of the MIPS C-compiler who do not have IDT/sim or MIPS SPP/e.

## HOW IDT/KIT IS USED

IDT's Kernel Integration Toolkit includes a robust set of tools for the embedded controller developer. They are "packaged" in accessible, modular containers, the IDT/kit libraries. The four libraries, arranged by function, supply most of the routines required by RISC applications. Only those libraries needed to resolve function calls must be entered on the link command line; the others are never accessed which establishes a fully modular environment.

IDT/kit serves as an envelope for the installation's application code. The source module, `idt_csu.S`, is linked first, then the development code and, finally, any kit libraries required to support function calls. This allows the developer to concentrate on the application and not waste resources re-developing the support routines. Although the libraries are provided complete and ready to link, source code for all

the functions is also distributed to allow easy examination for information or as a template for additional routines. All the necessary Make/Batch files are included to facilitate any changes, additions or corrections. Some examples:

*strcpy* (or any of the C library routines) — perhaps your installation has developed a super-algorithm. It isn't quite ANSI Standard, but does your job better. Simply edit the source in the `clib` subdirectory (or replace the one that is there), execute the makefile for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, `libc.a`, now contains your code. Your module could also be placed on the system Link line before the corresponding library and the call would be resolved before the library is searched.

*Interrupt Handling* — you want the default interrupt handler (it's already there), but you need an additional flag set. Edit the routine in the `killib` subdirectory, run the Make/batch file for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, `libkil.a`, now contains "your" default interrupt handler.

These kinds of simple modifications allow the IDT/kit routines to be tailored for a specific system without expending the time to investigate and understand all the routines; only the section applicable to the application need be tweaked and the Make/Batch files provide easy guidelines for doing it.

**IDT/kit FUNCTION LIST****CSU\_IDT.S: START UP MODULE**

start() -----Startup routine

**LIBIKIL.A: KERNEL INTEGRATION LIBRARY****Programmable interval timer driver**install\_timer\_driver() install timer driver  
i8254init() -----timer driver init  
i8254open() -----opens the device  
i8254ioctl() -----i/o control function**Assembly level exception handling**disable\_int() -----clear selected interrupts  
enable\_int() -----set selected interrupts  
exc\_norm\_code() ---general exception code  
exc\_utlb\_code() ---UTLB Miss code  
exception() -----general exception code  
init\_erc\_vecs() -----init vector code  
longjmp() -----go to setjmp() point  
other\_excpt() -----handles other exception  
setjmp() -----set setjmp() state**High level exception handling**add\_ext\_int\_func() --set default exc handler  
clr\_except\_ptr() -----clears setjmp pointer  
config\_memory() -----size of main memory  
extern\_int() -----external interrupt code  
exception() -----general exception code  
get\_except\_ptr() -----get exception pointer  
init\_tlb() -----initializes TLB  
mem\_exc\_hdr() -----memory exception code  
sae\_errmsg() -----prints msg & exits  
set\_except\_ptr() -----sets setjmp pointer  
spurious\_int() -----unexpected ext interrupt**FPU interface module**fp\_defaultHdlr() -----default handler  
fp\_disableTrap() -----clears trap bits in fpcsr  
fp\_enableTrap() -----sets trap bits in fpcsr  
fp\_init() -----init floating Point  
fp\_int() -----FP interrupt dispatcher  
fp\_signal() -----user exception handler  
fpclr\_stickybits() -----clear sticky bits in fpcsr  
fpget\_excregs() -----get Exc Regs  
fpget\_fpcsr() -----get FP Control/Status  
fpget\_RM() -----get rounding mode fpcsr  
fpget\_stickyBits() ---get sticky bits fpcsr  
fpset\_fpcsr() -----set FP Control/Status  
fpset\_RM() -----sets rounding mode  
fpset\_stickyBits() ---sets sticky bits in fpcsr  
fpset\_excregs() -----set Exc Register buffer**Assembly language FPU access**clr\_CAUSE() -----clears SW bits in CAUSE  
get\_CAUSE() -----returns contents of CAUSE  
get\_fpcsr() -----returns FPU csr  
get\_cp0epc() -----gets epc  
get\_STATUS() -----status register contents  
set\_CAUSE() -----sets CAUSE Register  
set\_fpcsr() -----sets FPU csr**Functions affecting I/D Caches**clear\_Dcache() -----invalidate portion of Dcache  
clear\_lcache() -----invalidate portion of lcacheconfig\_Dcache() -----size of Data cache  
config\_lcache() -----size Instruction cache  
flush\_Dcache() -----invalidates entire Data cache  
flush\_lcache() -----invalidates entire Inst cache  
get\_mem\_conf() -----gets memory configuration  
size\_cache() -----finds size of cache**Assembly language TLB access**resettlb() -----invalidates tlb entry  
ret\_tlblo() -----returns tlb entry lo reg  
ret\_tlbhi() -----returns tlb entry hi reg  
ret\_tlbpid() -----returns tlb process ID field  
set\_tlbpid() -----sets current tlb pid  
tlbprobe() -----probes tlb  
tlbmapping() -----maps tlb entry**Time support module**time\_cmd\_init() -----starts clock  
time\_init() -----init timer drv  
timer\_int -----clock interrupt routine  
time() -----returns timer tics  
time\_it() -----times the selected function**Assm language Write Buff Routine**

wblflush() -----flushes the write buffer

**LIBILNK: IDT/SIM LINK LIBRARY****Cache Routines**clear\_cache() -----clears portion of l and D  
flush\_cache() -----flushes entire l and D**Character Routines**getchar() -----inputs a character  
putchar() -----outputs a character  
showchar() -----makes character visible**Command Line Interpreter**cli() -----Command Line Interpreter  
get\_range() -----parses the range spec  
tokenize() -----parses the command line**Exit and Reenter Routines**\_exit() -----exit & return to monitor  
promexit() -----exit & return to monitor  
reinit() -----reinitializes monitor  
reset() -----resets prom monitor  
restart() -----restarts the debug monitor**Help Screen Routine**

help() -----prints Help Screen

**ROUTINES TO EXTEND IDT/SIM**install\_commands() -adds user commands  
install\_immediate\_intinstalls user interrupt  
install\_new\_dev() ---installs new device  
install\_normal\_int() --installs user interrupt**Routines for low level I/O**close() -----closes an open device  
open() -----opens a device  
read() -----reads data from device  
write() -----writes data to an device**I/O Control Function**

ioctl() -----sets I/O flags / calls drivers



**Routines to save /restore context**

longjmp() ----- restores setjmp context  
 setjmp() ----- saves the current context

**Memory configuration routines**

get\_mem\_conf() ----- returns mem configuration  
 set\_mem\_conf() ----- sets the mem configuration

**Formatting print routine**

printf() ----- formatting print routine

**Dummy routines for libc**

\_init\_file() ----- dummy file routine  
 \_init\_sbrk() ----- dummy sbrk routine

**String routines**

atob() ----- Ascii string convert  
 gets() ----- gets string function  
 puts() ----- outputs string to I/O  
 strcat() ----- concatenates two strings  
 strcmp() ----- compares two strings  
 strcpy() ----- copies one string to another  
 strlen() ----- returns length of string

**LIBIC.A: ANSI STANDARD C LIBRARY**

abs() ----- absolute value of integer  
 atof() ----- fp value of an Ascii string  
 atoi() ----- integer value of Ascii str  
 atol() ----- long value of Ascii str  
 bsearch() ----- binary search of a array  
 div() ----- rem & quot of int division  
 ferror() ----- error during a file operation?  
 atexit() ----- routines called at exit time  
 exit() ----- Terminate with status  
 fopen() ----- open file/ret file stream ptr.  
 fclose() ----- close a file  
 fdopen() ----- open stream  
 labs() ----- absolute value of long arg  
 ldiv() ----- rem & quotient of division  
 free() ----- free allocated memory  
 malloc() ----- memory allocation  
 realloc() ----- reallocation of memory  
 fscanf() ----- read data from a file  
 printf() ----- display data on the std I/O  
 qsort() ----- quick sort routine  
 rand() ----- generates random number  
 srand() ----- seed for random num genr  
 sbrk() ----- mem allocation bp routine  
 scanf() ----- read data from standard input  
 sprintf() ----- output data into a string  
 sscanf() ----- read data from a string  
 memcmp() ----- compare two memory arrays  
 memcpy() ----- memory array copy  
 memmove() ----- memory array move  
 memchr() ----- ret ptr to first matched char  
 memset() ----- place a char in memory array  
 strlen() ----- return string length  
 strcmp() ----- strings are identical?  
 strcpy() ----- copy string  
 strncpy() ----- copy n characters of a string  
 strchr() ----- ret ptr to first match of a char  
 strrchr() ----- ret ptr to last match of a char  
 strcat() ----- concatenate a strings  
 strncat() ----- concatenate strings

strspn() ----- len of prefix of str  
 strcspn() ----- len of prefix of str  
 strpbrk() ----- ptr to first occur of any char  
 strstr() ----- string a occurs in string b?  
 strtok() ----- return tokens  
 strtod() ----- convert string to a double  
 strtol() ----- convert string to long int

**LIBIMATH.A: TRANSCENDENTAL MATH LIBRARY**

acosh() ----- inv hyperbolic cosine of x  
 acos() ----- cos -1 (x)  
 asin() ----- sin -1(x)  
 asinh() ----- inverse hyperbolic sine of x  
 atan() ----- tan -1 (x)  
 atan2() ----- tan -1 (x/y)  
 atan2() ----- tan -1 (x/y)  
 atanh() ----- inv hyperbolic tangent of x  
 cabs() ----- complex absolute value  
 exp() ----- exponential function e^x  
 hypot() ----- sqrt (x^2 + y^2)  
 z\_abs() ----- double-complex absolute  
 cbrt() ----- cube root of x  
 cosh() ----- hyperbolic cosine of x  
 exp() ----- exponential function e^x  
 expm1() ----- exponent (x - 1)  
 ceil() ----- smallest int not < x, double  
 floor() ----- largest int not > x, double  
 rint() ----- nearest x in dir of round  
 fmod() ----- fp remof x/y, sign of x  
 atan() ----- tan -1 (x)  
 cos() ----- cos of x  
 exp() ----- exponential function e^x  
 log() ----- natural logarithm ln(x), x>0  
 log10() ----- base 10 logarithm, x>0  
 sin() ----- sine of x  
 sqrt() ----- square root of x, x>= 0  
 tan() ----- tan of x  
 xtoi() ----- raises x to integer power, i  
 sim\_fpint() ----- simulate IEEE standard trap  
 sim\_uint ----- sim FP Unimplemented Op  
 log() ----- natural logarithm ln(x), x>0  
 log10() ----- base 10 logarithm, x>0  
 log1p() ----- log (1 + x)  
 log\_L() ----- og(1 + x) -2s/s  
 pow() ----- x^y  
 cos() ----- cos of x  
 sin() ----- sine of x  
 sinh() ----- hyperbolic sine of x  
 copysign() ----- returns x with sign of y  
 drem() ----- x - n\*y, integer nearest n  
 finite() ----- 1 = real x; 0 = INF or NAN x  
 logb() ----- exponent of x^n  
 scalb() ----- x \* (2\*\*n) computed for n  
 sqrt() ----- square root of x, x>= 0  
 tan() ----- tan of x  
 expm1() ----- exponent (x - 1)  
 tanh() ----- hyperbolic tangent of x  
 fabs() ----- absolute value of number  
 frexp() ----- returns mantissa;exp in \*ptr  
 isnan() ----- tests for floating point NaN  
 ldexp() ----- returns quantity \*2^exp  
 pow() ----- x^y

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