intel

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**

- **1K x 8 ROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.
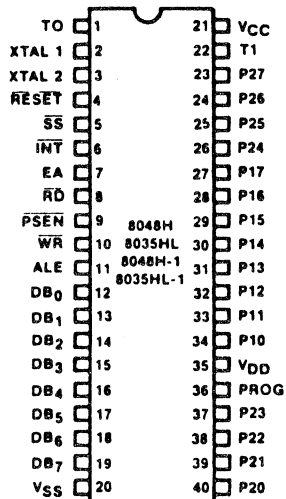
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.
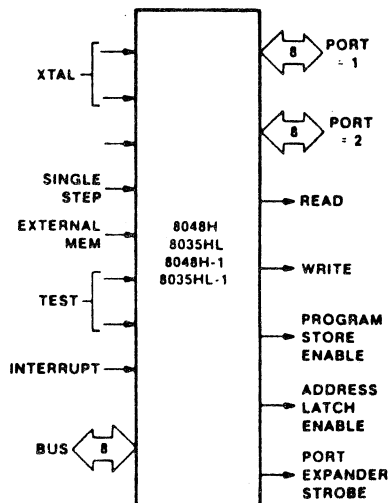
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.
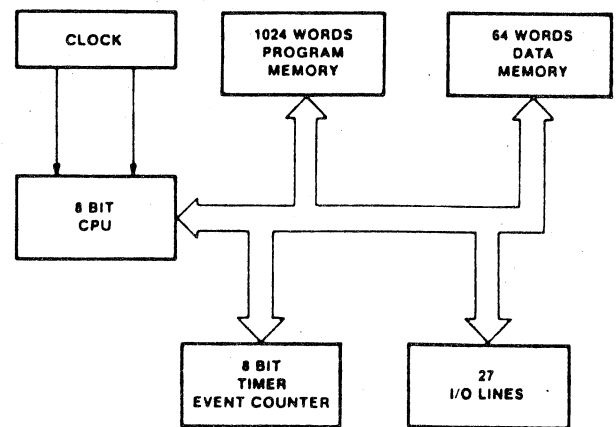

PIN CONFIGURATION   **LOGIC SYMBOL**   **BLOCK DIAGRAM**

PIN DESCRIPTION

Designation	Pin =	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also

Designation	Pin =	Function
		testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R*	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A. # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNT1	Enable timer/counter interrupt	1	1
DIS TCNT1	Disable timer/counter interrupt	1	1

Control

Mnemonic	Description	Bytes	Cycles
EN 1	Enable external interrupt	1	1
DIS 1	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING
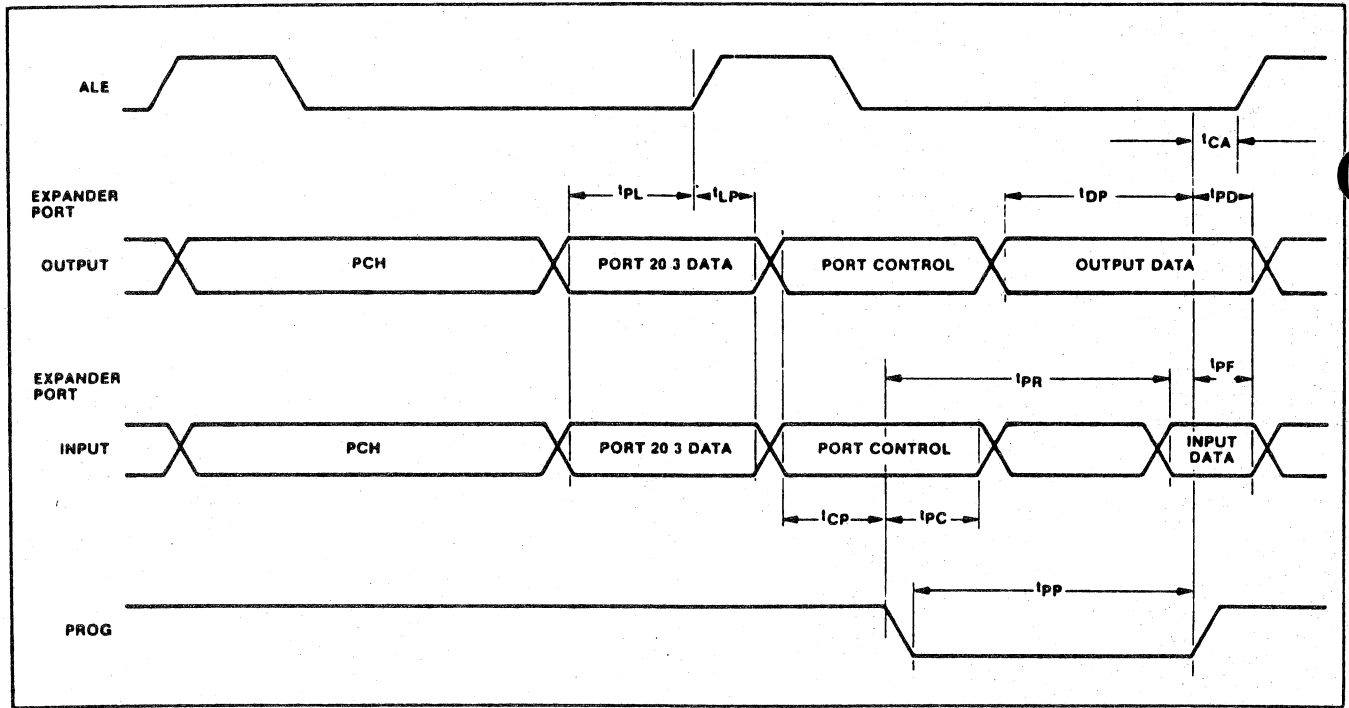
BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY			
T_{LL}	7/30	T_{CY}	MIN	
T_{AL}	1/10	T_{CY}	MIN	
T_{LA}	1/15	T_{CY}	MIN	
T_{CC} (1)	1/2	T_{CY}	MIN	T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2)	2/5	T_{CY}	MIN	T_{CC} (2) : $\overline{PSEN}$
T_{DW}	2/15	T_{CY}	MIN	
T_{WD}	1/15	T_{CY}	MIN	
T_{DR}	0		MIN	

SYMBOL	FUNCTION OF TCY			
T_{RD} (1)	11/30	T_{CY}	MAX	T_{RD} (1) : $\overline{RD}$
T_{RD} (2)	3/10	T_{CY}	MAX	T_{RD} (2) : $\overline{PSEN}$
T_{AW}	3/10	T_{CY}	MIN	
T_{AD} (1)	1/2	T_{CY}	MAX	
T_{AD} (2)	1/3	T_{CY}	MAX	T_{AD} (1) : $\overline{RD}$
T_{AFC}	1/30	T_{CY}	MIN	T_{AD} (2) : $\overline{PSEN}$
T_{CA}	1/15	T_{CY}	MIN	

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

WAVEFORMS

Instruction Fetch From External Program Memory

Read From External Data Memory

Write to External Data Memory

Input and Output for A.C. Tests.
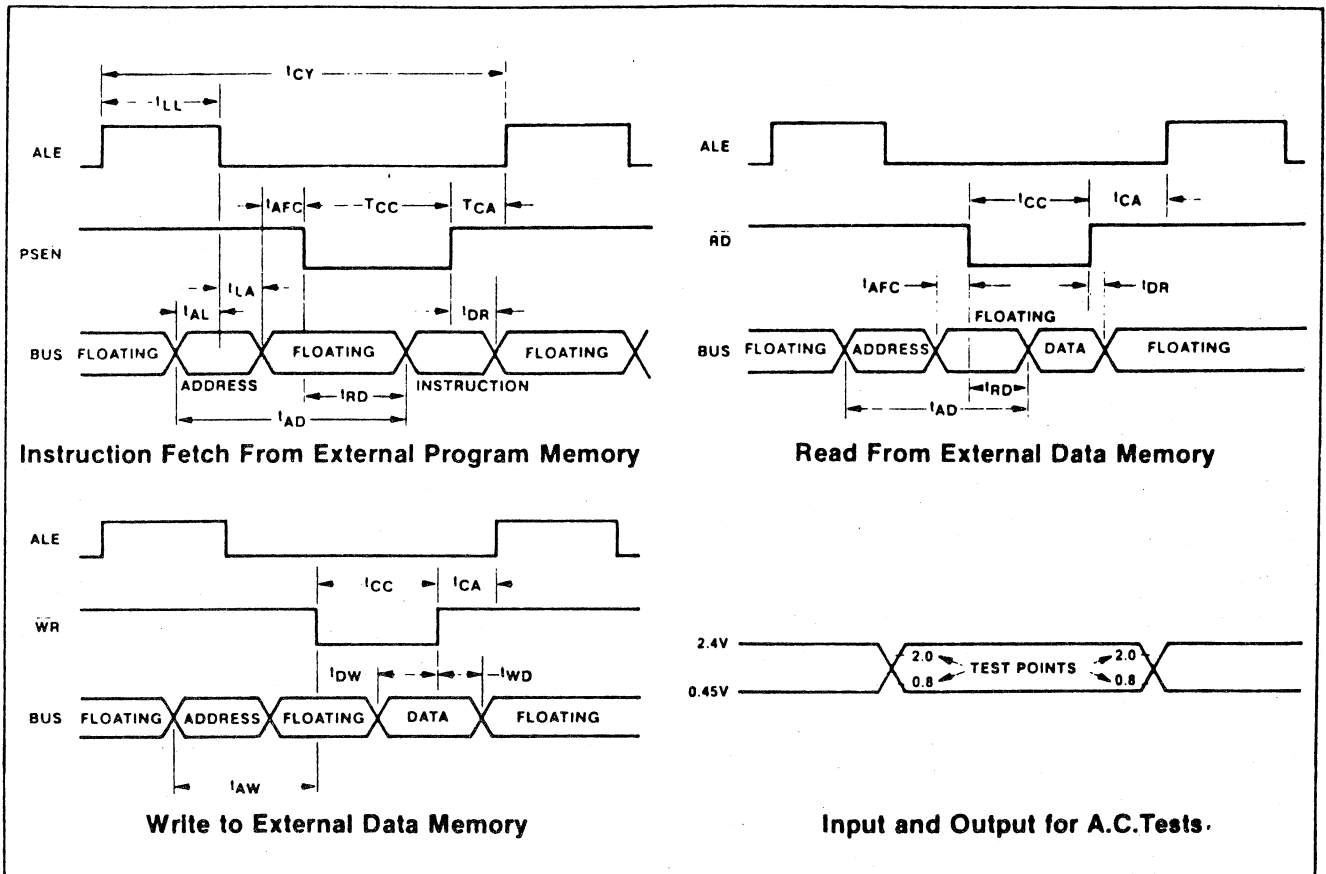
A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

| Symbol | Parameter | 8048H 8035HL | | | | 8048H-1 8035HL-1 | | Unit | Conditions (Note 1) |
| | | 6 MHz | | 8 MHz | | 11 MHz | | | |
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width (PSEN, RD, WR)	700		490		300		ns	
t_{DW}	Data Setup before WR	370		370		280		ns	
t_{WD}	Data Hold after WR	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	PSEN, RD to Data In		500		340		200	ns	
t_{AW}	Address Setup to WR	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to RD, PSEN	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

NOTE 1: Control outputs   CL = 80 pF
            BUS outputs   CL = 150 pF

NOTE 2: BUS High Impedance Load: 20 pF