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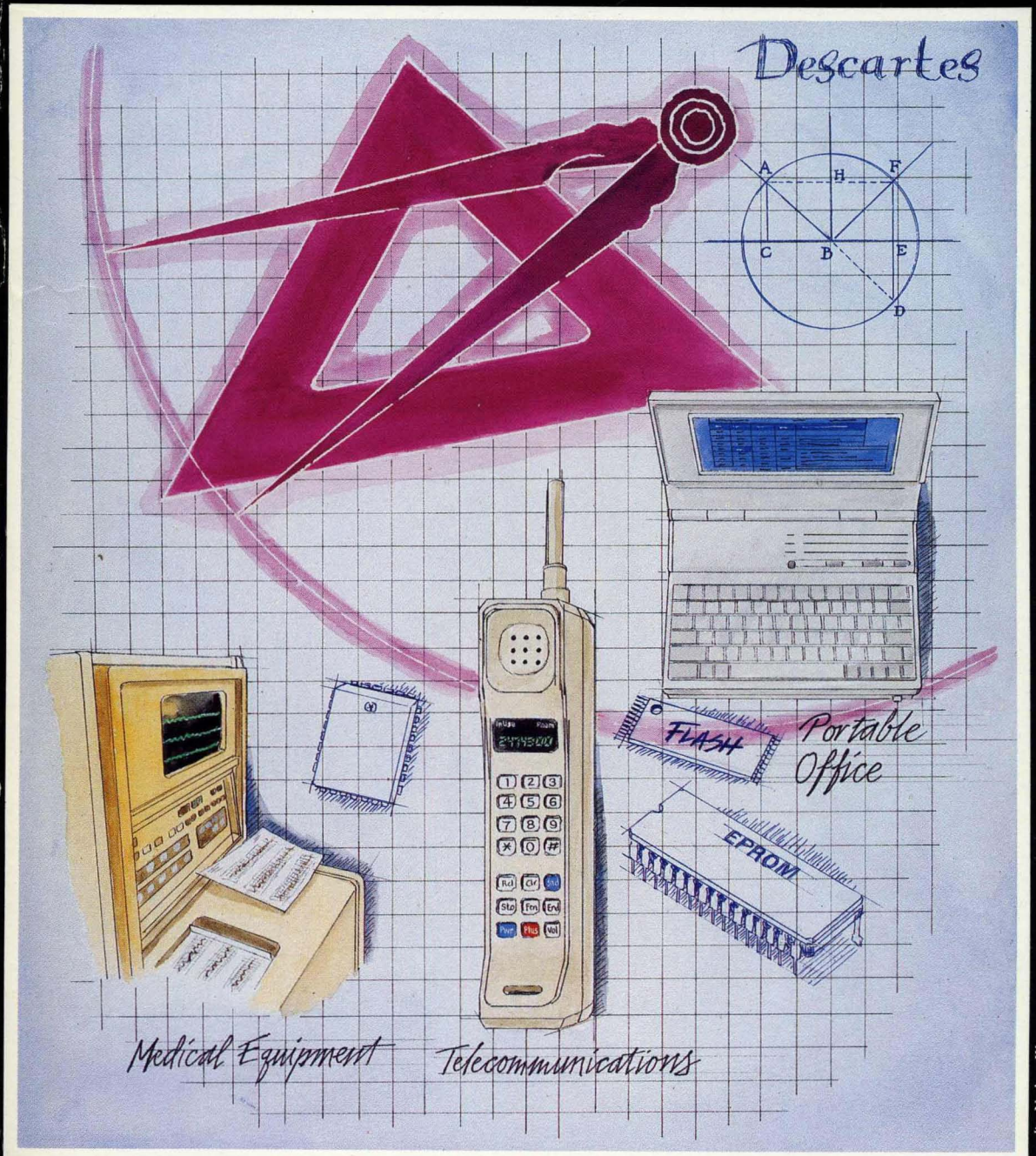

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MEMORY PRODUCTS

1991

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Memory Overview 1

MEMORY BACKGROUND AND DEVELOPMENT

Years ago, MOS LSI memories were little more than laboratory curiosities. Any engineer brave enough to design with semiconductor memories had a simple choice of which memory type to use. The 2102 Static RAM for ease of use or the 1103 Dynamic RAM for low power were the only two devices available. Since then, the memory market has come a long way, the types of memory devices have proliferated, and more than 3,000 different memory devices are now available. Consequently, the designer has many to choose from but the choice is more difficult, and therefore, effective memory selection is based on matching memory characteristics to the application.

Memory devices can be divided into two main categories: volatile and nonvolatile. Volatile memories retain their data only as long as power is applied. In a great many applications this limitation presents no problem. The generic term random access memory (RAM) has come to be almost synonymous with a volatile memory in which there is a constant rewriting of stored data.

Nonvolatile memories retain their data whether or not power is applied. In some situations it is critical that a nonvolatile device be used. An example of this requirement would be retaining data during a power failure. (Tape and disk storage are also non-volatile memories but are not included within the scope of this book, which confines itself to solid-state technologies in IC form.)

Thus, when considering memory devices, it's helpful to see how the memory in computer systems is segmented by applications and then look at the state-of-the-art in these cases.

Volatile Read/Write Memory

First examine read/write memory, which permits the access of stored memory (reading) and the ability to alter the stored data (writing).

Before the advent of solid-state read/write memory, active data (data being processed) was stored and retrieved from nonvolatile core memory (a magnetic-storage technology). Solid-state RAMs solved the size and power consumption problems associated with core, but added the element of volatility. Because RAMS lose their memory when you turn off their power, you must leave systems on all the time, add battery backup or store important data on a nonvolatile medium before the power goes down.

Despite their volatility, RAMs have become very popular, and an industry was born that primarily fed computer systems' insatiable appetites for higher bit capacities and faster access speeds.

RAM Types

Two basic RAM types have evolved since 1970. Dynamic RAMs are noted for high capacity, moderate speeds and low power consumption. Their memory cells are basically charge-storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted by the RAM's sense line as a logical 1 or 0. Because of the charge's natural tendency to distribute itself into a lower energy-state configuration, however, dynamic RAMs require periodic charge refreshing to maintain data storage.

Traditionally, this requirement has meant that system designers had to implement added circuitry to handle the dynamic RAM subsystem refresh. And at certain times, when refresh procedures made the RAM unavailable for writing and reading; the memory's control circuitry had to arbitrate access. LSI dynamic memory controllers reduce the refresh requirement to a minimal design by offering a monolithic controller solution.

Where users are less concerned with space and cost than with speed and reduced complexity, the second RAM type—static RAMs—generally prove best. Unlike their dynamic counterparts, static RAMs store ones and zeros using traditional flip-flop logic-gate configurations. They are faster and require no refresh. A user simply addresses the static RAM, and after a very brief delay, obtains the bit stored in that location. Static devices are also simpler to design with than dynamic RAMs, but the static cell's complexity puts these volatile chips far behind dynamics in bit capacity per square mil of silicon.

Nonvolatile Read-Only Memory

Another memory class, read-only memory (ROM), is similar to RAM in that a computer addresses it and then retrieves data stored at that address. However, ROM includes no mechanism for altering the data stored at that address—hence, the term read only.

ROM is basically used for storing information that isn't subject to change—at least not frequently. Unlike RAM, when system power goes down, ROM retains its contents.

ROM devices became very popular with the advent of microprocessors. Most early microprocessor applications were dedicated systems; the system's program was fixed and stored in ROM. Manipulated data could vary and was therefore stored in RAM. This application split caused ROM to be commonly called program storage, and RAM, data storage.

The first ROMs contained cell arrays in which the sequence of ones and zeros was established by a metallization interconnect mask step during fabrication. Thus, users had to supply a ROM vendor with an interconnect program so the vendor could complete the mask and build the ROMs. Set-up charges were quite high—in fact, even prohibitive unless users planned for large volumes of the same ROM.

To offset this high set-up charge, manufacturers developed a user-programmable ROM (or PROM). The first such devices used fusible links that could be melted or programmed with a special hardware system.

Once programmed, a PROM was just like a ROM. If the program was faulty, the chip had to be discarded. But, PROMs furnished a more cost-effective way to develop program memory or firmware for low-volume purposes than did ROMs.

As one alternative to fusable-link programming, Intel pioneered an erasable MOS-technology PROM (termed an EPROM) that used charge-storage programming. It came in a standard ceramic DIP package but had a window that permitted die exposure to light. When the chip was exposed to ultraviolet light, high energy photons could collide with the EPROM's electrons and scatter them at random, thus erasing the memory.

The EPROM was not intended for use in read/write applications, but it proved very useful in research and development for prototypes, where the need to alter the program several times is quite common. Indeed, the EPROM market originally consisted almost exclusively of development labs. As the fabrication process became mature, and volumes increased, EPROM's lower prices made them attractive even for medium-volume production-system applications. Today, millions of EPROMs are used in systems which require only periodic, off-line updates of information and parameters.

Nonvolatile Read/Write Memory

Technology advances have blurred the traditional lines drawn between read-only memories (ROMs) and read/write memories (RAMs). The first alternative was the EPROM, which required removal from the host system, placing it under ultraviolet light for erasure, and subsequent reprogramming and reinstallation into the host system.

The next advancement was the introduction of a nonvolatile memory that was electrically erasable and user rewritable on a byte-by-byte basis, called the EEPROM. The byte erase capability and high-level of feature integration of the EEPROM came with two penalties—density and cost. Cell and periphery complexity places EEPROM far behind EPROM or DRAM in bit capacity per square millimeter of silicon and the resulting lack of cost-effectiveness and density has caused it to lag behind other memory technologies.

The latest advancement is Flash memory. Flash memories combine the electrical erase capability of the EEPROM with the simplicity, density and cost-effectiveness of EPROM cell layout. Modification to the EPROM cell replaces block UV-erasure with block electrical erasure, which can be accomplished while the device is still installed in the host system. Flash memory can also be randomly read or written by the local system microprocessor or microcontroller.

The cost effectiveness and flexibility of Flash memory makes it applicable in code storage applications. Code can be quickly and easily updated during prototyping, incoming test, assembly or in the field, quickly and easily. High density and nonvolatile read/write capability also make Flash memory an innovative alternative for mass storage, and integrating main memory and backup storage functions into directly executable Flash memory boosts system performance, shrinks system size, reduces power requirements and increases reliability over that of electromechanical media, especially in extreme environmental conditions.

APPLICATIONS OF MEMORY DEVICES

Besides the particular characteristics of each device that has been discussed, there are a number of other factors to consider when choosing a memory product, such as cost, power consumption, performance, memory architecture and organization, and size of the memory. Each of these factors plays an important role in the final selection process.

Performance

Generally, the term performance relates to how fast the device can operate in a given system environment. This parameter is usually rated in terms of the access time. Fast SRAMs can provide access times as fast as 20 ns, while the fastest DRAM cannot go much beyond the 100 ns mark. A bipolar PROM has an access time of 35 ns. RAM and PROM access is usually controlled by a signal most often referred to as Chip Select ($\overline{CS}$). $\overline{CS}$ often appears in device specifications. In discussing access times, it is important to remember that in SRAMs and PROMs, the access time equals the cycle time of the system whereas in DRAMs, the access time is always less than the cycle time.

Cost

There are many ramifications to consider when evaluating cost. Often the cost of the physical device used is the smallest portion of the total cost of using a particular device. Total cost must comprehend other factors such as design-in time, test expense, update costs, as well as cost per bit, size of memory power consumption, etc.

Cost of design time is proportional to design complexity. For example, SRAMs generally require less design-in time than DRAMs because there is no refresh circuitry to consider. Conversely, the DRAM provides the lowest cost per bit because of its higher packing density. The cost of a service call to exchange or reprogram a ROM/PROM/EPROM versus an in-system update of a Flash memory costs orders of magnitude more than the device itself.

Memory Size

Memory size is generally specified in the number of bytes (a byte is a group of eight bits). The memory size of a system is usually segmented depending upon the general equipment category. Computer mainframes and most of today's minicomputers use blocks of read/write substantially beyond 64K bytes—usually in the hundreds of thousands to millions of bytes.

The microprocessor user generally requires memory sizes ranging from 2K bytes up to 64K bytes. In memories of this size, the universal site concept allows maximum flexibility in memory design.

Power Consumption

Power consumption is important because the total power required for a system directly affects overall cost. Higher power consumption requires bigger power supplies, more cooling, and reduced device density per board—all affecting cost and reliability. All things considered, the usual goal is to minimize power. Many memories now provide automatic power-down. With today's emphasis on saving energy and reducing cost, the memories that provide these features will gain an increasingly larger share of the market.

In some applications, extremely low power consumption is required, such as battery operation. For these applications, the use of devices made by the CMOS technology have a distinct advantage over the NMOS products. CMOS devices offer power savings of several magnitudes over NMOS. Non-volatile devices such as EPROMs or Flash memories are usually independent of power problems in these applications.

Power consumption also depends upon the organization of the device in the system. Organization usually refers to the width of the memory word. At the time of their inception, memory devices were organized as nK x 1 bits. Today, they are available in various configurations such as 4K x 1, 16K x 1, 64K x 1, 1K x 4, 2K x 8, etc. As the device width increases, fewer devices are required to configure a given memory word—although the total number of bits remains constant. The wider organization can provide significant savings in power consumption, because a fewer number of devices are required to be powered up for access to a given memory word. In addition, the board layout design is simpler due to fewer traces and better layout advantages. The wider width is of particular advantage in microprocessors and bit-slice processors because most microprocessors are organized in 8-bit or 16-bit architectures. A memory chip configured in the nK x 8 organization can confer a definite advantage—especially in universal site applications. Conversely, there is usually a small speed penalty, at the device level for a x8 or x16 organization.

Types of Memories

The first step to narrowing down your choice is to determine the type of memory you are designing—data store or program store. After this has been done, the next step is to prioritize the following factors:

Performance
Power Consumption
Density
Cost

SUMMARY

Global Memory

Generally, a global memory is greater than 64K bytes and serves as a main memory for a microprocessor system. Here, the use of dynamic RAMs or Flash memory for read/write memory is dictated to provide the highest density and lowest cost per bit. The cost of providing refresh circuitry for the dynamic RAMs is spread over a large number of memory bits, thus minimizing the cost impact.

Local Memory

Local memories are usually less than 64K bytes and reside in the proximity of the processor itself—usually on the same PC board. Types of memories often used in local memory applications are SRAM, EPROM, Flash memory, and EEPROM.

Memory Technologies 2

INTEL MEMORY TECHNOLOGIES

Most of this handbook is devoted to techniques and information to help you design and implement semiconductor memory in your application or system. In this section, however, the memory chip itself will be examined and the processing technology required to turn a bare slice of silicon into high performance memory devices is described. The discussion has been limited to the basics of MOS (Metal Oxide Semiconductor) technologies as they are responsible for the majority of memory devices manufactured at Intel.

There are three major MOS technology families—PMOS, NMOS, and CMOS (Figure 1). They refer to the channel type of the MOS transistors made with the technology. PMOS technologies implement p-channel transistors by diffusing p-type dopants (usually boron) into an n-type silicon substrate to form the source and drain. P-channel is so named because the channel is comprised of positively charged carriers. NMOS technologies are similar, but use n-type dopants (normally phosphorus or arsenic) to make n-channel transistors in p-type silicon substrates. N-channel is so named because the channel is comprised of negatively charged carriers. CMOS or Complementary MOS technologies combine both p-channel and n-channel devices on the same silicon. Either p- or n-type silicon substrates can be used, however, deep areas of the opposite doping type (called wells) must be defined to allow fabrication of the complementary transistor type.

Most of the early semiconductor memory devices, like Intel's pioneering 1103 dynamic RAM and 1702 EPROM were made with PMOS technologies. As higher speeds and greater densities were needed, most new devices were implemented with NMOS. This was due to the inherently higher speed of n-channel charge carriers (electrons) in silicon along with improved process margins. CMOS technology has begun to see widespread commercial use in memory devices. It allows for very low power devices used for battery operated or battery back-up applications. Historically, CMOS has been slower than any NMOS device. However, CMOS technology has been improved to produce higher speed devices. The extra cost of processing required to make both transistor types had kept CMOS memories limited to those areas where the technology's special characteristics would justify the extra cost. In the future, the learning curve for high performance CMOS costs are making a larger number of memory devices practical in CMOS.

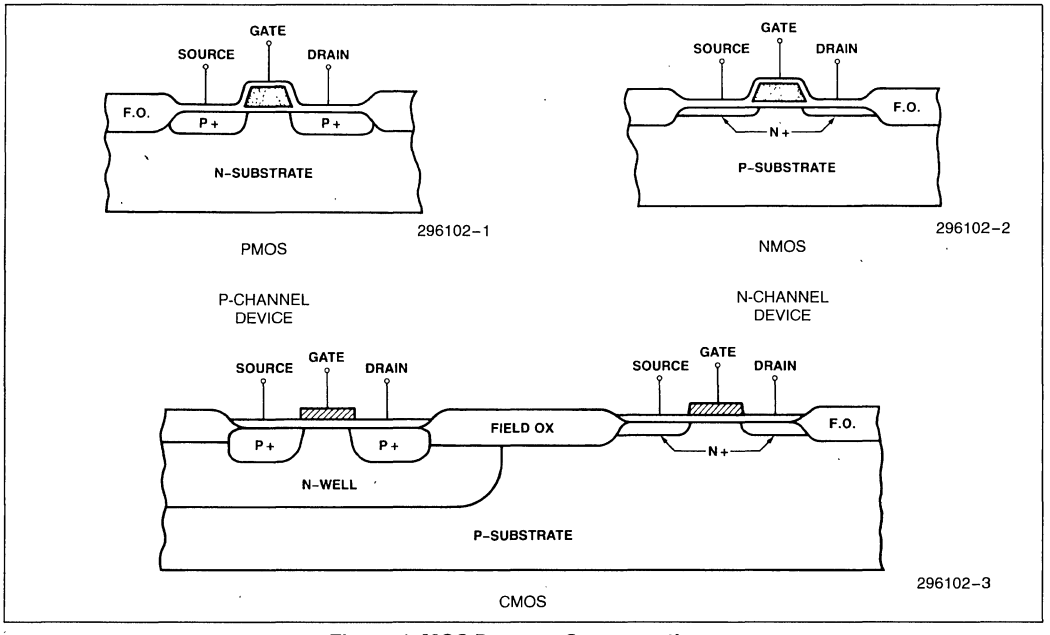


Figure 1. MOS Process Cross-sections

In the following section, the basic fabrication sequence for an HMOS circuit will be described. HMOS is a high performance n-channel MOS process developed by Intel for 5V single supply circuits. HMOS, and CHMOS, CHMOS-E (EPROM) and ETOX™ (Flash Memory), along with their evolutionary counterparts comprise the process family responsible for most of the memory components produced by Intel today.

The MOS IC fabrication process begins with a slice (or wafer) of single crystal silicon. Typically, it's 100 or 150 millimeter in diameter, about a half millimeter thick, and uniformly doped p-type. The wafer is then oxidized in a furnace at around 1000°C to grow a thin layer of silicon dioxide (SiO_2) on the surface. Silicon nitride is then deposited on the oxidized wafer in a gas phase chemical reactor. The wafer is now ready to receive the first pattern of what is to become a many layered complex circuit. The pattern is etched into the silicon nitride using a process known as photolithography, which will be described in a later section. This first pattern (Figure 2) defines the boundaries of the active regions of the IC, where transistors, capacitors, diffused resistors, and first level interconnects will be made.

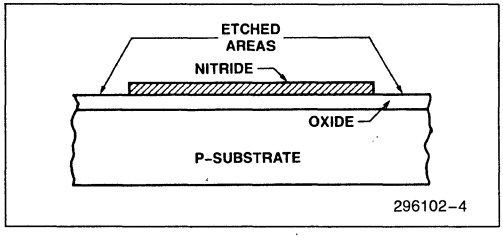


Figure 2. First Mask

The patterned and etched wafer is then implanted with additional boron atoms accelerated at high energy. The boron will only reach the silicon substrate where the nitride and oxide was etched away, providing areas doped strongly p-type that will electrically separate active areas. After implanting, the wafers are oxidized again and this time a thick oxide is grown. The oxide only grows in the etched areas due to silicon nitride's properties as an oxidation barrier. When the oxide is grown, some of the silicon substrate is consumed and this gives a physical as well as electrical isolation for adjacent devices as can be seen in Figure 3.

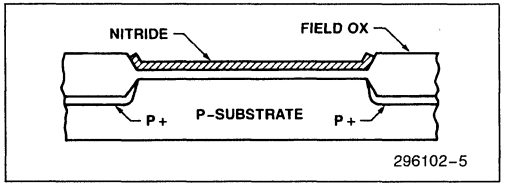


Figure 3. Post Field Oxidation

Having fulfilled its purpose, the remaining silicon nitride layer is removed. A light oxide etch follows taking with it the underlying first oxide but leaving the thick (field) oxide.

Now that the areas for active transistors have been defined and isolated, the transistor types needed can be determined. The wafer is again patterned and then if special characteristics (such as depletion mode operation) are required, it is implanted with dopant atoms. The energy and dose at which the dopant atoms are implanted determines much of the transistor's characteristics. The type of the dopant provides for depletion mode (n-type) or enhancement mode (p-type) operation.

The transistor types defined, the gate oxide of the active transistors are grown in a high temperature furnace. Special care must be taken to prevent contamination or inclusion of defects in the oxide and to ensure uniform consistent thickness. This is important to provide precise, reliable device characteristics. The gate oxide layer is then masked and holes are etched to provide for direct gate to diffusion ("buried") contacts where needed.

The wafers are now deposited with a layer of gate material. This is typically poly crystaline silicon ("poly") which is deposited in a gas phase chemical reactor similar to that used for silicon nitride. The poly is then doped (usually with phosphorus) to bring the sheet resistance down to 10–20 Ω/square. This layer is also used for circuit interconnects and if a lower resistance is required, a refractory metal/polysilicon composite or refractory metal silicide can be used instead. The gate layer is then patterned to define the actual transistor gates and interconnect paths (Figure 4).

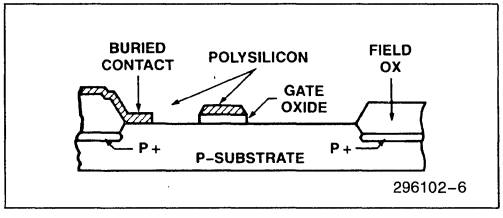


Figure 4. Post Gate Mask

The wafer is next diffused with n-type dopant (typically arsenic or phosphorus) to form the source and drain junctions. The transistor gate material acts as a barrier to the dopant providing an undiffused channel self-aligned to the two junctions. The wafer is then oxidized to seal the junctions from contamination with a layer of SiO_2 (Figure 5).

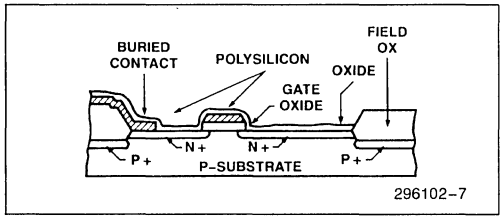


Figure 5. Post Oxidation

A thick layer glass is then deposited over the wafer to provide for insulation and sufficiently low capacitance between the underlying layers and the metal interconnect signals. (The lower the capacitance, the higher the inherent speed of the device.) The glass layer is then patterned with contact holes and placed in a high temperature furnace. This furnace step smooths the glass surface and rounds the contact edges to provide uniform metal coverage. Metal (usually aluminum or aluminum/silicon) is then deposited on the wafer and the interconnect patterns and external bonding pads are defined and etched (Figure 6). The wafers then receive a low temperature (approximately 500°C) alloy that insures good ohmic contact between the aluminum and diffusion or poly.

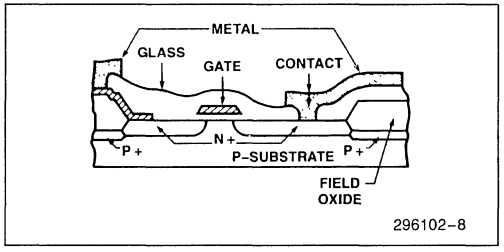


Figure 6. Complete Circuit (without passivation)

At this point the circuit is fully operational, however, the top metal layer is very soft and easily damaged by handling. The device is also susceptible to contamination or attack from moisture. To prevent this the wafers are sealed with a passivation layer of silicon nitride or a silicon and phosphorus oxide composite. Patterning is done for the last time opening up windows only over the bond pads where external connections will be made.

This completes basic fabrication sequence for a single poly layer process. Double poly processes such as those used for high density Dynamic RAMs, EPROMs, flash memories, and EEPROMs follow the same general process flow with the addition of gate, poly deposition, doping, and interlayer dielectric process modules required for the additional poly layer (Figure 7). These steps are performed right after the active areas have been defined (Figure 3) providing the capacitor or floating gate storage nodes on those devices.

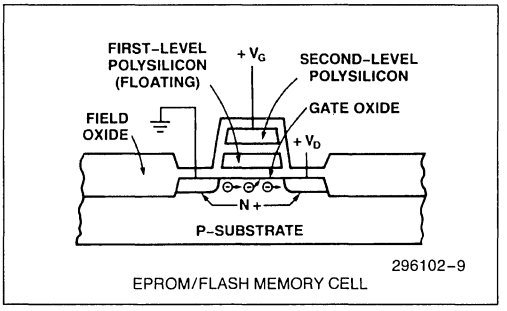


Figure 7. Double Poly Structure

After fabrication is complete, the wafers are sent for testing. Each circuit is tested individually under conditions designed to determine which circuits will operate properly both at low temperature and at conditions found in actual operation. Circuits that fail these tests are inked to distinguish them from good circuits. From here the wafers are sent from assembly where they are sawed into individual circuits with a paper-thin diamond blade. The inked circuits are then separated out and the good circuits are sent on for packaging.

Packages fall into two categories—hermetic and non-hermetic. Hermetic packages are Cerdip, where two ceramic halves are sealed with a glass fritt, or ceramic with soldered metal lids. An example of hermetic package assembly is shown in Table 1. Non-hermetic packages are molded plastics.

The ceramic package has two parts, the base, which has the leads and die (or circuit) cavity, and the metal lid. The base is placed on a heater block and a metal alloy preform is inserted. The die is placed on top of the preform which bonds it to the package. Once attached, wires are bonded to the circuit and then connected to the leads. Finally the package is placed in a dry inert atmosphere and the lid is soldered on.

The cerdip package consists of a base, lead frame, and lid. The base is placed on a heater block and the lead frame placed on top. This sets the lead frame in glass attached to the base. The die is then attached and bonded to the leads. Finally the lid is placed on the package and it is inserted in a seal furnace where the glass on the two halves melt together making a hermetic package.

In a plastic package, the key component is the lead frame. The die is attached to a pad on the lead frame and bonded out to the leads with gold wires. The frame then goes to an injection molding machine and the package is formed around the lead frame. After mold the excess plastic is removed and the leads trimmed.

After assembly, the individual circuits are retested at an elevated operating temperature to assure critical operating parameters and separated according to speed and power consumption into individual specification groups. The finished circuits are marked and then readied for shipment.

The basic process flow described above may make VLSI device fabrication sound straightforward, however, there are actually hundreds of individual operations that must be performed correctly to complete a working circuit. It usually takes well over two months to complete all these operations and the many tests and measurements involved throughout the manufacturing process. Many of these details are responsible for ensuring the performance, quality, and reliability you expect from Intel products. The following sections will discuss the technology underlying each of the major process elements mentioned in the basic process flow.

PHOTOLITHOGRAPHY

The photo or masking technology is the most important part of the manufacturing flow if for no other reason than the number of times it is applied to each wafer. The manufacturing process gets more complex in order to make smaller and higher performance circuits. As this happens the number of masking steps increases, the features get smaller, and the tolerance required becomes tighter. This is largely because the minimum size of individual pattern elements determine the size of the whole circuit, effecting its cost and limiting its potential complexity. Early MOS IC's used minimum geometries (lines or spaces) of 8–10 microns (1 micron = 10^{-6} meter ≅ 1/25,000 inch). The n-channel processes of the mid 1970's brought this down to approximately 5 microns, and today minimum geometries of one micron are in production. This dramatic reduction

Table 1. Typical Hermetic Package Assembly

Flow	Process/Materials	Typical Item	Frequency	Criteria
	Wafer			
	Die saw, wafer break			
	Die wash and plate			
	Die visual inspection	Passivation, metal	100% of die	
	QA gate		Every lot	0/76, LTPD = 5%
	Die attach (Process monitor)	Wet out	4 x /operator/shift	0/11 LTPD = 20%
	Post die attach visual		100% of devices	
	Wire bond (Process monitor)	Orientation, lead dressing, etc.	4 x /operator/ machine/shift	
	Post bond inspection		100% devices	
	QA gate	All previous items	every lot	1/129, LTPD = 3%
	Seal and Mark (Process monitor)	Cap align, glass integrity, moisture	4 x /furnace/shift	0/15, LTPD = 15%
	Temp cycle		10 x to mil std. 883 cond. C	1/11, LTPD = 20%
	Hermeticity check (Process monitor)	F/G leak	100% devices	
	Lead Trim (Process monitor)	Burrs, etc. (visual) Fine leak	4 x /station/shift 2 x /station/shift	0/15, LTPD = 15% 1/129, LTPD = 3%
	External visual	Solder voids, cap alignment, etc.	100% devices	
1.	QA gate	All previous items	All lots	1/129, LTPD = 3%
	Class test (Process monitor)	Run standards (good and reject) Calibrate every system using "autover" program	Every 48 hrs.	
	Mark and Pack			
2.	Final QA	(See attached)		

296102-11

NOTES:
1. Units for assembly reliability monitor.
2. Units for product reliability monitor.

in feature size was achieved using the newer high resolution photo resists and optimizing their processing to match improved optical printing systems.

A second major factor in determining the size of the circuit is the registration or overlay error. This is how accurately one pattern can be aligned to a previous one. Design rules require that space be left in all directions according to the overlay error so that unrelated patterns do not overlap or interfere with one another. As the error space increases the circuit size increases dramatically. Only a few years ago standard alignment tolerances were $\geq \pm 2$ microns; now advanced Intel processes have reduced this dramatically due mostly to the use of advanced projection and step and repeat exposure equipment.

The wafer that is ready for patterning must go through many individual steps before that pattern is complete. First the wafer is baked to remove moisture from its surface and is then treated with chemicals that ensure good resist adhesion. The thick photoresist liquid is then applied and the wafer is spun flat to give a uniform coating, critical for high resolution. The wafer is baked at a low temperature to solidify the resist into gel. It is then exposed with a machine that aligns a mask with the new pattern on it to a previously defined layer. The photo-resist will replicate this pattern on the wafer.

Negative working resists are polymerized by the light and the unexposed resist can be rinsed off with solvents. Positive working resists use photosensitive polymerization inhibitors that allow a chemically reactive developer to remove the exposed areas. The positive resists require much tighter control of exposure and development but yield higher resolution patterns than negative resistance systems.

The wafer is now ready to have its pattern etched. The etch procedure is specialized for each layer to be etched. Wet chemical etchants such as hydrofluoric acid for silicon oxide or phosphoric acid for aluminum are often used for this. The need for smaller features and tighter control of etched dimensions is increasing the use of plasma etching in fabrication. Here a reactor is run with a partial vacuum into which etchant gases are introduced and an electrical field is applied. This yields a reactive plasma which etches the required layer.

The wafer is now ready for the next process step. Its single journey through the masking process required the careful engineering of mechanics, optics, organic chemistry, inorganic chemistry, plasma chemistry, physics, and electronics.

DIFFUSION

The picture of clean room garbed operators tending furnace tubes glowing cherry red is the one most often associated with IC fabrication. These furnace operations are referred to collectively as diffusion because they employ the principle of sold state diffusion of matter to accomplish their results. In MOS processing, there are three main types of diffusion operations: predeps, drives, and oxidations.

Predeposition, or "predep," is an operation where a dopant is introduced into the furnace from a solid, liquid, or gaseous source and at the furnace temperature (usually 900°C–1200°C) a saturated solution is formed at the silicon surface. The temperature of the furnace, the dopant atom, and rate of introduction are all engineered to give a specific dose of the dopant on the wafer. Once this is completed the wafer is given a drive cycle where the dopant left at the surface by the predep is driven into the wafer by high temperatures. These are generally at different temperatures than the predeps and are designed to give the required junction depth and concentration profile.

Oxidation, the third category, is used at many steps of the process as was shown in the process flow. The temperature and oxidizing ambient can range from 800°C to 1200°C and from pure oxygen to mixtures of oxygen and other gases to steam depending on the type of oxide required. Gate oxides require high dielectric breakdown strength for thin layers (between 0.01 and 0.1 micron) and very tight control over thickness (typically ± 0.005 micron or less than $\pm 1/5{,}000{,}000$ inch), while isolation oxides need to be quite thick and because of this their dielectric breakdown strength per unit thickness is much less important.

The properties of the diffused junctions and oxides are key to the performance and reliability of the finished device so the diffusion operations must be extremely well controlled for accuracy, consistency and purity.

ION IMPLANT

Intel's high performance products require such high accuracy and repeatability of dopant control that even the high degree of control provided by diffusion operations is inadequate. However, this limitation has been overcome by replacing critical predeps with ion implantation. In ion implantation, ionized dopant atoms are accelerated by an electric field

and implanted directly into the wafer. The acceleration potential determines the depth to which the dopant is implanted.

The charged ions can be counted electrically during implantation giving very tight control over dose. The ion implanters used to perform this are a combination of high vacuum system, ion source, mass spectrometer, linear accelerator, ultra high resolution current integrator, and ion beam scanner. You can see that this important technique requires a host of sophisticated technologies to support it.

THIN FILMS

Thin film depositions make up most of the features on the completed circuit. They include the silicon nitride for defining isolation, polysilicon for the gate and interconnections, the glass for interlayer dielectric, metal for interconnection and external connections, and passivation layers. Thin film depositions are done by two main methods: physical deposition and chemical vapor deposition. Physical deposition is most common for deposition metal. Physical depositions are performed in a vacuum and are accomplished by vaporizing the metal with a high energy electron beam and redepositing it on the wafer or by sputtering it from a target to the wafer under an electric field.

Chemical vapor deposition can be done at atmospheric pressure or under a moderate vacuum. This type of deposition is performed when chemical gases react at the wafer surface and deposit a solid film of the reaction product. These reactors, unlike their general industrial counterparts, must be controlled on a microscale to provide exact chemical and physical properties for thin films such as silicon dioxide, silicon nitride, and polysilicon.

The fabrication of modern memory devices is a long, complex process where each step must be monitored, measured and verified. Developing a totally new manufacturing process for each new product or even product line takes a long time and involves significant risk. Because of this, Intel has developed process families, such as HMOS, on which a wide variety of devices can be made. These families are scalable so that circuits need not be totally redesigned to meet your needs for higher performance.[1] They are evolutionary so that development time of new processes and products can be reduced without compromising Intel's commitment to consistency, quality, and reliability.

The manufacture of today's MOS memory devices requires a tremendous variety of technologies and manufacturing techniques, many more than could be mentioned here. Each requires a team of experts to design, optimize, control and maintain it. All these people and thousands of others involved in engineering, design, testing and production stand behind Intel's products.

Because of these extensive requirements, most manufacturers have not been able to realize their needs for custom circuits on high performance, high reliability processes. To address this Intel's expertise in this area is now available to industry through the silicon foundry. Intel supplies design rules and support to design and debug circuits. This includes access to Intel's n-well CHMOS technology. Users of the foundry can now benefit from advanced technology without developing processes and IC manufacturing capability themselves.

[1]R. Pashley, K. Kokkonen, E. Boleky, R. Jecmen, S. Liu, and W. Owen, "H-MOS Scales Traditional Devices to Higher Performance Level," *Electronics*, August 18, 1977.

Dynamic RAMs (Random Access Memories)

3

21256
262,144 x 1-BIT DYNAMIC RAM WITH PAGE MODE

Symbol	Parameter	21256-06	21256-07	21256-08	21256-10	Units
t_{RAC}	Access Time from $\overline{RAS}$	60	70	80	100	ns
t_{CAC}	Access Time from $\overline{CAS}$	20	20	20	50	ns
t_{RC}	Read Cycle Time	110	130	150	190	ns

- **Page Mode Capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-Only and Hidden Refresh Capability**
- **TTL Compatible Inputs and Output**
- **Common I/O Using Early Write**
- **Single +5V ±10% Power Supply**
- **256 Cycle/4 ms Refresh**
- **JEDEC Standard Pinout in DIP, ZIP and PLCC**

The 21256 is a fully decoded dynamic random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The 21256 features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the 21256 to be housed in a JEDEC standard 16-pin DIP.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

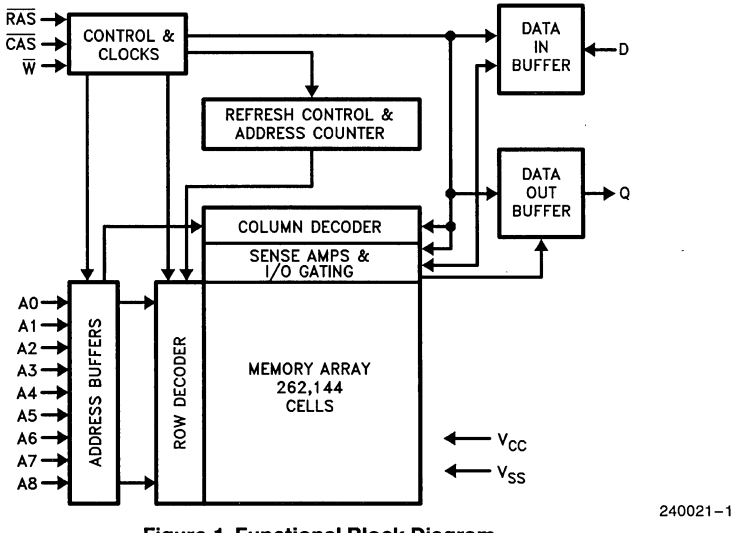
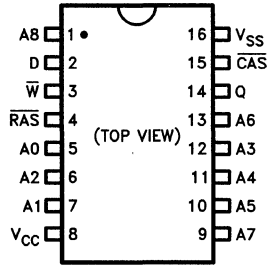


Figure 1. Functional Block Diagram

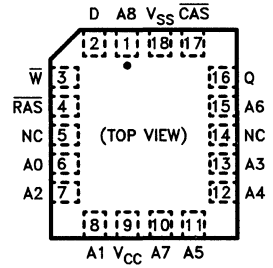
September 1990
Order Number: 240021-004

DIP



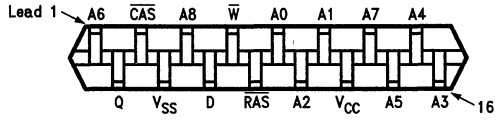
240021-2

PLCC



240021-3

ZIP



240021-4

(Bottom View)

Pin Names

A_0–A_8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin
Relative to V_{SS} ..... V_{OUT} −1.0V to +7.0V
Voltage on V_{CC} Supply
Relative to V_{SS} ..... −1.0V to +7.0V
Storage Temperature ..... −55°C to +125°C
Power Dissipation 1.0W
Short Circuit Output Current ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltages referenced to V_{SS}, T_A = 0 to 70°C

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		$V_{CC}+1$	V
V_{IL}	Input Low Voltage	−1		0.8	V

3

D.C. AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Symbol	Parameter		Min	Max	Units	Test Condition
I_{CC1}	Operating Current*	21256-06		75	mA	($\overline{RAS}$ and $\overline{CAS}$
		21256-07		70	mA	cycling @ t_{RC} = min.)
		21256-08		60	mA	
		21256-10		55	mA	
I_{CC2}	Standby Current	21256-06		2.0	mA	($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})
		21256-07		2.0	mA	
		21256-08		2.0	mA	
		21256-10		5.0	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current*	21256-06		75	mA	($\overline{CAS}$ = V_{IH}, $\overline{RAS}$
		21256-07		70	mA	cycling @ t_{RC} = min.)
		21256-08		60	mA	
		21256-10		40	mA	
I_{CC4}	Page Mode Current*	21256-06		50	mA	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling;
		21256-07		45	mA	t_{PC} = min.)
		21256-08		40	mA	
		21256-10		35	mA	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current*	21256-06		75	mA	($\overline{RAS}$ cycling @ t_{RC} = min.)
		21256-07		65	mA	
		21256-08		55	mA	
		21256-10		55	mA	
I_{CC6}	Standby Current			1.0	mA	($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)
I_{IL}	Input Leakage Current		−10	10	μA	(Any input 0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, All other pins not under test = 0.)
I_{OL}	Output Leakage Current		−10	10	μA	(Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V)

***NOTE:**
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as average current.

D.C. AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted. (Continued)

Symbol	Parameter		Min	Max	Units	Test Condition
V_{OH}	Output High Voltage Level		2.4		V	(I_{OH} = 5 mA)
V_{OL}	Output Low Voltage Level			0.4	V	(I_{OL} = 4.2 mA)

CAPACITANCE T_A = 25°C

Symbol	Parameter	Min	Max	Units
C_{IN1}	Input Capacitance (A_0–A_8, D)		5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		8	pF
C_{OUT}	Output Capacitance (Q)		7	pF

A.C. CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ±10%. See Notes 1, 2)

Symbol	Parameter	21256-06		21256-07		21256-08		21256-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120		135		150		190		ns	
t_{RWC}	Read-Modify-Write Cycle Time	135		155		175		220		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	3,4,11
t_{CAC}	Access Time from $\overline{CAS}$		15		25		30		50	ns	3,4,5
t_{AA}	Column Address Access Time		35		35		40		50	ns	3,10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		5		5		ns	3
t_{OFF}	Output Buffer Turn-Off Delay	0	25	0	25	0	25	0	30	ns	7
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	100	ns	2
t_{RP}	$\overline{RAS}$ Precharge Time	55		65		75		80		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15		25		30		50		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (All Cycles except Page Mode)	10		10		15		25		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	25	10,000	30	10,000	50	10,000	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	50	25	50	25	60	25	75	ns	4
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	20	35	20	40	20	55	ns	11
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time ($\overline{RAS}$ Only Refresh)	5		15		15		15		ns	
t_{ASR}	Row Address Setup Time	0		0		0		0		ns	

A.C. CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2) (Continued)

Symbol	Parameter	21256-06		21256-07		21256-08		21256-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAH}	Row Address Hold Time	15		15		15		15		ns	
t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	10		15		20		20		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50		55		65		75		ns	6
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	9
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	9
t_{WCS}	Write Command Setup Time	0		0		0		0		ns	8
t_{WCH}	Write Command Hold Time	15		15		15		35		ns	
t_{WP}	Write Command Pulse Width	10		15		15		35		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		25		30		35		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		25		30		35		ns	
t_{DS}	Data-In Setup Time	0		0		0		0		ns	10
t_{DH}	Data-In Hold Time	10		15		15		35		ns	10
t_{CWD}	$\overline{CAS}$ to Write Enable Delay	15		20		25		40		ns	8
t_{RWD}	$\overline{RAS}$ to Write Enable Delay	60		70		80		100		ns	8
t_{AWD}	Column Address to $\overline{W}$ Delay Time	35		35		40		50		ns	8
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	40		55		60		85		ns	6
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50		55		60		85		ns	6
t_{REF}	Refresh Period (256 Cycles)		4		4		4		4	ms	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH											
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	10		10		10		15		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	10		20		25		30		ns	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time	15		35		50		60		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	10		10		10		10		ns	
PAGE MODE											
t_{PC}	Page Mode Cycle Time	40		50		55		90		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode Only)	10		15		15		30		ns	

3

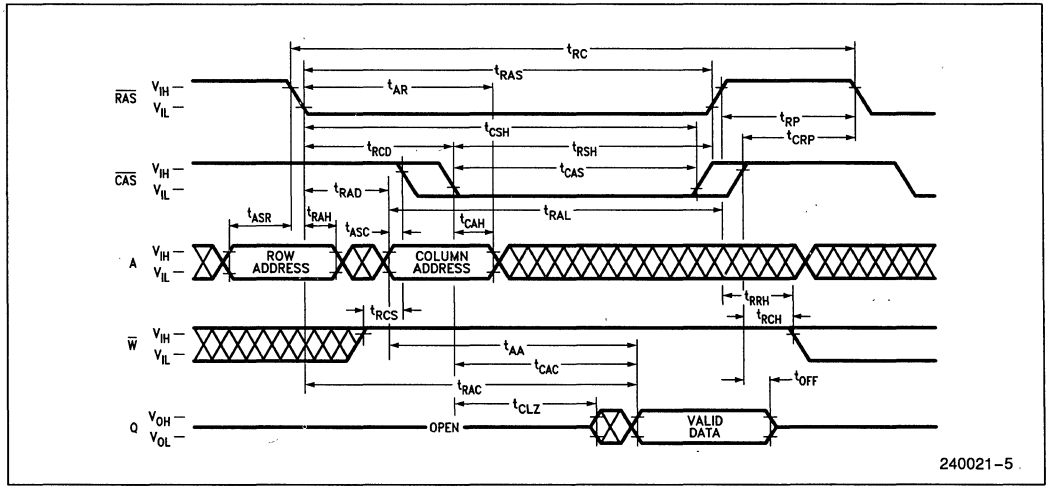
A.C. CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2) (Continued)

Symbol	Parameter	21256-06		21256-07		21256-08		21256-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
PAGE MODE (Continued)											
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		50		55	ns	3
t_{PRWC}	Fast Page Mode Read-Modify-Write	65		75		85		95		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	10,000	70	10,000	80	10,000	100	10,000	ns	

NOTES:
1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100 pF.
4. Operation within the T_{RCD}(max) limit ensures that T_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \ge t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \ge t_{CWD(min)}$, $t_{RWD} \ge t_{RWD(min)}$ and $t_{AWD} \ge t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

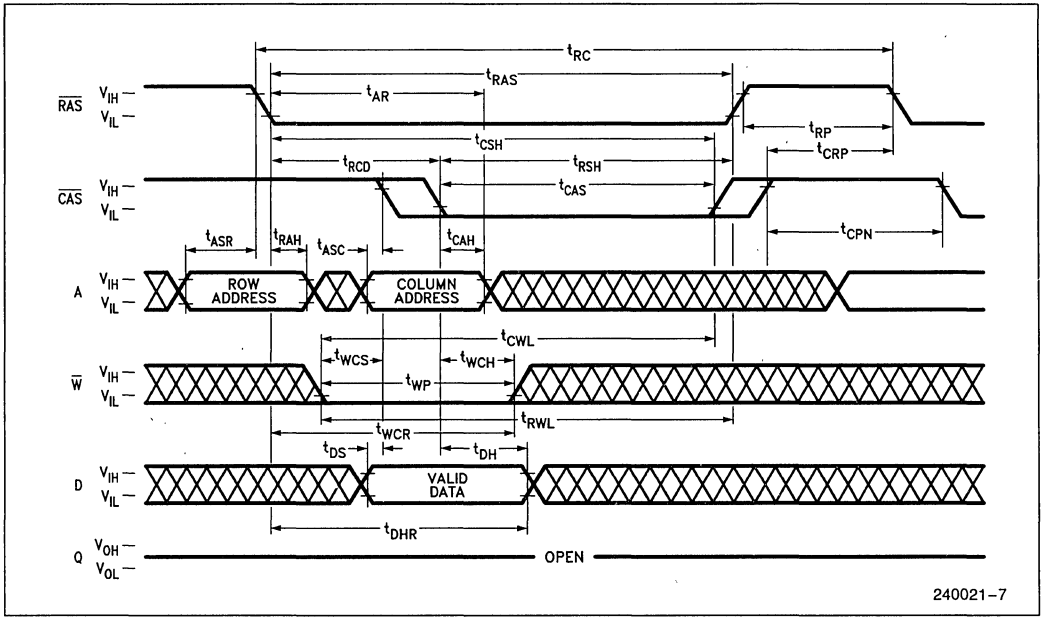


Don't Care

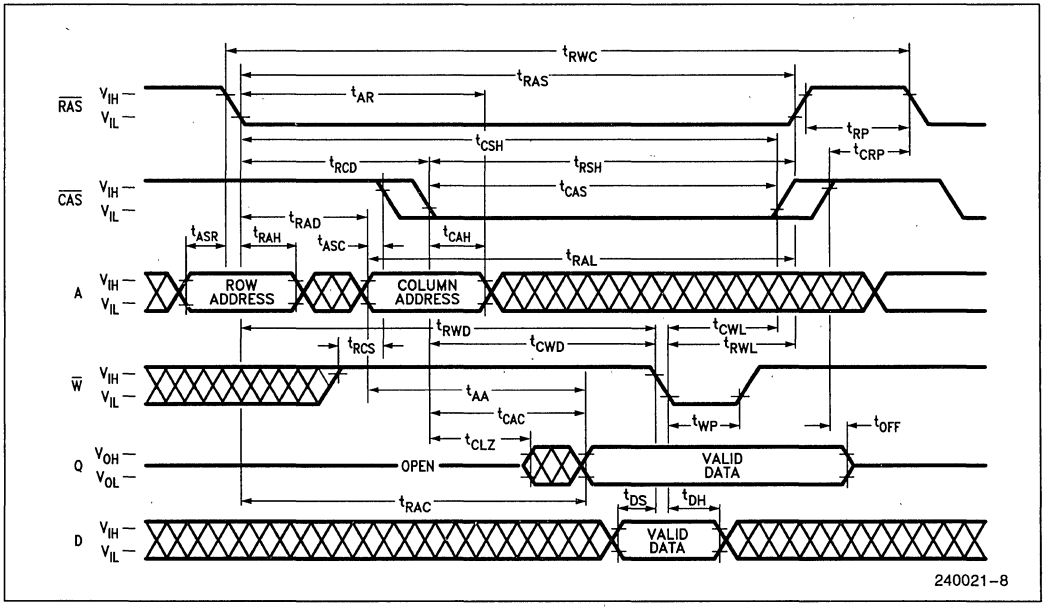
240021-6

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE

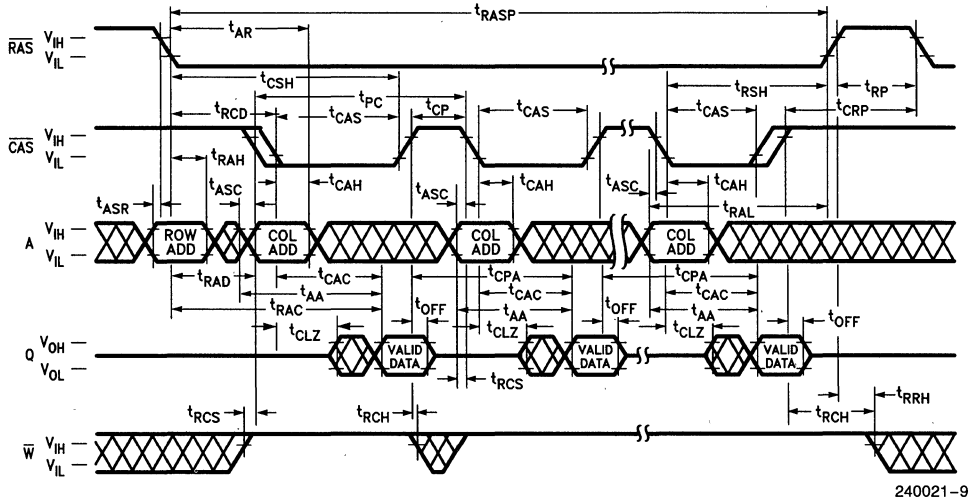


Don't Care

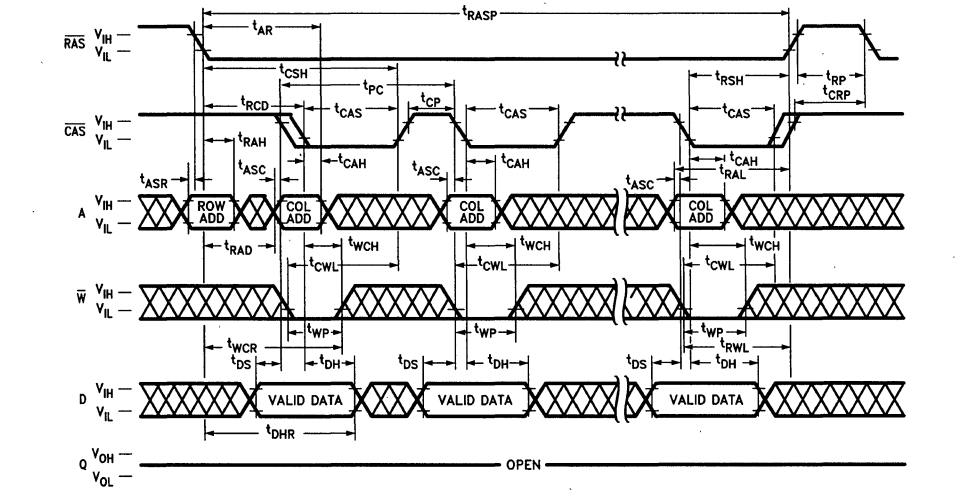
240021-6

TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



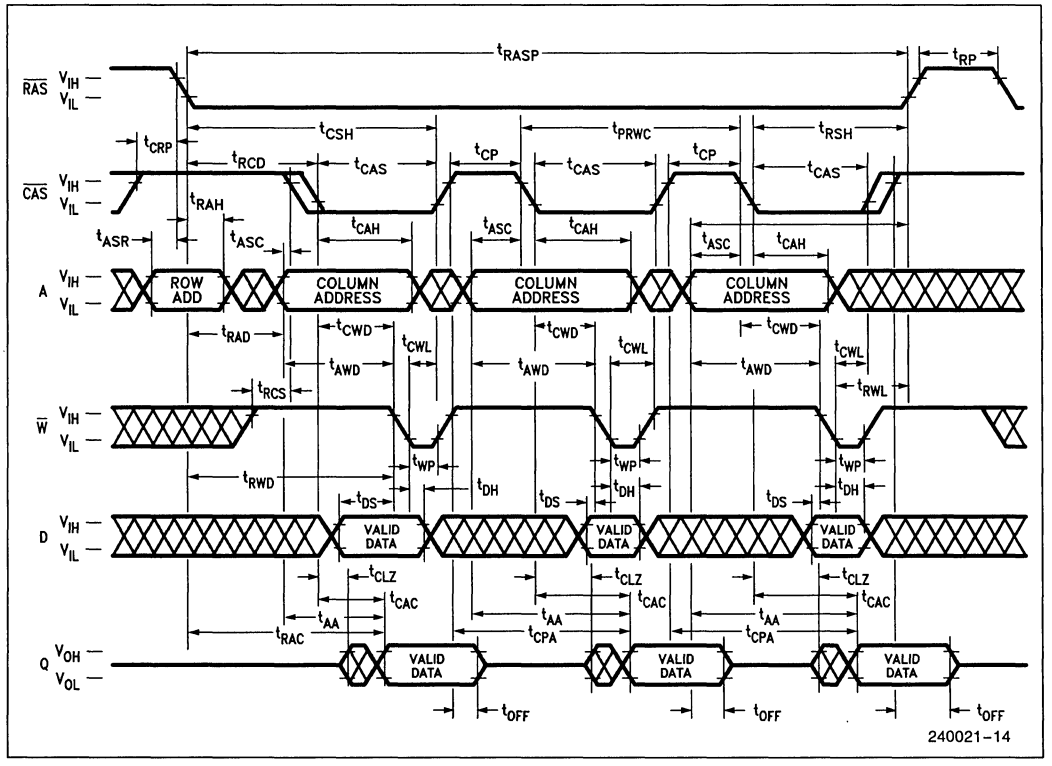
PAGE MODE WRITE CYCLE (EARLY WRITE)



Don't Care 240021-6

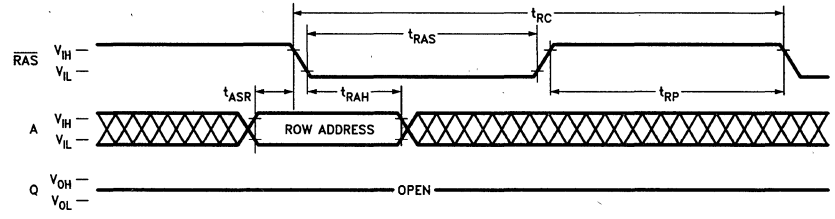
TIMING DIAGRAMS (Continued)

PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

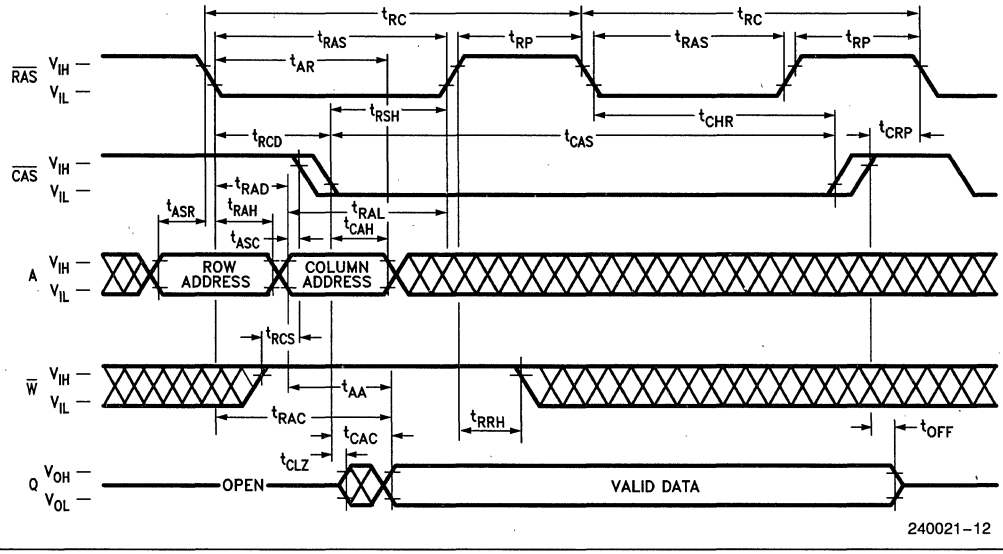
$\overline{RAS}$-ONLY REFRESH CYCLE



240021-11

NOTE:
$\overline{CAS}$ = V_{IH}: $\overline{W}$, D = Don't Care

HIDDEN REFRESH CYCLE



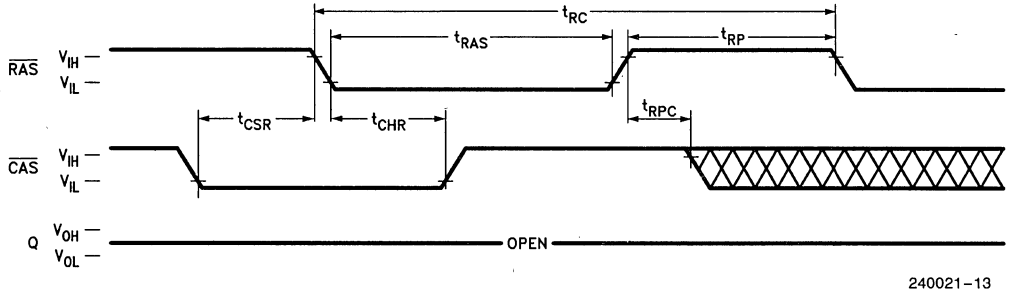
240021-12

Don't Care

240021-6

TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



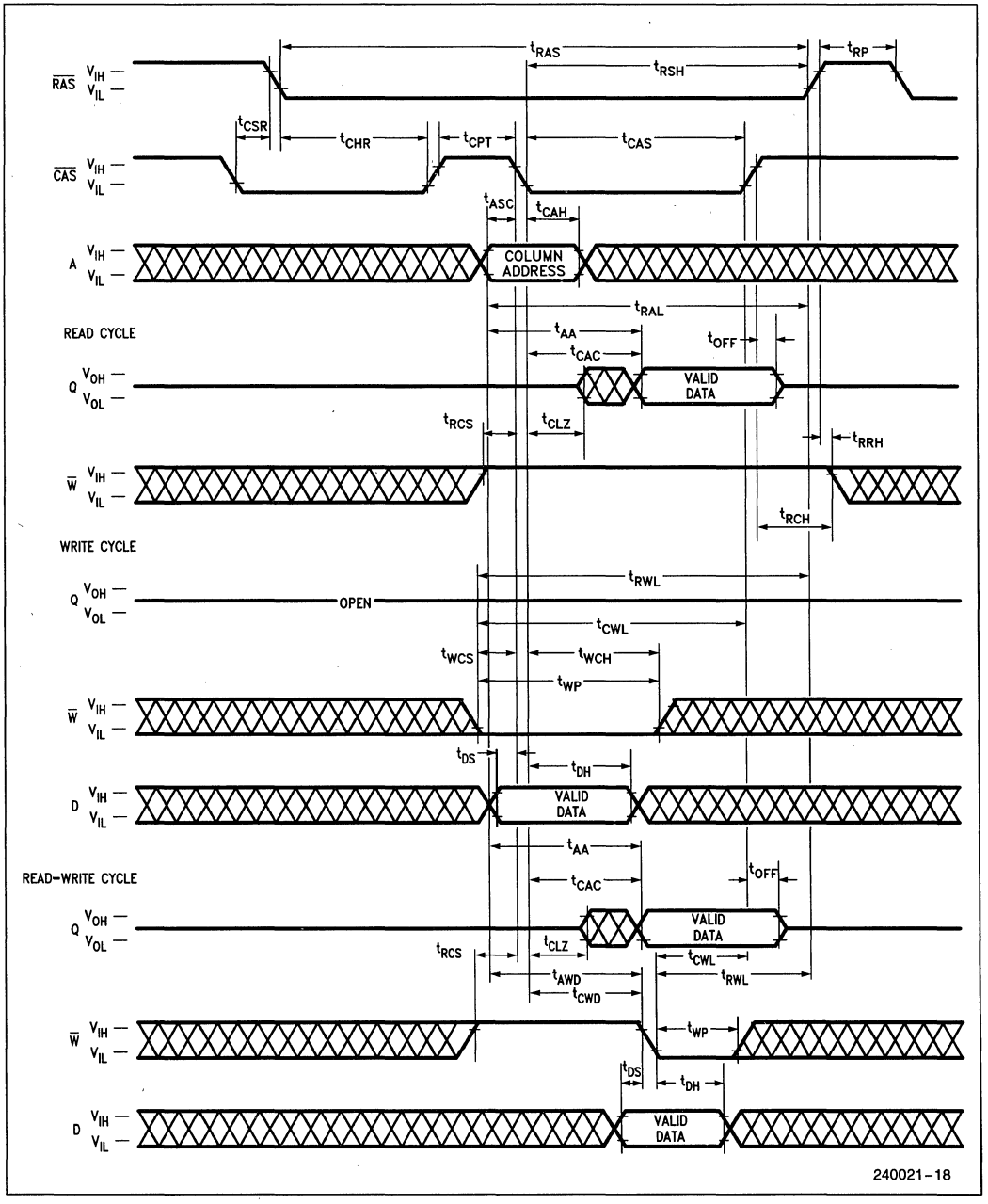
NOTE:
Address, $\overline{W}$, D = Don't Care

Don't Care 240021-6

3

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



Don't Care

240021-6

DEVICE OPERATION

The 21256 contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the 21256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}/\overline{CAS}$ cycle. The output of the 21256 remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 21256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21256 has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write). Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the 21256 is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the 21256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Page Mode

The 21256 has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21256 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. 8 initialization cycles are also required after any 4 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21256 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21256 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

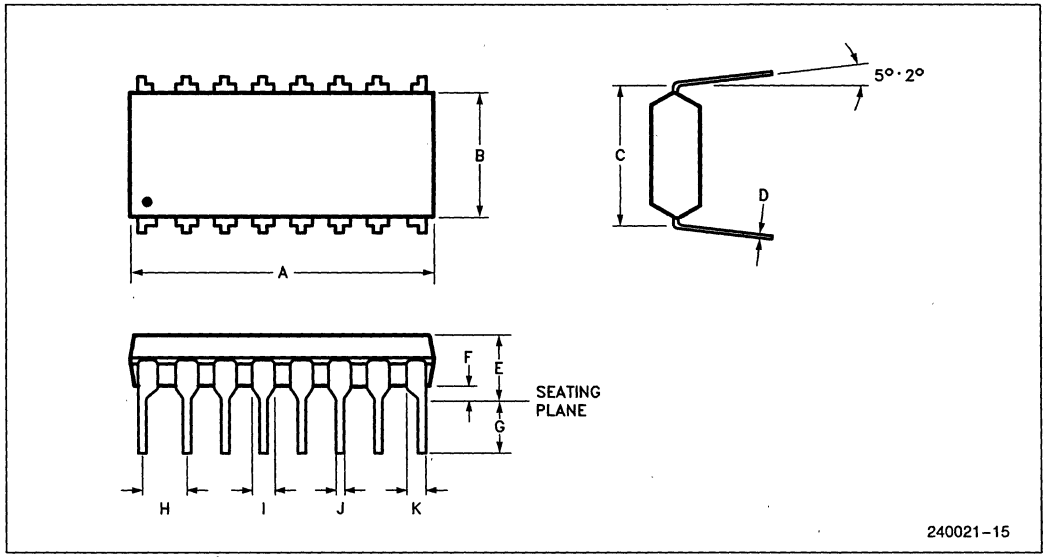
The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21256 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21256 and they supply much of the current used by the 21256 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

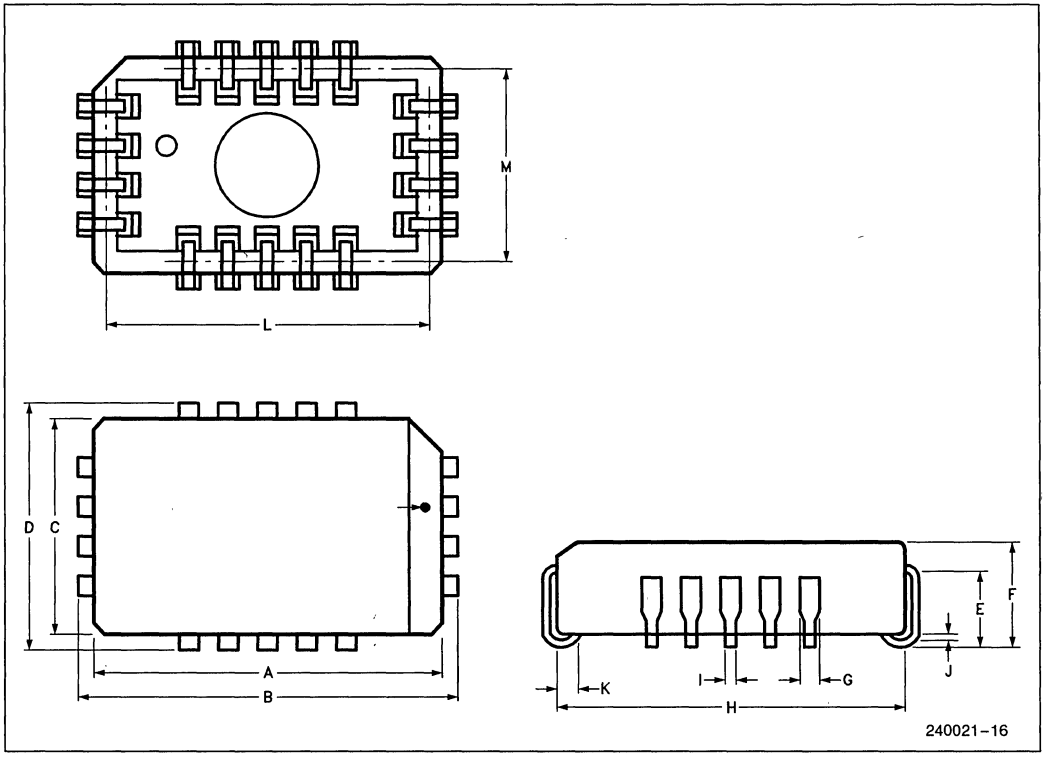
16-LEAD PLASTIC DUAL-IN-LINE PACKAGE



Item	Millimeters	Inches
A	19.43 ±0.05	0.765 ±0.002
B	6.86 ±0.05	0.270 ±0.002
C	7.62	0.300
D	0.25 ±0.025	0.010 ±0.001
E	3.56 ±0.05	0.140 ±0.002
F	0.506 ±0.1	0.020 ±0.004
G	3.3 ±0.1	0.130 ±0.004
H	2.54	0.100
I	1.52	0.060
J	0.457 ±0.05	0.018 ±0.002
K	0.1 ±0.05	0.040 ±0.002

PACKAGE DIMENSIONS (Continued)

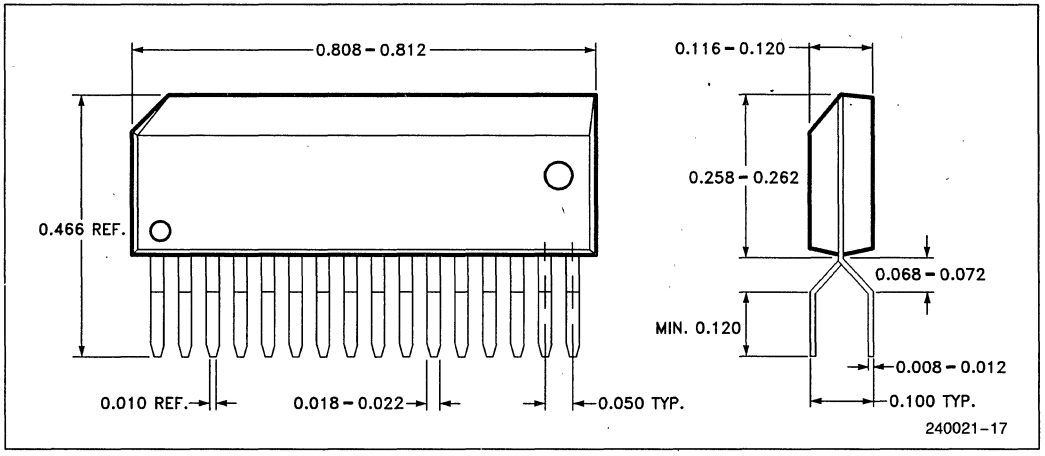
18-PIN PLASTIC LEADED CHIP CARRIER



Item	Millimeters	Inches
A	12.346 ±0.052	0.490 ±0.002
B	13.2585 ±0.0505	0.522 ±0.002
C	7.366 ±0.051	0.290 ±0.002
D	8.179 ±0.051	0.322 ±0.002
E	2.083 ±0.051	0.082 ±0.002
F	3.505 ±0.051	0.020 ±0.004
G	0.7365 ±0.0505	0.029 ±0.002
H	6.553 ±0.051	0.258 ±0.002
I	**0.43 typ**	**0.017 typ**
J	0.279 ±0.025	0.011 ±0.001
K	**0.76 typ**	**0.030 typ**
L	11.8365 ±0.0505	0.466 ±0.002
M	0.1 ±0.05	0.04 ±0.002

PACKAGE DIMENSIONS (Continued)

16-LEAD ZIG ZAG INLINE PACKAGE (ZIP)



21464
65,536 x 4-BIT DYNAMIC RAM WITH PAGE MODE

Symbol	Parameter	21464-06	21464-07	21464-08	21464-10	Units
t_{RAC}	Access Time from $\overline{RAS}$	60	70	80	100	ns
t_{CAC}	Access Time from $\overline{CAS}$	15	25	30	50	ns
t_{RC}	Read Cycle Time	110	130	150	190	ns

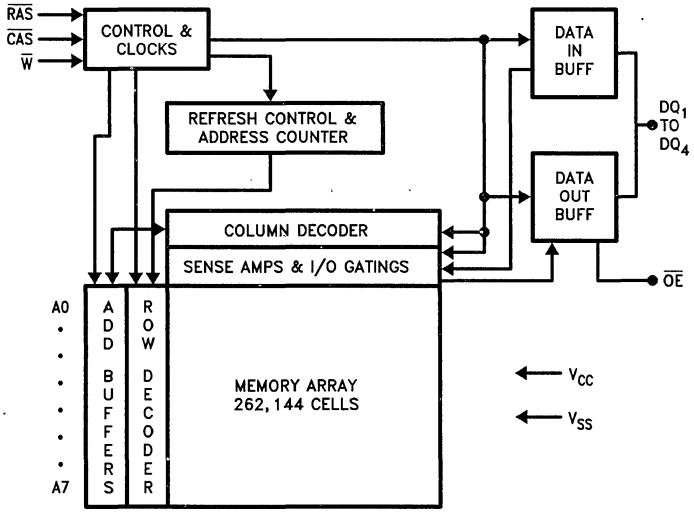
- **Page Mode Capability**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-Only and Hidden Refresh Capability**
- **TTL Compatible Inputs and Outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V ±10% Power Supply**
- **256 Cycle/4 ms Refresh**
- **JEDEC Standard Pinout in DIP, PLCC, ZIP**

The 21464 is a fully decoded 65,536 x 4 dynamic random access memory. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

3

The 21464 features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the 21464 to be housed in a standard 18-pin DIP.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.



240022-1

Figure 1. Functional Block Diagram

October 1990
Order Number: 240022-005

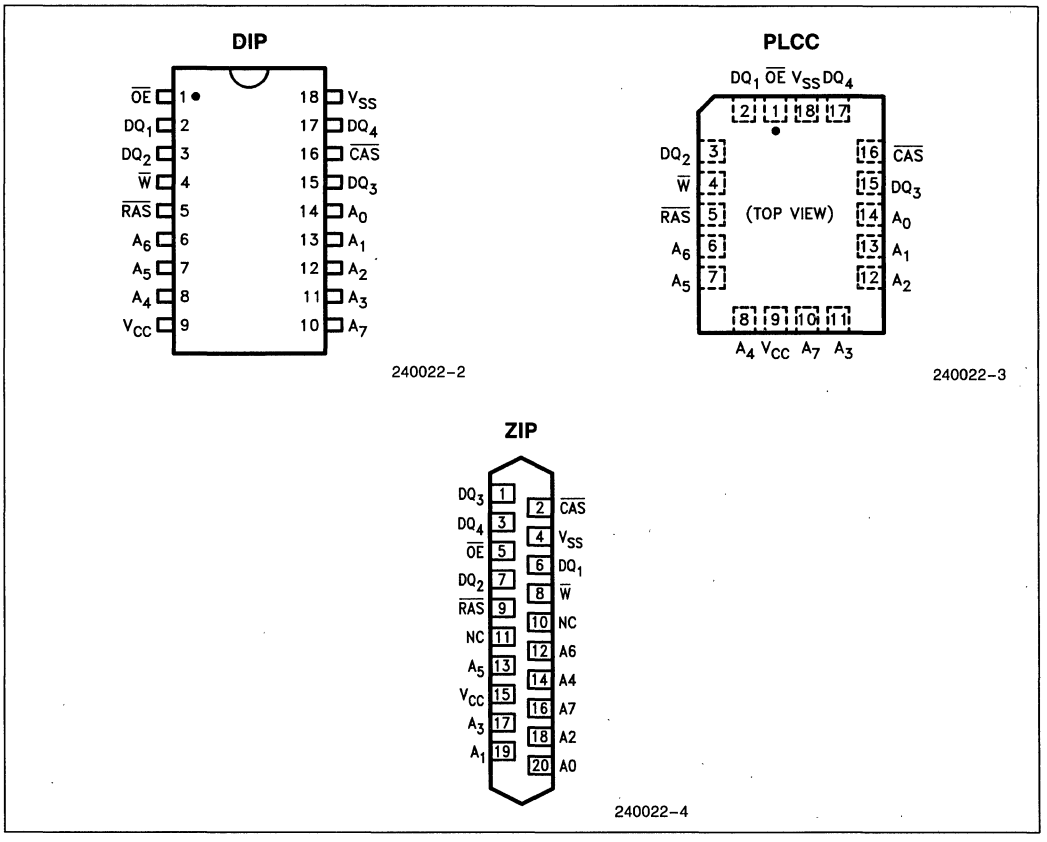


Figure 2. Pin Configurations

PIN NAMES

A_0–A_7	Address Input
DQ_1–DQ_4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
$\overline{OE}$	Output Enable

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin
Relative to V_{SS} ..... −1V to +7V
Voltage on V_{CC} Supply
Relative to V_{SS} ..... −1V to +7V
Storage Temperature ..... −55°C to +125°C
Power Dissipation 1.0W
Short Circuit Output Current ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltages referenced to V_{SS}, T_A = 0 to 70°C

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0		0.8	V

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D.C. OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted

Symbol	Parameter		Min	Max	Units	Test Condition
I_{CC1}	Operating Current*	21464-06		75	mA	$\overline{RAS}$ and $\overline{CAS}$ Cycling
		21464-07		70	mA	@ t_{RC} = Min
		21464-08		65	mA	
		21464-10		55	mA	
I_{CC2}	Standby Current	21464-06		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
		21464-07		2.0	mA	
		21464-08		2.0	mA	
		21464-10		5.0	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current*	21464-06		75	mA	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling
		21464-07		70	mA	@ t_{RC} = Min
		21464-08		60	mA	
		21464-10		40	mA	
I_{CC4}	Page Mode Current*	21464-06		50	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling:
		21464-07		45	mA	t_{PC} = Min
		21464-08		40	mA	
		21464-10		35	mA	
I_{CC5}	$\overline{CAS}$-Before-$\overline{RAS}$* Refresh Current	21464-06		75	mA	$\overline{RAS}$ Cycling @ t_{RC} = Min
		21464-07		70	mA	
		21464-08		65	mA	
		21464-10		55	mA	
I_{IL}	Input Leakage Current		−10	10	μA	Any Input 0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, All Other Pins Not Under Test = 0V
I_{DQL}	Output Leakage Current		−10	10	μA	Data Out is Disabled, 0V ≤ V_{OUT} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V
V_{OH}	Output High Voltage Level		2.4		V	I_{OH} = 5 mA
V_{OL}	Output Low Voltage Level			0.4	V	I_{OL} = 4.2 mA

NOTE:
*I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE T_A = 25°C

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (A_0–A_7)		5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)		8	pF
C_{DQ}	Output Capacitance (D_{Q1}–D_{Q4})		7	pF

A.C. CHARACTERISTICS ($0°C \leq T_A \leq 70°C = 5.0V \pm 10\%$. See notes 1, 2)

Symbol	Parameter	21464-06		21464-07		21464-08		21464-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120		135		150		190		ns	
t_{RWC}	Read-Modify-Write Cycle Time	165		195		225		265		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	3, 4, 11
t_{CAC}	Access Time from $\overline{CAS}$		15		25		30		50	ns	3, 4, 5
t_{AA}	Access Time from Column Address		35		35		40		50	ns	3, 10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		5		5		ns	3
t_{OFF}	Output Buffer Turn-Off Delay	0	25	0	25	0	25	0	30	ns	7
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	100	ns	2
t_{RP}	$\overline{RAS}$ Precharge Time	55		65		75		80		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15		25		30		50		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)	10		10		15		25		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	25	10,000	30	10,000	50	10,000	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	50	25	50	25	60	25	75	ns	4
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	20	35	20	40	20	55	ns	11
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time ($\overline{RAS}$ Only Refresh)	5		15		15		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	10		15		20		20		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50		55		65		75		ns	6

A.C. CHARACTERISTICS ($0°C \leq T_A \leq 70°C = 5.0V \pm 10\%$. See notes 1, 2) (Continued)

Symbol	Parameter	21464-06		21464-07		21464-08		21464-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	9
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	9
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns	8
t_{WCH}	Write Command Hold Time	15		15		15		35		ns	
t_{WP}	Write Command Pulse Width	10		15		15		35		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		25		30		35		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		25		30		35		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns	10
t_{DH}	Data-In Hold Time	10		15		15		35		ns	10
t_{CWD}	$\overline{CAS}$ to Write Enable Delay	35		50		60		70		ns	8
t_{RWD}	$\overline{RAS}$ to Write Enable Delay	90		100		110		135		ns	8
t_{AWD}	Column Address to $\overline{W}$ Delay Time	60		65		70		85		ns	8
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	40		55		60		85		ns	6
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50		55		60		85		ns	6
t_{OEA}	Access Time from $\overline{OE}$		15		20		20		25	ns	
t_{OED}	$\overline{OE}$ to Data in Delay Time	15		20		25		30		ns	
t_{OEZ}	Output Buffer Turn Off Delay from $\overline{OE}$		15		20		20	0	30	ns	
t_{OEH}	$\overline{OE}$ Hold Time Referenced to W	15		20		20		25		ns	
t_{REF}	Refresh Period (256 Cycles)		4		4		4		4	ms	

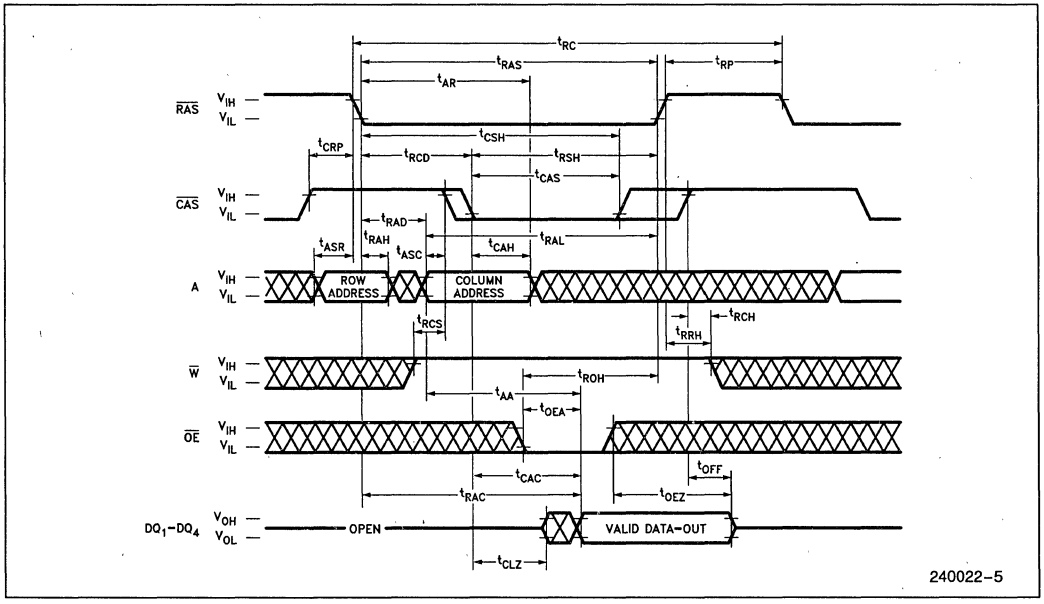
A.C. CHARACTERISTICS ($0°C \leq T_A \leq 70°C = 5.0V \pm 10\%$. See notes 1, 2) (Continued)

Symbol	Parameter	21464-06		21464-07		21464-08		21464-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	10		10		10		15		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh)	10		20		25		30		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10		10		10		10		ns	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge	15		35		50		60		ns	
t_{PC}	Page Mode Cycle Time	40		50		55		90		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode Only)	10		15		15		30		ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		50		55	ns	3
t_{PRWC}	Fast Page Mode Read-Modify-Write	95		105		120		140		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		15		20		20		ns	

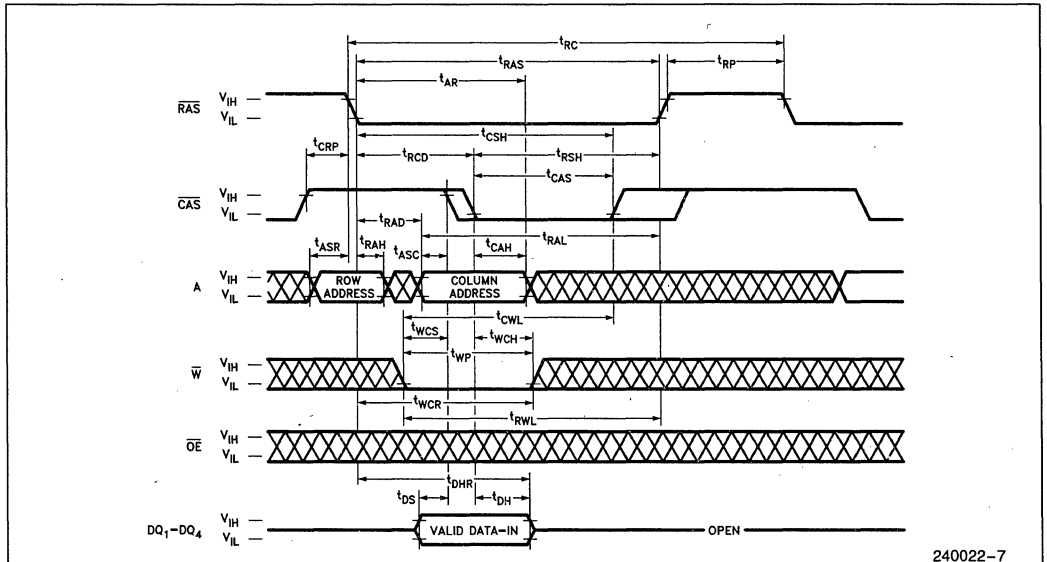
NOTES:
1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IN}(min) and V_{IL}(max) are referenced levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100 pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

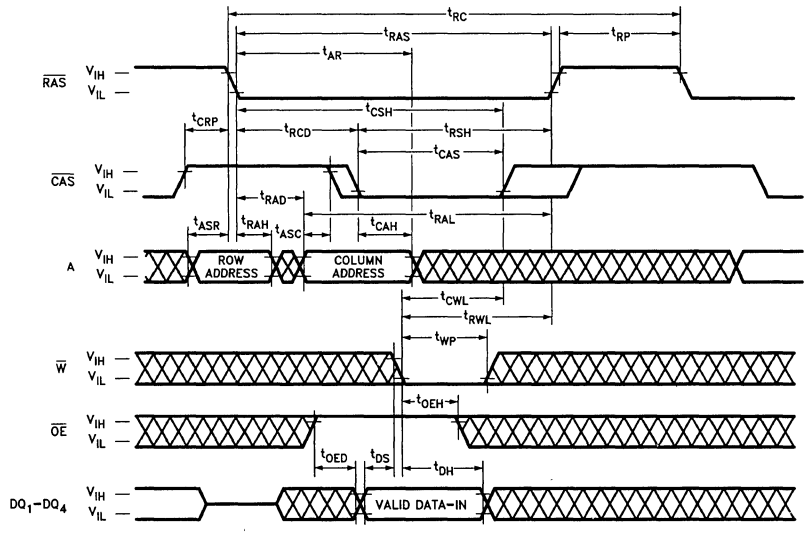


NOTE:
$\overline{OE}$ = Don't Care

240022–6

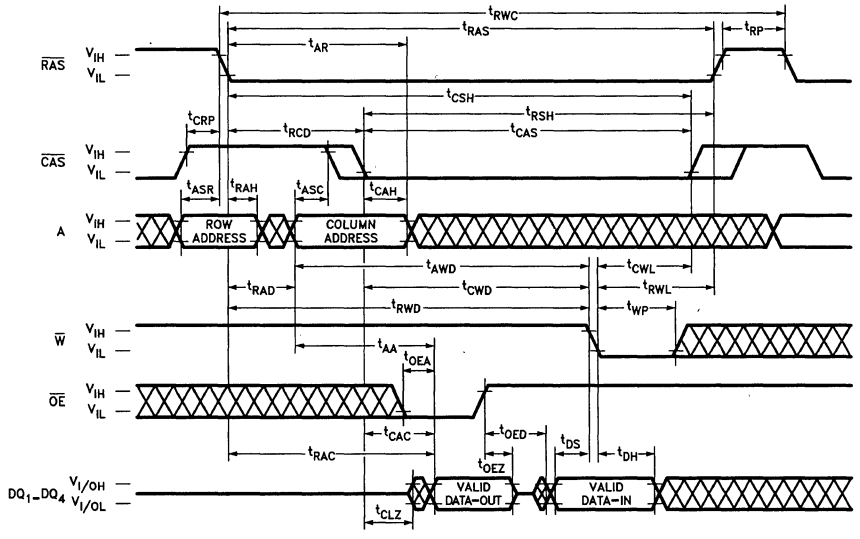
TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



240022-8

READ-MODIFY-WRITE CYCLE



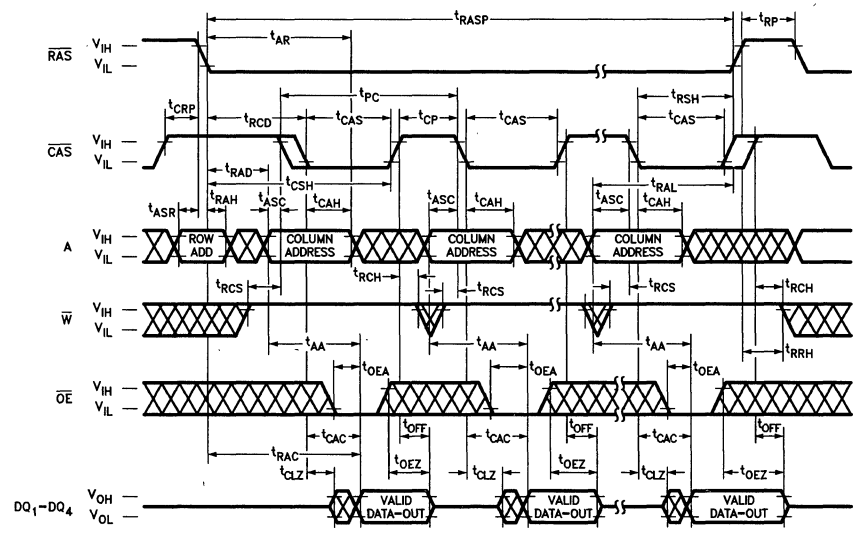
240022-9

DON'T CARE

240022-6

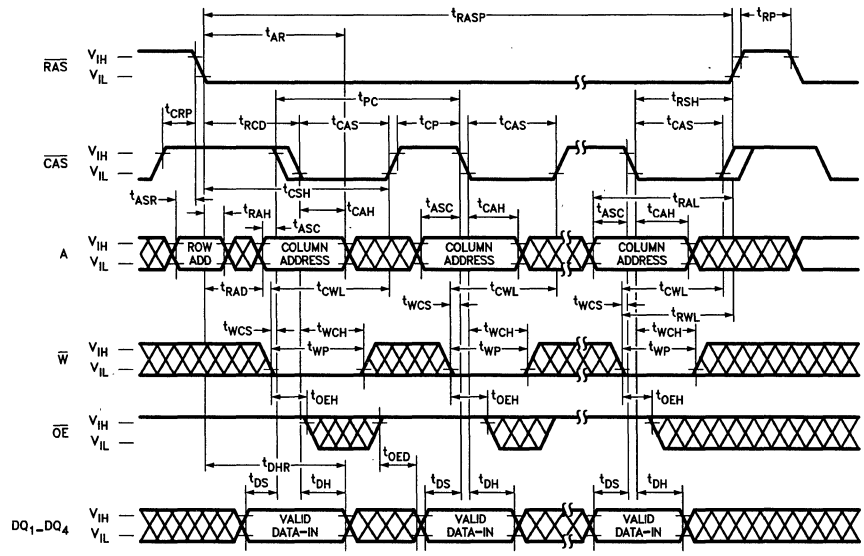
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



240022-10

PAGE MODE WRITE CYCLE



240022-11

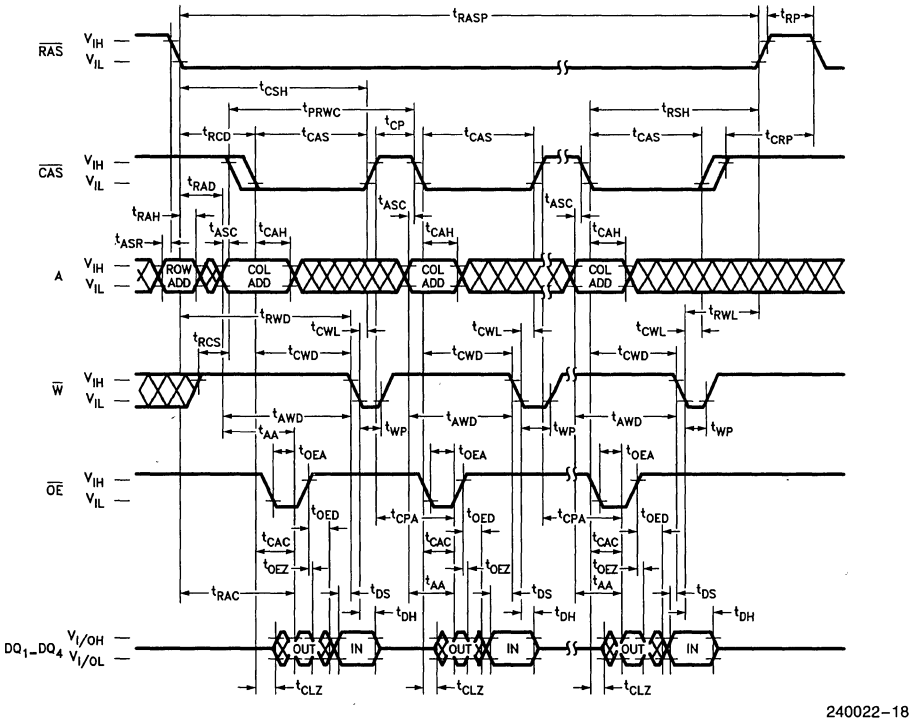
NOTE:
$\overline{OE}$ = Don't Care

DON'T CARE

240022-6

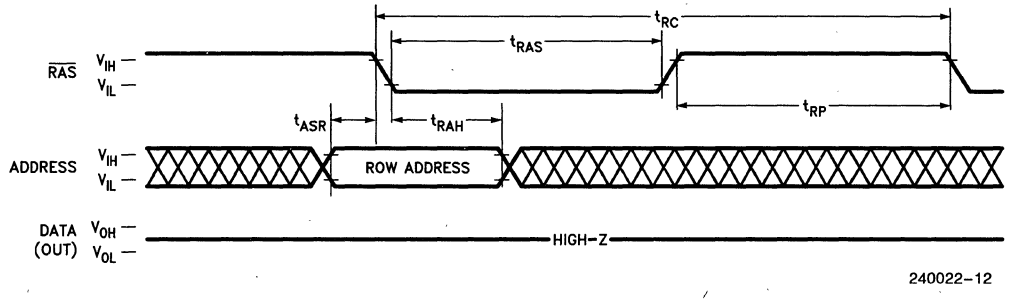
TIMING DIAGRAMS (Continued)

PAGE MODE READ-MODIFY-WRITE CYCLE



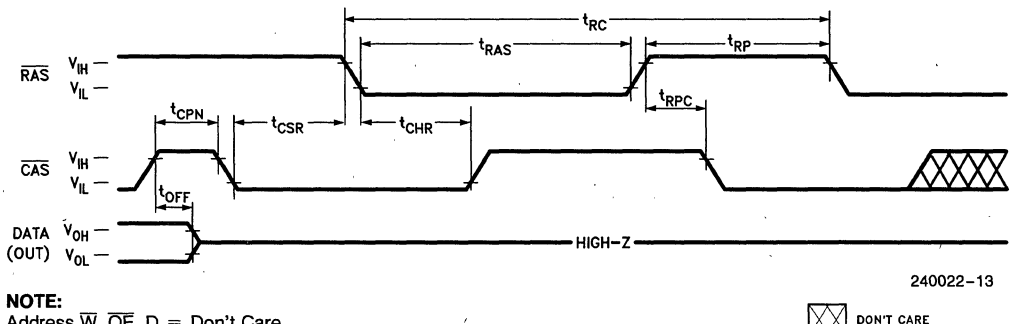
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE



NOTE:
$\overline{CAS}$ = V_{IH}; $\overline{W}$, $\overline{OE}$, D = Don't Care.

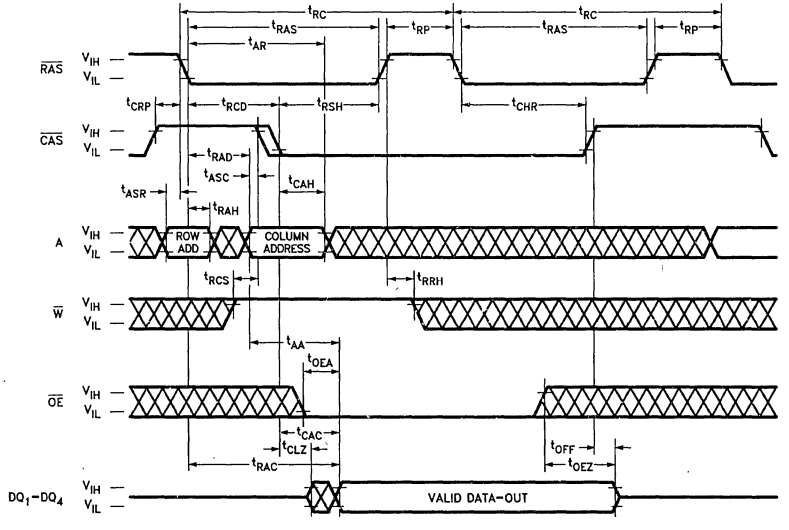
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE:
Address $\overline{W}$, $\overline{OE}$, D = Don't Care.

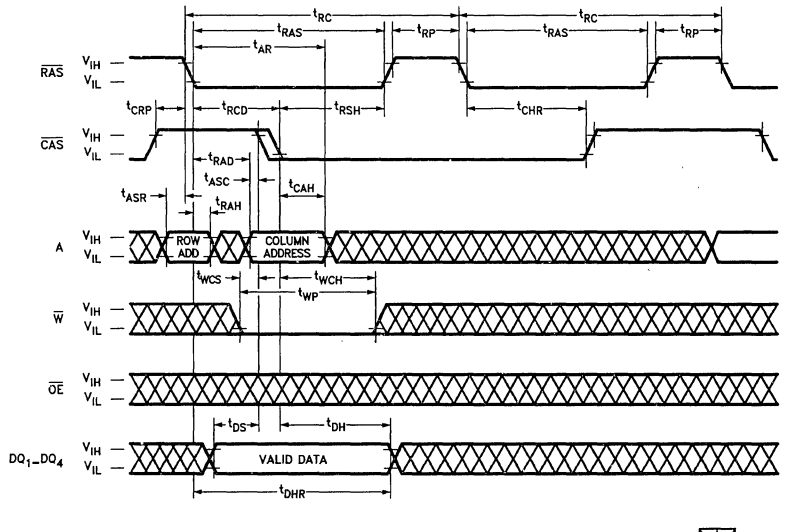
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



240022-6

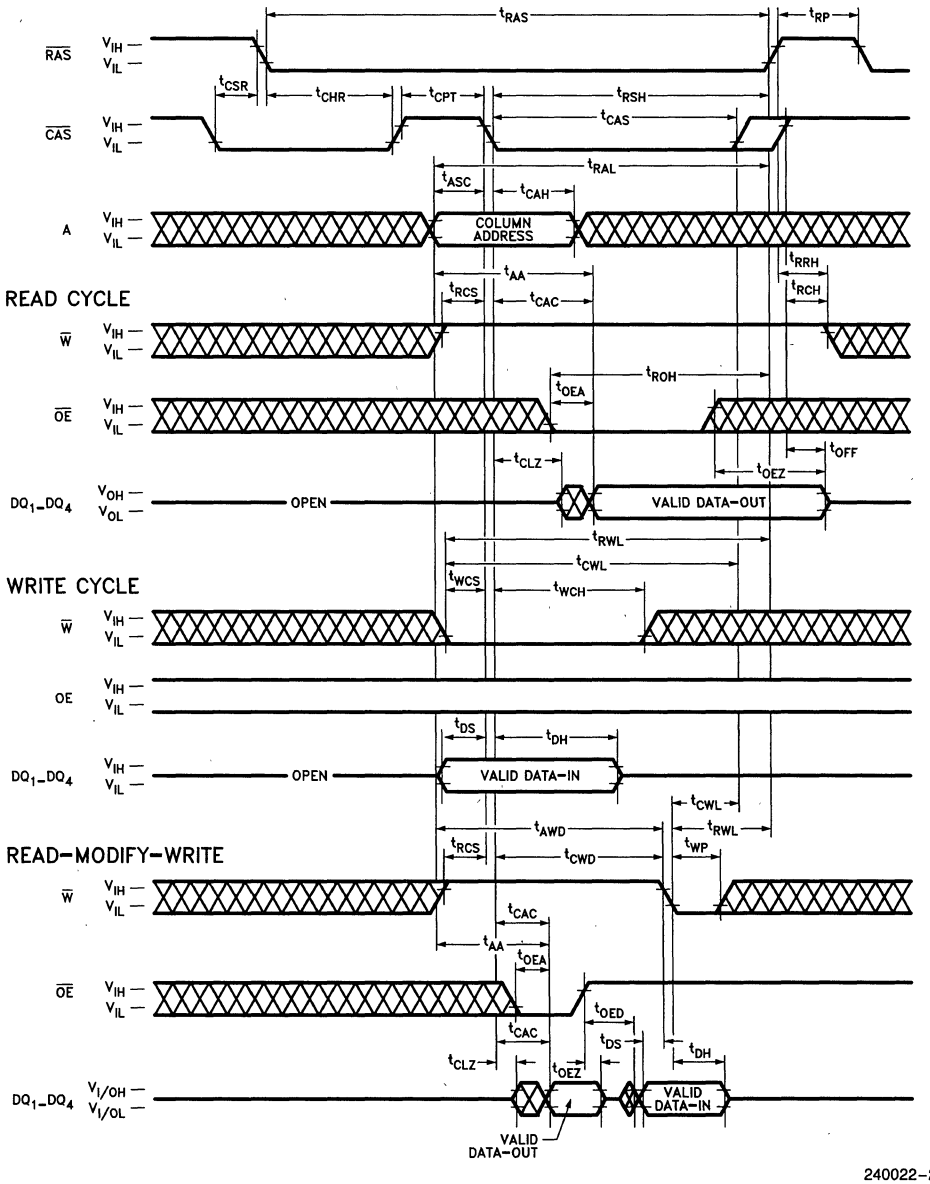
HIDDEN REFRESH CYCLE (WRITE)



240022-6

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

The 21464 contains 262,144 memory locations organized as 65,536 4-bit words. Sixteen address bits are required to address a particular 4-bit word in the memory array. Since the 21464 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), and the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21464 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21464 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enought to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21464 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The four outputs of the 21464 remain in the Hi-Z state until valid data appears at the outputs. The 21464 has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 21464 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the 21464 DQ pins.

Data Output

The 21464 has tri-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs first remain in the Hi-Z state until the data is valid and then the valid data appears at the outputs. The valid data remains at the outputs until either $\overline{CAS}$ or $\overline{OE}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21464 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode, Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-Only Refresh, Page Mode Write, $\overline{CAS}$-Only Cycle.

Indeterminate Output State; Delayed Write (t_{CWD} or t_{RWD} are not met).

Refresh

The data in the 21464 is stored on a tiny capacitor within each memory cell. Due to leakage the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This must be performed on each of the 256 row addresses (A_0–A_7) every 4 ms.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The 21464 has $\overline{CAS}$-Before-$\overline{RAS}$ refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set-up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-Before-$\overline{RAS}$ refresh Cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the lastest valid data at the outputs by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21464 hidden refresh cycle is actually a $\overline{CAS}$-Before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-Before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the 21464 by using read, write or read-modify-write cycles. Whenever a row is accessed all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-Before-$\overline{RAS}$ refresh are the preferred methods.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21464 might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{AS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initializations cycles are also required after an 4 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21464 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21464 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all the DRAMs run both horizontally and vertically and are connected at each intersection, or better yet, if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on the memory boards to facilitate

the shortest possible address and control lines to all the DRAMs.

Decoupling

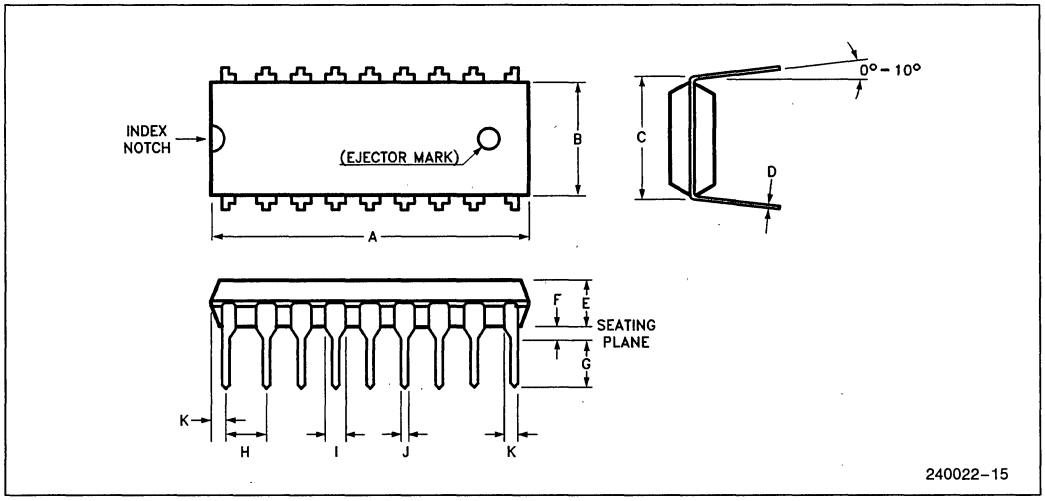
The importance of proper decoupling cannot be overemphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21464 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21464 and they supply much of the current used by the 21464 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor shuld be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

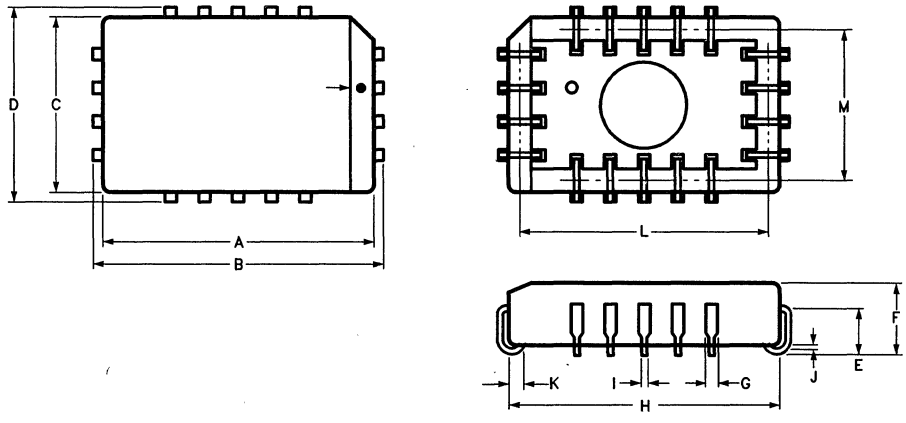
18-LEAD PLASTIC DUAL IN-LINE PACKAGE



Item	Millimeters	Inches
A	22.950 ± 0.05	0.903 ± 0.002
B	6.40 ± 0.05	0.252 ± 0.002
C	7.62	0.300
D	0.025 ± 0.025	0.010 ± 0.001
E	3.25 ± 0.05	0.128 ± 0.002
F	0.506 ± 0.1	0.020 ± 0.004
G	3.302 ± 0.1	0.130 ± 0.004
H	2.54	0.100
I	1.27 ± 0.05	0.050 ± 0.002
J	0.457 ± 0.05	0.018 ± 0.002
K	1.32	0.052

PACKAGE DIMENSIONS (Continued)

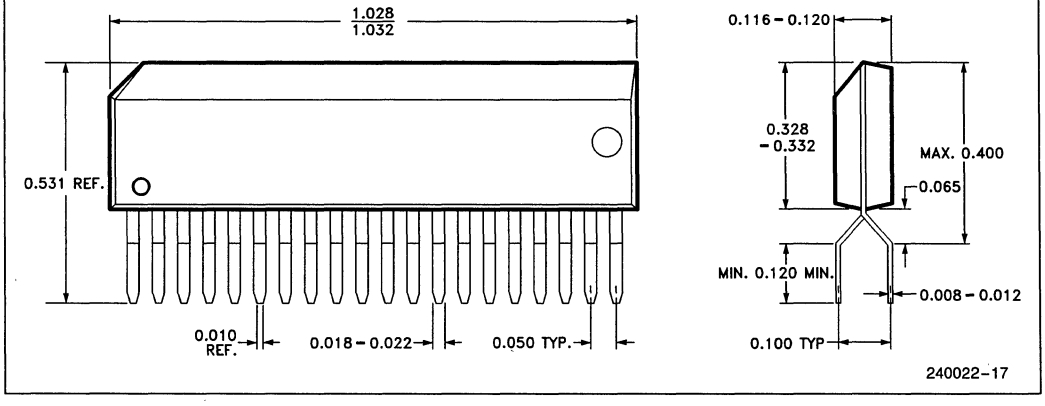
18-PIN PLASTIC LEADED CHIP CARRIER



Item	Millimeters	Inches
A	12.346 ± 0.052	0.490 ± 0.002
B	13.2585 ± 0.0505	0.522 ± 0.002
C	7.366 ± 0.051	0.290 ± 0.002
D	8.179 ± 0.051	0.322 ± 0.002
E	2.083 ± 0.051	0.082 ± 0.002
F	3.505 ± 0.051	0.138 ± 0.002
G	0.7365 ± 0.0505	0.029 ± 0.002

Item	Millimeters	Inches
H	6.553 ± 0.051	0.258 ± 0.002
I	**0.43 type**	**0.017 typ**
J	0.279 ± 0.025	0.011 ± 0.001
K	**0.76 typ**	**0.030 typ**
L	11.8365 ± 0.0505	0.466 ± 0.002
M	6.756 ± 0.051	0.266 ± 0.002

20-LEAD ZIG-ZAG INLINE PACKAGE (ZIP)



21010
1,048,576 x 1-Bit Dynamic RAM with Page Mode

Performance Range

	t_{RAC}	t_{CAC}	t_{RC}
21010-06	60 ns	20 ns	110 ns
21010-07	70 ns	20 ns	130 ns
21010-08	80 ns	20 ns	160 ns
21010-10	100 ns	25 ns	190 ns

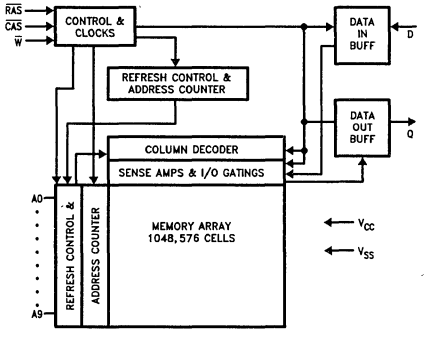
- **Fast Page Mode Operation**
- **$\overline{CAS}$ before $\overline{RAS}$ Refresh Capability**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **512 Cycles/8 ms refresh**
- **Available in Plastic DIP, SOJ and ZIP Packages**

Intel 21010 is a CMOS high speed 1,048,576 x 1 dynamic RAM optimized for high performance applications such as mainframes, graphics and microprocessor systems.

21010 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$ before $\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$ only refresh. All Inputs, Output and Clocks are fully CMOS and TTL compatible.

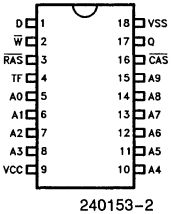
Functional Block Diagram



240153-1

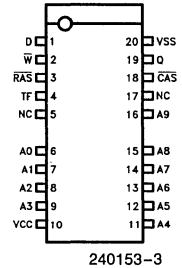
PIN CONFIGURATION

DIP



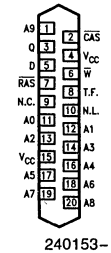
240153-2

SOJ



240153-3

ZIP



240153-16

NOTE:
T.F. = Test Function, Ground or No Connect

Pin Names

A_0–A_9	Address Inputs
$\overline{W}$	Read/Write Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D	Data In
Q	Data Out
V_{SS}	Ground
V_{CC}	Power +5V

August 1990
Order Number: 240153-005

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V
Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V
Storage Temperature (T_{stg}) ..... −55°C to +150°C
Power Dissipation (P_d) ..... 600 mW
Short Circuit Output Current (I_{OS}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

(Voltage Referenced to V_{SS}. T_A = 0°C to +70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0		0.8	V

NOTES:
1. V_{IL} (Min) = −1.0V for continuous DC level.
2. V_{IL} (Min) = −2.0V for pulse width < 20 ns.

Capacitance (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_{in1}	Input Capacitance (A_0–A_9, D)		6	pF
C_{in2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)		7	pF
C_{out}	Output Capacitance (Q)		7	pF

D.C. AND OPERATING CHARACTERISTICS

(Recommended Operating Conditions unless Otherwise Noted)

Symbol	Parameter	Speed	Min	Max	Units
I_{CC1}	Operating Current	-06		90	mA
I_{CC1}	($\overline{RAS}$ and $\overline{CAS}$ Cycling	-07		80	mA
	@ t_{RC} = Min	-08		70	mA
		-10		60	mA
I_{CC2}	Standby Current	-06		2	mA
	(TTL Power Supply Current)				
I_{CC3}	$\overline{RAS}$ Only Refresh Current	-06		90	mA
I_{CC3}	($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling	-07		80	mA
	@ t_{RC} = Min	-08		70	mA
		-10		60	mA
I_{CC4}	Fast Page Mode Current	-06		70	mA
I_{CC4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling	-07		60	mA
	@ t_{PC} = Min	-08		50	mA
		-10		40	mA

D.C. AND OPERATING CHARACTERISTICS (Continued)

(Recommended Operating Conditions unless Otherwise Noted)

Symbol	Parameter	Speed	Min	Max	Units
I_{CC5}	Standby Current (CMOS Power Supply Current)			1	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (RAS and CAS Cycling @ t_{RC} = Min	-06 -07 -08 -10		90 80 70 60	mA mA mA mA
I_{IL}	Input Leakage Current (Any Input $0 < V_{IN} < 6.5V$ All Other Pins = 0V)		−10	10	μA
I_{OL}	Output Leakage Current (Data Out is Disabled and $0 < V_{OUT} < 5.5V$)		−10	10	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)		2.4		V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0.4	V

NOTE:
ICC1, ICC3, ICC4, and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

A.C. CHARACTERISTICS (See Notes 1, 2)

(T_A = 0°C to +70°C, V_{CC} = 5V + 10%)

Symbol	Parameter	21010-06		21010-07		21010-08		21010-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{REF}	Time between Refresh		8		8		8		8	ms	
t_{RC}	Random R/W Cycle Time	110		130		160		190		ns	
t_{RWC}	RMW Cycle Time	135		155		185		220		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	(Notes 4, 7)
t_{CAC}	Access Time from $\overline{CAS}$		20		20		20		25	ns	(Notes 5, 7)
t_{AA}	Access Time from Column Address		30		35		40		50	ns	(Notes 6, 7)
t_{CLZ}	$\overline{CAS}$ to Output in Low Z	0		0		0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay Time	0	20	0	20	0	20	0	20	ns	
t_T	Transition Time	3	50	3	50	3	50	3	50	ns	

A.C. CHARACTERISTICS (See Notes 1, 2)

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%) (Continued)

Symbol	Parameter	21010-06		21010-07		21010-08		21010-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RP}	$\overline{RAS}$ Precharge Time	40		50		70		80		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20		20		25		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	25	60	25	75	ns	(Notes 9, 10)
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		15		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		20		20		ns	
t_{AR}	Column Address Time Referenced to $\overline{RAS}$	50		55		65		75		ns	
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	20	40	20	50	ns	(Note 11)
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns	
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	(Note 12)
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	(Note 12)
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns	(Note 13)
t_{WCH}	Write Command Hold Time	15		15		20		20		ns	

A.C. CHARACTERISTICS (See Notes 1, 2)

(T_A = 0°C to +70°C, V_{CC} = 5V + 10%) (Continued)

Symbol	Parameter	21010-06		21010-07		21010-08		21010-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WCR}	Write Command Referenced to $\overline{RAS}$	50		55			60		75	ns	
t_{WP}	$\overline{WE}$ Pulse Width	15		15		15		20		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		25		ns	
t_{DS}	D_{IN} Set-Up Time	0		0		0		0		ns	
t_{DH}	D_{IN} Hold Time	15		15		20		20		ns	
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50		55		60		75		ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60		70		80		100		ns	(Note 13)
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20		20		20		25		ns	(Note 13)
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30		35		40		50		ns	
t_{RPC}	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	10		10		10		10		ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		20		30		30		ns	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time	30		35		40		50		ns	

3

A.C. CHARACTERISTICS (See Notes 1, 2)

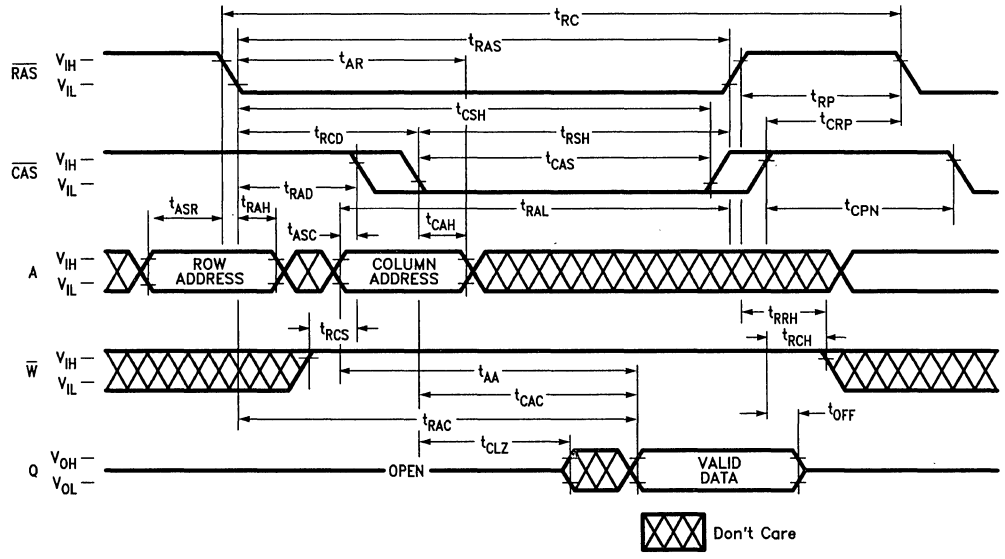
(T_A = 0°C to +70°C, V_{CC} = 5V + 10%) (Continued)

Symbol	Parameter	21010-06		21010-07		21010-08		21010-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
FAST PAGE MODE											
t_{PC}	Fast Page Mode Cycle Time	45		45		50		60		ns	
t_{PRWC}	Fast Page Mode RMW Cycle Time	70		70		75		90		ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		40		45		55	ns	(Notes 7, 14)
t_{CP}	Fast Page Mode CAS Precharge Time	10		10		10		10		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	100	100K	ns	

NOTES:

1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. characteristics assume t_T = 5 ns.
3. V_{IN} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing CAS from "L" to "H").

Read Cycle



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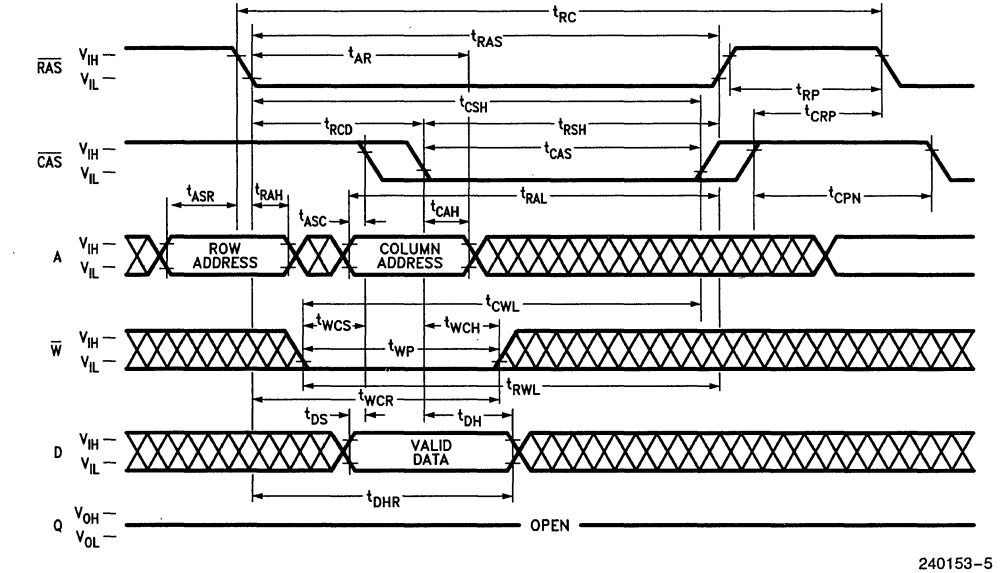
Write Cycle (Early Write)



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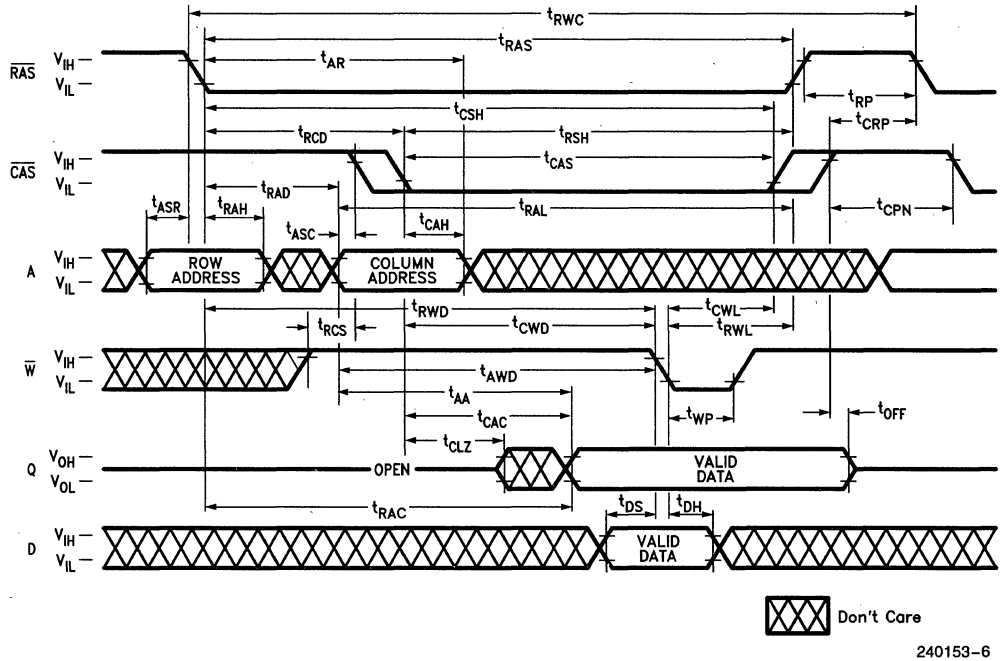
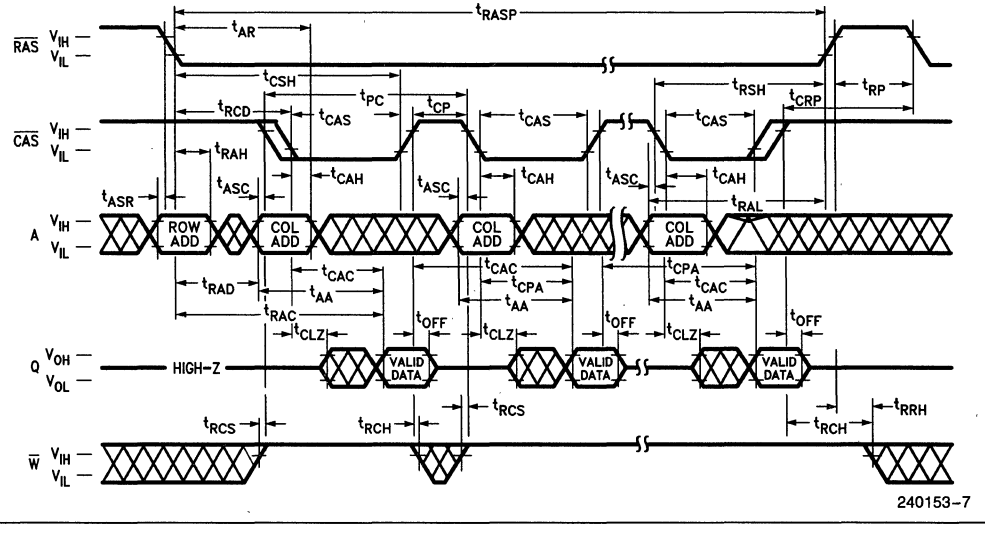
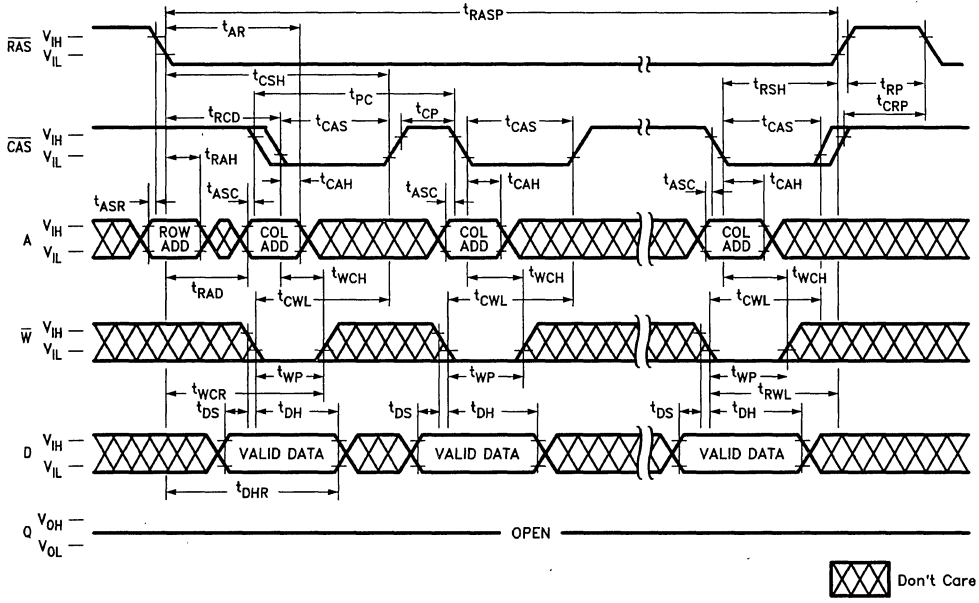
Read-Write/Read-Modify-Write Cycle



Fast Page Mode Read Cycle



Fast Page Mode Write Cycle



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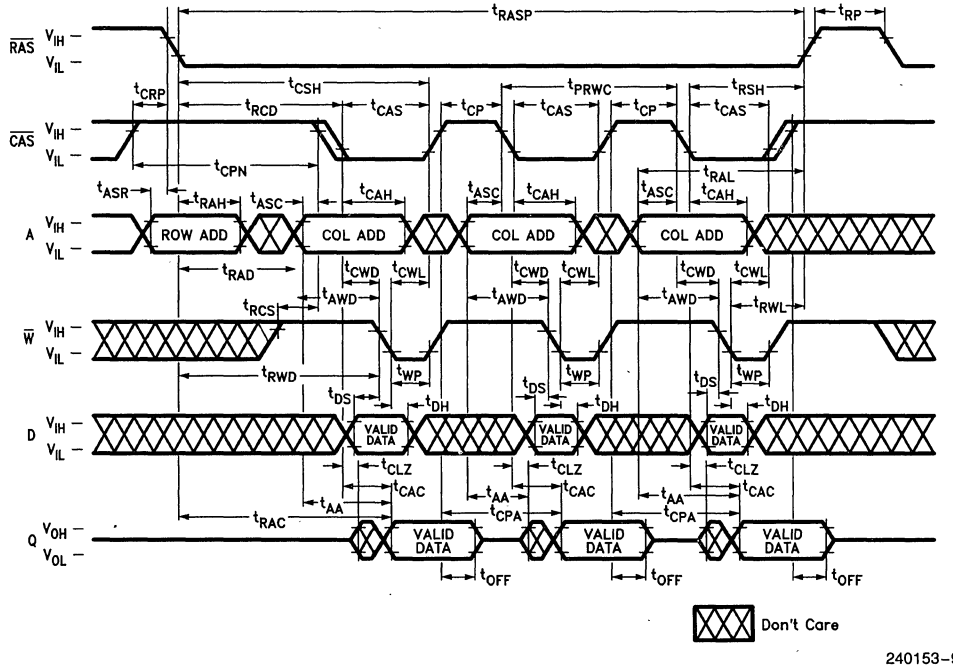
Fast Page Mode Read-Write Cycle



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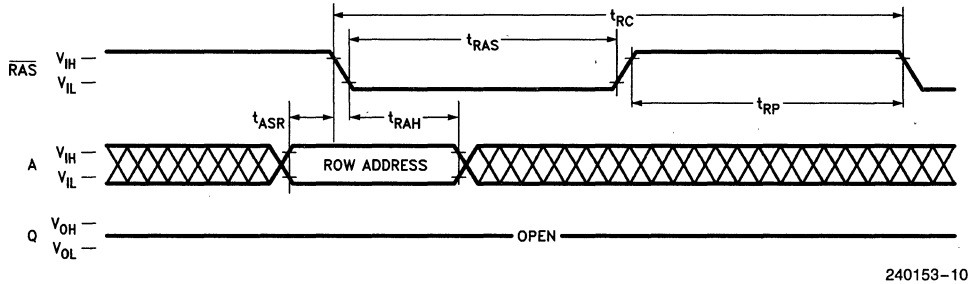
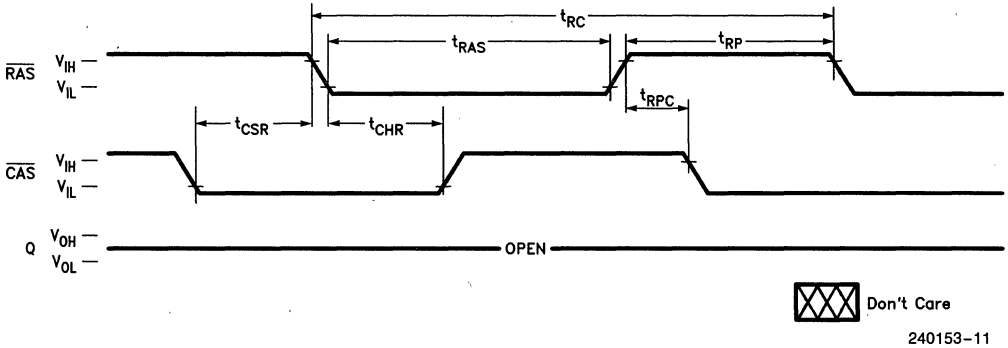
RAS-Only Refresh Cycle



240153-10

NOTE:
$\overline{WE}$, D_{IN} = Don't Care, A_g = V_{IH} or V_{IL}
$\overline{CAS}$ = V_{IH}, $\overline{W}$, D A_g = Don't Care

CAS-before-RAS Refresh Cycle



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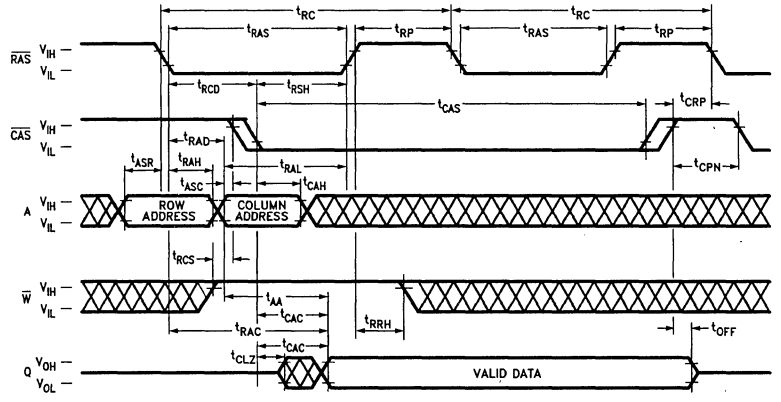
NOTE:
Address, $\overline{WE}$, D_{IN} = Don't Care

Hidden Refresh Cycle



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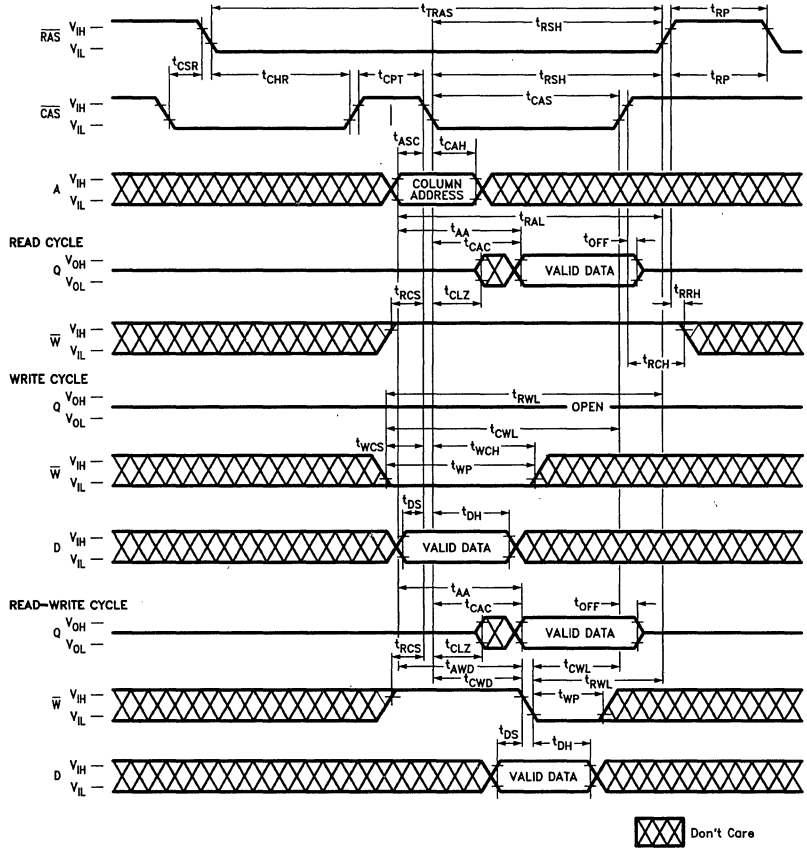
CAS-before-RAS Refresh Counter Test Cycle



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21010 OPERATION

Device Operation

The 21010 contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the 21010 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the 21010 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21010 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21010 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{CAS}$ goes low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAD(max)}$, the access time is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The 21010 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD}, and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21010 has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21010 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only Cycle.

Indeterminate Output State: Delayed Write.

Refresh

The data in the 21010 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity, it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0–A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21010 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter, which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21010 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the 21010 by using read, write, or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set high internally.

Fast Page Mode

The 21010 has Fast Page mode capability, which provides high speed read, write, or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

3

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21010 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μs is required after power-up, followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21010 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or

parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21010 input pin. The optimum value depends on the board layout. It must be determined experimentally and is ususally in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all the DRAMs run both horizontally and vertically and are connected at each intersection, or better yet, if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs, these lines should fan out from a central point like a fork or comb, rather than being connected in a serpentine pattern. Also, the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

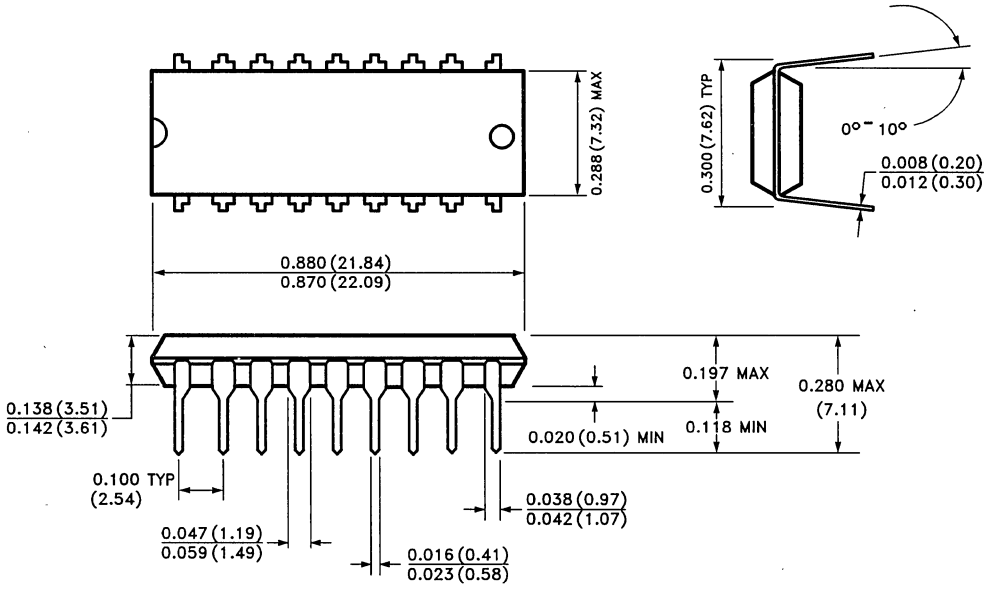
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21010 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21010, and they supply much of the current used by the 21010 during cycling.

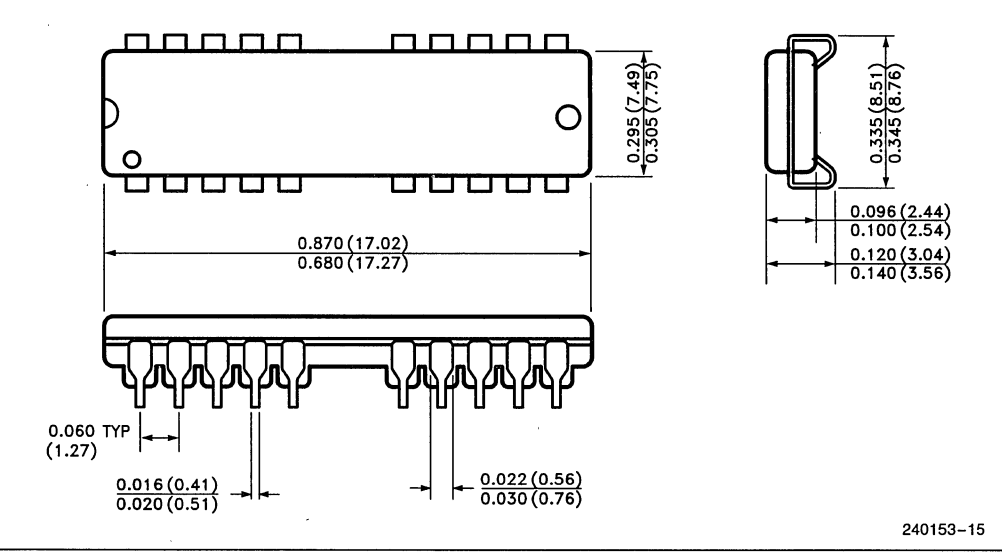
In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

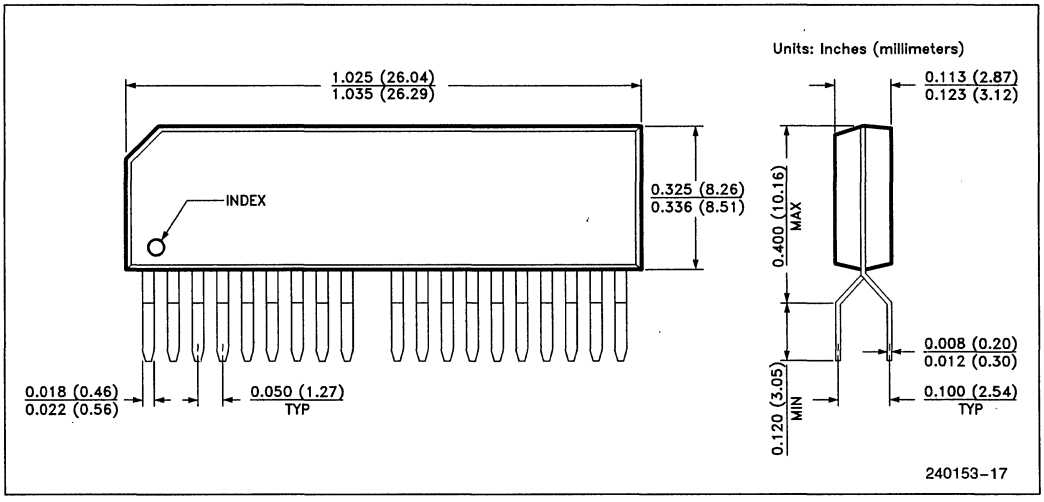


20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



21014
262,144 x 4-BIT DYNAMIC RAM WITH PAGE MODE

Performance Range:

	t_{RAC}	t_{CAC}	t_{RC}
21014-06	60 ns	15 ns	120 ns
21014-07	70 ns	20 ns	130 ns
21014-08	80 ns	20 ns	160 ns
21014-10	100 ns	25 ns	190 ns

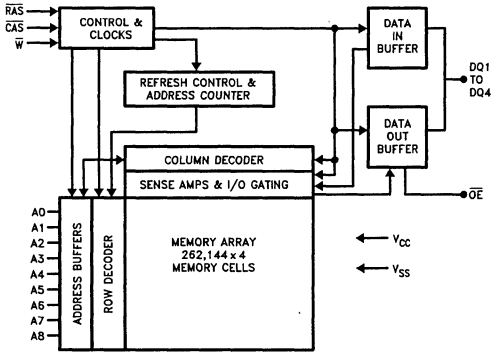
- **Fast Page Mode Operation**
- **$\overline{CAS}$ before $\overline{RAS}$ refresh capability**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **512 Cycles/8 ms Refresh**
- **Available in Plastic DIP, SOJ and ZIP Packages**

Intel 21014 is a CMOS high speed 262,144 x 4 dynamic RAM optimized for high performance applications such as mainframes, graphics and microprocessor systems.

21014 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$ before $\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$ only refresh. All Inputs, Outputs and Clocks are fully CMOS and TTL compatible.

Functional Block Diagram

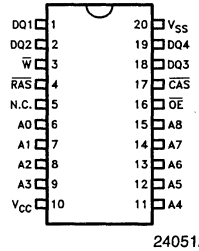


240512-1

Pin Name	Pin Function
A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1–DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

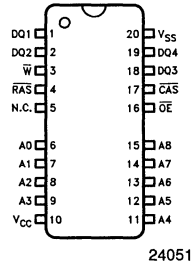
Pin Configurations

DIP



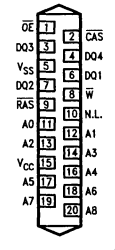
240512-2

SOJ



240512-3

ZIP



240512-4

August 1990
Order Number: 240512-003

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V
Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V
Storage Temperature (T_{stg}) ..... −55°C to +150°C
Power Dissipation (PD) ..... 600 mW
Short Circuit Output Current (I_{OS}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

NOTES:
1. V_{IL} (min) = 1.0V for continuous DC level.
2. V_{IL} (min) = 2.0V for pulse width < 20 ns.

CAPACITANCE T_A = 25°C

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (A_0–A_8)	—	6	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	—	7	pF
C_{OUT}	Output Capacitance (DQ_1–DQ_4)	—	7	pF

D.C. AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted

Symbol	Parameter	Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)	-06 -07 -08 -10	— — — —	90 80 70 60	mA mA mA mA
I_{CC2}	Standby Current (TTL Power Supply Current)		—	2	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = Min)	-06 -07 -08 -10	— — — —	90 80 70 60	mA mA mA mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @t_{PC} = Min)	-06 -07 -08 -10	— — — —	75 65 55 45	mA mA mA mA
I_{CC5}	Standby Current (CMOS Power Supply Current)		—	1	mA

D.C. AND OPERATING CHARACTERISTICS (Continued)

Recommended operating conditions unless otherwise noted

Symbol	Parameter	Speed	Min	Max	Units
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)	-06 -07 -08 -10	— — — —	90 80 70 60	mA mA mA mA
I_{IL}	Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$ All Other Pins = 0V)		−10	10	μA
I_{OL}	Output Leakage Current (Data Out is Disabled and $0 \leq V_{OUT} \leq 5.5V$)		−10	10	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)		2.4	—	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)		—	0.4	V

NOTE:
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

3

A.C. CHARACTERISTICS(1, 2)

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	21014-06		21014-07		21014-08		21014-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{REF}	Time between Refresh		8		8		8		8	ms	
t_{RC}	Random R/W Cycle Time	110		130		150		180		ns	
t_{RWC}	RMW Cycle Time	165		185		205		245		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	4, 7
t_{CAC}	Access Time from $\overline{CAS}$		20		20		20		25	ns	5, 7
t_{AA}	Access Time from Column Address		30		35		40		50	ns	6, 7
t_{CLZ}	$\overline{CAS}$ to Output in Low Z	0		0		0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay Time	0	20	0	20	0	20	0	20	ns	
t_T	Transition Time	3	50	3	50	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		70		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	25	60	25	75	ns	9, 10
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	

A.C. CHARACTERISTICS(1, 2) (Continued)

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	21014-06		21014-07		21014-08		21014-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		20		20		ns	
t_{AR}	Column Address Time Referenced to $\overline{RAS}$	50		55		65		75		ns	
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	20	40	20	50	ns	11
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns	
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	12
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	12
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns	13
t_{WCH}	Write Command Hold Time	15		15		15		20		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50		55		65		75		ns	
t_{WP}	$\overline{WE}$ Pulse Width	15		15		20		20		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		25		ns	
t_{DS}	D_{IN} Set-Up Time	0		0		0		0		ns	
t_{DH}	D_{IN} Hold Time	15		15		20		20		ns	
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50		55		65		75		ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80		100		110		135		ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40		50		50		60		ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50		65		70		85		ns	
t_{RPC}	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	10		10		10		10		ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	

A.C. CHARACTERISTICS(1, 2) (Continued)

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	21014-06		21014-07		21014-08		21014-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		20		25		30		ns	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time	30		35		40		50		ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		20		20		20		ns	
t_{OEA}	$\overline{OE}$ Access Time		15		20		20		25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15		20		20		25		ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	20	0	20	0	25	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	15		20		20		25		ns	

3

FAST PAGE MODE

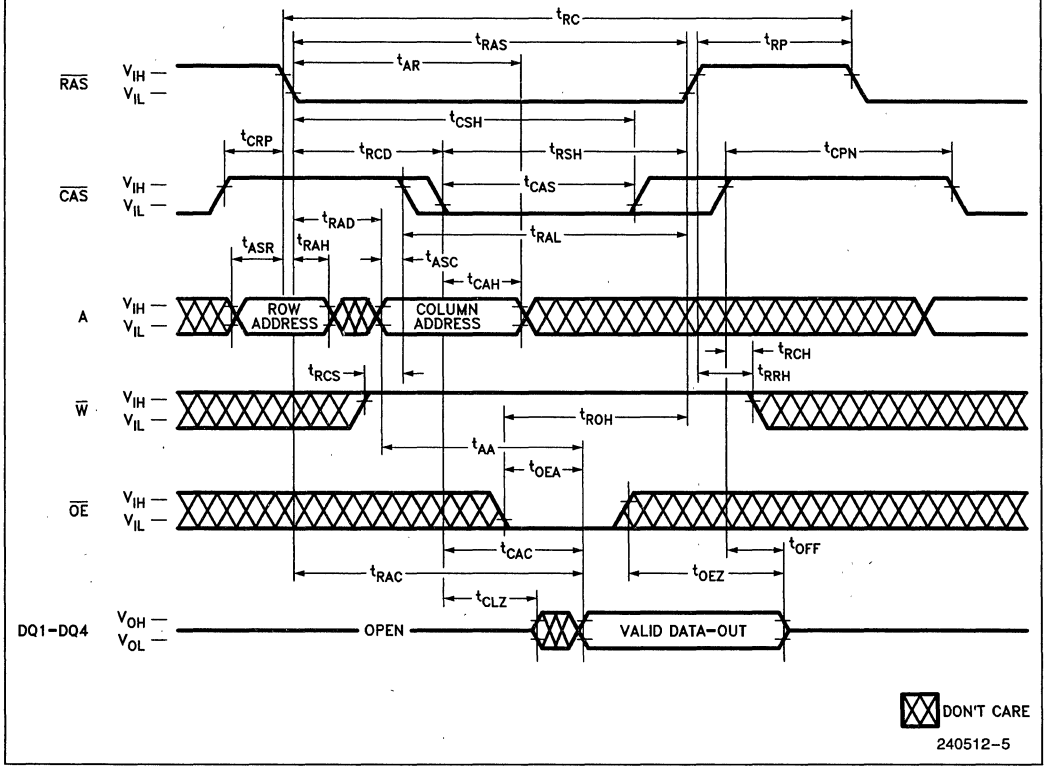
Symbol	Parameter	21014-06		21014-07		21014-08		21014-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45		45		50		60		ns	
t_{PRWC}	Fast Page Mode RMW Cycle Time	75		100		105		125		ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		45		55	ns	7, 14
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10		10		10		10		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	100	100K	ns	

NOTES:

1. An initial pause of 200 μs is required after power-up followed by any 8 RAS-only cycles before proper device operation is achieved.
2. A.C. characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are non restrictive operating parameters. They are included in the Data Sheet as Electrical characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing CAS from "L" to "H").

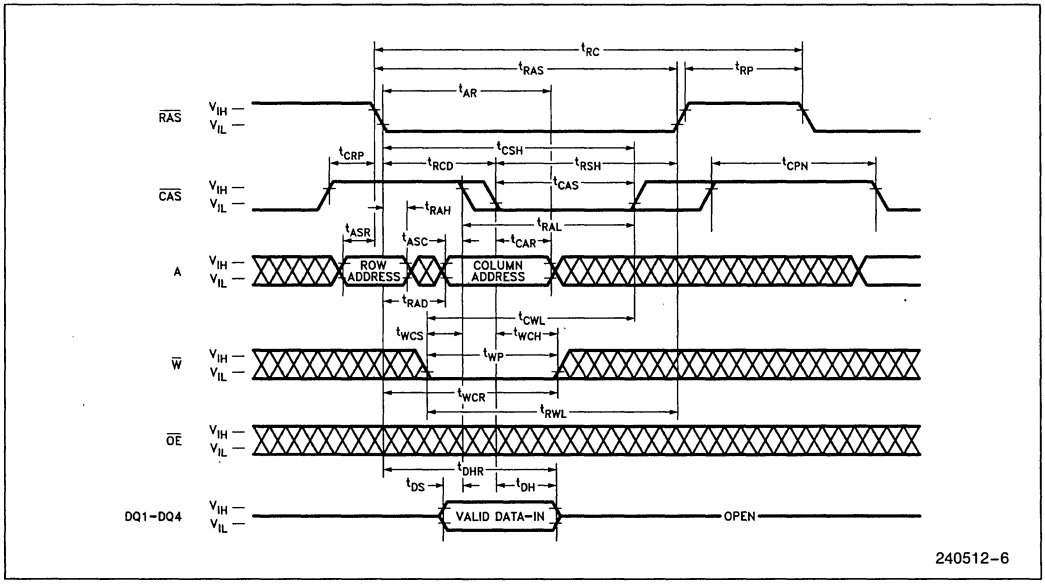
TIMING DIAGRAMS

READ CYCLE

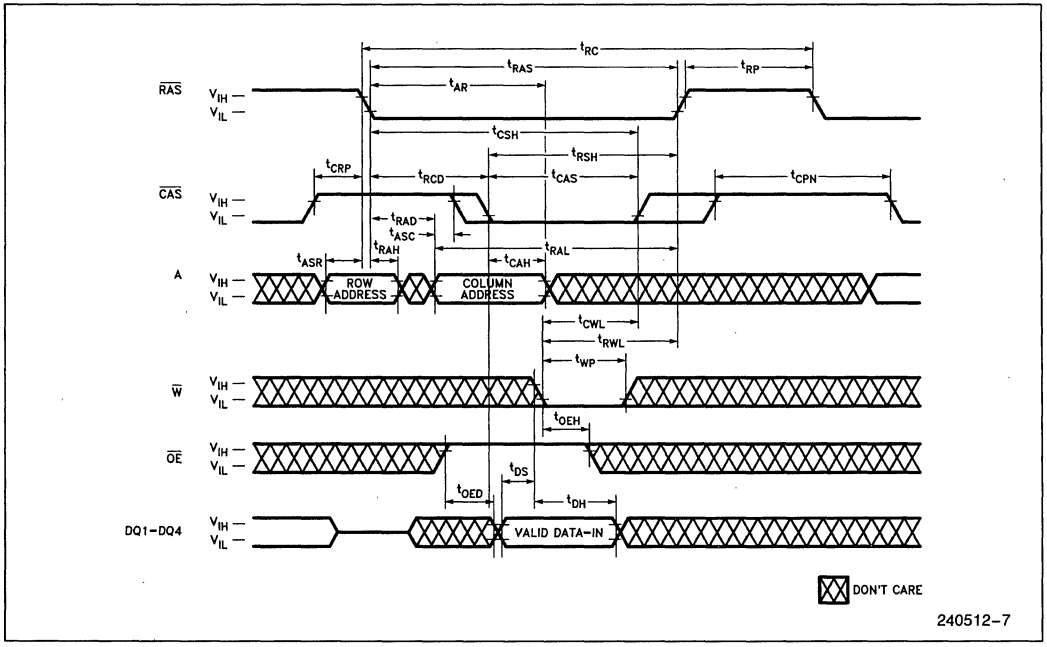


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

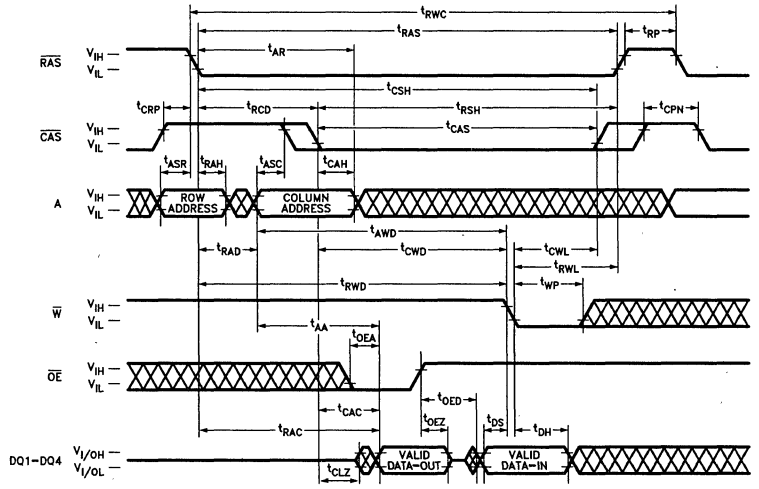


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE



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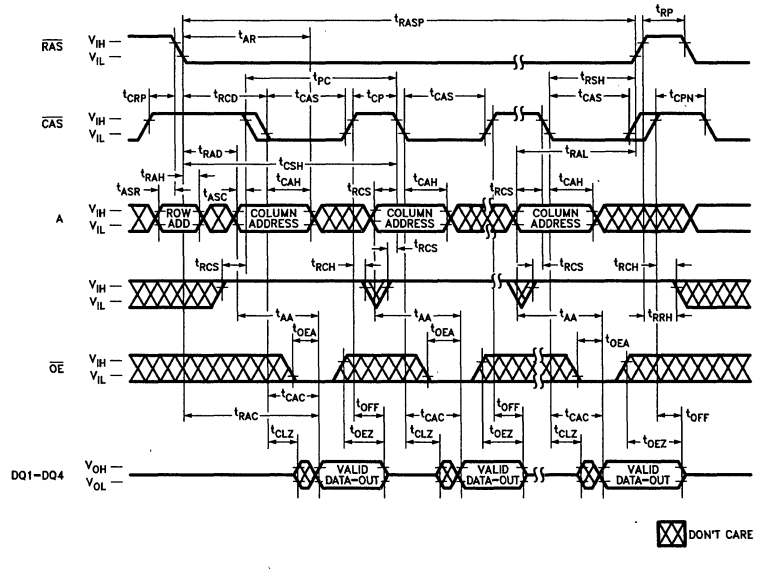
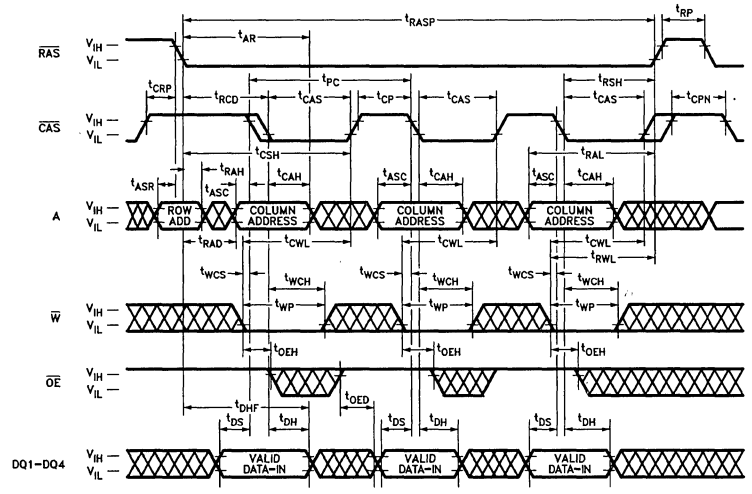
FAST PAGE MODE READ CYCLE



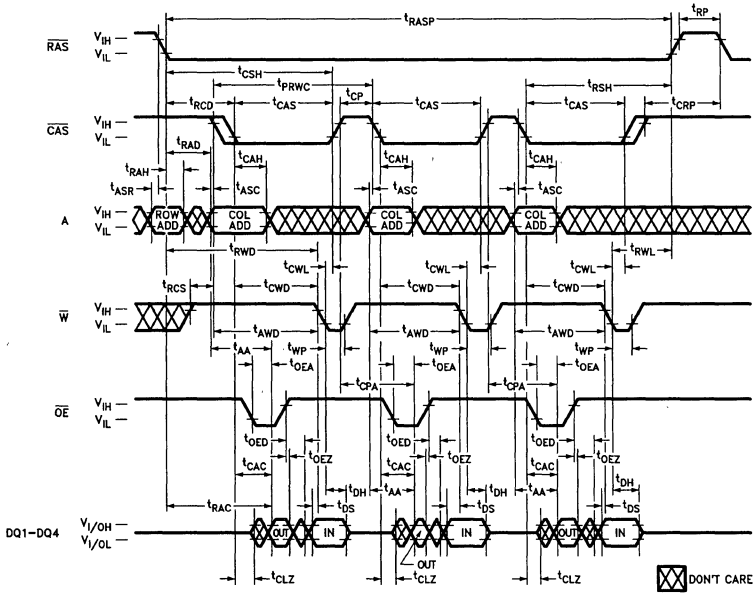
240512-9

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE



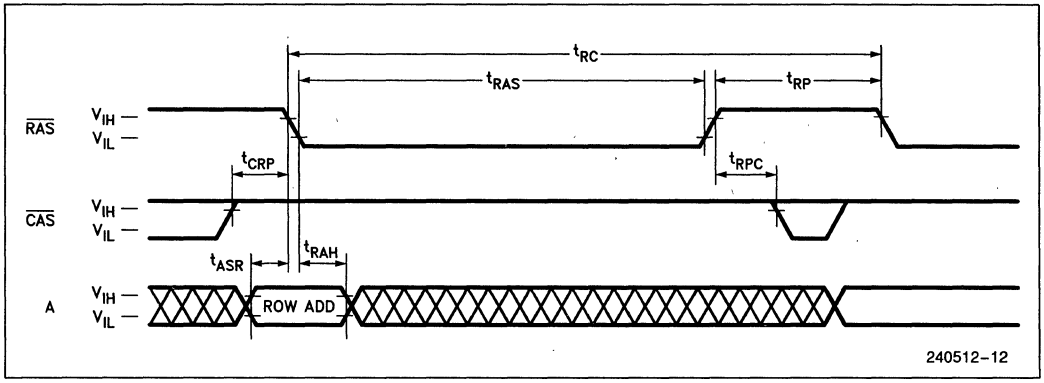
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

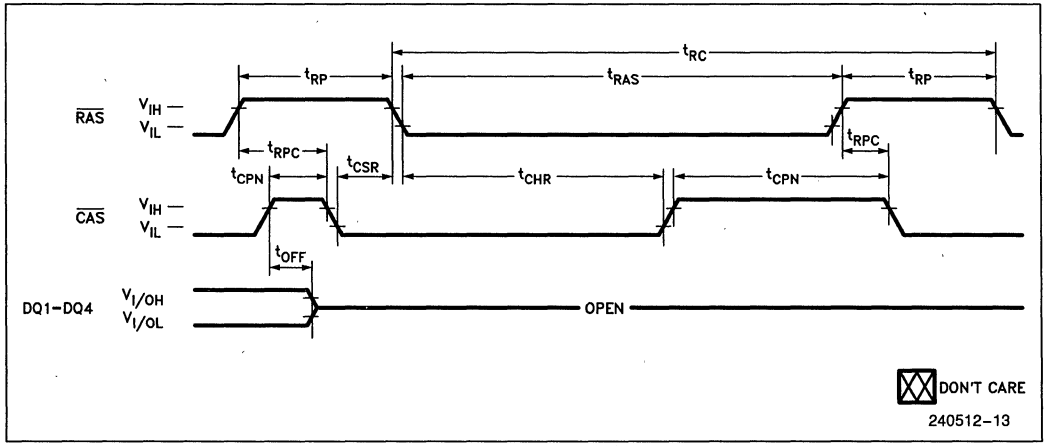
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



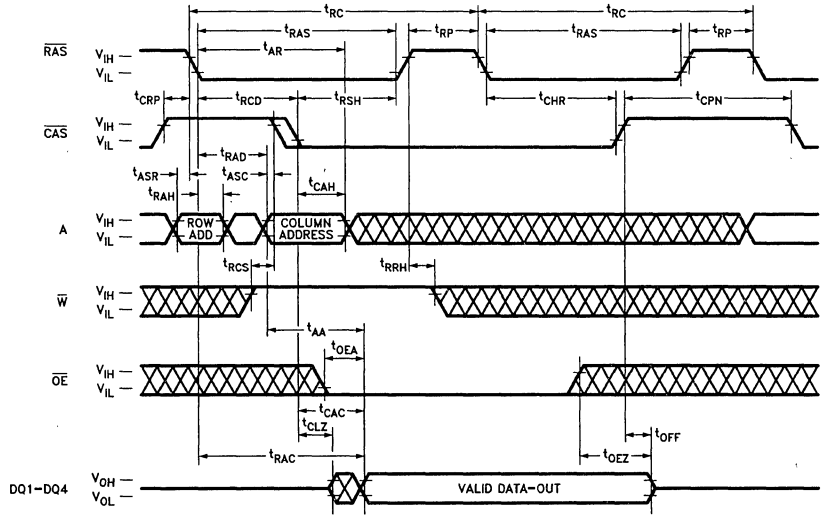
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$, A = Don't care



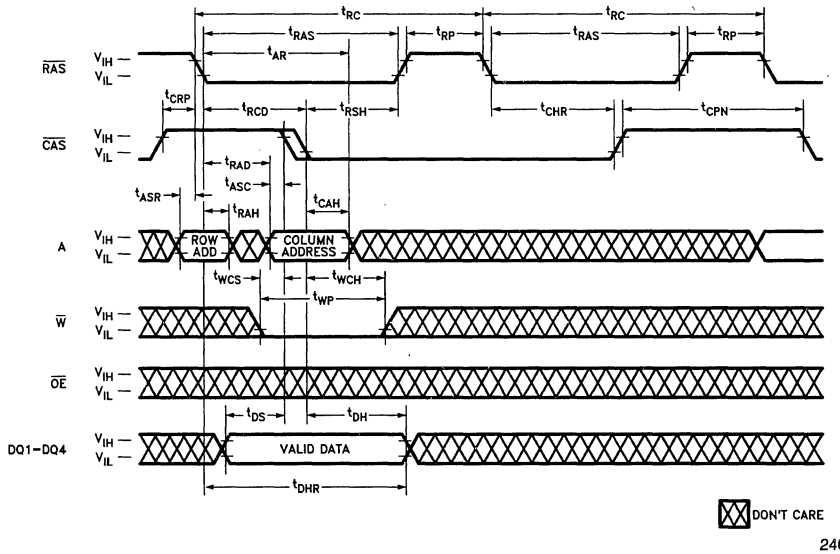
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



240512-14

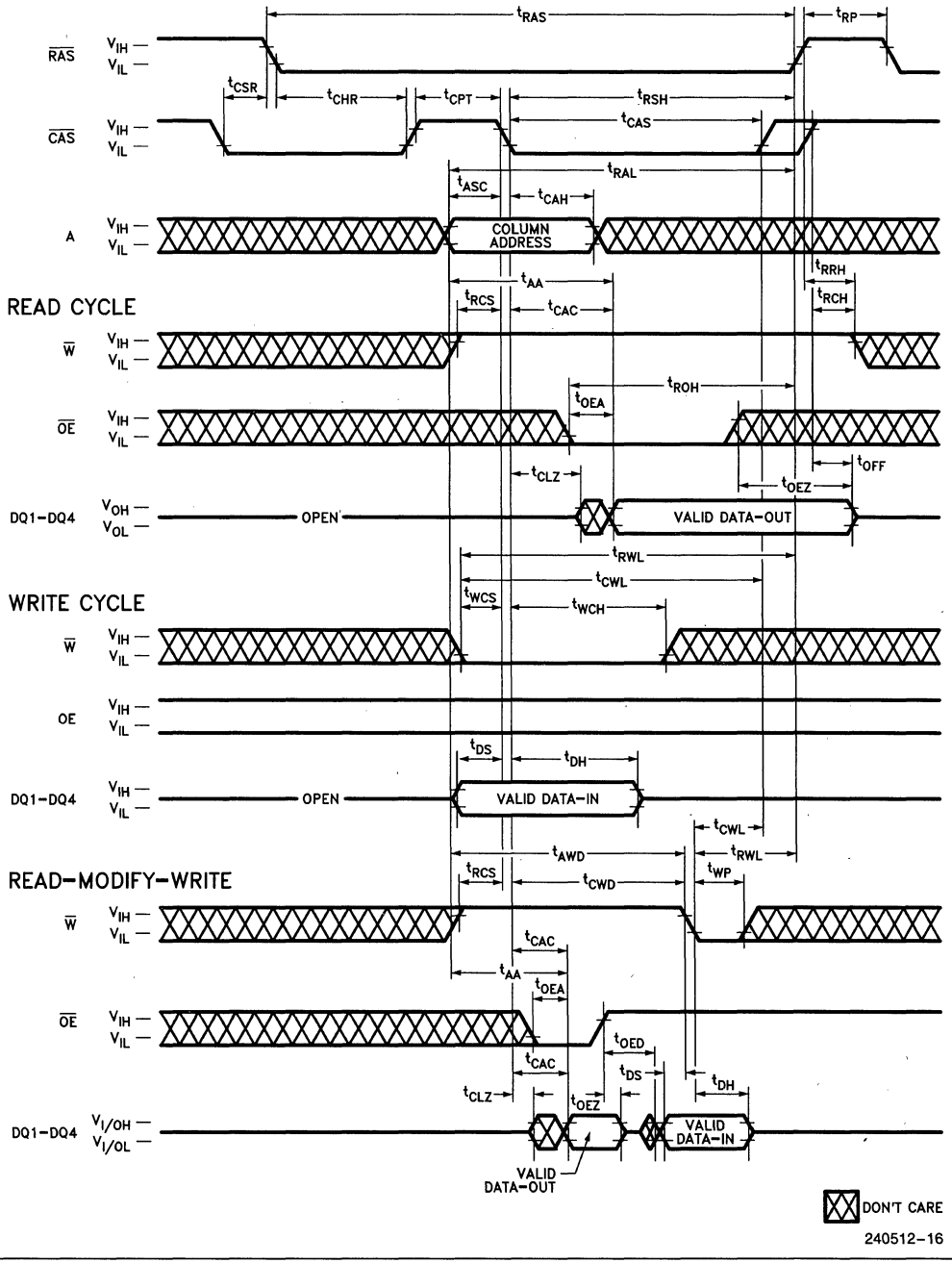
HIDDEN REFRESH CYCLE (WRITE)



240512-15

TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



21014 OPERATION

Device Operation

The 21014 contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the 21014 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21014 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21014 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21014 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD} (max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or if the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both t_{RCD} (max) and t_{RAD} (max).

The 21014 has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The 21014 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between W, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the 21014 DQ pins.

Data Output

The 21014 has tri-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21014 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met).

Refresh

The data in the 21014 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0–A_8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21014 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before RAS goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21014 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the 21014 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_8 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21014 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21014 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is

generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21014 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all the DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling can not be overemphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

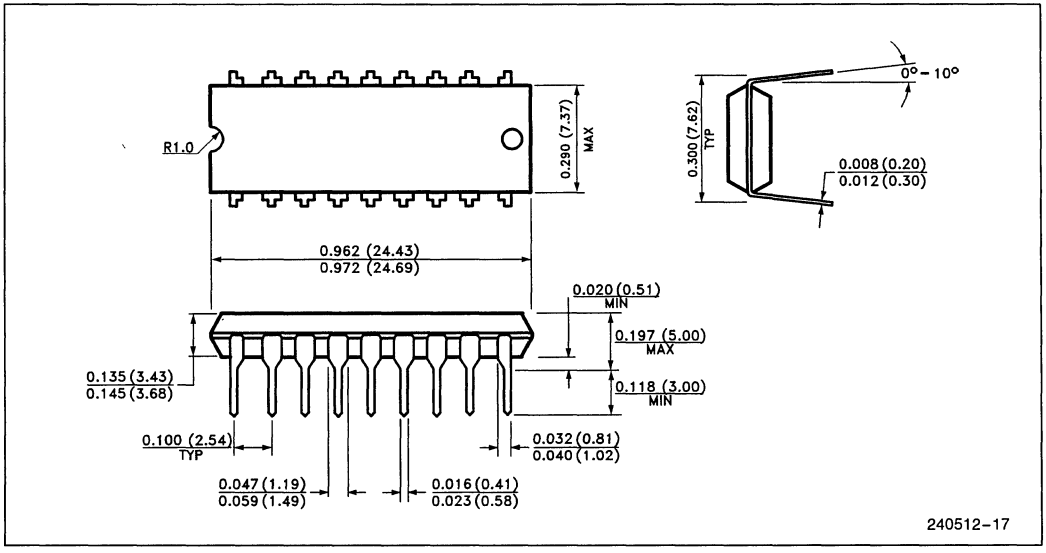
A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21014 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21014 and they supply much of the current used by the 21014 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

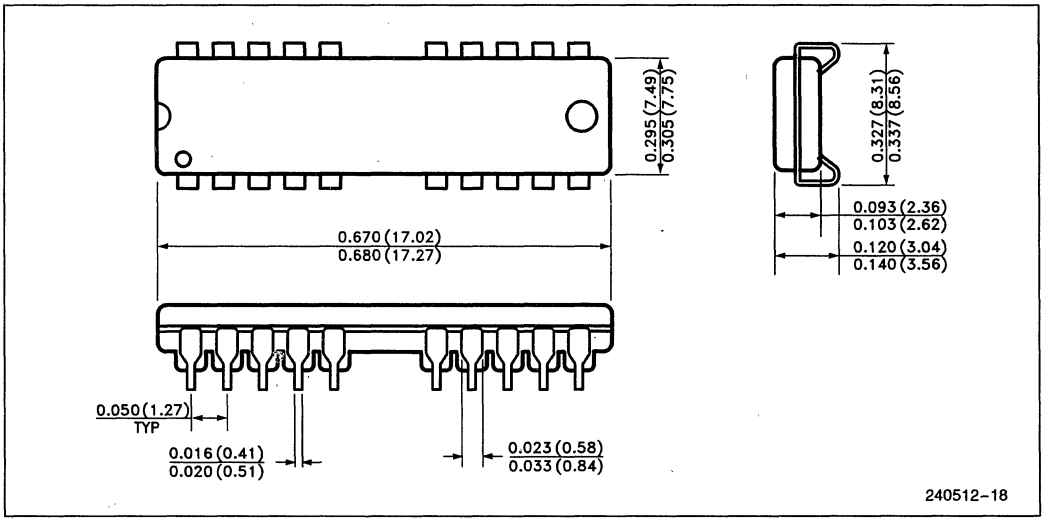
PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL-IN-LINE PACKAGE Units: Inches (millimeters)

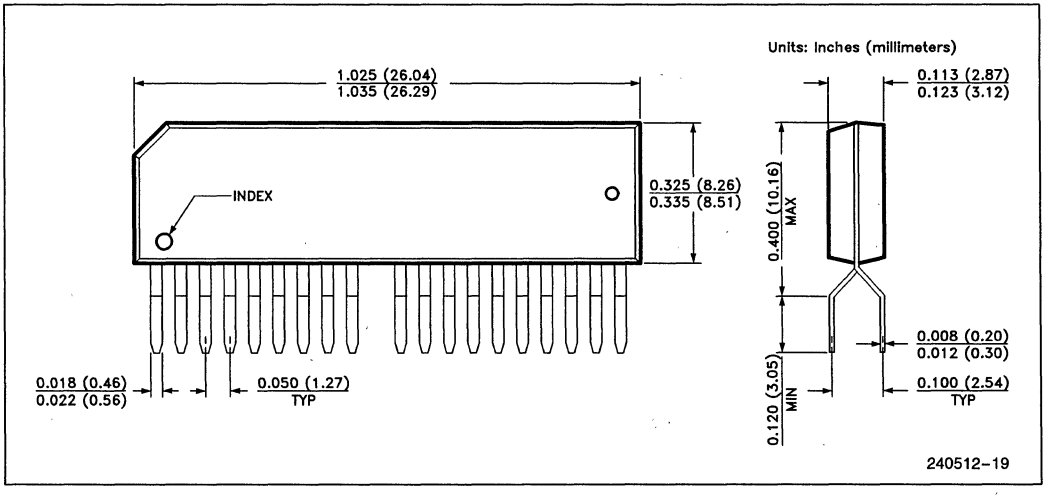


PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUTLINE J-LEAD Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



21040
4,194,304 x 1-BIT DYNAMIC RAM WITH PAGE MODE

- **Performance Range**

	21040-08	21040-10	21040-12	Units
tRAC	80	100	120	ns
tCAC	20	25	30	ns
tRC	160	190	220	ns

- **Fast Page Mode Operation**
- **Common I/O Using "Early Write" Operation**
- **1024 Cycles/16mS Refresh**
- **$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only Refresh, Hidden Refresh and Test Mode Capability**
- **Single 5V ± 10% Power Supply**
- **Available in Plastic SOJ and ZIP package types**

GENERAL INFORMATION

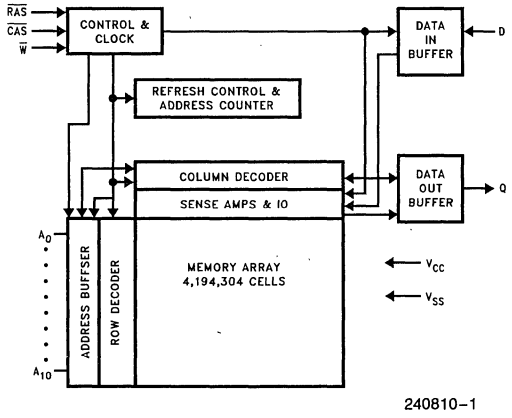
Intel 21040 is a CMOS high speed 4,194,304 × 1-bit dynamic RAM optimized for high performance applications such as mainframes, graphics and microprocessor systems.

21040 features Fast Page Mode operation which allow high speed random access of memory cells within the same row.

$\overline{CAS}$ before $\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$ only refresh. All Inputs, Output and clocks are fully CMOS and TTL compatible.

Multiplexed address inputs permit the 21040 device to be packaged in a standard 20/26 pin plastic SOJ and 20 pin plastic ZIP.

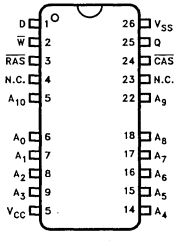
Functional Block Diagram



240810-1

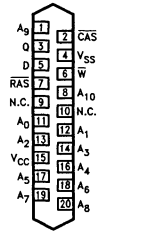
Pin Configuration

Plastic SOJ T21040



240810-2

Plastic ZIP Z21040



240810-3

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

September 1990
Order Number: 240810-001

ABSOLUTE MAXIMUM RATINGS*

SYMBOL	PARAMETER	VALUE	UNITS
V_{in}, V_{out}	Voltage on any pin relative to V_{SS}	−1 to +7.0	V
V_{CC}	Voltage on power supply relative to V_{SS}	−1 to +7.0	V
Tstg	Storage Temperature	−55 to +150	°C
Topr	Operating Temperature	0 to 70	°C
Pd	Power Dissipation	600	mW
Ios	Short Circuit Output Current	50	mA

*Permanent damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as defined in the operational sections of the Data Sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0°C to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.4	–	6.5	V
VIL	Input Low Voltage	−-1.0	–	0.8	V

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
Cin1	Input Capacitance (A0 – A10, Din)	–	5	pF
Cin2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
Cout	Output Capacitance (Dout)	–	7	pF

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

SYMBOL	PARAMETER	SPEED	MIN	MAX	UNIT
ICC1	Operating Current*	−08	–	100	mA
	($\overline{RAS}$ and $\overline{CAS}$ cycling @ ^tRC = min)	−10	–	85	mA
		−12	–	70	mA
ICC2	Standby Current				
	(TTL Power Supply Current)		–	2	mA
ICC3	RAS Only Refresh Current*	−08	–	100	mA
	($\overline{CAS}$ = VIH, $\overline{RAS}$ Cycling @ ^tRC = min)	−10	–	85	mA
		−12	–	70	mA
ICC4	Fast Page Mode Current*	−08	–	60	mA
	($\overline{RAS}$ = VIL, $\overline{CAS}$ Cycling @ ^tPC = min)	−10	–	50	mA
		−12	–	40	mA
ICC5	Standby Current				
	(CMOS Power Supply Current)		–	1	mA
ICC6	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current*	−08	–	100	mA
	($\overline{RAS}$ and $\overline{CAS}$ Cycling @ ^tRC = min)	−10	–	85	mA
		−12	–	70	mA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) (Continued)

SYMBOL	PARAMETER	SPEED	MIN	MAX	UNIT
ICC7	Standby Current ($\overline{RAS}$ = VIH, $\overline{CAS}$ = VIL, DOUT = Enable)	–	–	5	mA
IIL	Input Leakage Current (Any Input 0 ≤ Vin ≤ 6.5 Volts all other Pins = 0 Volts)	–	−10	10	uA
IOL	Output Leakage Current (Data out is disabled and 0 ≤ Vout ≤ 5.5 V)	–	−10	10	uA
VOH	Output High Voltage Level (IOH = −5mA)	–	2.4	–	V
VOL	Output Low Voltage Level (IOL = 4.2 mA)	–	–	0.4	V

***Note:**
ICC1, ICC3, ICC4 and ICC6 are dependant on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as average current.

3

AC CHARACTERISTICS (See Notes 1, 2) (Ta = 0°C to 70°, VCC = 5V ± 10%)

SYMBOL	PARAMETER	21040-08		21040-10		21040-12		UNITS	Notes
		Min	Max	Min	Max	Min	Max		
tREF	Time between Refresh		16		16		16	ms	
tRC	Random R/W Cycle Time	150		180		220		ns	
tRWC	RMW Cycle Time	175		210		255		ns	
tRAC	Access Time From $\overline{RAS}$		80		100		120	ns	3, 4
tCAC	Access Time From $\overline{CAS}$		20		25		30	ns	3, 4
tAA	Access Time From Column Address		40		50		60	ns	3, 10
tCLZ	$\overline{CAS}$ to Output in low Z	5		5		5		ns	3
tOFF	Output Buffer Turn-Off Delay Time	0	15	0	20	0	30	ns	6
tT	Transition Time	3	50	3	50	3	50	ns	2
tRP	$\overline{RAS}$ Precharge Time	60		70		90		ns	
tRAS	$\overline{RAS}$ Pulse Width	80	10K	100	10K	120	10K	ns	
tRSH	$\overline{RAS}$ Hold Time	20		25		30		ns	
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		10		10		ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	25	90	ns	4, 5
tCAS	$\overline{CAS}$ Pulse Width	20	10K	25	10K	30	10K	ns	
tCSH	$\overline{CAS}$ Hold Time	80		100		120		ns	
tCPN	$\overline{CAS}$ Precharge Time	35		40		45		ns	
tASR	Row Address Set-up Time	0		0		0		ns	
tRAH	Row Address Hold Time	10		15		20		ns	
tASC	Column Address Set-up Time	0		0		0		ns	
tCAH	Column Address Hold Time	15		20		25		ns	
tAR	Column Address Time referenced to $\overline{RAS}$	60		75		90		ns	

AC CHARACTERISTICS (See Notes 1, 2) (Ta = 0°C to 70°, VCC = 5V ± 10%) (Continued)

SYMBOL	PARAMETER	21040-08		21040-10		21040-12		UNITS	Notes
		Min	Max	Min	Max	Min	Max		
tRAD	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	25	60	ns	10
tRAL	Column Address to $\overline{RAS}$ Lead Time	40		50		60		ns	
tRCS	Read Command Set-Up Time	0		0		0		ns	
tRRH	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		ns	8
tRCH	Read Command Hold Time referenced to $\overline{CAS}$	0		0		0		ns	8
tWCS	Write Command Set-Up Time	0		0		0		ns	7
tWCH	Write Command Hold Time	15		20		25		ns	
tWCR	Write Command Hold referenced to $\overline{RAS}$	60		75		90		ns	
tWP	Write Command Pulse Width	15		20		25		ns	
tRWL	Write Command to $\overline{RAS}$ Lead Time	20		25		30		ns	
tCWL	Write Command to $\overline{CAS}$ Lead Time	20		25		30		ns	
tDS	Data Set-up Time	0		0		0		ns	9
tDH	Data Hold Time	15		20		25		ns	9
tDHR	Data-In Hold Time referenced to $\overline{RAS}$	60		75		90		ns	
tRWD	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80		100		120		ns	7
tCWD	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20		25		30		ns	7
tAWD	Column Address to $\overline{WRITE}$ Delay Time	40		50		60		ns	7
tRPC	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	0		0		0		ns	
tCSR	$\overline{CAS}$ Set-up Time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns	
tCHR	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ refresh	30		30		30		ns	
tCPT	$\overline{CAS}$ Precharge Time (Refresh Counter Test)	40		50		60		ns	
tWTS	Write Command Set-up Time (Test Mode in)	10		10		10		ns	
tWTH	Write Command Hold Time (Test Mode in)	10		10		10		ns	
tWRP	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		10		ns	
tWRH	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		10		ns	

AC CHARACTERISTICS (FAST PAGE MODE)
(See Notes 1, 2) (Ta = 0°C to 70°, VCC = 5V ± 10%) (Continued)

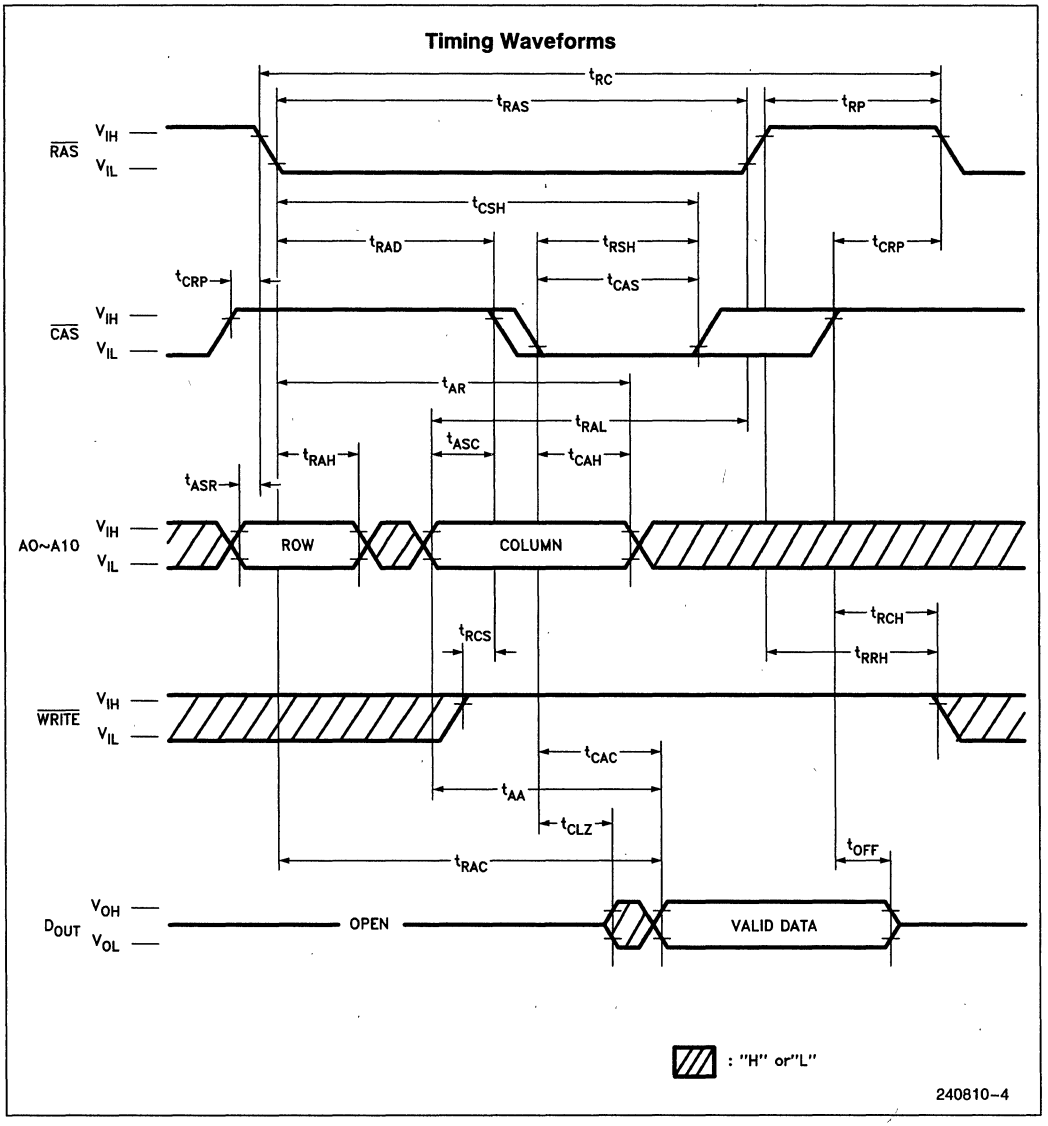
SYMBOL	PARAMETER	21040-08		21040-10		21040-12		UNITS	Notes
		Min	Max	Min	Max	Min	Max		
tPC	Fast Page Mode Cycle Time	55		60		70		ns	
tPRWC	Fast Page Mode RMW Cycle Time	80		90		105		ns	
tCPA	Access Time from $\overline{CAS}$ Precharge		50		55		60	ns	
tCP	Fast Page Mode $\overline{CAS}$ Precharge Time	10		10		15		ns	
tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200K	100	200K	120	200K	ns	

AC CHARACTERISTICS (TEST MODE) (Ta = 0°C to 70°, VCC = 5V ± 10%)

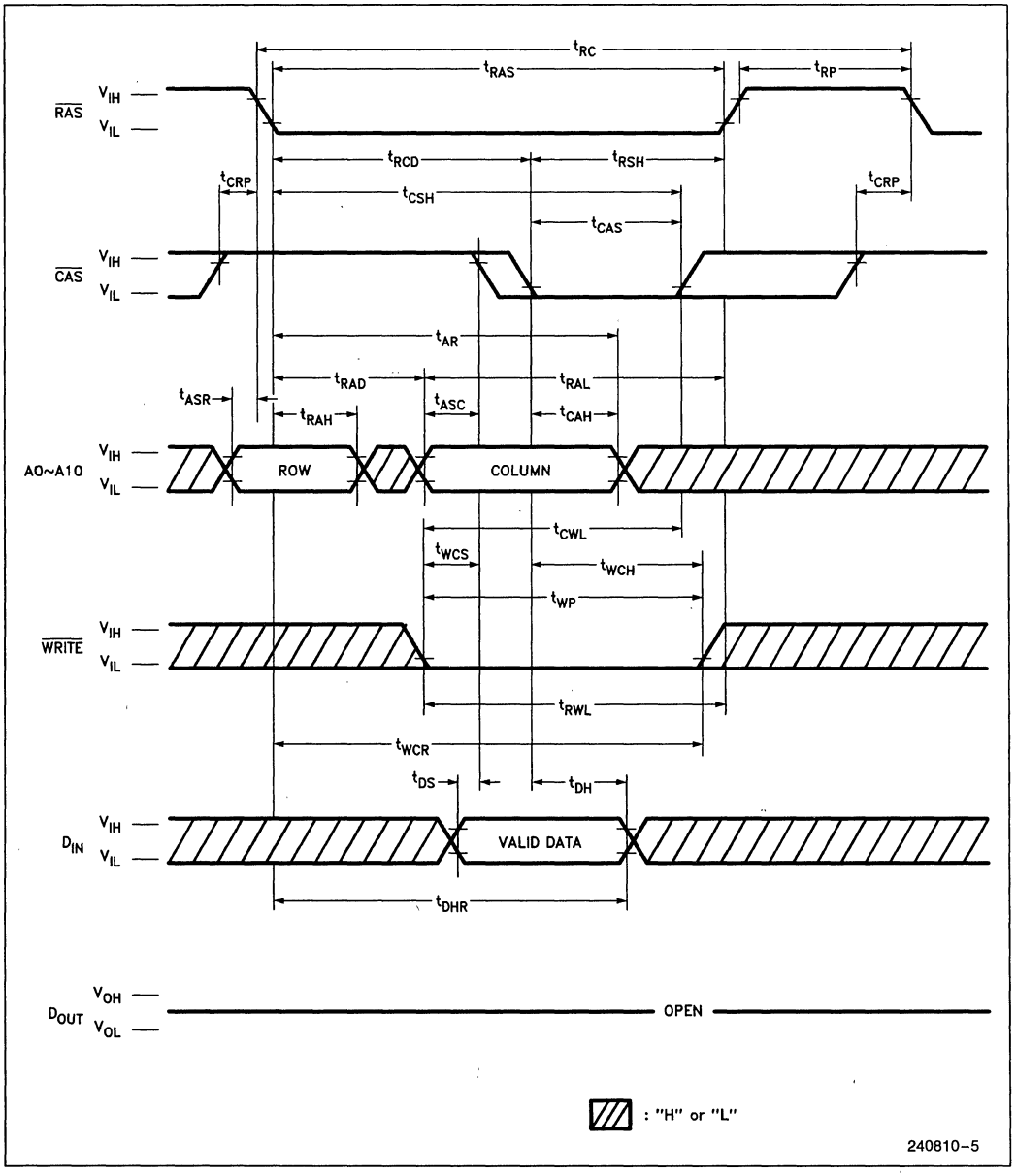
SYMBOL	PARAMETER	(Note 11)							
		21040-08		21040-10		21040-12		UNITS	Notes
		Min	Max	Min	Max	Min	Max		
tRC	Random R/W Cycle Time	155		185		225		ns	
tRWC	RMW Cycle Time	180		215		260		ns	
tPC	Fast Page Mode Cycle Time	60		65		75		ns	
PRWC	Fast Page Mode RMW Cycle Time	85		95		110		ns	
tRAC	Access Time From $\overline{RAS}$		85		105		125	ns	3, 4
tCAC	Access Time From $\overline{CAS}$		25		30		35	ns	3, 4
tAA	Access Time From Column Address		45		55		65	ns	3, 10
tCPA	Access Time From $\overline{CAS}$		55		60		65	ns	
tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200K	105	200K	125	200K	ns	
tRAS	$\overline{RAS}$ Pulse Width	85	10K	105	10K	125	10K	ns	
tRSH	$\overline{RAS}$ Hold Time	25		30		35		ns	
tCAS	$\overline{CAS}$ Pulse Width	25	10K	30	10K	35	10K	ns	
tCSH	$\overline{CAS}$ Hold Time	85		105		125		ns	
tRAL	Column Address To Lead Time	45		55		65		ns	
tRWD	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85		105		125		ns	7
tCWD	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25		30		35		ns	7
tAWD	Column Address to $\overline{WRITE}$ Delay Time	45		55		65		ns	7

NOTES:
1. An initial pause of 200 Microseconds is required after power-up followed by an 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. Vih (min) and Vil (max) are reference levels for measuring timing of input signals. Also, transition times are measured between Vih (min) and Vil (max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to two 2 TTL loads and 100 pF.
4. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. tWCS, tWD, tRWD, and tAWD are non restrictive operating parameters. They are included in the Data Sheet as Electrical characteristics only. If tWCS ≥ tWCS (min), the cycle is an early write cycle and data out pin will remain open circuit through the entire cycle; If tRWD ≥ tRWD (min), tCWD ≥ tCWD (min) and tAWD ≥ tAWD (min), the cycle is a read-write cycle and data out will contain data read from the selected cell; If neither of the above set of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the tRAD (max) limit insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled by tAA.
11. These specifications are applicable in the test mode.

READ CYCLE

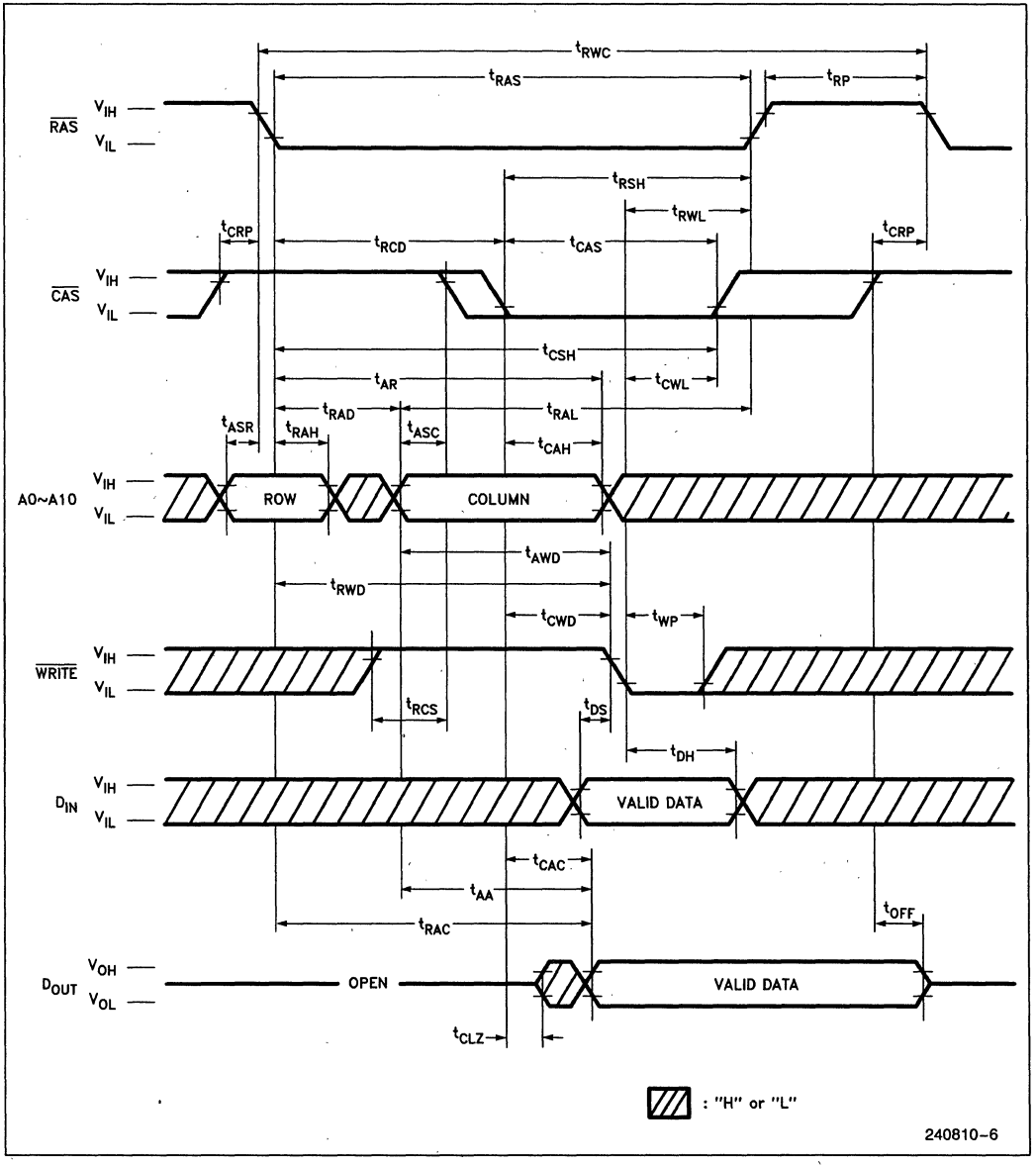

Timing Waveforms
tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRAD
tRSH
tCRP
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAL
tASC
tRAH
tCAH
tASR
AO~A10
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or"L"
240810-4

WRITE CYCLE (EARLY WRITE)

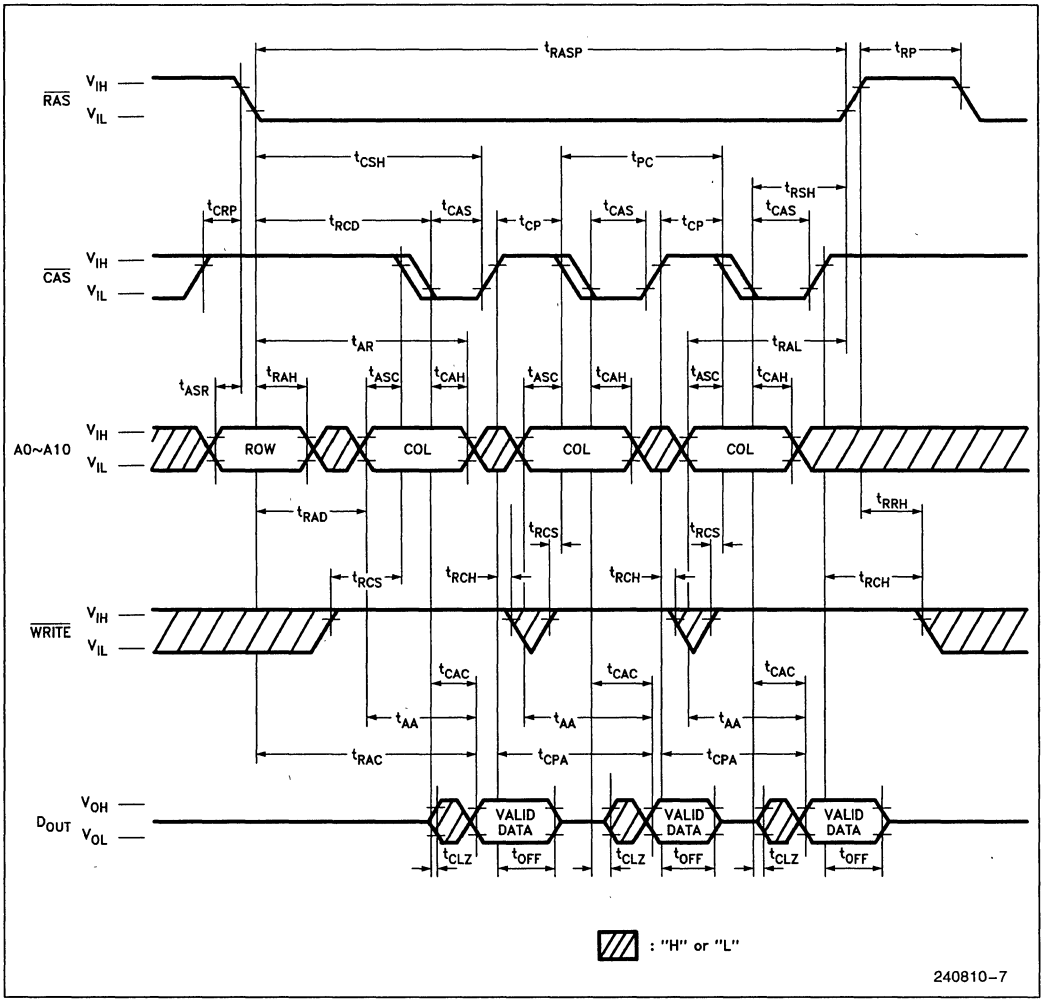


3

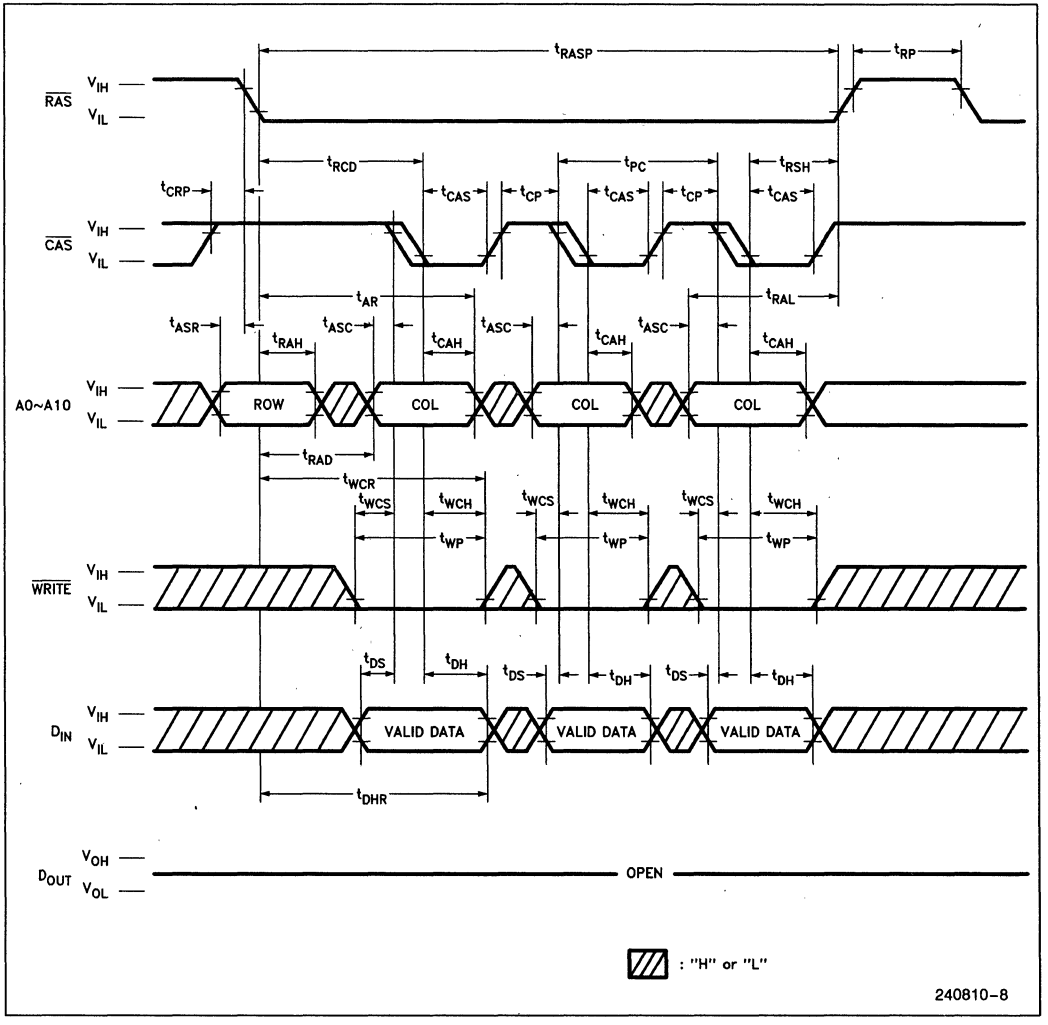
READ-WRITE CYCLE



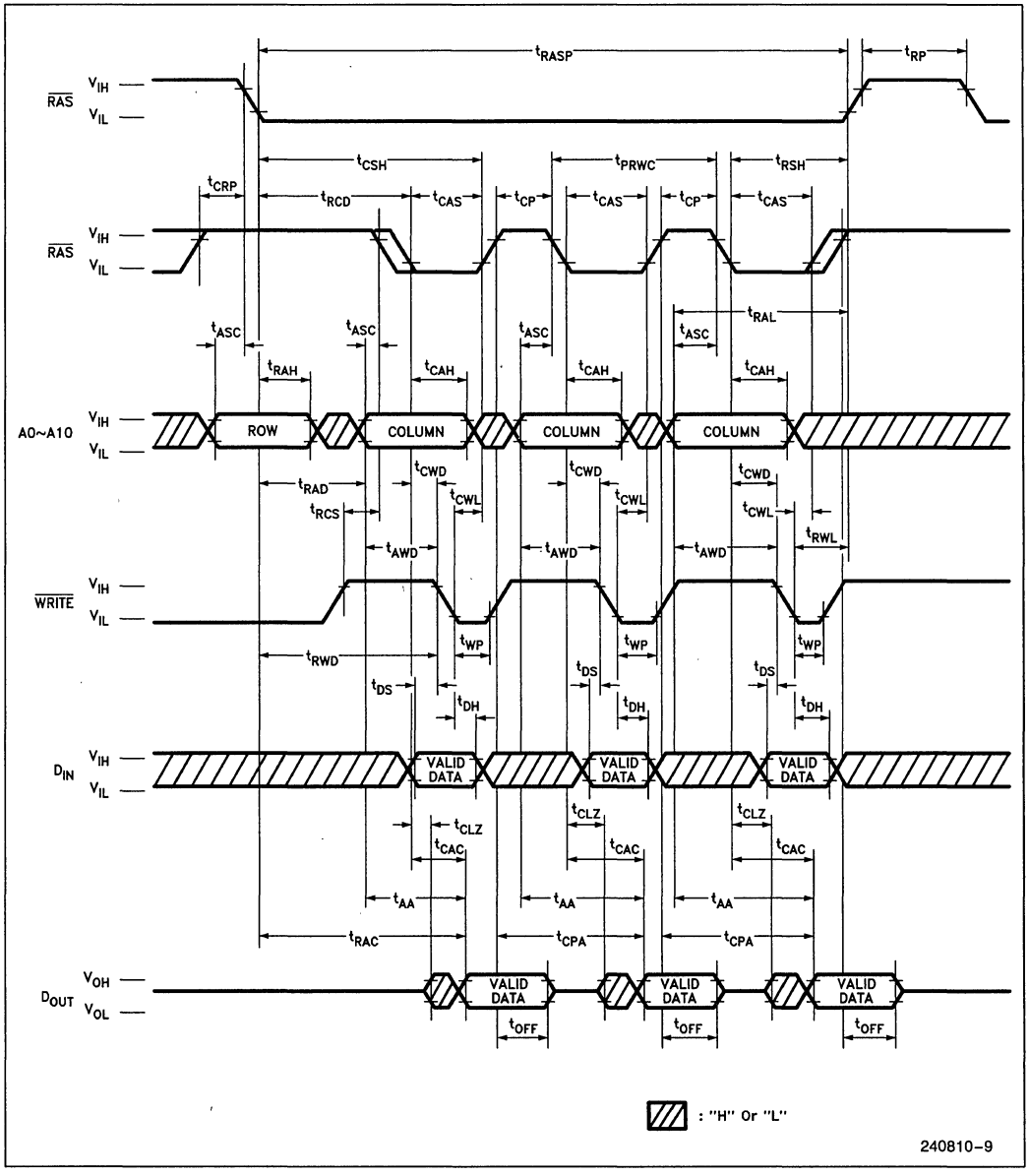
FAST PAGE MODE READ CYCLE



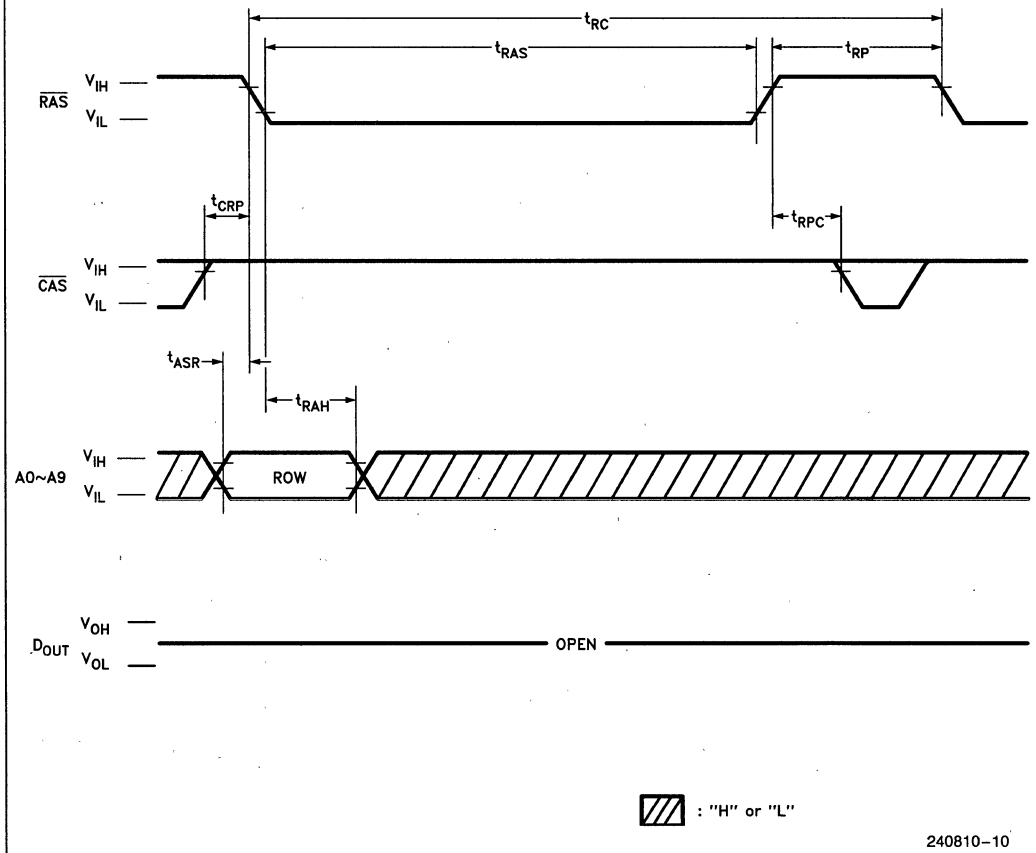
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-WRITE CYCLE

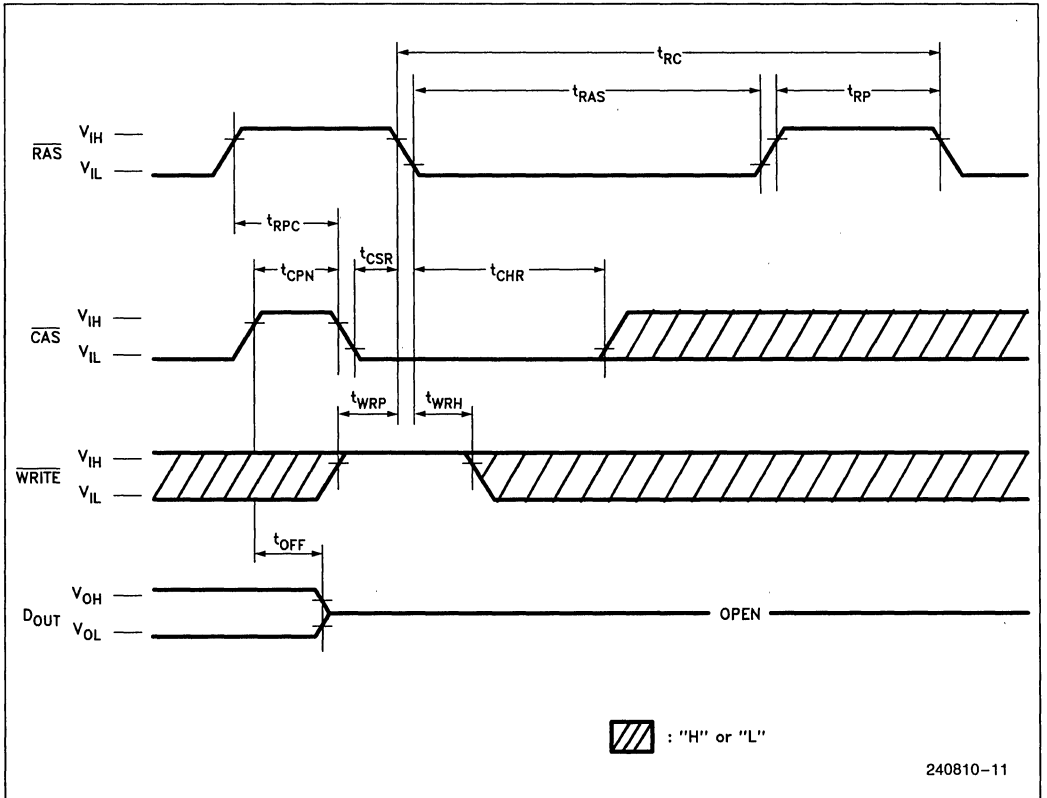


$\overline{RAS}$ ONLY REFRESH CYCLE



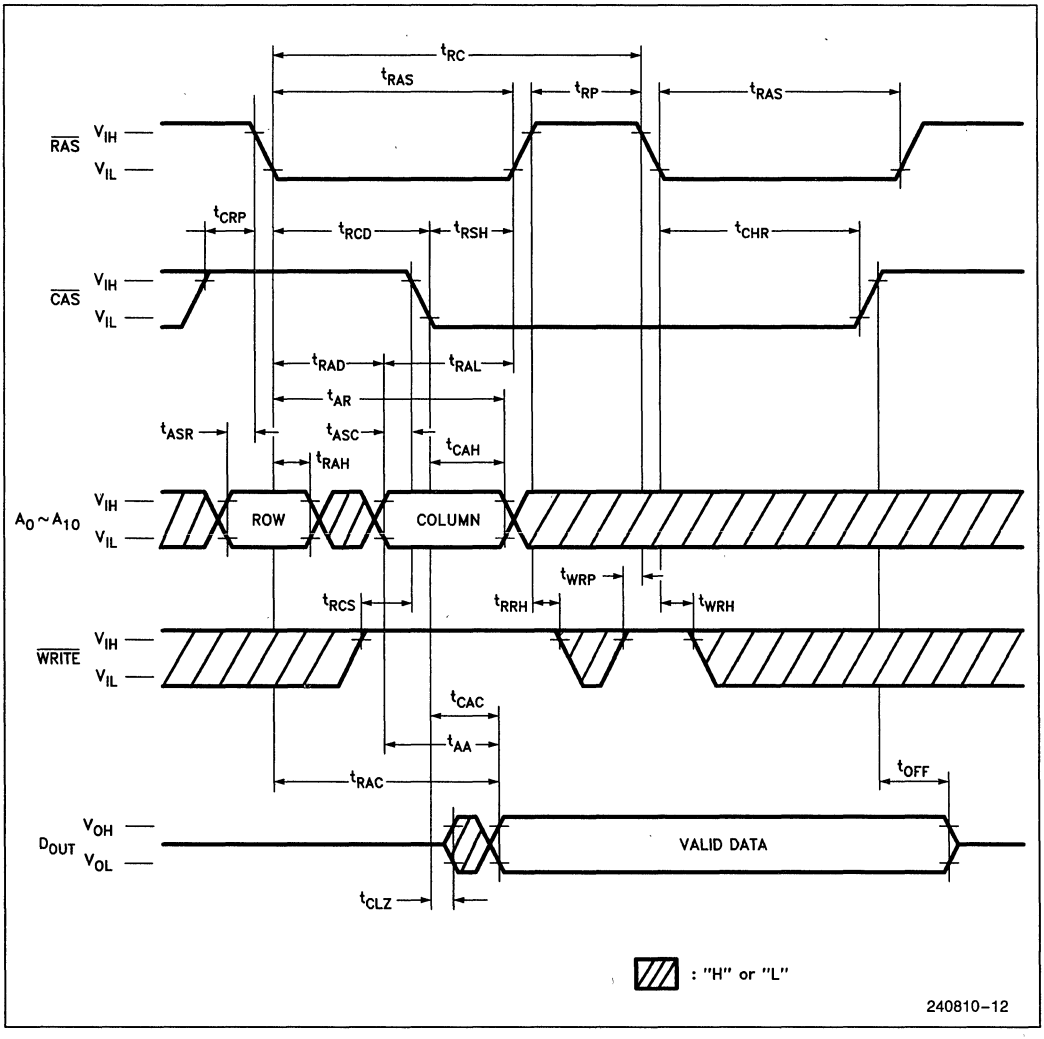
NOTE:
$\overline{WRITE}$ = "H" or "L", A10 = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

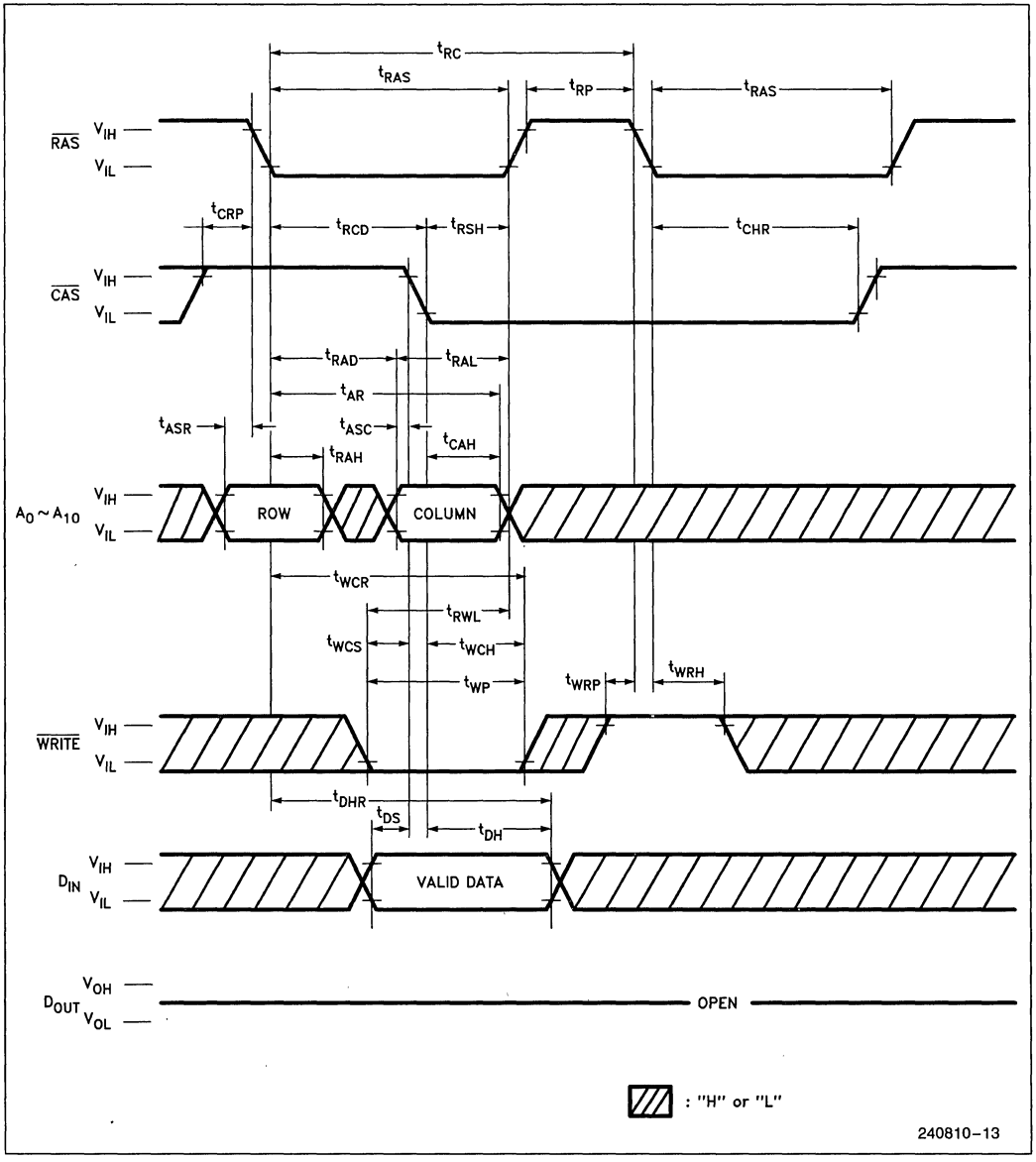


NOTE:
A0 ~ A10="H" or "L"

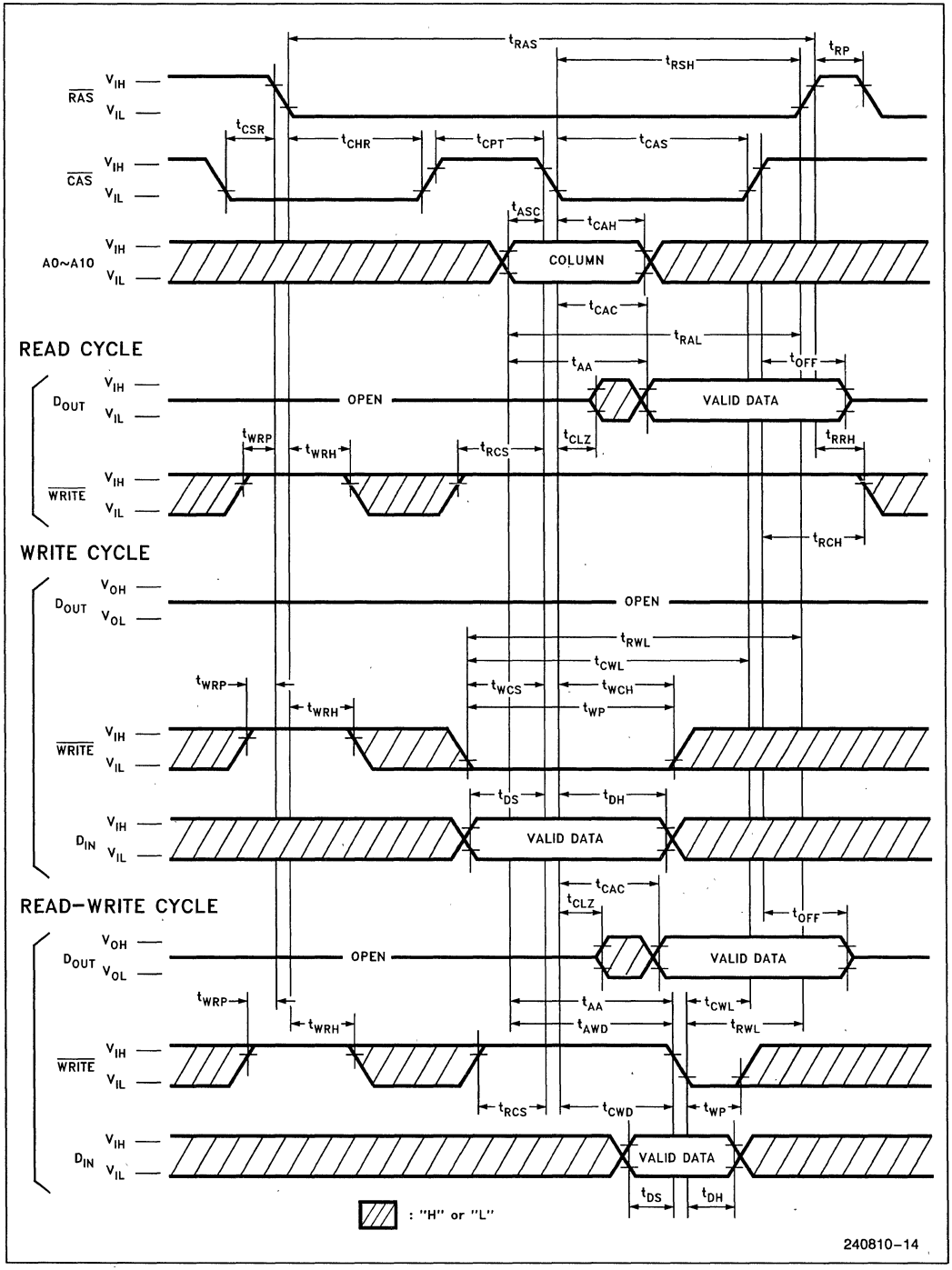
HIDDEN REFRESH CYCLE (READ)



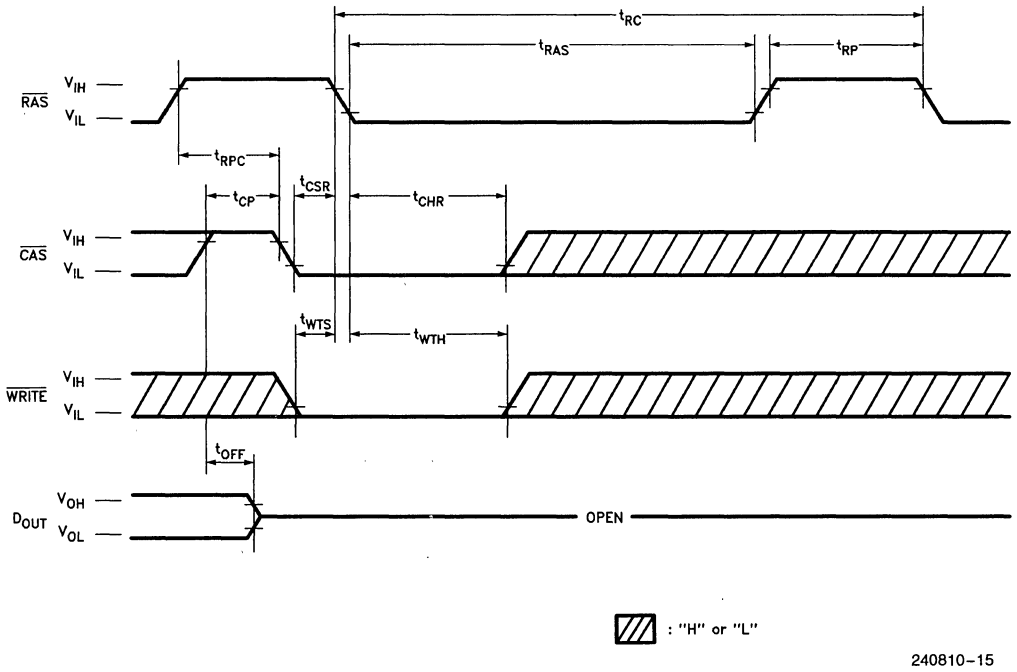
HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE



NOTE:
D_{IN}, A0 ~ A10: "H" or "L"

TEST MODE DESCRIPTION

The 21040 is internally organized as 524,288 words by 8 bits. In the "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used for designation of memory cells in the "Test Mode". If upon reading, all bits are equal (all "1"s, or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". In the "Test Mode", the 21040 device can be treated as if it were a 512K DRAM.

WRITE and $\overline{CAS}$ before $\overline{RAS}$ Refresh cycle is used to enter the "Test Mode" while "$\overline{RAS}$ only Refresh cycle" or "$\overline{CAS}$ before $\overline{RAS}$ Refresh cycle" is used to put the device back into the "Normal Mode". The "Test Mode" function can reduce the test time (1/8 for "N" type pattern) drastically by taking advantage of the 512K × 8 bits organization.

DEVICE OPERATION

The 21040 contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the 21040 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21040 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21040 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21040 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}/\overline{CAS}$ cycle. The output of the 21040 remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 21040 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21040 has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write). Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21040 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the 21040 is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21040 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21040 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the 21040 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Page Mode

The 21040 has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21040 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. 8 initialization cycles are also required after any 4 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21040 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21040 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

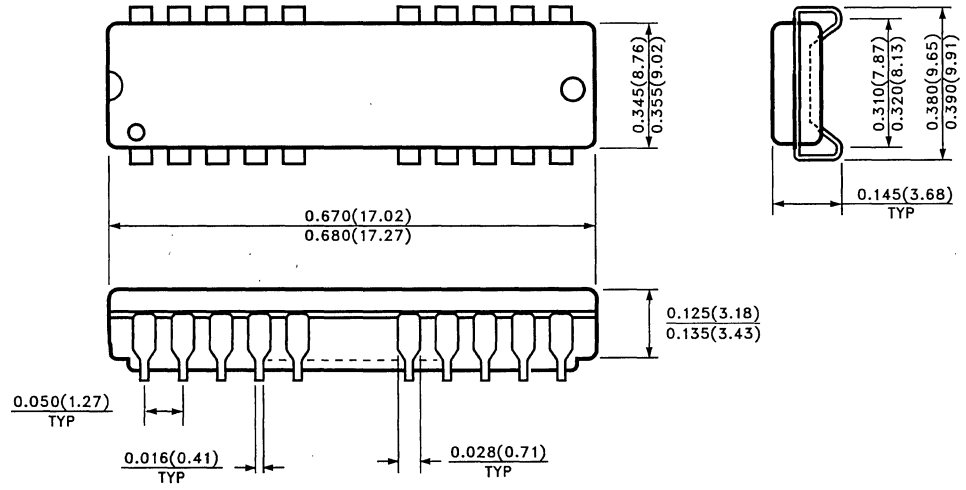
The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21040 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21040 and they supply much of the current used by the 21040 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

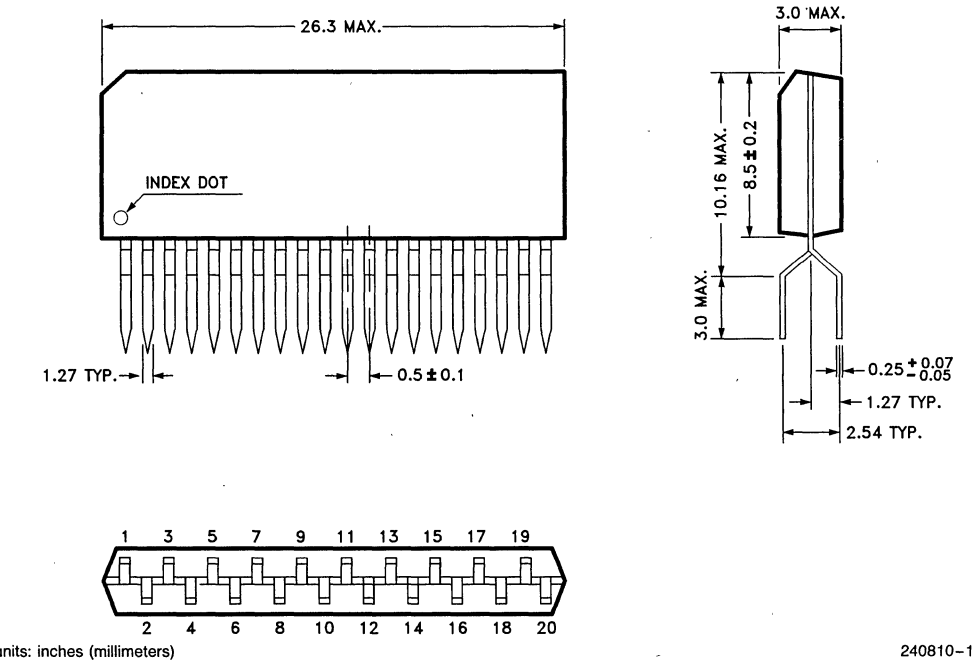
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



units: inches (millimeters)

240810-16

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



units: inches (millimeters)

240810-17

2D2569
256K x 9-BIT HIGH DENSITY DYNAMIC RAM MEMORY MODULE WITH PAGE MODE

■ Performance Range

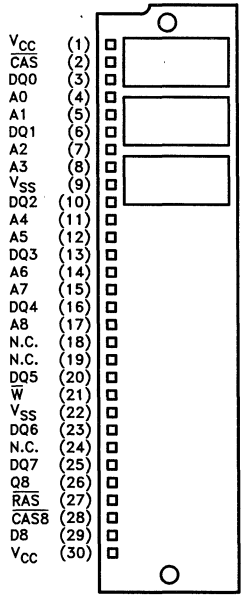
Parameter	2D2569-08	2D2569-10	Units
Acces Time from $\overline{RAS}$ (t_{RAC})	80	100	ns
Access Time from $\overline{CAS}$ (t_{CAC})	40	50	ns
Read Cycle Time (t_{RC})	250	190	ns

- **256K x 9-Bit Organization**
- **Industry Standard Pin-Out in a 30-Pin Single In-Line Memory Module (SIMM)**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **512 Refresh Cycles every 8 ms**
- **Separate $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ ($\overline{CAS8}$) Control for One Separate Pair of Data-In and Data-Out Lines**
- **Supports Page Mode Operation**
- **TTL Compatible Inputs and Outputs**

The 2D2569 is a 256K words by 9-bit memory module consisting of two industry standard 256K x 4-bit dynamic RAMs in SOJ package and one 256K x 1-bit PLCC package.

The 18 address bits are entered 10 bits at a time using $\overline{RAS}$ to latch the first 10 bits and $\overline{CAS}$ to control the latter 9 bits. The ninth bit D8, Q8 is generally used for parity and is controlled by $\overline{CAS8}$.

The common I/O feature requires the use of an early write cycle to prevent data contention on DQ lines.



240838-1

Figure 1. Pin Assignment

Pin Names

A0–A8	Address Inputs
DQ1–DQ7	Data Inputs/Outputs
D8	Data Input
Q8	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$–$\overline{CAS8}$	Column Address Strobe
$\overline{W}$	R/W Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

September 1990
Order Number: 240838-001

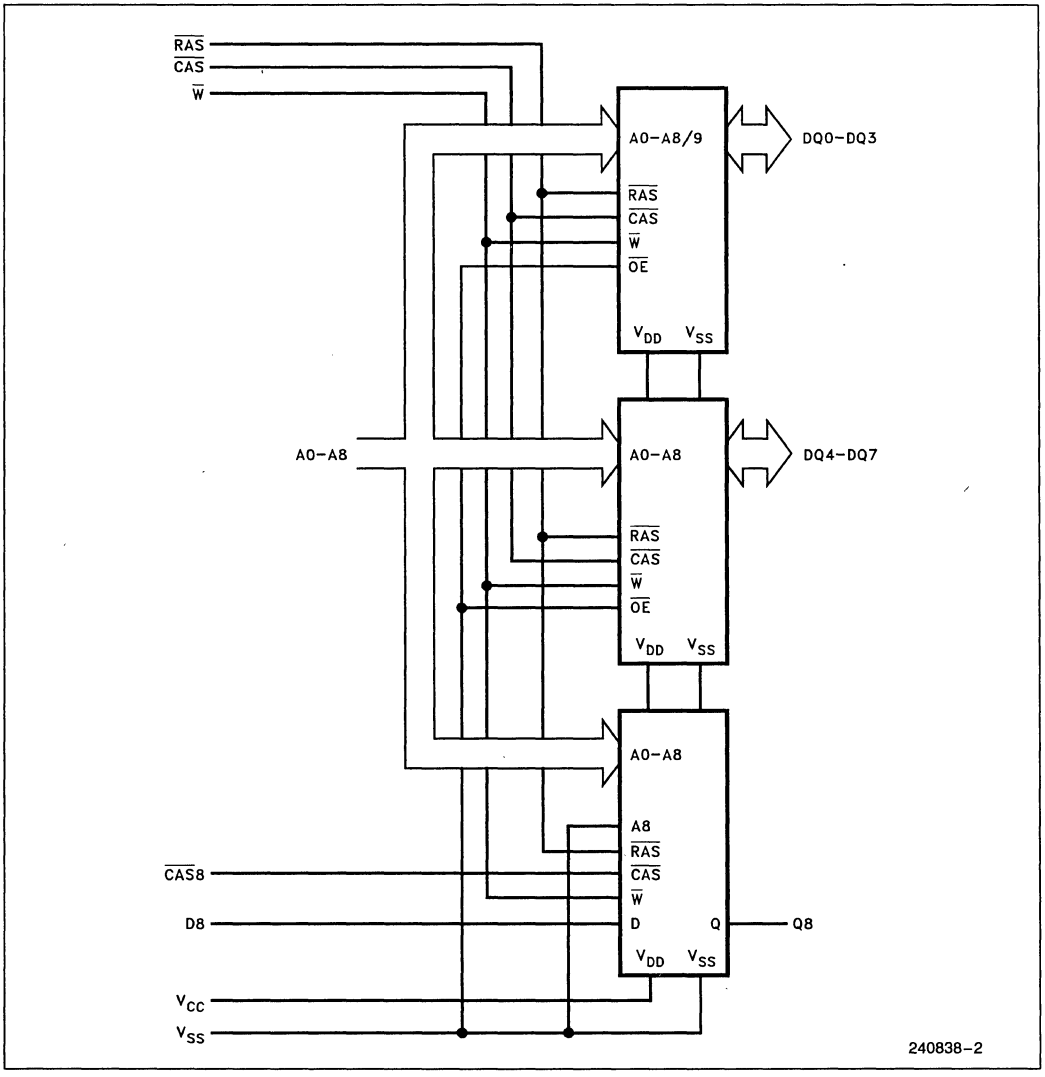


Figure 2. Block Diagram

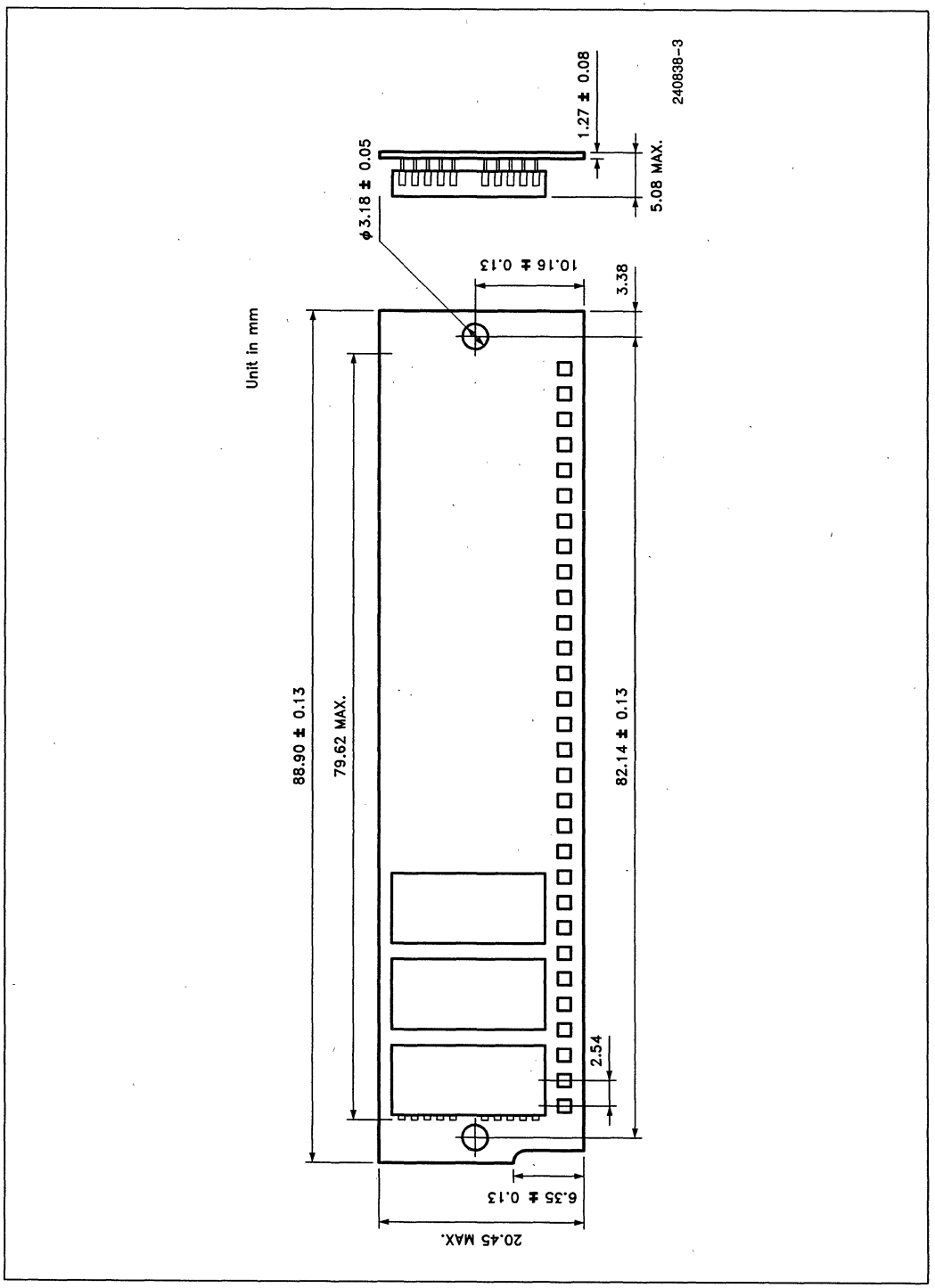


Figure 3. Outline Drawing

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V

Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V

Storage Temperature (T_{STG}) .... −55°C to +125°C

Soldering Temperature • Time (T_{solder}) ..... 260°C • 10 Sec

Power Dissipation (P_d) 9W

Short Circuit Output Current (I_{OUT}) ..... 50 mA

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS (Voltage Referenced to V_{SS}. T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

3

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_i (A)	Input Capacitance (A0–A9)		75	pF
C_{dq}	I/O Capacitance		20	pF
C_i ($\overline{W}$)	Input Capacitance, Write Control Input		80	pF
C_i ($\overline{RAS}$)	Input Capacitance, $\overline{RAS}$ Input		100	pF
C_i ($\overline{CAS}$)	Input Capacitance, $\overline{CAS}$ Input		100	pF
C_i ($\overline{CASP}$)	Input Capacitance, $\overline{CASP}$ Input		20	pF
C_i (DP)	Input Capacitance		15	pF
C_o (QP)	Output Capacitance		15	pF

D.C. AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter		Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		205 175	mA
I_{CC2}	Standby Current	$\overline{RAS} = \overline{CAS} = V_{IH}$			11	mA
		$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$			9	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC} = Min)		−08 −10		195 160	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC} = Min)		−08 −10		165 135	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		205 175	mA
I_{IL}	Input Current (Any Input $0 \leq V_{IN} \leq 6.5V$ All Other Pins = 0V)			−90	90	μA
I_{OZ}	Off State Output Current (Data Out is Disabled and $0 \leq V_{OUT} \leq 5.5V$)			−30	30	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)			2.4	V_{CC}	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0	0.4	V

NOTE:
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

A.C. CHARACTERISTICS[1, 2] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	2D2569-08		2D2569-10		Units	Notes
		Min	Max	Min	Mas		
t_{RAC}	Access Time from $\overline{RAS}$		80		100	ns	4, 7
t_{CAC}	Acces Time from $\overline{CAS}$		40		50	ns	5, 7
t_{CAA}	Access Time from Column Address		45		50	ns	6, 7
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		55	ns	7, 14
t_{CLZ}	Output Low Impedance Time from $\overline{CAS}$ Low	5		5		ns	7
t_{OFF}	Output Disable Time after $\overline{CAS}$ High	0	25	0	30	ns	
t_{REF}	Refresh Cycle Time		4		4	ms	
t_T	Transition Time	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ High Pulse Width	60		80		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		15		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	25	50	ns	9, 10
t_{CPN}	$\overline{CAS}$ High Pulse Width	20		25		ns	
t_{RAD}	Column Addres Delay Time from $\overline{RAS}$ Low	20	40	20	50	ns	11
t_{ASR}	Row Address Setup Time before $\overline{RAS}$ Low	0		0		ns	
t_{ASC}	Column Address Time before $\overline{CAS}$ Low	0		0		ns	
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ LOW	15		15		ns	
t_{CAH}	Column Address Hold Time after $\overline{CAS}$ Low or $\overline{W}$ Low	15		20		ns	

3

A.C. CHARACTERISTICS(1, 2) (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ AND REFRESH CYCLES

Symbol	Parameter	2D2569-08		2D2569-10		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	150		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	40	10K	50	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	40		50		ns	
t_{RCS}	Read Setup Time before $\overline{CAS}$ Low	0		0		ns	
t_{RCH}	Read Hold Time after $\overline{CAS}$ High	0		0		ns	12
t_{RRH}	Read Hold Time after $\overline{RAS}$ High	0		0		ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Setup Time	45		55		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Symbol	Parameter	2D2569-08		2D2569-10		Units	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	30		30		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	0		0		ns	

A.C. CHARACTERISTICS (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

WRITE CYCLE (Early Write)

Symbol	Parameter	2D2569-08		2D2569-10		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	160		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	130	10K	160	10K	ns	
t_{DS}	Data Setup Time	0		0		ns	
t_{DH}	Data Hold Time after $\overline{CAS}$ Low	20		20		ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{WCS}	Write Setup Time before $\overline{CAS}$ Low	0		0		ns	13
t_{WCH}	Write Hold Time after $\overline{CAS}$ Low	15		20		ns	
t_{WP}	Write Pulse Width	15		20		ns	

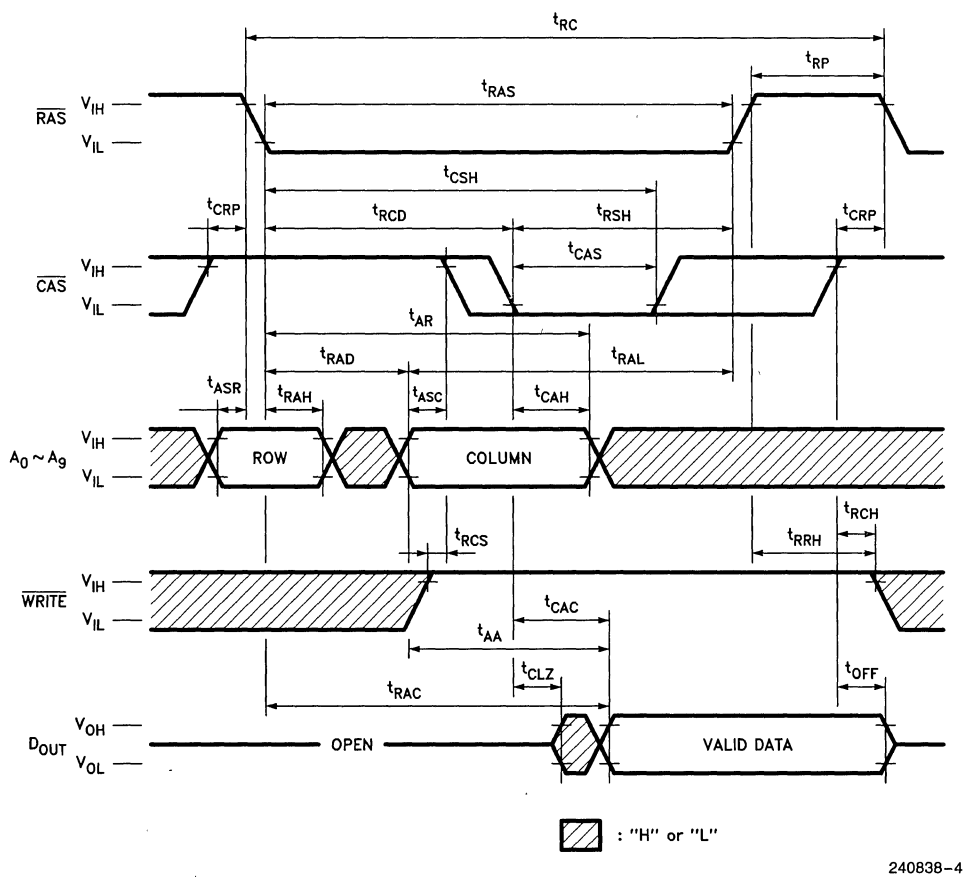
3

FAST PAGE MODE CYCLE (Read, Early Write cycles)

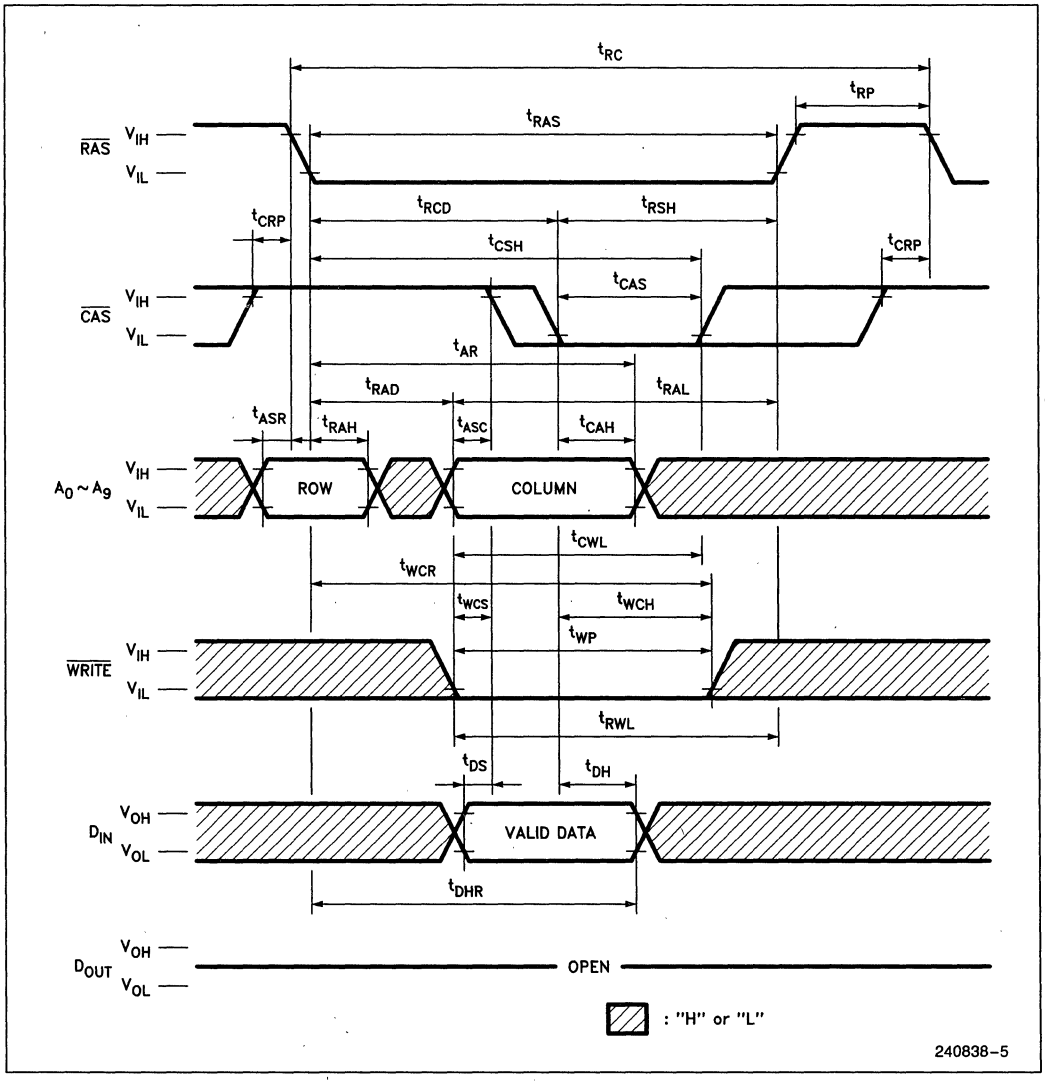
Symbol	Parameter	2D2569-08		2D2569-10		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	75		90		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	130	10K	160	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width for Read Cycle	20	10K	25	10K	ns	
t_{CP}	$\overline{CAS}$ High Pulse Width	25		30		ns	

NOTES:
1. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. Characteristics assume $t_T = 5$ ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$(max), $t_{RAD} \geq t_{RAD}$(max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ + t_{ASC}(min).
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H").

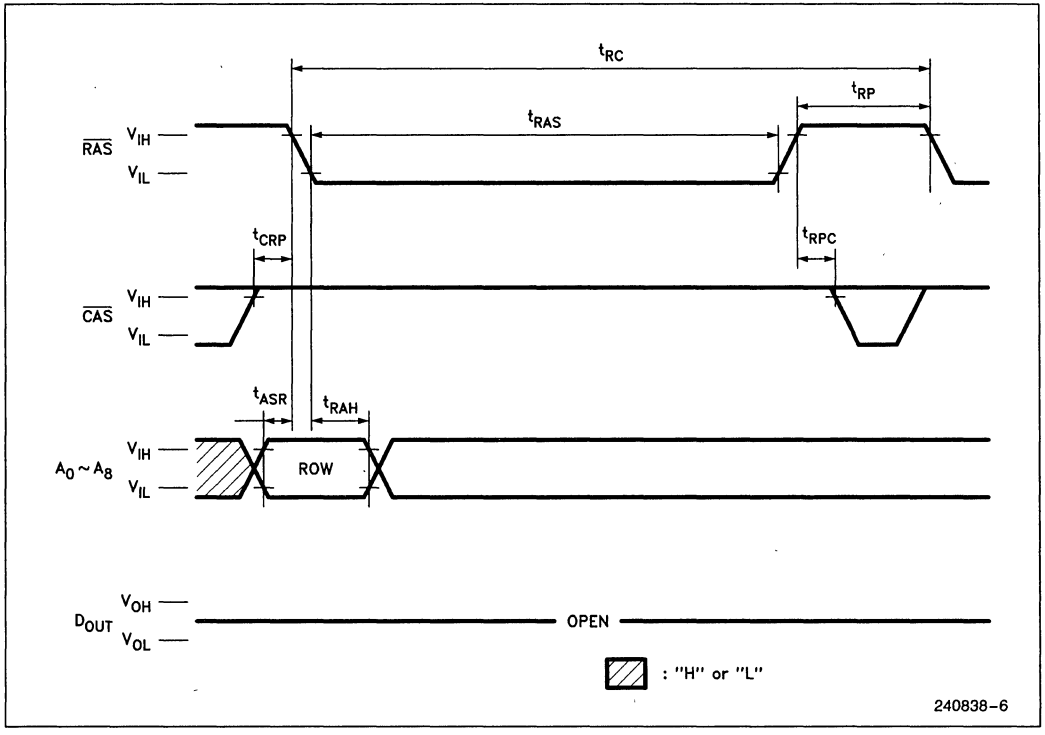
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0 ~ A9
VIH
VIL
ROW
COLUMN
tRCS
tRCH
tRRH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"
240838-4

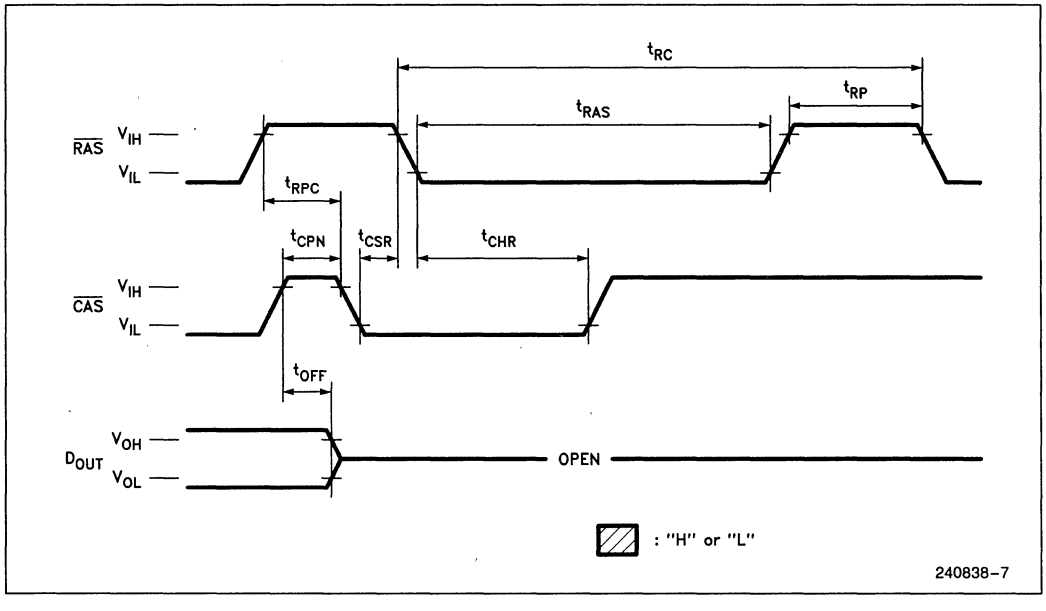
EARLY WRITE CYCLE



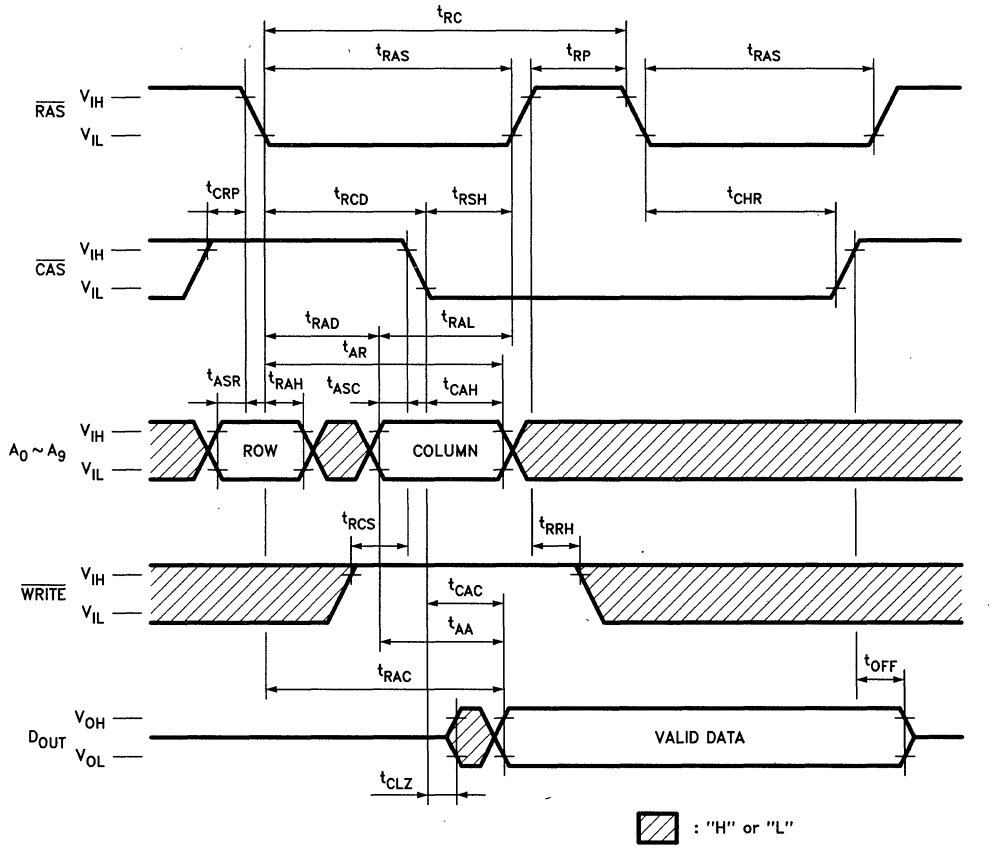
$\overline{RAS}$ ONLY REFRESH CYCLE



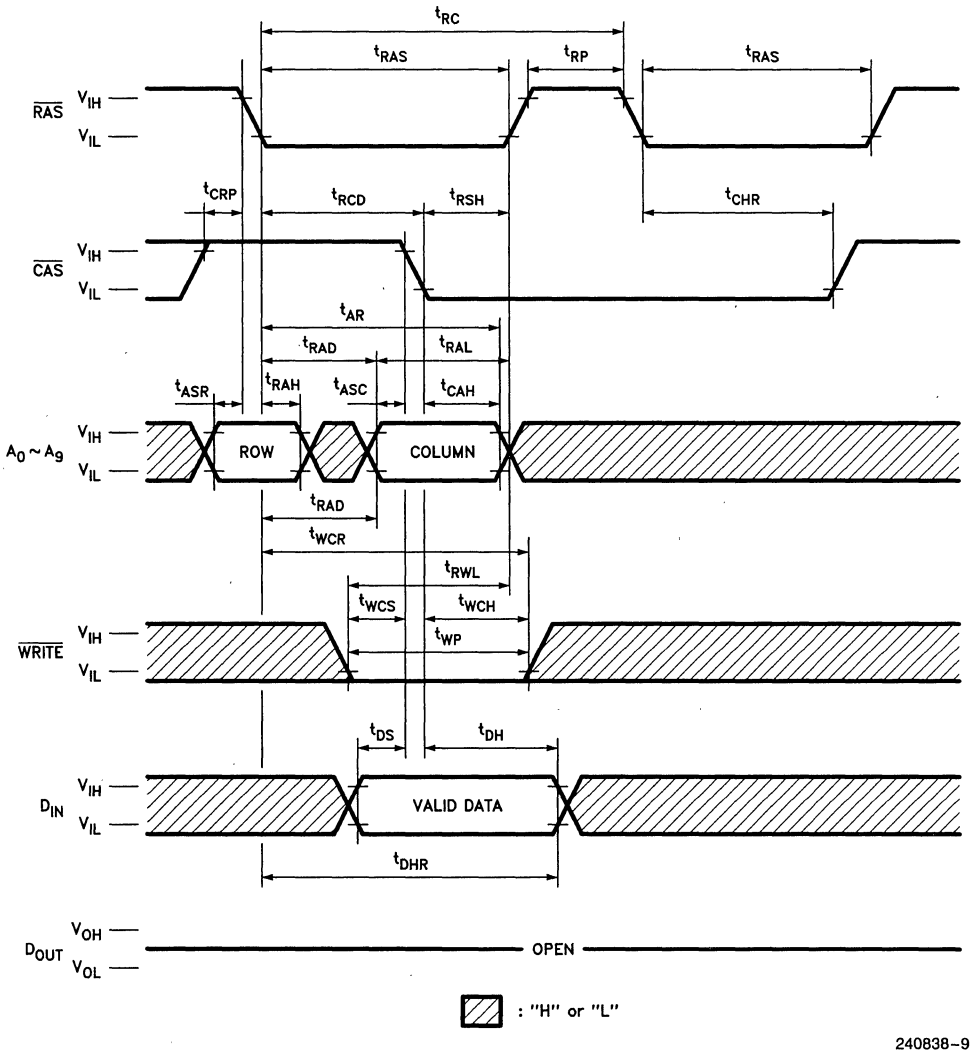
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



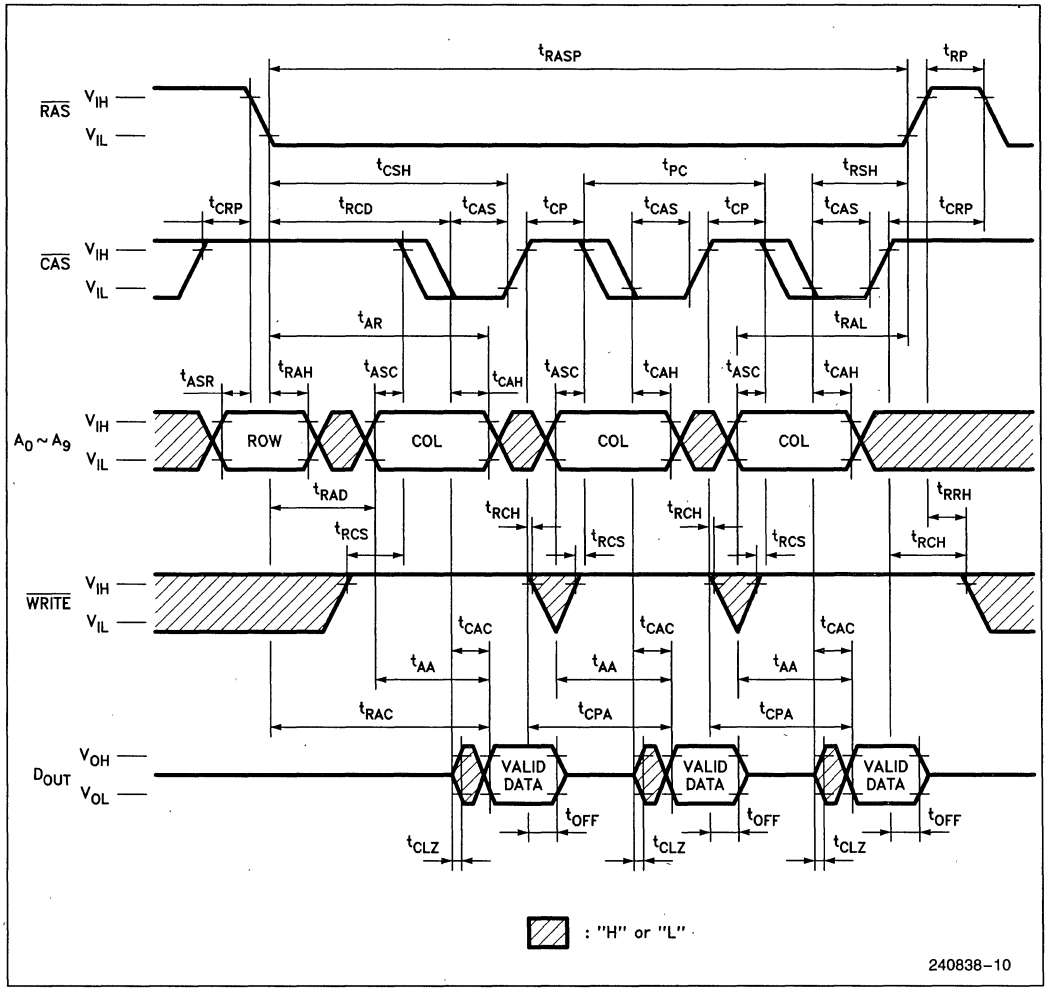
HIDDEN REFRESH CYCLE (READ)



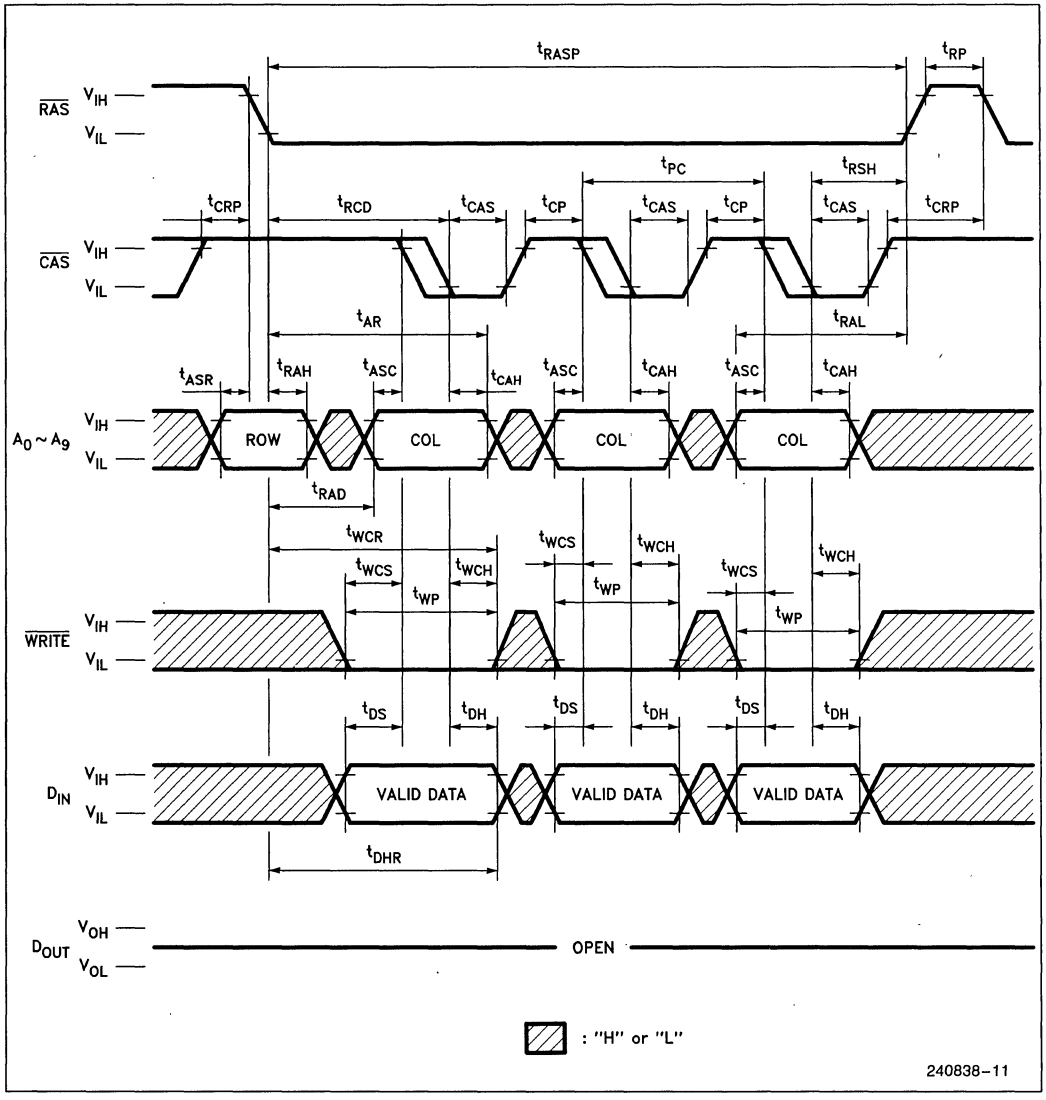
HIDDEN REFRESH CYCLE (WRITE)



FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



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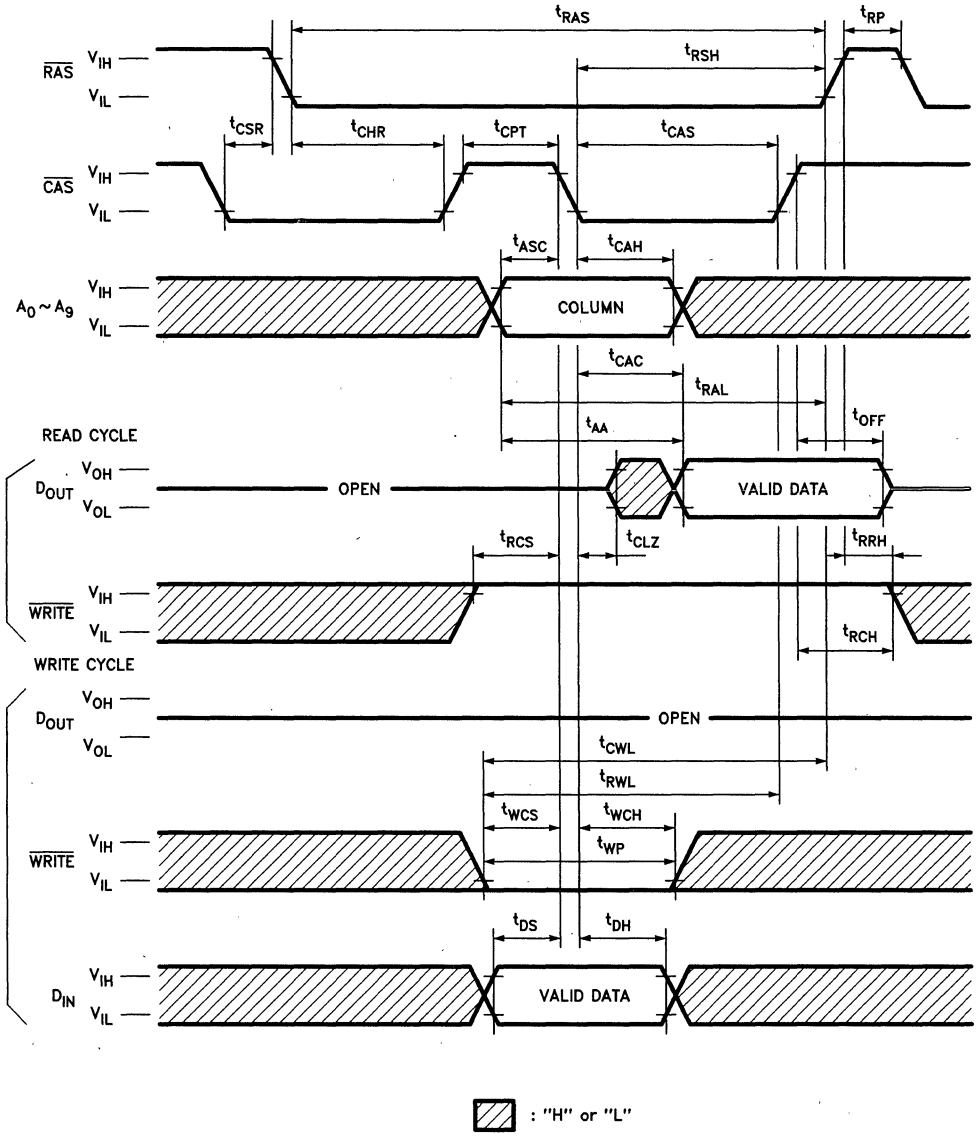
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



21019
1,048,576 x 9-BIT DYNAMIC RAM MEMORY MODULE WITH PAGE MODE

	21019-06	21019-07	21019-08	21019-10	Units
Acces Time from $\overline{RAS}$ (t_{RAC})	60	70	80	100	ns
Access Time from $\overline{CAS}$ (t_{CAC})	20	20	20	25	ns
Read Cycle Time (t_{RC})	125	140	160	190	ns

- **1,048,576 x 9-Bit Organization**
- **Industry Standard Pin-Out in a 30-Pin Single In-Line Memory Module (SIMM)**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **512 Refresh Cycles every 8 ms**
- **Separate $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ ($\overline{CAS8}$) Control for One Separate Pair of Data-In and Data-Out Lines**
- **TTL Compatible Inputs and Outputs**

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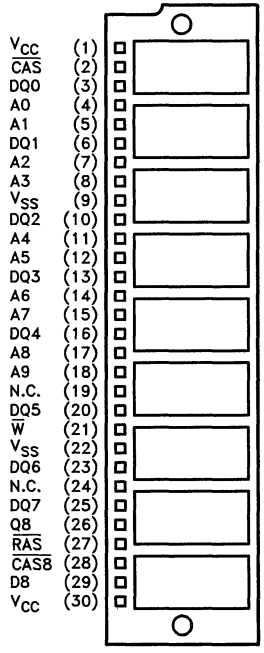
The 21019 is a 1,048,576 words by 9-bit memory module consisting of industry standard 1 Meg x 1 dynamic RAMs in SOJ package.

The 20 address bits are entered 10 bits at a time using $\overline{RAS}$ to latch the first 10 bits and $\overline{CAS}$ to control the latter 10 bits. The ninth bit D8, Q8 is generally used for parity and is controlled by $\overline{CAS8}$.

The common I/O feature requires the use of an early write cycle to prevent data contention on DQ lines.



240721-1

Figure 1. Pin Assignment

Pin Names

A0–A9	Address Inputs
DQ1–DQ7	Data Inputs/Outputs
D8	Data Input
Q8	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$–$\overline{CAS8}$	Column Address Strobe
$\overline{W}$	R/W Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

November 1990
Order Number: 240721-002

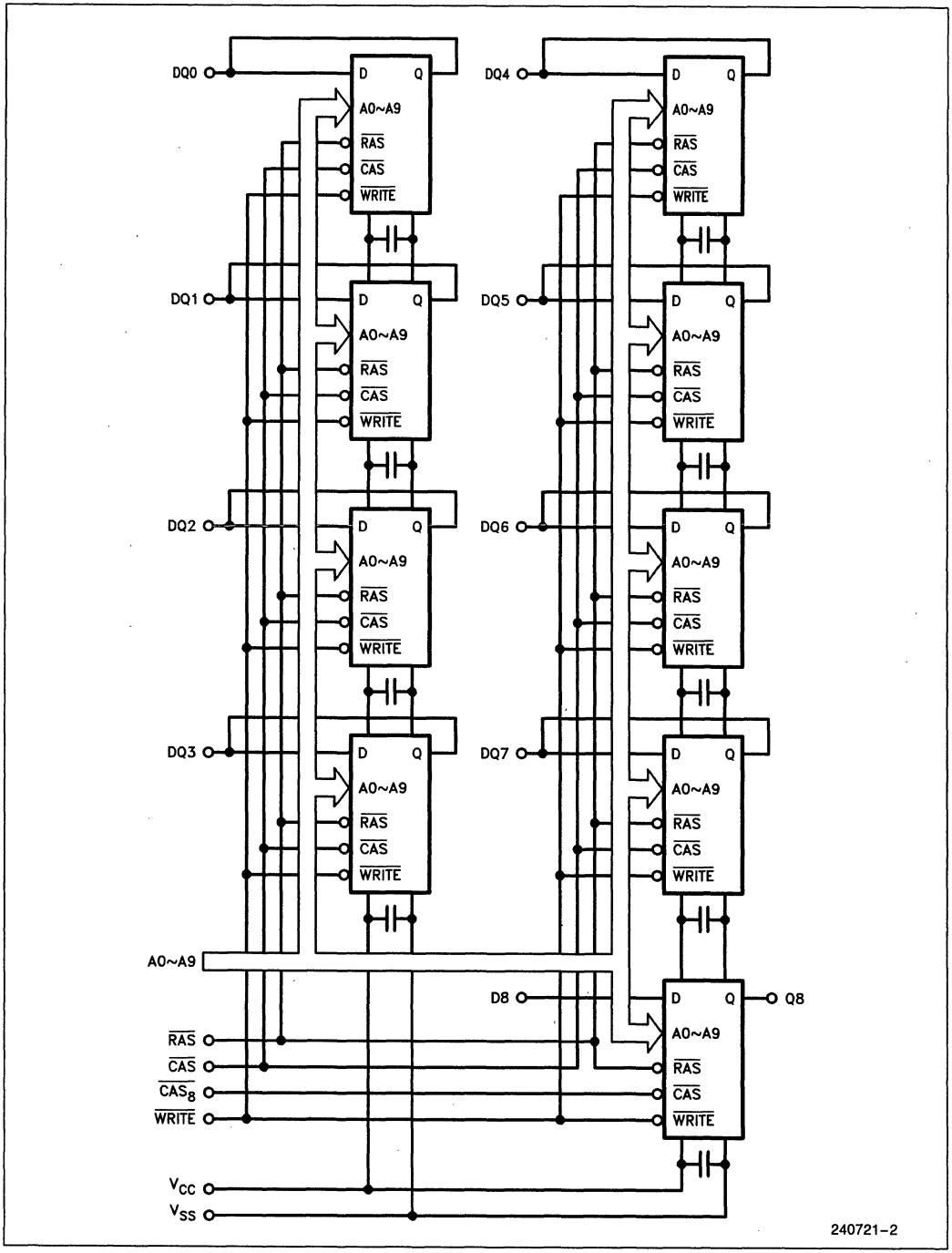


Figure 2. Block Diagram

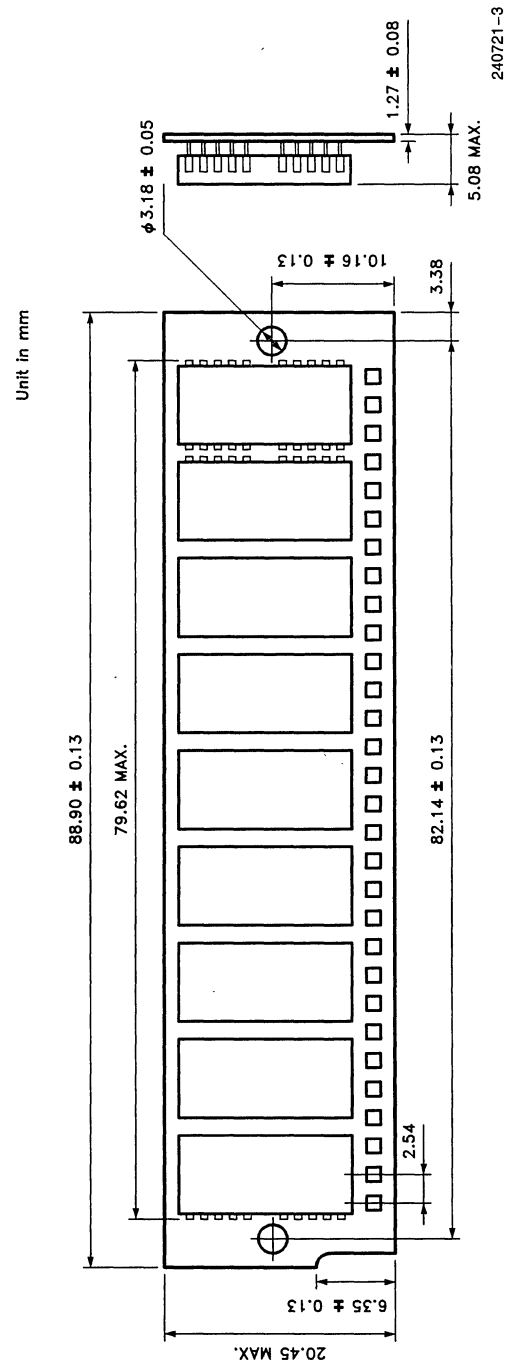


Figure 3. Outline Drawing

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V
Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V
Storage Temperature (T_{STG}) .... −55°C to +125°C
Soldering Temperature • Time (T_{solder}) ..... 260°C • 10 Sec
Power Dissipation (P_d) 9W
Short Circuit Output Current (I_{OUT}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS (Voltage Referenced to V_{SS}. T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_i (A)	Input Capacitance (A0–A9)		75	pF
C_{dq}	I/O Capacitance		20	pF
C_i ($\overline{W}$)	Input Capacitance, Write Control Input		80	pF
C_i ($\overline{RAS}$)	Input Capacitance, $\overline{RAS}$ Input		100	pF
C_i ($\overline{CAS}$)	Input Capacitance, $\overline{CAS}$ Input		100	pF
C_i ($\overline{CASP}$)	Input Capacitance, $\overline{CASP}$ Input		20	pF
C_i (DP)	Input Capacitance		15	pF
C_o (QP)	Output Capacitance		15	pF

D.C. AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter		Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−06 −07 −08 −10		810 720 675 540	mA
I_{CC2}	Standby Current	$\overline{RAS} = \overline{CAS} = V_{IH}$			18	mA
		$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$			9	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC} = Min)		−06 −07 −08 −10		810 720 675 540	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC} = Min)		−06 −07 −08 −10		630 560 540 450	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−06 −07 −08 −10		810 720 675 540	mA
I_{IL}	Input Current (Any Input 0 ≤ V_{IN} ≤ 6.5V All Other Pins = 0V)			−90	90	μA
I_{OZ}	Off State Output Current (Data Out is Disabled and 0 ≤ V_{OUT} ≤ 5.5V)			−20	20	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)			2.4	V_{CC}	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0	0.4	V

NOTE:
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

A.C. CHARACTERISTICS[1, 2] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	21019-06		21019-07		21019-08		21019-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	4, 7
t_{CAC}	Acces Time from $\overline{CAS}$		20		20		20		25	ns	5, 7
t_{CAA}	Access Time from Column Address		30		35		45		50	ns	6, 7
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		45		55	ns	7, 14
t_{CLZ}	Output Low Impedance Time from $\overline{CAS}$ Low	0	20	0	20	5		5		ns	7
t_{OFF}	Output Disable Time after $\overline{CAS}$ High	0	20	0	20	0	20	0	30	ns	
t_{REF}	Refresh Cycle Time		8		8		8		8	ms	
t_T	Transition Time	3	50	3	50	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ High Pulse Width	55		60		70		80		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	25	60	25	75	ns	9, 10
t_{CPN}	$\overline{CAS}$ High Pulse Width	35		35		35		35		ns	
t_{RAD}	Column Address Delay Time from $\overline{RAS}$ Low	15	30	15	35	20	40	20	50	ns	11
t_{ASR}	Row Address Setup Time before $\overline{RAS}$ Low	0		0		0		0		ns	
t_{ASC}	Column Address Time before $\overline{CAS}$ Low	0	20	0	20	0	20	0	20	ns	
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ LOW	15		15		15		15		ns	
t_{CAH}	Column Address Hold Time after $\overline{CAS}$ Low or $\overline{W}$ Low	20		20		20		20		ns	

A.C. CHARACTERISTICS[1, 2] (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ AND REFRESH CYCLES

Symbol	Parameter	21019-06		21019-07		21019-08		21019-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	125		140		160		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	60		70		80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		20		20		30		ns	
t_{RCS}	Read Setup Time before $\overline{CAS}$ Low	0		0		0		0		ns	
t_{RCH}	Read Hold Time after $\overline{CAS}$ High	0		0		0		0		ns	12
t_{RRH}	Read Hold Time after $\overline{RAS}$ High	10		10		10		10		ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Setup Time	30		35		45		55		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		10		10		ns	

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Symbol	Parameter	21019-06		21019-07		21019-08		21019-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	15		15		30		30		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	0		0		0		0		ns	

A.C. CHARACTERISTICS (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

WRITE CYCLE (Early Write)

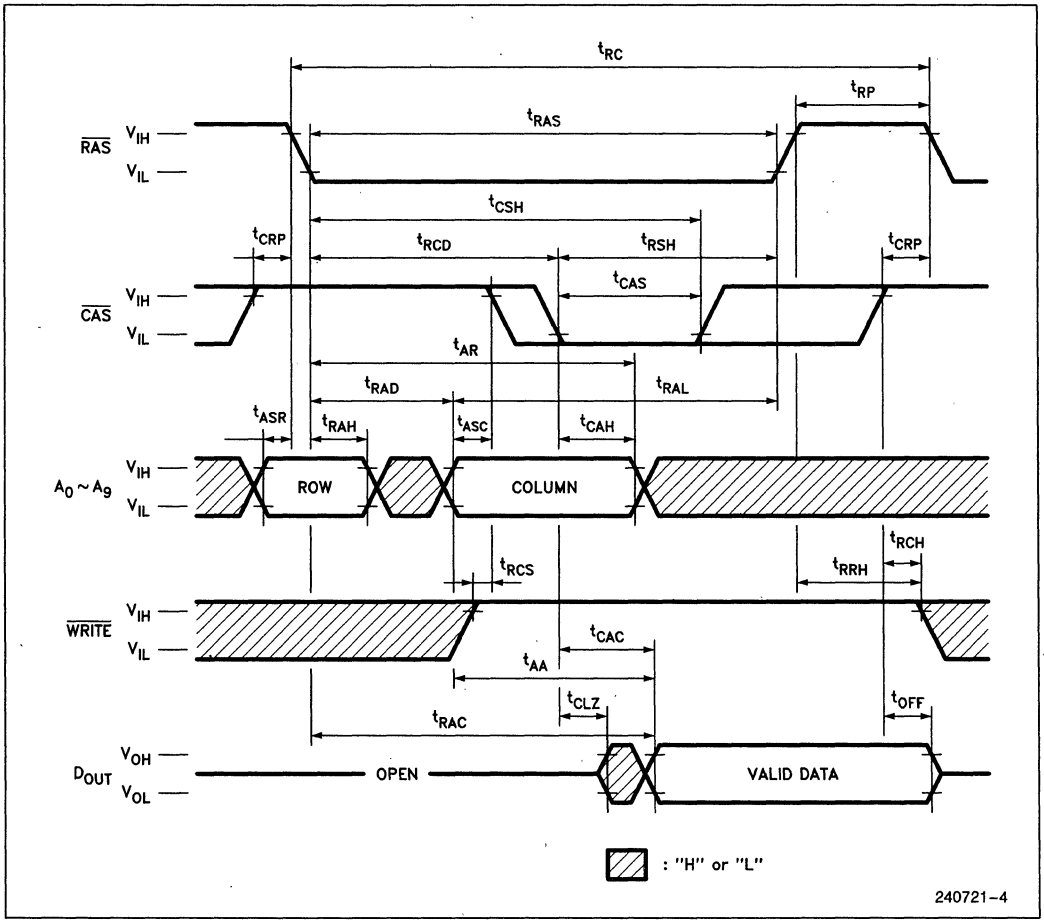
Symbol	Parameter	21019-06		21019-07		21019-08		21019-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	150		160		160		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	120		125		130	10K	160	10K	ns	
t_{DS}	Data Setup Time	0		0		0		0		ns	
t_{DH}	Data Hold Time after $\overline{CAS}$ Low	20		20		20		20		ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	20	10K	20	10K	25	10	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	60		70		80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		20		20		25		ns	
t_{WCS}	Write Setup Time before $\overline{CAS}$ Low	0		0		0		0		ns	13
t_{WCH}	Write Hold Time after $\overline{CAS}$ Low	15		15		15		20		ns	
t_{WP}	Write Pulse Width	15		15		15		20		ns	

FAST PAGE MODE CYCLE (Read, Early Write cycles)

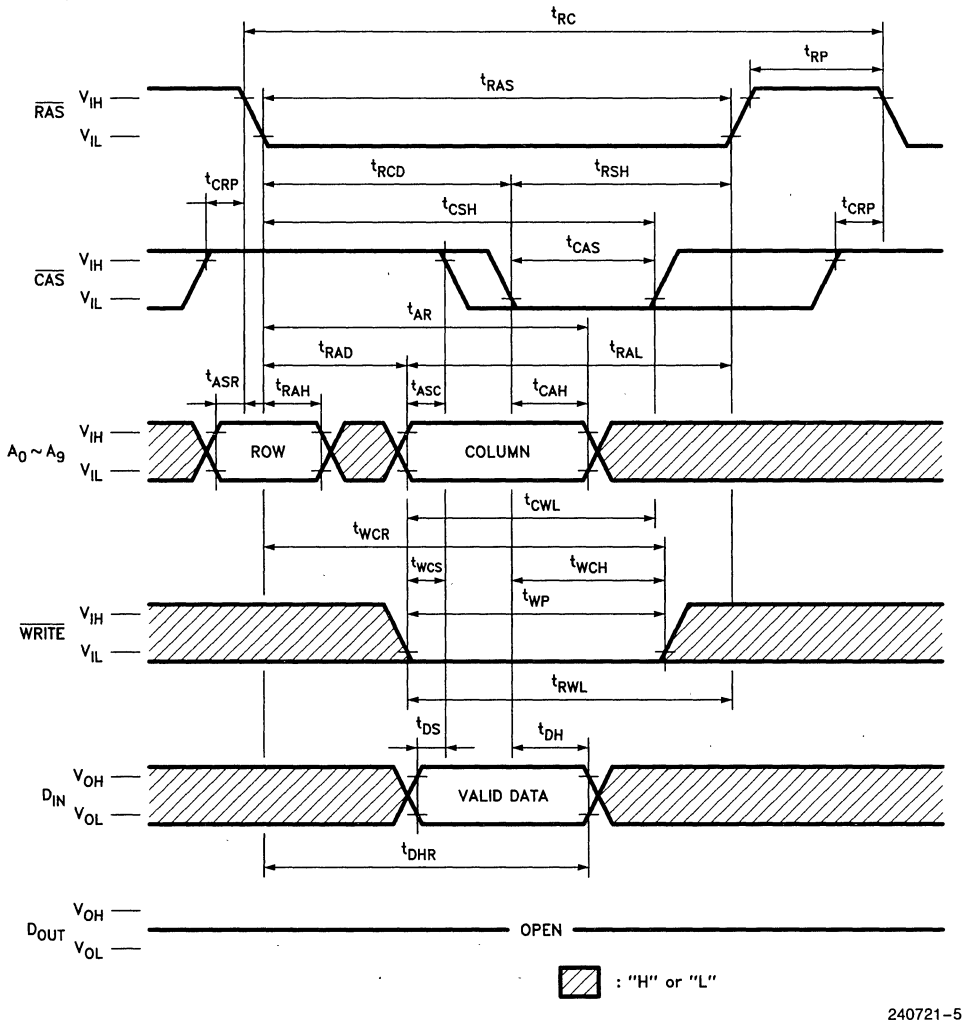
Symbol	Parameter	21019-06		21019-07		21019-08		21019-10		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45		50		50		60		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	120	10K	120	10K	130	10K	160	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width for Read Cycle	20	10K	20	10K	20	10K	25	10K	ns	
t_{CP}	$\overline{CAS}$ High Pulse Width	10	25	10	25	10	25	15	25	ns	

NOTES:
1. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. Characteristics assume $t_T = 5$ ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$(max), $t_{RAD} \geq t_{RAD}$(max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ + t_{ASC}(min).
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H").

READ CYCLE

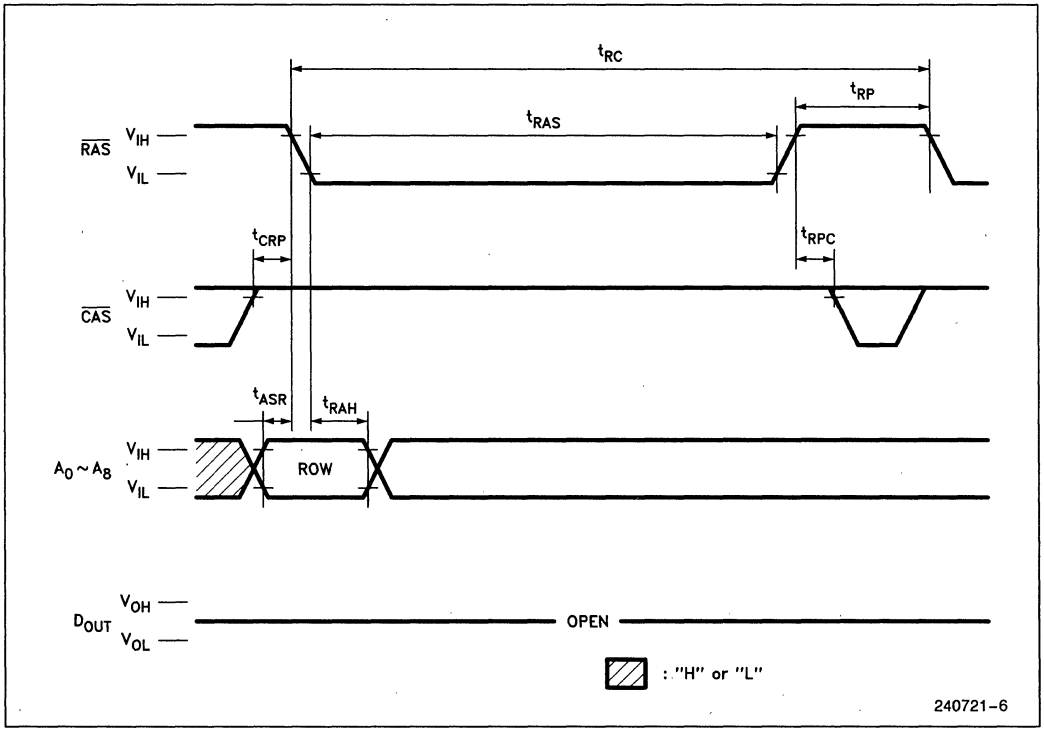

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0 ~ A9
VIH
VIL
ROW
COLUMN
tRCS
tRCH
tRRH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"
240721-4

EARLY WRITE CYCLE

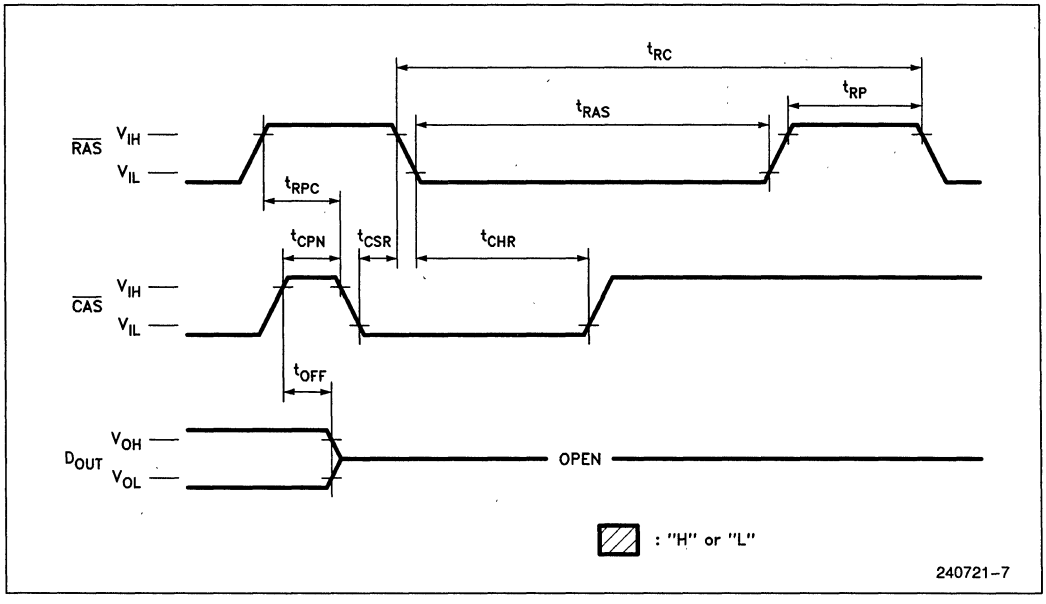


3

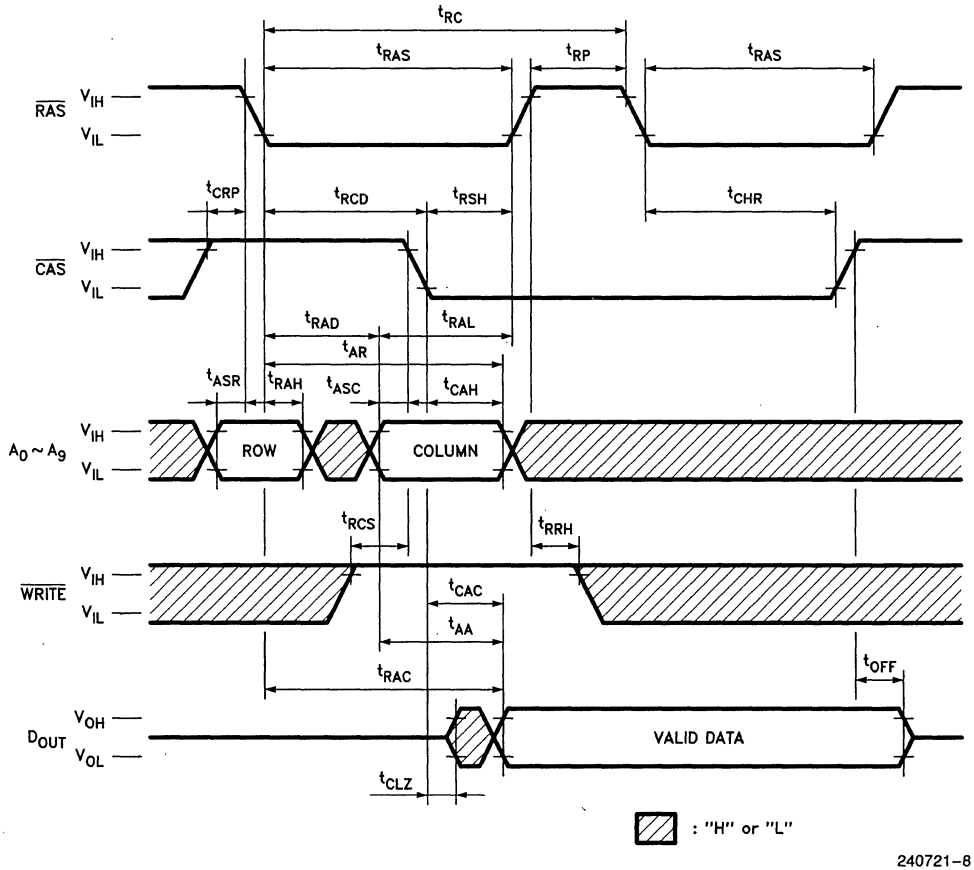
$\overline{RAS}$ ONLY REFRESH CYCLE



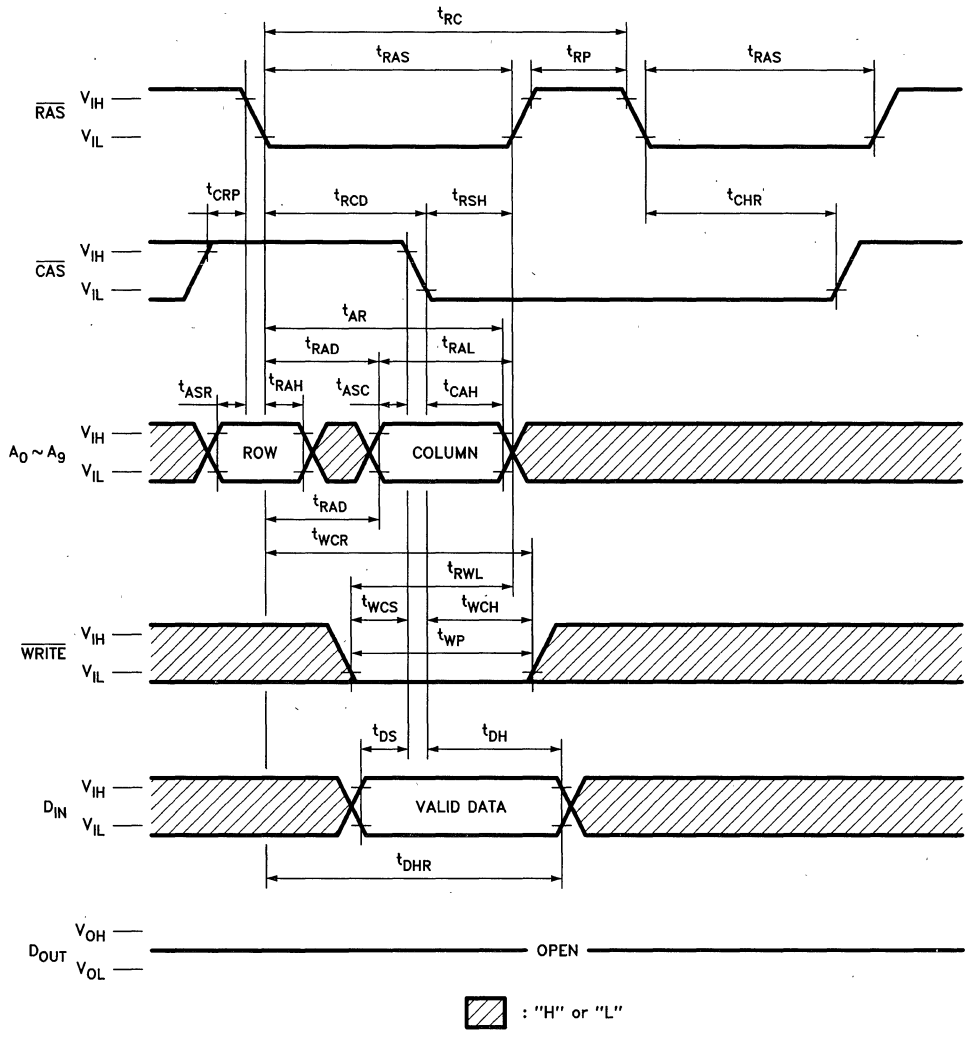
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



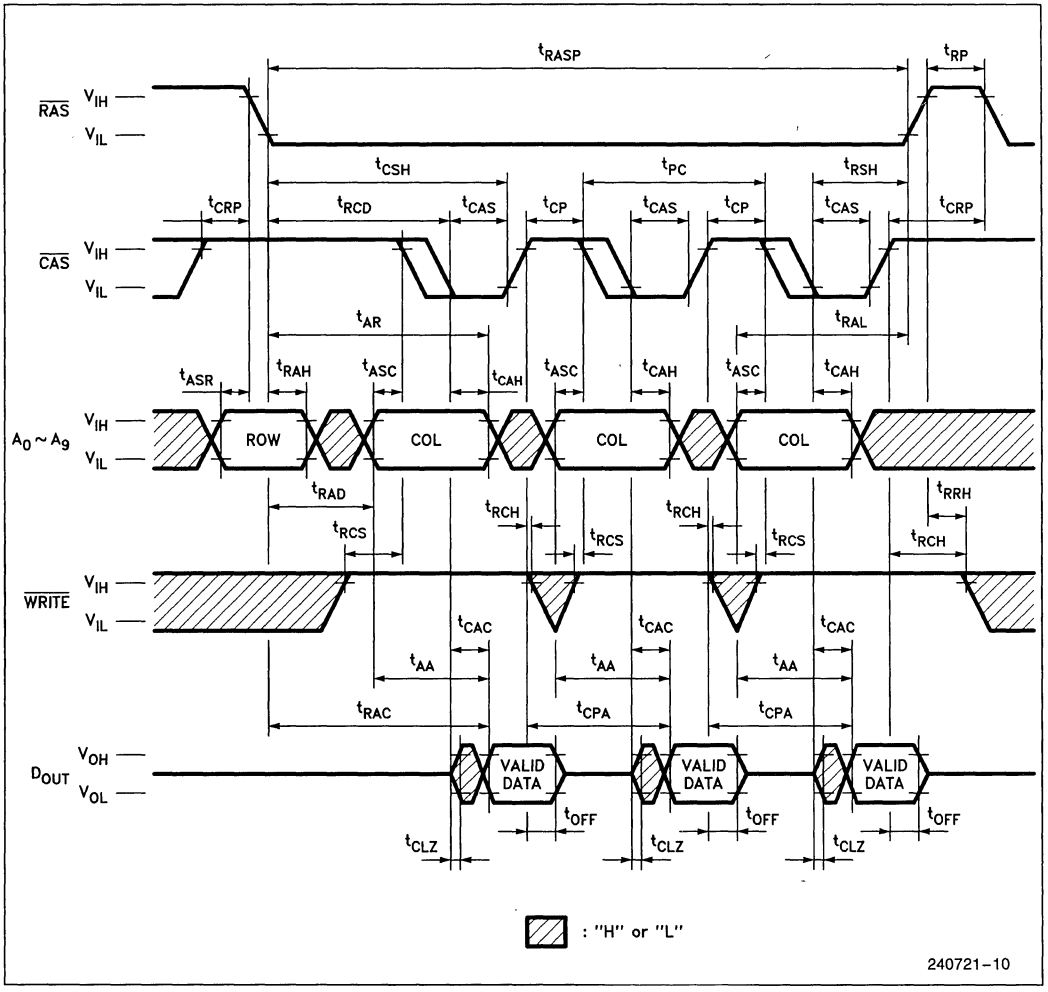
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

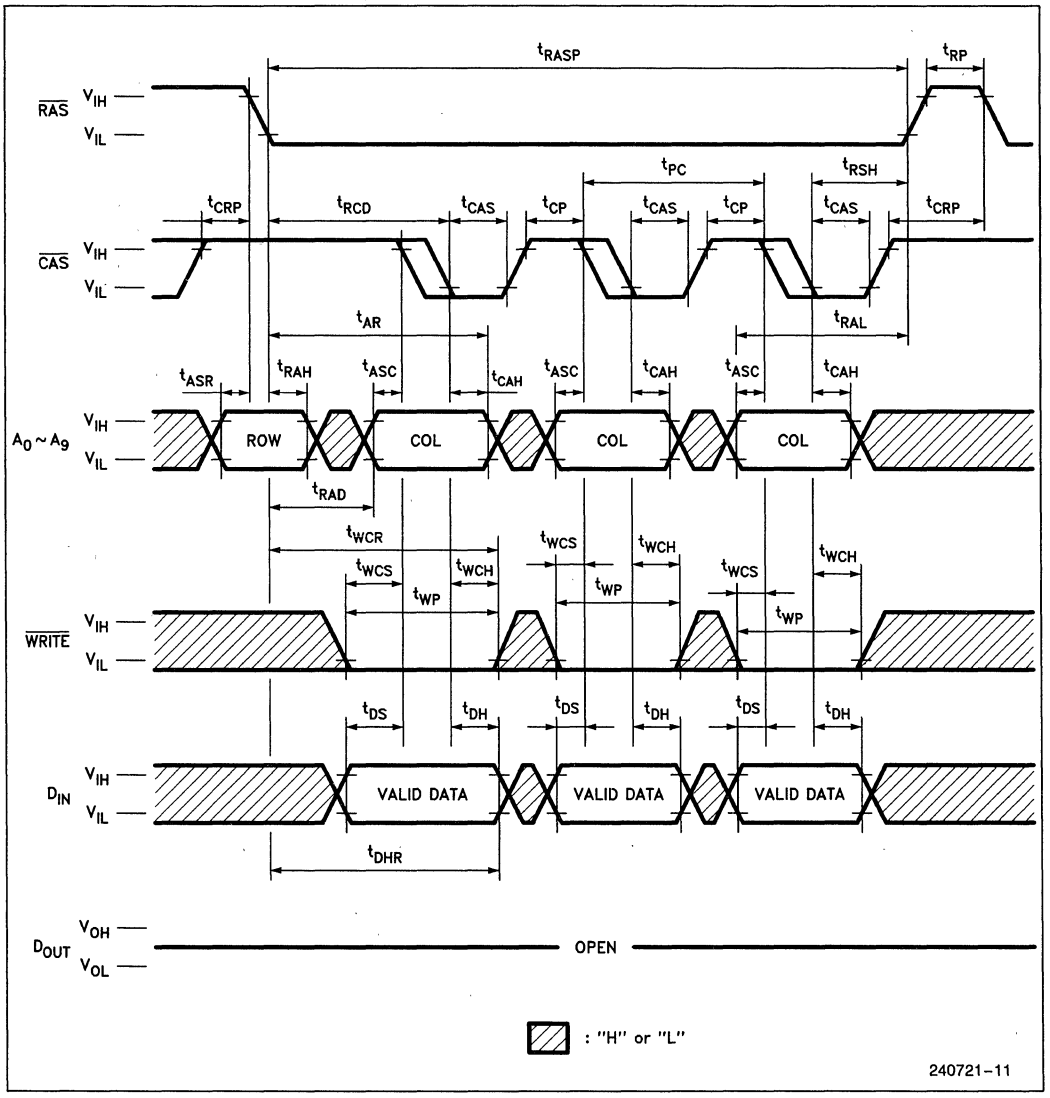


FAST PAGE MODE READ CYCLE

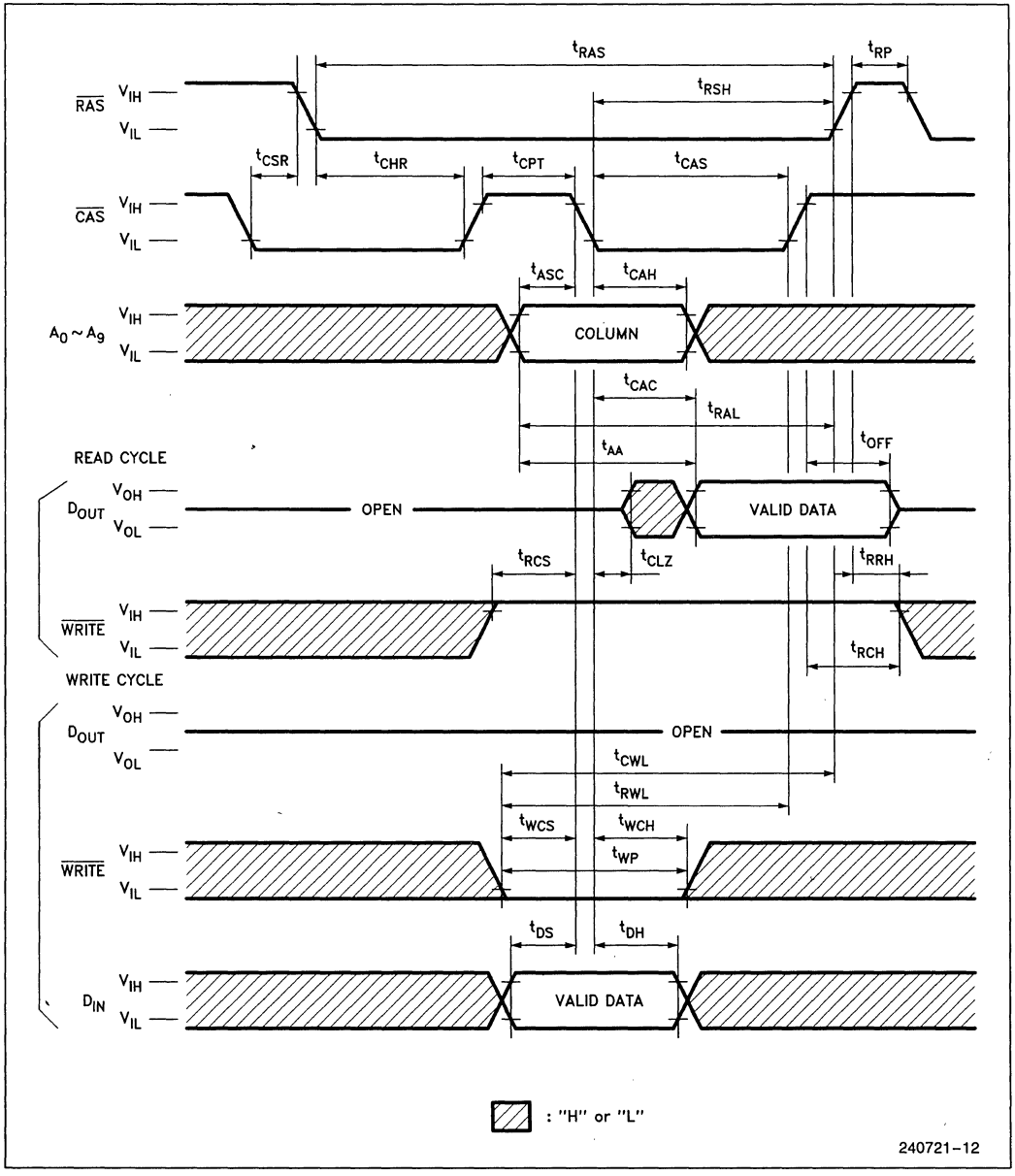


3

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



225636
256K x 36-BIT DYNAMIC RAM MEMORY MODULE WITH PAGE MODE

■ Performance Range

Parameters	225636-08	225636-10	Units
Access Time from $\overline{RAS}$ (t_{RAC})	80	100	ns
Access Time from $\overline{CAS}$ (t_{CAC})	20	25	ns
Read Cycle Time (t_{RC})	150	180	ns

- **256K x 36-Bit Organization**
- **Industry Standard Pin-Out in a 72-Pin Single In-Line Memory Module (SIMM)**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **512 Refresh Cycles every 8 ms**
- **Separate $\overline{CAS}$ Control for Each Nine Common Data-In and Data-Out Lines**
- **Fast Page Mode Operation**
- **TTL Compatible Inputs and Outputs**

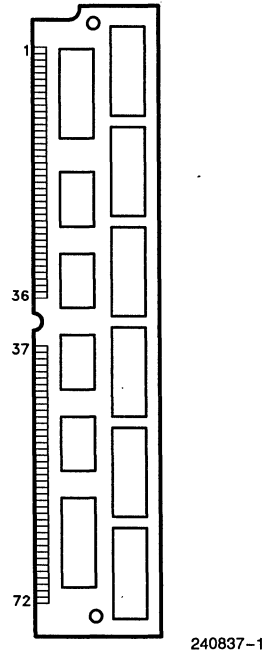
The 225636 is a 256K x 36-bit DRAM memory module consisting of Industry Standard CMOS 256K x 4-bit DRAMs and 256K x 1-bit DRAMs. The module contains eight 256K x 4-bit 20-pin SOJ packages and four 256K x 1-bit 18-pin PLCC packages. There are bypass capacitors on board on each module.

The 18 address bits are entered 9 bits at at time using $\overline{RAS}0$ or $\overline{RAS}2$ to latch the first 9 bits and $\overline{CAS}0$, $\overline{CAS}1$, $\overline{CAS}2$ or $\overline{CAS}3$ to control the latter 9 bits.

The common I/O feature requires the use of an early write cycle to prevent data contention on DQ lines.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	NC	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	NC	56	DQ_{30}
9	DQ_{21}	33	NC	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}2$	58	DQ_{31}
11	NC	35	DQ_{26}	59	V_{CC}
12	A_0	36	DQ_8	60	DQ_{32}
13	A_1	37	DQ_{17}	61	DQ_{14}
14	A_2	38	DQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}3$	66	NC
19	NC	43	$\overline{CAS}1$	67	PD1
20	DQ_4	44	$\overline{RAS}0$	68	PD2
21	DQ_{22}	45	NC	69	PD3
22	DQ_5	46	NC	70	PD4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}



240837-1

Figure 1. Pin Assignment

October 1990
Order Number: 240837-001

Pin Name	Pin Function
A_0–A_8	Address Inputs
DQ_0–DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}0$, $\overline{RAS}2$	Row Address Strobe
$\overline{CAS}0$–$\overline{CAS}3$	Column Address Strobe
PD1–PD4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins (Optional)

Pin	80 ns	100 ns
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	NC	V_{SS}
PD4	V_{SS}	V_{SS}

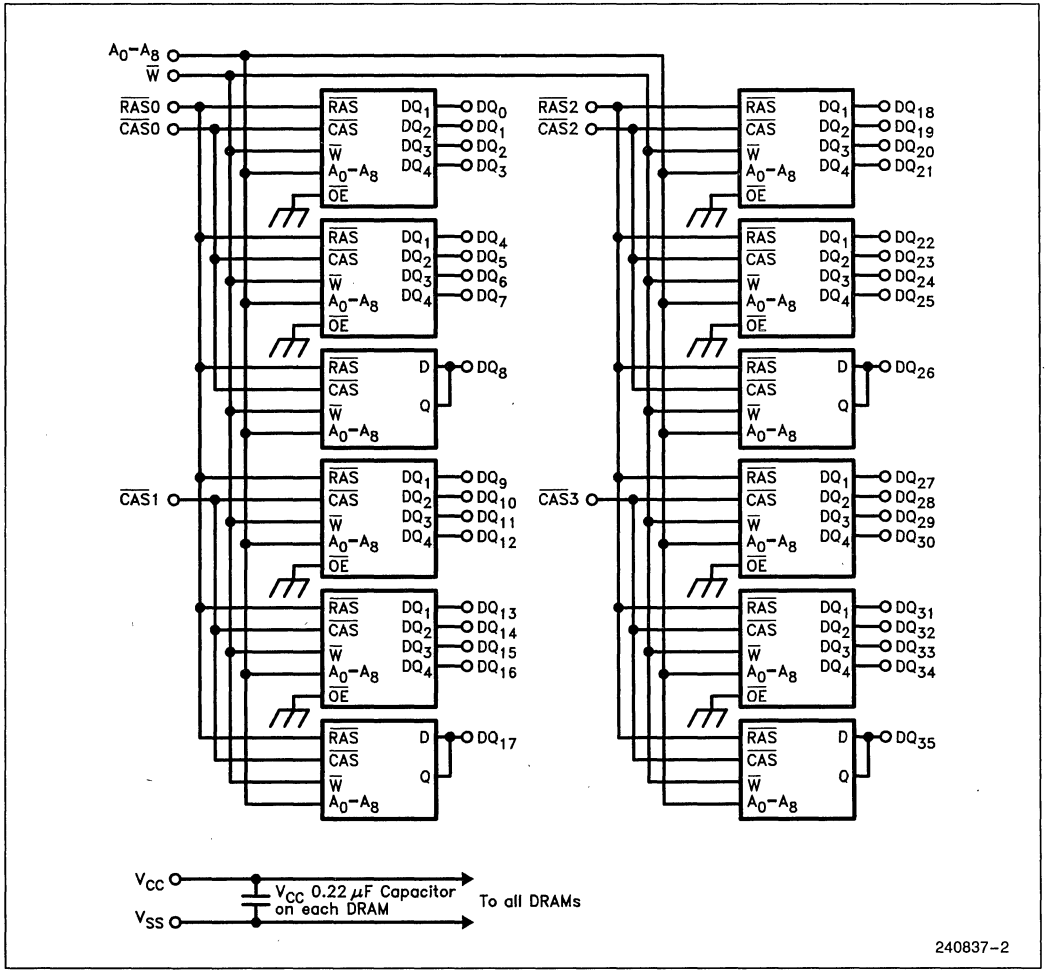


Figure 2. 256K x 36-Bit SIMM Block Diagram

PACKAGE DIMENSIONS

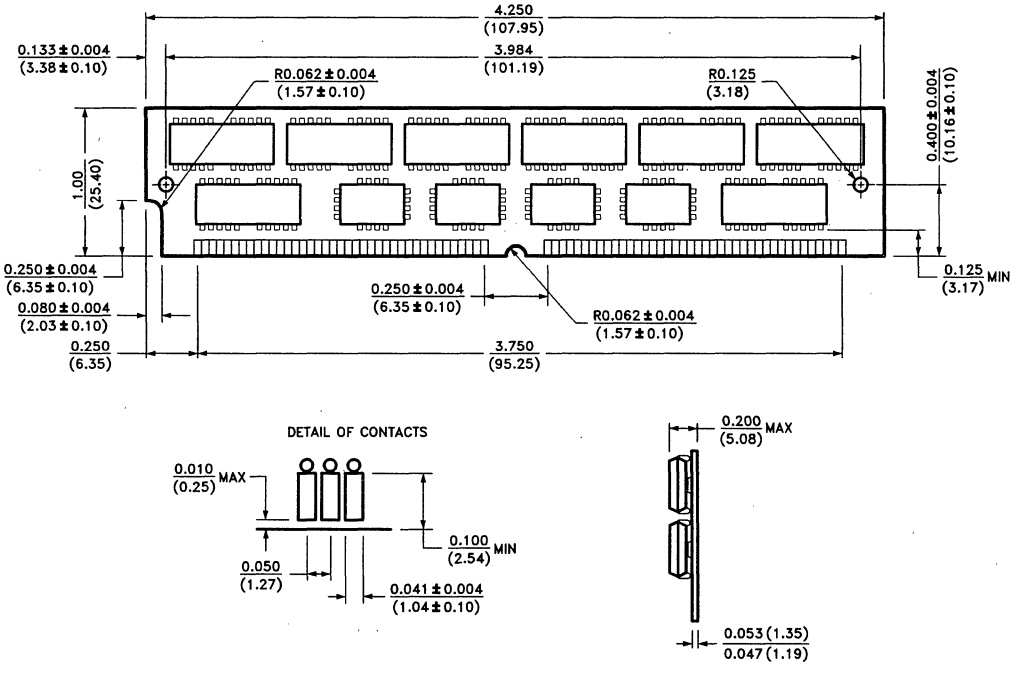


Figure 3. Outline Drawing

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V

Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V

Storage Temperature (T_{STG}) .... −55°C to +125°C

Soldering Temperature • Time (T_{solder}) ..... 260°C • 10 Sec

Power Dissipation (P_d) 9W

Short Circuit Output Current (I_{OUT}) ..... 50 mA

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS (Voltage Referenced to V_{SS}. T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

3

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_i (A)	Input Capacitance (A0–A9)		80	pF
C_{dq}	I/O Capacitance		20	pF
C_i ($\overline{W}$)	Input Capacitance, Write Control Input		94	pF
C_i ($\overline{RAS}$)	Input Capacitance, $\overline{RAS}$ Input		50	pF
C_i ($\overline{CAS}$)	Input Capacitance, $\overline{CAS}$ Input		40	pF
C_i ($\overline{CASP}$)	Input Capacitance, $\overline{CASP}$ Input		20	pF
C_i (DP)	Input Capacitance		15	pF
C_o (QP)	Output Capacitance		15	pF

D.C. AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter		Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 700	mA
I_{CC2}	Standby Current	$\overline{RAS} = \overline{CAS} = V_{IH}$			24	mA
		$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$			9	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 700	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC} = Min)		−08 −10		580 480	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 700	mA
I_{IL}	Input Current (Any Input $0 \leq V_{IN} \leq 6.5V$ All Other Pins = 0V)			−120	120	μA
I_{OZ}	Off State Output Current (Data Out is Disabled and $0 \leq V_{OUT} \leq 5.5V$)			−20	20	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)			2.4	V_{CC}	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0	0.4	V

NOTE:

I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

A.C. CHARACTERISTICS[1, 2] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	225636-08		225636-10		Units	Notes
		Min	Max	Min	Mas		
t_{RAC}	Access Time from $\overline{RAS}$		80		100	ns	4, 7
t_{CAC}	Acces Time from $\overline{CAS}$		20		25	ns	5, 7
t_{AA}	Access Time from Column Address		40		50	ns	6, 7
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		55	ns	7, 14
t_{CLZ}	Output Low Impedance Time from $\overline{CAS}$ Low	5		5		ns	7
t_{OFF}	Output Disable Time after $\overline{CAS}$ High	0	25	0	30	ns	
t_{REF}	Refresh Cycle Time		8		8	ms	
t_T	Transition Time	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ High Pulse Width	60		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	9, 10
t_{CPN}	$\overline{CAS}$ High Pulse Width	35		35		ns	
t_{RAD}	Column Addres Delay Time from $\overline{RAS}$ Low	20	40	20	50	ns	11
t_{ASR}	Row Address Setup Time before $\overline{RAS}$ Low	0		0		ns	
t_{ASC}	Column Address Time before $\overline{CAS}$ Low	0	20	0	20	ns	
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ LOW	15		15		ns	
t_{CAH}	Column Address Hold Time after $\overline{CAS}$ Low or $\overline{W}$ Low	20		20		ns	

3

A.C. CHARACTERISTICS[1, 2] (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ AND REFRESH CYCLES

Symbol	Parameter	225636-08		225636-10		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	150		180		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{RCS}	Read Setup Time before $\overline{CAS}$ Low	0		0		ns	
t_{RCH}	Read Hold Time after $\overline{CAS}$ High	0		0		ns	12
t_{RRH}	Read Hold Time after $\overline{RAS}$ High	0		0		ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Setup Time	40		50		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Symbol	Parameter	225636-08		225636-10		Units	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	30		30		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

A.C. CHARACTERISTICS (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

WRITE CYCLE (Early Write)

Symbol	Parameter	225636-08		225636-10		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	160		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	130	10K	160	10K	ns	
t_{DS}	Data Setup Time	0		0		ns	
t_{DH}	Data Hold Time after $\overline{CAS}$ Low	20		20		ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{WCS}	Write Setup Time before $\overline{CAS}$ Low	0		0		ns	13
t_{WCH}	Write Hold Time after $\overline{CAS}$ Low	20		20		ns	
t_{WP}	Write Pulse Width	15		20		ns	

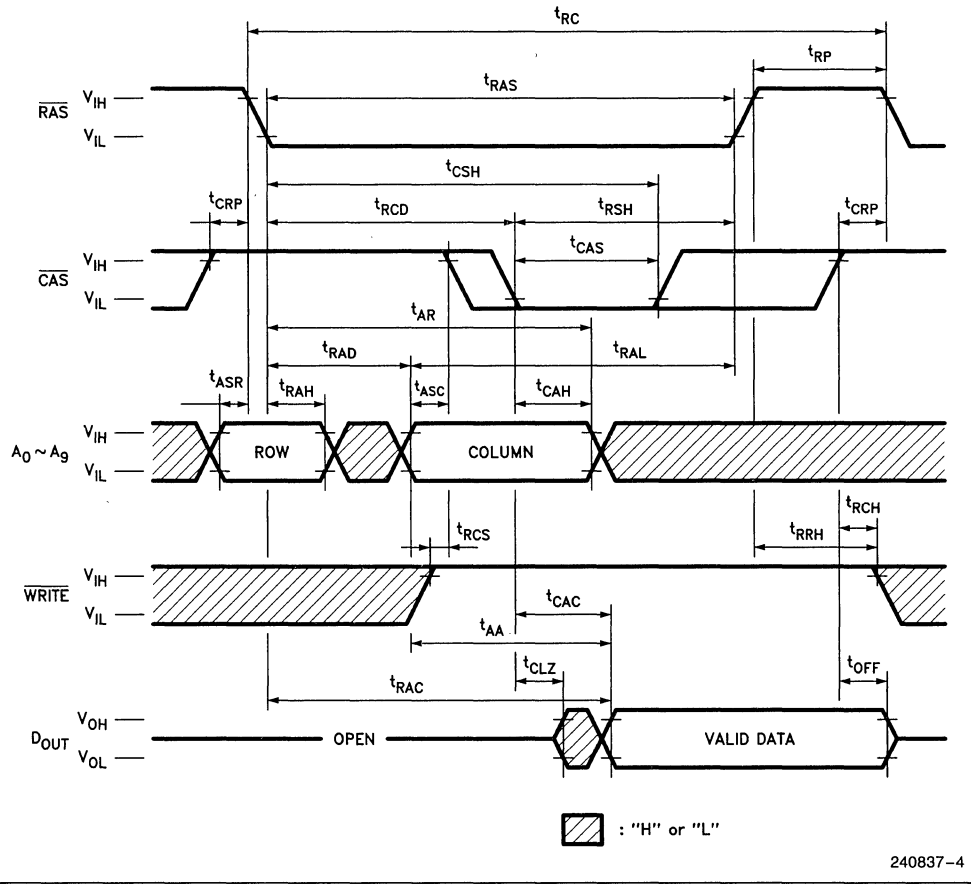
3

FAST PAGE MODE CYCLE (Read, Early Write cycles)

Symbol	Parameter	225636-08		225636-10		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50		60		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width for Read Cycle	20	10K	25	10K	ns	
t_{CP}	$\overline{CAS}$ High Pulse Width	10		15		ns	

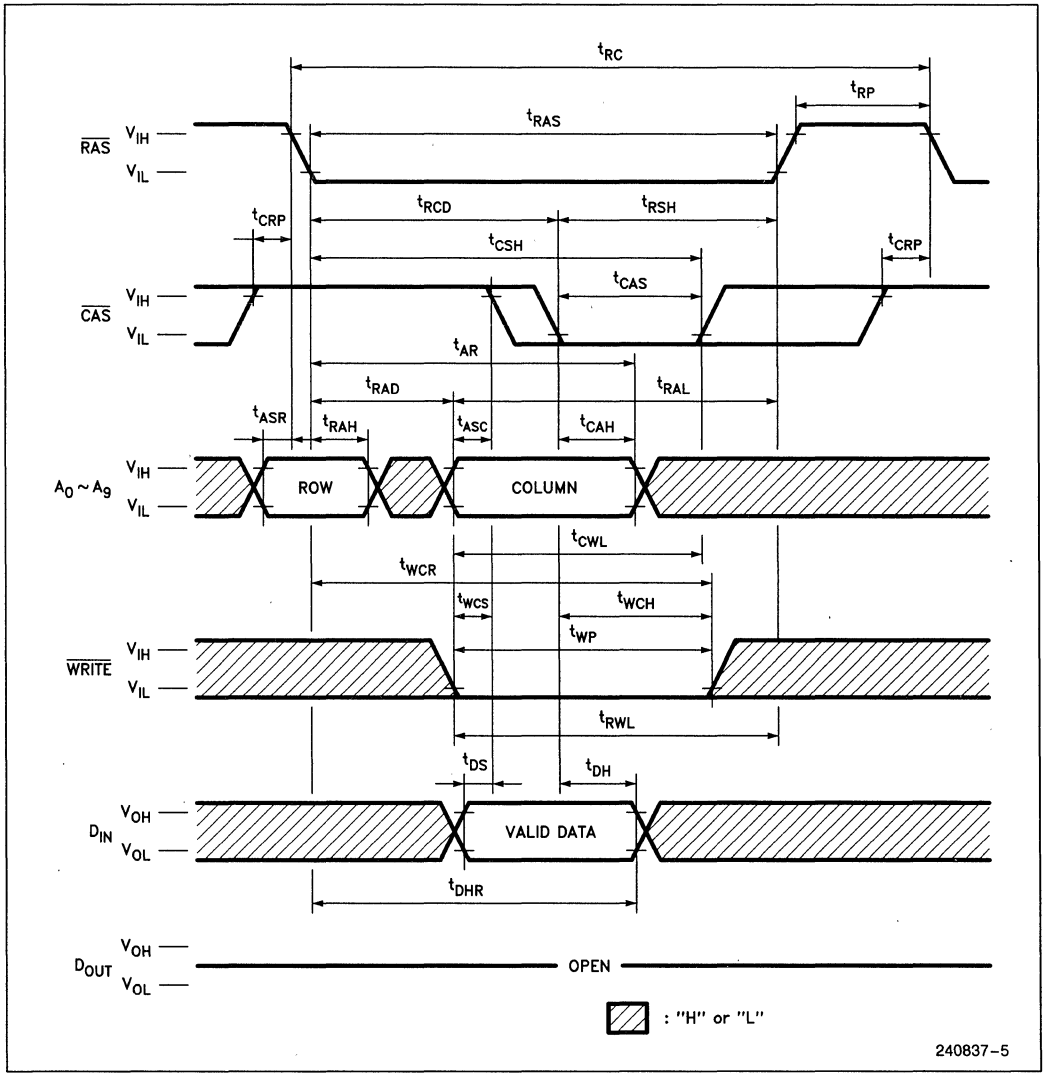
NOTES:
1. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. Characteristics assume $t_T = 5$ ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$(max), $t_{RAD} \geq t_{RAD}$(max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ + t_{ASC}(min).
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H").

READ CYCLE

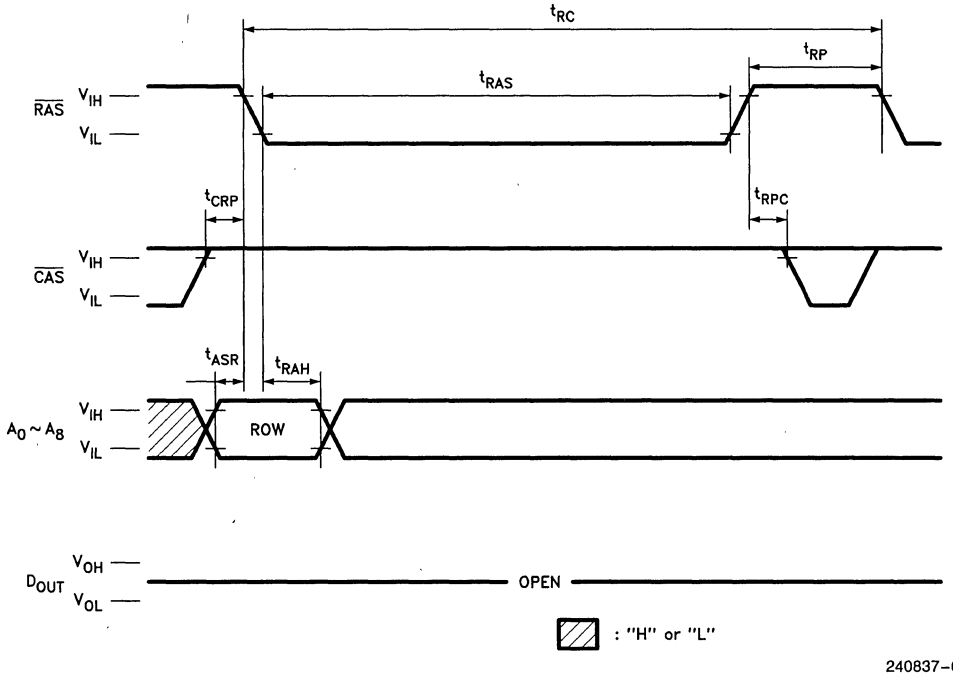

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0 ~ A9
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"
240837-4

3

EARLY WRITE CYCLE

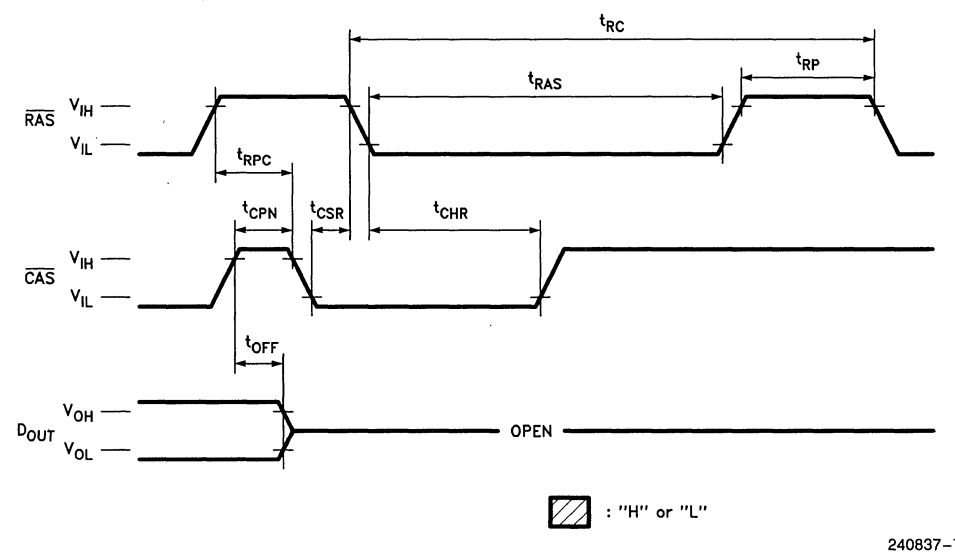


$\overline{RAS}$ ONLY REFRESH CYCLE



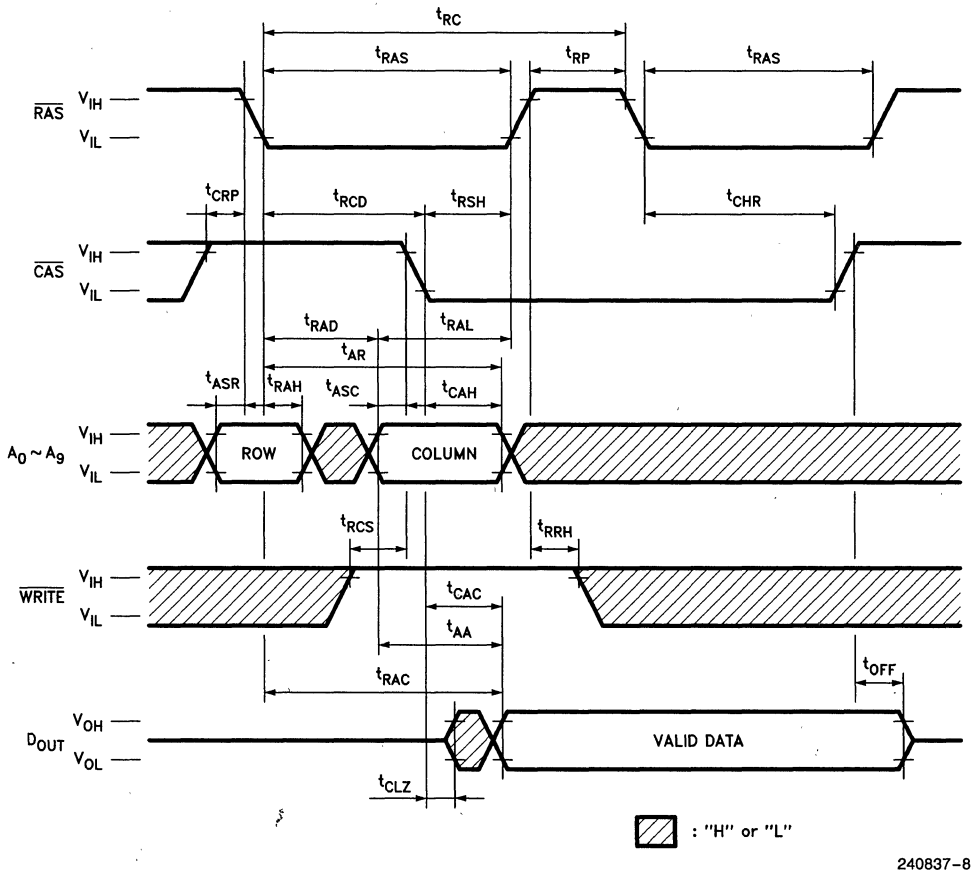
240837-6

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

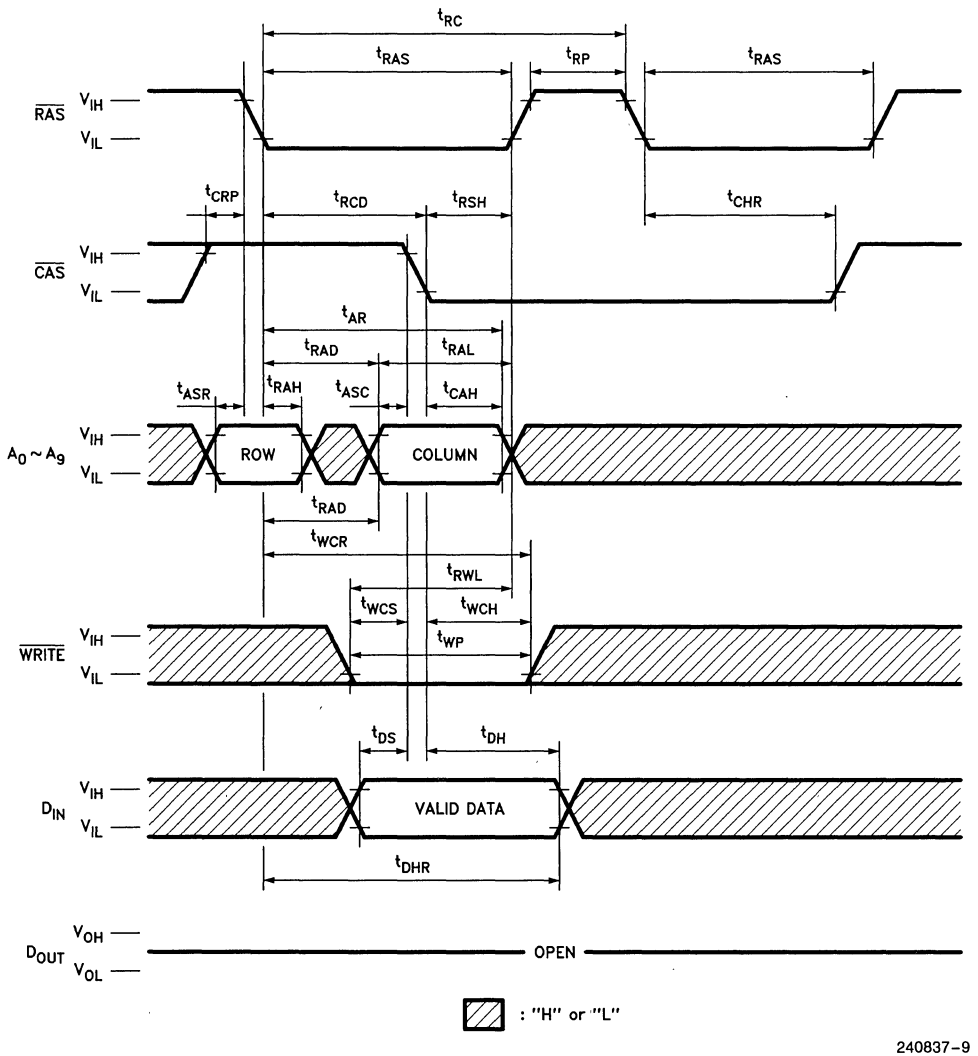


240837-7

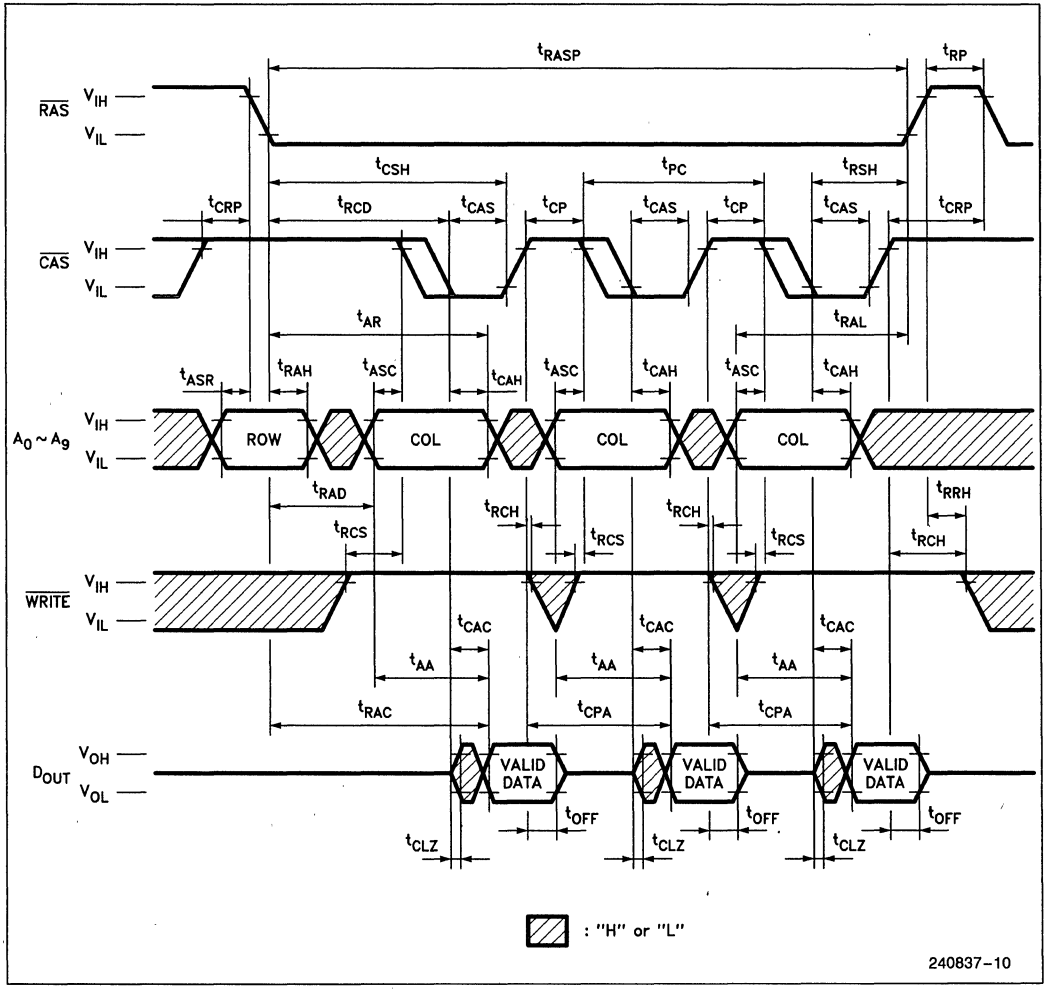
HIDDEN REFRESH CYCLE (READ)



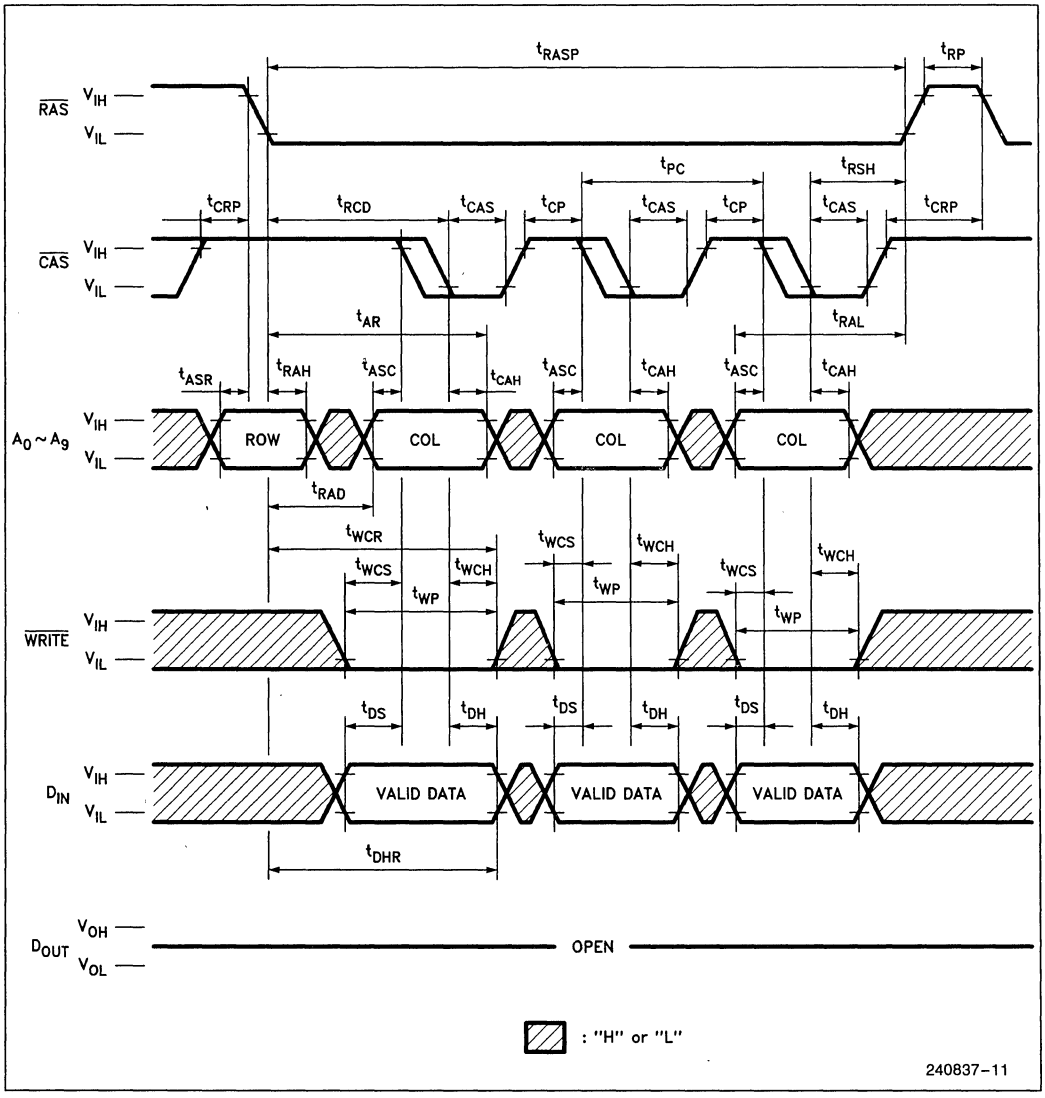
HIDDEN REFRESH CYCLE (WRITE)



FAST PAGE MODE READ CYCLE

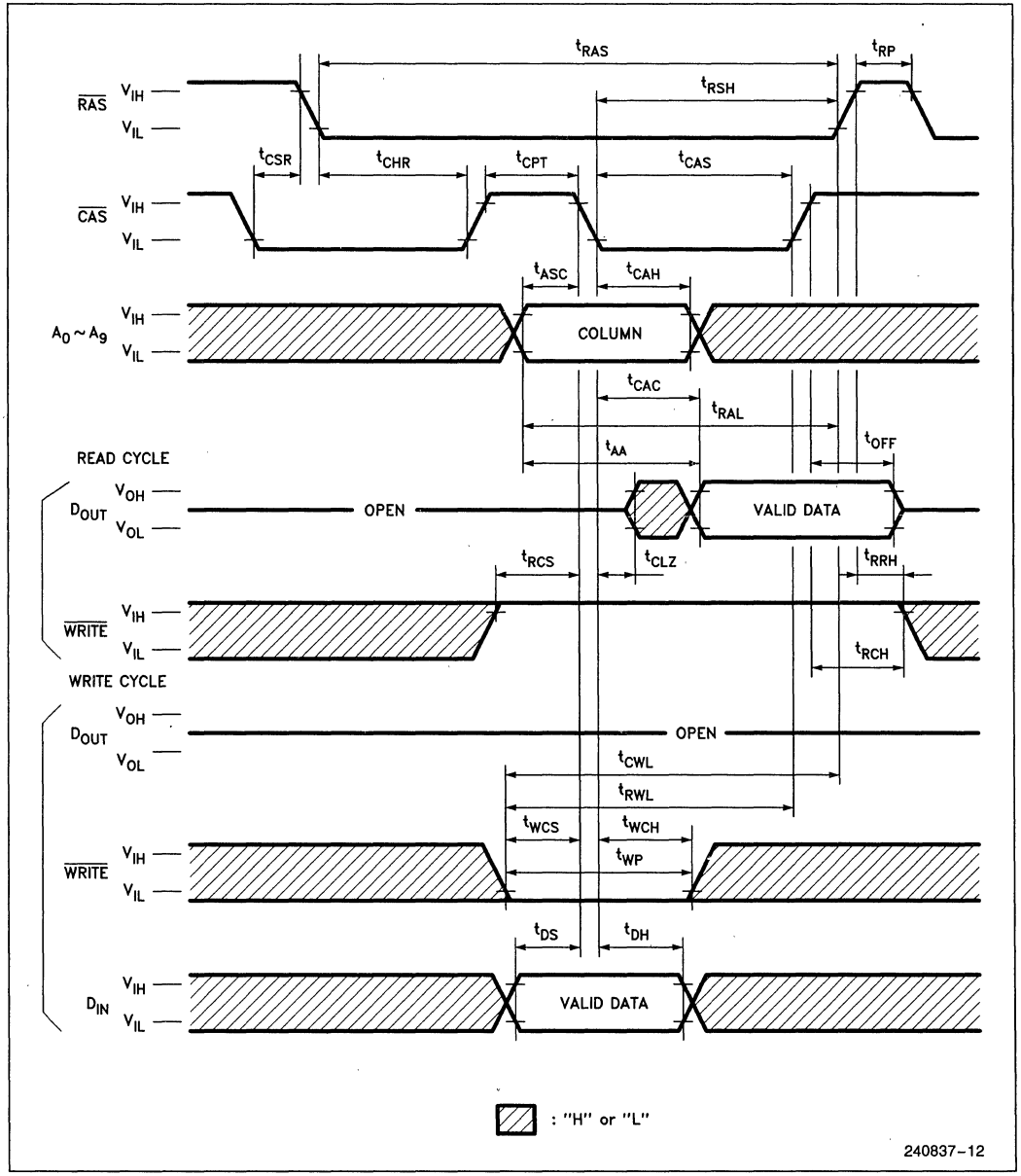


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



3

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



251236
512K x 36-BIT DYNAMIC RAM MEMORY MODULE WITH PAGE MODE

- **Performance Range**

Parameters	251236-08	251236-10	Units
Acces Time from $\overline{RAS}$ (t_{RAC})	80	100	ns
Access Time from $\overline{CAS}$ (t_{CAC})	20	25	ns
Read Cycle Time (t_{RC})	150	180	ns

- **512K x 36-Bit Organization**
- **Industry Standard Pin-Out in a 72-Pin Single In-Line Memory Module (SIMM)**
- **Common I/O Using "Early Write"**
- **Single 5V + 10% Power Supply**
- **Separate $\overline{CAS}$ Control for 4 Groups of 18 Common Data-In and Data-Out Lines**
- **512 Refresh Cycles every 4 ms**
- **Separate $\overline{CAS}$ ($\overline{CAS8}$) Control for One Separate Pair of Data-In and Data-Out Lines**
- **Separate RAS Control for 4 Groups of 18 Common Data-In and Data-Out Lines**
- **Fast Page Mode Operation**
- **TTL Compatible Inputs and Outputs**

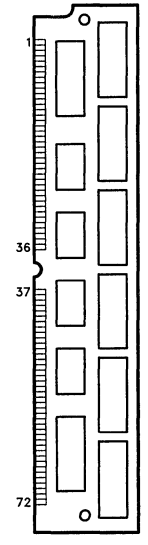
3

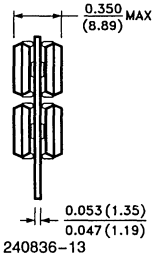
The 251236 is a 512K x 36-bit Dynamic RAM Memory Module consisting of industry standard CMOS, 256K x 4-bit DRAMs and 256K x 1-bit DRAMs. The module contains sixteen 256K x 4-bit in 20-pin plastic SOJ package and eight 256K x 1-bit in 18-pin PLCC. There are bypass capacitors on board each SIMM module.

The common I/O feature requires the use of an early write cycle to prevent data contention on DQ lines.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	NC	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	NC	56	DQ_{30}
9	DQ_{21}	33	NC	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS2}$	58	DQ_{31}
11	NC	35	DQ_{26}	59	V_{CC}
12	A_0	36	DQ_8	60	DQ_{32}
13	A_1	37	DQ_{17}	61	DQ_{14}
14	A_2	38	DQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS0}$	64	DQ_{34}
17	A_5	41	$\overline{CAS2}$	65	DQ_{16}
18	A_6	42	$\overline{CAS3}$	66	NC
19	NC	43	$\overline{CAS1}$	67	PD1
20	DQ_4	44	$\overline{RAS0}$	68	PD2
21	DQ_{22}	45	NC	69	PD3
22	DQ_5	46	NC	70	PD4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}





240836-13

NOTE:
Components are mounted on both sides of the board.

240836-12

Figure 1. Pin Assignment

October 1990
Order Number: 240836-001

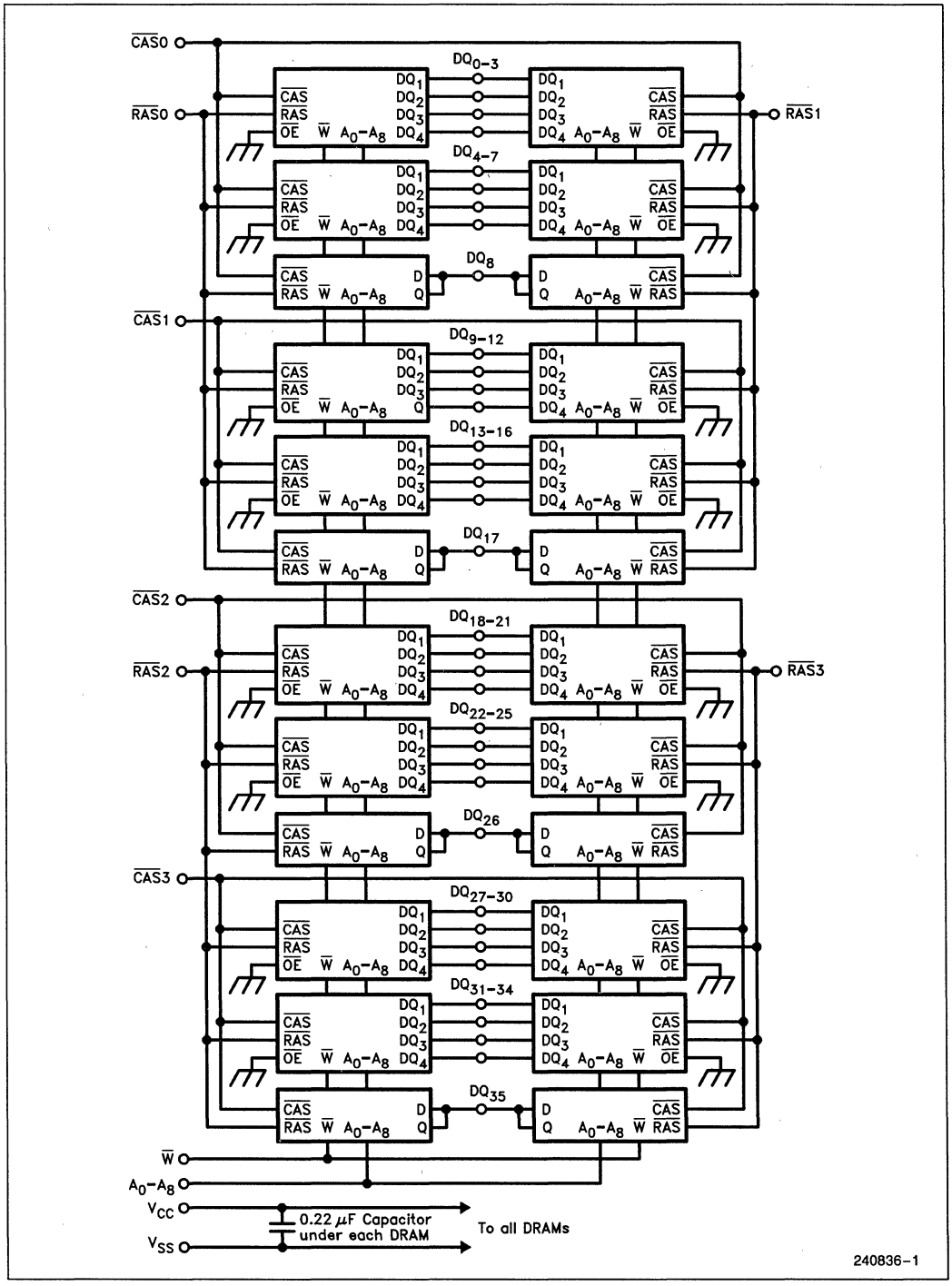


Figure 2. Block Diagram

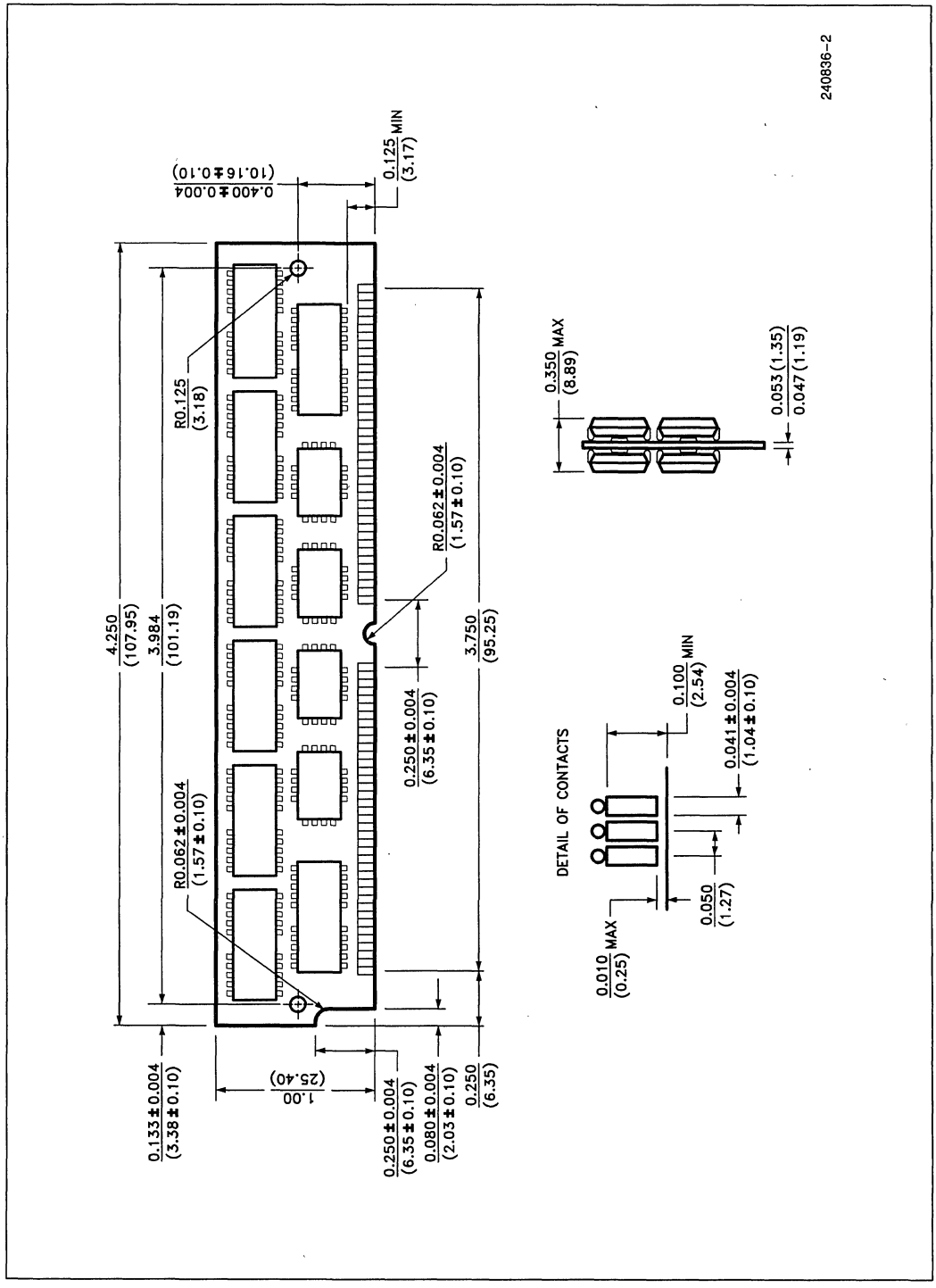


Figure 3. Outline Drawing

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (V_{IN}, V_{OUT}) ..... −1V to +7.0V

Voltage on Power Supply Relative to V_{SS} (V_{CC}) ..... −1V to +7.0V

Storage Temperature (T_{STG}) .... −55°C to +125°C

Soldering Temperature • Time (T_{solder}) ..... 260°C • 10 Sec

Power Dissipation (P_d) 9W

Short Circuit Output Current (I_{OUT}) ..... 50 mA

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS (Voltage Referenced to V_{SS}. T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_i (A)	Input Capacitance (A0–A9)		75	pF
C_{dq}	I/O Capacitance		20	pF
C_i ($\overline{W}$)	Input Capacitance, Write Control Input		94	pF
C_i ($\overline{RAS}$)	Input Capacitance, $\overline{RAS}$ Input		50	pF
C_i ($\overline{CAS}$)	Input Capacitance, $\overline{CAS}$ Input		40	pF
C_i ($\overline{CASP}$)	Input Capacitance, $\overline{CASP}$ Input		20	pF
C_i (DP)	Input Capacitance		15	pF
C_o (QP)	Output Capacitance		15	pF

D.C. AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter		Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 750	mA
I_{CC2}	Standby Current	$\overline{RAS} = \overline{CAS} = V_{IH}$			18	mA
		$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$			9	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 700	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC} = Min)		−08 −10		580 480	mA mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min)		−08 −10		820 700	mA
I_{IL}	Input Current (Any Input 0 ≤ V_{IN} ≤ 6.5V All Other Pins = 0V)			−120	120	μA
I_{OZ}	Off State Output Current (Data Out is Disabled and 0 ≤ V_{OUT} ≤ 5.5V)			−20	20	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5 mA)			2.4	V_{CC}	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)			0	0.4	V

NOTE:

I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

3

A.C. CHARACTERISTICS[1, 2] (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	251236-08		251236-10		Units	Notes
		Min	Max	Min	Mas		
t_{RAC}	Access Time from $\overline{RAS}$		80		100	ns	4, 7
t_{CAC}	Acces Time from $\overline{CAS}$		20		25	ns	5, 7
t_{CAA}	Access Time from Column Address		40		50	ns	6, 7
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		55	ns	7, 14
t_{CLZ}	Output Low Impedance Time from $\overline{CAS}$ Low	5		5		ns	7
t_{OFF}	Output Disable Time after $\overline{CAS}$ High	0	25	0	30	ns	
t_{REF}	Refresh Cycle Time		8		8	ms	
t_T	Transition Time	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ High Pulse Width	60		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		50		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	9, 10
t_{CPN}	$\overline{CAS}$ High Pulse Width	35		35		ns	
t_{RAD}	Column Addres Delay Time from $\overline{RAS}$ Low	20	40	20	50	ns	11
t_{ASR}	Row Address Setup Time before $\overline{RAS}$ Low	0		0		ns	
t_{ASC}	Column Address Time before $\overline{CAS}$ Low	0	20	0	20	ns	
t_{RAH}	Row Address Hold Time after $\overline{RAS}$ LOW	15		15		ns	
t_{CAH}	Column Address Hold Time after $\overline{CAS}$ Low or $\overline{W}$ Low	20		20		ns	

A.C. CHARACTERISTICS[1, 2] (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ AND REFRESH CYCLES

Symbol	Parameter	251236-08		251236-10		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	150		180		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{RCS}	Read Setup Time before $\overline{CAS}$ Low	0		0		ns	
t_{RCH}	Read Hold Time after $\overline{CAS}$ High	0		0		ns	12
t_{RRH}	Read Hold Time after $\overline{RAS}$ High	0		0		ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Setup Time	40		50		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Symbol	Parameter	251236-08		251236-10		Units	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	30		30		ns	
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	10		10		ns	

A.C. CHARACTERISTICS (Continued) (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

WRITE CYCLE (Early Write)

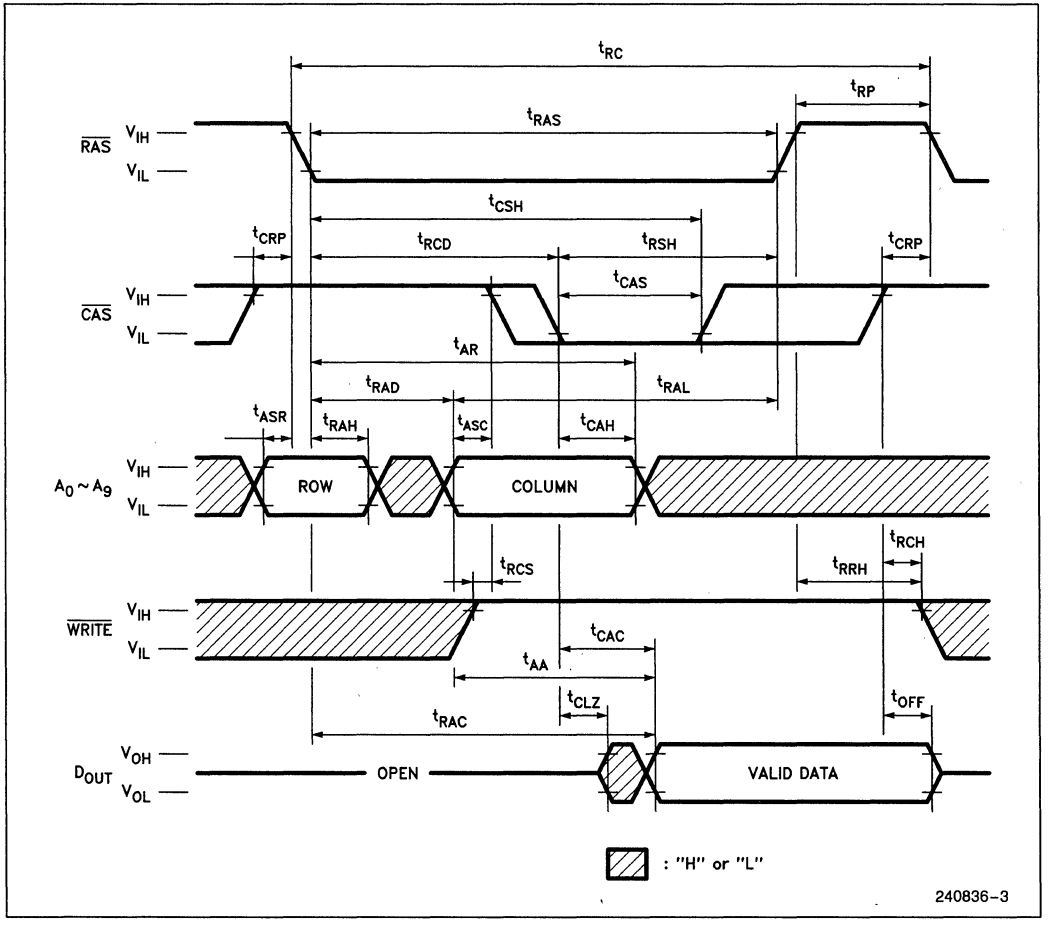
Symbol	Parameter	251236-08		251236-10		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	160		190		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width	130	10K	160	10K	ns	
t_{DS}	Data Setup Time	0		0		ns	
t_{DH}	Data Hold Time after $\overline{CAS}$ Low	20		20		ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time after $\overline{RAS}$ Low	80		100		ns	
t_{RSH}	$\overline{RAS}$ Hold Time after $\overline{CAS}$ Low	20		25		ns	
t_{WCS}	Write Setup Time before $\overline{CAS}$ Low	0		0		ns	13
t_{WCH}	Write Hold Time after $\overline{CAS}$ Low	20		20		ns	
t_{WP}	Write Pulse Width	15		20		ns	

FAST PAGE MODE CYCLE (Read, Early Write cycles)

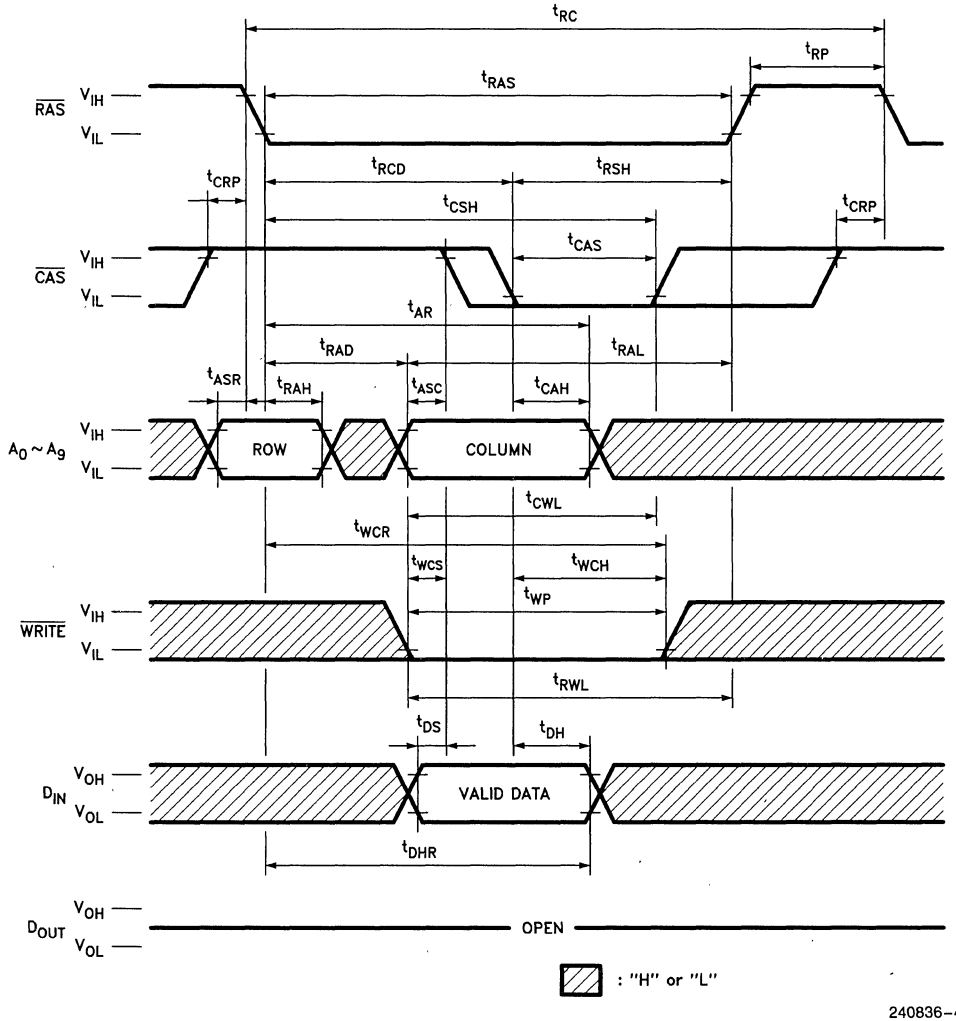
Symbol	Parameter	251236-08		251236-10		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50		60		ns	
t_{RAS}	$\overline{RAS}$ Low Pulse Width for Read, Write Cycle	80	10K	100	10K	ns	
t_{CAS}	$\overline{CAS}$ Low Pulse Width for Read Cycle	20	10K	25	10K	ns	
t_{CP}	$\overline{CAS}$ High Pulse Width	10	10	15	10	ns	

NOTES:
1. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. Characteristics assume $t_T = 5$ ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max), $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$(max), $t_{RAD} \geq t_{RAD}$(max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ + t_{ASC}(min).
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H").

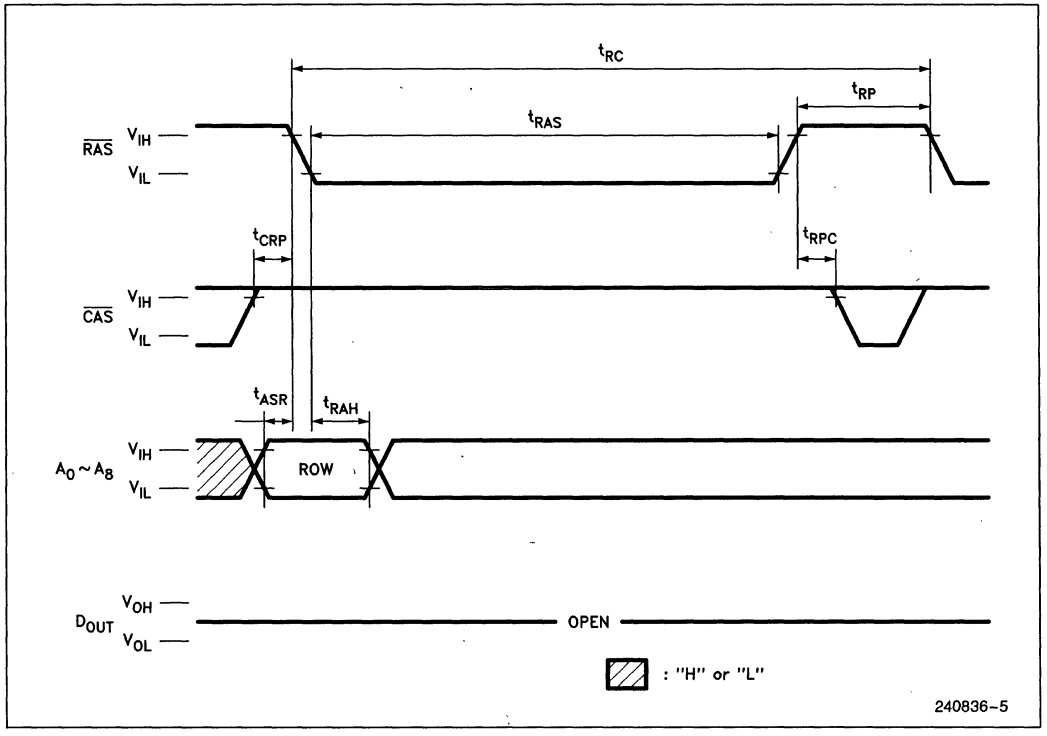
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0 ~ A9
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"
240836-3

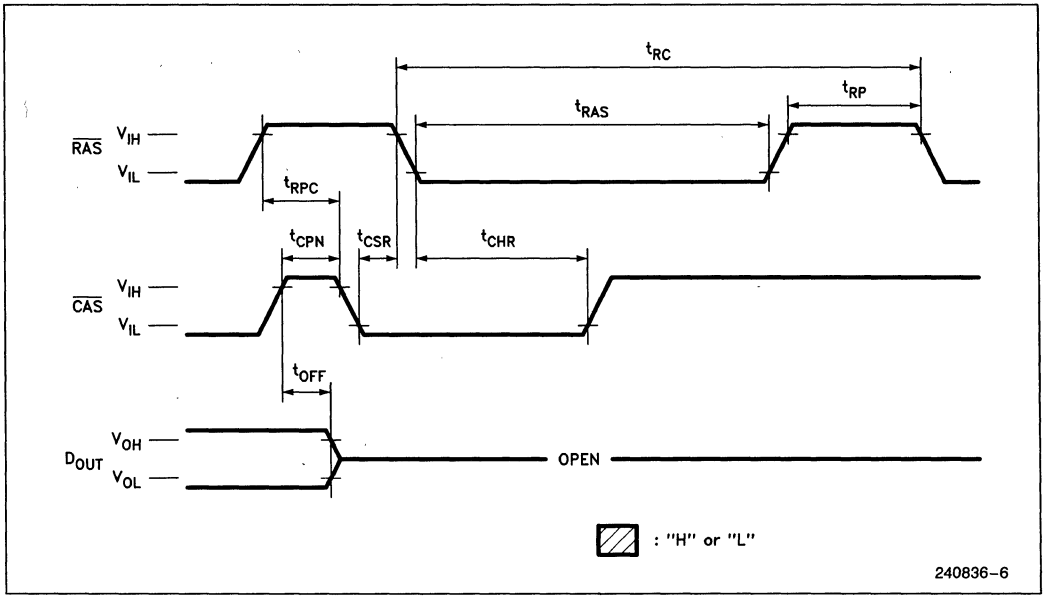
EARLY WRITE CYCLE



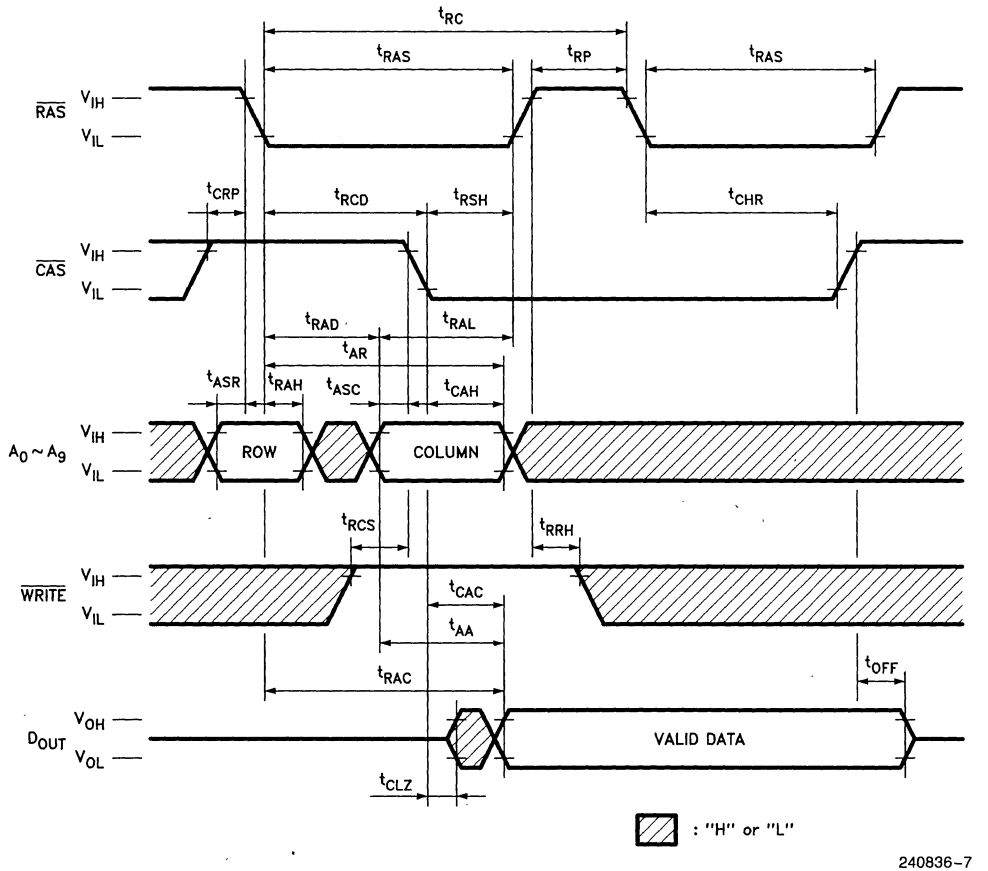
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

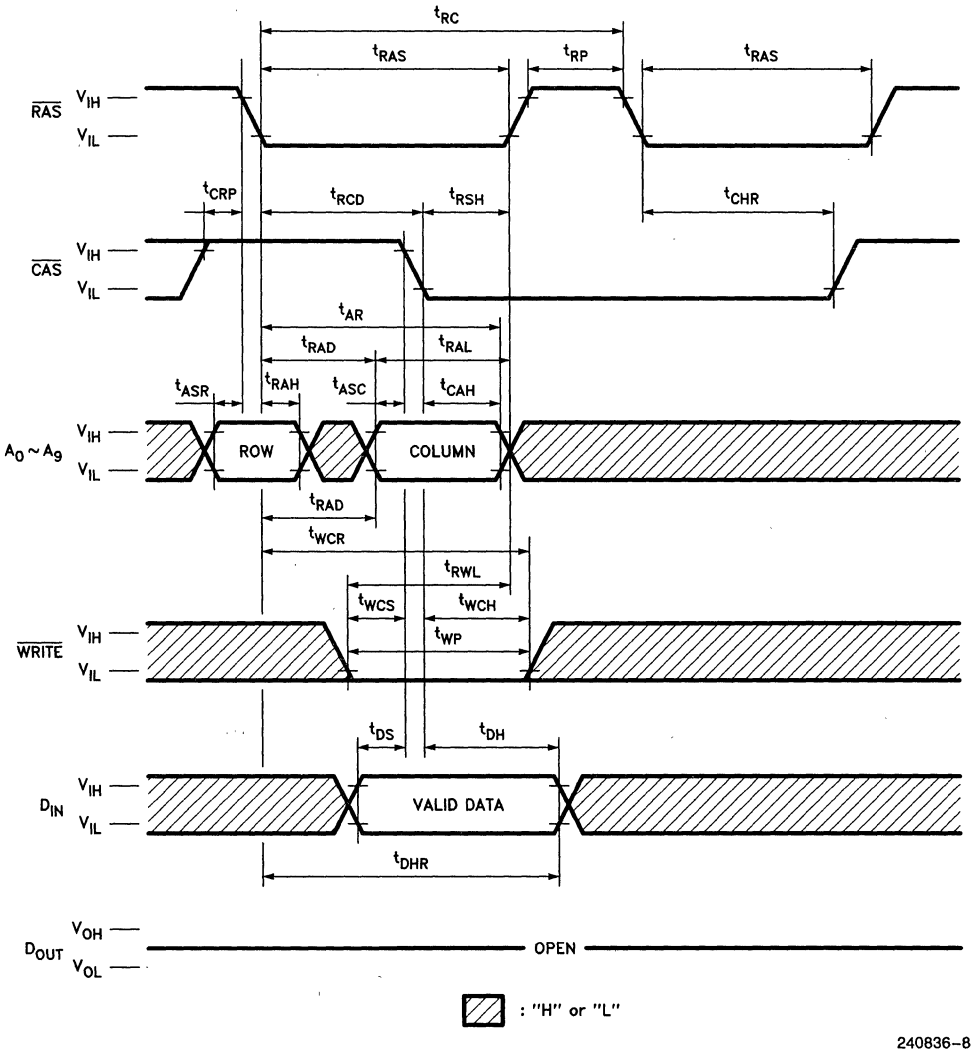


HIDDEN REFRESH CYCLE (READ)

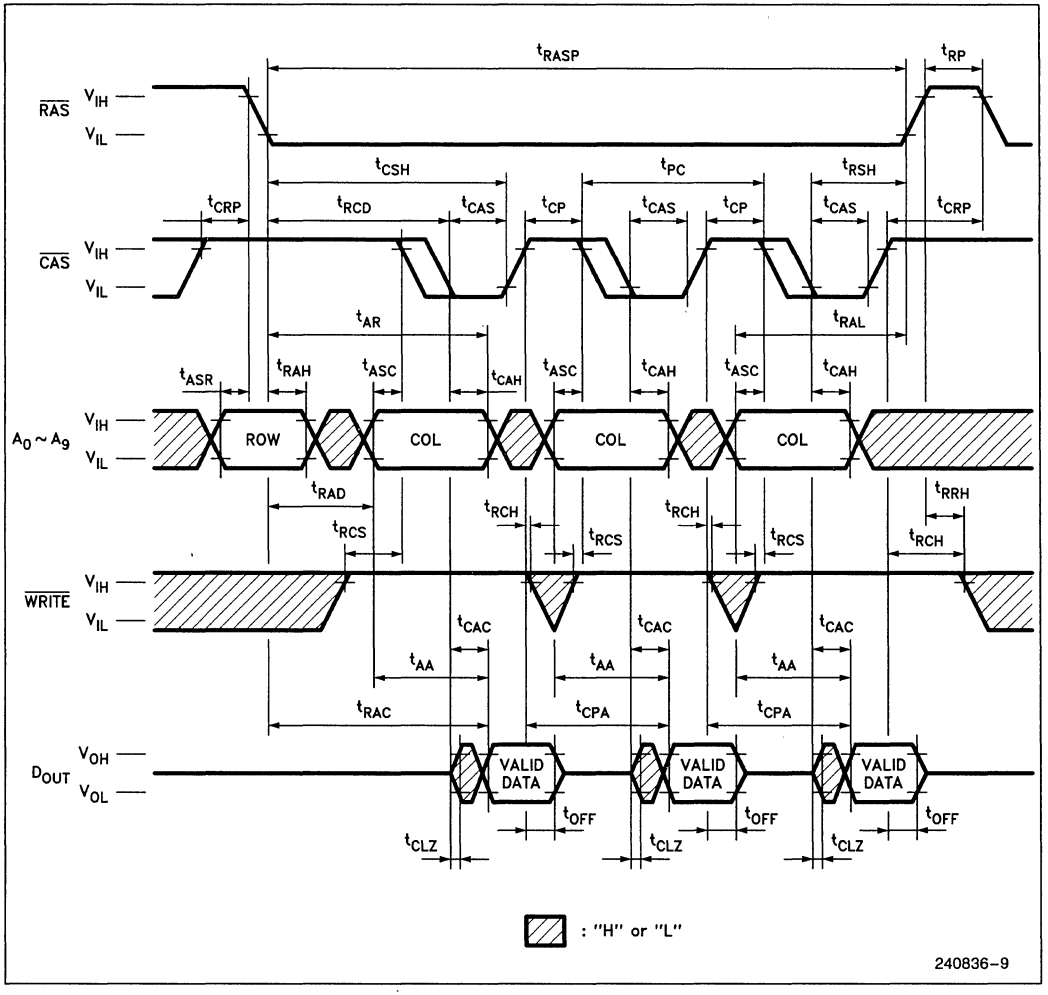


3

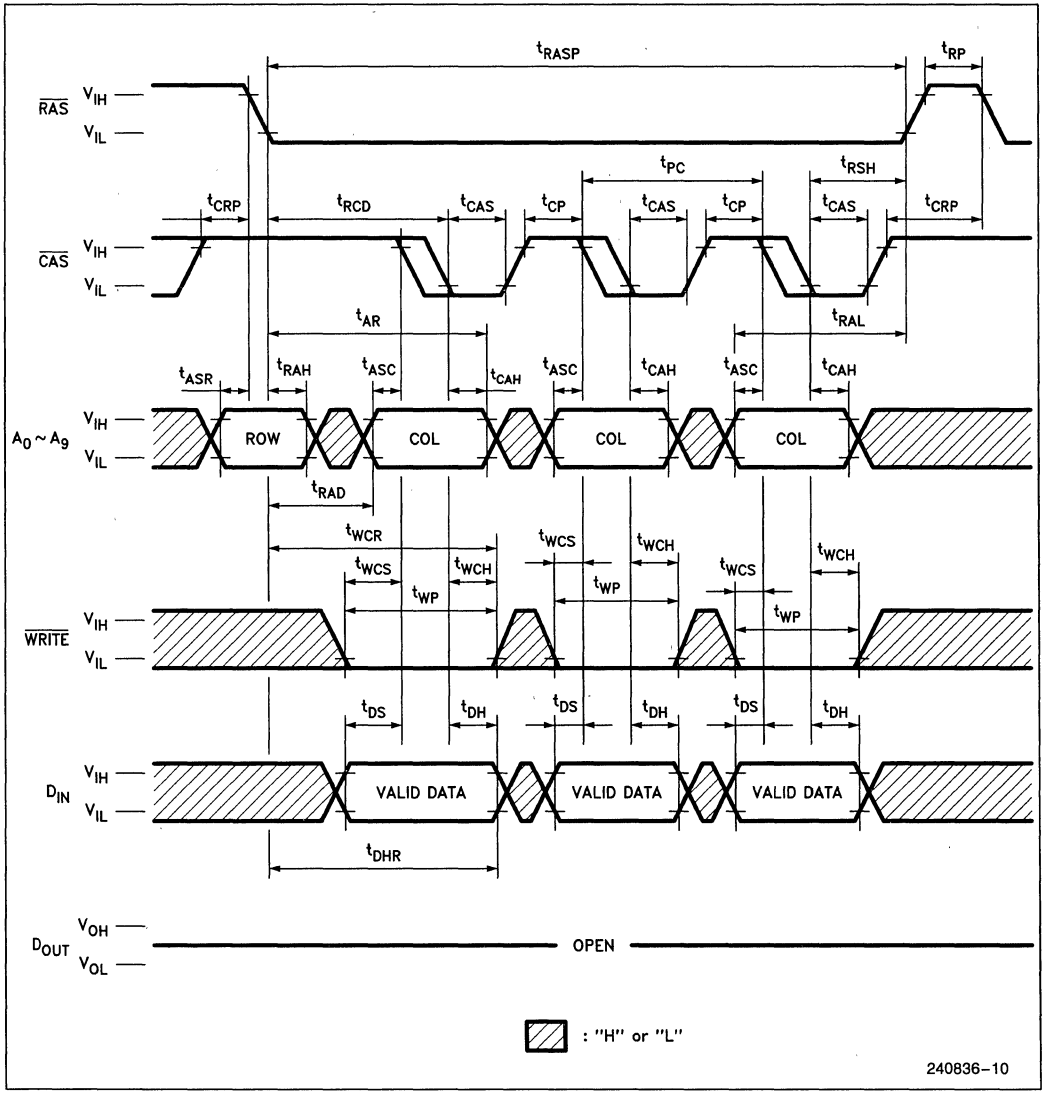
HIDDEN REFRESH CYCLE (WRITE)



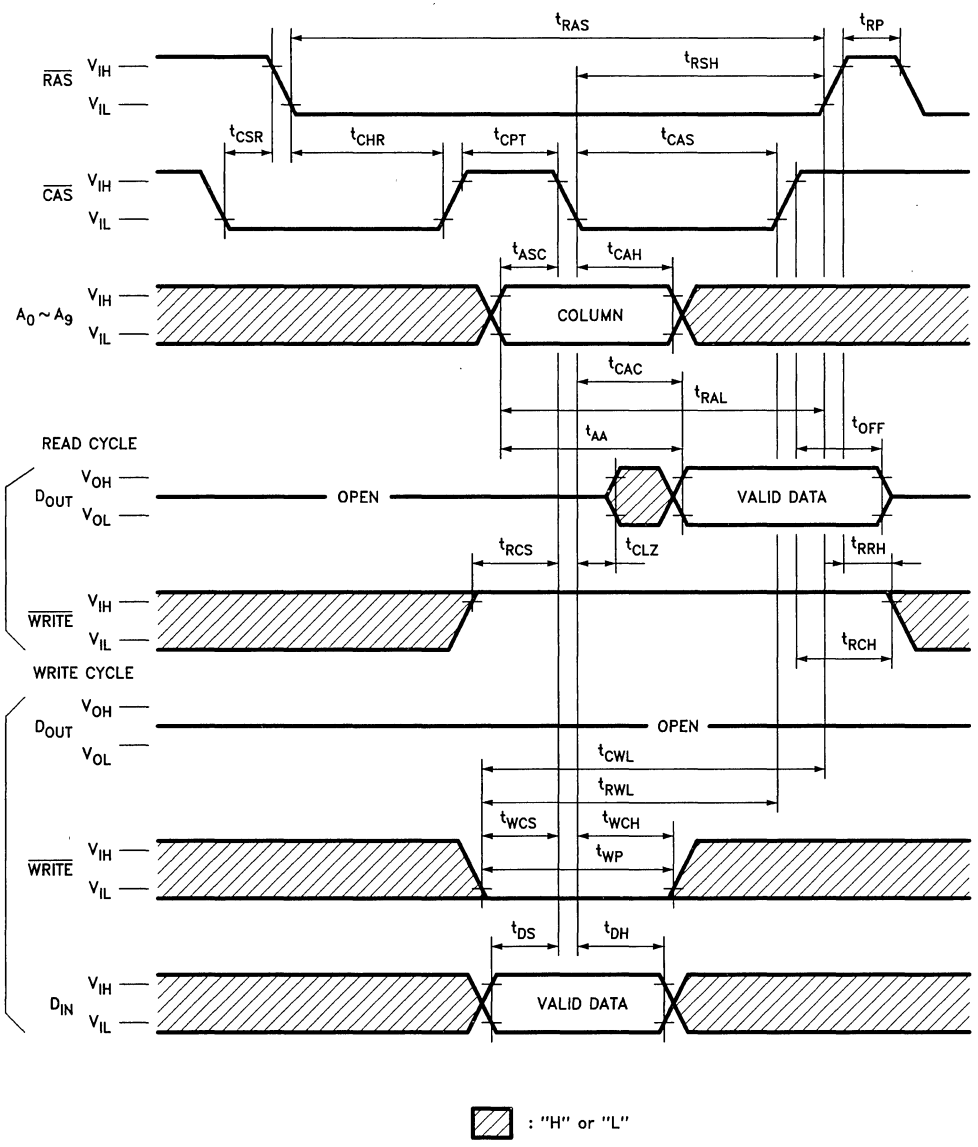
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



intel®

RELIABILITY REPORT

RR-62

September 1989

Dynamic RAM Reliability Report

MADHU NIMGAONKAR
COMPONENTS CONTRACTING DIVISION
QUALITY AND RELIABILITY ENGINEERING

Order Number: 240543-001

DRAM RELIABILITY DATA SUMMARY

CONTENTS

3

1.0 OVERVIEW

This reliability report is based on the combination of actual data from all Intel qualified and approved vendors. This data may vary from lot to lot and under different operating conditions encountered by the customer. Intel has published data sheet specifications that should be considered in evaluating the performance for specific application by the customer. This report does not give any assurance that the product is appropriate for any specific application as that decision is the responsibility of the customer.

Intel recognizes the need to monitor all contracted products to maintain and improve the level of quality and reliability consistent with internal goals and customer needs. This is achieved through continuous review of monitor data from all Intel qualified and approved vendors to acheive low defect levels.

2.0 RELIABILITY TESTS

High Temperature Dynamic Lifetest

This test is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures (125°C) and the use of biased operating conditions (5.5V). The translation from 125°C to 55°C is done by applying time acceleration factors based on the thermal activation energy assignments noted below. The time acceleration factors from 125°C to 55°C are: 3.42 for 0.3 eV, 7.67 for 0.5 eV and 58.96 for 1.0 eV, based on junction temperature offset for power dissipation.

Failure rate calculations are given for each relevant activation energy. These are made using the appropriate activation energy and the Arrhenius Plot as shown in Figure 1. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. The failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution to arrive at a confidence level associated failure rate. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV, 0.5 eV and 1.0 eV. In cases where the mechanism of the catastrophic failures cannot be determined, 0.3 eV activation energy is assumed.

When reviewing failure rate projections from different sources, it is important to understand the assumptions being made. Small changes in details can dramatically alter an estimated failure rate.

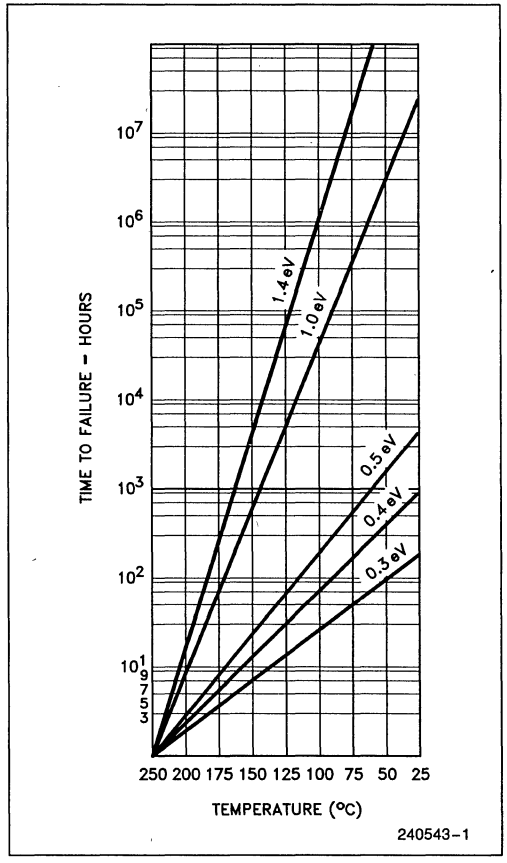


Figure 1. Arrhenius Plot

High Voltage (7V) Dynamic Lifetest

This test is performed to detect failure mechanisms which are accelerated by high voltage (7V) as well as high temperature (125°C). It is especially effective in accelerating oxide and leakage related failures. The total acceleration factor includes the time acceleration factors based on the assigned activation energies and voltage activation factor of 12.7 (7V to 5.5V).

High Temperature/Humidity Lifetest

This test is performed to evaluate moisture resistance characteristics of plastic encapsulated devices. A 1000–2000 hour test is performed under static bias conditions at 85°C/85% relative humidity with nominal voltages. In order to maximize metal corrosion conditions, the biasing configuration is either under low power or no power, with alternate pins biased at +5V or 0V.

Autoclave (Pressure Cooker) Test

This test is performed to identify the effects of high humidity and heat conditions on the die surface. Steam stressing accelerates moisture penetration through the plastic package material to the surface of the die, resulting in corrosion of metals.

High Temperature Storage Test

High temperature storage (bake) is a test in which devices are subjected to elevated temperature of 150°C with no bias. This test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability.

Temperature Cycle Test

This test consists of cycling the temperature of a chamber housing device from −65°C to +150°C with no applied bias. Temperature cycling (1000 cycles) is used to detect mechanical reliability problems and microcracks.

Electrostatic Discharge Test

This test is performed to identify device sensitivity to electrostatic discharge generated during system operation or device handling. All products incorporate ESD protection networks on the appropriate pins.

Soft Error Test (SER)

Soft error test is performed to identify the effects of alpha particles which are emitted in the radioactive decay of uranium and thorium present in packaging materials. Two methods commonly used to measure soft error rates are: 1) accelerated testing using alpha particle radiation source and 2) real time system level soft error testing.

3.0 PLASTIC RELIABILITY DATA SUMMARY

21256

Number of bits: 262,144
Organization: 256K x 1
Process: NMOS
Package: 16-Pin PDIP

Table 1. Reliability Data Summary

Year	125°C Dynamic Lifetest			7V Dynamic Lifetest		
	168 Hrs	500 Hrs	1000 Hrs	168 Hrs	500 Hrs	1000 Hrs
1988/89	3/11250	0/11247	2/11248	9/2400	5/2391	3/2386

Table 2. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours at 55°C	# Fail	Fail Rate %/1K Hours (60% UCL)
2E + 06 21E + 05	0.3 BI 0.3 VAF	30E + 06 95E + 06	5 17	
Total 0.3 eV Failures		=	22	0.0193 (**)
11E + 06	0.5	85E + 06	0	0.0012
11E + 06	1.0	643E + 06	0	0.0001
		Combined Failure Rate: FITs:		0.0206 206

**5.5V and 7V burn-in/lifetest equivalent hours have been combined.

				Thermal Accel. Factors 55°C
θJa	= 90°C/W (Est.)	BI/ELT	0.3 eV	3.42
V_{CC}	= 5.5V	Accel.	0.5 eV	7.67
I_{CC} @ 55°C	= 60 mA	Factors:	1.0 eV	58.96
I_{CC} @ 125°C	= 20 mA			
I_{CC} (max)	= 75 mA (Spec)	Voltage Accel. Factor (VAF): 12.7		

Temp. with Tja
T (55) = 358K
T (125) = 411K

K = 8.62E −05 eV/K

NOTE:
FIT = Failures in Time. 1 FIT = 1 Failure per 10E + 09 device hours.

Failure Analysis:
All failures assumed to be Oxide related.

Table 3. Additional Qualification Tests

Year	1000 Hours 85°C/85% R.H.	204 Hrs Steam	1000 Temp Cycles	150°C/1K Hrs High Temp Storage
1988/89	9/12552 (0.07%)	9/2002 (0.5%)	6/8120 (0.07%)	0/12200 (0.0%)

Table 4. System SER Results

V_{CC}	Cycle Time	Device Hours	# of Errors	FIT (60%)
5V	1 μs	1.4M	0	654

21464

Number of bits: 262,144
Organization: 64K x 4
Process: NMOS
Package: 18-Pin PDIP

Table 1. Reliability Data Summary

Year	125°C Dynamic Lifetest			7V Dynamic Lifetest		
	168 Hrs	500 Hrs	1000 Hrs	168 Hrs	500 Hrs	1000 Hrs
1988/89	3/11250	0/11247	2/11248	8/2370	3/2362	0/2359

Table 2. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours at 55°C	# Fail	Fail Rate %/1K Hours (60% UCL)
9E + 06 21E + 05	0.3 BI 0.3 VAF	30E + 06 91E + 06	5 11	
Total 0.3 eV Failures		=	16	0.0104 (**)
11E + 06	0.5	84E + 06	0	0.0012
11E + 06	1.0	645E + 06	0	0.0001
		Combined Failure Rate: FITs:		0.0117 117

**5.5V and 7V burn-in/lifetest equivalent hours have been combined.

				Thermal Accel. Factors 55°C
θJa	= 90°C/W (Est.)	BI/ELT	0.3 eV	3.42
V_{CC}	= 5.5V	Accel.	0.5 eV	7.67
I_{CC} @ 55°C	= 60 mA	Factors:	1.0 eV	58.96
I_{CC} @ 125°C	= 20 mA			
I_{CC} (max)	= 75 mA (Spec)	Voltage Accel. Factor (VAF): 12.7		
Temp. with T_{ja}				
T (55)	= 358K	K = 8.62E −05 eV/K		
T (125)	= 411K			

NOTE:
FIT = Failures in Time. 1 FIT = 1 Failure per 10E + 09 device hours.

Failure Analysis:
All failures assumed to be Oxide related.

Table 3. Additional Qualification Tests

Year	1000 Hours 85°C/85% R.H.	204 Hrs Steam	1000 Temp Cycles	150°C/1K Hrs High Temp Storage
1988/89	6/2310 (0.25%)	2/1320 (0.15%)	5/564 (0.6%)	1/1100 (0.10%)

Table 4. System SER Result

V_{CC}	Cycle Time	Device Hours	# of Errors	FIT (60%)
5V	1 μs	1.4M	0	630

21010

Number of bits: 1,048,576
Organization: 1M x 1
Process: CMOS
Package: 18-Pin PDIP

Table 1. Reliability Data Summary

Year	7V Dynamic Lifetest		
	168 Hrs	500 Hrs	1000 Hrs
1988/89	7/2060	4/2053	4/2049

Table 2. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours at 55°C	# Fail	Fail Rate %/1K Hours (60% UCL)
19E + 05	0.3	82E + 06	15	0.0204
19E + 05	0.5	15E + 06	0	0.0070
19E + 05	1.0	112E + 06	0	0.0009
			Combined Failure Rate:	0.0283
			FITs:	283

				Thermal Accel. Factors 55°C
θJa	= 90°C/W (Est.)	BI/ELT	0.3 eV	3.42
V_{CC}	= 5.5V	Accel.	0.5 eV	7.67
I_{CC} @ 55°C	= 60 mA	Factors:	1.0 eV	58.96
I_{CC} @ 125°C	= 20 mA			
I_{CC} (max)	= 75 mA (Spec)	Voltage Accel. Factor (VAF): 12.7		

Temp. with Tja
T (55) = 358K
T (125) = 411K

K = 8.62E −05 eV/K

NOTE:
FIT = Failures in Time. 1 FIT = 1 Failure per 10E + 09 device hours.

Failure Analysis:
All failures assumed to be Oxide related.

Table 3. Additional Qualification Tests

Year	1000 Hours 85°C/85% R.H.	204 Hrs Steam	1000 Temp Cycles	150°C/1K Hrs High Temp Storage
1988/89	9/2410 (0.3%)	1/2420 (0.04%)	1/1906 (0.05%)	3/2140 (0.14%)

Table 4. System SER Result

V_{CC}	Cycle Time	Device Hours	# of Errors	FIT (60%)
5V	1 μs	1.2M	0	763

Table 5. Latch-Up/ESD Test Results

# of Runs	Sample Size	Latch-Up Level	ESD Level
5	25 Units	>125 mA	>2500V

SOJ Package Qualification Data Summary

Year	1000 Hours 85°C/85% R.H.	204 Hours Steam	1000 Temp Cycles
1988/89	1/645 (0.16%)	2/504 (0.4%)	1/300 (0.3%)

21014

Number of bits: 1,048,576
Organization: 256K x 4
Process: CMOS
Package: 20-Pin PDIP

Table 1. Reliability Data Summary

Year	High Voltage (7V) Dynamic Lifetest		
	168 Hrs	500 Hrs	1000 Hrs
1989	3/600	1/597	0/597

Failure Rate Prediction:
Due to small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Table 2. Additional Qualification Tests

Year	1000 Hours 85°C/85% R.H.	204 Hrs Steam	1000 Temp Cycles	150°C/1K Hrs High Temp Storage
1989	1/250 (0.40%)	1/500 (0.20%)	0/250 (0.0%)	0/500 (0.0%)

APPENDIX A
COMMON MOS FAILURE MECHANISMS

Oxide Defects

Oxide defects can cause dielectric breakdown in MOS structures, resulting in an electrical short. Oxide dielectric breakdown is dependent on time, ambient temperature and operating voltage. Oxide defects could be induced by excessively thin oxide, polarization and contamination. The activation energy for Oxide defects is determined to be 0.3 eV.

Silicon Defects

Silicon defects are inherent in the unprocessed silicon wafers and may also be generated by stresses on the lattice during MOS processing. These silicon defects enhance parasitic leakage when they become active by "gettering" contaminants. The activation energy for silicon defects is determined to be 0.5 eV.

Refresh Degradation

In general, refresh failures are the result of degradation of random single bits caused by localized carrier generation. A localized silicon defect can act as a gathering site for contaminants and if this defect is located near a storage cell, it can cause this isolated cell to have poor refresh characteristics. The activation energy of refresh degradation is 0.5 eV.

Contamination

MOS circuits can fail due to threshold voltage (Vt) shifts when subjected to mobile ionic contamination. This ionic contamination reaches critical circuits through passivation defects subsequent to wafer processing. Sodium is the most common species of ionic contamination. The activation energy of ionic contamination is 1.0 eV.

Metallization Defects

Metallization defects (defects relating to metal conductor paths on the semiconductor die) can occur due to metal contamination, excess current density (electromigration) in the conductors, microcracks caused by sharp oxide steps and overalloying due to migration of metal through the semiconductor's contact. The activation energy is 0.5 eV.

Soft Errors

Soft errors refer to random non-recurring single bit errors and can be generated by noise in the device or system or by impact ionization from alpha particles. Alpha particles originating in the package penetrate the die surface, sometimes generating sufficient charge to switch the logic state of a cell. Soft error rates can be reduced by using low alpha packaging materials, die coating to prevent alpha particles from reaching the chip surface and optimal circuit designs to resist alpha particle disturbances.

Static RAMs (Random Access Memories)

4

5116S/L
2K x 8-BIT CMOS STATIC RAM

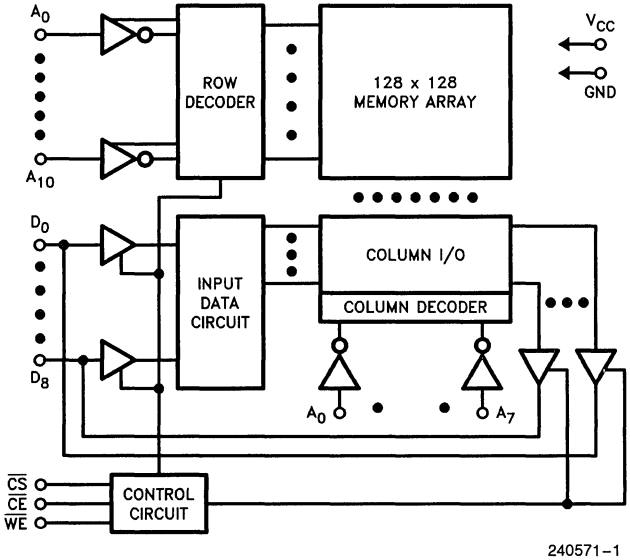
	5116S-10	5116S-12	Unit
Address Access Time (t_{AA})	100	120	ns
Chip Select Access Time (t_{ACS})	100	120	ns
Output Enable Access Time (t_{OE})	40	50	ns

- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **High Reliability 24-Pin 600 Mil PDIP Package**

The 5116S is a 2048-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

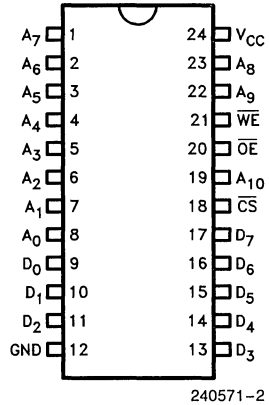
When the Chip Select is brought high, the device assumes a standby mode in which the standby current is reduced to 2 μA (max). The 5116S has a data retention mode that guarantees that data will remain at minimum power supply voltage of 2.0V.

Block Diagram



240571-1

Pin Connections



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Pin Names

A_0–A_{10}	Address Input
D_0–D_7	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power
GND	Ground

October 1989
Order Number: 240571-002

Device Operation

The 5116S has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin and should be used for device operation. $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins.

Standby Power

The 5116S is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	X	H	Read	High Z	Active

Write Mode

Write Cycles may be controlled by either $\overline{WE}$ or $\overline{CS}$. In either case, both $\overline{WE}$ and $\overline{CS}$ must be high (V_{IH}) during address transitions. During a $\overline{WE}$ Controlled write cycle, $\overline{CS}$ must be held low (V_{IL}) while $\overline{WE}$ is low. Address transfers occur on the falling edge of $\overline{WE}$ and the data transfers on rising edge of $\overline{WE}$. During a $\overline{CS}$ controlled cycle, $\overline{WE}$ must be held low (V_{IL}) while $\overline{CS}$ is low. The addresses are then transferred on the falling edge of $\overline{CS}$ and data on the rising edge of $\overline{CS}$. Data, in both cases, must be valid for a time t_{DW} before the controlling input is brought high (V_{IH}) and remain valid for a time t_{DH} after the controlling input is high.

Read Mode

$\overline{CS}$ must be low (V_{IL}) and $\overline{WE}$ must be high (V_{IH}) to activate a read cycle and obtain data at the outputs. Given stable addresses, valid data is available after a time t_{AA}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to +7V
Storage Temperature (T_{stg}) ..... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −3.5V for periods less than 20 ns.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		6	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		8	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

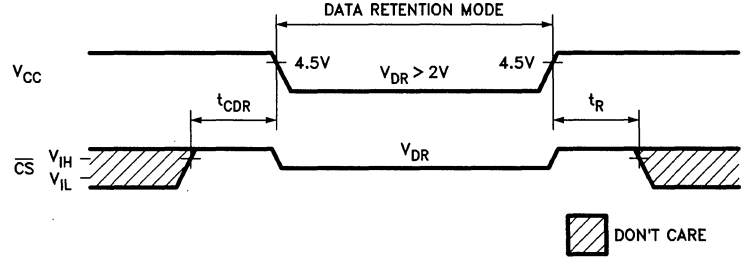
Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
I_{CC1}	Operating Current			30	40	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs open
I_{CC2}	Dynamic Current			30	60	mA	T_{cyc} = Min, V_{CC} = Max Outputs open
I_{SB}	Standby Current				3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		STD		4	50	μA	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} = GND to V_{CC}
		L		0.2*	2		
I_{LI}	Input Load Current		−1		1	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−1		1	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2.1 mA

*T_A = 25°C

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CDR}	Voltage for Data Retention		2			V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≥ V_{CC} − 0.2V		0.05	2	μA
t_{CDR}	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Low V_{CC} Data Retention Waveform



240571-3

A.C. TEST CONDITIONS

Input Pulse Levels .....0.8V to 2.4V
Input Rise and Fall Times .....10 ns
Timing Reference Level 1.5V
Output Load .....1 TTL Load + 100 pF

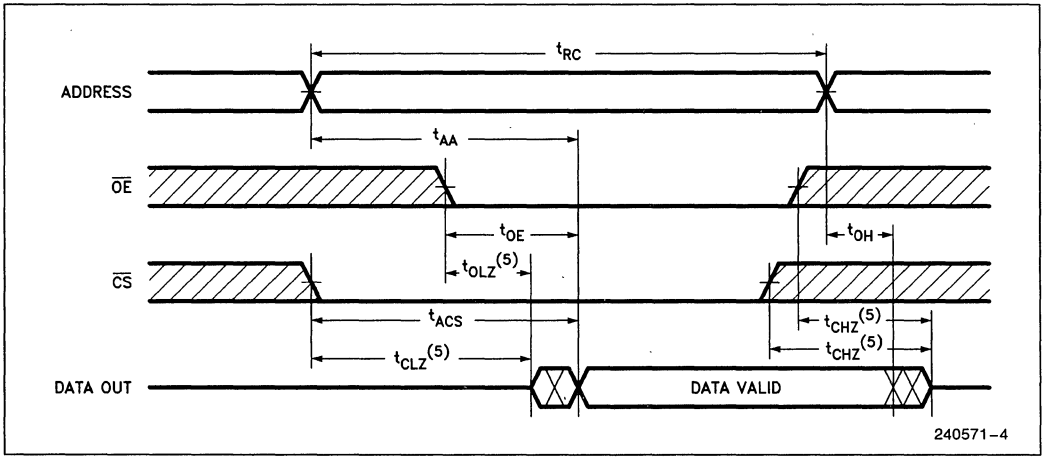
A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

READ CYCLE

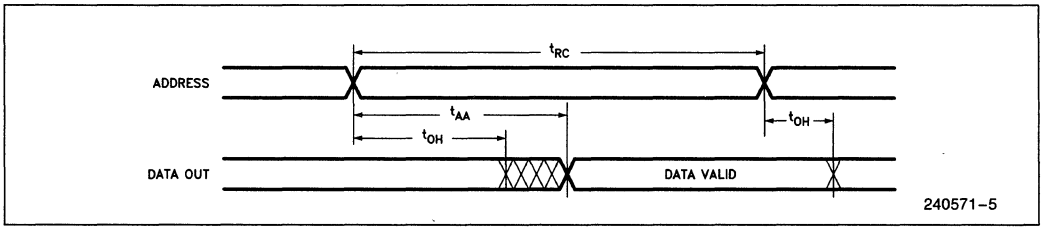
Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{RC}	READ Cycle Time	100		120		ns
t_{AA}	Address Access Time		100		120	ns
t_{ACS}	Chip Select Access Time		100		120	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{CLZ}	Chip Selection to Output in Low Z	10		10		ns
t_{CHZ}	Chip Deselection to Output in High Z	0	40	0	40	ns
t_{OE}	Output Enable Access Time	40		50		ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		ns
t_{OHZ}	Output Enable to Output in High Z	0	40	0	40	ns

4

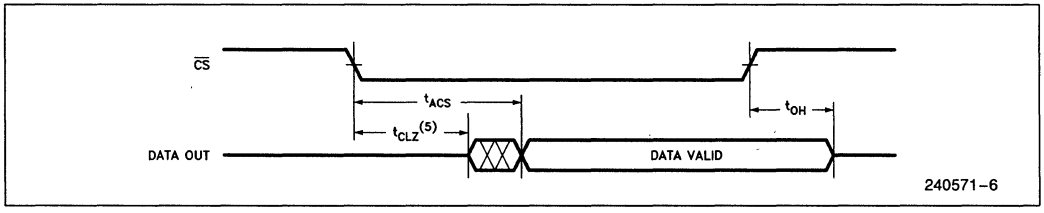
READ CYCLE NO. 1(1)



READ CYCLE NO. 2(1, 2, 4)



READ CYCLE NO.3(1, 3, 4)



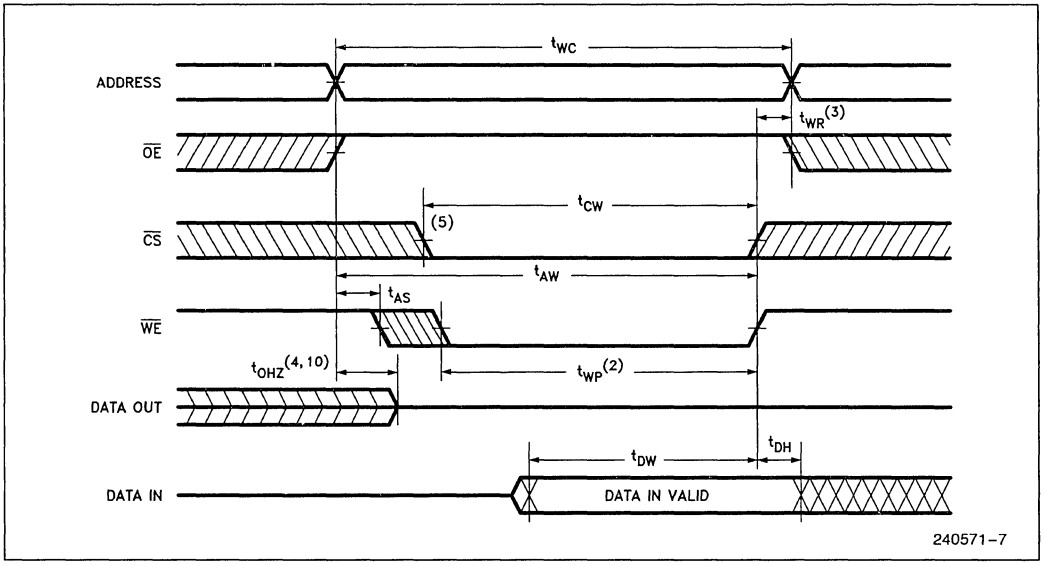
NOTES:
1. $\overline{WE}$ is high for READ Cycle. The first transitioning address.
2. Device is continuously selected; $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured at ±500 mV from steady state voltage.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10% (Continued)

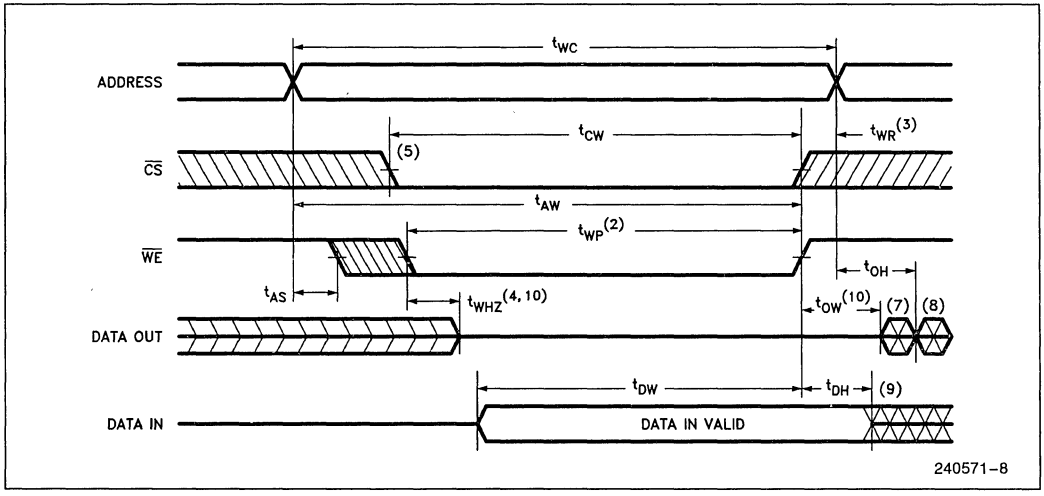
WRITE CYCLE

Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{WC}	WRITE Cycle Time	100		120		ns
t_{CW}	Chip Selection to End of Write	65		70		ns
t_{AW}	Address Valid to End of Write	80		105		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{WP}	Write Pulse Width	60		70		ns
t_{WR}	Write Recovery Time	10		10		ns
t_{DW}	Data Valid to End of Write	30		35		ns
t_{DH}	Data Hold Time	10		10		ns
t_{WHZ}	Write Enable to Output in High Z	0	30	0	35	ns
t_{OW}	Output Active from End of Write	10		10		ns
t_{OHZ}	Output Disable to Output in High Z	0	40	0	40	ns

WRITE CYCLE NO. 1(1)



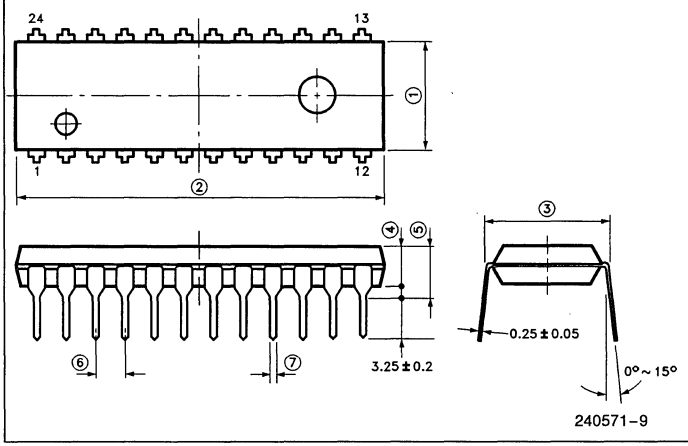
WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
4. During this period, I/O pins are in tri-state.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in tri-state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data on this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in output state.
10. Transition is measured at ±500 mV from steady state voltage.

PACKAGE OUTLINE

24-DIP



	Normal	Shrink
①	13.2 ± 0.25	6.35 ± 0.2
②	31.0 ± 0.3	22.0 ± 0.25
③	15.24 TYP.	7.62 TYP.
④	4.25 ± 0.2	3.45 ± 0.2
⑤	5.1 ± 0.2	4.2 ± 0.2
⑥	P − 2.54 TYP.	P − 1.778 TYP.
⑦	0.5 ± 0.1	0.46 ± 0.1

5164S/L
8K x 8-BIT CMOS STATIC RAM

	5164S/L-07	5164S/L-10	Units
Address Access Time (t_{AA})	70	100	ns
Chip Select Access Time (t_{ACS})	70	100	ns
Output Enable Access Time (t_{OE})	35	55	ns

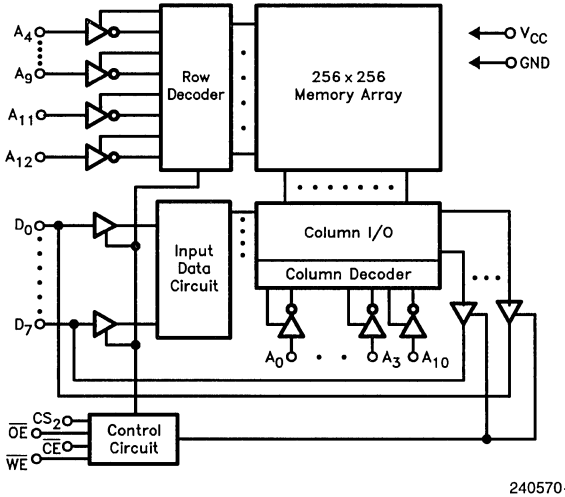
- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **High Reliability 28-Pin 600 Mil PDIP and 28-Pin SOP Package Types**

The 5164S/L is a 8192-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

The 5164S/L is placed in a standby or reduced power consumption mode by asserting either CS input ($\overline{CS}_1$, CS_2) false. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input. When device is deselected, standby current is reduced to 100 μA (max). The device will remain in standby mode until both pins are asserted true again. The device has a data retention mode that guarantees that data will remain valid at minimum V_{CC} of 2.0V.

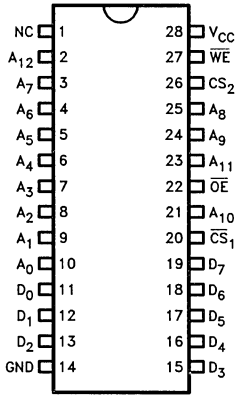
4

Block Diagram



240570-1

Pin Connections



240570-2

Pin Names

A_0–A_{12}	Address Input
D_0–D_7	Data Input/Output
$\overline{CS}_1$	Chip Select One
CS_2	Chip Select Two
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

April 1990
Order Number: 240570-004

Device Operation

The 5164S/L has three control inputs: Two Chip Selects ($\overline{CS_1}$, CS_2) and Write Enable ($\overline{WE}$). $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins. A write cycle starts at the lowest transition of $\overline{CS_1}$, low $\overline{WE}$ or high CS_2 and ends at the earliest transitiion of $\overline{CS_1}$, high WE or low CS_2. Out Enable (OE) is used for precise control of the outputs.

The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

Table 1. Mode Selection Truth Table

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Standby	High Z	Standby
X	L	X	X	Standby	High Z	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to 7V
Storage Temperature (T_{STG}) .... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS})..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −3.5V for periods less than 20 ns.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Units
C_{IN1}	Input Capacitance (V_{IN} = 0V)	—	6	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)	—	8	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

Symbol	Parameter		Min	Typ*	Max	Units	Test Conditions
I_{CC1}	Operating Current		—	30	40	mA	$\overline{CS1} = V_{IL}$, CS2 = V_{IH} I/O Open, V_{CC} = Max
I_{CC2}	Dynamic Current		—	30	60	mA	T_{CYC} = Min, V_{CC} = Max I/O Open
I_{SB}	Standby Current			—	3	mA	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL}
I_{SB1}		STD		0.02	2	mA	$\overline{CS1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} < 0.2V$
		L	—	2	100	μA	
I_{SB2}		STD		0.02	2	mA	CS2 ≤ $V_{CC} - 0.2V$
		L	—	2	100	μA	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
I_{LI}	Input Load Current		−1	—	1	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−1	—	1	μA	$\overline{CS1} = V_{IH}$, CS2 = V_{IL} V_{OUT} = Ground to V_{CC}
V_{OH}	Output High Voltage		2.4	—	—	V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage		—	—	0.4	V	I_{OL} = 2.1 mA

*V_{CC} = 5V, T_A = 25°C

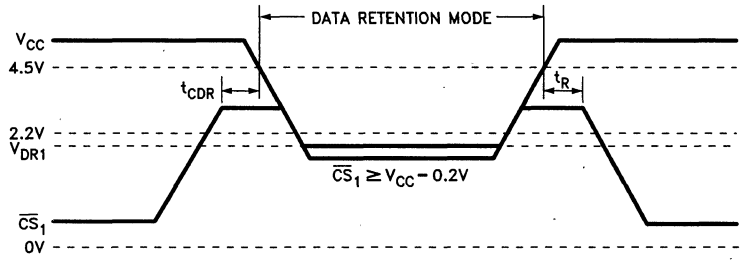
4

DATA RETENTION ELECTRICAL CHARACTERISTICS

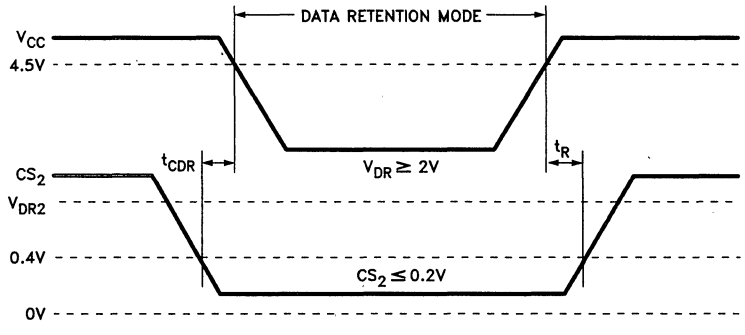
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{CDR}	Voltage for Data Retention	2		—	V	
I_{CCDR}	Data Retention Current		—	1	μA	$\overline{CS1} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
			—	1	μA	CS2 ≤ 0.2V $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	—	—	ns	
t_R	Opeation Recovery Time	t_{RC}**	—	—	ns	

**t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform



240570-3



240570-4

A.C. TEST CONDITIONS

Input Pulse Levels .....0.8V to 2.4V
Input Rise and Fall Times .....5 ns
Timing Reference Level 1.5V
Output Load.....1 TTL Load + 100 pF

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

READ CYCLE

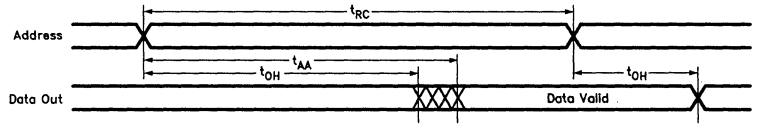
Symbol	Parameter	5164S/L-07		5164S/L-10		Units
		Min	Max	Min	Max	
t_{RC}	READ Cycle Time	70		100		ns
t_{AA}	Address Access Time		70		100	ns
t_{ACS}	Chip Select Access Time*		70		100	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{CLZ}	Chip Selection to Output in Low Z*	5		10		ns
t_{CHZ}	Chip Deselection to Output in High Z*	0	30	0	35	ns
t_{OE}	Output Enable Access Time	35		55		ns
t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	ns

*Timing parameters referenced to both $\overline{CS}1$ and CS2.

4

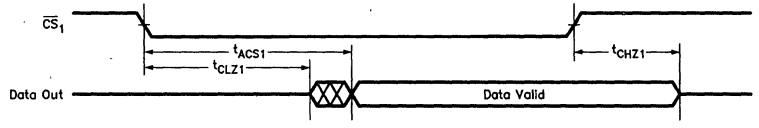
TIMING DIAGRAMS

READ CYCLE 1(1, 2, 4)



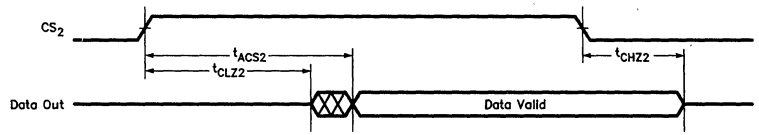
240570-5

READ CYCLE 2(1, 3, 4, 6)



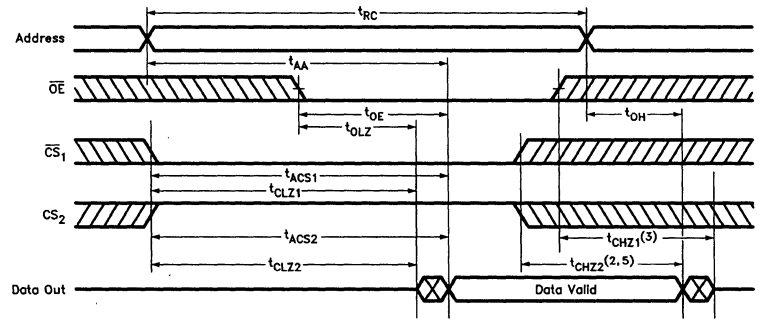
240570-6

READ CYCLE 3(1, 4, 7)



240570-7

READ CYCLE 4(1)



240570-8

NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected $\overline{CS1}$ = V_{IL} and CS2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.
6. CS2 is high.
7. $\overline{CS1}$ is low.

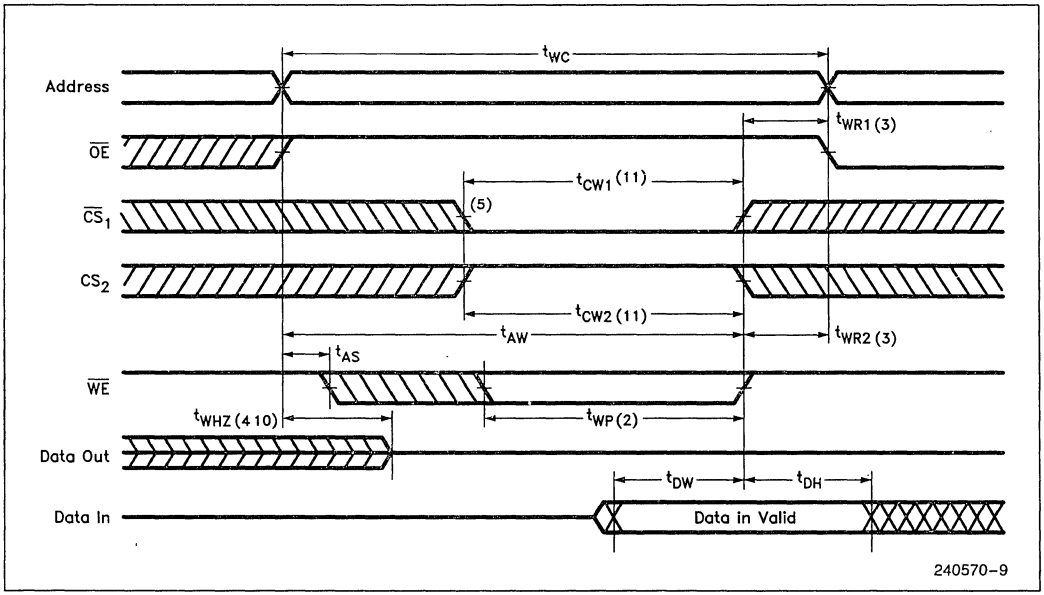
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

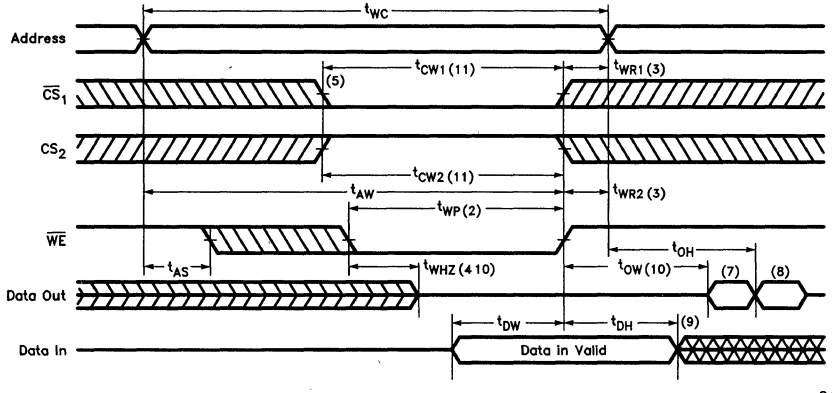
Symbol	Parameter	5164S/L-07		5164S/L-10		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70		100		ns
t_{CW}	Chip Selection to End of Write	60		70		ns
t_{AW}	Address Valid to End of Write	60		80		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{WP}	Write Pulse Width	40		60		ns
t_{WR}	Write Recovery Time	10		15		ns
t_{DW}	Data Valid to End of Write	30		40		ns
t_{DH}	Data Hold Time	0		15		ns
t_{WHZ}	Write Enable to Output in High Z	0	30	0	35	ns
t_{OW}	Output Active from End of Write	5		10		ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	ns

4

WRITE CYCLE 1(1)



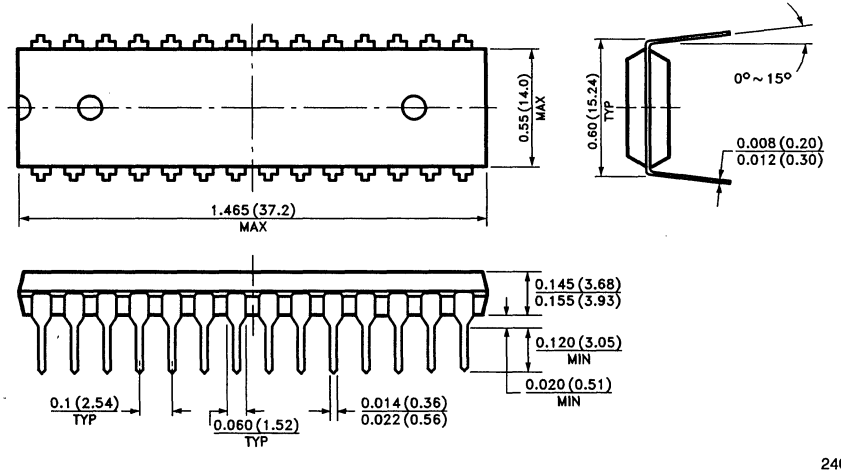
WRITE CYCLE 2(1, 6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$, a high CS, and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high or CS going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition or the CS high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$)
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low and CS is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.
11. t_{OW} is measured from the later of $\overline{CS}$ going low or CS going high to the end of write.

PACKAGE OUTLINE

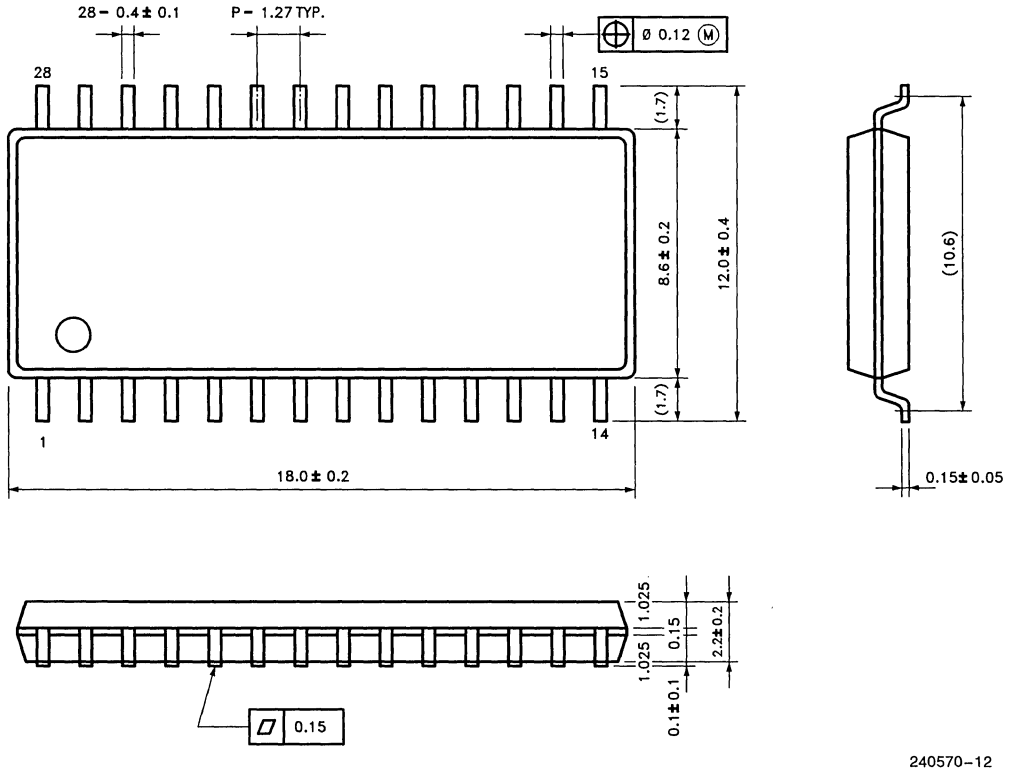
28-DIP



Units = millimeter (mm)

PACKAGE OUTLINE

28-PIN SOP



240570-12

Units = millimeter (mm)

4

51256S/L
32K x 8-BIT CMOS STATIC RAM

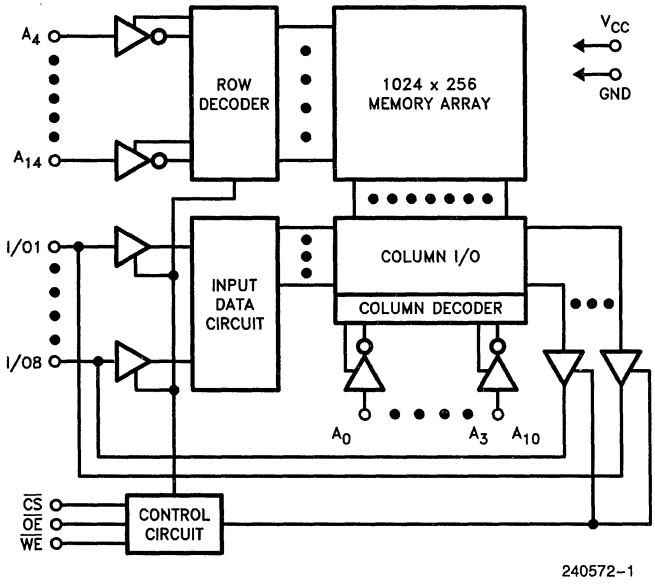
	51256S/L-07	51256S/L-10	Unit
Address Access Time (t_{AA})	70	100	ns
Chip Select Access Time (t_{ACS})	70	100	ns
Output Enable Access Time (t_{OE})	40	50	ns

- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **High Reliability 28-Pin 600 Mil PDIP and 28-Pin SOP Package Types**

The 51256S/L is a 32768-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

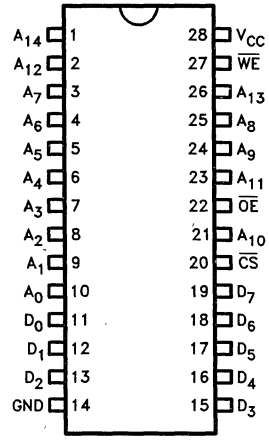
When the Chip Select is brought high, the device assumes a standby mode in which the standby current is reduced to 100 μA (max). The device has a data retention mode that guarantees that data will remain valid at minimum V_{CC} of 2.0V.

Functional Block Diagram



240572-1

Pin Connections



240572-2

Pin Names

A_0–A_{14}	Address
D_0–D_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

April 1990
Order Number: 240572-004

Device Operation

The 51256S/L has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin used for device operation. $\overline{WE}$ is the data control pin used to gate data at the I/O pins. Out Enable (OE) is used for precise control of the outputs.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	X	H	Read	High Z	Active
L	H	L	Read	D_{OUT}	Active
L	L	X	Write	D_{IN}	Active

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to 7V
Storage Temperature (T_{STG}) .... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS})..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V

NOTE:
V_{IL} (Min) = −3.0V for 20 ns pulse.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		8	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		10	pF

NOTE:
This parameter is sampled and not 100% tested.

4

D.C. AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

Symbol	Parameter		Min	Typ*	Max	Units	Test Conditions
I_{CC1}	Operating Current			35	40	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} I/O Open
I_{CC2}	Dynamic Operating Current			35	60	mA	Min Cycle, $\overline{CS}$ = V_{IL} V_{CC} = Max, I/O Open
I_{SB}	Standby Current			—	3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		Std.	—	—	1	mA	$\overline{CS}$ = V_{CC} ≥ 0.2V
		L	—	2	100	μA	
I_{LI}	Input Load Current		−1		1	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−1		1	μA	$\overline{CS}$ = V_{IH} V_{OUT} = Ground to V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = −2.1 mA

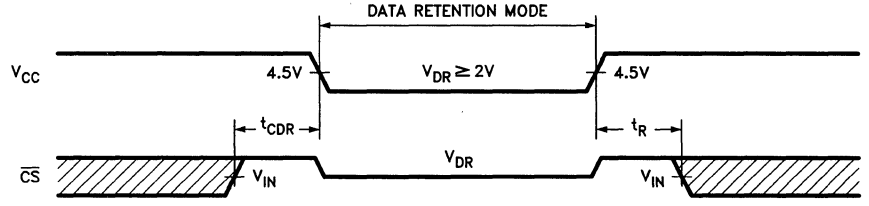
*V_{CC} = 5V, T_A = 25°C

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{CDR}	Voltage for Data Retention	2			V	
I_{CCDR}	Data Retention Current		2	50	μA	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{CC} = 3.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	t_{RC}**			ns	

**t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform



240572-3

A.C. TEST CONDITIONS

Input Pulse Levels .....0.8V to 2.4V
Input Rise and Fall Times .....5 ns
Timing Reference Level 1.5V
Output Load.....1 TTL Load + 100 pF

A.C. CHARACTERISTICS

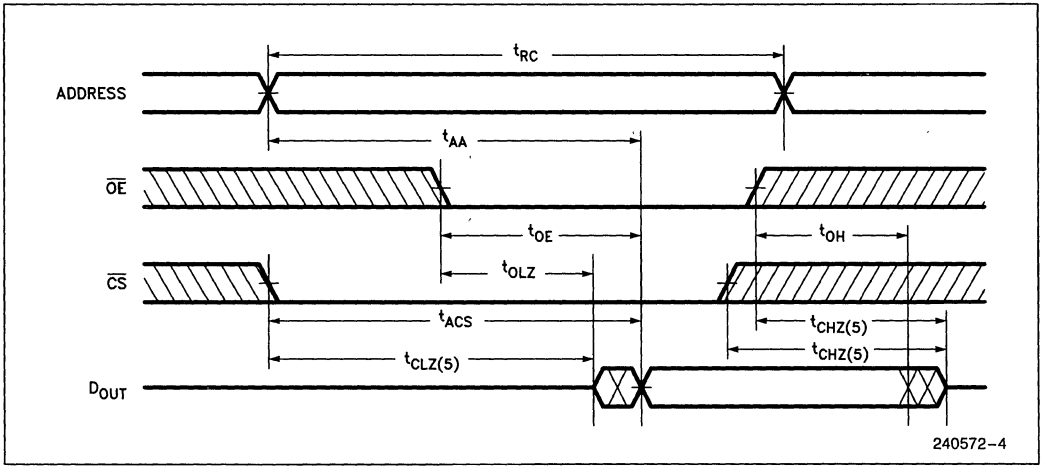
T_A = 0°C to 70°C, V_{CC} = 5V ±10%

READ CYCLE

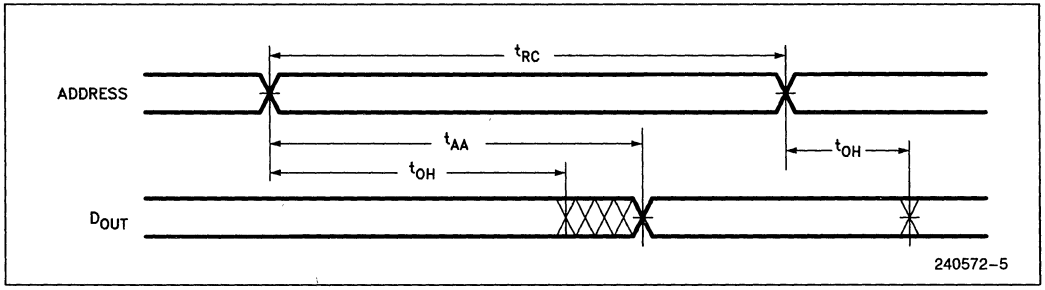
Symbol	Parameter	51256S/L-07		51256S/L-10		Unit
		Min	Max	Min	Max	
t_{RC}	READ Cycle Time	70		100		ns
t_{AA}	Address Access Time		70		100	ns
t_{ACS}	Chip Select Access Time		70		100	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{CLZ}	Chip Selection to Output in Low Z	5		10		ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	0	35	ns
t_{OE}	Output Enable Access Time		40		50	ns
t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	35	ns

TIMING DIAGRAMS

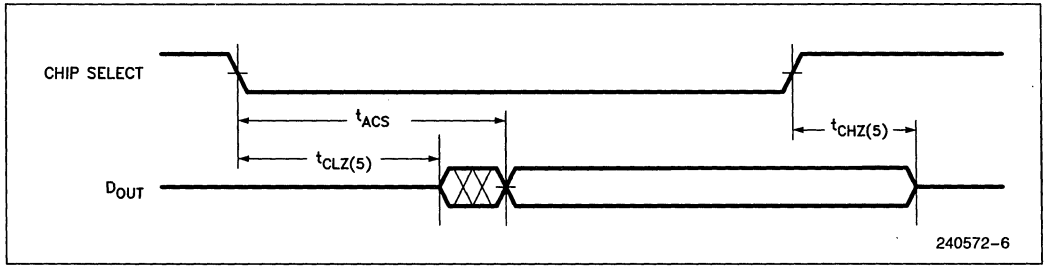
READ CYCLE(1)



READ CYCLE 2(1, 2, 4)



READ CYCLE 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500 mV from steady. This parameter is sampled and not 100% tested.

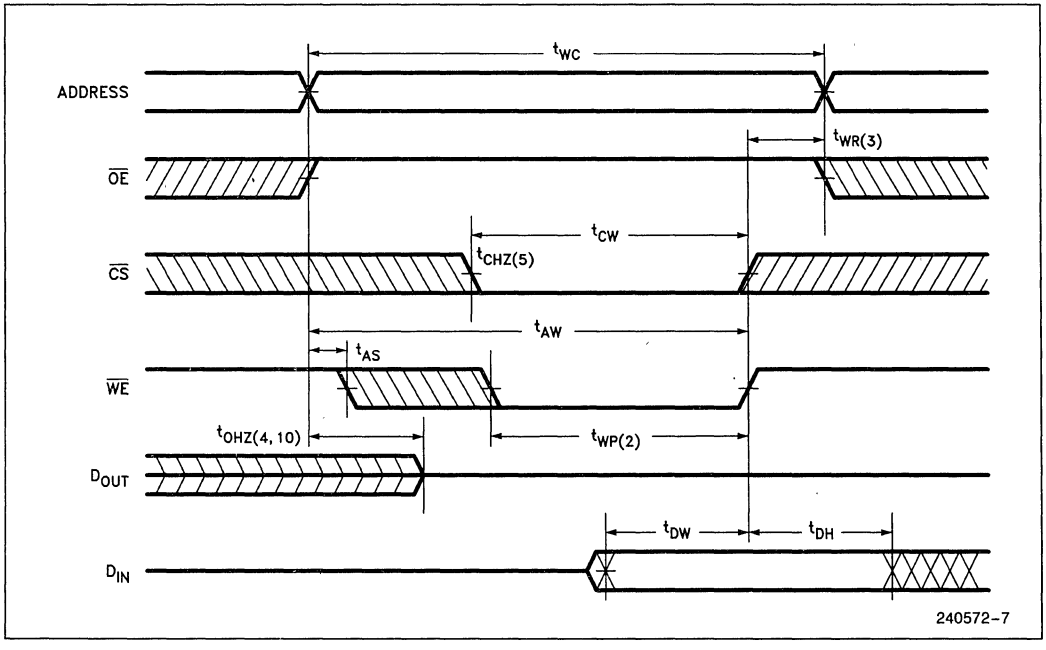
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

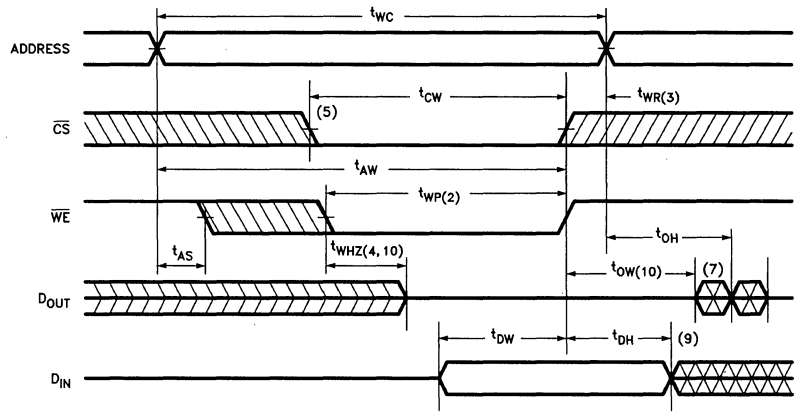
Symbol	Parameter	51256S/L-07		51256S/L-10		Unit
		Min	Max	Min	Max	
t_{WC}	WRITE Cycle Time	70		100		ns
t_{CW}	Chip Selection to End of Write	45		80		ns
t_{AW}	Address Valid to End of Write	65		80		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{WP}	Write Pulse Width	45		70		ns
t_{WR}	Write Recovery Time	5		5		ns
t_{DW}	Data Valid to End of Write	30		40		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WHZ}	Write Enable to Output in High Z	0	40	0	35	ns
t_{OW}	Output Active from End of Write	5		10		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	35	ns

4

WRITE CYCLE 1(1)



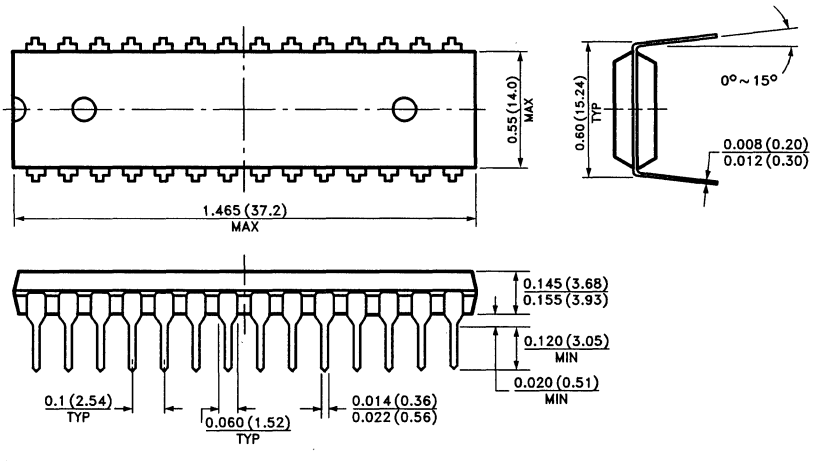
WRITE CYCLE 2(1, 6)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.

PACKAGE OUTLINE

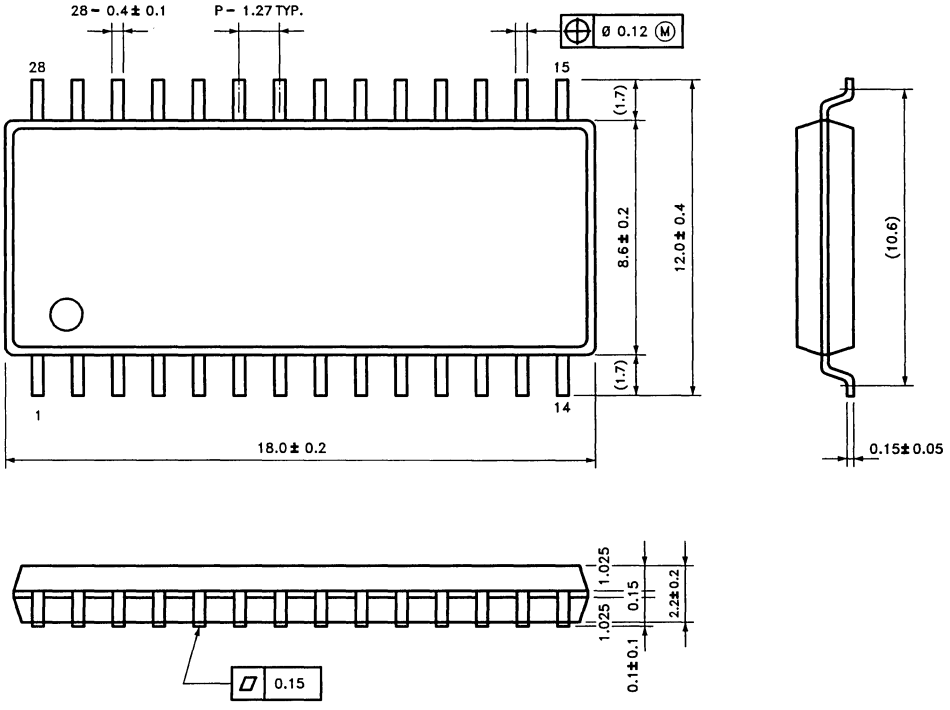
28-DIP



Units = inches

PACKAGE OUTLINE (Continued)

28-Pin SOP



240572-10

Units = millimeter (mm)

4

51C68
HIGH SPEED CHMOS 4096 x 4-BIT STATIC RAM

	51C68-30	51C68-35	51C68-35L
Max. Access Time (ns)	30	35	35
Max. Active Current (mA)	90	90	65
Max. Standby Current (mA)	10	10	5

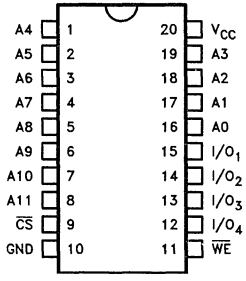
- **Double Metal CHMOS III Technology**
- **Completely Static Memory-No Clock**
- **Equal Access & Cycle Times**
- **Single +5V Supply**
- **Automatic Power Down**
- **0.8–2.0V Output Timing Reference**
- **High Density 20-Pin Package**
- **Directly TTL Compatible All Inputs and Outputs**
- **Common Data Input & Output**
- **Three-State Output**
- **2148H Upgrade**

The Intel 51C68 is a 16,384-bit Static Random Access Memory organized as 4096 words x 4-bits. This memory is fabricated using Intel's high performance double metal CHMOS III technology, with a full CHMOS 6T cell. This state of the art technology with HMOS III scaled transistors brings high performance to CMOS Static RAMs. The design of the 51C68 offers a 4X density improvement over the industry standard 2148H with improved performance.

$\overline{CS}$ controls the power down feature. In no more than a cycle time after $\overline{CS}$ goes high (deselecting the 51C68), the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature can result in system power savings as great as 90% in larger systems where the majority of devices are deselected. Its non-power down companion, the 51C69, is available to provide a fast chip select access time for speed critical applications.

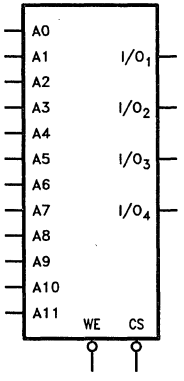
The 51C68 is assembled in a 20-pin plastic or cerdip, 300 mil package configured with the industry standard 4K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

Pin Configuration



290091-1

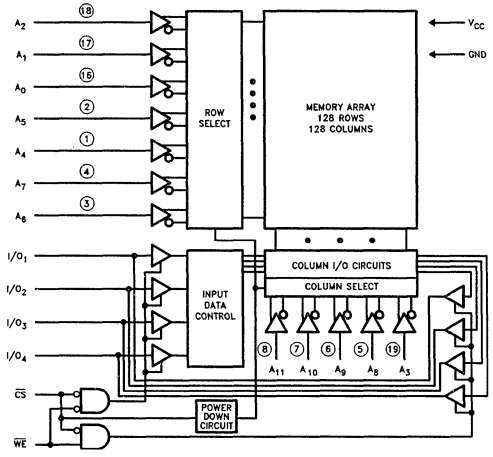
Logic Symbol



290091-2

Pin Names

A_0–A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1–I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground



290091-3

Figure 1. 51C68 Block Diagram

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

November 1989
Order Number: 290091-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature Cerdip .... −65°C to +150°C
Storage Temperature Plastic .... −65°C to +125°C
Voltage on Any Pin with Respect to Ground ..... −2.0V to +7V(4)
D.C. Continuous Output Current ..... 20 mA
Power Dissipation 1.0W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to +70°C, V_{CC} = +5V ±10% unless otherwise noted

Symbol	Parameter	Notes	Min	Typ(2)	Max	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)			0.01	1	µA	V_{CC} = Max, V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			0.1	10	µA	CS = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
I_{CC}	Operating Current	5		60	90	mA	V_{CC} = Max, CS = V_{IL}, Outputs Open
I_{SB}	Standby Current	6		3	10	mA	V_{CC} = Min to Max, CS = V_{IH}
V_{IL}	Input Low Voltage	4	−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		6.0	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −4 mA
I_{OS}	Output Short Circuit Current	3	−300		+300	mA	V_{CC} = Max, V_{IN} = GND to V_{CC}

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
   For Cerdip θ_{JA} (@ 400 fpm air flow) = 40° C/W
   θ_{JA} (still air) = 70° C/W
   θ_{JC} = 25°C C/W
   For Plastic θ_{JA} (@ 400 fpm air flow) = 70° C/W
   θ_{JA} (still air) = 109° C/W
   θ_{JC} = 42° C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C with load shown in Figure 2.
3. Output shorted for no more than 1 sec. No more than one output shorted at any time.
4. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
5. I_{CC} max for 51C68-35L is 65 mA.
6. I_{SB} max for 51C68-35L is 5 mA.

4

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Input Timing Reference Level 1.5V
Output Timing Reference Levels 0.8V–2.0V
Output Load ..... See Figure 2

CAPACITANCE[7] T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	V_{IN} = 0V
C_{IO}	Input/Output Capacitance	7	pF	V_{OUT} = 0V

NOTE:
7. This parameter is sampled and not 100% tested.

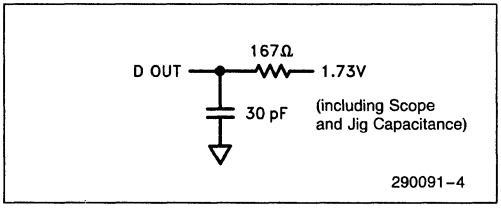


Figure 2. Output Load

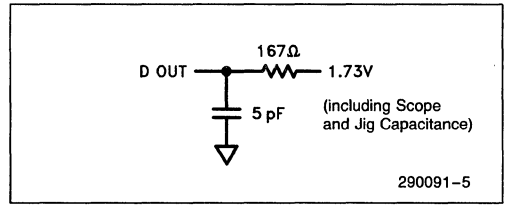


Figure 3. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

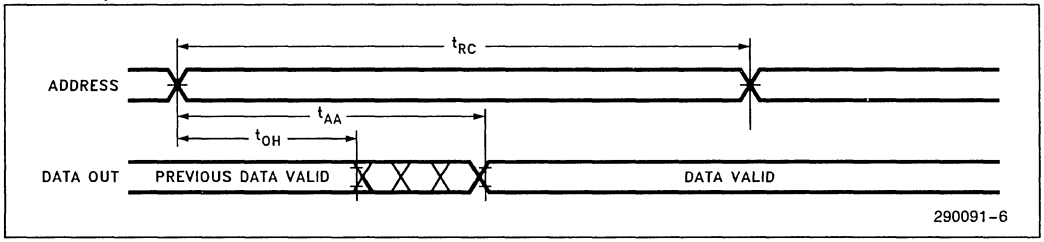
A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise noted

READ CYCLE

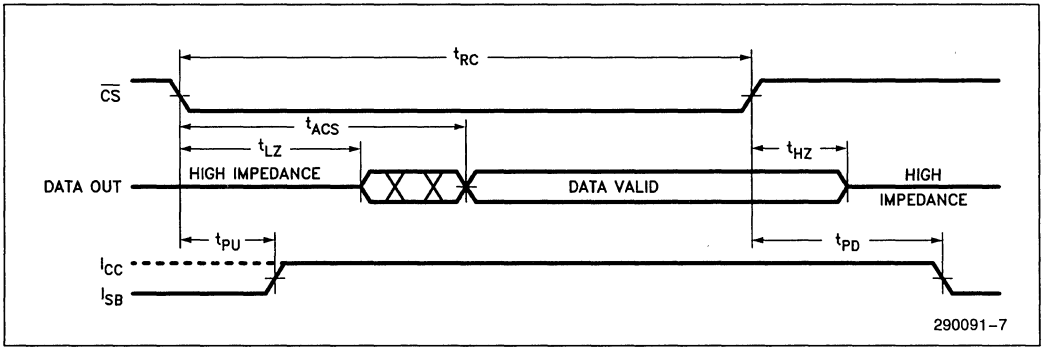
Symbol	Parameter	51C68-30		51C68-35 51C68-35L		Unit	Test Conditions
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	30		35		ns	(Note 1)
t_{AA}	Address Access Time		30		35	ns	
t_{ACS}	Chip Select Access Time		30		35	ns	(Note 8)
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	5		5		ns	(Notes 2, 3, & 7)
t_{HZ}	Chip Deselection Output in High Z		15		15	ns	(Notes 2, 3 & 7)
t_{PU}	Chip Selection to Power Up Time	0		0		ns	(Note 7)
t_{PD}	Chip Deselection to Power Down Time		30		35	ns	(Note 7)

WAVEFORMS

READ CYCLE NO. 1[4, 5]



READ CYCLE NO. 2[4, 6, 8]



NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 3.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for a finite time prior to selection. If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.

A.C. CHARACTERISTICS

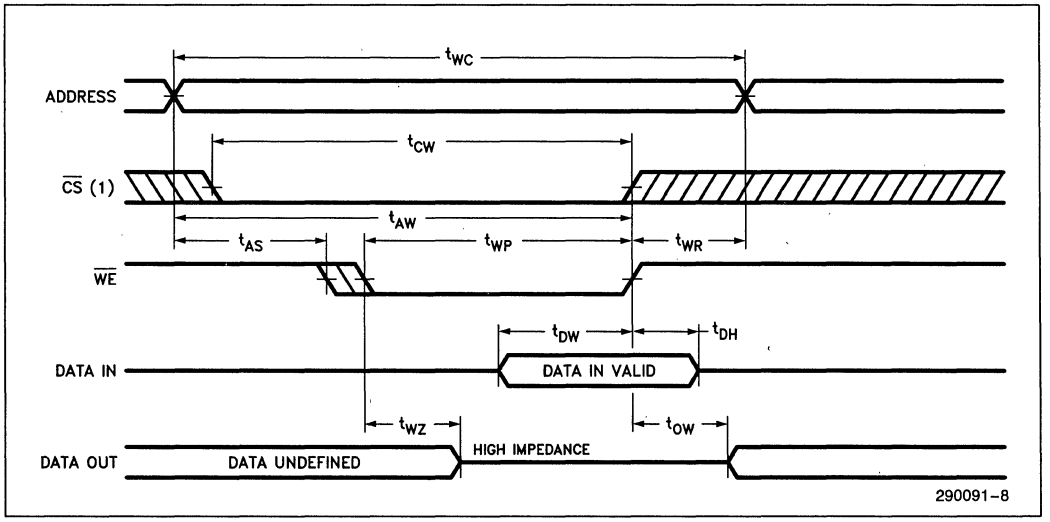
T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise noted (Continued)

WRITE CYCLE

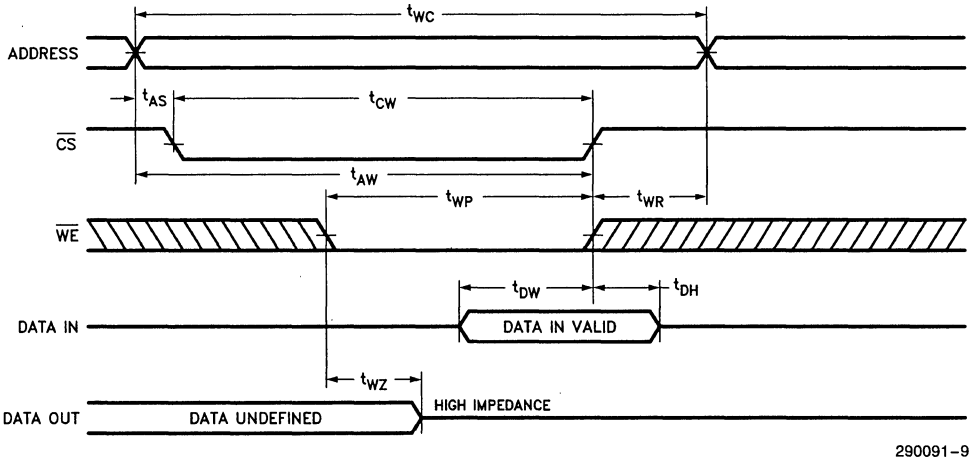
Symbol	Parameter	51C68-30		51C68-35 51C68-35L		Unit	Test Conditions
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	30		35		ns	(Note 2)
t_{CW}	Chip Selection to End of Write	25		30		ns	
t_{AW}	Address Valid to End of Write	25		30		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	25		30		ns	
t_{WR}	Write Recovery Time	5		5		ns	
t_{DW}	Data Valid to End of Write	15		15		ns	
t_{DH}	Data Hold Time	5		5		ns	
t_{WZ}	Write Enable to Output in High Z	0	15	0	15	ns	(Note 3)
t_{OW}	Output Active from End of Write	0		0		ns	(Note 3)

WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[4]



WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(4)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 3.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

4

51C98
HIGH SPEED CHMOS 16,384 x 4-BIT STATIC RAM

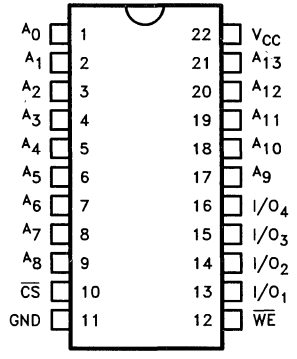
	51C98-20	51C98-25	51C98-30
Max. Access Time (ns)	20	25	30
Max. Active Current (mA)	100	100	100
Max. Standby Current (mA)	15	15	15

- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **High Reliability Ceramic Package**

The 51C98 is a 65,536-bit high speed static RAM configured as 16K x 4. It is fabricated using Intel's high performance 1.0 micron CHMOS IV technology. This state of the art technology, coupled with Intel's innovative 6T cell design, virtually eliminates latch-up and alpha induced soft errors without organic coating.

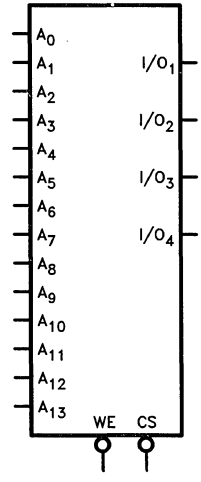
The power down feature, controlled by $\overline{CS}$, also contributes greatly to system reliability. The device's power consumption is reduced 10-fold when in this low power standby mode. In fact, 85% system power reduction is achievable in large systems where a majority of the devices are deselected.

Pin Configuration



240442-1

Logic Symbol



240442-2

Pin Names

A0–A13	Address Inputs	I/O1–I/O4	Data In/Out
$\overline{WE}$	Write Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	GND	Ground

December 1989
Order Number: 240442-002

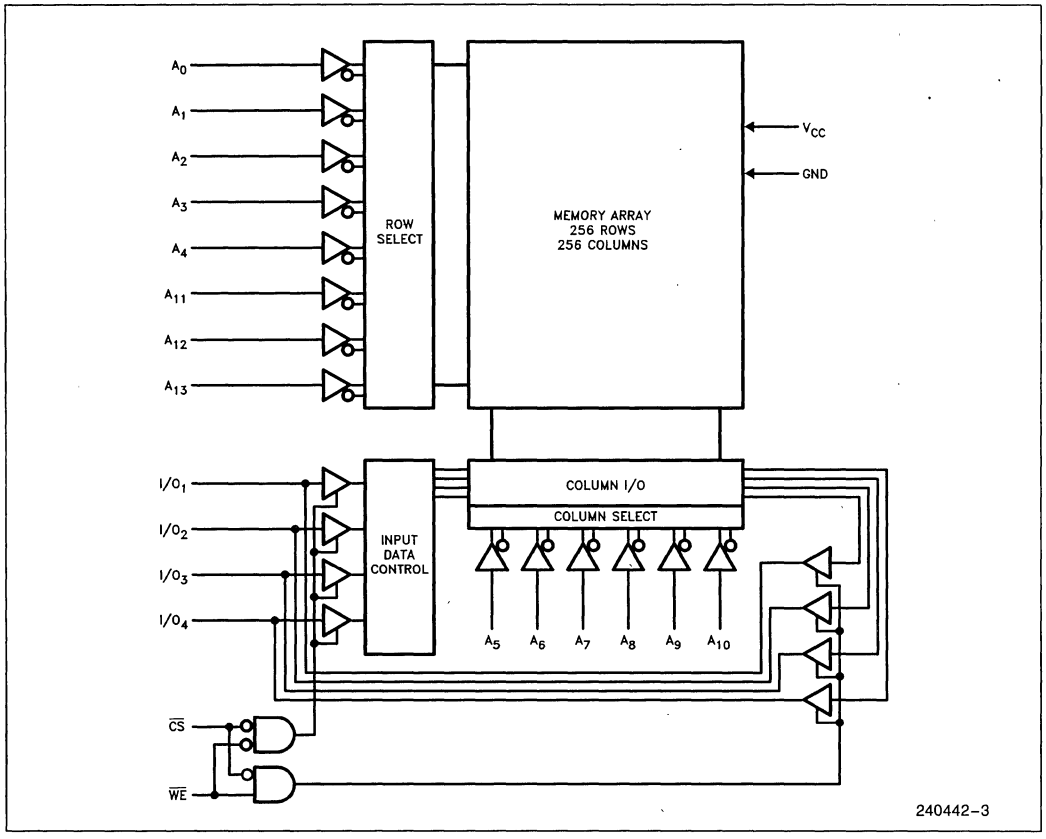


Figure 1. Block Diagram

DEVICE OPERATION

The 51C98 has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin and should be used for device operation. $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins.

Standby Power

The 51C98 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Standby	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

Write Mode

Write Cycles may be controlled by either $\overline{WE}$ or $\overline{CS}$. In either case, both $\overline{WE}$ and $\overline{CS}$ must be high (V_{IH}) during address transitions. During a $\overline{WE}$ Controlled write cycle, $\overline{CS}$ must be held low (V_{IL}) while $\overline{WE}$ is low. Address transfers occur on the falling edge of $\overline{WE}$ and the data transfers on rising edge of $\overline{WE}$. During a $\overline{CS}$ controlled cycle, $\overline{WE}$ must be held low (V_{IL}) while $\overline{CS}$ is low. The addresses are then transferred on the falling edge of $\overline{CS}$ and data on the rising edge of $\overline{CS}$. Data, in both cases, must be valid for a time t_{DW} before the controlling input is brought high (V_{IH}) and remain valid for a time t_{DH} after the controlling input is high.

Read Mode

$\overline{CS}$ must be low (V_{IL}) and $\overline{WE}$ must be high (V_{IH}) to activate a read cycle and obtain data at the outputs. Given stable addresses, valid data is available after a time t_{AA}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_{IN}, V_{OUT}) ..... −1.0V to +7.0V
Storage Temperature (Ceramic) (T_{stg}) ..... −65°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS}) ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS}, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

CAPACITANCE T_A = +25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Units
C_{IN1}	Input Capacitance (V_{IN} = 0V)		7	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		7	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

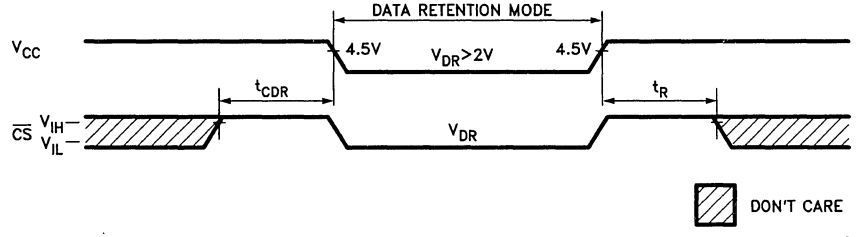
Recommended Operating Conditions unless otherwise noted

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	Operating Current		100	mA	V_{CC} = Max $\overline{CS}$ = V_{IL}, Outputs Open, T_{cycle} = Min
I_{SB}	Standby Current		15	mA	V_{CC} = Min to Max $\overline{CS}$ = V_{IH}
I_{LI}	Input Load Current	−10	10	µA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage	−10	10	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to 4.5V
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	
V_{CDR}	Voltage for Data Retention	2			V		
I_{CCDR}	Data Retention Current		95 350	500 750	μA μA	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$ $V_{CC} = 3V$
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}			ns		

Low V_{CC} Data Retention Waveform

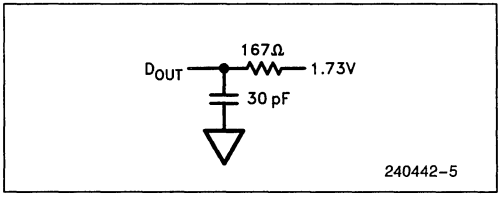


240442-4

4

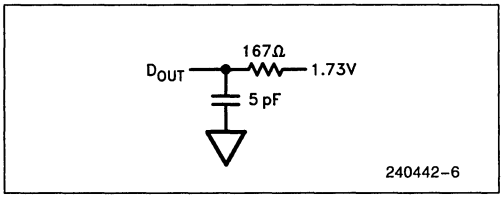
A.C. TEST CONDITIONS

Input Pulse Levels.....GND to 3.0V
Input Rise and Fall Times.....5 ns
Timing Reference Level.....1.5V
Output Load.....See Figures 2, 3



240442-5

Figure 2. Output Load



240442-6

Figure 3. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CHARACTERISTICS

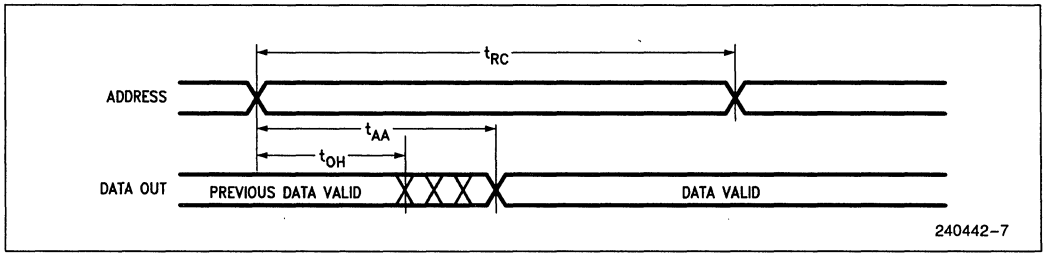
T_A = 0°C to +70°C, V_{CC} = 5V ±10%

READ CYCLE

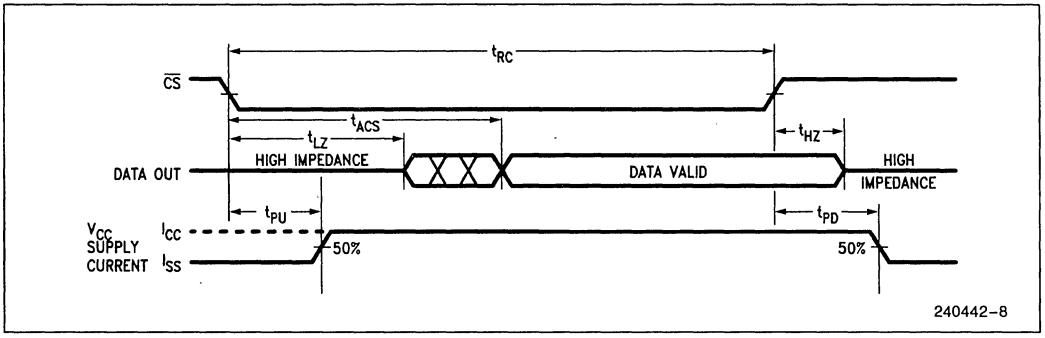
Symbol	Parameter	51C98-20		51C98-25		51C98-30		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	READ Cycle Time	20		25		30		ns
t_{AA}	Address Access Time		20		25		30	ns
t_{ACS}	Chip Select Access Time		20		25		30	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{LZ}	Chip Selection to Output in Low-Z	0		0		0		ns
t_{HZ}	Chip Deselection to Output in High-Z		15		15		20	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		25		30	ns

NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage, t_{HZ}(Max) is less than t_{LZ}(Min), both for a given device and from device to device.
3. Transition is measured at ±500 mV from steady state voltage with specified loading in Figure 3.

READ CYCLE NO. 1(1, 2)



READ CYCLE NO. 2(1, 3)



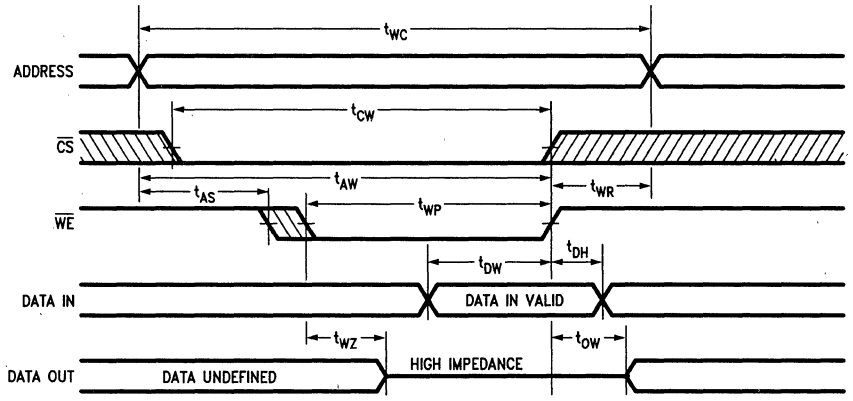
NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	51C98-20		51C98-25		51C98-30		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time(1)	20		25		30		ns
t_{CW}	Chip Selection to End of Write	15		20		25		ns
t_{AW}	Address Valid to End of Write	15		20		25		ns
t_{AS}	Address Set-Up Time	0		0		0		ns
t_{WP}	Write Pulse Width	15		20		20		ns
t_{WR}	Write Recovery Time	2		2		2		ns
t_{DW}	Data Valid to End of Write	12		15		15		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High-Z(2)	0	15	0	15	0	15	ns
t_{OW}	Output Active from End of Write(2)	0		0		0		ns

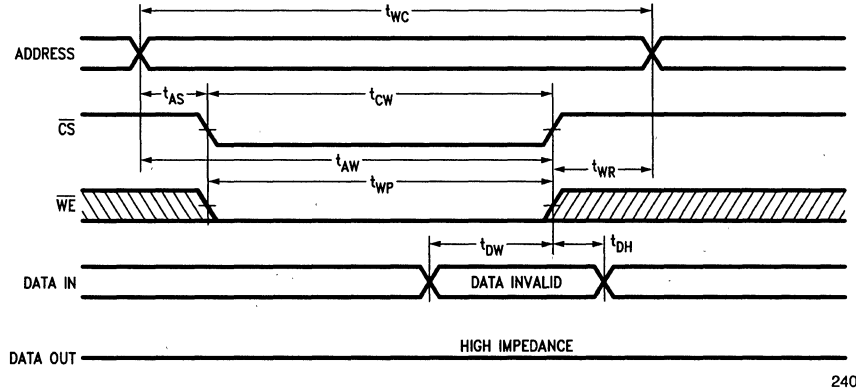
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(3)



240442-9

NOTES:
1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured at +500 mV from steady state voltage with specified loading in Figure 3.
3. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2)



240442-10

NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ switches low coincident with or after $\overline{WE}$ switches low, the outputs will stay in a high impedance state. If $\overline{CS}$ switches high or coincident with or after $\overline{WE}$ switches high, the outputs will stay in a high impedance state.

5164
HIGH SPEED 8192 x 8-BIT STATIC RAM

	5164-20	5164-25	5164-30	5164-35
Max Access Time (ns)	20	25	30	35
Max Active Current (mA)	120	110	100	100
Max Standby Current (mA)	30	30	30	30

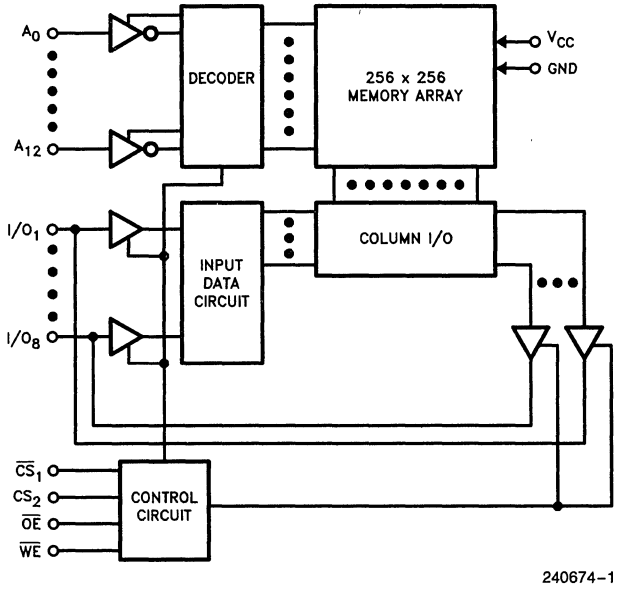
- **Static Operation — No Clock/Refresh Required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **2V Data Retention Option Available**
- **Power Down Mode**
- **TTL Compatible**
- **Common Data Input and Output**
- **28-Pin 300 Mil Plastic Package**

The 5164 is a 65,536-bit high speed static RAM configured as 8K x 8. Easy memory expansion is available with two chip enables ($\overline{CS1}$ and CS2) and an Output Enable ($\overline{OE}$).

The power down feature contributes greatly to system reliability. The device's power consumption is reduced when in this low power standby mode. In fact, 85% system power reduction is achievable in large systems where a majority of the devices are deselected.

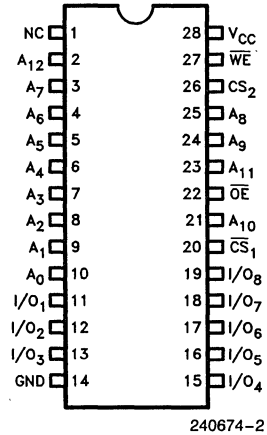
4

Functional Block Diagram



240674-1

Pin Configurations



240674-2

Pin Names

A_0–A_{12}	Address	$\overline{WE}$	Write Enable
I/O_1–I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS_1}$	Chip Select	GND	Ground
CS_2	Chip Select	V_{CC}	Power

May 1990
Order Number: 240674-002

Device Operation

The 5164 has three control inputs: Two Chip Selects ($\overline{CS1}$, CS2) and Write Enable ($\overline{WE}$). $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins. When $\overline{CS_1}$ and $\overline{WE}$ inputs are LOW and CS_2 is HIGH, data is written into the memory and reading is accomplished when $\overline{CS_1}$ and $\overline{OE}$ are active LOW, CS_2 active HIGH and $\overline{WE}$ remains inactive or HIGH.

Standby Power

The 5164 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS_1}$ input or low (V_{IL}) to the CS_2 input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Standby	High Z	Standby
X	L	X	X	Standby	High Z	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to Ground (V_{IN}, V_{OUT}) . . . −1.0V to +7V

Storage Temperature
(Ceramic) (T_{STG}) . . . . . −65°C to +150°C

Power Dissipation (P_D) 1.0W

DC Continuous Output Current (I_{OS}) . . . . . 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		7	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		7	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

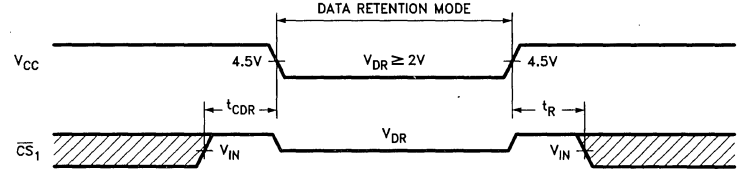
(Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	Operating Current		100	mA	V_{CC} = Max, $\overline{CS}_1$ = V_{IL} CS_2 = V_{IH}, Outputs Open, T_{CYCLE} = Min
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max $\overline{CS}_1$ = V_{IH} or CS_2 = V_{IL}
I_{SB1}			7	mA	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, V_{CC} = Max
I_{LI}	Input Load Current	−10	10	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage	−10	10	μA	$\overline{CS}_1$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to V_{CC}
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4 mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions	
V_{CDR}	Voltage for Data Retention	2			V		
I_{CCDR}	Data Retention Current		95	500	μA	V_{CC} = 2V	$\overline{CS}_1 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$
			350	750	μA	V_{CC} = 3V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}			ns		

Low V_{CC} Data Retention Waveform



240674-3

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Timing Reference Level 1.5V

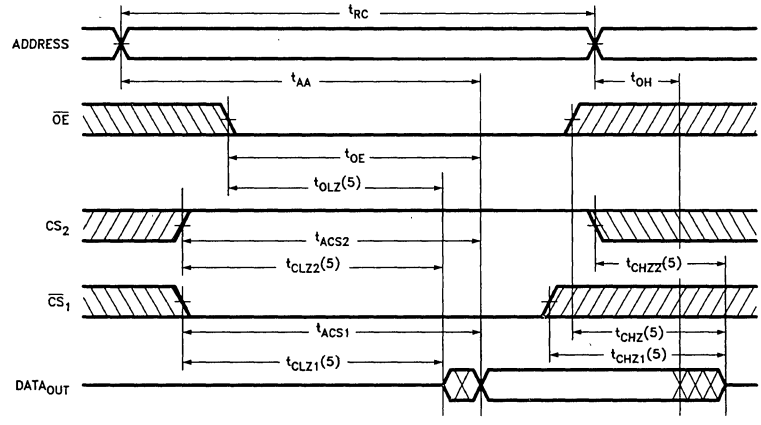
A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

READ CYCLE

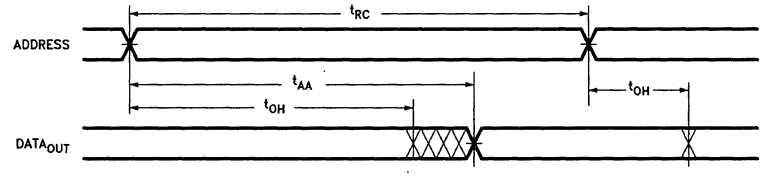
Symbol	Parameter	5164-20		5164-25		5164-30		5164-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{ACS1}	Chip Select 1 Access Time		20		25		30		35	ns
t_{ACS2}	Chip Select 2 Access Time		20		25		30		35	ns
t_{OE}	Output Enable to Output Valid		15		15		20		20	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{CLZ1}	Chip Select 1 to Output in Low Z	5		5		5		5		ns
t_{CLZ2}	Chip Select 2 to Output in Low Z	5		5		5		5		ns
t_{CHZ1}	Chip Select 1 to Output in High Z		15		15		20		20	ns
t_{CHZ2}	Chip Select 2 to Output in High Z		15		15		20		20	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Enable to Output in High Z		10		10		15		20	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		25		30		35	ns

NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage, t_{CHZ}(Max) is less than t_{CLZ}(Min), both for a given device and from device to device.

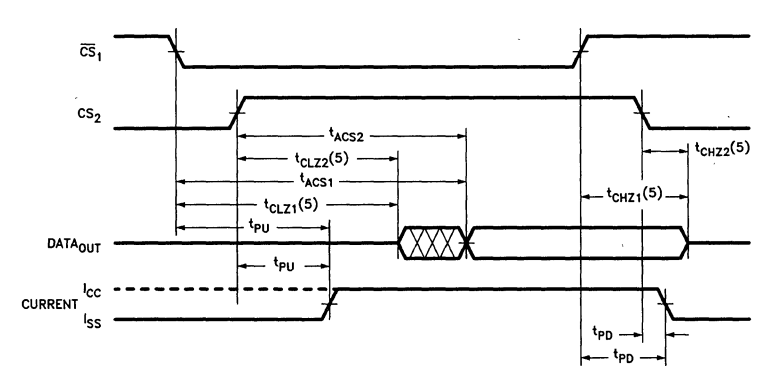
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



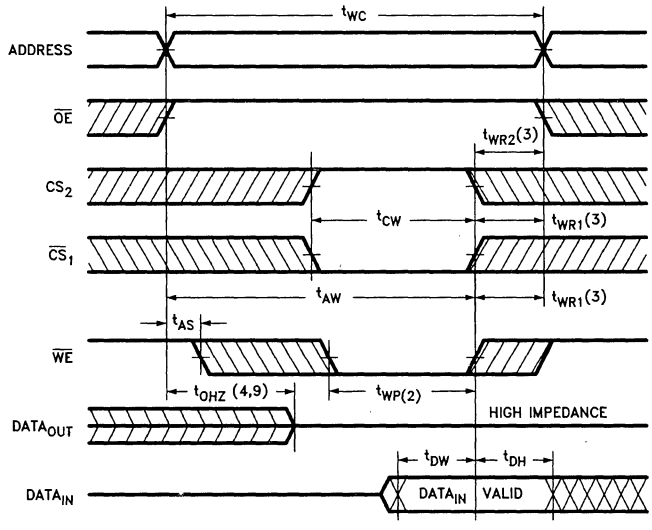
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±500 mV from steady state.

A.C. CHARACTERISTICS (Continued)

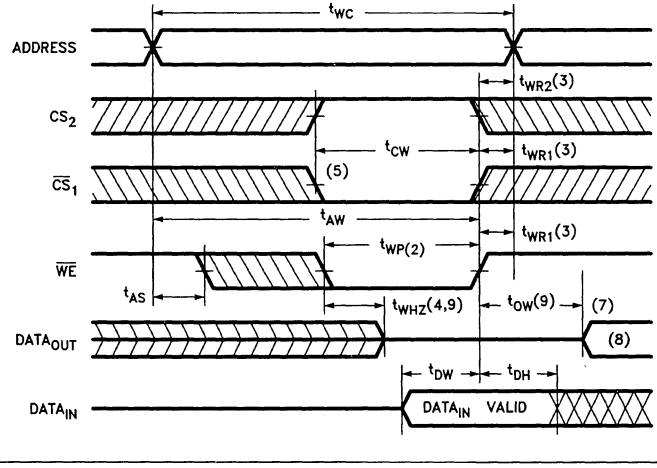
WRITE CYCLE

Symbol	Parameter	5164-20		5164-25		5164-30		5164-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{CW1}	Chip Selection 1 to End of Write	15		20		25		30		ns
t_{CW2}	Chip Selection 2 to End of Write	15		20		25		30		ns
t_{AW}	Address Valid to End of Write	15		20		25		30		ns
t_{AS}	Address Set-Up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	15		20		25		25		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	15		15		15		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WHZ}	Write Enable to Output in High Z	0	12	0	15	0	15	0	15	ns
t_{OW}	Output Active from End of Write	0		0		0		0		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)

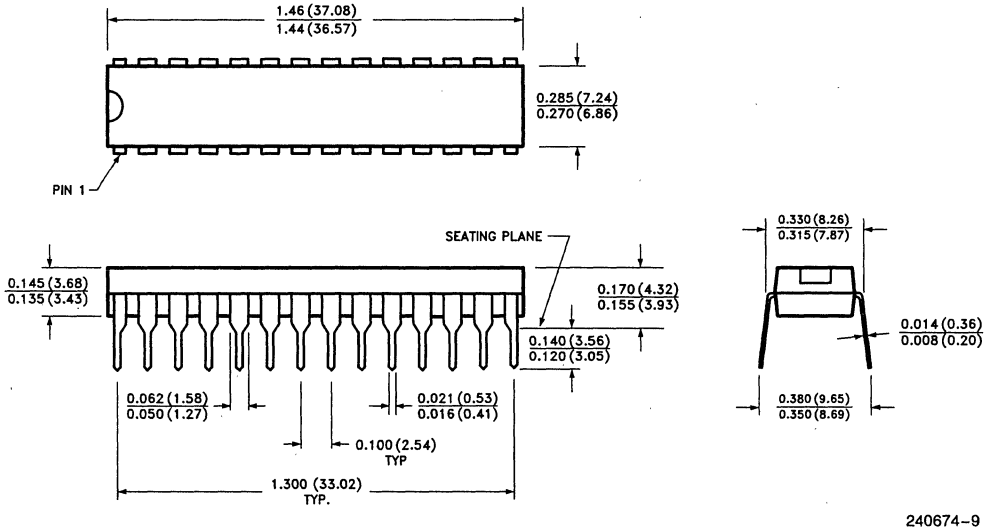


TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle, as long as address does not change.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ± 200 mV from steady state.

28-PIN PLASTIC DIP



51256
HIGH SPEED 32K x 8-BIT STATIC RAM

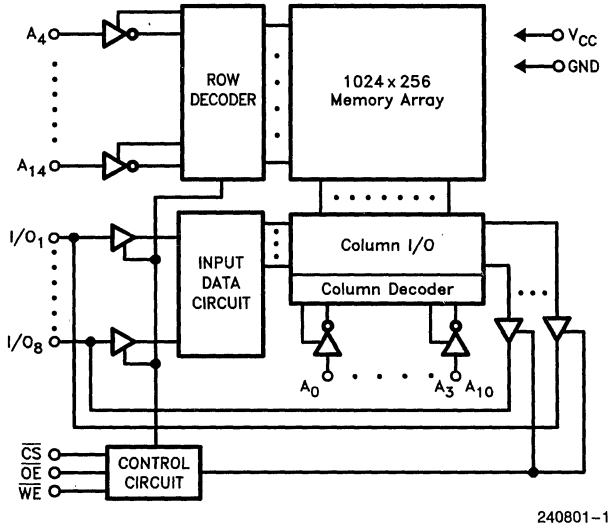
	51256-20	51256-25	51256-30	51256-35
Max Access Time (ns)	20	25	30	35
Max. Active Current (mA)	100	100	100	100
Max Standby Current (mA)	30	30	30	30

- **Static Operation — No Clock/Refresh required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **2V Data Retention Option Available**
- **Power Down Mode**
- **TTL compatible**
- **Common Data Input and Output**
- **28-Pin 300 Mil Plastic PDIP Package**

The 51256 is a 32,768-word by 8-bit high speed static RAM fabricated using a CMOS silicon gate process. Easy memory expansion is provided by an active low Chip Select ($\overline{CS}$) and an active low Output Enable. ($\overline{OE}$).

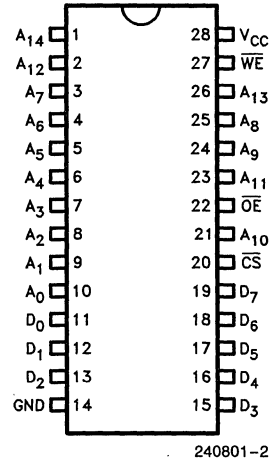
The power down feature contributes greatly to system reliability. The device's power consumption is reduced when in this low power standby mode.

Functional Block Diagram



240801-1

Pin Connections



240801-2

Pin Names

A_0-A_{14}	ADDRESS
D_0-D_7	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

August 1990
Order Number: 240801-001

DEVICE OPERATION

The 51256 has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{WE}$ is the data control pin to be used to gate data at the I/O pins. When $\overline{CS}$ and $\overline{WE}$ inputs are LOW, data is written into the memory and reading is accomplished when $\overline{CS}$ and $\overline{OE}$ are active LOW while Write Enable ($\overline{WE}$) remains inactive or HIGH.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H	Read	High Z	Active

STANDBY POWER

The 51256 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and outputs are in a high impedance state, independent of the $\overline{WE}$ input.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Voltage on any pin relative to Ground	V_{in}, V_{out}	−1.0 to +7V	V
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Power Dissipation	P_d	1.0	W
DC Continuous Output Current	I_{os}	50	mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5		0.8	V

NOTE:
During transitions, the inputs may undershoot to −2.0V for periods less than 20ns.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Max	Units
Input Capacitance (V_{IN} = 0V)	C_{IN}		8	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

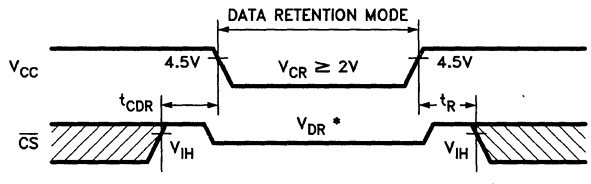
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	Test Conditions
Operating Current	I_{CC}		100	mA	V_{CC}=Max., $\overline{CS} \leq V_{IL}$ outputs open, T_{cycle} = Min.
Standby Power	I_{SB}		30	mA	V_{CC} = Max, $\overline{CS} \geq V_{IH}$
Supply Current	I_{SB1}		7	mA	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$, V_{CC}=Max
Input Load Current	I_{LI}	−10	10	μA	V_{CC} = Max $0V \leq V_{IN} \leq V_{CC}$
Output Leakage	I_{LO}	−10	10	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max $0V \leq V_{OUT} \leq V_{CC}$
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4.0 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8.0 mA

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CDR}	Voltage for Data Retention		2			V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq (V_{CC} - 0.2\,V)$ $V_{IN} \geq (V_{CC} - 0.2\,V)$ or $\leq 0.2V$ (V_{CC} = 2V)		95	50	μA
t_{CDR}	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}		ns	

LOW V_{CC} DATA RETENTION WAVEFORM



A.C. TEST QUESTIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Timing Reference Level 1.5V

A.C. CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5V ± 10%)

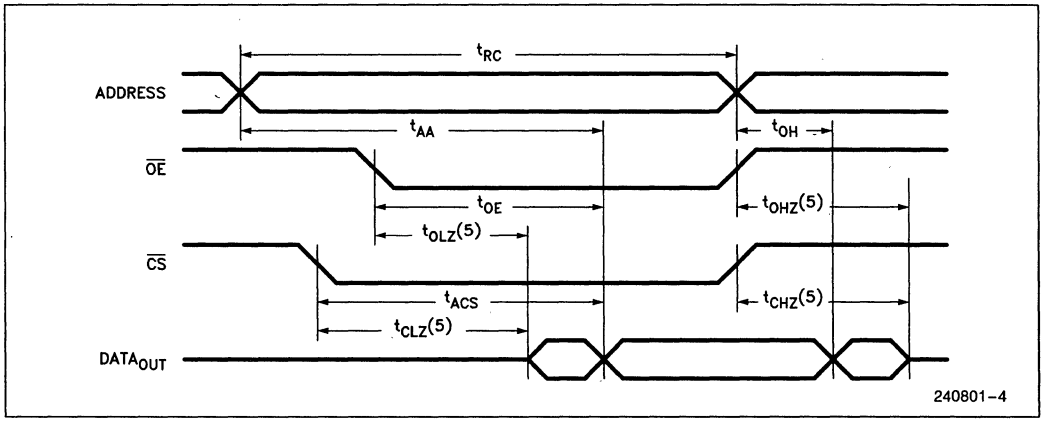
READ CYCLE

Symbol	Parameter	51256-25		51256-30		51256-35		51256-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address Access Time		25		30		35		45	ns
t_{ACS}	Chip Select Access Time		25		30		35		45	ns
t_{OE}	Output Enable to Output Valid		15		20		20		20	ns
t_{OH}	Output Hold from Address Change	5		5		5		5		ns
t_{CLZ}	Chip Select to Output in Low Z	5		5		5		5		ns
t_{CHZ}	Chip Deselect to Output in High Z		15		20		20		20	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		25		30		35		45	ns

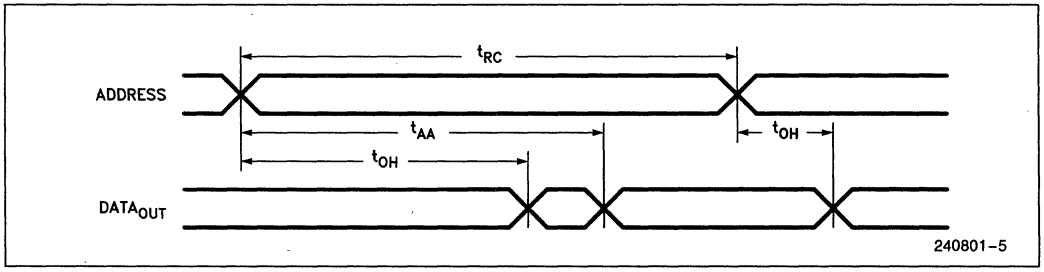
NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage, t_{CHZ} (Max) is less than t_{CLZ} (Min), both for a given device and from device to device.

4

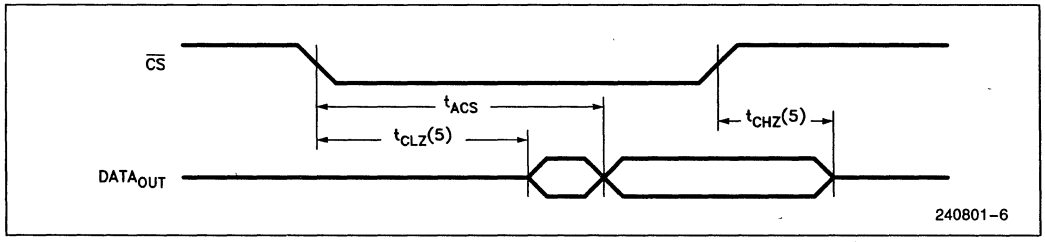
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ± 200 mV from steady state with 5 pF load (including scope and jig).

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	51256-25		51256-30		51256-35		51256-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{CW}	Chip Select To End of Write	20		25		30		40		ns
t_{AW}	Address Valid to End of Write	20		25		30		40		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	20		25		25		30		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	15		15		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WHZ}	Write Enable to Output in High Z	0	15	0	15	0	15	0	20	ns
t_{OW}	Output Active from End of Write	5		5		5		5		ns

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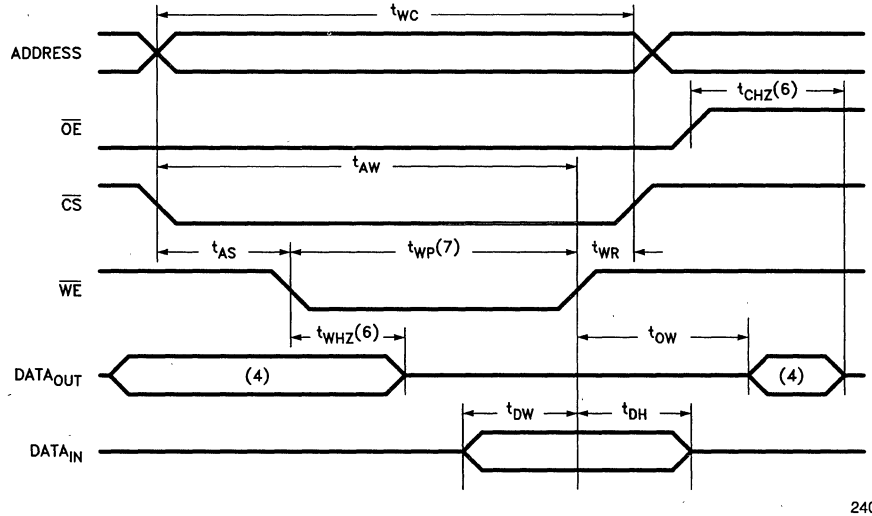
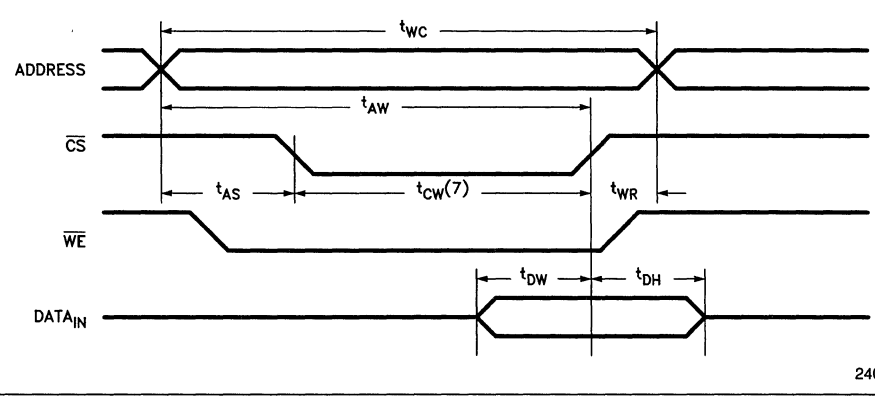
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



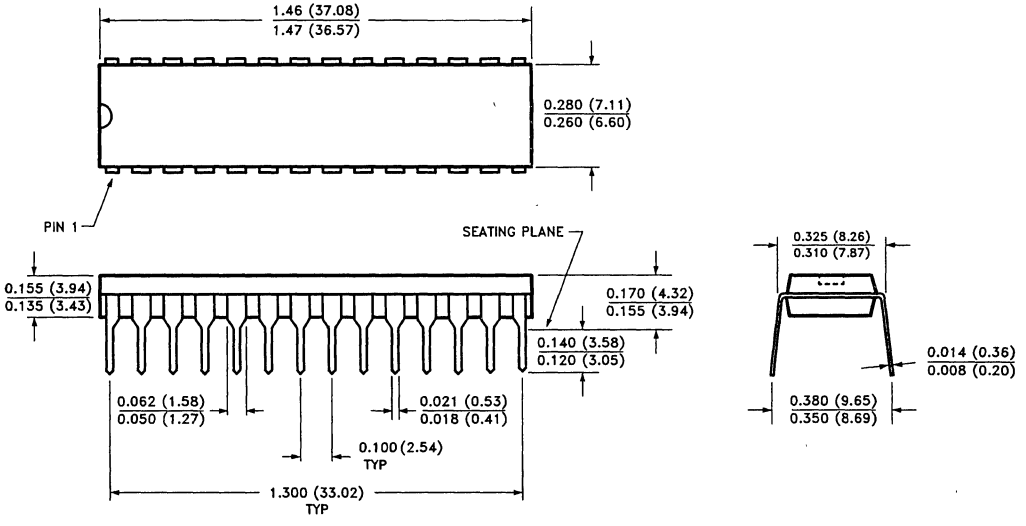
TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low CS and low WE.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 200 mV from steady state with a 5 pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS

28-Pin Plastic Dip



All dimensions in inches (millimeters) Max. / Min.

240801-9

4

51258
HIGH SPEED 64k x 4-BIT STATIC RAM

	51258-20	51258-25	51258-30	51258-35
Max Access Time (ns)	20	25	30	35
Max Active Current(mA)	100	100	100	100
Max Standby Current (mA)	30	30	30	30

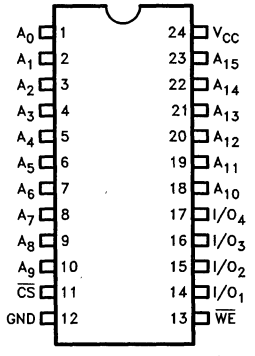
- **Static Operation — No Clock/Refresh required**
- **Equal Access and Cycle Times — Simplifies System Design**
- **Single +5V Supply**
- **2V Data Retention Option Available**
- **Power Down Mode**
- **TTL compatible**
- **Common Data Input and Output**
- **24-Pin 300 Mil Plastic PDIP Package**

The 51258 is a 65,536-word by 4 bit high speed static RAM fabricated using a CMOS silicon gate process. Easy memory expansion is provided by an active low Chip Select ($\overline{CS}$).

The power down feature contributes greatly to system reliability. The device's power consumption is reduced when in this low power standby mode.

Pin Configuration

DIP/SOIC



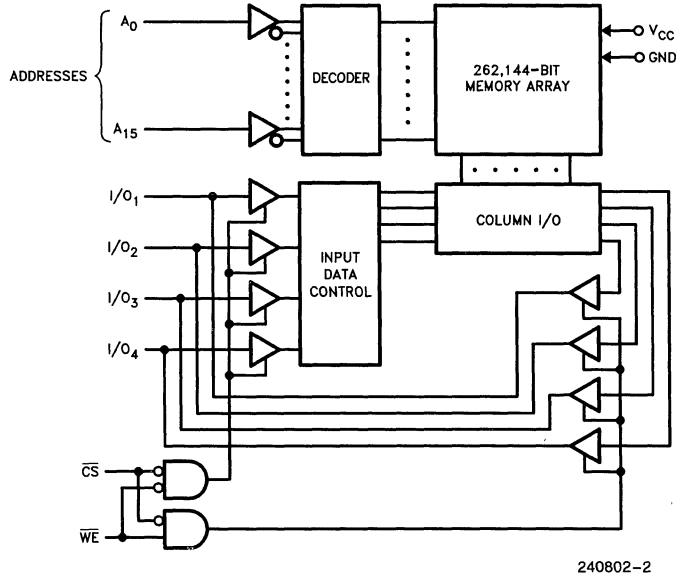
240802-1

Top View

Pin Names

A_0–A_{15}	Addresses
I/O_1–I/O_4	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
GND	Ground
V_{CC}	Power

Functional Block Diagram



240802-2

August 1990
Order Number: 240802-001

DEVICE OPERATION

The 51258 has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{WE}$ is the data control pin to be used to gate data at the I/O pins. When $\overline{CS}$ and $\overline{WE}$ inputs are LOW, data is written into the memory and reading is accomplished when $\overline{CS}$ goes active LOW while Write Enable ($\overline{WE}$) remains inactive or HIGH.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Standby	High Z	Standby
L	L	Write	D_{in}	Active
L	H	Read	D_{out}	Active

STANDBY POWER

The 51258 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and outputs are in a high impedance state, independent of the $\overline{WE}$ input.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Units
V_{in}, V_{out}	Voltage on any pin relative to Ground	−1.0 to +7V	V
T_{stg}	Storage Temperature (Ceramic)	−65 to +150	°C
P_d	Power Dissipation	1.0	W
I_{os}	D.C. Continuous Output Current	50	mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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RECOMMENDED OPERATING CONDITIONS

(Voltage referenced to V_{SS}, T_a = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	V_{CC}+0.5V	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V

NOTE:
During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min	Max	Units
C_{IN}	Input Capacitance (V_{IN} = OV)		–	8 pF
C_{OUT}	Output Capacitance (V_{OUT} = OV)		–	8 pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

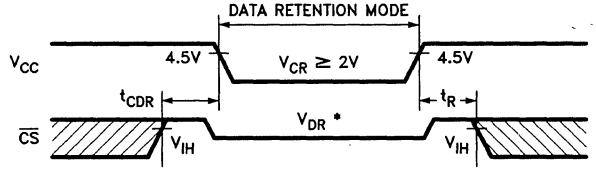
(Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	Operating Current	–	100	mA	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ Outputs Open, T_{Cycle} = min.
I_{SB}	Standby Power	–	30	mA	V_{CC} = Max, $\overline{CS} \geq V_{IH}$
I_{SB1}	Supply Current	–	7	mA	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$, V_{CC}=Max
I_{LI}	Input Load Current	−10	10	μA	V_{CC} = Max $0V \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage	−10	10	μA	$\overline{CS} = V_{IH}$, V_{CC} = Max $0V \leq V_{OUT} \leq V_{CC}$
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = −4.0 mA
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 8.0 mA

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CDR}	Voltage for Data Retention		2		–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq (V_{CC} - 0.2\ V)$ $V_{IN} \geq (V_{CC} - 0.2\ V)$ or $\leq 0.2V$ $(V_{CC} = 2V)$	–	95	500	μA
t_{CDR}	Chip Deselect to Data Retention Time		0		–	ns
t_R	Operation Recovery Time		t_{RC}			ns

LOW V_{CC} DATA RETENTION WAVEFORM



4

A.C. TEST QUESTIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Timing Reference Level 1.5V

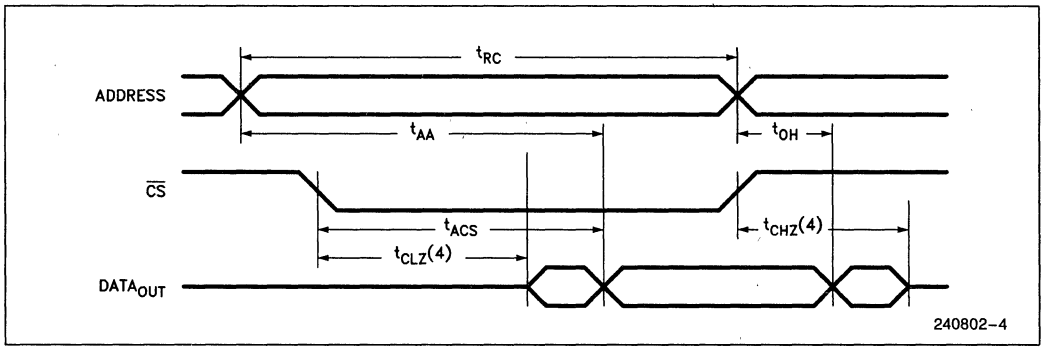
A.C. CHARACTERISTICS (T_A = 0°o to 70°oC, V_{CC} = 5V ± 10%)

READ CYCLE

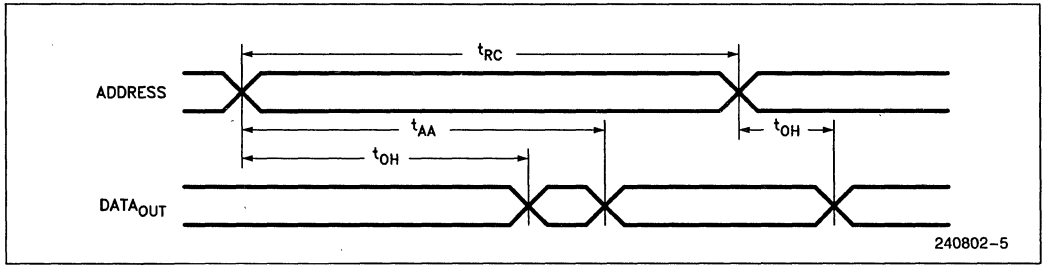
Symbol	Parameter	51258-20		51258-25		51258-30		51258-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{ACS}	Chip Select Access Time		20		25		30		35	ns
t_{OH}	Output Hold from Address Change	3		5		5		5		ns
t_{CLZ}	Chip Select to Output in Low Z	5		5		5		5		ns
t_{CHZ}	Chip Deselect to Output in High Z		15		15		20		20	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		25		30		35	ns

NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage, t_{CHZ} (Max) is less than t_{CLZ} (Min), both for a given device and from device to device.

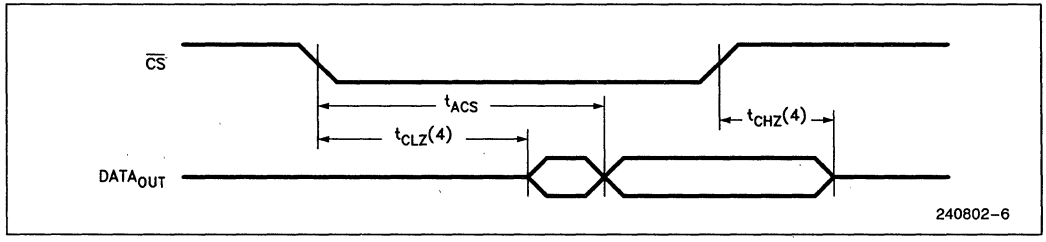
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ± 200 mV from steady state with 5 pF load (including scope and jig).

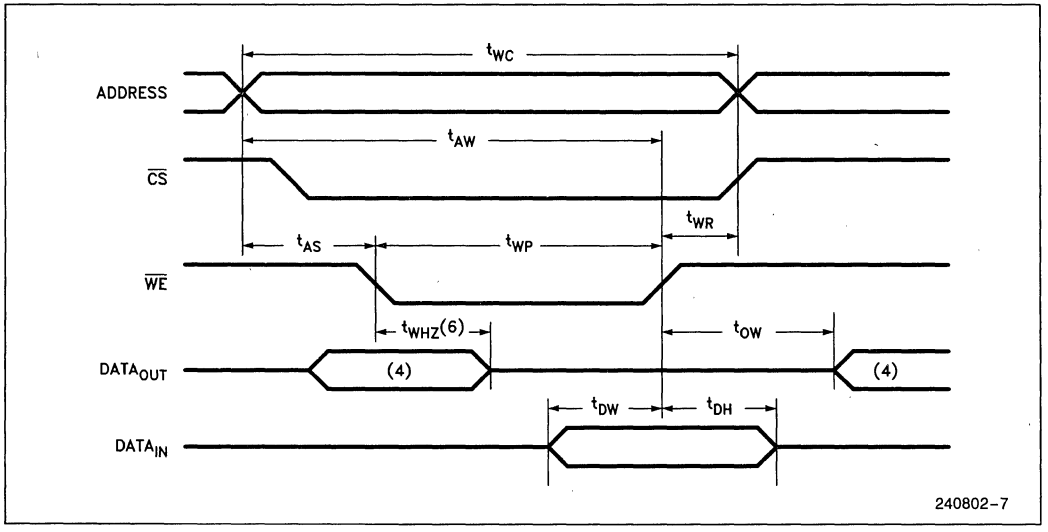
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

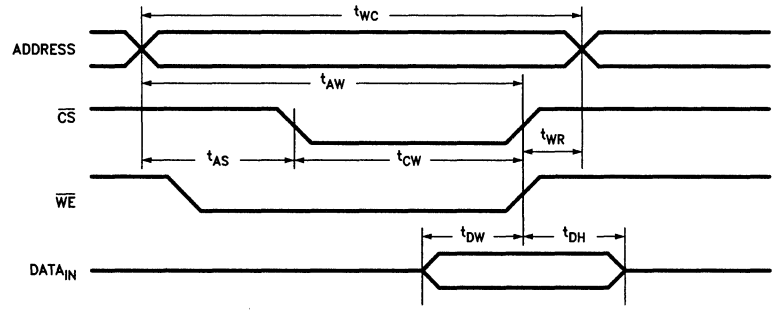
Symbol	Parameter	51258-20		51258-25		51258-30		51258-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{CW}	Chip Select to End of Write	15		20		25		25		ns
t_{AW}	Address Valid to End of Write	15		20		25		25		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	15		20		25		25		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	10		12		15		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WHZ}	Write Enable to Output in High Z	0	15	0	15	0	15	0	15	ns
t_{OW}	Output Active from End of Write	5		5		5		5		ns

4

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 6)

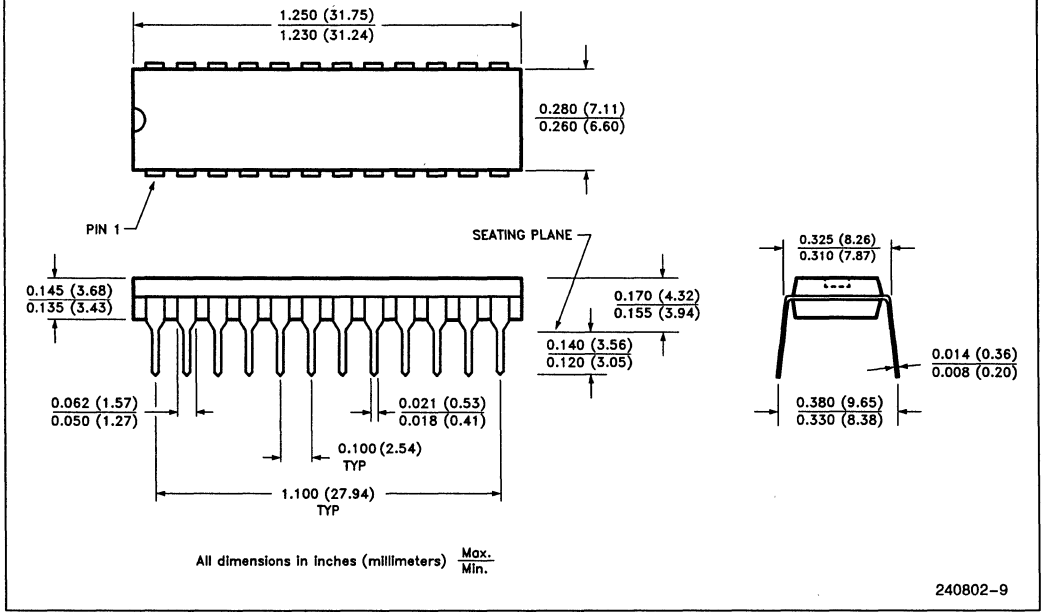


TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (^tCW or ^tWP) of a low $\overline{CS}$ and low $\overline{WE}$.
3. ^tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 200 mV from steady state with 5 pF load (including scope and jig).

PACKAGE DIMENSIONS



24-Pin Plastic Dip

August 1989

4

Static RAM Reliability Report

MADHU NIMGAONKAR
COMPONENTS CONTRACTING DIVISION
QUALITY AND RELIABILITY ENGINEERING

Order Number: 240544-001

SRAM RELIABILITY DATA SUMMARY

CONTENTS

1.0 INTRODUCTION

This report summarizes the reliability predictions of the MOS memory components and the methodology used in making the predictions. The methodology adopted by Intel is among the most conservative in the electronics industry. The reader should be aware of the different methodologies used by various manufacturers in making the reliability predictions and the profound effect a more liberal approach has on the failure rate reported.

2.0 RELIABILITY TESTS

High Temperature Burn-In

This test is used to establish infant mortality failure rates. Intel defines infant mortality as the early life failures observed after a 48 hour 125°C dynamic burn-in. In order to eliminate infant mortality fallout in determining long term failure rates, all devices used for lifetesting are subjected to standard Intel production screens plus a 48 burn-in.

High Temperature Dynamic Lifetest

This test is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures (125°C) and the use of biased operating conditions (5.5V). The translation from 125°C to 55°C is done by applying time acceleration factors based on the thermal activation energy assignments.

Failure rate calculations are given for each relevant activation energy. These are made using the appropriate activation energy and the Arrhenius Plot as shown in Figure 1. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. The failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution to arrive at a confidence level associated failure rate. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV, 0.5 eV and 1.0 eV. In cases where the mechanism of the catastrophic failures cannot be determined, 0.3 eV activation energy is assumed.

When reviewing failure rate projections from different sources, it is important to understand the assumptions being made. Small changes in details can dramatically alter an estimated failure rate.

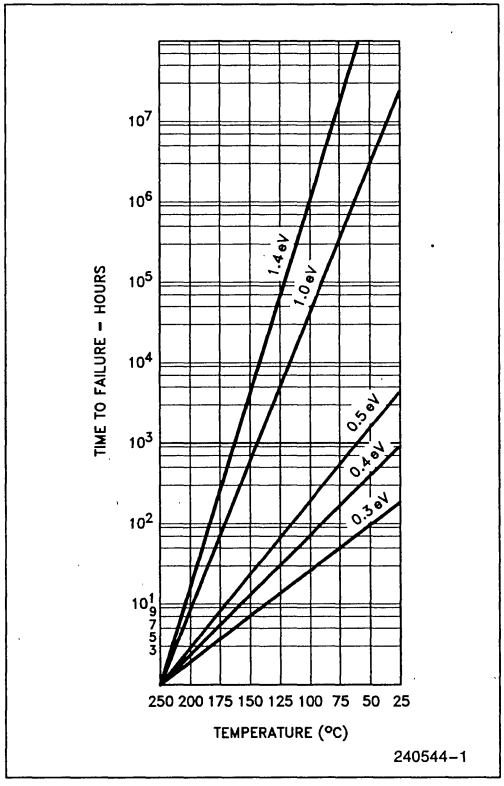


Figure 1. Arrhenius Plot

High Voltage (7V) Dynamic Lifetest

This test is used to detect failure mechanisms which are accelerated by high voltage as well as high temperature. It is especially effective in accelerating oxide and leakage related failures. The total acceleration factor includes the time acceleration factors based on the assigned activation energies and voltage acceleration factor (7V to 5.5V).

High Temperature Reverse Bias Test

This test is used to detect failure mechanisms which are accelerated by high temperature (150°C). This test is effective in accelerating leakage related failures and drifts in device parameters due to process instability.

Low Temperature Lifetest

This test is performed at maximum operating frequency to detect the effects of electron injection into the gate oxide. The conditions for electron injection occur during transitions when the transistors are in saturation.

4

High Temperature Storage Test

High temperature storage (bake) is a test in which devices are subjected to elevated temperatures (150°C for plastic packages and 250°C for hermetic packages) with no applied bias. This test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability.

Temperature Cycle Test

This test consists of cycling the temperature of a chamber housing device from −65°C to +150°C with no applied bias. Temperature cycling (1000 cycles) is used to detect mechanical reliability problems and microcracks.

3.0 RELIABILITY DATA SUMMARY

51C68

Number of bits: 16,384
Organization: 4K x 4

Process: CHMOS III
Package: 20-Pin

Table 1. Failure Rate Predictions

Actual Device Hours 125°C	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hours (60% UCL)	
		55°C	70°C		55°C	70°C
3.85E + 06	0.3	2.00E + 07	1.33E + 07	1	0.0101	0.0152
3.85E + 06	0.5	6.01E + 07	3.05E + 07	0	0.0015	0.0032
3.85E + 06	1.0	9.40E + 08	2.42E + 08	0	0.0001	0.0002
			Combined Failure Rate:		0.0117	0.0186
			FITs:		117	186

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10E + 09 device hours.

Table 2. Reliability Summary

Month	Package	125°C Dynamic Lifetest				
		48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1/86 *	Cerdip	1/1061	0/1034	0/600	0/600	—
3/86 *	Plastic	0/1536	0/1531	0/579	0/579	1/579
3/86 **	Plastic	0/150	0/150	0/150	0/150	0/150
5/86	Cerdip	0/1000	0/1000	0/150	0/150	—
6/86	Cerdip	0/879	0/868	0/150	0/150	—
9/86	Cerdip	1/1125	0/1123	0/150	0/150	—
5/87	Cerdip	0/743	0/743	0/150	0/150	—
7/87	Cerdip	0/1000	0/1000	0/150	0/150	—
7/87	Cerdip	0/769	0/769	0/200	0/200	—
7/87	Cerdip	2/675	0/673	0/200	0/200	—
Total		4/8938 (A)	0/8891 (B)	0/2479 (C)	0/2464 (D)	1/729 (E)

NOTE:
*Qual Data
**7V Qual Data

Table 3. Package Thermal Characteristics

Package Type	Junction Temp. @55°C Ambient	Junction Temp. @70°C Ambient	Junction Temp. @125°C Ambient
Cerdip	78	93	148
Plastic	91	106	161

Table 4. Failure Analysis Summary

Time Frame	Group	# Fail	Description	Ea (eV)
1/86	A	1	ISB Failure, Hot Spot on Cont. Gate Edge of Y4 Driver	0.3
9/86	A	1	Defect Not Found	0.3
7/87	A	1 1	Contamination Assembly Defect at Wire Heel	1.0 0.5
3/86	E	1	Single Bit Defect Not Found	0.3

51C98

Number of bits: 65,536
Organization: 16K x 4

Process: CHMOS IV
Package: 22-Pin

4

Table 1. High Temperature Lifetest Data

Year	Lot #	125°C (5.5V) Dynamic Lifetest				
		48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
Q4/88	27-921	3/1043	0/1040	0/890	0/890	0/890
Q4/88	22-957	0/488	1/488	1/337	0/336	2/335
Q4/88	24-985	4/759	1/755	0/604	1/604	0/603
Q4/88	26-903	2/708	0/706	1/556	0/755	1/755
Q4/88	26-910	1/999	0/997	1/847	0/845	0/845
Q1/89	40-980	0/536	0/536	0/536	0/536	—
Q1/89	42-988	1/580	1/579	0/578	0/578	—
Total		11/5113 (A)	3/5101 (B)	3/4348 (C)	1/4344 (D)	3/3228 (E)

Table 2. Failure Analysis Summary

Group	# Fail	Description	Ea (eV)
A	11	1 Ea Lost during Failure Analysis 2 Ea A1/Ti Particle in via Seam 2 Ea BPSG Crystals 1 Ea Passivation Damage 2 Ea Single Bit 1 Ea Bond Pad Corrosion 1 Ea Column Fail (M2 Particle) 1 Ea Column Fail (M1 Particle)	— 0.3 0.3 0.5 0.5 1.0 0.3 0.3
B	3	1 Ea Single Bit (Poly Extra) 1 Ea EOS (Electrical Overstress) 1 Ea Open (Lifted Bond)	0.3 — 1.0
C	3	2 Ea Single Bit 1 Ea Open (Lifted Bond)	0.3 1.0
D	1	1 Ea Single Bit	0.3
E	3	1 Ea Passivation Damage 1 Ea Leakage 1 Ea Metal 2 Input Open	0.5 0.3 0.5

Table 3. High Voltage Lifetest Data

Year	Lot #	High Voltage (7V) Dynamic Lifetest				
		48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
Q4/88	27-921	2/599	1/597	2/596	1/593	0/592
Q4/88	22-957	0/200	0/200	0/200	3/200	0/197
Q4/88	24-985	0/379	0/379	0/379	1/379	0/378
Q4/88	26-903	2/354	1/350	2/348	0/346	0/346
Q4/88	26-910	3/513	1/509	0/508	0/508	1/508
Q1/89	40-980	1/268	0/267	0/267	0/267	—
Q1/89	42-988	0/291	1/291	0/290	0/290	—
Total		8/2604 (A)	4/2593 (B)	4/2588 (C)	5/2583 (D)	1/2021 (E)

Table 4. Failure Analysis Summary

Group	# Fail	Description	Ea (eV)
A	8	1 Ea for Abnormal Contact 2 Ea A1/Ti in via Seam 3 Ea BPSG Crystals 1 Ea BPSG Crystal 1 Ea Column Fail (M2 Particle)	0.5 0.3 0.3 0.3 0.3
B	4	1 Ea Bond Pad Corrosion 1 Ea ISB Leakage (Corrosion) 1 Ea BPSG Crystal 1 Ea Single Bit	0.5 0.5 0.3 0.3
C	4	2 Ea BPSG Crystals 1 Ea Column (Passivation Damage) 1 Ea Column Fail	0.3 0.5 0.3
D	5	4 Ea Lifted Bond 1 Ea Passivation Damage	1.0 0.5
E	1	1 Ea Metal 2 Input Open	0.5

Table 5. Failure Rate Predictions

	125°C Actual Device Hours	Ea (eV)	Equivalent Hours at 55°C	# Fail	FIT Rate (60% UCL)	Total FIT Rate
5.5V	7.48E + 06	0.3	4.41E + 07	5	0.0142	165
	7.48E + 06	0.5	14.2E + 07	2	0.0022	
	7.48E + 06	1.0	26.9E + 08	2	0.0001	
7.0V	4.46E + 06	0.3	11.8E + 07	5	0.0053	130
	4.46E + 06	0.5	8.47E + 07	5	0.0074	
	4.46E + 06	1.0	16.1E + 08	4	0.0003	
Totals (**)	11.9E + 06	0.3	16.2E + 07	10	0.0071	110
	11.9E + 06	0.5	22.7E + 07	7	0.0037	
	11.9E + 06	1.0	43.0E + 08	6	0.0002	

*48 Hour failures at 125°C are not included in long term failure rate calculations.
**5.5V and 7V burn-in/lifetest equivalent hours have been combined.

Temp. with Tja

T (55) = 338K
T (125) = 408K

K = 8.62E −05 eV/K

		Thermal Accel. Factors 55°C
BI/ELT Accel. Factors:	0.3 eV	5.90
	0.5 eV	19.0
	1.0 eV	360

Voltage Accel. Factor: 4.48

NOTE:
FIT = Failures in Time. 1 FIT = 1 Failure per 10E + 09 device hours.

Table 6. Infant Mortality Evaluation Results

Year	Lot #	High Temperature (7V) Burn-In				
		6 Hrs	12 Hrs	24 Hrs	48 Hrs	168 Hrs
Q1/89	42-995	0/672	0/672	0/672	1/672	0/671
Q1/89	44-997	0/688	0/688	0/688	0/688	0/688
Q1/89	45-900	1/655	0/654	0/654	0/654	0/654
Q1/89	48-909	0/614	0/614	0/614	0/614	0/614
Total		1/2629 (A)	0/2628	0/2628	0/2627 (B)	0/2627

Failure Analysis
A) 1 Ea Func. fail (Metal 1 particle)
B) 1 Ea Invalid Failure (Cracked Package)

Table 7. Additional Qualification Tests

Year	Low Temp (−10°C) Lifetest (2K Hrs)	150°C HTRB 1K Hrs.	Temp Cycle 1K Cycles	160°C 1000 Hrs. Bake
1988/89	0/120	5/240 (A)	0/250	1/200 (B)

Failure Analysis

A) 1 Ea Passivation damage
1 Ea Func. fail @ <2.6V
1 Ea Open (Lifted Bond)
1 Ea Blown V_{SS} Pin
1 Ea Healed

B) 1 Ea Open (Lifted Bond)

APPENDIX A
COMMON MOS FAILURE MECHANISMS

Oxide Defects

Oxide defects can cause dielectric breakdown in MOS structures resulting in an electrical short. Oxide dielectric breakdown is dependent on time, ambient temperature and operating voltage. Oxide defects could be induced by excessively thin oxide, polarization and contamination. The thermal activation energy for oxide defects is determined to be 0.3 eV.

Silicon Defects

Silicon defects are inherent in the unprocessed silicon wafers and may also be generated by stresses on the lattice during MOS processing. These silicon defects enhance parasitic leakage when they become active by "gettering" contaminants. The activation energy for silicon defects is determined to be 0.5 eV.

Contamination

MOS circuits can fail due to threshold voltage (Vt) shifts when subjected to mobile ionic contamination. This ionic contamination reaches critical circuits through passivation defects subsequent to wafer processing. Sodium is the most common species of ionic contamination. The activation energy of ionic contamination is 1.0 eV.

Metallization Defects

Metallization defects (defects relating to metal conductor paths on the semiconductor die) can occur due to metal contamination, excess current density (electromigration) in the conductors, microcracks caused by sharp oxide steps and overalloying due to migration of metal through the semiconductor's contact. The activation energy is 0.5 eV.

EPROMs (Erasable Programmable Read Only Memories)

5

2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - **— 2716-1: 350 ns Max**
  - **— 2716-2: 390 ns Max**
  - **— 2716: 450 ns Max**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— Active Power: 525 mW Max**
  - **— Standby Power: 132 mW Max**
- **Pin Compatible to Intel "Universal Site" EPROMs**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Completely Static**

The Intel 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single-address programming. It makes designing with EPROMs fast, easy and economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with high-performance +5V microprocessors such as Intel's 8085 and 8086. Selected 2716-5s and 2716-6s are also available for slower speed applications. The 2716 also has a static standby mode which reduces power consumption without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 uses a simple and fast method for programming—a single TTL-level pulse. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Programming of any location at any time—either individually, sequentially or at random is possible with the 2716's single-address programming. Total programming time for all 16,384 bits is only 100 seconds.

5

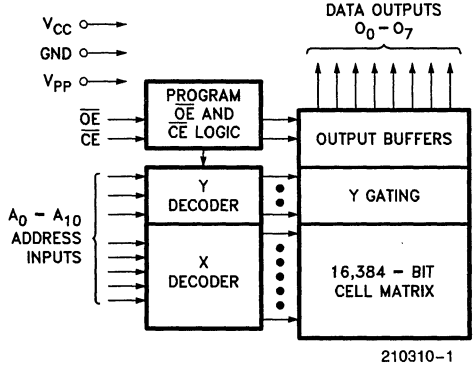


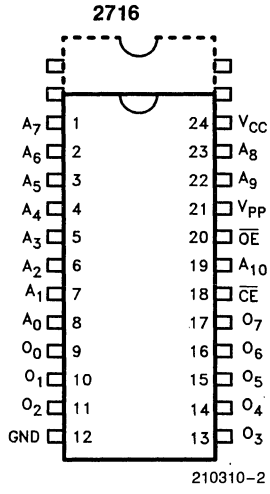
Figure 1. Block Diagram

Pin Names

A_0–A_{10}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs

September 1989
Order Number: 210310-003

27512 27C512	27256 27C256	27128A 27C128	2764A 27C64 87C64	2732A
A_{15}	V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



2732A	2764A 27C64 87C64	27128A 27C128	27256 27C256	27512 27C512
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A_{14}	A_{14}
V_{CC}	N.C.	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2716 pins.

Figure 2. Cerdip Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
I	−40°C to +85°C	44

EXPRESS OPTIONS

2716 Versions

Packaging Options	
Speed Versions	**Cerdip**
−1	Q
STD	Q, I

DEVICE OPERATION

The six modes of operation of the 2716 are listed in Table 1. It should be noted that inputs for all modes are TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The 2716 has a standby mode which reduces the maximum active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because 2716s are usually used in larger memory arrays, Intel has provided a 2-line control function that accommodates this use of multiple memory connections. The two-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 18) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low-power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active-high, TTL program pulse is applied to the $\overline{CE}$ input. A pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

5

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Output Disable	V_{IL}	V_{IH}	+5	+5	High Z
Standby	V_{IH}	X	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

NOTE:
1. X can be V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground ..... +6V to −0.3V
V_{PP} Supply Voltage with Respect
to Ground During Program ..... +26.5V to −0.3V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	2716	2716-1	2716-2
Temperature Range	0°C–70°C	0°C–70°C	0°C–70°C
V_{CC} Power Supply(1, 2)	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply(2)	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}(2)	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}(2)	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}(2)	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

A.C. CHARACTERISTICS

Symbol	Parameter	Limits (ns)						Test Conditions†
		2716		2716-1		2716-2		
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		450		350		390	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390	$\overline{OE}$ = V_{IL}
t_{OE}(4)	Output Enable to Output Delay		120		120		120	$\overline{CE}$ = V_{IL}
t_{DF}(4, 6)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	100	0	100	0	100	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2716s.

Program Inhibit

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL-level program pulse applied to a 2716's $\overline{CE}$ input with V_{PP} at 25V will program that 2716. A low-level $\overline{CE}$ input inhibits the other 2716 from being programmed.

Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room-level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure.

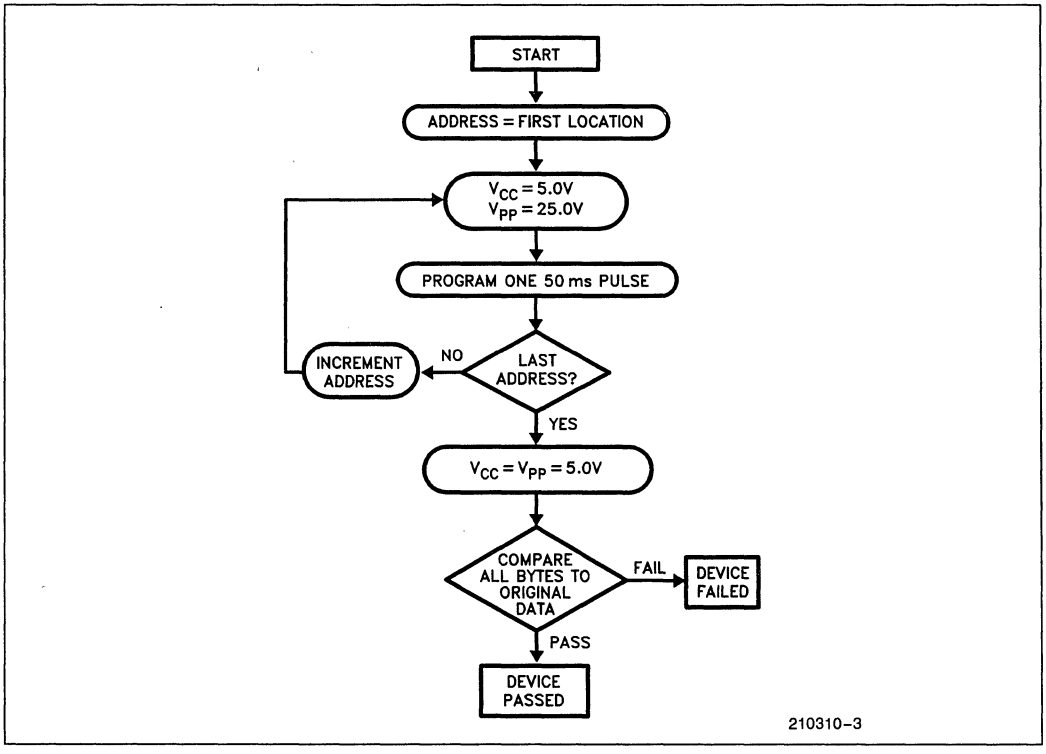


Figure 3. Standard Programming Flowchart

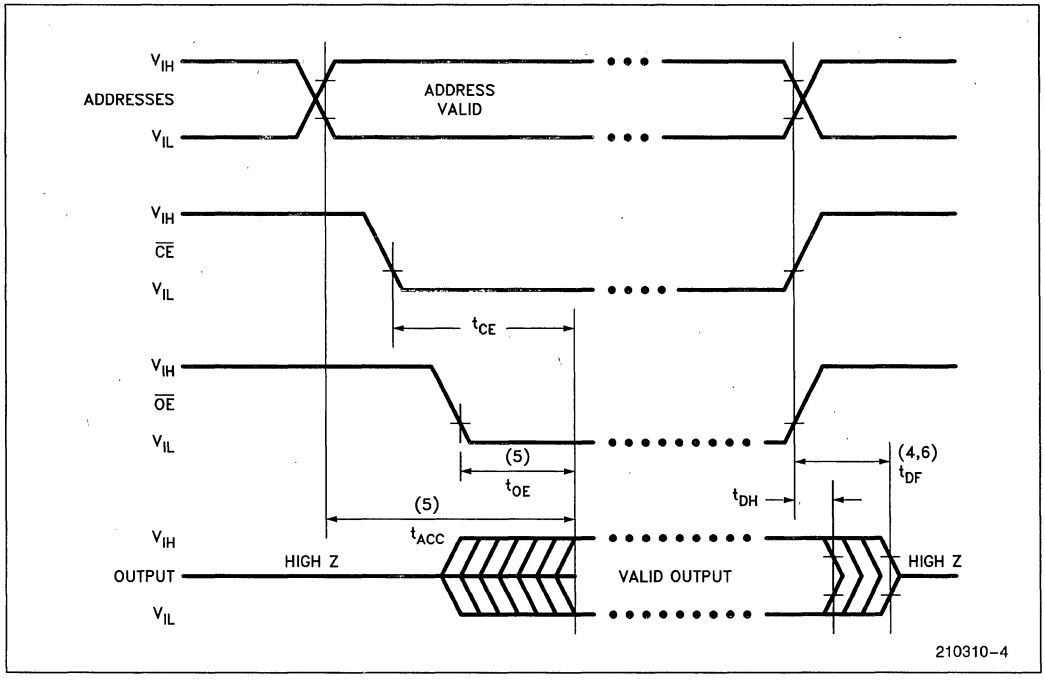
CAPACITANCE[4] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[3]	Max	Unit	Test Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

†A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times ..... ≤20 ns
Input Pulse Levels ..... 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs ..... 0.8V and 2V
Outputs ..... 0.8V and 2V

A.C. WAVEFORMS[1]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING CHARACTERISTICS

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$, V_{CC}(1) $= 5V \pm 5\%$, V_{PP}(1, 2) $= 25V \pm 1V$

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	$V_{IN} = 5.25V/0.45$
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE} = V_{IL}$
I_{PP2}	V_{PP} Supply Current during Programming Pulse			30	mA	$\overline{CE} = V_{IH}$
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	−0.1		0.8	V	
V_{IH}	Input High Level	2.0		$V_{CC} + 1$	V	

A.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$, V_{CC}(1) $= 5V \pm 5\%$, V_{PP}(1, 2) $= 25V \pm 1V$

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions*
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		200	ns	$\overline{CE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			200	ns	$\overline{CE} = V_{IL}$
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

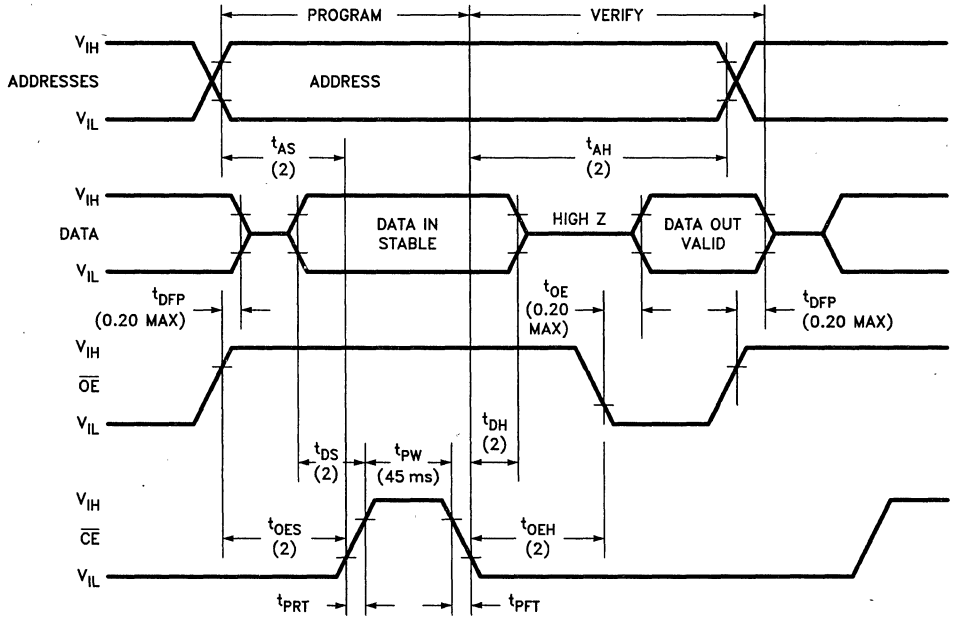
5

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.8V to 2.2V
Input Timing Reference Level ..... 0.8V and 2V
Output Timing Reference Level ..... 0.8V and 2V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

PROGRAMMING WAVEFORMS



NOTES:
1. All times shown in parenthesis are minimum times and are μs unless otherwise noted.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

REVISION HISTORY

Number	Description
03	Deleted -5 and -6 speed bins. Added Express options. Added Standard Programming Flowchart. Revised Pin Configuration and Block Diagram.

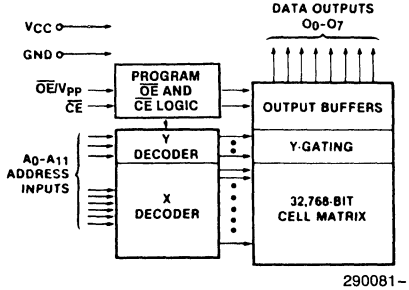
2732A
32K (4K x 8) UV ERASABLE PROMS

- **200 ns (2732A-2) Maximum Access Time ... HMOS*-E Technology**
- **Compatible with High-Speed Microcontrollers and Microprocessors ... Zero WAIT State**
- **Two Line Control**
- **10% V_{CC} Tolerance Available**
- **Low Current Requirement**
  −100 mA Active
  −35 mA Standby
- **int$_e$ligent Identifier™ Mode**
  −Automatic Programming Operation
- **Industry Standard Pinout ... JEDEC Approved 24 Pin Ceramic Package**
  (See Packaging Spec. Order #231369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE}$ = V_{IH}) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.



290081-1

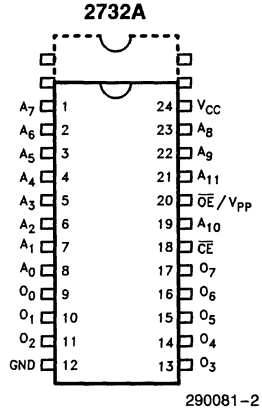
Figure 1. Block Diagram

Pin Names

A_0-A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
O_0-O_7	Outputs

5

27512 27C512	27256 27C256	27128A 27C128	2764A 27C64 87C64	2716
A_{15}	V_{PP}	V_{PP}	V_{PP}	
A_{12}	A_{12}	A_{12}	A_{12}	
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290081-2

2716	2764 2764A 87C64	27128A 27C128	27256 27C256	27512 27C512
	V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A_{14}	V_{CC} A_{14}
V_{CC}	N.C.	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip Pin Configuration

September 1989
Order Number: 290081-004

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A Min	TD2732A LD2732A Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. Maximum current value is with outputs O_0 to O_7 unloaded.

EXPRESS EPROM PRODUCT FAMILY

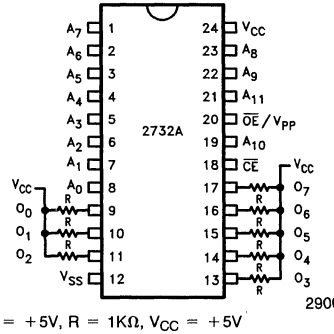
PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

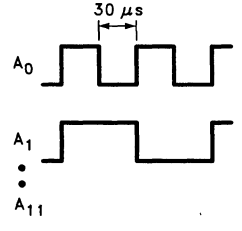
2732A Versions

Packaging Options	
Speed Versions	**Cerdip**
−2	Q
−25	Q, T, L



290081-3

$\overline{OE}/V_{PP} = +5V$, R = 1KΩ, $V_{CC} = +5V$
V_{SS} = GND, $\overline{CE}$ = GND



290081-4

Binary Sequence from A_0 to A_{11}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. During Read .....0°C to +70°C
Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
All Input or Output Voltages with Respect to Ground.....−0.3V to +6V
Voltage on A9 with Respect to Ground.....−0.3V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .....−0.3V to +22V
V_{CC} Supply Voltage with Respect to Ground .....−0.3V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(2)	V_{CC} Current (Standby)			35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(2)	V_{CC} Current (Active)			100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

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A.C. CHARACTERISTICS $0°C \le T_A \le 70°C$

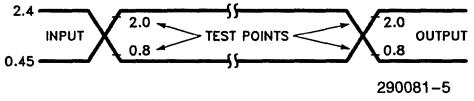
Versions	$V_{CC} \pm 5\%$	2732A-2		2732A		Units	Test Conditions
	$V_{CC} \pm 10\%$	2732A-20		2732A-25			
Symbol	Parameter	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		70		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}/V_{PP}$ High to Output Float	0	60	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}(4)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE (2) T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

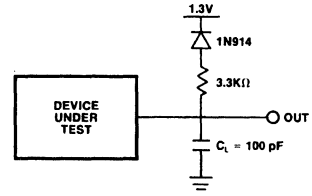
A.C. TESTING INPUT/OUTPUT WAVEFORM



290081-5

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

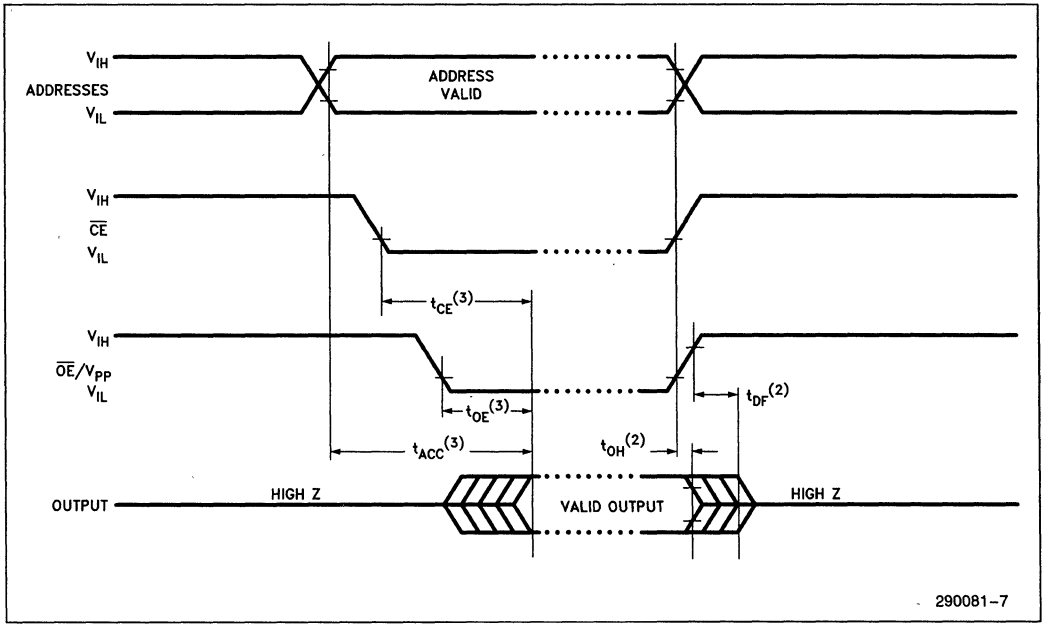
A.C. TESTING LOAD CIRCUIT



290081-6

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



290081-7

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{CE}.

DEVICE OPERATION

The modes of operation of the 2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming and 12V on A_9 for the int$_e$ligent Identifier™ mode. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read/Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	X	V_{CC}	High Z
Int$_e$ligent Identifier(3)						
—Manufacturer	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	89H
—Device	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	01H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12V ±0.5V.
3. A_1–A_8, A_{10}, A_{11} = V_{IL}.

Read Mode

The 2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum active current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) The lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's two-line control and by use of properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for

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every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

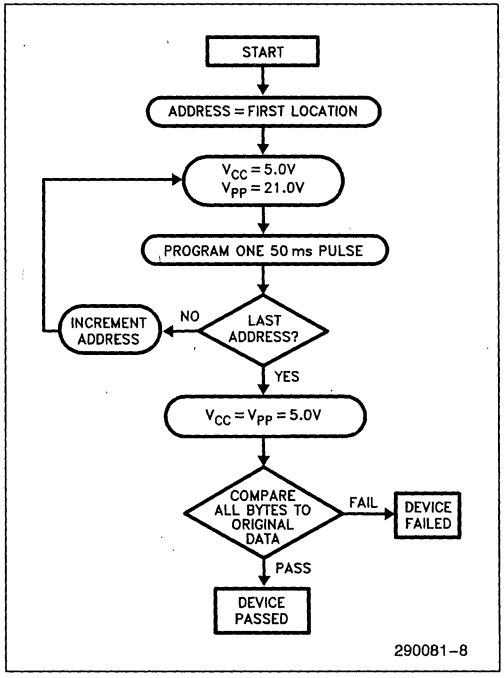


Figure 3. Standard Programming Flowchart

PROGRAMMING MODES

CAUTION: Exceeding 22V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure (cerdip EPROMs), all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" in cerdip EPROMs is by ultraviolet light erasure.

The device is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 20 ms (50 ms typical) active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed (see Figure 3). Any location can be programmed at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high level $\overline{CE}$ input inhibits the other EPROMs from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that selected device.

Program Verify

A verify (Read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions (Note 1)
		Min	Typ(3)	Max		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	I_{OH} = −400 μA
I_{CC2}(4)	V_{CC} Supply Current (Program and Verify)		85	100	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 inteligent Identifier Voltage	11.5		12.5	V	

5

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

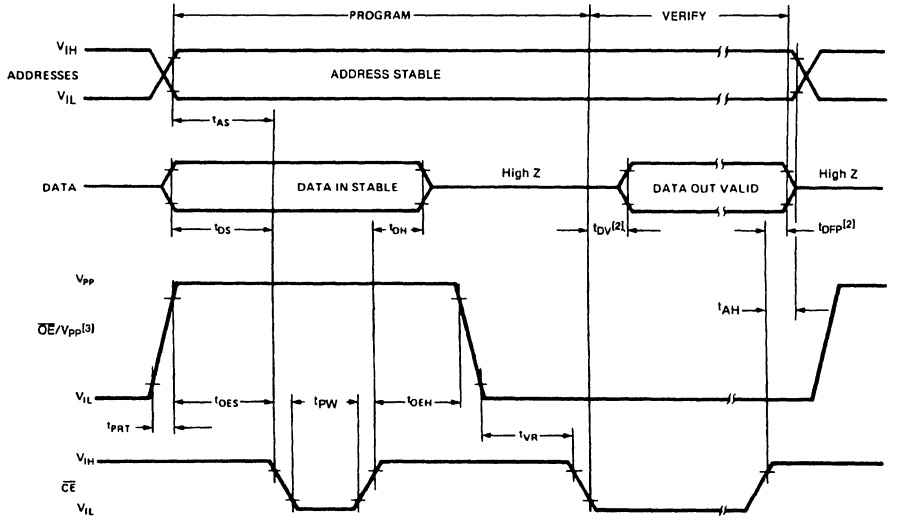
Symbol	Parameter	Limits			Units	Test Conditions* (Note 1)
		Min	Typ(3)	Max		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Not Driven	0		130	ns	(Note 2)
t_{PW}	$\overline{CE}$ Pulse Width During Programming	20	50	55	ms	
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{IL}$
t_{VR}	V_{PP} Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

*A.C. TEST CONDITIONS

Input Rise and Fall Time (10% to 90%) ..... ≤20 ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V and 2.0V
Output Timing Reference Level .....0.8V and 2.0V

PROGRAMMING WAVEFORMS



290081-9

NOTES:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

5

REVISION HISTORY

Number	Description
04	Revised Pin Configuration. Revised Express Options. Deleted −3, −30, −4, and −45 speed bins.

2764A
64K (8K x 8)
UV ERASABLE PROMs

- **Fast Access Time—HMOS* II E — 180 ns Cerdip D2764A-1**
- **Moisture Resistant**
- **Two-line Control**
- **int$_e$ligent Identifier™ Mode**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Package**
  (See Packaging Spec, Order #231369)

The Intel 2764A is a 5V only, 65,536-bit electrically programmable read-only memory (EPROM). The 2764A is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, power consumption, reliability and producibility.

The 2764A provides access times to 180 ns (2764A-1). This is compatible with high-performance microprocessors, such as Intel's 8 MHz iAPX 186 allowing full speed operation without the addition of WAIT states. The 2764A is also directly compatible with the 12 MHz 8051 family.

Two-line control and JEDEC-approved, 28 pin packaging are standard features of Intel higher density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between non-volatile memory alternatives.

*HMOS is a patented process of Intel Corporation.

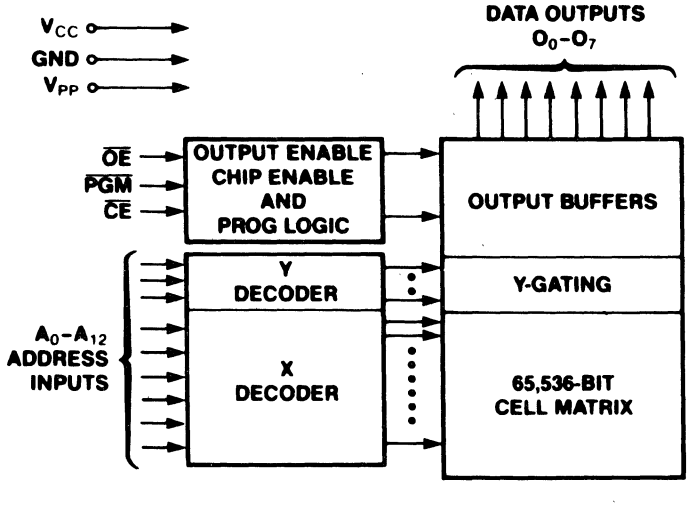


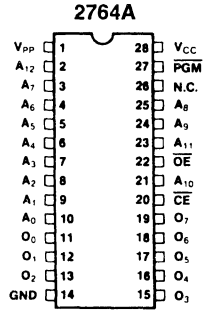
Figure 1. Block Diagram

September 1989
Order Number: 230864-006

Pin Names

A_0–A_{12}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
N.C.	No Connect

27512 27C512	27256 27C256	27128A 27C128	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



230864-2

2716	2732A	27128A 27C128	27256 27C256	27512 27C512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}
V_{CC}	V_{CC}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the 2764A pins.

Figure 2. Cerdip Pin Configuration

5

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2764A VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
−20	Q, T, L

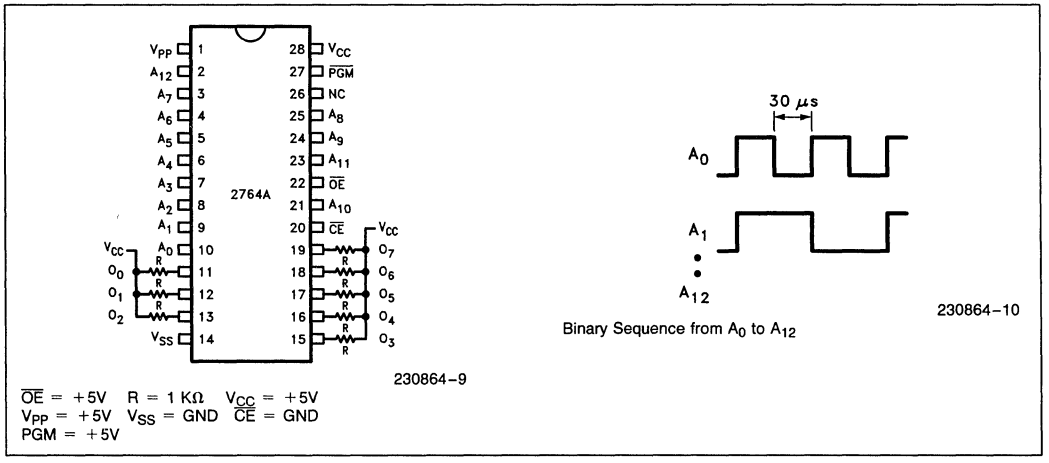
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2764A LD2764A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		40	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		75	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-in Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Inputs or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with
Respect to Ground
During Programming ..... −0.6V to +14.0V
V_{CC} Supply Voltage with Respect
to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Unit	
I_{LI}	Input Load Current		10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 0V to V_{CC}
I_{PP}(2)	V_{PP} Current Read		5	mA	V_{PP} = 5.5V
I_{SB}	V_{CC} Current Standby		35	mA	$\overline{CE}$ = V_{IH}
I_{CC}(2)	V_{CC} Current Active		75	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
V_{PP}(2)	V_{PP} Read Voltage	3.8	V_{CC}	V	V_{CC} = 5.0V ± 0.25V

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(4)	V_{CC} ± 5%	2764A-1		2764A-2		2764A		Unit	Test Conditions
	V_{CC} ± 10%			2764A-20		2764A-25			
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		180		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		180		200		250	ns	$\overline{OE}$ = V_{IL}
t_{OE}	$\overline{OE}$ to Output Delay		65		75		100	ns	$\overline{CE}$ = V_{IL}
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	55	0	55	0	60	ns	$\overline{CE}$ = V_{IL}
t_{OH}(3)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

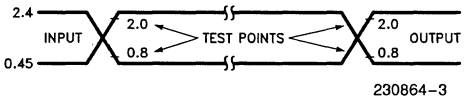
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. Model Number Prefixes: No prefix = CERDIP.

5

CAPACITANCE[2] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ [1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

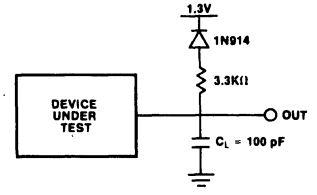
A.C. TESTING INPUT/OUTPUT WAVEFORM



230864-3

A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

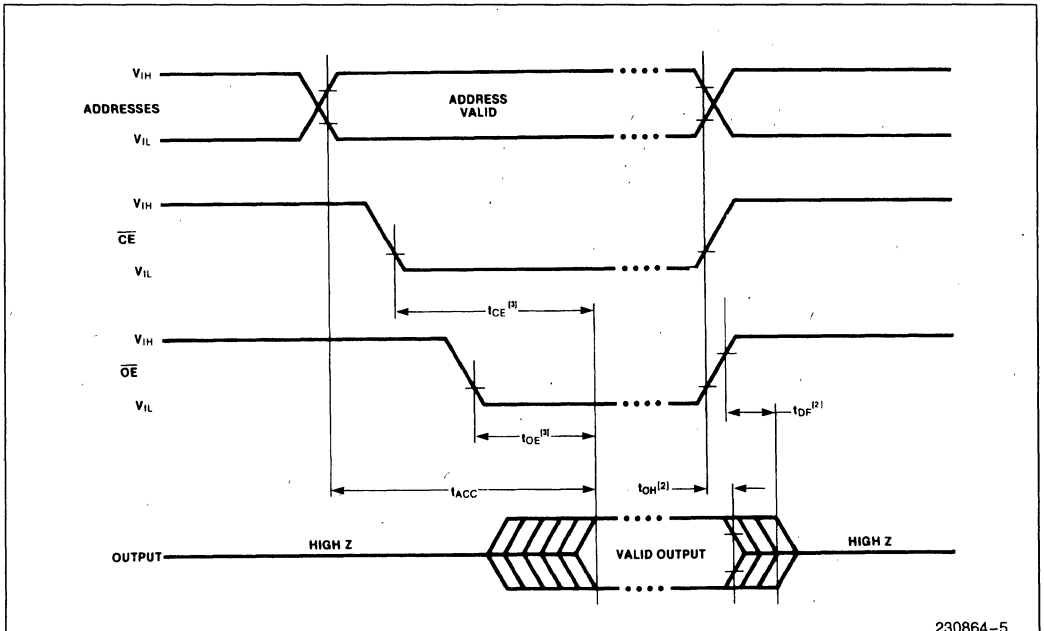
A.C. TESTING LOAD CIRCUIT



230864-4

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



230864-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 2764A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent identifier mode.

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	High Z
int$_e$ligent Identifier(3) —manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89H
—device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	08H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1–A_8, A_{10}–$A_{12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 2764A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

5

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage (see Table 2) will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1(A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The EPROM should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the EPROM to high intensity UV light for longer periods may cause permanent damage.

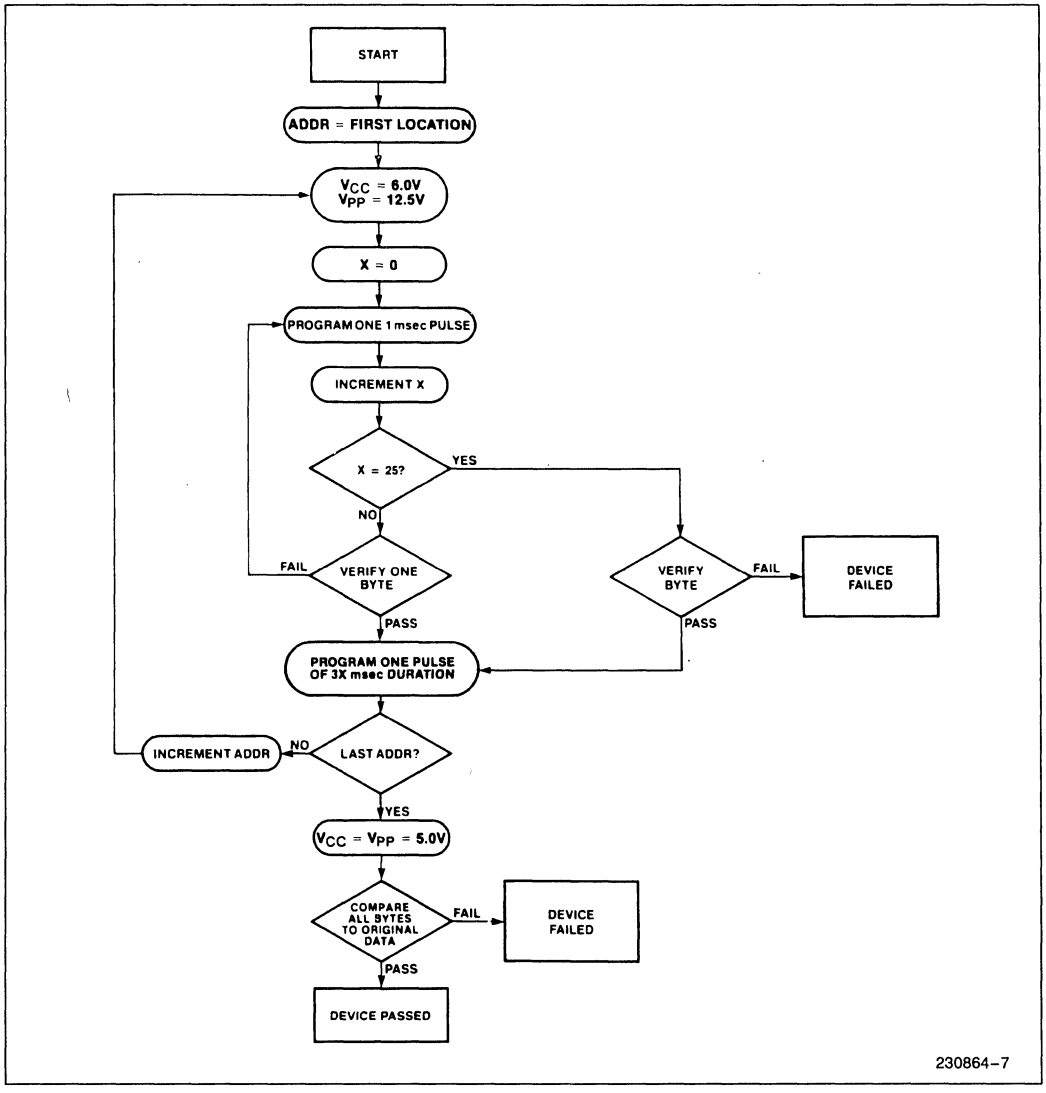


Figure 3. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, is required for all of Intel's 12.5V CERDIP EPROMs. Plastic EPROMs may also be programmed using this method. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 3.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

Table 2

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output HIgh Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		75	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

Symbol	Parameter	Limits				Test Conditions* (see Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(see Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times
(10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.45V to 2.4V

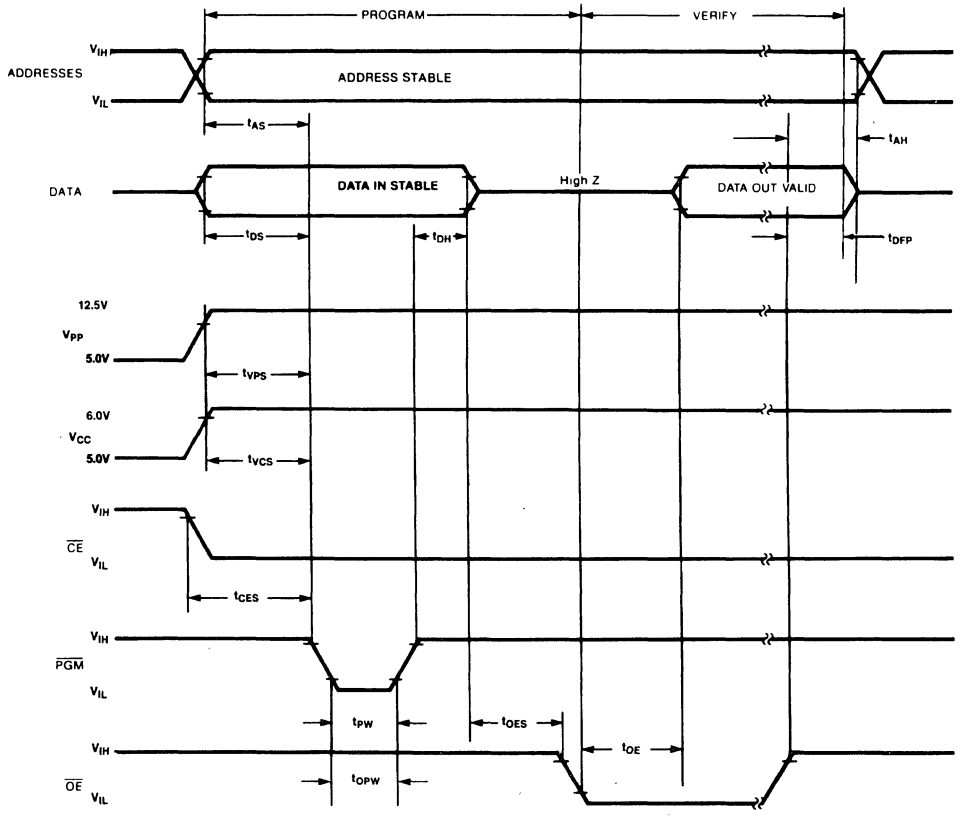
Input Timing Reference Level ..... 0.8V and 2.0V

Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with Outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2764A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

REVISION HISTORY

Number	Description
06	Deleted Plastic DIP package. Deleted QuickPulse sections. Revised Pin Configuration. Revised Express options. Deleted −3, −30, −4 and −45 speed bins. D.C. Characteristics - I_{LI} Conditions are V_{IN} = **0V to V_{CC}** D.C. Characteristics - I_{LO} Conditions are V_{OUT} = **0V to V_{CC}**

27128A
128K (16K x 8) PRODUCTION AND UV ERASABLE PROMs

- **Fast 150 nsec Access Time**
  — HMOS* II-E Technology
- **Low Power**
  — 100 mA Maximum Active
  — 40 mA Maximum Standby
- **int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **±10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec, Order #231369)

The Intel 27128A is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128A is fabricated with Intel's HMOS* II-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

The 27128A is currently available in the CERDIP package providing flexibility in prototyping and R&D environments where reprogrammability is required.

The 27128A is available in fast access times including 150 ns (27128A-1). This ensures compatibility with high-performance microprocessors, such as Intel's 8 MHz 80186 allowing full speed operation without the addition of WAIT states. The 27128A is also directly compatible with the 12 MHz 8051 family.

*HMOS is a patented process of Intel Corporation.

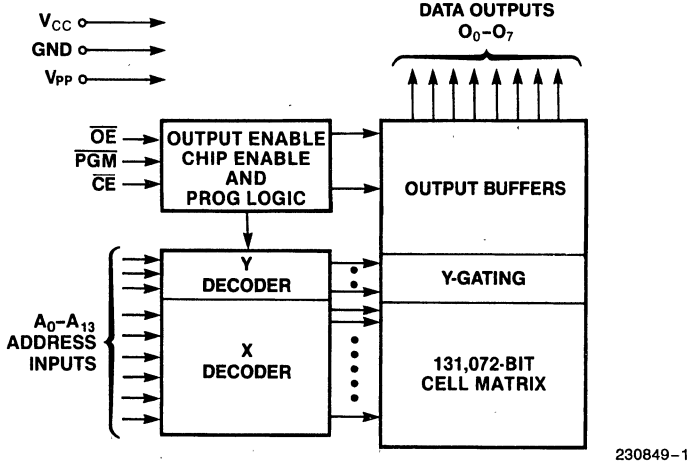


Figure 1. Block Diagram

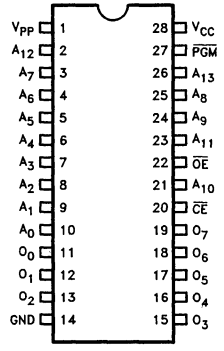
October 1990
Order Number: 230849-009

Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

27512 27C512	27256 27C256	2764A 27C64 87C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27128A



230849-2

2716	2732A	2764A 27C64 87C64	27256 27C256	27512 27C512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128A Pins

Figure 2. Cerdip(D) DIP Pin Configuration

5

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27128A Versions

Packaging Options	
Speed Versions	**Cerdip**
-20	T, L, Q

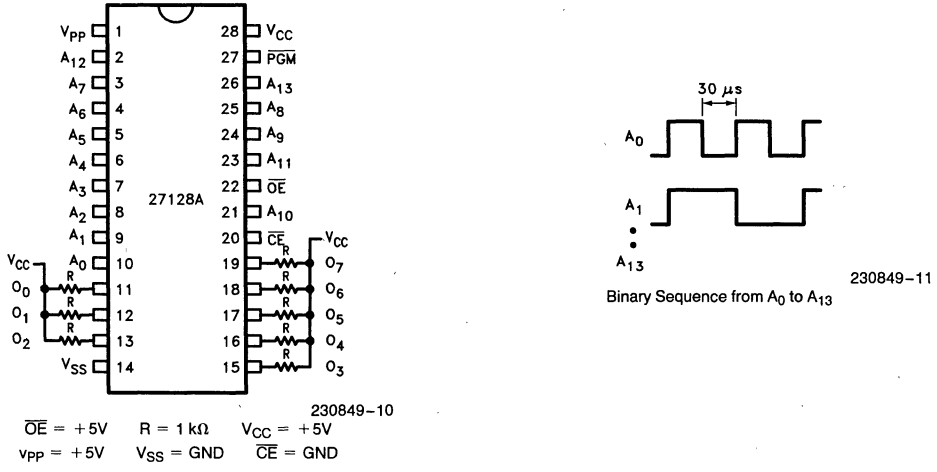
READ OPERATION

DC CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27128A, LD27128A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with Outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.25V

Voltage on A_9 with Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Notes	Limits			Units	Conditions
			Min	Typ(3)	Max		
I_{LI}	Input Load Current				10	µA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current				10	µA	$V_{OUT} = 0V$ to V_{CC}
I_{PP1}	V_{PP} Current Read	2			5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby				40	mA	$\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Current Active	2			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		+0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -400$ µA
V_{PP}	V_{PP} Read Voltage	2	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25$

AC CHARACTERISTICS $0°C \le T_A \le +70°C$

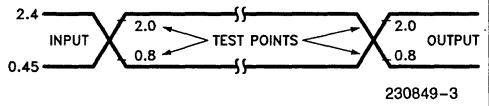
Versions(5)	$V_{CC} \pm 5\%$	Notes	27128A-1		27128A-2		27128A		Unit
	$V_{CC} \pm 10\%$				27128A-20		27128A-25		
Symbol	Characteristics		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay			150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay			65		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	4	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	4	0		0		0		ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

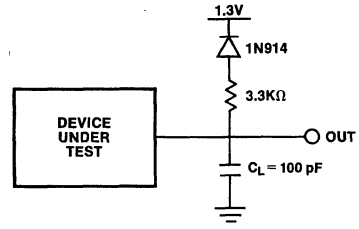
AC TESTING INPUT/OUTPUT WAVEFORM



230849-3

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

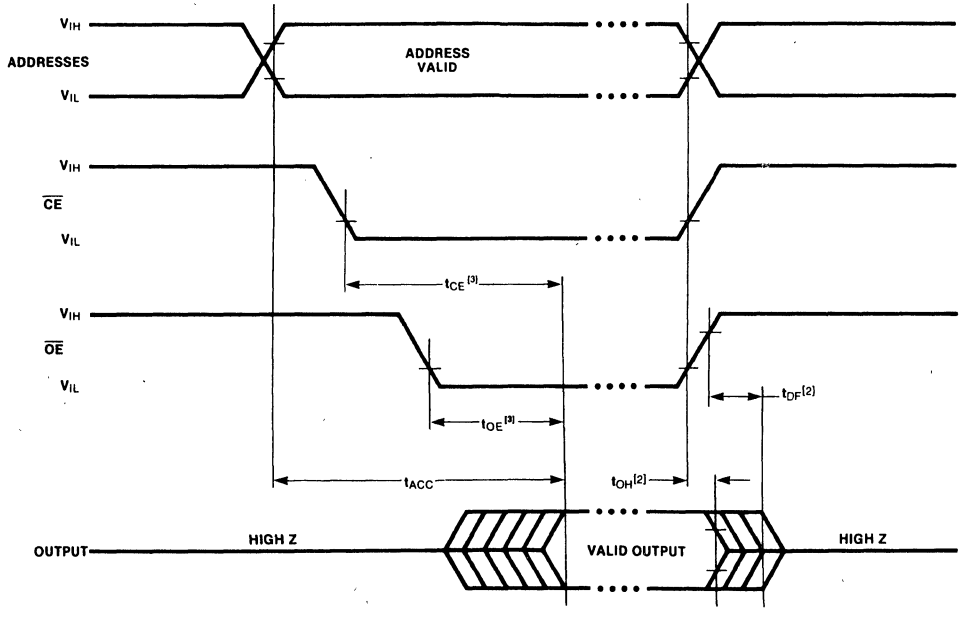
AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

230849-4

AC WAVEFORMS



230849-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier.

Table 1. Modes Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	D_{OUT}
Output Disable			V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		4	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.0V	D_{IN}
Program Verify		4	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.0V	D_{OUT}
Program Inhibit		4	V_{IH}	X	X	X	X	V_{PP}	6.0V	High Z
inteligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{CC}	5.0V	89 H
	Device	2, 3	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	5.0V	89 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27128A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

5

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

inteligent Identifier Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

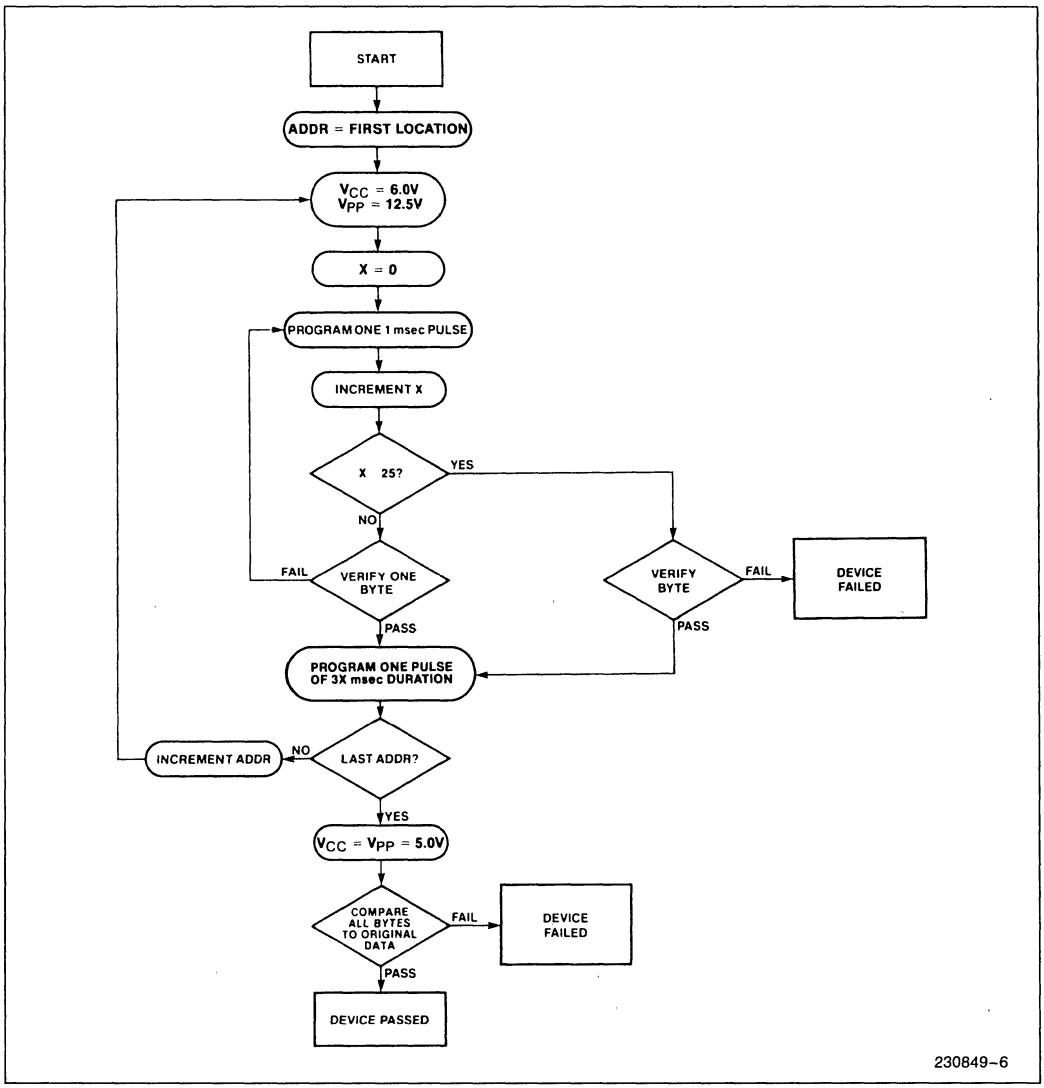


Figure 3. int$_e$ligent Programming Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming™ Algorithm, a standard in the industry for the past few years, is required for the 27128A. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 3.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

5

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

AC PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

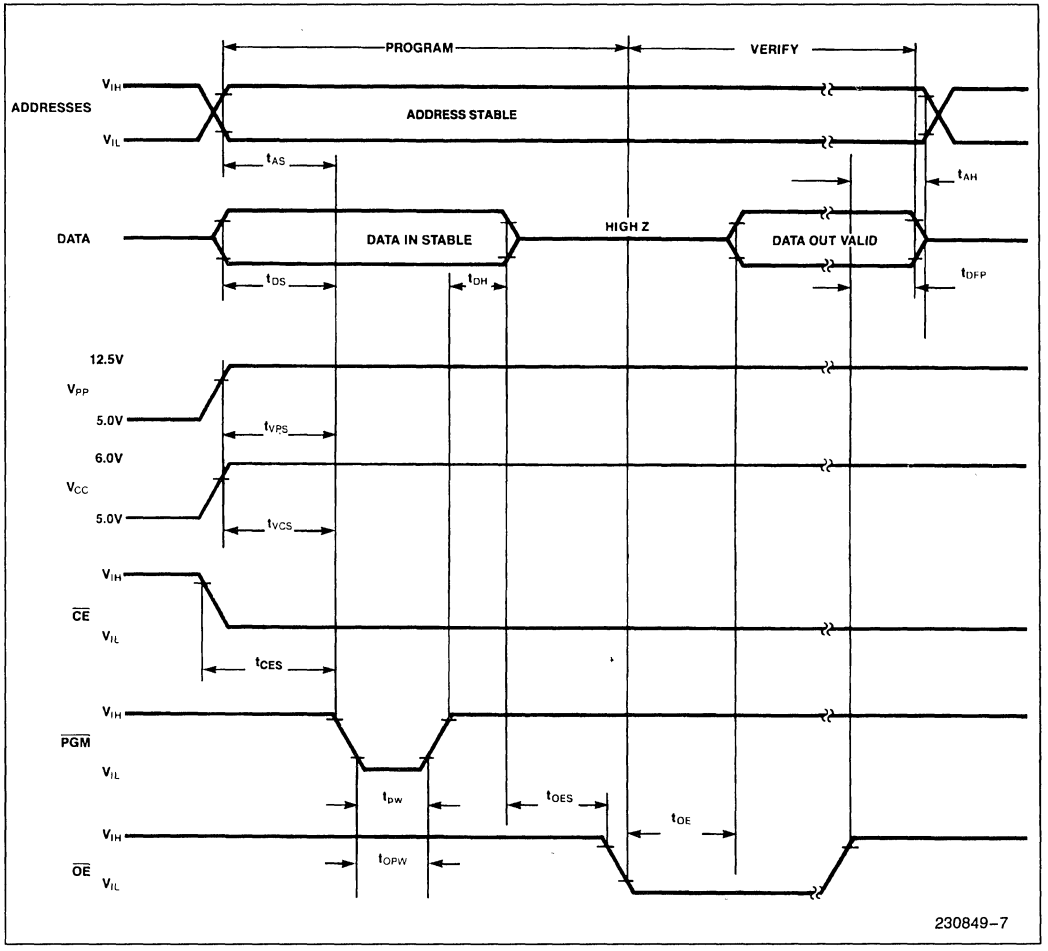
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

REVISION HISTORY

Number	Description
009	Removed Plastic Package

27256
256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
  - **— 4 Second Programming**
  - **— int$_e$ligent Programming™ Algorithm Compatible**
- **Fast Access Time**
  - **— 170 ns D27256-1**
  - **— 200 ns P27256-2**
- **int$_e$ligent Identifier™ Mode**
- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package**

(See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

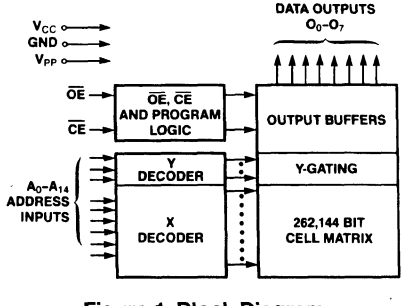
The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and elminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.



290097-1

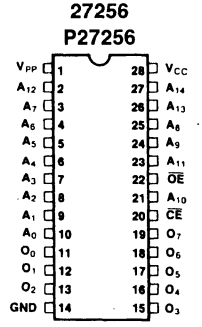
Figure 1. Block Diagram

September 1989
Order Number: 290097-004

Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
N.C.	No Connect

27512 27C512	27128A 27C128	2764A 27C64 87C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290097-2

2716	2732A	2764A 27C64 87C64	27182A 27C128	27512 27C512
		V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC}
				A_{14}
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel"Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

5

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27256 VERSIONS

Packaging Options	
Speed Versions	Cerdip
-20	Q, T, L

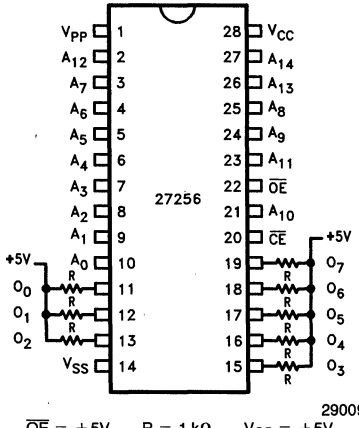
READ OPERATION

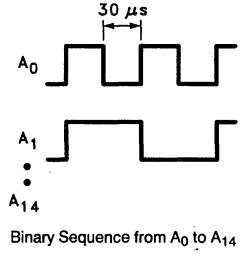
D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27256 LD27256		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.





Binary Sequence from A_0 to A_{14}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect
to Ground ..... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	27256-1, 27256-2, 27256-20, P27256-2 Limits			27256-25, 27256, P27256-25, P27256 Limits			Unit	Test Conditions
		Min	Typ (3)	Max	Min	Typ (3)	Max		
I_{LI}	Input Load Current			10			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10			10	μA	V_{OUT} = 0V to V_{CC}
I_{PP_1}(2)	V_{PP} Current Read/Standby			5			5	mA	V_{PP} = 5.5V
I_{SB}(2)	V_{CC} Current Standby		25	50		20	40	mA	$\overline{CE}$ = V_{IH}
I_{CC1}(2)	V_{CC} Current Active		55	125		45	100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} V_{PP} = V_{CC}
V_{IL}	Input Low Voltage	−0.1		+0.8	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −400 μA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	3.8		V_{CC}	V	V_{CC} = 5.0V ± 0.25V

5

READ OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(5)	$V_{CC} \pm 5\%$	27256-1		27256-2 P27256-2		27256 P27256		Unit	Test Conditions
	$V_{CC} \pm 10\%$			27256-20		27256-25 P27256-25			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
t_{ACC}	Address to Output Delay		170		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		70		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	35	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}(4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	

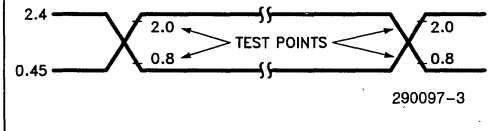
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP.

CAPACITANCE(2) ($T_A = 25°C$, f = 1 MHz)

Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

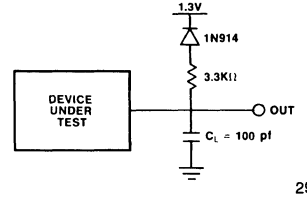
NOTES:
1. $T_A = 25°C$, $V_{CC} = 5.0V$.
2. This parameter is only sampled and is not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



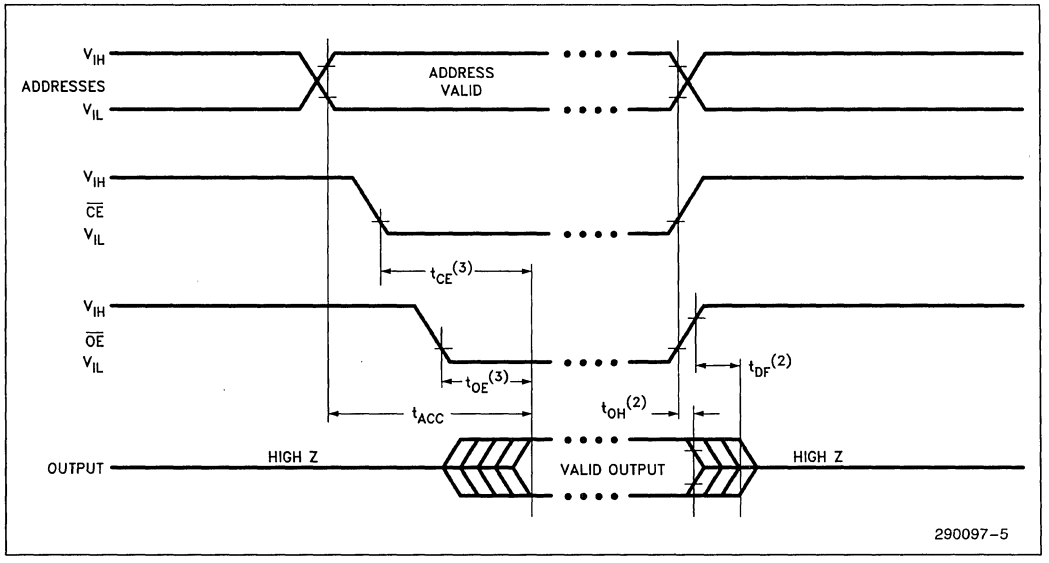
A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

Table 1. Operating Modes

Pins / Mode	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	(4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(4)	(4)	High Z
intelligent Identifier(3)							89H(5)
—manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	5.0V	5.0V	88H(5)
—device	V_{IL}	V_{IL}	V_H(2)	V_{IH}	5.0V	5.0V	04H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12.0V±0.5V.
3. A_1-A_8, $A_{10}-A_{13}$ = V_{IL}, A_{14} = V_{IH}.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturers identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

DEVICE OPERATION

The modes of operation of the 27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for intelligent identifier mode.

Read Mode

The P27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1"is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} and V_{CC} at their programming voltages.

Optional Program Verify

The optional verify may be performed in place of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at its programming voltage. The outputs will tri-state according to the signal presented to $\overline{OE}$. Therefore, all devices with V_{PP} = 12.75V (12.5V int$_e$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share a common bus, V_{PP} should be lowered to V_{CC} (= 6.25/6.0V—see Table 2) and the normal read mode used to execute a program verify.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

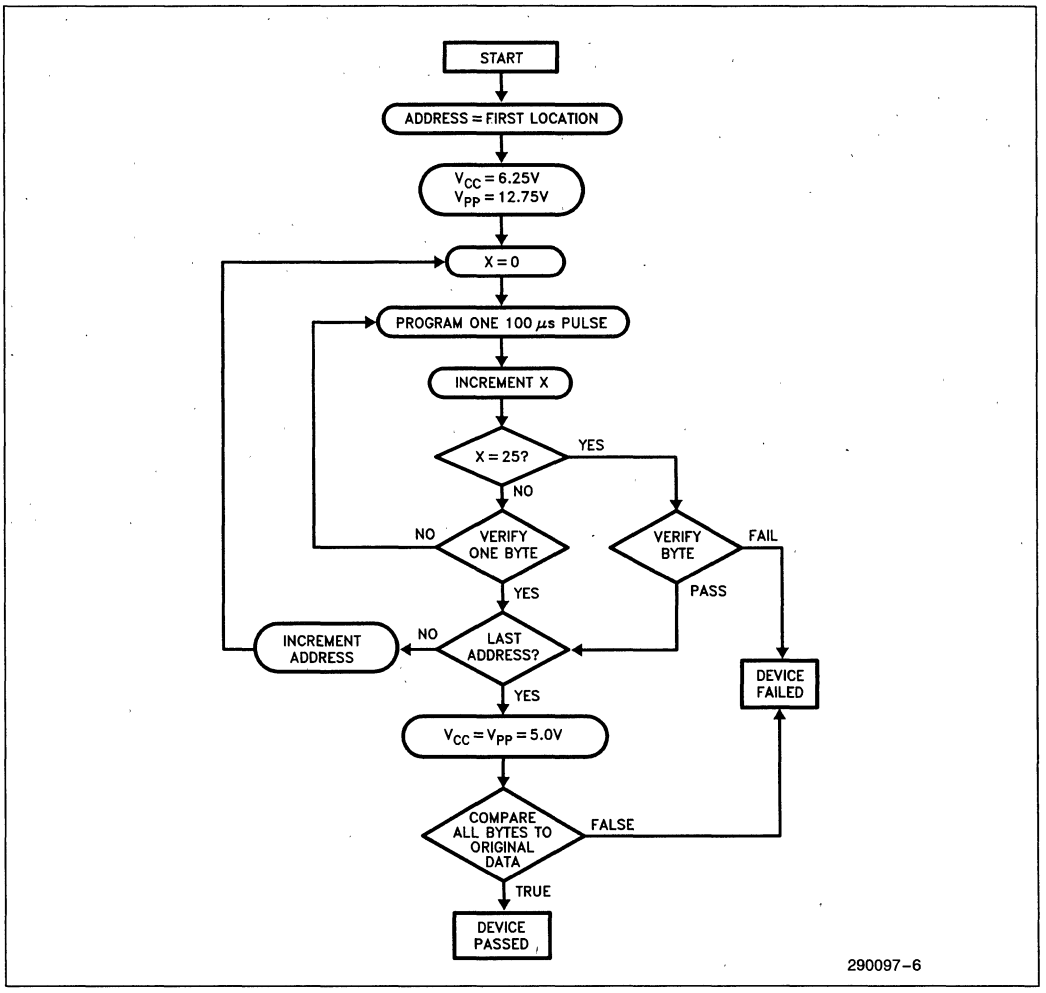


Figure 3. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic EPROMs)

Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic devices to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

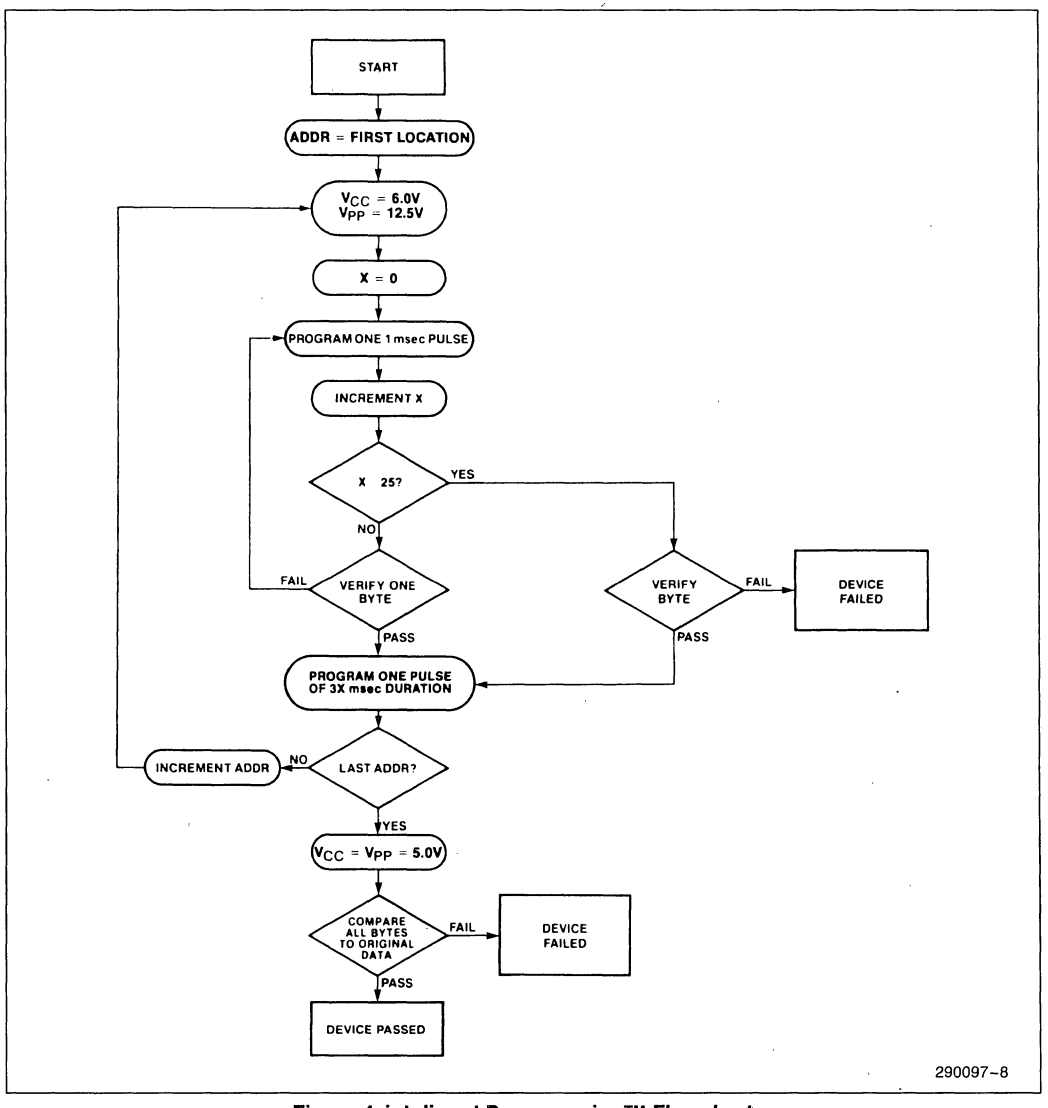


Figure 4. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output HIgh Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		125	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

Symbol	Parameter	Limits				Test Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Data Float Delay	0		130	μs	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.45V to 2.4V

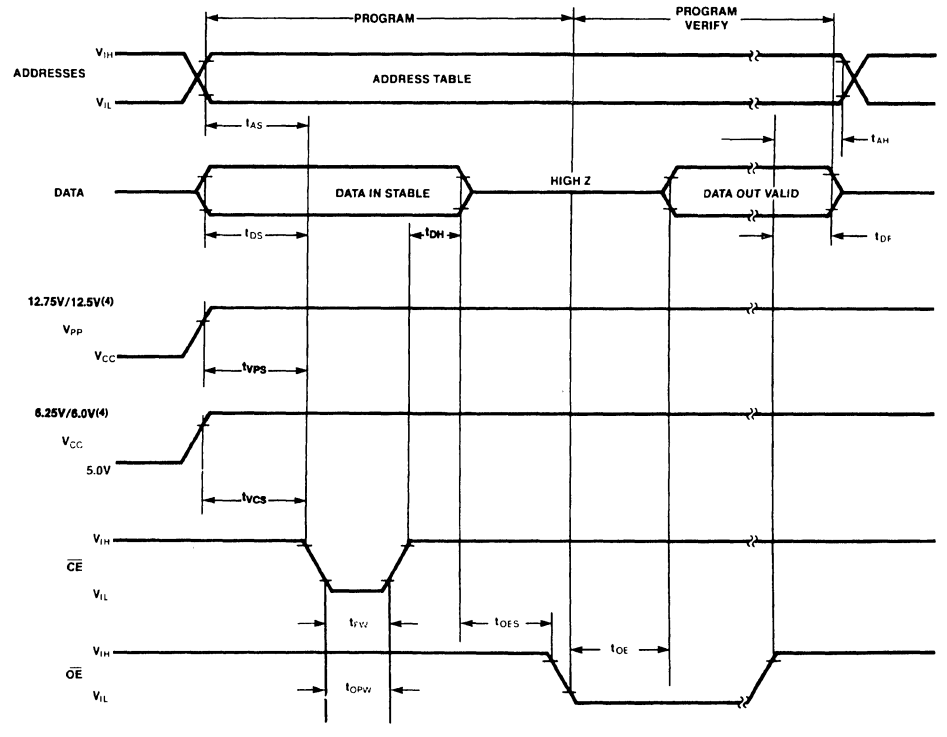
Input Timing Reference Level ..... 0.8V and 2.0V

Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (int$_e$ligent Programming Algorithm only).
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27256 a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm. 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

REVISION HISTORY

Number	Description
04	Revised Pin Configuration. Revised Express options. Deleted -3, -30, -5, L-2, L-20 and L-1 speed bins. D.C. Characteristics — I_{LI} Conditions are V_{IN} = **0V to V_{CC}.** D.C. Characteristics — I_{LO} Conditions are V_{OUT} = **0V to V_{CC}.**

27C256
256K (32K x 8) CHMOS EPROM

- **High Speed**
  - **120 ns Access Time**
- **Low Power Consumption**
  - **100 μA Standby, 30 mA Active**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm**
  - **Programming Time as Fast as 4 Seconds**
- **EPI Processing**
  - **Maximum Latch-up Immunity**
- **Simple Interfacing**
  - **Two Line Control**
  - **CMOS and TTL Compatible**
- **Versatile JEDEC-Approved Packaging**
  - **Standard 28-Pin CERDIP**
  - **Compact 32-Lead PLCC**
  - **Cost Effective Plastic DIP**

(See Packaging Spec., Order #231369)

Intel's 27C256 is a 5V only, 262,144-bit Erasable Programmable Read Only Memory, organized as 32,768 words of 8 bits. Its standard pinouts provide for simple upgrades to 512 Kbits in the future in both DIP and SMT.

The 27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-wait-state operation with the 12 MHz 80286. The 27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run 1-wait-state on a 16 MHz 386™ microprocessor.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 28-pin DIP package, Intel also offers a 32-lead PLCC version of the 27C256. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C256 is equally at home in both TTL and CMOS environments. The Quick-Pulse programming™ algorithm improves speed as much as 100 times over older methods, further reducing cost for system manufacturers.

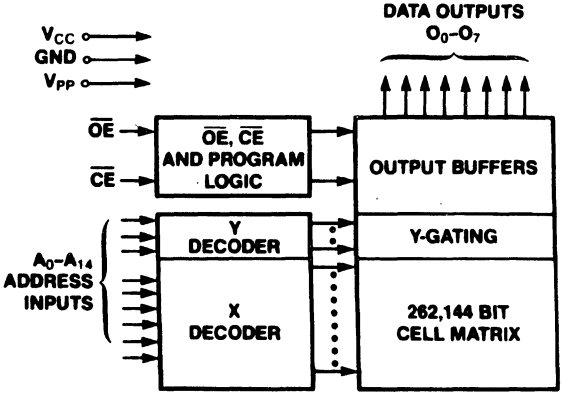


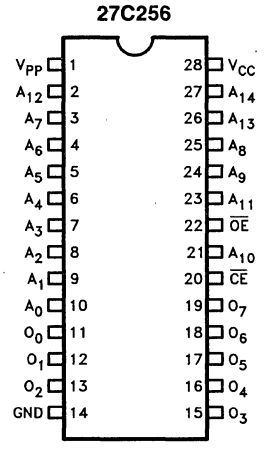
Figure 1. Block Diagram

September 1990
Order Number: 290044-010

Pin Names

A_0–A_{15}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
$\overline{PGM}$	PROGRAM
NC	NO CONNECT
DU	DON'T USE

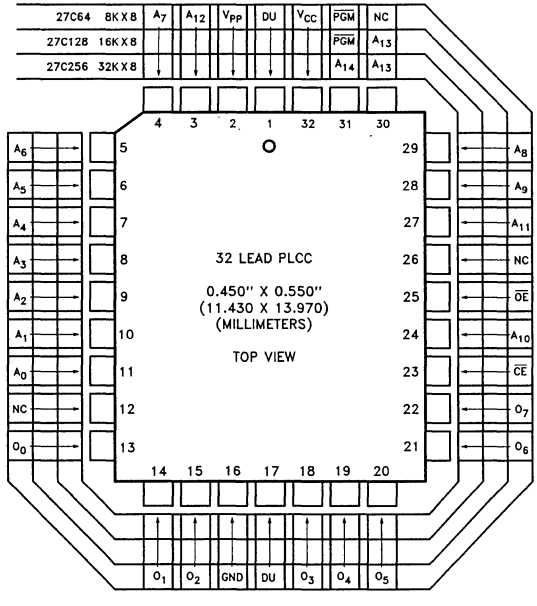
27512 27C512	27128A 27C128	2764A 27C64	2732A	2716
A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290044-2

2716	2732A	27C64 27C64	27128A 27C128	27512 27C512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A_{14}
V_{CC}	V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration



290044-10

Figure 3. PLCC Lead Configuration

5

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several densities allowing the appropriate memory size to match system requirements. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications. The EXPRESS product family is available in both 0°C to 70°C and −40°C to 85°C operating temperature range versions. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

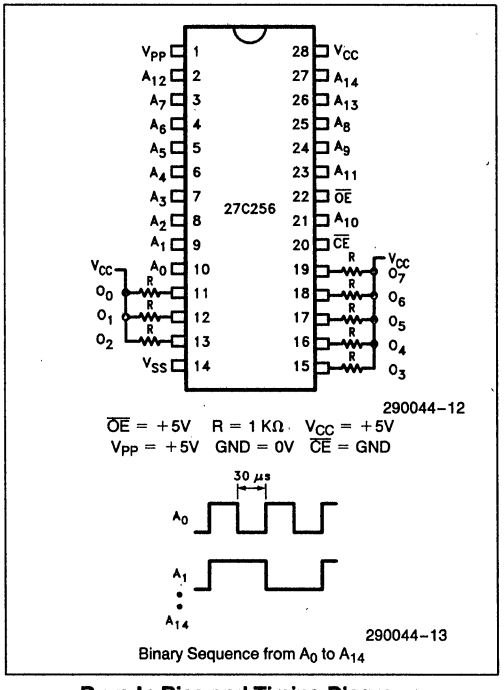
Options

Speed	Packaging		
	CERDIP	PLCC	PDIP
−120V10	Q, T, L	T	T
−200V10	Q, T, L	T	

EXPRESS EPROM FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to 70°C	168 ±8
T	−40°C to 85°C	NONE
L	−40°C to 85°C	168 ±8



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature Under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −2V to 7V(2)

Voltage on A_9 with Respect to GND ..... −2V to 13.5V(2)

V_{PP} Supply Voltage with Respect to GND ..... −2V to 14.0V(2)

V_{CC} Supply Voltage with Respect to GND ..... −2V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz
I_{PP}	V_{PP} Operating Current	3			200	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

NOTES:

1. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS versions.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.

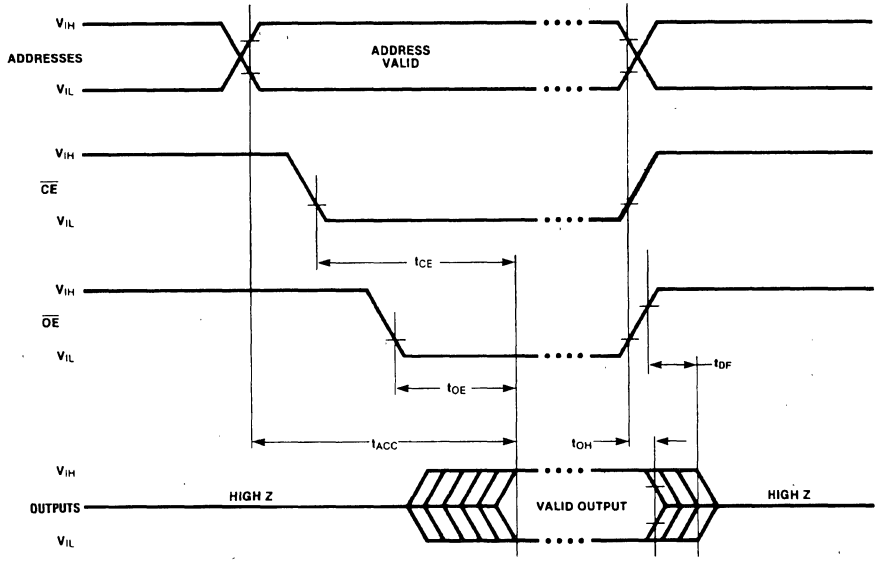
5

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ± 10%

Versions[4]		V_{CC} ±10%	27C256-120V10 P27C256-120V10 N27C256-120V10		27C256-150V10 P27C256-150V10 N27C256-150V10		27C256-200V10 P27C256-200V10 N27C256-200V10		Unit
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		55		60		75	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		30		50		55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Package Prefixes: No Prefix = CERDIP; N = PLCC; P = PDIP.

AC WAVEFORMS



290044-5

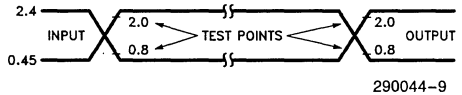
CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled, not 100% tested.

5

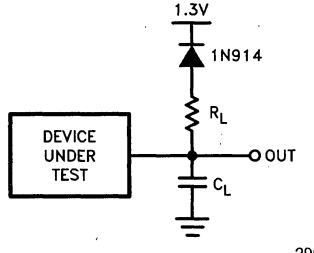
AC INPUT/OUTPUT REFERENCE WAVEFORM



290044-9

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤10 ns.

AC TESTING LOAD CIRCUIT



290044-3

C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

DEVICE OPERATION

The Mode Selection table lists 27C256 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	1	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby		V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	2	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	V_{CP}	HIGH Z
int$_e$ligent Identifier -Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier -Device	2, 3, 4	V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	V_{CC}	8D H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10-14} = V_{IL}.
4. Programming equipment may also refer to this device as the 27C256A. Older devices may have device ID = 8CH.

Read Mode

The 27C256 has two control functions, both must be enabed to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" are programmed, the data word can contain both "1's" and "0's". Ultraviolet light erasure is the only way to change "0's" to "1's".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE}$ = V_{IH} programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V + 0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{14} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ± 5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to the 512 Kbit density is easily accomplished due to the standardized pin configuration of the 27C256. A jumper between A_{15} and V_{CC} allows upgrade using the V_{PP} pin. Systems designed for 256 Kbit program memories today can be upgraded to 512 Kbit in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain flourescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 µW/cm^2).

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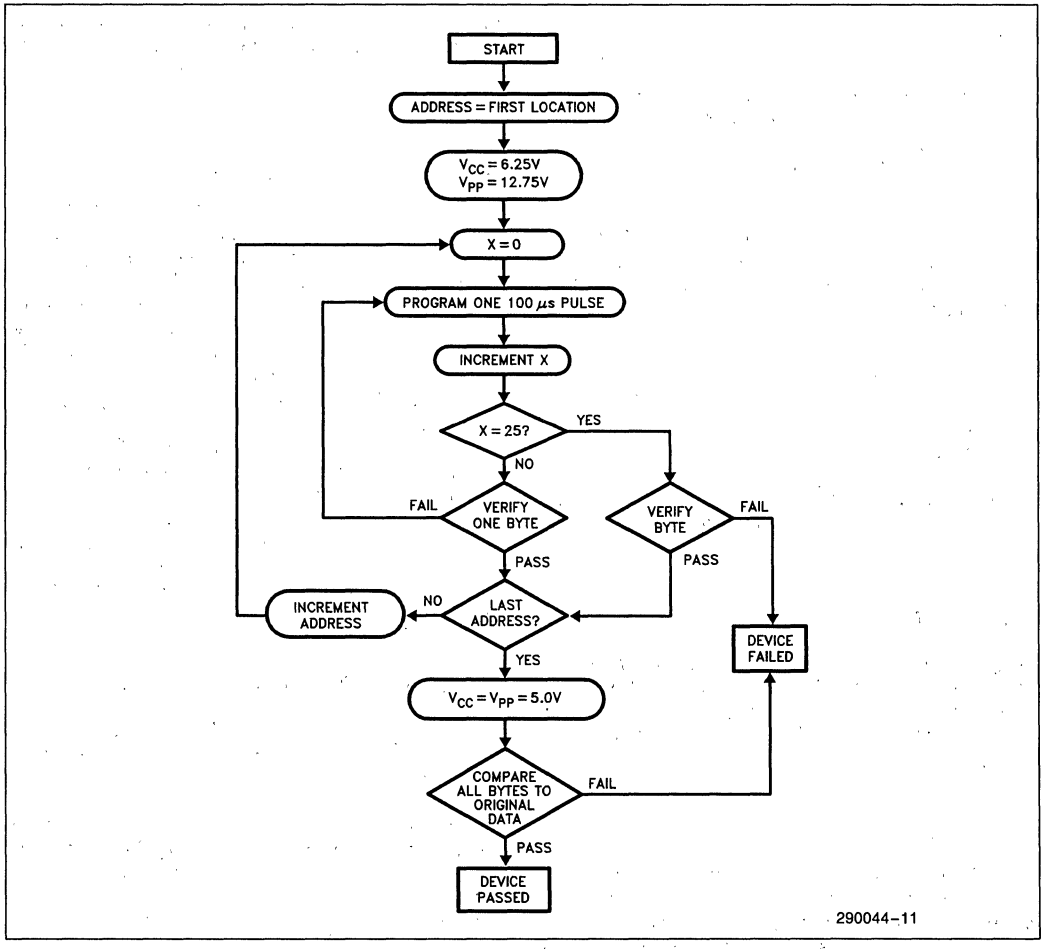

Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C256. Developed to substantially reduce programming throughput, this algorithm can program the 27C256 as fast as 4 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been sucessfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			30	mA	$\overline{CE} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 Int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current value is with outputs O_0 to O_7 unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurments.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

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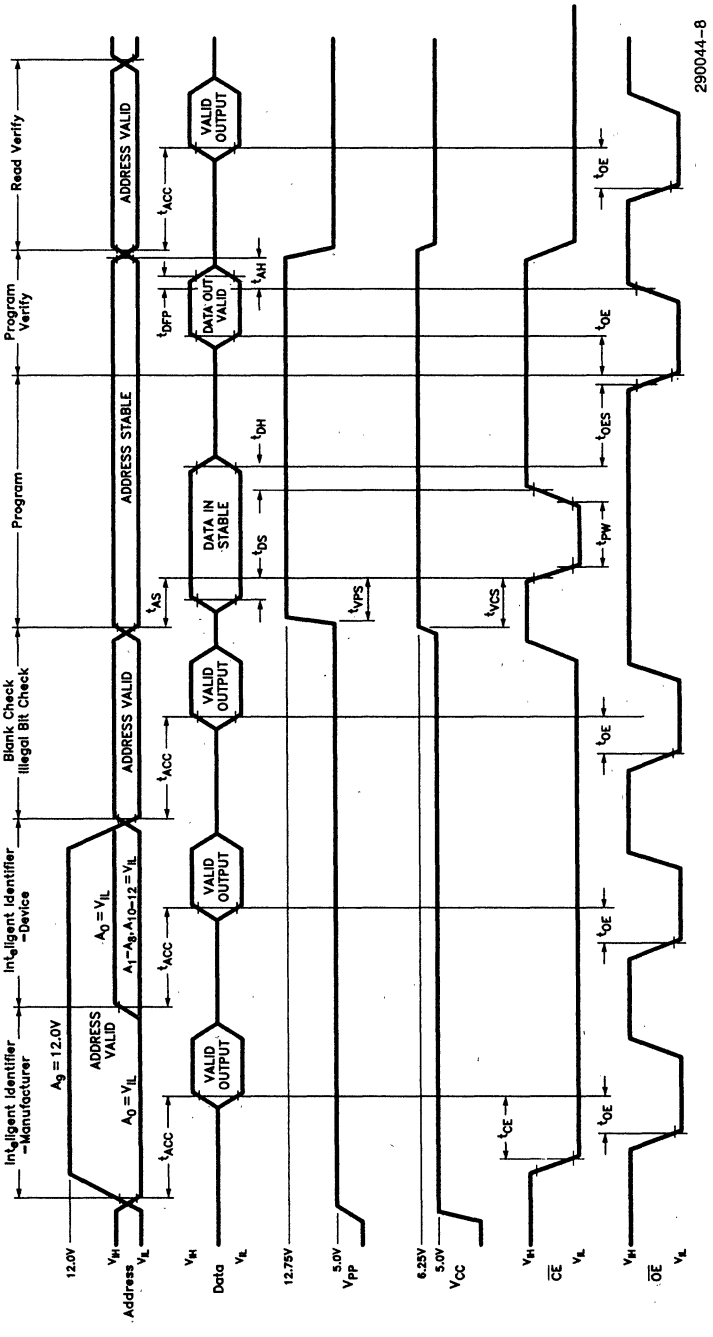
PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
010	Revised general datasheet structure, text to improve clarity Revised I_{SB} Test Condition from $\overline{CE}$ = **V_{CC}** to $\overline{CE}$ = **V_{CC} ± 0.2V** Revised V_{OH} from **3.5V** to **2.4V**, I_{OH} from **−2.5 mA** to **−400 μA** Deleted 512K PLCC pinout references Deleted −150V10, −2, −20, −STD and −25 EXPRESS offerings Added −120V10, −200V10, PLCC and PDIP EXPRESS offerings Deleted −20, −25 and all 5% V_{CC} speed bins Added PLCC and PDIP −120 speed bin packages

27C512
512K (64K x 8) CHMOS EPROM

- **Software Carrier Capability**
- **120 ns Access Time**
- **Two-Line Control**
- **Int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **CMOS and TTL Compatible**
- **Low Power**
  — 30 mA Max. Active
  — 100 μA Max. Standby
- **Fast Programming**
  — Quick-Pulse Programming™ Algorithm
  — Programming Time as Fast as 8 Seconds

The Intel 27C512 is a 5V-only, 524, 288-bit Erasable Programmable Read Only Memory (EPROM), organized as 65,536 words of 8 bits. Individual bytes are accessed in 120 ns. This ensures compatibility with high-performance microprocessors, such as the Intel 12 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27C512 is also directly compatible with Intel's 80C51 family of microcontrollers.

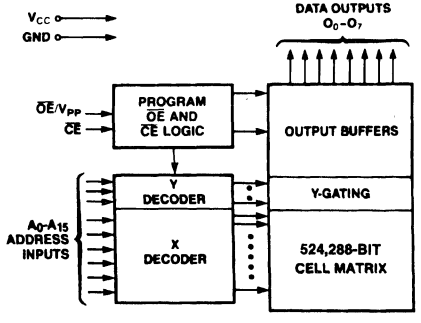
The 27C512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27C512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

The 27C512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27C512 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Intel's Quick-Pulse Programming™ algorithm enables the 27C512 to be programmed as fast as eight seconds (plus programmer overhead). Programming equipment which takes advantage of the int$_e$ligent Identifier™ will electronically identify the EPROM and automatically program it using a superior programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of the 27C512. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

CHMOS is a patented process of Intel Corporation.



290228-1

Figure 1. Block Diagram

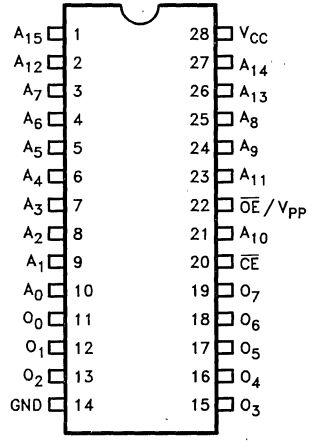
October 1990
Order Number: 290228-003

Pin Names

A_0–A_{15}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/V_{PP}
$\overline{PGM}$	PROGRAM
O_0–O_7	OUTPUTS
NC	NO CONNECT

27256 27C256	27C128 27128A	2764A 27C64	2732A	2716
V_{PP}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27C512



290228-2

2716	2732A	2764A 27C64	27C128 27128A	27256 27C256
		V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A_{14}
V_{CC}	V_{CC}	NC	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration

5

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several densities allowing the appropriate memory size to match system requirements. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications . The EXPRESS product family is available in both 0°C to 70°C and −40°C to 85°C operating temperature range versions. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

EXPRESS EPROM FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to 70°C	168 ± 8
T	−40°C to 85°C	None
L	−40°C to 85°C	168 ± 8

OPTIONS

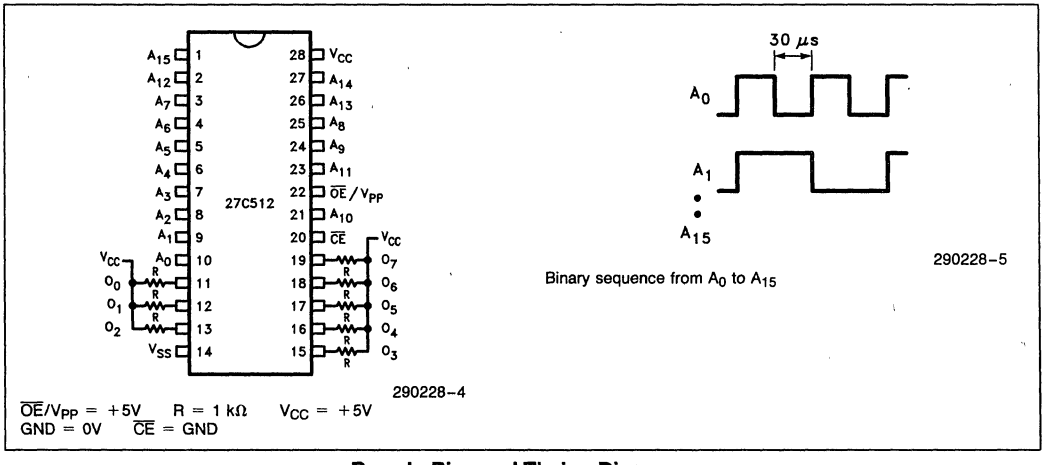
Packaging	
Speed	**CERDIP**
−120V10	Q, T, L

READ OPERATION DC CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27C512(2) LD27C512		Test Condition
		Min	Max	
I_{CC}(1)	V_{CC} Operating Current (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Operating Current at High Temperature (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.
2. D refers to the CERDIP package.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C(1)
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −2.0V to 7.0V(2)
Voltage on A_9 with Respect to GND ..... −2.0V to 13.5V(2)
V_{PP} Supply Voltage with Respect to GND ..... −2.0V to 14V(2)
V_{CC} Supply Voltage with Respect to GND ..... −2.0V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to +5.5V
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to +5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA

NOTES:
1. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS versions.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.

5

READ OPERATION AC CHARACTERISTICS V_{CC} = 5.0V ±10%

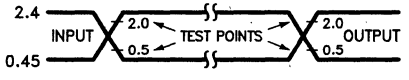
Versions[4]	V_{CC} ± 10%		27C512-120V10		27C512-150V10		27C512-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	2		55		60		70	ns
t_{DF}	$\overline{OE}/V_{PP}$ High to Output High Z	3	0	30	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	3	0		0		0		ns

NOTES:
1. See AC input/output reference waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Packaging Options: No Prefix = CERDIP.
5. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE[3] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[5]	Max	Unit	Condition
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{OE}/V_{PP}	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	V_{IN} = 0V

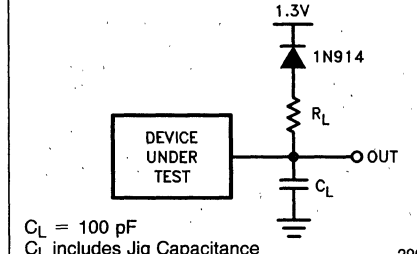
AC INPUT/OUTPUT REFERENCE WAVEFORM



290228-6

NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤ 10 ns.

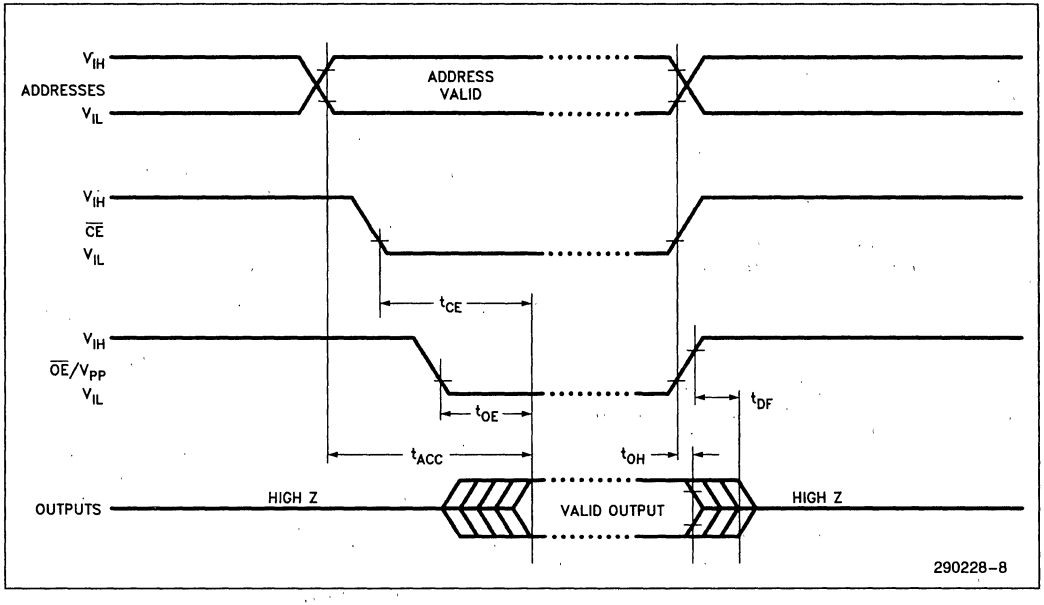
AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance
R_L = 3.3 kΩ

290228-7

AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C512 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and $\overline{OE}/V_{PP}$, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

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Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read	1	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby		V_{IH}	X	X	X	V_{CC}	High Z
Program	2	V_{IL}	V_{PP}	X	X	V_{CP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	V_{CP}	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	V_{CP}	High Z
Int$_e$ligent Identifier — Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	89H
Int$_e$ligent Identifier — Device		V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	FDH

NOTES:
1. X can be V_{IH} or V_{IL}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{15} = V_{IL}.

Read Mode

The 27C512 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}/V_{PP}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}/V_{PP}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}/V_{PP}$.

Two Line Output Control

EPROMS are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}/V_{PP}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Program Mode

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when $\overline{OE}/V_{PP}$ is raised to 12.75V. Data is introduced by applying an 8 bit word to the output pins. Pulsing $\overline{CE}$ low programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{OE}/V_{PP}$ at V_{IL}. Valid data is available t_{DV} after $\overline{CE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}/V_{PP}$, parallel EPROMS may have common inputs.

inteligent Identifier Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ± 0.5V on A_9. With $\overline{CE}$, $\overline{OE}/V_{PP}$, A_1–A_8 and A_{10}–A_{15} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

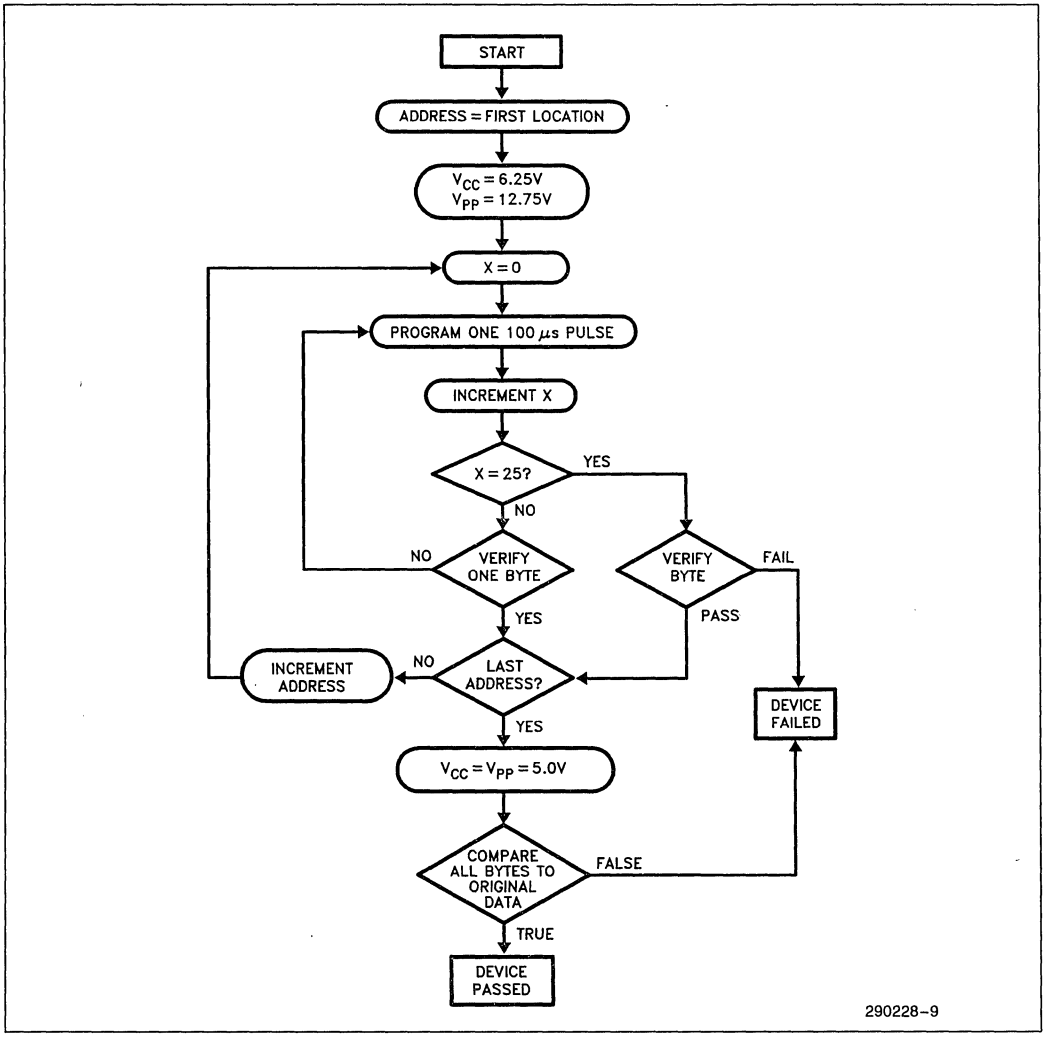


Figure 3. Quick-Pulse Programming Algorithm

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 µW/cm^2).

Quick-Pulse Programming Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C512. Developed to substantially reduce programming throughput, this algorithm can program the 27C512 as fast as 8 seconds. Actual programming time depends on the programmer overhead.

The Quick-Pulse Programming algorithm employs a 100 µs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{CC} = 6.25V. $\overline{OE}/V_{PP}$ toggles between 12.75V and V_{IL} for program and verify operations. When programming is complete, all bytes are compared to the original data with V_{CC} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5°C$

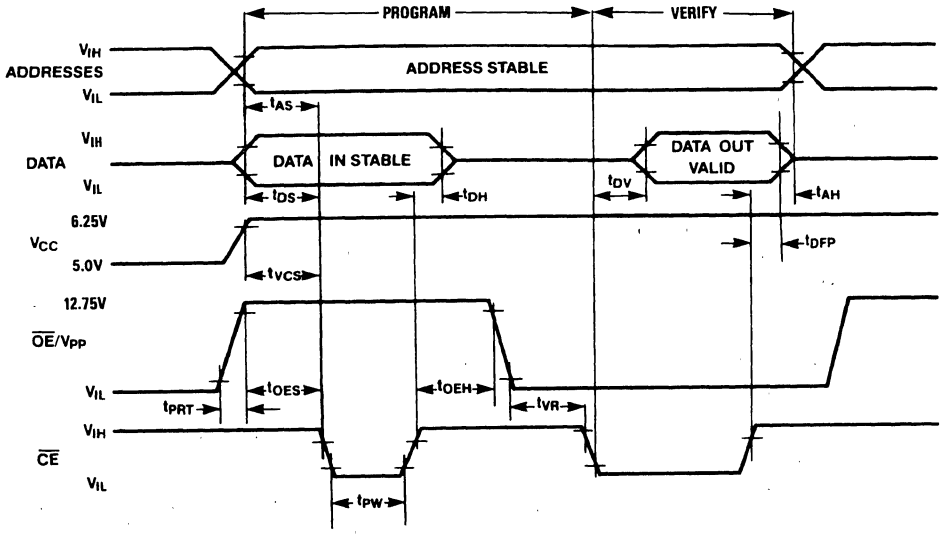
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25 \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2, 3	2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			μs
t_{DV}	Data Valid from $\overline{CE}$	5			1	μs
t_{DFP}	Output Disable to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current value is with outputs O_0 to O_7 unloaded.
2. V_{CP} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
3. When programming, a 0.1 μF capacitor is required across $\overline{OE}/V_{PP}$ and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveforms for timing measurements.
5. t_{DV} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
003	Deleted preliminary classification.

5

27513
PAGE-ADDRESSED 512K (4 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
  - **— No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power Up and On Demand with $\overline{RST}$ Signal(1)**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **— 125 mA max. Active**
  - **— 40 mA max. Standby**
- **Compatible with Industry Standard EPROM Pinouts**
  - **— Direct 27128A Compatibility**
  - **— 28-Pin Cerdip**

The Intel 27513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27513's paged organization brings 64 K-byte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 K-byte total addressing capability. The 27513 provides an ideal means of quadrupling current 16 K-byte code space.

The 27513's large storage capability of 64 K-bytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The 27513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27513 is manufactured using Intel's Compacted HMOS* II technology.

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

September 1989
Order Number: 231113-007

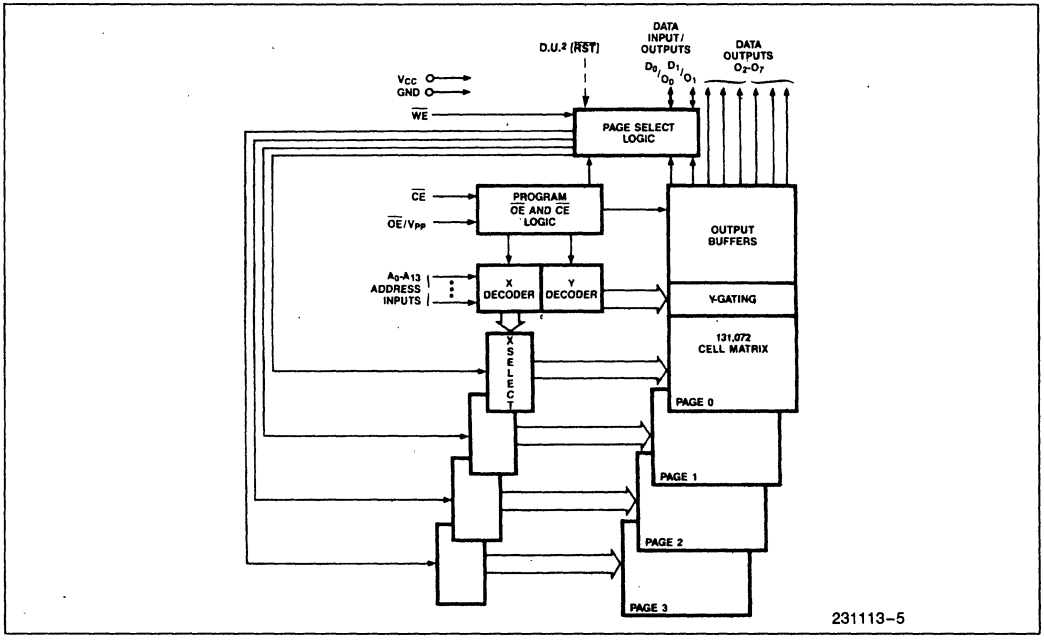
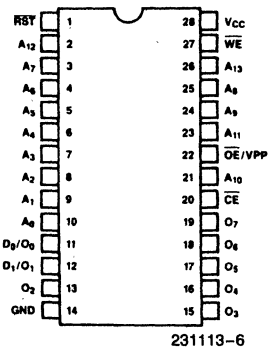


Figure 1. Block Diagram

2716	2732A	2764A 27C64 87C64	27128A 27C128	27256 27C256	27512 27C512
		V_{PP}	V_{PP}	V_{PP}	A_{15}
		A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND	GND



27512 27C512	27256 27C256	27128A 27C128	2764A 27C64 87C64	2732A	2716
V_{CC}	V_{CC}	V_{CC}	V_{CC}		
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$		
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}	V_{CC}
A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	V_{PP}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3

Figure 2. Pin Configuration

NOTES:
1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page-Select Write Enable
O_2–O_7	Outputs
D_0/O_0,D_1/O_1	Input/Outputs
$\overline{RST}$	Page Reset(1)

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27513 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-200V10	Q, L, T

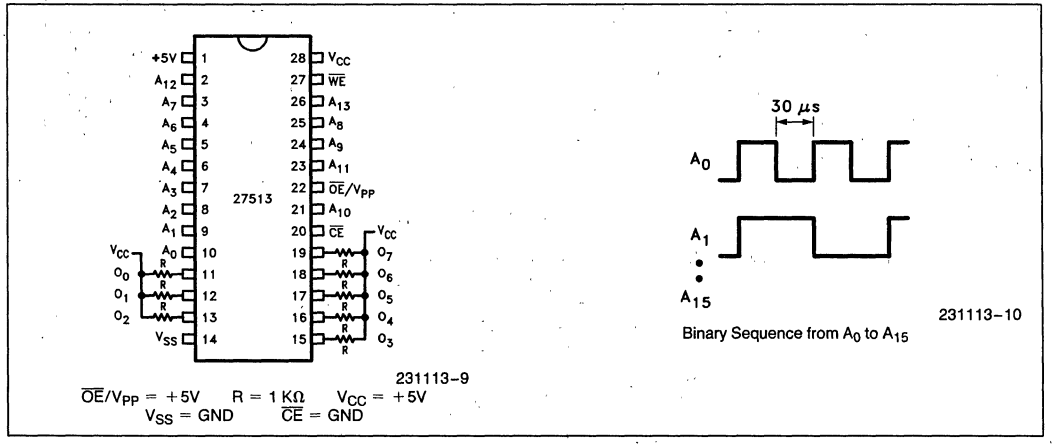
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27513 LD27513 Min	TD27513 LD27513 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† ..... −0.6V to +6.5V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
$\overline{OE}/V_{PP}$ Supply Voltage with
Respect to Ground ..... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

† includes Don't Connect (pin 1)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ AND PAGE-SELECT WRITE OPERATIONS

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$ to V_{CC}
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage		3.5	4.0	V	

READ OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(5)		$V_{CC} \pm 5\%$	27513-170V05		27513-2 27513-200V05		27513		Units	Test Conditions
		$V_{CC} \pm 10\%$	27513-170V10		27513-20 27513-200V10		27513-25			
Symbol	Parameter		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay			170		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			170		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay			60		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float		0	50	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First		0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

5

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

A.C. CHARACTERISTICS

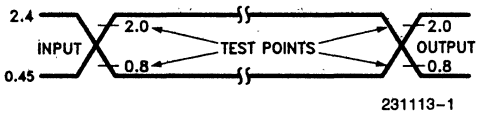
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	250		ns	
t_{RAV}	Reset to Address Valid	250		ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP; N = PLCC.
6. $\overline{RST}$ function is available only on parts with 6-digit suffix.

CAPACITANCE(2) $T_A = +25°C$, f = 1 MHz

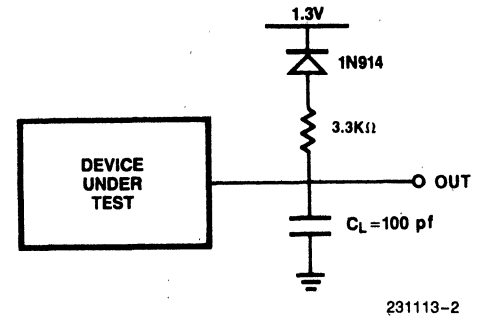
Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	$V_{IN} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM



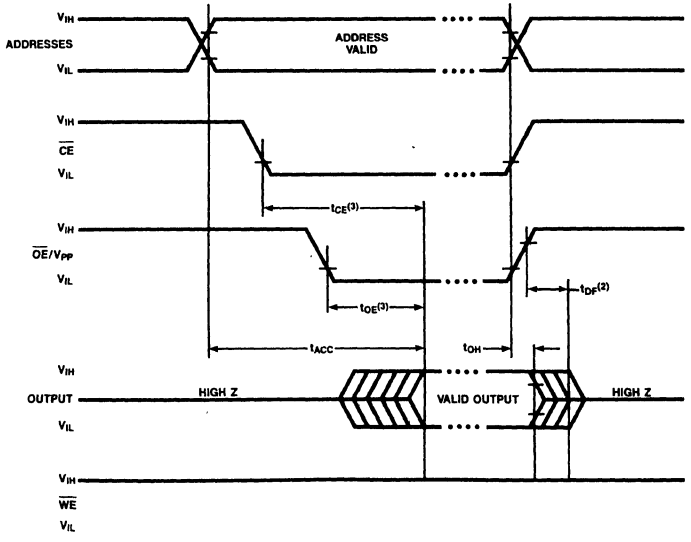
AC Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

A.C. TESTING LOAD CIRCUIT



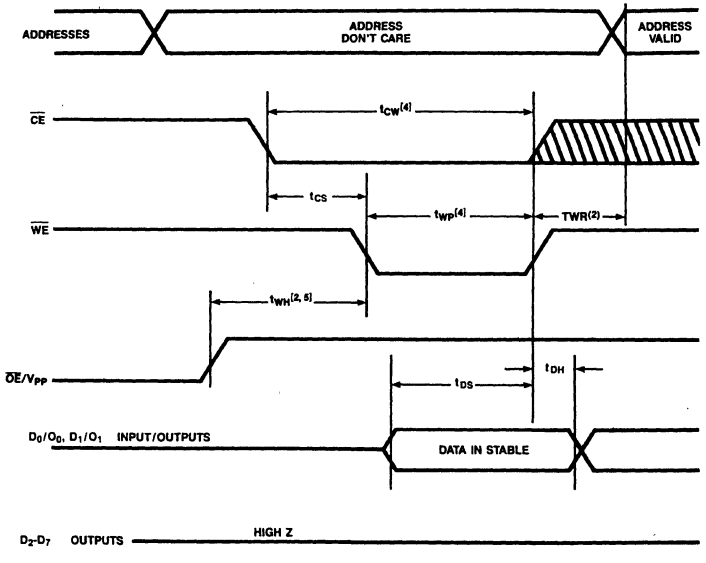
C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION



231113-3

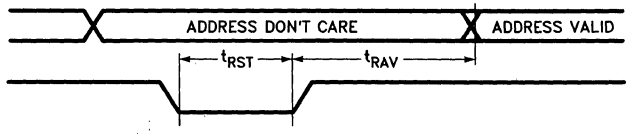
A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



231113-4

5

A.C. WAVEFORMS FOR PAGE-RESET OPERATIONS



231113-12

NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}/V_{PP}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for int$_e$ligent Identifier mode.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A_9	A_0	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X(1)	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC}(5)	High Z	Page(2) D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC}(5)	High Z	X
int$_e$ligent(4) —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IL}	5.0V	89H	89H
Identifier —Device	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IH}	5.0V	0FH(6)	0FH(6)

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. 27513s before 2H/86 have a device identifier of 0DH. 27513s after 2H/86 will have a device identifier of 0FH.
7. $V_H = 12.0V \pm 0.5\%$.

Read Mode

The 27513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

The 27513 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27513 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27513 is addressed by first selecting one of four 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case −10% V_{CC} supply condition) against spurious page latch clearing.

27513 parts with 6-digit suffixes also have a page reset pin: $\overline{RST}$. This pin should be tied to an active low system reset signal. These 27513s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27513s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the 27513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27513s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27513s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

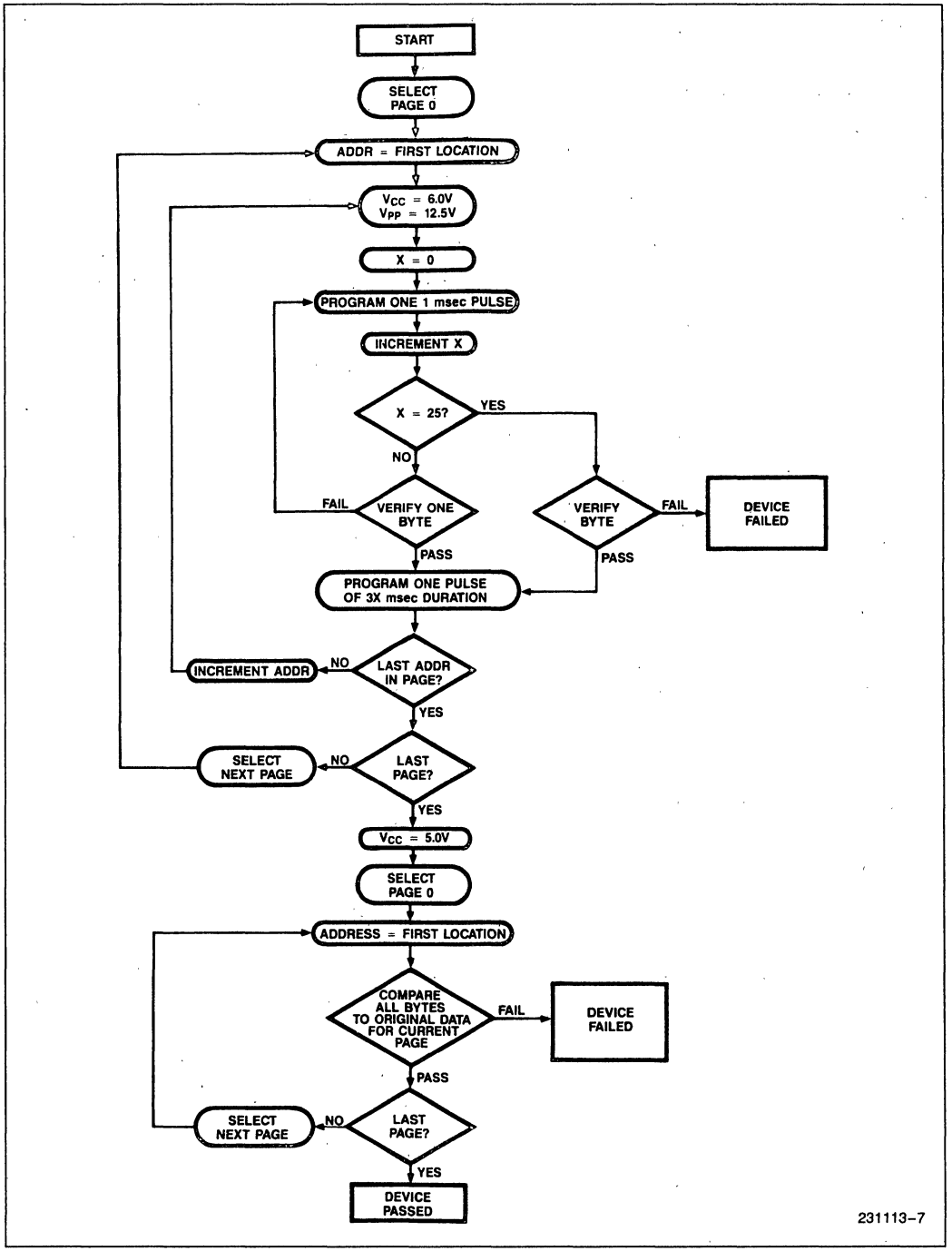


Figure 5. 27513 Int$_e$ligent Programming™ Flowchart

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

int$_e$ligent Programming™ ALGORITHM

The int$_e$ligent Programming Algorithm programs Intel EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of six minutes. Actual Programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27513 int$_e$ligent Programming Algorithm is shown in Figure 3. The only difference between the 27513 and other EPROM int$_e$ligent Programming is that the 27513 is programmed one 16 K-byte page at a time.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
I_{CC2}(2)	V_{CC} Supply Current (Program and Verify)		125	mA	
I_{PP2}(2)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0–O_7 unloaded.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			µs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			µs	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			µs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

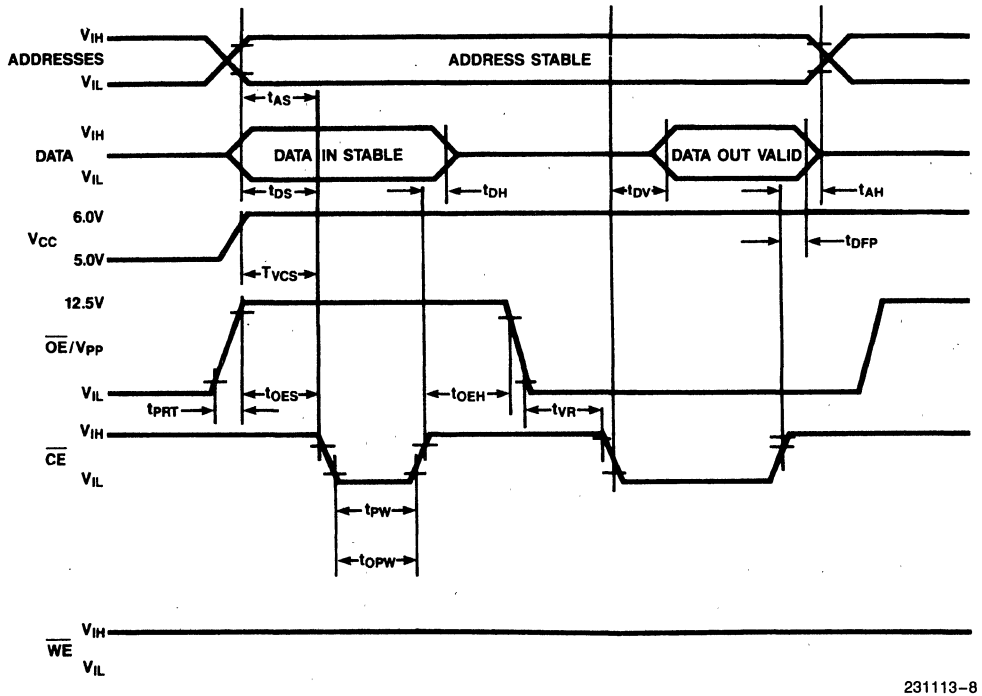
5

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 K-byte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
07	Revised Express Options Revised Pin Configuration D.C. Characteristics-I_{LI} Test Conditions-V_{IN} = **0V to V_{CC}** D.C. Characteristics-I_{LO} Test Conditions-V_{OUT} = **0V to V_{CC}**

27C513
PAGE-ADDRESSED 512K (4 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
  - **— No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power Up and On Demand with $\overline{RST}$ Signal**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **— 30 mA max. Active**
  - **— 100 μA max. Standby**
- **Compatible with Industry Standard EPROM Pinouts**
  - **— Direct 27128A Compatibility**
  - **— 28-Pin Cerdip**

The Intel 27C513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27C513's paged organization brings 64 Kbyte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 Kbyte total addressing capability. The 27C513 provides an ideal means of quadrupling current 16 Kbyte code space.

The 27C513's large storage capability of 64 Kbytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27C513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The 27C513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27C513 is manufactured using Intel's 1 micron CHMOS* III-E technology.

CHMOS is a patented process of Intel Corporation.

October 1990
Order Number: 290231-002

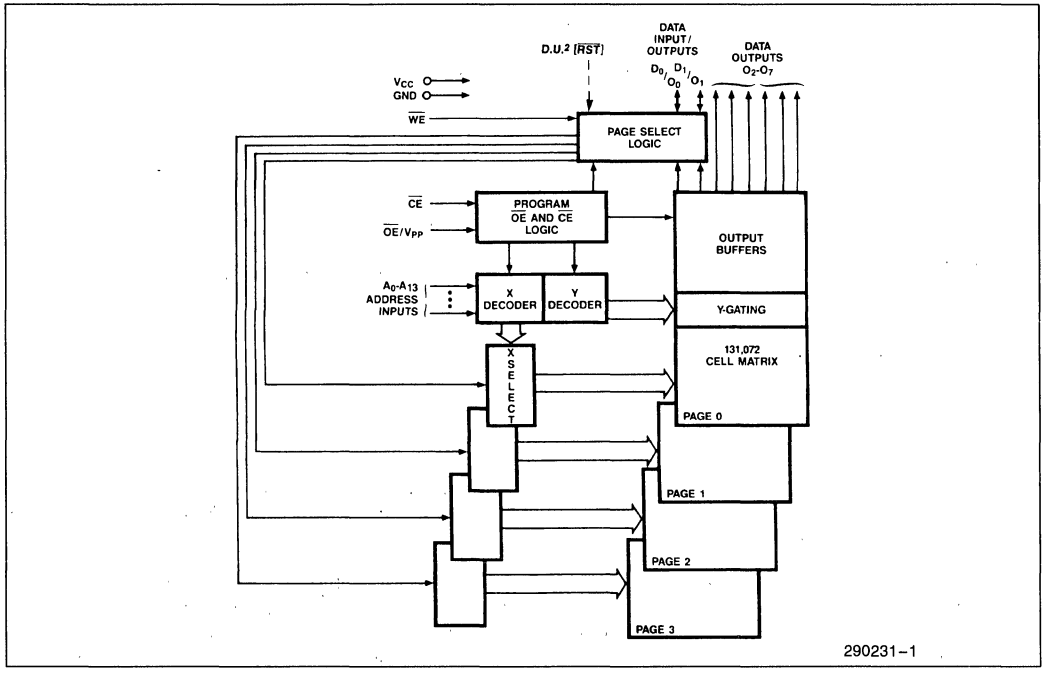
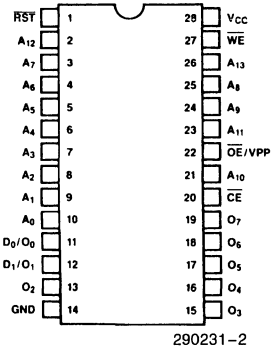


Figure 1. Block Diagram

2732A	27C64 2764A 87C64	27C128 27128A	27C256 27256	27C512 27512	27C011 27011
	V_{PP}	V_{PP}	V_{PP}	A_{15}	$V_{PP}/\overline{RST}$
	A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0	D_0/O_0
O_1	O_1	O_1	O_1	O_1	D_1/O_1
O_2	O_2	O_2	O_2	O_2	D_2/O_2
GND	GND	GND	GND	GND	GND



290231-2

27C011 27011	27C512 27512	27C256 27256	27C128 27128A	27C64 27C64A 87C64	2732A
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
$\overline{PGM}/\overline{WE}$	A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$	
A_{13}	A_{13}	A_{13}	A_{13}	N.C	V_{CC}
A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3

Figure 2. Pin Configuration

NOTES:
1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27C513 pins.

Pin Names

A_0-A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page-Select Write Enable
O_2-O_7	Outputs
$D_0/O_0, D_1/O_1$	Input/Outputs
$\overline{RST}$	Page Reset

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27C513 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-200V10	Q, T, L

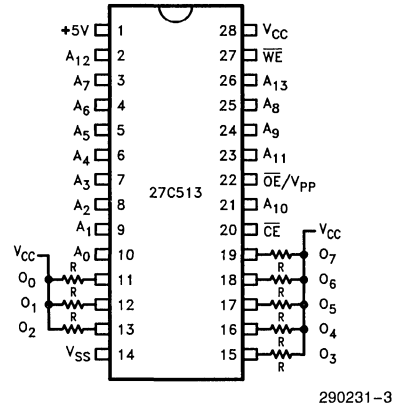
READ OPERATION

DC CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

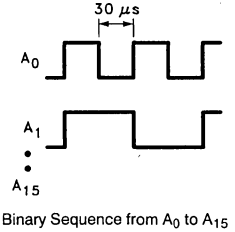
Symbol	Parameter	TD27C513 LD27C513		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		1.0	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC1} (1)	V_{CC} Active Current (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		50	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



290231-3

$\overline{OE}/V_{PP} = +5V$ R = 1 KΩ $V_{CC} = +5V$
V_{SS} = GND $\overline{CE}$ = GND



290231-4

Binary Sequence from A_0 to A_{15}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(2)
Temperature Under Bias .....−10°C to +80°C(2)
Storage Temperature .....−65°C to +125°C
Voltage on Any Pin with
Respect to Ground .....−2V to +7V(1)
Voltage on A_9 with
Respect to Ground .....−2V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground
during Programming .....−2V to +14.0V(1)
V_{CC} Supply Voltage with
Respect to Ground.....−2V to +7.0V(1)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS TTL and NMOS Inputs

Symbol	Parameter	Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current			0.01	1.0	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current				±10	μA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby				1.0	mA	$\overline{CE}$ = V_{IH}
I_{CC1}	V_{CC} Current Active	5			30	mA	$\overline{CE}$ = V_{IL} f = 5 MHz, I_{OUT} = 0 mA
I_{PP1}	V_{PP} Current Read	8			10	μA	V_{PP} = V_{CC}
V_{IL}	Input Low Voltage (±10% Supply)	1	−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)		2.0		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = 400 μA
I_{OS}	Output Short Circuit Current	6			100	mA	
V_{PP}	V_{PP} Read Voltage	7	V_{CC}−0.7		V_{CC}	V	
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage		3.5		4.0	V	

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
8. Maximum active power usage is the sum of I_{PP} and I_{CC}. The maximum current value is with no loading on outputs O_0 to O_7.

DC CHARACTERISTICS CMOS Inputs

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	μA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching	4			6	mA	$\overline{CE}$ = V_{IH}
		Stable				100	μA	$\overline{CE}$ = V_{IH}
I_{CC1}	V_{CC} Current Active		5			30	mA	$\overline{CE}$ = V_{IL} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)			−0.2		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			0.7 V_{CC}		V_{CC}+0.2	V	
V_{OL}	Output Low Voltage					0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			V_{CC} − 0.8			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
8. Maximum active power usage is the sum of I_{PP} and I_{CC}. The maximum current value is with no loading on outputs O_0 to O_7.

5

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

AC CHARACTERISTICS

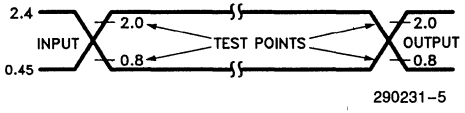
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	100		ns	$\overline{OE}/V_{PP}$ = V_{IH}
t_{WP}	Write Pulse Width	50		ns	$\overline{OE}/V_{PP}$ = V_{IH}
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP}$ = V_{IH}
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP}$ = V_{IH}
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE}/V_{PP}$ = V_{IH}
t_{WH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	100		ns	
t_{RAV}	Reset to Address Valid	150		ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging Options: No prefix = Cerdip.
6. $\overline{RST}$ function is available only on parts with 6-digit suffix.

CAPACITANCE[2] T_A = +25°C, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	V_{IN} = 0V

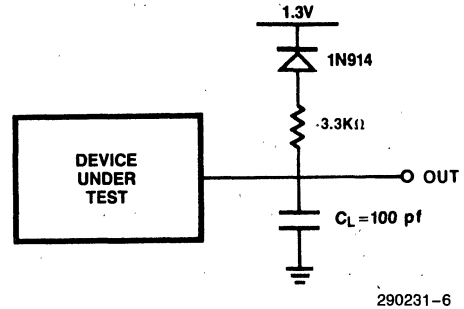
AC TESTING INPUT/OUTPUT WAVEFORM



290231-5

AC Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

AC TESTING LOAD CIRCUIT



290231-6

C_L = 100 pF
C_L Includes Jig Capacitance

AC CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

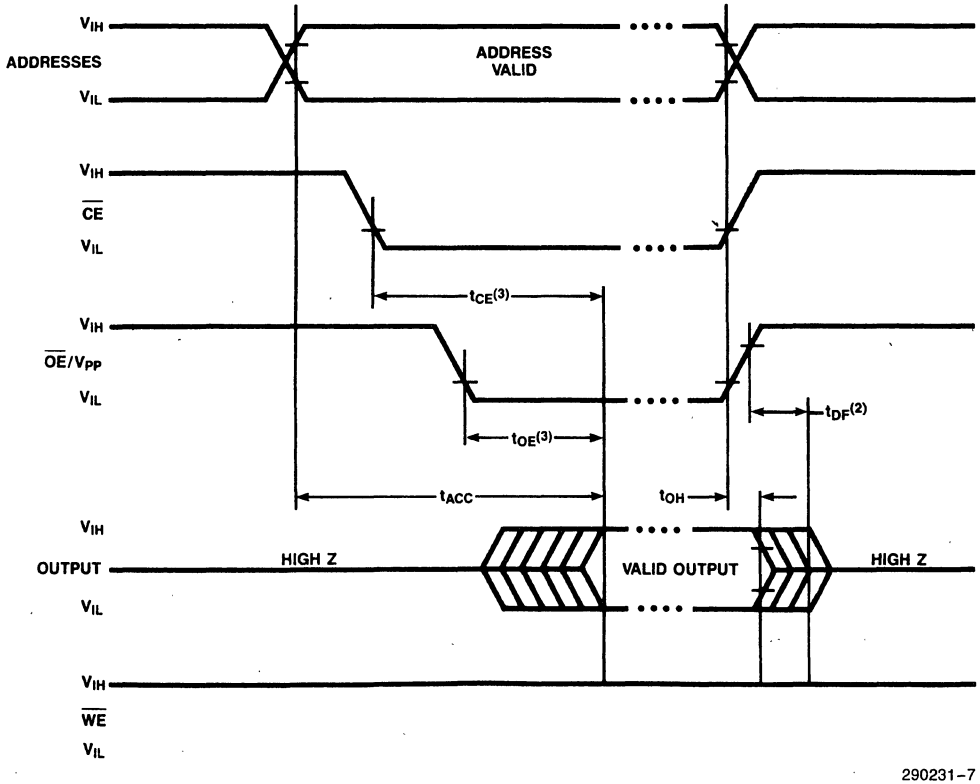
Versions[4]	V_{CC} ±10%	27C513-170V10		27C513-200V10		27C513-250V10		Units	Test Conditions
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		170		200		250	ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250	ns	$\overline{OE}/V_{PP}$ = V_{IL}
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		65		65		100	ns	$\overline{CE}$ = V_{IL}
t_{DF}[3]	$\overline{OE}/V_{PP}$ High to Output Float	0	55	0	55	0	60	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.
4. Packaging: No prefix = Cerdip.

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} to V_{OH}
Input Timing Reference Level 1.5V
Output Timing Reference Level ..... V_{IL} and V_{IH}

AC WAVEFORMS FOR READ OPERATION



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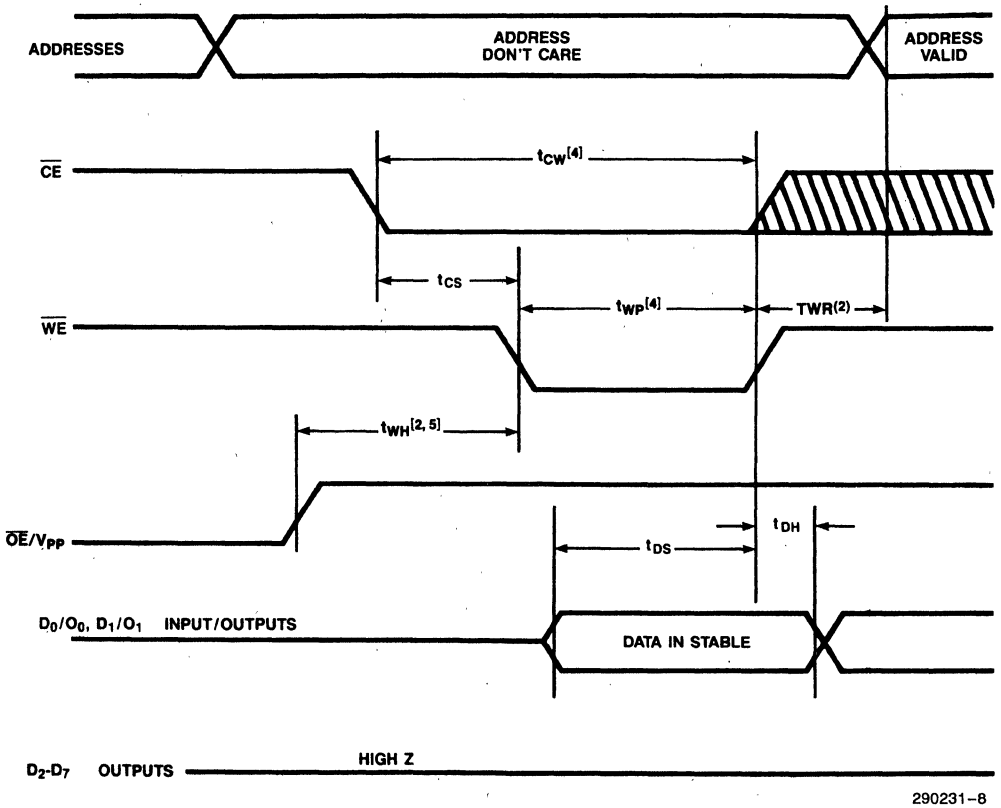
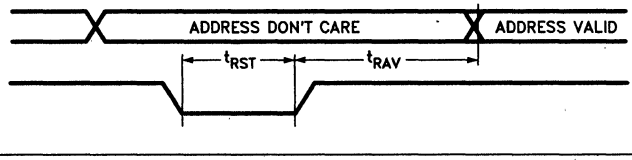
AC WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



AC WAVEFORMS FOR PAGE-RESET OPERATIONS



NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}/V_{PP}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27C513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A_9 for int$_e$ligent Identifier mode.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A_9	A_0	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X(1)	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC}(5)	High Z	Page(2) D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC}(5)	High Z	X
int$_e$ligent(4) —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(6)	V_{IL}	5.0V	89H	89H
Identifier —Device	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(6)	V_{IH}	5.0V	F9H	F9H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. A_1–A_8, A_{10}–A_{13}, = V_{IL}.
5. Page 0 is automatically selected at power-up (V_{CC} < 4.0V).
6. V_H = 12.0V ±0.5%.

5

Read Mode

The 27C513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27C513 is addressed by first selecting one of four 16 Kbyte pages. Individual bytes are then selected by normal random access within the 16 Kbyte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27C513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case -10% V_{CC} supply condition) against spurious page latch clearing.

The 27C513 also has a page reset pin: $\overline{RST}$. This pin should be tied to an active low system reset signal. These 27C513s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27C513s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the 27C513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27C513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27C513s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27C513s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27C513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier™ Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

Quick Pulse Programming™ Algorithm

Intel's 27C513 EPROM can be programmed using the Quick-Pulse Programming™ algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. this algorithm allows these devices to be programmed as fast as fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{CC} = 6.25V$ and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

5

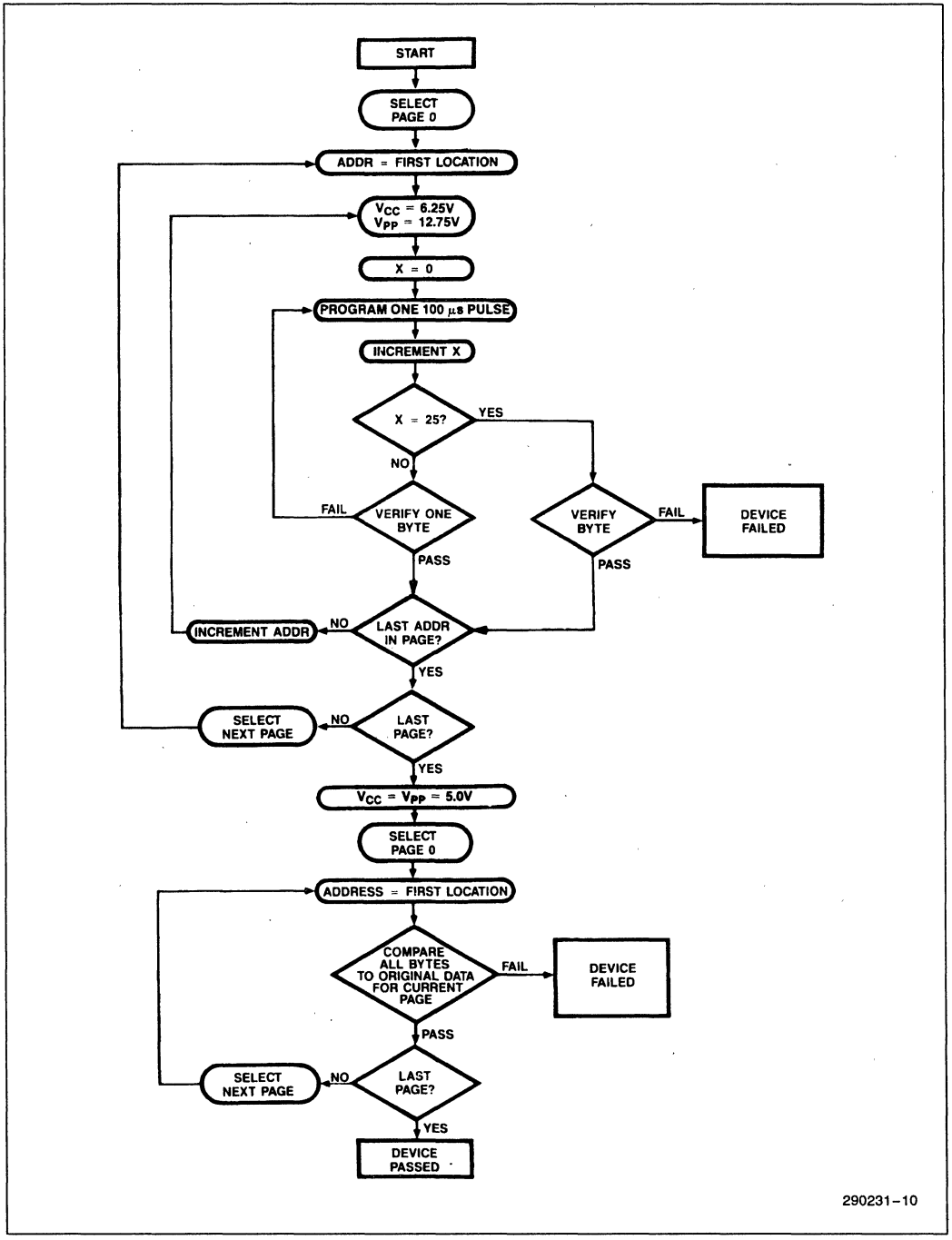


Figure 3. 27C513 Quick-Pulse Programming Flowchart

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

TABLE 2. DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		1	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.4	6.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	3.5		V	I_{OH} = −2.5 mA
I_{CC2}(2)	V_{CC} Supply Current (Program and Verify)		40	mA	
I_{PP2}(2)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0–O_7 unloaded.

5

AC PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

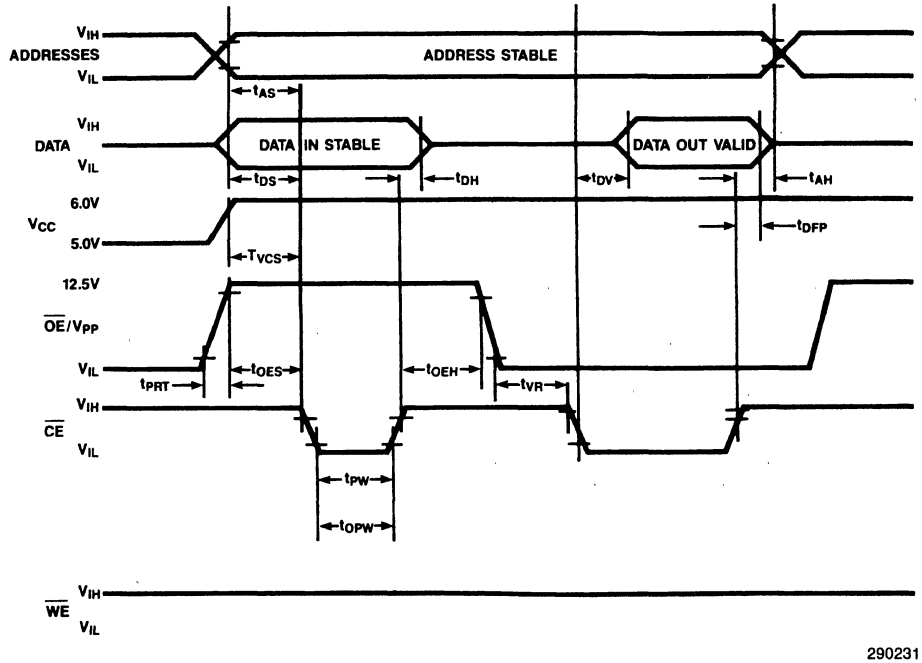
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 2)
t_{VCS}	V_{CC} Setup Time	2			μs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	μs	
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

***AC CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

PROGRAMMING WAVEFORMS



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NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
002	Change 150 speed option to 170.

27C011
PAGE-ADDRESSED 1M (8 x 16K x 8) EPROM

- **Paged Organization**
  - **Reduced Physical Address Requirement**
- **Compatible with 28-Pin JEDEC EPROMs**
  - **Single-Trace Modification for Retrofitting 27128-Based Designs**
- **No-Hardware-Change Upgrades**
  - **Drop-In 27513 Replacement**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm**
  - **Programming Time as Fast as 15 Seconds**
- **Automatic Page Clear**
  - **Resets to Page 0 on Power-Up and On Demand with $\overline{RST}$ Signal**
- **High-Performance**
  - **200 ns Access Time**
  - **Low 30 mA Active Power**
- **Standard EPROM Features**
  - **TTL Compatibility**
  - **Two Line Control**
  - **int$_e$ligent Identifier™ for Automated Programming**
- **Smallest Megabit DIP Package**
  - **28-Pin DIP, Minimal Footprint without Address/Data Multiplexing**

The Intel 27C011 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 8 pages of 16K 8-bit words. Its pin-compatibility with byte-wide JEDEC EPROMs allows retrofitting existing designs to the greater storage capacity afforded by the page-addressed organization. Its 16 K-byte physical address space requirement allows the 27C011 to be utilized in address-constrained system designs.

When a 28-pin DIP socket is configured for 27C64 or 27C128 EPROMs, it is easily retrofitted to the 27C011. By adding a WRITE ENABLE signal to pin 27 (DIP) (unused on 27C64 and 27C128), the 27C011 can be used in an existing design. Thus, the 27C011 enables product enhancements via additional feature sets and firmware-intensive performance upgrades.

The page-addressed organization allows the use of 28-pin DIP packages, the smallest megabit EPROM footprint with applicability to all microprocessors. This provides very efficient circuit board layouts.

The 27C011 is part of a multi-product megabit EPROM family. The other members are standard-addressed byte-wide and word-wide versions, the 27C010 and 27C210, respectively. The 27C010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 27C210 is packaged in a 40-pin DIP with a 64K x 16 organization.

The 27C011 has an automatic page clear circuit for ease of use of its paged organization. The page-select latch is automatically cleared to the lowest order page upon system power-up. The 27C011 also contains many industry-standard features such as two-line output control for simple interfacing and the int$_e$ligent Identifier™ feature for automated programming. It also can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm.

October 1990
Order Number: 290232-002

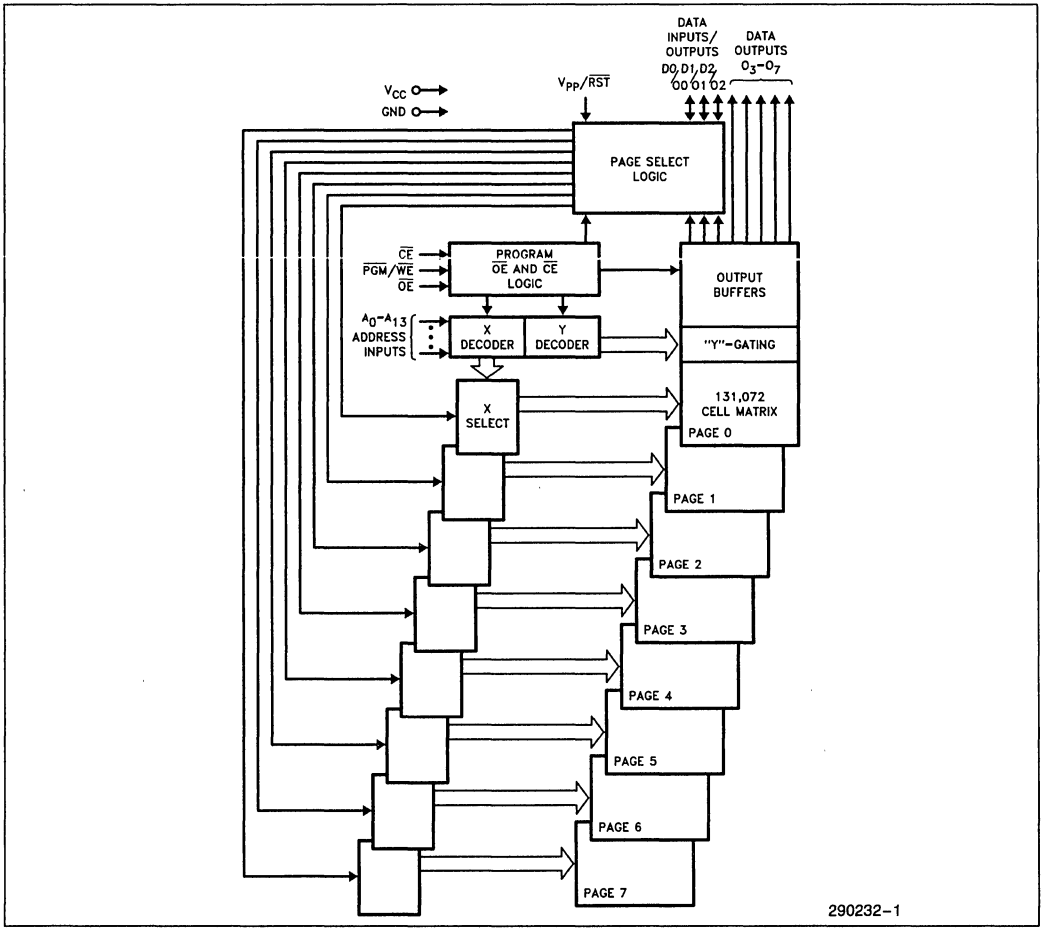
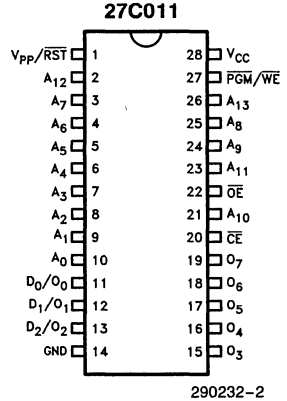


Figure 1. Block Diagram

27C513 27513	27C128 27128A
$\overline{RST}$	V_{PP}
A_{12}	A_{12}
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0
D_0/O_0	O_0
D_1/O_1	O_1
O_2	O_2
GND	GND



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27C128 27128A	27C513 27513
V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{WE}$
A_{13}	A_{13}
A_8	A_8
A_9	A_9
A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Figure 2. Pin Configuration

Pin Names

A_0–A_{13}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Page-Select Write Enable
O_3–O_7	Outputs
D_X/O_X	Input/Outputs (X = 0, 1, or 2)
$V_{PP}/\overline{RST}$	V_{PP}/Page Reset
NC	No Internal Connection
D.U.	Don't Use

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

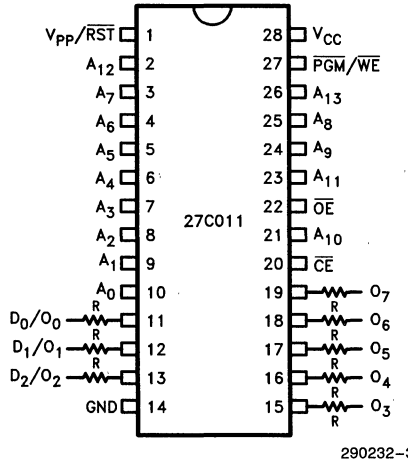
PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8

EXPRESS OPTIONS

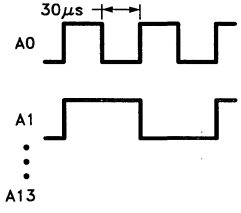
27C011 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-200V10	Q, T, L



290232-3

V_{PP} = +5V R = 1 KΩ V_{CC} = +5V
GND = 0V $\overline{CE}$ = GND



290232-4

Binary Sequence from A_0 to A_{13} required for each page. Page changes during burn-in require the following minimum timing parameter values (see Page-Select AC Characteristics):

t_{WH} = 500 ns
t_{WP} = 500 ns
t_{WR} = 500 ns
t_{DS} = 500 ns
t_{DH} = 500 ns

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.5V
Voltage on A_9 with Respect to Ground ..... −0.6V to +13.0V
V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS TTL and NMOS Inputs, 0°C ≤ T_A ≤ +70°C, V_{CC} ±10%

Symbol	Parameter	Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current			0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to 5.5V
I_{LRST}	$V_{PP}/\overline{RST}$ Load Current	9			500	µA	$V_{PP}/\overline{RST} \le V_{CC}$
I_{SB}	V_{CC} Current Standby				1.0	mA	$\overline{CE}$ = V_{IH}
I_{CC_1}	V_{CC} Current Active	5			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP1}	V_{PP} Current Read	7			10	µA	V_{PP} = V_{CC}
V_{IL}	Input Low Voltage (±10% Supply)	1	−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)		2.0		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{CLR}	Page Latch Clear—V_{CC}			3.5	4.0	V	
I_{OS}	Output Short Circuit Current	6			100	mA	
V_{PP}	V_{PP} Read Voltage	8	V_{CC}−0.7V		V_{CC}	V	

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. Maximum active power usage is the sum of I_{PP} and I_{CC}. The maximum current value is with no loading on outputs O_0 to O_7.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
9. $V_{PP}/\overline{RST}$ should be at a TTL V_{IH} level except during programming or during page 0 reset.

5

READ OPERATION (Continued)

DC CHARACTERISTICS CMOS Inputs

Symbol	Parameter	Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current			0.01	1.0	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current				±10	μA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby	4			100	μA	$\overline{CE}$ = V_{CC}
I_{CC1}	V_{CC} Current Active	5			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP1}	V_{PP} Current Read	7			10	μA	V_{PP} = V_{CC}
V_{IL}	Input Low Voltage (±10% Supply)		−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)		0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		V_{CC}−0.8			V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit Current	6			100	mA	

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled, not 100% tested.
7. Maximum active power usage is the sum of I_{PP} and I_{CC}. The maximum current value is with no loading on outputs O_0 to O_7.

AC CHARACTERISTICS(1) 0°C ≤ T_A ≤ +70°C

Versions	V_{CC} ±10%	27C011-200V10		Units
Symbol	Characteristics	Min	Max	
t_{ACC}	Address to Output Delay		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		70	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	0	60	ns
t_{OH}(2)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		ns

NOTES:
1. See AC Waveforms for Read Operation for timing measurements.
2. Sampled, not 100% tested.

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

AC CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	100		ns	$\overline{OE} = V_{IH}$
t_{WP}	Write Pulse Width	50		ns	$\overline{OE} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	100		ns	
t_{RAV}	Reset to Address Valid	150		ns	

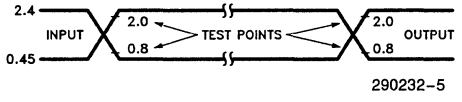
CAPACITANCE(1) $T_A = +25°C$, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{V_{PP}/\overline{RST}}$	$V_{PP}/\overline{RST}$ Capacitance	18	25	pF	$V_{IN} = 0V$

1. Sampled. Not 100% tested.

5

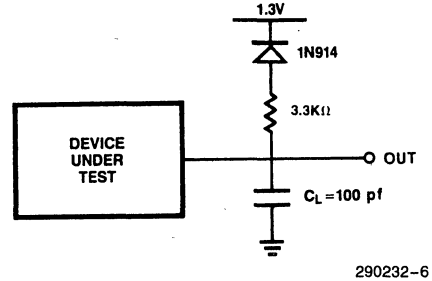
AC TESTING INPUT/OUTPUT WAVEFORM



290232-5

AC Testing inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

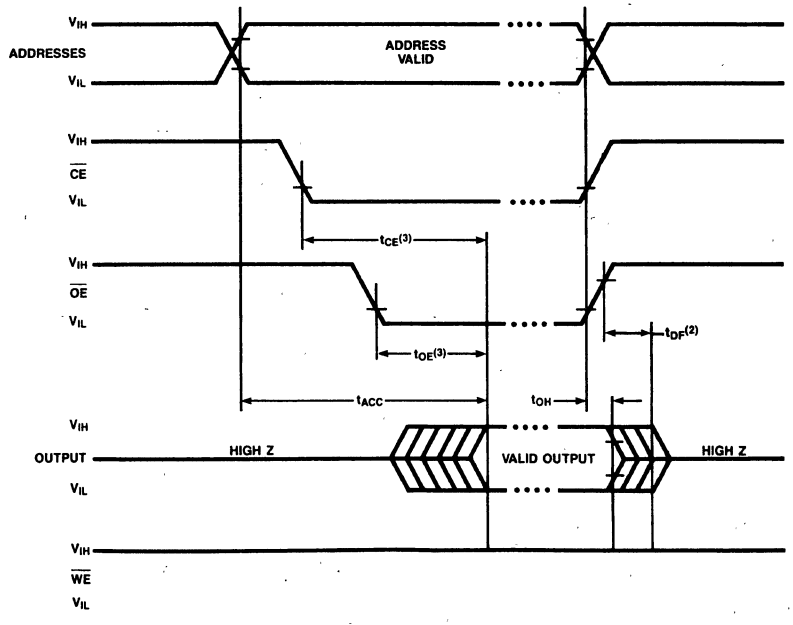
AC TESTING LOAD CIRCUIT



290232-6

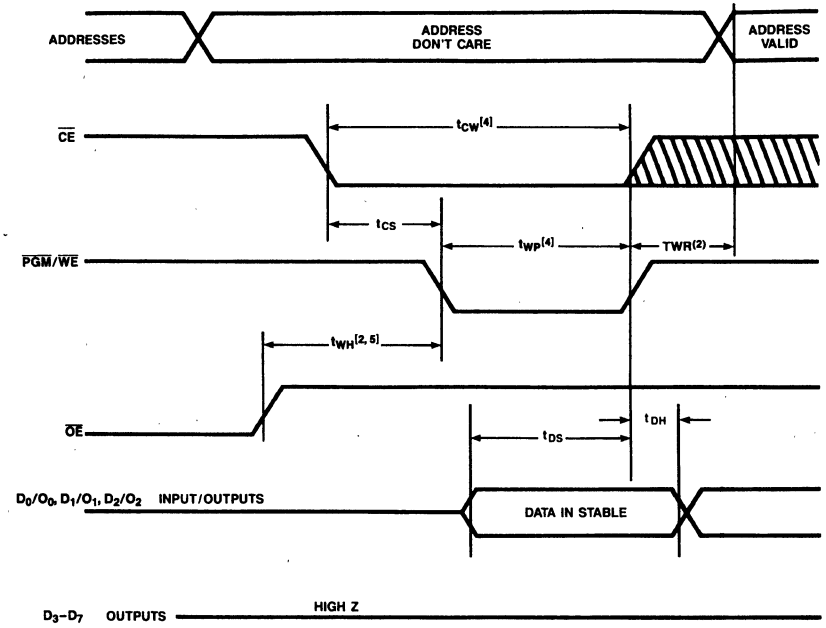
C_L = 100 pF
C_L Includes Jig Capacitance

AC WAVEFORMS FOR READ OPERATION



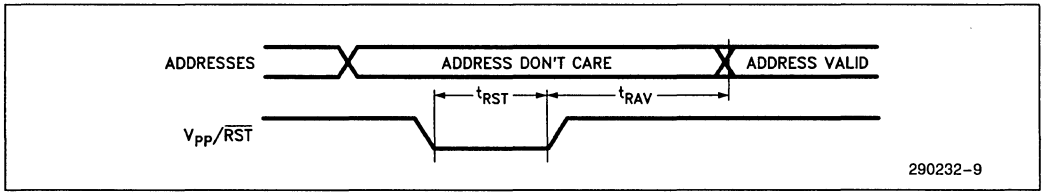
290232-7

AC WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



290232-8

AC WAVEFORMS FOR PAGE-RESET OPERATION



NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27C011 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}/\overline{WE}$	A_9	A_0	$V_{PP}/\overline{RST}$	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{IH}	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{IH}	5.0V	High Z	High Z
Standby	V_{IH}	X	X	X	X	V_{IH}	5.0V	High Z	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}(3)	V_{CC}(3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	X	X	V_{IH}	V_{CC}(5)	(Note 7)	Page D_{IN}
Page-Reset	X	X	X	X	X	V_{IL}	V_{CC}	(Note 7)	X
inteligent Identifier —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IL}	V_{IH}	5.0V	89H	89H
—Device	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IH}	V_{IH}	5.0V	31H	31H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 3 for V_{CC} and V_{PP}.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. $V_H = 12.0V \pm 0.5\%$.
7. State of outputs depends on state of $\overline{CE}$ and $\overline{OE}$. See Outputs State for Read, Output Disable, and Standby Modes.

5

Read Mode

The 27C011 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27C011 is addressed by first selecting one of eight 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0, D_1/O_1 and D_2/O_2. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output / Page Selection	D_2/O_2	D_1/O_1	D_0/O_0
Select Page 0	V_{IL}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}
Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 7	V_{IH}	V_{IH}	V_{IH}

Page Reset

The 27C011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case -10% V_{CC} supply condition) against spurious page latch clearing.

The 27C011 also has a page reset pin: $V_{PP}/\overline{RST}$. This pin should be tied to an active low reset line. These 27C011s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27C011s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The as-

sociated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding. In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} will permanently damage the 27C011.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27C011 is in the programming mode when the V_{PP} input is at its programming voltage and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27C011s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27C011s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27C011s may be common. A TTL low-level pulse applied to the $\overline{PGM}/\overline{WE}$ input with V_{PP} at its programming voltage will program the selected 27C011.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage

Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

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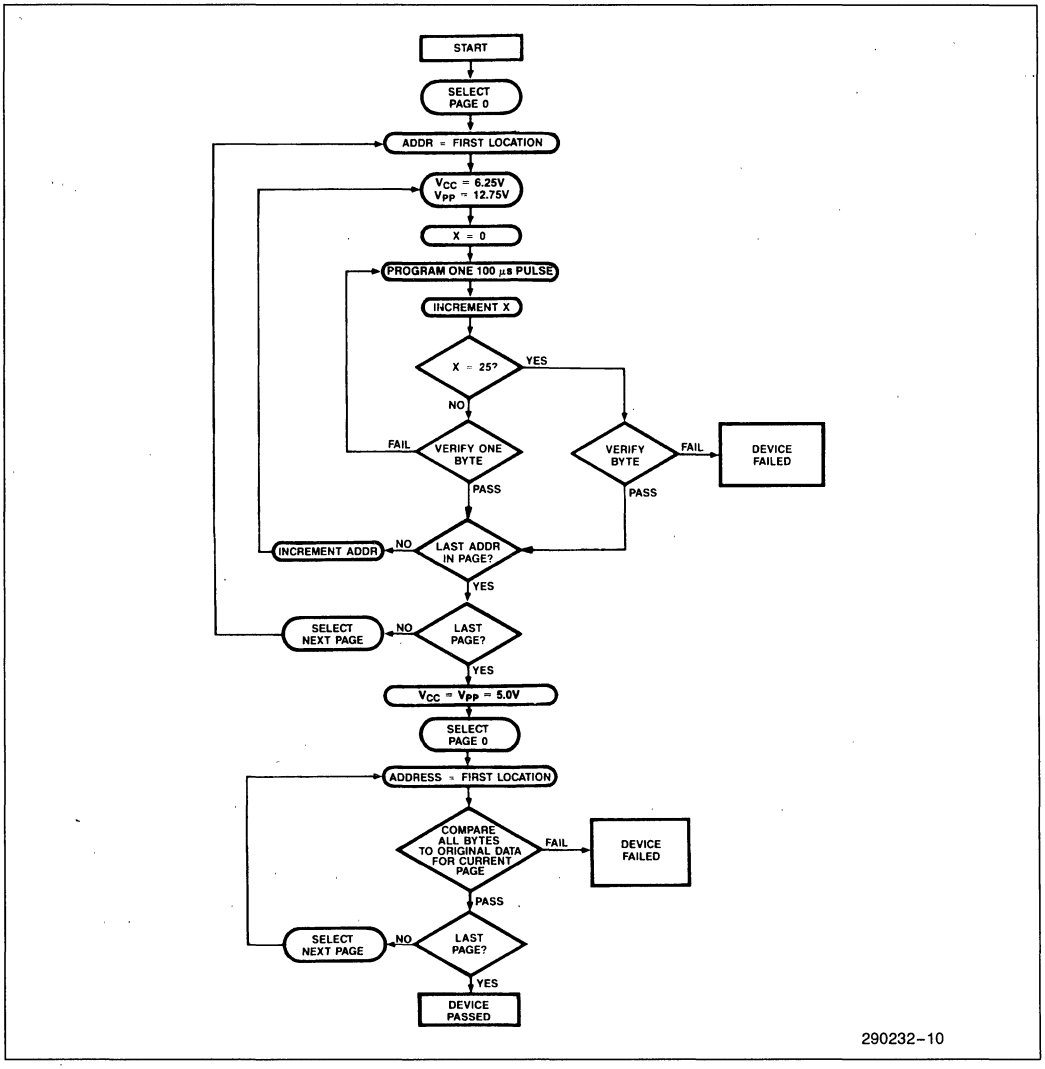


Figure 4. 27C011 Quick-Pulse Programming Flowchart

Quick Pulse Programming Algorithm

Intel's 27C011 EPROM is programmed using the Quick-Pulse Programming algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed as fast as fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming algorithm is shown in Figure 4.

For the Quick-Pulse Programming algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 3

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		1	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.4	6.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program and Verify)		40	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

AC PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 3 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

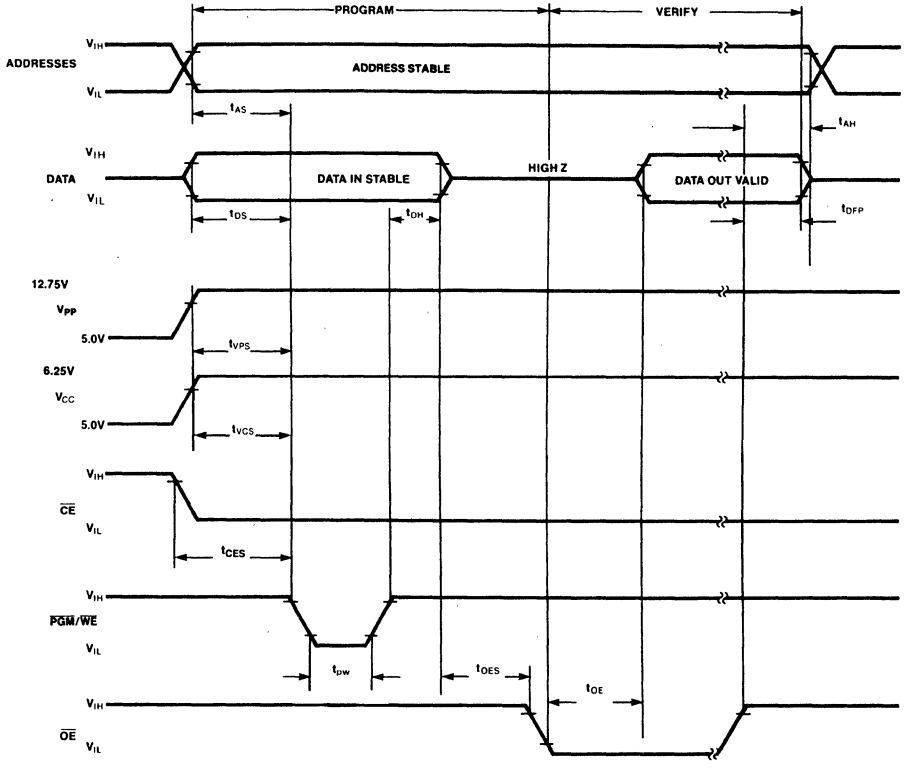
***AC CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

5

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
002	Remove 150 speed option

27C010
1M (128K x 8) CHMOS EPROM

- **JEDEC Approved EPROM Pinouts**
  - **— 32-Pin DIP, 32-Pin PLCC**
  - **— Simple Upgrade from Lower Densities**
- **Complete Upgrade Capability to Higher Densities**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Time as Fast as 15 Seconds**
- **High-Performance**
  - **— 120 ns, ± 10% V_{CC}**
  - **— 30 mA I_{CC} Active**
- **Surface Mount Packaging Available**
  - **— Smallest 1 Mbit Footprint in SMT**

Intel's 27C010 is a 5V only, 1,048,576-bit, Erasable Programmable Read Only Memory, organized as 129,536 words of 8 bits. It is pin compatible with lower density DIP EPROMs (JEDEC) and provides for simple upgrades to 8 Mbits in the future in both DIP and PLCC.

The 27C010 represents state-of-the-art 1 micron CHMOS manufacturing technology while providing unequaled performance. Its 120 ns speed (t_{ACC}) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic DIP (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic DIP (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 32-pin DIP package, Intel also offers a 32-lead PLCC version of the 27C010. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C010 is equally at home in both a TTL or CMOS environment. It programs as fast as 15 seconds using Intel's industry leading Quick-Pulse Programming algorithm.

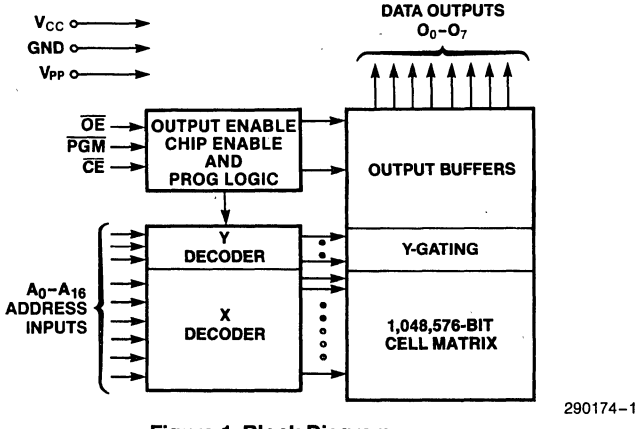


Figure 1. Block Diagram

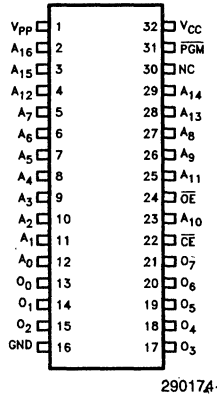
September 1990
Order Number: 290174-004

Pin Names

A_0–A_{19}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

8Mbit	4Mbit	2Mbit	512K	256K
A_{19}	V_{PP}	V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27C010



290174-2

256K	512K	2Mbit	4Mbit	8Mbit
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration

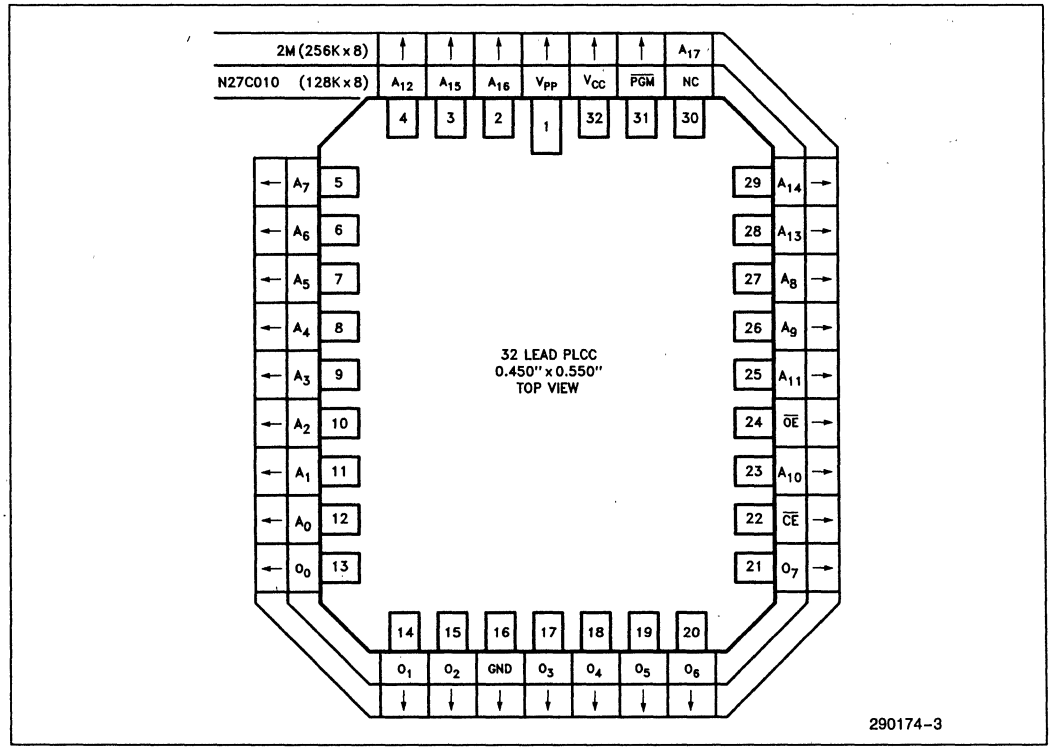


Figure 3. PLCC Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several densities allowing the appropriate memory size to match system requirements. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This processing meets or exceeds most industry burn-in specifications. The EXPRESS product family is available in both 0°C to +70°C and −40°C to +85°C operating temperature range versions. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

EXPRESS EPROM FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to 70°C	168 ±8
T	−40°C to 85°C	None
L	−40°C to 85°C	168 ±8

OPTIONS

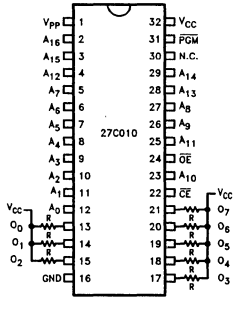
Packaging	
Speed	**CERDIP**
150V10	Q, T, L

READ OPERATION DC CHARACTERISTICS

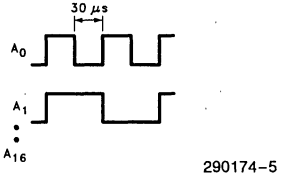
Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27C010(2) LD27C010		Test Condition
		Min	Max	
I_{CC}(1)	V_{CC} Operating Current (mA)		30	$\overline{OE} = \overline{CE} = V_{IL}$, $T_{Ambient} = -40°C$
	V_{CC} Operating Current at High Temperature (mA)		30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTES:
1. Maximum current is with outputs O_0 to O_7 unloaded.
2. D refers to the CERDIP package.



$\overline{OE}$ = +5V R = 1 kΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = GND
$\overline{PGM}$ = +5V



Binary Sequence from A_0 to A_{16}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature Under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.5V(2, 8)

Voltage on A_9 with Respect to GND ..... −0.6V to 13.0V(2)

V_{PP} Program Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS versions.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.
8. Absolute Maximum Ratings apply to NC pins.

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ±10%

Versions[4]		V_{CC} ±10%	27C010-120V10		27C010-150V10 P27C010-150V10 N27C010-150V10		27C010-200V10 P27C010-200V10 N27C010-200V10		Units
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		55		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		30		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{OE}.
3. Sampled, not 100% tested.
4. Model Number Prefixes: No Prefix = CERDIP, P = PDIP, N = PLCC.

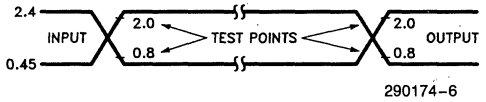
5

CAPACITANCE[1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[2]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

NOTES:
1. Sampled, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

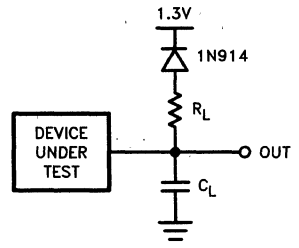
AC INPUT/OUTPUT REFERENCE WAVEFORM



290174-6

AC test inputs are driven at V_{OH} (2.4V $_{TTL}$) for a Logic "1" and V_{OL} (0.45V $_{TTL}$) for a Logic "0". Input timing begins at V_{IH} (2.0V $_{TTL}$) and V_{IL} (0.8V $_{TTL}$). Output timing ends at V_{IH} and V_{IL}. Input Rise and Fall Times (10% to 90%) ≤ 10 ns.

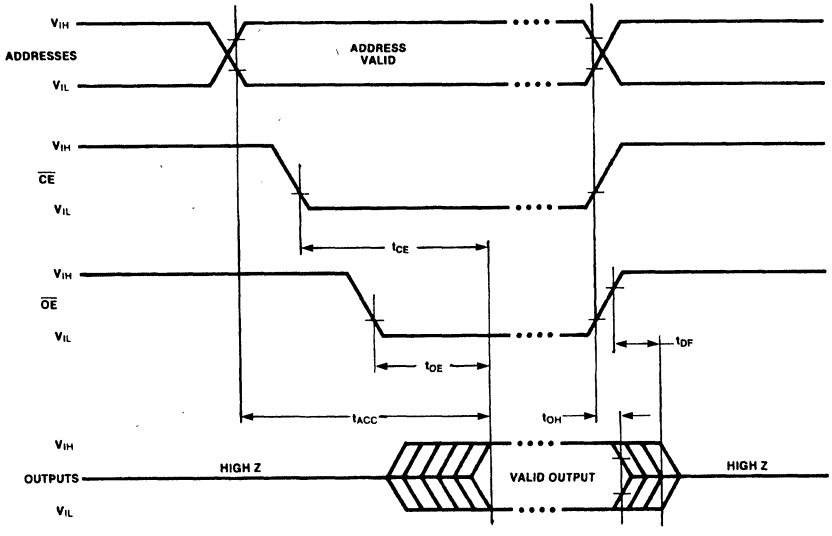
AC TESTING LOAD CIRCUIT



290174-7

C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

AC WAVEFORMS



290174-8

DEVICE OPERATION

The Mode Selection table lists 27C010 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during inteligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	X	X	X	X	V_{PP}	V_{CP}	High Z
inteligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89 H
	Device		V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	V_{CC}	V_{CC}	35 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{16} = V_{IL}.

Read Mode

The 27C010 has two control functions: both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

5

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{PGM}$ low while $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with it's proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{16} at V_{IL}, $A_0 = V_{IL}$ will present the manufacturer code and $A_0 = V_{IH}$ the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to 2-Mbit, 4-Mbit, and 8-Mbit densities are easily accomplished due to the standardized pin configuration of the 27C010. When the 27C010 is in Read Mode, the $\overline{PGM}$ input becomes non-functional. The $\overline{PGM}$ and NC pins may be V_{IL} or V_{IH}. This allows address lines A_{17}–A_{18} to be routed directly to these inputs in anticipation of future density upgrades. A jumper between V_{CC} and A_{19} allows further upgrade using the V_{PP} pin. Systems designed for 1-Mbit program memories today can be upgraded to higher densities (2-Mbit, 4-Mbit, and 8-Mbit) in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

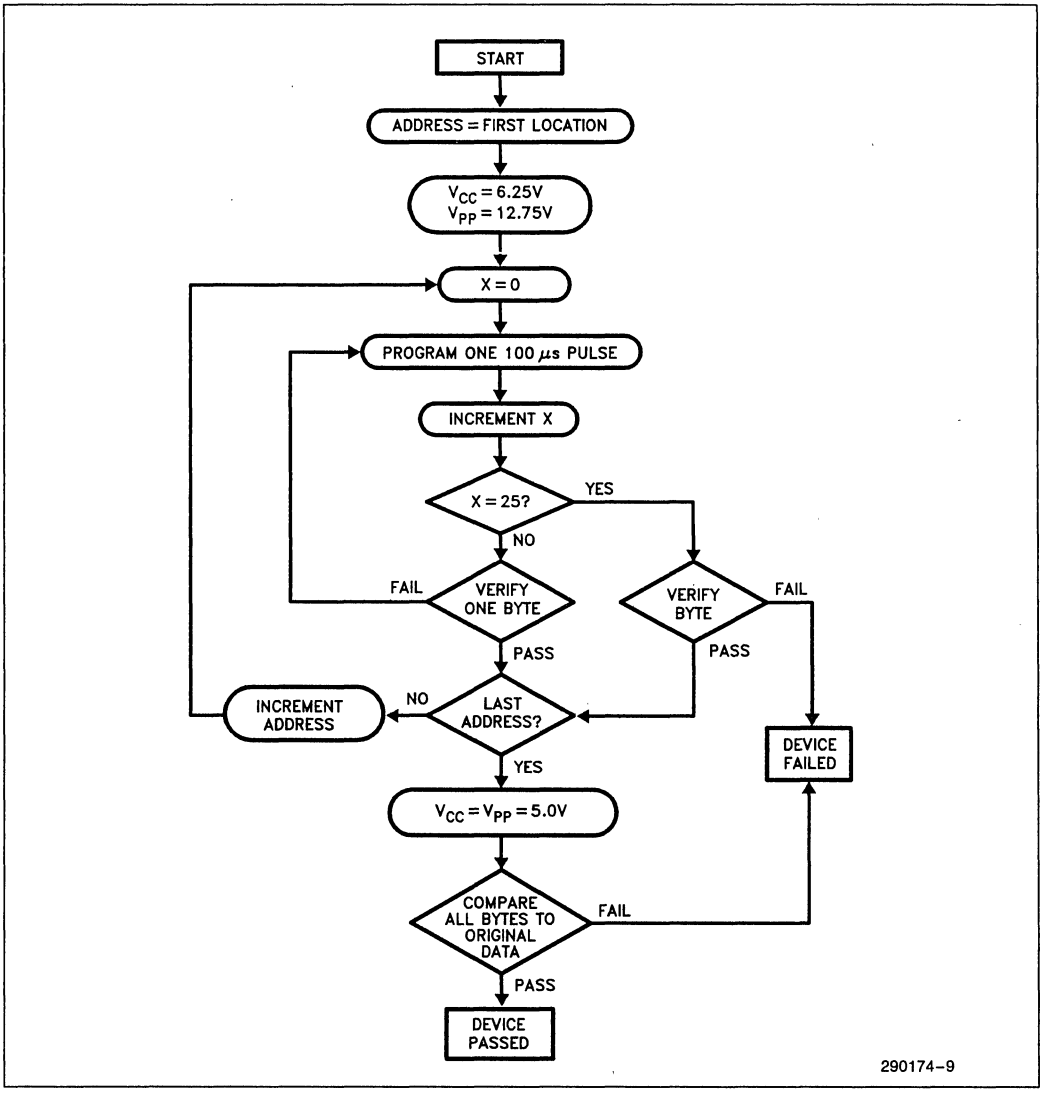


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse programming algorithm programs Intel's 27C010. Developed to substantially reduce programming throughput, this algorithm can program the 27C010 as fast as 15 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

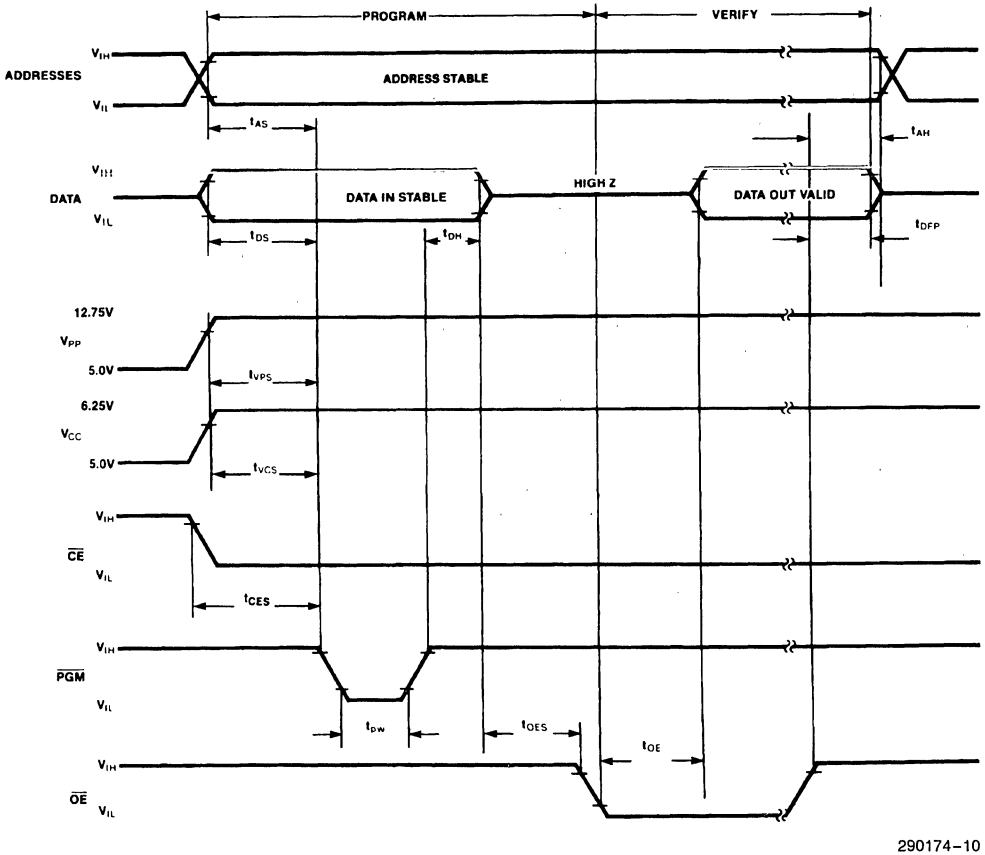
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			40	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_7 unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
04	Revised general datasheet structure, text to improve clarity. Added PDIP package Combined TTL/NMOS and CMOS Read Operation DC Characteristics tables. Deleted 4 Meg and 8 Meg PLCC pinout references.

27C100
1M (128K x 8) CHMOS EPROM

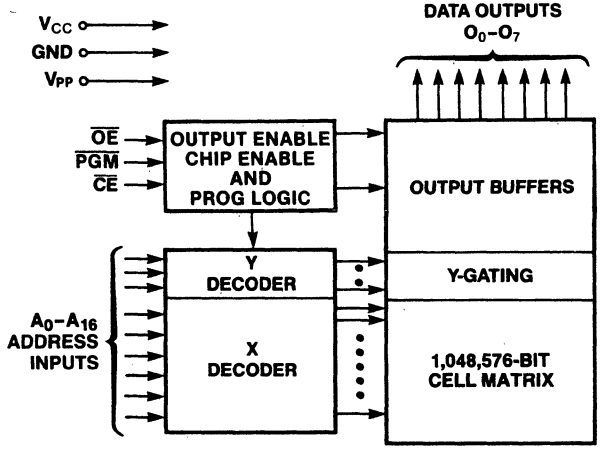
- **Pin Compatible with 28-Pin 1 Mbit MASK ROM**
- **Low Power Consumption**
  - **— 30 mA Max. Active**
  - **— 100 μA Max. Standby**
- **CMOS and TTL Compatibility**
- **High Performance**
  - **— ±10% V_{CC}**
  - **— 120 ns Maximum Access Time**
- **Quick-Pulse Programming™ Algorithm**
  - **— Programming as Fast as 15 Seconds**
- **32-Pin CERDIP and PDIP Packages**

Intel's 27C100 is a 5V-only, 1,048,576 bit, Erasable Programmable Read Only Memory organized as 131,072 bytes of 8 bits. It employs advanced CHMOS* III E circuitry for systems requiring low power, high speed performance and noise immunity. This device is pin compatible with 28-pin 1 Mbit MASK ROMs.

The 27C100's 120 ns speed (t_{ACC}) offers no-wait-state operation with high-performance CPUs in applications ranging from numerical control to office automation and telecommunications. The 27C100 is equally at home in both TTL and CMOS environments.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic DIP (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic DIP (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion. This EPROM solution is particularly well-suited for "Just-In Time" code customization to meet specific geographic or application needs in your product line. The Quick-Pulse Programming™ Algorithm provides fast, reliable programming.

*CHMOS is a patented process of Intel Corporation.



290270-1

Figure 1. Block Diagram

October 1990
Order Number: 290270-002

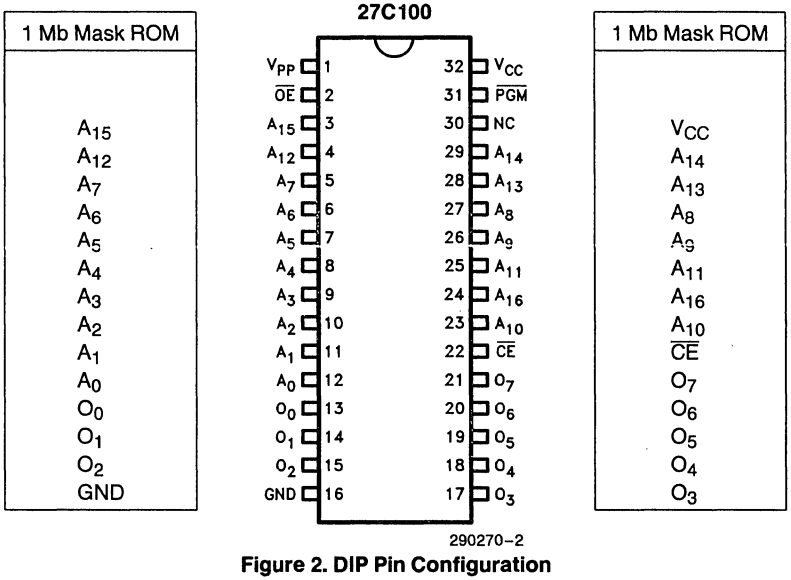


Figure 2. DIP Pin Configuration

Pin Names

A_0–A_{16}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
$\overline{PGM}$	PROGRAM
NC	NO CONNECT

5

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.25V(2)

Voltage on A_9 with Respect to GND ..... −0.6V to 13V(2)

V_{PP} Program Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7V(2)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			30	mA	f = 5 MHz, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

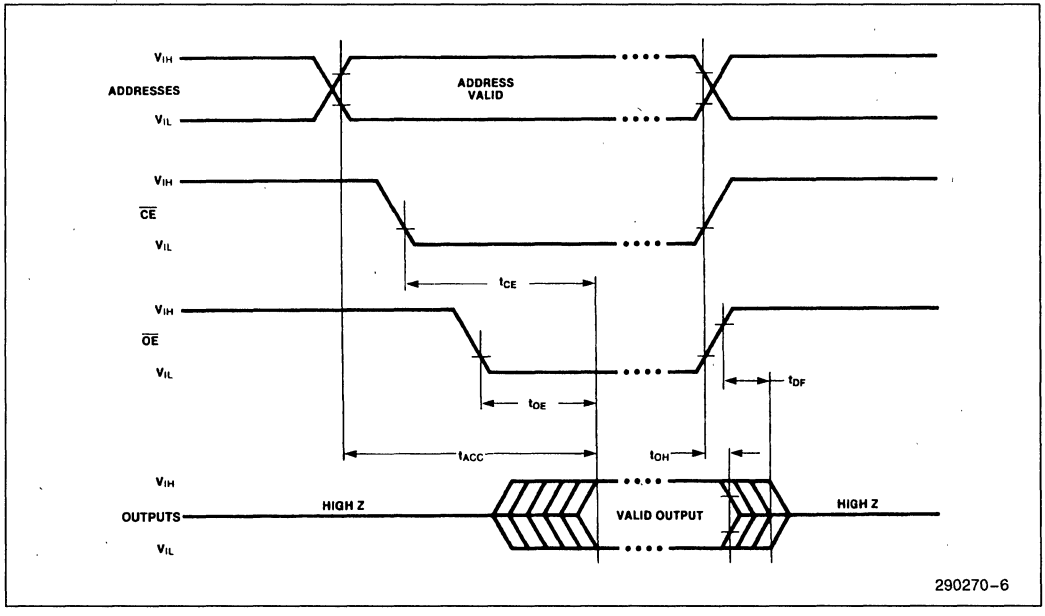
NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0–O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC} or may be 1 diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.
8. Absolute Maximum rating applies to NC pins.

READ OPERATION AC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Versions(4)	V_{CC} ±10%		27C100-120V10		27C100-150V10 P27C100-150V10		27C100-200V10 P27C100-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		55		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		30		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change— Whichever Occurs First	3	0		0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model Number Prefixes: No Prefix = CERDIP, P = PDIP.

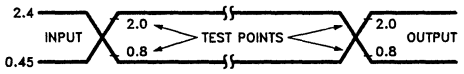
AC WAVEFORMS



CAPACITANCE[4] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[5]	Max	Unit	Condition
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	16	25	pF	V_{PP} = 0V

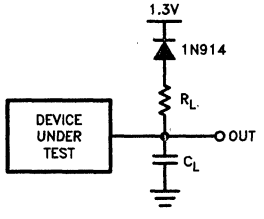
AC INPUT/OUTPUT REFERENCE WAVEFORM



290270-7

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤10 ns.

AC TESTING LOAD CIRCUIT



290270-8

C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

DEVICE OPERATION

The Mode Selection table lists 27C100 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier™ Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	1	V_{IL}	V_{IL}	X	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby		V_{IH}	X	X	X	X	V_{CC}	V_{CC}	High Z
Program	2	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	2, 3	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89H
-Manufacturer		V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	V_{CC}	V_{CC}	32H
-Device									

NOTES:
1. X can be V_{IL} or V_{IH}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{16} = V_{IL}.
4. Sampled, not 100% tested.
5. Typical limits are at V_{CC} = 5V, T_A = 25°C.

Read Mode

The 27C100 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{PGM}$ low while $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed with V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$, parallel EPROMs may have common inputs.

5

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With A_1–A_8, A_{10}–A_{16}, $\overline{CE}$ and $\overline{OE}$ at V_{IL}, A_0 = V_{IL} will present the manufacturer's code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

ROM Compatibility

The 27C100 is compatible with 28-pin mask ROMs to provide a reprogrammable memory solution during prototyping and early production. Reference Figure 2; design in the 32-pin socket for the 27C100 EPROM and connect V_{CC} to pins 1, 30 and 32. If the EPROM is replaced with a MROM, socket pins 1, 2, 31 and 32 are no longer required.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues—standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

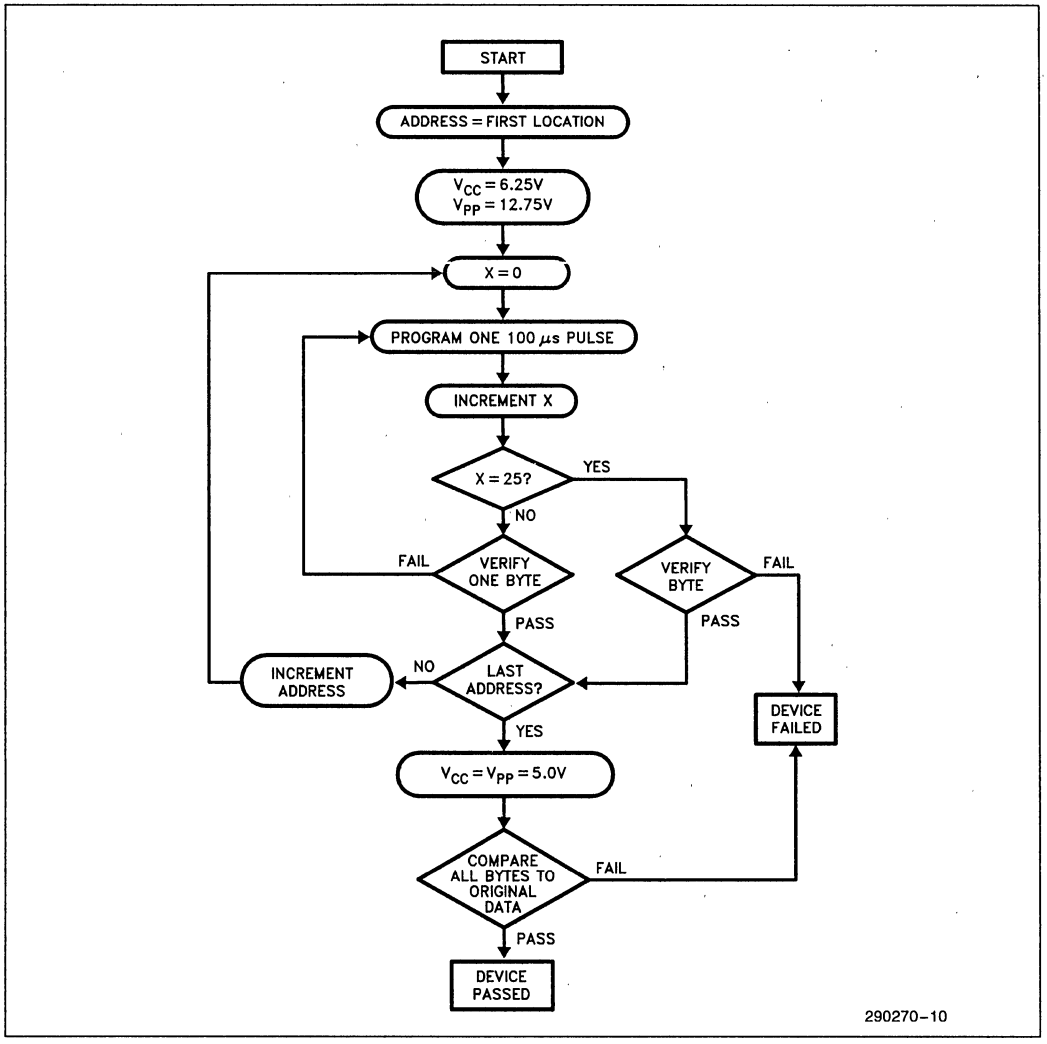


Figure 3. Quick-Pulse Programming Algorithm

Quick-Pulse Programming Algorithm

The Quick-Pulse programming algorithm programs Intel's 27C100. Developed to substantially reduce programming throughput, this algorithm can program the 27C100 as fast as 15 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program-pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

5

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

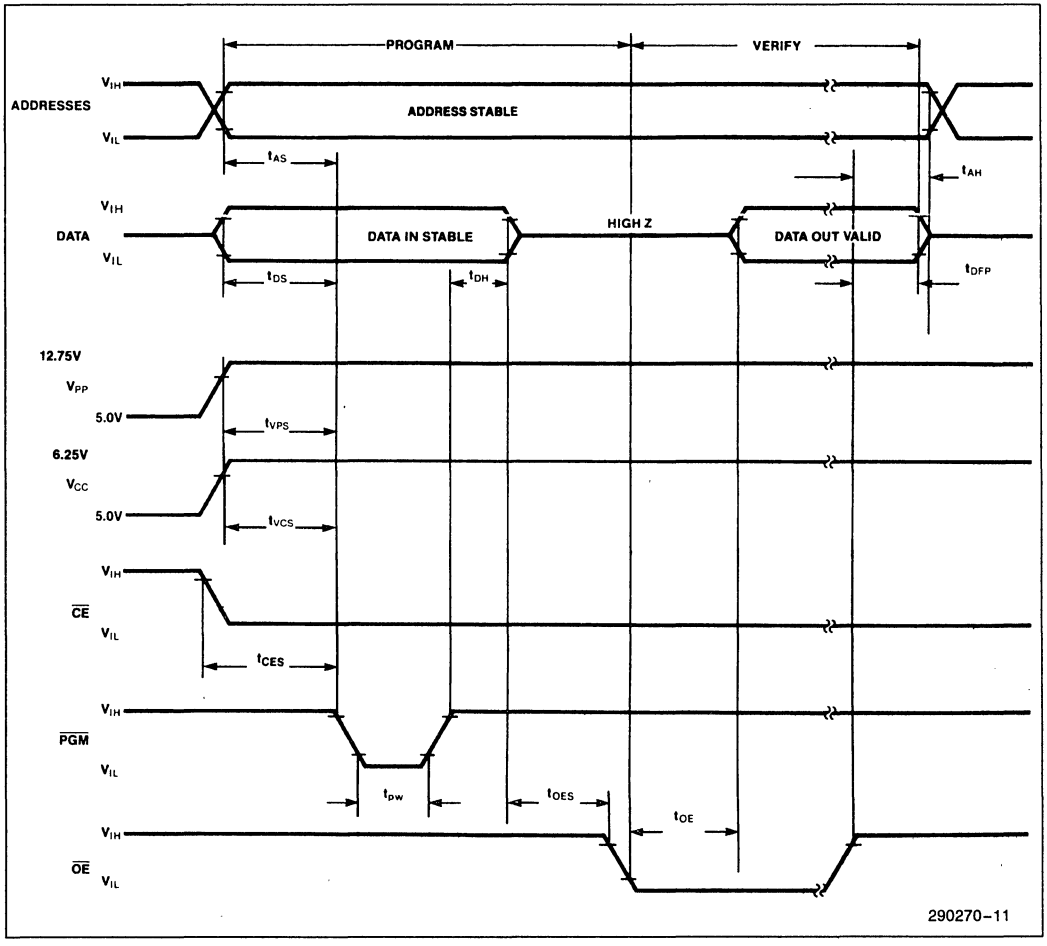
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			40	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 inteligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_7 unloaded.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required between V_{PP} and GND to suppress spurious voltage transients, which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
002	Deleted −120 PDIP package. Revised classification from **Advance Information** to **Preliminary**. Deleted Express Offerings.

27C020
2M (256K x 8) CHMOS EPROM

- **JEDEC Approved EPROM Pinouts**
  - **— 32-Pin DIP, 32-Pin PLCC**
  - **— Simple Upgrade from Lower Densities**
- **Complete Upgrade Capability to Higher Densities**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Time as Fast as 30 Seconds**
- **High-Performance**
  - **— 150 ns, ±10% V_{CC}**
  - **— 30 mA I_{CC} Active**
- **Surface Mount Packaging Available**
  - **— Smallest 1 Mbit Footprint in SMT**

Intel's 27C020 is a 5V-only, 2,097,152-bit Erasable Programmable Read Only Memory, organized as 262,144 words of 8 bits each. It is pin compatible with lower density DIP EPROMs (JEDEC) and provides for simple upgrades to 8 Mbits in the future in both DIP and PLCC.

The 27C020 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 150 ns speed (t_{ACC}) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic DIP (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic DIP (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 32-lead DIP package, Intel also offers a 32-lead PLCC version of the 27C020. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C020 is equally at home in both a TTL or CMOS environment. It programs as fast as 30 seconds using Intel's industry leading Quick-Pulse Programming algorithm.

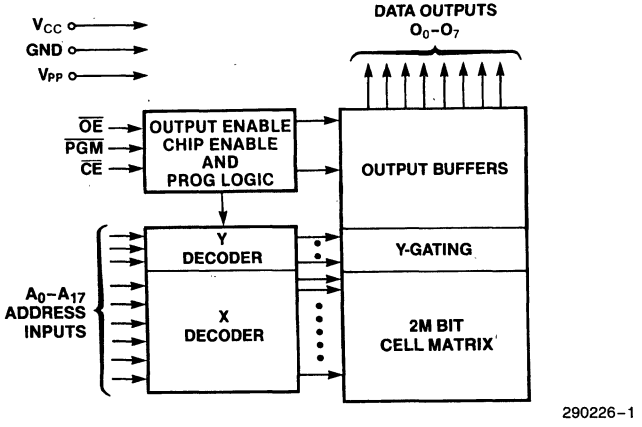


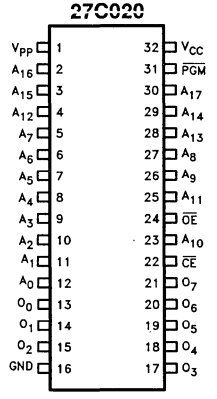
Figure 1. Block Diagram

September 1990
Order Number: 290226-003

Pin Names

A_0–A_{19}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

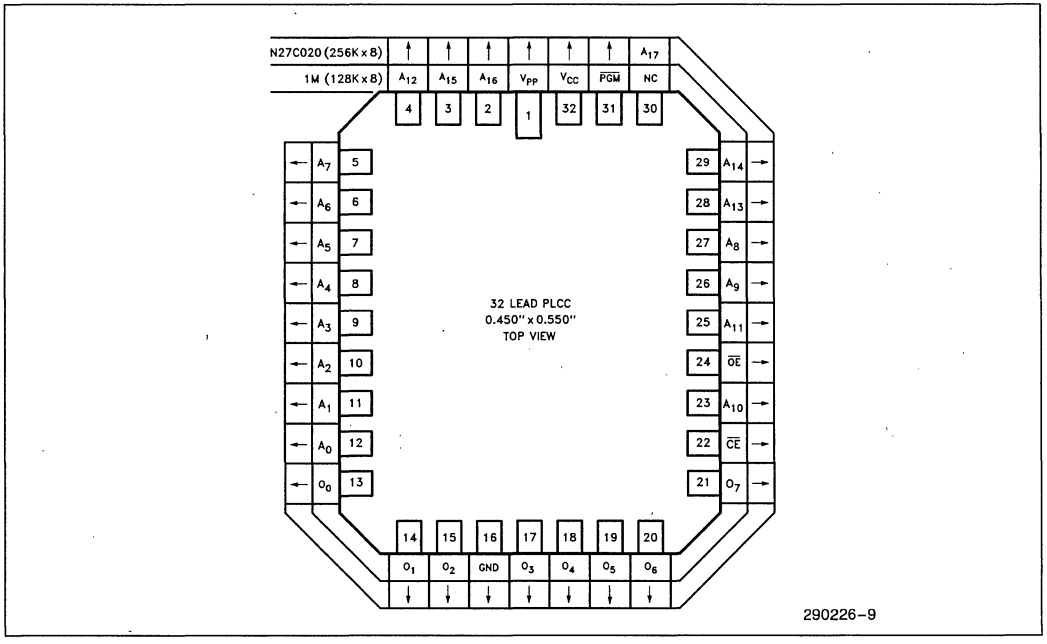
8Mbit	4Mbit	1Mbit	512K	256K
A_{19}	V_{PP}	V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290226-2

256K	512K	1Mbit	4Mbit	8Mbit
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	N.C.	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration



290226-9

Figure 3. PLCC Lead Configuration

5

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature Under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.5V(2)

Voltage on A_9 with Respect to GND ..... −0.6V to 13.0V(2)

V_{PP} Program Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7.0V(2)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	$V_{IN} = 0V$ to 5.5V
I_{LO}	Output Leakage Current				±10	µA	$V_{OUT} = 0V$ to 5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE} = V_{IH}$
					100	µA	$\overline{CE} = V_{CC} \pm 0.2V$
I_{CC}	V_{CC} Operating Current	3			30	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA
I_{PP}	V_{PP} Operating Current	3			10	µA	$V_{PP} = V_{CC}$
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -400$ µA
V_{PP}	V_{PP} Operating Voltage	5	$V_{CC} - 0.7$		V_{CC}	V	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum $I_{PP} + I_{CC}$. Maximum current is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.

READ OPERATION AC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Versions(4)		V_{CC} ±10%	27C020-150V10		27C020-200V10 P27C020-200V10 N27C020-200V10		Unit
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay			150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{OE}.
3. Sampled, not 100% tested.
4. Model number prefixes: No Prefix = CERDIP, P = PDIP, N = PLCC.

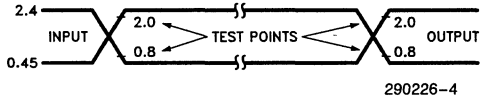
5

CAPACITANCE[1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[2]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

NOTES:
1. Sampled, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

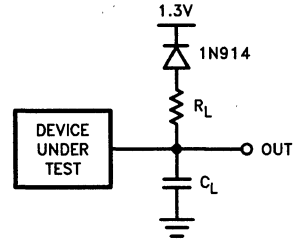
AC INPUT/OUTPUT REFERENCE WAVEFORM



290226-4

AC testing inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤10 ns.

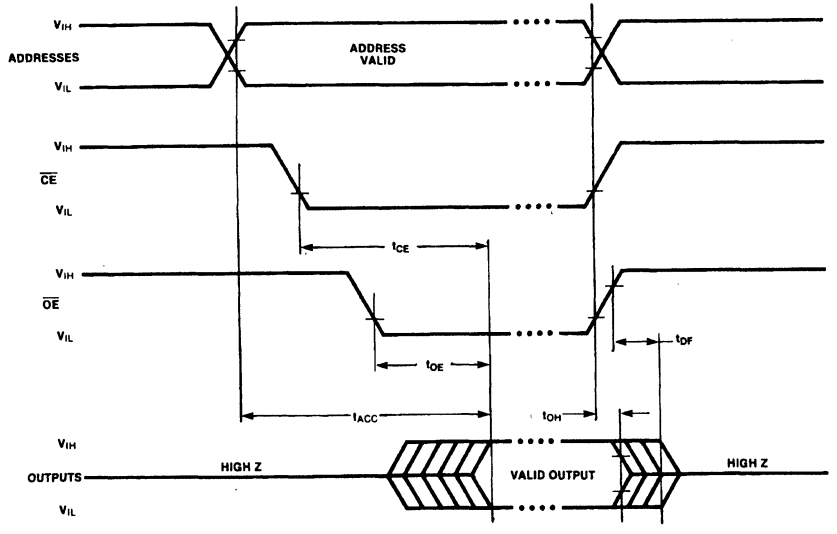
AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

290226-5

AC WAVEFORMS



290226-6

DEVICE OPERATION

The Mode Selection table lists 27C020 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	X	X	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89 H
	Device		V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	V_{CC}	V_{CC}	34 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. See DC Programming Characteristics for V_{CP}, V_{PP}, and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{17} = V_{IL}

Read Mode

The 27C020 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH} the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{PGM}$ low while $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1-A_8, and $A_{10}-A_{17}$ at V_{IL}, $A_0 = V_{IL}$ will present the manufacturer code and $A_0 = V_{IH}$ the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to 4-Mbit and 8-Mbit densities are easily accomplished due to the standardized pin configuration of the 27C020. When the 27C020 is in Read Mode, the $\overline{PGM}$ input becomes non-functional. This allows address line A_{18} to be routed directly to to this input in anticipation of future density upgrades. A jumper between V_{CC} and A_{19} allows further upgrade using the V_{PP} pin. Systems designed for 2-Mbit program memories today can be upgraded to higher densities (4-Mbit and 8-Mbit) in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm². Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm² (1 week @ 12000 μW/cm²).

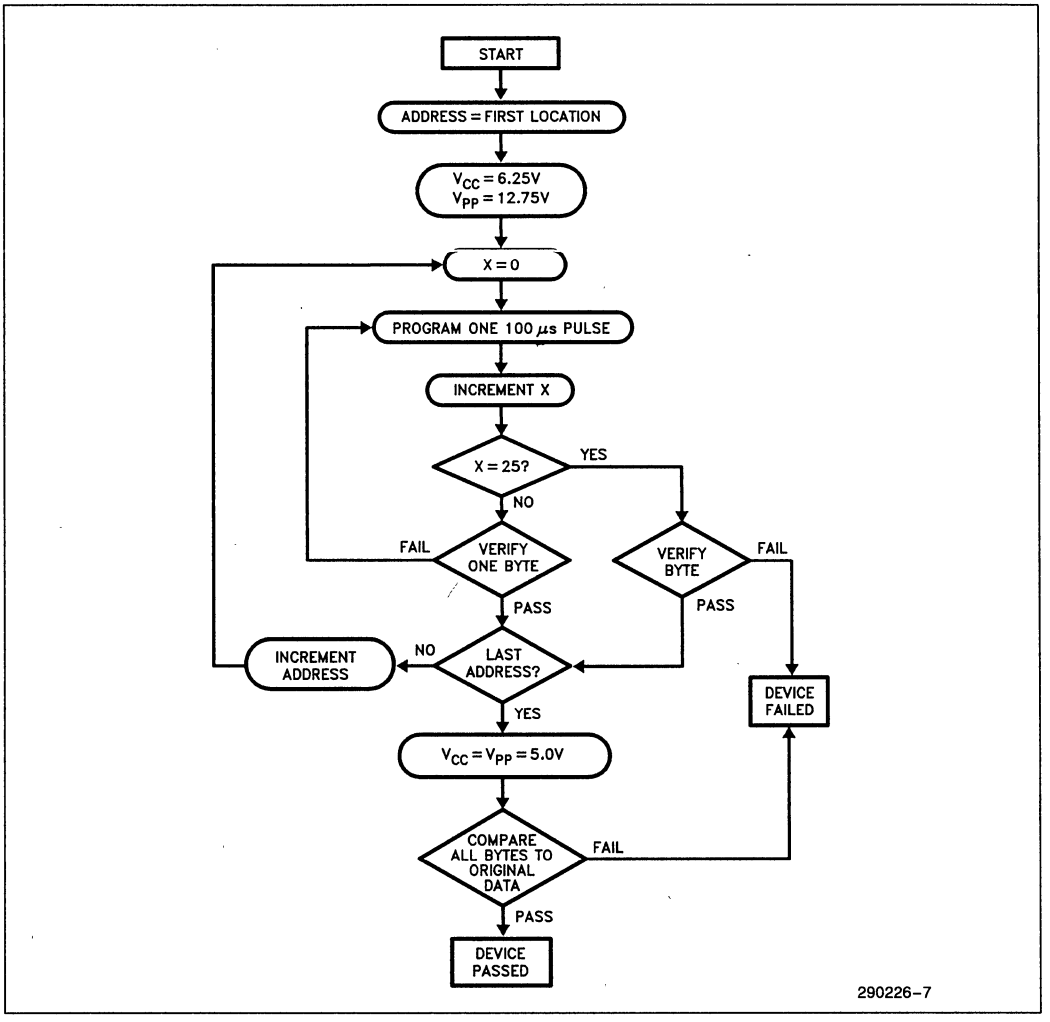


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse programming algorithm programs Intel's 27C020. Developed to substantially reduce programming throughput, this algorithm can program the 27C020 as fast as 30 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

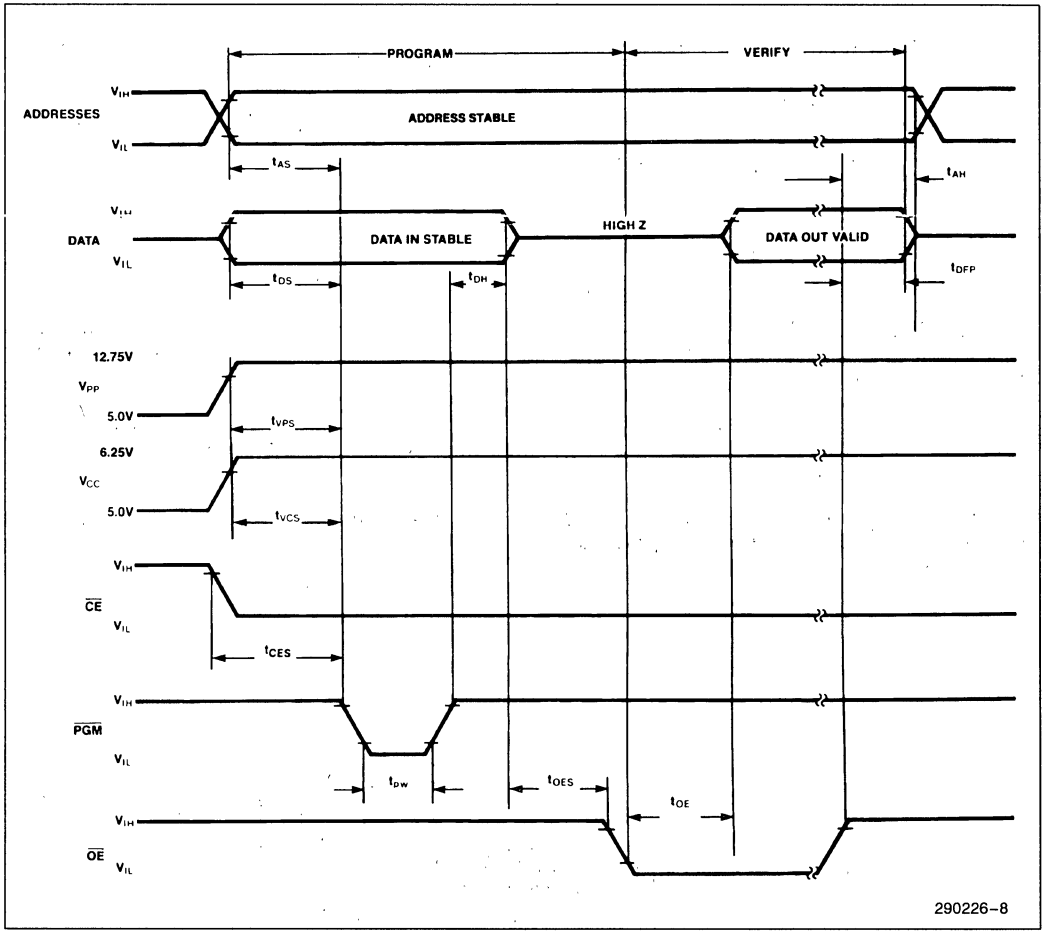
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			40	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0		
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CC} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_7 unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
003	Revised general datasheet structure, text to improve clarity Added PDIP package Combined TTL/NMOS and CMOS Read Operation Characteristics tables Revised classification from **Advance Information** to **Preliminary** Deleted 4 Meg and 8 Meg PLCC pinout references. Deleted EXPRESS page

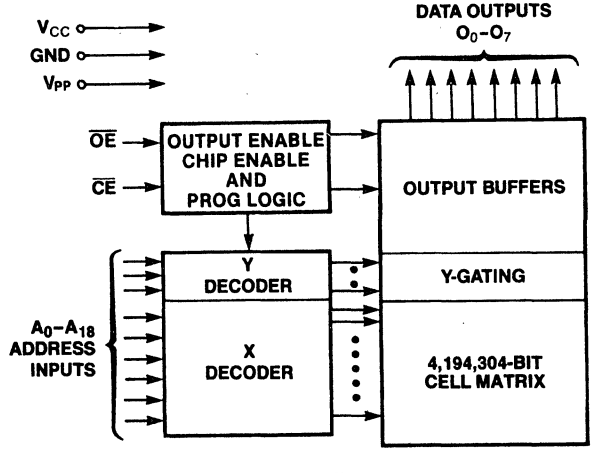
27C040
4M (512K x 8) CHMOS EPROM

- **JEDEC Approved EPROM Pinout**
  - **— 32-Pin DIP**
  - **— Simple Upgrade from Lower Densities**
- **Easy Upgrade Capability to 8 Mbit Density**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Time as Fast as 60 Seconds**
- **High-Performance**
  - **— 150 ns, ±10% V_{CC}**
  - **— 50 mA I_{CC} Active**

The Intel 27C040 is a 5V-only, 4,194,304-bit Erasable Programmable Read Only Memory, organized as 524,288 words of 8 bits each. It is pin compatible with lower density DIP EPROMs (JEDEC) and provides for simple upgrade to 8 Mbits in the future.

The 27C040 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 150 ns speed (T_{ACC}) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

The 27C040 is equally at home in both a TTL or CMOS environment. It programs as fast as 60 seconds using Intel's industry leading Quick-Pulse Programming algorithm.



290239-1

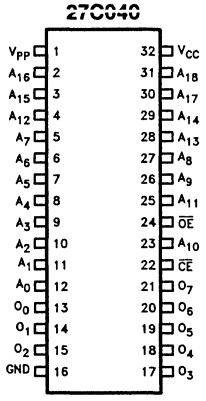
Figure 1. Block Diagram

September 1990
Order Number: 290239-002

Pin Names

A_0–A_{19}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O_0-O_7	OUTPUTS
NC	NO INTERNAL CONNECT

8Mbit	2Mbit	1Mbit	512K	256K
A_{19}	V_{PP}	V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



290239–2

256K	512K	1Mbit	2Mbit	8Mbit
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A_{18}
V_{CC}	V_{CC}	NC	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. DIP Pin Configuration

5

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature Under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.5V(2)

Voltage on A_9 with Respect to GND ..... −0.6V to 13.0V(2)

V_{PP} Supply Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7.0V(2)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	μA	$V_{IN} = 0V$ to 5.5V
I_{LO}	Output Leakage Current				±10	μA	$V_{OUT} = 0V$ to 5.5V
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE} = V_{IH}$
					100	μA	$\overline{CE} = V_{CC} \pm 0.2V$
I_{CC}	V_{CC} Operating Current	3			50	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	μA	$V_{PP} = V_{CC}$
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -400$ μA
V_{PP}	V_{PP} Operating Voltage	5	$V_{CC} - 0.7$		V_{CC}	V	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
3. Maximum active power usage is the sum $I_{PP} + I_{CC}$. Maximum current is with outputs O_0 to O_7 unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.

READ OPERATION AC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

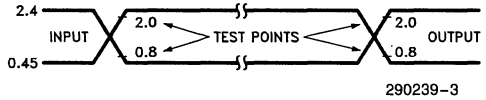
Versions(4)		V_{CC} ±10%	27C040-150V10		27C040-200V10		Units
Symbol	Parameter	Notes	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model number prefixes: No prefix = CERDIP.
5. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE(3) T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ(5)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

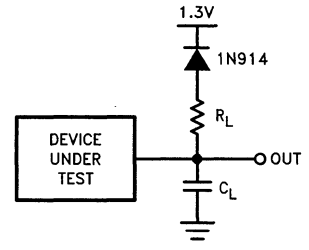
AC INPUT/OUTPUT REFERENCE WAVEFORM



290239-3

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤ 10 ns.

AC TESTING LOAD CIRCUIT

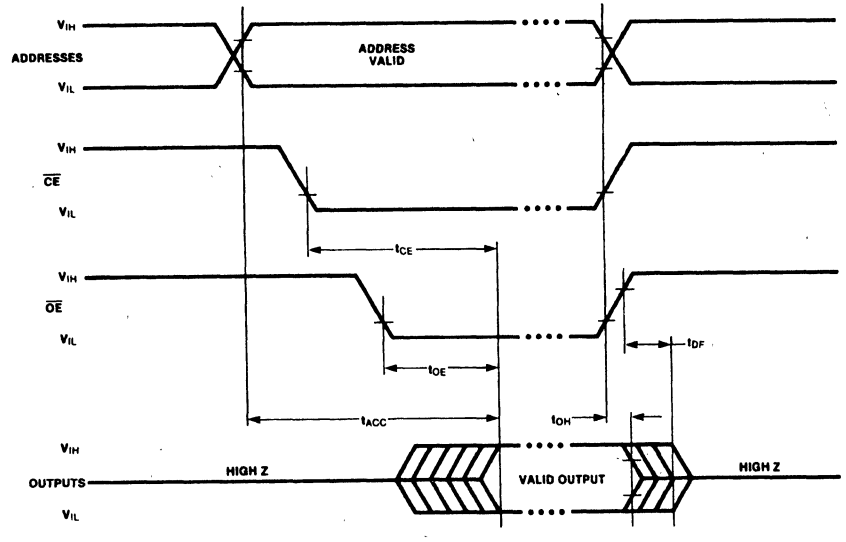


C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 KΩ

290239-4

5

AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C040 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	V_{IH}	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	V_{CC}	89 H
	Device		V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	V_{CC}	3D H

NOTES:
1. X can be V_{IL} or V_{IH}
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{18} = V_{IL}

Read Mode

The 27C040 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, and address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE}$ = V_{IH} programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V a substantial program margain is ensured. The verify is performed with $\overline{CE}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{18} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to the 8 Mbit density is easily accomplished due to the standardized pin configuration of the 27C040. A jumper between V_{CC} and A_{19} allows upgrade using the V_{PP} pin. Systems designed for 4 Mbit program memories today can be upgraded to 8 Mbit in the future with no circuit board changes.

5

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity $\times$ exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

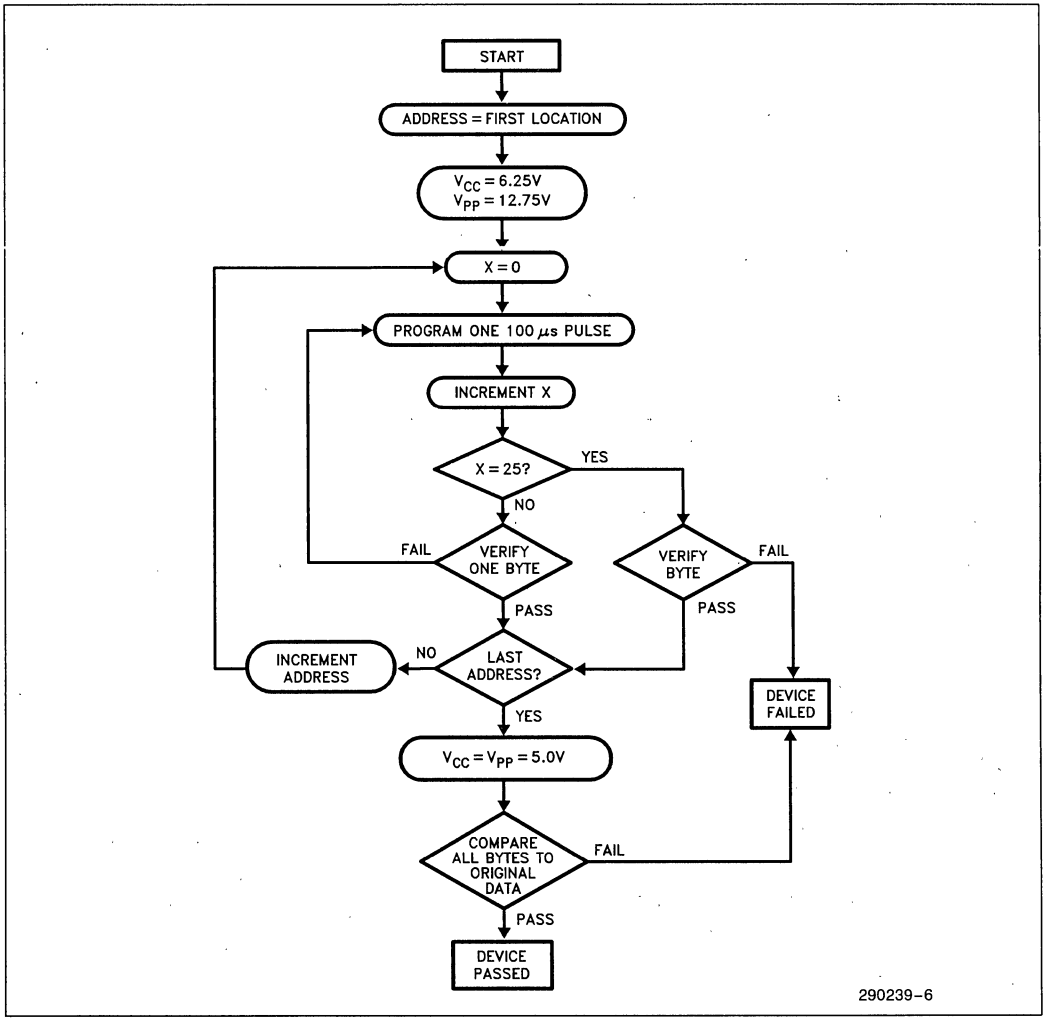


Figure 3. Quick-Pulse Programming Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming Algorithm programs Intel's 27C040. Developed to substantially reduce programming throughput, this algorithm can program the 27C040 as fast as 60 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse Programming Algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.0V.

5

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

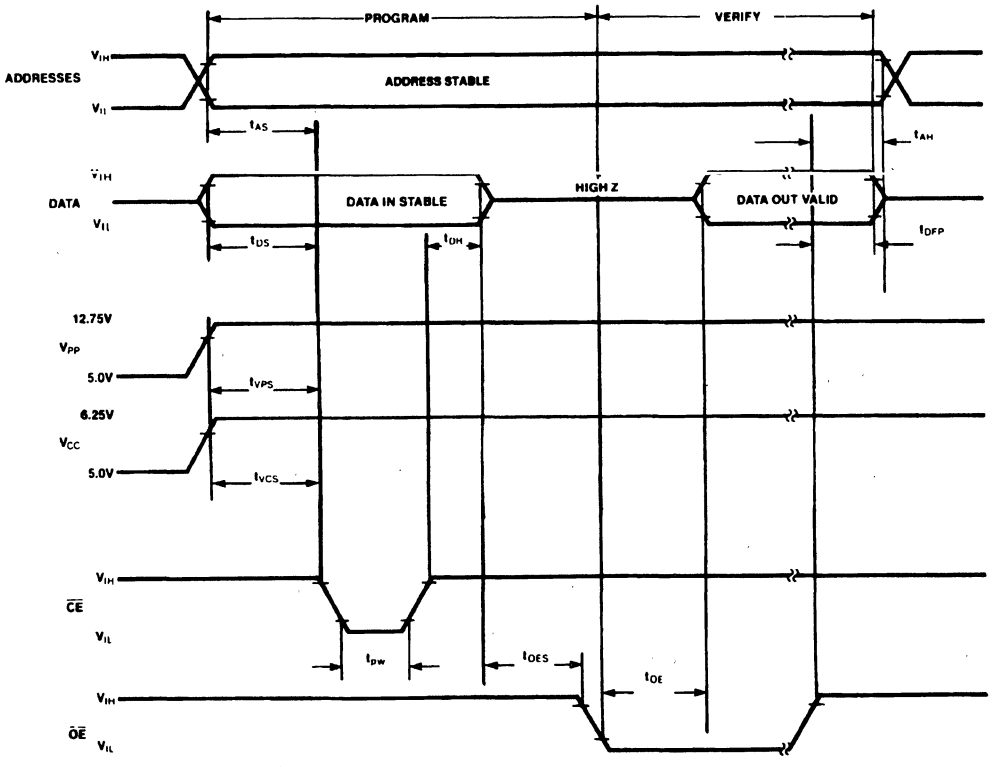
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_7 unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
02	Revised general datasheet structure, text to improve clarity. Combined TTL/NMOS and CMOS Read Operation DC Characteristics Tables. Mode Selection table-Program Inhibit-$\overline{OE}$ revised from **X** to V_{IH}.

27C210
1M (64K x 16) CHMOS EPROM

- **JEDEC Approved EPROM Pinouts**
  - **— 40-Pin DIP**
  - **— 44-Pin PLCC**
- **Complete Upgrade to Higher Densities**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **High-Performance**
  - **— 120 ns ±10% V_{CC}**
  - **— 50 mA I_{CC} Active**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Times As Fast As 8 Seconds**

Intel's 27C210 is a 5V only, 1,048,576-bit Erasable Programmable Read Only Memory, organized as 65,536 words of 16 bits each. Its standard pinouts provide for simple upgrades to 4 Mbits in the future.

The 27C210 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 120 ns speed (t_{ACC}) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 40-pin DIP package, Intel also offers a 44-lead PLCC version of the 27C210. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C210 is equally at home in both a TTL or CMOS environment. And like Intel's other 1 Mbit EPROMs, the 27C210 programs quickly using Intel's industry leading Quick-Pulse Programming algorithm.

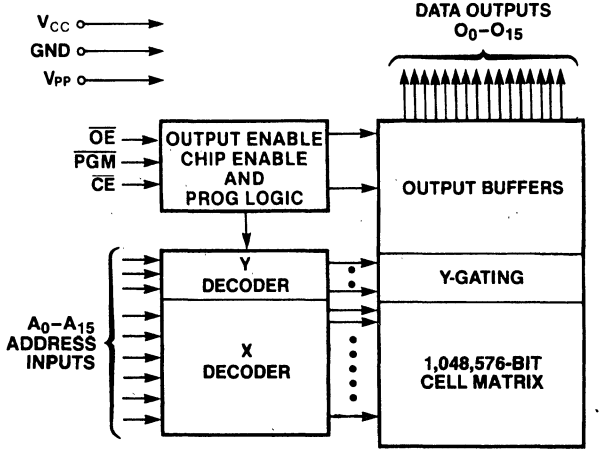


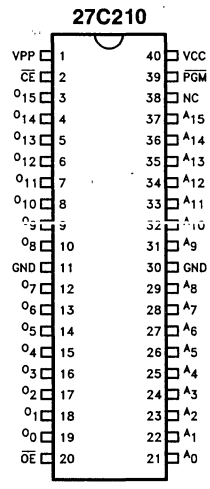
Figure 1. Block Diagram

September 1990
Order Number: 290193-003

Pin Names

A_0–A_{17}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

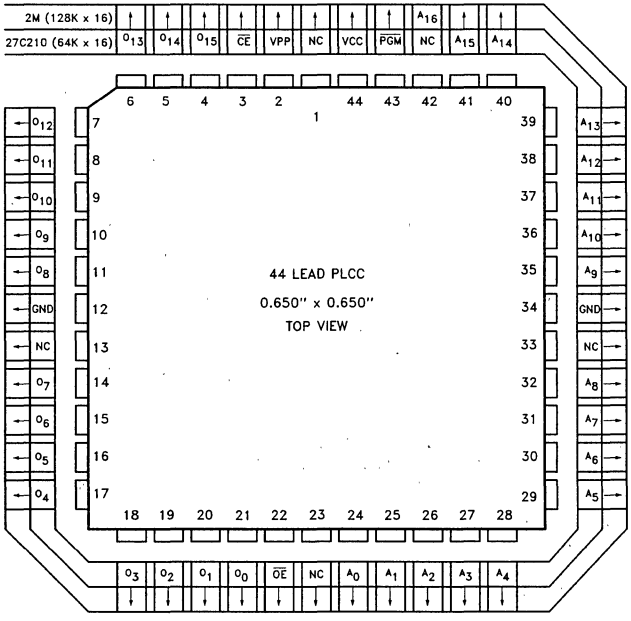
4M	2M
V_{PP}	V_{PP}
$\overline{CE}$	$\overline{CE}$
O_{15}	O_{15}
O_{14}	O_{14}
O_{13}	O_{13}
O_{12}	O_{12}
O_{11}	O_{11}
O_{10}	O_{10}
O_9	O_9
O_8	O_8
GND	GND
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3
O_2	O_2
O_1	O_1
O_0	O_0
$\overline{OE}$	$\overline{OE}$



2M	4M
V_{CC}	V_{CC}
$\overline{PGM}$	A_{17}
A_{16}	A_{16}
A_{15}	A_{15}
A_{14}	A_{14}
A_{13}	A_{13}
A_{12}	A_{12}
A_{11}	A_{11}
A_{10}	A_{10}
A_9	A_9
GND	GND
A_8	A_8
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0

290193-2

Figure 2. DIP Pin Configuration



290193-3

Figure 3. PLCC Lead Configuration

5

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)
Temperature Under Bias ..... −10°C to 80°C
Storage Temperature ..... −65°C to 125°C
Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.5V(2, 8)
Voltage on A_9 with Respect to GND ..... −0.6V to 13.0V(2)
V_{PP} Program Voltage with Respect to GND ..... −0.6V to 14V(2)
V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Notice: Specifications contained within the following tables are subject to change.

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			50	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0 to O_{15} unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.
8. Absolute Maximum ratings apply to NC pins.

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ±10%

Versions[4]		V_{CC} ±10%	27C210-120V10		27C210-150V10 P27C210-150V10 N27C210-150V10		27C210-200V10 P27C210-200V10 N27C210-200V10		Unit
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay			120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		55		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		30		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change—Whichever is First	3	0		0		0		ns

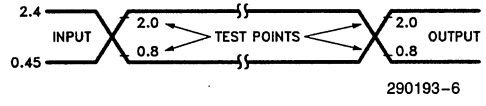
NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model Number Prefixes: no prefix = CERDIP, P = PDIP, N = PLCC.
5. Typical limits are set for T_A = 25°C and nominal supply voltages.

CAPACITANCE[3] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[5]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

5

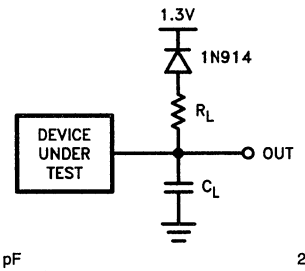
AC INPUT/OUTPUT REFERENCE WAVEFORM



290193-6

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input Rise and Fall times (10% to 90%) ≤ 10 ns.

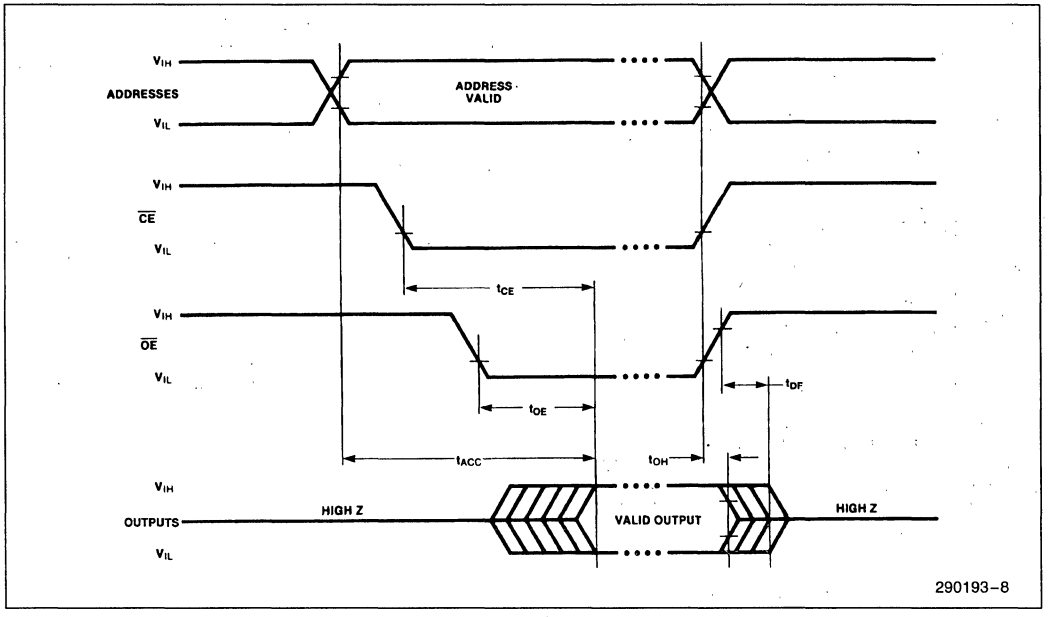
AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 kΩ

290193-7

AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C210 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	X	X	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	V_{CC}	V_{CC}	0089 H
	Device		V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	V_{CC}	V_{CC}	11EEH

NOTES:
1. X can be V_{IL} or V_{IH}
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{15} = V_{IL}

Read Mode

The 27C210 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying a 16-bit word to the output pins. Pulsing $\overline{PGM}$ low while $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with it's proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{15} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrades to 2 Mbit and 4 Mbit densities are easily accomplished due to the standardized pin configuration of the 27C210. When the 27C210 is in Read Mode, the $\overline{PGM}$ input becomes non-functional. The $\overline{PGM}$ and NC pins may be V_{IL} and V_{IH}. This allows address lines A_{16}–A_{17} to be routed directly to these inputs in anticipation of future density upgrades. Systems designed for 1 Mbit program memories today can be upgraded to higher densities (2 Mbit and 4 Mbit) in the future with no circuit board changes.

5

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity $\times$ exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

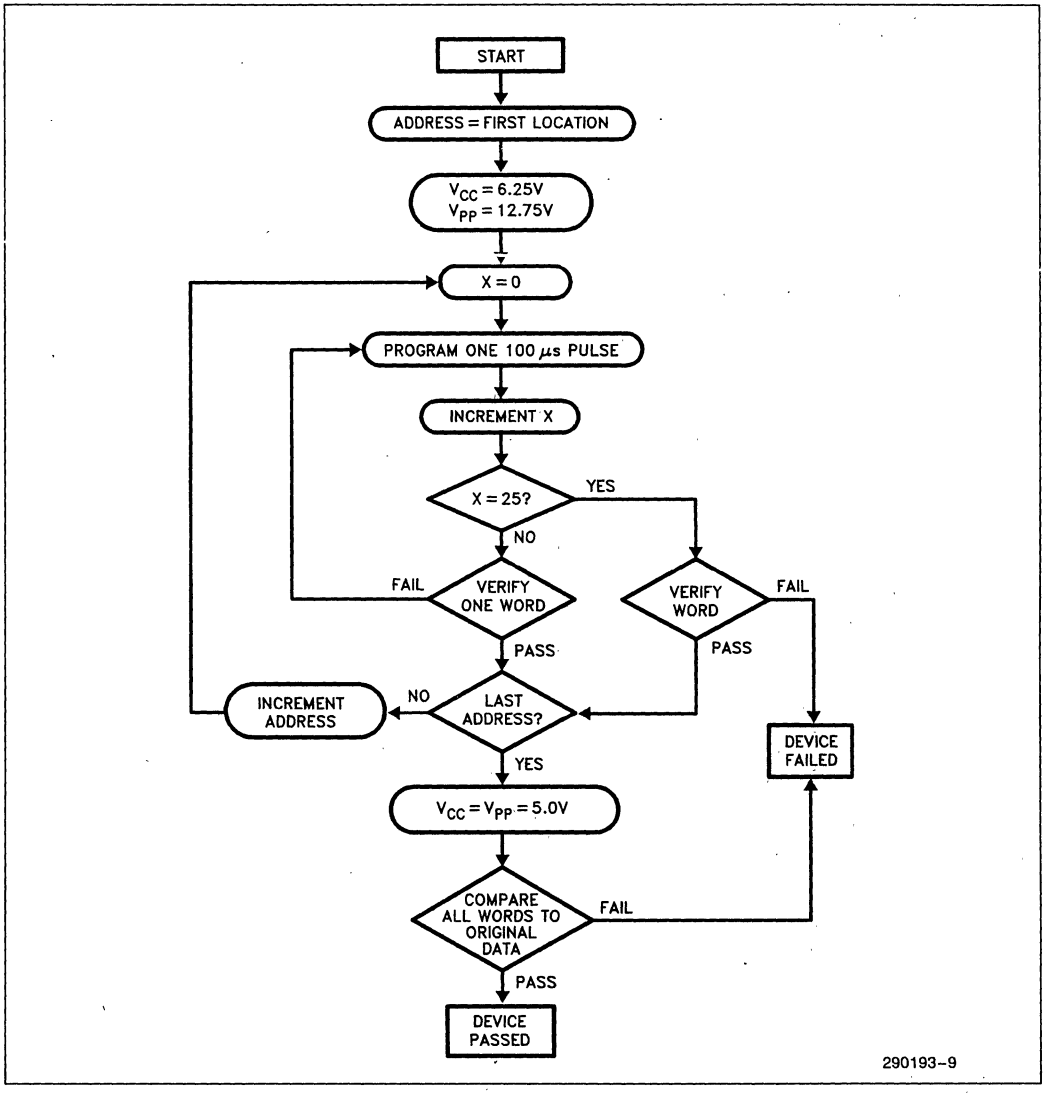


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C210. Developed to substantially reduce programming throughput, this algorithm can program the 27C210 as fast as 8 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse Programming algorithm employs a 100 μs pulse followed by a word verification to determine when the addressed word has been successfully programmed. The algorithm terminates if 25 attempts fail to program a word.

The entire program pulse/word verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all words are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

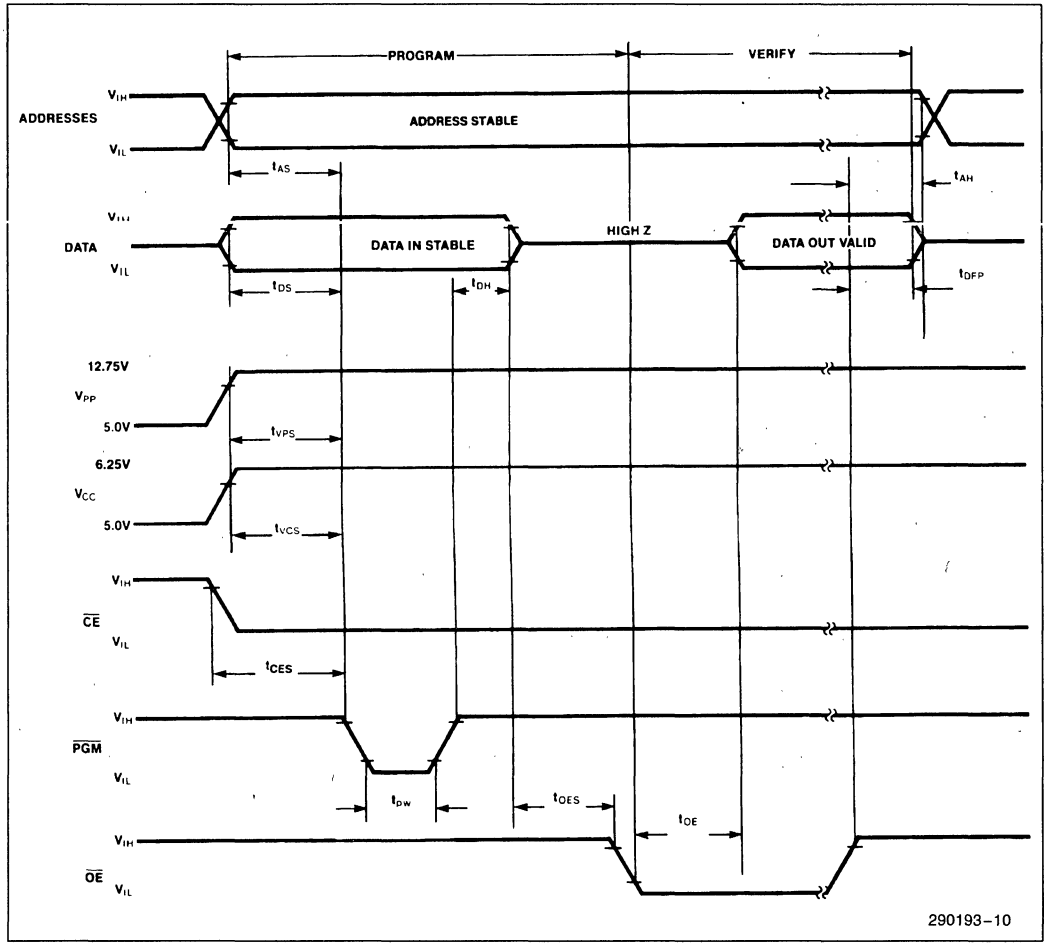
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 intelligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_{15} unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
03	Revised general datasheet structure, text to improve clarity Revised speed bin as follows: t_{ACC} was **130 ns**, is now **120 ns** t_{CE} was **130 ns**, is now **120 ns** t_{OE} was **60 ns**, is now **55 ns** Added PDIP package Revised I_{SB} Text Condition from $\overline{CE} = V_{CC}$ to $\overline{CE} = V_{CC} \pm 0.2V$ Revised V_{OL} from **0.4V** to **0.45V** Revised V_{OH} from $V_{CC} - 0.8V$ to **2.4V** Deleted 8 meg DIP, 4 and 8 Meg PLCC references Deleted EXPRESS page

27C220
2M (128K x 16) CHMOS EPROM

- **JEDEC Approved EPROM Pinouts**
  - **— 40-Pin DIP**
  - **— 44-Pin PLCC**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **High-Performance**
  - **— 150 ns ±10% V_{CC}**
  - **— 50 mA I_{CC} Active**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Times As Fast As 15 Seconds**
- **Surface Mount Packaging Available**
- **Complete Upgrade to Higher Densities**

Intel's 27C220 is a 5V only, 2,097,152-bit Erasable Programmable Read Only Memory. Organized as 131,072 words of 16 bits each. It is pin compatible with Intel's 1 Mbit 27C210 and provides for a simple upgrade to 4 Mbits in the future.

The 27C220 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 150 ns speed (t_{ACC}) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

Intel offers two DIP profile options to meet your prototyping and production needs. The windowed ceramic dip (CERDIP) package provides erasability and reprogrammability for prototyping and early production. Once the design is in full production, the plastic dip (PDIP) one-time programmable part provides a lower cost alternative that is well adapted for auto insertion.

In addition to the JEDEC 40-pin DIP package, Intel also offers a 44-lead PLCC version of the 27C220. This one-time-programmable surface mount device is ideal where board space consumption is a major concern or where surface mount manufacturing technology is being implemented across an entire production line.

The 27C220 is equally at home in both a TTL or CMOS environment. And like Intel's other high density EPROMs, the 27C220 programs quickly using Intel's industry leading Quick-Pulse Programming algorithm.

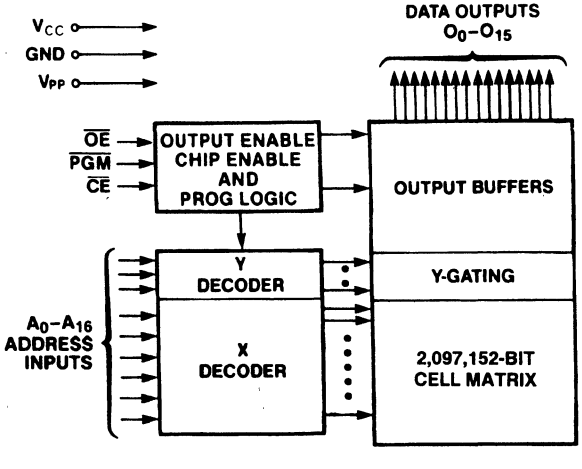
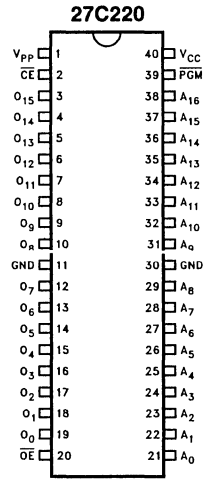


Figure 1. Block Diagram

October 1990
Order Number: 290217-005

4M	1M
V_{PP}	V_{PP}
$\overline{CE}$	$\overline{CE}$
O_{15}	O_{15}
O_{14}	O_{14}
O_{13}	O_{13}
O_{12}	O_{12}
O_{11}	O_{11}
O_{10}	O_{10}
O_9	O_9
O_8	O_8
GND	GND
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3
O_2	O_2
O_1	O_1
O_0	O_0
$\overline{OE}$	$\overline{OE}$



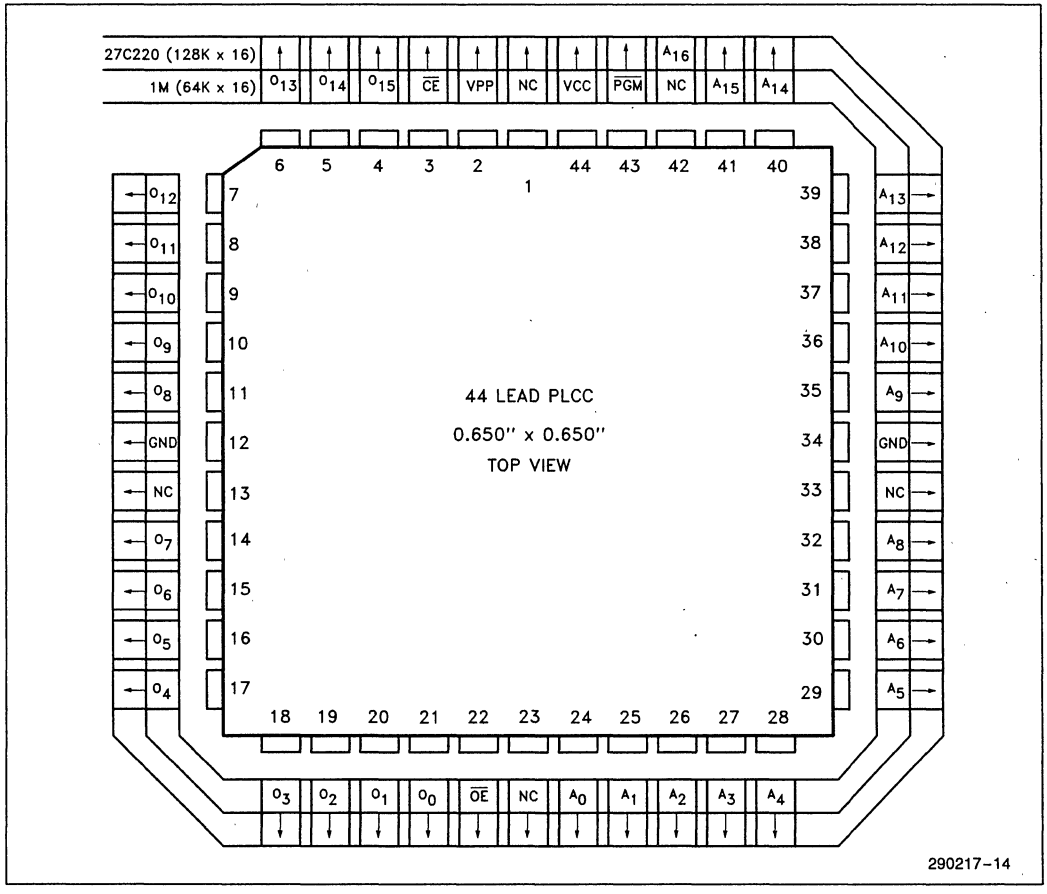
1M	4M
V_{CC}	V_{CC}
$\overline{PGM}$	A_{17}
NC	A_{16}
A_{15}	A_{15}
A_{14}	A_{14}
A_{13}	A_{13}
A_{12}	A_{12}
A_{11}	A_{11}
A_{10}	A_{10}
A_9	A_9
GND	GND
A_8	A_8
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0

290217-2

Figure 2. DIP Pin Configurations

Pin Names

A_0-A_{18}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT



290217-14

Figure 3. PLCC Lead Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature Under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltages on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND ..... −0.6V to 6.5V(2)

Voltage on A_9 with Respect to GND ..... −0.6V to 13.0V(2)

V_{PP} Supply Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7.0V(2)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	$V_{OUT} = 0V$ to V_{CC}
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE} = V_{IH}$
					100	µA	$\overline{CE} = V_{CC} \pm 0.2V$
I_{CC}	V_{CC} Operating Current	3			50	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA
I_{PP}	V_{PP} Operating Current	3			10	µA	$V_{PP} = V_{CC}$
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -400$ µA
V_{PP}	V_{PP} Operating Voltage	5	$V_{CC} - 0.7$		V_{CC}	V	

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum $I_{PP} + I_{CC}$. Maximum current is with outputs O_0 to O_{15} unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ±10%

Versions[4]		V_{CC} ±10%	27C220-150V10		27C220-200V10 P27C220-200V10 N27C220-200V10		Units
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay			150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

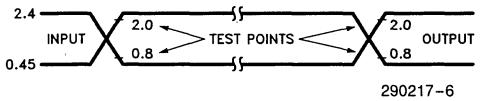
NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model Number Prefixes: No Prefix = CERDIP, P = PDIP, N = PLCC.
5. Typical limits are for T_A = 25°C and nominal supply voltages.

CAPACITANCE[3] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[5]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

5

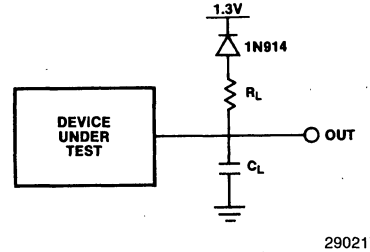
AC INPUT/OUTPUT REFERENCE WAVEFORM



290217-6

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤ 10 ns.

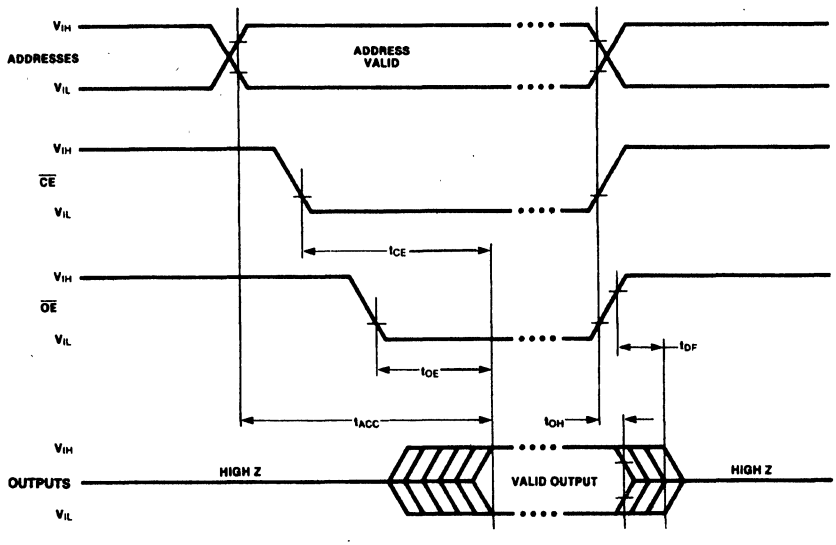
AC TESTING LOAD CIRCUIT



290217-7

C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 kΩ

AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C220 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X(1)	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	X	X	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	V_{CC}	V_{CC}	0089 H
	Device		V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	V_{CC}	V_{CC}	22EEH

NOTES:
1. X can be V_{IL} or V_{IH}
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{16} = V_{IL}

Read Mode

The 27C220 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE} = V_{IH}$, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying a 16-bit word to the output pins. Pulsing $\overline{PGM}$ low while $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$, parallel EPROMs may have common inputs.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{16} at V_{IL}, $A_0 = V_{IL}$ will present the manufacturer code and $A_0 = V_{IH}$ the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to the 4-Mbit density is easily accomplished due to the standardized pin configuration of the 27C220. When the 27C220 is in Read Mode, the $\overline{PGM}$ input becomes non-functional. This allows address line A_{17} to be routed directly to this input in anticipation of future density upgrades. Systems designed for 2-Mbit program memories today can be upgraded to 4-Mbit in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issures: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

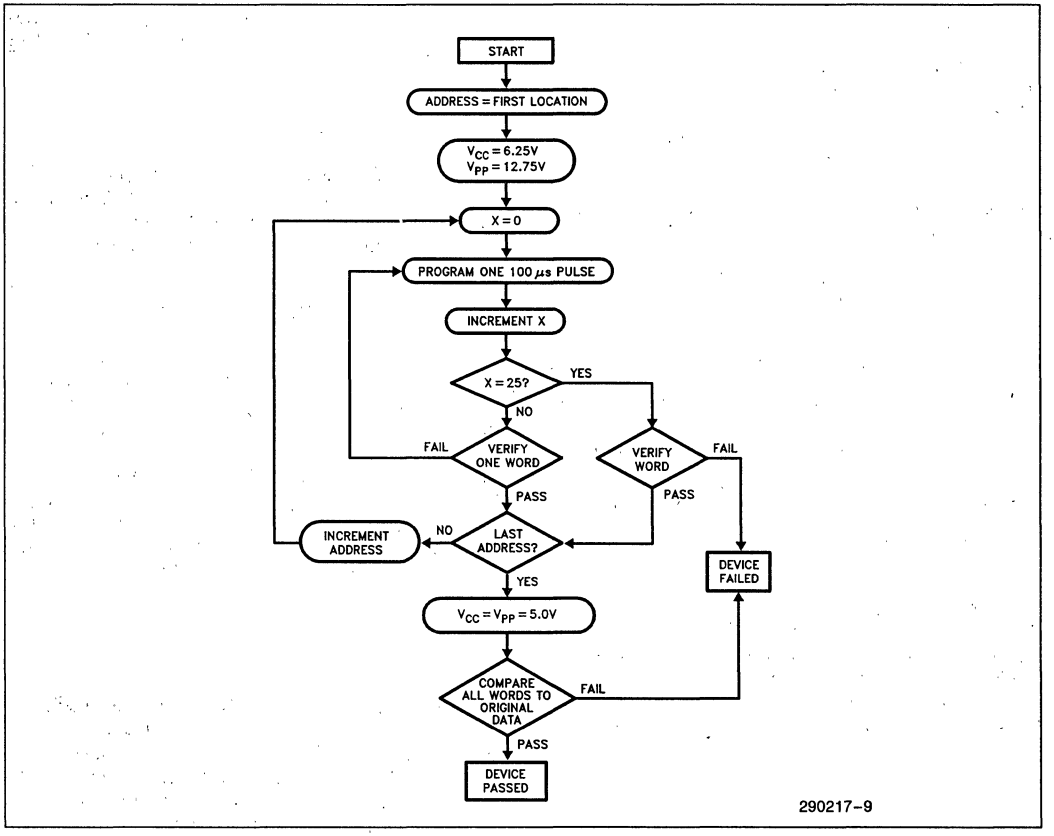


Figure 4. Quick-Pulse Programming™ Algorithm

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 µW/cm^2).

Quick-Pulse Programming™ Algorithm

The Quick-Pulse programming algorithm programs Intel's 27C220. Developed to substantially reduce programming throughput, this algorithm can program the 27C220 as fast as 15 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse programming algorithm employs a 100 µs pulse followed by a word verification to determine when the addressed word has been successfully programmed. The algorithm terminates if 25 attempts fail to program a word.

The entire program pulse/word verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all words are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

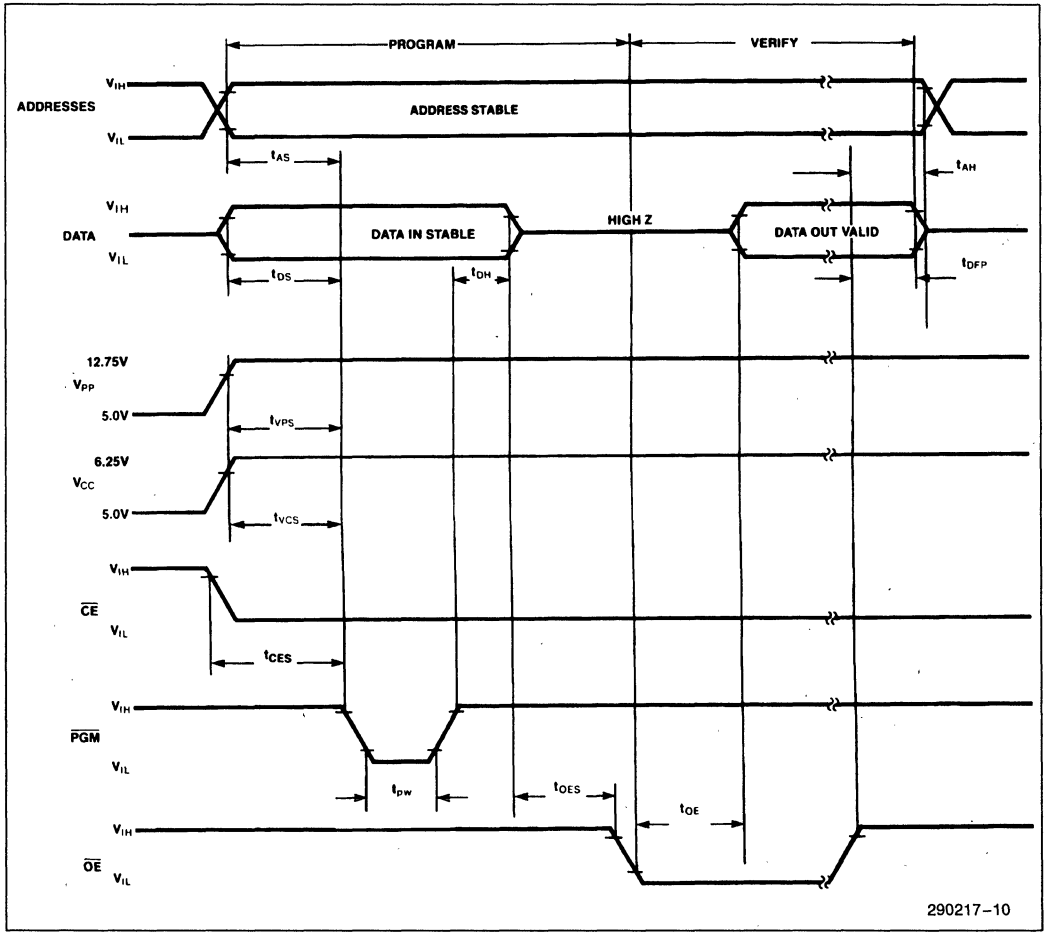
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A9 intelligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_{15} unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
005	Deleted -150 PDIP, PLCC packages

27C240
4M (256K x 16) CHMOS EPROM

- **JEDEC Approved EPROM Pinout**
  - **40-Pin DIP**
- **Versatile EPROM Features**
  - **CMOS and TTL Compatibility**
  - **Two Line Control**
- **High-Performance**
  - **170 ns ±10% V_{CC}**
  - **50 mA I_{CC} Active**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm**
  - **Programming Times as Fast as 30 Seconds**

Intel's 27C240 is a 5V only, 4,194,304-bit Erasable Programmable Read Only Memory, organized as 262,144 words of 16 bits each. It provides for a simple upgrade from 1 and 2 Mbits.

The 27C240 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 170 ns speed (t_{ACC}) optimizes operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

The 27C240 is equally at home in both a TTL or CMOS environment. And like Intel's other high density EPROMs, the 27C240 programs quickly using Intel's industry leading Quick-Pulse Programming™ algorithm.

CHMOS is a patented process of Intel Corporation.

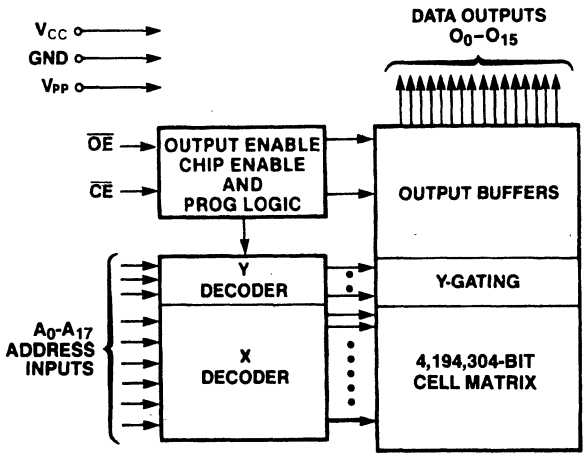


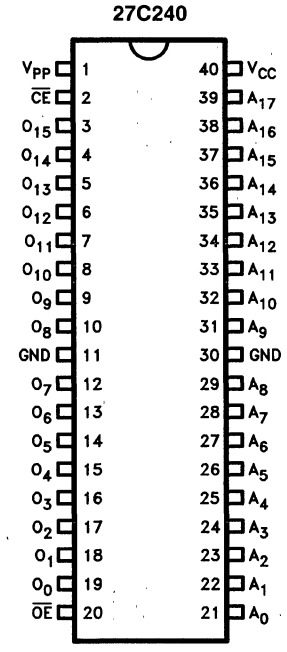
Figure 1. Block Diagram

October 1990
Order Number: 290229-004

Pin Names

A_0–A_{17}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO INTERNAL CONNECT

2M	1M
V_{PP}	V_{PP}
$\overline{CE}$	$\overline{CE}$
O_{15}	O_{15}
O_{14}	O_{14}
O_{13}	O_{13}
O_{12}	O_{12}
O_{11}	O_{11}
O_{10}	O_{10}
O_9	O_9
O_8	O_8
GND	GND
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3
O_2	O_2
O_1	O_1
O_0	O_0
$\overline{OE}$	$\overline{OE}$



290229-2

1M	2M
V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$
NC	A_{16}
A_{15}	A_{15}
A_{14}	A_{14}
A_{13}	A_{13}
A_{12}	A_{12}
A_{11}	A_{11}
A_{10}	A_{10}
A_9	A_9
GND	GND
A_8	A_8
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0

Figure 2. DIP Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C(1)

Temperature Under Bias . . . . . −10°C to 80°C

Storage Temperature . . . . . −65°C to 125°C

Voltage on Any Pin (except A_9, V_{CC} and V_{PP}) with Respect to GND . . . . . −0.6V to 6.5V(2)

Voltage on A_9 with Respect to GND . . . . . −0.6V to 13.0V(2)

V_{PP} Supply Voltage with Respect to GND . . . . . −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND . . . . . −0.6V to 7.0V(2)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Standby Current				1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ±0.2V
I_{CC}	V_{CC} Operating Current	3			50	mA	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA
V_{PP}	V_{PP} Operating Voltage	5	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current is with outputs O_0 to O_{15} unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. V_{PP} may be connected directly to V_{CC}, or may be one diode voltage drop below V_{CC}. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ±10%

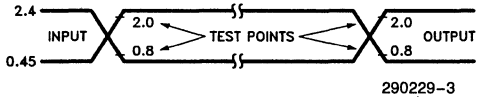
Versions[4]		V_{CC} ±10%	27C240-170V10		27C240-200V10		Units
Symbol	Parameter	Notes	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		65		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		55		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	3	0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model number prefixes: No Prefix = Ceramic Dip.
5. Typical limits are for T_A = 25°C and nominal supply voltages.

CAPACITANCE[3] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[5]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

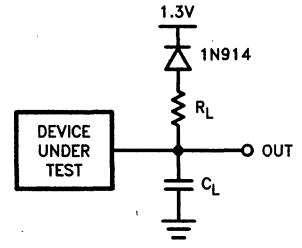
AC INPUT/OUTPUT REFERENCE WAVEFORM



290229-3

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤10 ns.

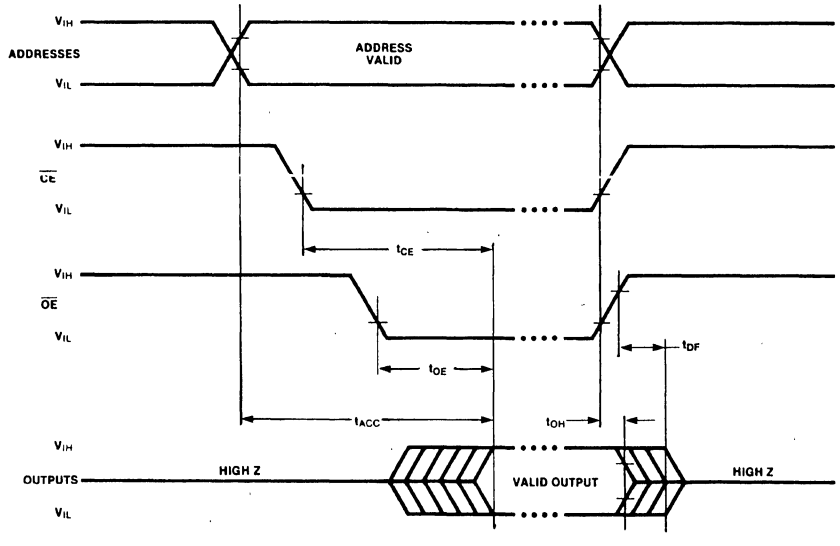
AC TESTING LOAD CIRCUIT



290229-4

C_L = 100 pF
C_L includes Jig Capacitance
R_L = 3.3 KΩ

AC WAVEFORMS



DEVICE OPERATION

The Mode Selection table lists 27C240 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and V_{PP}, and A_9 during int$_e$ligent Identifier™ Mode, are TTL or CMOS.

5

Table 1. Mode Selection

Mode		Notes	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		1	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable			V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby			V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program		2	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CP}	D_{IN}
Program Verify			V_{IH}	V_{IL}	X	X	V_{PP}	V_{CP}	D_{OUT}
Program Inhibit			V_{IH}	V_{IH}	X	X	V_{PP}	V_{CP}	High Z
int$_e$ligent Identifier	Manufacturer	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	V_{CC}	V_{CC}	0089 H
	Device		V_{IL}	V_{IL}	V_{ID}	V_{IH}	V_{CC}	V_{CC}	44EEH

NOTES:
1. X can be V_{IL} or V_{IH}
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{17} = V_{IL}

Read Mode

The 27C240 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the outputs are in a high impedance state, independent of $\overline{OE}$.

Program Mode

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when V_{PP} is raised to 12.75V. Data is introduced by applying a 16-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE}$ = V_{IH} programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IH}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with it's proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1–A_8, and A_{10}–A_{17} at V_{IL}, A_0 = V_{IL} will present the manufacturer code and A_0 = V_{IH} the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes

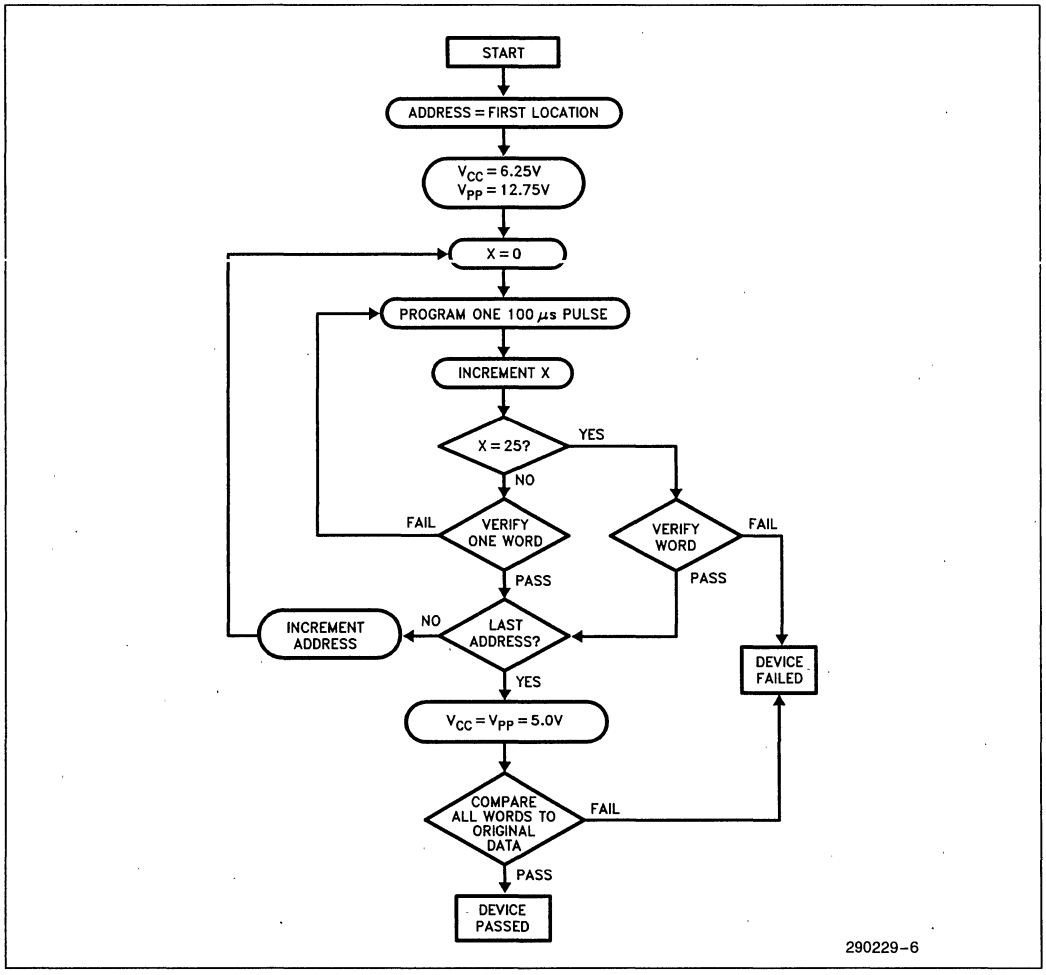


Figure 3. Quick-Pulse Programming Algorithm

approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 µW/cm^2).

Quick-Pulse Programming Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C240. Developed to substantially reduce programming throughput, this algorithm can program the 27C240 as fast as 30 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse Programming algorithm employs a 100 µs pulse followed by a word verification to determine when the addressed word has been successfully programmed. The algorithm terminates if 25 attempts fail to program a word.

The entire program pulse/word verify sequence is performed with V_{PP} = 12.75V and V_{CC} = 6.25V. When programming is complete, all words are compared to the original data with V_{CC} = V_{PP} = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

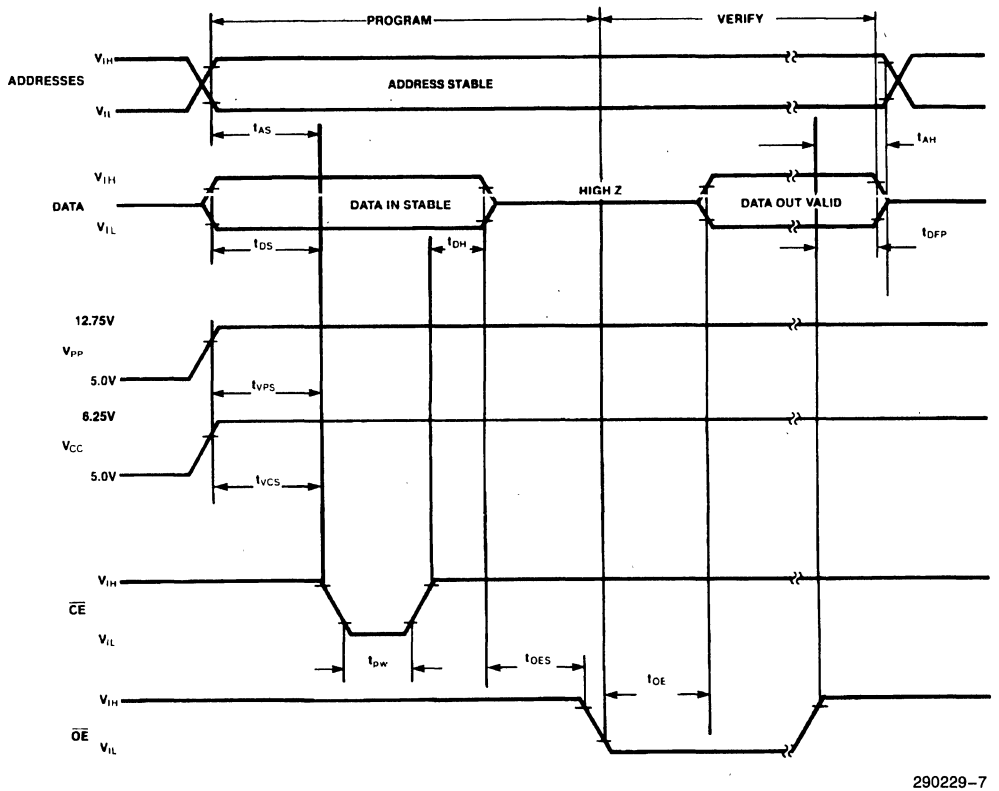
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CC} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 intelligent Identifier Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CC}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_{15} unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics, but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



REVISION HISTORY

Number	Description
04	Deleted -150 speed bin

27C400
4M (256K x 16 or 512K x 8) CHMOS EPROM

- **Word-Wide or Byte-Wide Configurable**
- **4M 40-Pin Mask ROM Compatible**
  - **40-Pin CERDIP Package**
- **Low Power Dissipation**
  - **50 mA Max Active @ 5 MHz**
  - **100 μA Max Standby**
- **High Performance**
  - **150 ns Maximum Access Time**
  - **V_{CC} = 5V $\pm$10%**
- **Quick-Pulse Programming™ Algorithm**
  - **Programming as Fast as 28 Seconds**
- **UV Erasable**

Intel's 27C400 is a 5V-only, 4,194,304 bit, Erasable Programmable Read Only Memory. It employs advanced CHMOS* III-E circuitry for systems requiring low power, high speed performance and noise immunity.

The device is organized as 262,144 words of 16 bits or 524,288 bytes of 8 bits through use of a byte enable switch on pin 31. The 27C400 is pinout and functionally compatible with 40-pin 4M Mask ROMs, providing a solution for both prototyping and production applications.

The 27C400 is offered in a ceramic DIP package. The UV-erasable CERDIP package facilitates fast time-to-market in minimum quantities with migration to mask ROMs for volume production. The Quick-Pulse Programming algorithm provides fast, reliable programming.

*CHMOS is a patented process of Intel Corporation.

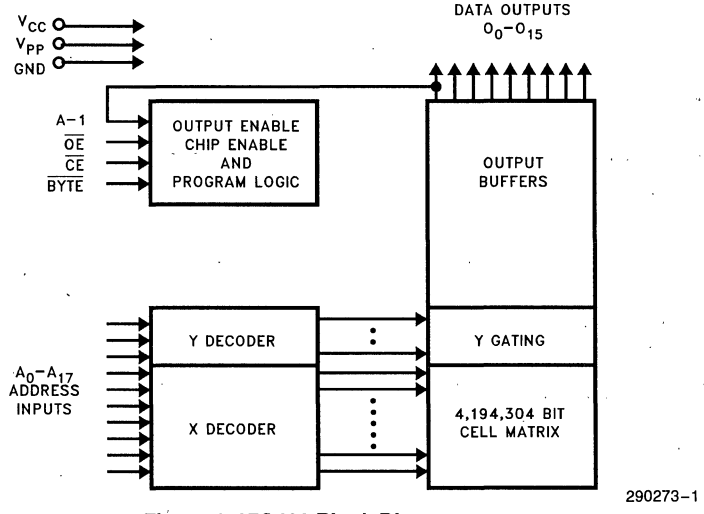


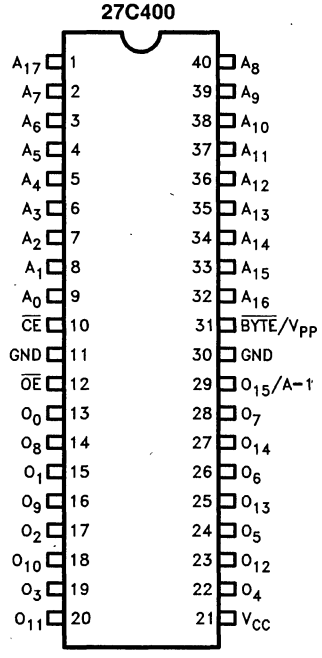
Figure 1. 27C400 Block Diagram

November 1990
Order Number: 290273-002

Pin Names

A_0–A_{18}	ADDRESSES
O_0–O_{15}	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
$\overline{BYTE}$	WORD/BYTE ENABLE
A-1	BYTE SELECT
NC	NO CONNECT

8 Mb	4 Mb Mask ROM
A_{18}	
A_{17}	A_{17}
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0
$\overline{CE}$	$\overline{CE}$
GND	GND
$\overline{OE}$	$\overline{OE}$
O_0	O_0
O_8	O_8
O_1	O_1
O_9	O_9
O_2	O_2
O_{10}	O_{10}
O_3	O_3
O_{11}	O_{11}



290273-2

4 Mb Mask ROM	8 Mb
	NC
A_8	A_8
A_9	A_9
A_{10}	A_{10}
A_{11}	A_{11}
A_{12}	A_{12}
A_{13}	A_{13}
A_{14}	A_{14}
A_{15}	A_{15}
A_{16}	A_{16}
$\overline{BYTE}$	$\overline{BYTE}/V_{PP}$
GND	GND
O_{15}/A-1	O_{15}/A-1
O_7	O_7
O_{14}	O_{14}
O_6	O_6
O_{13}	O_{13}
O_5	O_5
O_{12}	O_{12}
O_4	O_4
V_{CC}	V_{CC}

Figure 2. DIP Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C(1)

Temperature under Bias ..... −10°C to 80°C

Storage Temperature ..... −65°C to 125°C

Voltage on Any Pin (Except A_9, V_{CC} and $\overline{BYTE}/V_{PP}$) with Respect to GND ..... −0.6V to 6.5V(2)

Voltage on A_9, with Respect to GND ..... −0.6V to 13V(2)

$\overline{BYTE}/V_{PP}$ Program Voltage with Respect to GND ..... −0.6V to 14V(2)

V_{CC} Supply Voltage with Respect to GND ..... −0.6V to 7V(2)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION DC CHARACTERISTICS(1) V_{CC} = 5.0V ±10%

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Load Current	7		0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current				±10	µA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Standby Current	5			1.0	mA	$\overline{CE}$ = V_{IH}
					100	µA	$\overline{CE}$ = V_{CC} ± 0.2V
I_{CC}	V_{CC} Operating Current	3			50	mA	f = 5 MHz, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA
I_{PP}	V_{PP} Operating Current	3			10	µA	V_{PP} = V_{CC}
I_{OS}	Output Short Circuit Current	4, 6			100	mA	
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −400 µA

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum active power usage is the sum I_{PP} + I_{CC}. Maximum current value is with outputs O_0–O_{15} unloaded.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. $\overline{BYTE}/V_{PP}$ = V_{CC} ± 0.2V or GND ± 0.2V.
6. Sampled, not 100% tested.
7. Typical limits are at V_{CC} = 5V, T_A = 25°C.

READ OPERATION AC CHARACTERISTICS[1] V_{CC} = 5.0V ±10%

Version[4]	V_{CC} ± 10%		27C400-150V10[7]		27C400-200V10		Unit
Symbol	Parameter	Notes	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2		60		70	ns
t_{DF}	$\overline{OE}$ High to Output High Z	3		50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change— Whichever Occurs First	3	0		0		ns

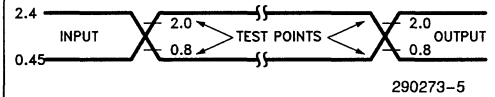
NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. Model Number Prefixes: No Prefix = CERDIP.
5. Typical values are for T_A = +25°C and nominal supply voltages.
6. Includes O_{15}/A-1.
7. Both byte- and word-wide-read mode are available with the 27C400-200V10. 27C400-150V10 specs are valid only in word-wide-read mode operation.

CAPACITANCE[3] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ[5]	Max	Unit	Condition
C_{IN}	Input Capacitance	4	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance[6]	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

5

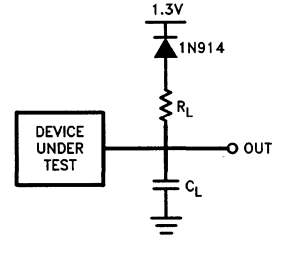
AC INPUT/OUTPUT REFERENCE WAVEFORM



290273-5

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) ≤ 10 ns.

AC TESTING LOAD CIRCUIT

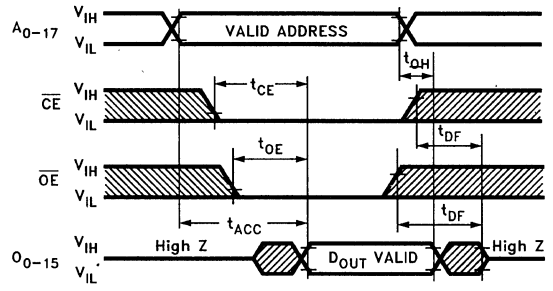


290273-6

C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 kΩ

AC WAVEFORMS

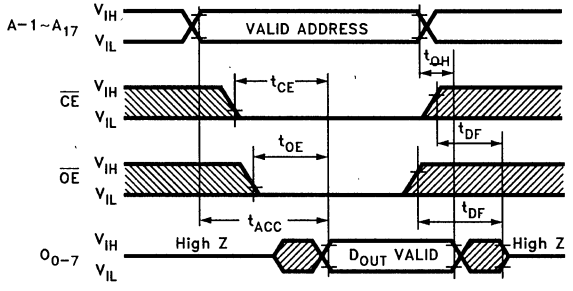
Word-Wide Read Mode



290273-7

NOTE:
$\overline{BYTE}/V_{PP} = V_{CC} \pm 0.2V$

Byte-Wide Read Mode



290273-8

NOTE:
$\overline{BYTE}/V_{PP} = GND \pm 0.2V$

DEVICE OPERATION

The Mode Selection table lists 27C400 operating modes. Read Mode requires a single 5V power supply. All inputs, except V_{CC} and $\overline{BYTE}/V_{PP}$, and A_9 during int$_e$ligent Identifier™ Mode, are TTL or CMOS.

Table 1. Mode Selection

Mode	Notes	$\overline{CE}$	$\overline{OE}$	A_9	A_0	O_{15}/A-1	$\overline{BYTE}/V_{PP}$(4)	V_{CC}	O_{8-14}	O_{0-7}
Read (Word)	1	V_{IL}	V_{IL}	X	X	D_{15} Out	V_{CC}	V_{CC}	D_{8-14} Out	D_{0-7} Out
Read (Upper Byte)		V_{IL}	V_{IL}	X	X	V_{IH}	GND	V_{CC}	High Z	D_{8-15} Out
Read (Lower Byte)		V_{IL}	V_{IL}	X	X	V_{IL}	GND	V_{CC}	High Z	D_{0-7} Out
Output Disable		V_{IL}	V_{IH}	X	X	High Z	X	V_{CC}	High Z	High Z
Standby		V_{IH}	X	X	X	High Z	X	V_{CC}	High Z	High Z
Program	2	V_{IL}	V_{IH}	X	X	D_{15} In	V_{PP}	V_{CP}	D_{8-14} In	D_{0-7} In
Program Verify		V_{IH}	V_{IL}	X	X	D_{15} Out	V_{PP}	V_{CP}	D_{8-14} Out	D_{0-7} Out
Program Inhibit		V_{IH}	V_{IH}	X	X	High Z	V_{PP}	V_{CP}	High Z	High Z
int$_e$ligent Identifier	2, 3	V_{IL}	V_{IL}	V_{ID}	V_{IL}	0B	V_{CC}	V_{CC}	OOH	89H
—Manufacturer		V_{IL}	V_{IL}	V_{ID}	V_{IH}	0B	V_{CC}	V_{CC}	44H	EFH
—Device										

NOTES:
1. X can be V_{IL} or V_{IH}.
2. See DC Programming Characteristics for V_{CP}, V_{PP} and V_{ID} voltages.
3. A_1–A_8, A_{10}–A_{17} = V_{IL}.
4. $\overline{BYTE}/V_{PP}$ is intended for operation under DC Voltage conditions only.

Read Mode

The 27C400 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after $\overline{OE}$'s falling edge, assuming t_{ACC} and t_{CE} times are met.

Word-Wide Mode

With $\overline{BYTE}/V_{PP}$ at V_{CC} ± 0.2V outputs O_{0-7} present data D_{0-7} and outputs O_{8-15} present data D_{8-15}, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

Byte-Wide Mode

With $\overline{BYTE}/V_{PP}$ at GND ± 0.2V, outputs O_{8-15} are tri-stated. If O_{15}/A-1 = V_{IH}, outputs O_{0-7} present data bits D_{8-15}. If O_{15}/A-1 = V_{IL}, outputs O_{0-7} present data bits D_{0-7}.

Read Operation AC Characteristic specifications are currently valid in byte-wide mode only when using the 27C400–200V10. Please contact your local Intel sales office for additional information.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a. lowest possible memory power dissipation

b. complete assurance that data bus contention will not occur

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

Standby Mode

Standby Mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, outputs are in a high impedance state, independent of $\overline{OE}$.

5

Program Mode

Caution: Exceeding 14V on $\overline{BYTE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when $\overline{BYTE}/V_{PP}$ is raised to 12.75V. Data is introduced by applying a 16-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE} = V_{IH}$ programs that data into the device.

Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With V_{CC} at 6.25V, a substantial program margin is ensured. The verify is performed with $\overline{CE}$ at V_{IH}. Valid data is available on O_{0-15} t_{OE} after $\overline{OE}$ falls low.

Program Inhibit

Program Inhibit mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on A_9. With $\overline{CE}$, $\overline{OE}$, A_1-A_8, and $A_{10}-A_{17} = V_{IL}$, $A_0 = V_{IL}$ will present the manufacturer's code and $A_0 = V_{IH}$ the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

UPGRADE PATH

Future upgrade to the 8M-bit density is easily accomplished due to the standardized pin configuration of the 27C400. Simply design in the 27C400 using pins 2–41 of a 42-pin socket. Route address line A_{18} directly to pin 1 in anticipation of future density upgrades. See Figure 2 for additional information. Systems designed for 4M-bit program memories today can be upgraded to 8M-bit in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current issues—standby currents levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. It the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelengths 2537Å. The intergrated dose (UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. Erasure time is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2).

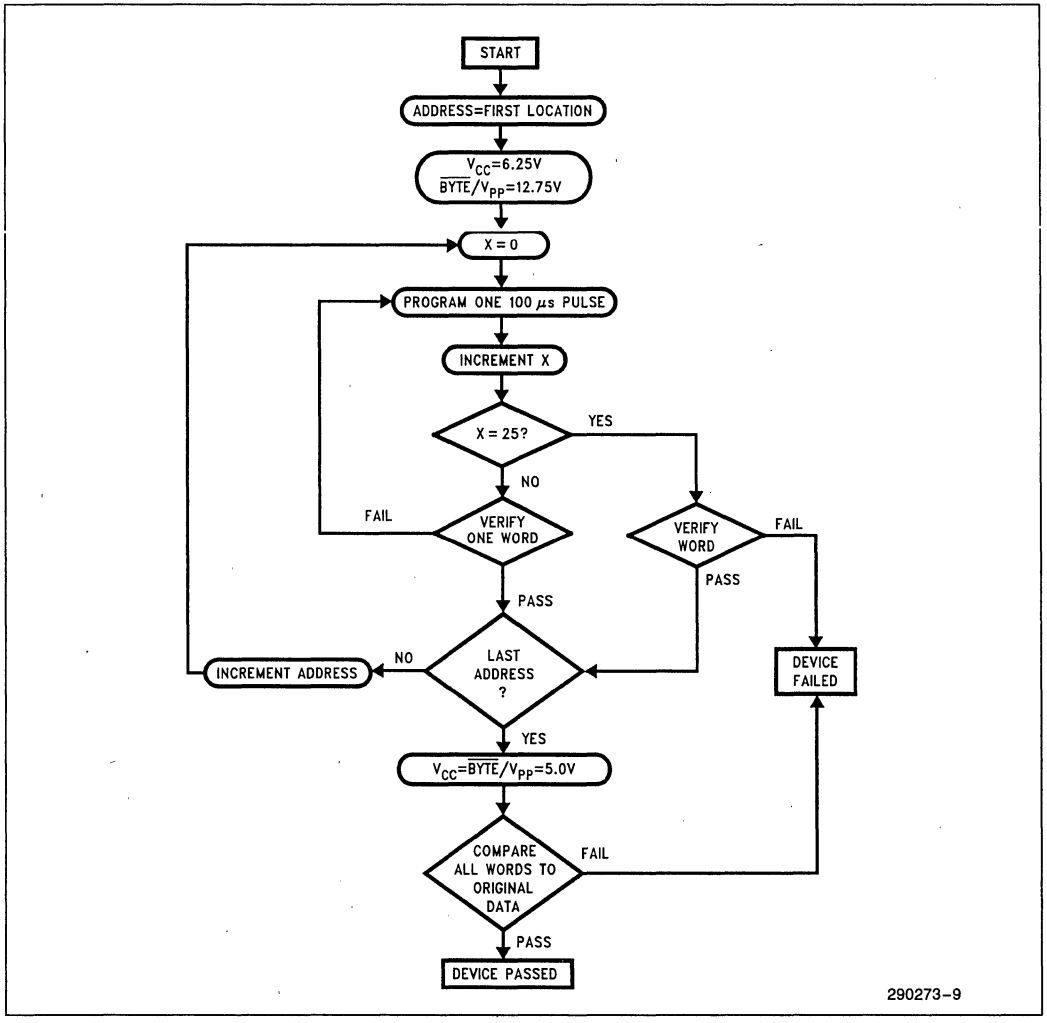


Figure 3. Quick-Pulse Programming Algorithm

Quick-Pulse Programming Algorithm

The Quick-Pulse Programming™ algorithm programs Intel's 27C400. Developed to substantially reduce programming throughput, this algorithm can program the 27C400 as fast as 28 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse Programming algorithm employs a 100 μs pulse followed by a word verification to determine when the addressed word has been successfully programmed. The algorithm terminates if 25 attempts fail to program a word.

The entire program-pulse/word-verify sequence is performed with $\overline{BYTE}/V_{PP}$ = 12.75V and V_{CC} = 6.25V. When programming is complete, all words are compared to the original data with V_{CC} = $\overline{BYTE}/V_{PP}$ = 5.0V.

DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

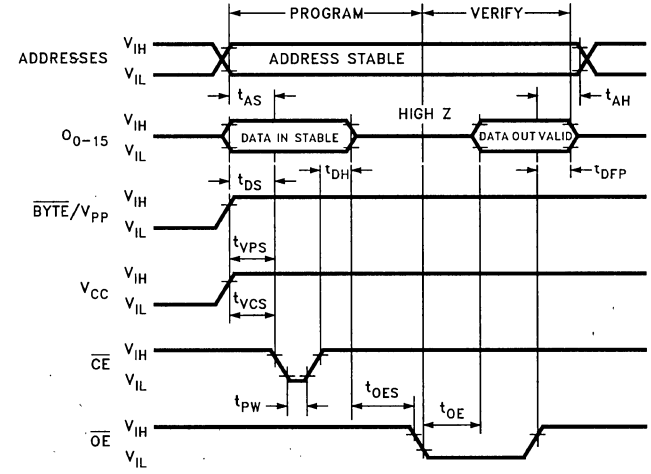
Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Conditions
I_{LI}	Input Load Current				1	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CP}	V_{CP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
I_{PP}	V_{PP} Program Current	1			50	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage		−0.1		0.8	V	
V_{IH}	Input High Voltage		2.4		6.5	V	
V_{OL}	Output Low Voltage (Verify)				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		3.5			V	$I_{OH} = -2.5$ mA
V_{ID}	A_9 intelligent Identifer Voltage		11.5	12.0	12.5	V	
V_{PP}	V_{PP} Program Voltage	2, 3	12.5	12.75	13.0	V	
V_{CP}	V_{CC} Supply Voltage (Program)	2	6.0	6.25	6.5	V	

AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{VCS}	V_{CP} Setup Time	2	2			μs
t_{VPS}	V_{PP} Setup Time	2	2			μs
t_{AS}	Address Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{PW}	$\overline{CE}$ Program Pulse Width		95	100	105	μs
t_{DH}	Data Hold Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{OE}	Data Valid from $\overline{OE}$	5			150	ns
t_{DFP}	$\overline{OE}$ High to Output High Z	5, 6	0		130	ns
t_{AH}	Address Hold Time		0			μs

NOTES:
1. Maximum current is with outputs O_0–O_{15} unloaded.
2. V_{CP} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming, a 0.1 μF capacitor is required between V_{PP} and GND to suppress spurious voltage transients, which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

PROGRAMMING WAVEFORMS



5

27960CX
PIPELINED BURST ACCESS 1M (128K x 8) CHMOS EPROM

- **Synchronous 4 Byte Data Burst Access**
- **No Glue Interface to 80960CA**
- **High Performance Clock to Data Out**
  - **— Zero Wait State Data to Data Burst**
  - **— Up to 33 MHz 80960CA Performance**
- **Asynch Microcontroller Reset Function**
  - **— Returns to Known State with High-Z Outputs**
- **Pipelined Addressing for Optimal Bus Bandwidth on 80960CA**
  - **— Next Addressing Overlaps Last Data Byte**
- **CHMOS III-E for High Performance and Low Power**
  - **— 125 mA Active, 30 mA Standby**
  - **— TTL Compatible Inputs**
- **1 Mbit Density Configures as 128K x 8**
  - **— Upgrade Path to 512K x 8**

Intel's 27960CX is a 5V only, 1,048,576 bit, Erasable Programmable Read Only Memory, organized as 128K words of 8 bits. It is a member of a new family of high performance EPROMs with synchronous burst access.

The 27960CX provides a no glue synchronous burst interface to the 80960CA bus. Internally the 27960CX is organized in 4 byte blocks, in which each byte is accessed sequentially. The internal state machine is factory configured to generate either 1 or 2 wait-states between the address and first data byte. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 33 MHz.

Pipelining capability allows addresses to overlap previous data, further optimizing bus bandwidth in 80960CA applications. An asynchronous microcontroller $\overline{\text{RESET}}$ feature puts the outputs in the high impedance state and takes the internal state machine to a known state where a new burst access can begin.

The 27960CX is available in either 44-lead Cerquad (reprogrammable) or PLCC packages. Cerquad allows for code changes in the R & D environment while PLCC provides optimum cost effectiveness during production. Two No Connects (NC) on the package allow for an upgrade to 4 Mbits (512K x 8).

The 27960CX is manufactured on Intel's 1 micron CHMOS III-E technology. The Quick-Pulse Programming™ algorithm provides fast, reliable programming with throughput under 17 seconds for optimized equipment.

*CHMOS is a Patentented Process of Intel Corporation.

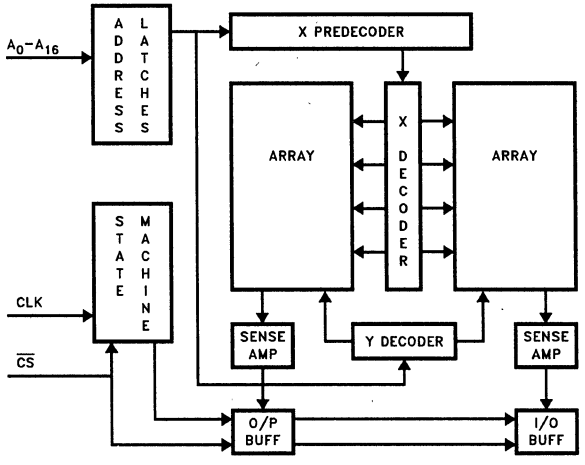


Figure 1. 27960CX Burst EPROM Block Diagram

January 1991
Order Number: 290236-004

27960CX BURST EPROM

EPROMs are established as the preferred code storage device in embedded applications. The non-volatile, flexible, reliable, cost effective EPROM makes a product easier to design, manufacture and service. Until recently, however, EPROMs could not match the performance needs of high-end systems. The 27960CX was designed to support the 80960CA embedded processor. It utilizes the burst interface to offer near zero wait-state performance without the high cost normally associated with this performance.

In embedded designs, board space and cost must be kept at a minimum without impacting performance and reliability. The 27960CX removes the need for expensive high-speed shadow RAM backed up by slow EPROM or ROM for non-volatile code storage. Code optimization concerns are reduced with "off-chip" code fetches no longer crippling to system performance. FONTs can be run directly out of these EPROMs at the same performance as high-speed DRAMs. With the 27960CX, the EPROM is the ideal code or FONT storage device for your 80960CA system.

Architecture

The 27960CX provides a no-glue, synchronous burst interface to the 80960CA's bus. It operates in pipelined or non-pipelined modes. Internally, the 27960CX is organized in 4 byte blocks which are accessed sequentially. A burst access begins on the first clock pulse after $\overline{ADS}$ and $\overline{CS}$ are asserted. The address of the 4 byte block is latched on the rising edge of clock following $\overline{ADS}$. After a preset number of wait-states (1 or 2), data is output one byte at a time on each subsequent clock cycle. A burst access is terminated on the rising edge of clock with $\overline{BLAST}$ asserted. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 33 MHz. Extra power and ground pins dedicated to the outputs reduce the effects of fast output switching on device performance.

The pipelining capability of the 27960CX allows the address to overlap the last data byte of the burst, further optimizing bus band width in 80960CA applications. In the pipelined mode, with a non-buffered interface, the 27960CX delivers 4 bytes of data in 6 clock cycles at 33 MHz. In a 32-bit configuration, this translates into a read bandwidth of 88 Mbytes/sec. Performance capability of the 27960CX in different 80960CA systems is given in Table I.

*CERQUAD is available in a socket only version.

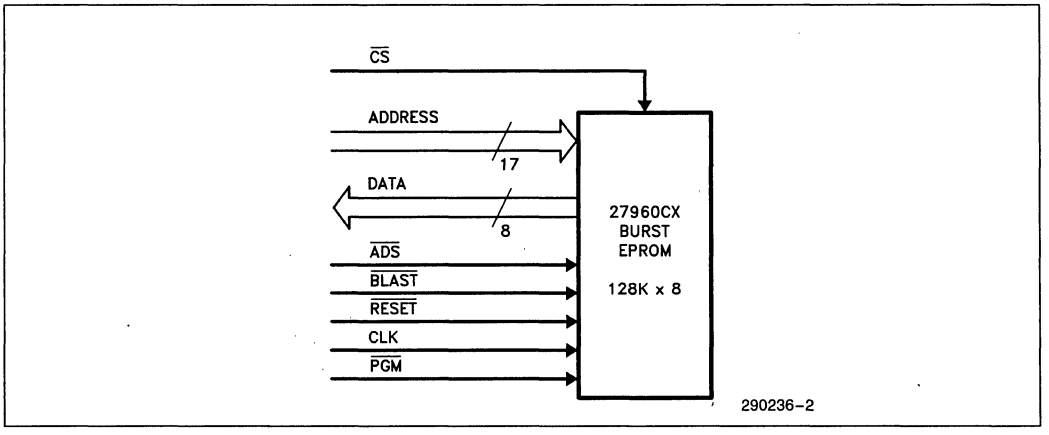


Figure 2. 27960CX Burst EPROM Signal Set

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Table 1. Performance Capability

33 MHz 2 WS Non-Buffered: 4 Words/6 Clock Cycles → 88 Mbytes/Sec

ADDR	A_{00}	WS	WS	—	—	—	A_{01}	WS	WS	—	—	—	A_{02}	WS
DATA	—	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	—	D_{10}	D_{11}	D_{12}	D_{13}	—
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_1

25 MHz 2 WS Buffered: 4 Words/6 Clock Cycles → 66 Mbytes/Sec

ADDR	A_{00}	WS	WS	—	—	—	A_{01}	WS	WS	—	—	—	A_{02}	WS
DATA	—	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	—	D_{10}	D_{11}	D_{12}	D_{13}	—
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_1

20 MHz 1 WS Buffered: 4 Words/5 Clock Cycles → 64 Mbytes/Sec

ADDR	A_{00}	WS	—	—	—	A_{01}	WS	—	—	—	A_{02}	WS	
DATA	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	D_{10}	D_{11}	D_{12}	D_{13}	—	
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_1	C_2	C_3	C_4	C_5	C_1	

16 MHz 1 WS Buffered: 4 Words/5 Clock Cycles → 51 Mbytes/Sec

ADDR	A_{00}	WS	—	—	—	A_{01}	WS	—	—	—	A_{02}	WS	
DATA	—	—	D_{00}	D_{01}	D_{02}	D_{03}	—	D_{10}	D_{11}	D_{12}	D_{13}	—	
PCLK	C_1	C_2	C_3	C_4	C_5	C_6	C_1	C_2	C_3	C_4	C_5	C_1	

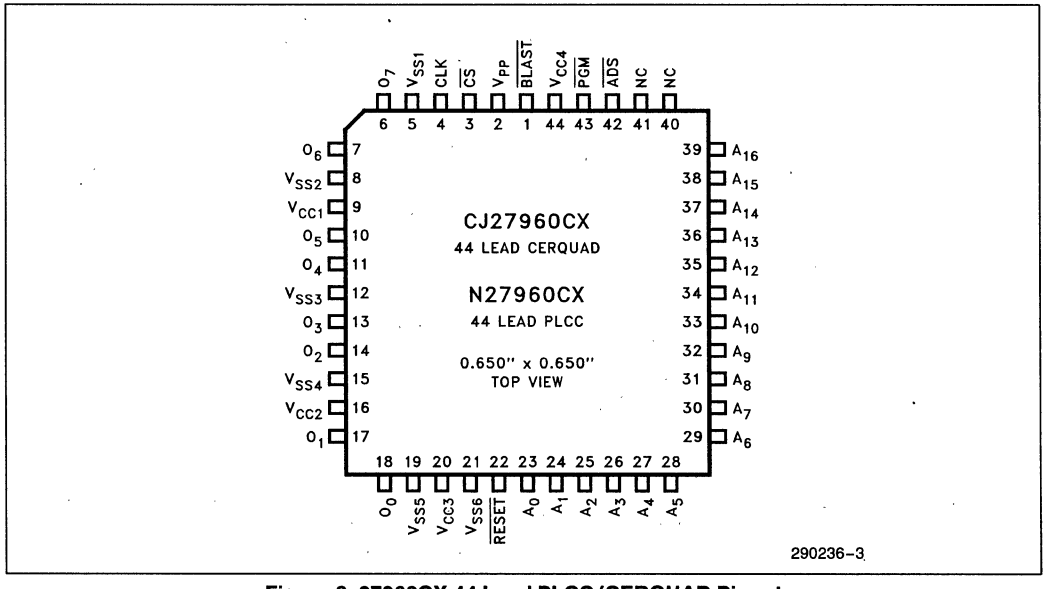

Figure 3. 27960CX 44 Lead PLCC/CERQUAD Pinout

PIN DESCRIPTIONS

Symbol	Pin	Function
A_0–A_{16}	23–39	**ADDRESS INPUTS:** During a burst operation, A_2–A_{16} provides the base address pointing to a block of four consective bytes. A_0 and A_1 select the first byte of the burst access. The 27960CX latches addresses in the first clock cycle. An internal address generator increments addresses A_0 and A_1 for subsequent bytes of the burst.
D_0–D_7	6, 7, 10, 11, 13, 14, 17, 18	**DATA INPUTS/OUTPUTS**
$\overline{ADS}$	42	**ADDRESS STROBE:** Indicates the start of a new bus access. $\overline{ADS}$ is active low in the first clock cycle of a bus access.
$\overline{CS}$	3	**CHIP SELECT:** Master device enable. When asserted (active low) data can be written to and read from the device. In read mode, $\overline{CS}$ enables the state machine and the I/O circuitry. **NOTE:** 1. The address decode path is independent of $\overline{CS}$, i.e., X and Y decoding is always powered up. 2. For programming, $\overline{CS}$ should remain low for the entire cycle. Program and verify functions are done one byte at a time. 3. $\overline{CS}$ going high does not terminate a concurrent burst cycle.
$\overline{BLAST}$	1	**BURST LAST:** Terminates a concurrent burst data cycle at the rising edge of the CLK. It must be asserted by the fourth data byte.
$\overline{RESET}$	22	**ASYNCHRONOUS RESET INPUT:** Resets the state machine into a known state, tri-states the outputs and puts address latches into the flow through mode. $\overline{RESET}$ must be asserted for a minimum of 10 clock cycles. At least 5 clock cycles are required after deassertion of $\overline{RESET}$ before beginning the next cycle. $\overline{RESET}$ will abort a concurrent bus cycle.
$\overline{PGM}$	43	**PROGRAM-PULSE CONTROL INPUT**
V_{PP}	2	**PROGRAMMING POWER SUPPLY**
V_{SS}	5, 8, 12, 15, 19, 21	**GROUND**
V_{CC}	9, 16, 20, 44	**SUPPLY VOLTAGE INPUT**

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INTERFACE EXAMPLE

Overview

This example illustrates 8-, 16- and 32-bit wide 27960CX interfaces to the 80960CA. The designs offer a simple "no-glue" interface.

A non-buffered 27960CX system organized as 256K x 32 is shown in Figure 4A. Since the 27960CX is capable of driving a 80 pF load, large, non-buffered systems can be implemented by stacking up to 2 banks of 4 EPROMs, resulting in a 256K x 32 memory subsystem. The input capacitive load seen on the address lines (due to the EPROM only) is 24 pF for a 128K x 32 system and 48 pF for a 256K x 32 system. The EPROM is specified at 6 pF for input capacitance (15 pF max) and 12 pF typical for output capacitance. Larger systems can be implemented with buffers (Figure 4B).

Chip Select Logic

High order address lines are decoded to provide $\overline{CS}$. Qualification with other signals is not required. The chip select logic can be implemented with standard asynchronous decoders, PAL's or PLD's (like Intel's 85C508).

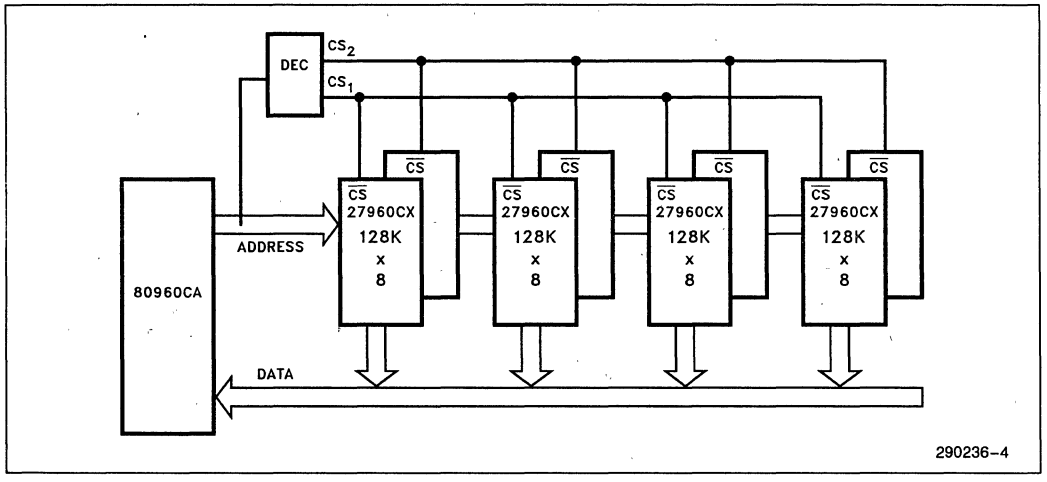


Figure 4A. 256K x 32 Non-Buffered Burst EPROM Memory System

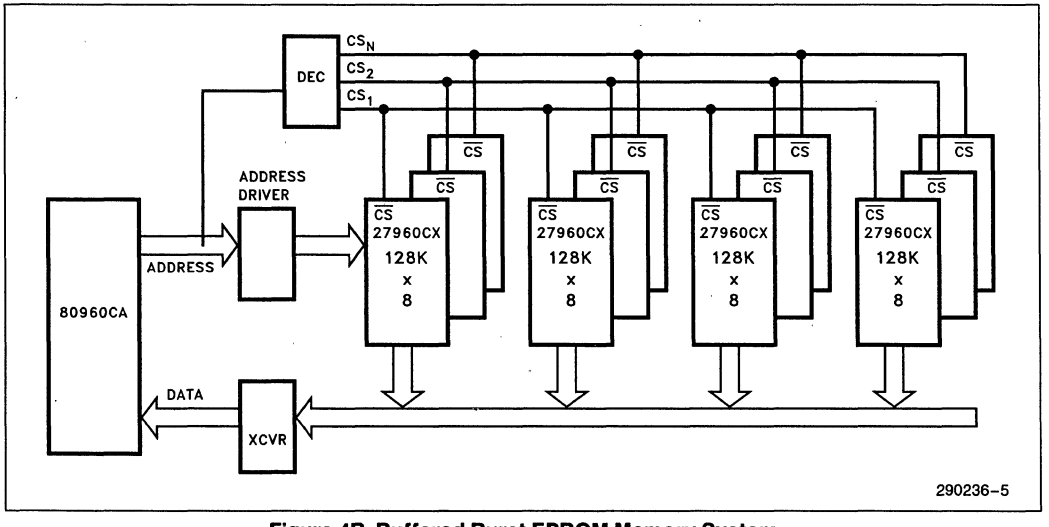


Figure 4B. Buffered Burst EPROM Memory System

Schematics

Figure 5 shows a non-buffered, 128K x 32 27960CX EPROM system.

Chip select logic, the only external logic that is required for this interface, can be derived from the global system chip select circuitry.

In a non-buffered, 16-bit system (Figure 6A) $\overline{BE1}$ and A_2 connect to the lower order address bits of the 27960CX. $\overline{BE1}$ connects to A_0 of both EPROMs, while A_2 connects to both A_1's.

In a non-buffered, 8-bit system (Figure 6B) $\overline{BE0}$ and $\overline{BE1}$ connect to A_0 and A_1 respectively.

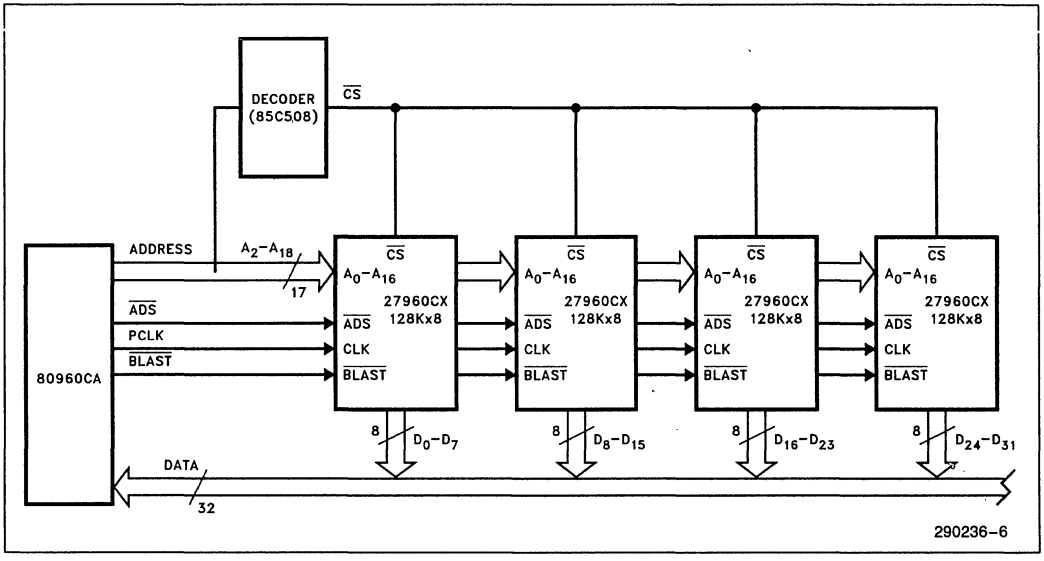


Figure 5. 128K x 32 27960CX Burst EPROM System

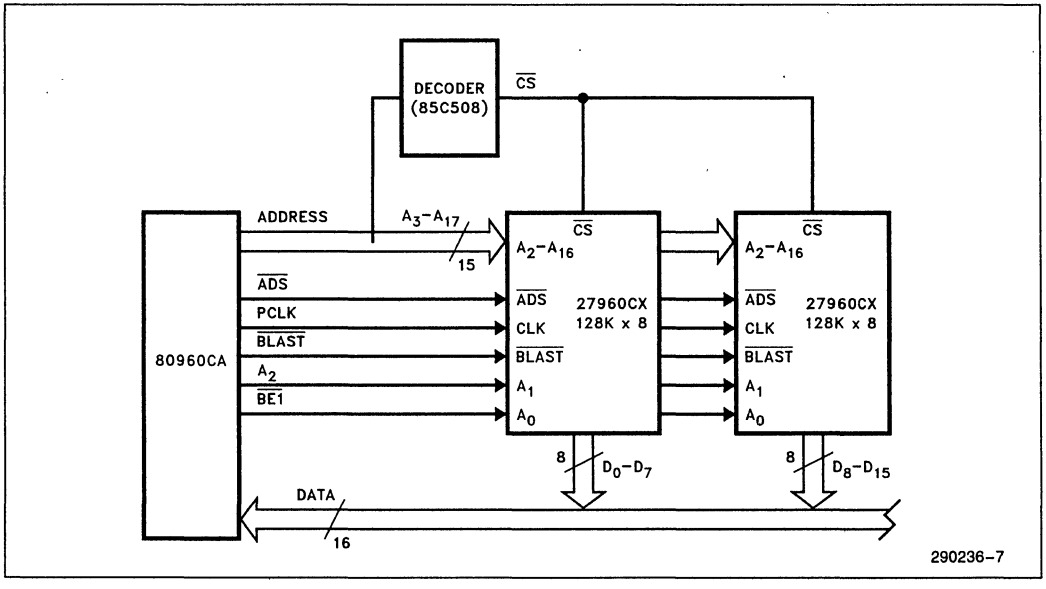


Figure 6A. 27960CX Burst EPROM in a 16-Bit System

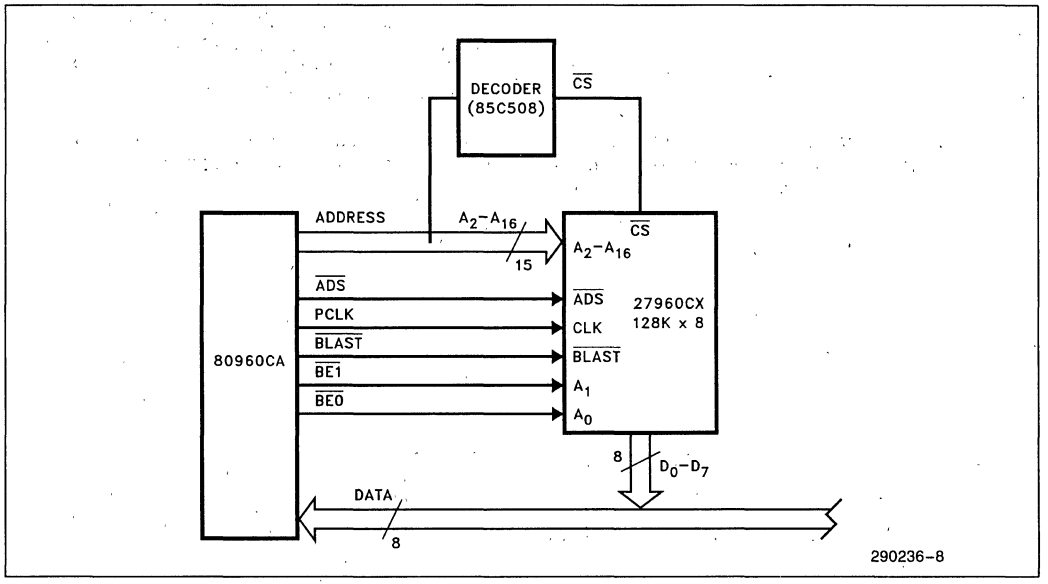


Figure 6B. 27960CX Burst EPROM in a 8-Bit System

Waveforms

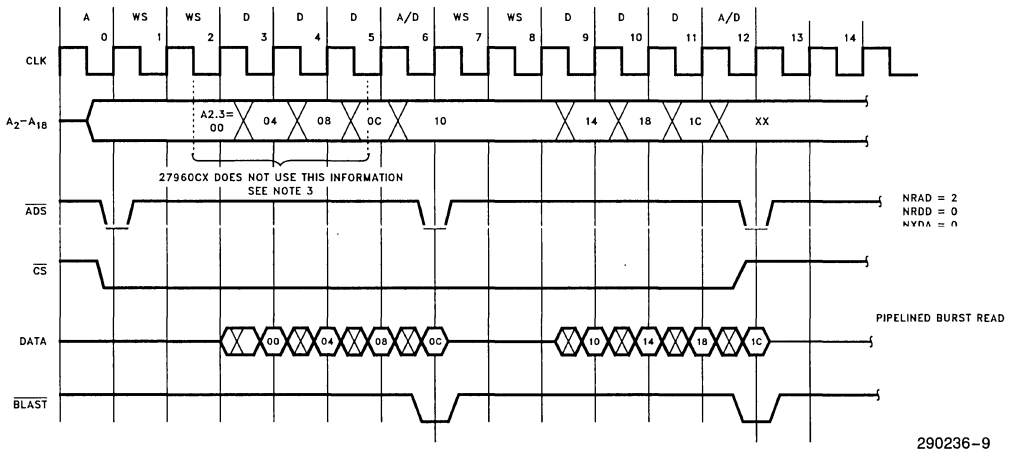
Figure 7 shows the timing waveforms of a 27960CX pipelined read in a 32-bit system.

$\overline{CS}$ Setup Time

$\overline{CS}$ setup time is the time between $\overline{CS}$ being asserted and the first CLK rising edge (during the address cycle). Since a memory access begins on the first CLK rising edge after $\overline{ADS}$ and $\overline{CS}$ are asserted, a minimum $\overline{CS}$ setup time of 5 ns (t_{SVCH}) at 33 MHz is required. With the 80960CA's maximum valid address delay of 18 ns at 33 MHz, 7 ns remains for $\overline{CS}$ decoding logic.

Bootup

The wait state configuration (1 or 2), of the 27960CX is programmed by the user into the 80960CA Region Table parameters of NRAD, NRDD, and NXDA. NRDD is always 0 for the 27960CX.



NOTES:
1. The EPROM can also operate in non pipelined mode i.e, next address and $\overline{ADS}$ can be asserted in the clock cycle following the last data word of the burst.
2. 2 – 0 – 0 – 0 Burst Read → 2 indicates the number of wait states to access the first word
   0's indicate the number of wait states for subsequent data words:
   0 in this case!
3. 27960CX latches addresses on the falling edge of clock cycle 1 after sampling $\overline{CS}$ and $\overline{ADS}$ it has an internal address generator which increments addresses for subsequent words of the burst. It ignores the states of A_2, A_3 and $\overline{BE0}$–$\overline{BE3}$ during a burst.

Figure 7. Two Cycles of a 27960CX 2 Wait State 4 Byte Read (2–0–0–0 Burst Read) in a 32 Bit System

During boot-up (Figure 8), the 80960CA picks up it's Region Table data from addresses FFFF FF00; FFFF FF04; FFFF FF08 and FFFF FF0C. Only the least significant byte of each of the above four 32-bit accesses is used to configure the Region Table. For boot-up, the wait-state parameters NRAD and NXDA default to 31 and 3 respectively. During boot-up, the 27960CX will wrap around the first word of the four-word burst and hold the first word until $\overline{BLAST}$ is asserted.

27960CX DEVICE NAMES

The device names on the 27960CX were derived as mnemonics that correspond to the number of wait states and expected operating frequency for the device. For example, the 25 MHz, 2 wait state 27960CX is named 27960C2-25.

AC TIMING DERIVATIONS

The AC timings for the 27960CX were generated specifically to meet the requirements of the 80960CA microprocessor. In each case the applicable 80960CA clock frequency and AC timing were taken together with an address buffer delay (if needed) and a typical 2 ns guardband to generate the 27960CX AC timing. Worst case timings were always assumed. The example below shows how the 27960C2-33 tavc$_0$h timing was derived.

@33 MHz the clock cycle is ~30 ns.
t_{OV2} of the 80960CA is 3 ns – 16 ns.
Typical 2 ns guardband.

27960C2-33 tavc$_0$h = 30 ns – 16 ns – 2 ns
= 12 ns

On timings where the EPROM is faster than the microprocessor, we specified the time required by the EPROM and left the excess time as additional system guardband.

Decoders are needed for the systems chip select decoding. For the 27960CX timings we assumed a 10 ns chip select decoder for 20 MHz and 16 MHz and a 7 ns decoder for 25 MHz and 33 MHz systems. The example below shows how the 27960C2-33 tsvch timing was derived.

@33 MHz the clock cycle is ~30 ns.
t_{OV2} of the 80960CA is 3 ns – 16 ns.
Decoder = 7 ns

27960C2-33 tsvch = 30 ns – 16 ns – 7 ns
= 7 ns

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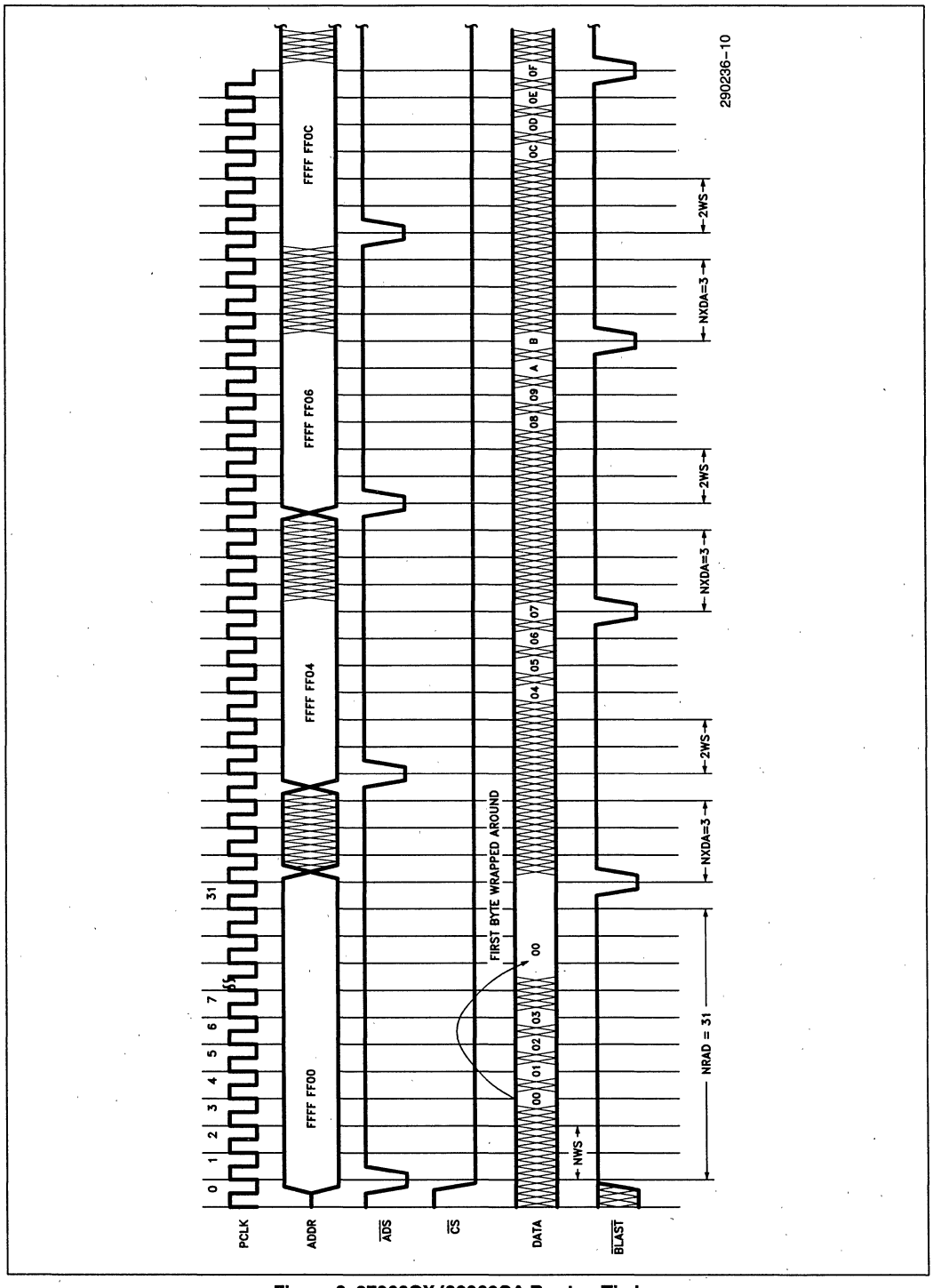

Figure 8. 27960CX/80960CA Bootup Timing

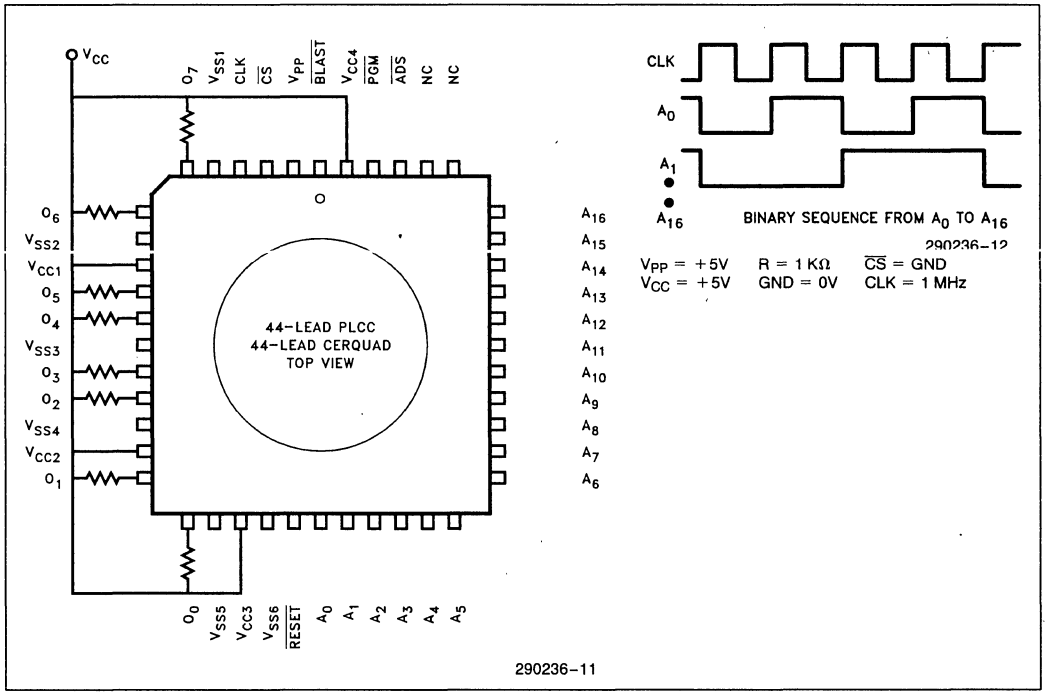

Figure 9. 27960CX Burn in Biasing Diagram

System Buffering Considerations

For large system applications buffering may be required between the microprocessor and memory devices. The 25, 20 and 16 MHz 27960CX AC timings take this into account. For applications not requiring buffering these devices will provide additional system guardband.

The list below shows the buffers used in generating the 27960CX timings:

	Input Buffer	Output Buffer
25 MHz	8 ns	5 ns
20 MHz	10 ns	7 ns
16 MHz	10 ns	7 ns

Note that the 25 MHz buffers are slightly faster in keeping with the increased sensitivity for higher performance. Significantly faster buffers are available for applications requiring them. The example below shows the tchqv timing analysis for a buffered 27960C2-25.

@25 MHz the clock cycle is ~40 ns.

t_{IH1} of the 80960CA is 5 ns.

Output buffer for 25 MHz = 5 ns

27960C2-25 t_{CHQV} = 40 ns − 5 ns − 5 ns
= 30 ns

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ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature . . . . . 0°C to +70°C(8)
Case Temperature Under Bias . . −10°C to +80°C(8)
Storage Temperature . . . . . −65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . −0.6V to +6.5V(4)
Voltage on A_9 with Respect to Ground . . . . . −0.6V to +13.0V(4)
V_{PP} Supply Voltage with Respect to Ground . . . . . −0.6V to +14.0V(4)
V_{CC} Supply Voltage with Respect to Ground . . . . . −0.6V to +7.0V(4)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS $0°C < T_A +70°C$, $V_{CC} = 5V \pm 10\%$, TTL Inputs

Symbol	Parameter		Notes	Min	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current				10	µA	$V_{OUT} = 5.5V$
I_{PP}	V_{PP} Load Current Read				10	µA	$V_{PP} = 0$ to V_{CC}, $\overline{PGM} = V_{IH}$
I_{SB}	V_{CC} Standby	Switching	2		45	mA	$\overline{CS} = V_{IH}$, f = 33 MHz
		Stable	2		30	mA	$\overline{CS} = V_{IH}$
I_{CC}	V_{CC} Active Current		1, 3, 7		125	mA	$\overline{CS} = V_{IL}$, f = 33 MHz, $I_{OUT} = 0$ mA
V_{IL}	Input Low Voltage		4	−0.5	0.8	V	
V_{IH}	Input High Voltage			2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage				0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		5	$V_{CC} - 0.8$		V	$I_{OH} = -100$ µA
			5	2.4		V	$I_{OH} = -400$ µA
I_{OS}	Output Short Circuit		6		100	mA	

NOTES:
1. Maximum current is with outputs unloaded.
2. I_{CC} standby current assumes no output loading i.e., $I_{OH} = I_{OL} = 0$ mA.
3. I_{CC} is the sum of current through $V_{CC3} + V_{CC4}$ and does not include the current through V_{CC1} and V_{CC2}. (V_{CC1} and V_{CC2} supply power to the output drivers. V_{CC3} and V_{CC4} supply power to the reset of the device.)
4. Minimum DC input voltage on input and output pins is −0.5V. During transitions, this level may undershoot to −2.0V for periods less than 20 ns.
5. Maximum DC voltage on input and output pins is $V_{CC} + 0.5V$ which may overshoot to $V_{CC} + 2.0V$ for periods less than 20 ns.
6. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
7. I_{CC} max measured with a 0.11 µF capacitor between V_{CC} and V_{SS}.
8. This specification defines commercial product operating temperatures.

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name. e.g., (CLK, $\overline{ADS}$, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated for the fourth character. The list below shows character representations.

A:	Address	R:	$\overline{Reset}$
B:	$\overline{BLAST}$	Q:	Data
C:	Clock	S:	$\overline{CS}$
H:	Logic High Level	t:	Time
L:	$\overline{ADS}$/Logic Low Level	V:	Valid
P:	V_{PP} Programming Voltage	Z:	Tri-state Level
X:	No longer a valid "driven" logic level		

AC CHARACTERISTICS: READ OPERATION $0°C < T_A < +70°C, V_{CC} = 5V \pm 10\%$

Versions				27960C2-33 33 MHz 2 Wait State		27960C2-25 25 MHz 2 Wait State		27960C1-20 20 MHz 1 Wait State		27960C1-16 16 MHz 1 Wait State		Unit
No.	Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{AVC_0H}	Address Valid to CLK High	CLK_0	12		10		14		22		ns
2	t_{C_NHAX}	CLK High to Address Invalid	2	0		0		0		0		ns
3	t_{LLCH}	$\overline{ADS}$ low to CLK High	CLK_0	8		8		14		22		ns
4	t_{CHLH}	CLK high to $\overline{ADS}$ High	5	6	22	6	32	6	36	6	40	ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High	1	7		7		6		14		ns
6	t_{C_NHSX}	CLK High to $\overline{CS}$ Invalid	2	0		0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		27		30		35		40	ns
8	t_{CHQX}	CLK High to Data Invalid		5		5		5		5		ns
9	t_{CHQZ}	CLK High to Data High Z	6		25		30		30		30	ns
10	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		8		8		14		22		ns
11	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	3	6	22	6	32	6	36	6	40	ns

NOTES:
1. Valid signal level is meant to be either a logic high or logic low.
2. The subscript N represents the number of wait states for this parameter. $\overline{CS}$ can be de-asserted (high) after the number of wait states (N) has expired and the EPROM will continue to burst out data for the current cycle.
3. BLAST# must be returned high before the next rising clock edge.
4. The sum of $t_{CHQV} + t_{AVCH} + N_{CLK}$ will not equal actual t_{AVQV} if independent test conditions are used to obtain t_{AVCH} and t_{CHQV} (N = number of wait states).
5. $\overline{ADS}$ must be returned high before the next rising clock edge.
6. Sampled, not 100% tested. The transition is measured ±500 mV from steady state voltage.
7. For capacitive loads above 80 pF, t_{CHQV} can be derated by 1 ns/20 pF.

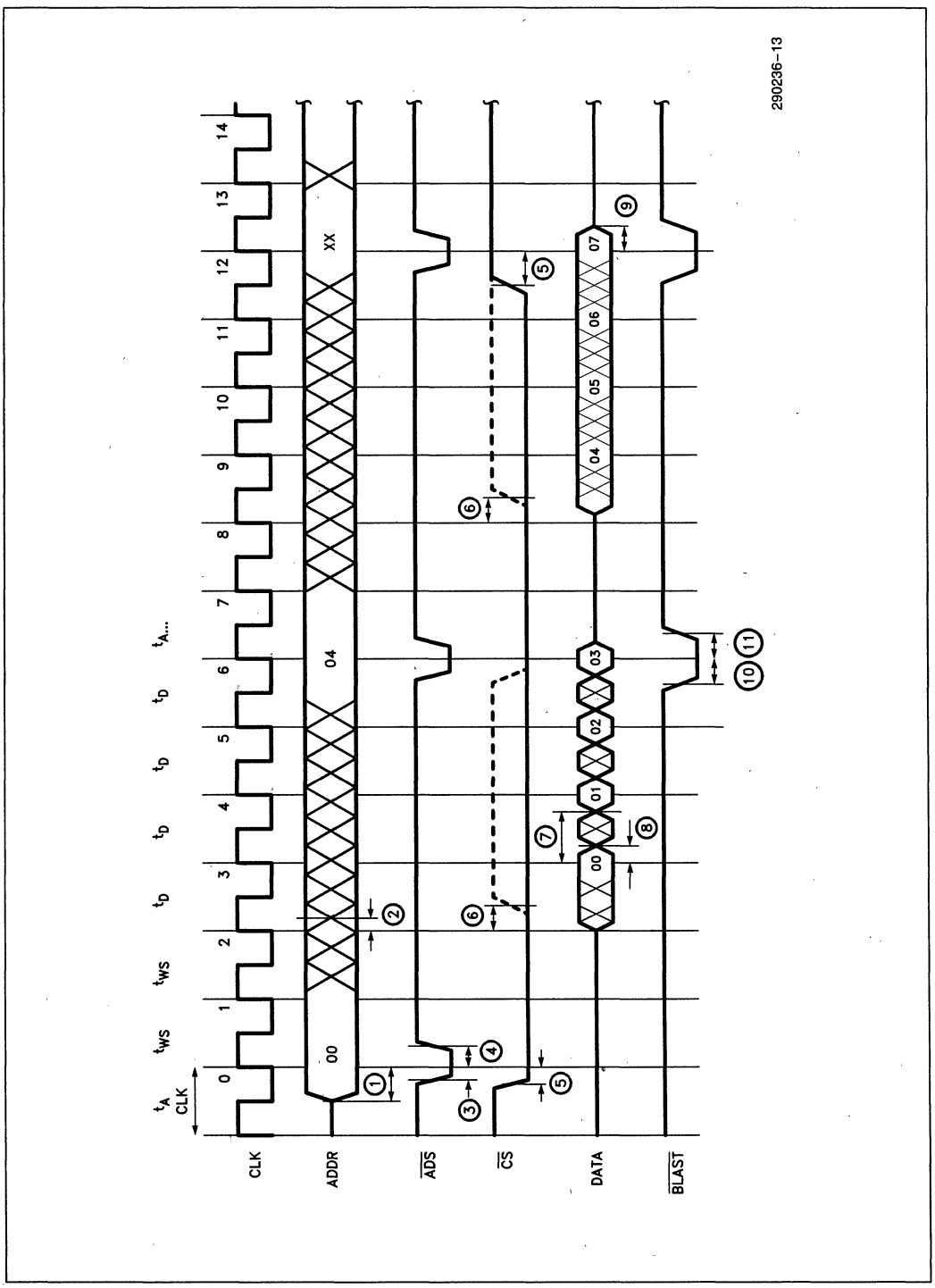

Figure 10. 27960CX Pipelined 2 Wait State AC Waveforms

AC CONDITIONS OF TEST

Input Rise and Fall Times
(10% to 90%) ..... 4 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Table 2. Mode Table

Mode	$\overline{CS}$	$\overline{PGM}$	$\overline{BLAST}$	$\overline{ADS}$	$\overline{RESET}$	A_9	V_{PP}	V_{CC}	OUTPUT
Read	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Standby(6)	V_{IH}	X	X	X	V_{IH}	X	V_{CC} (5)	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{IH}(2)	V_{IH}	X	(3)	(3)	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}	V_{IH}	X	(3)	(3)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{IH}	X	(3)	(3)	High Z
ID Byte 0: Manufacturer	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	89H
ID Byte 1: Part (27960)	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	E0H
ID Byte 2: CX	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	01B
ID Byte 3: 1 Wait State 2 Wait States	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	01B 10B
Reset	X	X	X	X	V_{IL}	X	V_{CC}	V_{CC}	High Z

NOTES:
1. V_{IH} until data terminated at which time $\overline{BLAST}$ must go to V_{IL}.
2. Need to toggle from V_{IH} to V_{IL} to V_{IH}.
3. See DC Programming Characteristics for V_{CC}, V_{ID} and V_{PP} voltages.
4. X can be V_{IL} or V_{IH}.
5. $V_{PP} = V_{CC}$ to meet standy current specification. $V_{CC} > V_{PP} > V_{IL}$ will cause a slight increase in standby current.
6. The device must be in the idle state (by asserting $\overline{RESET}$ or using $\overline{BLAST}$) before going into standby.

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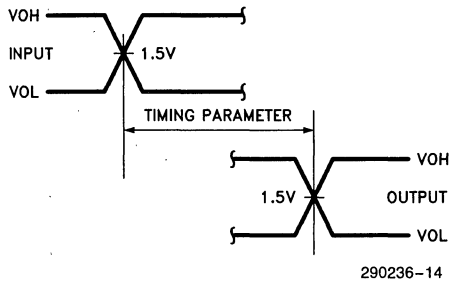
CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	15	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Capacitance	40	45	pF	$V_{IN} = 0V$

NOTE:
1. Sampled. Not 100% tested.

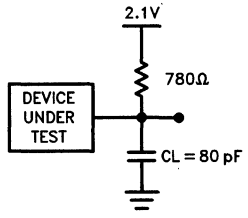
AC INPUT/OUTPUT REFERENCE WAVEFORMS



290236-14

Input and output timings are measured from 1.5V. Timing values are specified assuming maximum input and output rise and fall time = 4 ns.

AC TESTING LOAD CIRCUIT



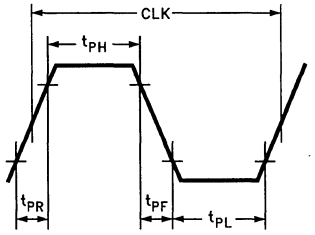
290236-15

CL includes jig capacitance
For t_{CHQZ} C_L = 5 pF and R_L = 405Ω

CLOCK CHARACTERISTICS

Versions		33 MHz		25 MHz		20 MHz		16 MHz		Units
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
CLK	Period	30.3		40		50		62.5		ns
t_{PR}	Rise Time	1	4	1	4	1	4	1	4	ns
t_{PF}	Fall Time	1	4	1	4	1	4	1	4	ns
t_{PL}	Low Time	(t/2) − 2	t/2	(t/2) − 3	t/2	(t/2) − 4	t/2	(t/2) − 4	t/2	ns
t_{PH}	High Time	(t/2) − 2	t/2	(t/2) − 3	t/2	(t/2) − 4	t/2	(t/2) − 4	t/2	ns
Max Rise Time for Programming CLK = 100 ns										

CLOCK WAVEFORM



290236-16

Program/Program Verify

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" can be programmed, both "1's" and "0's" can be present in the data word. Ultraviolet erasure is the only way to change "0's" to "1's".

Programming mode is entered when V_{PP} is raised to 12.75V. Program/Verify operation is synchronous with the clock and can only be initiated following an idle state. Program and Program Verify take place in 3 clock cycles. In the first clock cycle, addresses and data are input and programming occurs. Program Verify follows in the second clock cycle and the third clock cycle terminates synchronous Program/Verify operation, returning the state machine to the idle state with outputs at high impedance.

As in the Read mode, A_2–A_{16} point to a four byte block in the memory array. During programming, the internal address increment circuitry is disabled and the programmer must supply A_0 and A_1 to point to an individual byte within the four byte block that is to be programmed. Only one byte is programmed in each 3 cycle Program/Verify sequence.

Program Inhibit

The Program Inhibit mode allows parallel programming and verification of multiple devices with different data. With V_{PP} at 12.75V, a Program/Verify sequence is initiated for any device that receives a valid $\overline{ADS}$ pulse and rising clock edge while $\overline{CS}$ is asserted. A $\overline{PGM}$ pulse programs data in the first cycle of the sequence and data for Program Verify is output in the second cycle. The Program/Verify sequence is inhibited on any devices for which $\overline{CS}$ is not asserted. Data will not be programmed and the outputs will remain in their high impedance state.

inteligent Identifier™ Mode

The device's manufacturer, product type, and configuration are stored in a four byte block that can be accessed by using the inteligent Identifier™ mode. The programmer can verify the device identifier and choose the programming algorithm that corresponds to the Intel 27960CX. The inteligent Identifier can also be used to verify that the product is configured with the desired Read mode options for wait states.

inteligent Identifier mode is entered when A_9 (pin 32) is raised to its high voltage (V_{ID}) level. The internal state machine is then set for inteligent Identifier Read operation. Reading the identifier is similar to a Read operation on a one wait state configured product. Up to four bytes can be read in a single burst access. inteligent Identifier read is terminated by a synchronous $\overline{BLAST}$ input, returning the state machine to the idle state with outputs at high impedance.

The four byte block code for the inteligent Identifier code is located at address 00H through 03H and is encoded as follows:

MEANING	(A1, A0)	DATA
Intel ID	Byte 00	89h
27960	Byte 01	E0h
CX	Byte 10	01b
1 Wait State	Byte 11	01b
2 Wait States	Byte 11	10b

RESET MODE

Due to the synchronous nature of the 27960CX, the various operating modes must be initiated from a known idle state. During normal operation, the internal state machine returns to an idle state at the termination of a bus access (after $\overline{BLAST}$ is asserted).

During initial device power up, the state machine is in an indeterminant state. The reset mode is provided to force operation into the idle state. Reset mode is entered when the $\overline{RESET}$ pin is asserted. Output pins are asynchronously set to the high impedance state and address latches are put into the flow through mode. A reset is successfully completed and the state machine set in an idle state when $\overline{RESET}$ has been asserted for a minimum of 10 clock cycles and deasserted for five clock cycles.

5

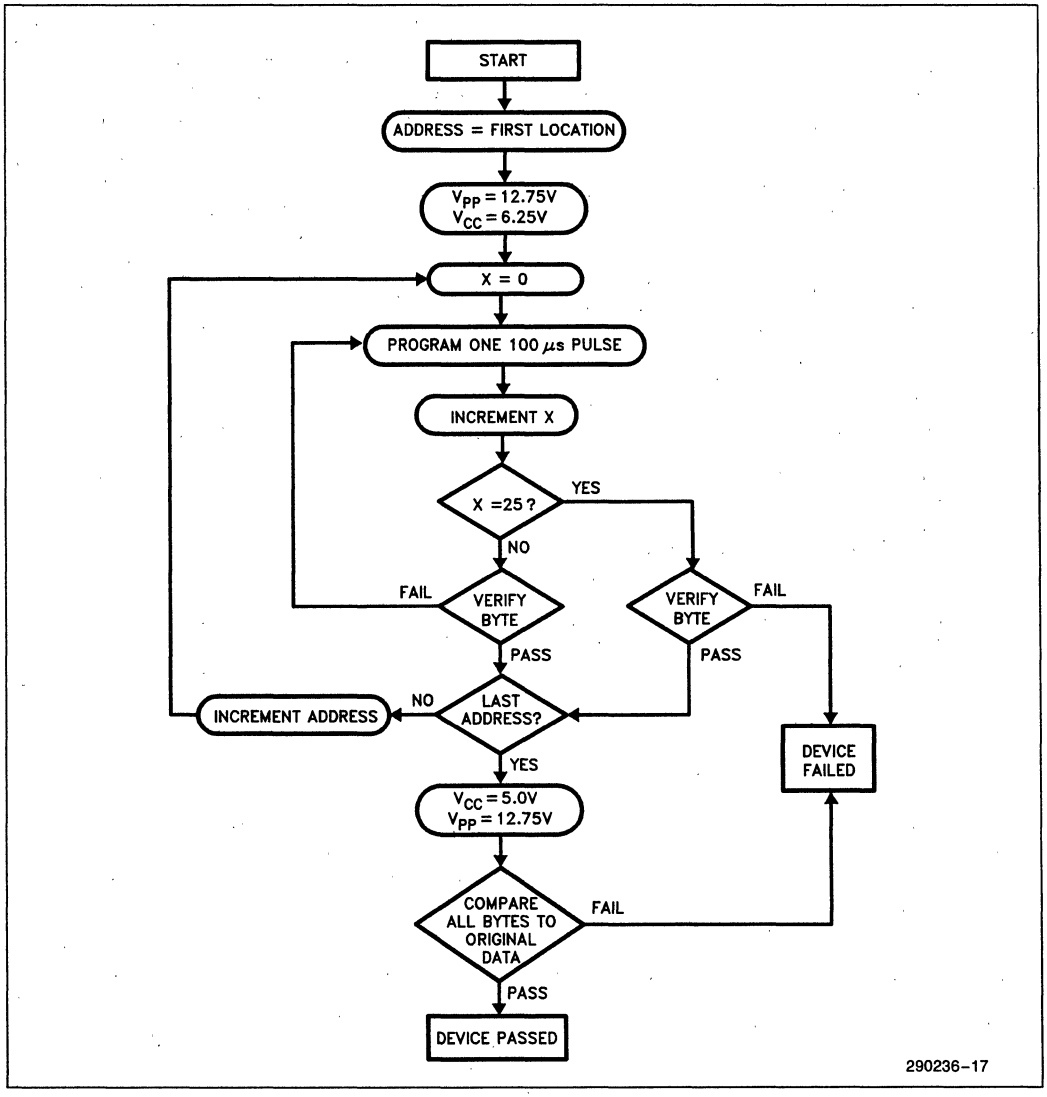


Figure 11. Quick-Pulse Programming™ Algorithm

ERASURE CHARACTERISTICS (FOR WINDOWED DEVICES)

Exposure to light of wavelength shorter than 4000 Angstroms begins erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000 Angstrom range. Constant exposure to room-level fluorescent light can erase the EPROM array in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537 Angstrom ultraviolet light. The minimum integrated erasure time using a 12000 fW/cm2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm2 (1 week @ 12000 fW/cm^2). High intensity UV light exposure for longer periods can cause permanent damage.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm programs Intel's 27960CX. Developed to substantially reduce programming throughput time, this algorithm allows optimized equipment to program a 27960CX in under 17 seconds. Actual programming time depends on the programmer used.

The Quick-Pulse Programming algorithm uses a 100 μs pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100 μs pulses fail to program a byte. Figure 11 shows the 27960CX Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. The program equipment must establish V_{CC} before applying voltages to any other pins. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V and V_{PP} = 12.75V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25° \pm 5°C$

Symbol	Parameter	Notes	Min	Max	Unit	Condition
I_{LI}	Input Load Current			10	μA	$V_{IN} = V_{IH}$ or V_{IL}
I_{CC}	V_{CC} Program Current	1		125	mA	$\overline{CS} = V_{IL}$
I_{PP}	V_{PP} Program Current	1		50	mA	$\overline{CS} = V_{IL}$
V_{IL}	Input Low Voltage		−0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(Verify)			0.40	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage(Verify)		V_{CC} − 0.8		V	I_{OH} = −400 μA
V_{ID}	A9 int$_e$ligent Identifier Voltage		11.5	12.5	V	
V_{CC}	Supply Voltage (Program)	2	6.0	6.5	V	
V_{PP}	Program Voltage	2	12.5	13.0	V	

NOTES:
1. The maximium current value is with outputs unloaded.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. During programming clock levels are V_{IH} and V_{IL}.

A.C. PROGRAMMING, RESET AND ID CHARACTERISTICS $0°C < T_A < +70°C$

No.	Symbol	Parameter	Notes	Min	Max	Unit
1	t_{AVPL}	Address Valid to $\overline{PGM}$ Low		2		μs
2	t_{CHAX}	CLK High to Address Invalid		50		ns
3	t_{LLCH}	$\overline{ADS}$ Low to CLK High	1	50		ns
4	t_{CHLH}	CLK High to $\overline{ADS}$ High	2	50		ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High		50		ns
6	t_{CHSX}	CLK High to $\overline{CS}$ Invalid	3			ns
7	t_{CHQV}	CLK High to D_{OUT} Valid		100		ns
8	t_{CHQX}	CLK High to D_{OUT} Invalid		0		ns
9	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		50		ns
10	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	4	50		ns
11	t_{QVPL}	DATA Valid to $\overline{PGM}$ Low		2		μs
12	t_{PLPH}	$\overline{PGM}$ Program Pulse Width		95	105	μs
13	t_{PHQX}	$\overline{PGM}$ High to D_{IN} Invalid		2		μs
14	t_{CLPL}	CLK Low to $\overline{PGM}$ Low		50		ns
15	t_{QZCH}	D_{IN} Tri-State to CLK High		2		μs
16	t_{VCS}	V_{CC} Program Voltage to CLK High	7	2		μs
17	t_{VPS}	V_{PP} Program Voltage to CLK High	7	2		μs
18	t_{A_9HCH}	A_9 V_{ID} Voltage to CLK High		2		μs
19	t_{CHA_9X}	CLK High to A_9 Not V_{ID} Voltage		2		μs
20	t_{RVCH}	$\overline{RESET}$ Valid to CLK High	6	50		ns
21	t_{CHCL}	CLK High to CLK Low	5	100		ns
22	t_{CLCH}	CLK Low to CLK High	5	100		ns

NOTES:
1. If $\overline{CS}$ is low, $\overline{ADS}$ can go low no sooner than the falling edge of the previous CLK.
2. $\overline{ADS}$ must return high prior to the next rising edge of clock.
3. $\overline{CS}$ must remain low until after the rising edge of CLK1.
4. $\overline{BLAST}$ must return high prior to the next rising edge of CLK.
5. Max CLK rise/fall time is 100 ns.
6. $\overline{RESET}$ must be low for 10 clock cycles and high for 5 clock cycles.
7. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

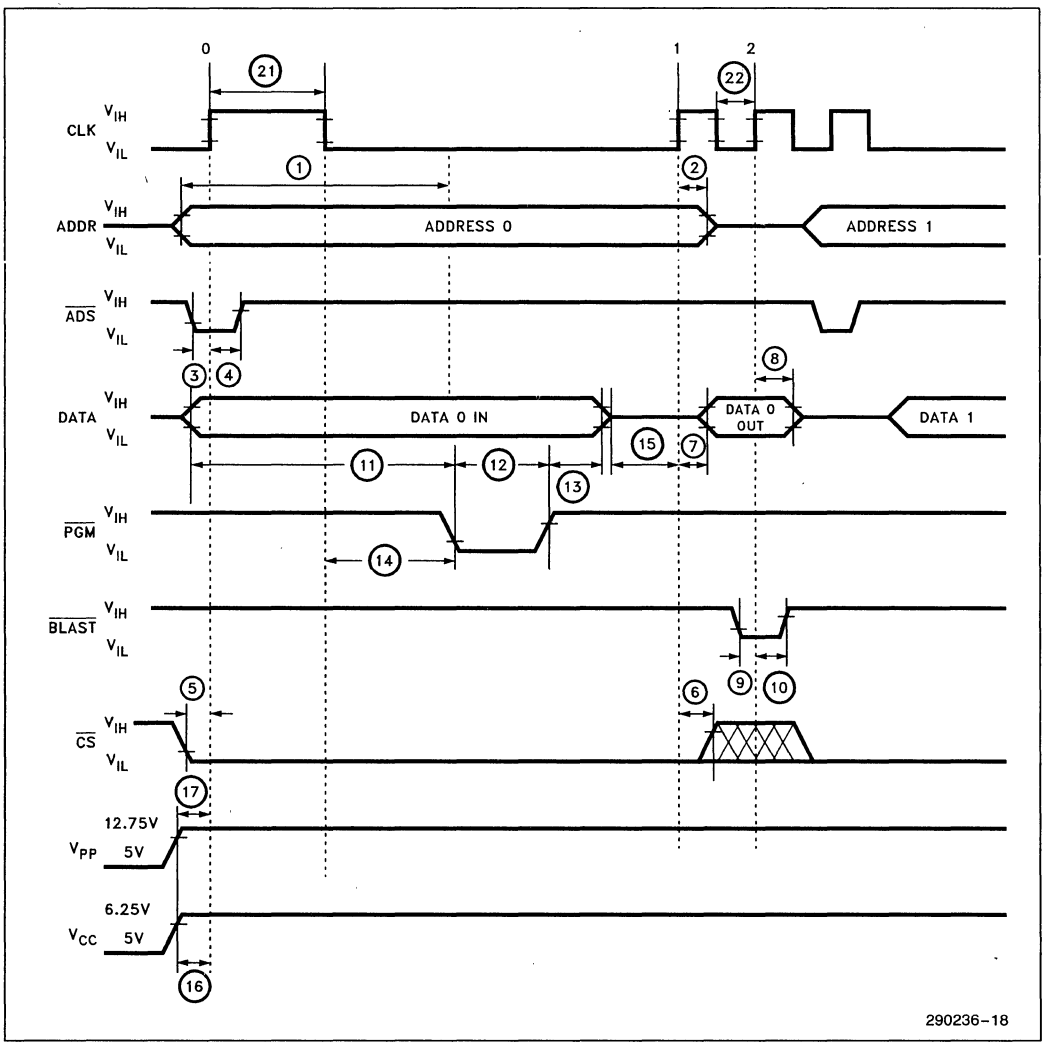


Figure 12. 27960CX Programming Waveforms

RESET and int$_e$ligent Identifier Waveforms

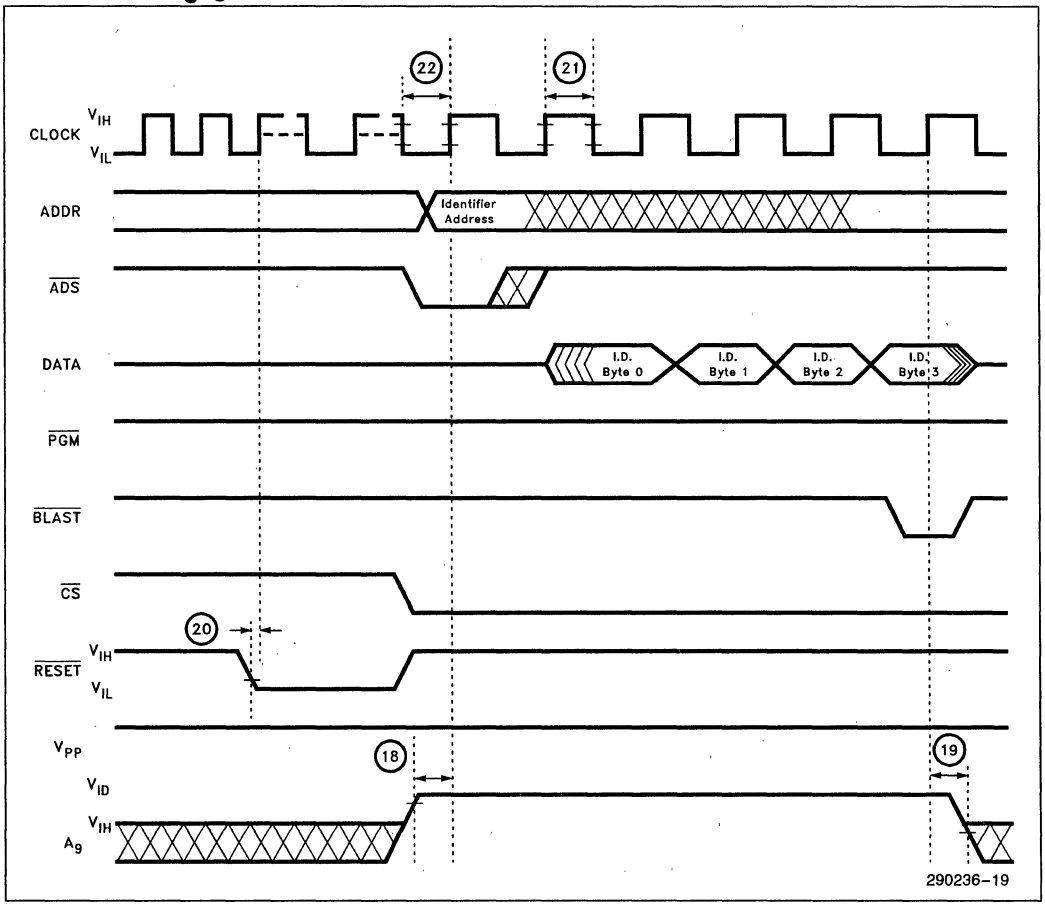


Figure 13. 27960CX RESET and ID Waveforms

27960KX
BURST ACCESS 1M (128K x 8) CHMOS EPROM

- **Synchronous 4-Byte Data Burst Access**
- **Simple Interface to the 80960KA/KB**
- **High Performance Clock to Data Out**
  - **— Zero Wait State Data-to-Data Burst**
  - **— Supports 16, 20 and 25 MHz 80960KA/KB Devices**
- **Asynch Microcontroller Reset Function**
  - **— Returns to Known State with High Z Outputs**
- **CHMOS* III-E for High Performance and Low Power**
  - **— 125 mA Active, 30 mA Standby**
  - **— TTL Compatible Inputs**
- **1 Mbit Density Configures as 128K x 8**
  - **— Upgrade Path to 512K x 8**

Intel's 27960KX is a 5V only, 1,048,576 bit, Erasable Programmable Read Only Memory, organized as 128K words of 8 bits. It is a member of a new family of high performance EPROMs with synchronous burst access.

The 27960KX provides a simple synchronous burst interface to the 80960KA/KB bus. Internally the 27960KX is organized in 4 byte blocks, in which each byte is accessed sequentially. The internal state machine is factory configured to generate either 1 or 2 wait-states between the address and first data byte. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 25 MHz.

An asynchronous microcontroller $\overline{\text{RESET}}$ feature puts the outputs in the high impedance state and takes the internal state machine to a known state where a new burst access can begin.

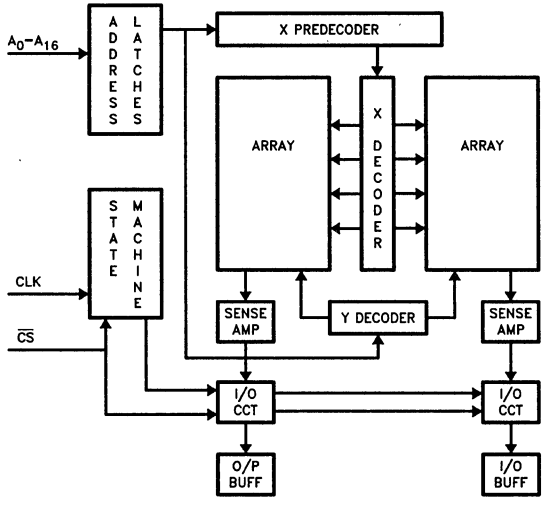
The 27960KX is available in either 44 lead Cerquad (reprogrammable) or PLCC packages. Cerquad allows for code changes in the R & D environment while PLCC provides optimum cost effectiveness during production. Two No Connects (NC) on the package allow for an upgrade to 4 Mbits (512K x 8).

The 27960KX is manufactured on Intel's 1 micron CHMOS III-E technology. The Quick-Pulse Programming™ algorithm provides fast, reliable programming with throughput under 17 seconds for optimized equipment.

Cerquad is available in a socket only version.

*CHMOS is a patented process of Intel Corporation.

5



290237-1

Figure 1. 27960KX Burst EPROM Block Diagram

October 1990
Order Number: 290237-004

27960KX BURST EPROM

EPROMs are established as the preferred code storage device in embedded applications. The non-volatile, flexible, reliable, cost effective EPROM makes a product easier to design, manufacture and service. Until recently, however, EPROMs could not match the performance needs of high-end systems. The 27960KX was designed to support the 80960KA/KB embedded processor. It utilizes the burst interface to offer near zero-wait state performance without the high cost normally associated with this performance.

In embedded designs, board space and cost must be kept at a minimum without impacting performance and reliability. The 27960KX removes the need for expensive high-speed shadow RAM backed up by slow EPROM or ROM for non-volatile code storage. Code optimization concerns are reduced with "off-chip" code fetches no longer crippling to system performance. FONTs can be run directly out of these EPROMs at the same performance as high-speed DRAMs. With the 27960KX, the EPROM is the ideal code or FONT storage device for your 80960KA/KB system.

Architecture

The 27960KX provides a simple, synchronous burst interface to the 80960KA/KB's bus. Internally, the 27960KX is organized in 4 byte blocks each byte is accessed sequentially. A burst access begins on the first clock pulse after $\overline{CS}$ is asserted. The address of the four byte block is latched by the rising edge of $\overline{ALE}$. After a preset number of wait-states (1 or 2), data is output one byte at a time on each subsequent clock cycle. A burst access is terminated on the rising edge of CLOCK if $\overline{BLAST}$ is asserted. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 25 MHz. Extra power and ground pins dedicated to the outputs reduce the effects of fast output switching on device performance.

The 27960KX delivers 4 bytes of data in 8 clock cycles at 25 MHz and 4 bytes of data in 7 clock cycles at 20 MHz. In a 32-bit configuration, this translates into a read bandwidth of 50 Mbytes/sec and 45 Mbytes/sec respectively. Performance capability of the 27960KX in different 80960KA/KB systems is given in Table 1.

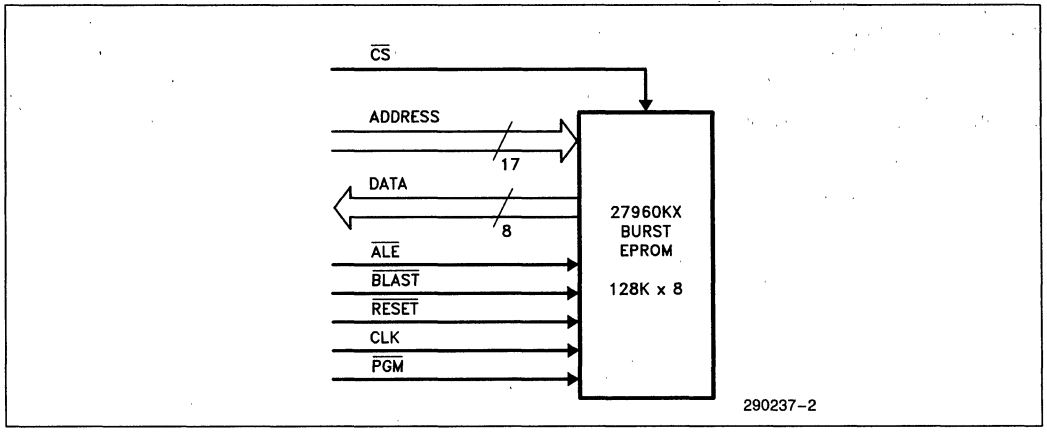


Figure 2. 27960KX Burst EPROM Signal Set

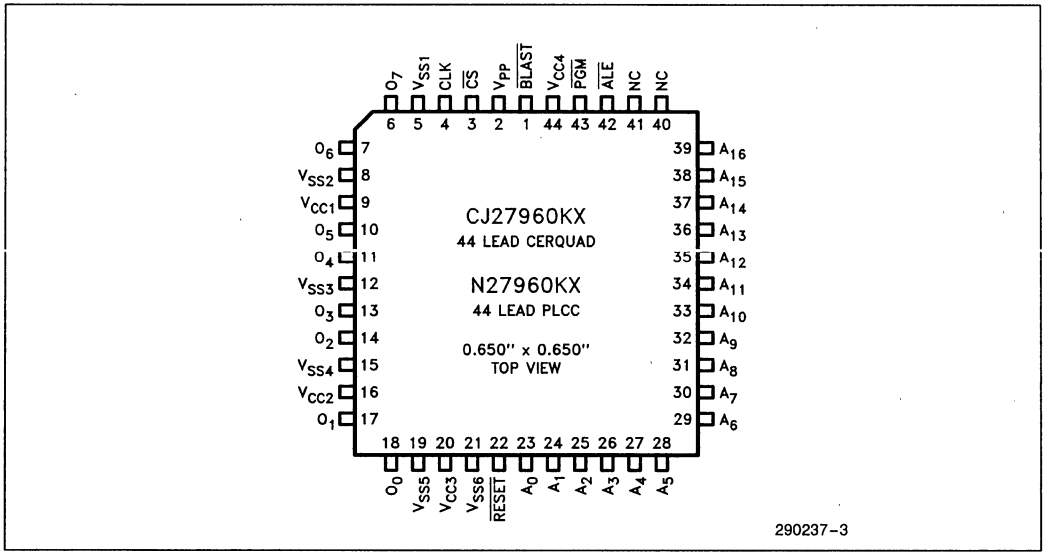


Figure 3. 27960KX 44-Lead PLCC/CERQUAD Pinout

PIN DESCRIPTIONS

Symbol	Pin	Function
A_0–A_{16}:	23–39	**ADDRESS INPUTS:** During a burst operation, A_2 and A_{16} provide the base address pointing to a block of four consecutive bytes. A_0 and A_1 select the first byte of the burst access. The 27960KX latches valid addresses in the first clock cycle. An internal address generator increments addresses A_0 and A_1 for subsequent bytes of the burst.
D_0–D_7:	6, 7, 10, 11, 13, 14, 17, 18	**DATA INPUTS/OUTPUTS**
$\overline{ALE}$	42	**ADDRESS LATCH ENABLE:** Indicates the transfer of a physical address. $\overline{ALE}$ is an active low signal used to latch the addresses from the processor. Addresses are latched on the rising edge of $\overline{ALE}$. Valid addresses must be present at or before $\overline{ALE}$ becomes valid.
$\overline{CS}$	3	**CHIP SELECT:** Master device enable. When asserted (active low) data can be written to and read from the device. In read mode, $\overline{CS}$ enables the state machine and the I/O circuitry. **NOTES:** 1. The address decode path is independent of $\overline{CS}$, i.e., X and Y decoding is always powered up. 2. For programming, $\overline{CS}$ should remain low for the entire cycle. Program and verify functions are done one byte at a time. 3. $\overline{CS}$ going high does not terminate a concurrent burst cycle. 4. $\overline{CS}$ must be deasserted between bursts.
$\overline{BLAST}$	1	**BURST LAST:** Terminates a concurrent burst data cycle at the rising edge of the CLK. It must be asserted by the fourth data byte.
$\overline{RESET}$	22	**ASYNCHRONOUS RESET INPUT:** Resets the state machine into a known state, tri-states the outputs and puts address latches into the flow through mode. The duration of $\overline{RESET}$ should be 10 CLK cycles minimum. At least 5 clock cycles are required after deassertion of $\overline{RESET}$ before beginning the next cycle. Reset will abort a concurrent bus cycle.

5

PIN DESCRIPTIONS (Continued)

Symbol	Pin	Function
$\overline{PGM}$	43	**PROGRAM-PULSE CONTROL INPUT**
V_{PP}	2	**PROGRAMMING POWER SUPPLY V_{PP}**
V_{SS}	5, 8, 12, 15, 19, 21	**GROUND**
V_{CC}	9, 16, 20, 44	**SUPPLY VOLTAGE INPUT**

Table 1. Performance Capability

25/20 MHz 2 WS NON-BUFFERED : 4 WORDS/8 CLOCK CYCLES → 50/40 MBYTES/SEC

ADDR	A_{00}	WS	WS	-	-	-	-	RS	A_{01}	WS	WS	-	-	-	-	RS
DATA	-	-	-	D_{00}	D_{01}	D_{02}	D_{03}	-	-	-	-	D_{10}	D_{11}	D_{12}	D_{13}	
CLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8

20 MHz 1 WS NON-BUFFERED : 4 WORDS/7 CLOCK CYCLES → 45 MBYTES/SEC

ADDR	A_{00}	WS	-	-	-	-	RS	A_{01}	WS	-	-	-	-	RS	A_{03}	WS
DATA	-	-	D_{00}	D_{01}	D_{02}	D_{03}	-	-	-	D_{10}	D_{11}	D_{12}	D_{13}			
CLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_7		

16 MHz 1 WS BUFFERED : 4 WORDS/7 CLOCK CYCLES → 36 MBYTES/SEC

ADDR	A_{00}	WS	-	-	-	-	RS	A_{01}	WS	-	-	-	-	RS	A_{03}	WS
DATA	-	-	D_{00}	D_{01}	D_{02}	D_{03}	-	-	-	D_{10}	D_{11}	D_{12}	D_{13}			
CLK	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_1	C_2	C_3	C_4	C_5	C_6	C_7		

INTERFACE EXAMPLE

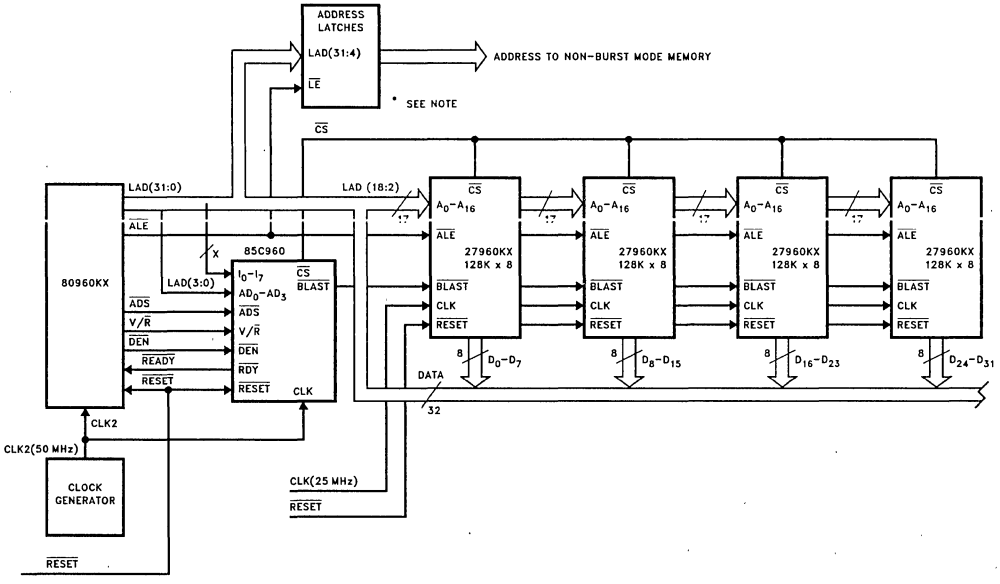
Overview

The following design offers a simple interface to the 80960KA/KB's bus.

A non-buffered 27960KX burst EPROM system is shown in Figure 4. Since the 27960KX is capable of driving a 120 pF load, large, non-buffered systems can be implemented by stacking up to 2 banks of 4 EPROMs, giving a memory size of 256K x 32. The input capacitive load seen on the address lines (due to the EPROM only) is 24 pF for a 128K x 32 system (shown) and 48 pF for a 256K x 32 system. The EPROM is specified at 4 pF for input capacitance and 12 pF typical for output capacitance. Larger systems can be implemented with buffers.

Chip Select Logic

High order address lines are decoded to provide $\overline{CS}$. Qualification with other signals is not required. The chip select logic can be implemented with standard asynchronous decoders, PAL's or PLD's (like Intel's 85C960).



NOTE:
27960KX does not require address latches

Figure 4. 128K x 32 Burst EPROM System

5

Waveforms

Figure 5 shows the timing waveforms of 27960KX reads in a 32-bit system.

$\overline{CS}$ setup time

$\overline{CS}$ setup time is the time between $\overline{CS}$ asserted and the first rising CLK edge of CLK (during the address cycle). Since a memory access begins on the first CLK rising edge after $\overline{CS}$ asserted, a minimum $\overline{CS}$ setup time of 5 ns (t_{SVCH}) at 25 MHz is required. With the 80960KA/KB's maximum valid address delay of 18 ns at 25 MHz, 13 ns remains for $\overline{CS}$ decoding logic.

$\overline{CS}$ Deassert between bursts

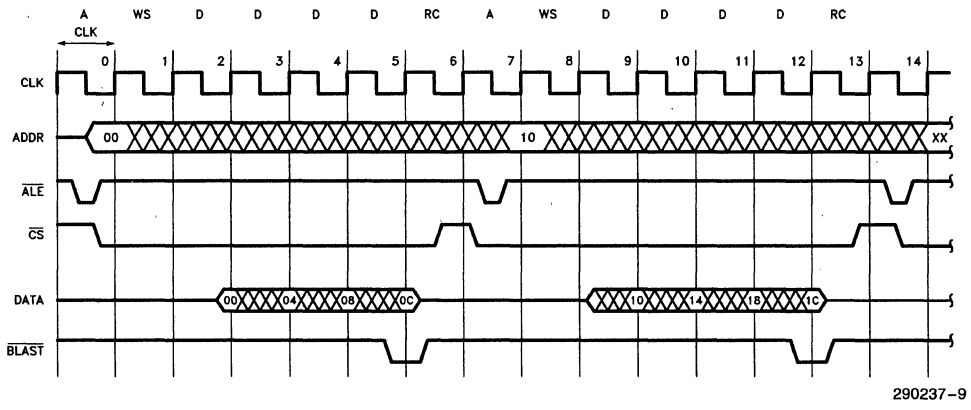
After every EPROM read (one to four words) $\overline{CS}$ must be deasserted.

Reset and $\overline{RESET}$

The 27960KX uses $\overline{RESET}$. The 80960 KA/KB RESET signal must be inverted for the 27960KX.

Clock Phase

The initial rising edge of CLK and CLK2 must be in phase with as small a skew as possible.



NOTES:
1. 1-0-0-0 Burst Read → 1 indicates the number of wait states to access the first word
   0's indicate the number of wait states for subsequent data words (0 in this case)
2. 27960KX latches addresses on the rising edge of ALE: it has an internal address generator which increments addresses for subsequent words of the burst.

Figure 5. Two Cycles of a 27960KX 1 Wait State, 4-Byte Read (1-0-0-0 Burst Read) in a 32-Bit System

27960KX DEVICE NAMES

The device names on the 27960KX were derived as mnemonics that correspond to the number of wait states and expected operating frequency for the device. For example, the 25 MHz, 2 wait state 27960KX is named 27960K2-25.

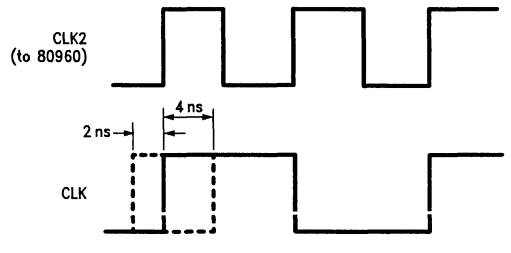
AC TIMING DERIVATIONS

The AC timings for the 27960KX were generated specifically to meet the requirements of the 80960KA/KB microprocessor. In each case the applicable 80960KA/KB clock frequency and AC timing were taken together with an address buffer delay (if needed) and a 4 ns positive clock skew or a 2 ns negative clock skew (see Figure 6A) guardband to generate the 27960KX AC timing. Examples of clock generation circuits (like Figures 6B and 6C) with detailed analysis and PAL equations will be made available in a separate Applications note. Worst case timings were always assumed. The example below shows how the 27960K1-20 $tavc_0h$ timing was derived.

@20 MHz the clock cycle is ~50 ns.
t_6 of the 80960KA/KB is 2–20 ns.
4 ns clock skew guardband.

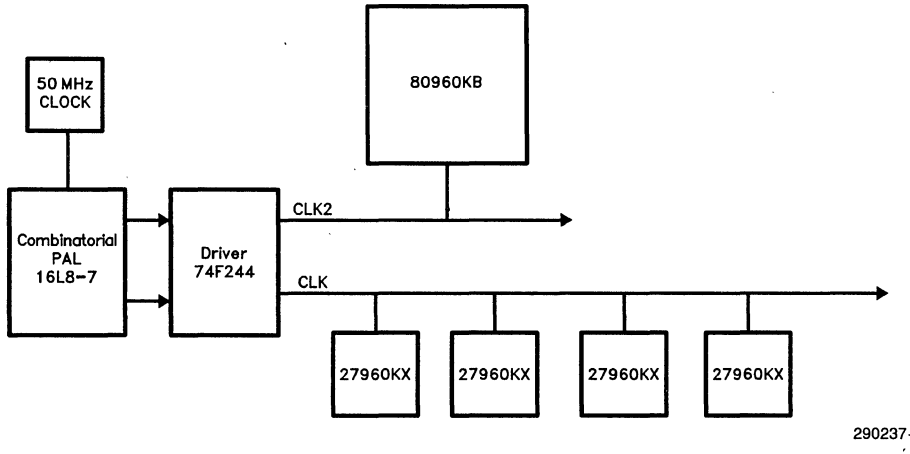
$$27960K1\text{-}20\ tavc_0h = 50\ ns - 20\ ns - 4\ ns = 26\ ns$$

On timings such as this, where the EPROM is faster than the microprocessor, we specified the EPROM's timing leaving the excess time as system guardband.



NOTE:
The 27960KX allows a positive clock skew (CLK2 leading CLK) of up to 4 ns and a negative clock skew (CLK2 lagging CLK) of up to 2 ns. The larger positive clock skew takes into account longer trace lengths and heavier loading on the 1x clock trace.

Figure 6A. Definition of Positive and Negative Clock Skew



NOTE:
CLK and CLK2 are generated by the same PAL. This minimizes skew between CLK and CLK2. Both PAL outputs are fed to a 74F244 driver. The EPROMs should be as close to the clock driver as possible.

Figure 6B. Example Clock Circuit with Minimum Skew

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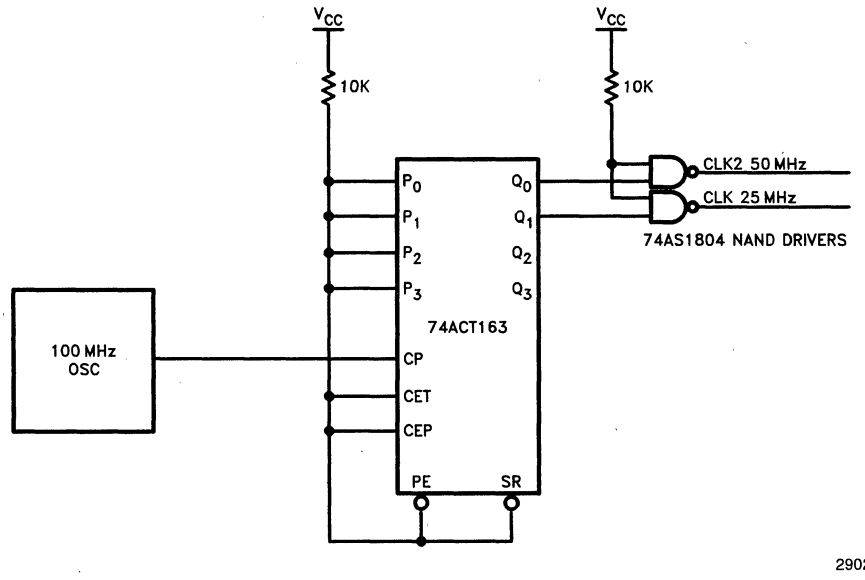


NOTE:
This clock generation circuit uses a 100 MHz oscillator. The EPROMs should be as close to the NAND drivers as possible.

Figure 6C. Example Clock Circuit Using a 100 MHz Oscillator

Decoders are needed for the systems address (chip select) decoding. For the 27960KX's timings we assumed a 5–10 ns chip select decoder for 16 MHz and 20 MHz frequencies and a 5–9 ns decoder for 25 MHz systems. The example below shows how the 27960K2-25 tsvch timing was derived.

@25 MHz the clock cycle is ~40 ns.
t_6 of the 80960KA/KB is 2–18 ns.
Decoder = 9 ns
4 ns clock skew guardband

27960K2-25 tsvch = 40 ns − 18 ns − 9 ns − 4 ns
= 9 ns

SYSTEM BUFFERING CONSIDERATIONS

For many large system applications buffering may be required between the microprocessor and memory devices. The 20 MHz − 2 WS and 16 MHz 27960KX AC timings take this into account. For applications at these frequencies not requiring buffering these devices will provide an additional 5–10 ns of system guardband.

The list below shows the buffers used in generating these timings:

	Input Buffer	Output Buffer
20 MHz	9 ns	5 ns
16 MHz	10 ns	7 ns

The 20 MHz buffers are slightly faster in keeping with the increased sensitivity for higher performance. We chose the above buffers because of their wide availability. Significantly faster buffers are available for applications requiring them. The example below shows tchqv for the 27960K2-20.

@20 MHz the clock cycle is ~50 ns.
t_{10} of the 80960KA/KB is 3 ns.
Output buffer for 20 MHz = 7 ns.
4 ns clock skew guardband

27960K2-20 tchqv = 50 ns − 7 ns − 3 ns − 4 ns
= 36 ns

ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature . . . . . 0°C to +70°C(8)

Case Temperature under Bias . . −10°C to +80°C(8)

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages . . . . . −0.6V to +6.5V(4) with Respect to Ground

Voltage on A_9 . . . . . −0.6V to +13.0V(4) with Respect to Ground

V_{PP} Supply Voltage . . . . . −0.6V to +14.0V(4) with Respect to Ground

V_{CC} Supply Voltage . . . . . −0.6V to +7.0V(4) with Respect to Ground

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS: READ OPERATION

0°C < T_A < +70°C, V_{CC} = 5V ± 10%, TTL Inputs

Symbol	Parameter		Notes	Min	Max	Unit	Test Condition
I_{LI}	Input Load Current				1	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				10	μA	V_{OUT} = 5.5V
I_{PP}	V_{PP} Load Current Read				10	μA	V_{PP} = 0 to V_{CC}, $\overline{PGM}$ = V_{IH}
I_{SB}	V_{CC} Standby	Switching	2		45	mA	$\overline{CS}$ = V_{IH}, f = 25 MHz
		Stable	2		30	mA	$\overline{CS}$ = V_{IH}
I_{CC}	V_{CC} Active Current		1, 3, 7		125	mA	$\overline{CS}$ = V_{IL}, f = 25 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage		4	−0.5	0.8	V	
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		5	V_{CC}−0.8		V	I_{OH} = −100 μA
			5	2.4		V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit		6		100	mA	

NOTES:
1. Maximum current is with outputs unloaded.
2. I_{CC} standby current assumes no output loading, i.e., I_{OH} = I_{OL} = 0 mA.
3. I_{CC} is the sum of current through V_{CC3} + V_{CC4} and does not include the current through V_{CC1} and V_{CC2}. (V_{CC1} and V_{CC2} supply power to the output drivers. V_{CC3} and V_{CC4} supply power to the rest of the device.)
4. Minimum DC voltage on input and output pins is −0.5V. During transitions, this level may undershoot to −2.0V for periods less than 20 ns.
5. Maximum DC voltage on input and output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
6. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
7. I_{CC} max measured with a 0.11 μF capacitor between V_{CC} and V_{SS}.
8. This specification defines commercial product operating temperatures.

5

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name, e.g., (CLK, $\overline{ALE}$, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated for the fourth character. The list below shows character representations.

A:	Address	R:	$\overline{Reset}$
B:	$\overline{BLAST}$	Q:	Data
C:	Clock	S:	$\overline{CS}$
H:	Logic High Level	t:	Time
L:	$\overline{ALE}$/Logic Low Level	V:	Valid
P:	V_{PP} Programming Voltage	Z:	Tri-state level
X:	No longer a valid "driven" logic level		

AC CHARACTERISTICS: READ OPERATION $0\,°C < T_A < +70°C$, $V_{CC} = 5V \pm 10\%$

Versions				27960K2-25		27960K1-20		27960K2-20		27960K1-16		Unit
				25 MHz 2 Wait States		20 MHz 1 Wait State		20 MHz 2 Wait States		16 MHz 1 Wait State		
No	Symbol	Characteristic	Notes	Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{AVC_0H}	Address Valid to CLK High	CLK 0	12		18		10		15		ns
2	t_{AVLH}	Address Valid to $\overline{ALE}$ High		10		10		10		10		ns
3	t_{LLLH}	$\overline{ALE}$ Low to $\overline{ALE}$ High		12		12		12		12		ns
4	t_{LHAX}	$\overline{ALE}$ High to Address Invalid		8		8		8		8		ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High	1, 5	5		8		7		8		ns
6	t_{C_NHSX}	CLK High to $\overline{CS}$ Invalid	2	0		0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		33		43		38		45	ns
8	t_{CHQX}	CLK High to Data Invalid		7		7		7		7		ns
9	t_{CHQZ}	CLK High to Data High-Z	6		30		35		35		35	ns
10	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		15		15		15		15		ns
11	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	3	5	35	5	45	5	45	5	45	ns

NOTES:
1. Valid signal level is meant to be either a logic high or logic low.
2. t_{C_NHSX}—The subscript N represents the number of wait states for this parameter. $\overline{CS}$ can be de-asserted (high) after the number of wait states (N) has expired. The EPROM will continue to burst out data for the current cycle.
3. $\overline{BLAST}$ must be returned high before the next rising clock edge.
4. The sum of t_{CHQV} + t_{AVCH} + NCLK will not equal actual t_{AVQV} if independent test conditions are used to obtain t_{AVCH} and t_{CHQV} (N = number of wait states).
5. $\overline{CS}$ must be deasserted after every burst read (see Figure 7).
6. Sampled, not 100% tested. The transition is measured ±500 mV from steady state voltage.
7. For capacitive loads above 120 pF, t_{CHQV} can be derated by 1 ns/20 pF.

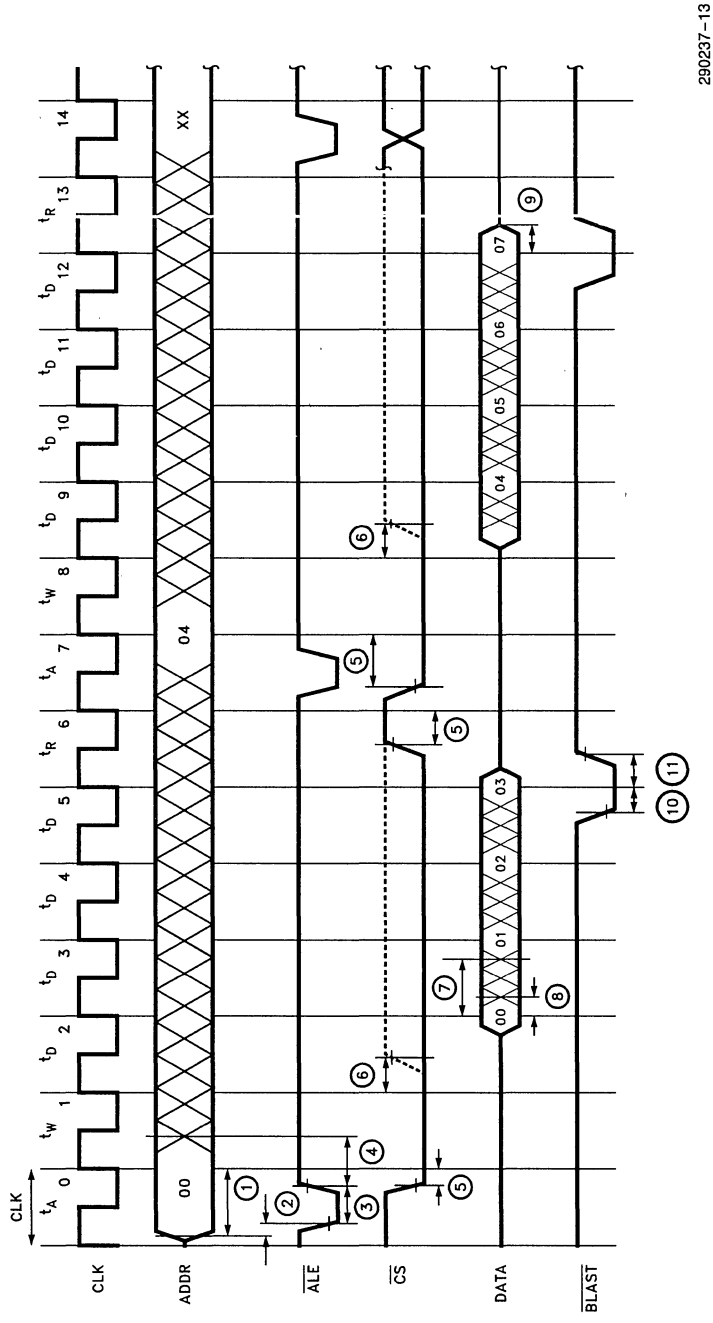


Figure 7. 27960KX 1 WS AC Read Waveforms

AC CONDITIONS OF TEST

Input Rise and Fall Times
(10% to 90%) ..... 4 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level 1.5V
Output Timing Reference Level ..... 0.8V and 2.0V

Table 2. Mode Table

MODE	$\overline{CS}$	$\overline{PGM}$	$\overline{BLAST}$	$\overline{ALE}$	$\overline{RESET}$	A_9	V_{PP}	V_{CC}	OUTPUT
Read	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	X(4)	V_{CC}	V_{CC}	D_{OUT}
Standby (6)	V_{IH}	X	X	X	V_{IH}	X	V_{CC}(5)	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{IH}(2)	V_{IH}	X	(3)	(3)	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}	V_{IH}	X	(3)	(3)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{IH}	X	(3)	(3)	High Z
ID Byte 0: Manufacturer	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	89H
ID Byte 1: Part (27960)	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	E0H
ID Byte 2: KX	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	00B
ID Byte 3: 1 Wait-State 2 Wait-States	V_{IL}	V_{IH}	V_{IH}(1)	V_{IH}(2)	V_{IH}	V_{ID}(3)	V_{CC}	V_{CC}	01B 10B
Reset	X	X	X	X	V_{IL}	X	V_{CC}	V_{CC}	High Z

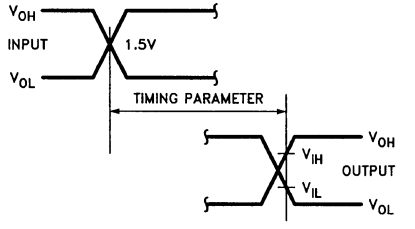
NOTES:
1. V_{IH} until data terminated at which time $\overline{BLAST}$ must go to V_{IL}.
2. Need to toggle from V_{IH} to V_{IL} to V_{IH} to latch address.
3. See DC Programming Characteristics for V_{CC}, V_{ID} and V_{PP} voltages.
4. X can be V_{IL} or V_{IH}.
5. $V_{PP} = V_{CC}$ to meet standby current specification. $V_{CC} > V_{PP} > V_{IL}$ will cause a slight increase in standby current.
6. The device must be in the idle state (by asserting $\overline{RESET}$ or using $\overline{BLAST}$) before going into standby.

CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	15	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	40	45	pF	V_{IN} = 0V

NOTE:
1. Sampled, not 100% tested

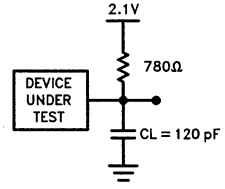
AC INPUT/OUTPUT REFERENCE WAVEFORMS



290237-14

AC test inputs are driven at 2.4V (V_{OH}) for a logic '1' and 0.45V (V_{OL}) for a logic '0'.
Input timing begins at 1.5V.
Output timing ends at V_{IH} (2.0V) and V_{IL} (0.8V)
Input Rise and fall times (10% to 90%) < 4.0 ns

AC TESTING LOAD CIRCUIT



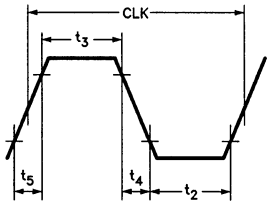
290237-15

For t_{CHQZ} C_L = 5 pF and R_L = 405Ω
C_L includes jig capacitance

CLOCK CHARACTERISTICS

Versions		25 MHz		20 MHz		16 MHz		Units
Symbol	Parameter	Min	Max	Min	Max	Min	Max	
CLK	Period	40		50		62.5		ns
T_5	Rise Time		10		10		10	ns
T_4	Fall Time		10		10		10	ns
T_2	Low Time	7		8		11		ns
T_3	High Time	7		8		11		ns
Max CLK Rise Time during Programming is 100 ns								

CLOCK WAVEFORM



290237-16

Program/Program Verify

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" can be programmed, both "1's" and "0's" can be present in the data word. Ultraviolet erasure is the only way to change "0's" to "1's".

Program mode is entered when V_{PP} is raised to 12.75V. Program/Verify operation is synchronous with the clock and can only be initiated following an idle state. Program and Program Verify take place in 3 clock cycles. In the first clock cycle, addresses and data are input and programming occurs. Program Verify follows in the second clock cycle and the third clock cycle terminates synchronous Program/Verify operation, returning the state machine to the idle state with outputs at high impedance.

As in the Read mode, A_2–A_{16} point to a four byte block in the memory array. During Programming the internal address increment circuitry is disabled and the programmer must supply A_0 and A_1 to point to an individual byte within the four byte block that is to be programmed. Only one byte is programmed in each 3 cycle program/Verify sequence.

Program Inhibit

Program Inhibit mode allows parallel programming and verification of multiple devices with different data. With V_{PP} at 12.75V, a Program/Verify sequence is initiated for any device that receives a valid $\overline{ALE}$ pulse and rising clock edge while $\overline{CS}$ is asserted. A $\overline{PGM}$ pulse programs data in the first cycle of the sequence and data for Program Verify is output in the second cycle. The Program/Verify sequence is inhibited on any devices for which $\overline{CS}$ is not asserted during the first ($\overline{ALE}$) cycle. Data will not be programmed and the outputs will remain in their high impedance state.

int$_e$ligent Identifier™ Mode

The device's manufacturer, product type, and configuration are stored in a four byte block that can be accessed by using the int$_e$ligent Identifier™ mode. The programmer can verify the device identifier and choose the programming algorithm that corresponds to the Intel 27960KX. The int$_e$ligent Identifier can also be used to verify that the product is configured with the desired Read mode options for wait states.

Int$_e$ligent Identifier mode is entered when A_9 (pin 32) is raised to its high voltage (V_H) level. The internal state machine is then set for int$_e$ligent Identifier Read operation. Reading the Identifier is similar to a Read operation on a one wait state configured product. Up to four bytes can be read in a single burst access. int$_e$ligent Identifier read is terminated by a synchronous $\overline{BLAST}$ input, returning the state machine to the idle state with outputs at high impedance.

The four byte block code for the int$_e$ligent Identifier code is located at address 00H through 03H and is encoded as follows:

MEANING	(A_1, A_0)	DATA
Intel ID	Byte 00	89h
27960	Byte 01	E0h
KX	Byte 10	00b
1 wait state	Byte 11	01b
2 wait states	Byte 11	10b

RESET MODE

Due to the synchronous nature of the 27960KX, the various operating modes must be initiated from a known idle state. During normal operation, the internal state machine returns to an idle state at the termination of a bus access (after $\overline{BLAST}$ is asserted).

During initial device power up, the state machine is in an indeterminant state. The reset mode is provided to force operation in to the idle state. Reset mode is entered when the $\overline{RESET}$ pin is asserted. Output pins are asynchronously set to the high impedance state and address latches are put into the flow through mode. A reset is successfully completed and the state machine set in an idle state in the cycle after $\overline{RESET}$ has been asserted for a minimum of 10 clock cycles and deasserted for five clock cycles.

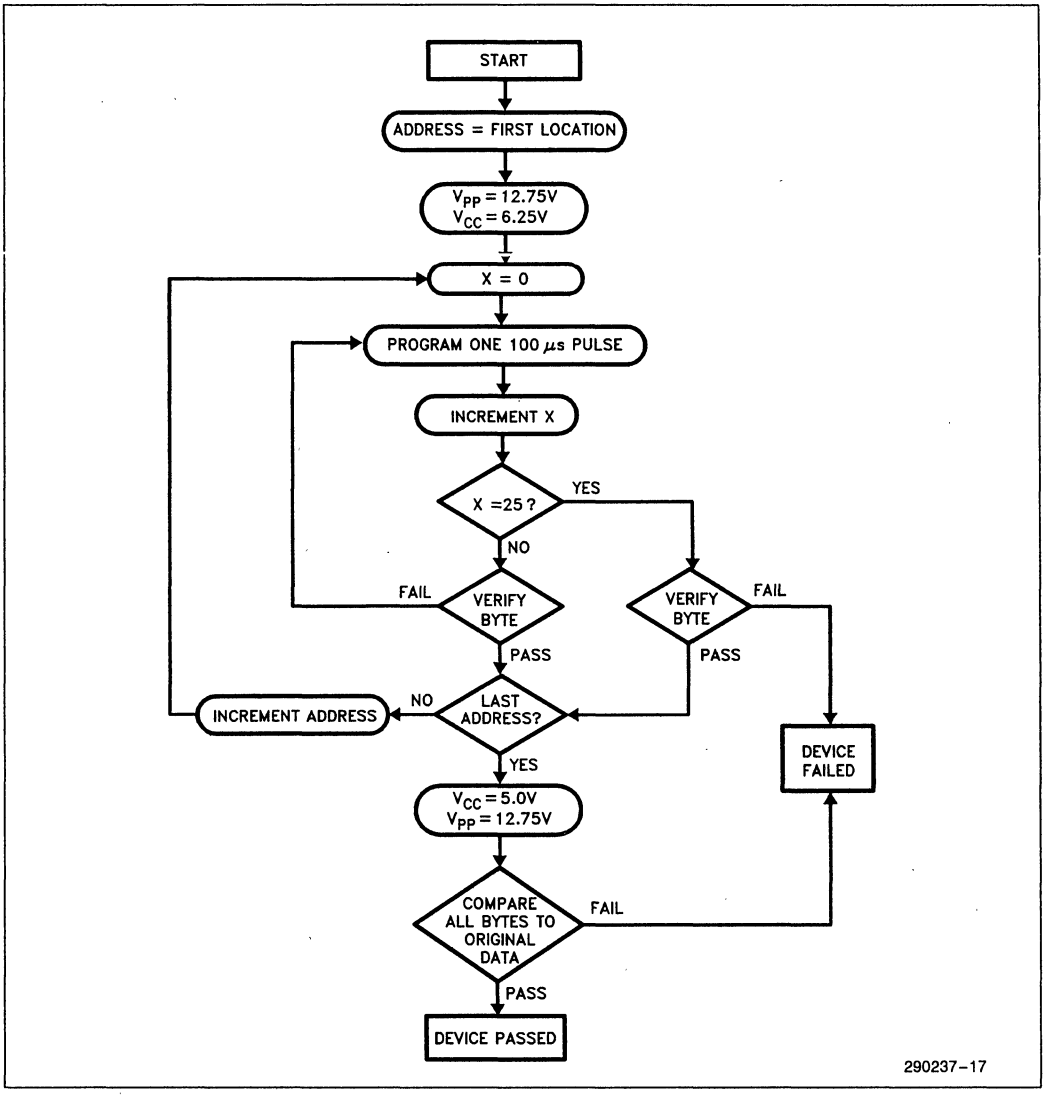


Figure 8. Quick-Pulse Programming™ Algorithm

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ERASURE CHARACTERISTICS (FOR WINDOWED DEVICES)

Exposure to light of wavelength shorter than 4000 Angstroms begins erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000 Angstrom range. Constant exposure to room-level fluorescent light can erase the EPROM array in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537 Angstrom ultraviolet light. The minimum integrated erasure time using a 12000 fW/cm2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm2 (1 week @ 12000 fW/cm2). High intensity UV light exposure for longer periods can cause permanent damage.

QUICK-PULSE PROGRAMMING ALGORITHM

The Quick-Pulse Programming algorithm programs Intel's 27960KX. Developed to substantially reduce programming throughput time, this algorithm allows optimized equipment to program a 27960KX in under 17 seconds. Actual programming time depends on the programmer used.

The Quick-Pulse Programming algorithm uses a 100 μs pulse followed by a byte verfication to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100μs pulses fail to program a byte. Figure 8 shows the 27960KX Quick-Pulse Programming algorithm flowchart.

The entire program-pulse, byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. The programming equipment must establish V_{CC} before applying voltages to any other pins. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V and V_{PP} = 12.75V.

D.C. PROGRAMMING CHARACTERISTICS T_A = 25°C ±5°C

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
I_{LI}	Input Load Current			10	μA	$V_{IN} = V_{IH}$ or V_{IL}
I_{CC}	V_{CC} Program Current	1		125	mA	$\overline{CS} = V_{IL}$
I_{PP}	V_{PP} Program Current	1		50	mA	$\overline{CS} = V_{IL}$
V_{IL}	Input Low Voltage		−0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage (Verify)			0.40	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage (Verify)		V_{CC}−0.8		V	I_{OH} = −400 μA
V_{ID}	A_9 inteligent Identifier Voltage		11.5	12.5	V	
V_{CC}	Supply Voltage (Program)	2	6.0	6.5	V	
V_{PP}	Program Voltage	2	12.5	13.0	V	

NOTES:
1. The maximum current value is with outputs unloaded.
2. V_{CC} must be applied simultaneously or before V_{PP} and remove simultaneously or after V_{PP}.
3. During programming clock levels are V_{IH} and V_{IL}.

AC PROGRAMMING, RESET AND ID CHARACTERISTICS $0°C < T_A < +70°C$

No	Symbol	Parameter	Notes	Min	Max	Units
1	t_{AVPL}	Address Valid to $\overline{PGM}$ Low		2		μs
2	t_{CHAX}	CLK High to Address Invalid		50		ns
3	t_{LLCH}	$\overline{ALE}$ Low to CLK High	1	50		ns
4	t_{CHLH}	CLK High to $\overline{ALE}$ High	2	50		ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High		50		ns
6	t_{CHSX}	CLK High to $\overline{CS}$ Invalid	3			ns
7	t_{CHQV}	CLK High to D_{OUT} Valid			100	ns
8	t_{CHQX}	CLK High to D_{OUT} Invalid		0		ns
9	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		50		ns
10	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	4	50		ns
11	t_{QVPL}	DATA Valid to $\overline{PGM}$ Low		2		μs
12	t_{PLPH}	$\overline{PGM}$ Program Pulse Width		95	105	μs
13	t_{PHQX}	$\overline{PGM}$ High to D_{IN} Invalid		2		μs
14	t_{CLPL}	CLK Low to $\overline{PGM}$ Low		50		ns
15	t_{QZCH}	D_{IN} in Tri-State to CLK High		2		μs
16	t_{VCS}	V_{CC} Program Voltage to CLK High	7	2		μs
17	t_{VPS}	V_{PP} Program Voltage to CLK High	7	2		μs
18	t_{A_9HCH}	A_9 V_{ID} Voltage to CLK High		2		μs
19	t_{CHA_9X}	CLK High to A9 not V_{ID} Voltage		2		μs
20	t_{RVCH}	$\overline{RESET}$ Valid to CLK High	6	50		ns
21	t_{CHCL}	CLK High to CLK Low	5	100		ns
22	t_{CLCH}	CLK Low to CLK High	5	100		ns

NOTES:
1. If $\overline{CS}$ is low, $\overline{ALE}$ can go low no sooner than the falling edge of the previous CLK.
2. $\overline{ALE}$ must return high prior to the next rising edge of clock.
3. $\overline{CS}$ must remain low until after the rising edge CLK1.
4. $\overline{BLAST}$ must return high prior to the next rising edge of CLK.
5. Max CLK rise/fall time is 100 ns.
6. $\overline{RESET}$ must be held low for 10 cycles and high for 5 cycles before performing a read.
7. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

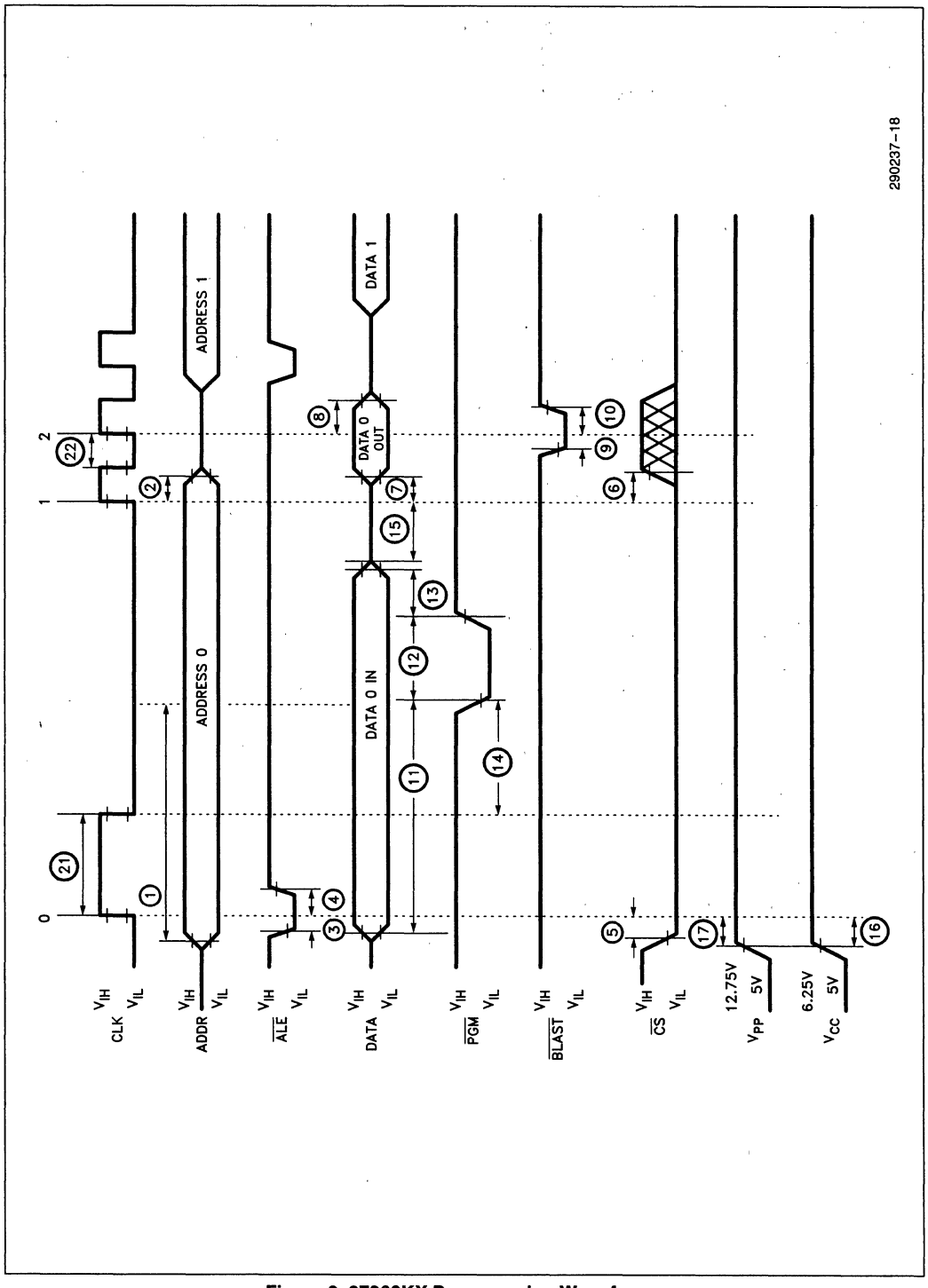

Figure 9. 27960KX Programming Waveforms

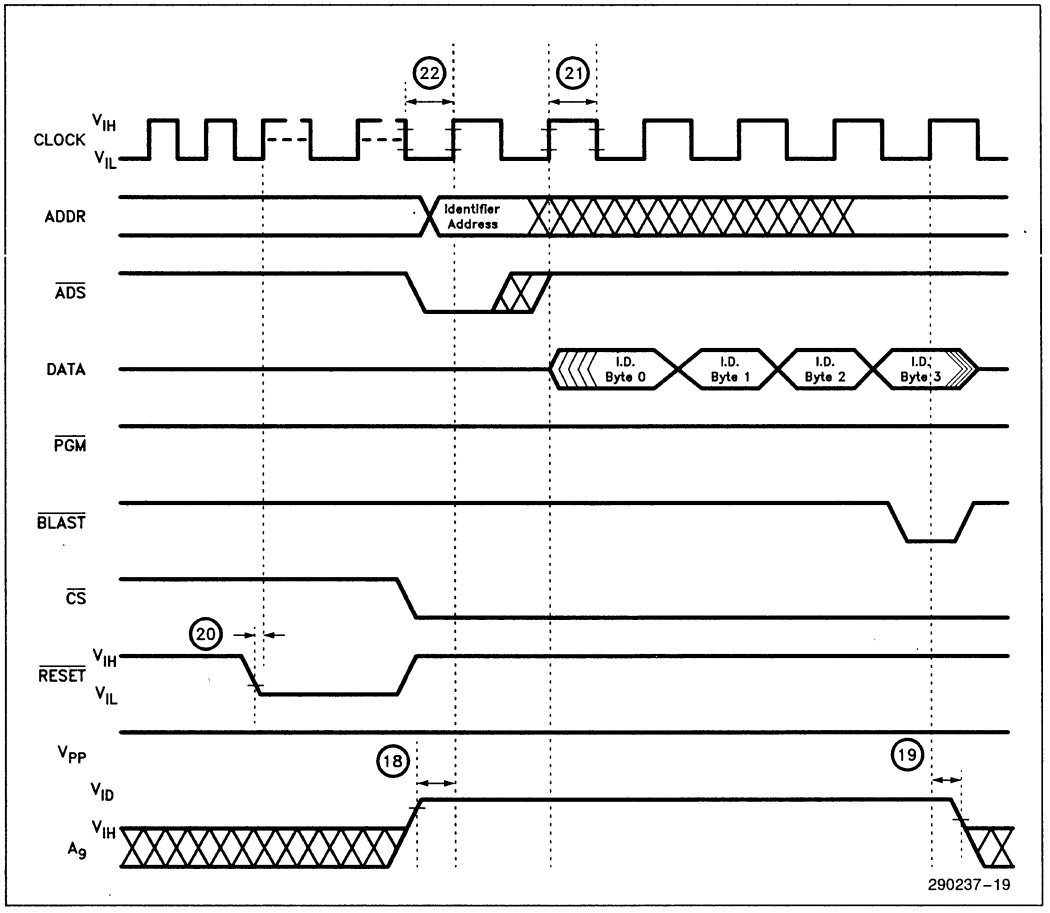

Figure 10. 27960KX RESET and ID Waveforms

intel®

APPLICATION NOTE

AP-329

November 1990

68030/27960CX Burst EPROM Interface

DEAN PARMAR
SENIOR APPLICATIONS ENGINEER
PROGRAMMABLE MEMORY OPERATION

Order Number: 292064-001

68030/27960CX BURST EPROM INTERFACE

CONTENTS

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INTRODUCTION

This application note describes the design of a circuit to interface the 27960CX burst EPROM to Motorola's 68030 microprocessors (μP). The 68030 μP is capable of burst mode operation, accessing a maximum of four long words (long word = 32 bits) during a burst cycle.

A 2-0-0-0 burst operation (2 wait states for the first word access and zero wait state for subsequent accesses) is possible at 25 MHz using the 27960C2-25 burst EPROM. At 33 MHz, a 3-0-0-0 operation is possible using the 27960C2-33 burst EPROM. This memory interface monitors control signals from the μP, provides handshake logic for the μP and generates ADS and $\overline{\text{BLAST}}$ signals for the EPROMs. It also monitors cache burst request ($\overline{\text{CBREQ}}$) and cache inhibit ($\overline{\text{CIIN}}$) signals from the μP, and generates $\overline{\text{BLAST}}$ as appropriate.

Two designs are considered for this interface, a 33-MHz system and a 25/20 MHz system. The 33-MHz interface can be implemented with a 16R4-7 PAL, four 74F374 latches and a D-type flip/flop. The latches are required because the 68030 latches data on the falling edge of the clock, while the 27960 provides data on the rising edge of clock. The latches provide plenty of setup and hold time. The 25/20 MHz interface can be implemented with a 16R4-7 PAL and a couple of D-type flip/flops, but requires a delayed clock for the PAL and EPROMs. Because the clock is delayed no latches are required.

1.0 SIGNAL DEFINITIONS

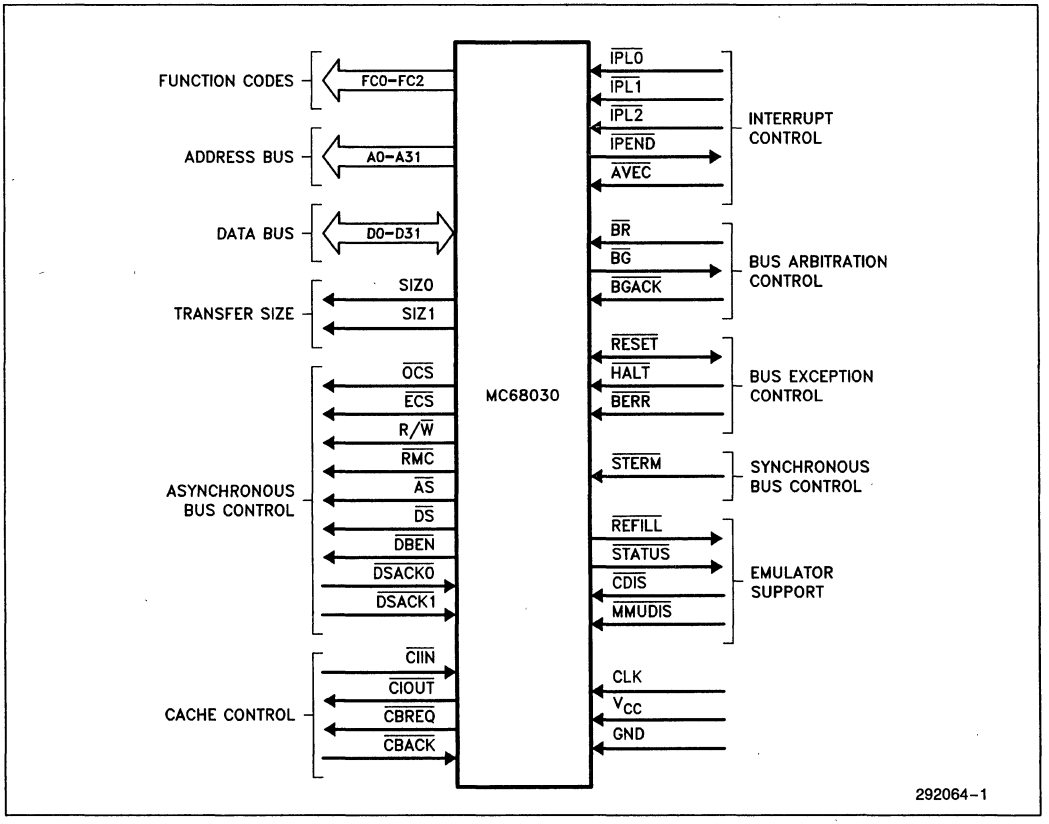


Figure 1. MC68030 Functional Signal Groups

1.1 68030 Signals

This section describes 68030 μP signals which are relevant to this interface.

1.1.1 $\overline{ECS}$ (Output)

Provides an indication that a bus cycle is beginning. The external cycle start ($\overline{ECS}$) signal is the earliest indication that the μP is initiating a bus cycle. The MC68030 initiates a bus cycle by driving the address, size, function code, cache inhibit-out, and read/write outputs and asserting $\overline{ECS}$.

1.1.2 ADDRESS BUS

The address bus signals (A0–A31) define the address of the byte (or the significant byte) to be transferred during a bus cycle. The μP places the address on the bus at the beginning of a bus cycle. The address is valid while $\overline{AS}$ is asserted.

1.1.3 $\overline{AS}$ (Output)

The address strobe ($\overline{AS}$) is a timing signal that indicates the validity of an address on the address bus and of many control signals. It is asserted one half clock after the beginning of a bus cycle.

1.1.4 DATA BUS

The data bus signals (D0–D31) run on a bi-directional, non-multiplexed, parallel bus that contains the data being transferred to or from the μP. A read or write operation may transfer 8, 16, 24 or 32 bits of data (one, two, three or four bytes) in one bus cycle. During a read cycle the data is latched by the μP on the last falling edge of the clock for that bus cycle.

1.1.5 $\overline{DS}$ (Output)

The data strobe ($\overline{DS}$) is a timing signal that applies to the data bus. For a read cycle the μP asserts $\overline{DS}$ to signal the external device to place data on the bus. It is asserted at the same time as $\overline{AS}$ during a read cycle. For a write cycle $\overline{DS}$ signals to the external device that the data to be written is valid. The μP asserts $\overline{DS}$ one full clock cycle after the assertion of $\overline{AS}$ during a write cycle.

1.1.6 $\overline{DBEN}$ (Output)

The data buffer enable signal ($\overline{DBEN}$) can be used to enable external data buffers while data is present on the data bus. During a read operation $\overline{DBEN}$ is asserted one clock cycle after the beginning of the bus cycle, and is negated as $\overline{DS}$ is negated. In a write operation, $\overline{DBEN}$ is asserted at the time $\overline{AS}$ is asserted, and is held active for the duration of the cycle. $\overline{DBEN}$ timings may prevent the use of a synchronous system using two-clock bus cycles.

1.1.7 $\overline{STERM}$ (Input)

This input is a bus handshake signal indicating that the addressed port size is 32 bits and that data is to be latched on the next falling clock edge for a read cycle. This signal applies only to synchronous operation. For synchronous bus cycles, external devices assert the synchronous termination signal ($\overline{STERM}$) as part of the bus protocol. During a read cycle, the assertion of $\overline{STERM}$ causes the μP to latch the data. During a write cycle, it indicates that the external device has successfully stored the data. In either case, it terminates the cycle, and indicates that the transfer was made to a 32-bit port.

1.1.8 $\overline{CBREQ}$ (Output)

This three-state output signal requests a burst mode operation to fill a line in the instruction or data cache.

1.1.9 $\overline{CBACK}$ (Input)

This input signal indicates that the accessed device can operate in the burst mode, and can supply at least one more long word for the instruction or data cache.

1.1.10 $\overline{CIIN}$ (Input)

This input signal prevents data from being loaded into the MC68030 instruction and data caches. It is a synchronous input signal and is interpreted on a bus-cycle-by-bus-cycle basis. $\overline{CIIN}$ is ignored during all write cycles.

1.2 27960 EPROM Control Signals

1.2.1 $\overline{ADS}$: ADDRESS STROBE

Indicates the start of a new bus access. It is active low in the first clock cycle of a bus access.

1.2.2 $\overline{BLAST}$: BURST LAST

Terminates a concurrent burst data cycle at the rising edge of CLK. Must be asserted by the fourth data word.

1.2.3 $\overline{CS}$: CHIP SELECT

Master device enable. When asserted (active low) data can be written to and read from the device. In read mode, $\overline{CS}$, enables the state machine and the I/O circuitry. A memory access begins on the first rising edge of clock after $\overline{ADS}$ and $\overline{CS}$ are asserted. $\overline{CS}$ can be de-asserted after the number of wait-states, N, has expired, and the EPROM will continue to burst out data for the current cycle. If $\overline{CS}$ is de-asserted during the wait-state period the burst access will be aborted.

2.0 INTERFACE REQUIREMENTS

The interface logic is designed to work in burst mode, with the synchronous termination signal, $\overline{STERM}$, as the handshake for the μP indicating EPROM readiness for a burst transfer. The interface logic will monitor control signals from the μP, i.e., $\overline{ECS}$, $\overline{AS}$, $\overline{DBEN}$ and $\overline{CBREQ}$ and generate $\overline{ADS}$ and $\overline{BLAST}$ signals for the 27960 and $\overline{STERM}$ and $\overline{CBACK}$ signals for the μP. $\overline{STERM}$ will be asserted by the interface logic after the number of wait states, N, has expired. The logic will also monitor $\overline{CBREQ}$ and $\overline{CIIN}$ signals and generate $\overline{BLAST}$ as appropriate.

Figures 2 and 3 show schematics of the 68030/27960 Burst EPROM interfaces.

3.0 CIRCUIT DESCRIPTION

This section describes the burst mode operation of the 68030 μP followed by a brief description of the interface circuits (Figures 2 and 3). Figure 2 shows a 33 MHz design which allows 3-0-0-0 burst operation; Figure 3 shows a 25/20 MHz design which allows a 2-0-0-0 and a 1-0-0-0 burst operation at 25 MHz and 20 MHz respectively.

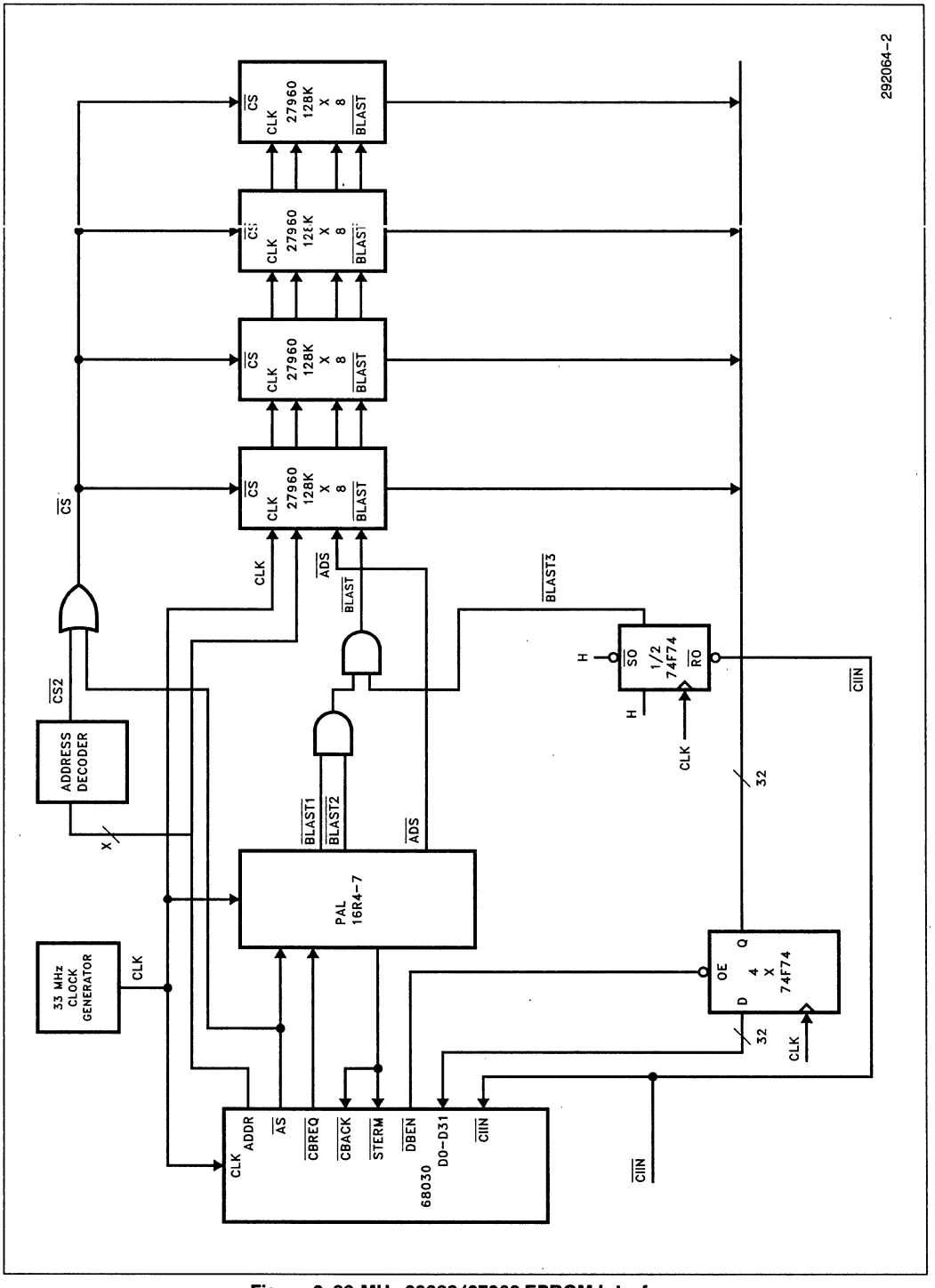


Figure 2. 33-MHz 68030/27960 EPROM Interface

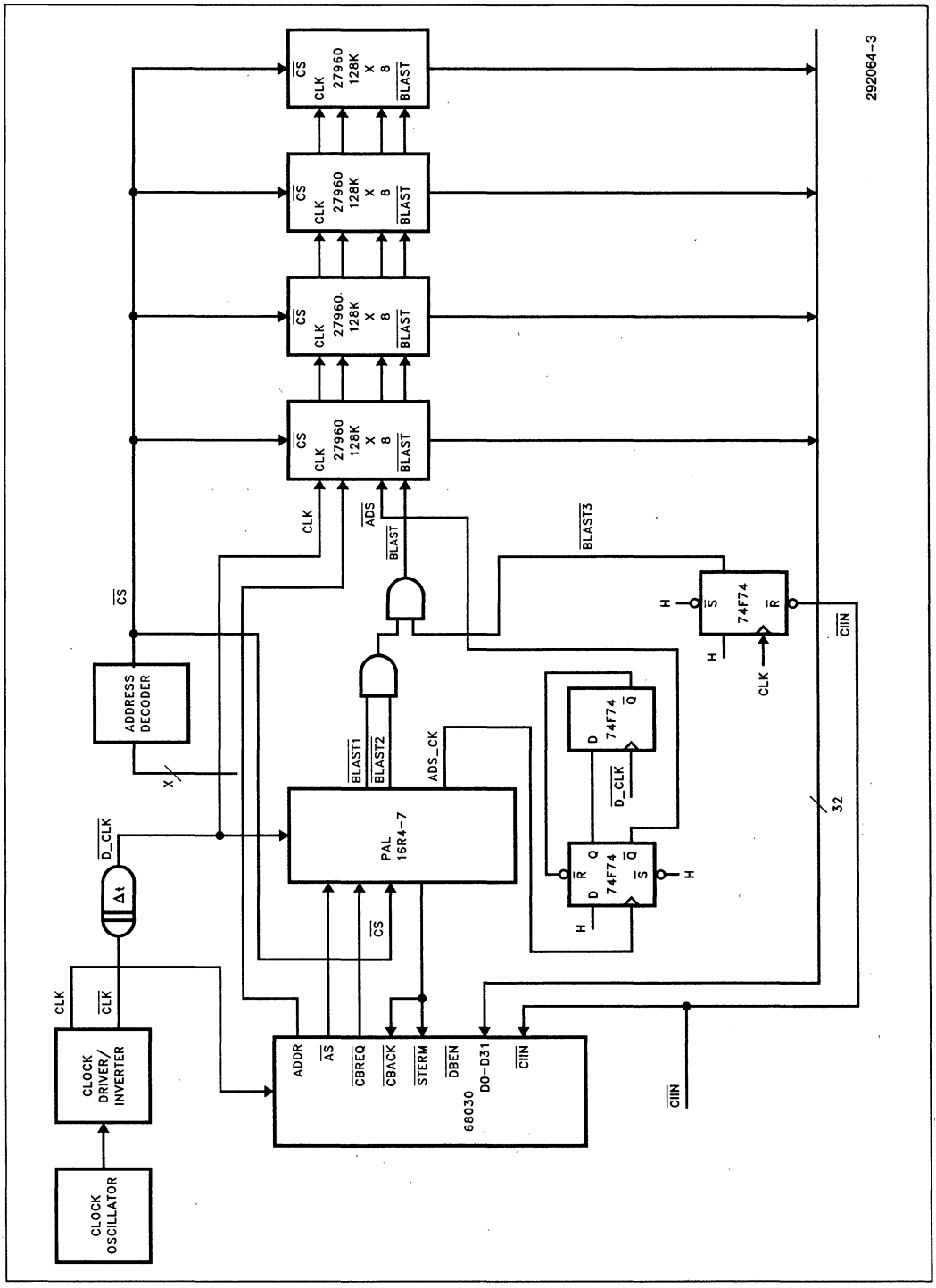


Figure 3. 25/20-MHz 68030/27960 EPROM Interface

The circuits are designed to operate in a 32-bit burst mode. Four long words (long word = 32 bits) may be transferred during a single burst operation. Figure 4 shows a burst operation cycle.

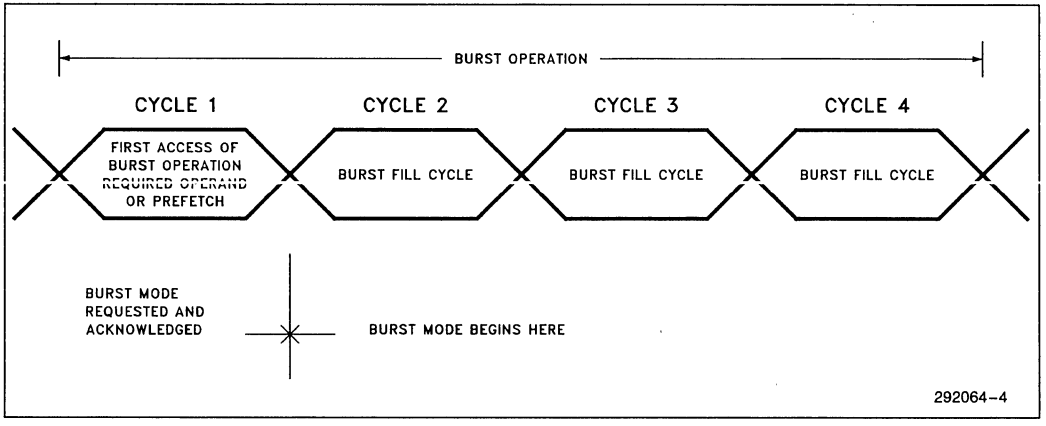


Figure 4. Burst Operation Cycles

The circuits also allow address wrap around so that the entire four long words in the cache line can be filled in a single burst operation regardless of the initial address. Figure 5 shows a burst filling wrap-around example.

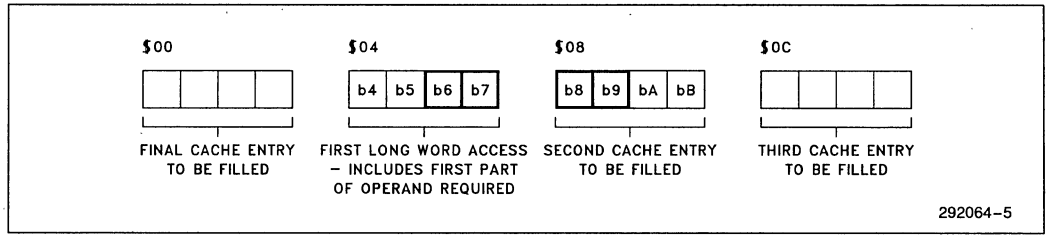


Figure 5. Burst Filling Wrap-Around Example

The initial cycle is a long word access from address $06. Because the interface logic returns $\overline{\text{CBACK}}$ and $\overline{\text{STERM}}$ (signaling a 32-bit port), the entire long word at base address $04 is transferred. Since the initial address is $06 when $\overline{\text{CBREQ}}$ is asserted, the next entry to be burst filled into the cache should correspond to address $08, then $0C, and last, $00.

The 68030 μP does not assert $\overline{\text{CBREQ}}$ during the first portion of a misaligned access if the remainder of the access does not correspond to the same cache line. Figure 6 shows an example in which the first portion of a misaligned access is at address $0F. With a 32-bit port the first access corresponds to the cache entry at address $0C, which is filled using a single-entry load operation. The second access at address $10 (corresponding to the second cache line) requests a burst fill and the processor asserts $\overline{\text{CBREQ}}$. During this burst operation long words $10, $14, $18 and $1C are all filled, and in that order.

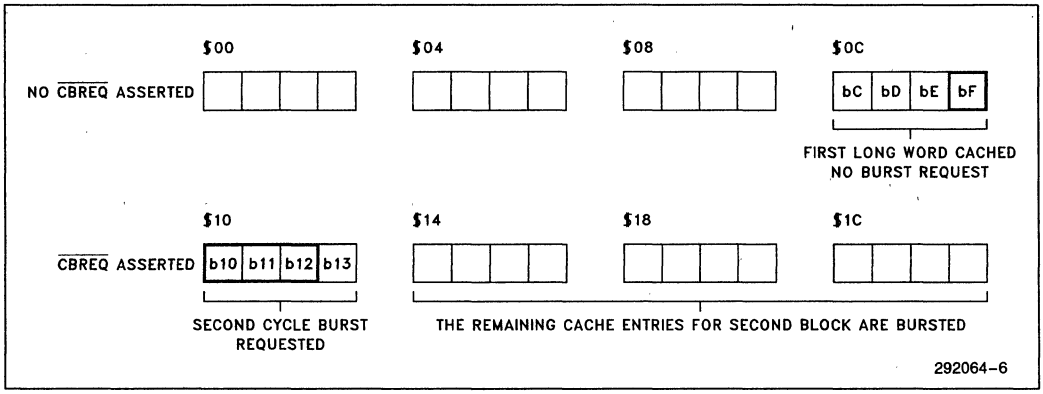


Figure 6. Deferred Burst Filling Example

The μP does not assert $\overline{\text{CBREQ}}$ if the cycle is for the first access of an operand that spans two cache lines (crosses a modulo 16 boundary).

3.1 $\overline{\text{ADS}}$ Generation

Figure 7 shows the timing of $\overline{\text{ADS}}$ for the 33-MHz design of Figure 2. A 4-bit counter is implemented in the PAL which is used for timing of $\overline{\text{ADS}}$, $\overline{\text{STERM}}$, $\overline{\text{CBACK}}$, and $\overline{\text{BLAST}}$. Assertion of $\overline{\text{AS}}$ enables the 4-bit counter. $\overline{\text{ADS}}$ is asserted following Count 1 (CNT1), and de-asserted at Count 2 (CNT2).

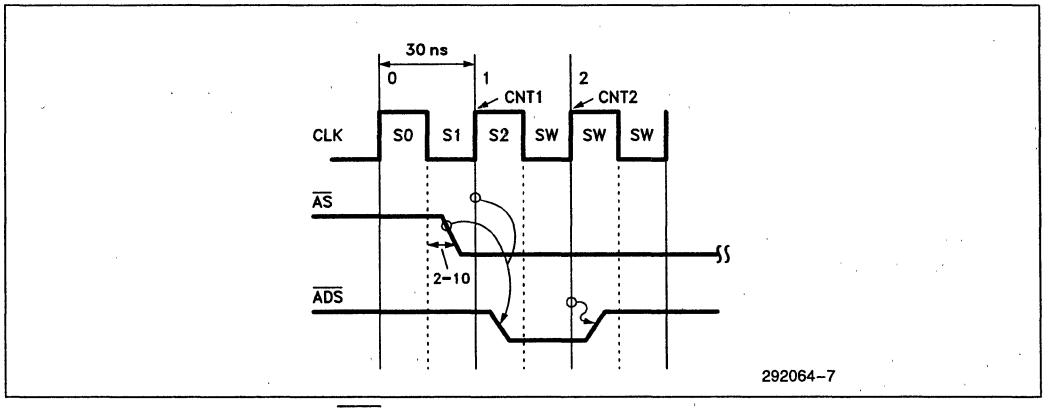


Figure 7. $\overline{\text{ADS}}$ Generation for 33-MHz Circuit of Figure 2

For the 25/20-MHz system (Figure 3) $\overline{ADS}$ is referenced to $\overline{D\_CLK}$ (Figure 8A). $\overline{D\_CLK}$ is the inverted and delayed version of CLK. $\overline{D\_CLK}$ is used for generating $\overline{ADS}$, $\overline{STERM}$, $\overline{CBACK}$ and $\overline{BLAST}$. For this design a 3-bit counter is implemented in the PAL. $\overline{ADS}$ is asserted when ADS_CK clocks the first flip/flop. ADS_CK makes the low to high transition when both $\overline{AS}$ and $\overline{CS}$ are valid. The next rising edge of $\overline{D\_CLK}$ resets the first flip/flop, and $\overline{ADS}$ is pulled high. With this implementation data latches are not required, and a 2-0-0-0 or a 1-0-0-0 burst operation is possible at 25 MHz and 20 MHz respectively. This design buys an extra wait state as shown in the timing diagram of Figure 10. If the use of delay line is not preferred, then the design shown in Figure 2 can be used to provide 3-0-0-0 and 2-0-0-0 performance at 25 MHz and 20 MHz respectively.

3.2 $\overline{STERM}$ Generation

3.2.1 33 MHz DESIGN

$\overline{STERM}$ is asserted after the number of wait states, N, has expired (N is the number of wait states with respect to the EPROM). For the 33-MHz design, a 2 wait-state EPROM (27960C2-33) is used, which equates to a 3 wait state system performance. $\overline{STERM}$ is asserted on count 4 and de-asserted on count 8 (Figure 9).

3.2.2 25 MHz DESIGN

For the 25 MHz design, $\overline{STERM}$ is asserted on count 3 (reference to $\overline{D\_CLK}$) and de-asserted on count 7 (Figure 10).

3.3 $\overline{CBACK}$ Generation

The timing of $\overline{CBACK}$ is the same as $\overline{STERM}$.

3.4 $\overline{BLAST}$ Generation

$\overline{BLAST}$ is used to terminate a burst cycle. For a 4-word burst $\overline{BLAST}$ is asserted following the rising edge of CLK in the next to last clock cycle (Figures 9 and 10). It is also used to terminate a burst operation of less than 4 words. Assertion of $\overline{BLAST}$ during the wait-state period is ignored by the EPROM. There are three conditions for generation of $\overline{BLAST}$ (i.e., $\overline{BLAST1}$ through $\overline{BLAST3}$) which are AND gated to produce the $\overline{BLAST}$ signal for the EPROM:

3.4.1 $\overline{BLAST1}$: (Normal Burst End)

$\overline{BLAST1}$ is used to terminate a 4-word burst. For the 33-MHz design $\overline{BLAST1}$ is asserted on count 7 and de-asserted on count 8 (Figure 9). For the 25-MHz design, $\overline{BLAST1}$ is asserted on count 6 of $\overline{D\_CLK}$ and de-asserted on count 7 of $\overline{D\_CLK}$ (Figure 10).

3.4.2 $\overline{BLAST2}$: (Deferred Burst)

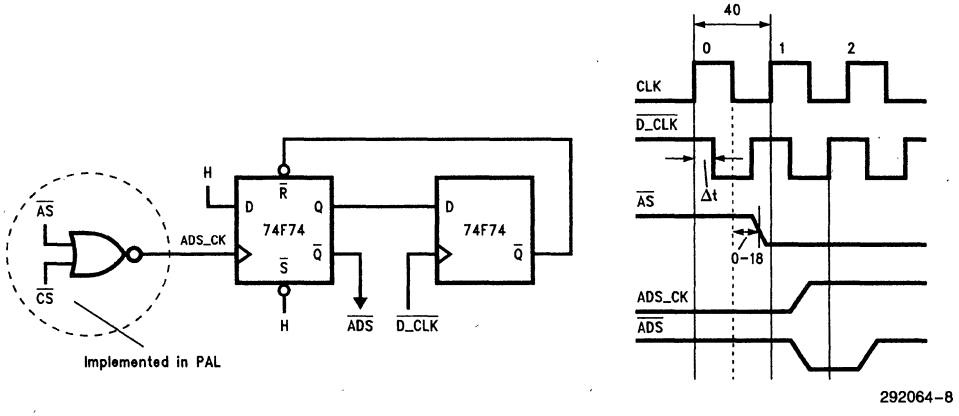
$\overline{BLAST2}$ is generated if the μP accesses a misaligned operand. Figure 11A shows an access to a misaligned operand followed by a deferred burst access. In this case the burst operation is deferred because the first access corresponds to cache entry at \$0C which is accessed as a single word. The second access at address \$10 corresponds to the second cache line, and a burst request is made. The μP asserts $\overline{CBREQ}$ during a burst request. $\overline{BLAST2}$ is used to terminate the single word access. Figure 11B shows the logic for generating $\overline{BLAST2}$. The state of $\overline{CBREQ}$ is monitored, and if it is high $\overline{BLAST2}$ is asserted on count 4 (after the number of wait states, N, has expired) and de-asserted on count 5.

3.4.3 $\overline{BLAST3}$

$\overline{BLAST3}$ is generated if $\overline{CIIN}$ is asserted during a burst cycle. Figure 12 shows the timing diagram for generation of $\overline{BLAST3}$. $\overline{CIIN}$ resets the flip/flop, and the next rising edge of clock pulls $\overline{BLAST3}$ high.

3.5 Data Latches

The four data latches latch the 32-bit data on the rising edge of CLK (since the 27960 burst EPROM provides data on the rising edge of CLK). The 68030 μP reads the data on the falling edge of CLK. The latches provide plenty of setup and hold times for the data. $\overline{DBEN}$ signal is used to enable the data latches.



NOTES:
D_CLK is inverted and delayed version of CLK.
Δt = 5 ±1 ns for 25 MHz System.
Δt = 9 ±1 ns for 20 MHz System.

Figure 8A. ADS Generation for 25/20 MHz Circuit of Figure 3

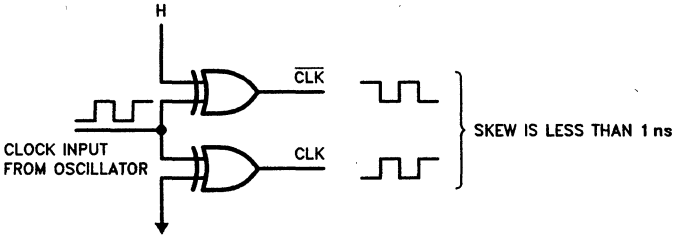
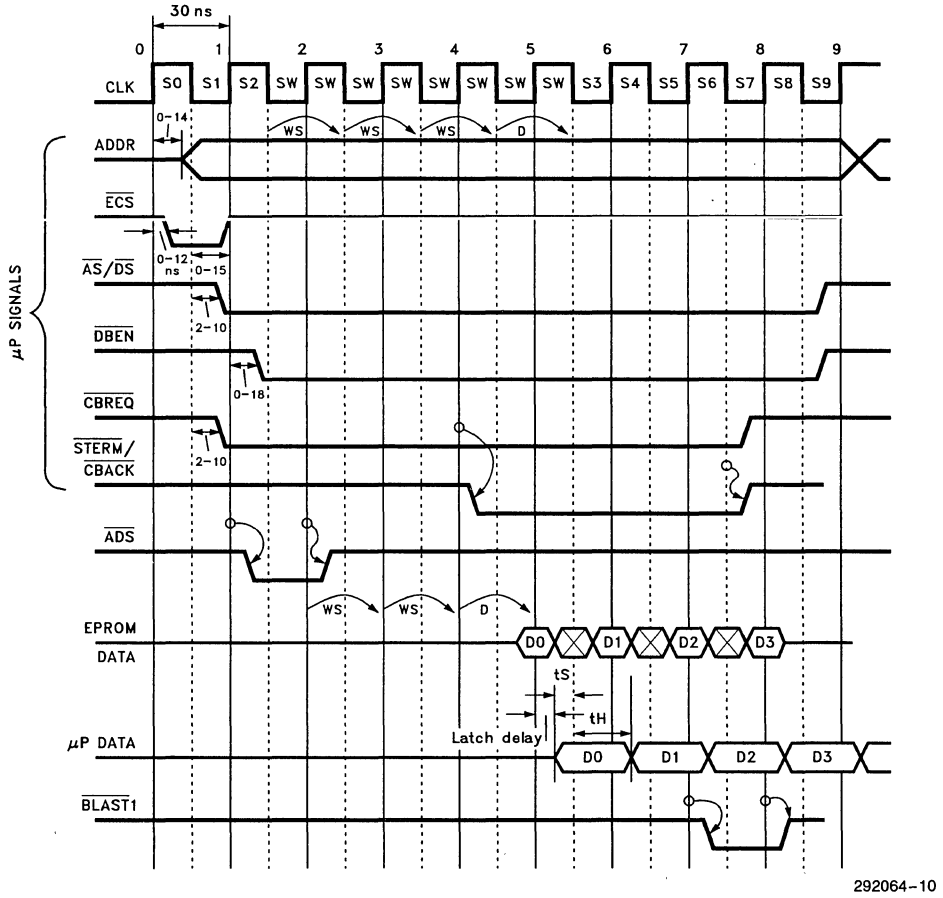


Figure 8B. Circuit for Generating Opposite Phases of CLK



NOTES:
3-0-0-0 = 3 wait states for first word access, 0 wait states for subsequent words.
68030 latches data on the falling edge of clock.
A 4-bit counter is implemented in the PAL which provides timing for $\overline{\text{STERM}}$, $\overline{\text{CBACK}}$, $\overline{\text{ADS}}$ and $\overline{\text{BLAST1}}$.
$\overline{\text{BLAST1}}$ is ANDed with $\overline{\text{BLAST2/3}}$ to generate $\overline{\text{BLAST}}$ for the EPROMs (see Figure 2).

Figure 9. 3-0-0-0 4 Word Burst Operation (33 MHz)

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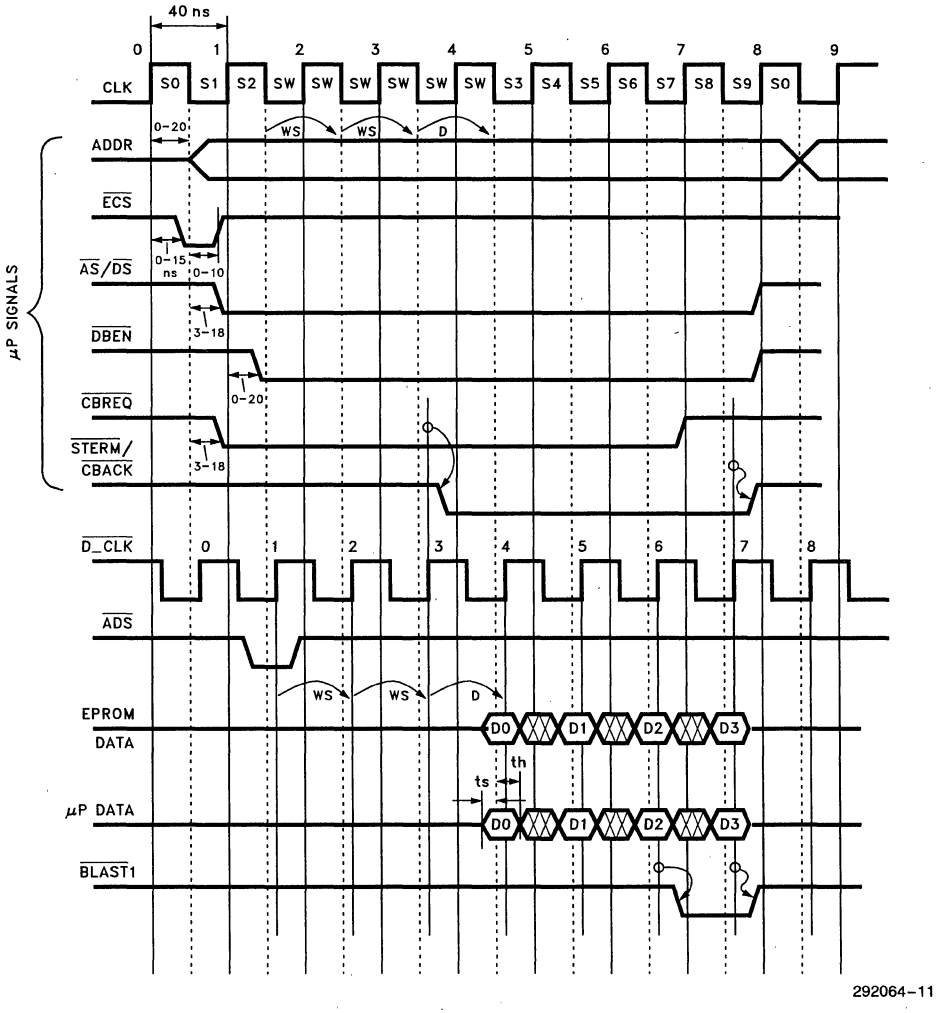

NOTES:
2-0-0-0 = 2 wait states for first word access, 0 wait states for subsequent words.
68030 latches data on the falling edge of CLK.
$\overline{D\_CLK}$ is used for generating $\overline{STERM}$, $\overline{CBACK}$, $\overline{ADS}$ and $\overline{BLAST1}$.
A 3-bit counter is implemented in the PAL which is used for generating the above signals.
$\overline{BLAST1}$ is ANDed with $\overline{BLAST2/3}$ to generate $\overline{BLAST}$ for the EPROMs (see Figure 3).

Figure 10. 2-0-0-0 4-Word Burst Operation (25 MHz)

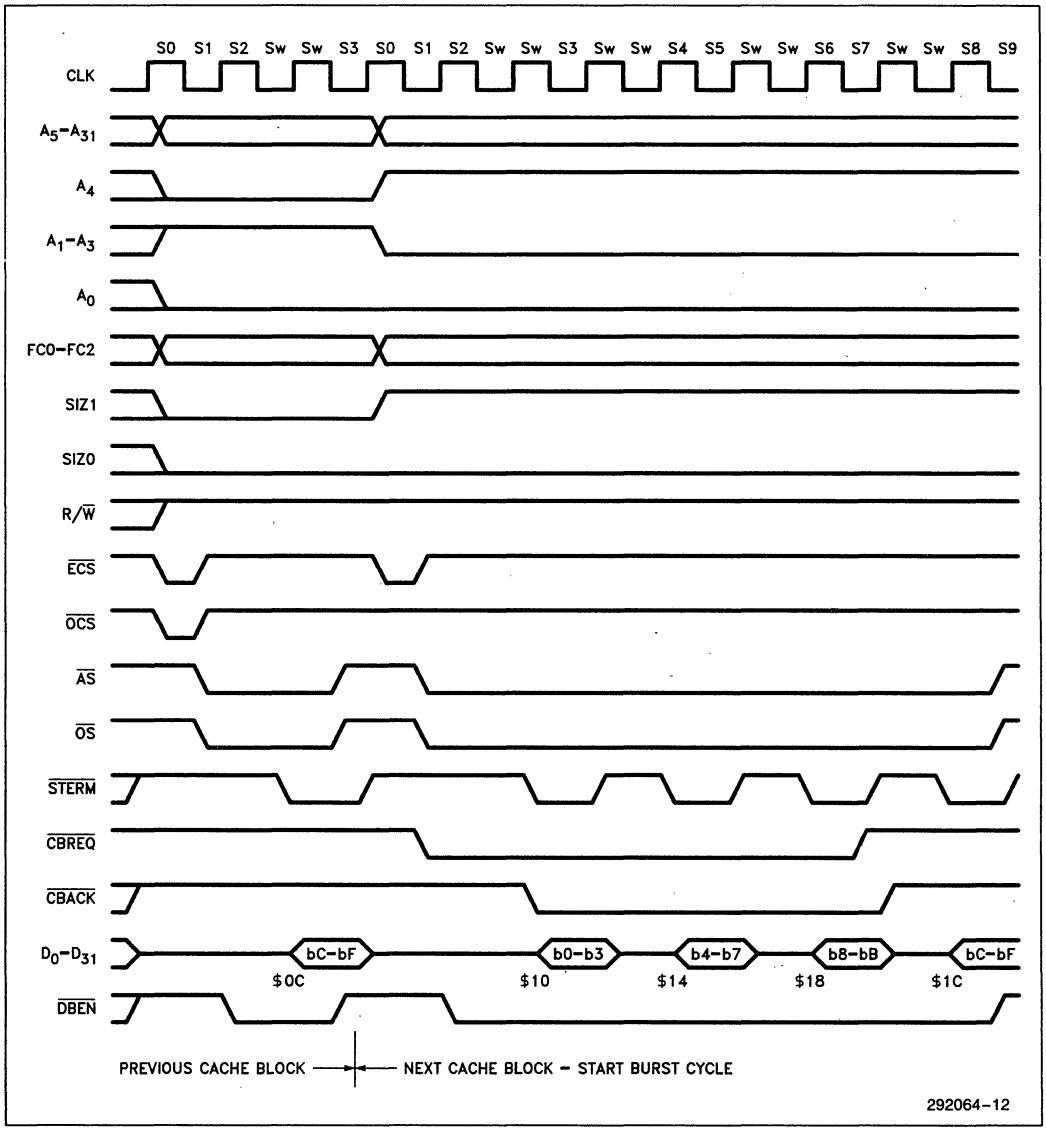

Figure 11A. Long-Word Request from $0E—Burst Deferred

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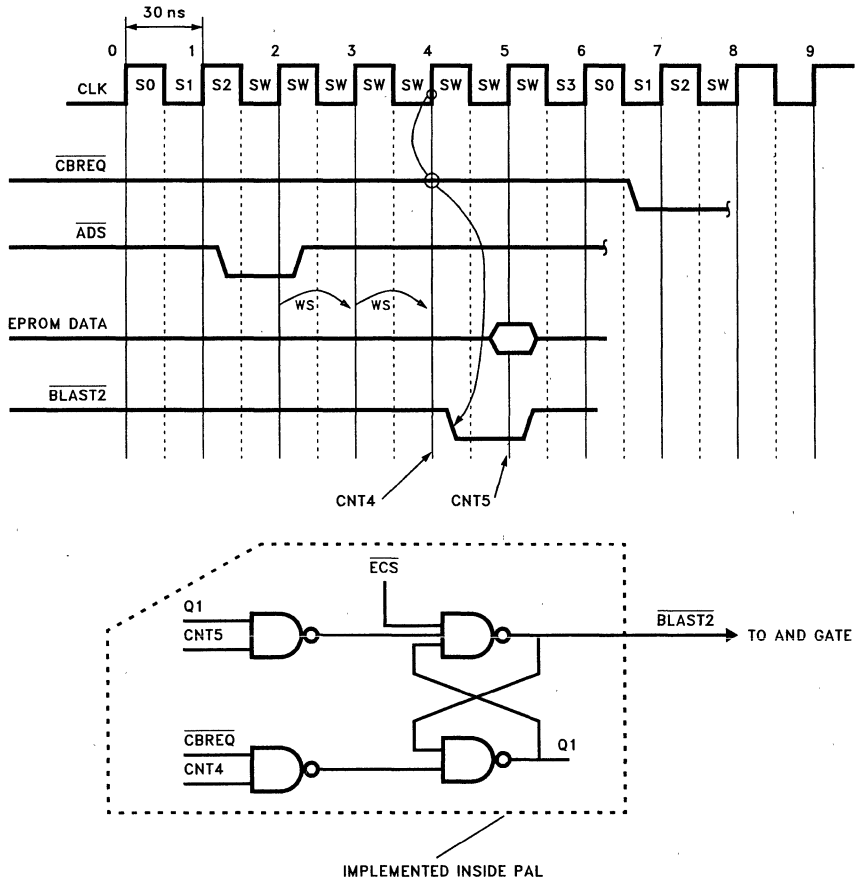

NOTES:
BLAST2 is asserted on count 4 (after the number of wait states, N, has expired) and deasserted on count 5.
N = 2 in this case.

Figure 11B. Logic for Generating BLAST2 for a Deferred Burst

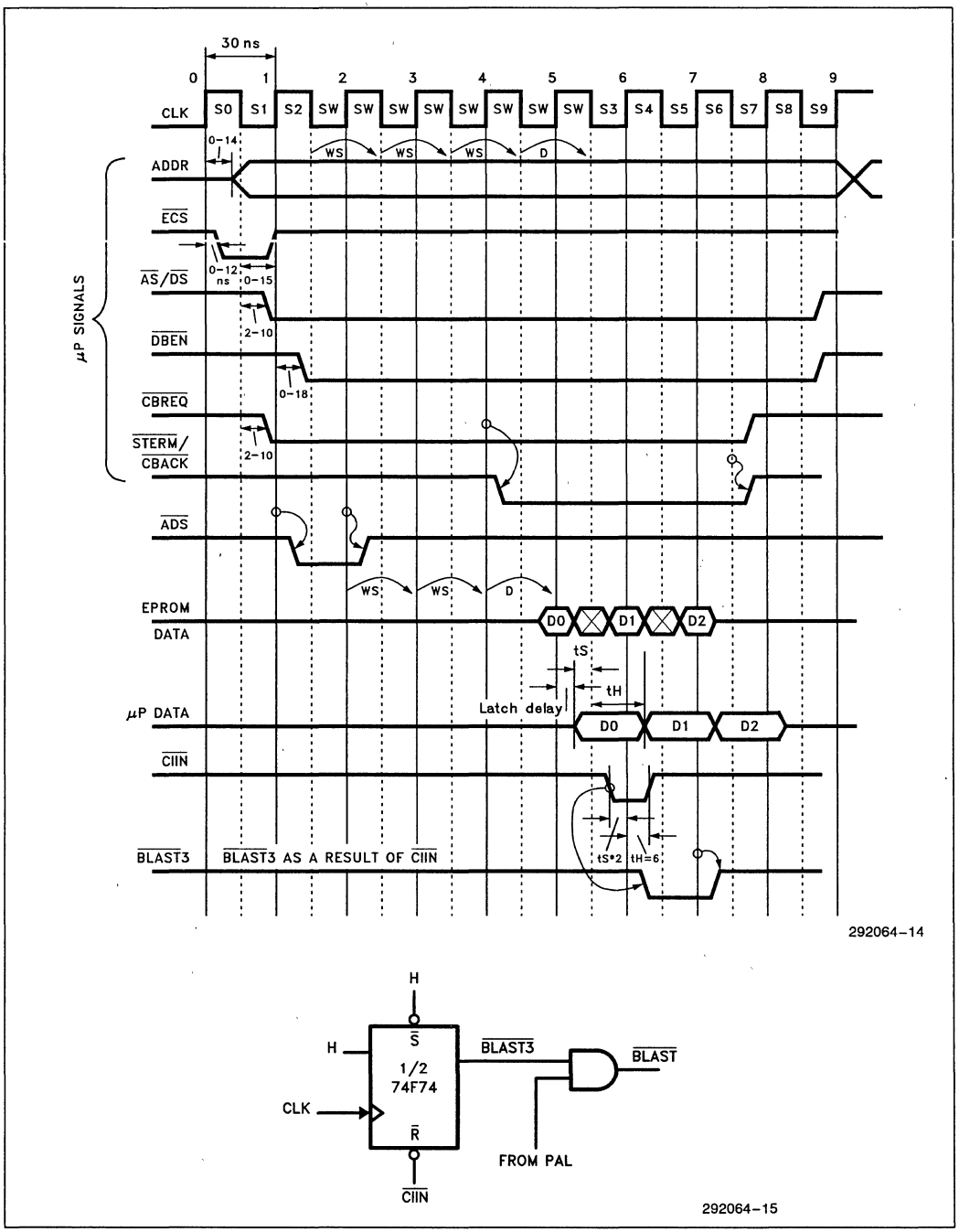

Figure 12. Timing Diagram for Generation of $\overline{\text{BLAST}}$ as Result of $\overline{\text{CIIN}}$ While $\overline{\text{STERM}}$ is Asserted

APPENDIX A

CONTENTS

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name (e.g., CLK, $\overline{ADS}$, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated by the fourth character. The list below shows character representations.

A:	Address	R:	$\overline{Reset}$
B:	$\overline{BLAST}$	Q:	Data
C:	Clock	S:	$\overline{Chip\ Select}$
H:	Logic High Level	t:	Time
L:	$\overline{ADS}$/Logic Low Level	V:	Valid
P:	V_{PP} Programming Voltage	Z:	Tristate Level
X:	No longer a valid "driven" logic level		

AC CHARACTERISTICS $0°C < T_A < +70°C, V_{CC} = 5V \pm 10\%$

Versions				27960C2-33		27960C2-25		27960C1-20		27960C1-16		Units
				33 MHz 2 Wait State		25 MHz 2 Wait State		20 MHz 1 Wait State		16 MHz 1 Wait State		
No.	Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{AVC_0H}	Address Valid to CLK High	CLK0	12		10		14		22		ns
2	t_{C_NHAX}	CLK High to Address Invalid	2	0		0		0		0		ns
3	t_{LLCH}	$\overline{ADS}$ Low to CLK High	CLK0	8		8		14		22		ns
4	t_{CHLH}	CLK High to $\overline{ADS}$ High	5	6	22	6	32	6	36	6	40	ns
5	t_{SVCH}	Chip Select Valid to CLK High	1	7		7		6		14		ns
6	t_{C_NHSX}	CLK High to Chip Select Invalid	2	0		0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		27		30		35		40	ns
8	t_{CHQX}	CLK High to Data Invalid		5		5		5		5		ns
9	t_{CHQZ}	CLK High to Data Hi-Z	6		25		30		30		30	ns
10	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		8		8		14		22		ns
11	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	3	6	22	6	32	6	36	6	40	ns

NOTES:
1. Valid signal level is meant to be either a logic high or logic low.
2. The subscript N represents the number of wait states for this parameter. $\overline{CS}$ can be de-asserted (high) after the number of wait states (N) has expired. The EPROM will continue to burst out data for the current cycle.
3. $\overline{BLAST}$ must be returned high before the next rising clock edge.
4. The sum of $t_{CHQV} + t_{AVCH} +$ NCLK will not equal actual t_{AVQV} if independent test conditions are used to obtain t_{AVCH} and t_{CHQV} (N = number of wait states).
5. $\overline{ADS}$ must be returned high before the next rising clock edge.
6. Sampled but not 100% tested. The transition is measured ±500 mV from steady state voltage.
7. For capacitive loads above 80 pF, t_{CHQV} can be derated by 1 ns/20 pF.

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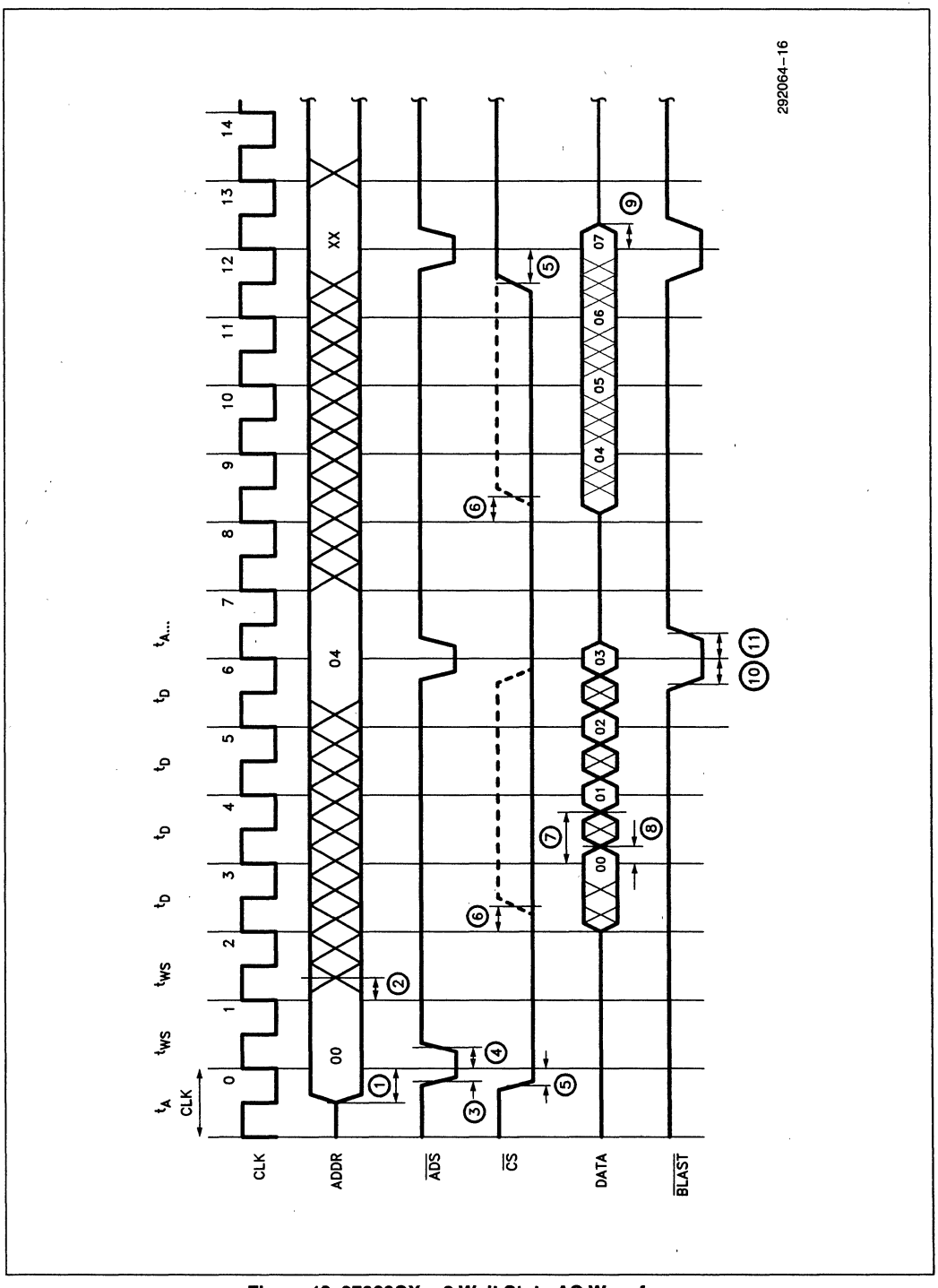

Figure 10. 27960CX 2 Wait State AC Waveforms

AC ELECTRICAL SPECIFICATIONS — CLOCK INPUT (see Figure 9)

Num.	Characteristic	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation	12.5	16.67	12.5	20	12.5	25	20	33.33	MHz
1	Cycle Time Clock	60	80	50	80	40	80	30	50	ns
2, 3	Clock Pulse Width Measured from 1.5 V to 1.5 V	28	52	23	57	19	61	14	36	ns
4, 5	Clock Rise and Fall Times	—	5	—	5	—	4	—	3	ns

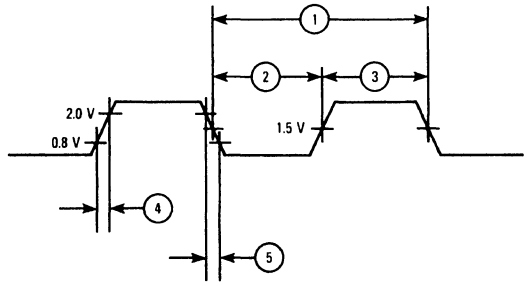

Figure 9. Clock Input Timing Diagram

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AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; T_A = 0 to 70°C; see Figures 11 through 16)

Num.	Characteristic	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock High to Function Code, Size, $\overline{RMC}$, $\overline{IPEND}$, $\overline{CIOUT}$, Address Valid	0	30	0	25	0	20	0	14	ns
6A	Clock High to $\overline{ECS}$, $\overline{OCS}$ Asserted	0	20	0	15	0	15	0	12	ns
6B	Function Code, Size, $\overline{RMC}$, $\overline{IPEND}$, $\overline{CIOUT}$, Address Valid to Negating Edge of $\overline{ECS}$	5	—	4	—	3	—	3	—	ns
7	Clock High to Function Code, Size, $\overline{RMC}$, $\overline{CIOUT}$, Address, Data High Impedance	0	60	0	50	0	40	0	30	ns
8	Clock High to Function Code, Size, $\overline{RMC}$, $\overline{IPEND}$, $\overline{CIOUT}$, Address Invalid	0	—	0	—	0	—	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$ Asserted, $\overline{CBREQ}$ Valid	3	30	3	20	3	18	2	10	ns
9A[1]	$\overline{AS}$ to $\overline{DS}$ Assertion Skew (Read)	−15	15	−10	10	−10	10	−8	8	ns
9B[14]	$\overline{AS}$ Asserted to $\overline{DS}$ Asserted (Write)	37	—	32	—	27	—	22	—	ns
10	$\overline{ECS}$ Width Asserted	20	—	15	—	10	—	8	—	ns
10A	$\overline{OCS}$ Width Asserted	20	—	15	—	10	—	8	—	ns
10B[7]	$\overline{ECS}$, $\overline{OCS}$ Width Negated	15	—	10	—	5	—	5	—	ns
11	Function Code, Size, $\overline{RMC}$, $\overline{CIOUT}$, Address Valid to $\overline{AS}$ Asserted (and $\overline{DS}$ Asserted, Read)	15	—	10	—	7	—	5	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CBREQ}$ Negated	0	30	0	20	0	18	0	10	ns
12A	Clock Low to $\overline{ECS}$/$\overline{OCS}$ Negated	0	30	0	20	0	18	0	15	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to Function Code, Size, $\overline{RMC}$ $\overline{CIOUT}$, Address Invalid	15	—	10	—	7	—	5	—	ns
14	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted (Asynchronous Cycle)	100	—	85	—	70	—	45	—	ns
14A[11]	$\overline{DS}$ Width Asserted (Write)	40	—	38	—	30	—	23	—	ns
14B	$\overline{AS}$ (and $\overline{DS}$, Read) Width Asserted (Synchronous Cycle)	40	—	35	—	30	—	23	—	ns
15	$\overline{AS}$, $\overline{DS}$ Width Negated	40	—	38	—	30	—	23	—	ns
15A[8]	$\overline{DS}$ Negated to $\overline{AS}$ Asserted	35	—	30	—	25	—	18	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{DBEN}$, $\overline{CBREQ}$ High Impedance	—	60	—	50	—	40	—	30	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	15	—	10	—	7	—	5	—	ns
18	Clock High to R/$\overline{W}$ High	0	30	0	25	0	20	0	15	ns
20	Clock High to R/$\overline{W}$ Low	0	30	0	25	0	20	0	15	ns
21	R/$\overline{W}$ High to $\overline{AS}$ Asserted	15	—	10	—	7	—	5	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	75	—	60	—	47	—	35	—	ns
23	Clock High to Data-Out Valid	—	30	—	25	—	20	—	14	ns
24	Data-Out Valid to Negating Edge of $\overline{AS}$	12	—	8	—	5	—	3	—	ns
25[11]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid	15	—	10	—	7	—	5	—	ns
25A[9,11]	$\overline{DS}$ Negated to $\overline{DBEN}$ Negated (Write)	15	—	10	—	7	—	5	—	ns
26[11]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	15	—	10	—	7	—	5	—	ns
27	Data-In Valid to Clock Low (Setup)	5	—	4	—	2	—	1	—	ns
27A	Late $\overline{BERR}$/$\overline{HALT}$ Asserted to Clock Low (Setup)	15	—	10	—	5	—	3	—	ns
28[12]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated (Asynchronous Hold)	0	60	0	50	0	40	0	30	ns
28A[12]	Clock Low to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated (Synchronous Hold)	15	100	12	85	8	70	6	50	ns
29[12]	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Asynchronous Hold)	0	—	0	—	0	—	0	—	ns
29A[12]	$\overline{AS}$, $\overline{DS}$ Negated to Data-In High Impedance	—	60	—	50	—	40	—	30	ns
30[12]	Clock Low to Data-In Invalid (Synchronous Hold)	15	—	12	—	8	—	6	—	ns
30A[12]	Clock Low to Data-In High Impedance (Read followed by Write)	—	90	—	75	—	60	—	45	ns

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AC ELECTRICAL SPECIFICATIONS (Continued)

Num.	Characteristic	16.67 MHz		20 MHz		25 MHz		33.33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
31[2]	$\overline{DSACKx}$ Asserted to Data-In Valid (Asynchronous Data Setup)	—	50	—	43	—	28	—	20	ns
31A[3]	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	—	15	—	10	—	7	—	5	ns
32	$\overline{RESET}$ Input Transition Time	—	1.5	—	1.5	—	1.5	—	1.5	Clks
33	Clock Low to $\overline{BG}$ Asserted	0	30	0	25	0	20	0	15	ns
34	Clock Low to $\overline{BG}$ Negated	0	30	0	25	0	20	0	15	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	0	1.5	0	1.5	0	1.5	0	1.5	Clks
39[6]	$\overline{BG}$ Width Negated	90	—	75	—	60	—	45	—	ns
39A	$\overline{BG}$ Width Asserted	90	—	75	—	60	—	45	—	ns
40	Clock High to $\overline{DBEN}$ Asserted (Read)	0	30	0	25	0	20	0	18	ns
41	Clock Low to $\overline{DBEN}$ Negated (Read)	0	30	0	25	0	20	0	18	ns
42	Clock Low to $\overline{DBEN}$ Asserted (Write)	0	30	0	25	0	20	0	18	ns
43	Clock High to $\overline{DBEN}$ Negated (Write)	0	30	0	25	0	20	0	18	ns
44	R/$\overline{W}$ Low to $\overline{DBEN}$ Asserted (Write)	15	—	10	—	7	—	5	—	ns
45[5]	$\overline{DBEN}$ Width Asserted — Asynchronous Read	60	—	50	—	40	—	30	—	ns
	$\overline{DBEN}$ Width Asserted — Asynchronous Write	120	—	100	—	80	—	60	—	
45A[9]	$\overline{DBEN}$ Width Asserted — Synchronous Read	10	—	10	—	5	—	5	—	ns
	$\overline{DBEN}$ Width Asserted — Synchronous Write	60	—	50	—	40	—	30	—	
46	R/$\overline{W}$ Width Asserted (Asynchronous Write or Read)	150	—	125	—	100	—	75	—	ns
46A	R/$\overline{W}$ Width Asserted (Synchronous Write or Read)	90	—	75	—	60	—	45	—	ns
47A	Asynchronous Input Setup Time to Clock Low	5	—	4	—	2	—	2	—	ns
47B	Asynchronous Input Hold Time from Clock Low	15	—	12	—	8	—	6	—	ns
48[4]	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	—	30	—	20	—	25	—	18	ns
53	Data-Out Hold from Clock High	3	—	3	—	3	—	2	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	30	—	25	—	20	—	15	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	512	—	512	—	512	—	512	—	Clks
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	0	—	0	—	0	—	0	—	ns
58[10]	$\overline{BGACK}$ Negated to Bus Driven	1	—	1	—	1	—	1	—	Clks
59[10]	$\overline{BG}$ Negated to Bus Driven	1	—	1	—	1	—	1	—	Clks
60[13]	Synchronous Input Valid to Clock High (Setup Time)	5	—	4	—	2	—	2	—	ns
61[13]	Clock High to Synchronous Input Invalid (Hold Time)	15	—	12	—	8	—	6	—	ns
62	Clock Low to $\overline{STATUS}$, $\overline{REFILL}$ Asserted	0	30	0	25	0	20	0	15	ns
63	Clock Low to $\overline{STATUS}$, $\overline{REFILL}$ Negated	0	30	0	25	0	20	0	15	ns

NOTES:

1. This number can be reduced to 5 nanoseconds if strobes have equal loads.
2. If the asynchronous setup time (#47A) requirements are satisfied, the $\overline{DSACKx}$ low to data setup time (#31) and $\overline{DSACKx}$ low to $\overline{BERR}$ low setup time (#48) can be ignored. The data must only satisfy the data-in clock low setup time (#27) for the following clock cycle and $\overline{BERR}$ must only satisfy the late $\overline{BERR}$ low to clock low setup time (#27A) for the following clock cycle.
3. This parameter specifies the maximum allowable skew between $\overline{DSACK0}$ to $\overline{DSACK1}$ asserted or $\overline{DSACK1}$ to $\overline{DSACK0}$ asserted; specification #47A must be met by $\overline{DSACK0}$ or $\overline{DSACK1}$.
4. This specification applies to the first ($\overline{DSACK0}$ or $\overline{DSACK1}$) $\overline{DSACKx}$ signal asserted. In the absence of $\overline{DSACKx}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47A).
5. $\overline{DBEN}$ may stay asserted on consecutive write cycles.
6. The minimum values must be met to guarantee proper operation. If this maximum value is exceeded, $\overline{BG}$ may be reasserted.
7. This specification indicates the minimum high time for $\overline{ECS}$ and $\overline{OCS}$ in the event of an internal cache hit followed immediately by another cache hit, a cache miss, or an operand cycle.
8. This specification guarantees operation with the MC68881/MC68882, which specifies a minimum time for $\overline{DS}$ negated to $\overline{AS}$ asserted (specification #13A in the *MC68881/MC68882 User's Manual*). Without this specification, incorrect interpretation of specifications #9A and #15 would indicate that the MC68030 does not meet the MC68881/MC68882 requirements.

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NOTES (Continued)

9. This specification allows a system designer to guarantee data hold times on the output side of data buffers that have output enable signals generated with $\overline{DBEN}$. The timing on $\overline{DBEN}$ precludes its use for synchronous READ cycles with no wait states.
10. These specifications allow system designers to guarantee that an alternate bus master has stopped driving the bus when the MC68030 regains control of the bus after an arbitration sequence.
11. $\overline{DS}$ will not be asserted for synchronous write cycles with no wait states.
12. These hold times are specified with respect to strobes (asynchronous) and with respect to the clock (synchronous). The designer is free to use either time.
13. Synchronous inputs must meet specifications #60 and #61 with stable logic levels for ***all*** rising edges of the clock while $\overline{AS}$ is asserted. These values are specified relative to the high level of the rising clock edge. The values originally published were specified relative to the low level of the rising clock edge.
14. This specification allows system designers to qualify the $\overline{CS}$ signal of an MC68881/MC68882 with $\overline{AS}$ (allowing 7 ns for a gate delay) and still meet the $\overline{CS}$ to $\overline{DS}$ setup time requirement (spec 8B) of the MC68881/MC68882.

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These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

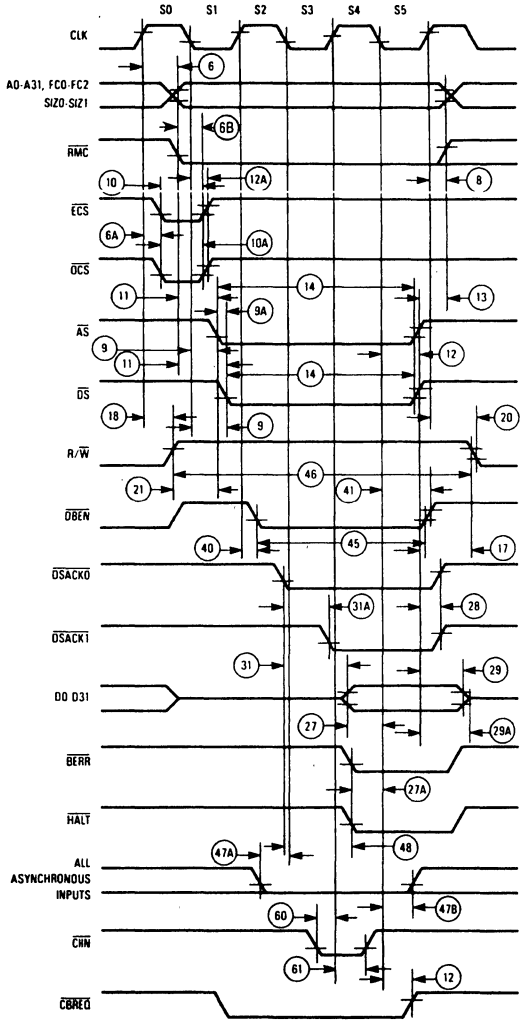

Figure 11. Asynchronous Read Cycle Timing Diagram

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These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

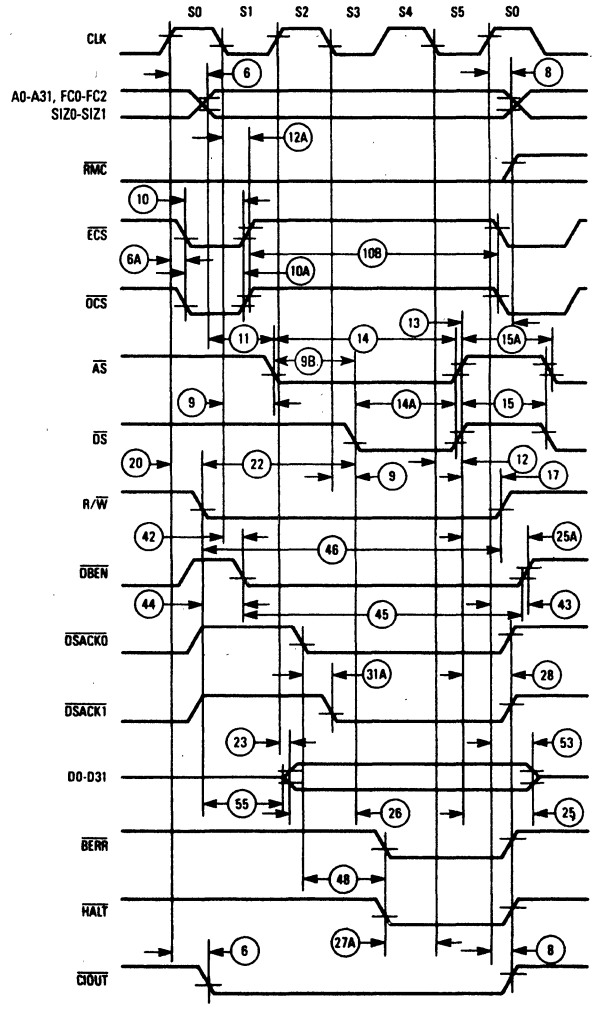

Figure 12. Asynchronous Write Cycle Timing Diagram

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These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

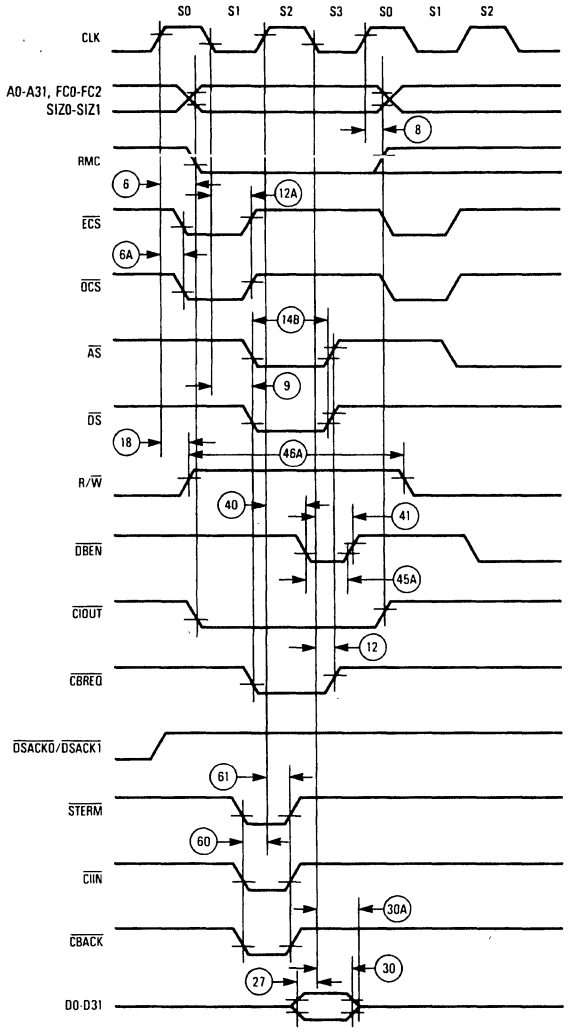

Figure 13. Synchronous Read Cycle Timing Diagram

292064-23

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These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

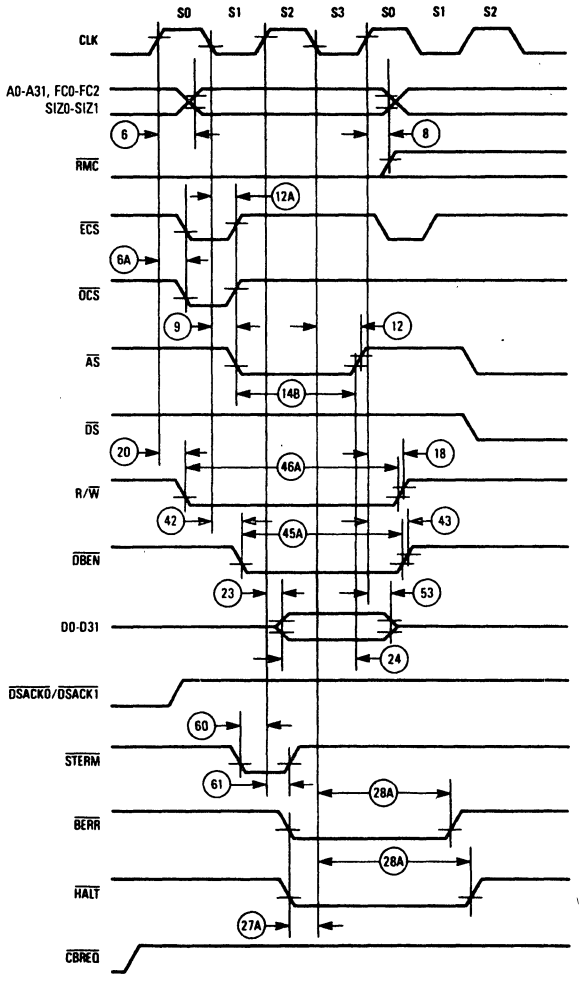

Figure 14. Synchronous Write Cycle Timing Diagram

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Delay Line Information

Delay lines with tolerances of +1 ns can be obtained from:

ECC
3580 Sacramento Drive
San Luis Obispo, CA 93403

This company can also manufacture at customer's request a delay line with inverted output at virtually the same cost as their regular devices.

Other delay line manufacturers are:

Dallas Semiconductor
4350 Beltwood Parkway South
Dallas, Texas 75244

EG&G Reticon Corp.
345 Portero Ave.
Sunnyvale, CA 94086

PRELIMINARY
AP-346

APPLICATION NOTE

November 1990

Am29000*/27960CX Burst EPROM Interface

INTEL
PROGRAMMABLE MEMORY OPERATION

*Am29000 is a trademark of Advanced Micro Devices, Inc.

Order Number: 292081-001

29000/27960CX BURST EPROM INTERFACE

CONTENTS

CONTENTS

5

This application note describes the design of a circuit to interface the 27960CX burst EPROM to AMD's Am29000* microprocessor. The 29000 microprocessor is capable of operating in a burst mode, accessing a maximum of 256 long words (long word = 32 bits) during a burst access. The burst EPROM supports a maximum of 4 words during a burst access. To accommodate the longer burst cycle of the 29k, the interface has an 8-bit external counter which supplies the lower eight addresses to the EPROMs.

A 1-0-0-0 burst operation (one wait-state for the first word access and zero wait-state for the remaining three accesses) is possible at 20 MHz using the 27960C1-20 burst EPROMs. Effectively this results in a 4 words/5 clock cycles performance for this interface. A 2-0-0-0 burst operation (non-buffered system) is possible at 25 MHz/33 MHz using the 27960C2-25/33 burst EPROMs. This memory interface monitors control signals from the microprocessor and provides handshake logic for the microprocessor, and generates $\overline{ADS}$ and $\overline{BLAST}$ signals for the burst EPROMs.

The interface can be implemented with a 16R6D PAL, an 8-bit counter, a 9-bit latch, a D-type flip-flop, an address decoder and some discrete AND and OR gates. The discrete gates may be integrated into the control logic PAL or another system PAL. Address and data buffers may be required if the capacitive loading is large.

SIGNAL DEFINITIONS/INTERFACE REQUIREMENTS

1.0 SIGNAL DEFINITIONS

1.1 29000 Signals

This section describes the 29000 signals which are relevant to this interface.

1.1.1 $\overline{IREQ}$—INSTRUCTION REQUEST (OUTPUT)

This signal requests an instruction access. When it is active, the address bus has a valid address for the access.

1.1.2 $\overline{IBREQ}$—INSTRUCTION BURST REQUEST (OUTPUT)

This signal is used to establish a burst-mode instruction access and to request instruction transfers during a burst-mode instruction access.

*Am29000 is a trademark of Advanced Micro Devices, Inc.

1.1.3 $\overline{BINV}$—BUS INVALID (OUTPUT)

This signal indicates that the Address Bus and related control signals are invalid. It defines an idle cycle for the channel.

1.1.4 $\overline{IRDY}$—INSTRUCTION READY (INPUT)

This signal indicates that a valid instruction is on the instruction bus.

1.1.5 IREQT—INSTRUCTION REQUEST TYPE (OUTPUT)

This signal specifies the address space of an instruction request, when $\overline{IREQ}$ is active:

$\overline{IREOT}$

0— Instruction/Data Memory Access

1— Instruction Read Only Memory Access

1.1.6 $\overline{IBACK}$—INSTRUCTION BURST ACKNOWLEDGE (INPUT)

This input is active whenever a burst-mode instruction has been established. It may be active even though no instructions are currently being accessed, for example in a suspended burst access.

1.2 27960CX Burst EPROM Control Signals

1.2.1 $\overline{ADS}$—ADDRESS STROBE (INPUT)

Indicates the start of a new bus access. It is active low in the first clock cycle of a bus access.

1.2.2 $\overline{BLAST}$—BURST LAST (INPUT)

Terminates a concurrent burst data cycle. Must be asserted by the fourth data word.

1.2.3 $\overline{CS}$—CHIP SELECT (INPUT)

Master device enable. When asserted, data can be written to and read from the device. In read mode, $\overline{CS}$ enables the state machine and the I/O circuitry. A memory access begins on the first rising edge of CLK after $\overline{ADS}$ and $\overline{CS}$ are asserted. $\overline{CS}$ can be de-asserted after the number of wait-states, N, has expired, but the EPROM will continue to burst out data for the current cycle. If $\overline{CS}$ is de-asserted during the wait-state period, the burst access will be aborted.

2.0 INTERFACE REQUIREMENTS

The interface is designed to work in the burst mode,with the instruction burst acknowledge signal, $\overline{IBACK}$, as the handshake for the microprocessor indicating that the EPROM memory is capable of supporting a burst access. The interface logic will monitor control signals from the microprocessor, i.e., $\overline{IREQ}$, $\overline{IBREQ}$, $\overline{BINV}$, and generate $\overline{IRDY}$ and $\overline{IBACK}$ for the microprocessor and $\overline{ADS}$ and $\overline{BLAST}$ signals for the 27960 EPROM. Since the burst EPROM is capable of bursting a maximum of four words, the interface will suspend the burst after the fourth word by de-asserting $\overline{IRDY}$ and resume the burst by re-asserting $\overline{IRDY}$ one clock cycle later. The interface will preempt the burst access in response to the burst access being suspended by the microprocessor.

Figure 1 shows the block diagram of the 29000/27960CX Burst EPROM interface.

3.0 CIRCUIT DESCRIPTION

This section describes the burst-mode operation of the 29000 microprocessor followed by a description of the interface circuit as shown in Figure 1.

3.1 Burst-Mode Access

The burst mode-access allows multiple instructions or data words at sequential addresses to be accessed with a single address transfer. A burst access is requested via the Instruction Burst Request ($\overline{IBREQ}$). The initial address of this burst access is indicated by assertion of Instruction Request ($\overline{IREQ}$) signal. The memory system may assert Instruction Burst Acknowledge ($\overline{IBACK}$) to indicate that it supports burst-mode accesses. If $\overline{IBACK}$ is asserted while the initial address appears on the address bus, the burst-mode access is established. In the following cycle, the 29k will de-assert the $\overline{IREQ}$ signal and remove the initial address of the burst access, but will continue to assert $\overline{IBREQ}$. If the burst-mode is never established, the default behavior is to have the processor transmit an address every access. After the burst-mode access is established, $\overline{IBREQ}$ is used during subsequent accesses to indicate that the processor requires at least one more access. If $\overline{IBREQ}$ is active at the end of a cycle in which an access is successfully completed ($\overline{IRDY}$ is active), the processor requires another access.

3.2 Burst Suspension

The burst-mode instruction access may be suspended in certain situations. The processor suspends a burst-access by de-asserting $\overline{IBREQ}$. The burst-mode access remains suspended unless the processor requests a new instruction access (in which case $\overline{IREQ}$ is asserted), or unless the instruction memory preempts the burst-mode access. A suspended burst-mode instruction becomes active whenever the processor activates the burst-mode access by asserting $\overline{IBREQ}$.

3.3 Burst Preemption

A burst access is preempted by de-asserting $\overline{IBACK}$. If $\overline{IBREQ}$ was active in the cycle before $\overline{IBACK}$ was de-asserted, one last word of information must be transferred before the burst access is ended. The last word can be transferred in the same cycle that the Burst Acknowledge is de-asserted or some later cycle, but until it is transferred the burst access is not complete and no new access of the memory may begin.

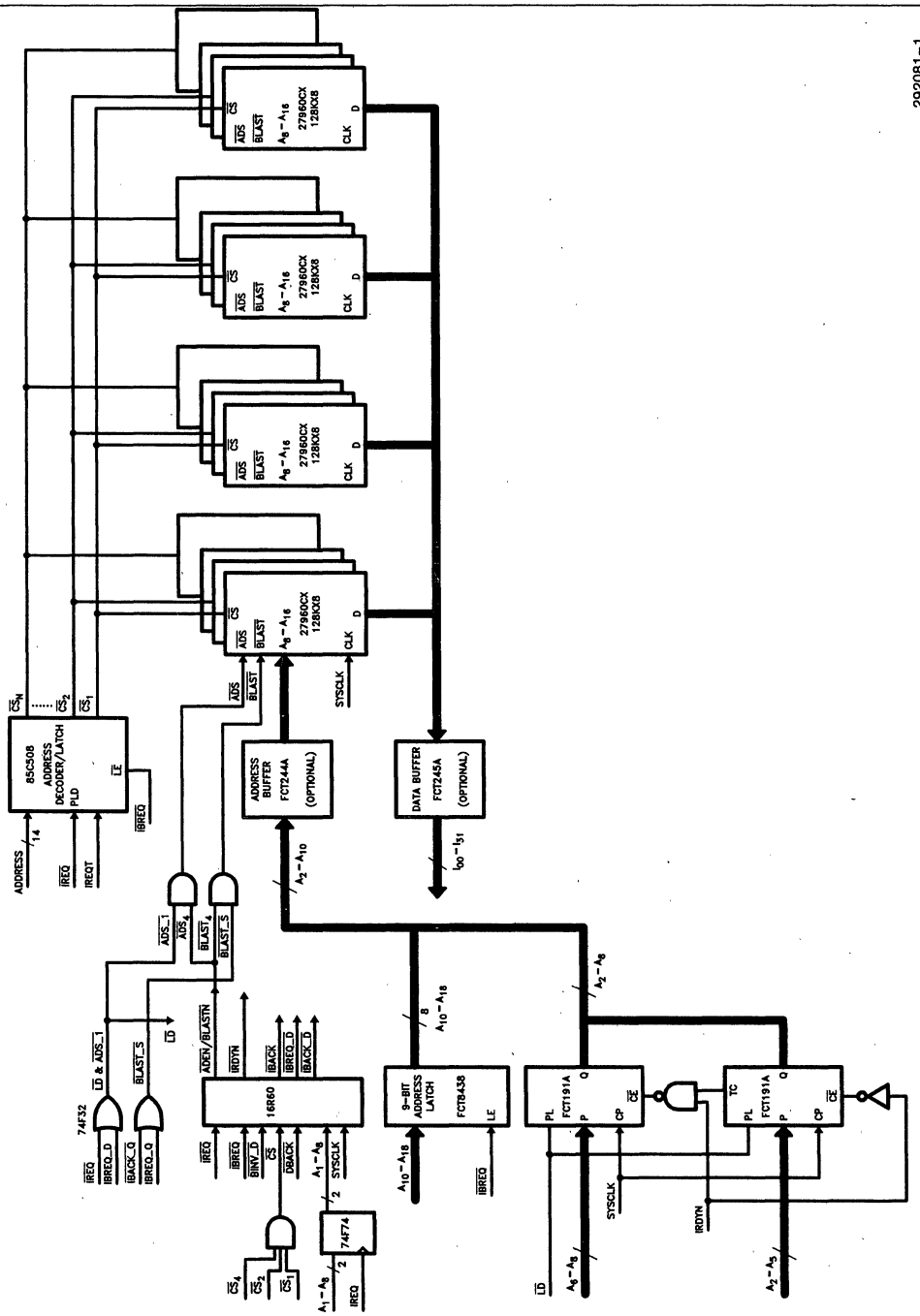
4.0 29000/27960CX INTERFACE (FIGURE 1)

4.1 Burst EPROMS

The memory block consists of 27960CX, 128k x 8-bit burst EPROMs. A minimum of four EPROMS are required for a 32-bit system. The 27960CX supports burst-mode operation, and is capable of accessing four long words (long word = 32 bits) during a burst cycle. Each burst cycle begins with a valid address being latched in the first clock cycle, when both $\overline{ADS}$ and $\overline{CS}$ are asserted. After a set number of wait-states (1 or 2), data is output one word at a time on each subsequent clock cycle. A burst access is terminated with the $\overline{BLAST}$ signal. A 1-0-0-0 burst operation (1 wait-state for the first word access and zero wait-state for subsequent accesses) is possible at 20 MHz using 27960C1-20 burst EPROMs. A 2-0-0-0 burst operation (non-buffered system) is possible at 25 MHz/33 MHz using the 27960C2-25/33 burst EPROMs.

4.2 Address/Instruction Bus Buffers

The address and instruction buses may be buffered with high speed buffers. If the memory block were made up of multiple banks of memory devices, the instruction bus might need buffering to isolate the heavier capacitive load of multiple memory banks from the rest of the system. Also address buffers may be needed to drive address inputs of multiple banks.



NOTES:
The discrete gates in this design could be integrated in an another system PAL or a bigger PAL could be used. Address and data buffers are required if capacitive loading is large.

Figure 1. 29000/27960CX Interface

4.3 Address Latch and Counter

To support burst accesses, the lower eight address bits to the burst EPROMs come from a loadable counter. The 8-bit counter is built from 74FCT191 4-bit binary counters. These high speed counters are needed if the access is to begin in the first clock cycle when $\overline{IREQ}$ is asserted. If the initial access begins in the second clock cycle, i.e., $\overline{ADS}$ is generated in the next clock cycle following assertion of $\overline{IREQ}$, a slower 8-bit counter may be used. The upper eight bits need not come from a counter, since the 29k will always output a new address when a 256-word boundary is crossed. The upper 8 bits of address are simply latched.

4.4 Control Logic

The control logic generates memory response signals, $\overline{IRDY}$, $\overline{IBACK}$, for the processor and $\overline{ADS}$ and $\overline{BLAST}$ for the burst EPROMs. It also controls loading/counting of the external 8-bit counter and address latch.

5.0 LOGIC DETAILS

NOTE:
All signals implemented in the PAL are described in active high terms, although the final output will often be active low as required by the actual circuit design.

A registered PAL output will be represented by :=

A combinatorial PAL output will be represented by =

5.1 Signal Descriptions

A 16R6D PAL is used to general $\overline{IRDY}$, $\overline{ADS}$, $\overline{BLAST}$, and $\overline{IBACK}$. A modulo 5 counter is implemented in the PAL which is used to generate timings for $\overline{IRDY}$, $\overline{ADS}_N$ and $\overline{BLAST}_N$.

5.2 Modulo 5 Counter Equations:

$Z := \overline{Z} \bullet Y \bullet X \bullet IBACK$

$Y := Z\,(Y \bullet \overline{X} + \overline{Y} \bullet X) \bullet IBACK$

$X := \overline{Z} \bullet \overline{X} \bullet IBACK$

The modulo 5 counter equations are qualified with IBACK. X is the least significant bit, and Z is the most significant bit.

5

5.3 $\overline{ADS}$ Generation

The $\overline{ADS}$ signal is derived by ANDing $\overline{ADS\_i}$ and $\overline{ADSN}$. $\overline{ADS\_i}$ is generated by ORing $\overline{IREQ}$ and $\overline{IBREQ\_D}$ (See Figure 2). ($\overline{IBREQ\_D}$ is delayed and inverted version of $\overline{IBREQ}$). $\overline{ADS\_i}$ is generated only once at the beginning of a burst access. $\overline{ADS_N}$ is generated at regular intervals every 5 clock cycles. $\overline{ADS_N}$ (where N = 0 to 3) is asserted on the first, second, third, or fourth word of the first burst access, based on the initial burst address. $\overline{ADS_N}$ is defined as follows:

$$\overline{ADS\_i} = \overline{IREQ} + IBREQ\_D$$

$$ADS_N = \overline{ADS_0} \bullet A_1 \bullet A_0 + \overline{ADS_1} \bullet A_1 \bullet \overline{A_0} + \overline{ADS_2} \bullet \overline{A_1} \bullet A_0 + \overline{ADS_3} \bullet \overline{A_1} \bullet \overline{A_0}$$

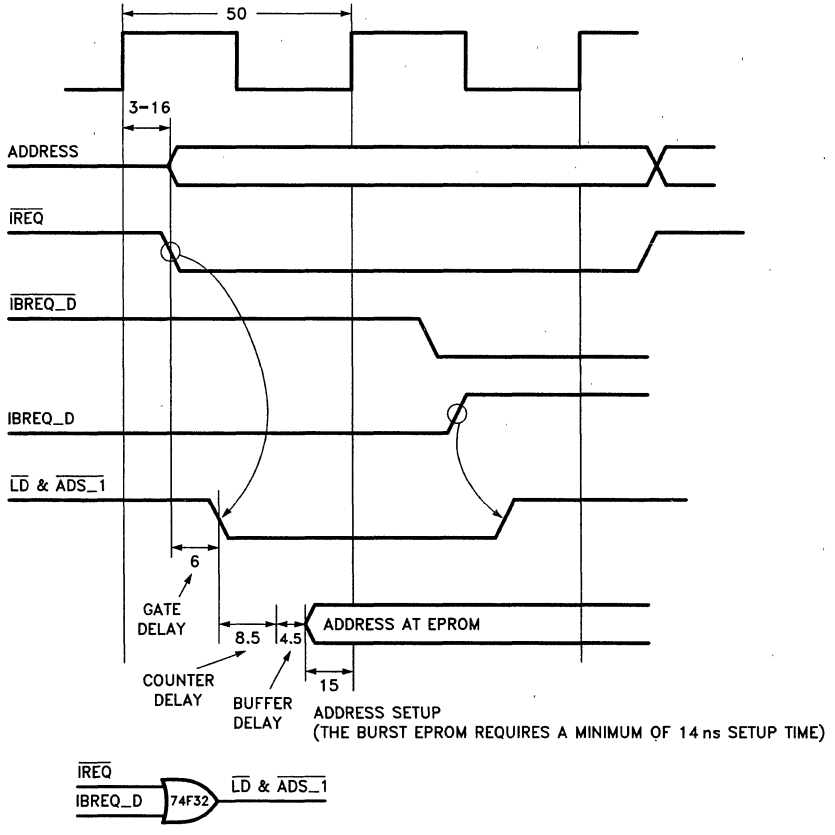
$$ADS_0 = X \bullet \overline{Y} \bullet \overline{Z}$$

$$ADS_1 = \overline{X} \bullet Y \bullet \overline{Z}$$

$$ADS_2 = X \bullet Y \bullet \overline{Z}$$

$$ADS_3 = \overline{X} \bullet \overline{Y} \bullet Z$$

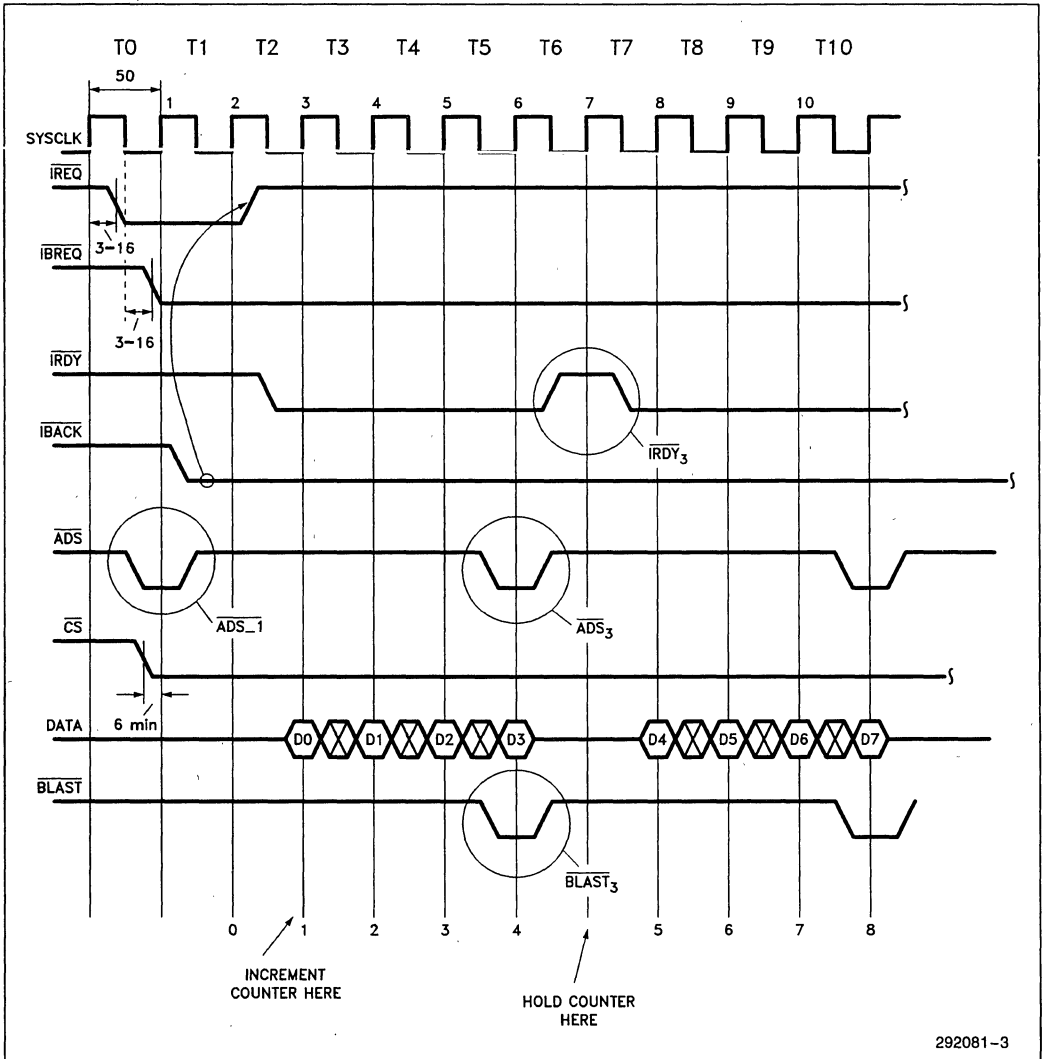
ADS_N is a multiplexer equation implemented in the PAL. The state of A_1A_0 is latched in the D-type flip-flop by $\overline{IREQ}$ as shown in Figure 1.



NOTES:
$\overline{LD}$ is used to load the 8-bit counter with the initial address.
$\overline{ADS\_i}$ is ANDed with $\overline{ADS_N}$ to generate the $\overline{ADS}$ signal for the burst EPROM.
$\overline{ADS_N}$ is generated at regular intervals at every fifth clock after the first burst access.
$\overline{ADS\_i}$ is generated only once at the beginning of a burst access.

Figure 2. Timing Diagram Showing Generation of $\overline{LD}$ and $\overline{ADS\_i}$

If the initial address of the burst access is at 0 or divisible by 4, i.e., $A_1A_0 = 00$, then the first burst access will consist of four words (maximum supported by the burst EPROM). When $A_1A_0 = 00$, $\overline{ADS}$, $\overline{IRDY}$ and $\overline{BLAST}$ are designated as $\overline{ADS_3}$, $\overline{IRDY_3}$, and $\overline{BLAST_3}$. See Figure 3A for the timing Diagram.



NOTE:
The 27960 is operating in pipelined mode; effectively this results in 4 words/5 clock cycles performance.

Figure 3A. 29000/27960C1-20 Timing Diagram Showing Burst Operation (Initial Address Is at 0 or Divisible by 4, i.e., $A_1A_0 = 00$)

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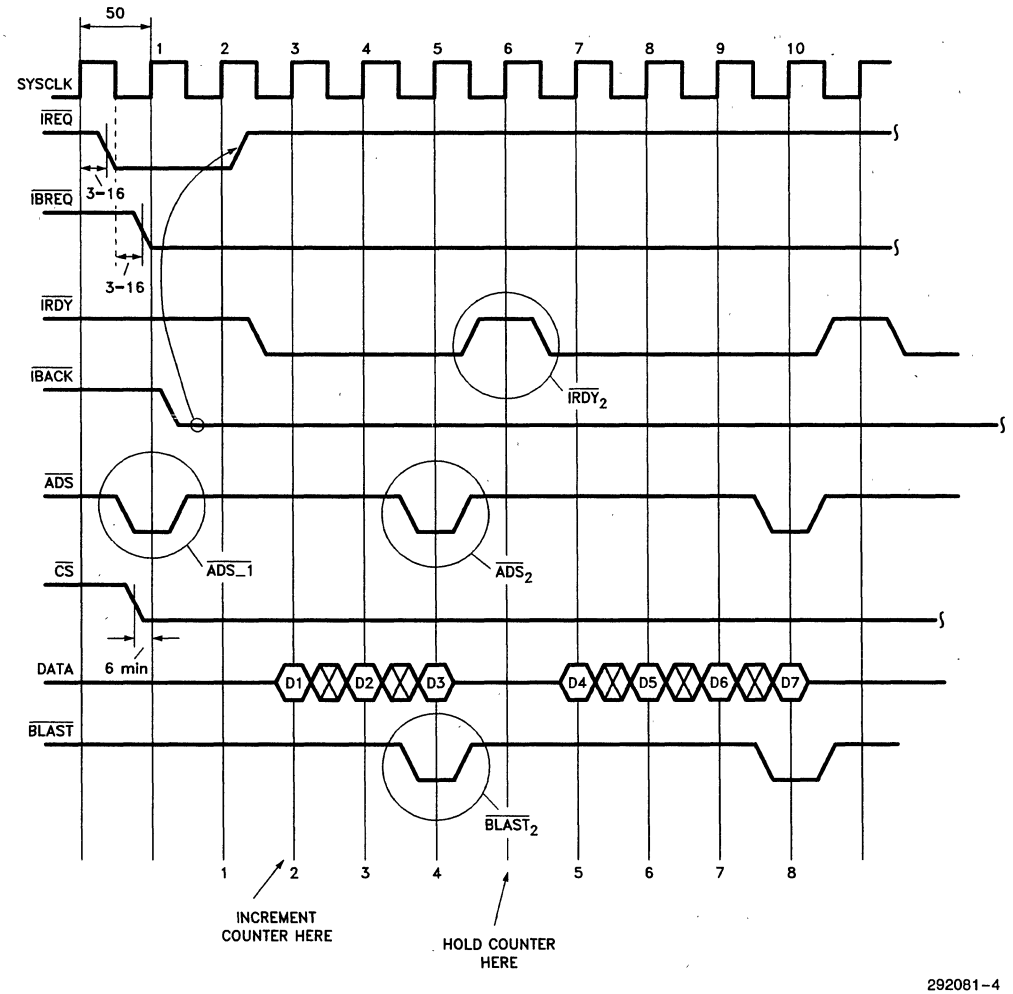
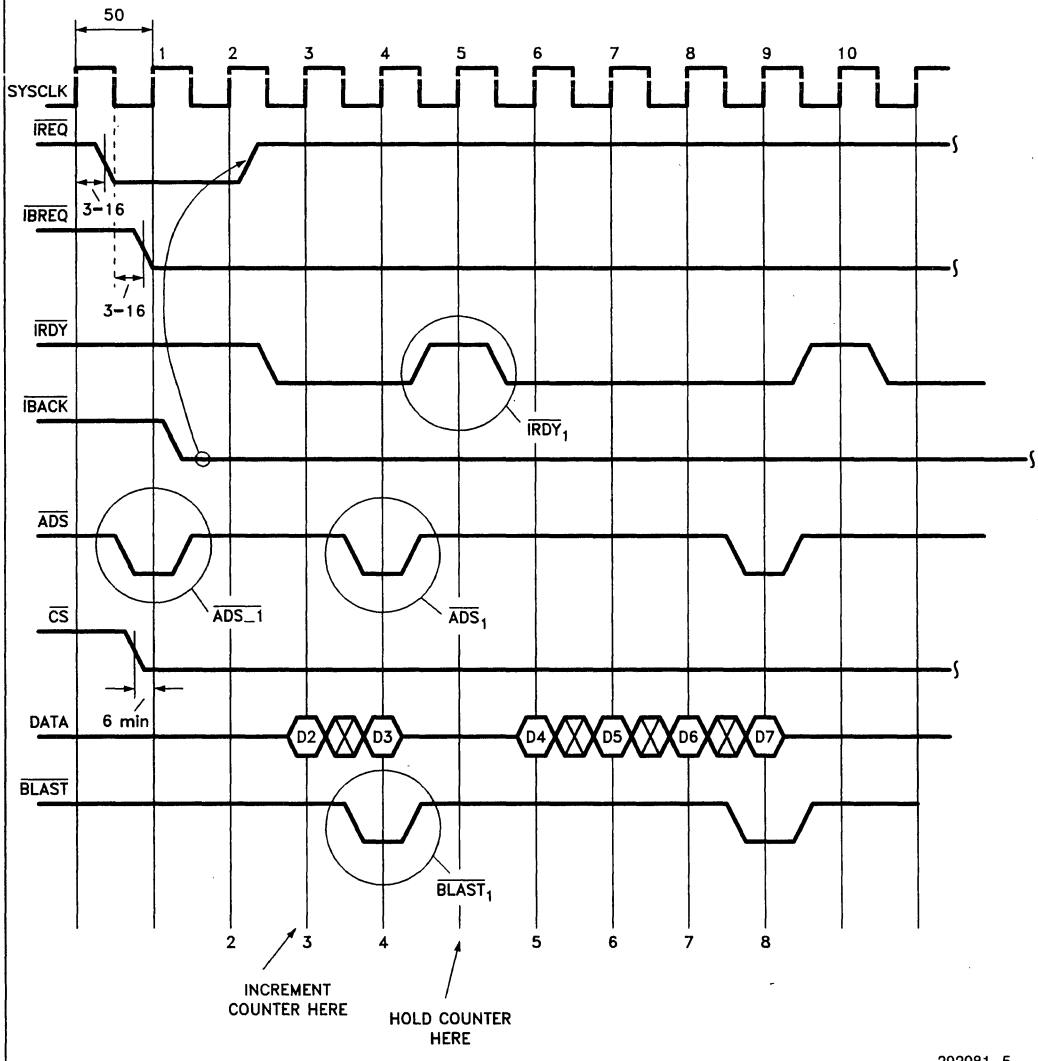
If the initial address of the burst access is non-divisible by 4, i.e., A_1A_0 = 01, then the first burst access will consist of 3 words. To avoid wrap-around of the data from the EPROMs, $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the third word of the first burst access. For the remaining burst accesses $\overline{ADS}$, $\overline{BLAST}$ and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 01, $\overline{ADS}$, $\overline{IRDY}$, and $\overline{BLAST}$ are designated as $\overline{ADS_2}$, $\overline{IRDY_2}$, and $\overline{BLAST_2}$. See Figure 3B for the timing diagram.



NOTES:
The burst EPROM will support a burst access of 4 words.
If A_1 A_0 = 01, then the first burst access will consist of 3 words. To avoid wrap-around, $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the third word of the first burst access. For the remaining burst accesses, $\overline{ADS}$, $\overline{BLAST}$ and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 01, $\overline{ADS}$, $\overline{BLAST}$, and $\overline{IRDY}$ are designated as $\overline{ADS_2}$, $\overline{BLAST_2}$, and $\overline{IRDY_2}$.

Figure 3B. 29000/27960C1-20 Timing Diagram Showing Burst Operation (Address of the First Word is Non-Divisible by 4; A_1A_0 = 01)

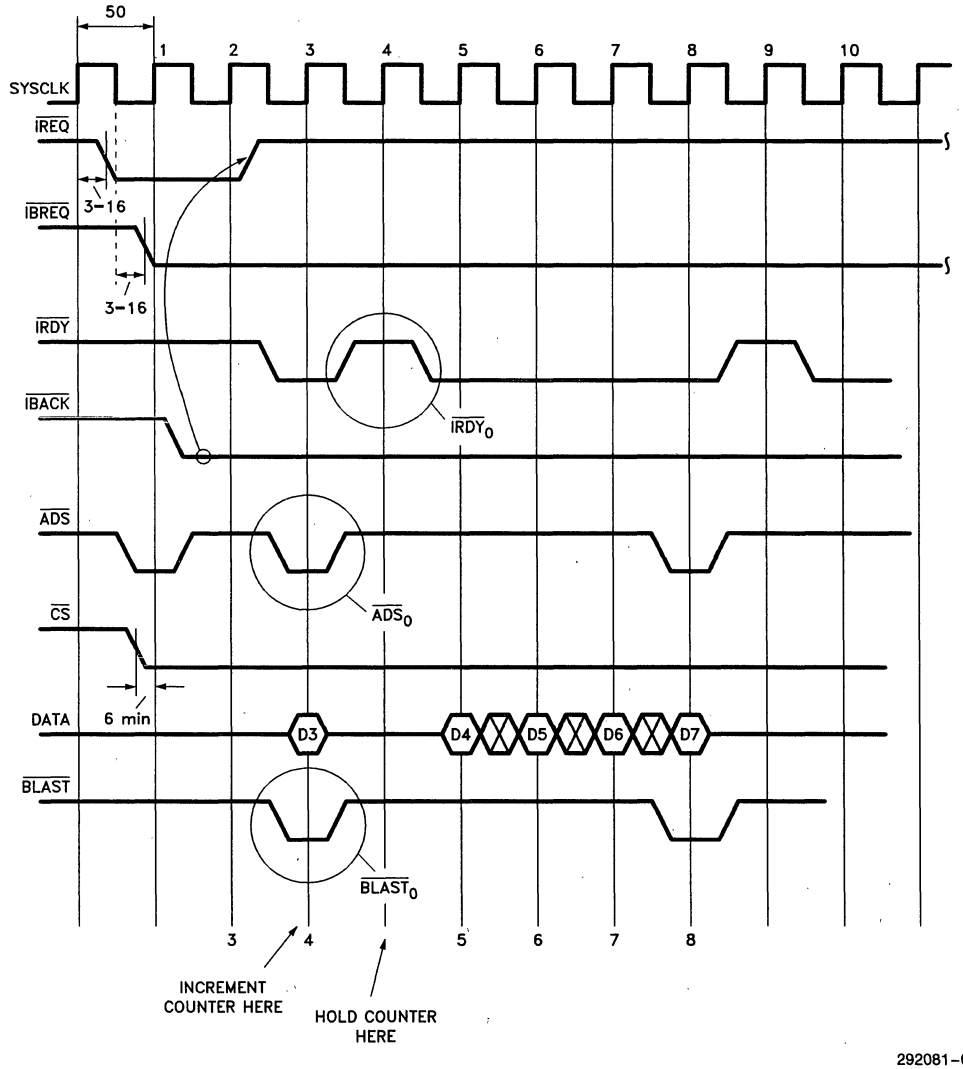
If the initial address of the burst access is non-divisible by 4, i.e., A_1A_0 = 10, then the first burst access will consist of 2 words. To avoid wrap-around of the data from the EPROMs, $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the second word of the first burst access. For the remaining burst accesses $\overline{ADS}$, $\overline{BLAST}$ and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 10, $\overline{ADS}$, $\overline{IRDY}$, and $\overline{BLAST}$ are designated as $\overline{ADS_1}$, $\overline{IRDY_1}$, and $\overline{BLAST_1}$. See Figure 3C for the timing diagram.



NOTES:
The burst EPROM will support a burst access of 4 words.
If A_1A_0 = 10, then the first burst access will consist of 2 words. To avoid wrap-around, $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the second word of the first burst access. For the remaining burst accesses, $\overline{ADS}$, $\overline{BLAST}$ and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 10, $\overline{ADS}$, $\overline{BLAST}$, and $\overline{IRDY}$ are designated as $\overline{ADS_1}$, $\overline{BLAST_1}$, and $\overline{IRDY_1}$.

Figure 3C. 29000/27960C1-20 Timing Diagram Showing Burst Operation (Address of the First Word is Non-Divisible by 4; A_1A_0 = 10)

If the initial address of the burst access is non-divisible by 4, i.e., A_1A_0 = 11, then the first burst access will consists of 1 word. To avoid wrap-around of the data from the EPROMs, $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the first word of the first burst access. For the remaining burst accesses $\overline{ADS}$, $\overline{BLAST}$ and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 11, $\overline{ADS}$, $\overline{IRDY}$, and $\overline{BLAST}$ are designated as $\overline{ADS_0}$, $\overline{IRDY_0}$, and $\overline{BLAST_0}$. See Figure 3D for the timing diagram.



NOTES:
The burst EPROM will support a burst access of 4 words.
If A_1A_0 = 11, then the first burst access will consist of 1 word. To avoid wrap-around $\overline{ADS}$ and $\overline{BLAST}$ are asserted on the first word of the first burst access. For the remaining burst accesses $\overline{ADS}$, $\overline{BLAST}$, and $\overline{IRDY}$ are asserted at regular intervals every 5 clock cycles. When A_1A_0 = 11, $\overline{ADS}$, $\overline{BLAST}$, and $\overline{IRDY}$ are designated as $\overline{ADS_0}$, $\overline{BLAST_0}$, and $\overline{IRDY_0}$.

Figure 3D. 29000/27960C1-20 Timing Diagram Showing Burst Operation (Address of the First Word is Non-Divisible by 4; A_1A_0 = 11)

5.4 $\overline{\text{BLAST}}$ Generation

The $\overline{\text{BLAST}}$ signal is derived by ANDing $\overline{\text{BLAST\_S}}$ and $\overline{\text{BLAST}}_N$. $\overline{\text{BLAST\_S}}$ is generated by ORing $\overline{\text{IBACK\_D}}$ and $\overline{\text{IBREQ\_D}}$ (see Figure 1). $\overline{\text{IBACK\_D}}$ is a delayed version of $\overline{\text{IBACK}}$. $\overline{\text{BLAST\_S}}$ is generated in response to burst access being suspended by the processor (see Figure 4). $\overline{\text{BLAST}}_N$ (N = 0 to 3) is generated at regular intervals at every 5 clock cycles, whose timing depends on initial burst address as explained above for the $\overline{\text{ADS}}$ case. $\overline{\text{BLAST}}_N$ has the same timing as $\overline{\text{ADS}}_N$.

$$\overline{\text{BLAST\_S}} = \overline{\text{IBACK\_D}} + \text{IBREQ\_D}$$

$$\text{BLAST}_N = \text{BLAST}_0 \bullet A_1 \bullet A_0 + \text{BLAST}_1 \bullet A_1 \bullet \overline{A_0} + \text{BLAST}_2 \bullet \overline{A_1} \bullet A_0 + \text{BLAST}_3 \bullet \overline{A_1} \bullet \overline{A_0}$$

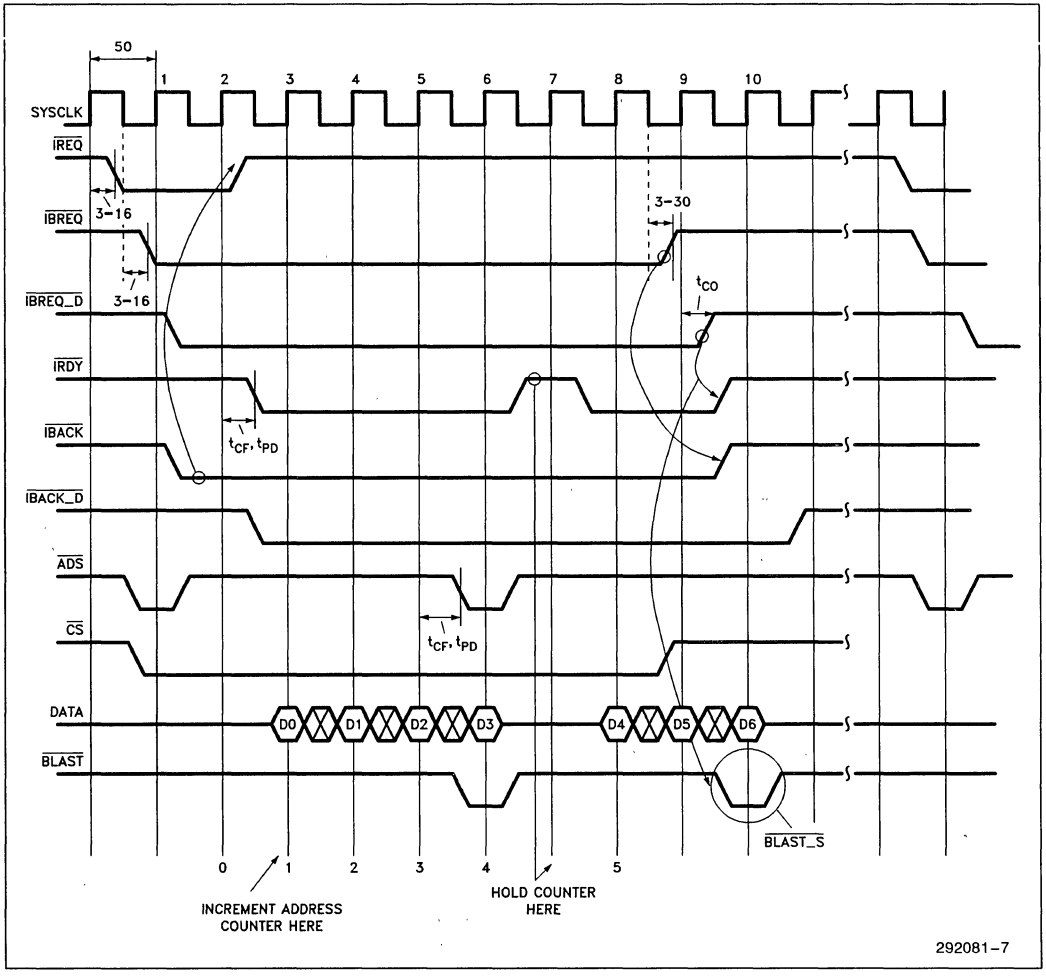


Figure 4. 29000/27960C1-20 Timing Diagram Showing Burst Suspended by Master and Later Preempted by Slave

5.5 $\overline{LD}$ Generation

$\overline{LD}$ has the same timing as $\overline{ADS\_i}$. $\overline{LD}$ is used to load the 8-bit counter.

$$\overline{LD} = \overline{IREQ} + IBREQ\_D$$

5.6 $\overline{IRDY}$ Generation

$\overline{IRDY_N}$ (N = 0 to 3) is asserted in the clock cycle when the burst EPROM is ready to output the first word, i.e., after the number of wait-states (1 or 2) have expired, and is de-asserted after the fourth word. $\overline{IRDY}$ is asserted appropriately based on the state of A_1A_0 as explained above.

$$IRDY_N = (IRDY_0 \bullet A_1 \bullet A_0 + IRDY_1 \bullet A_1 \bullet \overline{A_0} + IRDY_2 \bullet \overline{A_1} \bullet A_0 + IRDY_3 \bullet \overline{A_1} \bullet \overline{A_0}) \bullet IBREQ\_D \bullet \overline{BINV\_D}$$

$$IRDY_0 = X + \overline{Y} + Z$$

$$IRDY_1 = \overline{X} + \overline{Y} + Z$$

$$IRDY_2 = X + Y + \overline{Z}$$

$$IRDY_3 = X + Y + Z$$

5.7 $\overline{IBACK}$ Generation

$\overline{IBACK}$ is asserted in the clock cycle following $\overline{IBREQ}$. $\overline{IBACK}$ is a registered output from the PAL.

$$IBACK := IBREQ \bullet CS \bullet \overline{DBACK}$$

5.8 $\overline{CS}$ Generation

Intel's 85C508 Decoder/Latch PLD is used to generate the chip selects for the EPROMs. This device has 16 dedicated inputs for address/data bus decoding and 8 latched outputs. The burst EPROM requires a minimum of 5 ns/6 ns chip select setup time in the clock cycle during which the addresses are latched. The 85C508 PLD provides plenty of margin for $\overline{CS}$ setup as shown in Figure 5. The multiple chip selects for the various banks can be gated together to provide a single $\overline{CS}$ input to the PAL.

$$CS = IREQ \bullet \overline{IREQT} \bullet A_{31} \bullet A_{29} \bullet A_{28}$$

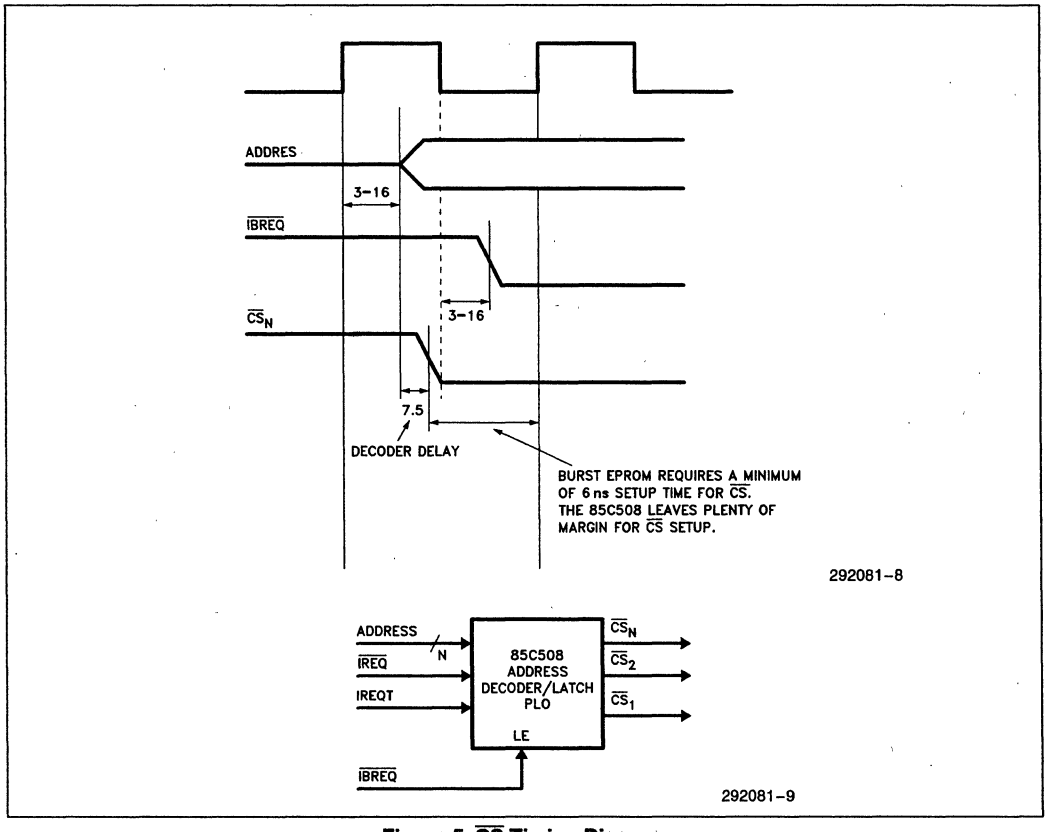


Figure 5. $\overline{CS}$ Timing Diagram

APPENDIX A

1. A.C. parameters and timing waveforms for the 27960CX burst EPROM and the Am29000 microprocessor.

ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature .....0°C to +70°C(8)

Case Temperature
under Bias .....−10°C to +80°C(8)

Storage Temperature .....−65°C to +125°C

All Input or Output Voltages
with Respect to Ground .....−0.6V to +6.5V(4)

Voltage on Pin A_9
with Respect to Ground.....−0.6V to +13V(4)

V_{PP} Supply Voltage
with Respect to Ground.....−0.6V to +14V(4)

V_{CC} Supply Voltage
with Respect to Ground.....−0.6V to +7V(4)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS 0°C < T_A +70°C, V_{CC} = 5V ±10%, TTL Inputs

Symbol	Parameter		Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Load Current				1	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				10	μA	V_{OUT} = 5.5V
I_{PP}	V_{PP} Load Current Read				10	μA	V_{PP} = 0 to V_{CC}, $\overline{PGM}$ = V_{IH}
I_{SB}	V_{CC} Standby	Switching	2		45	mA	$\overline{CS}$ = V_{IH}, f = 33 MHz
		Stable	2		30	mA	$\overline{CS}$ = V_{IH}
I_{CC}	V_{CC} Active Current		1, 3, 7		125	mA	$\overline{CS}$ = V_{IL}, f = 33 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage		4	−0.5	0.8	V	
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		5	V_{CC} − 0.8		V	I_{OH} = −100 μA
			5	2.4		V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit		6		100	mA	

NOTES:
1. Maximum value is with outputs unloaded.
2. I_{CC} standby current assumes no output loading i.e., I_{OH} = I_{OL} = 0 mA.
3. I_{CC} is the sum of current through V_{CC3} + V_{CC4} and does not include the current through V_{CC} and V_{CC2}. (V_{CC1} and V_{CC2} supply power to the output drivers. V_{CC3} and V_{CC4} supply power to the reset of the device.)
4. Minimum D.C. input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns.
5. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
6. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
7. I_{CC} max measured with a 0.11 μF capacitor between V_{CC} and V_{SS}.
8. This specification defines commercial product operating temperatures.

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name, e.g., (CLK, $\overline{ADS}$, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated for the fourth character. The list below shows character representations.

A: Address
B: $\overline{BLAST}$
C: Clock
H: Logic High Level
L: $\overline{ADS}$/Logic Low Level
P: V_{PP} Programming Voltage
X: No longer a valid "driven" logic level
R: $\overline{RESET}$
Q: Data
S: $\overline{CS}$
t: Time
V: Valid
Z: High-Z Level

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AC CHARACTERISTICS: READ OPERATION $0°C < T_A < +70°C$, $V_{CC} = 5V \pm 10\%$

Product Name				27960C2-33		27960C2-25		27960C1-20		27960C1-16		Units
Read Timing				33 MHz 2 Wait State		25 MHz 2 Wait State		20 MHz 1 Wait State		16 MHz 1 Wait State		
No.	Symbol	Parameter	Notes	Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{AVC_0H}	Address Valid to CLK High	CLK0	12		10		14		22		ns
2	t_{C_NHAX}	CLK High to Address Invalid	2	0		0		0		0		ns
3	t_{LLCH}	$\overline{ADS}$ Low to CLK High		8		8		14		22		ns
4	t_{CHLH}	CLK High to $\overline{ADS}$ High	5	6	22	6	32	6	36	6	40	ns
5	t_{SVCH}	$\overline{CS}$ Valid to CLK High	1	7		7		6		14		ns
6	t_{C_NHSX}	CLK High to $\overline{CS}$ Valid	2	0		0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		27		30		35		40	ns
8	t_{CHQX}	CLK High to Data Invalid		5		5		5		5		ns
9	t_{CHQZ}	CLK High to Data High-Z	6		25		30		30		30	ns
10	t_{BVCH}	$\overline{BLAST}$ Valid to CLK High		8		8		14		22		ns
11	t_{CHBX}	CLK High to $\overline{BLAST}$ Invalid	3	6	22	6	32	6	36	6	40	ns

NOTES:

1. Valid signal level is meant to be either a logic high or logic low.
2. T_{C_NHSX}—The subscript N represents the number of wait states for this parameter. $\overline{CS}$ can be de-asserted (high) after the number of wait states (N) has expired. The EPROM will continue to burst out data for the current cycle.
3. BLAST# must be returned high before the next rising clock edge.
4. The sum of $T_{CHQV} + T_{AVCH} +$ NCLK will not equal actual T_{AVQV} if independent test conditions are used to obtain T_{AVCH} and T_{CHQV} (N = number of wait states).
5. $\overline{ADS}$ must be returned high before the next rising clock edge.
6. Sampled but not 100% tested. The transition is measured ±500 mV from steady state voltage.
7. For capacitive loads above 80 pF, T_{CHQV} can be derated by 1 ns/20 pF.

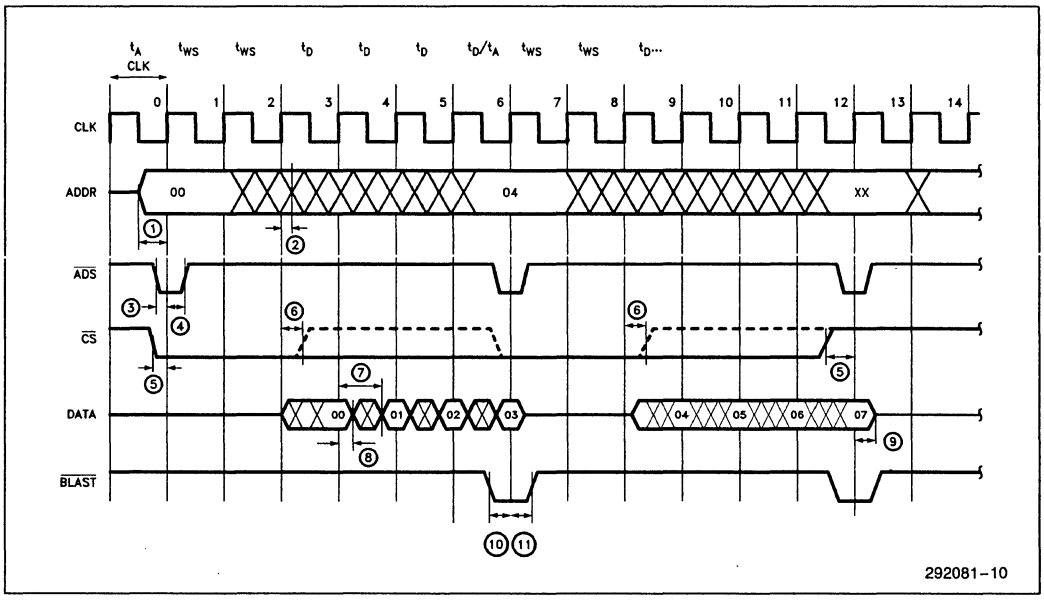

Figure 10. 27960CX Pipelined 2 Wait State A.C. Waveforms

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to GND	−0.5 to V_{CC} +0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +85°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Military Devices

Case Temperature (T_C)*	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*measured "instant on"

DC CHARACTERISTICS over COMMERCIAL and MILITARY operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage		−0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILSYSCLK}$	SYSCLK Input Low Voltage		−0.5	0.8	V
$V_{IHSYSCLK}$	SYSCLK Input High Voltage		V_{CC} −0.8	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except SYSCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for All Outputs except SYSCLK	I_{OH} = −400 µA	2.4		V
I_{LI}	Input Leakage Current	0.45V ≤ V_{IN} ≤ V_{CC} −0.45V		±10	µA
I_{LO}	Output Leakage Current	0.45V ≤ V_{OUT} ≤ V_{CC} −0.45V		±10	µA
I_{CCOP}	Operating Power-Supply Current	V_{CC} = 5.25V, Outputs Floating; Holding $\overline{\text{RESET}}$ active with externally supplied SYSCLK		22 for Commercial 25 for Military	mA/MHz
V_{OLC}	SYSCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	SYSCLK Output High Voltage	I_{OHC} = 20 mA	V_{CC} −0.6		V
I_{OSGND}	SYSCLK GND Short Circuit Current	V_{CC} = 5.0 V	100		mA
I_{OSVCC}	SYSCLK V_{CC} Short Circuit Current	V_{CC} = 5.0 V	100		mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	fC = 1 MHz (Note 1)		15	pF
C_{INCLK}	INCLK Input Capacitance			20	pF
C_{SYSCLK}	SYSCLK Capacitance			90	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note: 1. Not 100% tested.

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Description	Test Conditions	33 MHz Min.	33 MHz Max.	25 MHz Min.	25 MHz Max.	Unit
1	System Clock (SYSCLK) Period (T)	Note 1			40	1000	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 13			0.5T−1	0.5T+1	ns
2	SYSCLK High Time when used as input	Note 13			19		ns
3	SYSCLK Low Time when used as input	Note 13			17		ns
4	SYSCLK Rise Time	Note 2				5	ns
5	SYSCLK Fall Time	Note 2				5	ns
6	Synchonous SYSCLK Output Valid Delay	Notes 3, 12			3	14	ns
6A	Synchronous SYSCLK Output Valid Delay for D_{31}–D_0	Note 12			4	18	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 4, 14, 15			3	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 5, 12			3	14	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 5, 14, 15			3	30	ns
9	Synchronous Input Setup Time	Note 7			12		ns
9A	Synchronous Input Setup Time for D_{31}–D_0, I_{31}–I_0				6		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$				13		ns
10	Synchronous Input Hold Time	Note 6			2		ns
11	Asynchronous Input Minimum Pulse Width	Note 8			T+10		ns
12	INCLK Period				20	500	ns
12A	INCLK to SYSCLK Delay				2	10	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay				2	10	ns
13	INCLK Low Time				8		ns
14	INCLK High Time				8		ns
15	INCLK Rise Time					5	ns
16	INCLK Fall Time					5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 9			0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 10			4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 12			1	7	ns
20	Three-State synchronous SYSCLK output invalid delay for D_{31}–D_0	Notes 11, 14, 15			3	20	ns

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Am29000™

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PRELIMINARY

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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

No.	Parameter Description	Test Conditions	20 MHz Min.	20 MHz Max.	16 MHz Min.	16 MHz Max.	Unit
1	System Clock (SYSCLK) Period (T)	Note 1	50	1000	60	1000	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 13	0.5T−1	0.5T+1	0.5T−2	0.5T+2	ns
2	SYSCLK High Time when used as input	Note 13	22		27		ns
3	SYSCLK Low Time when used as input	Note 13	19		22		ns
4	SYSCLK Rise Time	Note 2		5		5	ns
5	SYSCLK Fall Time	Note 2		5		5	ns
6	Synchonous SYSCLK Output Valid Delay	Notes 3, 12	3	16	3	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D_{31}–D_0	Note 12	4	20	4	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 4, 14, 15	3	30	3	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 5, 12	3	16	3	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 5, 14, 15	3	30	3	30	ns
9	Synchronous Input Setup Time	Note 7	15		15		ns
9A	Synchronous Input Setup Time for D_{31}–D_0, I_{31}–I_0		8		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		16		16		ns
10	Synchronous Input Hold Time	Note 6	2		2		ns
11	Asynchronous Input Minimum Pulse Width	Note 8	T+10		T+10		ns
12	INCLK Period		25	500	30	500	ns
12A	INCLK to SYSCLK Delay		2	12	2	15	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	12	2	15	ns
13	INCLK Low Time		10		12		ns
14	INCLK High Time		10		12		ns
15	INCLK Rise Time			5		5	ns
16	INCLK Fall Time			5		5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 9	0	5	0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 10	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 12	1	8	1	9	ns
20	Three-State synchronous SYSCLK output invalid delay for D_{31}–D_0	Notes 11, 14, 15	3	25	3	25	ns

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PRELIMINARY

SWITCHING CHARACTERISTICS over MILITARY operating range

No.	Parameter Description	Test Conditions	20 MHz Min.	20 MHz Max.	16 MHz Min.	16 MHz Max.	Unit
1	System Clock (SYSCLK) Period (T)	Note 1	50	1000	60	1000	ns
1A	SYSCLK at 1.5V to $\overline{\text{SYSCLK}}$ at 1.5V when used as an output	Note 13	0.5T−1	0.5T+1	0.5T−2	0.5T+2	ns
2	SYSCLK High Time when used as input	Note 13	22		27		ns
3	SYSCLK Low Time when used as input	Note 13	19		22		ns
4	SYSCLK Rise Time	Note 2		5		5	ns
5	SYSCLK Fall Time	Note 2		5		5	ns
6	Synchonous SYSCLK Output Valid Delay	Notes 3, 12	3	16	3	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D_{31}–D_0	Note 12	4	20	4	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	Notes 4, 14, 15	3	30	3	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	Notes 5, 12	3	16	3	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	Notes 5, 14, 15	3	30	3	30	ns
9	Synchronous Input Setup Time	Note 7	15		15		ns
9A	Synchronous Input Setup Time for D_{31}–D_0, I_{31}–I_0		8		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		16		16		ns
10	Synchronous Input Hold Time	Note 6	2		2		ns
11	Asynchronous Input Minimum Pulse Width	Note 8	T+10		T+10		ns
12	INCLK Period		25	500	30	500	ns
12A	INCLK to SYSCLK Delay			12		15	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay			12		15	ns
13	INCLK Low Time		10		12		ns
14	INCLK High Time		10		12		ns
15	INCLK Rise Time			5		5	ns
16	INCLK Fall Time			5		5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	Note 9	0	5	0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	Note 10	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	Note 12	1	8	1	9	ns
20	Three-State synchronous SYSCLK output invalid delay for D_{31}–D_0	Notes 11, 14, 15	4	25	4	25	ns

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PRELIMINARY

Notes:

1. AC measurements made relative to 1.5 V, except where noted.
2. SYSCLK rise and fall times measured between 0.8 V and (V_{CC} – 1.0 V).
3. Synchronous Outputs relative to SYSCLK rising edge include: A_{31}–A_0, $\overline{BGRT}$, $R/\overline{W}$, $SUP/\overline{US}$, $\overline{LOCK}$, $MPGM_1$–$MPGM_0$, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, $DREQT_1$–$DREQT_0$, $\overline{PDA}$, OPT_2–OPT_0, $STAT_2$–$STAT_0$, and MSERR.
4. Three-state Synchronous Outputs relative to SYSCLK rising edge include: A_{31}–A_0, $R/\overline{W}$, $SUP/\overline{US}$, $\overline{LOCK}$, $MPGM_1$–$MPGM_0$, $\overline{IREQ}$, IREQT, $\overline{PIA}$, $\overline{DREQ}$, $DREQT_1$–$DREQT_0$, $\overline{PDA}$, and OPT_2–OPT_0.
5. Synchronous Outputs relative to SYSCLK falling edge ($\overline{SYSCLK}$): $\overline{IBREQ}$, $\overline{DBREQ}$.
6. Synchronous Inputs include: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{DERR}$, $\overline{DBACK}$, $\overline{CDA}$, I_{31}–I_0, $\overline{DRDY}$, and D_{31}–D_0.
7. Synchronous Inputs include: $\overline{BREQ}$, $\overline{PEN}$, $\overline{IRDY}$, $\overline{IERR}$, $\overline{IBACK}$, $\overline{DERR}$, $\overline{DBACK}$, and $\overline{CDA}$.
8. Asynchronous Inputs include: $\overline{WARN}$, $\overline{INTR_3}$–$\overline{INTR_0}$, $\overline{TRAP_3}$–$\overline{TRAP_0}$, and $CNTL_1$–$CNTL_0$.
9. $\overline{RESET}$ is an asynchronous input on assertion/deassertion. As an option to the user, $\overline{RESET}$ deassertion can be used to force the state of the internal divide-by-two flip-flop to synchronize the phase of SYSCLK (if internally generated) relative to $\overline{RESET}$/INCLK.
10. $\overline{WARN}$ has a minimum pulse width requirement upon deassertion.
11. To guarantee Store/Load with one-cycle memories, D_{31}–D_0 must be asserted relative to SYSCLK falling edge from an external drive source.
12. Refer to Capacitive Output Delay table when capacitive loads exceed 80 pF.
13. When used as an input, SYSCLK presents a 90-pF max. load to the external driver. When SYSCLK is used as an output, timing is specified with an external load capacitance of ≤ 200 pF.
14. Three-State Output Inactive Test Load. Three-State Synchronous Output Invalid Delay is measured as the time to a ±500 mV change from prior output level.
15. When a three-state output makes a synchronous transition from a valid logic level to a high-impedance state, data is guaranteed to be held valid for an amount of time equal to the lesser of the minimum Three-State Synchronous Output Invalid Delay and the minimum Synchronous Output Valid Delay.

Conditions:

a. All inputs/outputs are TTL compatible for V_{IH}, V_{IL}, V_{OH}, and V_{OL} unless otherwise noted.
b. All output timing specifications are for 80 pF of loading.
c. All setup, hold, and delay times are measured relative to SYSCLK or INCLK unless otherwise noted.
d. All input Low levels must be driven to 0.45 V and all input High levels must be driven to 2.4 V except SYSCLK.

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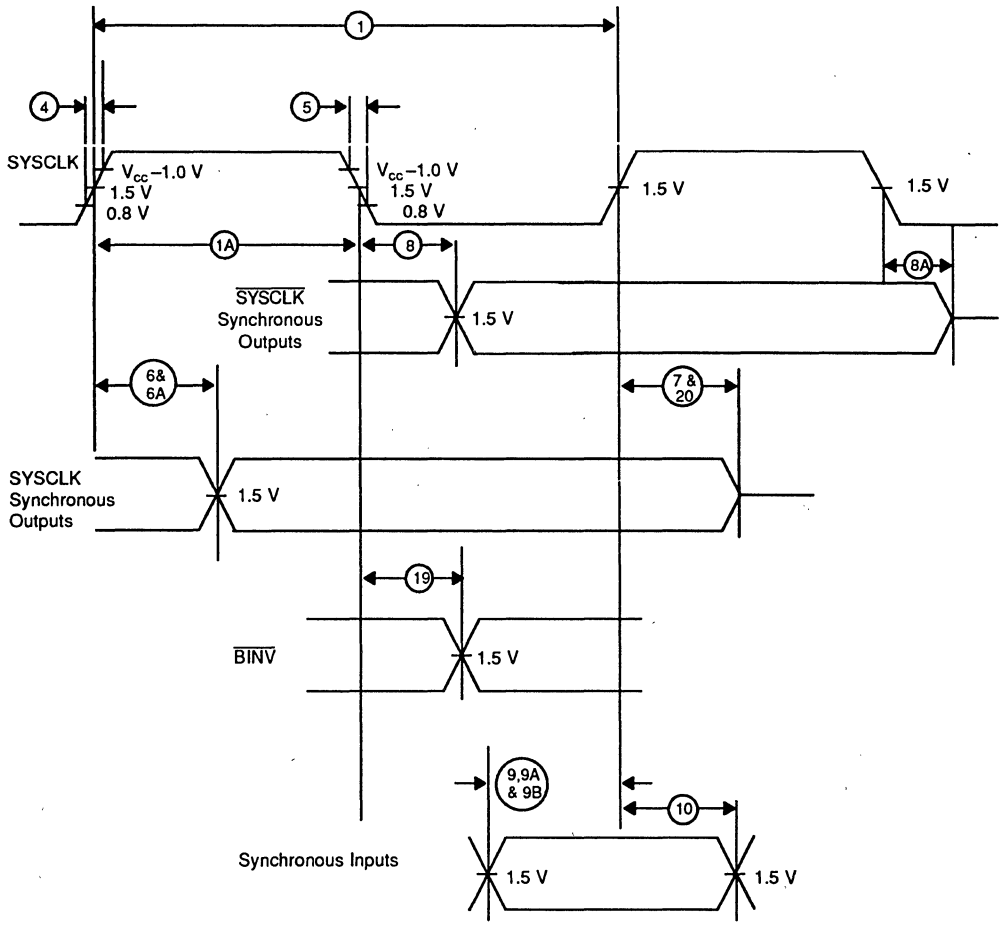
SWITCHING WAVEFORMS



Relative to SYSCLK

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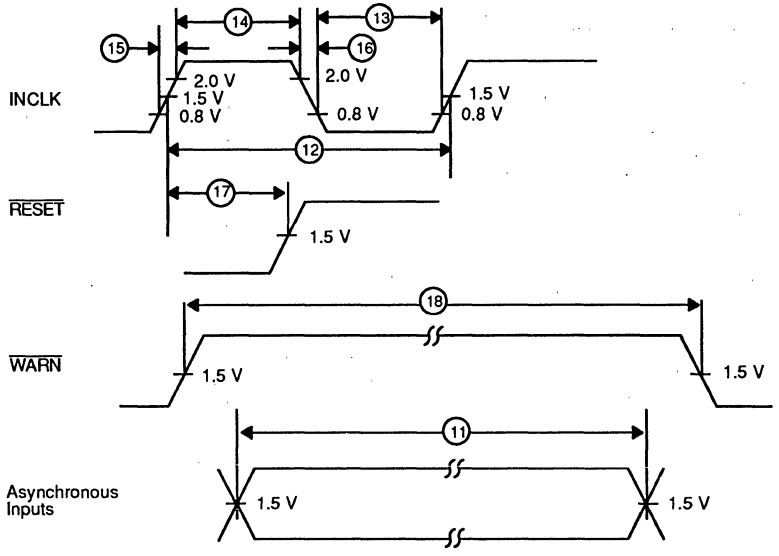
SWITCHING WAVEFORMS



INCLK and Asynchronous Inputs

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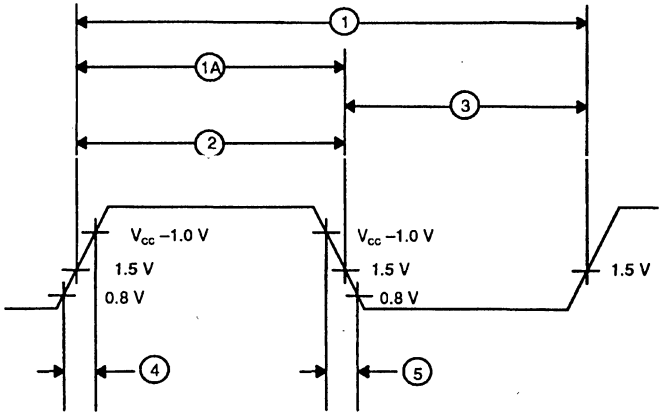
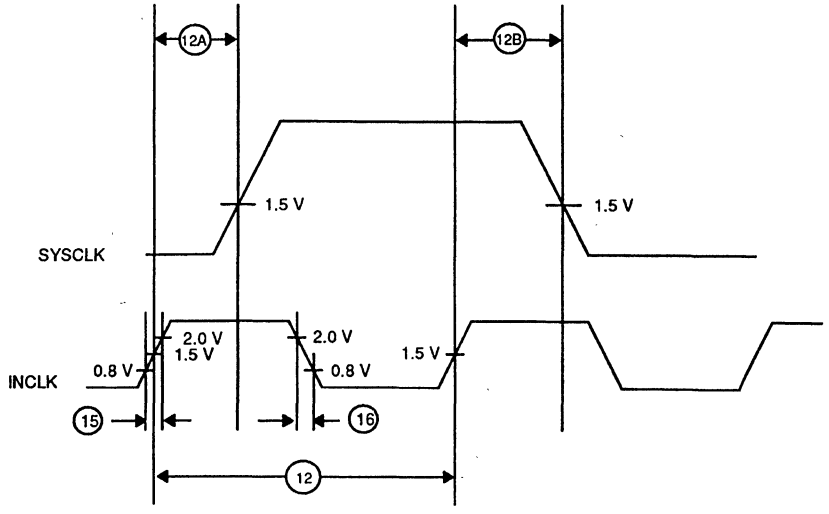
SWITCHING WAVEFORMS



SYSCLK Definition



INCLK to SYSCLK Delay

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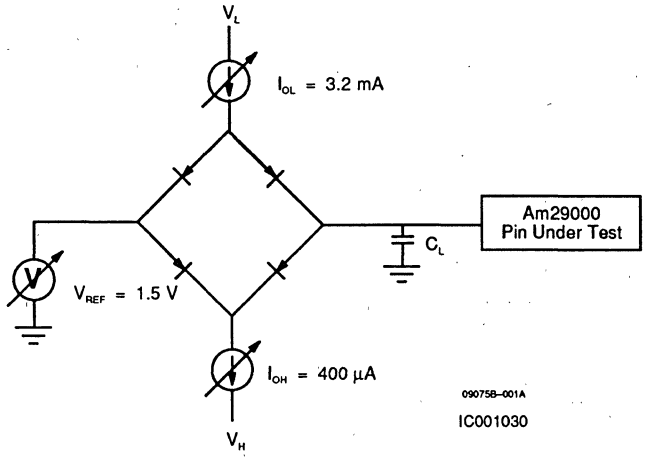
Capacitive Output Delays

For loads greater than 80 pF

This table describes the additional output delays for capacitive loads greater than 80 pF. Values in the Maximum Additional Delay column should be added to the value listed in the Switching Characteristics table. For loads less than or equal to 80 pF, refer to the delays listed in the Switching Characteristics table.

No.	Parameter Description	Total External Capacitance	Maximum Additional Delay
6	Synchronous SYSCLK Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
6A	Synchronous SYSCLK Output Valid Delay for D_{31}–D_0	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +6 ns +10 ns +15 ns +19 ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +3 ns +4 ns +6 ns +7 ns

SWITCHING TEST CIRCUIT



C_L is guaranteed to 80 pF. For capacitive loading greater than 80 pF, refer to the Capacitive Output Delay table.

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PRELIMINARY

November 1990

EPROM RELIABILITY DATA SUMMARY

Order Number: 210473-007

INTEL EPROM RELIABILITY DATA SUMMARY

CONTENTS

THE IMPORTANCE OF RELIABILITY

Reliability of the non-volatile memories in your end product is critical to your total system reliability. The use of Intel EPROMs can make a difference. Reliability is not just tested, but designed into each component Intel manufactures.

QUALITY ≠ RELIABILITY

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product. While Intel is a quality leader, we also adhere to stringent reliability standards which we have established for ourselves.

Consider Quality vs. Reliability

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end user of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

MONITOR PROGRAM

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is a proven tool that Intel has used for seven years and is now available to its customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. But it's much more than burn-in and device testing. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program. It is the most comprehensive reliability program anywhere.

The paramount objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts—and the performance—that they ordered by specifying Intel. Reliability qualification assures that all new production meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained, day in, day out, over the duration of a device's life. This reliability improves the lifetime reputation of your product, reducing the required number of field service calls.

EPROM RELIABILITY DATA SUMMARY

Intel routinely publishes this "EPROM Reliability Data Summary", a continuing update of reliability information covering Intel's entire EPROM product line. This document includes a discussion on EPROM reliability testing methodology and the most current failure rate calculations, failure analyses and lifetest results.

Intel's commitment to the reliability of our products is clearly reflected in the information we make available to customers. We believe that supplying detailed reliability information to our customers is part of the total solution Intel offers, and is an important part of Intel's leadership in microelectronics technology.

EPROM RELIABILITY TESTING

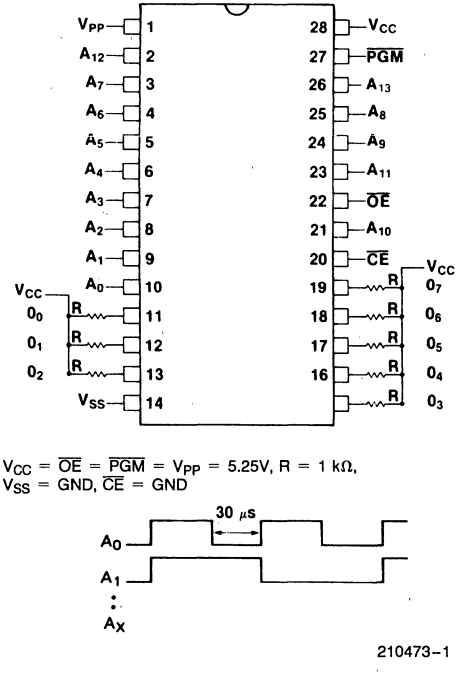
Intel EPROMs undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and/or during ongoing monitor checks. Where testing differs for plastic packaged production EPROMs, it is so noted.

Intel continually reviews its testing procedures and makes improvements to its methodology whenever overall reliability can be enhanced. Our goal is to be the industry leader in delivering reliable parts and no compromises are accepted.

Information on Intel's reliability testing procedures follows.

High Temperature Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test the memory is sequentially addressed and the outputs are exercised, but not monitored or loaded. A checkerboard data pattern is used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with the failure analysis.

In order to best determine long-term failure rate, all devices used for lifetesting are first subjected to standard INTEL testing. The 48 hour burn-in results are an indication of infant mortality. These results are not included in the failure rate calculation. (See Figure 1 for typical burn-in bias and timing diagrams.)



NOTE:
Alternate Configuration is the same as Figure 3.
Binary Sequence From A_0 to A_X
O_0–O_7 may be N/C

Figure 1. 2764A Burn-In Bias and Timing Diagrams

Failure Rate Calculations—Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy[1,2,3,4] and the Arrhenius Plot as shown in Figure 2*. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. To arrive at a confidence level associated failure rate, the failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Devices submitted to stresses other than lifetest received a 168 hour lifetest prior to stressing.

*The activation energies for various failure mechanisms are listed in Table 1. For an explanation of this plot, see Appendix A.

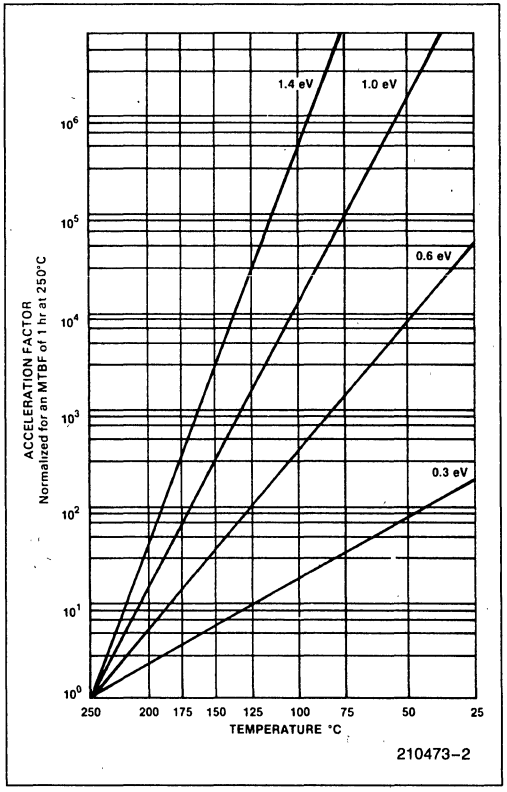


Figure 2. Arrhenius Plot

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mechanism	Each
Oxide	0.3
SBCL/SBCG/MBCL/MBCG	0.6
Contamination	1.0
Speed Degradation	0.3–1.0
Intrinsic Charge Loss	1.4

Failure Definitions

Oxide—An Oxide Failure Related Fault
SBCL—Single Bit Charge Loss
SBCG—Single Bit Charge Gain
MBCL—Multiple Bit Charge Loss
MBCG—Multiple Bit Charge Gain
Contamination—Ionic Contamination Failure
Speed Degradation—Device Speed Degraded Over Test

A typical lifetest bias and timing diagram is shown in Figure 3.

High Temperature 6.5V Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic life test except V_{CC} and V_{PP} are at 6.5V. The acceleration factor due to this test can be found in Figure 4. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 98%+ programmed pattern to a 250°C bake (140° for plastic) with no applied bias. In addition to data retention, this test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability. This test is sometimes referred to as *Data Retention Bake Test.*

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. Two hundred cycles are performed with a complete cycle taking 20 minutes. This test is to detect mechanical reliability problems and microcracks.

ESD Testing—This test is performed to validate the products tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks on appropriate pins. Two types of tests are performed. First, all devices are tested using Mil STD 883 test criteria. In addition, a charged device test is performed to further validate protection occurring during mechanical handling.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is a distinct part of a product qual. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products.

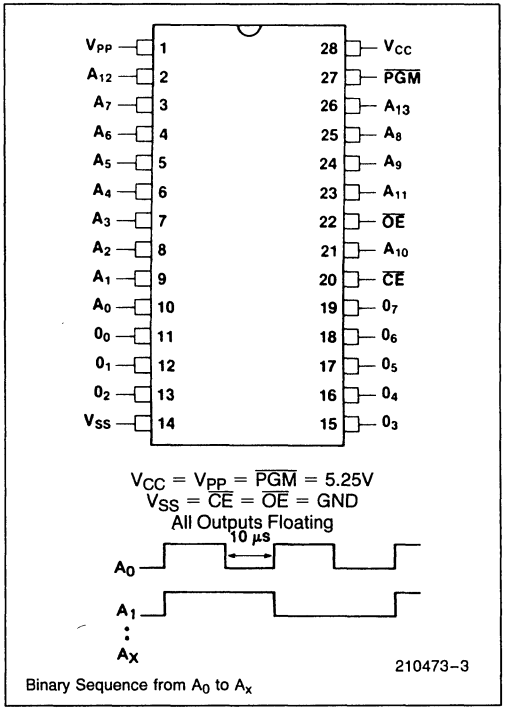


Figure 3. 2764A Lifetest Bias and Timing Diagram

Type	Supply Voltage (Volts)	Oxide Thickness (A)	Operating Stress (MV/cm)	Acceleration Factor at __% Over Stress				
				10%	20%	30%	50%	100%
HMOS E	5	700	0.714	3.2	10	32	3.2E+2	1.0E+5
HMOS II E	5	400	1.25	7.5	55	422	2.4E+4	5.6E+8
CHMOS II E	5	400	1.25	7.5	55	422	2.4E+4	5.6E+8

ASSUMES:
1. No bias generators
2. Depletion loads
3. Failure rate calculations use the appropriate acceleration factor for stress voltage and maximum operating voltage (conservative).

Figure 4. Time-Dependent Oxide Failure Acceleration

*HMOS and CHMOS are patented processes of Intel Corporation.

REFERENCES

1. S. Rosenberg, D. Crook, B. Euzent, "16th Annual Proceedings of the International Reliability Physics Symposium," pp 19–25, 1978.
2. J. Caywood, B. Euzent, B. Shiner, "Data Retention in EPROMs," 1980 IEEE International Reliability Physics Symposium.
3. S. Rosenberg, B. Euzent, "HMOS Reliability" Reliability Report RR-18, INTEL Corporation, 1979.
4. N. Mielke, "New EPROM Data-Loss Mechanisms," 1983. International Reliability Physics Symposium.
5. R.M. Alexander, "Calculating Failure Rates From Stress Data," April 1984 International Reliability Physics Symposium.

NOTE:

The methodology for calculating failure rates is detailed in Appendix A.

CERDIP Reliability Data Summary

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates. Data for CERDIP and plastic EPROMs is treated separately.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler problems cause failures to occur. These "failures" are not a result of the specific test just completed. They are removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and these suspected "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

D2732A

The Intel 2732A (CERDIP) is a 32K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM).

Number of Bits: 32,768
Organization: 4K x 8
Pin Out: 24 pin, JEDEC Approved

Die Size: 163 x 97 mil.
Process: HMOS-E
Cell Size: 11.5 x 8.75 μM
Programming Voltage: 21.0V
Technology NMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	3/21982	5/21977	0/2112	0/2111	0/1056	0/1056	0/1055	0/0
1989	0/10998	0/10997	0/192	0/192	0/672	0/672	0/672	0/575
Totals	3/32980	5/32974	0/2304	0/2303	0/1728	0/1728	0/1727	0/575
	A	B						

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	4/2836	1/2830	1/2828	0/858
1989	2/1419	1/1417	0/1031	0/779
Totals	6/4255	2/4247	1/3859	0/1637
	C	D	E	

D2732A (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
5.67×10^6	0.3 B.I.	3.34×10^7	2.16×10^7	1		
1.15×10^6	0.3*VAF	6.55×10^7	4.23×10^7	0		
			Total 0.3 eV Failures =	1	0.0020	0.0032
5.87×10^6	0.6 B.I.	1.90×10^8	7.94×10^7	3		
1.99×10^6	0.6 BAKE	5.46×10^9	2.16×10^9	9		
1.15×10^6	0.6 HVELT	3.72×10^7	1.56×10^7	0		
			Total 0.6 eV Failures =	12	0.0002	0.0006
5.87×10^6	1.0 B.I.	1.93×10^9	4.51×10^8	1		
1.15×10^6	1.0 HVELT	3.79×10^8	8.84×10^7	0		
			Total 1.0 eV Failures =	1	0.0001	0.0004
			Combined Failure Rate:		0.0023	0.0042
			FITs:		23	42

48 Hour Burn-In Infant Mortality: 91 DPM

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	55° C/W	Temp with θ_{ja}				
V_{CC} =	5.50V	T(55) = 347.92°K	BI/ELT	0.3	5.7	3.7
I_{CC} @ 55 =	69 mA	T(70) = 363.79°K	Accel.	0.6	32.4	43.5
I_{CC} @ 70 =	72 mA	T(125) = 421.25°K	Factors:	1.0	329.1	76.8
I_{CC} @ 125 =	80 mA	T(250) = 523.15°K				
			250°C Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 10

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-column charge loss 0.6 eV
2-SBCG 0.6 eV

B. 2-SBCG 0.6 eV
1-ionic contamination 1.0 eV
1-oxide breakdown 0.3 eV
1-line corrosion 0.6 eV

C. 5-SBCL 0.6 eV
1-SBCG 0.6 eV

D. 2-SBCL 0.6 eV

E. 1-SBCL 0.6 eV

5

D2764A

The Intel 2764A (CERDIP) is a 64K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM).

Number of Bits: 65,536
Organization: 8K x 8
Pin Out: 28 pin, JEDEC Approved

Die Size: 98 x 117 mils
Process: HMOS II-E
Cell Size: 6 x 6 μM
Programming Voltage: 12.5V
Technology: NMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/15993	2/15990	0/1536	0/1536	0/768	0/768	1/768	0/0
1989	0/4923	1/4921	0/192	0/192	0/384	0/383	0/383	0/285
Totals	0/20916	3/20911	0/1728	0/1728	0/1152	0/1151	1/1151	0/285
		A					B	

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	6/2063	1/2056	2/2045	0/623
1989	0/645	0/644	0/644	0/234
Totals	6/2708	1/2700	2/2689	0/857
	C	D	E	

D2764A (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
3.95×10^6	0.3 B.I.	2.17×10^7	1.44×10^7	1		
7.18×10^5	0.3*VAF	2.16×10^8	1.43×10^8	1		
			Total 0.3 eV Failures =	1	0.0013	0.0020
3.95×10^6	0.6 B.I.	1.20×10^8	5.25×10^7	2		
1.34×10^6	0.6 BAKE	3.69×10^9	1.46×10^9	9		
7.18×10^5	0.6 HVELT	2.17×10^7	9.55×10^6	0		
			Total 0.6 eV Failures =	11	0.0003	0.0008
3.95×10^6	1.0 B.I.	1.16×10^9	2.95×10^8	0		
7.18×10^5	1.0 HVELT	2.11×10^8	5.36×10^7	0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate:		0.0016	0.0028
			FITs:		16	28

48 Hour Burn-In Infant Mortality: 0 DPM

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	48°C/W	Temp with θ_{ja}	BI/ELT	0.3	5.5	3.6
V_{CC} =	5.50V	T(55) = 340.10°K	Accel.	0.6	30.3	13.3
I_{CC} @55 =	48 mA	T(70) = 354.34°K	Factors:	1.0	294.1	74.6
I_{CC} @70 =	45 mA	T(125) = 408.08°K				
I_{CC} @125 =	40 mA	T(250) = 523.15°K				
			250°C Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-oxide breakdown 0.3 eV
1-MBCL 0.6 eV
1-SBCL 0.6 eV

B. 1-oxide breakdown 0.3 eV

C. 2-MBCL 0.6 eV
3-SBCL 0.6 eV
1-oxygen doner 0.6 eV

D. 1-MBCL 0.6 eV

E. 1-SBCL 0.6 eV
1-MBCL 0.6 eV

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D27128A

The Intel 27128A (CERDIP) is a 128K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). This part differs from the 27128 in that it requires 12.5 Vpp vs. 21.0 Vpp and the process technology is HMOS II-E vs. HMOS-E.

Number of Bits: 131,072
Organization: 16K x 8
Pin Out: 28 pin, JEDEC Approved

Die Size: 169 x 117 mils
Process: HMOS II-E
Cell Size: 6 x 6 μM
Programming Voltage: 12.5V
Technology: NMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/5953	0/5952	0/576	0/576	1/288	0/286	0/286	0/0
1989	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0
Totals	0/5953	0/5952	0/576	0/576	1/288	0/286	0/286	0/0
					A			

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	1/774	0/772	1/771	0/234
1989	0/0	0/0	0/0	0/0
Totals	1/774	0/772	1/771	0/234
	B		C	

D27128A (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
1.19×10^6	0.3 B.I.	6.14×10^6	4.18×10^6	0		
1.43×10^5	0.3*VAF	4.02×10^7	2.74×10^7	0		
			Total 0.3 eV Failures =	0	0.0020	0.0029
1.19×10^6	0.6 B.I.	3.16×10^7	1.46×10^7	0		
3.86×10^5	0.6 BAKE	1.05×10^9	4.17×10^8	2		
1.43×10^5	0.6 HVELT	3.78×10^6	1.75×10^6	1		
			Total 0.6 eV Failures =	3	0.0004	0.0010
1.19×10^6	1.0 B.I.	2.80×10^8	7.78×10^7	0		
1.43×10^5	1.0 HVELT	3.36×10^7	9.32×10^6	0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate:		0.0024	0.0039
			FITs:		24	39

48 Hour Burn-In Infant Mortality: 0 DPM

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	45°C/W	Temp with θ_{ja}	BI/ELT	0.3	5.1	3.5
V_{CC} =	5.50V	T(55) = 346.90°K	Accel.	0.6	26.4	12.3
I_{CC} @55 =	80 mA	T(70) = 360.72°K	Factors:	1.0	234.7	65.1
I_{CC} @70 =	75 mA	T(125) = 414.54°K				
I_{CC} @125 =	70 mA	T(250) = 523.15°K				
			250°C Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-SBCG 0.6 eV
B. 1-SBCL 0.6 eV
C. 1-multi bit charge loss 0.6 eV

D27256

Intel 27256 (CERDIP) is a 256K ultraviolet erasable and Electricaly Programmable Read Only Memory (EPROM).

Number of Bits: 262,144
Organization: 32K x 8
Pin Out: 28 pin, JEDEC Approved

Die Size: 180 x 193 mils
Process: HMOS II-E
Cell Size: 6 x 6 μM
Programming Voltage: 12.5V
Technology: NMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/13954	1/13909	0/1344	1/1344	0/672	0/672	0/633	0/0
1989	3/10715	4/10709	0/384	0/383	0/864	0/864	0/863	0/671
Totals	4/24669	5/24618	0/1728	0/1727	0/1536	0/1536	0/1526	0/671
	A	B						

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	7/1806	8/1799	8/1790	0/545
1989	2/1404	7/1402	5/1395	0/546
Totals	9/3210	15/3201	13/3185	0/1091
	C	D	E	

D27256 (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours 55°C	Equivalent Hours 70°C	# Fail	Fail Rate %/1K Hrs (60% UCL) 55°C	Fail Rate %/1K Hrs (60% UCL) 70°C
4.39×10^6	0.3 B.I.	2.27×10^7	1.54×10^7	2		
1.10×10^6	0.3*VAF	3.10×10^8	2.11×10^8	0		
			Total 0.3 eV Failures =	2	0.0009	0.0014
4.39×10^6	0.6 B.I.	1.17×10^8	5.41×10^7	2		
1.59×10^6	0.6 BAKE	4.37×10^9	1.73×10^9	37		
1.10×10^6	0.6 HVELT	2.94×10^7	1.36×10^7	0		
			Total 0.6 eV Failures =	39	0.0009	0.0023
4.39×10^6	1.0 B.I.	1.05×10^9	2.89×10^8	1		
1.10×10^6	1.0 HVELT	2.62×10^8	7.24×10^7	0		
			Total 1.0 eV Failures =	1	0.0002	0.0006
			Combined Failure Rate:		0.0020	0.0043
			FITs:		20	43

48 Hour Burn-In Infant Mortality: 162 DPM

					Thermal Accel. Factors 55°C	70°C
Theta Ja =	44°C/W	Temp with θ_{ja}				
V_{CC} =	5.50V	T(55) = 346.48°K	BI/ELT	0.3	5.2	3.5
I_{CC} @55 =	80 mA	T(70) = 360.33°K	Accel.	0.6	26.7	12.3
I_{CC} @70 =	75 mA	T(125) = 414.17°K	Factors:	1.0	238.4	65.8
I_{CC} @125 =	70 mA	T(250) = 523.15°K				
			250° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 2-SBCL 0.6 eV
1-ionic breakdown 1.0 eV
1-oxide breakdown 0.3 eV

B. 2-oxide breakdown 0.3 eV
1-package crack 1.0 eV
1-decoder charge loss 0.6 eV
1-single row charge loss 0.6 eV

C. 6-SBCL 0.6 eV
2-clustered bit charge loss 0.6 eV
1-MBCL 0.6 eV

D. 15-SBCL 0.6 eV

E. 5-SBCL 0.6 eV
5-clustered bit charge loss 0.6 eV
3-MBCL 0.6 eV

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D27C256

The Intel 27C256 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM).

Number of Bits: 262,144
Organization: 32K x 8
Pin Out: 28 Pin JEDEC Approved

Die Size: 172 x 176 mils
Process: CHMOS II-E
Cell Size: 6 x 6 μM
Programming Voltage: 12.5V
Technology: CMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	2/14976	1/14973	0/960	0/863	0/432	0/432	0/431	0/0
1989	0/10937	0/10931	0/1055	0/1055	0/864	0/864	0/863	0/0
Totals	2/25913	1/25904	0/2015	0/1918	0/1296	0/1296	0/1294	0/0
	A	B						

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	0/1934	2/1921	0/1401	0/390
1989	0/1418	2/1417	1/1414	0/702
Totals	0/3352	4/3338	1/2815	0/1092
		C	D	

D27C256 (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
4.74×10^6	0.3 B.I.	3.00×10^7	1.90×10^7	1		
6.47×10^5	0.3*VAF	2.24×10^8	1.41×10^8	0		
			Total 0.3 eV Failures =	1	0.0008	0.0013
4.74×10^6	0.6 B.I.	1.90×10^8	7.59×10^7	2		
1.50×10^6	0.6 BAKE	4.10×10^9	1.62×10^9	3		
6.47×10^5	0.6 HVELT	2.59×10^7	1.04×10^6	0		
			Total 0.6 eV Failures =	5	0.0001	0.0004
4.74×10^6	1.0 B.I.	2.22×10^9	4.82×10^8	0		
6.47×10^5	1.0 HVELT	3.04×10^7	6.59×10^7	0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate:		0.0009	0.0017
			FITs:		9	17

48 Hour Burn-In Infant Mortality: 77 DPM

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	40°C/W	Temp with θ_{ja}				
V_{CC} =	5.50V	T(55) = 330.35°K	BI/ELT	0.3	6.3	4.0
I_{CC} @55 =	10 mA	T(70) = 345.35°K	Accel.	0.6	40.1	16.0
I_{CC} @70 =	10 mA	T(125) = 400.35°K	Factors:	1.0	468.9	101.7
I_{CC} @125 =	10 mA	T(250) = 523.15°K				
			250° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-charge loss (defect) 0.6 eV
1-charge gain (defect) 0.6 eV
B. 1-oxide breakdown 0.3 eV
C. 2-charge loss (defect) 0.6 eV
2-charge loss (intrinsic) 1.0 eV
D. 1-charge loss (defect) 0.6 eV

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D87C257

The Intel 87C257 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM) which incorporates an internal address latch.

Number of Bits: 262,144
Organization: 32K x 8
Pin Out: 28 Pin JEDEC Approved

Die Size: 182 x 175 mils
Process: CHMOS II-E
Cell Size: 6 x 6 μM
Programming Voltage: 12.5V
Technology: CMOS

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/6965	0/6961	0/0	0/0	0/0	0/0	0/0	0/0
1989	0/2951	0/2951	0/0	0/0	0/0	0/0	0/0	0/0
Totals	0/9916	0/9912	0/0	0/0	0/0	0/0	0/0	0/0

Table 2: Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1988	2/903	1/901	0/0	0/0
1989	0/187	1/187	0/0	0/0
Totals	2/1090	2/1088	0/0	0/0
	A	B		

D87C257 (Continued)

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
1.19×10^6	0.3 B.I.	7.53×10^6	4.76×10^6	0		
0	0.3*VAF	0	0	0		
			Total 0.3 eV Failures =	0	0.0122	0.0192
1.19×10^6	0.6 B.I.	4.16×10^7	1.90×10^7	0		
1.83×10^5	0.6 BAKE	5.01×10^8	1.98×10^8	2		
0	0.6 HVELT	0	0	0		
			Total 0.6 eV Failures =	2	0.0006	0.0014
1.19×10^6	1.0 B.I.	5.58×10^8	1.21×10^8	0		
0	1.0 HVELT	0	0	0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate:		0.0128	0.0206
			FITs:		128	206

48 Hour Burn-In Infant Mortality: 0 DPM

					Thermal Accel. Factors 55°C	70°C
Theta Ja =	40°C/W	Temp with θ_{ja}				
V_{CC} =	5.50V	T(55) = 330.35°K	BI/ELT	0.3	6.3	4.0
I_{CC} @55 =	10 mA	T(70) = 345.35°K	Accel.	0.6	40.1	16.0
I_{CC} @70 =	10 mA	T(125) = 400.35°K	Factors:	1.0	468.9	101.7
I_{CC} @125 =	10 mA	T(250) = 523.15°K				
			250°C Bake	0.3	N/A	N/A
		K = 8.62×10^{-5} eV/°K	Accel.	0.6	2737.2	1081.8
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-charge loss (defect) 0.6 eV
1-charge loss (intrinsic) 1.0 eV

B. 1-charge loss (defect) 0.6 eV
1-charge loss (intrinsic) 1.0 eV

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Plastic Reliability Data Summary

INTRODUCTION

The following information is written to provide OTP (one time programmable) users with the description and reliability summary of Intel's plastic production EPROMs in both DIP and PLCC packages. It includes brief test descriptions, a description of plastic packaging compounds and the reliability data obtained during the qualification and subsequent product monitors of the P2764A, P27128A, P27256 and P/N27C256 devices.

PLASTIC PACKAGE CHARACTERISTICS

The EPROM plastic package is composed of flame retardant plastic/epoxy which meets the rating requirements of US94V0 $\frac{1}{8}$" minimum. The die attach incorporates a silver-filled adhesive die attach on a silver spot plated leadframe. Bonding is accomplished through gold thermal compression bonding and lead finish is either tin plated or 60/40 solder dipped tin/lead.

EPROM ELECTRICAL CHARACTERISTICS

OTP EPROMs in plastic are tested to the same electrical/parametric levels as their counterparts in CERDIP. The characteristics include input/output voltage levels, speeds, leakage, and power requirement characteristics over the full commercial temperature operating range of 0°C–70°C. Performance capabilities are identical to that of CERDIP EPROMs with speeds to 200 ns currently available.

RELIABILITY/QUALITY STRESSES

High Temperature 125°C Dynamic Lifetest (HTDL)—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and outputs are exercised but not monitored or loaded. A checkerboard data pattern is typically used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with failure analysis. In order to best determine long-term failure rates, all devices used for lifetesting are subjected to a standard Intel screening. The 48-hour burn-in results measure infant mortality and are not included in the failure rate calculations.

High Temperature Extended Lifetest (HTELT)—This test is also performed at 125°C but uses a smaller sample size. The parts are kept in the full active mode for the duration of the test with outputs driven. The test is intended to evaluate the long-term reliability of the product.

High Voltage 6.5V Extended Lifetest (HVELT)—This test is used to accelerate oxide breakdown failures. The test is set up identical to the one used for dynamic lifetest except for V_{CC} and V_{PP} which are raised to 6.5V. The voltage acceleration factor for this configuration on Intel HMOS IIE product has been determined to be 55 and is applicable to the 0.3 eV failure mode components.

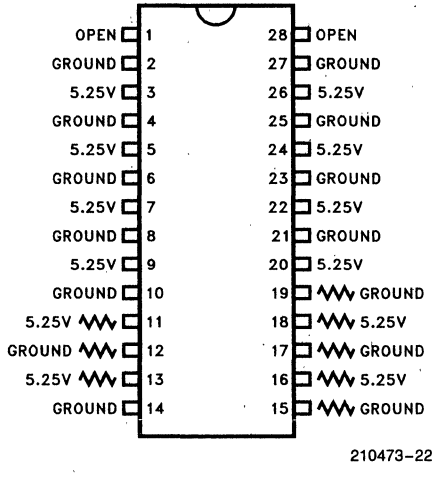
High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 98% + program pattern to a 140°C bake with no applied bias. In addition to data retention, this test can also be used to detect mechanical reliability problems such as bond integrity or process instabilities. The test is sometimes referred to as a data retention bake test.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is treated as a distinct part of a product qualification. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products. The new Quick-Pulse Programming™ Algorithm has been extensively verified and the data easily surpasses the 99.5% programmability criteria of Intel's qualification requirements. Qualification results are presented in the following table:

Product	Quantity	# Fail	% Yield
P2764A	8269	0	100%
P27128A	10,399	2	99.98%
P27256	19,040	10	99.95%
N27C256	2079	1	99.95%

MOISTURE RESISTANCE

Two types of moisture resistance testing are performed by Intel. The first is 85°C/85% relative humidity stressing and the second is steam stressing consisting of 121°C, 2 atm.



Pin	Pin Name	Stress
1	V_{PP}	Open*
2	A_{12}	Ground
3	A_7	5.25V
4	A_6	Ground
5	A_5	5.25V
6	A_4	Ground
7	A_3	5.25V
8	A_2	Ground
9	A_1	5.25V
10	A_0	Ground
11	O_0	5.25V
12	O_1	Ground
13	O_2	5.25V
14	Ground	Ground
15	O_3	Ground
16	O_4	5.25V
17	O_5	Ground
18	O_6	5.25V
19	O_7	Ground
20	$\overline{CE}$	5.25V
21	A_{10}	Ground
22	$\overline{OE}$	5.25V
23	A_{11}	Ground
24	A_9	5.25V
25	A_8	Ground
26	A_{13}	5.25V
27	A_{14}	Ground
28	V_{CC}	Open*

*NMOS has pins 1 and 28 open
CMOS has V_{PP} and V_{CC} at 5.25V

Figure 1. Typical 85/85 Bias Diagram

During the 85°C/85% relative humidity test, the devices are subjected to a high temperature, high humidity environment. The object of the test is to accelerate failure mechanisms through an electrolytic process. This is accomplished through a combination of moisture penetration of the plastic, voltage potentials and contamination which, if present, would combine with the moisture to act as an electrolyte. See Figure 1 for typical 85/85 Bias Diagram.

Steam stressing accelerates moisture penetration through the plastic package material to the surface of the die. The objective of this test is to accelerate failures of the device as a result of moisture on the die surface. Corrosion, as typically seen in plastic encapsulated devices, is a very minor contributor to the EPROM failure mechanisms. Due to the floating gate storage cell composition, EPROMs have a distinctive failure mode which requires special considerations and solutions. The floating gate itself is a highly phosphorous doped structure on which electrons are stored, thus creating the non-volatile memory cell. Passivation defects or marginalities can allow moisture penetration to a single EPROM cell causing oxide deterioration, thus showing up as a charge loss failure. This becomes the predominant failure mode for EPROMs, opposed to corrosion which historically has been the dominant plastic mode of failure. Intel has developed a proprietary, multi-layer passivation which has successfully solved this problem.

QUALITY/RELIABILITY STANDARDS

The table below contains Intel's current requirements for qualification for plastic OTP EPROMs. The failure rate criteria has been established based on a survey of major customers world-wide. Intel consistently meets or exceeds these requirements.

HTDL 48-Hr	HTELT 168/500/1K Hrs	140°C Bake 48/168/500-Hrs	HVELT 168/500/1K Hrs	Steam 168-Hrs	85/85 1K Hrs
<.05%	<200 FITs Combined Failure Rate			<2%	<0.5% cum

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P2764A

The P2764A is functionally identical to the 2764A except that it is housed in a windowless plastic package and is one-time programmable.

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	1/2668	1/2667	0/384	0/384	0/192	0/192	0/192	0/0
1989	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0
Totals	1/2668	1/2667	0/384	0/384	0/192	0/192	0/192	0/0
	A	B						

Table 2: Additional Qualification Tests

Year	140°C Data Retention Bake				200 Temp Cycles	168 Hrs Steam	85°C/85% RH		
	48 Hrs	168 Hrs	500 Hrs	1K Hrs			168 Hrs	500 Hrs	1K Hrs
1988	0/0	0/0	0/514	0/514	0/156	0/192	0/396	0/396	0/396
1989	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0
Totals	0/0	0/0	0/514	0/514	0/156	0/192	0/396	0/396	0/396

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
6.39×10^5 9.60×10^4	0.3 B.I. 0.3*VAF	2.98×10^6 2.44×10^7	2.08×10^6 1.71×10^7	0 0		
Total 0.3 eV Failures =				0	0.0033	0.0048
6.39×10^5 5.14×10^5 9.60×10^4	0.6 B.I. 0.6 BAKE 0.6 HVELT	1.39×10^7 4.06×10^7 2.09×10^6	6.79×10^6 1.60×10^7 1.02×10^6	0 0 0		
Total 0.6 eV Failures =				0	0.0000	0.0000
6.39×10^5 9.60×10^4	1.0 B.I. 1.0 HVELT	1.08×10^8 1.62×10^7	3.28×10^7 4.92×10^6	1 0		
Total 1.0 eV Failures =				1	0.0016	0.0054
Combined Failure Rate: FITs:					0.0049 49	0.0102 102

48 Hour Burn-In Infant Mortality: 375 DPM

P2764A (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	103°C/W	Temp with θ_{ja}	BI/ELT	0.3	4.7	3.3
V_{CC} =	5.25V	T(55) = 353.96°K	Accel.	0.6	21.7	10.6
I_{CC} @55 =	48 mA	T(70) = 367.33°K	Factors:	1.0	169.1	51.3
I_{CC} @70 =	45 mA	T(125) = 419.63°K				
I_{CC} @125 =	40 mA	T(140) = 413.15°K				
			140° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	79.0	31.2
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-microcracks 0.6 eV

B. 1-ionic contamination 1.0 eV

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P27128A

The P27128A is functionally identical to the 27128A except that it is housed in a windowless plastic package and is one-time programmable.

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/2673	0/2673	0/384	0/384	0/192	0/191	0/192	0/0
1980	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0
Totals	0/2673	0/2673	0/384	0/384	0/192	0/191	0/192	0/0

Table 2: Additional Qualification Tests

Year	140°C Data Retention Bake				200 Temp Cycles	168 Hrs Steam	85°C/85% RH		
	48 Hrs	168 Hrs	500 Hrs	1K Hrs			168 Hrs	500 Hrs	1K Hrs
1988	0/0	0/0	0/516	0/514	0/156	0/312	0/384	0/373	1/369
1989	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0	0/0
Totals	0/0	0/0	0/516	0/514	0/156	0/312	0/384	0/373	1/369
									A

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
6.40×10^5 9.60×10^4	0.3 B.I. 0.3*VAF	2.65×10^6 2.17×10^7	1.94×10^6 1.59×10^7	0 0		
Total 0.3 eV Failures =				0	0.0038	0.0051
6.40×10^5 4.28×10^5 9.60×10^4	0.6 B.I. 0.6 BAKE 0.6 HVELT	1.10×10^7 3.38×10^7 1.65×10^6	5.89×10^6 1.34×10^7 8.83×10^5	0 0 0		
Total 0.6 eV Failures =				0	0.0000	0.0000
6.40×10^5 9.60×10^4	1.0 B.I. 1.0 HVELT	7.30×10^7 1.09×10^7	2.59×10^7 3.88×10^6	0 0		
Total 1.0 eV Failures =				0	0.0000	0.0000
Combined Failure Rate: FITs:					0.0038 38	0.0051 51

48 Hour Burn-In Infant Mortality: 0 DPM

P27128A (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	95°C/W	Temp with θ_{ja}				
V_{CC} =	5.25V	T(55) = 367.95°K	BI/ELT	0.3	4.1	3.0
I_{CC} @55 =	80 mA	T(70) = 380.41°K	Accel.	0.6	17.1	9.2
I_{CC} @70 =	75 mA	T(125) = 432.91°K	Factors:	1.0	114.1	40.4
I_{CC} @125 =	70 mA	T(140) = 413.15°K				
			140° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	79.0	31.2
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-oxide breakdown 0.3 eV

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P27256

The P27256 is functionally identical to the 27256 except that it is housed in a windowless plastic package and is one-time programmable.

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	2/8706	1/8662	0/1248	0/1248	0/624	0/624	0/591	0/0
1989	0/6684	1/6680	0/288	0/288	0/624	0/615	0/615	0/470
Totals	2/15390	2/15342	0/1536	0/1536	0/1248	0/1239	1/1206	0/470
	A	B					C	

Table 2: Additional Qualification Tests

Year	140°C Data Retention Bake				200 Temp Cycles	168 Hrs Steam	85°C/85% RH		
	48 Hrs	168 Hrs	500 Hrs	1K Hrs			168 Hrs	500 Hrs	1K Hrs
1988	0/0	0/0	2/1672	0/1669	0/468	2/1012	0/1264	0/1262	0/1243
1989	0/0	0/0	0/1031	0/1031	4/624	1/780	0/960	1/960	3/956
Totals	0/0	0/0	2/2703	0/2700	4/1092	3/1792	0/2224	1/2222	3/2199
			D		E	F		G	H

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
3.12×10^6 8.44×10^5	0.3 B.I. 0.3*VAF	1.32×10^7 1.95×10^8	9.59×10^6 1.42×10^8	0 0		
			Total 0.3 eV Failures =	0	0.0004	0.0006
3.12×10^6 2.70×10^6 8.44×10^5	0.6 B.I. 0.6 BAKE 0.6 HVELT	5.51×10^7 1.77×10^8 1.51×10^7	2.95×10^7 7.01×10^7 7.98×10^6	2 2 1		
			Total 0.6 eV Failures =	5	0.0025	0.0058
3.12×10^6 8.44×10^5	1.0 B.I. 1.0 HVELT	3.81×10^8 1.03×10^8	1.32×10^8 3.57×10^7	0 0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate: FITs:		0.0029 29	0.0064 64

48 Hour Burn-In Infant Mortality: 130 DPM

P27256 (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	90°C/W	Temp with θ_{ja}				
V_{CC} =	5.25V	T(55) = 365.85°K	BI/ELT	0.3	4.2	3.1
I_{CC} @55 =	80 mA	T(70) = 378.44°K	Accel.	0.6	17.9	9.5
I_{CC} @70 =	75 mA	T(125) = 431.08°K	Factors:	1.0	122.0	42.3
I_{CC} @125 =	70 mA	T(140) = 413.15°K				
			140° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	79.0	31.2
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

NOTE:
FIT = Failure Unit. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1-ionic contamination 1.0 eV
1-MBCL 0.6 eV

B. 2-SBCL 0.6 eV

C. 1-SBCL 0.6 eV

D. 1-scratched die 0.5 eV
1-MBCL 0.6 eV

E. 3-cracked die 0.5 eV
1-microcracks 0.6 eV

F. 1-SBCL 0.6 eV
1-passivation hole 1.0 eV
1-partial row charge gain 0.6 eV

G. 1-pad corrosion 0.5 eV

H. 1-ref. generator charge gain 0.6 eV
1-ionic contamination 1.0 eV
1-pad corrosion 0.5 eV

5

P/N27C256

The P/N27C256 products are functionally identical to the 27C256 except that they are housed in a windowless plastic DIP (P) or a windowless plastic PLCC (N) package and are one-time programmable.

Table 1: Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest			
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/4615	0/4607	0/672	1/663	0/336	0/334	0/333	0/0
1989	0/7355	0/7345	0/480	0/478	0/525	0/523	0/512	0/0
Totals	0/11970	0/11952	0/1152	1/1141	0/861	0/857	0/845	0/0
				A				

Table 2: Additional Qualification Tests

Year	140°C Data Retention Bake				200 Temp Cycles	168 Hrs Steam	85°C/85% RH		
	48 Hrs	168 Hrs	500 Hrs	1K Hrs			168 Hrs	500 Hrs	1K Hrs
1988	0/0	0/0	0/883	1/883	0/312	0/542	0/700	0/697	0/697
1989	0/0	0/0	0/1031	0/1029	0/468	2/854	0/898	0/893	0/789
Totals	0/0	0/0	0/1914	1/1912	0/780	2/1396	0/1598	0/1590	0/1486
				B		C			

Table 3: Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.39×10^6 4.25×10^5	0.3 B.I. 0.3*VAF	1.47×10^7 1.43×10^8	9.38×10^6 9.11×10^7	0 0		
Total 0.3 eV Failures =				0	0.0006	0.0009
2.39×10^6 1.59×10^6 4.25×10^5	0.6 B.I. 0.6 BAKE 0.6 HVELT	9.09×10^7 1.26×10^8 1.62×10^7	3.68×10^7 4.97×10^7 6.55×10^6	0 0 0		
Total 0.6 eV Failures =				0	0.0000	0.0000
2.39×10^6 4.25×10^5	1.0 B.I. 1.0 HVELT	1.03×10^9 1.83×10^8	2.28×10^8 4.06×10^7	0 0		
Total 1.0 eV Failures =				0	0.0000	0.0000
Combined Failure Rate: FITs:					0.0006 6	0.0009 9

48 Hour Burn-In Infant Mortality: 0 DPM

P/N27C256 (Continued)

					Thermal Accel. Factors 55°C	70°C
Theta Ja =	88°C/W	Temp with θ_{ja}				
V_{CC} =	5.25V	T(55) = 332.62°K	BI/ELT	0.3	6.2	3.9
I_{CC} @55 =	10 mA	T(70) = 347.62°K	Accel.	0.6	38.1	15.4
I_{CC} @70 =	10 mA	T(125) = 402.62°K	Factors:	1.0	430.8	95.6
I_{CC} @125 =	10 mA	T(140) = 413.15°K				
			140° Bake	0.3	N/A	N/A
		$K = 8.62 \times 10^{-5}$ eV/°K	Accel.	0.6	79.0	31.2
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55

Failure Analysis:

A. 1 Au cratering 1.2 eV
B. 1 Au cratering 1.2 eV
C. 2 Ionic contamination 1.0 eV

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APPENDIX A
Failure Rate Calculations for 60% Upper Confidence Level

Step 1. Collect burn-in and lifetest data for each lot after 48 hours of burn-in through lifetest for each lot.

Step 2. Determine the failure mechanism and assign an activation energy (E_A) for each failure, except those occurring during the first 48 hrs. (See Table 1 below.)

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours accumulated beyond 48 hours of burn-in. (Note: 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation.)

Example: 125°C Burn-In/Lifetest for a 2 lot sample

$$\frac{\#\text{ failures}}{\text{total }\#\text{ devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

$$\text{Device Hours} = \sum \text{(Number of Devices in Stress Interval) (Number of Hours in Stress Interval)}$$

$$\text{Total Device Hours} = 1201\ (168\text{ hrs} - 48\text{ hrs}) + 1200\ (500\text{ hrs} - 168\text{ hrs}) + 1098\ (1000\text{ hrs} - 500\text{ hrs}) + 1093\ (2000\text{ hrs} - 1000\text{ hrs})$$

$$= 1201\ (120\text{ hrs}) + 1200\ (332\text{ hrs}) + 1098\ (500\text{ hrs}) + 1093\ (1000\text{ hrs})$$

$$= 2.185 \times 10^6 \text{ Device Hours}$$

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \exp\left[\frac{-E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°K (Boltzmann's constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A_1 \exp\left[\frac{-E_A}{KT_1}\right]}{A_2 \exp\left[\frac{-E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

Where $A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

Where R_1 and R_2 are rates for a normal operating temp and an elevated temperature respectively.

$$R_1 = R_2 \times \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

However, since rate (R) has the units 1/time, we can think in terms of time to one failure or MTBF.

Thus:

$$R_1 = \frac{1}{t_1} \text{ where } t_1 = \text{MTBF at some temperature } T_1$$

and:

$$R_2 = \frac{1}{t_2} \text{ where } t_2 = \text{MTBF at some temperature } T_2$$

Thus the Arrhenius Relation becomes:

$$\frac{1}{t_1} = \frac{1}{t_2} \times \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

or:

$$t_1 = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \times t_2$$

We then define the Acceleration Factor as:

$$\text{A.F.} = \frac{t_1}{t_2} = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398$°K, $T_1 = 328$°K

$$t_1 = 41.7\, t_2$$

Therefore, one hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy E_A = 0.6 eV. Then 41.7 is the thermal acceleration factor for time.

NOTE:
The Arrhenius Plot (Figure 2 Page 2) is simply ln (Acceleration Factor) vs. 1/Temperature normalized for an MTBF (t_2) of one hour at 250°C (T_2). This plot can also be used to determine the acceleration factor between two temperatures (other than 250°C).

For example: For a 0.3 eV failure at 125°C, the acceleration factor is 8.1 relative to a 0.3 eV failure at 250°C. For a 0.3 eV failure at 25°C, the acceleration factor is 152 relative to 250°C. Therefore, the acceleration factor between 125°C and 25°C is:

$$A.F. = \frac{t_1}{t_2} = \frac{152}{8.1} = 18.7$$

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:
The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the ambient temperature to arrive at the actual burn-in/lifetest temperature.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\,(IV @ T_{Ambient}) + T_{Ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	# Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

The failure rates for individual failure mechanisms and the total combined failure rate can be predicted using the data table and the following formula:

$$\%\ fail/1K\ hrs. = \frac{\chi^2\,(n, \alpha)}{2T}\left(10^5\right)$$

Where χ^2 (n, α) is the value of the chi-squared distribution for n degrees of freedom and confidence level of α. The degrees of freedom, n = [2 (# of failures) + 2] for this application. T is the total equivalent device hours at T_1. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL, the above formula converts to the following:

# Failures	% Fail/1K Hours (60% UCL)
0	$0.915 \times 10^5/T$
1	$2.02 \times 10^5/T$
2	$3.105 \times 10^5/T$
3	$4.17 \times 10^5/T$
$3 < \# < 15$	$\left[\frac{1.049\,(\#\text{failures for a particular } E_A) + 1.0305}{T}\right]\left[10^5\right]$
>15	$\frac{[0.2533 + \sqrt{(4 \times \#\ \text{Failed}) + 3}]^2}{4T}\left[10^5\right]$

Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient}$ = 125°C and I_{CC} active is 60 mA at $T_{Ambient}$ = 55°C.

Also assume that θ_{JA} = 35°C/W.

Then,

T_2 = (35°C/W) (57 mA) (5V) + 125°C

≈ 135°C = 408°K

T_1 = (35°C/W) (60 mA) (5V) + 55°C

≈ 65°C = 338°K

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C % Fail/ 1K Hrs
0.3	2.185×10^6	5.85	1.278×10^7	0	0.0081
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
				Total Combined Failure Rate =	0.0126
				=	126 FITs

Example 2:

Assume that an additional lot of 800 HMOS*IIE devices is burned in using a 6.5V lifetest. Using Table 2 below, a voltage acceleration factor of 55 results from a 20% overstress (5.5V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0/800	1/800	0/799

Device Hours = 800 (48 hrs − 0 hrs) + 800 (168 hrs − 48 hrs) + 799 (500 hrs − 168 hrs)
= 3.997×10^5

Table 2. Time-Dependent Oxide Failure Accelerations

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/cm)	Acceleration Factor at ____% Over Stress				
				10%	20%	30%	50%	100%
HMOS E	5	700	0.714	3.2	10	32	3.2E+2	1.0E+5
HMOS II E	5	400	1.25	7.5	55	422	2.4E+4	5.6E+8
CHMOS II E	5	400	1.25	7.5	55	422	2.4E+4	5.6E+8

ASSUMES:
1. No Bias Generators
2. Depletion Loads
3. Failure rate calculations use the appropriate acceleration factor for stress voltage and maximum operating voltage (conservative).

Since this voltage accelerated stress is used to predict an oxide breakdown failure rate, the 5.5V burn-in/lifetest 55°C equivalent hours for E_A = 0.3 eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours as follows:

125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C
5.5V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 x 55)	1.286×10^8
			Total Equivalent E_A = 0.3 eV Device Hours =	1.414×10^8

The following failure rate predictions include the total equivalent 55°C, E_A = 0.3 eV device hours found above:

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C	# Fail	55°C % Fail/ 1K Hours
0.3	2.185×10^6	5.85	—	—	—
0.3 + 55(1)	3.997×10^5	(5.85 x 55)	1.414×10^8	1	0.0015
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
			Total Combined Failure Rate =		0.0060
			=		60 FITs

NOTES:
(1) The notation 0.3 + 55 is used to show that 6.5V and 5.5V burn-in/lifetest equivalent hours have been combined.
(2) Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.

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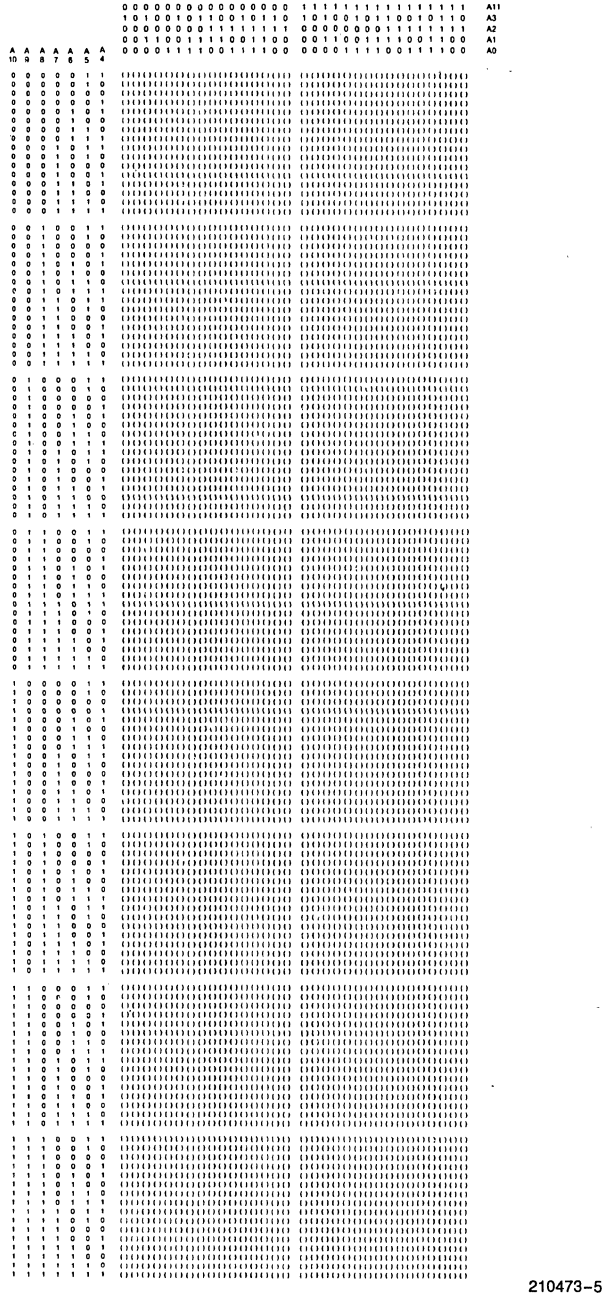
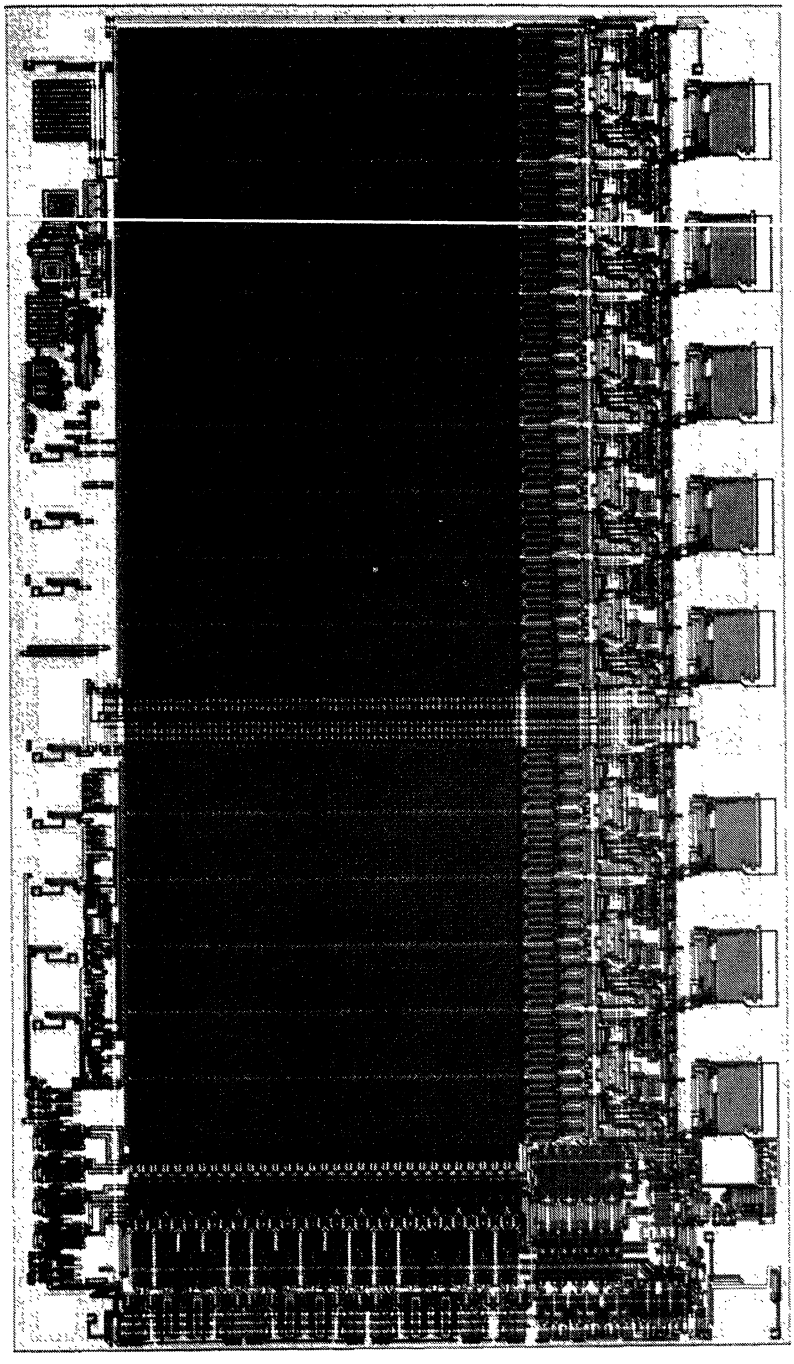
*HMOS & CHMOS are patented processes of Intel Corporation.

APPENDIX B
EPROM Bit Maps and Die Photos



2732A Bit Map (1 of 8 Outputs Shown)



210473-6

2732A Die Photograph

Column Selects

	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}	Y_{16}	Y_{17}	Y_{18}	Y_{19}	Y_{20}	Y_{21}	Y_{22}	Y_{23}	Y_{24}	Y_{25}	Y_{26}	Y_{27}	Y_{28}	Y_{29}	Y_{30}	Y_{31}
A_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
A_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A_0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A_{10}	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A_{11}	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

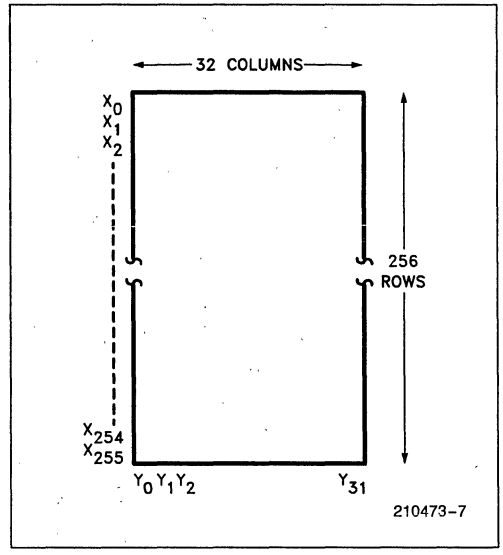
Row Selects

	X_0	X_1	X_2	X_3	X_4	X_5	X_{253}	X_{254}	X_{255}
A_7	0	0	0	0	0	0	1	1	1
A_6	0	0	0	0	0	0	1	1	1
A_5	0	0	0	0	0	0	1	1	1
A_4	0	0	0	0	0	0	1	1	1
A_3	0	0	0	0	0	0	1	1	1
A_{12}	0	0	0	0	1	1	1	1	1
A_9	0	0	1	1	0	0	0	1	1
A_8	0	1	0	1	0	1	1	0	1

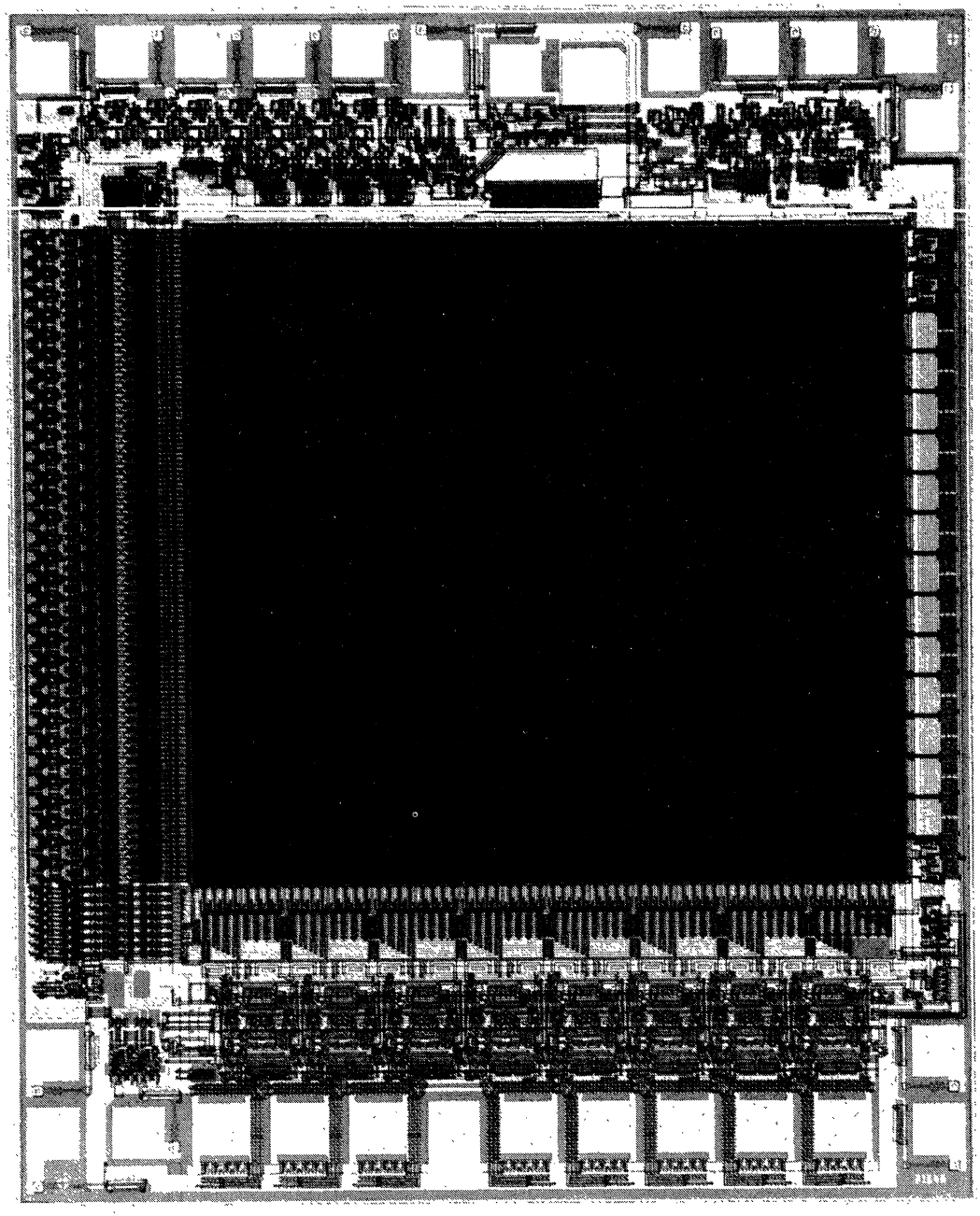
Array Organization

ROW SELECT	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
	Column Select							

Bit Map for One Output (Same for All Outputs)

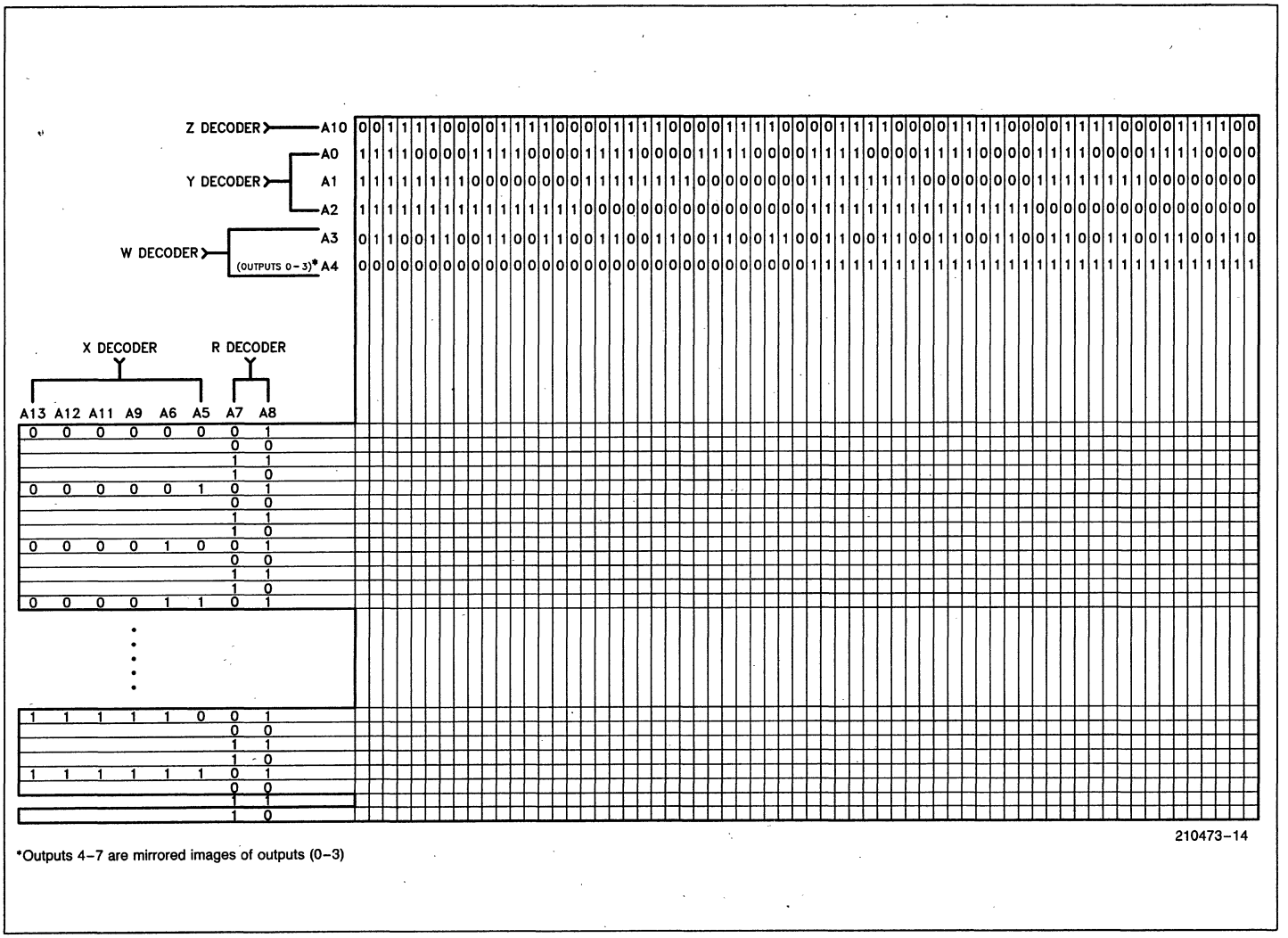


2764A Bit Map

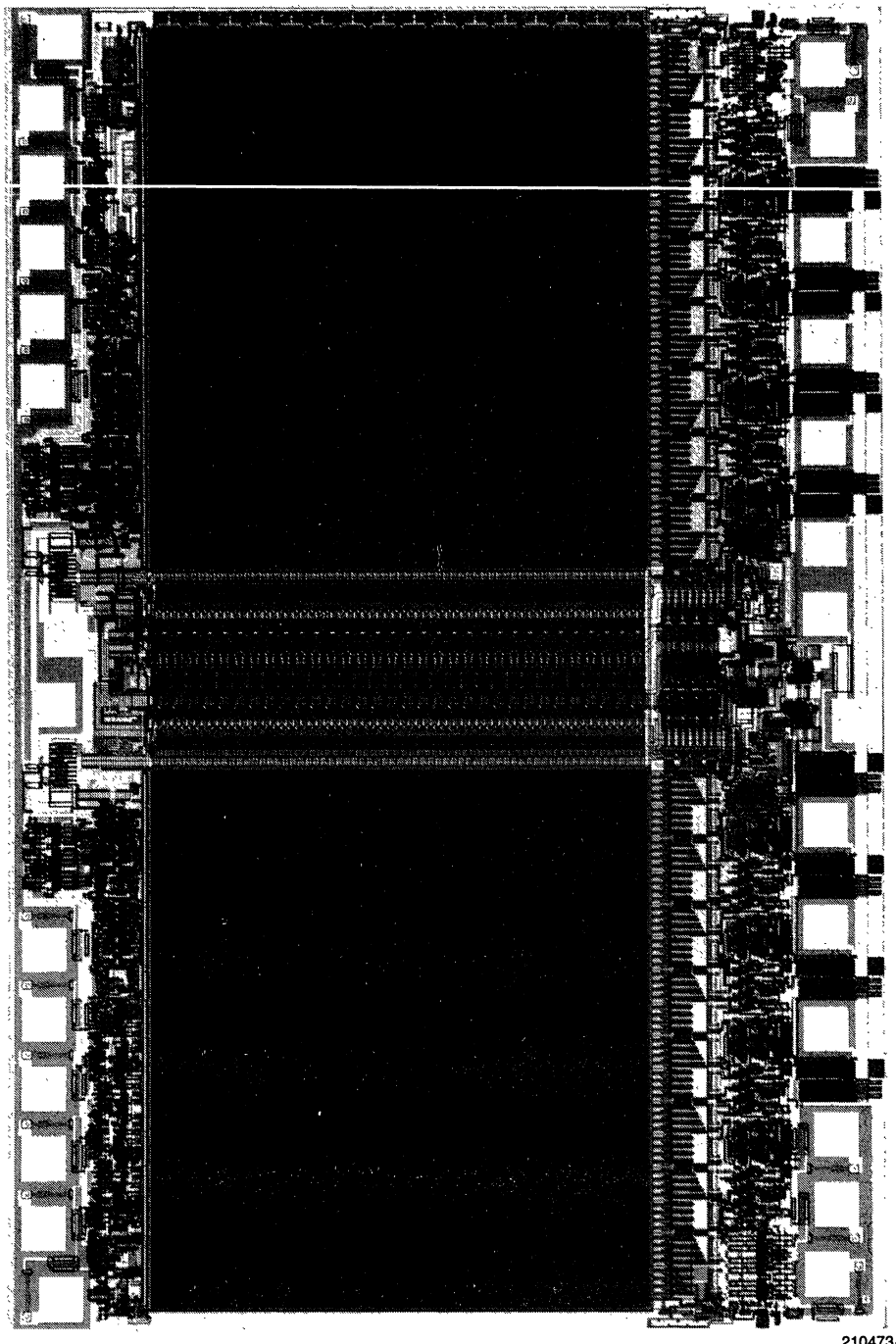


210473-8

2764A Die Photograph



*Outputs 4–7 are mirrored images of outputs (0–3)



210473-15

27128A Die Photograph

Address Decoding

Y Decode

	A_4	A_{10}	A_1	A_2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

W Decode

	A_0	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

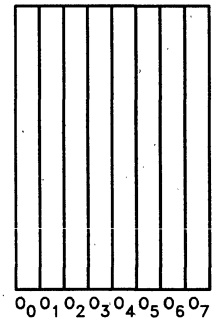
X Decode

	A_{14}	A_{13}	A_{12}	A_8	A_7	A_6
X_0	0	0	0	0	0	0
X_1	0	0	0	0	0	0
X_2	0	0	0	0	0	0
•						
•						
•						
X_{511}	1	1	1	1	1	1

R Decode

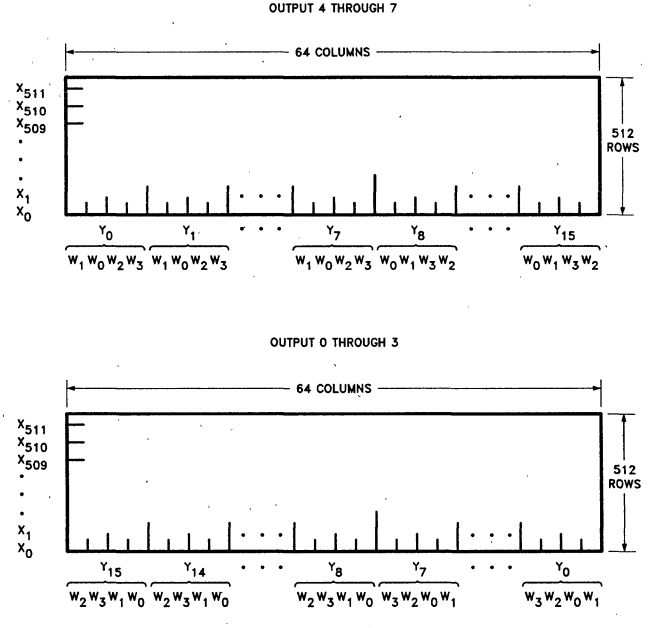
A_{11}	A_9	A_5
0	0	0
0	0	1
0	1	0
1	1	1

Array Organization



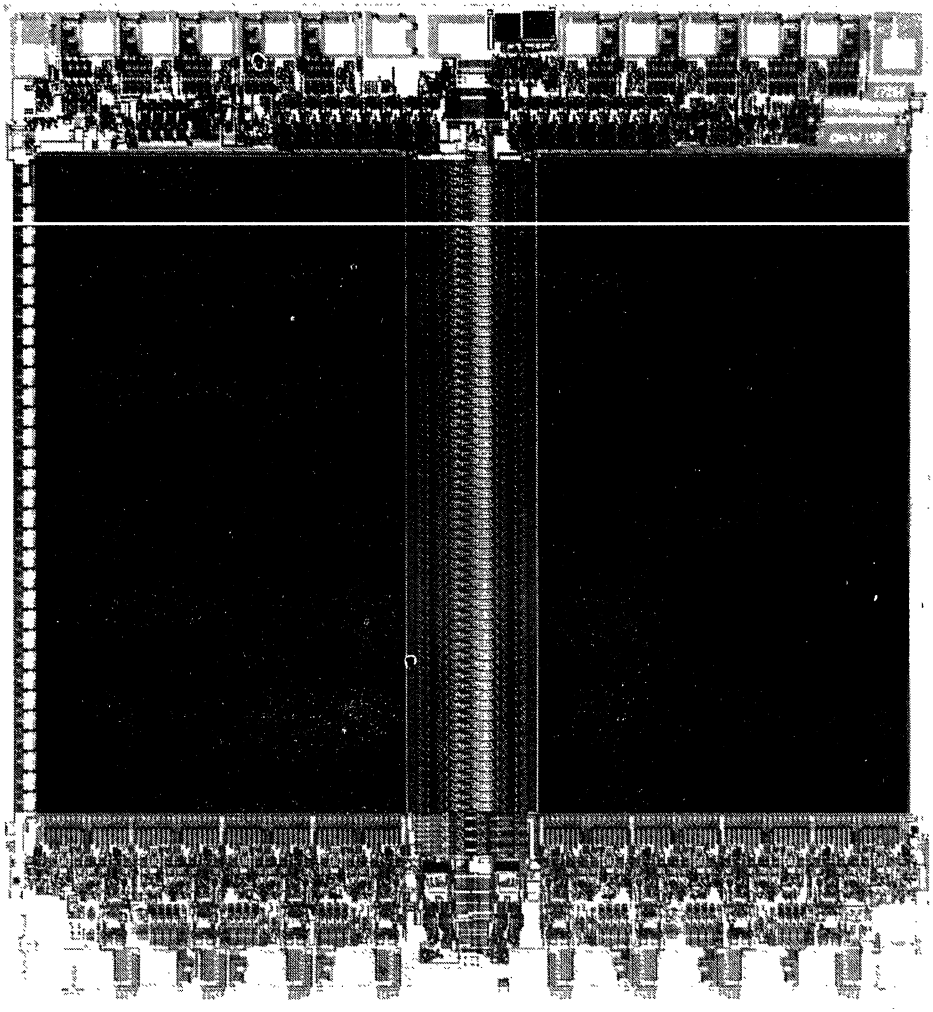
210473-16

Bit Map



210473-17

27256 Bit Map



210473-18

27256 Die Photograph

Address Decoding

Y Decode

	A_2	A_1	A_0	A_{10}
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

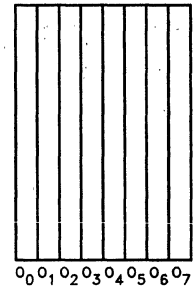
W Decode

	A_4	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

X Decode

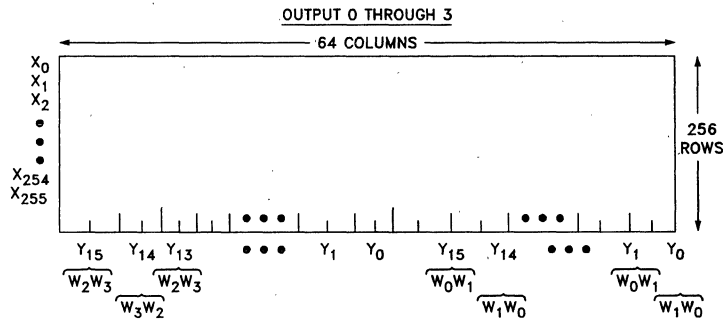
	A_{14}	A_{13}	A_{12}	A_7	A_6	A_5	A_{11}	A_9	A_8
X_0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	1	0
•									
•									
X_{510}	1	1	1	1	1	1	1	1	0
X_{511}	1	1	1	1	1	1	1	1	1

Array Organization

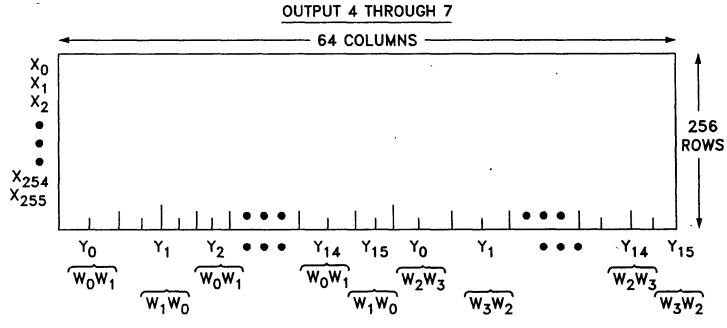


210473-16

Bit Map

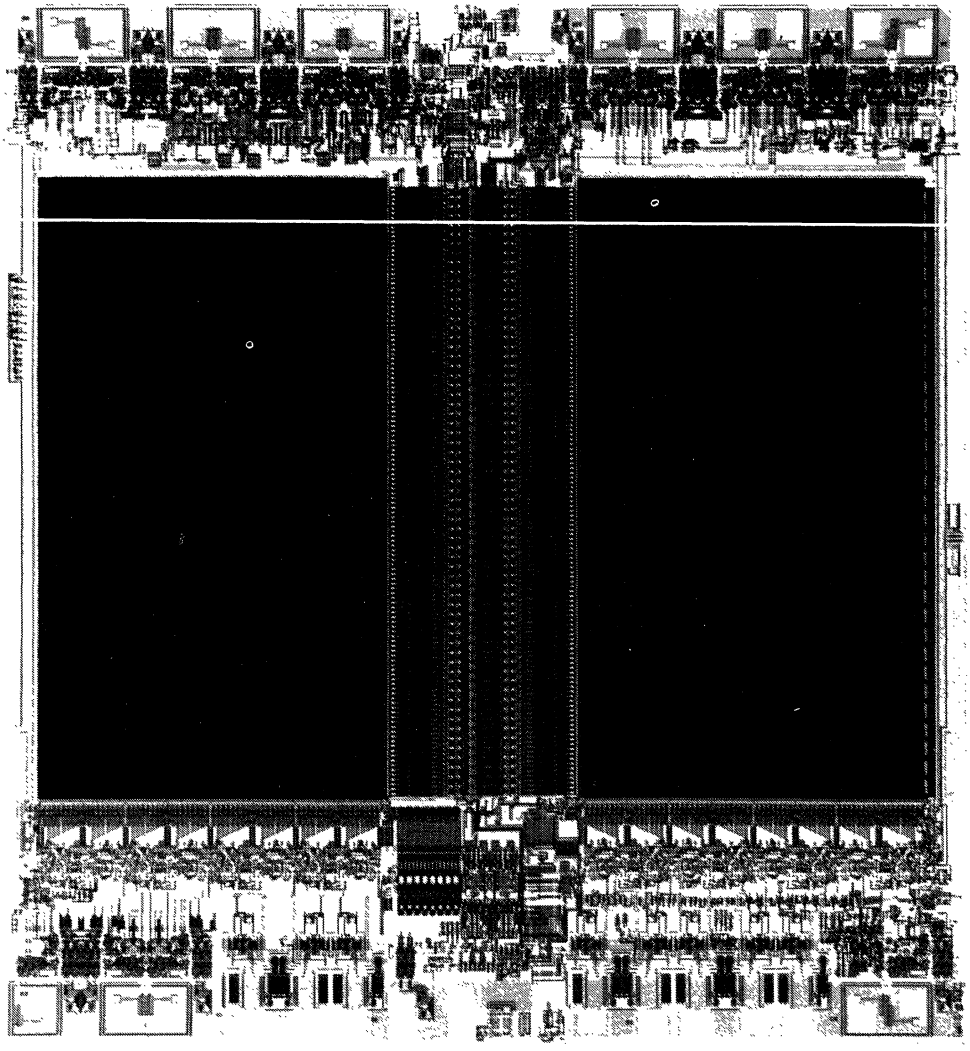


210473-24



210473-25

27C256 Bit Map



210473-26

27C256 Die Photograph

Address Decoding

X Decoders

A_{14}	A_{13}	A_{12}	A_7	A_6	A_5	A_{11}	A_9	A_8
WL0	0	0	0	0	0	0	0	0
WL1	0	0	0	0	0	0	0	1
WL2	0	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
WL510	1	1	1	1	1	1	1	0
WL511	1	1	1	1	1	1	1	1

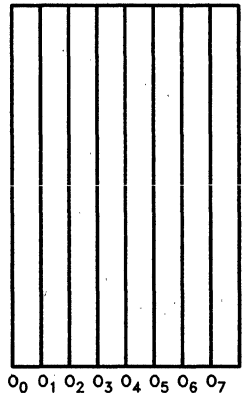
*W Decoders

A_4	A_3	W
0	0	W0
0	1	W1
1	0	W2
1	1	W3

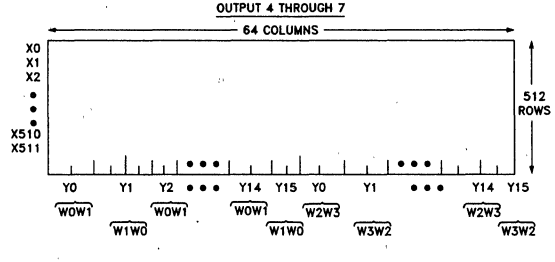
Y Decoders

A_2	A_1	A_0	A_{10}	Y
0	0	0	0	Y0
0	0	0	1	Y1
0	0	1	0	Y2
0	0	1	1	Y3
0	1	0	0	Y4
0	1	0	1	Y5
0	1	1	0	Y6
0	1	1	1	Y7
1	0	0	0	Y8
1	0	0	1	Y9
1	0	1	0	Y10
1	0	1	1	Y11
1	1	0	0	Y12
1	1	0	1	Y13
1	1	1	0	Y14
1	1	1	1	Y15

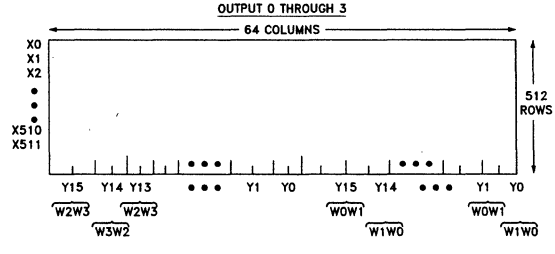
Array Organization



210473-36

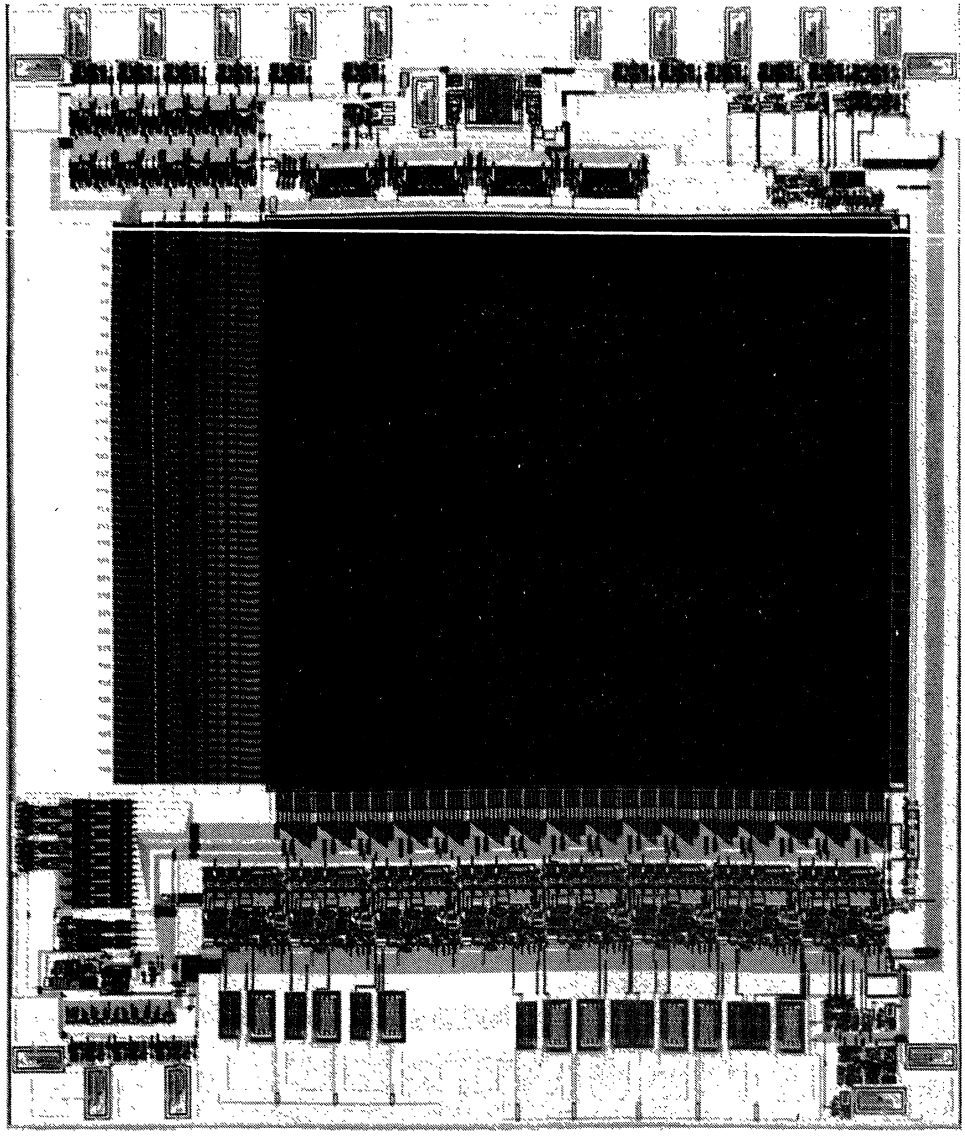


210473-37



210473-38

27C256 Bit Map (Six Digit Suffixes)



210473-35

27C256 Die Photograph
(Six Digit Suffix)

Address Decoding

Y Decode

	A_2	A_1	A_0	A_{10}
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

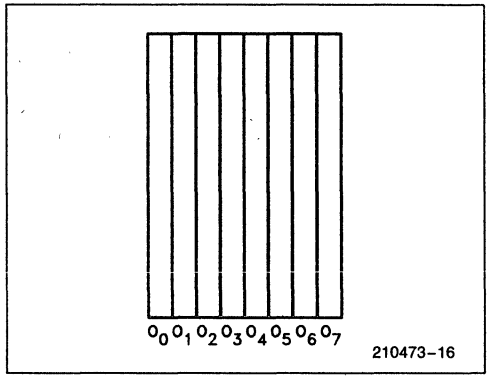
W Decode

	A_4	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

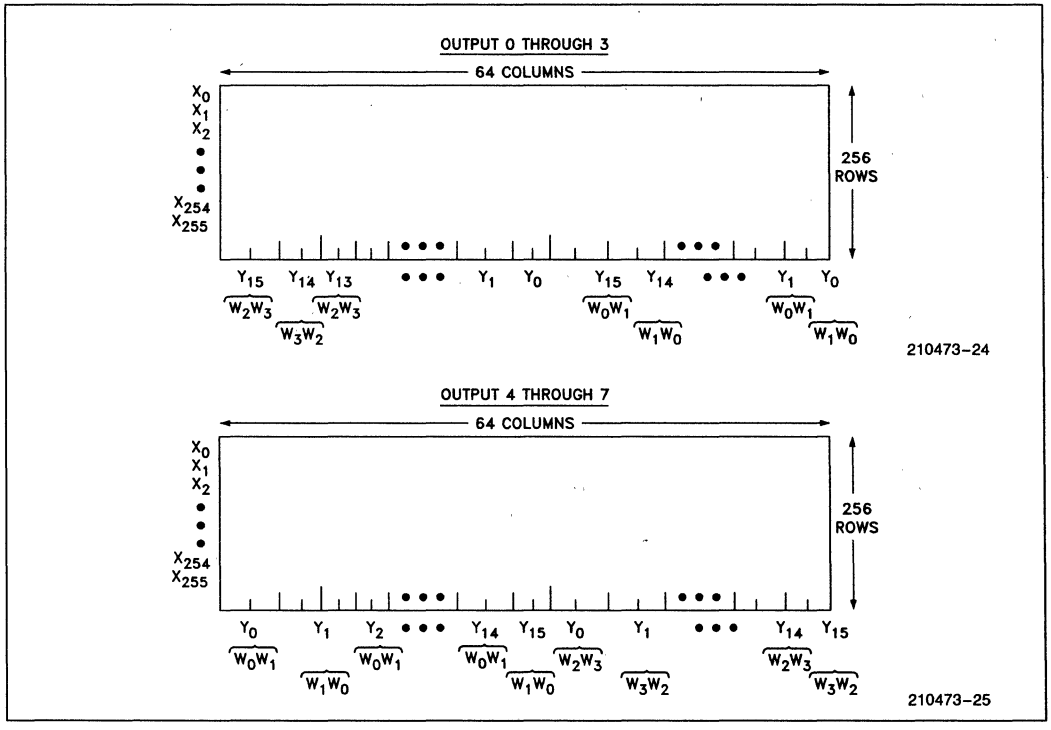
X Decode

	A_{14}	A_{13}	A_{12}	A_7	A_6	A_5	A_{11}	A_9	A_8
X_0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	1	0
•									
•									
•									
X_{510}	1	1	1	1	1	1	1	1	0
X_{511}	1	1	1	1	1	1	1	1	1

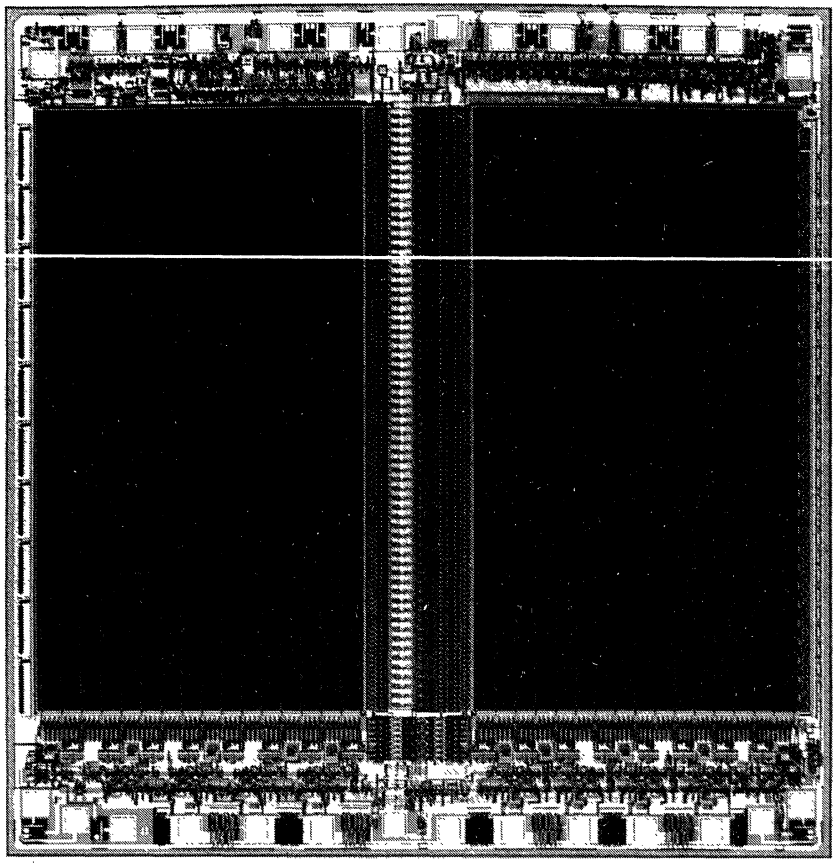
Array Organization



Bit Map



87C257 Bit Map



210473-34

87C257 Die Photograph

November 1990

EPROM Reliability Data Summary CHMOS III-E

Order Number: 293004-002

INTEL EPROM
RELIABILITY DATA SUMMARY: CHMOS III-E

CONTENTS

CONTENTS

INTRODUCTION/SCOPE

Quality and Reliability: The Cornerstone of Business

In the world of electronic hardware, no facet is more important to the user of a system than the reliability of its individual components. This single point has been an instrumental factor in the philosophy of product development, qualification, and manufacturing within Intel. Being the inventor of the EPROM, we are proud of the continuous quality and reliability leadership position that we have maintained.

In the spirit of service to our customers and their customers, this publication has been assembled for your convenience and reference. The scope of this document is limited to Intel's latest EPROM VLSI products from the 256 Kbit to the 2 Mbit density manufactured on our CHMOS* III-E process technology. Other EPROM product/process reliability summaries can be found in the latest revision of RR-35. The data provided herein is the product of just one of Intel's qualification and reliability monitoring systems. The purpose of this report is to supplement Intel's Quality and Reliability handbook with product specific data. For additional information, please contact your Field Sales or Customer Quality Engineer.

Quality Versus Reliability

The traditional concepts segregating quality from reliability is one of time. Quality is a measure of the ability of a product to meet performance expectations at a single point in time. This "point in time" is usually interpreted as your initial board power-up or incoming inspection. Reliability, on the other hand, is a measure of a product's ability to maintain its "time zero" quality throughout its life cycle. A reliability failure usually occurs after your product has shipped to your customer.

The cost of poor quality can be objectively totalled within your organization. It includes the cost of detection and in-house repair. However, the cost of poor reliability has a much higher cost. Besides an inherently higher repair cost per defective unit, reliability failures create customer concern about design and/or workmanship standards used in the manufacture of the product. Loss of goodwill with your customers can have many long term negative effects on your business. Therefore, Intel advocates that you make reliability a key consideration for the selection of your system's components.

The Roots of Reliability

The manufacture of a reliable VLSI semiconductor device using a modern technology is a dynamic and evolutionary process. Success of this process is highly dependent upon the interplay between knowledgeable and experienced manufacturing engineers, materials physicists, and responsible/responsive management. Only the correct combination can consistently deliver high volumes of reliable product. In this model, the experienced process engineer selects and defines the stresses to be performed and the performance criteria to be met, utilizing appropriate statistical tools and limits. The materials physicist then determines the root causes of failure, if and when failure occurs, and provides effective solutions and/or containment recommendations. Finally, management provides the resources for the entire process from initial monitor to root cause corrective action.

MONITORS: THE CONTROL MECHANISM OF RELIABILITY

A Comprehensive Program Is The Key

Intel has developed and implemented many types of reliability monitoring systems. Since continuous delivery of reliable product is of paramount importance, most of the monitors are in-line and are designed to provide as close to "real time" feedback on the reliability of the product in-process as possible. The monitors are located throughout the fab, assembly and test areas. The data from these monitors are an indication of process health and overall statistical control. They are not necessarily directly correlatable to the reliability of the product that will ship to your location. For this reason, a final finished product monitor which randomly selects product is used as the yardstick to measure the success of our factory in meeting your customer's reliability goals. Figure 1 demonstrates the typical monitor stress cells and flows which are periodically used on every major product in Intel's EPROM family. A similar stress flow is also used for plastic devices. The data presented in the device section of this report is a compilation of this monitor data plus the initial product qualification testing results.

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*CHMOS is a patented process of Intel Corporation.

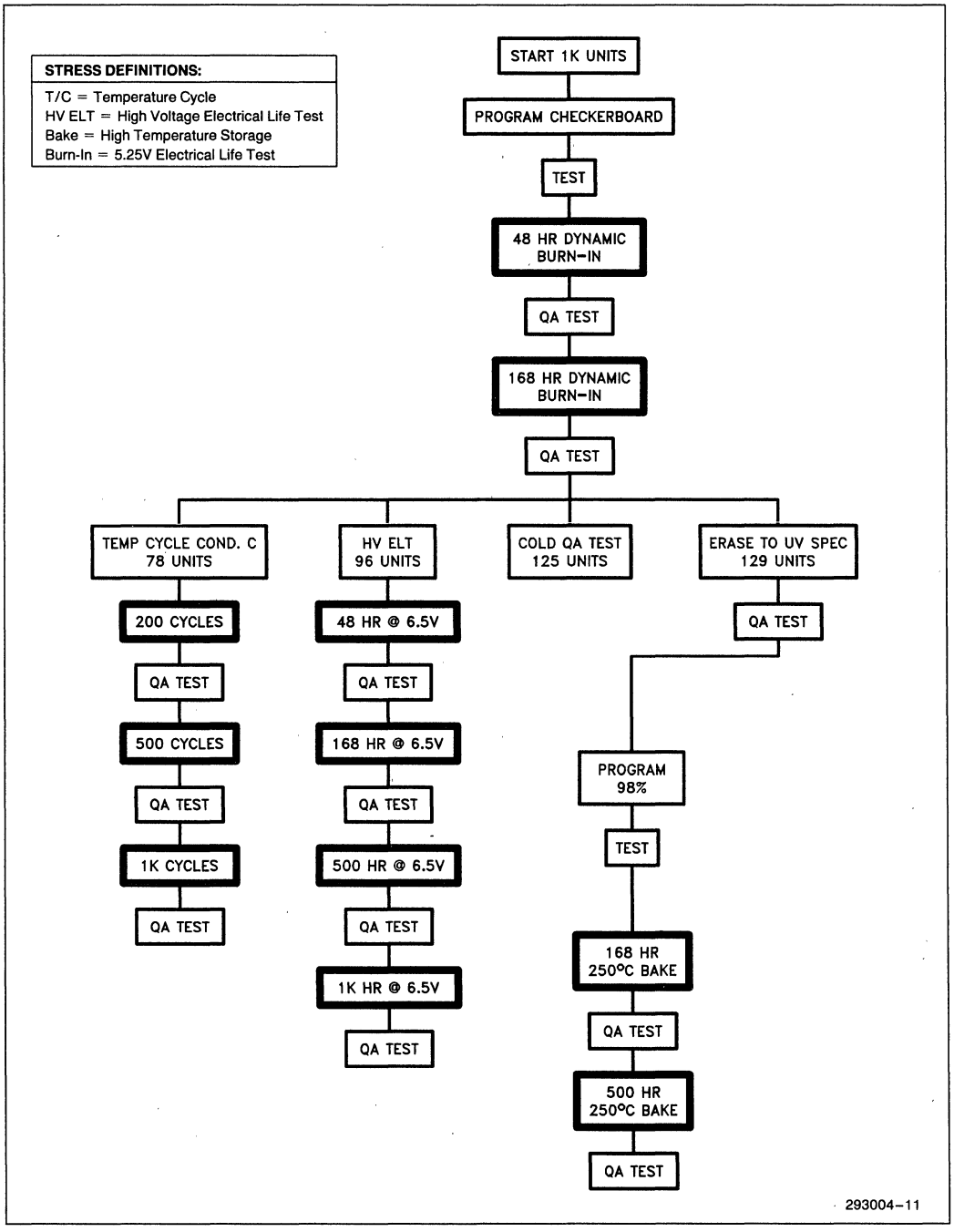

Figure 1. CERDIP EPROM Standard Monitor Flow

EPROM Failure Mechanisms

The typical EPROM is about 10% decoder and "special" test mode circuitry. This 10% of the circuitry is similar in design and layout to the circuitry found in a common logic device. Expected failure mechanisms are therefore considered to be primarily oxide stress and contamination based. For more information on these and other mechanisms, please refer to the Intel Quality and Reliability Handbook. The remaining 90% of the EPROM area is a very dense matrix of isolated floating gate memory cells manufactured using the latest process technology. The major function of the EPROM cell is to store a very small amount of charge on a floating polysilicon gate, and to do so for a time period well in excess of 20 years under normal operating conditions. Electrons are electrically injected through the isolating oxides onto the floating polysilicon gate during programming. Because a typical EPROM cell may only need 100,000 electrons on this floating gate to look "programmed," it can be sensitive to leakage currents of as little as 1 x 10^{-23} amps [1]. Small amounts of charge loss or gain in excess of intrinsic expectations can, through time and usage, significantly raise or lower the threshold voltage of the memory cell causing the device to functionally misread the intended pattern.

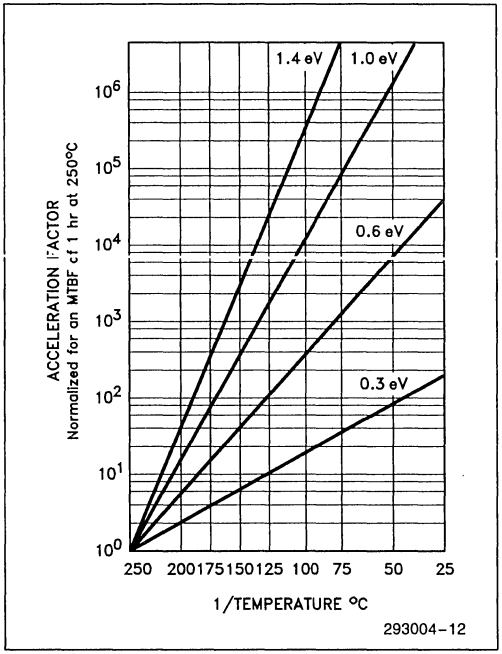

Figure 2. Arrhenius Plot and Failure Activation Energies Relevant to EPROMs

STRESSES: THE ACCELERATION OF TIME AND USE

Acceleration Factors

In order to determine if a device's reliability performance can be accelerated, normal operating condition failure mechanisms must be completely understood and characterized to the accelerating stress. The familiar Arrhenius equation is then used for the calculation of the acceleration factor which most closely approximates the condition of the stress. Figure 2 is an example of how the Arrhenius curves would appear for the most common semiconductor failure mechanisms which are accelerated by temperature over a period of time. All known operating condition failure mechanisms in semiconductor devices can be accelerated with the use of various stresses. These stresses include: temperature, voltage, current, moisture, mechanical stress, and radiation. Table 1 indicates the most common failure mechanisms and their activation energies which are associated with being thermally accelerated. The mechanics of deriving an operating failure rate (FIT rate) from these factors is described in Appendix A.

Table 1. Activation Energy Table

Failure Mechanism	Each
Oxide	0.3
Single Bit Charge Loss/Gain	0.6
Contamination	1.0
Speed Degradation	0.3–1.0
Intrinsic Charge Loss	1.4

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Commonly Monitored EPROM Stresses

As discussed earlier, it is important to have a comprehensive reliability monitoring program that can uncover the many potential failure mechanisms which may have an impact to total quality, reliability and deliverability. The listing below represents only the major and most consistently performed reliability monitor stresses. They are executed on randomly selected finished product inventory.

HIGH-TEMPERATURE DYNAMIC LIFETEST (5.25V and 6.5V)

This stress is considered the most relevant of all accelerating stresses. The device is programmed with a checkerboard data pattern to simulate a random customer pattern. It is then functionally exercised at 125°C at either a V_{CC} of 5.25V or 6.5V. The memory is sequentially addressed and the outputs are exercised but not loaded. See Figure 3 for a typical bias and timing diagram. The 5.25V stress is considered thermally accelerating only. The 6.5V stress is considered both thermally and voltage accelerating for oxide fault type mechanisms(1). The end point electrical tests are conducted within a fixed period of time to worst case data sheet parameters. The Memory Components Division also periodically takes variables data on selected data sheet parameters to monitor the stability of the process. Low-temperature lifetesting has also been performed on this process to assure that no intrinsic hot electron mechanisms are present.

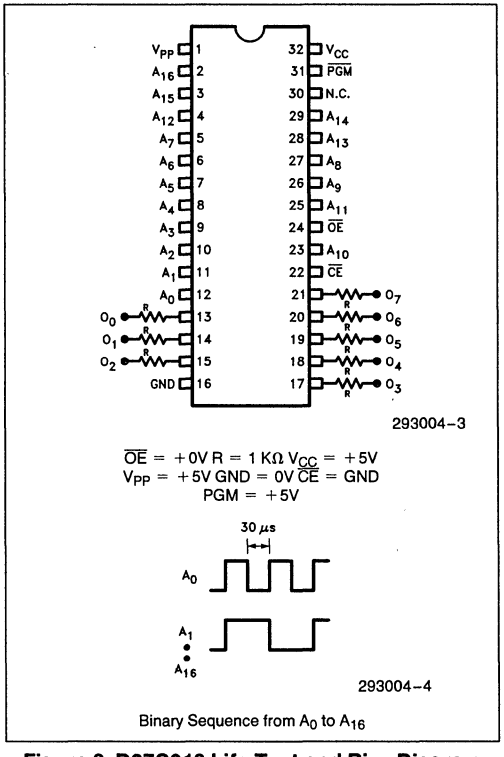

Figure 3. D27C010 Life Test and Bias Diagram

DATA RETENTION BAKE

This stress primarily accelerates charge loss from the floating gate. The devices are more than 98% programmed and baked at 250°C for ceramic and 140°C for plastic devices. No electrical bias is applied. This test also evaluates mechanical reliability and process stability. Data retention bake is also referred to as high-temperature bake or storage. The acceleration factors are stated for this stress, but the results are not included in the FIT rate calculation. Typically, fewer than 1% of the devices will fail to hold their programmed pattern after 150 years at 55°C.

TEMPERATURE CYCLE

Temperature cycling evaluates the package's mechanical integrity by sequentially exposing the devices to an air-to-air temperature extreme of −65°C to +150°C (Condition C) or −55°C to +125°C (Condition B) per MIL-STD-883. A broad variety of mechanical failure modes such as loss of hermeticity (CerDIP), die attach failure, bond wire lifting, thin film damage, and die cracking are expected to be accelerated during this test. Since electrical parameter can be affected by this test, both electrical and hermetic testing are performed as the end point tests.

REFERENCES

1. D. Baglee, L. Nanneman, C. Huang, "28th Annual Proceedings of the International Reliability Physics Symposium," pp 12–18, 1990.
2. E. Anolick, G. Nelson, "17th Annual Proceedings of the International Reliability Physics Symposium," 1979.
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CERDIP Reliability Data Summary

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates. Data for CERDIP and plastic EPROMs is treated separately.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler problems cause failures to occur. These "failures" are not a result of the specific test just completed. They are removed from the sample lot size and are not included in any failure rate calculations. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and these suspected "invalid" failures are put aside for retesting, decreasing the lot size for a succeeding test. If these parts are found to be defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

D27C256
(Six Digit Suffixes)

The Intel 27C256 is a 256K bit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM).

Number of Bits: 262,144
Organization: 32K x 8
Pin Out: 28 Pin JEDEC Approved

Die Size: 167 mils x 86 mils
Process: CHMOS III-E
Cell Size: 3.4 μm x 3.5 μm
Programming Voltage: 12.75V
Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1989	0/2000	0/1999	0/0	0/0	0/173	0/173	0/173	0/173	0/0
1990	1/4922	1/4859	0/0	0/0	0/2088	0/2088	0/642	0/546	1/450
Totals	1/6922	1/6858	0/0	0/0	0/2261	0/2261	0/815	0/719	1/450
	A	B							C

Infant Mortality Rate based on 48 hour ELT and HVELT data is 0.011%. ($1/_{8722}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
1.38×10^6 8.23×10^5	0.3 HVELT 0.3 ELT	2.25×10^8 5.15×10^6	1.43×10^8 3.27×10^6	1 1		
			Total 0.3 eV Failures =	2	13.4	21.1
1.38×10^6 8.23×10^5	0.6 HVELT 0.6 ELT	5.42×10^7 3.22×10^7	2.18×10^7 1.30×10^7	0 0		
			Total 0.6 eV Failures =	0	0.0	0.0
1.38×10^6 8.23×10^5	1.0 HVELT 1.0 ELT	6.25×10^8 3.72×10^8	1.37×10^8 8.15×10^7	0 0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate:		13.4	21.1

θ_{JA} = 58°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 331.2°K
T(70) = 346.2°K
T(125) = 401.2°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.2	452.0	2722.1
70°C	4.0	15.8	99.0	1076.7

D27C256 (Continued)
(Six Digit Suffixes)

Table 3: Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1989	0/0	0/258	0/258	0/78	0/78	0/78
1990	0/600	1/1245	0/1116	0/360	0/282	0/282
Totals	0/600	1/1503	0/1374	0/438	0/360	0/360
Percent	0.0%	0.073%	0.0%	0.0%	0.0%	0.0%
		D				

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 1 defect not found
B 1 V_{CC} min fail (0.3 eV)
C 1 defect not found (0.3 eV)
D 1 charge loss failure

5

D27C512

The Intel 27C512 is a 512K ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM).

Number of Bits: 524,288
Organization: 64K x 8
Pin Out: 28 Pin JEDEC Approved

Die Size: 210 mils x 127 mils
Process: CHMOS III-E
Cell Size: 3.4 μm x 3.5 μm
Programming Voltage: 12.75V
Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1989	N/A	N/A	N/A	N/A	2/4595	1/4593	0/450	0/450	2/450
Totals	0/0	0/0	0/0	0/0	1/4595	0/4593	0/450	0/450	2/450
					A	B			C

Infant Mortality Rate based on 48 hour HVELT data is 0.044%. ($^{2}/_{4595}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
1.38×10^6	0.3 HVELT	2.26×10^8	1.43×10^8	2		
			Total 0.3 eV Failures =	2	13.6	21.5
1.38×10^6	0.6 HVELT	5.45×10^7	2.19×10^7	1		
			Total 0.6 eV Failures =	0	36.9	92.0
1.38×10^6	1.0 HVELT	6.32×10^8	1.38×10^8	0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate:		50.6	113.5

θ_{JA} = 52°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.9°K
T(70) = 345.9°K
T(125) = 400.9°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.4	456.8	2722.1
70°C	4.0	15.8	99.8	1076.7

D27C512 (Continued)

Table 3: Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1990	0/599	0/599	0/598	0/204	0/204	2/204
Totals	0/599	0/599	1/598	0/204	0/204	2/204
Percent	0.0%	0.0%	0.167%	0.0%	0.0%	0.980%
			D			E

Failure Analysis:

Unit ID Failure Mechanism or Mode

A 1 single bit charge loss, 1 single bit charge gain
B 1 single bit charge gain (0.6 eV)
C 2 outputs blown (0.3 eV)
D 1 single bit charge loss
E 2 gross leak failures
F 1 gross leak failure

5

D27C010/27C011/27C100

The Intel 27C010, 27C011 and 27C100 are 1 Mbit ultraviolet Erasable and electrically Programmable Read Only Memories (EPROMs).

Number of Bits: 1,048,576

Organization: 128K x 8 (27C010/100)
8 x 16K x 8 (27C011)

Pin Out: 32 Pin JEDEC Approved (27C010)
28 Pin JEDEC Approved (27C011)
32 Pin ROM Compatible (27C100)

Die Size: 209 mils x 196 mils

Process: CHMOS III-E

Cell Size: 3.4 μm x 3.5 μm

Programming Voltage: 12.75V

Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1989	13/33049	6/32952	0/1385	0/342	6/1200	3/1193	2/1164	0/1040	0/331
1990	4/9470	0/9450	0/0	0/0	0/288	0/280	0/192	0/192	0/125
Totals	17/42519	6/42453	0/1385	0/342	6/1488	3/1473	2/1356	0/1232	0/456
	A	B			C	D	E		

Infant Mortality Rate based on 48 hour ELT and HVELT data is 0.040%. ($^{17}/_{42766}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
1.43×10^6 5.93×10^6	0.3 HVELT 0.3 ELT	2.35×10^8 3.73×10^7	1.49×10^8 2.36×10^7	9 5		
			Total 0.3 eV Failures =	14	58.2	91.9
1.43×10^6 5.93×10^6	0.6 HVELT 0.6 ELT	5.69×10^7 2.35×10^8	2.28×10^7 9.42×10^7	1 0		
			Total 0.6 eV Failures =	1	6.9	17.2
1.43×10^6 5.93×10^6	1.0 HVELT 1.0 ELT	6.61×10^8 2.73×10^9	1.44×10^8 5.95×10^8	0 1		
			Total 1.0 eV Failures =	1	0.6	2.7
			Combined Failure Rate:		65.7	111.8

θ_{JA} = 48°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.7°K
T(70) = 345.7°K
T(125) = 400.7°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.6	460.1	2722.1
70°C	4.0	15.9	100.3	1076.7

D27C010/27C011/27C100 (Continued)

Table 3. Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1989	1/399	5/3201	6/3156	1/1012	0/1011	2/1011
1990	0/0	0/677	1/488	0/156	0/156	0/156
Totals	1/399	5/3878	7/3644	1/1168	0/1167	2/1167
Percent	0.251%	0.129%	0.192%	0.086%	0.0%	0.171%
	F	G	H	I		J

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 7 mobile ionic contamination, 5 charge gain/loss, 3 speed downbinners, 1 V_{CC}min, 1 NVD
B 1 junction spiking (0.6 eV), 2 fab defects (0.3 eV), 1 ionic contamination (1.0 eV), 2 NVD (0.3 eV)
C 2 output shorts (0.3 eV), 3 fab defects (0.3 eV), 1 particle induced lsb fail (0.3 eV)
D 2 fab defects (0.3 eV), 1 junction spike (0.6 eV)
E 1 particle induced decoder fail (0.3 eV), 1 defect not found (0.3 eV)
F 1 single bit charge loss
G 3 single bit charge loss/gain, 2 defect not found
H 4 single bit charge loss, 1 spiked contact, 1 BPSG breakdown, 1 defect not found
I 1 single bit charge loss
J 2 speed degradation—defect not found

5

D27C210

The Intel 27C210 is a 1 Mbit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM).

Number of Bits: 1,048,576

Organization: 64K x 16

Pin Out: 40 Pin JEDEC Approved

Die Size: 201 mils x 236 mils

Process: CHMOS III-E

Cell Size: 3.4 μm x 3.5 μm

Programming Voltage: 12.75V

Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1989	7/27729	5/19772	1/399	1/398	1/1378	3/1362	7/1359	2/892	0/0
1990	0/4193	0/2192	0/195	0/195	1/4577	1/4476	1/1025	0/931	0/401
Totals	7/31922	5/21964	1/594	1/593	2/5955	4/5838	8/2384	2/1823	0/401
	A	B	C	D	E	F	G	H	

Infant Mortality Rate based on 48 hour ELT and HVELT data is 0.021%. ($^{8}/_{36971}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
2.87×10^6 3.13×10^6	0.3 HVELT 0.3 ELT	4.17×10^8 1.98×10^7	2.98×10^8 1.25×10^7	12 3		
			Total 0.3 eV Failures =	15	34.5	54.5
2.87×10^6 3.13×10^6	0.6 HVELT 0.6 ELT	1.14×10^8 1.25×10^8	4.58×10^7 5.00×10^7	4 2		
			Total 0.6 eV Failures =	6	30.6	76.6
2.87×10^6 3.13×10^6	1.0 HVELT 1.0 ELT	1.33×10^9 1.46×10^9	2.90×10^8 3.17×10^8	0 0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate:		65.1	131.1

θ_{JA} = 42°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.4°K
T(70) = 345.4°K
T(125) = 400.4°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.9	465.0	2722.1
70°C	4.0	16.0	101.1	1076.7

D27C210 (Continued)

Table 3: Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1989	2/613	4/2495	6/2438	0/695	1/766	1/686
1990	1/1136	0/1519	0/1391	0/510	0/510	1/432
Totals	3/1747	4/4014	6/3829	0/1205	1/1276	2/1118
Percent	0.172%	0.100%	0.157%	0.0%	0.078%	0.179%
	I	J	K		L	M

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 3 input leakage, 2 charge loss, 1 V_{OH} fail, 1 NVD
B 4 single bit charge loss (0.6 eV), 1 NVD (0.3 eV)
C 1 input leakage (0.3 eV)
D 1 byte failure (0.3 eV)
E 2 lsb failures (0.3 eV)
F 1 speed failure (0.3 eV), 2 lsb (0.3 eV), 1 input leakage (0.3 eV)
G 1 V_{OL}/V_{OH} fail (0.3 eV), 2 charge loss fails (0.6 eV), 5 lsb failures (0.3 eV)
H 2 lsb failures (0.3 eV)
I 1 lsb failure, 1 column leakage, 1 single bit charge loss
J 2 charge loss, 1 fab defect, 1 lsb fail
K 2 single bit charge loss, 1 V_{CC}min fail, 1 lsb fail, 1 NVD, 1 defect not found
L 1 single bit charge loss
M 1 fine leak failure, 1 oxide breakdown

5

D27C020

The Intel 27C020 is a 2 Mbit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM).

Number of Bits: 2,097,152

Organization: 256K x 8

Pin Out: 32 Pin JEDEC Approved

Die Size: 210 mils x 342 mils

Process: CHMOS III-E

Cell Size: 3.4 μm x 3.5 μm

Programming Voltage: 12.75V

Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1990	0/317	0/316	0/316	0/314	4/4231	2/4218	2/2636	0/428	5/2455
Totals	0/317	0/316	0/316	0/314	4/4231	2/4218	2/2636	0/428	5/2455
					A	B	C		D

Infant Mortality Rate based on 48 hour ELT and HVELT data is 0.088%. ($^{4}/_{4548}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FiTS (60% UCL)	
		55°C	70°C		55°C	70°C
4.09×10^6 3.02×10^5	0.3 HVELT 0.3 ELT	6.70×10^8 1.90×10^6	4.24×10^8 1.21×10^6	9 0		
			Total 0.3 eV Failures =	9	15.7	24.8
4.09×10^6 3.02×10^5	0.6 HVELT 0.6 ELT	1.62×10^8 1.20×10^7	6.50×10^7 4.81×10^6	0 0		
			Total 0.6 eV Failures =	0	0.0	0.0
4.09×10^6 3.02×10^5	1.0 HVELT 1.0 ELT	1.89×10^9 1.40×10^8	4.11×10^8 3.04×10^7	0 0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate:		15.7	24.8

θ_{JA} = 42°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.6°K
T(70) = 345.6°K
T(125) = 400.6°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.7	461.7	2722.1
70°C	4.0	15.9	100.6	1076.7

D27C020 (Continued)

Table 3: Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1990	1/736	0/597	0/595	0/228	0/228	1/227
Totals	1/736	1/597	0/595	0/228	0/228	0/227
Percent	0.136%	0.168%	0.0%	0.0%	0.0%	0.0%
	E	F				

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 4 mobile ionic contamination
B 1 I_{PP} leakage (0.3 eV), 1 lsb failure (0.3 eV)
C 1 speed downgraded unit (0.3 eV), 1 I_{PP} leakage (0.3 eV)
D 4 speed failures (0.3 eV), 1 lsb fail (0.3 eV)
E 1 V_{CC}min fail
F 1 single bit charge loss

5

D27C220

The Intel 27C220 is a 2 Mbit ultraviolet Erasable and electrically Programmable Read Only Memory (EPROM).

Number of Bits: 2,097,152

Organization: 128K x 16

Pin Out: 40 Pin JEDEC Approved

Die Size: 216 mils x 385 mils

Process: CHMOS III-E

Cell Size: 3.4 μm x 3.5 μm

Programming Voltage: 12.75V

Technology: CMOS

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1990	0/315	1/314	0/308	0/308	0/1741	1/1741	0/331	0/331	0/0
Totals	0/315	1/314	0/308	0/308	0/1741	1/1741	0/331	0/331	0/0
		A				B			

Infant Mortality Rate based on 48 hour ELT and HVELT data is 0.0%. ($\%_{2056}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
4.87×10^5	0.3 HVELT	7.99×10^7	5.06×10^7	1		
6.07×10^5	0.3 ELT	3.83×10^6	2.42×10^6	0		
			Total 0.3 eV Failures =	1	24.0	38.0
4.87×10^5	0.6 HVELT	1.94×10^7	7.77×10^6	0		
6.07×10^5	0.6 ELT	2.42×10^7	9.68×10^6	0		
			Total 0.6 eV Failures =	0	0.0	0.0
4.87×10^6	1.0 HVELT	2.26×10^8	4.92×10^7	0		
6.07×10^5	1.0 ELT	2.82×10^8	6.14×10^7	1		
			Total 1.0 eV Failures =	1	4.0	18.2
			Combined Failure Rate:		28.0	56.2

θ_{JA} = 42°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.4°K
T(70) = 345.4°K
T(125) = 400.4°K
T(250) = 523.1°K

Thermal Acceleration Factors

	125°C			250°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.9	465.0	2722.1
70°C	4.0	16.0	101.1	1076.7

D27C220 (Continued)

Table 3: Additional Qualification Tests

Year	250°C Data Retention Bake			Temp Cycles −65°C to +150°C		
	48 Hrs	168 Hrs	500 Hrs	200 Cy	500 Cy	1K Cy
1990	0/1049	1/1049	0/1048	0/294	0/294	0/294
Totals	0/1049	1/1049	0/1048	0/294	0/294	0/294
Percent	0.0%	0.095%	0.0%	0.0%	0.0%	0.0%
		C				

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 1 contamination failure (1.0 eV)

B 1 speed failure, single bit related (0.3 eV)

C 1 column leakage at 4.5V (0.3 eV)

5

Plastic Reliability Data Summary

INTRODUCTION

The following information is written to provide OTP (one time programmable) users with a reliability summary of Intel's plastic production EPROMs in both DIP and PLCC packages. It includes brief test descriptions, a description of plastic packaging compounds and the reliability data obtained during the qualification and subsequent monitor of the N27C256, N27C010, and N27C210 devices.

PLASTIC PACKAGE CHARACTERISTICS

The EPROM plastic package is composed of flame retardant plastic/epoxy which meets the rating requirements of US94V0, $\frac{1}{8}$" minimum. The die is attached with non-conductive epoxy to a copper leadframe. Bonding is accomplished through gold thermal compression bonding and the leads are finished with a 60% tin/40% lead solder coat.

EPROM ELECTRICAL CHARACTERISTICS

OTP EPROMs in plastic are tested to the same electrical/parametric levels as their counterparts in CERDIP. These characteristics include input and output voltage levels, speeds, leakage, and power requirement characteristics over the full commercial temperature operating range of 0°C to 70°C. Performance capabilities are identical to that of the corresponding CERDIP versions, though plastic speed offerings may differ.

RELIABILITY/QUALITY TESTS

Reliability tests performed on plastic packaged devices are essentially identical to those used on the corresponding CERDIP versions. However, because plastic encapsulation cannot hermetically seal the die from the environment, two separate moisture resistance tests are regularly performed to determine the effect of moisture on the die and package. In addition, with plastic in intimate contact with the die surface, temperature cycling and thermal shock testing become especially important to check for thermal expansion mismatches between the layers, which could lead to thin film cracking. The High Temperature Storage test, run at 250°C for CERDIP, must be done at 140°C to prevent damaging the plastic epoxy. A brief description of the two plastic specific moisture tests follows. A description of the remaining reliability stresses, common to both plastic and CERDIP may be found in the discussion preceding the CERDIP reliability data.

85°C/85% RH

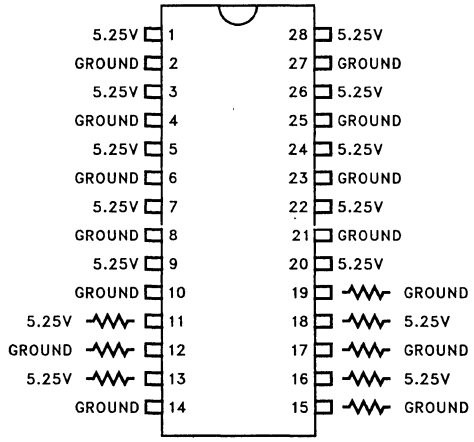
This test subjects the device to a high temperature, high humidity environment while bias is applied. The object of the test is to accelerate failure mechanisms through electrolytic processes, such as metal corrosion.

Once moisture penetrates the plastic to the die surface, voltage and/or moisture may activate contaminants within the die thin films or on the die surface to create electrolytic corrosion or other moisture effects, such as charge loss. See Figure 4 for a typical 85/85 bias diagram.

STEAM TEST

This test places the device in a 121°C/2 atm pressure environment (100% humidity) without bias. The objective of this test is to accelerate failures of the device due strictly to moisture effects within the die thin films. Corrosion, as typically seen in plastic encapsulated devices, is a very minor contributor to Intel EPROM failure mechanisms. The EPROM storage cell, with its unique structure and composition, generates a distinctive failure mode which requires special considerations and solutions. The floating gate is a highly phosphorous doped structure which stores electrons, forming the basis of the nonvolatile memory cell. Passivation defects or marginalities can allow moisture penetration to a single EPROM cell causing oxide deterioration and subsequent charge loss. This becomes the predominant failure mode for EPROMs, as opposed to corrosion which historically has been the dominant plastic mode of failure. Intel has developed a proprietary, multi-layer passivation which, by preventing moisture penetration through the die thin films, has successfully eliminated this failure mechanism.

In addition to these two standard moisture tests, Intel subjects all surface mount plastic devices to "pre-conditioning" stresses before 85/85 stressing and temperature cycling. The devices are put into an 85°C/30% RH environment for 168 hours to provide a specified level of moisture in the plastic, then the devices are put through a simulated surface mount solder cycle. At the high solder temperatures encountered, the plastic may delaminate from the leadframe or die cracking may develop. All the CHMOS III-E plastic EPROMs pass this test without problems.



Pin	Pin Name	Stress
1	V_{PP}	5.25V
2	A_{12}	Ground
3	A_7	5.25V
4	A_6	Ground
5	A_5	5.25
6	A_4	Ground
7	A_3	5.25V
8	A_2	Ground
9	A_1	5.25V
10	A_0	Ground
11	O_0	5.25V
12	O_1	Ground
13	O_2	5.25V
14	Ground	Ground
15	O_3	Ground
16	O_4	5.25V
17	O_5	Ground
18	O_6	5.25V
19	O_7	Ground
20	$\overline{CE}$	5.25V
21	A_{10}	Ground
22	$\overline{OE}$	5.25V
23	A_{11}	Ground
24	A_9	5.25V
25	A_8	Ground
26	A_{13}	5.25V
27	A_{14}	Ground
28	V_{CC}	5.25V

Figure 4. Typical 85/85 Bias Diagram

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N27C256

The N27C56 is identical to the D27C256, except that it is encapsulated in a windowless plastic package and so may be programmed only once. This lack of re-programmability requires unique factory testing and qualification tests. Since plastic encapsulation is inherently non-hermetic and places additional stress on the die, device performance in stresses such as 85°C/85% RH, steam (121°C/2 atm/100% RH) and temperature cycling become important.

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1990	0/0	0/0	0/0	0/0	0/998	0/998	0/300	0/300	0/300
Totals	0/0	0/0	0/0	0/0	0/998	0/998	0/300	0/300	0/300

Infant Mortality Rate based on 48 hour HVELT data is 0.0%. ($\%_{998}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
3.72×10^5	0.3 HVELT	5.97×10^7	3.80×10^7	0		
		Total 0.3 eV Failures =		0	15.9	25.0
3.72×10^5	0.6 HVELT	1.42×10^7	5.75×10^6	0		
		Total 0.6 eV Failures =		0	0.0	0.0
3.72×10^5	1.0 HVELT	1.61×10^8	3.56×10^7	0		
		Total 1.0 eV Failures =		0	0.0	0.0
			Combined Failure Rate:		15.9	25.0

θ_{JA} = 83°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 332.5°K
T(70) = 347.5°K
T(125) = 402.5°K
T(250) = 413.2°K

Thermal Acceleration Factors

	125°C			140°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.2	38.2	432.0	78.7
70°C	3.9	15.5	95.9	31.1

N27C256 (Continued)

Table 3: Additional Qualification Tests

Year	Temperature/Humidity/Bias 85°C/85% RH				Steam 121°C/2 atm		
	168 Hrs	500 Hrs	1K Hrs	2K Hrs	96 Hrs	168 Hrs	336 Hrs
1990	0/201	0/201	0/201	0/201	0/401	0/401	0/401
Totals	0/201	0/201	0/201	0/201	0/401	0/401	0/401
Percent	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%

Year	Temp Cycles −55°C to +125°C		
	200 Cy	500 Cy	1K Cy
1990	0/225	0/225	0/225
Totals	0/225	0/225	0/225
Percent	0.0%	0.0%	0.0%

Year	140°C Data Retention Bake		
	168 Hrs	500 Hrs	1K Hrs
1990	0/201	0/201	0/201
Totals	0/201	0/201	0/201
Percent	0.0%	0.0%	0.0%

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N27C010

The N27C010 is identical to the D27C010, except that it is encapsulated in a windowless plastic package and so may be programmed only once. This lack of re-programmability requires unique factory testing and qualification tests. Since plastic encapsulation is inherently non-hermetic and places additional stress on the die, device performance in stresses such as 85°C/85% RH, steam (121°C/2 atm/100% RH) and temperature cycling take on added significance.

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1990	1/5926	1/5925	0/0	0/0	0/0	2/2675	0/500	3/498	0/299
Totals	1/5926	1/5925	0/0	0/0	0/0	2/2675	0/500	3/498	0/299
	A	B				C		D	

Infant Mortality Rate based on 48 hour HVELT data is 0.017%. ($1/_{5926}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
7.40×10^5	0.3 HVELT	1.20×10^8	7.60×10^7	5		
7.11×10^5	0.3 ELT	4.42×10^6	2.81×10^6	1		
			Total 0.3 eV Failures =	6	59.1	93.1
7.40×10^5	0.6 HVELT	2.86×10^7	1.15×10^7	0		
7.11×10^5	0.6 ELT	2.75×10^7	1.11×10^7	0		
			Total 0.6 eV Failures =	0	0.0	0.0
7.40×10^5	1.0 HVELT	3.27×10^8	7.21×10^7	0		
7.11×10^5	1.0 ELT	3.14×10^8	6.92×10^7	0		
			Total 1.0 eV Failures =	0	0.0	0.0
			Combined Failure Rate:		59.1	93.1

θ_{JA} = 71°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 331.9°K
T(70) = 346.9°K
T(125) = 401.9°K
T(250) = 413.1°K

Thermal Acceleration Factors

	125°C			140°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	38.6	441.8	78.7
70°C	4.0	15.6	97.4	31.1

N27C010 (Continued)

Table 3: Additional Qualification Tests

Year	Temperature/Humidity/Bias 85°C/85% RH				Steam 121°C/2 atm		
	168 Hrs	500 Hrs	1K Hrs	2K Hrs	96 Hrs	168 Hrs	336 Hrs
1990	0/466	0/466	0/466	0/225	0/0	1/762	1/759
Totals	0/466	0/466	0/466	0/225	0/0	1/762	1/759
Percent	0.0%	0.0%	0.0%	0.0%	0.0%	0.131%	0.132%
						E	F

Year	Temp Cycles −65°C to +150°C		
	200 Cy	500 Cy	1K Cy
1990	0/413	0/413	0/185
Totals	0/413	0/413	0/185
Percent	0.0%	0.0%	0.0%

Year	140°C Data Retention Bake		
	168 Hrs	500 Hrs	1K Hrs
1990	0/100	0/100	0/100
Totals	0/100	0/100	0/100
Percent	0.0%	0.0%	0.0%

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 1 single bit charge loss
B 1 I_{PP} failure (0.3 eV)
C 2 single bit charge loss (0.6 eV)
D 3 lsb failures (0.3 eV)
E 1 single bit charge loss—passivation damage
F 1 single bit charge loss—no passivation damage

5

N27C210

The N27C210 is identical to the D27C210, except that it is encapsulated in a windowless plastic package and so may be programmed only once. This lack of re-programmability requires unique factory testing and qualification tests. Since plastic encapsulation is inherently non-hermetic and places additional stress on the die, device performance in stresses such as 85°C/85% RH, steam (121°C/2 atm/100% RH) and temperature cycling become important.

Table 1: Lifetest Data Summary

Year	Burn-In 48 Hrs	5.25V/125°C Dynamic Lifetest			6.5V/125°C Dynamic Lifetest				
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1990	0/0	0/0	0/0	0/0	0/1095	0/1094	0/300	0/300	0/297
Totals	0/0	0/0	0/0	0/0	0/1095	0/1094	0/300	0/300	0/297

Infant Mortality Rate based on 48 hour HVELT data is 0.0%. ($0/_{1095}$)

Table 2: Failure Rate Predictions

Actual Device Hours	Ea (eV)	Equivalent Device Hours		# Fail	Fail Rate in FITS (60% UCL)	
		55°C	70°C		55°C	70°C
6.83×10^5	0.3 HVELT	1.10×10^8	6.97×10^7	0		
		Total 0.3 eV Failures =		0	8.6	13.6
6.83×10^5	0.6 HVELT	2.69×10^7	1.08×10^7	0		
		Total 0.6 eV Failures =		0	0.0	0.0
6.83×10^5	1.0 HVELT	3.11×10^8	6.80×10^7	0		
		Total 1.0 eV Failures =		0	0.0	0.0
			Combined Failure Rate:		8.6	13.6

θ_{JA} = 53°C/W
V_{CC} = 5.25V
I_{CC} = 10 mA
VAF(6.5V/5.25V) = 26

Temp with θ_{JA}
T(55) = 330.9°K
T(70) = 345.9°K
T(125) = 400.9°K
T(250) = 413.1°K

Thermal Acceleration Factors

	125°C			140°C
	0.3 eV	*0.6 eV*	*1.0 eV*	*0.6 eV*
55°C	6.3	39.4	456.0	78.7
70°C	4.0	15.8	99.7	31.1

N27C210 (Continued)

Table 3: Additional Qualification Tests

Year	Temperature/Humidity/Bias 85°C/85% RH				Steam 121°C/2 atm		
	168 Hrs	500 Hrs	1K Hrs	2K Hrs	96 Hrs	168 Hrs	336 Hrs
1990	0/279	0/278	0/278	0/277	0/353	0/353	3/353
Totals	0/279	0/278	0/278	0/277	0/353	0/353	3/353
Percent	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.850%
							A

Year	Temp Cycles −55°C to +125°C			
	200 Cy	500 Cy	1K Cy	2K Cy
1990	0/211	0/211	0/400	1/400
Totals	0/211	0/211	0/400	1/400
Percent	0.0%	0.0%	0.0%	0.250%
				B

Year	140°C Data Retention Bake		
	168 Hrs	500 Hrs	1K Hrs
1990	0/310	0/310	0/310
Totals	0/310	0/310	0/310
Percent	0.0%	0.0%	0.0%

Failure Analysis:

Unit ID *Failure Mechanism or Mode*

A 3 lsb failures

B 1 lsb failure

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APPENDIX A

Failure Rate Calculations for 60% Upper Confidence Level

Step 1. Collect burn-in and lifetest data for each lot after 48 hours of burn-in through lifetest for each lot.

Step 2. Determine the failure mechanism and assign an activation energy (E_A) for each failure, except those occurring during the first 48 hrs.

Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0 eV–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours accumulated beyond 48 hours of burn-in.

NOTE:
The first 48 hours of burn-in at either 5.25V or 6.5V measure infant mortality and are not included in the failure rate calculation. Monitor lots will use only 5.25V data for the infant mortality evaluation (IME). See monitor flow chart, Figure 1.

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Example: 125°C Burn-In/Lifetest for a 2 lot sample

$$\frac{\#\text{ failures}}{\text{total }\#\text{ devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

Actual Device Hours = Σ (Number of Devices in Stress Interval) (Number of Hours in Stress Interval)
= 1201 (168 hrs–48 hrs) + 1200 (500 hrs–168 hrs)
+ 1098 (1000 hrs–500 hrs) + 1093 (2000 hrs–1000 hrs)
= 1201 (120 hrs) + 1200 (332 hrs) + 1098 (500 hrs)
+ 1093 (1000 hrs)
2.185 x 10^6 Device Hours

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \exp\left[\frac{-E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°K (Boltzmann's constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A_1 \exp\left[\frac{-E_A}{KT_1}\right]}{A_2 \exp\left[\frac{-E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

Where $A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

Where R_1 and R_2 are rates for a normal operating temp and an elevated temperature respectively.

$$R_1 = R_2 \times \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

However, since rate (R) has the units 1/time, we can think in terms of time to one failure or MTBF.

Thus:

$$R_1 = \frac{1}{t_1} \text{ where } t_1 = \text{MTBF at some temperature } T_1$$

and:

$$R_2 = \frac{1}{t_2} \text{ where } t_2 = \text{MTBF at some temperature } T_2$$

Thus the Arrhenius relation becomes:

$$\frac{1}{t_1} = \frac{1}{t_2} \times \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

or:

$$t_1 = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \times t_2$$

We then define the Acceleration Factor as:

$$\text{A.F.} = \frac{t_1}{t_2} = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398$°K, $T_1 = 328$°K

$$t_1 = 41.7\, t_2$$

Therefore, one hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy E_A = 0.6 eV. Then 41.7 is the thermal acceleration factor for time.

NOTE:
The Arrhenius Plot (Figure 2, Page 3) is simply ln (Acceleration Factor) vs. 1/Temperature normalized for an MTBF of one hour at 250°C (T_2). This plot can also be used to determine the acceleration factor between two temperatures other than 250°C.

For example: For a 0.3 eV failure at 125°C, the acceleration factor is 8.1 relative to a 0.3 eV failure at 250°C. For a 0.3 eV failure at 25°C, the acceleration factor is 152 relative to 250°C. Therefore, the acceleration factor between 125°C and 25°C is:

$$\text{A.F.} = \frac{t_1}{t_2} = \frac{152}{8.1} = 18.7$$

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:
The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the ambient temperature to arrive at the actual burn-in/lifetest temperatures.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\,(IV @ T_{Ambient}) + T_{Ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	#Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

The failure rates for individual failure mechanisms and the total combined failure rate can be predicted using the data table and the following formula:

$$\text{FITs} = \frac{\chi^2\,(n, \alpha)}{2T}\left(10^9\right)$$

Where χ^2 (n, α) is the value of the chi-squared distribution for n degrees of freedom and confidence level of α. The degrees of freedom, n = [2(# of failures)+2] for this application. T is the total equivalent device hours at T_1. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL (Upper Confidence Limit), the above formula converts to the following:

#Failures	FIT Rate (60% UCL)
0	$0.915 \times 10^9/T$
1	$2.02 \times 10^9/T$
2	$3.105 \times 10^9/T$
3	$4.17 \times 10^9/T$
3<#<15	$\left[\frac{1.049\,(\#\text{failures for a particular } E_A) + 1.0305}{T}\right]\left[10^9\right]$
>15	$\frac{[0.2533 + \sqrt{(4 \times \#\text{Failed}) + 3}]^2}{4T}\left[10^9\right]$

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Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient}$ = 125°C and I_{CC} active is 60 mA at $T_{Ambient}$ = 55°C.

Also assume that θ_{JA} = 35°C/W.

Then,

T_2 = (35°C/W) (57 mA) (5V) + 125°C
≅ 135°C = 408°K

T_1 = (35°C/W) (60 mA) (5V) + 55°C
≅ 65°C = 338°K

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors For 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C FIT Rate
0.3	2.185×10^6	5.85	1.278×10^7	0	81
0.6	2.185×10^6	34.18	7.468×10^7	2	42
1.0	2.185×10^6	359.93	7.864×10^8	1	3
				Total Combined Failure Rate =	126 FITs

Example 2:

Assume than an additional lot of 800 CHMOS III-E devices is burned in using a 6.5V lifetest as shown below. Assume further that the one failure shown at 168 hours is a 0.3 eV oxide failure. Using Table 2 below, a voltage acceleration factor of 26 results from a 1.25V voltage overstress (5.25V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0/800	1/800	0/799

Actual Device Hours = 800 (48 hrs−0 hrs) + 800 (168 hrs−48 hrs) + 799 (500 hrs−168 hrs)
= 3.997×10^5

Table 2. Time-Dependent Oxide Failure Voltage Accelerations Relative to 5.25V

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/cm)	Lifetest Stress Voltage			
				5.5V	6.0V	6.5V	7.0V
CHMOS III-E	5	235	2.15	1.9	7.0	26	93

ASSUMES:
1. Failure rate calculations use the appropriate acceleration factor for stress voltage versus 5.25V operating voltage (conservative).
2. Reference [2] E. Nelson Anolick.

Since this voltage accelerated stress is used to predict an oxide breakdown failure rate, the 5.25V burn-in/lifetest 55°C equivalent hours for E_A = 0.3 eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours as follows:

125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @55°C
5.25V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 x 26)	6.079×10^7
			Total Equivalent Device Hours for 0.3 eV Failures =	7.357×10^7

The following failure rate predictions include the total equivalent 55°C, E_A = 0.3 eV device hours found above:

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @55°C	# Fail	55°C FIT Rate
0.3 ELT	2.185×10^6	5.85	7.357×10^7	1	27
0.3 HVELT	3.997×10^5	(5.85 x 26)			
0.6 ELT	2.185×10^6	34.18	8.834×10^7	2	35
0.6 HVELT	3.997×10^5	34.18			
1.0 ELT	2.185×10^6	359.93	9.303×10^8	1	2
1.0 HVELT	3.997×10^5	359.93			
			Total Combined Failure Rate =		84 FITs

NOTES:
1. Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.
2. 1 FIT = 1 Failure Unit = 0.0001%/1K hours.

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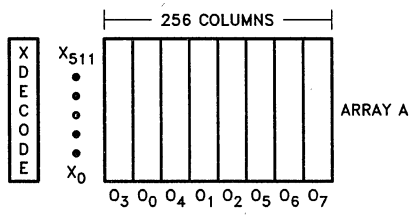
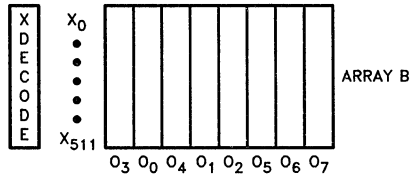
APPENDIX B
EPROM Bit Maps and Die Photos

27C256
(Six Digit Suffix) Array Organization and Bitmap



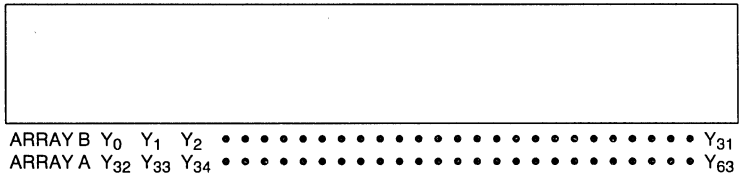
293004-22



293004-23

OUTPUTS 0–7

64 COLUMNS (32 IN ARRAY A, 32 IN ARRAY B)



Y DECODE

	A_{12}	A_{13}	A_{10}	A_1	A_0
Y_{00}	0	0	0	0	0
Y_{01}	0	0	0	0	1
Y_{02}	0	0	0	1	0
•	•	•	•	•	•
•	•	•	•	•	•
Y_{63}	1	1	1	1	1

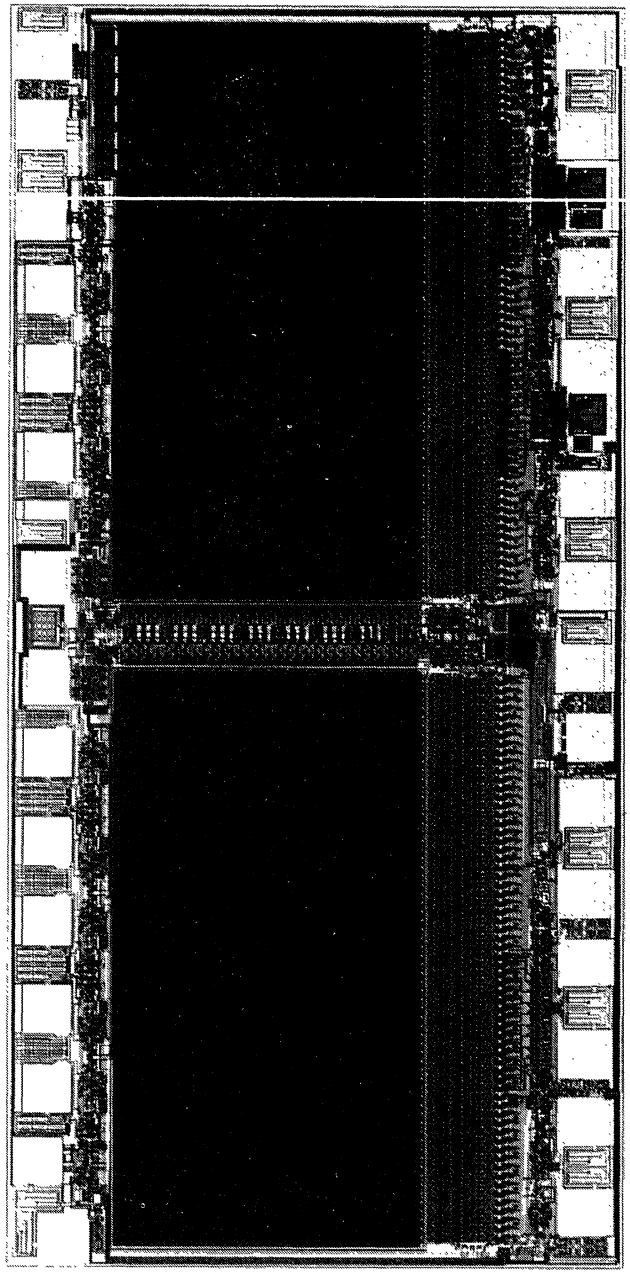
ARRAY SELECT

	A_{14}
ARRAY A	1
ARRAY B	0

X DECODE

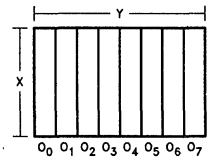
	A_7	A_6	A_5	A_4	A_3	A_2	A_{11}	A_9	A_8
X_{00}	0	0	0	0	0	0	0	0	0
X_{01}	0	0	0	0	0	0	0	0	1
X_{02}	0	0	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
X_{511}	1	1	1	1	1	1	1	1	1

27C256 (Six Digit Suffix) Die Photograph



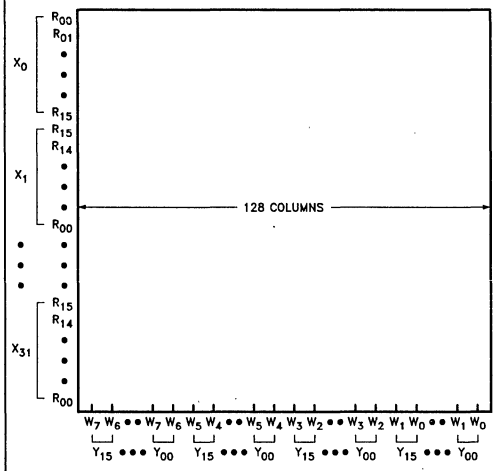
293004-18

27C512 Array Organization and Bitmap



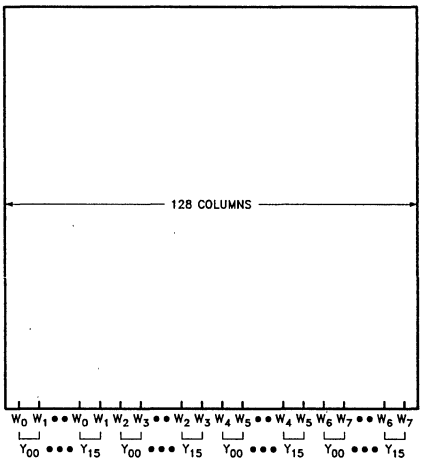
293004-25

OUTPUTS 0 THROUGH 3



293004-26

OUTPUTS 4 THROUGH 7



293004-27

Y DECODE

	A_{10}	A_2	A_1	A_0
Y_{00}	0	0	0	0
Y_{01}	0	0	0	1
Y_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
Y_{15}	1	1	1	1

W DECODE

	A_{12}	A_7	A_{14}
W_0	0	0	0
W_1	0	0	1
W_2	0	1	0
•	•	•	•
•	•	•	•
W_7	1	1	1

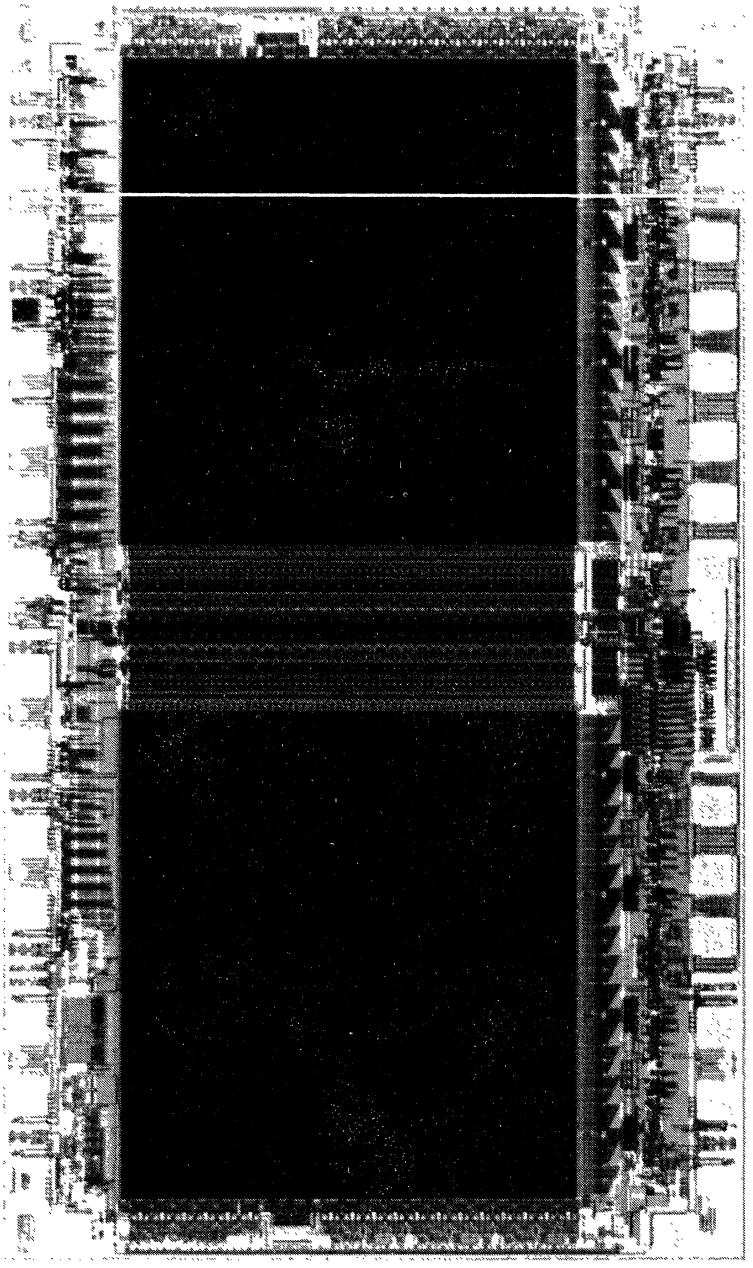
X DECODE

	A_6	A_5	A_4	A_3	A_{15}
X_{00}	0	0	0	0	0
X_{01}	0	0	0	0	1
X_{02}	0	0	0	1	0
•	•	•	•	•	•
•	•	•	•	•	•
X_{31}	1	1	1	1	1

R DECODE

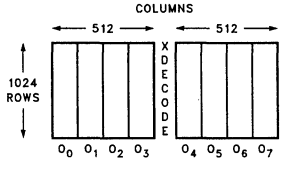
	A_{13}	A_{11}	A_9	A_8
R_{00}	0	0	0	0
R_{01}	0	0	0	1
R_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
R_{15}	1	1	1	1

27C512 Die Photograph



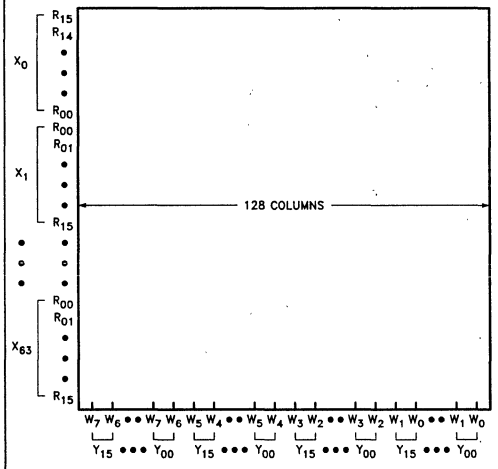
293004-24

27C010/100 Array Organization and Bitmap



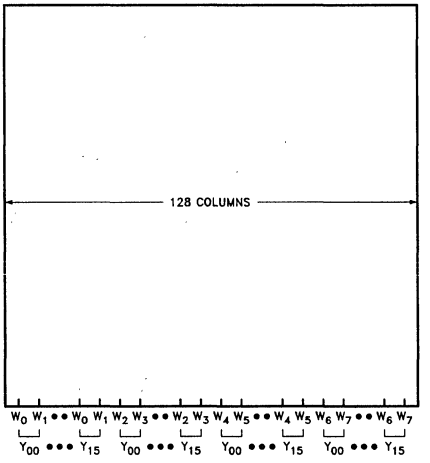
293004-19

OUTPUTS 0 THROUGH 3



293004-20

OUTPUTS 4 THROUGH 7



293004-21

Y DECODE

	A_{10}	A_2	A_1	A_0
Y_{00}	0	0	0	0
Y_{01}	0	0	0	1
Y_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
Y_{15}	1	1	1	1

W DECODE

	A_{16}	A_{15}	A_3
W_0	0	0	0
W_1	0	0	1
W_2	0	1	0
•	•	•	•
•	•	•	•
W_7	1	1	1

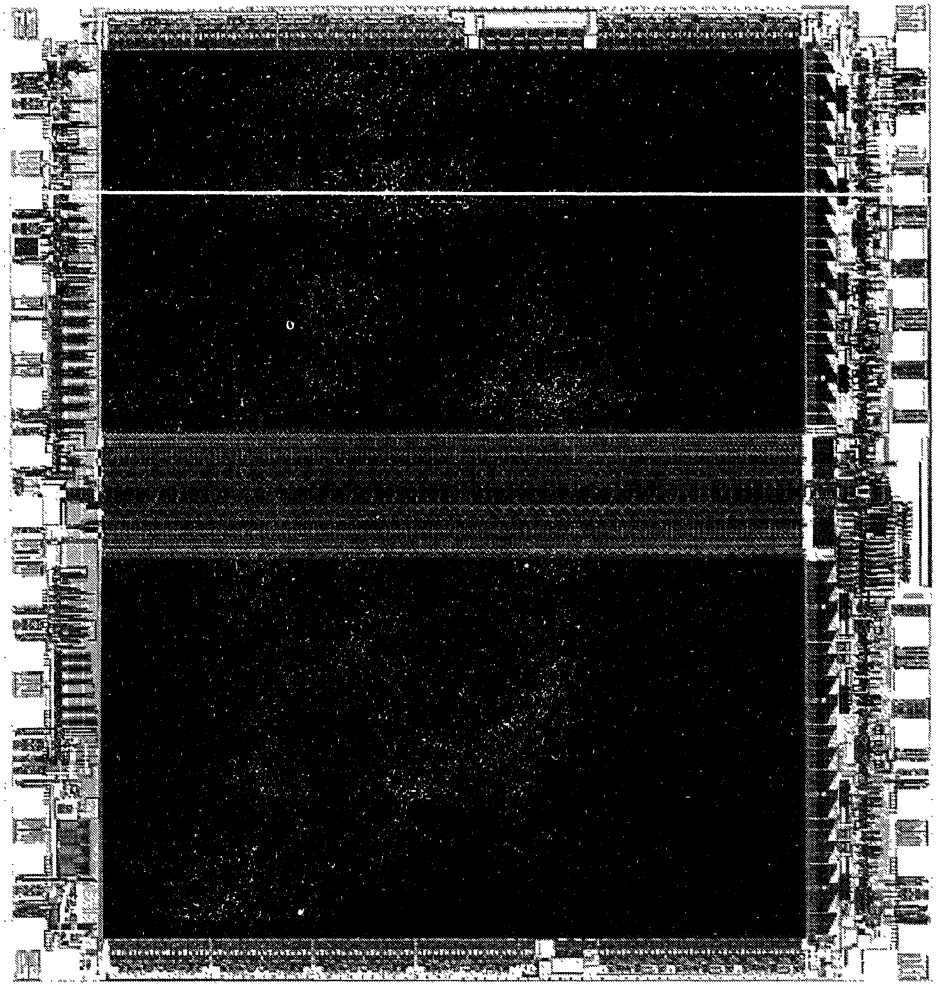
X DECODE

	A_4	A_5	A_6	A_7	A_{12}	A_{14}
X_{00}	0	0	0	0	0	0
X_{01}	0	0	0	0	0	1
X_{02}	0	0	0	0	1	0
•	•	•	•	•	•	•
•	•	•	•	•	•	•
X_{63}	1	1	1	1	1	1

R DECODE

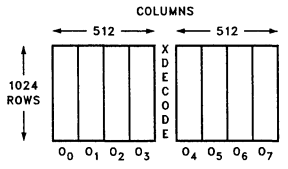
	A_{13}	A_{11}	A_9	A_8
R_{00}	0	0	0	0
R_{01}	0	0	0	1
R_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
R_{15}	1	1	1	1

27C010/27C100 Die Photograph



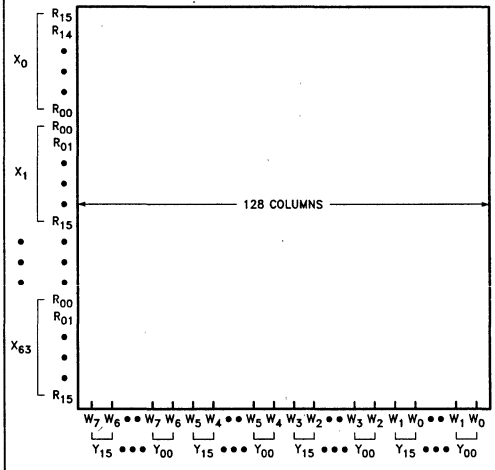
293004-7

27C011 Array Organization and Bitmap



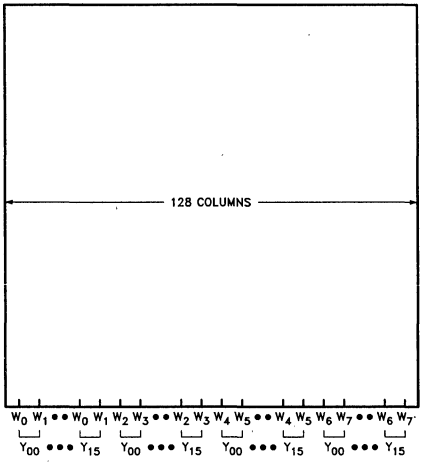
293004-15

OUTPUTS 0 THROUGH 3



293004-16

OUTPUTS 4 THROUGH 7



293004-17

Y DECODE

	A_{10}	A_2	A_1	A_0
Y_{00}	0	0	0	0
Y_{01}	0	0	0	1
Y_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
Y_{15}	1	1	1	1

W DECODE

	A_{12}	A_7	D_0
W_0	0	0	0
W_1	0	0	1
W_2	0	1	0
•	•	•	•
•	•	•	•
W_7	1	1	1

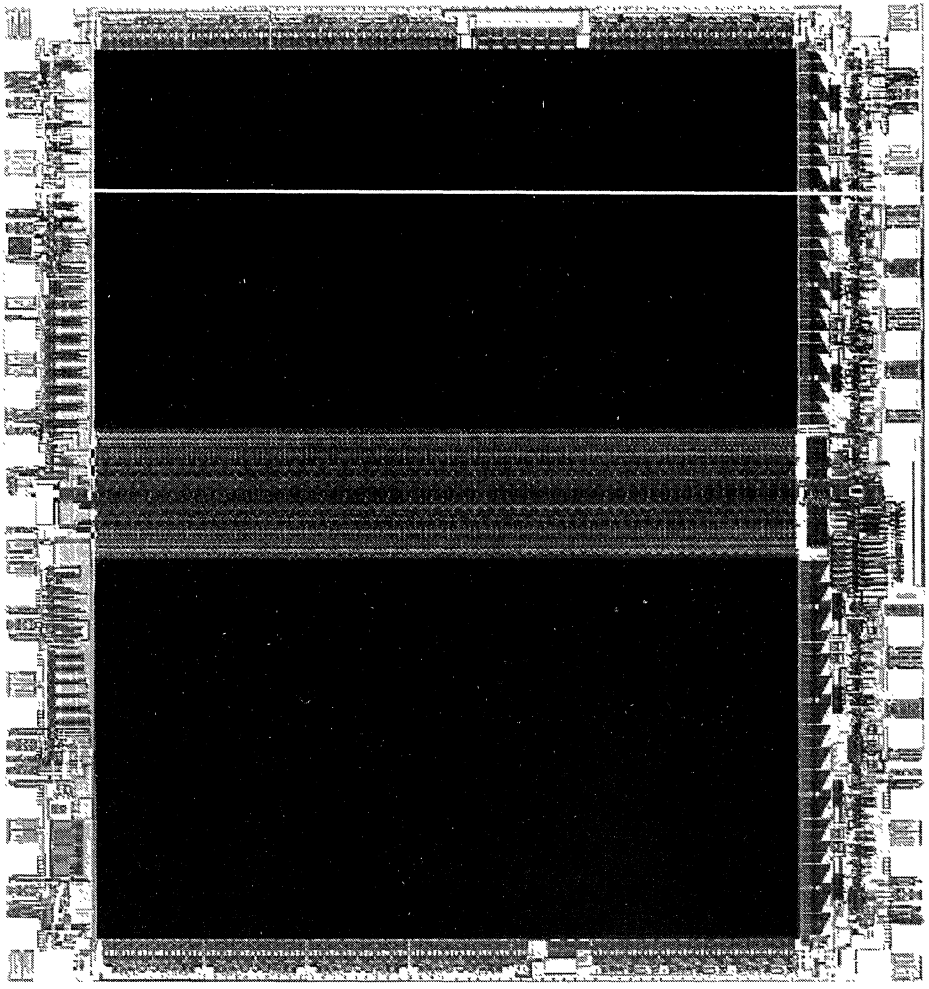
X DECODE

	D_1	A_3	A_4	A_5	A_6	A_8
X_{00}	0	0	0	0	0	0
X_{01}	0	0	0	0	0	1
X_{02}	0	0	0	0	1	0
•	•	•	•	•	•	•
•	•	•	•	•	•	•
X_{63}	1	1	1	1	1	1

R DECODE

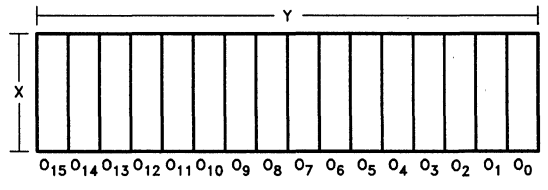
	A_{13}	D_2	A_9	A_{11}
R_{00}	0	0	0	0
R_{01}	0	0	0	1
R_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
R_{15}	1	1	1	1

27C011 Die Photograph

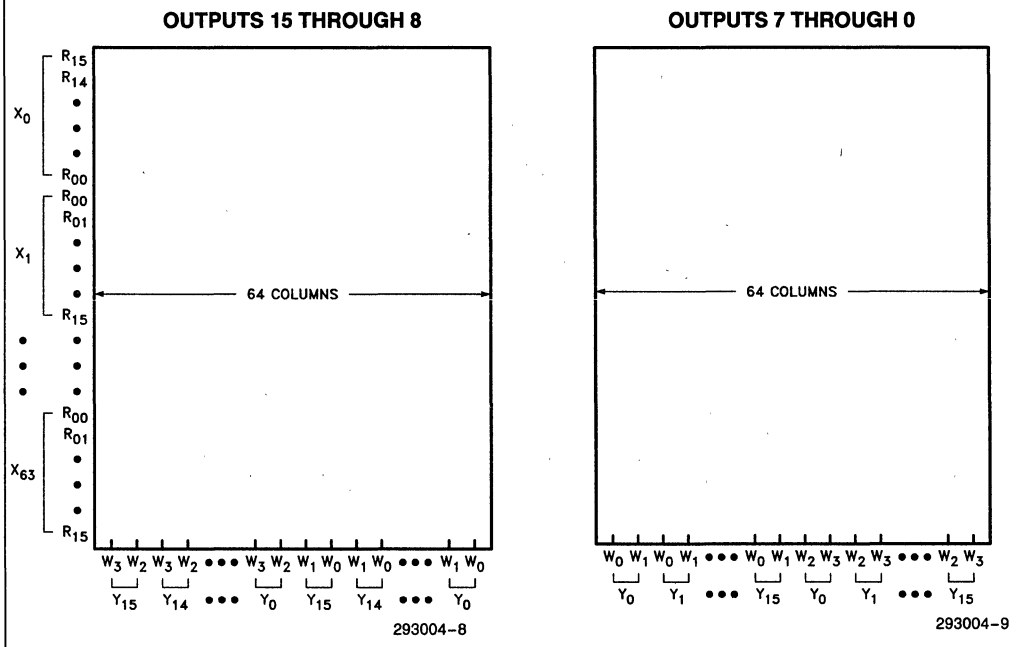


293004-7

27C210 Array Organization and Bitmap



293004-30



293004-8

293004-9

Y DECODE

	A_{13}	A_{15}	A_{14}	A_0
Y_{00}	0	0	0	0
Y_{01}	0	0	0	1
Y_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
Y_{15}	1	1	1	1

W DECODE

	A_1	A_2
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

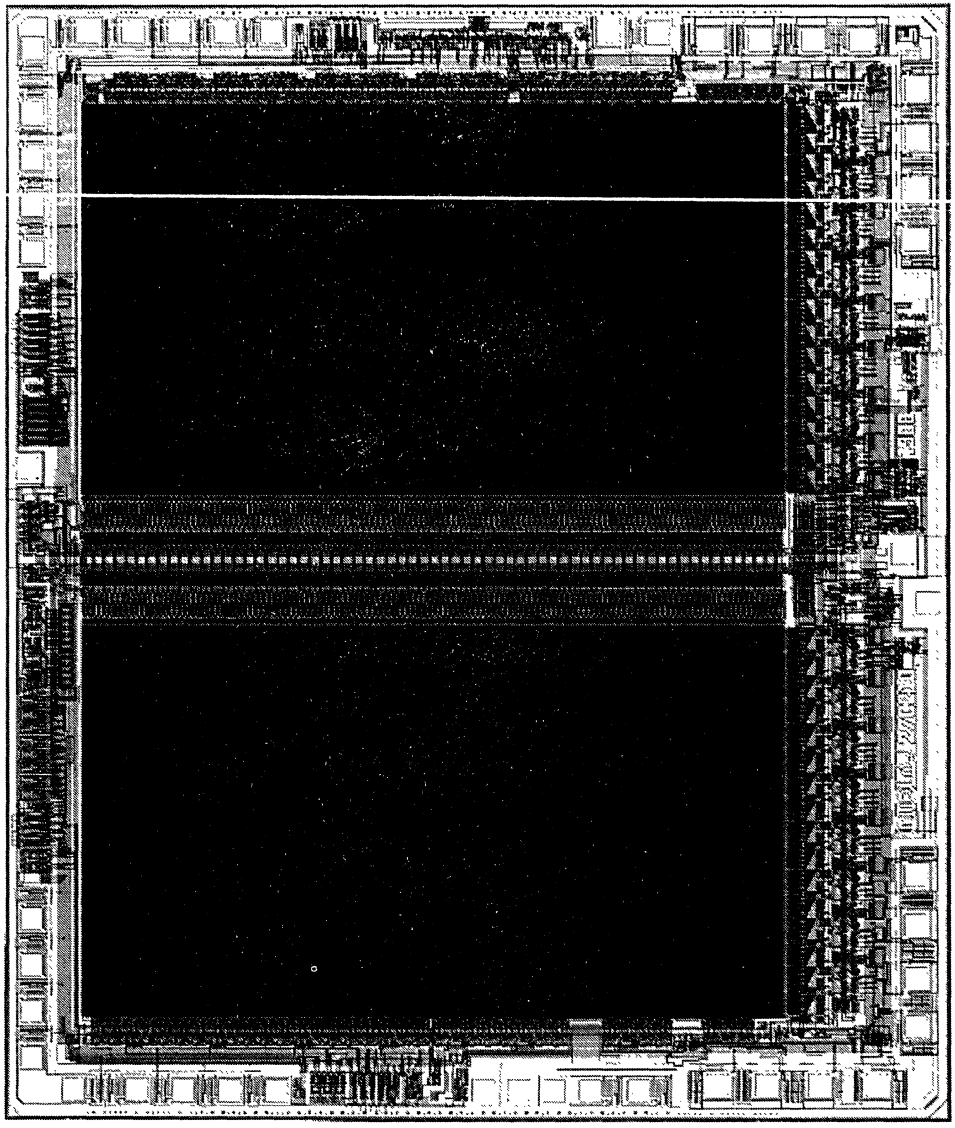
X DECODE

	A_8	A_7	A_6	A_5	A_4	A_3
X_{00}	0	0	0	0	0	0
X_{01}	0	0	0	0	0	1
X_{02}	0	0	0	0	1	0
•	•	•	•	•	•	•
•	•	•	•	•	•	•
X_{63}	1	1	1	1	1	1

R DECODE

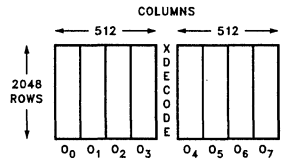
	A_{12}	A_{11}	A_{10}	A_9
R_{00}	0	0	0	0
R_{01}	0	0	0	1
R_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
R_{15}	1	1	1	1

27C210 Die Photograph



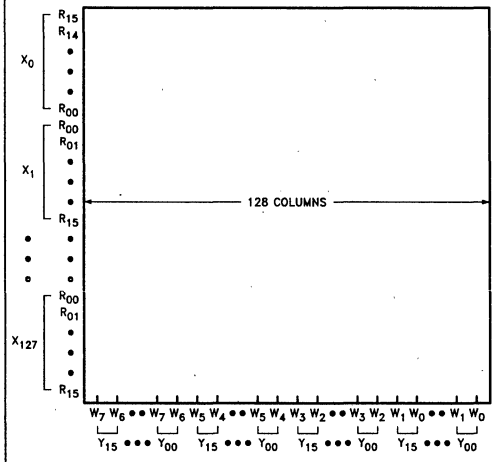
293004-2

27C020 Array Organization and Bitmap



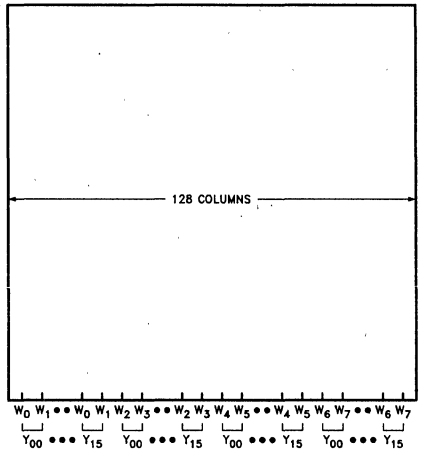
293004-29

OUTPUTS 0 THROUGH 3



293004-13

OUTPUTS 4 THROUGH 7



293004-14

Y DECODE

	A_{10}	A_2	A_1	A_0
Y_{00}	0	0	0	0
Y_{01}	0	0	0	1
Y_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
Y_{15}	1	1	1	1

W DECODE

	A_{14}	A_{15}	A_3
W_0	0	0	0
W_1	0	0	1
W_2	0	1	0
•	•	•	•
•	•	•	•
W_7	1	1	1

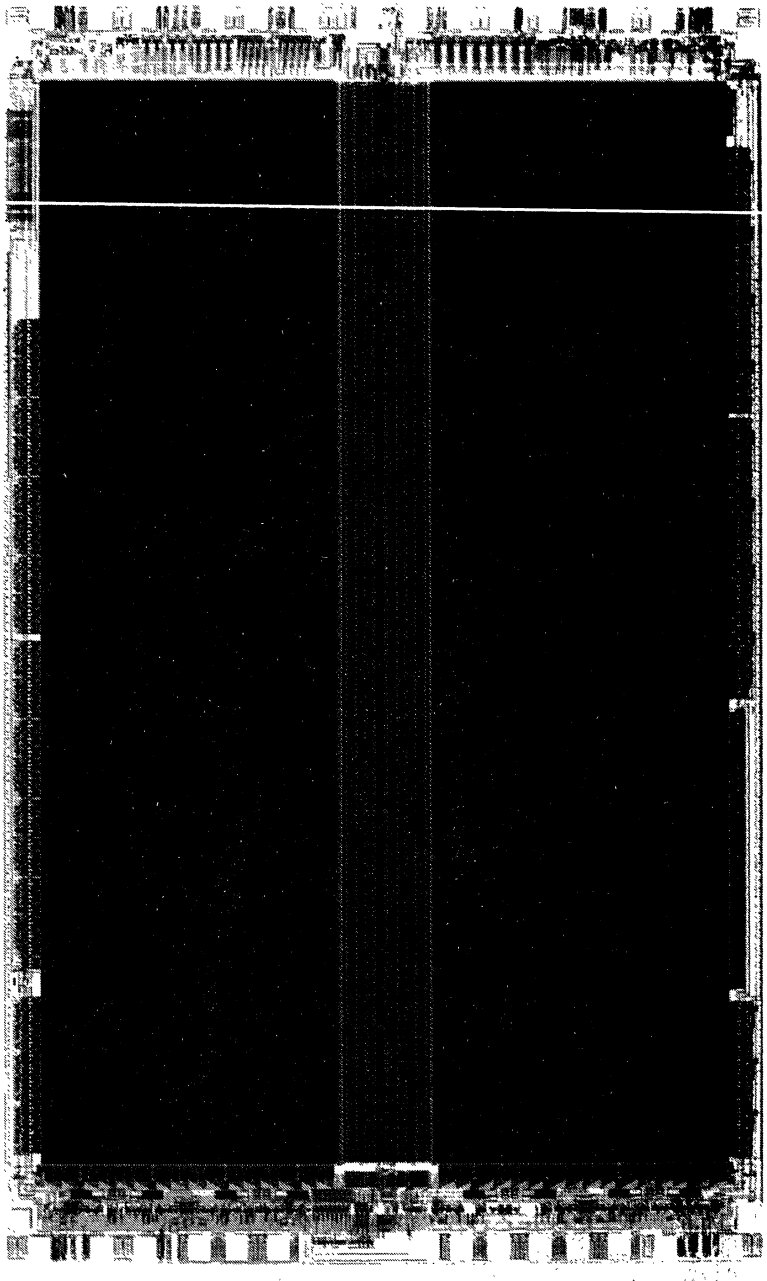
X DECODE

	A_{17}	A_{16}	A_{12}	A_7	A_6	A_5	A_4
X_{00}	0	0	0	0	0	0	0
X_{01}	0	0	0	0	0	0	1
X_{02}	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
X_{127}	1	1	1	1	1	1	1

R DECODE

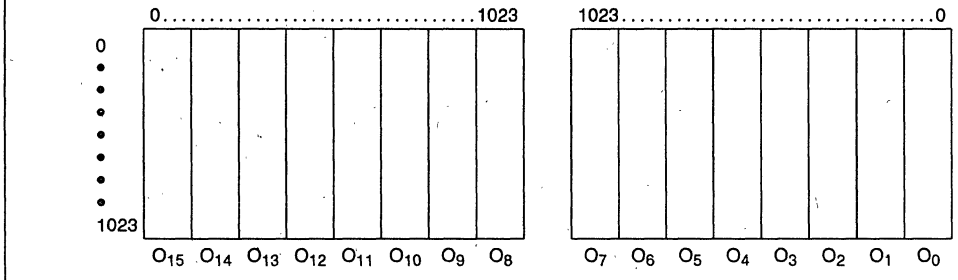
	A_{13}	A_{11}	A_9	A_8
R_{00}	0	0	0	0
R_{01}	0	0	0	1
R_{02}	0	0	1	0
•	•	•	•	•
•	•	•	•	•
R_{15}	1	1	1	1

27C020 Die Photograph



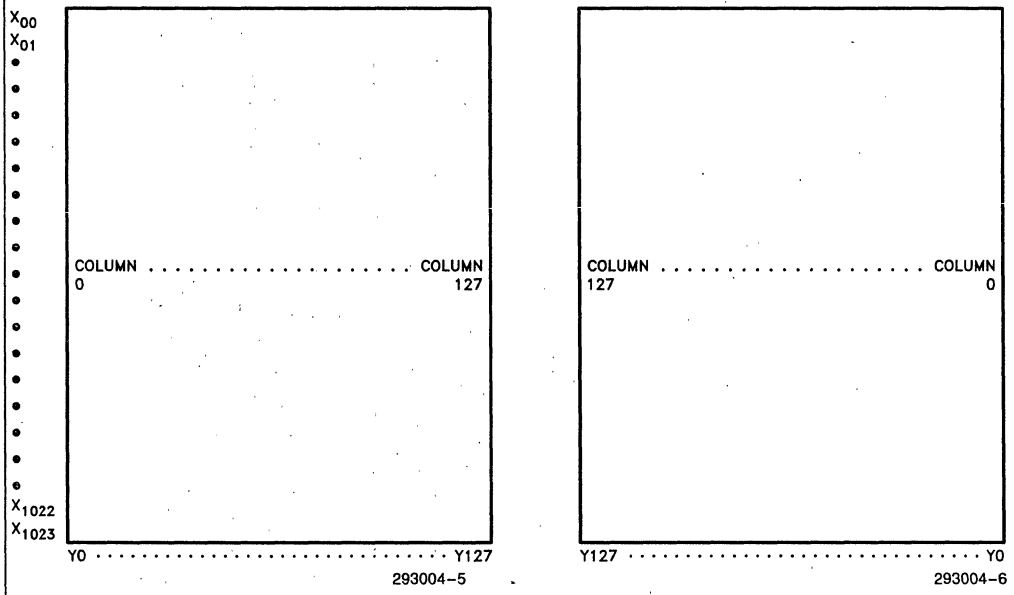
293004-10

27C220 Array Organization and Bitmap



OUTPUTS 15 THROUGH 8

OUTPUTS 7 THROUGH 0



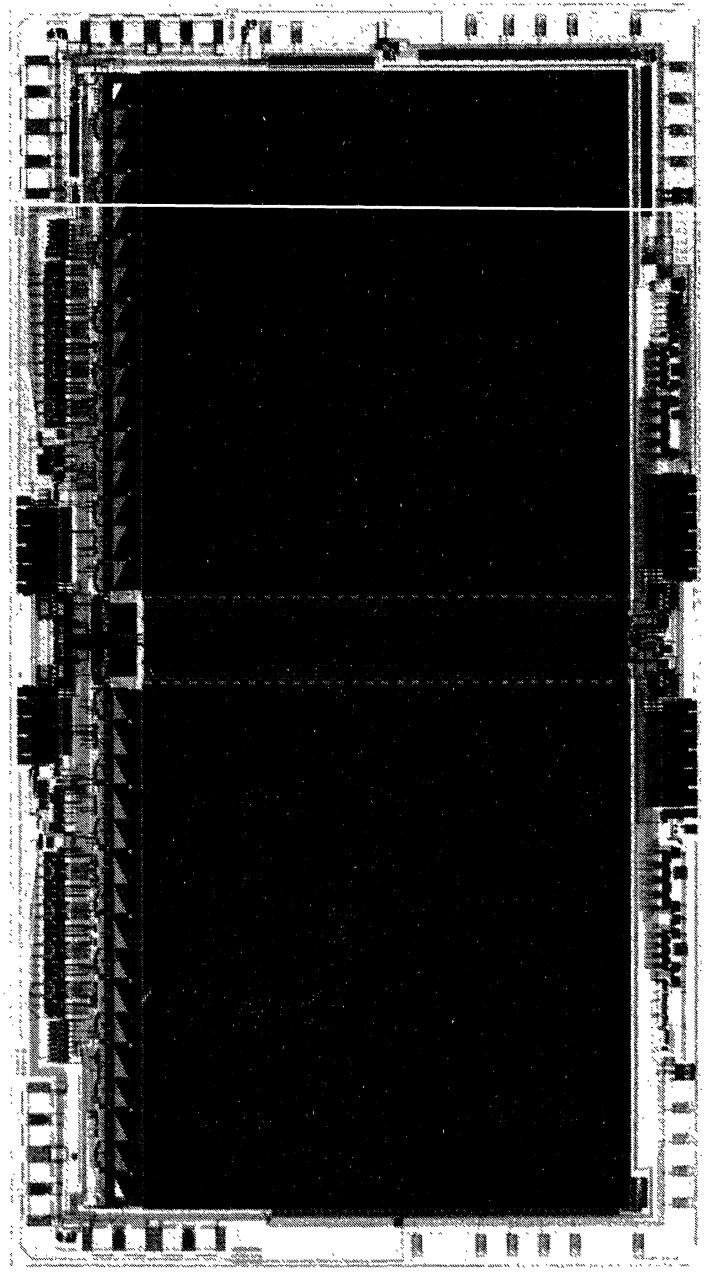
Y DECODE

	A_{16}	A_{15}	A_{14}	A_{13}	A_2	A_1	A_0
Y_{00}	0	0	0	0	0	0	0
Y_{01}	0	0	0	0	0	0	1
Y_{02}	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
Y_{127}	1	1	1	1	1	1	1

X DECODE

	A_{12}	A_{11}	A_6	A_5	A_4	A_3	A_{10}	A_9	A_8	A_7
X_{00}	0	0	0	0	0	0	0	0	0	0
X_{01}	0	0	0	0	0	0	0	0	0	1
X_{02}	0	0	0	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
X_{1023}	1	1	1	1	1	1	1	1	1	1

27C220 Die Photograph



293004-1

Marriage Of CMOS And PLCC Sparking Rapid Change In Mounting Memories

By Alan Hanson

The surge in circuit complexity over the past year or two has pushed the standard DIP size beyond workable dimensions, and rendered it obsolete where high lead count is required.

Meanwhile, the semiconductor industry's shift to CMOS processing for memories, as well as other ICs, is helping usher in the era of surface-mountable packages. Chief among these packages for memories is the plastic-leaded chip carrier (PLCC).

The technology for surface mountables and CMOS processing emerged from shaky beginnings. Although surface-mount packaging has been available for nearly two decades, its potential has just begun to be realized.

Several technical problems hampered its early acceptance: the need for automated factory equipment; prohibitively high packaging costs; and the lack of necessary construction tools.

As of 1984, only 6 percent of all components used in the United States were surface-mount types. Industry analysts predict, however, that with the increase in packaging options, the availability of development tools and the rising demand for surface-mountable devices, more than 25 percent of components will be surface mounted by 1988. And an estimated 128 million of the 600 million PLCCs manufactured in 1988 are expected to be memories.

CMOS has had to fight a similar battle. Prohibitively high cost, inherently low performance (metal gates) and lack of a complete lineup of products necessary to provide low-power system solutions were the chief reasons for CMOS' slow start. But, these problems have now been overcome and the number of products combining CMOS technology and surface-mount packages is accelerating rapidly.

PLCC Inroads

The decision to move from insertion (through-hole) to surface-mount technology is not an easy one. The available options are somewhat confusing:

- Are space constraints a problem?
- Is more functionality required?
- Will surface mounting make a more competitive product?
- Will manufacturing-cost savings be realized?
- Is the proper assembly equipment already available?
- Do components meet JEDEC standards?
- Will socketing be required?

The drive for smaller, more functional and more competitive products is forcing many engineers to scale down existing designs; to strive for VLSI solutions; and to use PLCC packages and other surface-mount packaging options, which can reduce board size dramatically.

Decisions as to which surface-mount option to use are usually based on board-size restrictions. In general, PLCCs minimize the area footprint on a board for lead counts ranging from 28 to 124.

One example of the space-saving ability of a PLCC package is Intel's new 32-lead PLCC package which it is developing for its 64k and 256k CHMOS EPROMS. The PLCC measures 0.45 × 0.55 inch, whereas the 28-pin DIP that would normally be used here measures 1.4 × 0.6 inch. The reduction in area footprint is 70 percent.

The contact area for chip leads can be closer for a PLCC device because the mounting holes mandatory for insertion devices are eliminated. Surface mounting also allows components to be placed and soldered on both sides of a pc board where through-hole mounting is not employed. Depending on the complexity and type of components required in the board layout, a 35- to 60-percent reduction in board size is possible.

To minimize total chip requirements, manufacturers of products such as EPROMs are incorporating an address latch on the address and data pins to allow direct interface with a microcontroller or microprocessor. This eliminates the need for an external latch, as well as reducing board size.

Surface-mount elements can also reduce component weight as much as 75 percent.

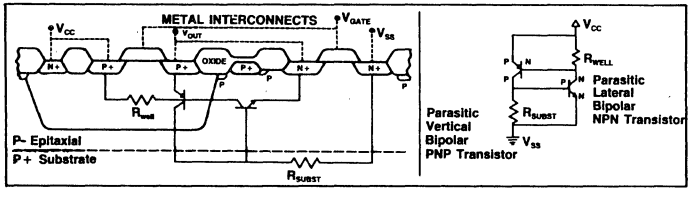
Lightweight PLCC packages tend to be ideal for high-vibration industrial and automotive applications, as well as for portable applications.

Surface mounting requires a substantial investment in capital equipment. New techniques for soldering components to boards (i.e., vapor phase or wave soldering) must be considered and automated machinery such as pick-and-place assemblers must be employed—new pick-and-place machinery employing vacuum pickup has been developed to handle the wide array of different sized packages available for surface mounting.

Today, many different machines are available. Their processing capacity ranges anywhere from 500 to 500,000 devices per hour. (Surface-mounting technology is even used in small-volume, custom facilities, such as for making portable medical equipment, where the devices are manually soldered to boards.)

The benefits of factory-automated assembly are numerous. Less floor space is required. Since raw materials are contained in smaller packages, storage space is diminished. Lighter-weight components reduce shipping and handling expenses. Space-saving benefits can be achieved in the layout of the assembly equipment itself. Some manufacturers have been able to reduce the required factory floor space by as much as 25 percent. Other cost savings include a reduced labor force, the ability to maintain a no-shutdown assembly, improved reliability and reduction of inspection and rework.

These benefits must outweigh, of course, the costs of automating the factory, as well as the cost of restructuring and retraining.



This CMOS EPROM combines both n-channel and p-channel transistors onto a p-type epitaxial substrate to reduce greatly current requirements as compared with an NMOS counterpart.

Electronic Engineering Times — Monday, September 30, 1985

Order Number: 295007-001

When choosing between packaging alternatives, consideration should always be given to industry-wide standardization to avoid unnecessary design mismatching and insure upgradeability. For example, the 32-lead PLCC package was chosen for high-density EPROMs because as much as 512 kbits of address space is easily contained within this package size. Furthermore, PLCC devices with as many as 124 J-type leads have been registered with JEDEC, the standard-setting body for the industry.

A J-type lead extends out of the four sides of a PLCC package and is tucked under the body into small pockets. It was chosen as the industry-standard lead type as opposed to gull wing for several reasons. A minimum-area footprint is best achieved with a J-lead—gull wings extend horizontally out from the body of the package, increasing the required area footprint of the component. Because of their extended leads, gull-wing devices are also at greater risk to damage during assembly or transporting.

J-type leads are also more aptly suited for socketing, which may be particularly important for memory components subject to periodic updates. The J-lead PLCC does, however, have its drawbacks, the most noticeable being the difficulty encountered in inspecting solder joints.

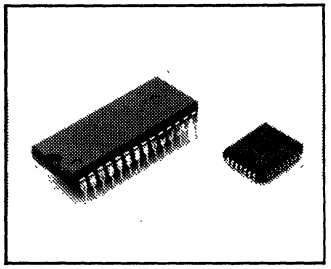
The next step for design engineers who have decided to use PLCC components is to investigate the available process-technology alternatives.

CMOS And PLCC Packaging

Applications ideal for both CMOS parts and PLCC packages lie in low-power portable products in space-constrained environments. Examples can easily be found in the automotive, telecommunication and portable-instrument markets.

Alan Hanson is product marketing engineer, Intel Corp., Folsom, Calif.

CMOS' greatest strength lies in its low-power properties. For example, Intel's 27C64 CHMOS EPROM, which combines both n-channel and p-channel transistors onto a p-type epitaxial substrate, maintains a maximum operating current of 10 mA, standby current of 100 mA and offers 200-ns total access time. Its NMOS counterpart would require six times more active current, 200 times greater standby current and would offer no improvement to total access time.



Both the 28-pin DIP and 32-lead PLCC can hold anywhere from 32k to 512k EPROMs. But, the carrier is roughly a third smaller.

PLCC packages are essential in portable applications because of their space-saving and lightweight features. Minimizing component packaging size, however, achieves little if used in conjunction with bulky power supplies, batteries and cooling devices. Because of its low-power requirements, CMOS helps minimize the need for large power supplies and cooling devices, as well as enhancing PLCC-device reliability.

Because of their reduced package size and plastic construction, PLCCs are poor heat conductors compared with the larger DIP packages. So heat-related breakdowns are more likely—heat dissipation is generally a function of package material, length and construction of leads, package surface area and, of course, the power consumed by the devices.

In improving the overall integrity and reliability of surface-mountable components, methods must be employed to deal with thermal-management problems. The chief way to accomplish this for PLCCs is to reduce the resistance to heat flow from the active junction to the atmosphere.

Thermal resistance ranges from about 40C° per watt for a 68-lead PLCC package to more than 100C° per watt for the 20-lead device. Copper alloy leads, modified substrate materials, and special heat sinks are being used at the package and board levels to maximize heat conduction.

In VLSI applications where increased device functionality is required, thermal management becomes an acute problem. As functionality increases, power demands likewise increase. The resulting higher operating temperatures may result in severe degradation to device operation and performance.

CMOS offers a solution to thermal-management problems. For example, the 27C64, with a maximum operating current of 10 mA, generates 50 mW of heat—a sixth the amount of its NMOS counterpart.

Depending on the particular design and application, special heat-sink designs and/or cooling fans can be reduced or even eliminated with CMOS parts.

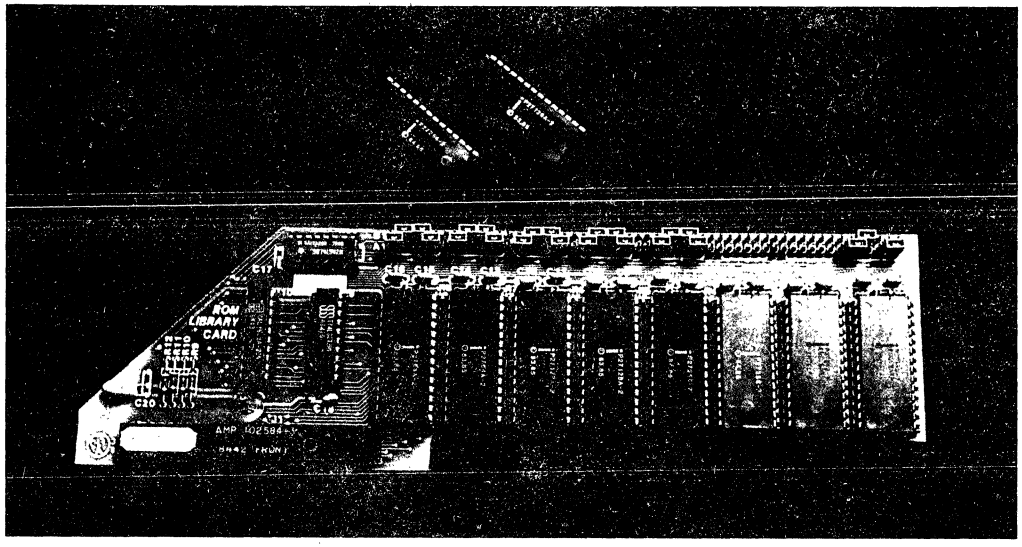
CMOS is particularly valuable in extended-temperature environments, such as automotive engine-control applications where operating temperatures range from −40°C to 80°C and as high as 125°C. In these applications, CMOS may be the only way to provide reliable device operation.

CMOS also brings to a PLCC package wider V_{CC} tolerances and HMOS compatability.

Support tools such as testing, soldering and programming equipment have also become available for CMOS-based surface-mount designs. **EET**

One-Time Programmable EPROMs

Plastic-packaged OTP EPROMs can offer the same performance as their cerdip counterparts, while being more cost-effective.



***1. Eight OTP EPROMs** of varying densities stuffed in this EPROM library board store bootstrap code, the microprocessor instruction set, and EPROM programming algorithms.*

By Richard Immekus and Richard Foehringer, Memory Components Div., Intel Corp., Folsom, Calif.

Ultraviolet EPROMs (erasable, programmable read-only memory), introduced in the early 1970s, have encountered phenomenal acceptance in the marketplace in the past few years. Annual usage is measured today in the hundreds of millions of units.

Where once EPROMs were used primarily in R&D environments and preproduction phases of a new product, today they are found in a multitude of mass-produced products ranging from telephones and video games to automobiles and home computers. The penetration into markets once dominated by masked ROMs is both due to their inherent flexibility of EPROMs (they can be programmed at a moment's notice) and the rapid convergence of EPROM and ROM prices over the last few years.

OTPs and test

A type of device known as "one-time programmable" (OTP) EPROMs offers the same performance as its cerdip counterpart, yet is inherently more cost-effective. In addition, these plastic production EPROMs can now be programmed nearly 100 times faster than cerdips. This dramatically reduces throughput time and paves the way for cost-effective, automated on-line programming.

Although most memory products (ROMs, DRAMs, SRAMs, etc.) have been available in plastic for years, this has not been the case with EPROMs. The essential characteristic of these devices, i.e., their UV-erasibility, made packaging them in plastic extremely difficult. Some early attempts were made by various manufacturers to produce plastic parts that incorporate a "window," similar to cerdip parts. These windows, however, tended to fall out or leak during steam and moisture testing and never proved reliable.

Without the window, the UV-erasability feature of an EPROM is lost and a major barrier to manufacturing OTP parts is erected. To be useful to the customer, EPROMs must be received in a blank state, yet still be tested during the manufacturing pro-

Order Number: 295016-001

cess to verify that they comply to published specifications and that each cell can in fact be programmed. Thus, verification entails programming, testing, and erasure. Intel has succeeded in refining its testing methodology to the point that each die is individually and thoroughly tested at the wafer level; the wafer is then UV-erased. In addition, proprietary innovative test modes have been incorporated into the EPROM design to allow performance testing at the post-packaging level. The result is that the customer receives fully tested OTP parts with the same guaranteed performance and programmability found on cerdip EPROMs.

Because plastic-packaged parts are non-hermetic, moisture resistance is always a concern to reliability engineers. In the semiconductor industry, nitride is very commonly used as a passivation layer and moisture barrier on ICs. With EPROMs, however, standard nitride passivation is not acceptable due to its non-UV-transmissive composition. In addition, EPROMs have a special sensitivity to moisture not found in any other state-of-the-art NMOS product.

Due to the nature of the storage cell in an EPROM structure, data is maintained in a non-volatile state via charges trapped on a phosphorus-doped floating polysilicon gate. Entry of moisture is due to passivation defects or passivation process marginalities and causes oxide damage, thereby creating a leakage path for the charge cell. Such occurrences can readily be induced via steam "pressure cooker" testing or extended 85°C, 85 percent RH exposure, and are manifested as charge-loss failures.

In order to provide OTP parts that can withstand the effects of moisture and steam — i.e., exhibit no evidence of corrosion or charge loss and still be erased properly when exposed to UV light — Intel developed a proprietary multilayer passivation process. The resulting protective layers were the last missing element in a systems solution to providing cost-effective production EPROMs.

Qualification

Every engineer knows that the transition from lab-condition product design to mass production in a high-volume manufacturing environment is difficult at best. To minimize risks and ensure reproduceability, Intel takes each new product through a rigorous qualification procedure (see table) in which exhaustive tests, both destructive and non-destructive, are performed for both electrical and mechanical testing. Substantial amounts of electrical data are collected and scrutinized, and failures are analyzed to the last detail.

To ensure the quality and reliability of its products, Intel follows a "zero defects" program. Reliability monitors (Fig. 2) and lot-quality inspection sampling are carried out on each and every manufacturing lot. Electrical and visual inspection is performed to a 0.1 percent acceptable quality level (AQL).

Not only is outgoing quality sampled and verified, but programmability, infant mortality and long-term reliability are monitored on a weekly basis. These tests are conducted on finished products and, since OTPs are non-erasable, all devices used for quality and reliability monitors must be scrapped.

The results of electrical testing carried out to date show that OTP EPROMs are as reliable as cerdip EPROMs. Using data from qualification and process monitor tests, the calculated low failure rates of OTPs (less than 0.02 percent per 1,000 device hours) match those of their cerdip counterparts.

In addition, moisture resistance is exceptionally high for these plastic OTP parts. A survey of major customers regarding needs for moisture performance has revealed that a percentage defect allowable (PDA) of 3 to 5 percent is required. Intel's in-house qualification procedures generally require plastic packaged parts to withstand 96 hours of steam and 1,000 hours of 85°C, 85 percent RH. This specification equals or exceeds that of Intel's major customers.

Many people today assume that because cerdip packages are hermetic, they are inherently more reliable and better suited to production than plastic units. This was true years ago, but with the advent of automated assembly lines, and particularly autoinsertion equipment, a problem with cerdip usage began to emerge. It was found that cerdip packages occasionally chip or crack if not handled properly. Plastic packaged components, however, do not experience this deficiency.

Today, plastic EPROMs are prevalent in most computers, video games, modems, printers, electronic typewriters, and other products. The increasing demand for highly automated assembly lines and production flow demanded by these items will lead to increasing use of plastic packaged components at the expense of cerdip packages.

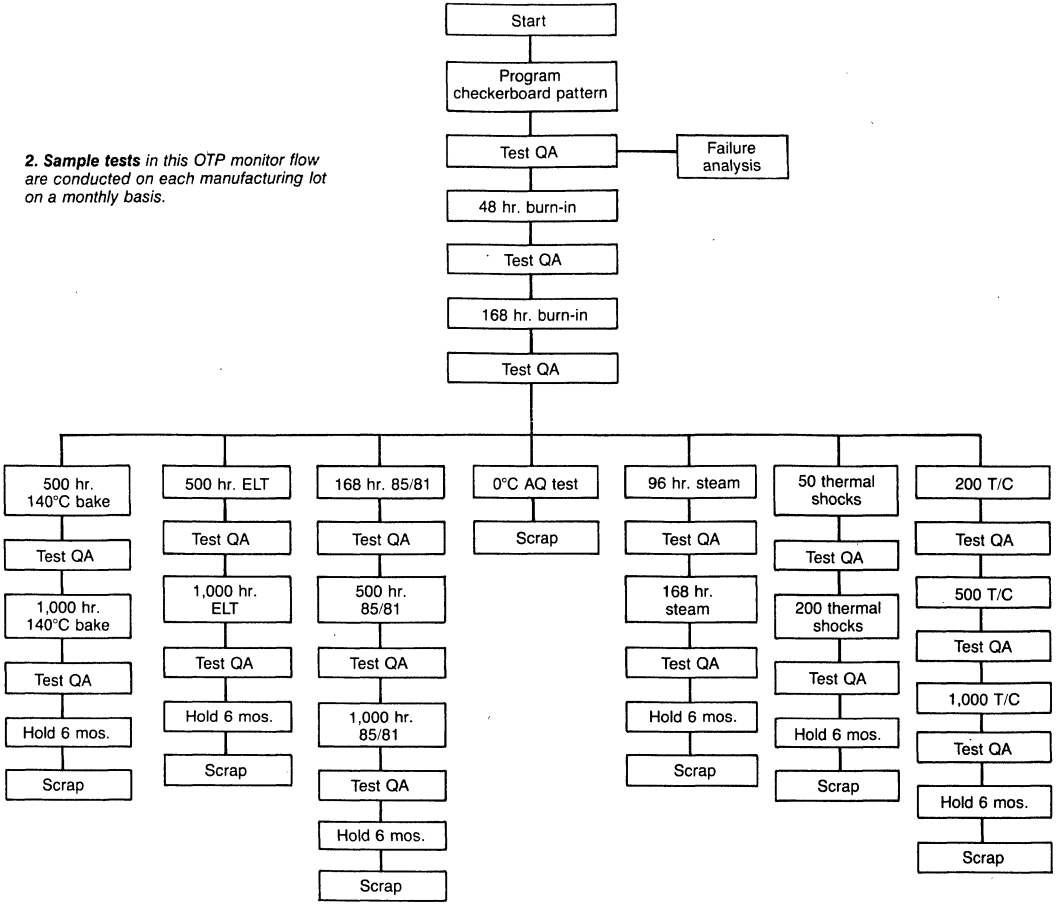
Fast programming issues

Earlier it was stated that OTP production EPROMs can be programmed almost two orders of magnitude faster

OTP qualification process

Test	Conditions
Programmability	All voltage corners
Speed performance	0°C, 25°C, 70°C (equivalent)
Theta JA by device type	Thermal impedance of the package
Burn-in	48-hr/168-hr 125°C dynamic burn-in
Elevated temperature life test	500-hr/1,000-hr 125°C dynamic life test
High-voltage ELT	168-hr/125°C high-voltage ELT (6.5 V)
Data retention bake	1,000-hr/140°C static data retention bake
Steam	96-hr/168-hr 121°C 30 psi steam
85/85	1,000-hr 85°C/85% relative humidity
Test*	**Description/methodology**
Temperature cycle	Mil std 883, method 1010C
Thermal shock	Mil std 883, method 1011C
Centrifuge	Mil std 883, method 2001
Bond pull	Mil std 883, method 2011
Die shear	Mil std 883, method 2019
Lead fatigue	Mil std 883, method 2004
Solderability	In-house, 2-hr 170°C, 1-hr steam

*Tests conducted to determine the mechanical worthiness of Intel's 28-pin OTP package.



***2. Sample tests** in this OTP monitor flow are conducted on each manufacturing lot on a monthly basis.*

than cerdip equivalents. When one considers that most 256K EPROMs generally program in four to six minutes and that an OTP such as the P27256 can be programmed in less than four seconds, one begins to realize the magnitude of the time savings and increased throughput potentially available to the user with OTPs, without a corresponding compromising of device reliability.

A new approach, designated by Intel as the Quick-Pulse Programming algorithm, permits these faster programming speeds through the use of much shorter pulses than required by previous programming algorithms. For example, Intel's earlier Intelligent programming algorithm, which is still required for cerdip parts, uses a one millisecond pulse and an overpulse scheme. By contrast, the Quick-Pulse Programming algorithm usually needs only a short 0.1 millisecond pulse with no overpulse. Increased Vpp latch-up protection is designed into these new OTP devices, and when V_{pp} and V_{cc} are raised program cell margin increases. ■

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ELECTRONIC COMPONENT NEWS
TECHNOLOGICAL HORIZONS

OTP EPROMs with Quick-Pulse Programming™ offer ideal mass production firmware storage

V. Siva Kumar
Product Marketing Engineer
Intel Corporation

In today's manufacturing environment – where production flexibility, just-in-time inventory management, and, above all, quick throughput are needed – EPROMs have established themselves as the solution for cost-effective firmware production. Intel Corporation, having invented the EPROM in the seventies, has continued to pioneer advances that have made EPROMs the choice over masked ROMs as high-volume firmware carriers. Intel's one-time programmable (OTP) plastic-packaged EPROMs, that can be programmed in a few seconds using the new Quick-Pulse Programming™ algorithm, will supplant both CERDIP EPROMs and masked ROMs in this firmware storage task.

These plastic-packaged production EPROMs, currently available in densities up to 256 kilobits, are the world's first EPROMs that are programmable using the new Quick-Pulse Programming algorithm. This programming algorithm achieves up to two orders of magnitude reduction in programming time compared to existing programming algorithms. Volume usage of high density EPROMs is now more cost-effective than ever through the use of OTP plastic packaged EPROMs with programming techniques employing this algorithm.

To high-volume users of EPROMs, programming time is a large component of throughput time. As EPROM density has continued to treadmill toward the megabit level, programming times have become a major concern to system manufacturers. Even the industry standard Inteligent™ algorithm consumes a sizable amount of time in programming mature densities. Therefore, if high-density EPROMs are to serve the manufacturing requirement of quick throughput, programming times must be reduced. Innovation yielded the answer to this problem in the form of Intel's new Quick-Pulse Programming algorithm.

EPROM programming time evolution

Until the advent of Intel's Inteligent Programming algorithm in 1983, EPROM programming was done using a nominal 50-millisecond programming pulse per EPROM byte, a method that required about 1.5 minutes to program a 16 kilobit EPROM. If that same programming technique were employed for higher EPROM densities such as the 256-kilobit, as many as 24 minutes would be required to program the device. The Inteligent algorithm therefore was devised to improve programming throughput for the higher densities available at that time – namely the 64-kilobit and 128-kilobit EPROMs.

The Inteligent Programming algorithm was the first algorithm to exploit the fact that only a few EPROM cells required 50-millisecond pulses to program while a majority of the cells were successfully programmed with substantially shorter pulses.

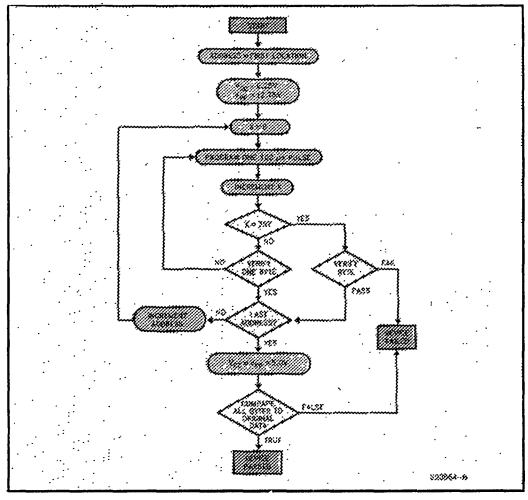

Fig. 1 – Quick-Pulse Programming Flowchart

This algorithm employed a closed-loop technique of margin checking. Nevertheless, this programming technique still required pulse widths in the millisecond range with mandatory overpulses. Hence, the Inteligent algorithm takes several minutes to program the highest density EPROMs available today (265 and 512 kilobits).

Thus, the stage was set for a breakthrough in programming algorithm development. The objectives were simple: (1) ensure the shortest possible programming time with the present technology and (2) maintain the programmability and data retention characteristics of the earlier algorithms. The Quick-Pulse Programming algorithm satisfies these objectives.

Quick-Pulse Programming algorithm

For the first time, advances in EPROM design and process technology allow the use of short programming pulses of only 100 microseconds.

The Quick-Pulse Programming algorithm takes advantage of tighter programming voltage tolerances in conjunction with the increased V_{PP} latch-up protection designed into Intel EPROMs. This latch-up protection allows V_{PP} and V_{CC} to be raised above the levels previously employed for programming, thus providing for greater program cell margins. The algorithm is made possible because of the improved HMOS II-E EPROM cell characteristics, carefully controlled cell profiles, oxide thickness and quality and channel length controls (see "Quick-Pulse – a Technical Explanation").

The flow chart of the Quick-Pulse Programming algorithm is shown in Fig. 1. One can immediately see that the algorithm is inherently similar to the earlier Inteligent Programming algorithm in that it benefits from the different characteristics of individual EPROM bits. Different cells require a varying number of programming pulses, and an iterative closed-loop scheme allows flexibility in employing just the right number of pulses required by each cell.

The programming of an EPROM using the Quick-Pulse Programming algorithm is done as follows. The programming voltage V_{PP} should be set at 12.75 V with V_{CC} set to 6.25 V (higher than the 5V V_{CC} used during normal operation). Iterative programming pulses of 100 microseconds are then applied. After each pulse, the algorithm checks the EPROM output to verify the desired programmed value. If the output is incorrect, the algorithm repeats the pulse-and-check operation. If after 25 such iterations the output of that byte still does not verify correctly, the device failed programming and is rejected. If the byte verifies accurately within 25 pulses, programming of that byte has been accomplished and the next byte is similarly treated. Data gathered from the programming characterization of the Intel EPROM cell shows that over 99 percent of the cells only require one programming pulse. After all the bytes are programmed, there is a final verification operation that compares all the programmed bytes to the original.

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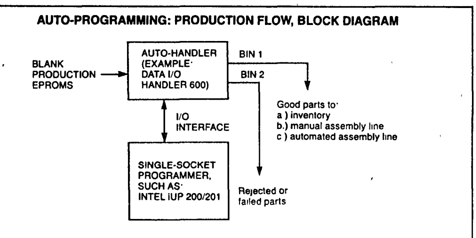
TECHNOLOGICAL HORIZONS



Using the Quick-Pulse Programming algorithm, the 256-kilobit EPROM can be programmed in a theoretical minimum time of 3.3 seconds compared to about four to six minutes required if the Inteligent algorithm were used. This fast programming time is achievable when the overhead associated with the programming equipment is minimized. The term "overhead" refers to the time required by the EPROM programming equipment to perform some operations needed to program an EPROM. Some of these operations are (a) verifying that the EPROM is inserted into the socket in the correct orientation, (b) reading the EPROM device identifier and manufacturer's code, (c) selecting the appropriate programming voltages, and (d) checking to see if the EPROM is in an unprogrammed state.

Most programmers currently available in the market are based on older and slower microprocessor designs and consequently have large programming overhead. However, newer programmer designs anticipated in the near future will utilize more efficient microprocessors, such as the Intel 80186 or 80188, and should therefore have substantially reduced overhead. The Quick-Pulse Programming algorithm, when used in conjunction with low programming overhead, achieves programming times close to the theoretical minimum, yielding a major improvement over the Inteligent Programming algorithm. Many manufacturers using large volumes of EPROMs design their own programmers or employ "on-board" programming (in-circuit programming of EPROMs). This new programming algorithm will allow these manufacturers to obtain the benefits of the reduced programming time. Table 1 shows the comparison of the programming times possible with the Quick-Pulse Programming algorithm on programmers available today as well as the theoretical minimum programming time with no programmer overhead.

PROGRAMMING TIMES

	2764A	27128A	27256
With Data I/O Model 120/121 (Firmware version V10):			
Current algorithm	62 sec.	124 sec.	272 sec.
Quick-Pulse	16 sec.	32 sec.	68 sec.
Improvement	3.9×	3.9×	4×
With Intel Fast 27/K*			
Current algorithm	41 sec.	80 sec.	158 sec.
Quick-Pulse	10 sec.	14 sec.	35 sec.
Theoretical limit with no overhead on programmer			
	0.9 sec.	1.7 sec.	3.3 sec.

Table 1

Comparison: Quick-Pulse Programming vs. Inteligent Programming

The two main reasons that the Quick-Pulse Programming algorithm achieves its speed are the extremely short programming pulses and the elimination of the over-programming pulses.

The Inteligent Programming algorithm needed longer pulses of 1 millisecond for programming. However, the use of a higher V_{PP} programming voltage in the Quick-pulse algorithm (12.75 V compared to 12.5 V) increases efficiency (due to higher drain voltage) and maximum margin (due to higher gate voltages). This reduces the need for longer pulses and allows the new algorithm to employ pulses of 100 microseconds.

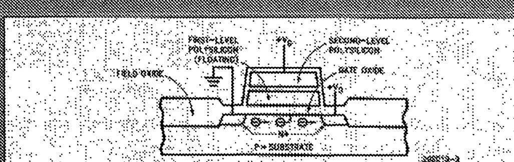
The Inteligent Programming algorithm utilizes a 3× over-program pulse at the end of each byte verification to ensure programming margin. This means that even when a cell takes only one 1-millisecond pulse to program, the over-programming caused the cell programming time to be 4 milliseconds; if the cell takes 2 milliseconds to program, the total time increases to 8 milliseconds. Thus, if the cell needed the maximum of 25 pulses to program, the total time consumed for program pulses and overprogram pulse would add up to 100 milliseconds.

The Quick-Pulse Programming algorithm does not need the over-programming pulse to ensure adequate programming margins. The use of a higher V_{CC} is a more direct means of achieving the same result.

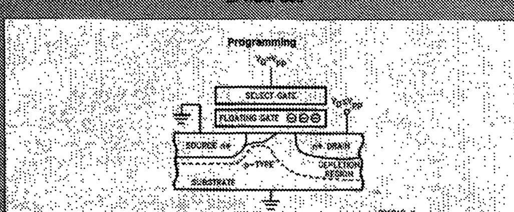
Thus, other than the reduction in the pulse width and the elimination of the over-programming pulse, the Quick-Pulse Programming algorithm resembles the Inteligent Programming algorithm, with both V_{CC} and V_{PP} programming voltages increased by 0.25 V. Table 2 shows the comparison of the two algorithms.

(cont. on next page)

Quick-Pulse — a technical explanation



EPROM Cell



Programs Via Hot Electron Injection from Drain Depletion Region

Quick-Pulse Programming has been made possible through improved cell characteristics, carefully controlled cell profiles, oxide thickness quality, and channel length controls.

Intel's HMOS II-E process uses a second level bipolar latch-up programming phenomenon, which occurs when an N-channel MOS device acts like an NPN bipolar transistor. The source of the substrate junction becomes forward biased due to a high level of impact ionization currents being formed during normal MOS operation. This secondary current acts as base drive for the NPN like structure which has formed.

This second level condition causes the drain current to increase significantly over normal available MOS levels of current. This drain reaction event is controlled through a depletion device configured in the form of a constant current source, effectively acting as a current limiter for the phenomenon. The end result of this process is that with injection efficiency being the same, the increased drain current, due to the second level programming causes increased program current to the floating gate. The result to the user is directly reflected in greatly reduced programming time.

Intel's capability to mass produce HMOS II-E lies in the tight process control of the cell profile, dropping levels of channel length, channel depth and oxide thickness.

COMPARISON: QUICK-PULSE VS. INTELIGENT PROGRAMMING

	Quick-Pulse	Inteligent
Pulse width	0.1 msec.	1 msec.
Max. # of pulses	25	25
Over-prog. pulses	no	yes (3× msec.)
V_{PP}	12.5–13.0 V	12.0–13.0 V
V_{CC} (programming)	6.0–6.5 V	5.75–6.25 V

Table 2

Programmability and data retention test results for the Intel P2764A and P27256 EPROMs are as follows for 168-hour burn-in: P2764A 1700 tested/0 failed; 7685 tested/0 failed. The test results show that the Quick-Pulse Programming algorithm does not compromise reliability and quality to achieve programming speed. Extensive characterization and reliability data were accrued to validate the algorithm.

OTP & Quick-Pulse Programming: cost-effective combination

The EPROMs currently qualified to be programmed using the Quick-Pulse Programming algorithm are Intel's production EPROMs, the P2764A, the P27128A and the P27256, which are plastic-packaged OTP (one-time programmable) versions of the 64-, 128-, and 256-kilobit EPROMs respectively. The P27512 and the P27513, the plastic-packaged 512-kilobit EPROMs, as well as upcoming plastic leaded chip carrier (PLCC)-packaged EPROMs, will also be qualified on this new algorithm.

Intel's OTP production EPROMs have qualities that are well suited for high-volume firmware manufacturing environments. It is in such high-volume manufacture that the benefits of reducing the programming time per device are magnified into large gains in productivity through reduced throughput. Thus the combination of production EPROMs with the Quick-Pulse Programming algorithm offers a significant advantage to large-scale firmware producers.

The reduction in programming times for the mature densities with the Quick-Pulse algorithm is significant. The savings in programming time translates directly into savings in programming costs, and, of course, the cost savings increase as the number of programmed parts increases.

Programming combines with auto-handling of OTPs

The high-reliability plastic package of the OTP EPROM has several unique advantages over the CERDIP package that make it highly suited for completely automated manufacture. The plastic package is extremely rugged and will not chip or crack in tube-to-tube auto-handling unlike the brittle ceramic package. The CERDIP package also may not have its base and lid aligned in exactly the same orientation, which also causes breakages when machine handled. The plastic packages are molded in one single piece with no separate lid or base and consequently have no alignment-related auto-handling losses.

Modern production technology is increasingly focusing towards complete automation as the means of improving quality and reliability and reducing manufacturing costs. With full automation as the goal, the advent of the Quick-Pulse Programming algorithm coupled with the OTP allows for the first time for the programming process to be incorporated in the manufacturing flow. Using automatic handlers that are available today, one can completely process the P2764A (64-kilobit OTP), including the programming step in less than two seconds. The OTP 256-kilobit EPROM only takes four or five seconds to be programmed and assembled on the system.

OTPs make ROMs obsolete

OTP plastic EPROMs have a major advantage to traditional ROM users and that is greater flexibility. In the fiercely competitive environment of today, quick time to market with the right product that meets the customers' changing needs is of the utmost importance. Maintaining an inventory of unprogrammed OTPs saves the firm from having to store many line items of masked ROMs. The simplicity and speed of programming an OTP allows for quick changes of software without any increased overhead and management costs. With changing requirements, ROM code obsolescence is a major cost increase factor that can again be eliminated with OTPs.

For further information, ask for Lit. # W-361, Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052-8065.

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Keeping data safe with nonvolatile memory

The author sorts out the myriad nonvolatile memory options available, including ROMs, PROMs, EPROMs, E²PROMs, NVRAMs, plus others.

Terry Kendall
Technical Marketing Engineer
Memory Components Div.
Intel Corporation
Folsom, CA

Nonvolatile memory (NVM) devices have one primary characteristic—they don't "forget" when power is removed. Without them, no computerized system can wake itself or begin operation.

NVMs come in many forms. Some, such as masked ROMs (read-only memories), have data "manufactured" into them. Others, ranging from PROMs to bubble memories, are user-programmable. PROMs and EPROMs are read-only memories while E²PROMs, NVRAMs, and battery-backed static RAMs provide in-system read and write capability. In harsh environments where disk storage won't function, bubble memory provides compact, highly reliable read/write mass memory.

This article looks at the NVMs currently available, explains their important characteristics, and gives some pointers on choosing the best type for your application.

ROMs

Masked ROMs (Fig. 1) are used in applications that have stable code and that require an NVM featuring a long life cycle. Firmware is written and debugged by the OEM, then submitted to the ROM manufacturer.

ROMs are typically manufactured using NMOS (N-channel metal oxide semiconductor) technology. A generic transistor array is custom-programmed during one of the final process steps.

Because the cost of programming (or masking) a custom ROM is high, these NVMs are used mostly in high volume applications, where costs can be amortized over a large quantity of units. One drawback: If ROM firmware has even one error or an upgrade is required, entire stocks of programmed ROMs must be discarded and replaced.

PROMs

Bipolar PROMs (programmable ROMs, Fig. 2) were one of the first user-programmable memories developed. PROMs use a fusible link to store data. They're supplied by the manufacturer with all fuses intact; *blowing* the appropriate fuses programs the devices.

While very fast, bipolar PROMs are also power-hungry. The relatively small memory in each package (32 to 2K bytes) leads to higher system chip count, increasing system size and power consumption. However, when computational speed is a primary objective, access times as fast as 25 ns make bipolar PROMs obvious contenders.

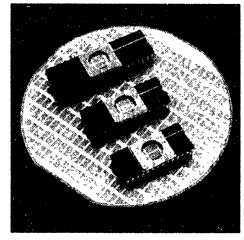
EPROMs

EPROMs (ultraviolet erasable programmable ROMs) can be purged of data and reprogrammed. They use a data storage technique different from ROMs and PROMs. Rather than mechanical connections (metal lines or blown fuse-links), data is represented by altering an internal storage transistor's threshold (turn-on) voltage. Exposing the EPROM to ultraviolet light erases it.

EPROMs have taken the lead in high-density NVM flexibility. Word-wide (16 bits) EPROMs and single-chip densities from 16K to 64K words are available now,and up to 512K words will be available in the future. To accommodate the limited address range of 8-bit microcontrollers and microprocessors, byte-wide page-addressed EPROMs and ROMs pack 64K or 128K bytes (up to 4 million bytes in the future) into a single 16K-byte address space. Multiple transistor cell techniques are yielding high-speed EPROMs with access times rivaling bipolar PROMs.

EPROMS are ideal for system prototyping. Less expensive plastic OTP (one time programmable) EPROMs can be used when systems go into production.

When power consumption is a primary consideration, CMOS ROMs and EPROMs are available. In addition, CMOS



These EPROMs are the highest-density units available—each can store one million bits.

I&CS September, 1987

Order Number: 295029-001

has speed and current drive capabilities superior to NMOS. Standard CMOS memories have access times as fast as 100 ns, and output current-source capabilities of 2.5 mA.

E²PROMs

E²PROMs (electrically erasable and programmable ROMs, Fig. 3)—sometimes called EEPROMs or EAROMs—are cousins of EPROMs and functionally identical in read mode. E²PROMs, however, have a significant advantage over EPROMs—they can be erased and reprogrammed in-circuit, a byte at a time. E²PROMs contain on-chip circuitry that makes them pin-compatible with static RAMs and EPROMs. Simply writing new data to the E²PROM, like writing to RAM, will change data.

An E²PROM requires about 5 ms to perform an auto-erase/store operation, substantially slower than a typical RAM write. But E²PROMs have the capability to store up to sixteen bytes simultaneously in 5 ms, or about 312 µs per byte. This cycle time per byte is compatible to normal memory write cycles. E²PROMs have a minimum erase-store endurance of 10,000 cycles, and undisturbed data will remain valid for at least 10 years.

NVRAMs

NVRAM (nonvolatile random access memory, Fig. 4) takes flexibility and reprogrammability one step further. It consists of two parallel memory planes. The foreground memory is static RAM, and each RAM bit is backed up by an E²PROM storage cell. Read and write operations deal only with RAM, at RAM speeds. On power-up, or when commanded, E²PROM data is transferred to RAM. When system power is lost, power-fail circuitry transfers RAM data to E²PROM. Built-in protective circuitry prevents spurious writes of unstable data during power fluctuations.

NVRAM comes in 128- to 512-byte packages, enough for most critical storage applications. It is used for secure storage of small amounts (128 to 512 bytes) of frequently altered data, such as system parameters, current operating status, data stack, and scratch-pad information.

NVRAMs have a 10,000 cycle-per-byte minimum store endurance and at least 10 year data retention.

Battery-backed static RAMs

The most convenient alterable memory is static RAM. To make static RAM nonvolatile, a battery is added, either packaged with the RAM chip or on the circuit board. To prevent discharge, it is isolated from other board devices and powers the RAM only when system power is removed. During normal operation, the system's supply powers the RAM and can trickle-charge rechargeable batteries.

Battery-backed RAM requires special circuitry to inhibit chip select and write signals during power transitions.

Battery-backed RAM does have some limitations: batteries have limited life spans and are sensitive to temperature fluctuations. Nonrechargeable batteries used in battery-backed RAM can last from several months to 10 years. But rechargeable batteries do develop *discharge memory*. Periodic equipment maintenance programs should include data back-up and battery replacement.

Bubble memories

Magnetic bubble memory is a form of nonvolatile mass memory that relies on magnetic domains in a thin magnetic film on a gallium gadolinium garnet substrate. External permanent magnets induce a bias field that shrinks the film's magnetic domains into cylindrical bubbles. Data is written to the memory by creating or destroying bubbles.

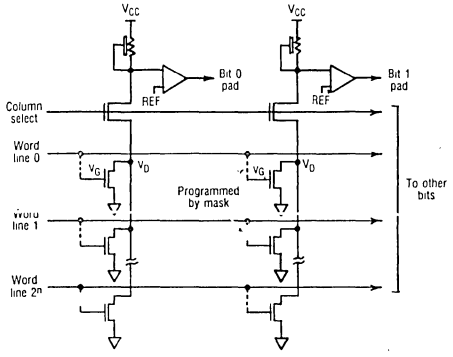


Fig. 1: A masked ROM is programmed by the manufacturer in the final metalization step. Individual transistors are connected or disconnected to encode 1s and 0s.

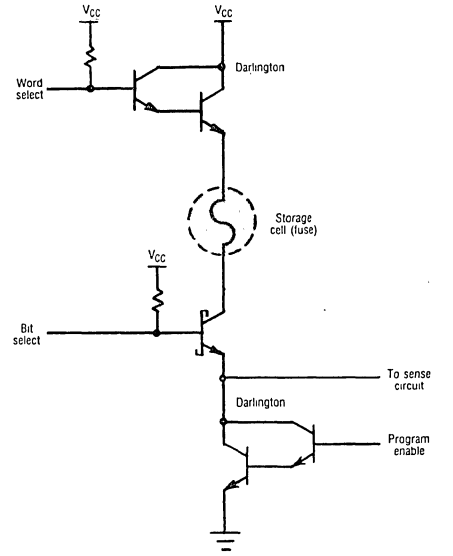


Fig. 2: A single storage cell in a bipolar PROM is user-programmed by blowing an internal fuse.

Wire coils surrounding the substrate produce a rotating magnetic field that moves bubbles along data loops. A maze of magnetic chevrons on the thin film forms memory cells that separate and guide bubbles as they move. During read operations, sensors detect bubbles as they pass.

While relatively expensive, bubble memory is the only choice when nonvolatile mass storage is required in harsh environments, space-constrained systems, or systems that cannot tolerate disk crashes. One- and 4-megabit bubble memory packages can be combined to form complete disk drive emulators. Ready-to-install PC compatible expansion cards are also available.

Typical densities

A few years ago, 4K bytes of nonvolatile memory and small quantities (128 bytes) of RAM were sufficient for

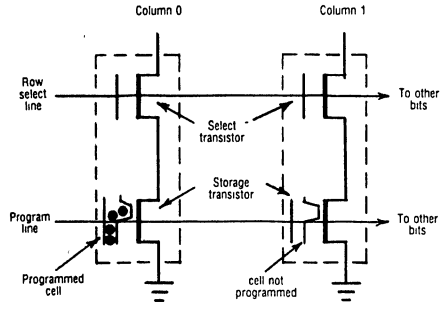


Fig. 3: An E²PROM memory cell is programmed by trapping charge in the gate structure of a transistor. The charge can be electrically removed.

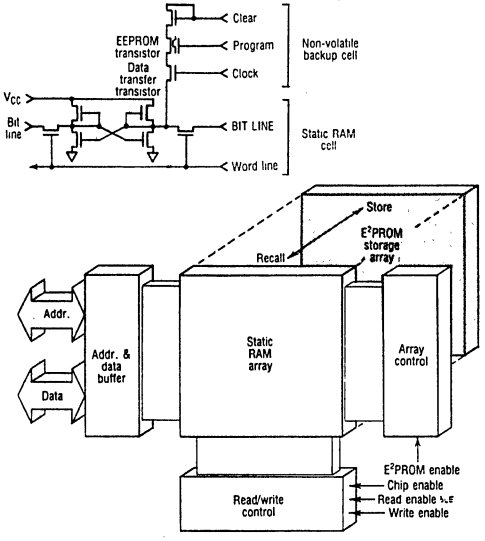


Fig. 4: An NVRAM contains both a standard RAM and an E²PROM; data is written into the RAM during system operation, then stored in the E²PROM on power-down. When power is restored, the data is loaded from E²PROM to RAM.

most control applications. A single chip could contain the microcontroller and this small memory. Today it is not unusual to find controllers connected to 8K or even 64K byte NVM arrays. In fact, some applications use 16-bit processors not for their power but for additional address lines.

Nonvolatile memories come in densities-per-package that range from 128 bytes to as much as 512K bytes. ROMs and EPROMs have the highest densities. Both can accommodate densities up to 1 megabit (131,072 bytes). NVRAMs, PROMs, and E²PROMs have lower densities;their applications, however, are usually less memory intensive.

Comparing the alternatives

Each nonvolatile memory type fits specific application needs depending on its particular characteristics and limitations. Memory-related variables include unit quantity (present and future), application, software and hardware overhead, data security, available board space, package style, and programming ease. Manufacturing-related variables include production quantities, upgrade frequency, inventory logistics, service needs, code stability, and cost. Further, the particular application will determine the proportion of read-only and alterable memory amounts required. General purpose computers may require less than 1% of the total memory to be nonvolatile. In control systems, however, NVM may comprise over 98% of total memory—mostly ROM or EPROM with E²PROM, NVRAM, and RAM in lesser amounts. Keep in mind that device cost is only part of a nonvolatile memory's cost effectiveness.

Weighing NVM costs

Device costs are directly related to die size and manufacturing technology. Simple devices, such as ROMs, EPROMs, and E²PROMs, have very low cost-per-bit. More complex memories—NVRAM, RAM, and bubbles—have fewer bits per die area and more complicated manufacturing processes. These memories have much higher per-bit costs.

Per-bit costs should not be confused with cost effectiveness, however, since other factors enter into the equation. ROMs are the lowest cost-per-bit memories, but only for high-volume productions, and only if *code crashes* (firmware that outgrows a memory chip's capacity) and firmware errors do not occur. Frequently, firmware errors are discovered after system production begins; their likelihood increases as codes become longer and more complex. A severe error could require costly scrapping of an entire stock of ROMs; in this case, EPROMs can be more cost-effective. They offer erasability, on-the-spot programmability, and a single-device inventory. Since production EPROMs are usually programmed only once, plastic DIP EPROMs can be used to decrease costs even further.

If EPROMs are erased and reprogrammed in a field application, the EPROM must be replaced. Returned EPROMs are cleaned, erased, reprogrammed, inventoried, and restocked. These maintenance costs could probably be deferred by using E²PROMs. Because E²PROMs are in-circuit reprogrammable, new code can be downloaded via modem, eliminating the need for a service call.

Battery-backed RAM is initially less expensive than E²PROM or NVRAM, and it can be cost effective in properly maintained systems. However, battery failure wipes out stored memory and requires servicing to replace the battery and reestablish destroyed data.

Initial costs, software and hardware overhead costs, code failure costs, and maintenance costs should all be evaluated when considering nonvolatile memory alternatives. The NVM that provides the lowest system life-cycle cost will be the most cost-effective memory. ■

About the author

Terry Kendall has been with Intel for roughly two years. His present assignment is in the Memory Components Division, working on EPROM products applications. He has a BA in architecture from the University of Oregon and a BSEE from California State University in Sacramento.

Flash Memories (Electrically Erasable and Reprogrammable Non-Volatile Memories)

6

FLASH
A NEW WAY TO DEAL WITH MEMORY

Computers use memory to perform several functions—backup storage, executable code storage, and data manipulation. Today, in systems where the code changes, RAM is used to serve the function of code storage for execution by the processor. RAM also serves the purpose of allowing data manipulation in the same technology. Since DRAM is volatile, mass storage or battery-backed SRAM is used to provide nonvolatility. A small amount of ROM/EPROM also provides the storage technology to start computers (direct executable and nonvolatile).

A relatively new semiconductor technology, called flash memory, stands to fundamentally change this scenario. Because of its true nonvolatility, electrical erasability and low cost, flash memory is regarded as an ideal memory for embedded applications requiring code or data updates. And so it is. However, because of its inherent performance and cost characteristics and recent third-party software developments, flash memory is also the technology that will reshuffle the existing memory hierarchy within portable reprogrammable applications more dramatically than any other.

WHAT IS FLASH MEMORY?

At the semiconductor technology level, Intel's ETOX™ (EPROM tunnel oxide) flash memory is based on a single-transistor EPROM cell. As such, flash memory is nonvolatile, meaning that it retains its contents even if power is removed. This is in contrast to volatile memory technologies like static and dynamic RAMs that require continuous power to store information. Flash memory's cell structure and EPROM foundation also ensure that it is extremely cost-effective to manufacture, continually scalable to higher densities (Figure 1), and highly reliable—a combination of characteristics other semiconductor memory technologies currently lack.

In contrast to EPROMs, however, which can only be erased through exposure to ultraviolet light, the flash memory array is electrically erasable—in bulk. This distinguishes it from traditional EEPROMs (electrically erasable programmable read-only memory) that are by definition byte-alterable; the flash memory erase function empties the entire device all at once (the device can be *programmed* incrementally, however—an important capability for PC applications that require frequent data/file updates). EEPROM technology's byte-alterability, truly needed in a very small number of applications, comes at a high price in terms of cell complexity, limited density and questionable reliability (Figure 2).

	Intel ETOX™ Flash	EEPROM
Transistors	1	2
Cell Size (1-Micro Lithography)	15μ	38μ
Cycling Failures	0.1%	5%

Figure 2

Lastly, unlike competitive approaches to flash memory, Intel's ETOX process produces devices that can be cycled, or erased and reprogrammed, hundreds of thousands of times without fail. Again, this is a unique and essential capability within reprogrammable applications where files are updated frequently.

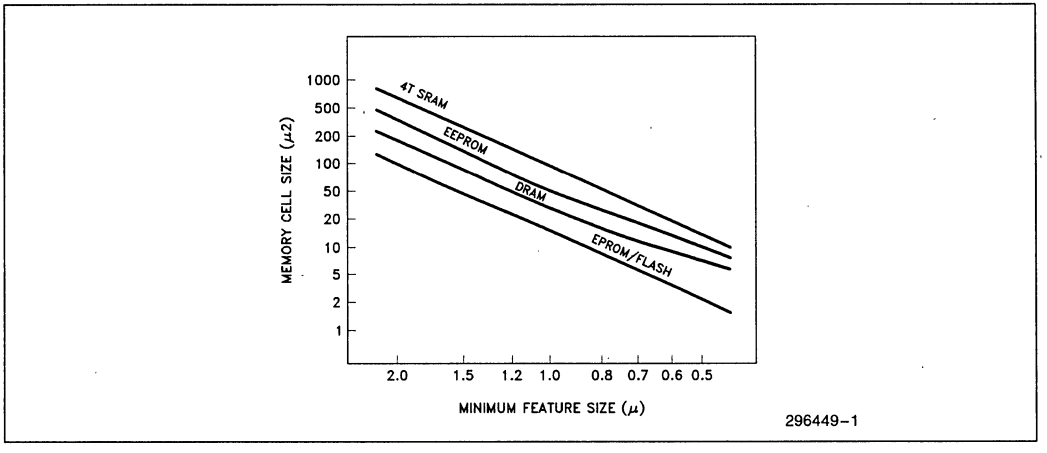


Figure 1

Order Number: 296449-002

In simple terms, therefore, flash memory is a cost-effective, highly reliable read/write nonvolatile memory. Functionally, since it is random-access, flash memory can also be considered a nonvolatile RAM—making it an ideal medium for both program code (application software) and data (user file) storage within a wide variety of computer systems. As portable systems continue to be impeded by the limitations of more established memory technologies, designers will undoubtedly recognize the unique performance and technology advantages provided by flash technology.

THE IMPETUS BEHIND THE 'SOLID-STATE' DISK

Because the disk-based PC is so prevalent and eminently familiar to both designers and end users, many of today's portable systems still rely on this memory configuration as their primary media. At the same time, disk drive manufacturers have made great strides toward improving the reliability, size and performance of their systems, as well as the disk media themselves.

Yet the disk drive is an electro-mechanical system with inherent limitations. Any mechanical system is much more vulnerable to the shock, vibration and impurities that portable computers are likely to encounter during normal use than solid-state, semiconductor technologies which have no moving parts. The drive also typically requires anywhere from 3 watts to as many as 8 watts of power to run—which means a rapid drain of a portable system's batteries. Compare this to a flash-based disk that uses just 0.5 watt. In fact, the disk drive's power drain can be so rapid that many batteries used in today's portable computers last only a couple of hours during normal usage. Needless to say, this represents a severe hindrance to the average user who may not have ready access to a power outlet, backup batteries or a battery charger.

Additional shortcomings of disk drives are their size, weight and floor costs. The size of the mechanical elements required to physically run a drive, as well as the support components and the casing, can be reduced only a finite amount and still be operable. Similarly, the cost of the hardware also has finite limits that, in low-density configurations sufficient for portable PC applications, can add substantial overhead to overall system cost (Figure 3).

From a performance standpoint, disk-based systems still require some form of supplementary memory that is directly executable. Typically, this takes the form of a RAM cache: Data from the disk is downloaded into the cache before users can access the information. Then when a save operation is desired, the data is uploaded from RAM back onto the disk. This download/upload process slows down system throughput while the redundant memory media produce even more system overhead in the form of added space, power consumption and weight (Figure 4).

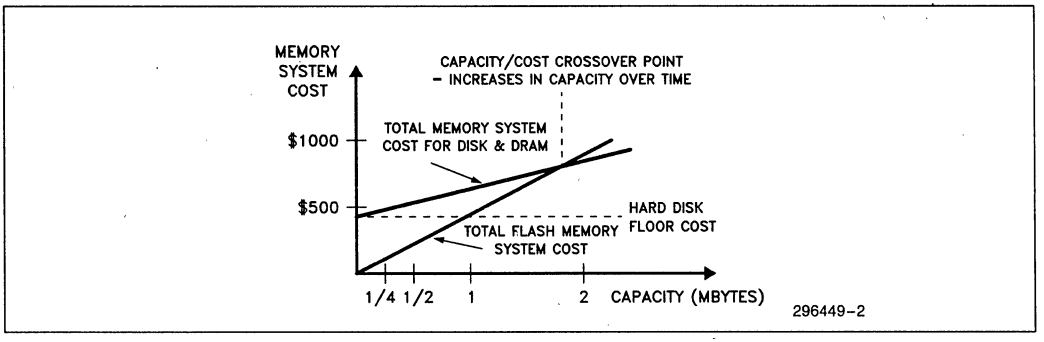


Figure 3

	Disk/DRAM	Flash
Average Seek Time	28.0 ms	0
Latency	8.3 ms	0
Data Transfer Rate Read: Write:	 8 Mbits/Sec. 8 Mbits/Sec. . . . Now Read from RAM	 106.7 Mbits/Sec. 1 Mbit/Sec. Direct Processor Access
Total Time to Access (1 kByte File)	37.3 ms	0.077 ms

Figure 4

WHY NOT STATIC RAMs?

On the surface, static RAMs seem to be well-suited as a solid-state memory alternative to disk/DRAM systems. Static RAM is a very fast read/write technology ideal for direct execution. And to provide nonvolatility, static RAMs can be designed with battery-backup.

However, static RAM's high-speed performance comes at a high cost in terms of silicon technology. Static RAM cells require from four to six transistors to store one bit of information, increasing the silicon area, constraining the achievement of higher densities, and increasing cost.

Add to this the fact that batteries, no matter how advanced, will fail in time. Some elaborate system-level schemes have been devised to warn users when the battery is running low, or to power-down those system features not in use at a given time. Nevertheless, batteries make static RAM-based systems vulnerable to loss of data at inopportune or even critical moments. Plus, the battery adds space and weight to a system—attributes that are increasingly precious as systems are designed to be smaller and lighter.

SOFTWARE DEVELOPMENTS POSITION FLASH FOR PORTABLE APPLICATIONS

Even if from a hardware standpoint flash out-performs disk-based systems, is it realistic to expect that flash memory could truly replace disk drives? After all, flash technology has distinctly different performance attributes than disks . . . attributes that might seem to preclude its use with the huge existing software base that was developed with disk execution in mind. In fact, the majority of today's personal computers and supporting software programs are designed to run using Microsoft Corp.'s MS-DOS* disk operating system. MS-DOS was developed to optimize the serial performance characteristics of disk drives and allow broad-based compatibility between systems and software. Through its adoption by most major computer manufacturers and software developers, it has become the personal computer industry's de facto operating system standard. Attempting to change this scenario to accommodate the advent of flash memory would be a formidable task.

Fortunately, it is not necessary. Thanks to recent software developments by Microsoft, flash memory can effectively serve as the main memory within portable PCs, providing user functions virtually identical to, and even improved over, those of disk-based systems. Specifically, two recent developments allow this achievement: DOS in a ROM-executable form (DOS was formerly designed to be stored on disk and then downloaded to/executed out of RAM); and a file system designed for Intel's flash technology that allows the devices to perform block erasures.

ROM-executable DOS provides several benefits to both system manufacturers and ultimately end users. First, since most of the operating system is composed of fixed code, the amount of system RAM required to execute DOS is reduced from 50k to 15k, thereby conserving system space and power. Secondly, since DOS can now be permanently stored in and executed from a single ROM-type of device (such as flash memory) within the system, floppy disks are eliminated as well as the need for dealer or end-user DOS installation: Systems come ready to run. Lastly, users enjoy "instant-on" performance since the traditional disk-to-DRAM boot function and software downloading steps are eliminated.

Since erasing and writing data to flash memory is a distinctly different operation than rewriting information to a disk, new software techniques were necessary to allow flash to emulate disk functionality. Microsoft's flash file system was developed to fill this need. The block erase capability provided by the flash file system, developed specifically to optimize the read/write characteristics of Intel's ETOX flash technology, allows users to store and retrieve data or applications programs exactly as they would from a conventional disk drive. In fact, the only difference that a user might perceive is that program and file access is much faster with a system based on flash memory than one based on traditional disk and RAM.

Yet another emerging software development is a modification of the basic input/output system, or BIOS software, found in every PC, so that it may be stored in flash memory. Currently, BIOS programs are typically stored in ROMs or EPROMs. Once the BIOS program code is burned into the ROM or programmed into the EPROM, it cannot be changed for the lifetime of the computer without completely disassembling the system and physically removing the ROM or UV-erasing the EPROM. Flash memory's electrical erasure allows system BIOS to be easily updated by the system manufacturer, a dealer, software developer or end user simply by downloading a new BIOS program from a floppy disk or over a modem.

Updatable BIOS introduces a number of novel capabilities to each party. System manufacturers can easily accommodate last-minute changes to the BIOS software

*Microsoft and MS-DOS are registered trademarks of Microsoft Corporation.

as revisions are made. They can also tailor their systems at the very end of the manufacturing process to accommodate different configurations or peripheral equipment.

Flash memory provides a BIOS software developer the ability to upgrade the program to accommodate emerging disk formats, such as 2.5″ or optical, or new screen and keyboard options. Upgrades are made available to the OEM, who can then easily and immediately program subsequent systems with the latest revision. Similarly, even after a computer is purchased and in use, the end user can be sent a floppy disk containing the updated BIOS. With a few keystrokes, users can update their system's flash memory-resident BIOS program—a capability never before possible or cost-effective.

Sophisticated end users themselves may want to take advantage of the ability to update the BIOS as they add or change disk configurations or formats, screens or keyboards. No longer are they locked into the constraints of their initial system; they may enjoy a new level of system upgrade flexibility and performance achievement that will extend the lifetime and usefulness of a basic system.

CONCLUSION

Intel flash memory presents an entirely new personal computer memory technology alternative. As a high-density, nonvolatile read/write semiconductor technology, it is exceptionally well-suited to serve as a solid-state disk drive or a cost-effective and highly reliable replacement for battery-backed static RAMs. Its inherent advantages over these technologies make it particularly useful in portable systems that require the utmost in low power, compact size and durability while maintaining high performance and full functionality.

Flash memory offers:

— **Inherent Nonvolatility:** Unlike static RAMs, no backup battery is required to ensure data retention. Nor is a disk required as backup storage to dynamic RAM.

— **Cost-Effective High Density:** Intel 1 megabit flash memories cost less than half that of static RAMs on a per-bit basis, not even including the added cost and space of a battery. Their cost is only slightly higher than equivalent dynamic RAMs, yet they don't require the added cost and space of auxiliary (disk) memory.

— **Directly Executable:** Since no disk-to-RAM download step, seek or latency times are incurred with flash memory, users enjoy significantly higher-speed program and file access as well as systems that turn on instantly.

— **Solid-State Performance:** As a semiconductor technology, flash memory is low-power, compact and has no moving parts. Portable computers need no longer drain the battery to run the disk drive motor, or accommodate the disk assembly's added bulk and weight. Nor must users be threatened with the possibility of a disk crash when the going gets rough.

When weighed against alternative technologies, it is clear that flash memory reshuffles the traditional memory hierarchy and possesses the attibutes needed to improve established memory usage techniques.

28F256A
256K (32K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **10 μs Typical Byte-Program**
  - **0.5 Second Chip-Program**
- **10,000 Erase/Program Cycles Minimum**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0 Watts Data Retention Power**
- **Integrated Program/Erase Stop Timer**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ II Flash Nonvolatile Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **JEDEC-Standard Pinouts**
  - **32-Pin Cerdip**
  - **32-Lead PLCC**

(See Packaging Spec., Order #231369)

Intel's 28F256A CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F256A adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F256A increases memory flexibility, while contributing to time and cost savings.

The 28F256A is a 256-kilobit nonvolatile memory organized as 32,768 bytes of 8 bits. Intel's 28F256A is offered in 32-pin plastic dip and 32-lead PLCC. Pin assignments conform to JEDEC standards.

Extended erase and program cycling capability is designed into Intel's ETOX™ II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F256A performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F256A employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 ns access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Typical standby current of 50 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX II process base, the 28F256A levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

October 1990
Order Number: 290243-003

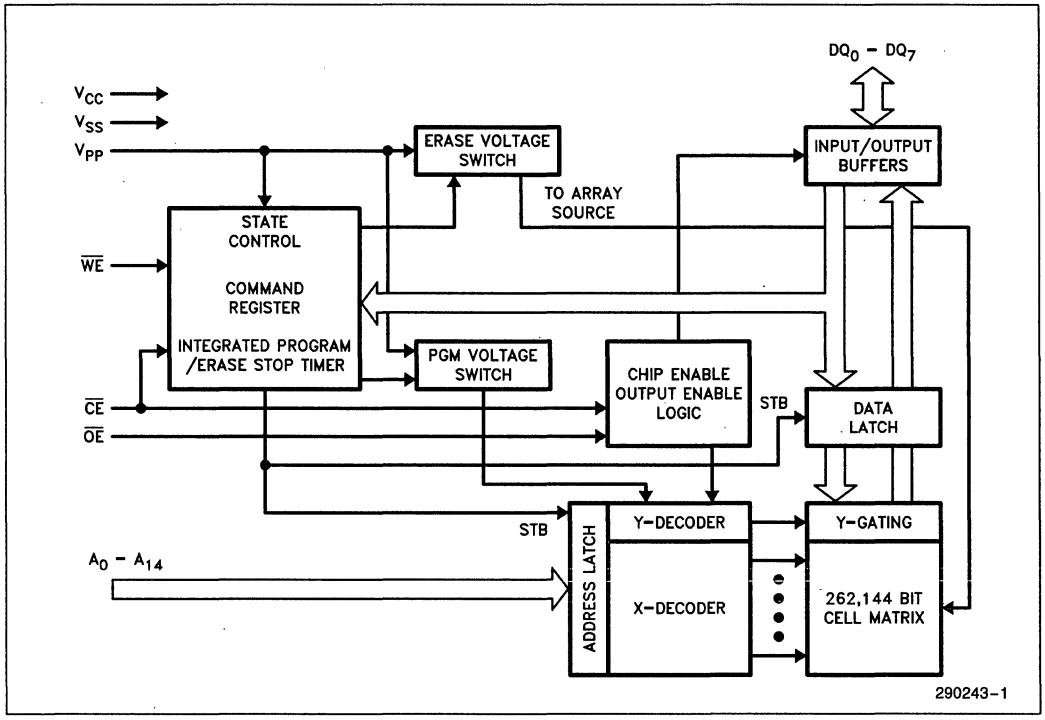


Figure 1. 28F256A Block Diagram

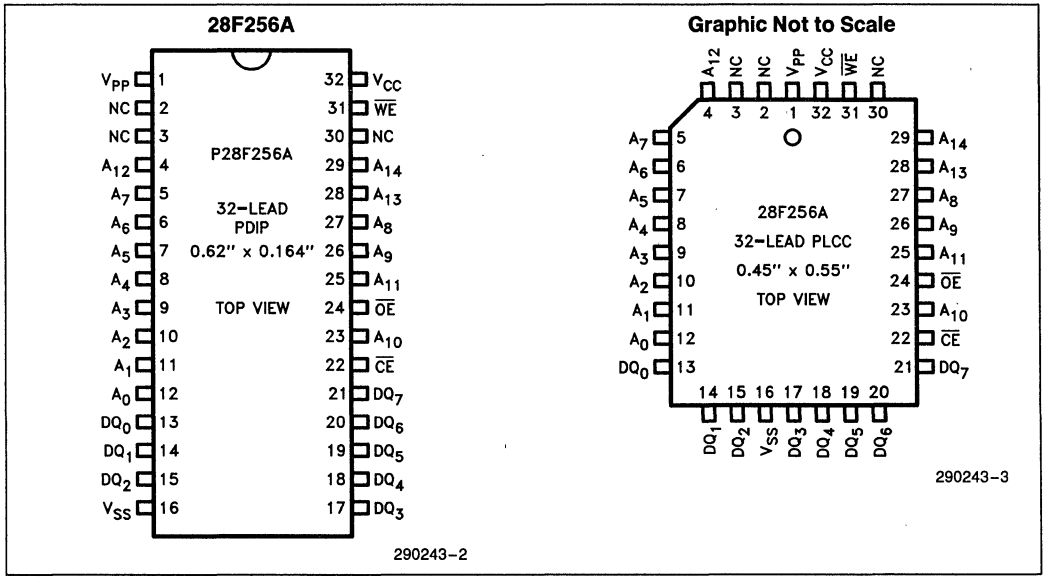


Figure 2. 28F256A Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{14}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE** activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE** controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY (5V ± 10%).**
V_{SS}		**GROUND.**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

APPLICATIONS

The 28F256A flash memory provides nonvolatility along with the capability to typically perform over 100,000 electrical chip-erasusre/reprogram cycles. These features make the 28F256A an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and data-tables are required, the 28F256A's reprogrammability and nonvolatility make it the obvious and ideal replacement for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-DRAM download process. This results in a dramatic enhancement of performance and substantial reduction of power consumption—considerations particularly important in portable equipment. Flash memory increases flexibility with electrical chip-erasure and in-system update capability of operating systems and application code. With updatable BIOS, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems become instant-on. Reliability exceeds that of electromechanical media. Often in these environments, power interrupts force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communications protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/ disk for main system memory or nonvolatile backup storage, the 28F256A provides higher performance, lower power consumption, instant-on capability, and allows an "execute in place" memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacturing to after-sale service. The electrical chip-erasure and reprogramming ability of the 28F256A allows in-circuit alterability; this eliminates unnecessary handling and less-reliable socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system inte-

gration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revision to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F256A, code updates are implemented locally via an edge-connector, or remotely over a communications link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip-erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate".

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F256As tied to the 80C186 system bus. The 28F256A's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

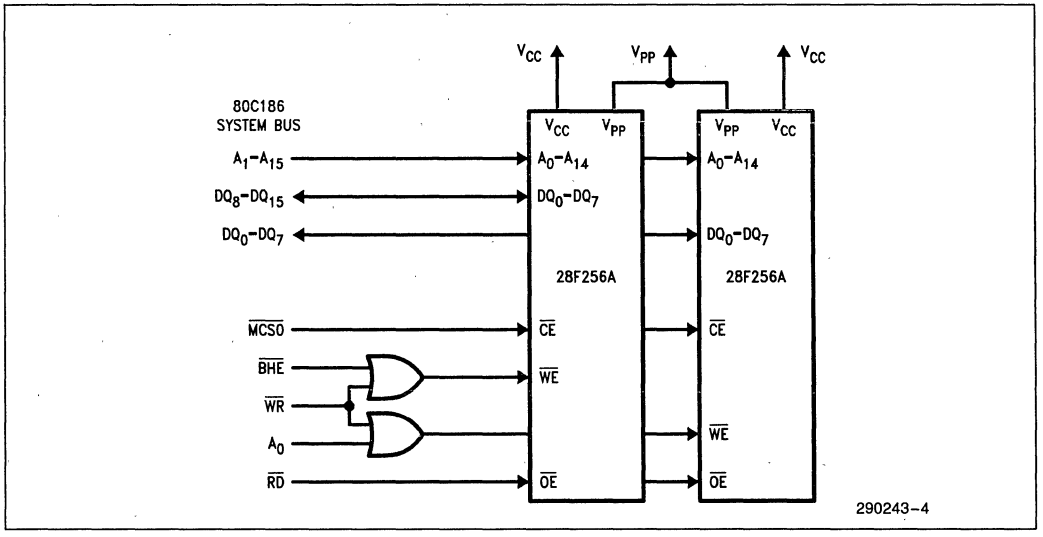


Figure 3. 28F256As in a 80C186 System

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F256A is a functional superset of one or more of the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straightforward interfacing, and in-circuit alterability offer designers unlimited flexibility to meet the high standards of today's designs.

PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F256A introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supply during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F256A is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming and erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

Integrated Program/Erase Stop Timer

Successive command write cycles define the duration of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the 28F256A a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection). The 28F256A is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F256A has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to AC read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operations can be used to access array data, to output the int$_e$ligent Identifier codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can access only the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F256A's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance

state, independent of the Output-Enable signal. If the 28F256A is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

inteligent Identifier™ Operation

The inteligent Identifier operation outputs the manufacturer code (89H) and device code (B9H). Programming equipment automatically matches the device with its proper erase and programming algorithms. With Chip-Enable and Output-Enable at a logic low level, rising A_9 to high voltage V_{ID} (see D.C. Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F256A is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B9H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F256A register commands.

Table 2. 28F256A Bus Operations

	Pins / Operation	V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X(7)	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	inteligent ID Manufacturer(2)	V_{PPL}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	inteligent ID Device(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = B9H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In (6)

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the inteligent Identifier high voltage. Refer to D.C. Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the inteligent Identifier codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read int$_e$ligent ID Codes	3	Write	X	90H	Read	(4)	(4)
Set-Up Erase/Erase(6)	2	Write	X	20H	Write	X	20H
Erase Verify(6)	2	Write	EA	A0H	Read	X	EVD
Set-Up Program/Program(5)	2	Write	X	40H	Write	PA	PD
Program Verify(5)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operation are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memroy location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification. (Mfr = 89H, Device = B9H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of the Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read int$_e$ligent ID command, two read operations access manufacturer and device codes.
5. Figure 4 illustrates the Quick-Pulse Programming Algorithm.
6. Figure 5 illustrates the Quick-Erase Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alternation of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F256A, the device powers-up and remains enabled for reads until the command register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier™ Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F256A contains an int$_e$ligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code 89H. A read cycle from address 0001H returns the device code B9H. To terminate the operation, it is necessary to write another valid command into the register.

Set-Up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erase of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register. To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminate with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence

of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F256A applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-Up Erase/Erase.) Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-Up) to the command register. Figure 5, the Quick-Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F256A. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-Up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program Verify Command

The 28F256A is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F256A applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the 28F256A Quick-Pulse Programming algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an

advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower then EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wear out by a factor of 100,000,000.

The 28F256A is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming and Quick-Ease algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further reliability information, see Reliability Report RR-60 (ETOX II Reliability Data Summary).

QUICK-PULSE PROGRAMMING™ ALGORITHM

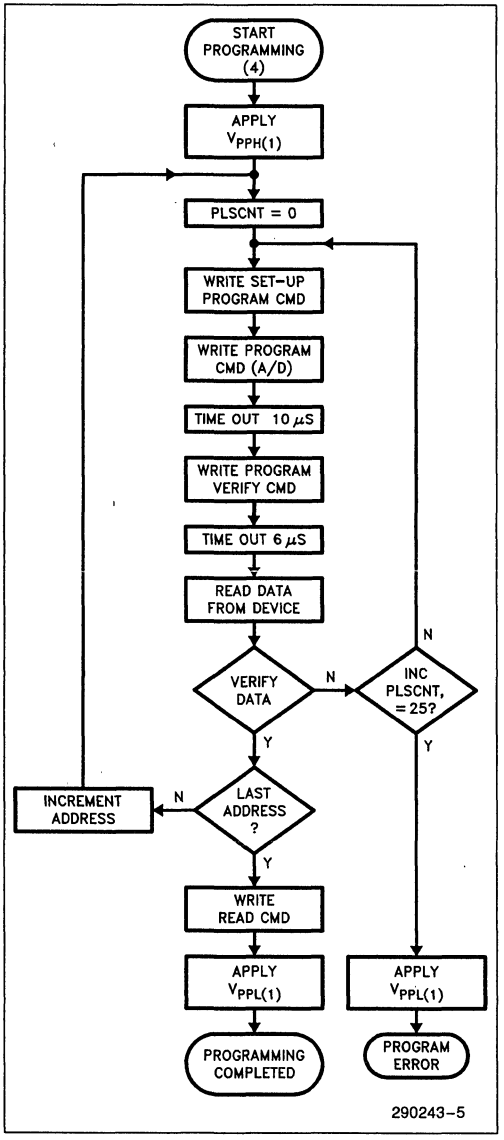
The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming algorithm, to simultaneously remove charge from all bits in the array. Erasure begins with a read of memory contents. The 28F256A is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately one-half second.

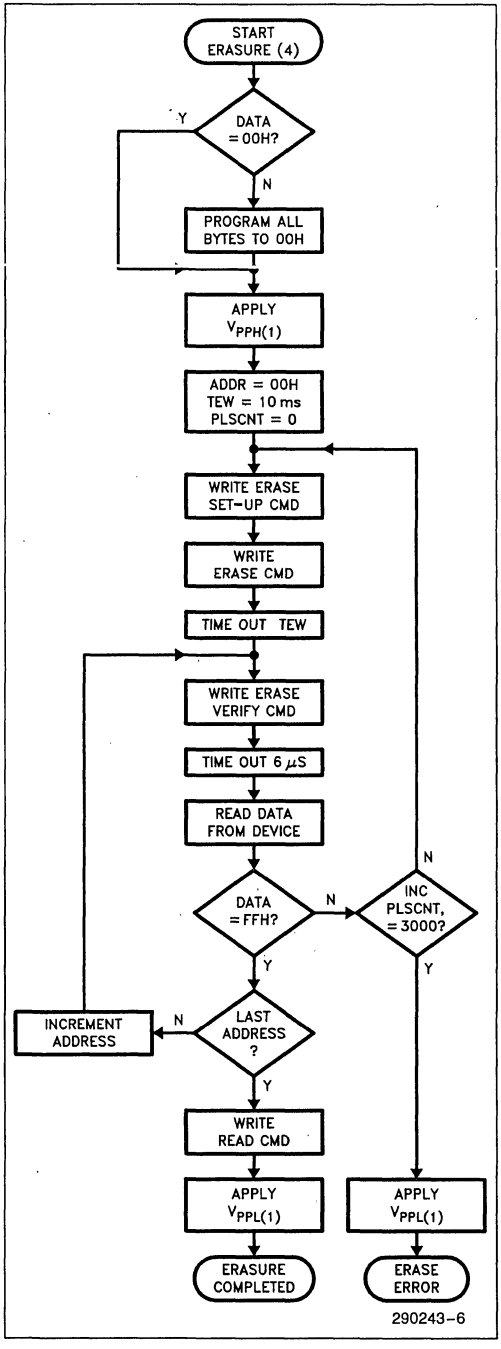
Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (1) Initialize pulse-count
Write	Set-Up Program	Data = 40H
Write	Program	Valid address/data
Standby		Duration of Program operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops (3) Program Operation
Standby		t_{WHGL}
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 4. 28F256A Quick-Pulse Programming™ Algorithm



Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (1) Use Quick-Pulse Programming (Fig. 4)
		Initialize Addresses, Erase Pulse Width, and Pulse Count
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify(2)	Addr = Byte to verify; Data = A0H; Stops Erase Operation (3)
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 5. 28F256A Quick-Pulse™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To efficiently use these two control units, an address-decoder output should drive chip-enable, while the system's read signal controls all flash memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control, and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target smith, requires that the printed circuit board designer pay attention to the V_{PP} pin power supply trace. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The 28F256A is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F256A is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. **Power supply sequencing is not required.** Internal circuitry in the 28F256A ensures that the command register is reset to the read mode upon power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

28F256A Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the 28F256A does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 28F256A.

Table 4. 28F256A Typical Update Power Dissipation(4)

Operation	Power Dissipation (Watt-Seconds)	Notes
Array Program/Program Verify	0.043	1
Array Erase/Erase Verify	0.083	2
One Complete Cycle	0.169	3

NOTES:

1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{PP2} typical + t_{WHGL} × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{CC2} typical + t_{WHGL} × I_{CC4} typical)].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{pp} (I_{PP3} typical × t_{ERASE} typical + I_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC}(I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(1)
During Erase/Program .....0°C to +70°C

Temperature Under Bias .....−10°C to +80°C

Storage Temperature .....−65°C to +125°C

Voltage on Any Pin with
Respect to Ground .....−2.0V to +7.0V(2)

Voltage on Pin A_9 with
Respect to Ground .....−2.0V to +13.5V(2, 3)

V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program .....−2.0V to +14.0(2, 3)

V_{CC} Supply Voltage with
Respect to Ground .....−2.0V to +7.0V(2)

Output Short Circuit Current.....100 mA(4)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods less than 20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

6

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	μA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1			1.0	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erasure Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10.0	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current, or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	20	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$min
V_{ID}	A_9 int$_e$ligent Identifier Voltage		11.50		13.00	V	
I_{ID}	A_9 int$_e$ligent Identifier Current			90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	μA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		50	100	μA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{CC} \pm 0.2V$
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10.0	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current, or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	20	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		$0.85V_{CC}$			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min
V_{OH2}			V_{CC} −0.4				I_{OH} = 100 μA, $V_{CC} = V_{CC}$ min
V_{ID}	A_9 intelligent Identifier Voltage		11.50		13.00	V	
I_{ID}	A_9 intelligent Identifier Current			90	200	μA	$A_9 = V_{ID}$

6

DC CHARACTERISTICS—CMOS COMPATIBLE (Continued)

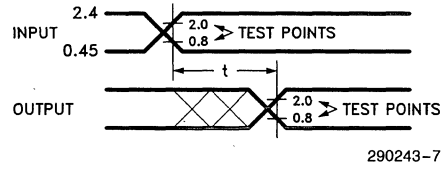
Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

CAPACITANCE(3) T = 25°C, f = 1.0 MHz

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
C_{IN}	Address/Control Capacitance		6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance		12	pF	$V_{OUT} = 0V$

NOTES FOR DC CHARACTERISTICS AND CAPACITANCE:
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, T = 25°C. These currents are valid for all product versions (Packages and Speeds).
2. Not 100% tested: characterization data available.
3. Sampled, not 100% tested.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

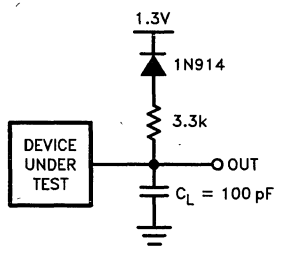
AC TESTING INPUT/OUTPUT WAVEFORM



290243-7

AC Testing: Inputs are driven at 2.5V for a logic "1" and 0.45 for a logic "0". Testing measurements are made at 2.0 for a logic "1" and 0.8 for a logic "0". Rise/Fall time ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

290243-8

AC Test Conditions

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... 0.45 and 2.4
Input Timing Reference Level ..... 0.8 and 2.0
Output Timing Reference Level ..... 0.8 and 2.0

AC CHARACTERISTICS Read-Only Operations[2]

Versions		Notes	28F256A-120		28F256A-150		28F256A-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	3	120		150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			120		150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time			120		150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			50		55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	3		55		55		60	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	3	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	4		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change[1]	3	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall time ≤ 10 ns.
3. Not 100% tested: characterization data available.
4. Guaranteed by design.

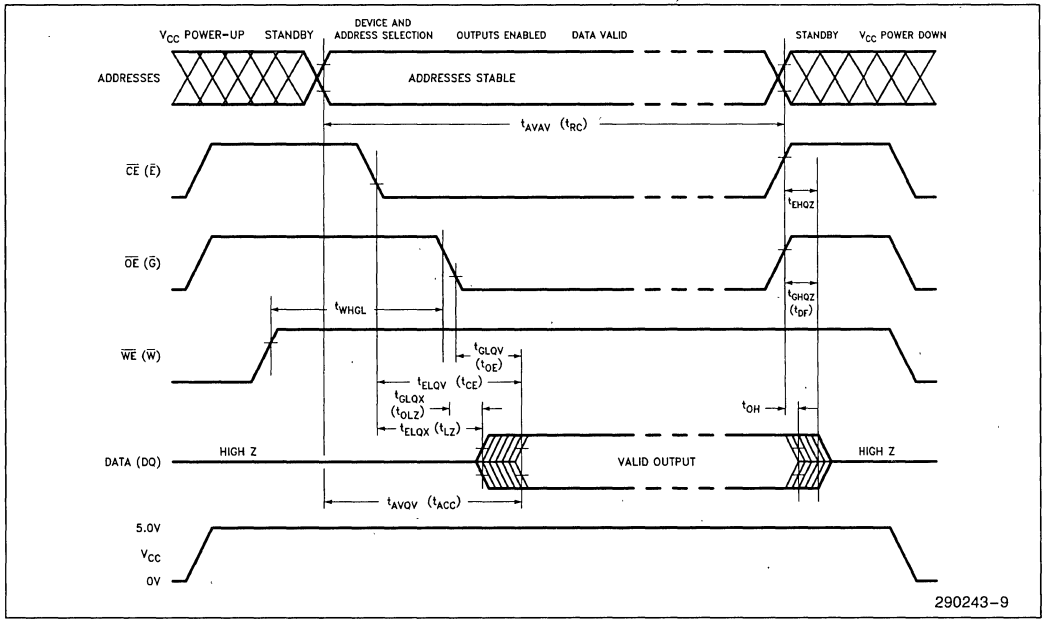


Figure 6. AC Waveform for Read Operations

AC CHARACTERISTICS—For Write/Erase/Program Operations(1, 2)

Versions		Notes	28F256A-120		28F256A-150		28F256A-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		120		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time		0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		60		75		ns
t_{DVWH}/t_{DS}	Data Set-Up Time		50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		μs
t_{GHWL}	Read Recovery Time before Write		0		0		0		μs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write		20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	2	60		60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		10		μs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		9.5		ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		1.0		μs

NOTES:
1. Read timing parameters during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits									Unit
		28F256A-120			28F256A-150			28F256A-200			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		1	10		1	10		1	30	sec
Chip Program Time	1, 2, 4		0.5	3		0.5	3		0.5	3	sec
Erase/Program Cycles	1, 5	10,000	100,000		10,000	100,000		10,000	100,000		cycles

NOTES:
1. "Typicals" are not guaranteed, but based on a limited number of samples taken from production lots. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time excluding system overhead is 16 μs program + 6 μs write recovery), while maximum is 400 μs/byte (16 μs x 25 loops allowed by algorithm). Max chip programming is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming Prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX" II Flash Memory Reliability Data Summary for typical cycling data and failure rate calculations.

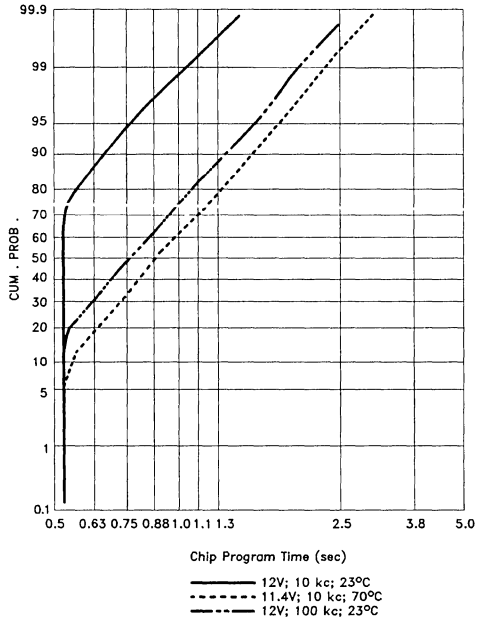


Figure 7. 28F256A Typical Programming Capability

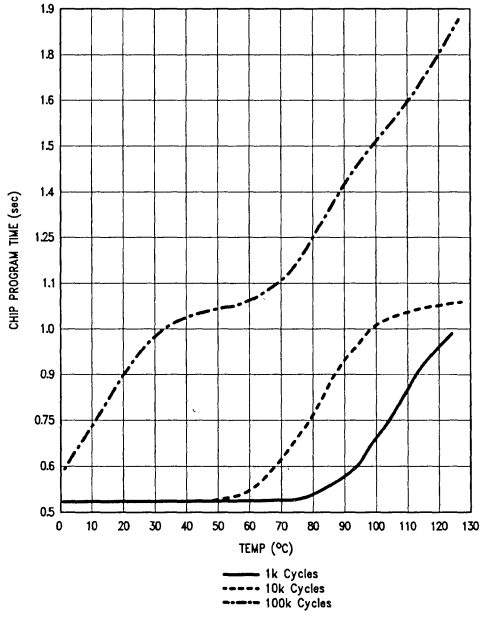


Figure 8. 28F256A Typical Program Time at 12V

6

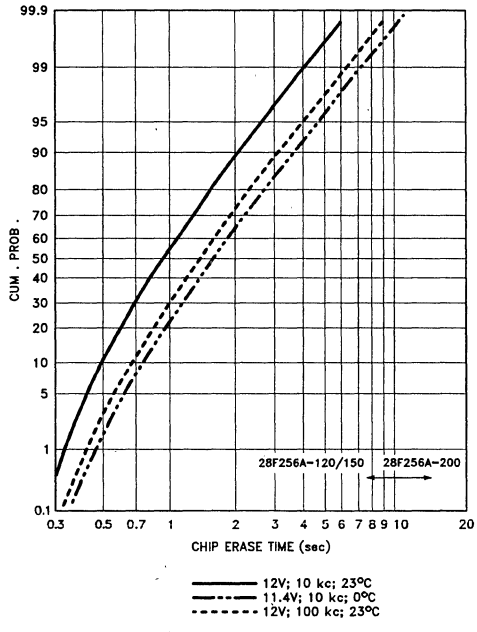


Figure 9. 28F256A Typical Erase Capability

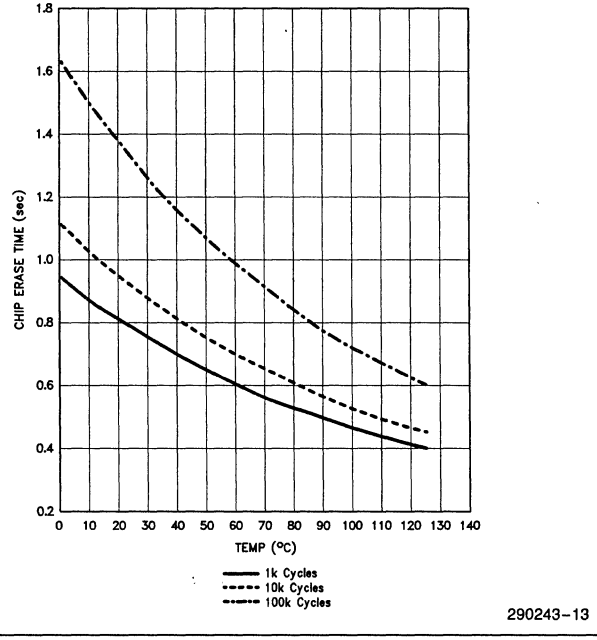


Figure 10. 28F256A Typical Erase Time at 12.0V

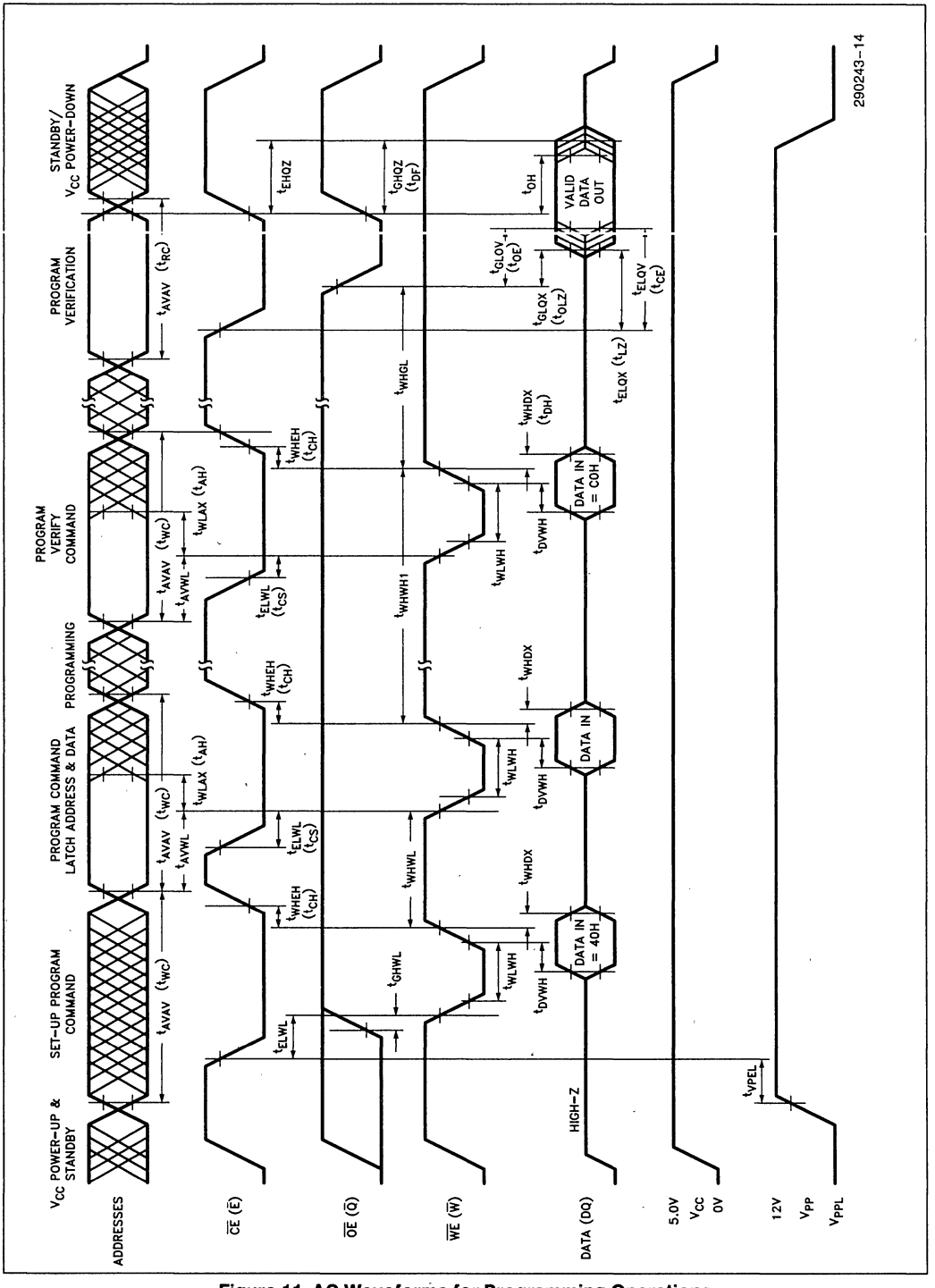


Figure 11. AC Waveforms for Programming Operations

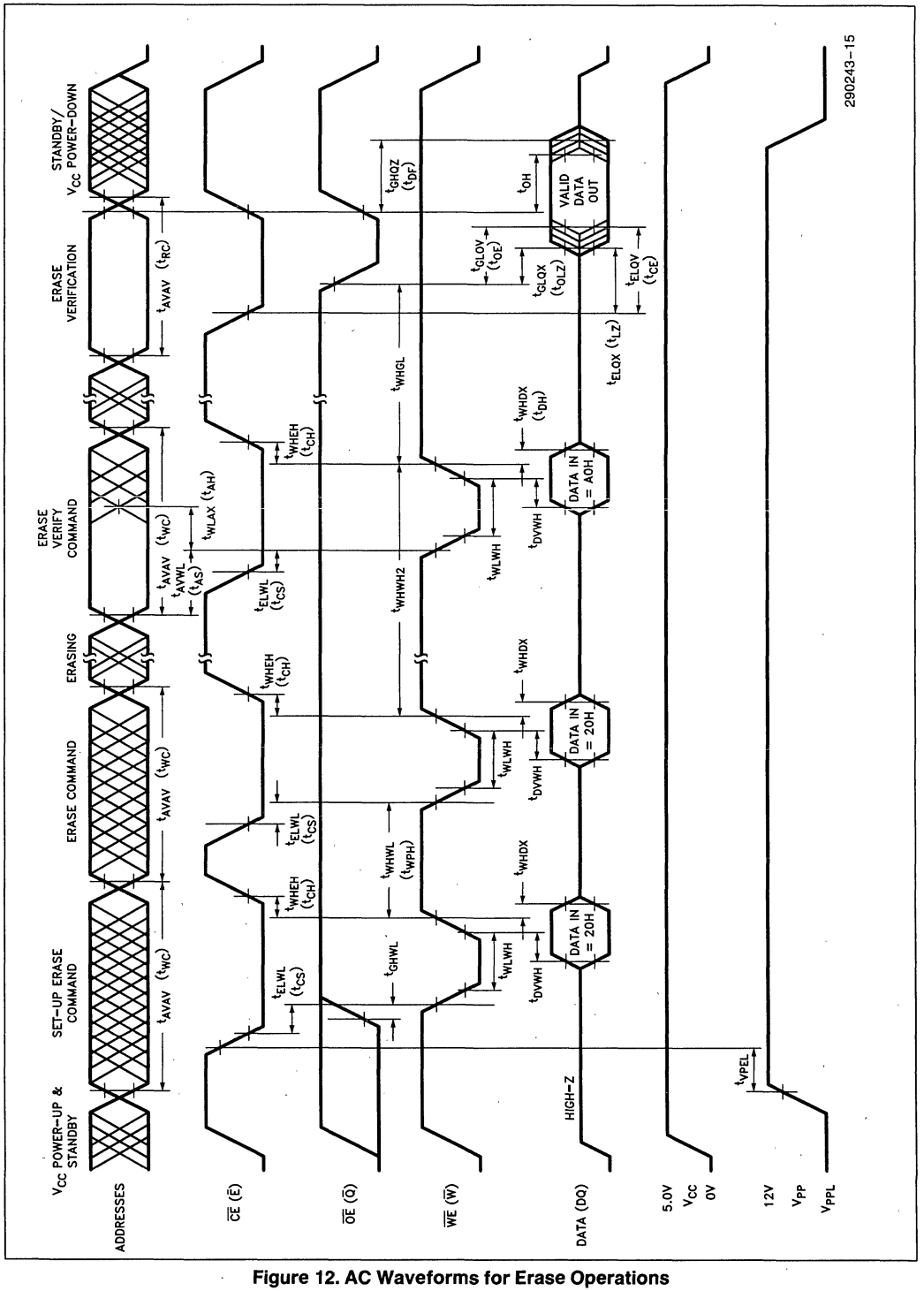


Figure 12. AC Waveforms for Erase Operations

ALTERNATIVE CE-CONTROLLED WRITES

Versions		Notes	28F256A-120		28F256A-150		28F256A-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		120		150		200		ns
t_{AVEL}	Address Set-Up Time		0		0		0		ns
t_{ELAX}	Address Hold Time		80		80		95		ns
t_{DVEH}	Data Set-Up Time		50		50		50		ns
t_{EHDX}	Data Hold Time		10		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		6		µs
t_{GHEL}	Read Recover Time before Write		0		0		0		µs
t_{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		70		80		ns
t_{EHEL}	Write Pulse Width High		20		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip-Enable Low		1.0		1.0		1.0		µs

NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (with a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.

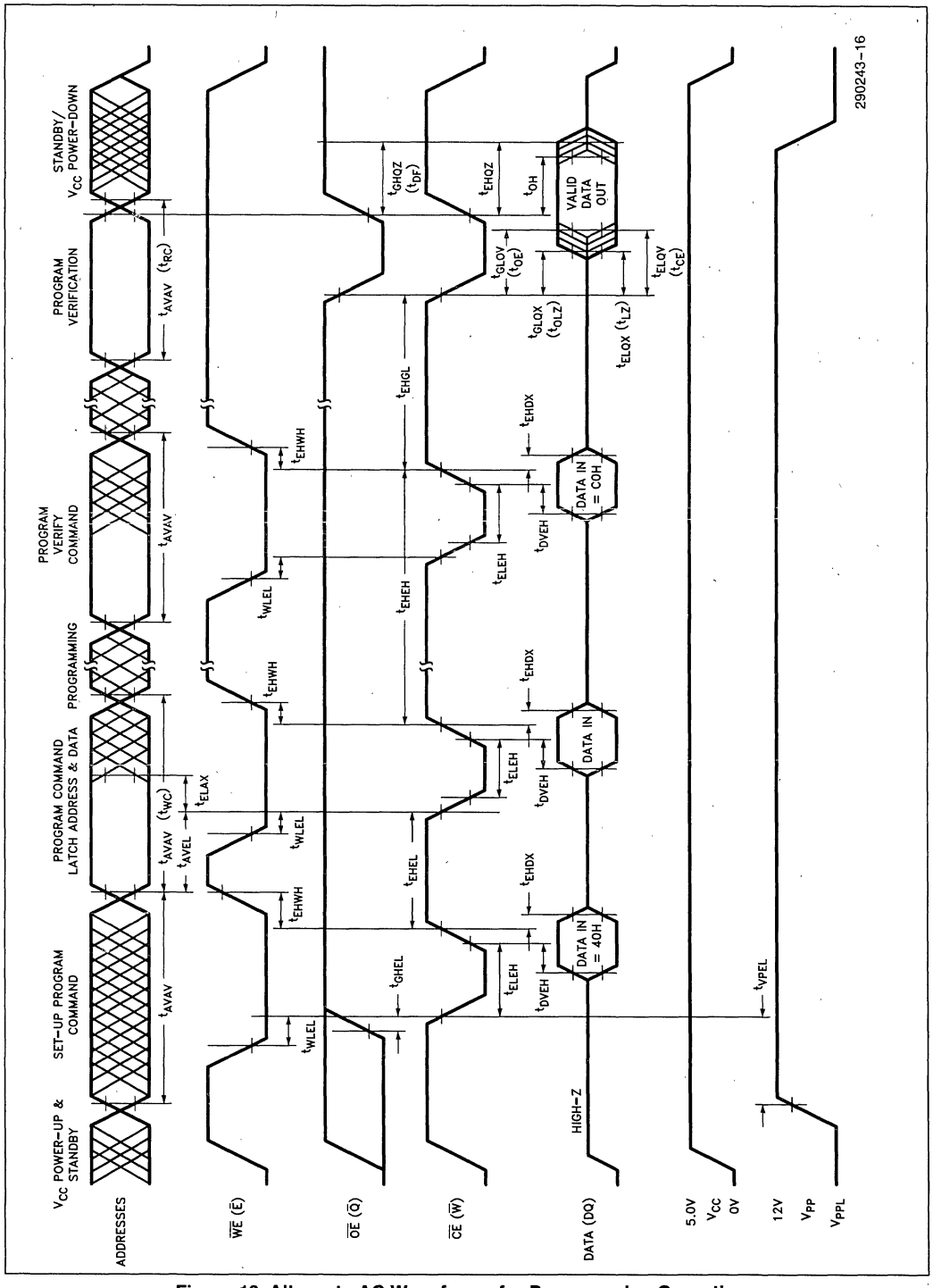
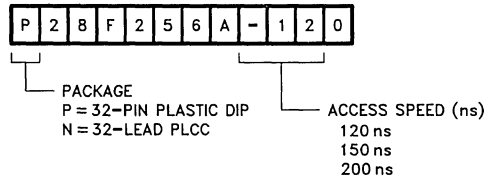


Figure 13. Alternate AC Waveforms for Programming Operations

ORDERING INFORMATION



230240-17

VALID COMBINATIONS:
P28F256A-120
P28F256A-150
P28F256A-200
N28F256A-120
N28F256A-150
N28F256A-200

ADDITIONAL INFORMATION

	Order Number
ER-20, "ETOX II Flash Memory Technology"	294005
ER-24, "The Intel 28F010 Flash Memory"	294008
RR-60, "ETOX II Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogramming Nonvolatile Storage"	292046
AP-325, "Guide to Flash Memory Reprogramming"	292059

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28F512
512K (64K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **10 μs Typical Byte-Program**
  - **1 Second Chip-Program**
- **10,000 Erase/Program Cycle Minimum**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0W Data Retention Power**
- **Integrated Program/Erase Stop Timers**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ II Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **JEDEC-Standard Pinouts**
  - **32-Pin Plastic Dip**
  - **32-Lead PLCC**

  (See Packaging Spec., Order #231369)

Intel's 28F512 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F512 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F512 increases memory flexibility, while contributing to time- and cost-savings.

The 28F512 is a 512-kilobit nonvolatile memory organized as 65,536 bytes of 8 bits. Intel's 28F512 is offered in 32-pin plastic dip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F512 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F512 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX II process base, the 28F512 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

October 1990
Order Number: 290204-005

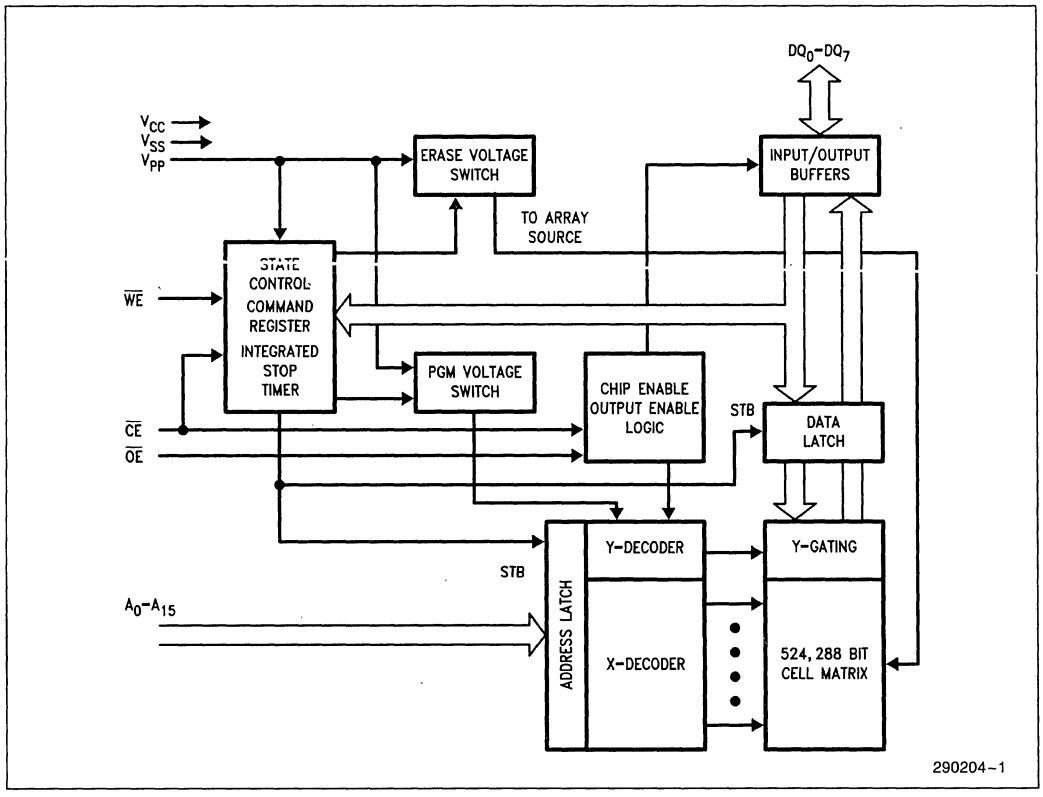


Figure 1. 28F512 Block Diagram

6

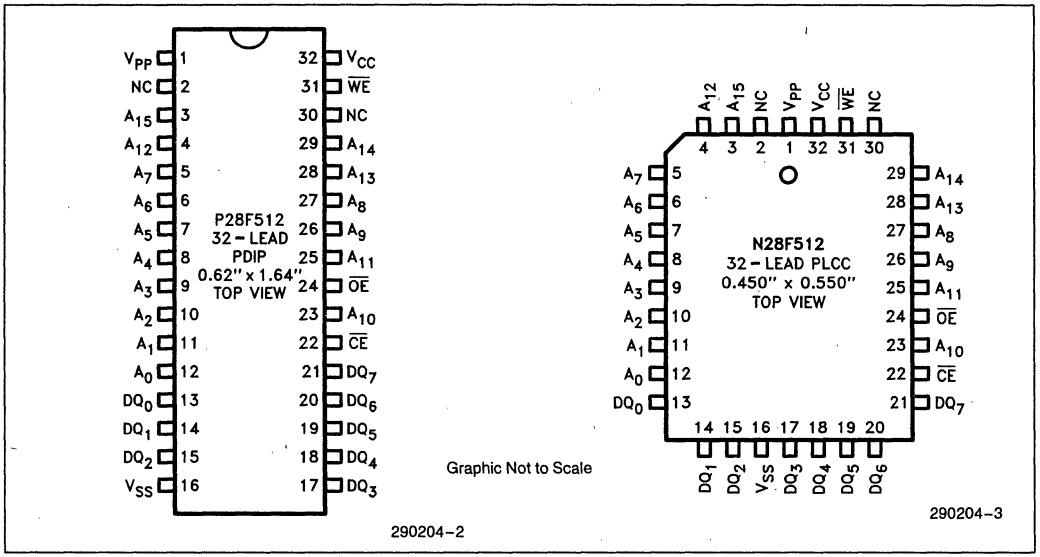


Figure 2. 28F512 Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{15}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ±10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

APPLICATIONS

The 28F512 flash memory provides nonvolatility along with the capability to typically perform over 100,000 electrical chip-erasure/reprogram cycles. These features make the 28F512 an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and datatables are required, the 28F512's reprogrammability and nonvolatility make it the obvious and ideal replacement for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-to-DRAM download process. This results in dramatic enhancement of performance and substantial reduction of power consumption — a consideration particularly important in portable equipment. Flash memory increases flexibility with electrical chip erasure and in-system update capability of operating systems and application code. With updatable BIOS, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems are instant-on. Reliability exceeds that of electromechanical media. Often in these environments, power interruptions force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, the 28F512 flash memory offers a solid state alternative in a minimal form factor. The 28F512 provides higher performance, lower power consumption, instant-on capability, and allows an "execute in place" memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life — from prototyping to system manufacture to after-sale service. The electrical chip-erasure and reprogramming ability of the 28F512 allows in-circuit alterability; this eliminates unnecessary handling and less-reliable socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system integration — the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F512, code updates are implemented locally via an edge-connector, or remotely over a communcation link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate".

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F512s tied to the 80C186 system bus. The 28F512's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F512 offers advantages to the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straight-forward interfacing, and in-circuit alterability offers designers unlimited flexibility to meet the high standards of today's designs.

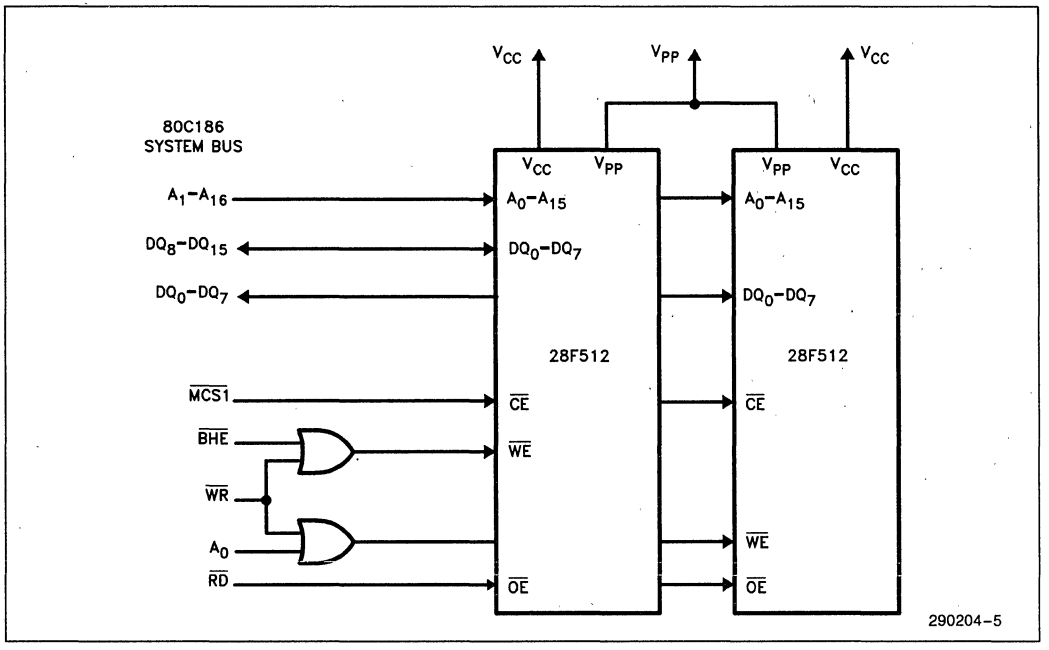


Figure 3. 28F512 in a 80C186 System

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F512 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F512 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

Integrated Stop Timer

Successive command write cycles define the duration of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the 28F512 a read-only memory. In this mode, the memory contents cannot be altered.

Table 2. 28F512 Bus Operations

Operation	Pins	V_{PP}[1]	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	int$_e$ligent Identifier™ (Mfr)[2]	V_{PPL}	V_{IL}	V_{ID}[3]	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	int$_e$ligent Identifier™ (Device)[2]	V_{PPL}	V_{IH}	V_{ID}[3]	V_{IL}	V_{IL}	V_{IH}	Data = B8H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out[4]
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby[5]	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In[6]

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the int$_e$ligent Identifier high voltage. Refer to DC Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the int$_e$ligent Identifier™ codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection). The 28F512 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F512 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to AC read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the int$_e$ligent Identifier™ codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can **only** access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F512's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F512 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

int$_e$ligent Identifier™ Operation

The int$_e$ligent Identifier operation outputs the manufacturer code (89H) and device code (B8H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

6

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F512 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B8H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F512 register commands.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read int$_e$ligent Identifier™ Code(4)	3	Write	X	90H	Read	(4)	(4)
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B8H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read int$_e$ligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Quick-Erase™ algorithm.
6. Figure 4 illustrates the Quick-Pulse Programming™ algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F512, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F512 contains an int$_e$ligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B8H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F512 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 5, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F512. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F512 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F512 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the 28F512 Quick-Pulse Programming™ algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The 28F512 is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming™ and Quick-Erase™ algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further information, see Reliability Report RR-60 (ETOX-II Reliability Data Summary).

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

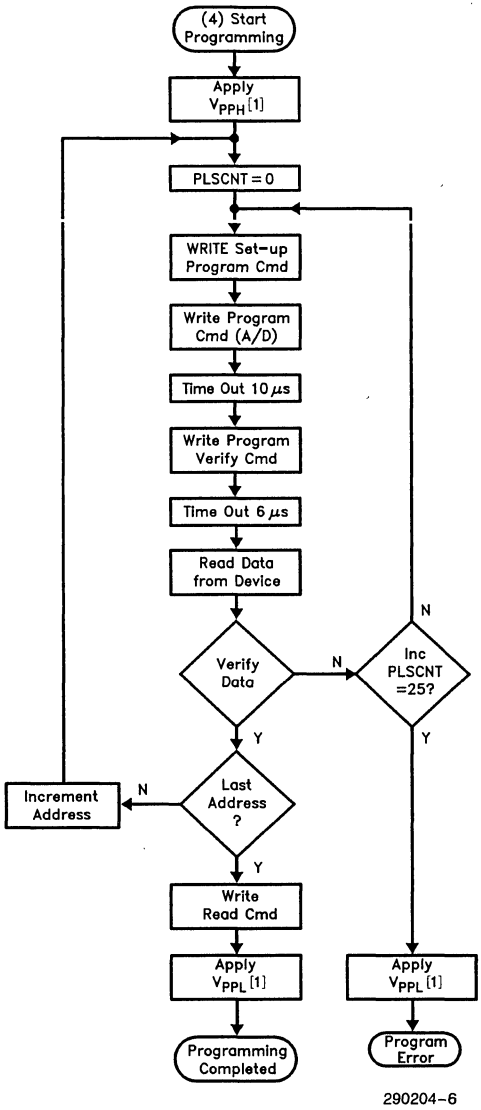
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately one second.

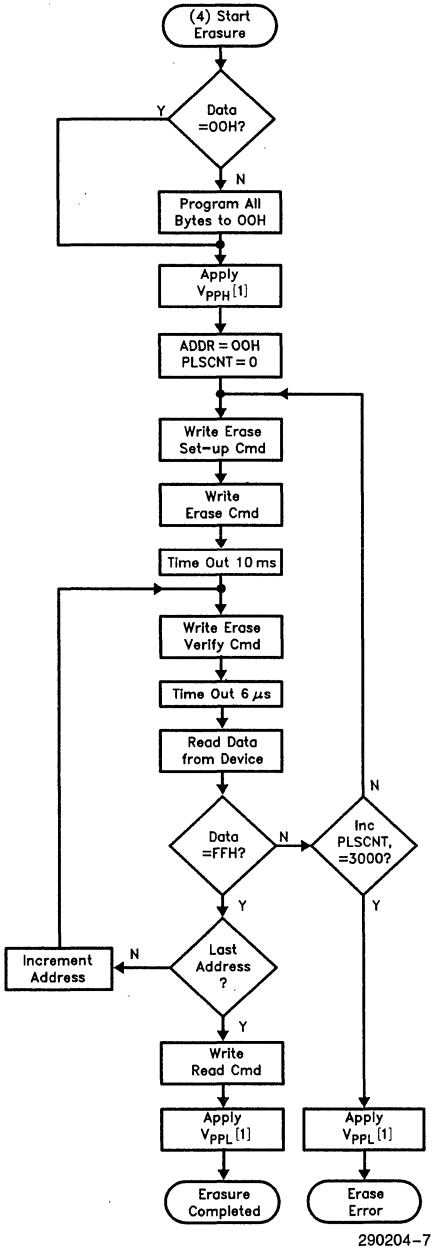
Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 4. 28F512 Quick-Pulse Programming™ Algorithm



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Bus Operation	Command	Comments
		Entire memory must = 00H before erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase(2) Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for value of V_{PPH} and V_{PPL}.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. 28F512 Quick-Erase™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,

b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The 28F512 is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F512 is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the 28F512 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

28F512 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the 28F512 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 28F512.

Table 4. 28F512 Typical Update Power Dissipation(4)

Operation	Notes	Power Dissipation (Watt-Seconds)
Array Program/ Program Verify	1	0.085
Array Erase/ Erase Verify	2	0.092
One Complete Cycle	3	0.262

NOTES:
1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes x Typical # Prog Pulses (t_{WHWH1} × I_{PP2} Typical + t_{WHGL} × I_{PP4} Typical)] + [V_{CC} × # Bytes × Typical # Prog Pulses (t_{WHWH1} × I_{CC2} Typical + t_{WHGL} × I_{CC4} Typical).
2. Formula to calculate typical Erase/Erase Verify Power = [V_{PP}(I_{PP3} Typical × t_{ERASE} Typical + I_{PP5} Typical × t_{WHGL} × # Bytes)] + [V_{CC}(I_{CC3} Typical × t_{ERASE} Typical + I_{CC5} Typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(1)
During Erase/Program .....0°C to +70°C

Temperature Under Bias .....−10°C to +80°C

Storage Temperature .....−65°C to +125°C

Voltage on Any Pin with
Respect to Ground .....−2.0V to +7.0V(2)

Voltage on Pin A_9 with
Respect to Ground .....−2.0V to +13.5V(2, 3)

V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program ....−2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with
Respect to Ground .....−2.0V to +7.0V(2)

Output Short Circuit Current.....100 mA(4)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{LI}	Input Leakage Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1			1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10.0	µA	$V_{PP} \le V_{CC}$
I_{PP1}	V_{PP} Read Current, Standby Current, or ID Current	1		90	200	µA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \le V_{CC}$

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 int$_e$ligent Identifier™ Voltage		11.50		13.00	V	
I_{ID}	A_9 int$_e$ligent Identifier Current			90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		50	100	μA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC}$ ±0.2V
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress

6

DC CHARACTERISTICS—CMOS COMPATIBLE (Continued)

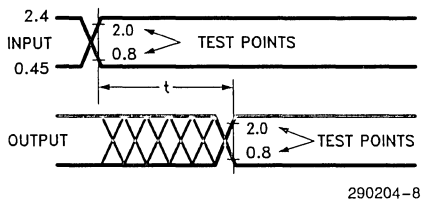
Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{PPS}	V_{PP} Leakage Current	1			±10.0	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current, or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		0.85 V_{CC}			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}			V_{CC} − 0.4				I_{OH} = −100 μA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifier Voltage		11.50		13.00	V	$A_9 = V_{ID}$
I_{ID}	A_9 intelligent Identifier Current			90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN}	Address/Control Capacitance	3		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	3		12	pF	V_{OUT} = 0V

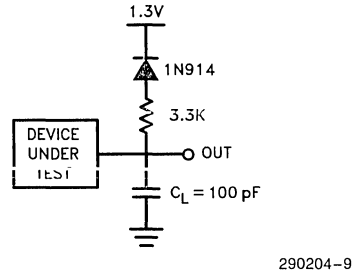
NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = +25°C. These currents are valid for all product versions (packages and speeds).
2. Not 100% tested: characterization data available.
3. Sampled, not 100% tested.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

AC TESTING INPUT/OUTPUT WAVEFORM



AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Testing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0". Rise/Fall time ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V and 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

AC CHARACTERISTICS—Read-Only Operations(2)

Versions		Notes	28F512-120		28F512-150		28F512-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	3	120		150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			120		150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time			120		150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			50		55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	3		55		55		55	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	3	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	4		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change(1)	3	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.
3. Not 100% tested: characterization data available.
4. Guaranteed by design.

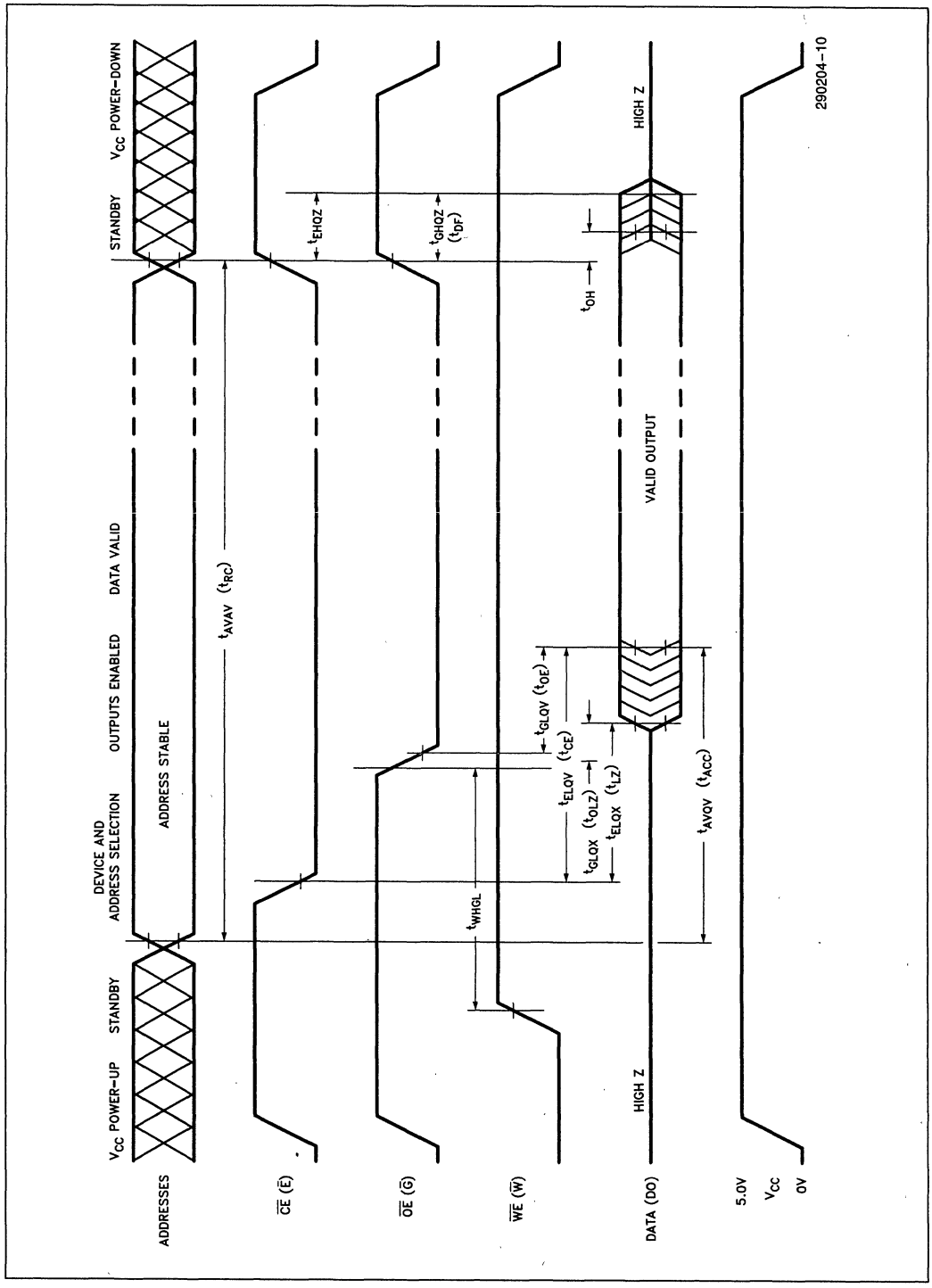


Figure 6. AC Waveforms for Read Operations

AC CHARACTERISTICS—Write/Erase/Program Operations[1, 2]

Versions		Notes	28F512-120		28F512-150		28F512-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		120		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time		0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		60		75		ns
t_{DVWH}/t_{DS}	Data Set-up Time		50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		μs
t_{GHWL}	Read Recovery Time before Write		0		0		0		μs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write		20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	2	60		60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		10		μs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		9.5		ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		1.0		μs

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits									Unit
		28F512-120			28F512-150			28F512-200			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		1	10		1	10		1	30	Sec
Chip Program Time	1, 2, 4		1	6.25		1	6.25		1	6.25	Sec
Erase/ Program Cycles	1, 5	10,000	100,000		10,000	100,000		10,000	100,000		Cycles

NOTES:
1. "Typicals" are not guaranteed, but based on a limited number of samples from production lots. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time excluding system overhead is 16 μs (10 μs program + 6 μs write recovery), while maximum is 400 μs/byte (16 μs × 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming Prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX™ II Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

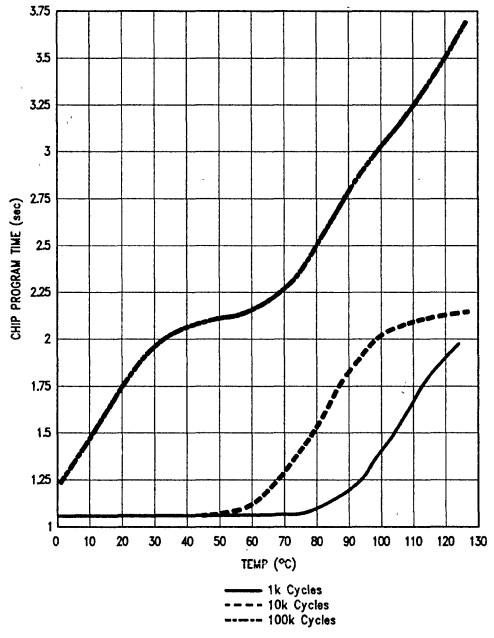


Figure 7. 28F512 Typical Program Time at 12V

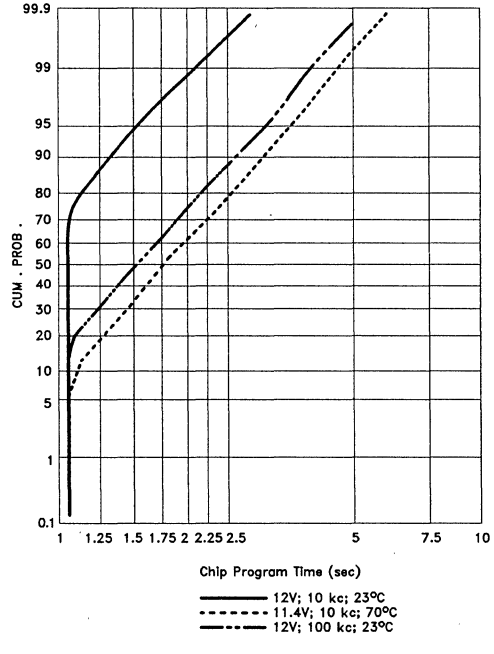
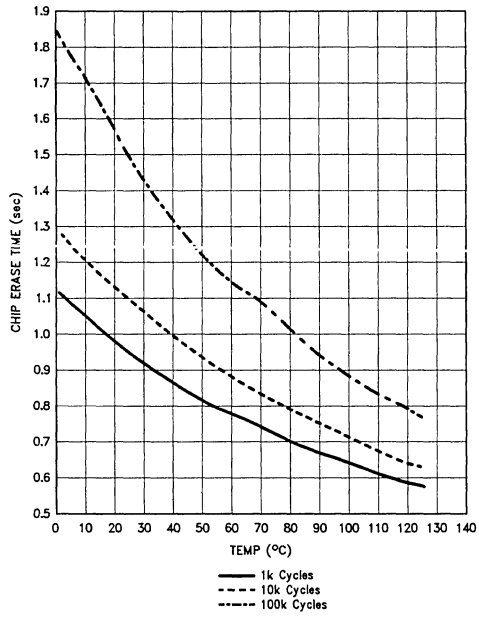


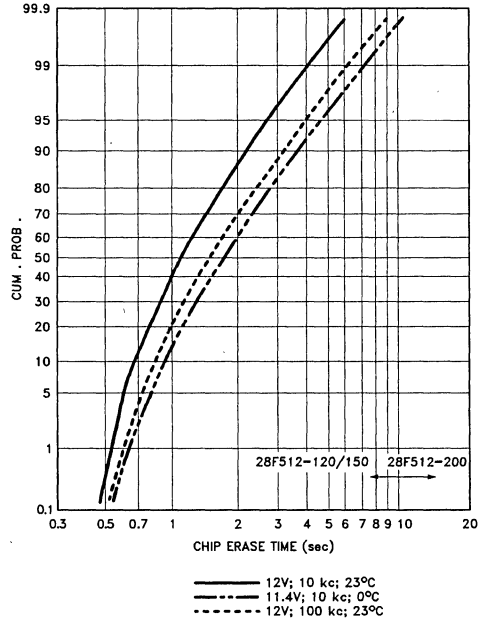
Figure 8. 28F512 Typical Programming Capability



290204-16

NOTE:
Does not include Pre-Erase program.

Figure 9. 28F512 Typical Erase Time at 12V



290204-17

NOTE:
Does not include Pre-Erase program.

Figure 10. 28F512 Typical Erase Capability

6

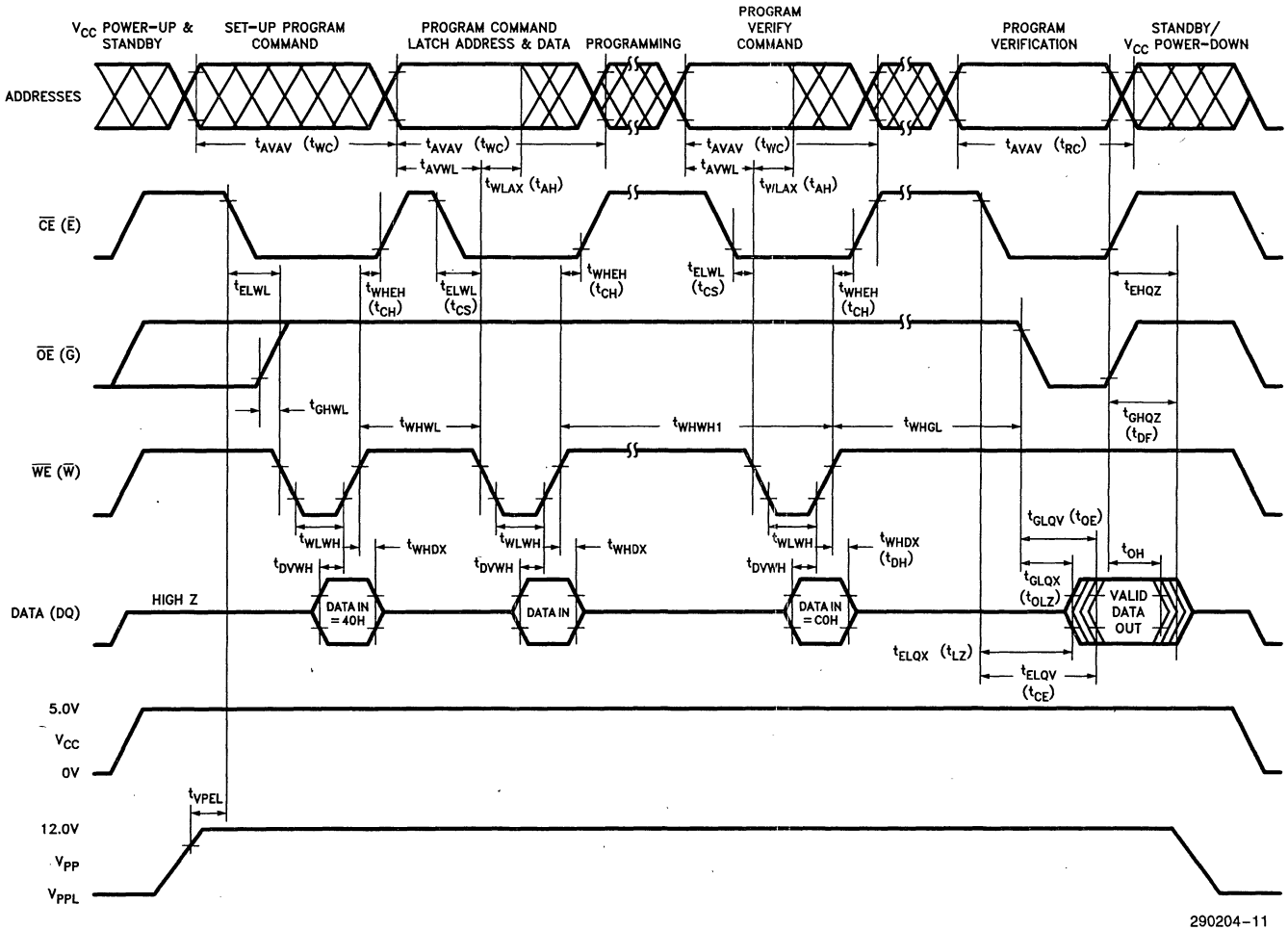


Figure 11. AC Waveforms for Programming Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Versions		Notes	28F512-120		28F512-150		28F512-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		120		150		200		ns
t_{AVEL}	Address Set-Up Time		0		0		0		ns
t_{ELAX}	Address Hold Time		80		80		95		ns
t_{DVEH}	Data Set-Up Time		50		50		50		ns
t_{EHDX}	Data Hold Time		10		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		6		μs
t_{GHEL}	Read Recovery Time before Write		0		0		0		μs
t_{WLEL}	Write Enable Set-Up Time before Chip Enable		0		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		70		80		ns
t_{EHEL}	Write Pulse Width High		20		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		1.0		μs

NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.

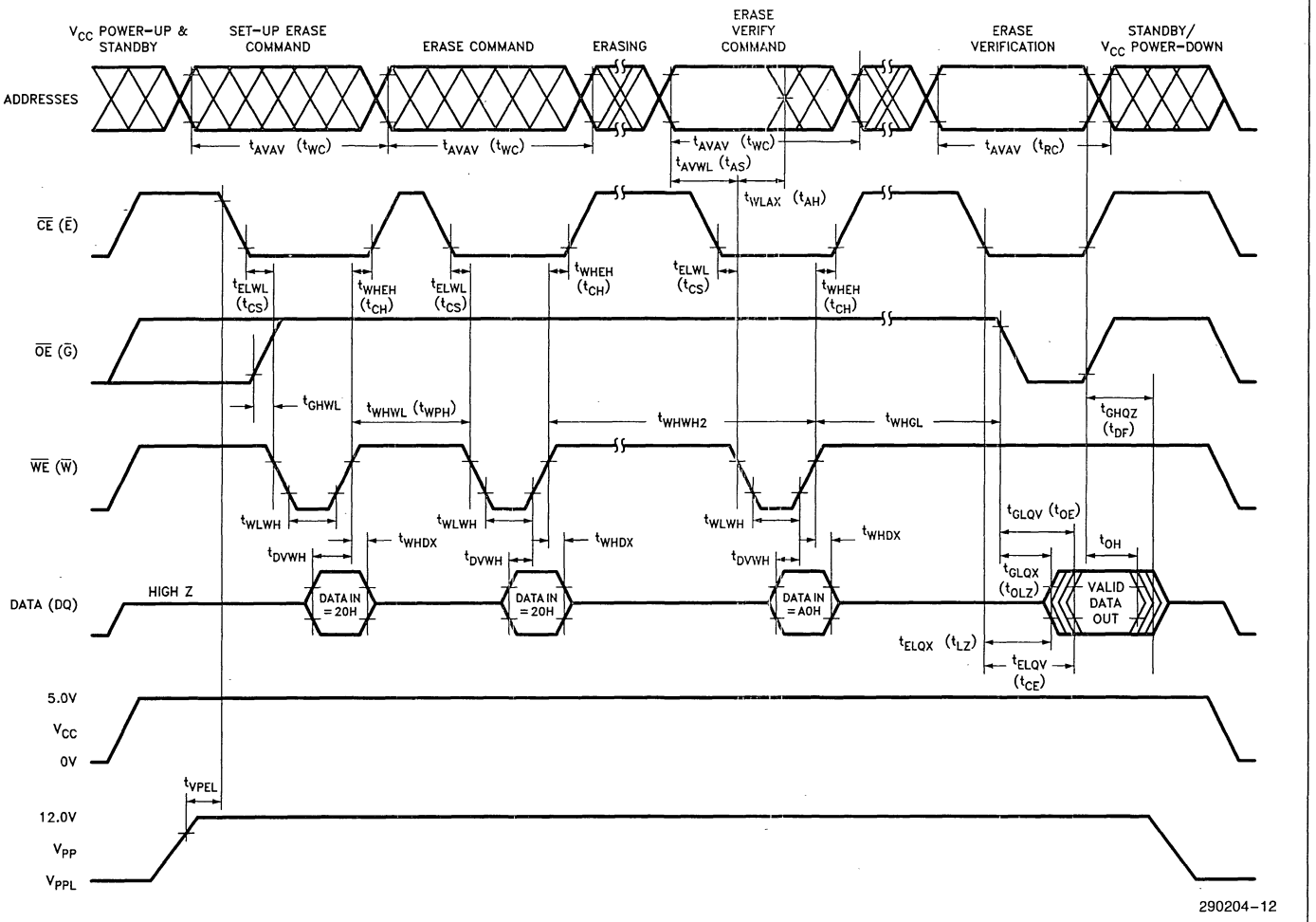


Figure 12. AC Waveforms for Erase Operations

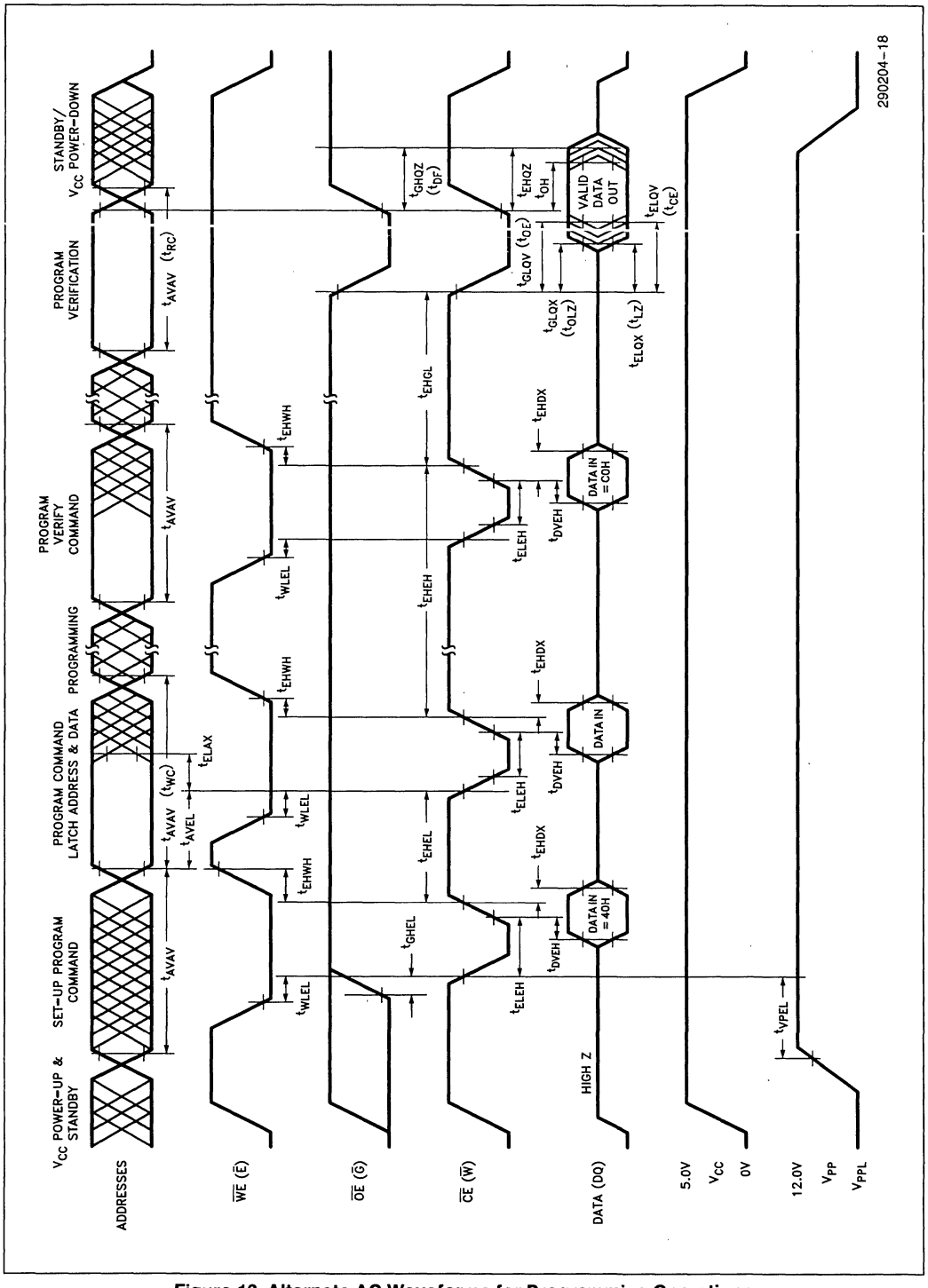
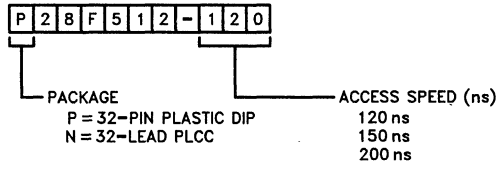


Figure 13. Alternate AC Waveforms for Programming Operations

Ordering Information



Valid Combinations:

P28F512-120	N28F512-120
P28F512-150	N28F512-150
P28F512-200	N28F512-200

ADDITIONAL INFORMATION

	Order Number
ER-20, "ETOX™ II Flash Memory Technology"	294005
ER-23, "The Intel 28F512 Flash Memory"	294007
RR-60, "ETOX™ II Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
AP-325 "Guide to Flash Memory Reprogramming"	292059

28F010
1024K (128K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **10 μs Typical Byte-Program**
  - **2 Second Chip-Program**
- **10,000 Erase/Program Cycles Minimum**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0 Watts Data Retention Power**
- **Integrated Program/Erase Stop Timer**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ II Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **JEDEC-Standard Pinouts**
  - **32-Pin Plastic Dip**
  - **32-Lead PLCC**
  - **32-Lead TSOP**

(See Packaging Spec., Order #231369)

Intel's 28F010 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F010 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F010 increases memory flexibility, while contributing to time- and cost-savings.

The 28F010 is a 1024-kilobit nonvolatile memory organized as 131,072 bytes of 8 bits. Intel's 28F010 is offered in 32-pin plastic dip or 32-lead PLCC and TSOP packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F010 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F010 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX II process base, the 28F010 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

November 1990
Order Number: 290207-006

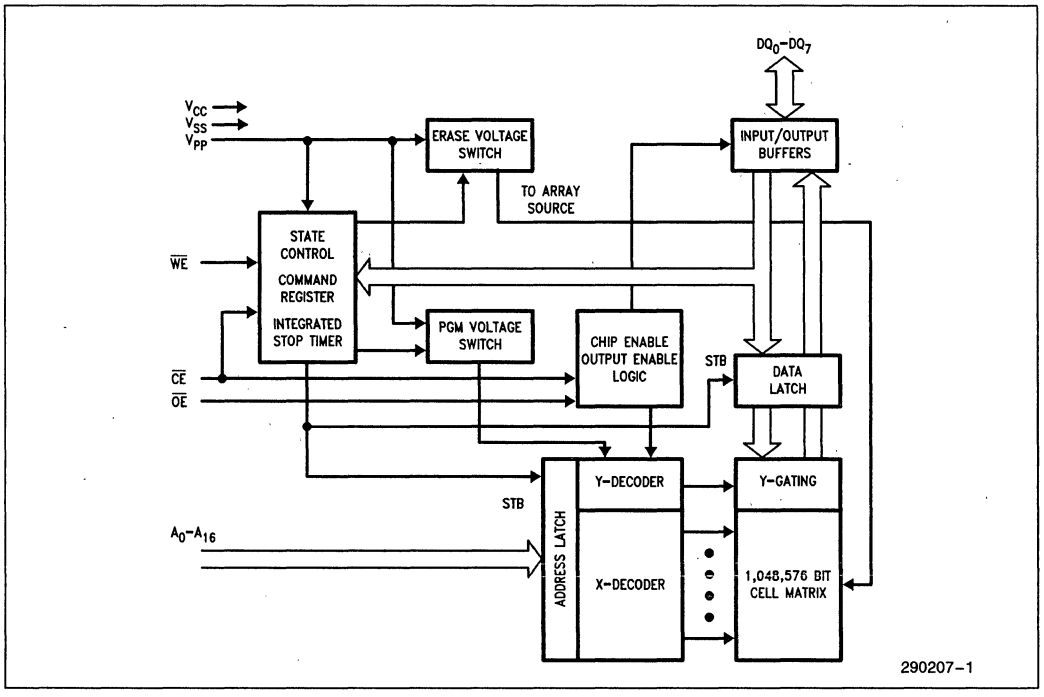


Figure 1. 28F010 Block Diagram

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ±10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

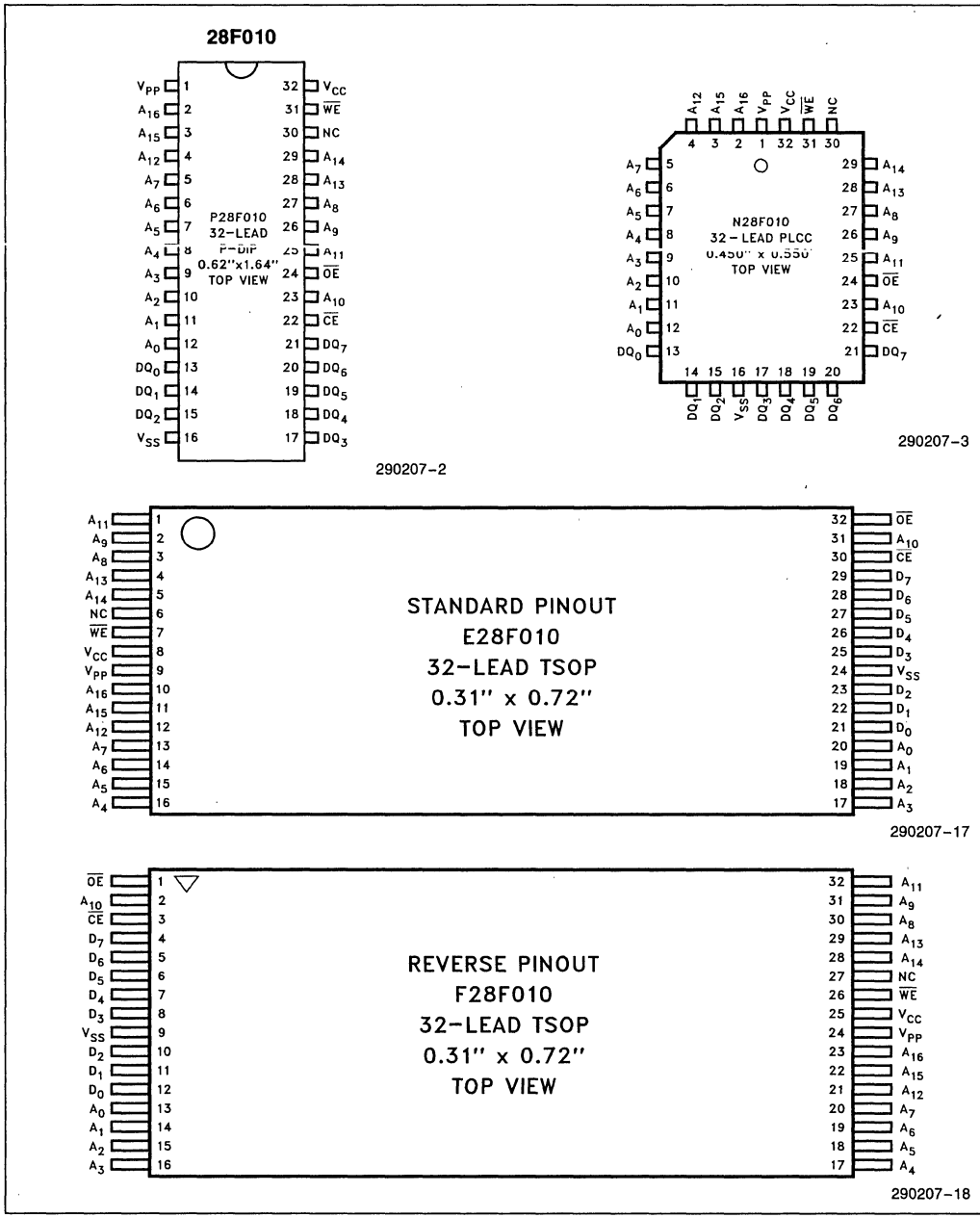


Figure 2. 28F010 Pin Configurations

APPLICATIONS

The 28F010 flash memory provides nonvolatility along with the capability to typically perform over 100,000 electrical chip-erasure/reprogram cycles. These features make the 28F010 an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and datatables are required, the 28F010's reprogrammability and nonvolatility make it the obvious and ideal replacement for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-to-DRAM download process. This results in dramatic enhancement of performance and substantial reduction of power consumption — a consideration particularly important in portable equipment. Flash memory increases flexibility with electrical chip erasure and in-system update capability of operating systems and application code. With updatable BIOS, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems are instant-on. Reliability exceeds that of electromechanical media. Often in these environments, power interruptions force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, the 28F010 flash memory offers a solid state alternative in a minimal form factor. The 28F010 provides higher performance, lower power consumption, instant-on capability, and allows an "execute in place" memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life — from prototyping to system manufacture to after-sale service. The electrical chip-erasure and reprogramming ability of the 28F010 allows in-circuit alterability; this eliminates unnecessary handling and less-reliable socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system integration — the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F010, code updates are implemented locally via an edge-connector, or remotely over a communcation link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate".

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 4 depicts two 28F010s tied to the 80C186 system bus. The 28F010's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

The outstanding feature of the TSOP (Thin Small Outline Package) is the 1.2 mm thickness. With standard and reverse pin configurations, TSOP reduces the number of board layers and overall volume necessary to layout multiple 28F010s. TSOP is particularly suited for portable equipment and applications requiring large amounts of flash memory. Figure 3 illustrates the TSOP Serpentine layout.

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F010 offers advantages to the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straight-forward interfacing, and in-circuit alterability offers designers unlimited flexibility to meet the high standards of today's designs.

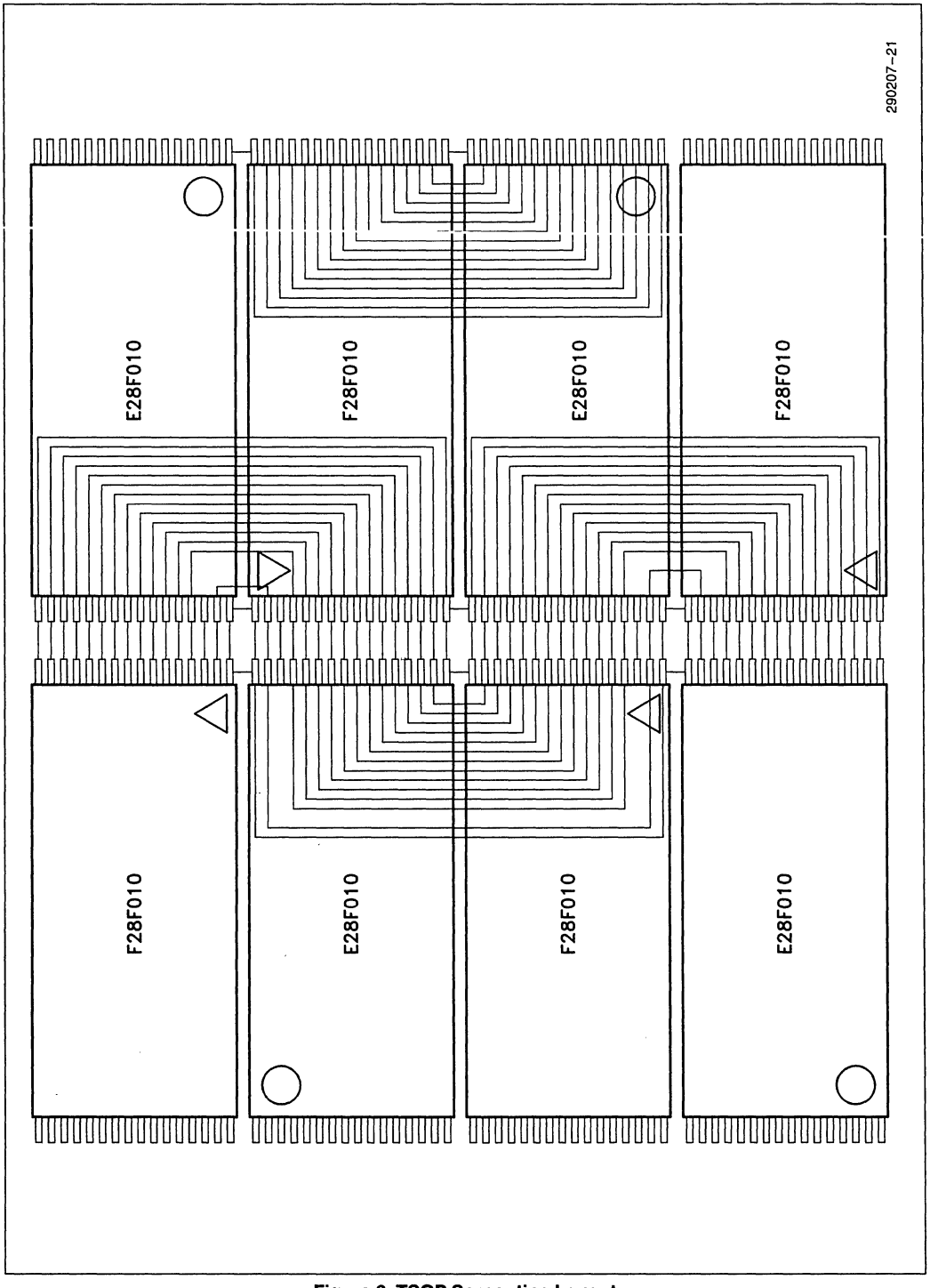


Figure 3. TSOP Serpentine Layout

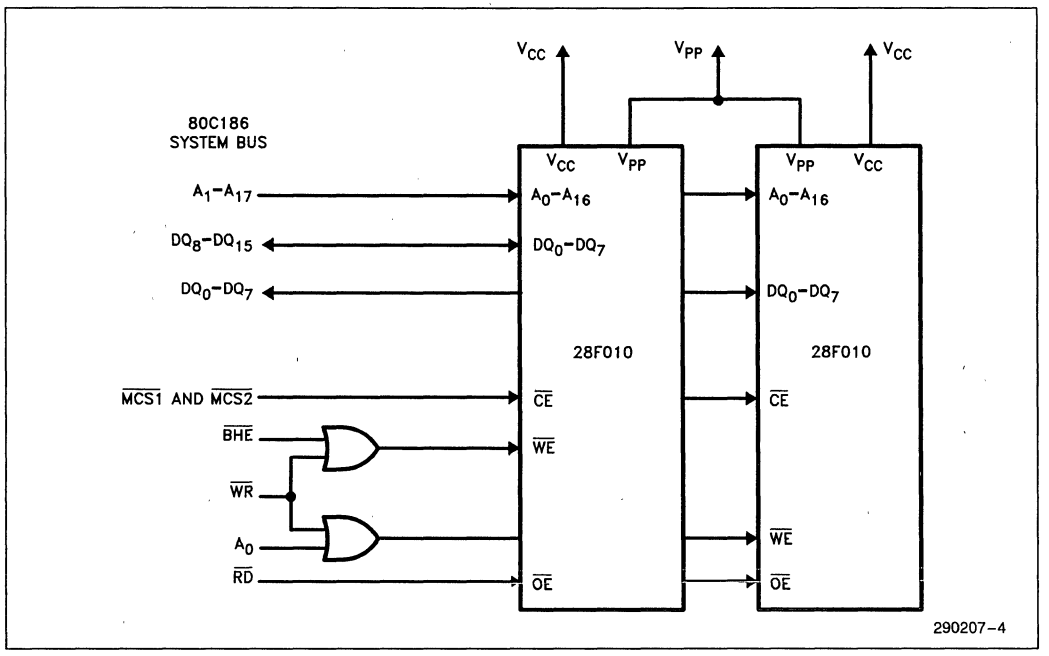


Figure 4. 28F010 in a 80C186 System

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F010 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F010 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

Integrated Stop Timer

Successive command write cycles define the durations of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the con-

Table 2. 28F010 Bus Operations

Operation \ Pins		V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	inteligent Identifier™ (Mfr)(2)	V_{PPL}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	inteligent Identifier™ (Device)(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = B4H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In(6)

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the inteligent Identifier high voltage. Refer to DC Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the inteligent Identifier™ codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

tents of the register default to the read command, making the 28F010 a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection) The 28F010 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F010 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to AC read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the inteligent Identifier™ codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can **only** access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F010's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F010 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

inteligent Identifier™ Operation

The inteligent Identifier operation outputs the manufacturer code (89H) and device code (B4H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F010 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B4H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F010 register commands.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read int$_e$ligent Identifier™ Codes(4)	3	Write	X	90H	Read	(4)	(4)
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B4H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read int$_e$ligent ID command, two read operations access manufacturer and device codes.
5. Figure 6 illustrates the Quick-Erase™ Algorithm.
6. Figure 5 illustrates the Quick-Pulse Programming™ Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F010, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F010 contains an int$_e$ligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B4H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F010 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 6, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F010. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F010 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F010 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 5, the 28F010 Quick-Pulse Programming™ algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The 28F010 is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming™ and Quick-Erase™ algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further information, see Reliability Report RR-60.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 5 illustrates the Quick-Pulse Programming algorithm.

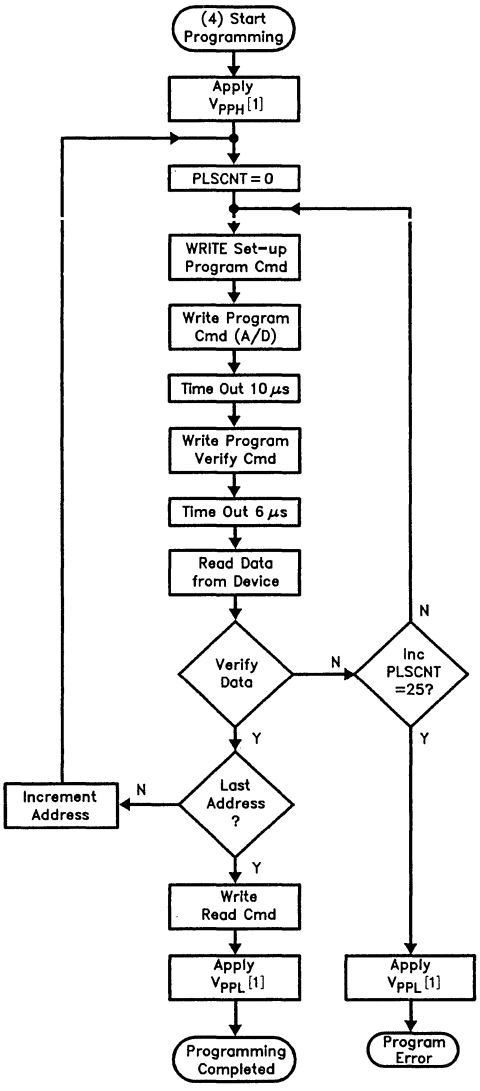
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 6 illustrates the Quick-Erase algorithm.



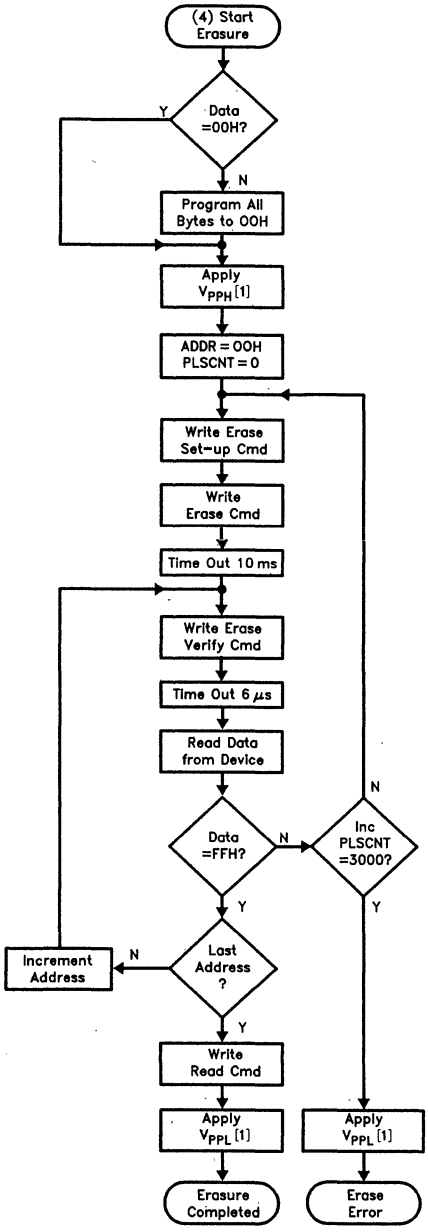
290207-5

Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. 28F010 Quick-Pulse Programming™ Algorithm

6



290207-6

Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 5)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase(2) Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 6. 28F010 Quick-Erase™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The 28F010 is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F010 is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in the 28F010 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

28F010 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the 28F010 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 28F010.

Table 4. 28F010 Typical Update Power Dissipation(4)

Operation	Notes	Power Dissipation (Watt-Seconds)
Array Program/Program Verify	1	0.171
Array Erase/Erase Verify	2	0.136
One Complete Cycle	3	0.478

NOTES:
1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{PP2} typical + t_{WHGL} × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{CC2} typical + t_{WHGL} × I_{CC4} typical].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{PP} (V_{PP3} typical × t_{ERASE} typical + I_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC} (I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C(1)
During Erase/Program ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground ..... −2.0V to +7.0V(2)
Voltage on Pin A_9 with
Respect to Ground ..... −2.0V to +13.5V(2, 3)
V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program .... −2.0V to +14.0V(2, 3)
V_{CC} Supply Voltage with
Respect to Ground ..... −2.0V to +7.0V(2)
Output Short Circuit Current ..... 100 mA(4)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1			1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10	µA	$V_{PP} \leq V_{CC}$

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{PP1}	V_{PP} Read Current or Standby Current	1		90	200	µA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifier™ Voltage		11.50		13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current	1		90	200	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		50	100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC}$ ±0.2V
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10	µA	$V_{PP} \leq V_{CC}$

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DC CHARACTERISTICS—CMOS COMPATIBLE (Continued)

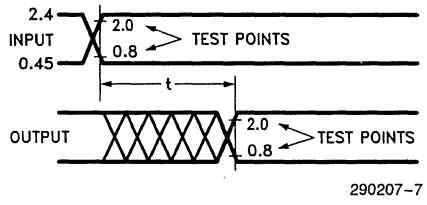
Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{PP1}	V_{PP} Read Current, ID Current or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		6.0	30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		0.85 V_{CC}			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}			V_{CC} − 0.4				I_{OH} = −100 μA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage		11.50		13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current	1		90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Programs are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN}	Address/Control Capacitance	3		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	3		12	pF	V_{OUT} = 0V

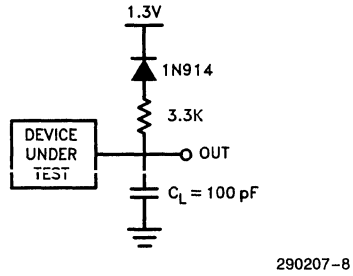
NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. Not 100% tested: characterization data available.
3. Sampled, not 100% tested.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

AC TESTING INPUT/OUTPUT WAVEFORM



AC Testing: Inputs are driven at 2.4 for a logic "1" and 0.45 for a logic "0". Testing measurements are made at 2.0 for a logic "1" and 0.8 for a logic "0". Rise/Fall time ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... 0.45 and 2.4
Input Timing Reference Level ..... 0.8 and 2.0
Output Timing Reference Level ..... 0.8 and 2.0

AC CHARACTERISTICS—Read-Only Operations(2)

Versions		Notes	28F010-120		28F010-150		28F010-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	3	120		150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			120		150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time			120		150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			50		55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	3	0		0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	3		55		55		55	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	3	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	4		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change	1, 3	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.
3. Not 100% tested: characterization data available.
4. Guaranteed by design.

6

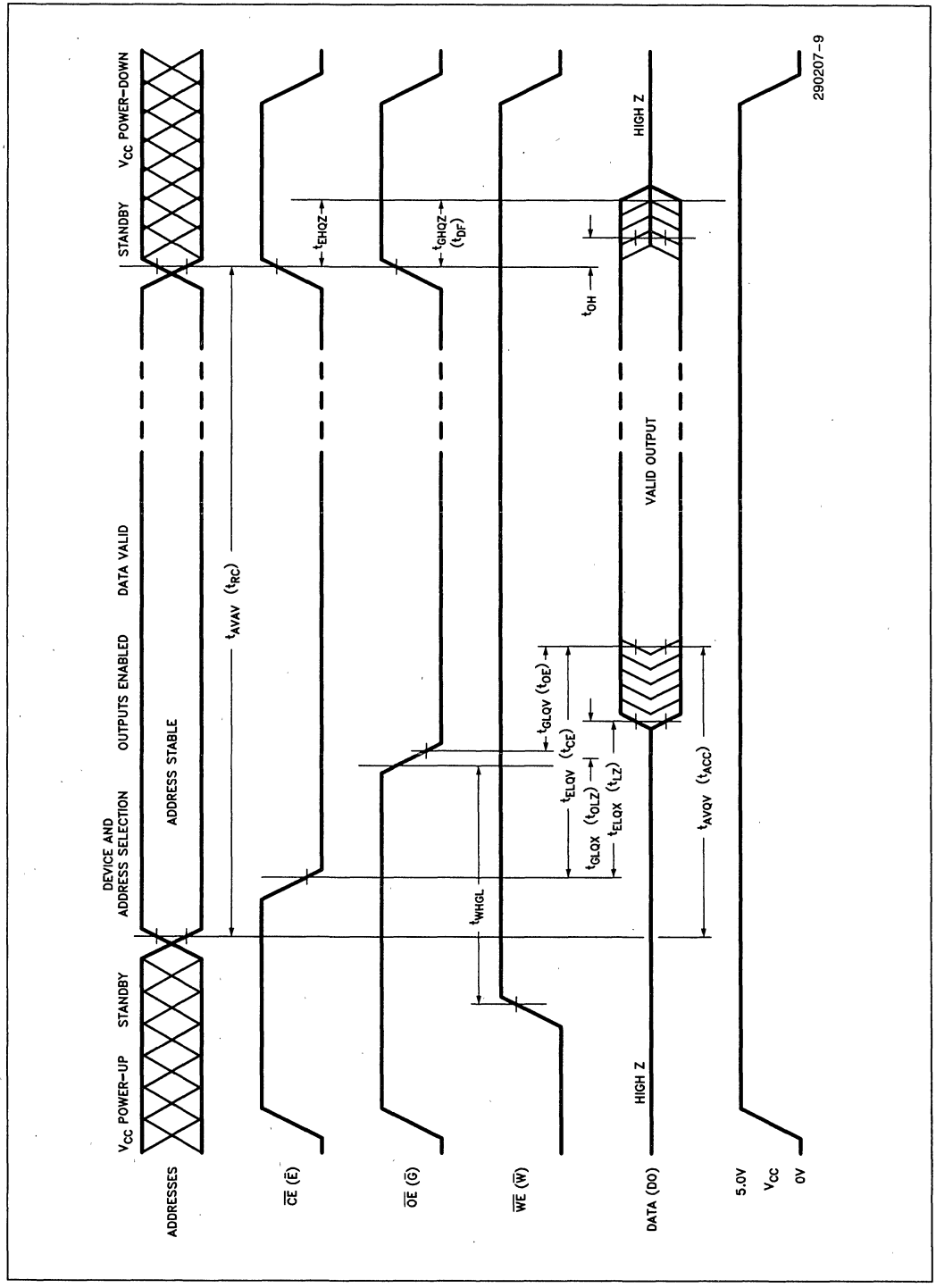


Figure 7. AC Waveforms for Read Operations

AC CHARACTERISTICS—Write/Erase/Program Operations[1, 2]

Versions		Notes	28F010-120		28F010-150		28F010-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		120		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time		0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		60		75		ns
t_{DVWH}/t_{DS}	Data Set-Up Time		50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		6		µs
t_{GHWL}	Read Recovery Time before Write		0		0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write		20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	2	60		60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		10		µs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		9.5		ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		1.0		µs

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

6

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits									Unit
		28F010-120			28F010-150			28F010-200			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		1.0	10		1.0	10		1.0	30	Sec
Chip Program Time	1, 2, 4		2	12.5		2	12.5		2	12.5	Sec
Erase/Program Cycles	1, 5	10,000	100,000		10,000	100,000		10,000	100,000		Cycles

NOTES:
1. "Typicals" are not guaranteed, but based on a limited number of samples from production lots. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time excluding system overhead is 16 µsec (10 µsec program + 6 µsec write recovery), while maximum is 400 µsec/byte (16 µsec x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX™ II Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

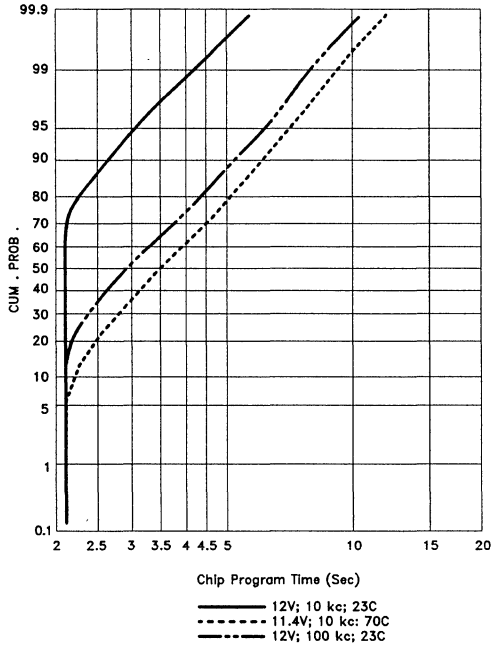


Figure 8. 28F010 Typical Programming Capability

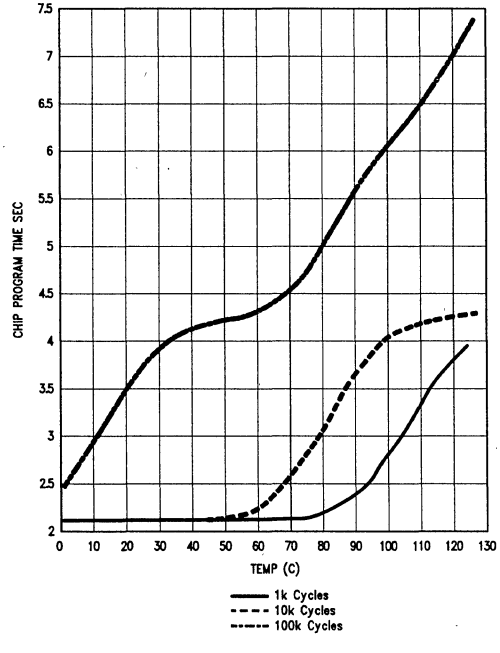


Figure 9. 28F010 Typical Program Time at 12V

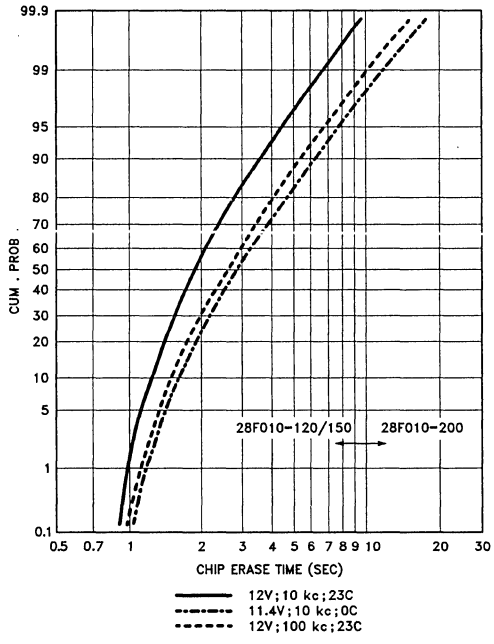


Figure 10. 28F010 Typical Erase Capability

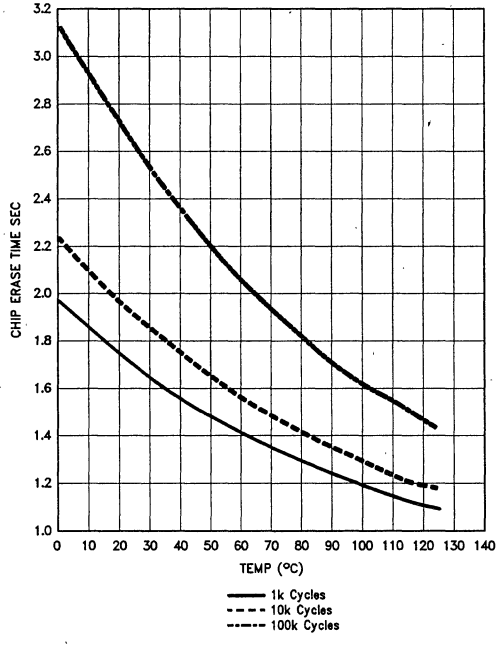


Figure 11. 28F010 Typical Erase Time at 12V

6

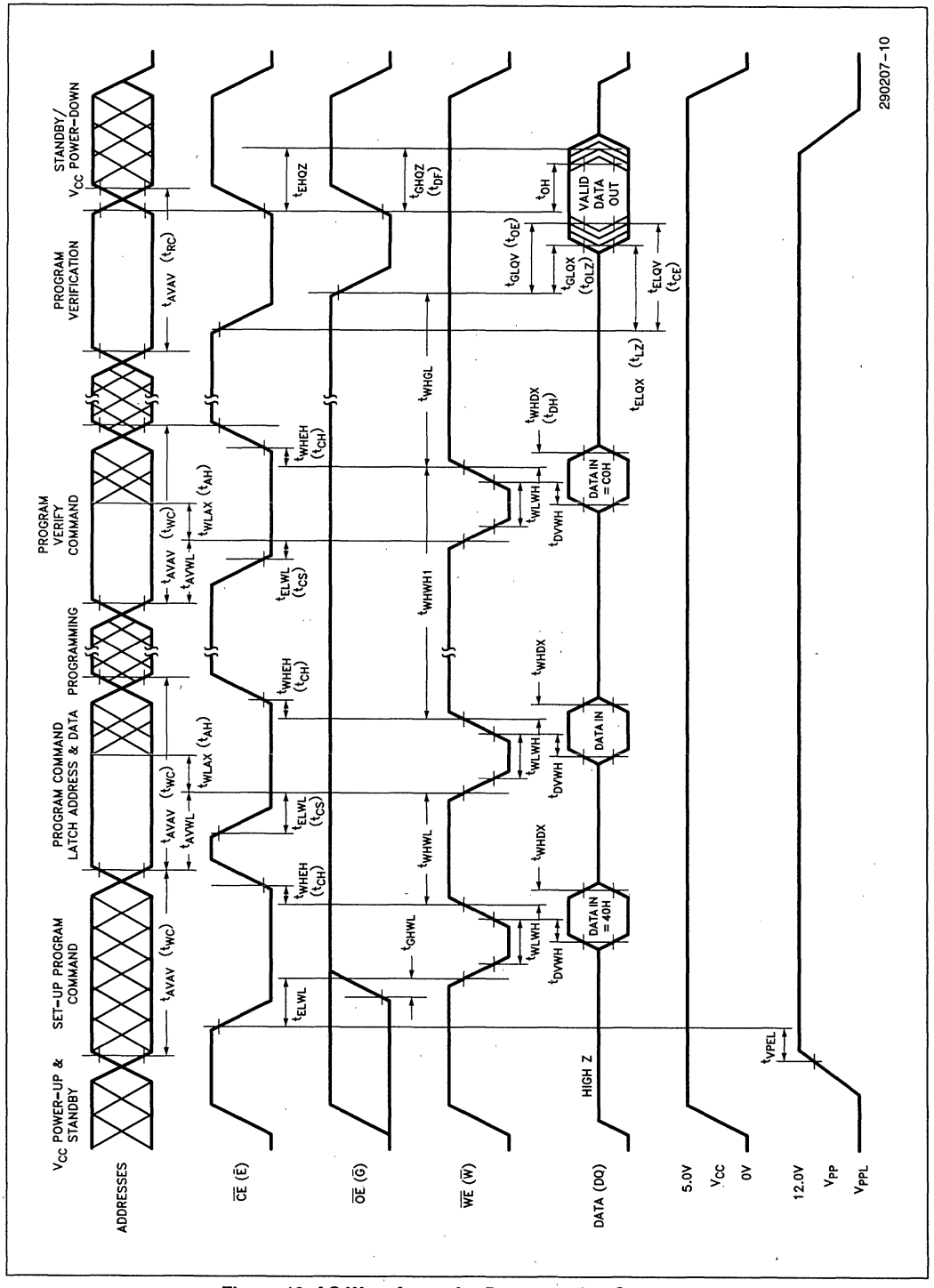


Figure 12. AC Waveforms for Programming Operations

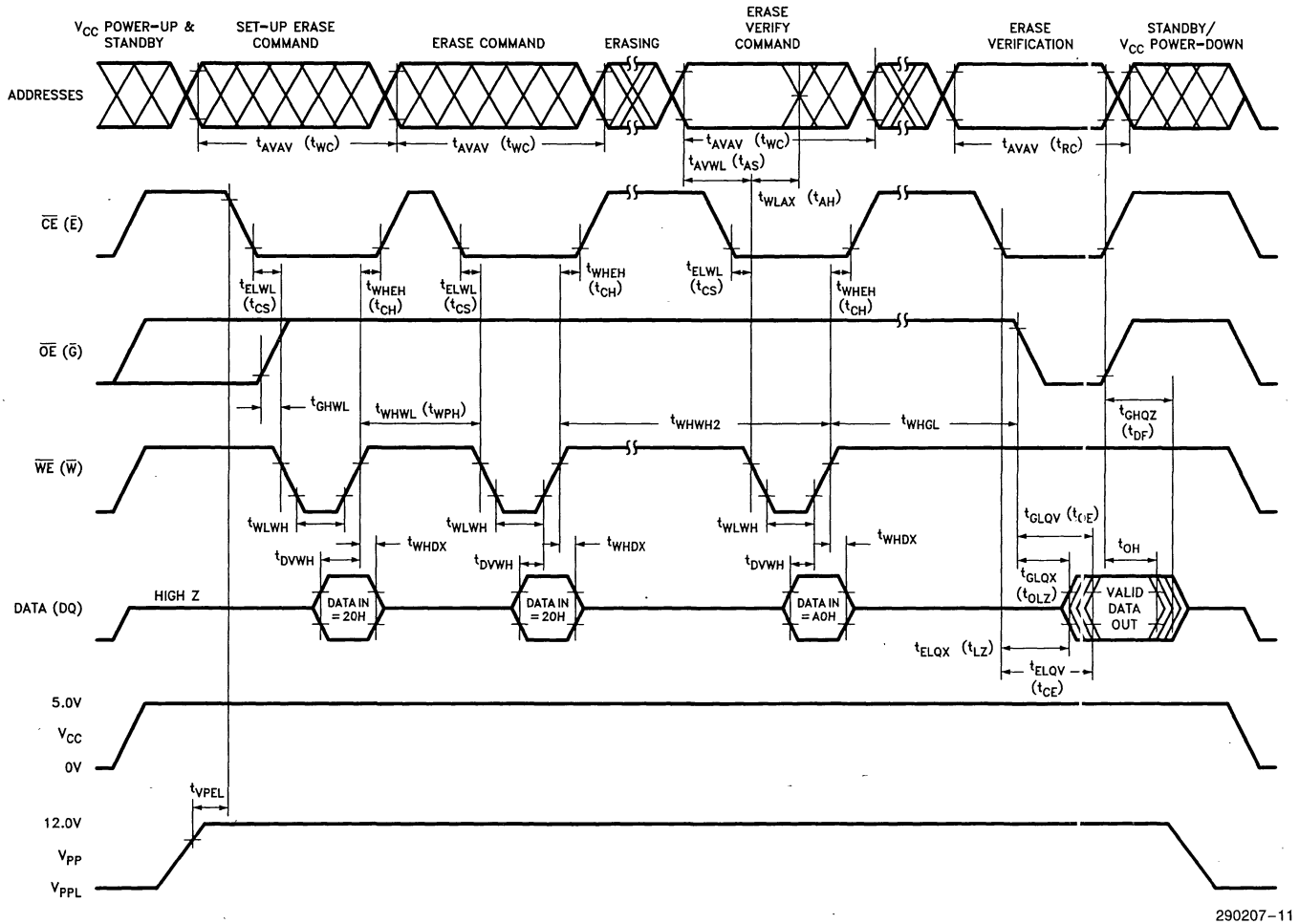
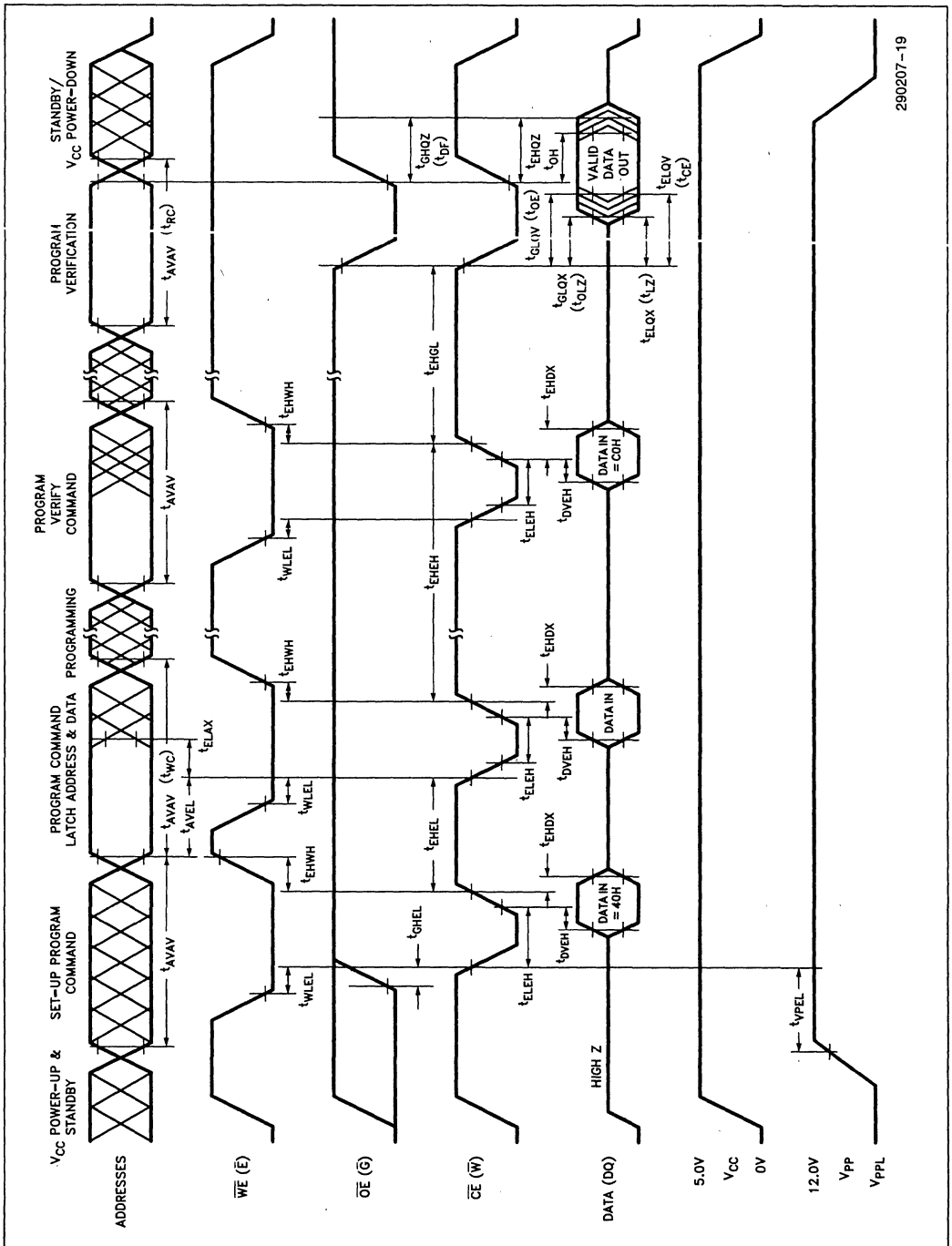


Figure 13. AC Waveforms for Erase Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Versions		Notes	28F010-120		28F010-150		28F010-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		120		150		200		ns
t_{AVEL}	Address Set-Up Time		0		0		0		ns
t_{ELAX}	Address Hold Time		80		80		95		ns
t_{DVEH}	Data Set-Up Time		50		50		50		ns
t_{EHDX}	Data Hold Time		10		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		6		μs
t_{GHEL}	Read Recovery Time before Write		0		0		0		μs
t_{WLEL}	Write Enable Set-Up Time before Chip Enable		0		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		70		80		ns
t_{EHEL}	Write Pulse Width High		20		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		1.0		μs

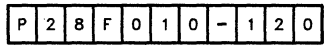
NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.



NOTE:
Alternative $\overline{CE}$-Controlled Write Timings also apply to erase operations.

Figure 14. Alternate AC Waveforms for Programming Operations

ORDERING INFORMATION



PACKAGE
P = 32-PIN PLASTIC DIP
N = 32-LEAD PLCC
E = STANDARD 32-LEAD TSOP
F = REVERSE 32-LEAD TSOP

ACCESS SPEED (ns)
120 ns
150 ns
200 ns

290207-20

VALID COMBINATIONS:

P28F010-120	N28F010-120
P28F010-150	N28F010-150
P28F010-200	N28F010-200
E28F010-120	F28F010-120
E28F010-150	F28F010-150
E28F010-200	F28F010-200

ADDITIONAL INFORMATION

		Order Number
ER-20,	"ETOX™ II Flash Memory Technology"	294005
ER-24,	"The Intel 28F010 Flash Memory"	294008
RR-60,	"ETOX™ II Flash Memory Reliability Data Summary"	293002
AP-316,	"Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
AP-325	"Guide to Flash Memory Reprogramming"	292059

28F020
2048K (256K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **2 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **10 μs Typical Byte-Program**
  - **4 Second Chip-Program**
- **10,000 Erase/Program Cycles Minimum**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **150 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0 Watts Data Retention Power**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ II Nonvolatile Flash Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **JEDEC-Standard Pinouts**
  - **32-Pin Plastic Dip**
  - **32-Lead PLCC**
  - **32-Lead TSOP**
- **Integrated Program/Erase Stop Timer**

(See Packaging Spec., Order #231369)

Intel's 28F020 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F020 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F020 increases memory flexibility, while contributing to time- and cost-savings.

The 28F020 is a 2048-kilobit nonvolatile memory organized as 262,144 bytes of 8 bits. Intel's 28F020 is offered in 32-pin plastic DIP, 32-lead PLCC, and 32-lead TSOP packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX™ II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F020 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F020 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 150 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX II process base, the 28F020 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

November 1990
Order Number: 290245-003

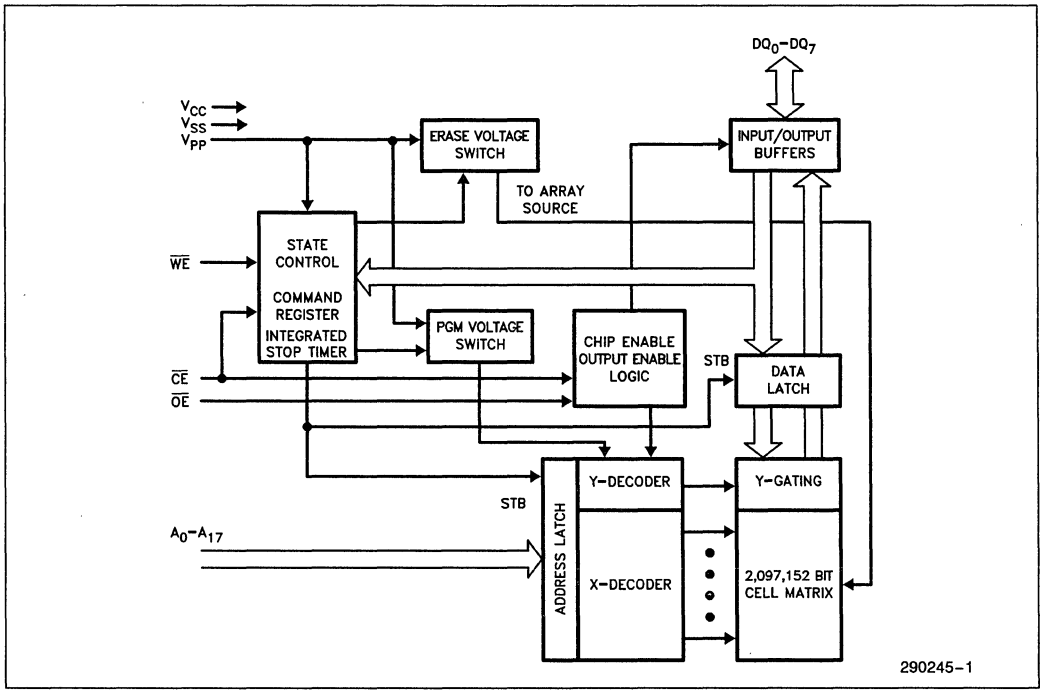
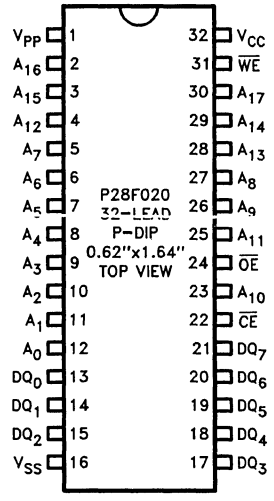


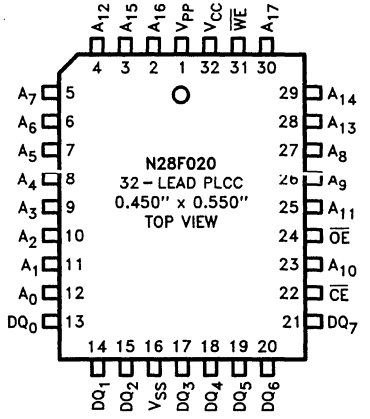
Figure 1. 28F020 Block Diagram

Table 1. Pin Description

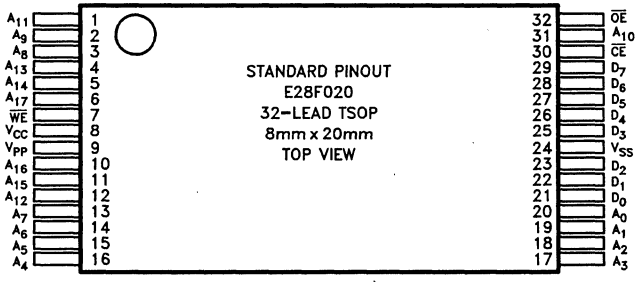
Symbol	Type	Name and Function
A_0–A_{17}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ±10%)
V_{SS}		**GROUND**



290245-2



290245-3



290245-4

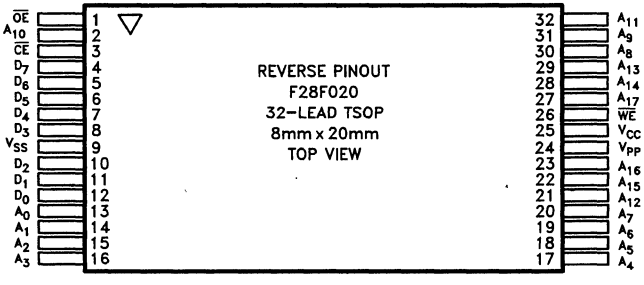


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Figure 2. 28F020 Pin Configurations

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APPLICATIONS

The 28F020 flash memory provides nonvolatility along with the capability to typically perform over 100,000 electrical chip-erasure/reprogram cycles. These features make the 28F020 an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and datatables are required, the 28F020's reprogrammability and nonvolatility make it the obvious and ideal replacement for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-to-DRAM download process. This results in dramatic enhancement of performance and substantial reduction of power consumption — a consideration particularly important in portable equipment. Flash memory increases flexibility with electrical chip erasure and in-system update capability of operating systems and application code. With updatable BIOS, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems are instant-on. Reliability exceeds that of electromechanical media. Often in these environments, power interruptions force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, the 28F020 flash memory offers a solid state alternative in a minimal form factor. The 28F020 provides higher performance, lower power consumption, instant-on capability, and allows an "execute in place" memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life — from prototyping to system manufacture to after-sale service. The electrical chip-erasure and reprogramming ability of the 28F020 allows in-circuit alterability; this eliminates unnecessary handling and less-reliable socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system integration — the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F020, code updates are implemented locally via an edge-connector, or remotely over a communcations link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate".

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F020s tied to the 80C186 system bus. The 28F020's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

The outstanding feature of the TSOP (Thin Small Outline Package) is the 1.2 mm thickness. With standard and reverse pin configurations, TSOP reduces the number of board layers and overall volume necessary to layout multiple 28F020s. TSOP is particularly suited for portable equipment and applications requiring large amounts of flash memory. Figure 4 illustrates the TSOP Serpentine layout.

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F020 offers advantages to the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straight-forward interfacing, and in-circuit alterability offers designers unlimited flexibility to meet the high standards of today's designs.

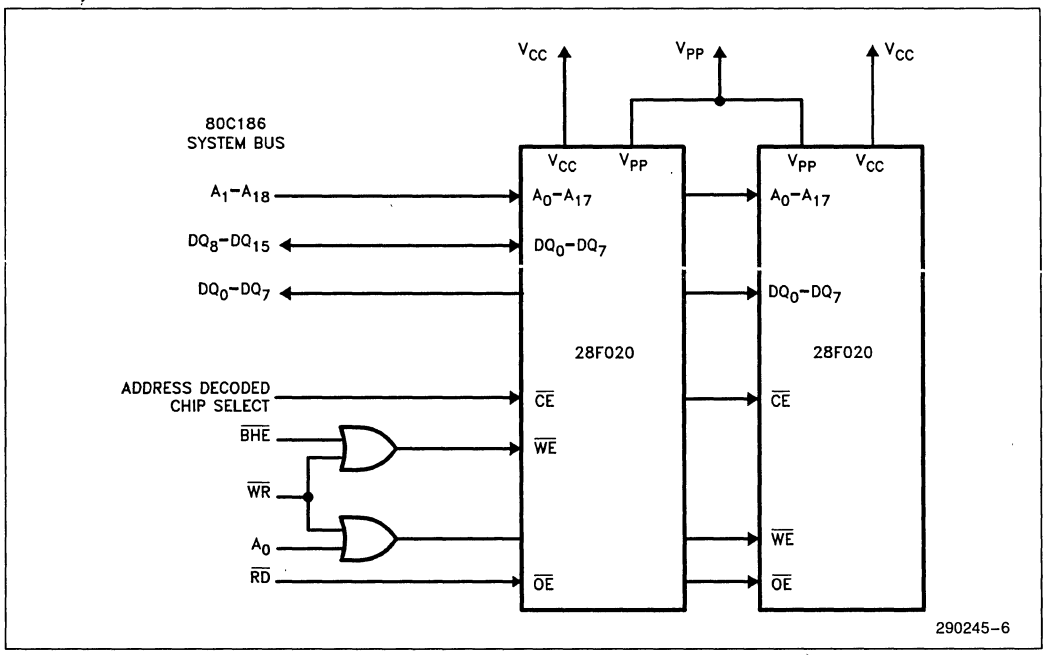

Figure 3. 28F020 in a 80C186 System

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F020 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F020 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

Integrated Stop Timer

Successive command write cycles define the durations of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the 28F020 a read-only memory. In this mode, the memory contents cannot be altered.

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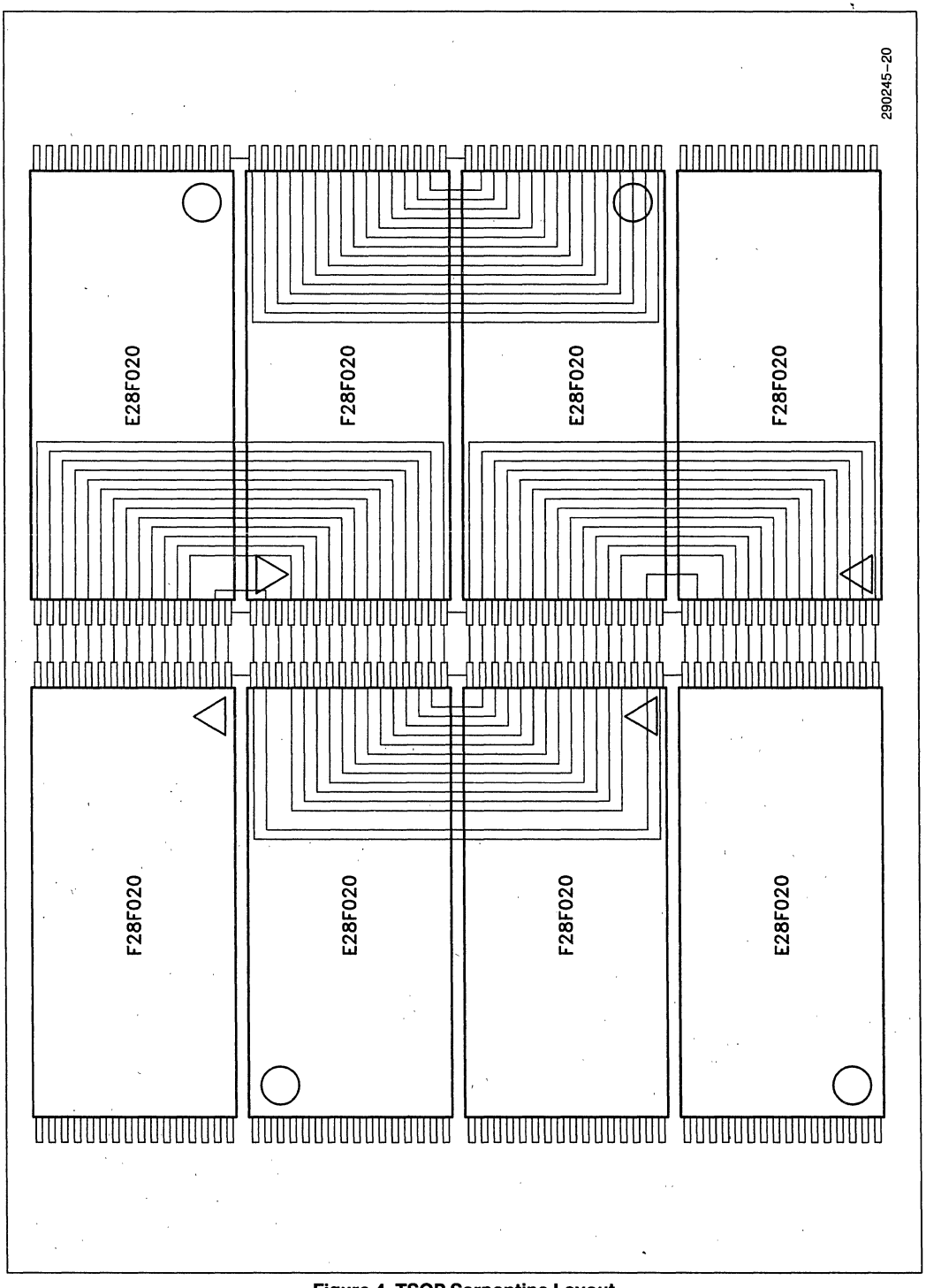

Figure 4. TSOP Serpentine Layout

Table 2. 28F020 Bus Operations

Operation	Pins	V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	int$_c$ligent Identifier™ (Mfr)(2)	V_{PPI}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	int$_e$ligent Identifier™ (Device)(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = BDH
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In(6)

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the int$_e$ligent Identifier high voltage. Refer to DC Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the int$_e$ligent Identifier™ codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection.) The 28F020 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F020 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to AC read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the int$_e$ligent Identifier™ codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can **only** access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F020's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F020 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

int$_e$ligent Identifier™ Operation

The int$_e$ligent Identifier operation outputs the manufacturer code (89H) and device code (BDH). Programming equipment automatically matches the device with its proper erase and programming algorithms.

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With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F020 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (BDH).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F020 register commands.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read int$_e$ligent Identifier™ Codes(4)	3	Write	X	90H	Read	(4)	(4)
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = BDH).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read int$_e$ligent ID command, two read operations access manufacturer and device codes.
5. Figure 6 illustrates the Quick-Erase™ Algorithm.
6. Figure 5 illustrates the Quick-Pulse Programming™ Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F020, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

inteligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F020 contains an inteligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of BDH. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F020 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 6, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F020. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F020 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F020 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 5, the 28F020 Quick-Pulse Programming™ algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The 28F020 is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming™ and Quick-Erase™ algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further information, see Reliability Report RR-60.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 5 illustrates the Quick-Pulse Programming algorithm.

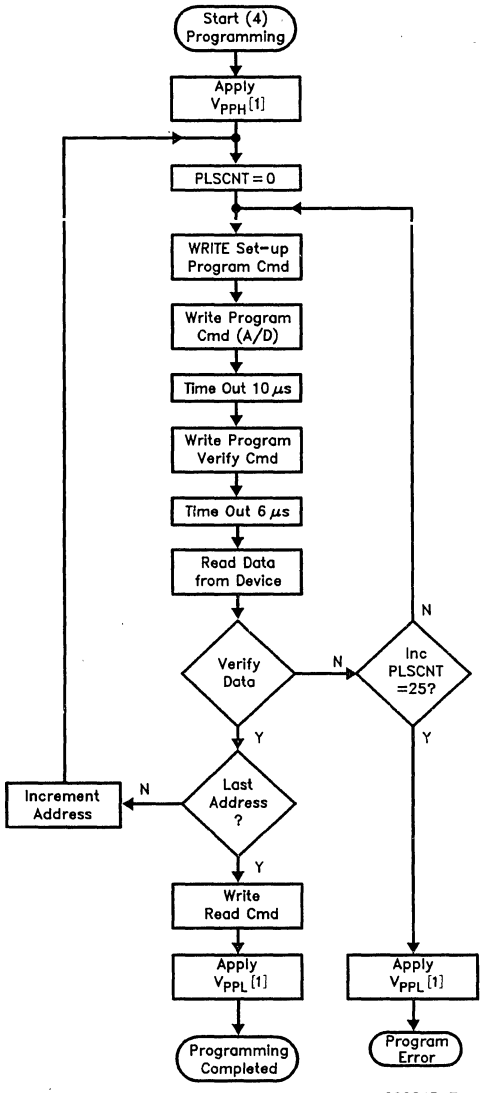
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately four seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in two seconds. Figure 6 illustrates the Quick-Erase algorithm.



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Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. 28F020 Quick-Pulse Programming™ Algorithm

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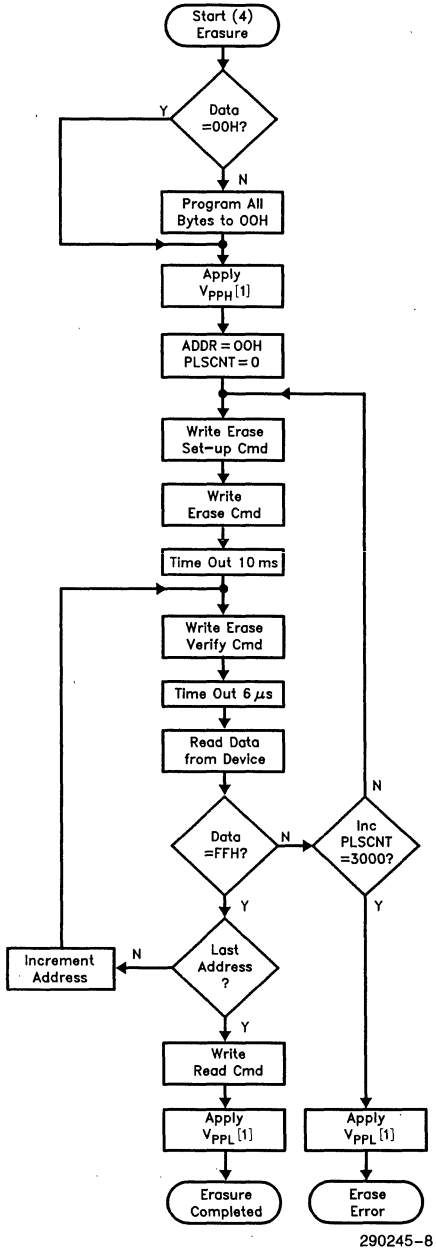

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Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase(2) Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation(3)
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. Refer to principles of operation.
4. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 6. 28F020 Quick-Erase™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The 28F020 is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F020 is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. **Power supply sequencing is not required.** Internal circuitry in the 28F020 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

28F020 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the 28F020 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 28F020.

Table 4. 28F020 Typical Update Power Dissipation(4)

Operation	Notes	Power Dissipation (Watt-Seconds)
Array Program/Program Verify	1	0.34
Array Erase/Erase Verify	2	0.37
One Complete Cycle	3	1.05

NOTES:
1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulse (t_{WHWH1} × I_{PP2} typical + t_{WHGL} × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{CC2} typical + t_{WHGL} × I_{CC4} typical)].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{PP} (I_{PP3} typical × t_{ERASE} typical + I_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC} (I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed but based on a limited number of samples from production lots.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(1)
During Erase/Program .....0°C to +70°C
Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
Voltage on Any Pin with
Respect to Ground .....−2.0V to +7.0V(2)
Voltage on Pin A_9 with
Respect to Ground .....−2.0V to +13.5V(2, 3)
V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program ....−2.0V to +14.0V(2, 3)
V_{CC} Supply Voltage with
Respect to Ground .....−2.0V to +7.0V(2)
Output Short Circuit Current.....100 mA(4)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1			1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1, 2			±10	µA	$V_{PP} \leq V_{CC}$

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{PP1}	V_{PP} Read Current, ID Current or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		10	30	mA	$V_{PP} = V_{PPH}$
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage		11.50		13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current	1		90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		50	100	μA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC}$ ±0.2V
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress

6

DC CHARACTERISTICS—CMOS COMPATIBLE (Continued)

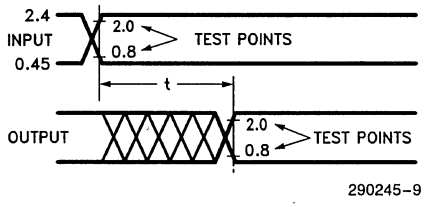
Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I_{PPS}	V_{PP} Leakage Current	1			±10	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8	30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		10	30	mA	$V_{PP} = V_{PPH}$, Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$, Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		0.85 V_{CC}			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}			V_{CC} − 0.4				I_{OH} = −100 μA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage		11.50		13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current	1		90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Programs are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN}	Address/Control Capacitance	3		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	3		12	pF	V_{OUT} = 0V

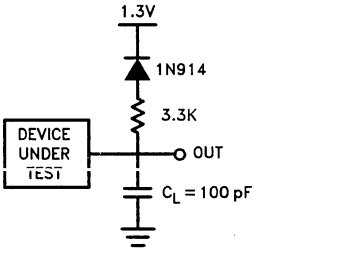
NOTES for DC Characteristics and Capacitance:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).
2. Not 100% tested: Characterization data available.
3. Sampled, not 100% tested.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

AC TESTING INPUT/OUTPUT WAVEFORM



AC Testing: Inputs are driven at 2.4 for a logic "1" and 0.45 for a logic "0". Testing measurements are made at 2.0 for a logic "1" and 0.8 for a logic "0". Rise/Fall time ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45 and 2.4
Input Timing Reference Level . . . . . 0.8 and 2.0
Output Timing Reference Level . . . . . 0.8 and 2.0

AC CHARACTERISTICS—Read-Only Operations(2)

Versions		Notes	28F020-150		28F020-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	3	150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time			150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	3	0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	3		55		55	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	3	0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	4		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change(1)	3	0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.
3. Not 100% Tested: Characterization Data Available.
4. Guaranteed by Design.

6

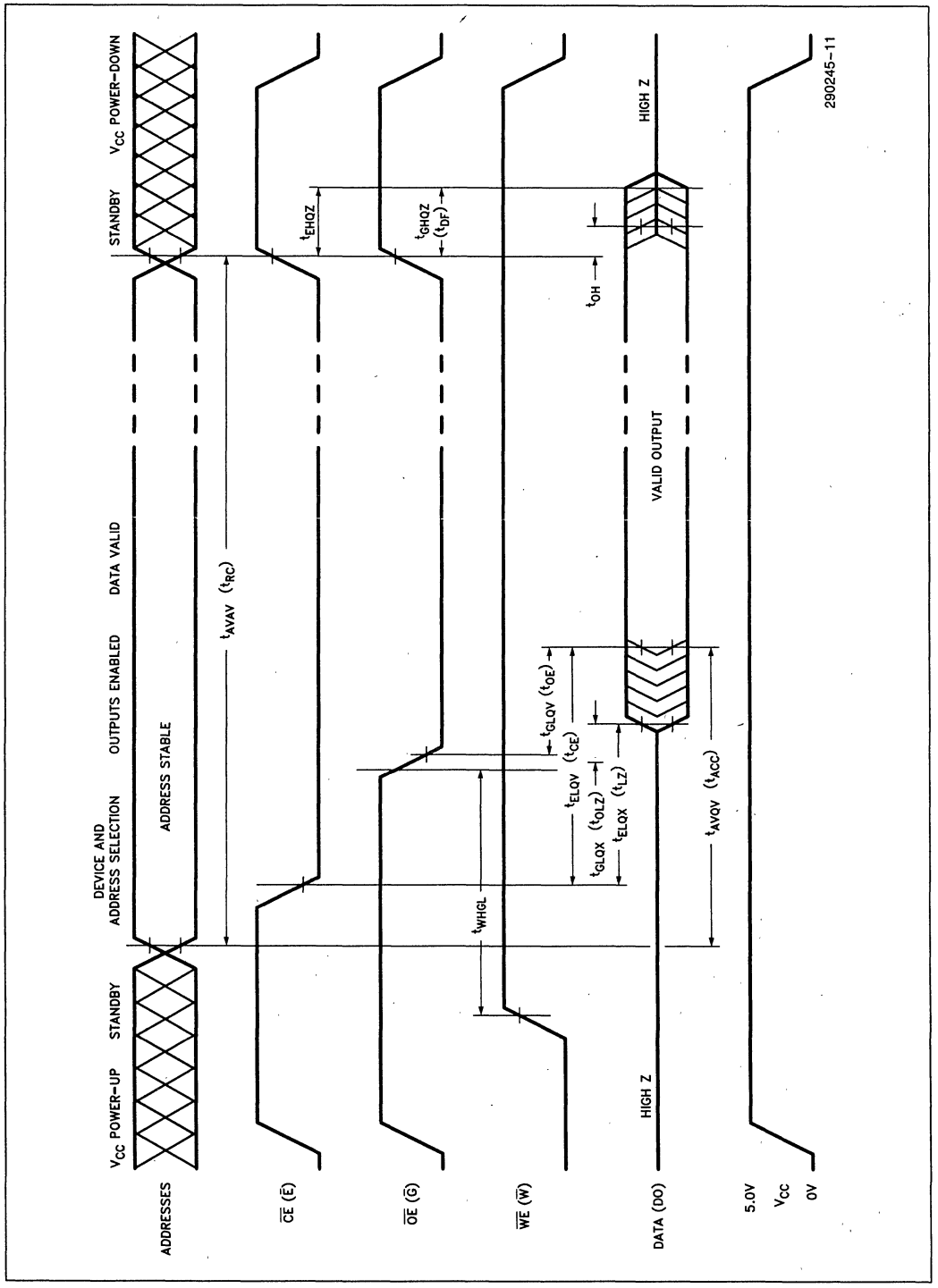


Figure 7. AC Waveforms for Read Operations

AC CHARACTERISTICS—Write/Erase/Program Operations(1, 2)

Versions		Notes	28F020-150		28F020-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		75		ns
t_{DVWH}/t_{DS}	Data Set-Up Time		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		μs
t_{GHWL}	Read Recovery Time before Write		0		0		μs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	2	60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		μs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		μs

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

6

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits						Unit
		28F020-150			28F020-200			
		Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		2	30		2	30	Sec
Chip Program Time	1, 2, 4		4	25		4	25	Sec
Erase/Program Cycles		10,000	100,0001, 5		10,000	100,000		Cycles

NOTES:
1. "Typicals" are not guaranteed, but based on a limited number of samples from production lots. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time excluding system overhead is 16 μsec (10 μsec program + 6 μsec write recovery), while maximum is 400 μsec/byte (16 μsec x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX™ II Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

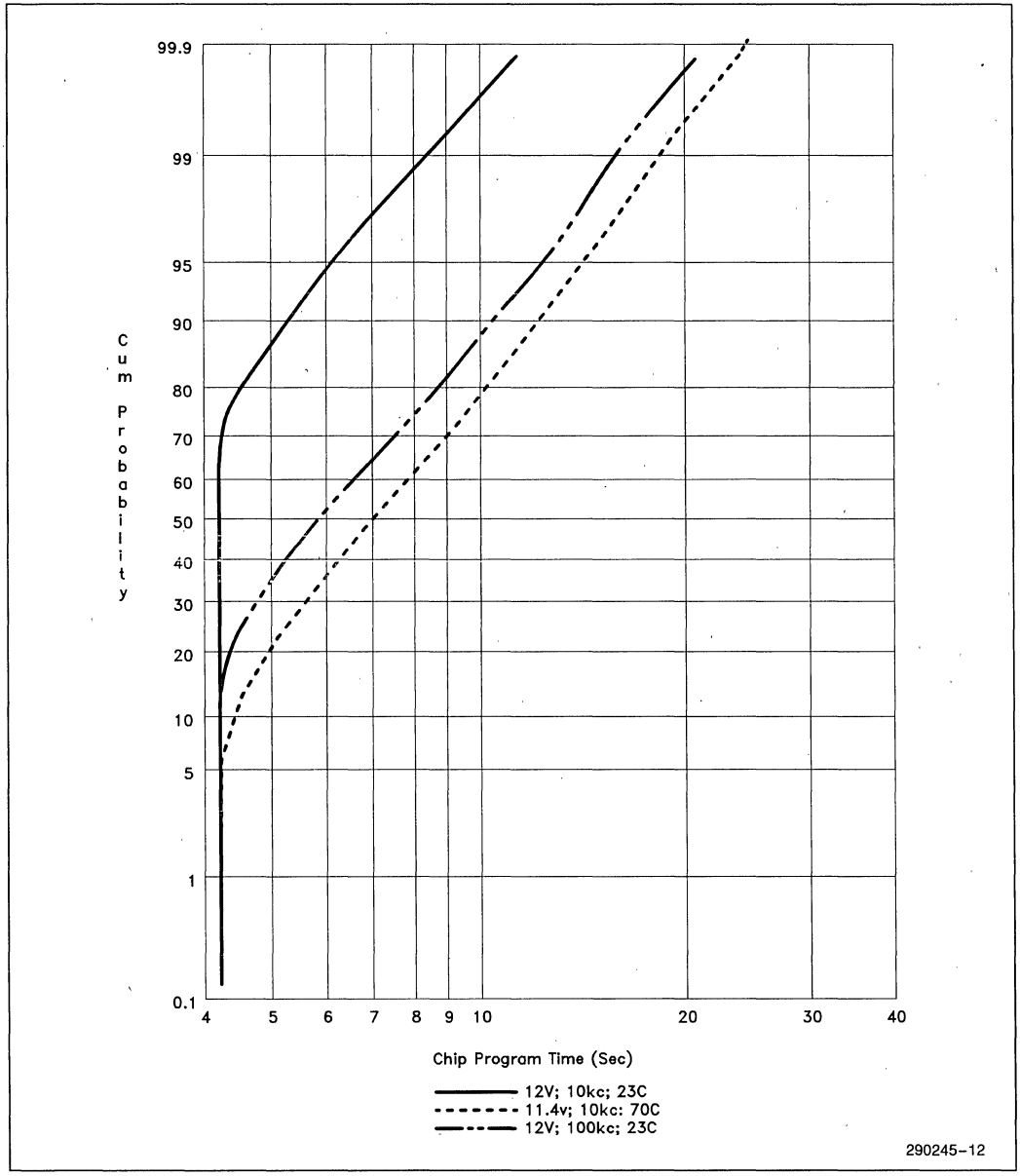


Figure 8. 28F020 Typical Programming Capability

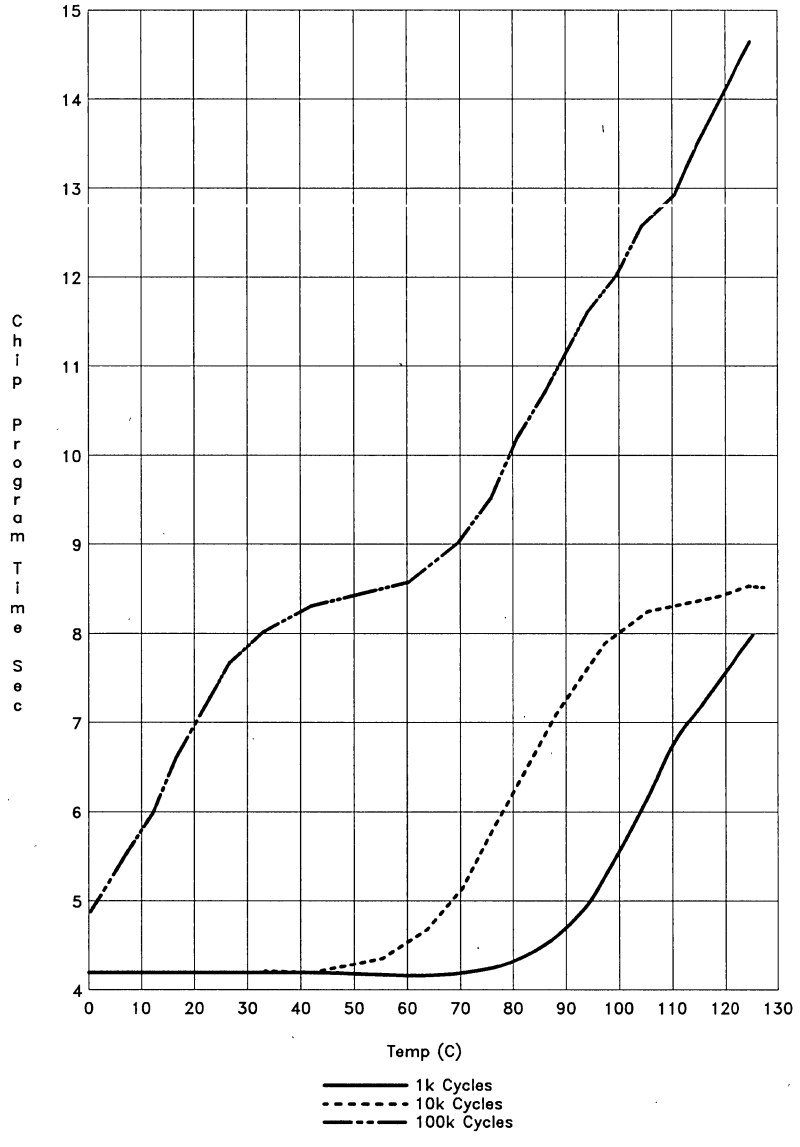
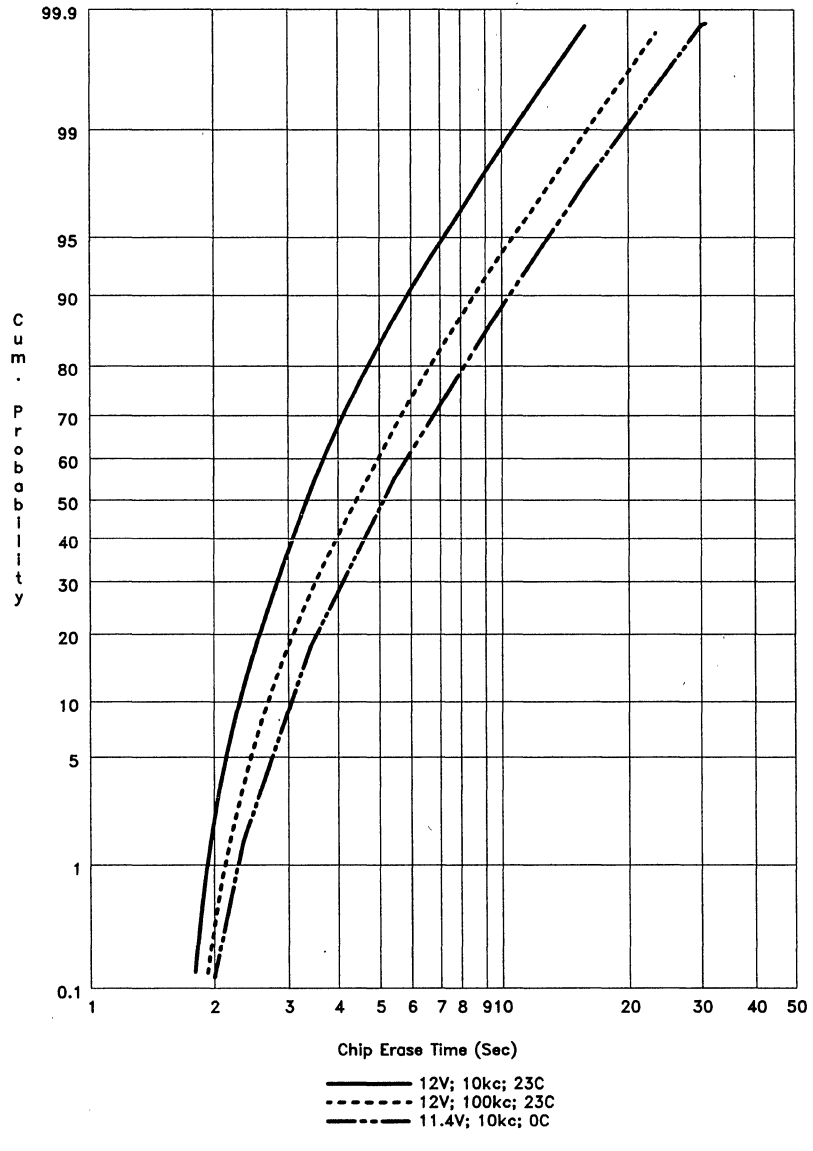
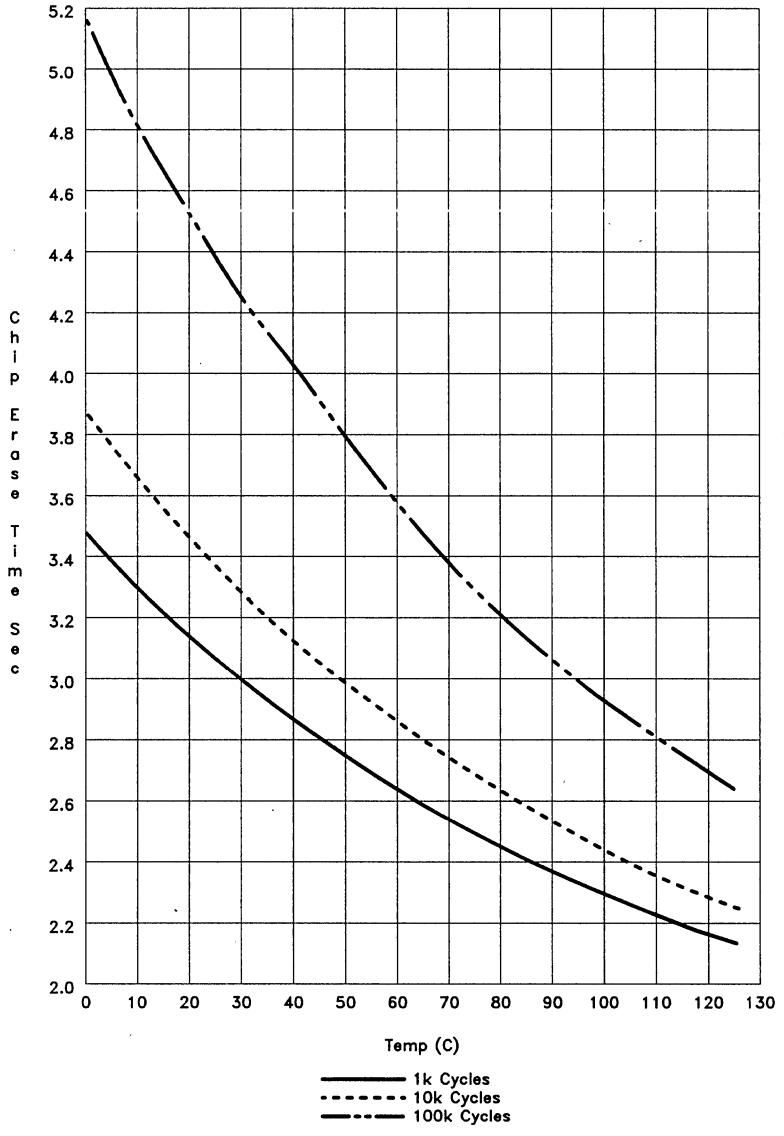


Figure 9. 28F020 Typical Program Time at 12V



NOTE:
Does not include Pre-Erase Program.

Figure 10. 28F020 Typical Erase Capability



NOTE:
Does not include Pre-Erase Program.

Figure 11. 28F020 Typical Erase Time at 12.0V

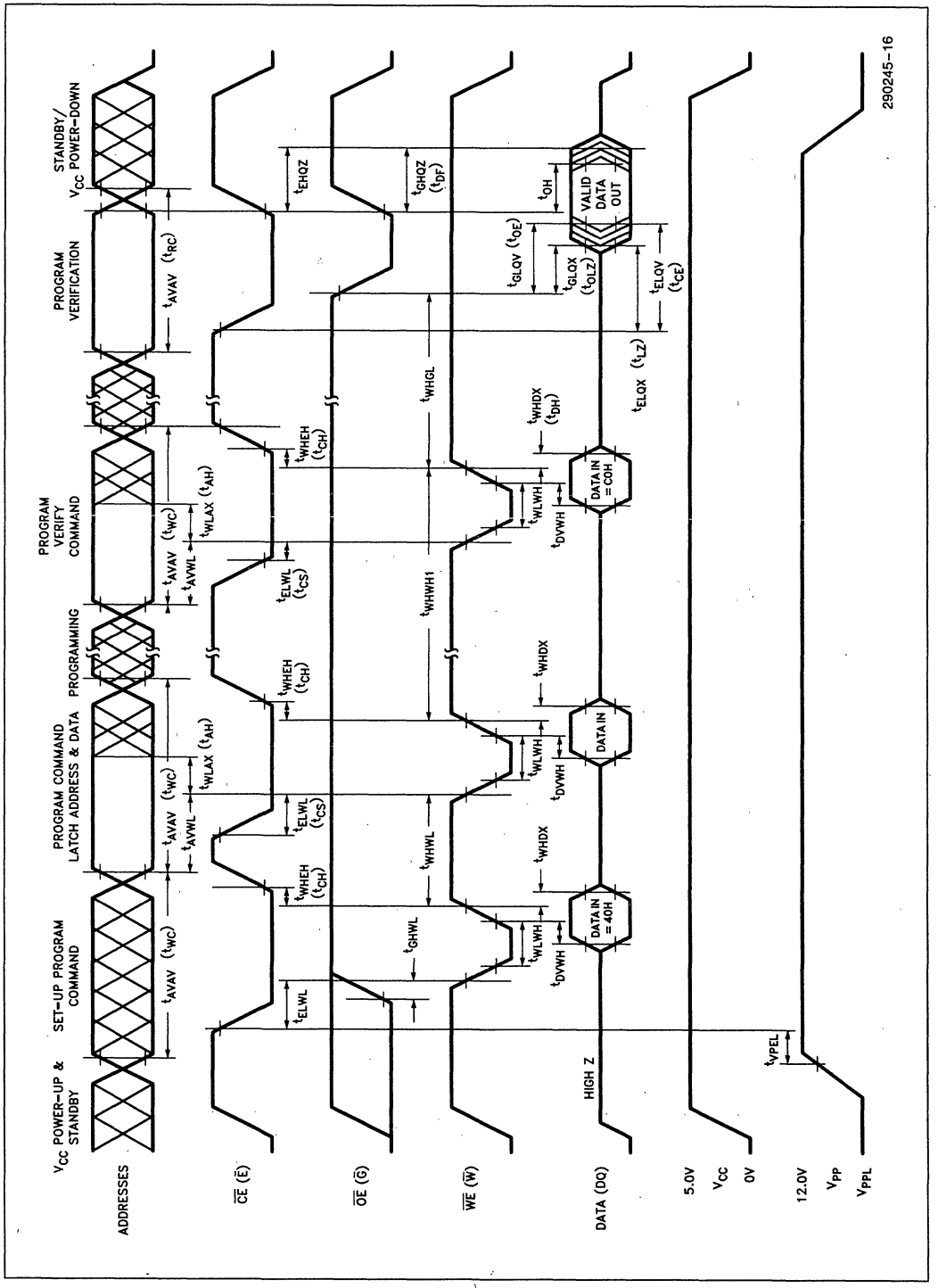


Figure 12. AC Waveforms for Programming Operations

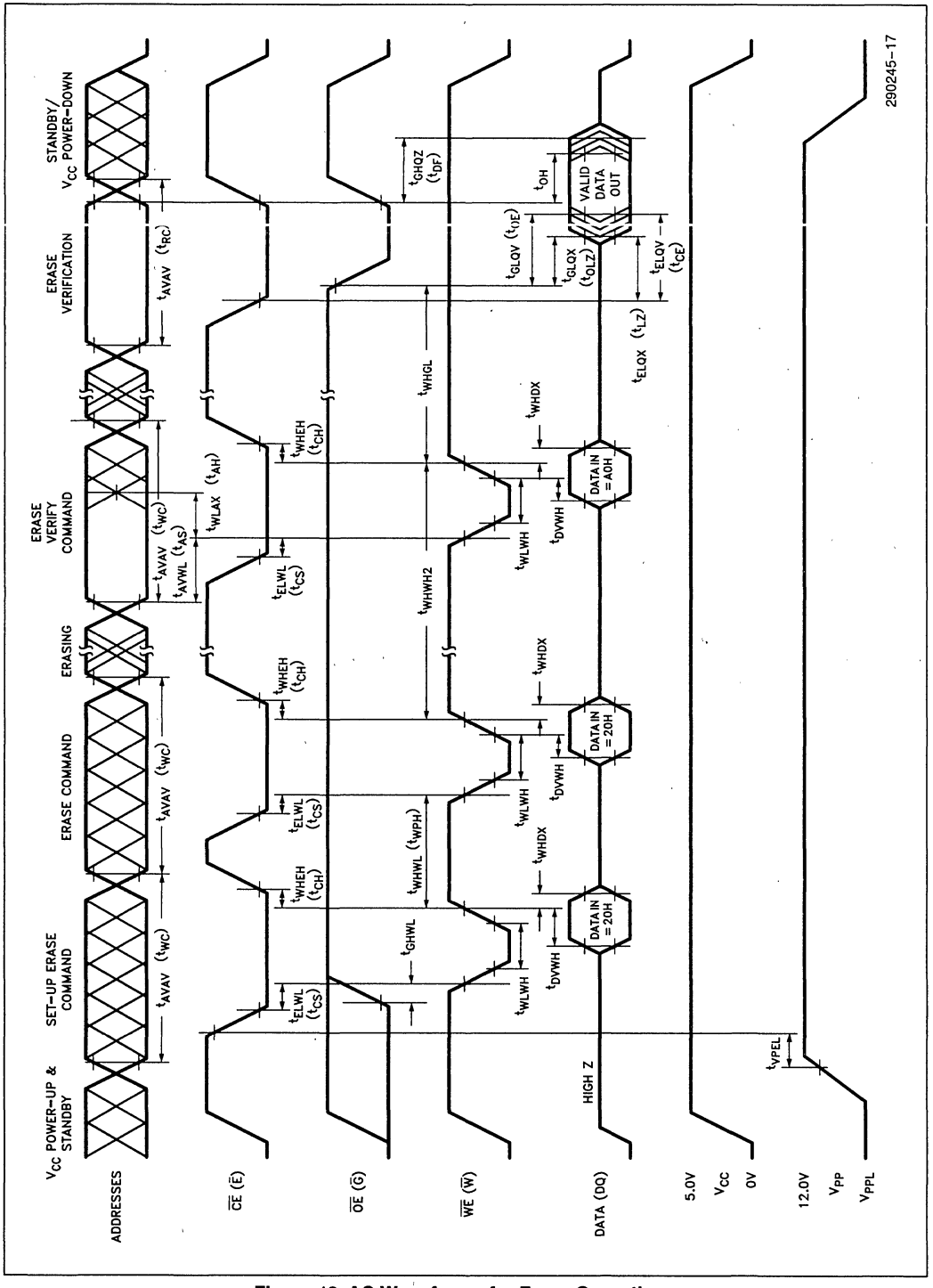
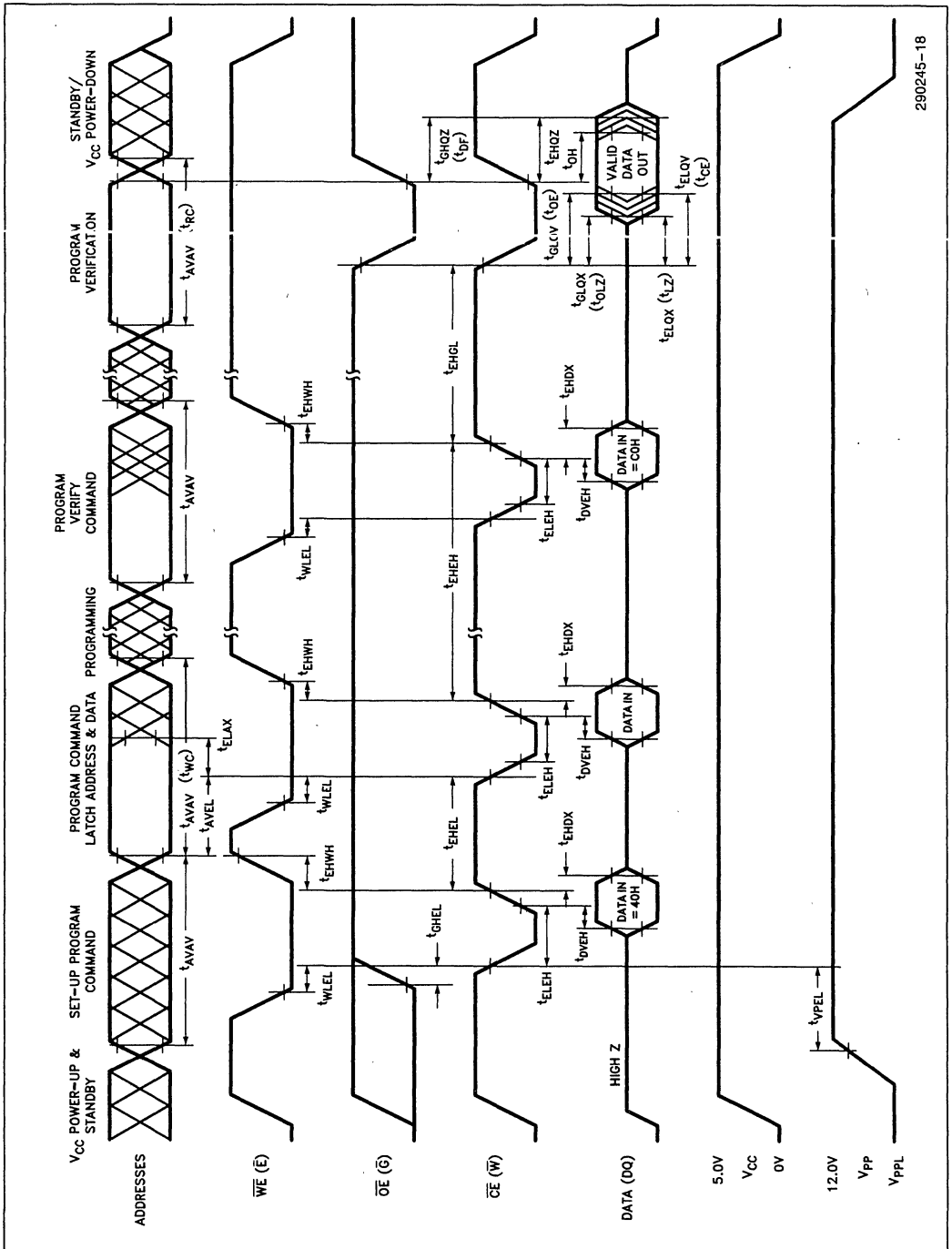


Figure 13. AC Waveforms for Erase Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Versions		Notes	28F020-150		28F020-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		150		200		ns
t_{AVEL}	Address Set-Up Time		0		0		ns
t_{ELAX}	Address Hold Time		80		95		ns
t_{DVEH}	Data Set-Up Time		50		50		ns
t_{EHDX}	Data Hold Time		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		µs
t_{GHEL}	Read Recovery Time before Write		0		0		µs
t_{WLEL}	Write Enable Set-Up Time before Chip Enable		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		80		ns
t_{EHEL}	Write Pulse Width High		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		µs

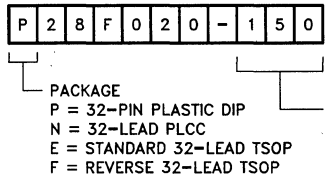
NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.



NOTE:
Alternative $\overline{CE}$-Controlled Write Timings also apply to erase operations.

Figure 14. Alternate AC Waveforms for Programming Operations

ORDERING INFORMATION



290245-19

VALID COMBINATIONS:

P28F020-150	N28F020-150
P28F020-200	N28F020-200
E28F020-150	F28F020-150
E28F020-200	F28F020-200

ADDITIONAL INFORMATION

		Order Number
ER-20,	"ETOX™ II Flash Memory Technology"	294005
ER-24,	"The Intel 28F020 Flash Memory"	294008
RR-60,	"ETOX™ II Flash Memory Reliability Data Summary"	293002
AP-316,	"Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
AP-325	"Guide to Flash Memory Reprogramming"	292059

iSM001FLKA
1 MBYTE (512K x 16) CMOS FLASH SIMM

- **High-Performance**
  - **— 120 ns Maximum Access Time**
  - **— 16.67 MB/s Read Transfer Rate**
- **10,000 Rewrite Cycles Minimum/ Component**
- **Flash Electrical Chip-Erase**
  - **— 1 Second Typical Chip-Erase**
- **16 μs Typical Word Write**
  - **— Up to 1 Mb/s Write Transfer Rate**
- **Inherent Non-volatility**
  - **— No Batteries or Disk Required for Back-up**
  - **— 0W Data Retention Power**
- **CMOS Low Power Consumption**
  - **— 20.3 mA Typical Active Current**
  - **— 0.4 mA Typical Standby Current**
- **Standard 80-Pin Insertable Module**
  - **— 0.050 Centerline Lead Spacing**
  - **— Upgrade Path through 128M bytes**
- **Hardware Presence Detect**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **— $\pm$10% V_{CC} Tolerance**
  - **— Maximum Latch-Up Immunity Through EPI Processing**
- **12.0V $\pm$5% V_{PP}**
- **Integrated Program/Erase Stop Timer**
- **ETOX™ II Nonvolatile Flash Technology**
  - **— High-Volume Manufacturing Experience**

Intel's iSM001FLKA flash SIMM (Single In-Line Memory Module) is targeted at high-density read/write nonvolatile memory. The iSM001FLKA enables you to optimize board space; to offer incremental memory expansion similar to today's DRAM; and to assure continued access to today's and tomorrow's surface-mount technologies. Intel's iSM001FLKA offers a reliable sold-state alternative for mass storage. The flash memory module is also ideal for high performance code and data storage as well as data recording and accumulation.

The iSM001FLKA, composed of eight 1 Mb flash memories in plastic leaded chip carrier (N28F010), is organized as 524,288 words of 16 bits. The PLCCs are mounted, four to a side, together with 0.1 μF decoupling capacitors on an 80-pin standard, low-profile module.

Extended erase and program cycling capability is designed into Intel's ETOX™ II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional nonvolatile memory.

Intel's iSM001FLKA flash SIMM employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 ns access time provides no WAIT state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 0.8 mA translates into power savings when the memory module is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from -1V to V_{CC} + 1V.

November 1990
Order Number: 290244-004

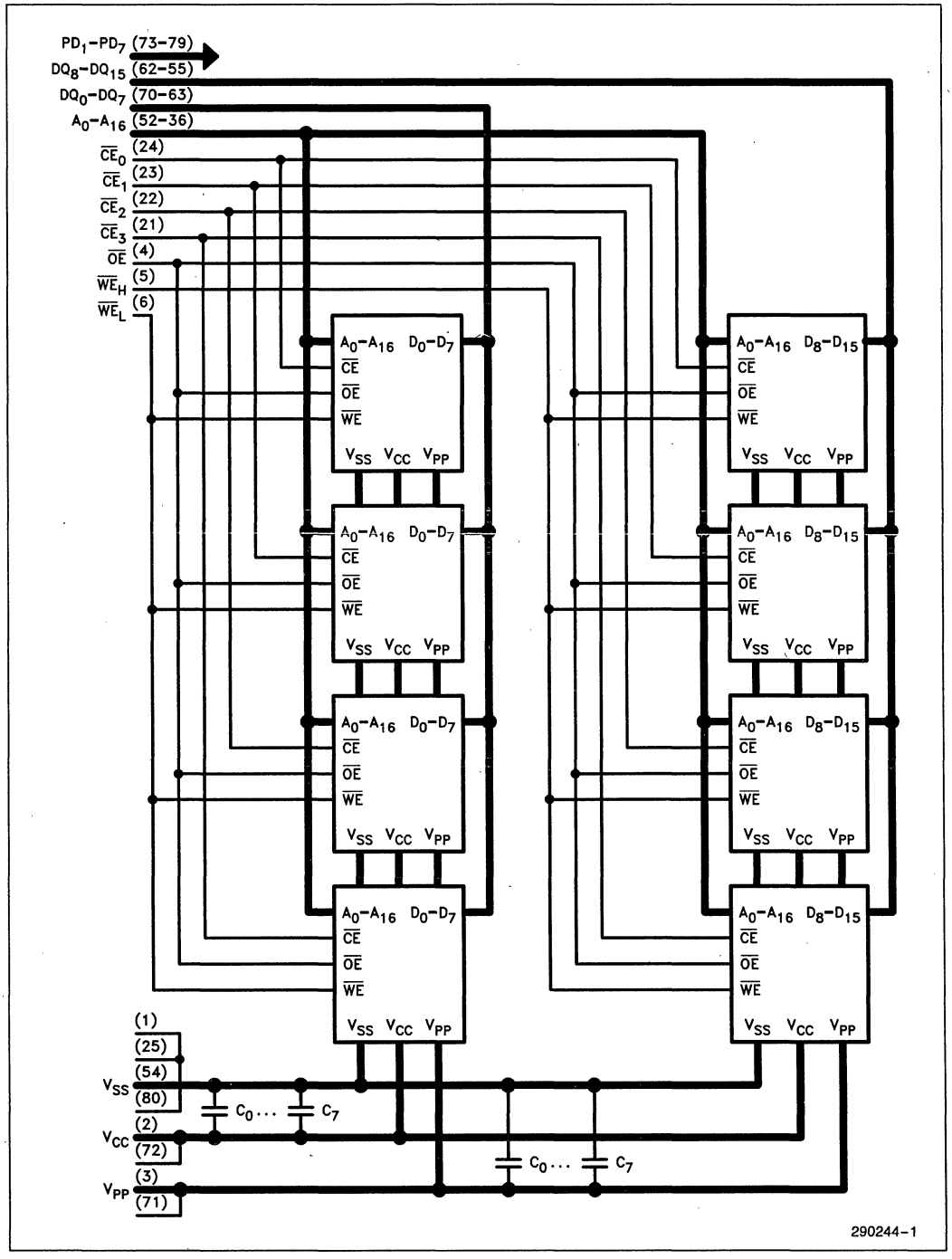


Figure 1. iSM001FLKA Functional Block Diagram

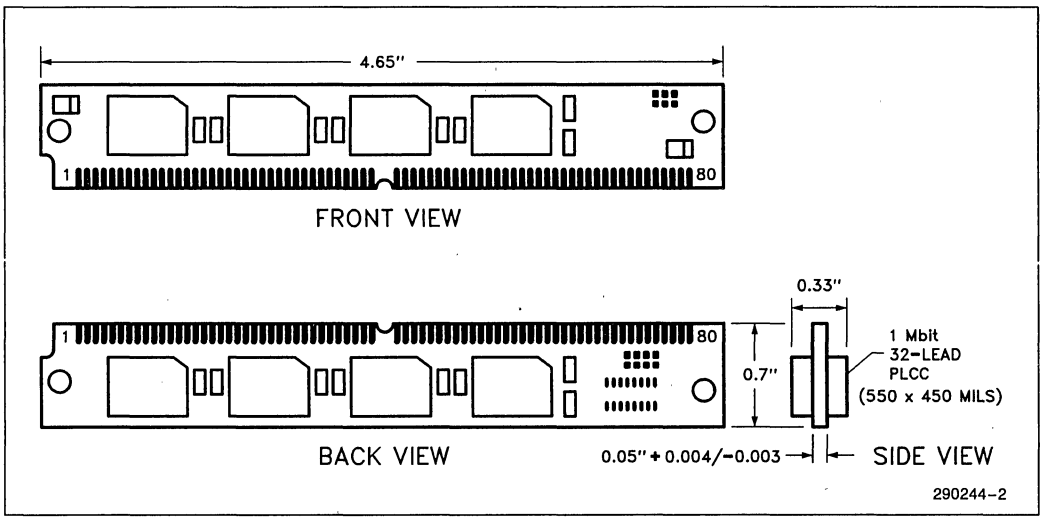


Figure 2. iSM001FLKA Pin Configurations

Table 1. Pinout

1	V_{SS}	21	$\overline{CE3}$	41	A_{11}	61	DQ_9
2	V_{CC}	22	$\overline{CE2}$	42	A_{10}	62	DQ_8
3	V_{PP}	23	$\overline{CE1}$	43	A_9	63	DQ_7
4	$\overline{OE}$	24	$\overline{CE0}$	44	A_8	64	DQ_6
5	$\overline{WEH}$	25	V_{SS}	45	A_7	65	DQ_5
6	$\overline{WEL}$	26	RES	46	A_6	66	DQ_4
7	NC	27	RES	47	A_5	67	DQ_3
8	RES	28	RES	48	A_4	68	DQ_2
9	RES	29	RES	49	A_3	69	DQ_1
10	RES	30	NC	50	A_2	70	DQ_0
11	RES	31	NC	51	A_1	71	V_{PP}
12	RES	32	NC	52	A_0	72	V_{CC}
13	RES	33	NC	53	RES	73	PD_1
14	RES	34	NC	54	V_{SS}	74	PD_2
15	RES	35	NC	55	DQ_{15}	75	PD_3
16	RES	36	A_{16}	56	DQ_{14}	76	PD_4
17	NC	37	A_{15}	57	DQ_{13}	77	PD_5
18	NC	38	A_{14}	58	DQ_{12}	78	PD_6
19	NC	39	A_{13}	59	DQ_{11}	79	PD_7
20	NC	40	A_{12}	60	DQ_{10}	80	V_{SS}

6

Table 2. Pin Description

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}_0$–$\overline{CE}_3$	INPUT	**CHIP ENABLE:** Activates each device's control logic, input buffers, decoders, and sense amplifiers. Each line is unique to one set of 2 devices (word). $\overline{CE}_X$ is active low; $\overline{CE}_X$ high deselects the memory device and reduces power consumption to standby levels. Only one $\overline{CE}_X$ may be active at a time.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}_H$; $\overline{WE}_L$	INPUT	**WRITE ENABLE** controls writes to the control register and the array. ($\overline{WE}_H$ = High Byte; $\overline{WE}_L$ = Low Byte) Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **NOTE:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array (12V ± 5%).
V_{CC}		**DEVICE POWER SUPPLY:** (5V ± 10%).
V_{SS}		**GROUND.**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.
RES		**RESERVED** for future product enhancements.
PD_1–PD_7		**PRESENCE DETECT:** Denotes word depth (512K) and access time of device. See Table 3, "Presence Detect "PD" Pins" on Page 5.

Pin	Function
17	$\overline{CE}_7$
18	$\overline{CE}_6$
19	$\overline{CE}_5$
20	$\overline{CE}_4$
30	A_{22}
31	A_{21}
32	A_{20}
33	A_{19}
34	A_{18}
35	A_{17}

Table 3. Presence Detect "PD" Pins

MODULE CAPACITY IDENTIFICATION			
MODULE CAPACITY WORD DEPTH	**PD6**	**PD2**	**PD1**
NO MODULE	O	O	O
256K/32M	O	O	S
512K/64M	O	S	O
1M/128M	O	S	S
2M/256M	S	O	O
4M/512M	S	O	S
8M/1G	S	S	O
16M/2G	S	S	S

MODULE SPEED IDENTIFICATION				
MAXIMUM ACCESS TIME	**PD7**	**PD5**	**PD4**	**PD3**
>300 ns	S	S	S	S
300 ns	S	S	S	O
250 ns	S	S	O	S
200 ns	S	S	O	O
185 ns	S	O	S	S
150 ns	S	O	S	O
135 ns	S	O	O	S
120 ns	S	O	O	O
100 ns	O	S	S	S
85 ns	O	S	S	O
70 ns	O	S	O	S
60 ns	O	S	O	O
50 ns	O	O	S	S
40 ns	O	O	S	O
30 ns	O	O	O	S
ND	O	O	O	O

O = OPEN CIRCUIT ON MODULE
S = SHORT CIRCUIT TO GROUND ON MODULE
ND = NOT DEFINED

6

SINGLE IN-LINE MEMORY MODULE BOARD

PC substrate: Glass Epoxy [0.05" +0.004/−0.003 nominal thickness]. The iSM001FLKA low-profile SIMM mounts easily between expansion slots. See Appendix A for a list of 80-pin socket suppliers.

APPLICATIONS

With high density, nonvolatility, and extended cycling capability, Intel's iSM001FLKA flash SIMMs offer an innovative alternative to disk and battery-backed static RAM.

Primary applications and operating systems can be stored in flash, eliminating the slow disk-to-DRAM download process. Performance is dramatically enhanced and power consumption is reduced—a consideration particularly important in portable equipment. Flexibility is increased with Flash's electrical chip erasure allowing in-system updates to operating systems and application code.

In diskless workstations and terminals, network traffic is reduced to a minimum and systems are instant-on. Reliability exceeds that of electro-mechanical media. Often in these environments, power glitches force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communication protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/disk for main system memory or nonvolatile backup storage, Flash SIMMs provide a solid state alternative in a minimal form factor. Flash memory provides higher performance, lower power consumption and instant-on capability. Additionally, flash is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

For systems currently using a high-density static RAM/battery configuration for code updates and data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The possibility of battery failure is removed. This consideration is important for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a four-to-one cost advantage over SRAM.

Flash memory's electrical chip erasure, byte reprogrammability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank-slate" in which to log or record data. Data can be periodically off-loaded for analysis-erasing the slate and repeating the cycle.

Flash SIMMs add additional flexibility to designers by offering end-users incremental expansion memory. As code requirements grow or as memory prices drop, your customers have the option of adding more memory.

PRINCIPALS OF OPERATION

The iSM001FLKA operates as eight N28F010 flash memories connected as shown in the Functional Block Diagram on Page 2.

The iSM001FLKA, organized as 512K x 16, can also be configured for 8- and 32-bit systems. For 32-bit systems, add a second SIMM to your design as currently done with DRAM. For byte-wide operation, buffer the SIMMs DQ_0–DQ_7 and DQ_8–DQ_{15} lines with an octal transceiver; then, tie the buffered outputs together to form the 8-bit bus. Decode the transceiver's enable input with an address line.

The iSM001FLKA features hardware presence detect pins to facilitate memory design. The presence detect pins (PD1–PD7) indicate module word depth and maximum access speed (see Table 3 on the previous page). The pins allow memory-specific wait-state generation upon system initialization. To use the presence capability, pull-up the PD1–PD7 lines through a pull-up resistor. Read the lines through a port and select the appropriate memory depth and speed from a PD data table.

In the absence of high voltage on the modules V_{PP} pins, the iSM001FLKA is a read-only memory array. Manipulation of the module's control pins yields standard read, standby and output disable functions.

Read, standby and output disable operations are also available when high voltage is applied to the V_{PP} pins. In addition, high voltage on the V_{PP} pins enables erasure and programming of the module's devices. All functions associated with altering the memory contents of one or more devices—erase, erase verify, program and program verify—are accessed via each flash device's command register.

Commands are written to a device's command register using standard microprocessor write timings. Register contents serve as input to the devices internal state-machine which controls the erase and programming circuitry. Write cycles to a device also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to a device's register, standard microprocessor read timings output array data, access the int$_e$ligent identifier codes, or output data for erase and program verification.

Table 4. Bus Operations

Operation	Pins	V_{PP}(1)	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_{15}
READ-ONLY	Read	V_{PPL}	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	V_{IH}	X	X	Tri-State
READ/WRITE	Read	V_{PPH}	V_{IL}	V_{IL}	V_{IH}	Data Out(3)
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(4)	V_{PPH}	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	Data In(5)

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes are accessed via a command register write sequence. Refer to Table 5. All other addresses are low.
3. Read operations with $V_{PP} = V_{PPH}$ may access array data or the int$_e$ligent Identifier™ codes.
4. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
5. Refer to Table 5 for valid Data-In during a write operation.
6. X can be V_{IL} or V_{IH}.

Integrated Stop Timer

Successive command write cycles define the duration of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

A device's command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the iSM001FLKA a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The iSM001FLKA is designed to accommodate either design practice, and to encourage optimization of flash's processor-memory interface.

The following section first discusses byte-wide organization, building a basic understanding of byte-wide bus operations, command definitions, and programming and erasure algorithms. The section concludes with performance enhancements for both 16- and 32-bit systems.

BUS OPERATIONS

Read

Each of the iSM001FLKA's flash memory devices has two control functions, both of which must be logically active, to obtain data. Chip-Enable ($\overline{CE}_X$) is the power control and should be used for device selection. Four chip enables ($\overline{CE}_0$–$\overline{CE}_3$) control the array's eight devices. Each line is unique to one set of two devices (word). Only one $\overline{CE}_X$ may be active at a time.

Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from a device to the output pins on the module, independent of device selection. One $\overline{OE}$ line serves the iSM001FLKA's flash devices. Figure 7 illustrates read timing waveforms.

When the V_{PP} lines are high (V_{PPH}), a read operation can be used to access array data, to output a device's int$_e$ligent identifier™ code, and to access a device's data for program/erase verification. When V_{PP} is low (V_{PPL}), a read operation can **only** access array data.

Output Disable

With the iSM001FLKA's Output-Enable pin at a logic-high level (V_{IH}), outputs from all devices are disabled. They are placed in a high-impedance state.

STANDBY

With Chip-Enable at a logic-high level, the standby operation disables most of the deselected devices circuitry and substantially reduces device power consumption. The outputs of the deselected devices are place in a high-impedance state, independent of the Output-Enable signal. If a word is deselected during erase, programming, or program/erasure verification, the device draws active current until the operation is terminated.

Inteligent Identifier™ Operation

The inteligent identifier operation outputs the selected devices' manufacturer code (89H) and device code (B4H). The manufacturer code and device code are read via the devices' command register. Following a write of 90H to a device's command register, a read from address location 0000H outputs the manufacture code (89H). A read from address 0001H outputs the device code (B4H).

Write

Erasure and programming is accomplished via each device's command register, when high voltage is applied to the V_{PP} pins. The contents of each device's register serve as input to its internal state-machine. The state machine outputs dictate the function of each device.

A device's command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

Two write enable lines are provided, $\overline{WE}_H$ and $\overline{WE}_L$, allowing selective write control of upper and lower bytes.

A device's command register is written by selecting the device (Chip-Enable low), then bringing Write-Enable ($\overline{WE}_H$ or $\overline{WE}_L$) to a logic-low level (V_{IL}). If both WE lines are a logic low, both upper and lower bytes are written. Addresses are latched on the falling edge of the Write-Enable signal, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timing are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the module's V_{PP} pins, the contents of all devices' command registers default to 00H, enabling read-only operations.

Placing high voltage on the module's V_{PP} pins allows read/write operation on selected devices. Operations are selected by writing specific data patterns to the device(s) command register. Table 5 defines these register commands.

Table 5. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read inteligent identifier™ Codes(4)	3	Write	X	90H	Read	(4)	(4)
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 4.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device B4H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read inteligent ID command, two read operations access manufacturer and device codes.
5. Figure 4 illustrates the Quick-Erase™ Algorithm.
6. Figure 3 illustrates the Quick-Pulse Programming™ Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, the selected devices memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register of each device. Microprocessor read cycles retrieve array data. The selected devices remain enabled for reads until their command register contents are altered.

The default contents of each device's command register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration to the iSM001FLKA's memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hardwired to the iSM001FLKA's V_{PP} pins, all eight devices power-up and remain enabled for reads until their command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier™ Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system.

Each flash memory device contains an int$_e$ligent Identifier operation. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B4H. To terminate the operation, it is necessary to write another valid command into the register.

The int$_e$ligent Identifier and the Presence Detect pins give you complementary information. While the PD pins denote speed and depth, the int$_e$ligent Identifier operation gives you manufacture and device data.

Set-Up Erase/Erase Commands

Set-up Erase is a command-only operation that stages a selected device for electrical erasure of all bytes in its array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of a Write-Enable pulse ($\overline{WE}_H$ or $\overline{WE}_L$) and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pins. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the selected device(s) in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register of the device. The address for the byte to be verified must be supplied as it is latched on the falling edge of a Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

Each 28F010 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte of the device until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes of the device have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-up) to the command register of the device. Figure 4, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of each 28F010. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-Up Program/Program Commands

Set-up program is a command-only operation that stages a device for byte programming. Writing 40H into the command register of the device performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

Each 28F010 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register of the device. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

Each 28F010 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 3, the Quick-Pulse Programming™ algorithm (8-bit Systems), illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences to a device. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

Each of the iSM001FLKA's eight 28F010s is specified for a minimum of 10,000 program/erase cycles. Each device is programmed and erased using Intel's Quick-Pulse Programming and Quick-Erase algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further information, see Reliability Report RR-60 (ETOX II Reliability Data Summary).

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 3 illustrates the Quick-Pulse Programming algorithm for 8-bit systems.

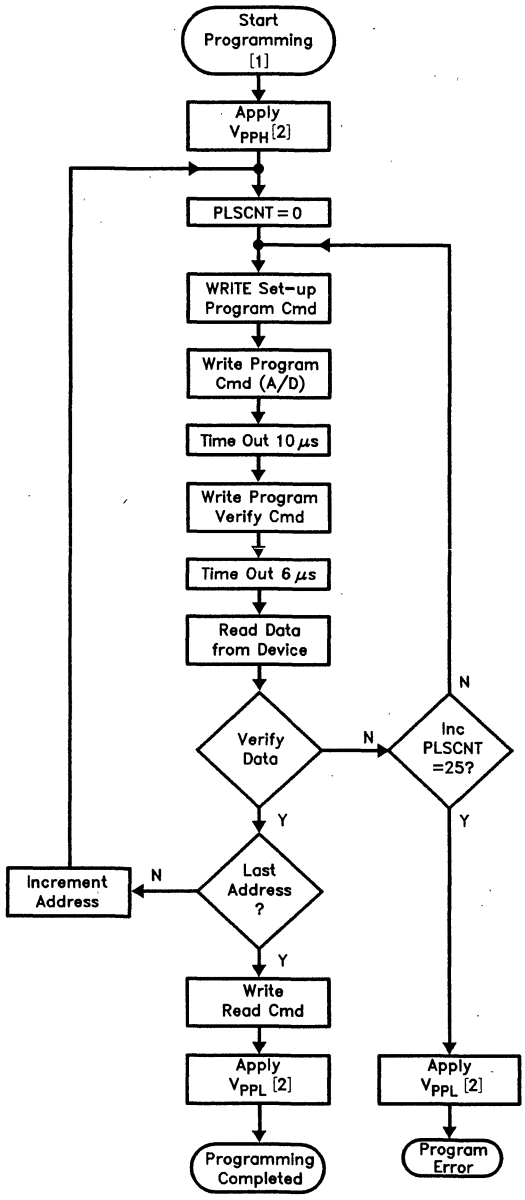
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The iSM001FLKA is erased when shipped from the factory. Reading FFH data from each device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 4 illustrates the Quick-Erase algorithm for 8-bit systems.



290244-3

Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(3) Verify	Data = C0H; Stops Program Operation(4)
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(2)

NOTES:

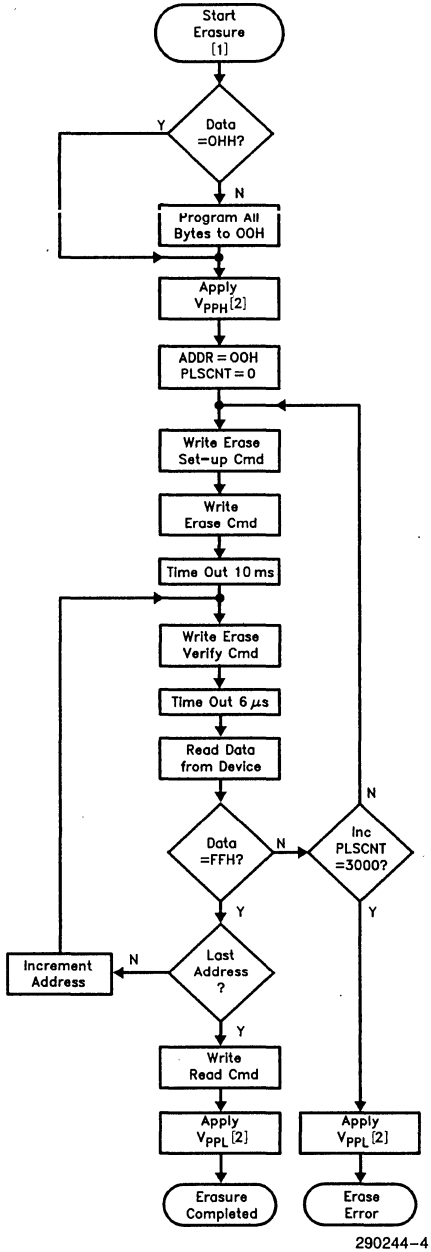
1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

2. See DC Characteristics for value of V_{PPH} and V_{PPL}.

3. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.

4. Refer to principles of operation

Figure 3. Quick-Pulse Programming™ Algorithm (8-Bit Systems)



290244-4

Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(2)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase(3) Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation(4)
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(2)

NOTES:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

2. See DC Characteristics for value of V_{PPH} and V_{PPL}.

3. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.

4. Refer to principles of operation.

Figure 4. Quick-Erase™ Algorithm (8-Bit Systems)

HIGH PERFORMANCE PARALLEL DEVICE ERASURE

Total erase time for the SM28F001AX is reduced by implementing a parallel erase algorithm (Note 1). You save time by erasing all devices at the same time. However, since flash memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the command register Reset command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020h twice in succession. This starts erasure. After 10 ms, the CPU writes the data word verify command A0A0h to stop erasure and setup erase verification. If both bytes are erased at the given address, then the CPU increments the address (by 2) and then writes the verify command A0A0h again. If neither byte is erased, then the CPU issues the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFh data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFh and the verify command would be A0FFh. Once the high byte verifies at that address, the CPU modifies the command back to the default 2020h and A0A0h, increments the address by 2, and writes the verify command to the next address.

See Figure 5 for a conceptual view of the parallel erase flow chart and Appendix B for the detailed version. These flow charts are for 16-bit systems and can be expanded for 32-bit designs.

NOTE:
1. Parallel Erasure and Programming require appropriate choice of V_{PP} supply to support the increased power consumption.

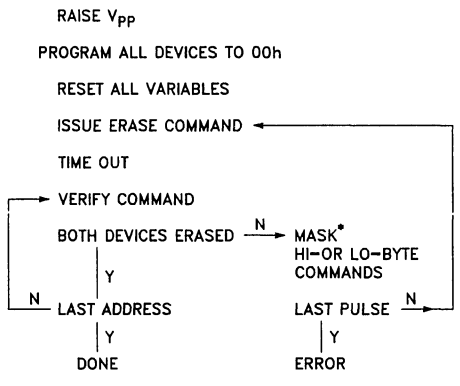
HIGH PERFORMANCE PARALLEL DEVICE PROGRAMMING

Software for word- or double-word programming can be written in two different manners. The first method offers simplicity of design and minimizes software overhead by using a byte programming routine on each device independently (using host CPU's byte addressing mode). The second method offers higher performance by programming the word or double-word data in parallel. This method manipulates the command register instructions for independent byte control. See Figure 6 for conceptual 2-device parallel programming flow chart and Appendix C for the detailed version. Here you can use the host CPU's appropriate word- or double-word addressing modes (i.e., incrementing by 2- or 4-byte addresses, respectively).

NOTE:
Word or double-word programming assumes 2 or 4 8-bit flash memory devices.

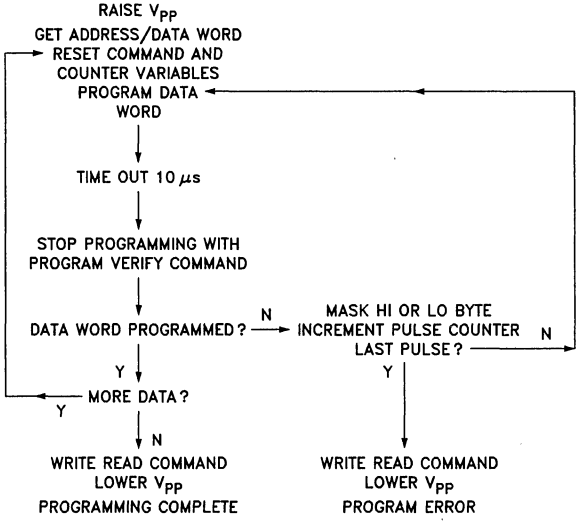
Parallel Programming Algorithm Summary:

- Decreases programming time by programming 2 flash memories (16 bits) in parallel. The algorithm can be expanded for 32-bit systems.
- Eliminates tracking of high/low byte addresses and respective number of program pulses by directing the CPU to write data-words (16-bit) to the command register.
- Maintains word write and read operations. Should a byte on one device program prior to a byte on the other, the CPU continues to write word-commands to both devices. However, it deselects the verified byte with software commands. An alternative is to independently program high and low bytes using hardware select capability (byte-addressing mode of host CPU).



*You mask the device by substituting a Reset command for the Erase and Verify commands. That way, the erased byte idles through the next erase loop.

Figure 5. High Performance Parallel Erasure (Conceptual Overview)



*You mask the device by substituting a Reset command for the Program and Verify commands. That way, the programmed bytes do not get further programmed on subsequent pulses.

Figure 6. Parallel Programming Flow Chart (Conceptual Overview)

6

DESIGN CONSIDERATIONS

Two-Line Output Control

Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The iSM001FLKA features a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Also, a 4.7 μF tantalum capacitor decouples the array's power supply between V_{CC} and V_{SS} and between V_{PP} and V_{SS}. The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The two V_{PP} pins supply current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots. Be sure to connect both module V_{PP} inputs to your 12V supply.

Power Up/Down Protection

The iSM001FLKA is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, each 28F010 is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. Power supply sequencing is not required. Internal circuitry in each 28F010 ensures that the command register is reset to the read mode on power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because each 28F010 does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating each 28F010.

Table 4. 28F010 Typical Update Power Dissipation(4)

Operation	Power Dissipation (Watt-Seconds)
Array Program/Program Verify(1)	0.171
Array Erase/Erase Verify(2)	0.136
One Complete Cycle(3)	0.478

NOTES:
1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{PP2} typical + t_{WHGL} × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{CC2} typical + t_{WHGL} × I_{CC4} typical].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{PP} (V_{PP3} typical × t_{ERASE} typical + I_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC} (I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals are not guaranteed but based on a limited number of samples taken from production lots.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(1)
During Erase/Program .....0°C to +70°C

Temperature Under Bias .....−10°C to +80°C

Storage Temperature .....−50°C to +100°C

Voltage on Any Pin with
Respect to Ground .....−2.0V to +7.0V(2)

V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program ....−2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with
Respect to Ground .....−2.0V to +7.0V(2)

Output Short Circuit Current.....100 mA(4)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

6

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{LI}	Input Leakage Current	3			±8.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	3			±40.0	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1, 3			8.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	2, 3		26	66	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	2, 3		8.0	26	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	2, 3		16.0	36	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	2, 3		16.0	36	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	2, 3		16.0	36	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	3			±80	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					±80	μA	$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	2, 3		16.5	61.2	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	2, 3		12.5	61.2	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

NOTES:
1. V_{CC} standby current for 8 devices.
2. Calculations assume only the 2 devices of the 16-bit word are enabled. The remaining 6 devices are in standby. Current will be higher if interleaving is used.
3. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).

DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typ	Max		
I_{LI}	Input Leakage Current	3			±8.0	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	3			±40.0	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1, 3		0.4	0.8	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2V$
I_{CC1}	V_{CC} Active Read Current	2, 3		20.3	60.6	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	2, 3		2.3	20.6	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	2, 3		10.3	30.6	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	2, 3		10.3	30.6	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	2, 3		10.3	30.6	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current				±80	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					±80	μA	$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	2, 3		16.5	61.2	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	2, 3		12.5	61.2	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	2, 3		4.5	11.2	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage		0.85 V_{CC}			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}			V_{CC} − 0.4				I_{OH} = −100 μA, $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Read-Only Operations		0.00		6.5	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

NOTES:
1. V_{CC} standby current for 8 devices.
2. Calculations assume only the 2 devices of the 16-bit word are enabled. The remaining 6 devices are in standby. Current will be higher if interleaving is used.
3. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C. These currents are valid for all product versions (packages and speeds).

CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN1}	Address Capacitance	2		60	pF	V_{IN} = 0V
C_{IN2}	Control Capacitance	2		65	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	2		55	pF	V_{OUT} = 0V

NOTES:
1. Trace capacitance calculated, not measured.
2. Address and control capacitance of a typical device is 6 pF.
3. Output capacitance of a typical device is 12 pF.

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%).....10 ns
Input Pulse Levels .....0.45V and 2.4V
Input Timing Reference Level .....0.8V and 2.0V
Output Timing Reference Level .....0.8V and 2.0V

AC CHARACTERISTICS—Read-Only Operations[2]

Versions		Notes	iSM001FLKA-120		iSM001FLKA-200		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	3	120		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			120		200	ns
t_{AVQV}/t_{ACC}	Address Access Time			120		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			50		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	3	0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	3		55		55	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	3	0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z		4	30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change	3	0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.
3. Not 100% tested: Characterization data available.
4. Guaranteed by design.

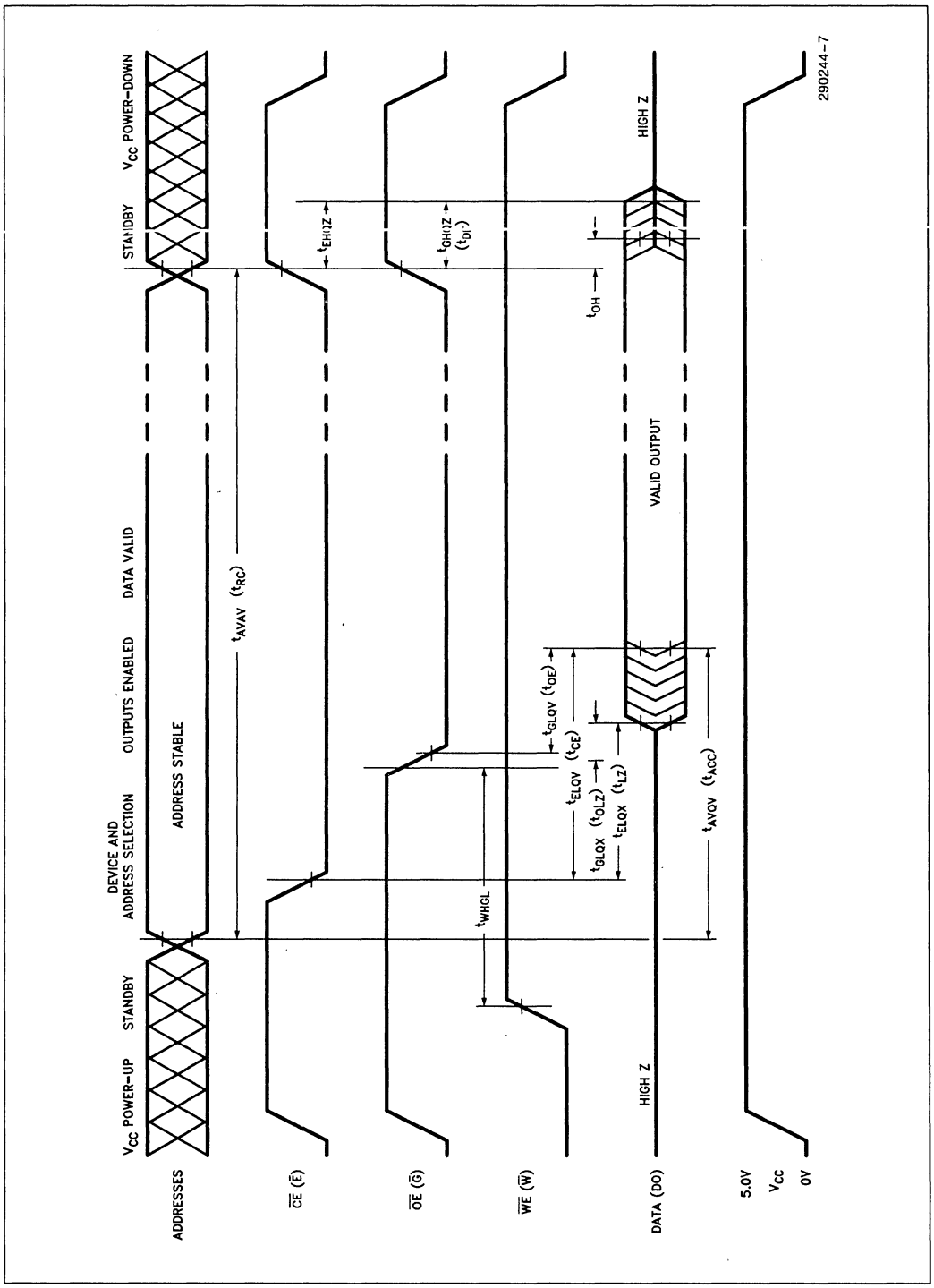


Figure 7. AC Waveforms for Read Operations

AC CHARACTERISTICS—Write/Erase/Program Operations(1, 2)

Versions			iSM001FLKA-120		iSM001FLKA-200		Unit
Symbol	Characteristic	Notes	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		120		200		ns
t_{AVWL}/t_{AS}	Address Set-up Time		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		75		ns
t_{DVWH}/t_{DS}	Data Set-up Time		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		μs
t_{GHWL}	Read Recovery Time before Write		0		0		μs
t_{ELWL}/t_{CS}	Chip Enable Set-up Time before Write		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	2	60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		μs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		ms
t_{VPEL}	V_{PP} Set-up Time to Chip Enable Low		1.0		1.0		μs

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10 ns.
3. The integrated stop timer terminates the program/erase operations, thereby eliminating the need for a maximum specification.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits						Unit
		28F010-120			28F010-200			
		Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		1	10		1	30	Sec
Chip Program Time	1, 2, 4		2	12.5		2	12.5	Sec
Erase/Program Cycles	1, 5	10,000	100,000		10,000	100,000		Cycles

NOTES:
1. Typicals are not guaranteed, but based on a limited number of samples from production lots. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time excluding system overhead is 16 μs (10 μs program + 6 μs write recovery), while maximum is 400 μs/byte (16 μs x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX™II Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

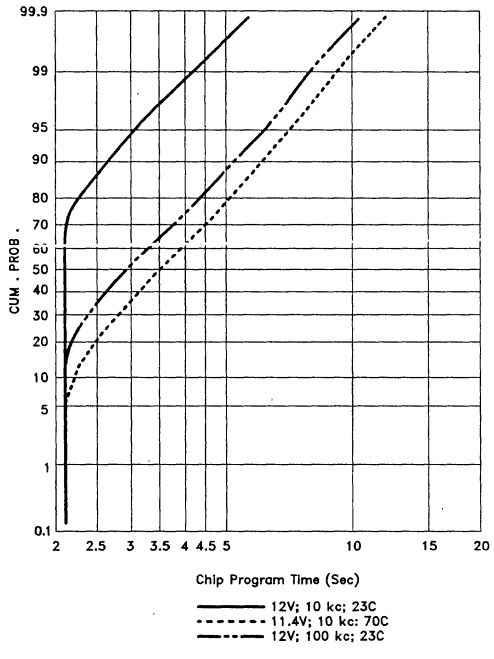


Figure 8. 28F010 Typical Programming Capability

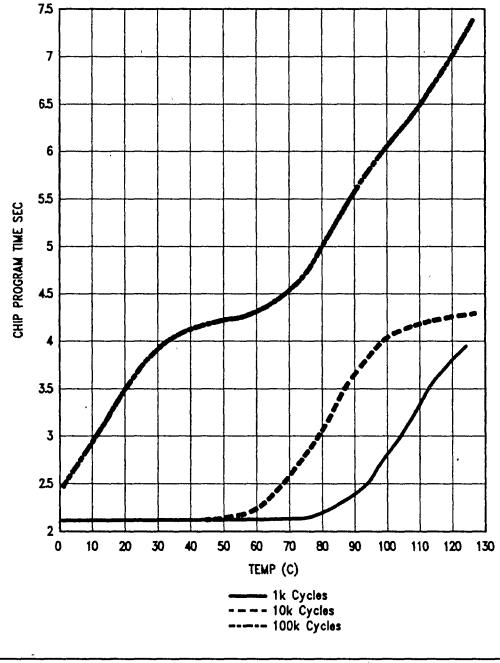


Figure 9. 28F010 Typical Program Time at 12V

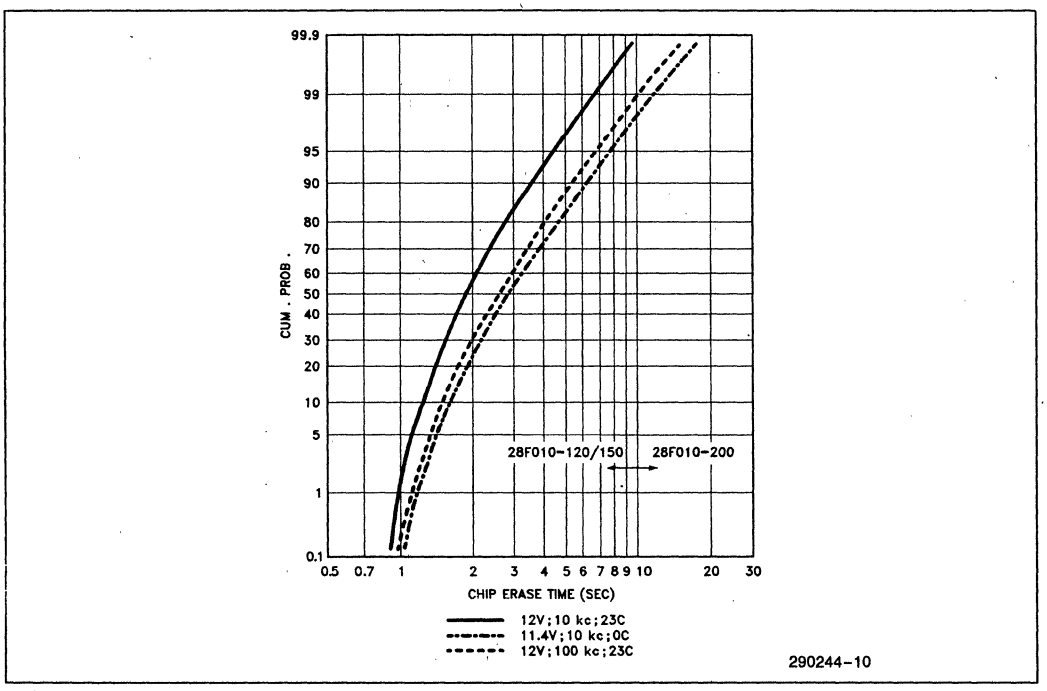


Figure 10. 28F010 Typical Erase Capability

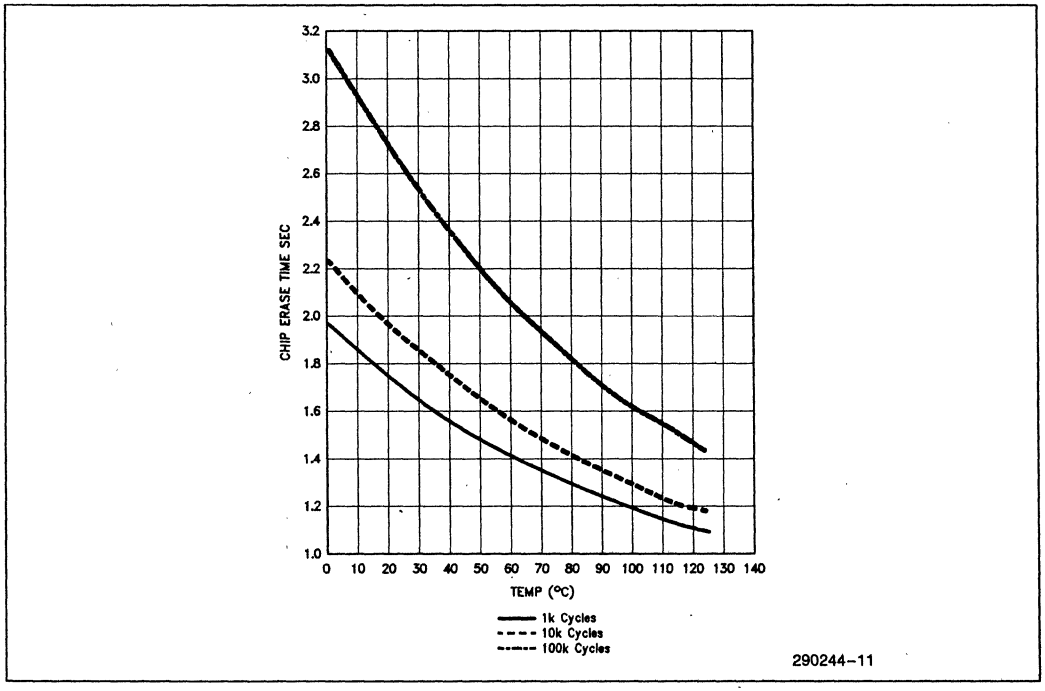


Figure 11. 28F010 Typical Erase Time at 12.0V

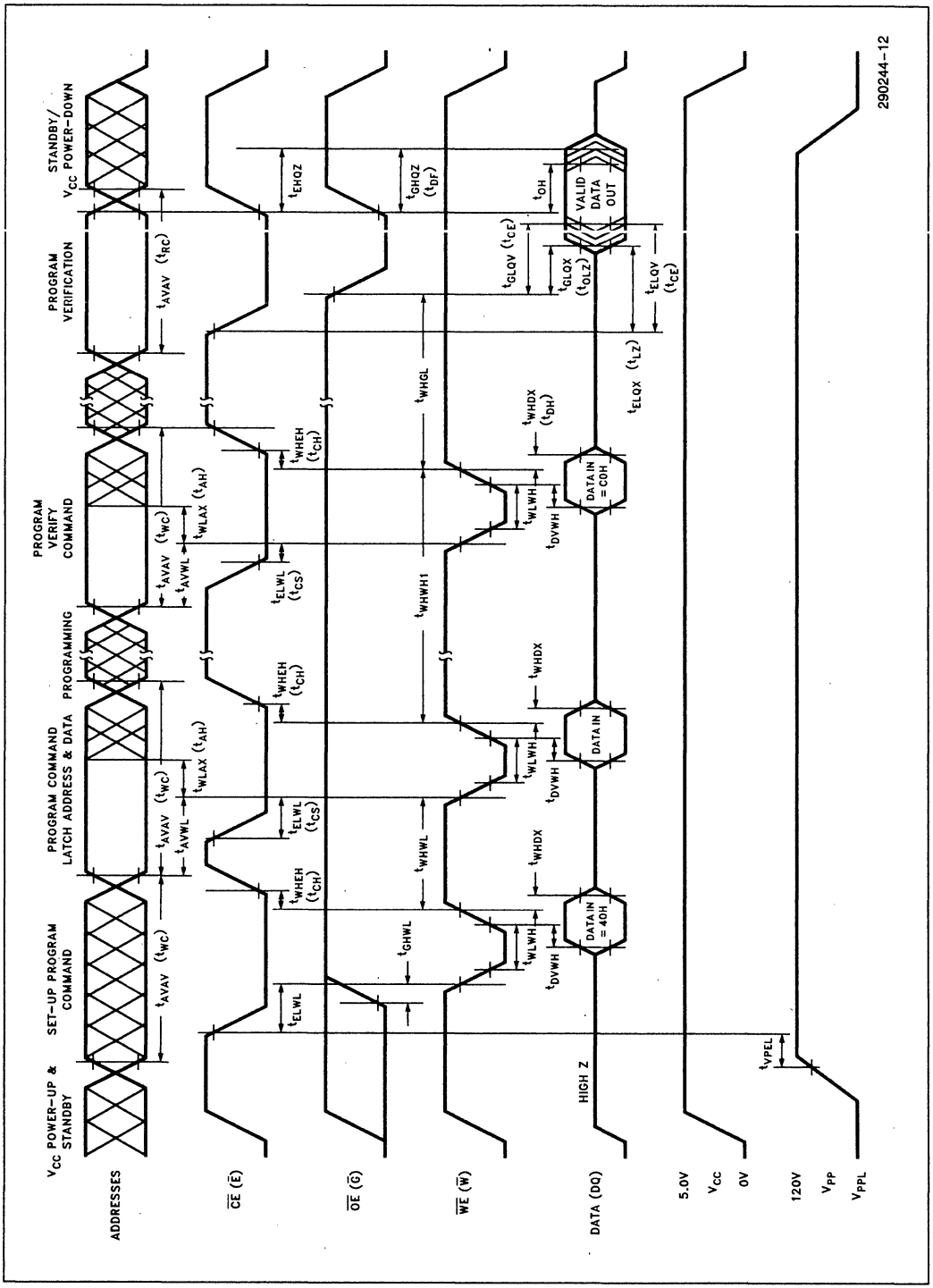


Figure 12. AC Waveforms for Programming Operations

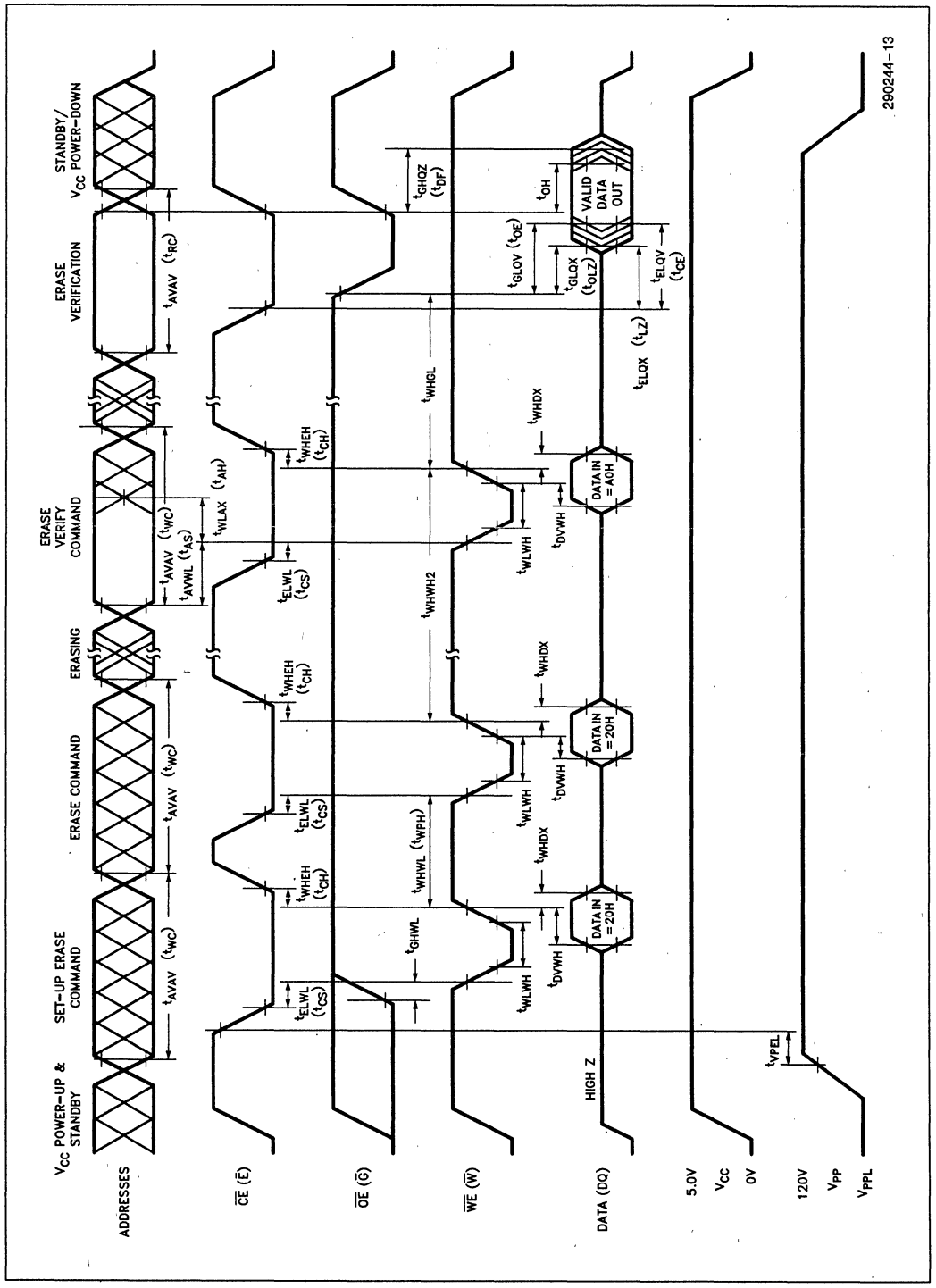
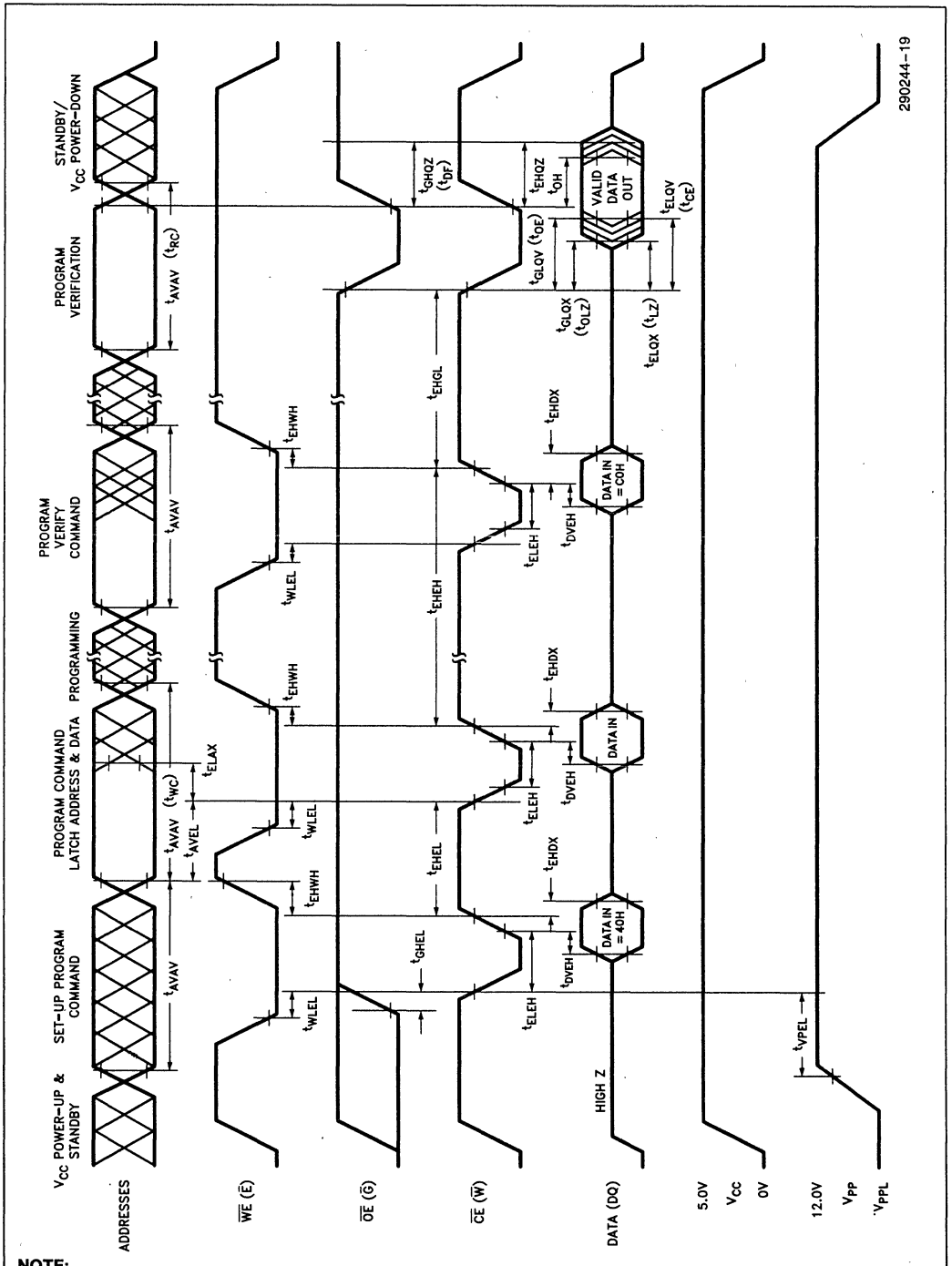


Figure 13. AC Waveforms for Erase Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Versions			28F010-120		28F010-200		Unit
Symbol	Characteristic	Notes	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		120		200		ns
t_{AVEL}	Address Set-Up Time		0		0		ns
t_{ELAX}	Address Hold Time		80		95		ns
t_{DVEH}	Data Set-Up Time		50		50		ns
t_{EHDX}	Data Hold Time		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		µs
t_{GHEL}	Read Recovery Time before Write		0		0		µs
t_{WLEL}	Write Enable Set-Up Time before Chip Enable		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		80		ns
t_{EHEL}	Write Pulse Width High		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low		1.0		1.0		µs

NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.



NOTE:
Alternative $\overline{CE}$-Controlled Write Timings also apply to erase operations.

Figure 14. Alternate AC Waveforms for Programming Operations

APPENDIX A
PARTIAL LIST(1) OF 80-PIN SIMM SOCKET COMPANIES

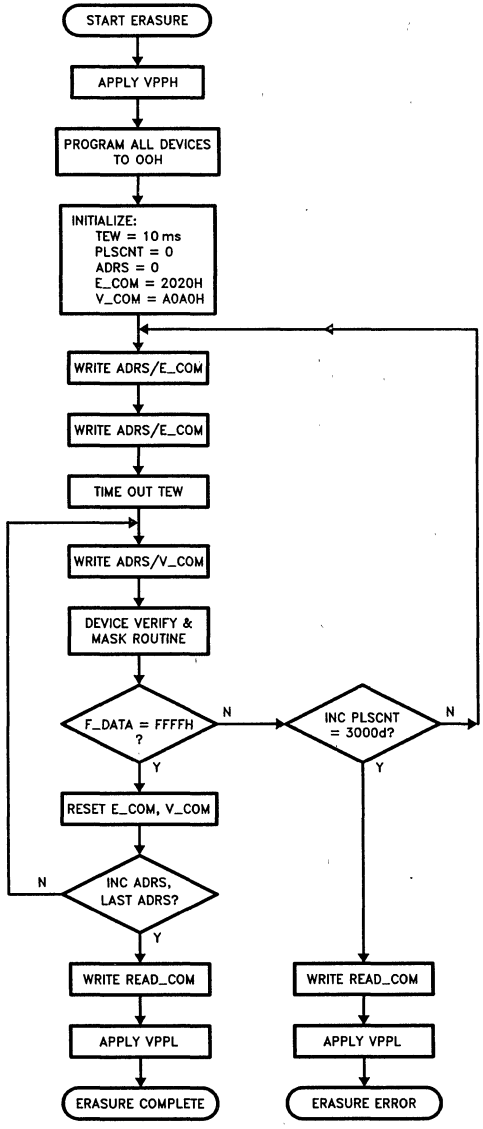
AMP INCORPORATED
HARRISBURG, PA 17105
(800) 522-6752

BURNDY CORPORATION
51 RICHARDS AVENUE
NORWALK, CT 06856
(203) 838-4444

MOLEX
2222 WELLINGTON COURT
LISLE, IL 60532
(708) 969-4550

NOTES:
1. This list is intended for example only, and in no way represents all companies that support 80-pin SIMM Sockets. Intel Corporation assumes no responsibility for circuitry other than circuitry embodies in an Intel product. No other circuit patent licenses are implied.
2. Socket reliability data can be obtained from the above companies upon request.

APPENDIX B
PARALLEL ERASE FLOW CHART



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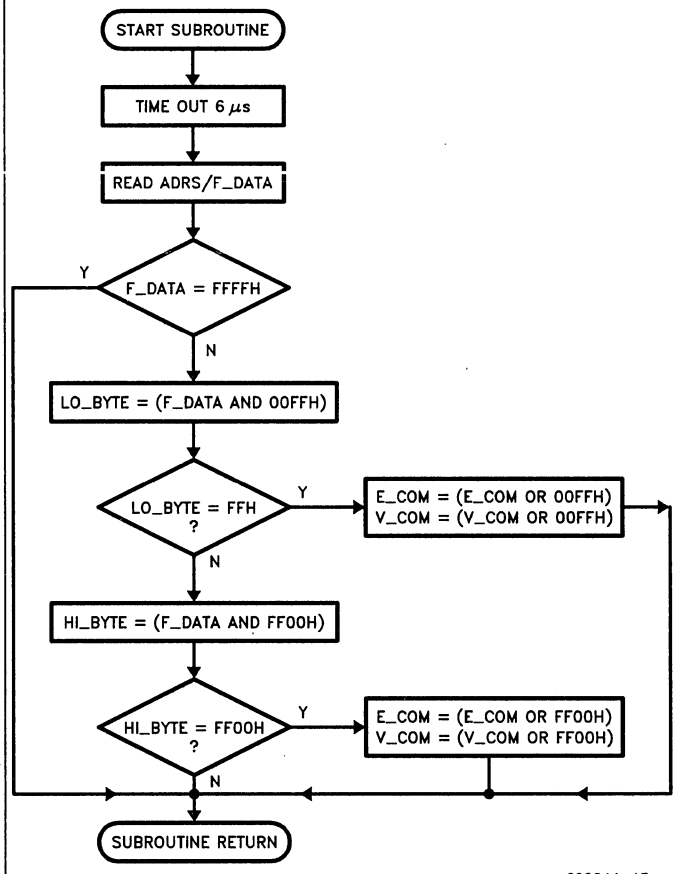
COMMENTS
Wait for V_{PP} to stabilize.
Use Quick-Pulse Programming algorithm.
Initialize Variables: TEW = Erase duration (width) PLSCNT = Pulse Counter ADRS = Address E_COM = Erase Command V_COM = Verify Command
Erase Set-up Command
Start Erasing
Duration of Erase Operation.
Erase Verify Command stops erasure.
See next page for subroutine.
When both devices at ADRS are erased, F_DATA = FFFFH. If not equal, increment the pulse counter and check for last pulse.
Reset commands to default (E_COM = 2020H, V_COM = A0A0H) before verifying next ADRS.
Reset devices for read operation.
Turn off V_{PP}.

Device Verify and Mask Subroutine



290244-15

COMMENTS
This subroutine reads the data word (F__DATA). It then masks the HI or LO Byte of the Erase and Verify commands from executing during the next operation.
If both HI and LO bytes verify, then return.
Mask* the HI Byte with 00H.
If the LO Byte verifies erasure, then mask* the erase and verify commands with 00FFH(Reset).
Mask* the LO Byte with 00H.
If the HI Byte verifies erasure, then mask* the erase and verify commands with FF00H(Reset).

NOTE:
*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming flash data (F__DATA), the erase commands and the verify commands. Then manipulate the HI or LO register contents.

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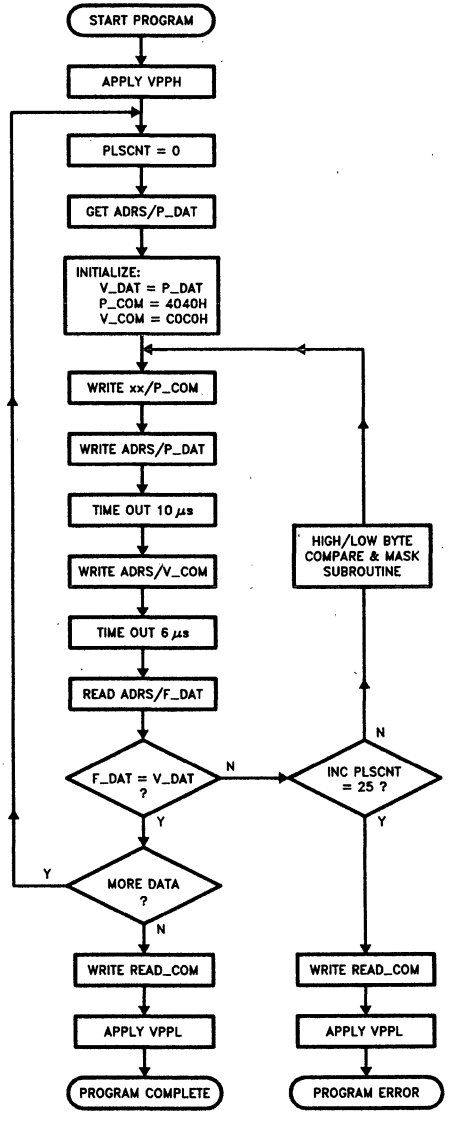
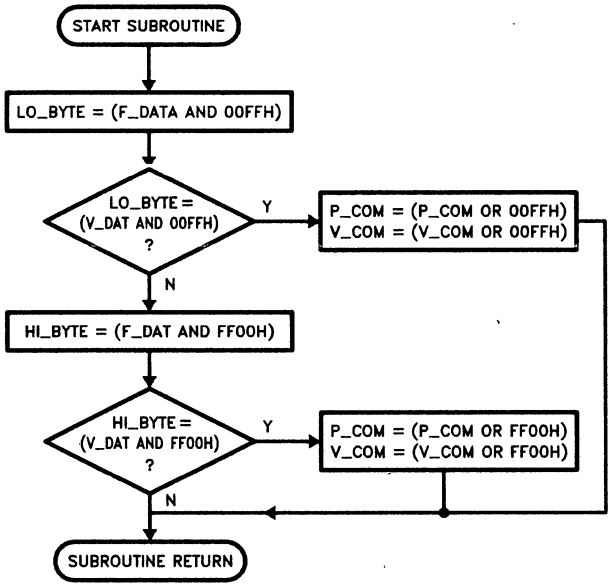
APPENDIX C
PARALLEL PROGRAMMING FLOW CHART



290244-16

COMMENTS
Wait for V_{PP} ramp to V_{PPH}
PLSCNT = Pulse Counter
ADRS = address to program P__DAT = data word to program
Initialize Data Word Variables: V__DAT = valid data P__COM = Program Command V__COM = Verify Command
Program Set-up Command xx = Address don't care
Program
See next page for subroutine
Program Verify Command
F__DAT = flash memory data
Compare flash memory data to valid data (word compare). If not equal, increment pulse counter and check for last pulse. If not last pulse, compare High and Low Byte.
Check buffer or I/O port for more data to program.
Reset device for read operation.
Turn off V_{PP}.

Program Verify and Mask Subroutine



290244-17

COMMENTS
MASK* the HI Byte with 00H.
If the LO Byte Verifies, then mask* the program and verify command with 00FFH (RESET).
Mask* the LO Byte with 00H.
If HI Byte Verifies, then mask* the program and erase command with FF00H (RESET).

NOTE:
*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming flash data (F__DATA), the erase commands and the verify commands. Then manipulate the HI or LO register contents.

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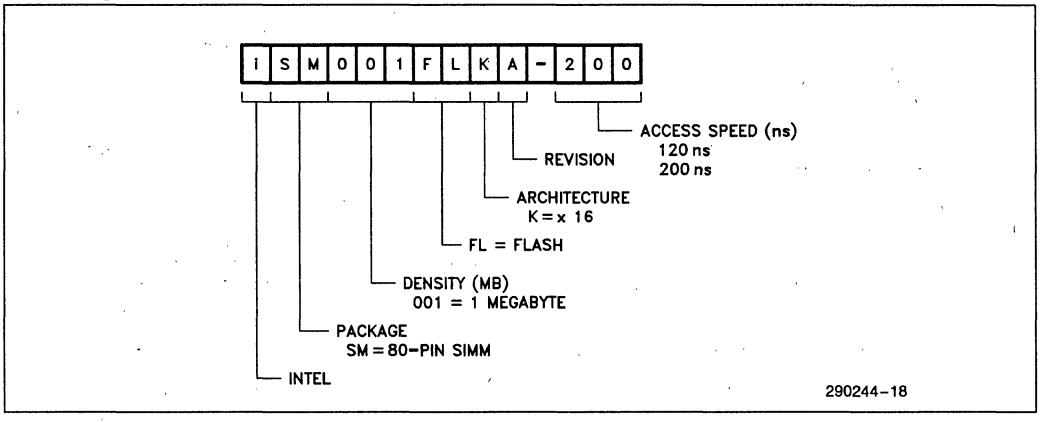
Ordering Information



Valid Combinations:

iSM001FLKA-120
iSM001FLKA-200

ADDITIONAL INFORMATION

	Order Number
ER-20, "ETOX™ II Flash Memory Technology"	294005
ER-24, "The Intel 28F010 Flash Memory"	294008
RR-60, "ETOX™ II Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
AP-325, "Guide to Flash Memory Reprogramming"	292059
AP-343, "Flash Memory — A Mass Storage Medium"	292079

iMC001FLKA
1-MEGABYTE FLASH MEMORY CARD

- **Inherent Nonvolatility (Zero Retention Power)**
  - **No Batteries Required for Back-up**
- **Over 1,000,000 Hours MTBF**
  - **More Reliable than Disk**
- **High-Performance Read**
  - **250 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **25 mA Typical Active Current (X8)**
  - **400 μA Typical Standby Current**
- **Flash Electrical Zone-Erase**
  - **1 Second Typical per 128 K-Byte Zone**
  - **Multiple Zone Erase > 128 K-Bytes/Sec**
- **Random Writes to Erased Zones**
  - **10 μs Typical Byte Write**
- **Write Protect Switch to Prevent Accidental Data Loss**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **ETOX™ II Flash Memory Technology**
  - **5V Read, 12V Erase/Write**
  - **High-Volume Manufacturing Experience**
- **PCMCIA/JEIDA 68-Pin Standard**
  - **Byte- or Word-wide Selectable**
- **Independent Software & Hardware Vendor Support**
  - **Integrated System Solution Using Flash Filing Systems**

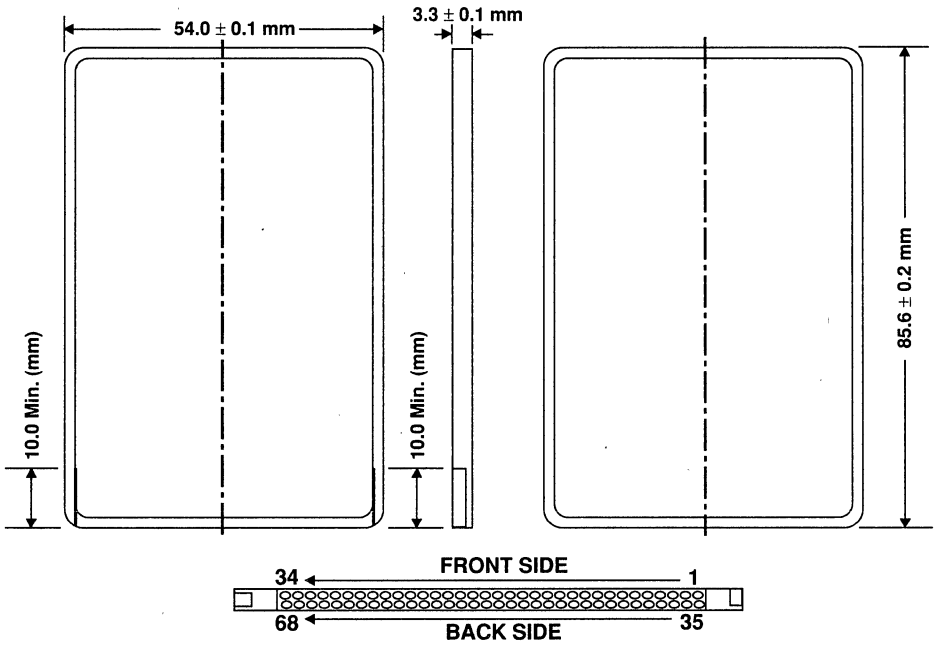
Intel's Flash Memory Card is the integrated memory solution for portable PCs. The iMC001FLKA enables OEM system manufacturers to design portable PCs that no longer require rotating electro-mechanical media to store application code and data files. This allows the design and manufacture of PCs that are higher performance, more rugged, consume less battery power, and weigh much less than traditional disk-based portable PCs. The flash memory card supports the emerging "Mobile Office" by allowing the user to transport both application code and data files between desktop PCs and portables.

The iMC001FLKA conforms to the PCMCIA/JEIDA international standard, providing compatibility at the hardware and data interchange level. OEMs may opt to write the Card Information Structure (CIS) at the memory card's address 00000H with a format utility. This information provides data interchange functional compatibility. The 250 nanosecond access time allows for "execute-in-place" capability, for popular low-power microprocessors. Intel's 1-Megabyte Flash Memory Card operates in a byte-wide and word-wide configuration providing performance/power options for different systems.

Intel's Flash Memory card employs Intel's ETOX II Flash Memories. Filing systems, such as Microsoft's* Flash File System (FFS), facilitate sequential data file storage and card erasure using a purely nonvolatile medium. Flash filing systems, coupled with the Intel Flash Memory Card, effectively create an all-silicon nonvolatile read/write random access memory system that is more reliable and higher performance than disk-based memory systems.

*Microsoft is a trademark of Microsoft Corp.

Order Number: 290399-001



1	GND	18	V_{pp1}	35	GND	52	V_{pp2}
2	D_3	19	A_{16}	36	$\overline{CD}_1$	53	NC
3	D_4	20	A_{15}	37	D_{11}	54	NC
4	D_5	21	A_{12}	38	D_{12}	55	NC
5	D_6	22	A_7	39	D_{13}	56	NC
6	D_7	23	A_6	40	D_{14}	57	NC
7	$\overline{CE}_1$	24	A_5	41	D_{15}	58	NC
8	A_{10}	25	A_4	42	$\overline{CE}_2$	59	NC
9	$\overline{OE}$	26	A_3	43	NC	60	NC
10	A_{11}	27	A_2	44	NC	61	$\overline{REG}$[1]
11	A_9	28	A_1	45	NC	62	$\overline{BVD}_2$[2]
12	A_8	29	A_0	46	A_{17}	63	$\overline{BVD}_1$[2]
13	A_{13}	30	D_0	47	A_{18}	64	D_8
14	A_{14}	31	D_1	48	A_{19}	65	D_9
15	$\overline{WE}$	32	D_2	49	NC	66	D_{10}
16	NC	33	WP	50	NC	67	$\overline{CD}_2$
17	V_{cc}	34	GND	51	V_{cc}	68	GND

NOTES:
1. $\overline{REG}$ = register memory select = No Connect (NC), unused. When $\overline{REG}$ is brought low, PCMCIA/JEIDA standard card information structure data is expected. This is accomplished by formatting the card with this data.
2. $\overline{BVD}$ = battery detect voltage = No Connect (NC), unused.

Figure 1. iMC001FLKA Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0-A_{19}	INPUT	**ADDRESS INPUTS** for memory locations. Addresses are internally latched during a write cycle.
D_0-D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the card is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE:** activates the card's high and low byte control logic, input buffers, zone decoders, and associated memory devices. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory card and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** gates the cards output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE** controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. Note: With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP1}, V_{PP2}		**ERASE/WRITE POWER SUPPLY** for writing the command register, erasing the entire array, or writing bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ± 5%).
GND		**GROUND**
$\overline{CD}_1$, $\overline{CD}_2$	OUTPUT	**CARD DETECT.** The card is detected at $\overline{CD}_{1,2}$ = ground.
WP	OUTPUT	**WRITE PROTECT.** All write operations are disabled with WP = active high.
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.
$\overline{BVD}_1$, $\overline{BVD}_2$	OUTPUT	**BATTERY VOLTAGE DETECT. NOT REQUIRED.**

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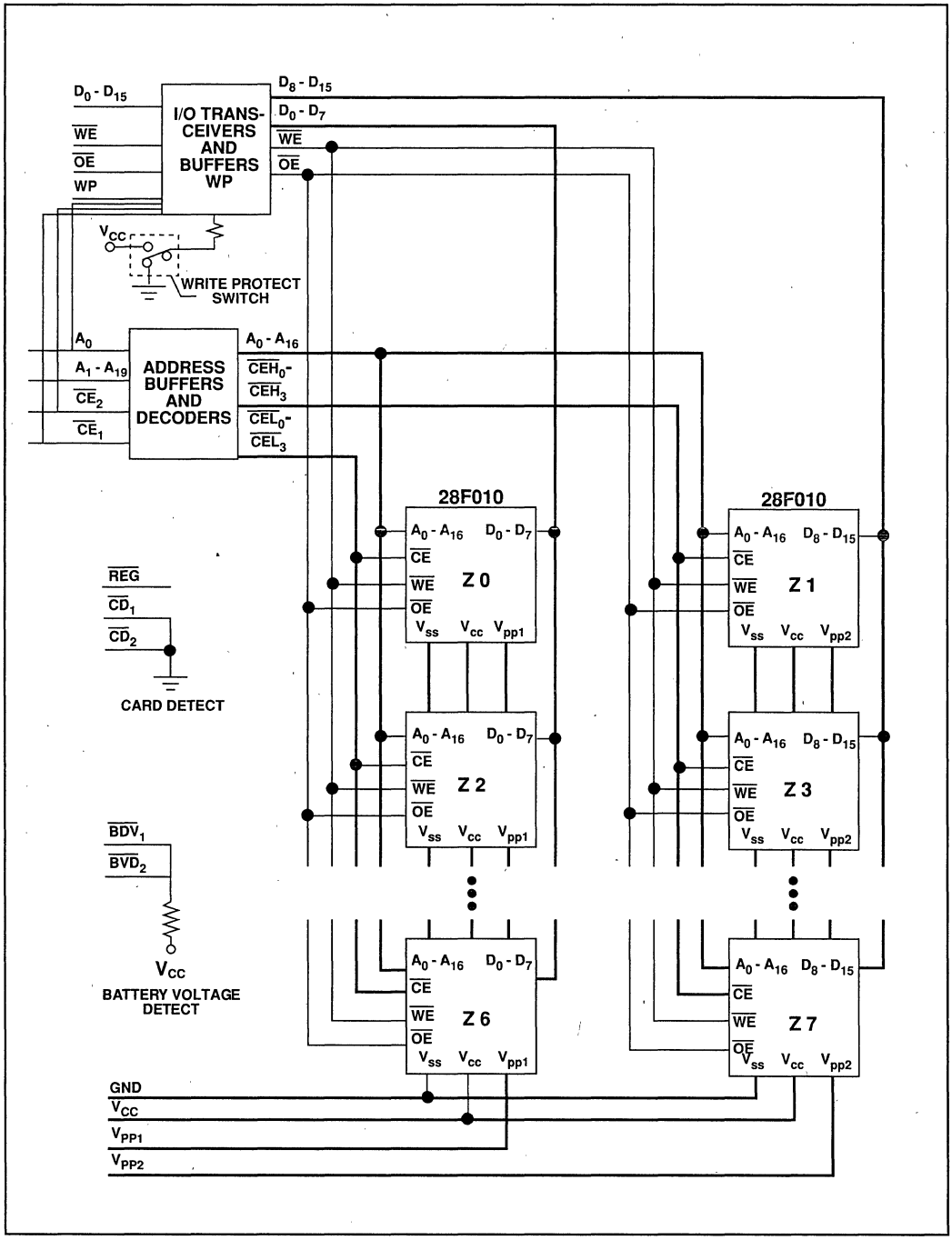

Figure 2. iMC001FLKA Block Diagram

APPLICATIONS

The iMC001FLKA Flash Memory Card allows for the storage of data files and application programs on a purely solid-state removable medium. System resident flash filing systems, such as Microsoft's Flash File System, allow Intel's ETOX II highly reliable Flash Memory Card to effectively function as a physical disk drive. The Intel Flash Memory Card in conjunction with flash filing systems provides an innovative alternative to both fixed hard disks and floppy disks in DOS-compatible portable PCs.

User application software stored on the flash memory card substantially reduces the slow disk-DRAM download process. Replacing the disk results in a dramatic enhancement of read performance and substantial reduction of active power consumption, size, and weight — considerations particularly important in portable PCs and equipment. The iMC001FLKA's high performance read access time and command register microprocessor write interface allows for use of the flash memory system in an "execute-in-place" architecture. This configuration eliminates the need for the redundancy associated with DRAM and Disk memory system architectures. ROM based operating systems, such as Microsoft's MS-DOS ROM Version allow for "instant-on" capability. This enables the design of PCs that boot, operate, store data files, and execute application code from/to purely nonvolatile memory.

Flash write performance is often 50% higher than hard disks for typical user file storage. This equates to ten times more performance when compared to "spun-down" disks, the common practice for portable machines.

Flash filing systems enable the storage and modification of data files by allocating flash memory space intelligently, thus minimizing the number of rewrite cycles. This management function allows the user to rewrite reliably to the flash memory card many more times than a fixed or floppy disk which concentrate rewrite operations into small fixed portions of the medium.

Flash filing systems implement Intel's Flash Memory Card as a redirected disk drive; similar to structures used in local area networks. This enables the end user to interact with the flash memory card in precisely the same way as a magnetic disk. Filing systems that run under popular operating systems, such as MS-DOS, can use the installed base of application software.

The Microsoft Flash File System enables the storage and modification of data files by utilizing a linked list directory structure that is evenly distributed along with the data across the memory card. The linked list approach minimizes file fragmentation losses by using variable-sized data structures rather than the standard sector/cluster method of disk-based systems.

The integration of the PCMCIA/JEIDA 68-pin interface with flash filing systems enables the end-user to transport user files and application code between portable PCs and desktop PCs with memory card Reader/Writers. Intel Flash PC cards provide durable nonvolatile memory storage for Notebook PCs on the road, facilitating simple transfer back into the desktop environment.

For systems currently using a static RAM/battery configuration for data acquisition, the iMC001FLKA's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable computers and medical instruments, both requiring continuous operation. The iMC001FLKA consumes no power when the system is off. In addition, the iMC001FLKA offers a considerable cost and density advantage over memory cards based on static RAM with battery backup.

The flash memory card's electrical zone-erasure, byte writability, and complete nonvolatility fit well with data accumulation and recording needs. Electrical zone-erasure gives the designer the flexibility to selectively rewrite zones of data while saving other zones for infrequently updated look-up tables.

PRINCIPLES OF OPERATION

Intel's Flash Memory Card combines the functionality of two mainstream memory technologies: the rewritability of RAM and the nonvolatility of EPROM. The flash memory card consists of an array of individual memory devices, each of which defines a physical zone. The iMC001FLKA's memory devices erase as individual blocks, equivalent in size to the 128 K-Byte zone. Multiple zones can be erased simultaneously provided sufficient current for the appropriate number of zones (memory devices). Note, multiple zone erasure requires higher current from both the V_{PP} and V_{CC} power supplies. Erased zones can then be written in bit- or byte-at-a-time fashion and read randomly like RAM. Bit level write capability also supports disk emulation.

In the absence of high voltage on the $V_{PP1/2}$ pins, the iMC001FLKA remains in the read-only mode. Manipulation of the external memory card-control pins yields the standard read, standby, and output disable operations.

The same read, standby, and output disable operations are available when high voltage is applied to the $V_{PP1/2}$ pins. In addition, high voltage on $V_{PP1/2}$ enables erasure and rewriting of the accessed zone(s). All functions associated with altering zone contents — erase, erase verify, write, and write verify — are accessed via the command register.

Commands are written to the internal memory register(s), decoded by zone size, using standard microprocessor write timings. Register contents for a given zone serve as input to that zone's internal state-machine which controls the erase and rewrite circuitry. Write cycles also internally latch addresses and data needed for write and erase operations. With the appropriate command written to the register(s), standard microprocessor read timings output zone data, or output data for erase and write verification.

Byte-wide or Word-wide Selection

The flash memory card can be read, erased, and written in a byte-wide or word-wide mode. In the word-wide configuration V_{PP1} and/or $\overline{CE}_1$ control the LO-Byte (with $A_0 = O$) while V_{PP2} and $\overline{CE}_2$ control the HI-Byte (A_0 = don't care).

Read, Write, and Verify operations are byte- or word-oriented, thus zone independent. Erase Set-up and Begin Erase Commands are zone dependent such that commands written to any address within a 128 K-Byte zone boundary initiate the erase operation in that zone (or two 128 K-Byte zones under word-wide operation).

Conventional x8 operation uses $\overline{CE}_1$ active-low, with $\overline{CE}_2$ high, to read or write data through the D_0-D_7 only. "Even bytes" are accessed when A_0 is low, corresponding to the low byte of the complete x16 word. When A_0 is high, the "odd byte" is accessed by transposing the high byte of the complete x16 word onto the D_0-D_7 outputs. This odd byte corresponds to data presented on D_8-D_{15} pins in x16 mode.

Note that two zones logically adjacent in x16 mode are multiplexed through D_0-D_7 in x8 mode and are toggled by the A_0 address. Thus, zone specific erase operations must be kept discrete in x8 mode by addressing even bytes only for one-half of the zone pair, then addressing odd bytes only for the other half.

Card Detection

The flash memory card features two card detect pins ($\overline{CD}_{1/2}$) that allow the host system to determind if the card is properly loaded. Note that the two pins are located at opposite ends of the card. Each $\overline{CD}$ output should be read through a port bit. Should only one of the two bits show the card to be present, then the system should instruct the user to re-insert the card squarely into the socket. Card detection can also tell the system whether or not to redirect drives in the case of system booting. $\overline{CD}_{1/2}$ is active low, internally tied to ground.

Write Protection

The flash memory card features three types of write protection. The first type features a mechanical Write Protect Switch that disables the circuitry that control Write Enable to the flash devices. When the switch is activated, $\overline{WE}$ is forced high, which disables any writes to the Command Register. The second type of write protection is based on the PCMCIA/JEIDA socket. Unique pin length assignments provide protective power supply sequencing during hot insertion and removal. The third type operates via software control through the Command Register when the card resides in its connector. The Command Register of each zone is only active when $V_{PP1/2}$ is at high voltage. Depending upon the application, the system designer may choose to make $V_{PP1/2}$ power supply switchable — available only when writes are desired. When $V_{PP1/2} = V_{PPL}$, the contents of the register default to the read command, making the iMC001FLKA a read-only memory card. In this mode, the memory contents cannot be altered.

The system designer may choose to leave $V_{PP1/2} = V_{PPH}$, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage, V_{LKO}. (See the section on Power Up/Down Protection.) The iMC001FLKA is designed to accommodate either design practice, and to encourage optimization of the processor-memory card interface.

BUS OPERATIONS

Read

The iMC001FLKA has two control functions, both of which must be logically active, to obtain data at the outputs. Card Enable ($\overline{CE}$) is the power control and should be used for high and/or low zone(s) selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of accessed zone selection. In the byte-wide configuration, only one $\overline{CE}$ is required. The word-wide configuration requires both $\overline{CE}$s active low.

When $V_{PP1/2}$ is high (V_{PPH}), the read operations can be used to access zone data and to access data for write/erase verification. When $V_{PP1/2}$ is low (V_{PPL}), only read accesses to the zone data are allowed.

Output Disable

With Output Enable at a logic-high level (V_{IH}), output from the card is disabled. Output pins are placed in a high-impedance state.

Standby

With one Card Enable at a logic-high level, the standby operation disables one-half of the x16 output's read/write buffer. Further, only the zone corresponding to the selected address within the upper or lower $\overline{CE}_{1,2}$ bank is active at a time. (NOTE: A_0 must be low to select the low half of the x16 word when $\overline{CE}_2 = 1$ and $\overline{CE}_1 = 0$.) All other zones are deselected, substantially reducing card power consumption. For deselected banks, the outputs are placed in a high-impedance state, independent of the Output Enable signal. If the iMC001FLKA is deselected during erasure, writing, or write/erase verification, the accessed zone draws active current until the operation is terminated.

Int$_e$ligent Identifier™ Command

The manufacturer- and device-codes can be read via the Command Register, for instances where the iMC001FLKA is erased and rewritten in a universal reader/writer. Following a write of 90H to a zone's Command Register, a read from address location 00000H on any zone outputs the manufacturer code (89H). A read from address 0002H outputs the memory device code (B4H).

Write

Zone erasure and rewriting are accomplished via the Command Register, when high voltage is applied to $V_{PP1/2}$. The contents of the register serve as input to that zone's internal state-machine. The state-machine outputs dictate the function of the targeted zone.

The Command Register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The Command Register is written by bringing Write Enable to a logic-low level (V_{IL}), while Card Enable(s) is/are low. Addresses are latched on the falling edge of Write Enable, while data is latched on the rising edge of the Write Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Write Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin(s), the contents of the zone Command Register(s) default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin(s) enable(s) read/write operations. Zone operations are selected by writing specific data patterns into the Command Register. Tables 3 and 4 define these iMC001FLKA register commands for both byte-wide and word-wide configurations.

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Table 2. Bus Operations

	Pins / Operation	Notes	[1, 7] V_{PP2}	[1, 7] V_{PP1}	A0	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{OE}$	$\overline{WE}$	D_8-D_{15}	D_0-D_7
READ-ONLY	Read (x8)	8	V_{PPL}	V_{PPL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Even
	Read (x8)	9	V_{PPL}	V_{PPL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Odd
	Read (x8)	10	V_{PPL}	V_{PPL}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out	High Z
	Read (x16)	11	V_{PPL}	V_{PPL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data Out	Data Out
	Output Disable		V_{PPL}	V_{PPL}	X	X	X	V_{IH}	V_{IH}	High Z	High Z
	Standby		V_{PPL}	V_{PPL}	X	V_{IH}	V_{IH}	X	X	High Z	High Z
READ/WRITE	Read (x8)	3, 8	V_{PPX}	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Even
	Read (x8)	3, 9	V_{PPH}	V_{PPX}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Odd
	Read (x8)	10	V_{PPH}	V_{PPX}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out	High Z
	Read (x16)	3, 11	V_{PPH}	V_{PPH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data Out	Data Out
	Write (x8)	5, 8	V_{PPX}	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High Z	Data In-Even
	Write (x8)	9	V_{PPH}	V_{PPX}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High Z	Data In-Odd
	Write (x8)	10	V_{PPH}	V_{PPX}	X	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data In	High Z
	Write (x16)	11	V_{PPH}	V_{PPH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Data In	Data In
	Standby	4	V_{PPH}	V_{PPH}	X	V_{IH}	V_{IH}	X	X	High Z	High Z
	Output Disable		V_{PPH}	V_{PPH}	X	X	X	V_{IH}	V_{IL}	High Z	High Z

Notes:

1. Refer to DC Characteristics. When $V_{PP1/2} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. Read operations with $V_{PP1/2}$ = Vpph may access array data or the Inteligent Identifier codes.
4. With $V_{PP1/2}$ at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
5. Refer to Table 3 for valid Data-In during a write operation.
6. X can be V_{IL} or V_{IH}.
7. $V_{PPX} = V_{PPH}$ or V_{PPL}.
8. This x8 operation reads or writes the low byte of the x16 word on DQ_{0-7}, i.e., A_0 low reads "even" byte in x8 mode.
9. This x8 operation reads or writes the high byte of the x16 word on DQ_{0-7} (transposed from DQ_{8-15}), i.e., A_0 high reads "odd" byte in x8 mode.
10. This x8 operation reads or writes the high byte of the x16 on DQ_{8-15}. A_0 is "don't care."
11. A_0 is "don't care," unused in x16 mode. High and low bytes are presented simultaneously.

Table 3. Command Definitions byte-wide mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation[1]	Address[2]	Data[3]	Operation[1]	Address[2]	Data[3]
Read Memory		1	Write	X	00H			
Read Inteligent ID Codes	4	3	Write	IA	90H	Read		
Set-up Erase/Erase	5	2	Write	ZA	20H	Write	ZA	20H
Erase Verify	5	2	Write	EA	A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	40H	Write	WA	WD
Write Verify	6	2	Write	WA	C0H	Read	WA	WVD
Reset	7	2	Write	X	FFH	Write	X	FFH

Table 4. Command Definitions word-wide mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation[1]	Address[2]	Data[3]	Operation[1]	Address[2]	Data[3]
Read Memory		1	Write	X	0000H			
Read Inteligent ID Codes	4	3	Write	IA	9090H	Read		
Set-up Erase/Erase	5	2	Write	ZA	2020H	Write	ZA	2020H
Erase Verify	5	2	Write	EA	A0A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	4040H	Write	WA	WD
Write Verify	6	2	Write	WA	C0C0H	Read	WA	WVD
Reset	7	2	Write	X	FFFFH	Write	X	FFFFH

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Notes:

1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   WA = Address of memory location to be written.
   ZA = Address of 128 K-Byte zones involved in erase operation.
   Addresses are latched on the falling edge of the Write Enable pulse.
3. ID = Data read from location IA during device identification. (Mfr = 89H, Device = B4H).
   EVD = Data read from location EA during erase verify.
   WD = Data to be written at location WA. Data is latched on the rising edge of Write Enable.
   WVD = Data read from location WA during write verify. WA is latched on the Write command.
4. Following the Read Inteligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Erase Algorithm.
6. Figure 6 illustrates the Write Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While $V_{PP1/2}$ is high, for erasure and writing, zone memory contents can be accessed via the read command. The read operation is initiated by writing 00H (0000H for the word-wide configuration) into the zone Command Register(s). Microprocessor read cycles retrieve zone data. The accessed zone remains enabled for reads until the Command Register(s) contents are altered.

The default contents of each zone's register(s) upon $V_{PP1/2}$ power-up is 00H (00000H for word-wide). This default value ensures that no spurious alteration of memory card contents occurs during the $V_{PP1/2}$ power transition. Where the $V_{PP1/2}$ supply is left at V_{PPH}, the memory card powers-up and remains enabled for reads until the command Register contents of targeted zones are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier Command

Each zone of the iMC001FLKA contains an int$_e$ligent Identifier to identify memory card device characteristics. The operation is initiated by writing 90H (9090H for word-wide) into the Command Register(s). Following the command write, a read cycle from address 00000H retrieves the manufacturer code 89H (8989H for word-wide). A read cycle from address 0002H returns the device code B4H (B4B4H for word-wide). To terminate the operation, it is necessary to write another valid command into the register(s).

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the targeted zone(s) for electrical erasure of all bytes in the zone. The set-up erase operation is performed by writing 20H to the Command Register (2020H for word-wide).

To commence zone-erasure, the erase command (20H or 2020H) must again be written to the register(s). The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that zone memory contents are not accidentally erased. Also, zone-erasure can only occur when high voltage is applied to the $V_{PP1/2}$ pins. In the absence of this high voltage, zone memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the zone in parallel. After each erase operation, all bytes in the zone must be individually verified. In byte-mode operations, zones are segregated by A_0 in odd and even banks; erase and erase verify operations must be done in complete passes of even-bytes-only then odd-bytes-only. See the Erase Algorithm for byte-wide mode. The erase verify operation is initiated by writing A0H (A0A0H for word-wide) into the Command Register(s). The address for the byte(s) to be verified must be supplied as it is latched on the falling edge of the Write Enable pulse. The register write terminates the erase operation with the rising edge of its Write Enable pulse.

The enabled zone applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. Similarly, reading FFFFH from the addressed word indicates that all bits in the word are erased.

The erase-verify command must be written to the Command Register prior to each byte (word) verification to latch its address. The process continues for each byte (word) in the zone(s) until a byte (word) does not return FFH (FFFFH) data, or the last address is accessed.

In the case where the data read is not FFH (FFFFH), another erase operation is performed. (Refer to Set-up Erase/Erase.) Verification then resumes from the address of the last-verified byte (word). Once all bytes (words) in the zone(s) have been verified, the erase step is complete. The accessed zone can now be written. At this point, the verify operation is terminated by writing a valid command (e.g., Write Set-up) to the Command Register. The Erase algorithms for byte-wide and word-wide configurations illustrate how commands and bus operations are combined to perform electrical erasure of the iMC001FLKA. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Write/Write Commands

Set-up write is a command-only operation that stages the targeted zone for byte writing. Writing 40H (4040H) into the Command Register(s) performs the set-up operation.

Once the write set-up operation is performed, the next Write Enable pulse causes a transition to an active write operation. Addresses are internally latched on the falling edge of the Write Enable pulse. Data is internally latched on the rising edge of the Write Enable pulse. The rising edge of Write Enable also begins the write operation. The write operation terminates with the next rising edge of Write Enable, which is used to write the verify command. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Write Verify Command

The iMC001FLKA is written on a byte-by-byte or word-by-word basis. Byte or word writing may occur sequentially or at random. Following each write operation, the byte or word just written must be verified.

The write-verify operation is initiated by writing C0H (C0C0) into the Command Register(s). The register write(s) terminate(s) the write operation with the rising edge of its Write Enable pulse. The write-verify operation stages the accessed zone(s) for verification of the byte or word last written. No new address information is latched. The zone(s) apply(ies) an internally-generated margin voltage to the byte or word. A microprocessor read cycle outputs the data. A successful comparison between the written byte or word and true data means that the byte or word is successfully written. The write operation then proceeds to the next desired byte or word location. The Write algorithms for byte-wide and word-wide configurations illustrate how commands are combined with bus operations to perform byte and word writes. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or write-command sequences. Following either set-up command (erase or write) with two consecutive writes of FFH (FFFFH for word-wide) will safely abort the operation. Zone memory contents will not be altered. A valid command must then be written to place the accessed zone in the desired state.

EXTENDED ERASE/WRITE CYCLING

Intel has designed extended cycling capability into its ETOX II flash memory technology enabling a flash memory card with a MTBF that is approximately 20 times more reliable than rotating disk technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field minimizes the probability of oxide defects in the region. The lower electric field greatly reduces oxide stress and the probability of failure.

WRITE ALGORITHMS

The write algorithm(s) use write operations of 10μs duration. Each operation is followed by a byte or word verification to determine when the addressed byte or word has been successfully written. The algorithm(s) allows for up to 25 write operations per byte or word, although most bytes and words verify on the first or second operation. The entire sequence of writing and byte/word verification is performed with V_{PP} at high voltage.

ERASE ALGORITHM

The Erase algorithm(s) yield(s) fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the write algorithm, to simultaneously remove charge from all bits in the accessed zone(s).

Erasure begins with a read of memory zone contents. Reading FFH (FFFFH) data from the accessed zone(s) can be immediately followed by writing to the desired zone(s).

For zones being erased and rewritten, uniform and reliable erasure is ensured by first writing all bits in the accessed zone to their charged state (data = 00H byte-wide, 00000H word-wide). This is accomplished, using the write algorithm, in approximately two seconds per zone.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH byte-wide, FFFFH word-wide) begins at address 00000H and continues through the zone to the last address, or until data other than FFH (FFFFH) is encountered. (Note: byte-wide erase operation requires separate even- and odd-address passes to handle the individual 128 K-Byte zones.) With each erase operation, an increasing number of bytes or words verify to the erased state. Erase efficiency may be improved by storing the address of the last byte or word verified in a register(s). Following the next erase operation, verification starts at that stored address location. Follow this procedure until all bytes in the zone are erased. Then, re-start the procedure for the next zone or word-wide zone pair. Erasure typically occurs in one second per zone.

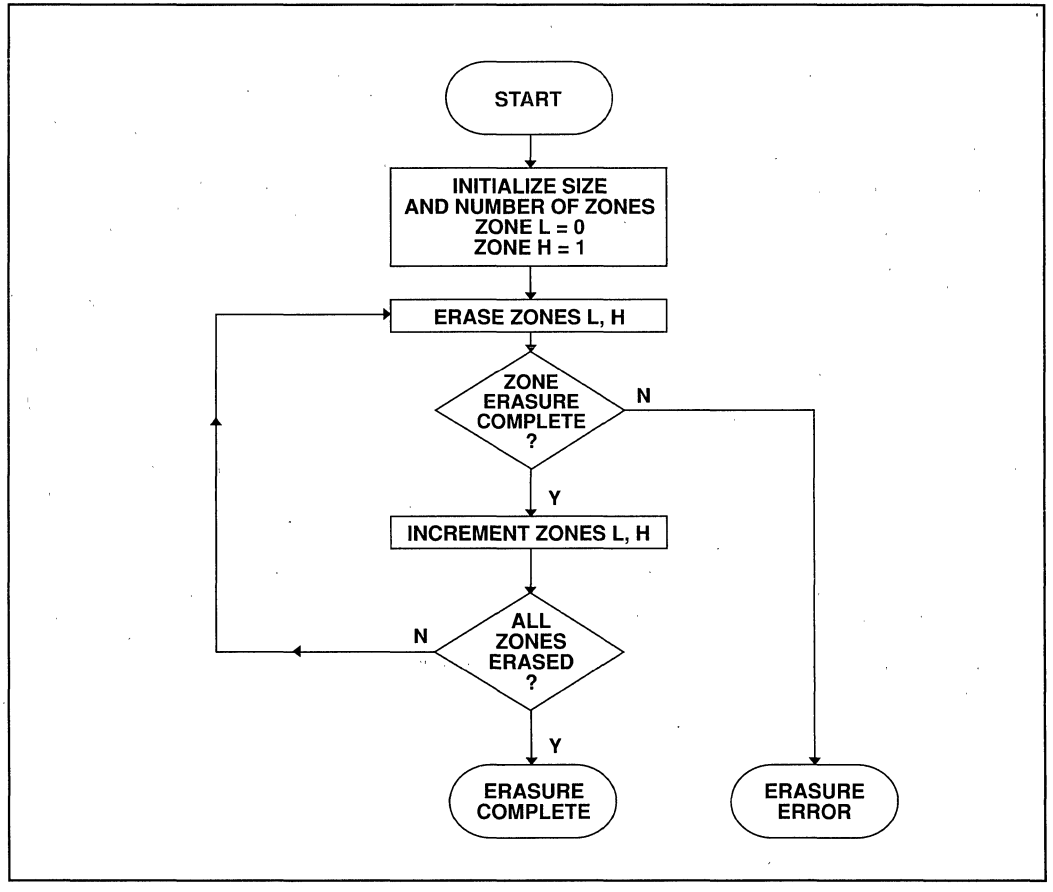
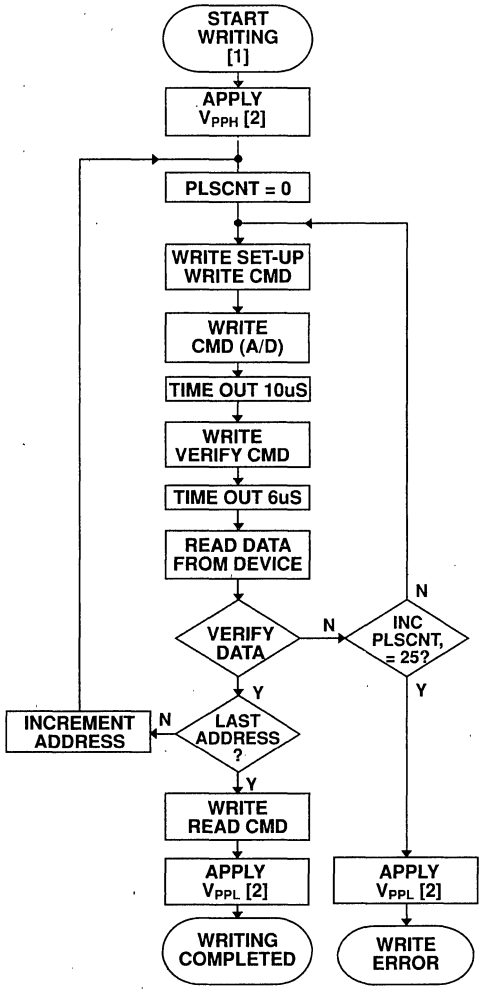


Figure 3. Full Card Erase Flow



BUS OPERATION	COMMAND	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [2]
		Initialize pulse-count
Write	Set-up Write	Data = 40H
Write	Write	Valid address/data
Standby		Duration Of Write operation (t_{WHWH1})
Write	Write Verify [3]	Data = C0H; Stops [4] Write Operation
Standby		t_{WHGL}
Read		Read byte to verify Write Operation
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [2]

Notes:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
3. Write Verify is only performed after a byte write operation. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 4. Write Algorithm for byte-wide mode

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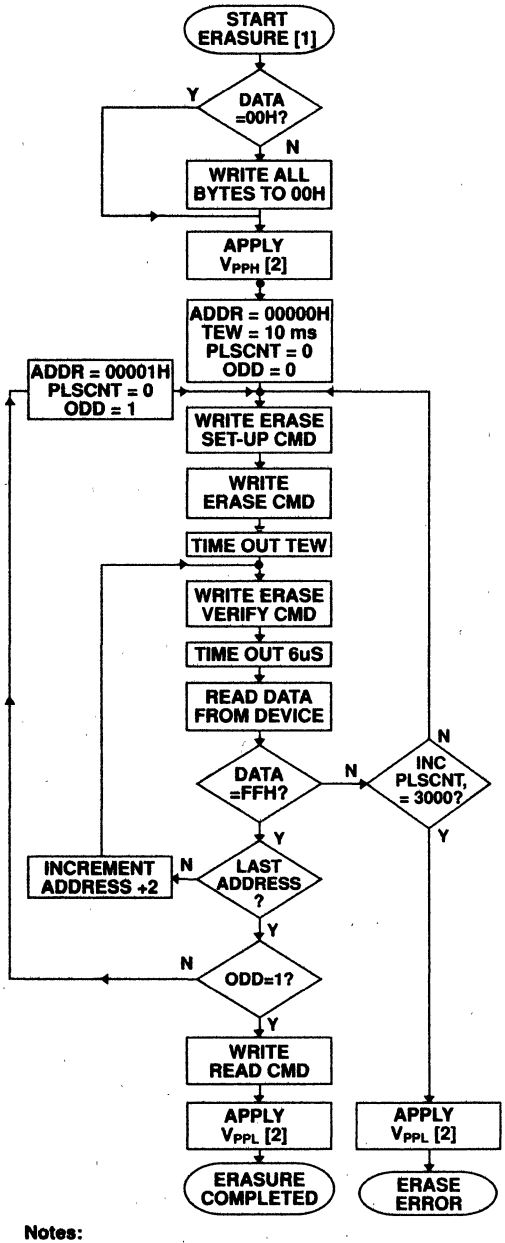


BUS OPERATION	COMMANDS	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [2]
		Use Write Operation Algorithm
		Initialize even/odd Addresses, Erase Pulse Width, and Pulse Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify [3]	Addr = Byte to verify; Data = A0H; Stops Erase Operation [4] t_{WHGL}
Standby		
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [2]

Notes:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
3. Erase Verify is only performed after chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 5. Erase Algorithm for byte-wide mode

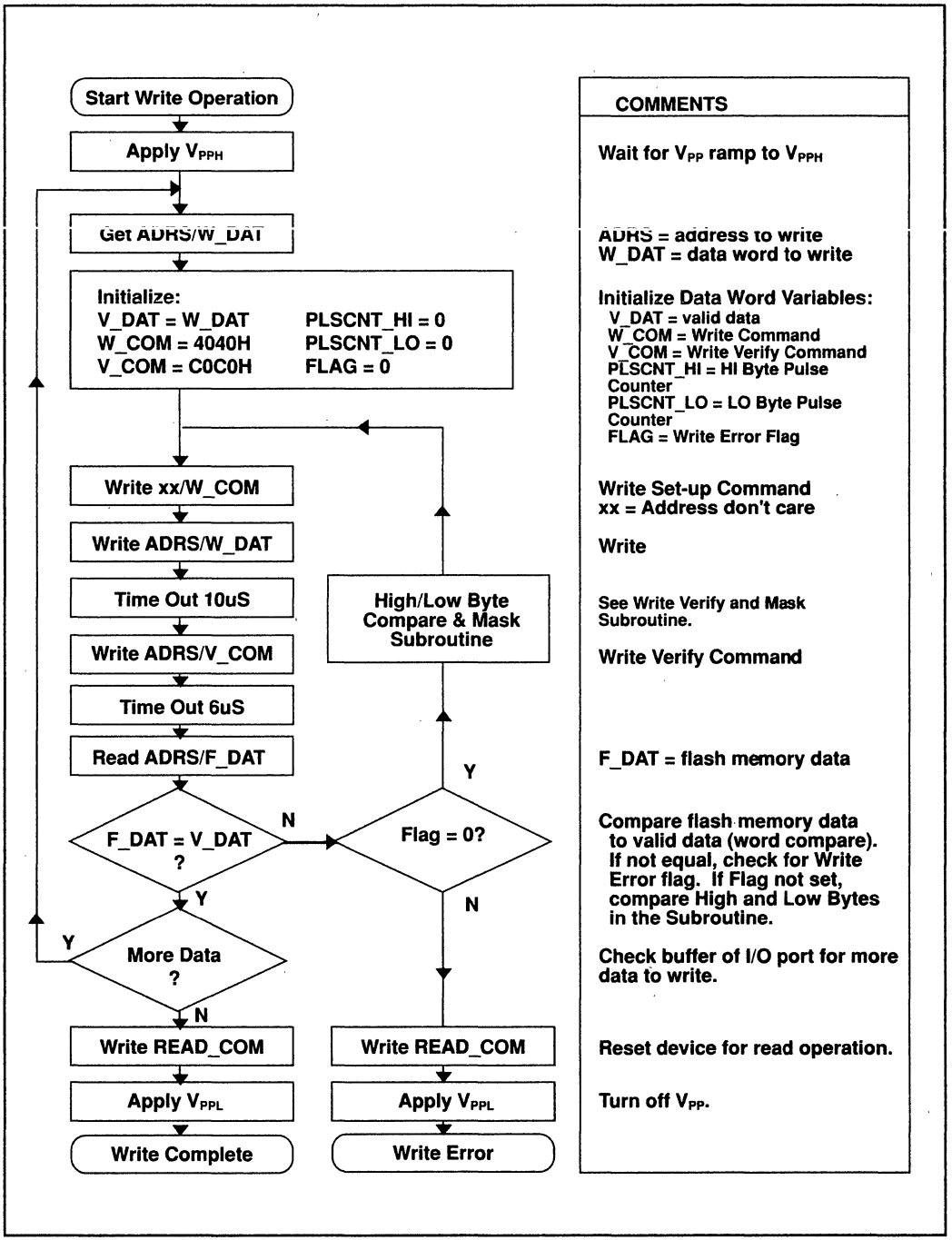


Figure 6. Write Algorithm for word-wide mode

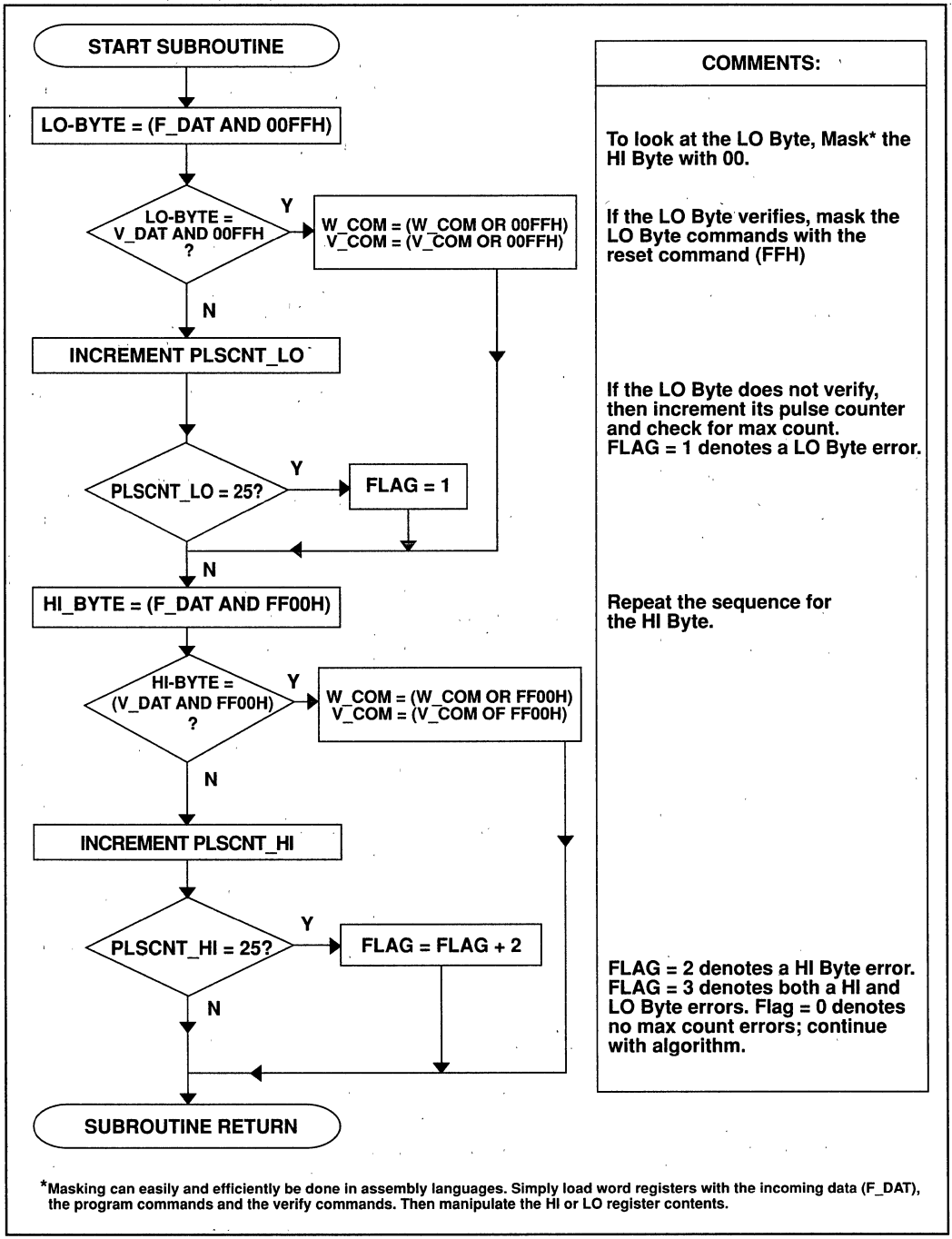
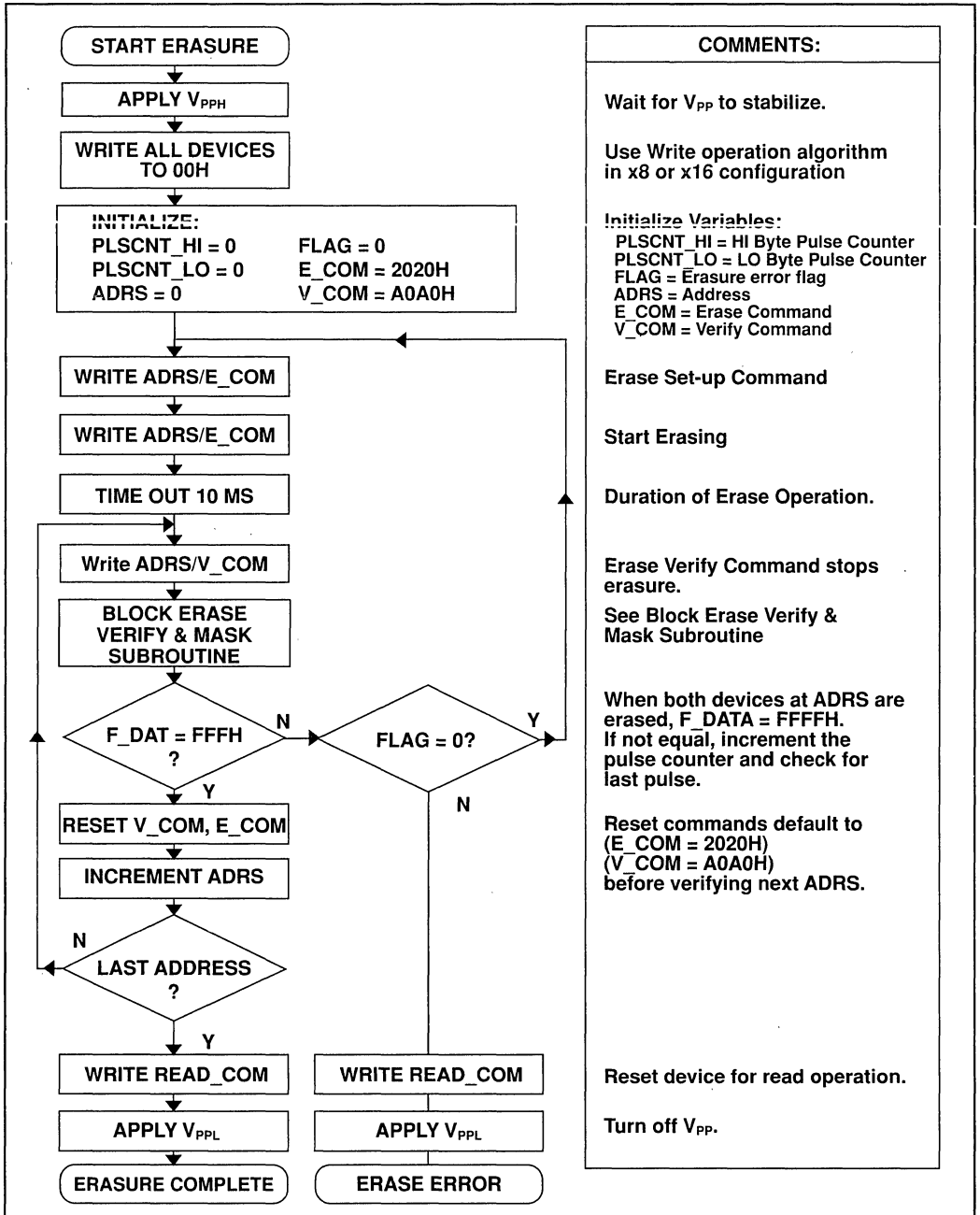


Figure 7. Write Verify and Mask Subroutine for word-wide mode



NOTES:
X16 Addressing uses A_1-A_{19} only. A_0=0 throughout word-wide operation.

Figure 8. Erase Algorithm for word-wide mode

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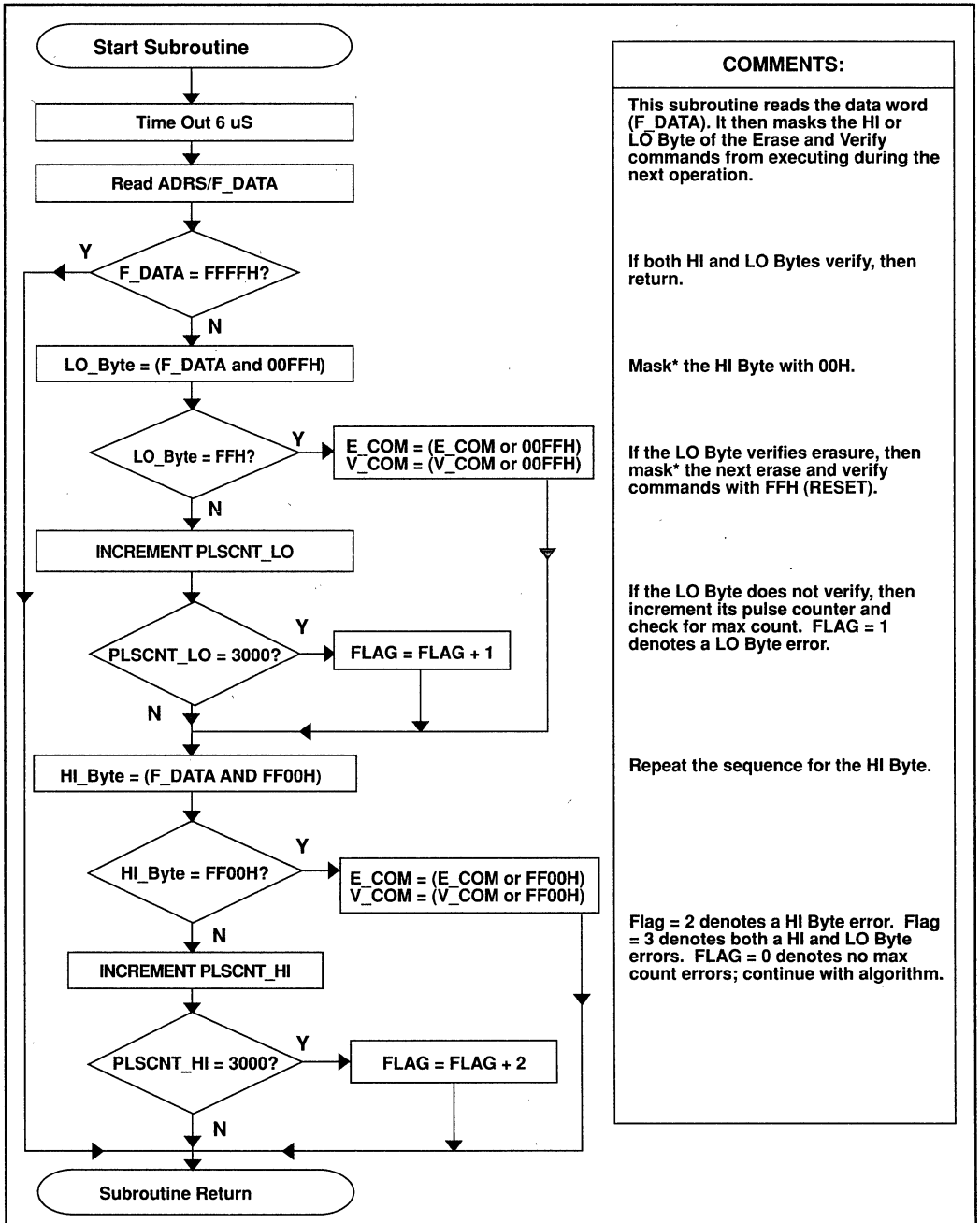

*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Figure 9. Erase Verify and Mask Subroutine for word-wide mode.

SYSTEM DESIGN CONSIDERATIONS

Three-Line Control

Three-line control provides for:

a. the lowest possible power dissipation and,

b. complete assurance that output bus contention will not occur.

To efficiently use these three control inputs, an address-decoder output should drive $\overline{CE}_{1,2}$, while the system's Read signal controls the card $\overline{OE}$ signal, and other parallel zones. This, coupled with the internal zone decoder, assures that only enabled memory zones have active outputs, while deselected zones maintain the low power standby condition.

Power-Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues — standby, active and transient current peaks, produced by falling and rising edges of $\overline{CE}_{1/2}$. The capacitive and inductive loads on the card and internal flash memory zones determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The iMC001FLKA features on-card ceramic decoupling capacitors connected between V_{CC} and V_{SS}, and between V_{PP1}/V_{PP2} and V_{SS}.

The card connector should also have a 4.7μF electrolytic capacitor between V_{CC} and V_{SS}, as well as between V_{PP1}/V_{PP2} and V_{SS}. The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

Power Up/Down Protection

The PCMCIA/JEIDA socket is specified, via unique Pin lengths, to properly sequence the power supplies to the flash memory card. This assures that hot insertion and removal will not result in card damage or data loss.

Each zone in the iMC001FLKA is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}_{1,2}$ must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of zone contents only occurs after successful completion of the two-step command sequences.

While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady state value before raising $V_{PP1/2}$ above $V_{CC}+2.0V$. In addition, upon powering-down, $V_{PP1/2}$ should be below $V_{CC}+2.0V$, before lowering V_{CC}.

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
  During Read ..... 0°C to + 60°C(1)
  During Erase/Write ..... 0°C to + 60°C
Temperature Under Bias ..... −10°C to + 70°C
Storage Temperature ..... −30°C to + 70°C
Voltage on Any Pin with
  Respect to Ground ..... −2.0V to + 7.0V(2)
V_{PP1}/V_{PP2} Supply Voltage with
  Respect to Ground
  During Erase/Write ..... −2.0V to + 14.0V(2,3)
V_{CC} Supply Voltage with
  Respect to Ground ..... −2.0V to + 7.0V(2)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the card. This is a stress rating only and functional operation of the card at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect card reliability.

NOTICE: Specifications contained within the following tables are subject to change.

Notes:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V for periods less than 20 ns.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	60	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.75	5.25	V	
V_{PPH}	Active V_{PP1}, V_{PP2} Supply Voltages	11.40	12.60	V	
V_{PPL}	V_{PP} During Read Only Operations	0.00	6.50	V	

DC CHARACTERISTICS — Byte Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Condition
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		0.4	0.8	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1,2		25	50	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IL}$ f = 6MHz, I_{OUT} = 0mA
I_{CC2}	V_{CC} Write Current	1,2		1.0	10.0	mA	Writing in progress
I_{CC3}	V_{CC} Erase Current	1,2		5.0	15	mA	Erasure in progress
I_{CC4}	V_{CC} Write Verify Current	1,2		5.0	15	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{CC5}	V_{CC} Erase Verify Current	1,2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
I_{PPS}	V_{PP} Leakage Current	1			±40	uA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	1,3		0.4	0.8	mA	$V_{PP} > V_{CC}$
					±.04		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Write Current	1,3		8.0	30	mA	$V_{PP} = V_{PPH}$ Write in progress
I_{PP3}	V_{PP} Erase Current	1,3		10	30	mA	$V_{PP} = V_{PPH}$ Erasure in progress
I_{PP4}	V_{PP} Write Verify Current	1,3		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{PP5}	V_{PP} Erase Verify Current	1,3		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Low Voltage				0.40	V	I_{OL} = 3.2mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		3.8			V	I_{OH} = −2.0mA $V_{CC} = V_{CC}$ min
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write lock voltage		2.5			V	

Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25° C.
2. 1 chip active and 7 in standby for byte-wide mode.
3. Assumes 1 V_{PP} is active.

6

DC CHARACTERISTICS — Word Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Condition
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		0.4	0.8	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1,2		40	80	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IL}$ f = 6MHz, I_{OUT} = 0mA
I_{CC2}	V_{CC} Write Current	1,2		2.0	20	mA	Writing in progress
I_{CC3}	V_{CC} Erase Current	1,2		10	30	mA	Erasure in progress
I_{CC4}	V_{CC} Write Verify Current	1,2		10	30	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{CC5}	V_{CC} Erase Verify Current	1,2		10	30	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
I_{PPS}	V_{PP} Leakage Current	1			±80	uA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	1,3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					±.08		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Write Current	1,3		16	60	mA	$V_{PP} = V_{PPH}$ Write in progress
I_{PP3}	V_{PP} Erase Current	1,3		20	60	mA	$V_{PP} = V_{PPH}$ Erasure in progress
I_{PP4}	V_{PP} Write Verify Current	1,3		5.0	12	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{PP5}	V_{PP} Erase Verify Current	1,3		5.0	12	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Low Voltage				0.40	V	I_{OL} = 3.2mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		3.8			V	I_{OH} = −2.0mA $V_{CC} = V_{CC}$ min
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write lock voltage		2.5			V	

Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25° C.
2. 2 chips active and 6 in standby for word-wide mode.
3. Assumes 2 V_{PP}s are active.

CAPACITANCE T = 25° C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN1}	Address Capacitance			8	pF	V_{IN} = 0V
C_{IN2}	Control Capacitance			16	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			21	pF	V_{OUT} = 0V
$C_{I/O}$	I/O Capacitance			16	pF	$V_{I/O}$ = 0V

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... Vol and Voh1
Input Timing Reference Level ..... Vil and Vih
Output Timing Reference Level ..... Vil and Vih

AC CHARACTERISTICS — Read-Only Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{RC}	Read Cycle Time	2	250		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time	2		250	ns
t_{AVQV}/t_{ACC}	Address Access Time	2		250	ns
t_{GLQV}/t_{OE}	Output Enable Access Time	2		120	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	2	5		ns
t_{EHQZ}	Chip Disable to Output in High Z	2		60	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	2	5		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	2		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change	1,2	5		ns
t_{WHGL}	Write Recovery Time Before Read	2	6		us

Notes:
1. Whichever occurs first.
2. Rise/Fall time ≤ 10ns.

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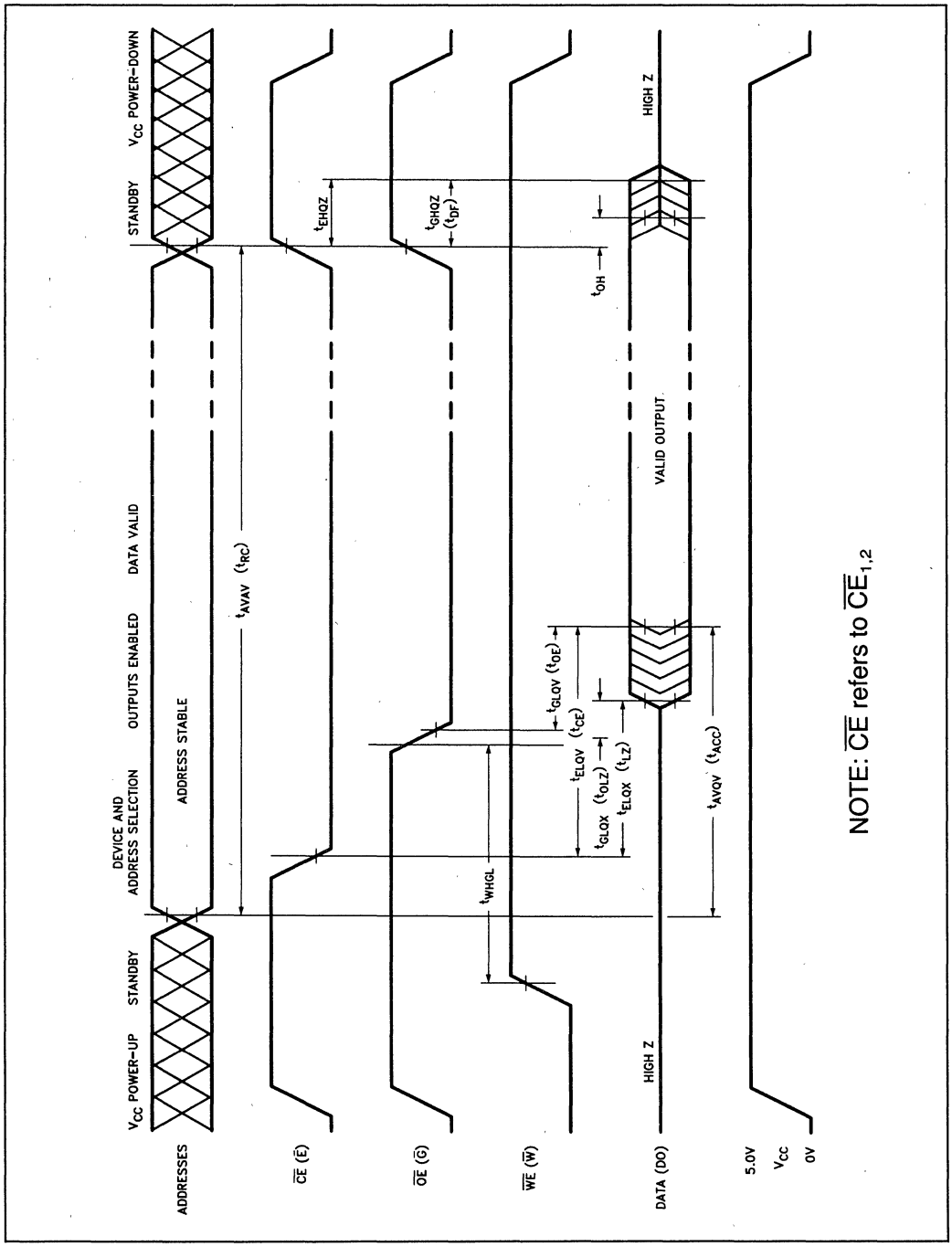


Figure 10. AC Waveforms for Read Operations

AC CHARACTERISTICS — For Write/Erase Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{WC}	Write Cycle Time	1,2	250		ns
t_{AVWL}/t_{AS}	Address Set-up Time	1,2	0		ns
t_{WLAX}/t_{AH}	Address Hold Time	1,2	100		ns
t_{DVWH}/t_{DS}	Data Set-up Time	1,2	80		ns
t_{WHDX}/t_{DH}	Data Hold Time	1,2	30		ns
t_{WHGL}	Write Recovery Time Before Read	1,2	6		us
t_{GHWL}	Read Recovery Time Before Write	1,2	0		us
t_{WLOZ}	Output High-Z from Write Enable	1,2	5		ns
t_{WHOX}	Output Low-Z from Write Enable	1,2		60	ns
t_{ELWL}/t_{CS}	Chip Enable Set-up Time Before Write	1,2	40		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	1,2	0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	1,2	100		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	1,2	20		ns
t_{WHWH1}	Duration of Write Operation	1,2,3	10		us
t_{WHWH2}	Duration of Erase Operation	1,2,3	9.5		ms
t_{VPEL}	V_{PP} Set-up Time to Chip Enable Low	1,2	100		ns

Notes:

1. Read timing parameters during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10ns.
3. The integrated stop timer terminates the write/erase operations, thereby eliminating the need for a maximum specification.

6

ERASE/WRITE PERFORMANCE

Parameter	Notes	Min	Typ	Max	Unit
Zone Erase Time	1,3,4		1.0	10	sec
Zone Write Time	1,2,4		2.0	12.5	sec
MTBF	5		10^6		Hrs

Notes:

1. 25° C, 12.0V V_{PP}.
2. Minimum byte writing time excluding system overhead is 16 usec (10 usec program + 6 usec write recovery), while maximum is 400 usec/byte (16 usec x 25 loops allowed by algorithm). Max chip write time is specified lower than the worst case allowed by the write algorithm since most bytes write significantly faster than the worst case byte.
3. Excludes 00H writing Prior to Erasure.
4. One zone equals 128K Bytes.
5. MTBF = Mean Time Between Failure, 50% failure point for disk drives.

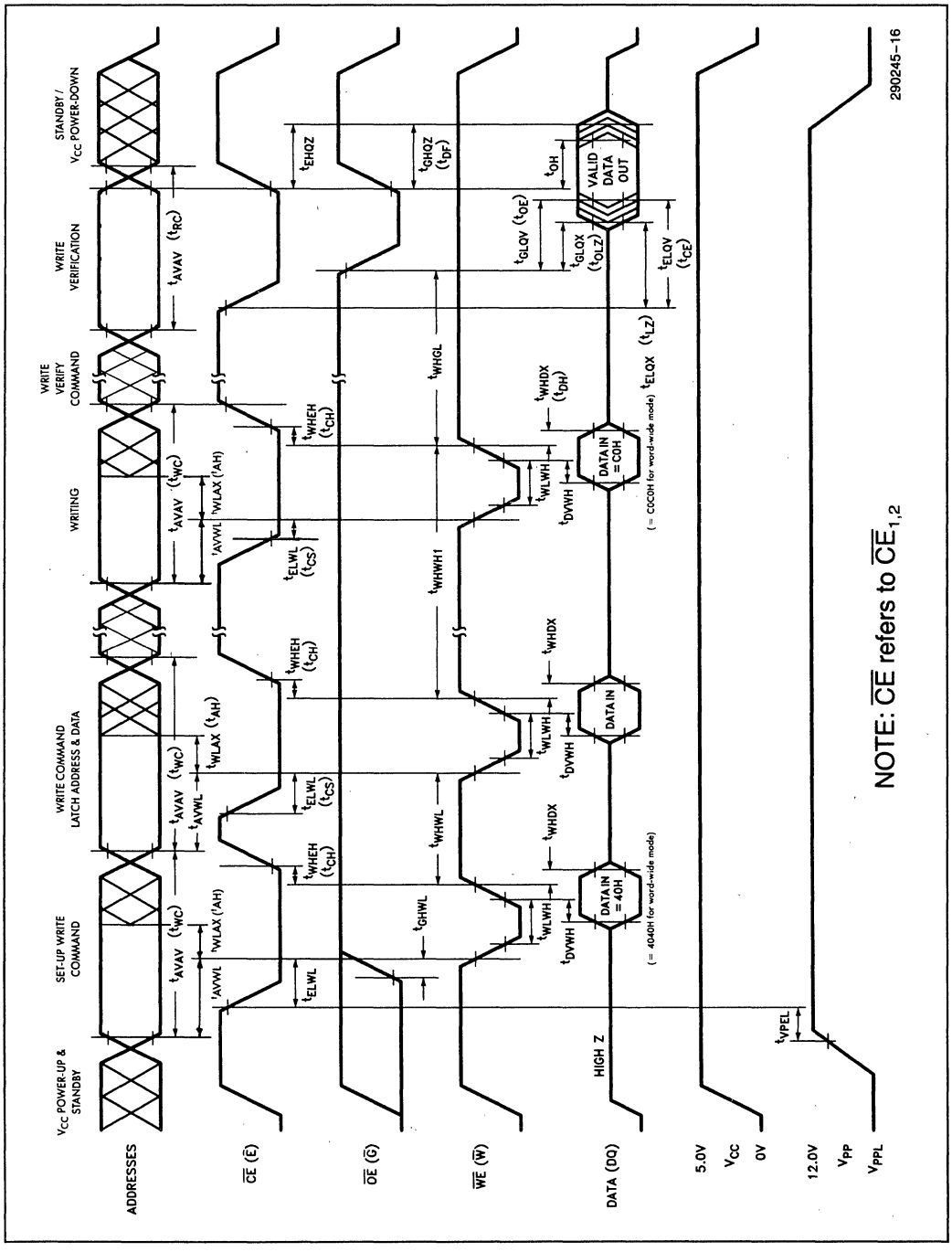


Figure 11. AC Waveforms for Write Operations

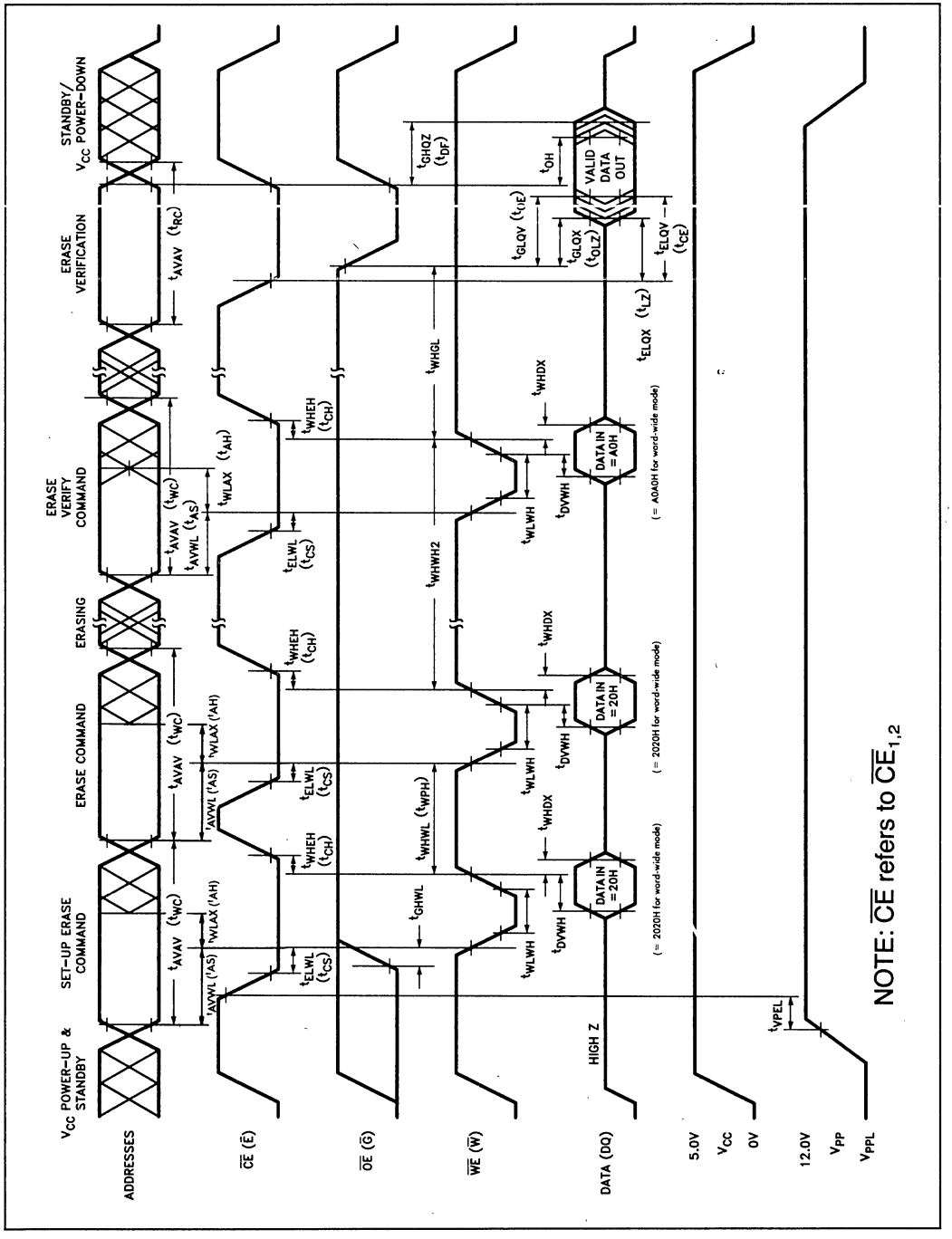


Figure 12. AC Waveforms for Erase Operations

6

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		250		ns
t_{AVEL}	Address Set-up Time		0		ns
t_{ELAX}	Address Hold Time		100		ns
t_{DVEH}	Data Set-up Time		80		ns
t_{EHDX}	Data Hold Time		30		ns
t_{EHGL}	Write Recovery Time Before Read		6		us
t_{GHEL}	Read Recovery Time Before Write		0		us
t_{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		ns
t_{EHWH}	Write Enable Hold Time		0		ns
t_{ELEH}	Write Pulse Width	1	100		ns
t_{EHEL}	Write Pulse Width High		20		ns
t_{PEL}	V_{PP} Set-Up Time to Chip-Enable Low		100		ns

Notes:

1. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width (with a longer Write Enable timing waveform) all set-up, hold and inactive Write Enable times should be measured relative to the Chip Enable waveform.

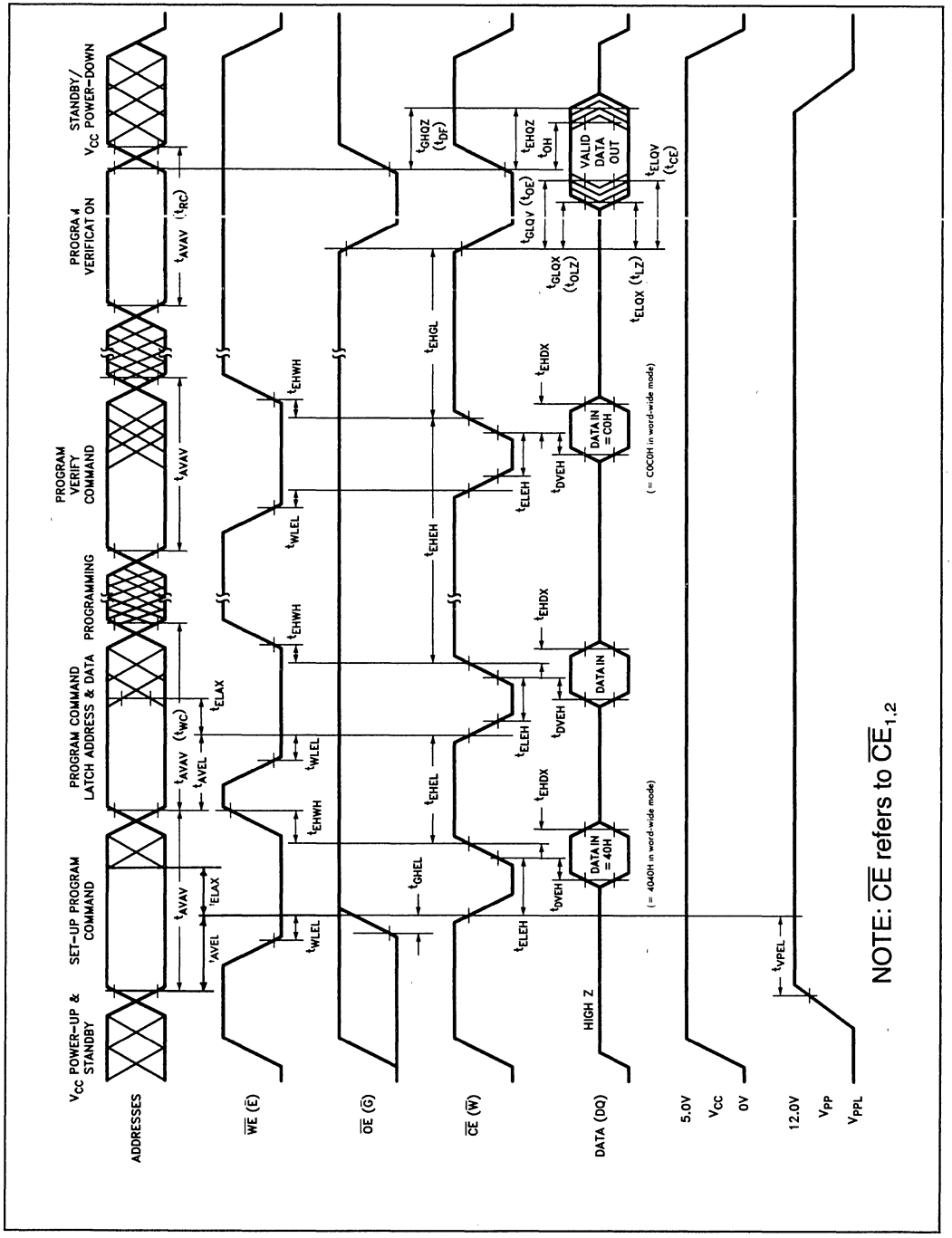
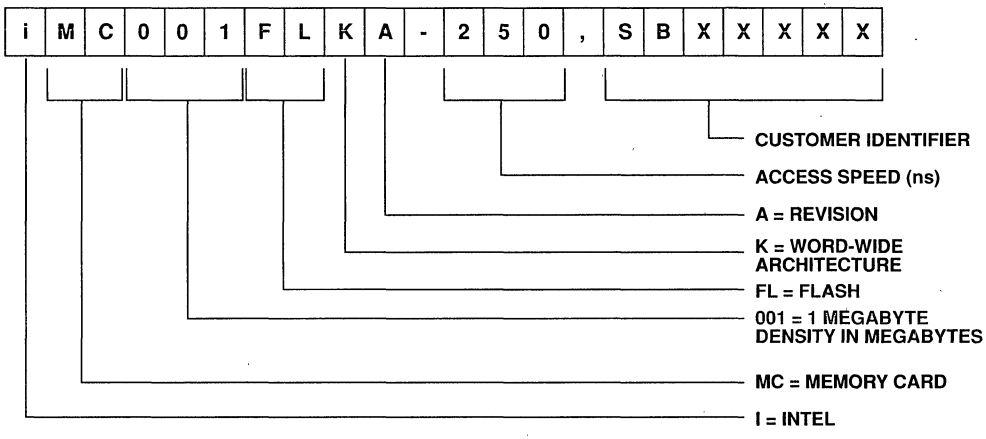


Figure 13. Alternate AC Waveforms for Write Operations

ORDERING INFORMATION



ADDITIONAL INFORMATION	Order Number
ER-20, "ETOX II Flash Memory Technology"	294005
RR-60, "ETOX II Flash Memory Reliability Data Summary"	293002
AP-343, "Solutions for High Density Applications using Flash Memory"	292079

iMC004FLKA
4-MEGABYTE FLASH MEMORY CARD

- Inherent Nonvolatility (Zero Retention Power)
  - No Batteries Required for Back-up
- Over 1,000,000 Hours MTBF
  - More Reliable than Disk
- High-Performance Read
  - 250 ns Maximum Access Time
- CMOS Low Power Consumption
  - 40 mA Typical Active Current (X8)
  - 800 μA Typical Standby Current
- Flash Electrical Zone-Erase
  - 2 Seconds Typical per 256 K-Byte Zone
  - Multiple Zone-Erase
- Random Writes to Erased Zones
  - 10 μs Typical Byte Write
- Write Protect Switch to Prevent Accidental Data Loss
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- ETOX™ II Flash Memory Technology
  - 5V Read, 12V Erase/Write
  - High-Volume Manufacturing Experience
- PCMCIA/JEIDA 68-Pin Standard
  - Byte- or Word-wide Selectable
- Independent Software & Hardware Vendor Support
  - Integrated System Solution Using Flash Filing Systems

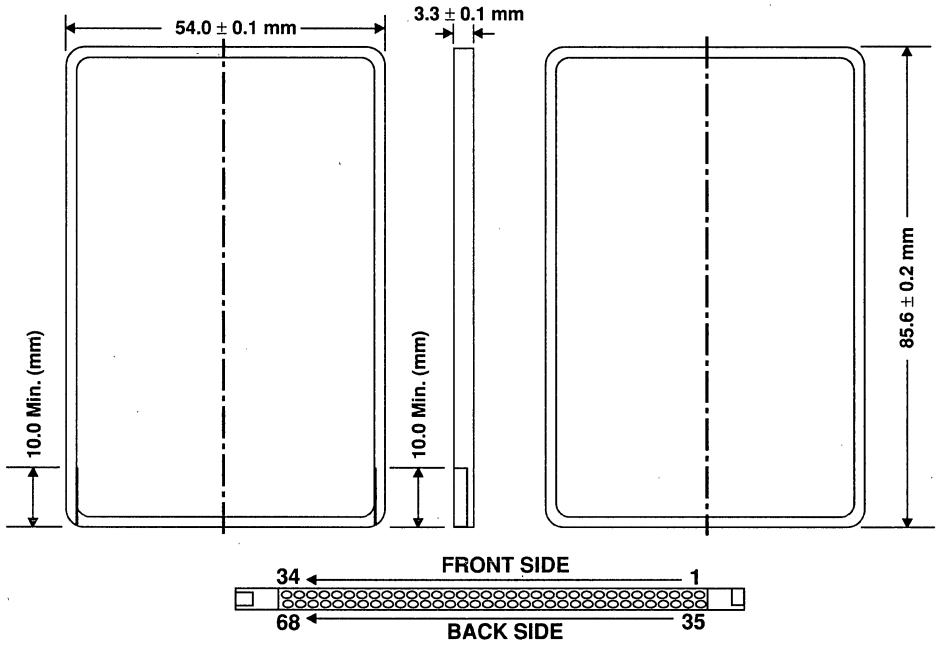
Intel's Flash Memory Card is the integrated memory solution for portable PCs. The iMC004FLKA enables OEM system manufacturers to design portable PCs that no longer require rotating electro-mechanical media to store application code and data files. This allows the design and manufacture of PCs that are higher performance, more rugged, consume less battery power, and weigh much less than traditional disk-based portable PCs. The flash memory card supports the emerging "Mobile Office" by allowing the user to transport both application code and data files between desktop PCs and portables.

The iMC004FLKA conforms to the PCMCIA/JEIDA international standard, providing standardization at the hardware and data interchange level. OEMs may opt to write the Card Information Structure (CIS) at the memory card's address 00000H with a format utility. This information provides data interchange functional capability. The 250 nanosecond access time allows for "execute-in-place" capability, for popular low-power microprocessors. Intel's 4-Megabyte Flash Memory Card operates in a byte-wide and word-wide configuration providing performance/power options for different systems.

Intel's Flash Memory card employs Intel's ETOX II Flash Memories. Filing systems, such as Microsoft's* Flash File System (FFS), facilitate sequential data file storage and card erasure using a purely nonvolatile medium. Flash filing systems, coupled with the Intel Flash Memory Card, effectively create an all-silicon nonvolatile read/write random access memory system that is more reliable and higher performance than disk-based memory systems.

*Microsoft is a trademark of Microsoft Corp.

Order Number: 290388-001



1	GND
2	D_3
3	D_4
4	D_5
5	D_6
6	D_7
7	$\overline{CE}_1$
8	A_{10}
9	$\overline{OE}$
10	A_{11}
11	A_9
12	A_8
13	A_{13}
14	A_{14}
15	$\overline{WE}$
16	NC
17	V_{cc}

18	V_{pp1}
19	A_{16}
20	A_{15}
21	A_{12}
22	A_7
23	A_6
24	A_5
25	A_4
26	A_3
27	A_2
28	A_1
29	A_0
30	D_0
31	D_1
32	D_2
33	WP
34	GND

35	GND
36	$\overline{CD}_1$
37	D_{11}
38	D_{12}
39	D_{13}
40	D_{14}
41	D_{15}
42	$\overline{CE}_2$
43	NC
44	NC
45	NC
46	A_{17}
47	A_{18}
48	A_{19}
49	A_{20}
50	A_{21}
51	V_{cc}

52	V_{pp2}
53	NC
54	NC
55	NC
56	NC
57	NC
58	NC
59	NC
60	NC
61	$\overline{REG}$[1]
62	$\overline{BVD}_2$[2]
63	$\overline{BVD}_1$[2]
64	D_8
65	D_9
66	D_{10}
67	$\overline{CD}_2$
68	GND

NOTES:
1. $\overline{REG}$ = register memory select = No Connect (NC), unused. When $\overline{REG}$ is brought low, PCMCIA/JEIDA standard card information structure data is expected. This is accomplished by formatting the card with this data.
2. $\overline{BVD}$ = battery detect voltage = No Connect (NC), unused.

Figure 1. iMC004FLKA Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0-A_{21}	INPUT	**ADDRESS INPUTS** for memory locations. Addresses are internally latched during a write cycle.
D_0-D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the card is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE:** activates the card's high and low byte control logic, input buffers, zone decoders, and associated memory devices. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory card and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** gates the cards output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE** controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. Note: With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP1}, V_{PP2}		**ERASE/WRITE POWER SUPPLY** for writing the command register, erasing the entire array, or writing bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ± 5%).
GND		**GROUND**
$\overline{CD}_1$, $\overline{CD}_2$	OUTPUT	**CARD DETECT.** The card is detected at $\overline{CD}_{1,2}$ = ground.
WP	OUTPUT	**WRITE PROTECT.** All write operations are disabled with WP = active high.
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.
$\overline{BVD}_1$, $\overline{BVD}_2$	OUTPUT	**BATTERY VOLTAGE DETECT. NOT REQUIRED.**

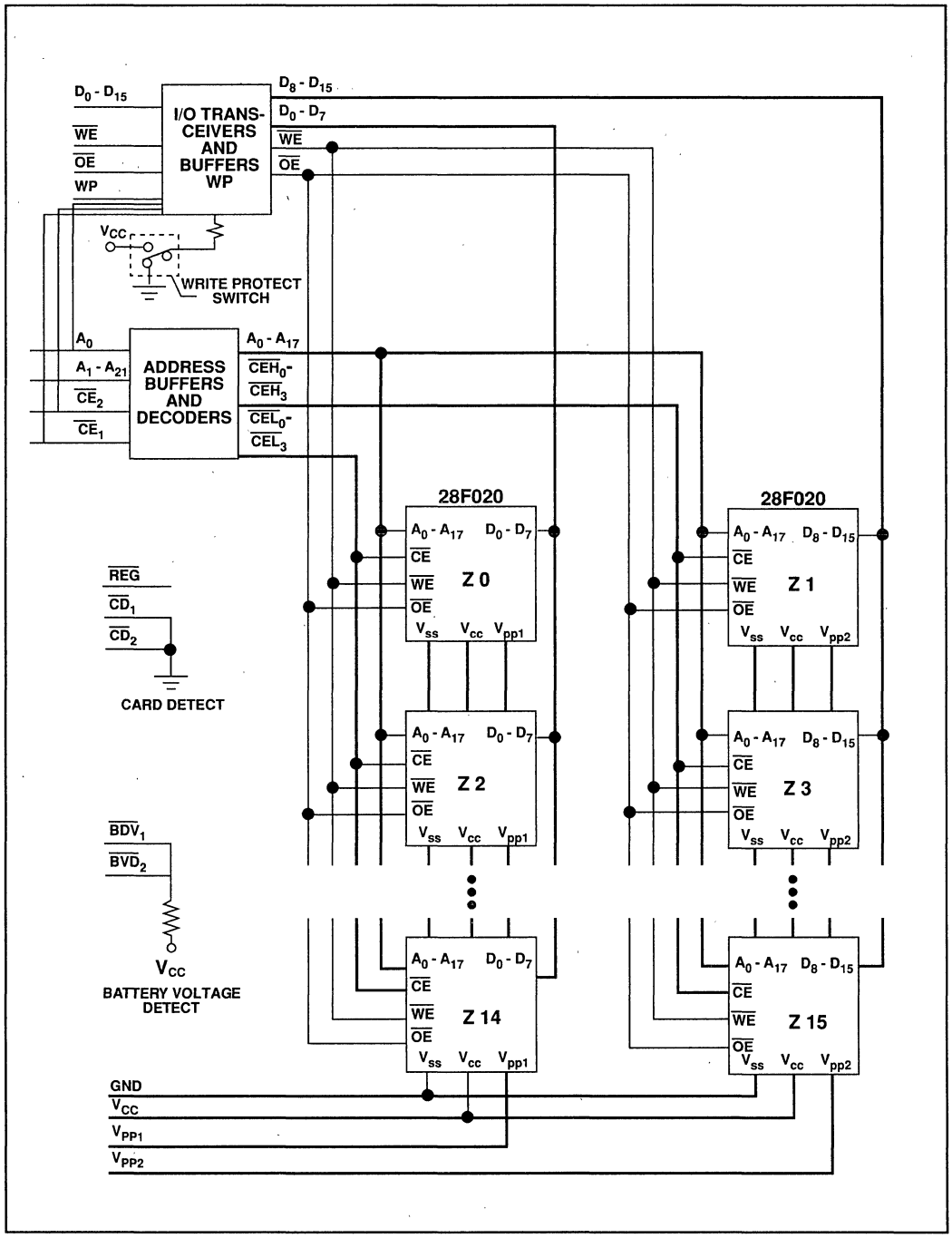


Figure 2. iMC004FLKA Block Diagram

APPLICATIONS

The iMC004FLKA Flash Memory Card allows for the storage of data files and application programs on a purely solid-state removable medium. System resident flash filing systems, such as Microsoft's Flash File System, allow Intel's ETOX II highly reliable Flash Memory Card to effectively function as a physical disk drive. The Intel Flash Memory Card in conjunction with flash filing systems provides an innovative alternative to both fixed hard disks and floppy disks in DOS-compatible portable PCs.

User application software stored on the flash memory card substantially reduces the slow disk-DRAM download process. Replacing the disk results in a dramatic enhancement of read performance and substantial reduction of active power consumption, size, and weight — considerations particularly important in portable PCs and equipment. The iMC004FLKA's high performance read access time and command register microprocessor write interface allows for use of the flash memory system in an "execute-in-place" architecture. This configuration eliminates the need for the redundancy associated with DRAM and Disk memory system architectures. ROM based operating systems, such as Microsoft's MS-DOS ROM Version allow for "instant-on" capability. This enables the design of PCs that boot, operate, store data files, and execute application code from/to purely nonvolatile memory.

Flash write performance is often 50% higher than hard disks for typical user file storage. This equates to ten times more performance when compared to "spun-down" disks, the common practice for portable machines.

Flash filing systems enable the storage and modification of data files by allocating flash memory space intelligently, thus minimizing the number of rewrite cycles. This management function allows the user to rewrite reliably to the flash memory card many more times than a fixed or floppy disk which concentrate rewrite operations into small fixed portions of the medium.

Flash filing systems implement Intel's Flash Memory Card as a redirected disk drive; similar to structures used in local area networks. This enables the end user to interact with the flash memory card in precisely the same way as a magnetic disk. Filing systems that run under popular operating systems, such as MS-DOS, can use the installed base of application software.

The Microsoft Flash File System enables the storage and modification of data files by utilizing a linked list directory structure that is evenly distributed along with the data across the memory card. The linked list approach minimizes file fragmentation losses by using variable-sized data structures rather than the standard sector/cluster method of disk-based systems.

The integration of the PCMCIA/JEIDA 68-pin interface with flash filing systems enables the end-user to transport user files and application code between portable PCs and desktop PCs with memory card Reader/Writers. Intel Flash PC cards provide durable nonvolatile memory storage for Notebook PCs on the road, facilitating simple transfer back into the desktop environment.

For systems currently using a static RAM/battery configuration for data acquisition, the iMC004FLKA's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable computers and medical instruments, both requiring continuous operation. The iMC004FLKA consumes no power when the system is off. In addition, the iMC004FLKA offers a considerable cost and density advantage over memory cards based on static RAM with battery backup.

The flash memory card's electrical zone-erasure, byte writability, and complete nonvolatility fit well with data accumulation and recording needs. Electrical zone-erasure gives the designer the flexibility to selectively rewrite zones of data while saving other zones for infrequently updated look-up tables.

PRINCIPLES OF OPERATION

Intel's Flash Memory Card combines the functionality of two mainstream memory technologies: the rewritability of RAM and the nonvolatility of EPROM. The flash memory card consists of an array of individual memory devices, each of which defines a physical zone. The iMC004FLKA's memory devices erase as individual blocks, equivalent in size to the 256 K-Byte zone. Multiple zones can be erased simultaneously provided sufficient current for the appropriate number of zones (memory devices). Note, multiple zone erasure requires higher current from both the V_{PP} and V_{CC} power supplies. Erased zones can then be written in bit- or byte-at-a-time fashion and read randomly like RAM. Bit level write capability also supports disk emulation.

In the absence of high voltage on the $V_{PP1/2}$ pins, the iMC004FLKA remains in the read-only mode. Manipulation of the external memory card-control pins yields the standard read, standby, and output disable operations.

The same read, standby, and output disable operations are available when high voltage is applied to the $V_{PP1/2}$ pins. In addition, high voltage on $V_{PP1/2}$ enables erasure and rewriting of the accessed zone(s). All functions associated with altering zone contents — erase, erase verify, write, and write verify — are accessed via the command register.

Commands are written to the internal memory register(s), decoded by zone size, using standard microprocessor write timings. Register contents for a given zone serve as input to that zone's internal state-machine which controls the erase and rewrite circuitry. Write cycles also internally latch addresses and data needed for write and erase operations. With the appropriate command written to the register(s), standard microprocessor read timings output zone data, or output data for erase and write verification.

Byte-wide or Word-wide Selection

The flash memory card can be read, erased, and written in a byte-wide or word-wide mode. In the word-wide configuration V_{PP1} and/or $\overline{CE}_1$ control the LO-Byte (with $A_0 = O$) while V_{PP2} and $\overline{CE}_2$ control the HI-Byte (A_0 = don't care).

Read, Write, and Verify operations are byte- or word-oriented, thus zone independent. Erase Setup and Begin Erase Commands are zone dependent such that commands written to any address within a 256 K-Byte zone boundary initiate the erase operation in that zone (or two 256 K-Byte zones under word-wide operation).

Conventional x8 operation uses $\overline{CE}_1$ active-low, with $\overline{CE}_2$ high, to read or write data through the D_0-D_7 only. "Even bytes" are accessed when A_0 is low, corresponding to the low byte of the complete x16 word. When A_0 is high, the "odd byte" is accessed by transposing the high byte of the complete x16 word onto the D_0-D_7 outputs. This odd byte corresponds to data presented on D_8-D_{15} pins in x16 mode.

Note that two zones logically adjacent in x16 mode are multiplexed through D_0-D_7 in x8 mode and are toggled by the A_0 address. Thus, zone specific erase operations must be kept discrete in x8 mode by addressing even bytes only for one-half of the zone pair, then addressing odd bytes only for the other half.

Card Detection

The flash memory card features two card detect pins ($\overline{CD}_{1/2}$) that allow the host system to determind if the card is properly loaded. Note that the two pins are located at opposite ends of the card. Each $\overline{CD}$ output should be read through a port bit. Should only one of the two bits show the card to be present, then the system should instruct the user to re-insert the card squarely into the socket. Card detection can also tell the system whether or not to redirect drives in the case of system booting. $\overline{CD}_{1/2}$ is active low, internally tied to ground.

Write Protection

The flash memory card features three types of write protection. The first type features a mechanical Write Protect Switch that disables the circuitry that control Write Enable to the flash devices. When the switch is activated, $\overline{WE}$ is forced high, which disables any writes to the Command Register. The second type of write protection is based on the PCMCIA/JEIDA socket. Unique pin length assignments provide protective power supply sequencing during hot insertion and removal. The third type operates via software control through the Command Register when the card resides in its connector. The Command Register of each zone is only active when $V_{PP1/2}$ is at high voltage. Depending upon the application, the system designer may choose to make $V_{PP1/2}$ power supply switchable — available only when writes are desired. When $V_{PP1/2} = V_{PPL}$, the contents of the register default to the read command, making the iMC004FLKA a read-only memory card. In this mode, the memory contents cannot be altered.

The system designer may choose to leave $V_{PP1/2} = V_{PPH}$, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage, V_{LKO}. (See the section on Power Up/Down Protection.) The iMC004FLKA is designed to accommodate either design practice, and to encourage optimization of the processor-memory card interface.

BUS OPERATIONS

Read

The iMC004FLKA has two control functions, both of which must be logically active, to obtain data at the outputs. Card Enable ($\overline{CE}$) is the power control and should be used for high and/or low zone(s) selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of accessed zone selection. In the byte-wide configuration, only one $\overline{CE}$ is required. The word-wide configuration requires both $\overline{CE}$s active low.

When $V_{PP1/2}$ is high (V_{PPH}), the read operations can be used to access zone data and to access data for write/erase verification. When $V_{PP1/2}$ is low (V_{PPL}), only read accesses to the zone data are allowed.

Output Disable

With Output Enable at a logic-high level (V_{IH}), output from the card is disabled. Output pins are placed in a high-impedance state.

Standby

With one Card Enable at a logic-high level, the standby operation disables one-half of the x16 output's read/write buffer. Further, only the zone corresponding to the selected address within the upper or lower $\overline{CE}_{1,2}$ bank is active at a time. (NOTE: A_0 must be low to select the low half of the x16 word when $\overline{CE}_2 = 1$ and $\overline{CE}_1 = 0$.) All other zones are deselected, substantially reducing card power consumption. For deselected banks, the outputs are placed in a high-impedance state, independent of the Output Enable signal. If the iMC004FLKA is deselected during erasure, writing, or write/erase verification, the accessed zone draws active current until the operation is terminated.

Int$_e$ligent Identifier™ Command

The manufacturer- and device-codes can be read via the Command Register, for instances where the iMC004FLKA is erased and rewritten in a universal reader/writer. Following a write of 90H to a zone's Command Register, a read from address location 00000H on any zone outputs the manufacturer code (89H). A read from address 0002H outputs the memory device code (BDH).

Write

Zone erasure and rewriting are accomplished via the Command Register, when high voltage is applied to $V_{PP1/2}$. The contents of the register serve as input to that zone's internal state-machine. The state-machine outputs dictate the function of the targeted zone.

The Command Register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The Command Register is written by bringing Write Enable to a logic-low level (V_{IL}), while Card Enable(s) is/are low. Addresses are latched on the falling edge of Write Enable, while data is latched on the rising edge of the Write Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Write Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin(s), the contents of the zone Command Register(s) default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin(s) enable(s) read/write operations. Zone operations are selected by writing specific data patterns into the Command Register. Tables 3 and 4 define these iMC004FLKA register commands for both byte-wide and word-wide configurations.

Table 2. Bus Operations

Pins / Operation		Notes	[1, 7] V_{PP2}	[1, 7] V_{PP1}	A0	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{OE}$	$\overline{WE}$	D_8-D_{15}	D_0-D_7
READ-ONLY	Read (x8)	8	V_{PPL}	V_{PPL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Even
	Read (x8)	9	V_{PPL}	V_{PPL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Odd
	Read (x8)	10	V_{PPL}	V_{PPL}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out	High Z
	Read (x16)	11	V_{PPL}	V_{PPL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data Out	Data Out
	Output Disable		V_{PPL}	V_{PPL}	X	X	X	V_{IH}	V_{IH}	High Z	High Z
	Standby		V_{PPL}	V_{PPL}	X	V_{IH}	V_{IH}	X	X	High Z	High Z
READ/WRITE	Read (x8)	3, 8	V_{PPX}	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Even
	Read (x8)	3, 9	V_{PPH}	V_{PPX}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Data Out-Odd
	Read (x8)	10	V_{PPH}	V_{PPX}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out	High Z
	Read (x16)	3, 11	V_{PPH}	V_{PPH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Data Out	Data Out
	Write (x8)	5, 8	V_{PPX}	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High Z	Data In-Even
	Write (x8)	9	V_{PPH}	V_{PPX}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High Z	Data In-Odd
	Write (x8)	10	V_{PPH}	V_{PPX}	X	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data In	High Z
	Write (x16)	11	V_{PPH}	V_{PPH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Data In	Data In
	Standby	4	V_{PPH}	V_{PPH}	X	V_{IH}	V_{IH}	X	X	High Z	High Z
	Output Disable		V_{PPH}	V_{PPH}	X	X	X	V_{IH}	V_{IL}	High Z	High Z

Notes:

1. Refer to DC Characteristics. When $V_{PP1/2} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. Read operations with $V_{PP1/2}$ = Vpph may access array data or the Inteligent Identifier codes.
4. With $V_{PP1/2}$ at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
5. Refer to Table 3 for valid Data-In during a write operation.
6. X can be V_{IL} or V_{IH}.
7. $V_{PPX} = V_{PPH}$ or V_{PPL}.
8. This x8 operation reads or writes the low byte of the x16 word on DQ_{0-7}, i.e., A_0 low reads "even" byte in x8 mode.
9. This x8 operation reads or writes the high byte of the x16 word on DQ_{0-7} (transposed from DQ_{8-15}), i.e., A_0 high reads "odd" byte in x8 mode.
10. This x8 operation reads or writes the high byte of the x16 on DQ_{8-15}. A_0 is "don't care."
11. A_0 is "don't care," unused in x16 mode. High and low bytes are presented simultaneously.

Table 3. Command Definitions byte-wide mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation[1]	Address[2]	Data[3]	Operation[1]	Address[2]	Data[3]
Read Memory		1	Write	X	00H			
Read Inteligent ID Codes	4	3	Write	IA	90H	Read		
Set-up Erase/Erase	5	2	Write	ZA	20H	Write	ZA	20H
Erase Verify	5	2	Write	EA	A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	40H	Write	WA	WD
Write Verify	6	2	Write	WA	C0H	Read	WA	WVD
Reset	7	2	Write	X	FFH	Write	X	FFH

Table 4. Command Definitions word-wide mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation[1]	Address[2]	Data[3]	Operation[1]	Address[2]	Data[3]
Read Memory		1	Write	X	0000H			
Read Inteligent ID Codes	4	3	Write	IA	9090H	Read		
Set-up Erase/Erase	5	2	Write	ZA	2020H	Write	ZA	2020H
Erase Verify	5	2	Write	EA	A0A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	4040H	Write	WA	WD
Write Verify	6	2	Write	WA	C0C0H	Read	WA	WVD
Reset	7	2	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   WA = Address of memory location to be written.
   ZA = Address of 256 K-Byte zones involved in erase operation.
   Addresses are latched on the falling edge of the Write Enable pulse.
3. ID = Data read from location IA during device identification. (Mfr = 89H, Device = BDH).
   EVD = Data read from location EA during erase verify.
   WD = Data to be written at location WA. Data is latched on the rising edge of Write Enable.
   WVD = Data read from location WA during write verify. WA is latched on the Write command.
4. Following the Read Inteligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Erase Algorithm.
6. Figure 6 illustrates the Write Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While $V_{PP1/2}$ is high, for erasure and writing, zone memory contents can be accessed via the read command. The read operation is initiated by writing 00H (0000H for the word-wide configuration) into the zone Command Register(s). Microprocessor read cycles retrieve zone data. The accessed zone remains enabled for reads until the Command Register(s) contents are altered.

The default contents of each zone's register(s) upon $V_{PP1/2}$ power-up is 00H (00000H for word-wide). This default value ensures that no spurious alteration of memory card contents occurs during the $V_{PP1/2}$ power transition. Where the $V_{PP1/2}$ supply is left at V_{PPH}, the memory card powers-up and remains enabled for reads until the command Register contents of targeted zones are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier Command

Each zone of the iMC004FLKA contains an int$_e$ligent Identifier to identify memory card device characteristics. The operation is initiated by writing 90H (9090H for word-wide) into the Command Register(s). Following the command write, a read cycle from address 00000H retrieves the manufacturer code 89H (8989H for word-wide). A read cycle from address 0002H returns the device code BDH (BDBDH for word-wide). To terminate the operation, it is necessary to write another valid command into the register(s).

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the targeted zone(s) for electrical erasure of all bytes in the zone. The set-up erase operation is performed by writing 20H to the Command Register (2020H for word-wide).

To commence zone-erasure, the erase command (20H or 2020H) must again be written to the register(s). The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that zone memory contents are not accidentally erased. Also, zone-erasure can only occur when high voltage is applied to the $V_{PP1/2}$ pins. In the absence of this high voltage, zone memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the zone in parallel. After each erase operation, all bytes in the zone must be individually verified. In byte-mode operations, zones are segregated by A_0 in odd and even banks; erase and erase verify operations must be done in complete passes of even-bytes-only then odd-bytes-only. See the Erase Algorithm for byte-wide mode. The erase verify operation is initiated by writing A0H (A0A0H for word-wide) into the Command Register(s). The address for the byte(s) to be verified must be supplied as it is latched on the falling edge of the Write Enable pulse. The register write terminates the erase operation with the rising edge of its Write Enable pulse.

The enabled zone applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. Similarly, reading FFFFH from the addressed word indicates that all bits in the word are erased.

The erase-verify command must be written to the Command Register prior to each byte (word) verification to latch its address. The process continues for each byte (word) in the zone(s) until a byte (word) does not return FFH (FFFFH) data, or the last address is accessed.

In the case where the data read is not FFH (FFFFH), another erase operation is performed. (Refer to Set-up Erase/Erase.) Verification then resumes from the address of the last-verified byte (word). Once all bytes (words) in the zone(s) have been verified, the erase step is complete. The accessed zone can now be written. At this point, the verify operation is terminated by writing a valid command (e.g., Write Set-up) to the Command Register. The Erase algorithms for byte-wide and word-wide configurations illustrate how commands and bus operations are combined to perform electrical erasure of the iMC001FLKA. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Write/Write Commands

Set-up write is a command-only operation that stages the targeted zone for byte writing. Writing 40H (4040H) into the Command Register(s) performs the set-up operation.

Once the write set-up operation is performed, the next Write Enable pulse causes a transition to an active write operation. Addresses are internally latched on the falling edge of the Write Enable pulse. Data is internally latched on the rising edge of the Write Enable pulse. The rising edge of Write Enable also begins the write operation. The write operation terminates with the next rising edge of Write Enable, which is used to write the verify command. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Write Verify Command

The iMC004FLKA is written on a byte-by-byte or word-by-word basis. Byte or word writing may occur sequentially or at random. Following each write operation, the byte or word just written must be verified.

The write-verify operation is initiated by writing C0H (C0C0) into the Command Register(s). The register write(s) terminate(s) the write operation with the rising edge of its Write Enable pulse. The write-verify operation stages the accessed zone(s) for verification of the byte or word last written. No new address information is latched. The zone(s) apply(ies) an internally-generated margin voltage to the byte or word. A microprocessor read cycle outputs the data. A successful comparison between the written byte or word and true data means that the byte or word is successfully written. The write operation then proceeds to the next desired byte or word location. The Write algorithms for byte-wide and word-wide configurations illustrate how commands are combined with bus operations to perform byte and word writes. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or write-command sequences. Following either set-up command (erase or write) with two consecutive writes of FFH (FFFFH for word-wide) will safely abort the operation. Zone memory contents will not be altered. A valid command must then be written to place the accessed zone in the desired state.

EXTENDED ERASE/WRITE CYCLING

Intel has designed extended cycling capability into its ETOX II flash memory technology enabling a flash memory card with a MTBF that is approximately 20 times more reliable than rotating disk technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field minimizes the probability of oxide defects in the region. The lower electric field greatly reduces oxide stress and the probability of failure.

WRITE ALGORITHMS

The write algorithm(s) use write operations of 10μs duration. Each operation is followed by a byte or word verification to determine when the addressed byte or word has been successfully written. The algorithm(s) allows for up to 25 write operations per byte or word, although most bytes and words verify on the first or second operation. The entire sequence of writing and byte/word verification is performed with V_{PP} at high voltage.

ERASE ALGORITHM

The Erase algorithm(s) yield(s) fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the write algorithm, to simultaneously remove charge from all bits in the accessed zone(s).

Erasure begins with a read of memory zone contents. Reading FFH (FFFFH) data from the accessed zone(s) can be immediately followed by writing to the desired zone(s).

For zones being erased and rewritten, uniform and reliable erasure is ensured by first writing all bits in the accessed zone to their charged state (data = 00H byte-wide, 00000H word-wide). This is accomplished, using the write algorithm, in approximately four seconds per zone.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH byte-wide, FFFFH word-wide) begins at address 00000H and continues through the zone to the last address, or until data other than FFH (FFFFH) is encountered. (Note: byte-wide erase operation requires separate even- and odd-address passes to handle the individual 256 K-Byte zones.) With each erase operation, an increasing number of bytes or words verify to the erased state. Erase efficiency may be improved by storing the address of the last byte or word verified in a register(s). Following the next erase operation, verification starts at that stored address location. Follow this procedure until all bytes in the zone are erased. Then, re-start the procedure for the next zone or word-wide zone pair. Erasure typically occurs in two seconds per zone.

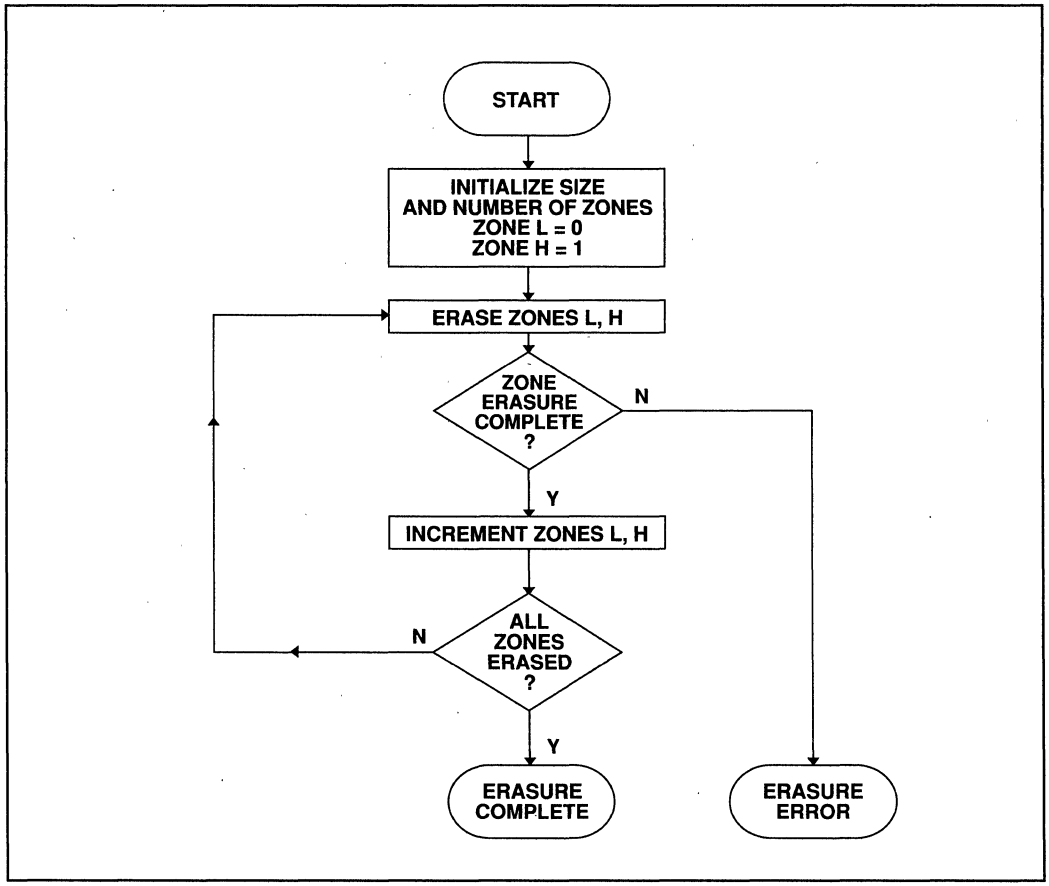
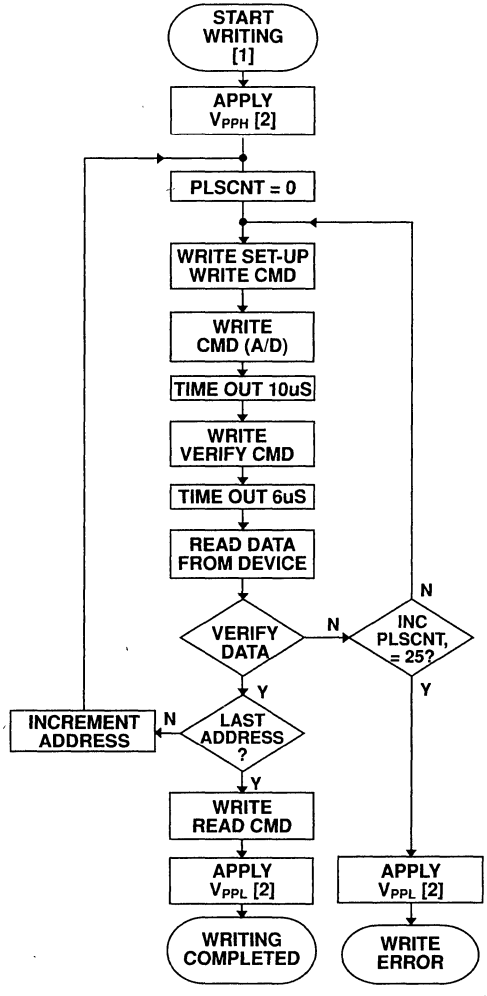


Figure 3. Full Card Erase Flow



BUS OPERATION	COMMAND	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [2]
		Initialize pulse-count
Write	Set-up Write	Data = 40H
Write	Write	Valid address/data
Standby		Duration Of Write operation (t_{WHWH1})
Write	Write Verify [3]	Data = C0H; Stops [4] Write Operation
Standby		t_{WHGL}
Read		Read byte to verify Write Operation
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [2]

Notes:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
3. Write Verify is only performed after a byte write operation. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 4. Write Algorithm for byte-wide mode

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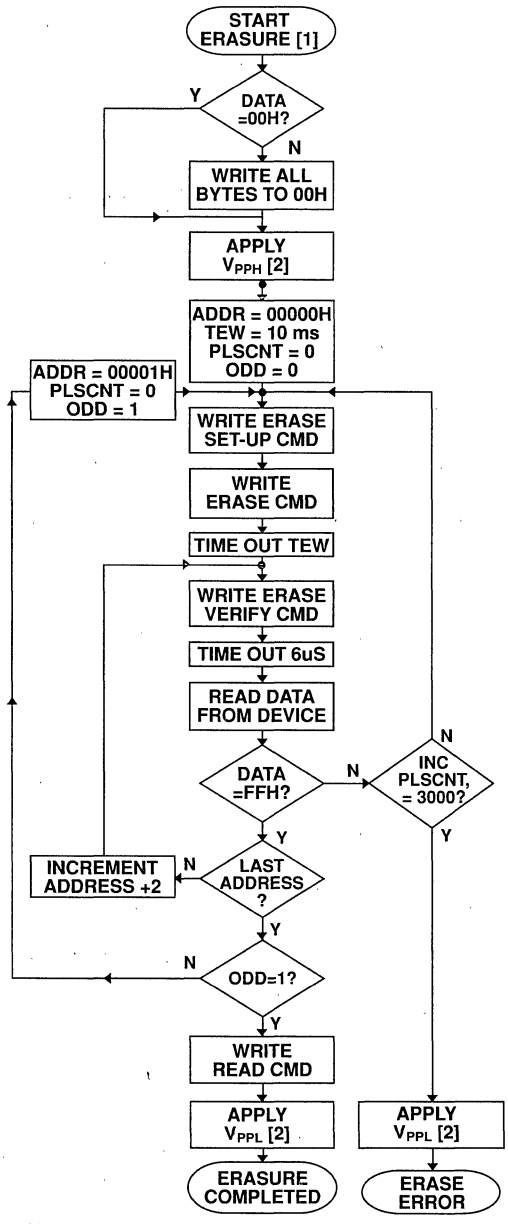


BUS OPERATION	COMMANDS	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [2]
		Use Write Operation Algorithm
		Initialize even/odd Addresses, Erase Pulse Width, and Pulse Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify [3]	Addr = Byte to verify; Data = A0H; Stops Erase Operation [4]
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [2]

Notes:
1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
3. Erase Verify is only performed after chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 5. Erase Algorithm for byte-wide mode

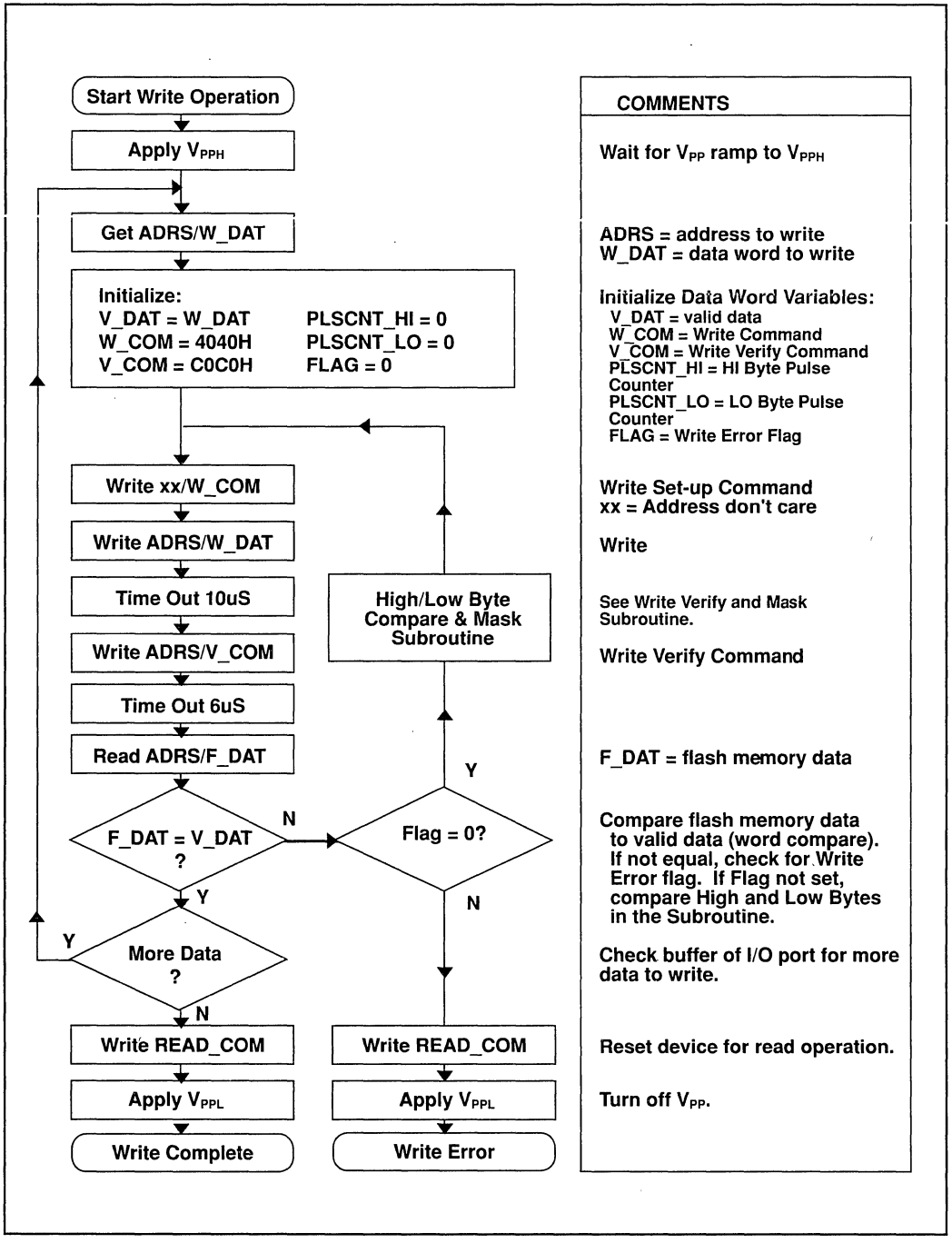
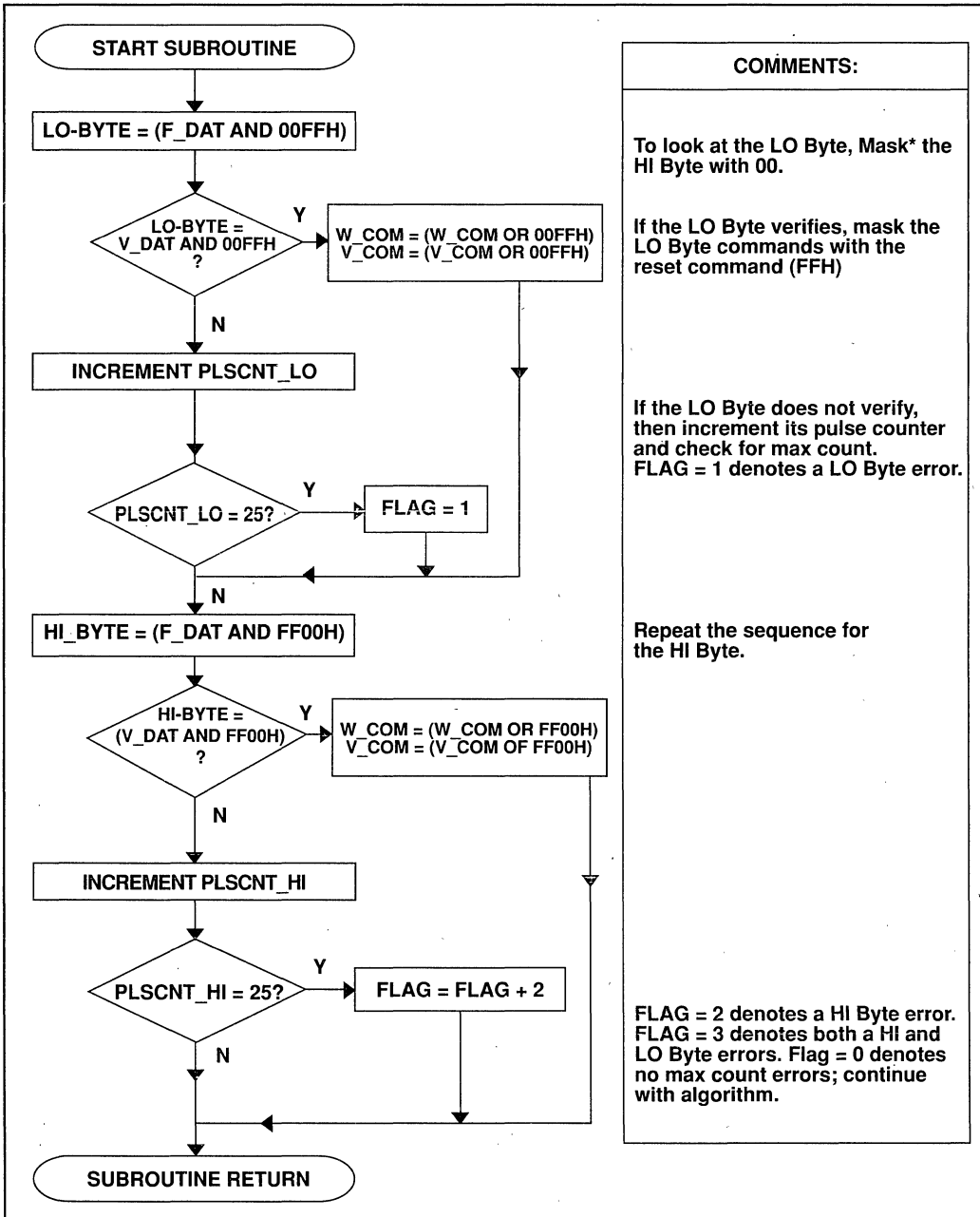
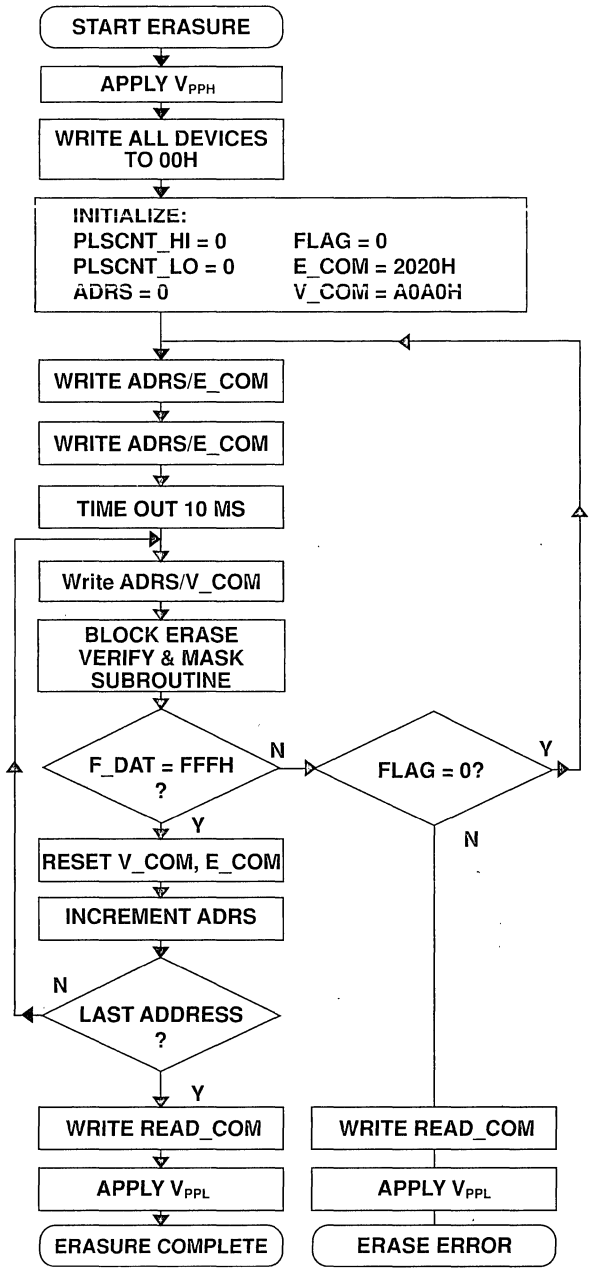


Figure 6. Write Algorithm for word-wide mode



*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Figure 7. Write Verify and Mask Subroutine for word-wide mode



COMMENTS:

Wait for V_{PP} to stabilize.

Use Write operation algorithm in x8 or x16 configuration

Initialize Variables:
PLSCNT_HI = HI Byte Pulse Counter
PLSCNT_LO = LO Byte Pulse Counter
FLAG = Erasure error flag
ADRS = Address
E_COM = Erase Command
V_COM = Verify Command

Erase Set-up Command

Start Erasing

Duration of Erase Operation.

Erase Verify Command stops erasure.

See Block Erase Verify & Mask Subroutine

When both devices at ADRS are erased, F_DATA = FFFFH. If not equal, increment the pulse counter and check for last pulse.

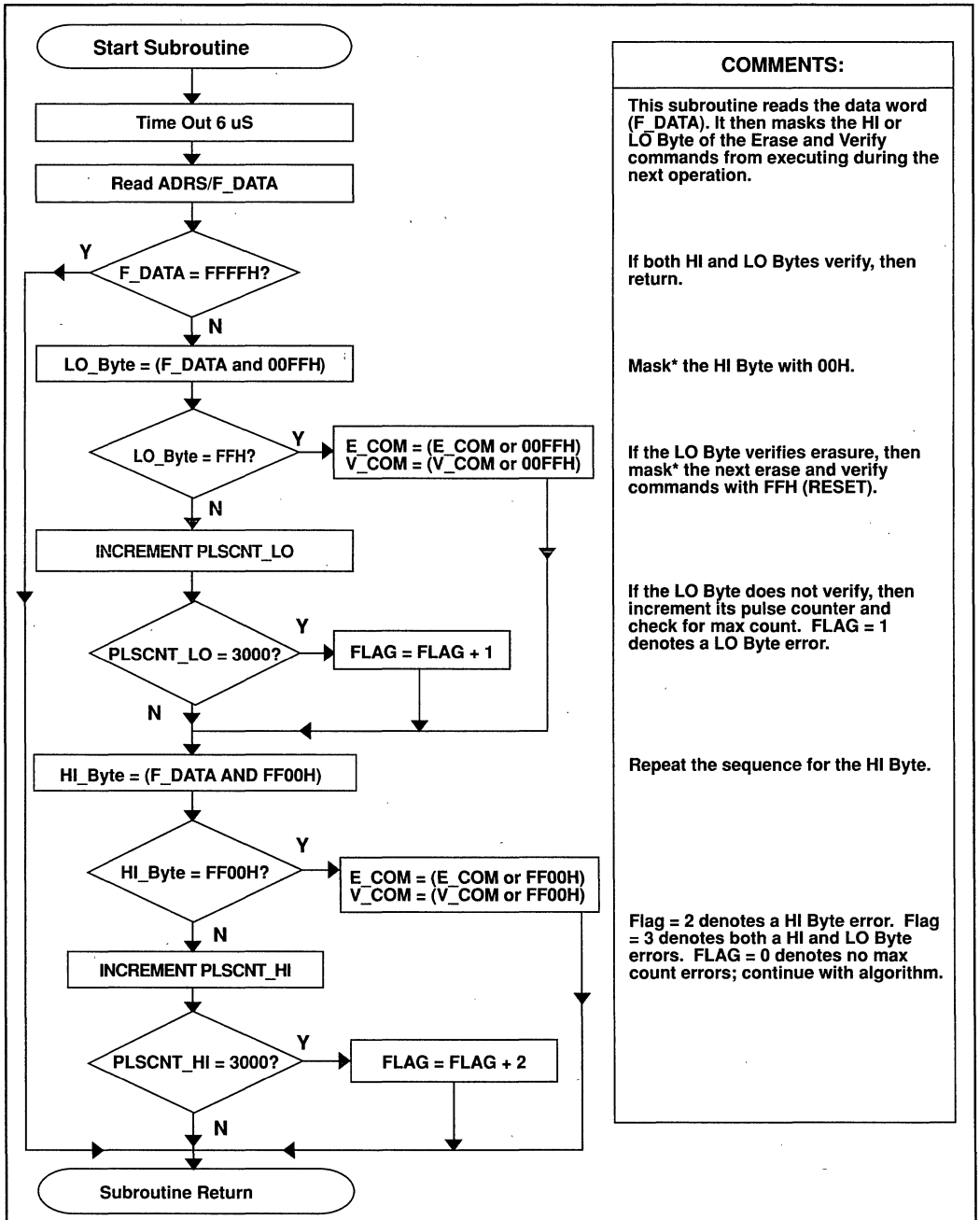
Reset commands default to (E_COM = 2020H) (V_COM = A0A0H) before verifying next ADRS.

Reset device for read operation.

Turn off V_{PP}.

NOTES:
X16 Addressing uses A_1-A_{21} only. A_0=0 throughout word-wide operation.

Figure 8. Erase Algorithm for word-wide mode



*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Figure 9. Erase Verify and Mask Subroutine for word-wide mode.

SYSTEM DESIGN CONSIDERATIONS

Three-Line Control

Three-line control provides for:

a. the lowest possible power dissipation and,

b. complete assurance that output bus contention will not occur.

To efficiently use these three control inputs, an address-decoder output should drive $\overline{CE}_{1,2}$, while the system's Read signal controls the card $\overline{OE}$ signal, and other parallel zones. This, coupled with the internal zone decoder, assures that only enabled memory zones have active outputs, while deselected zones maintain the low power standby condition.

Power-Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues — standby, active and transient current peaks, produced by falling and rising edges of $\overline{CE}_{1/2}$. The capacitive and inductive loads on the card and internal flash memory zones determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The iMC004FLKA features on-card ceramic decoupling capacitors connected between V_{CC} and V_{SS}, and between V_{PP1}/V_{PP2} and V_{SS}.

The card connector should also have a 4.7µF electrolytic capacitor between V_{CC} and V_{SS}, as well as between V_{PP1}/V_{PP2} and V_{SS}. The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

Power Up/Down Protection

The PCMCIA/JEIDA socket is specified, via unique Pin lengths, to properly sequence the power supplies to the flash memory card. This assures that hot insertion and removal will not result in card damage or data loss.

Each zone in the iMC004FLKA is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}_{1,2}$ must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of zone contents only occurs after successful completion of the two-step command sequences.

While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady state value before raising $V_{PP1/2}$ above $V_{CC}+2.0V$. In addition, upon powering-down, $V_{PP1/2}$ should be below $V_{CC}+2.0V$, before lowering V_{CC}.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to + 60°C(1)
During Erase/Write ..... 0°C to + 60°C
Temperature Under Bias ..... −10°C to + 70°C
Storage Temperature ..... −30°C to + 70°C
Voltage on Any Pin with
Respect to Ground ..... −2.0V to + 7.0V(2)
V_{PP1}/V_{PP2} Supply Voltage with
Respect to Ground
During Erase/Write ..... −2.0V to + 14.0V(2,3)
V_{CC} Supply Voltage with
Respect to Ground ..... −2.0V to + 7.0V(2)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the card. This is a stress rating only and functional operation of the card at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect card reliability.

NOTICE: Specifications contained within the following tables are subject to change.

Notes:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V for periods less than 20 ns.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	60	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.75	5.25	V	
V_{PPH}	Active V_{PP1}, V_{PP2} Supply Voltages	11.40	12.60	V	
V_{PPL}	V_{PP} During Read Only Operations	0.00	6.50	V	

DC CHARACTERISTICS — Byte Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Condition
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		0.8	1.6	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1,2		40	70	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IL}$ f = 6MHz, I_{OUT} = 0mA
I_{CC2}	V_{CC} Write Current	1,2		1.0	12.0	mA	Writing in progress
I_{CC3}	V_{CC} Erase Current	1,2		6.0	17	mA	Erasure in progress
I_{CC4}	V_{CC} Write Verify Current	1,2		6.0	17	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{CC5}	V_{CC} Erase Verify Current	1,2		6.0	17	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
I_{PPS}	V_{PP} Leakage Current	1			±80	uA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	1,3		0.7	1.6	mA	$V_{PP} > V_{CC}$
					±.08		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Write Current	1,3		8.0	30	mA	$V_{PP} = V_{PPH}$ Write in progress
I_{PP3}	V_{PP} Erase Current	1,3		10	30	mA	$V_{PP} = V_{PPH}$ Erasure in progress
I_{PP4}	V_{PP} Write Verify Current	1,3		3.0	6.0	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{PP5}	V_{PP} Erase Verify Current	1,3		3.0	6.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Low Voltage				0.40	V	I_{OL} = 3.2mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		3.8			V	I_{OH} = −2.0mA $V_{CC} = V_{CC}$ min
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write lock voltage		2.5			V	

Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25° C.
2. 1 chip active and 15 in standby for byte-wide mode.
3. Assumes 1 V_{PP} is active.

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DC CHARACTERISTICS — Word Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Condition
			Min	Typical	Max		
I_{LI}	Input Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1		±1.0	±20	uA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		0.8	1.6	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1,2		50	100	mA	$V_{CC} = V_{CC}$ max $\overline{CE} = V_{IL}$ f = 6MHz, I_{OUT} = 0mA
I_{CC2}	V_{CC} Write Current	1,2		2.0	20	mA	Writing in progress
I_{CC3}	V_{CC} Erase Current	1,2		10	30	mA	Erasure in progress
I_{CC4}	V_{CC} Write Verify Current	1,2		10	30	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{CC5}	V_{CC} Erase Verify Current	1,2		10	30	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
I_{PPS}	V_{PP} Leakage Current	1			±160	uA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	1,3		1.5	3.0	mA	$V_{PP} > V_{CC}$
					±.16		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Write Current	1,3		17	63	mA	$V_{PP} = V_{PPH}$ Write in progress
I_{PP3}	V_{PP} Erase Current	1,3		20	60	mA	$V_{PP} = V_{PPH}$ Erasure in progress
I_{PP4}	V_{PP} Write Verify Current	1,3		5.0	12	mA	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{PP5}	V_{PP} Erase Verify Current	1,3		5.0	12	mA	$V_{PP} = V_{PPH}$ Erase Verify in progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Low Voltage				0.40	V	I_{OL} = 3.2mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		3.8			V	I_{OH} = −2.0mA $V_{CC} = V_{CC}$ min
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write lock voltage		2.5			V	

Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25° C.
2. 2 chips active and 14 in standby for word-wide mode.
3. Assumes 2 V_{PP}s are active.

CAPACITANCE T = 25° C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN1}	Address Capacitance			8	pF	V_{IN} = 0V
C_{IN2}	Control Capacitance			16	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			21	pF	V_{OUT} = 0V
$C_{I/O}$	I/O Capacitance			10	pF	$V_{I/O}$ = 0V

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... Vol and Voh1
Input Timing Reference Level ..... Vil and Vih
Output Timing Reference Level ..... Vil and Vih

AC CHARACTERISTICS — Read-Only Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{RC}	Read Cycle Time	2	250		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time	2		250	ns
t_{AVQV}/t_{ACC}	Address Access Time	2		250	ns
t_{GLQV}/t_{OE}	Output Enable Access Time	2		120	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	2	5		ns
t_{EHQZ}	Chip Disable to Output in High Z	2		60	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	2	5		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	2		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change	1,2	5		ns
t_{WHGL}	Write Recovery Time Before Read	2	6		us

Notes:
1. Whichever occurs first.
2. Rise/Fall time ≤ 10ns.

6

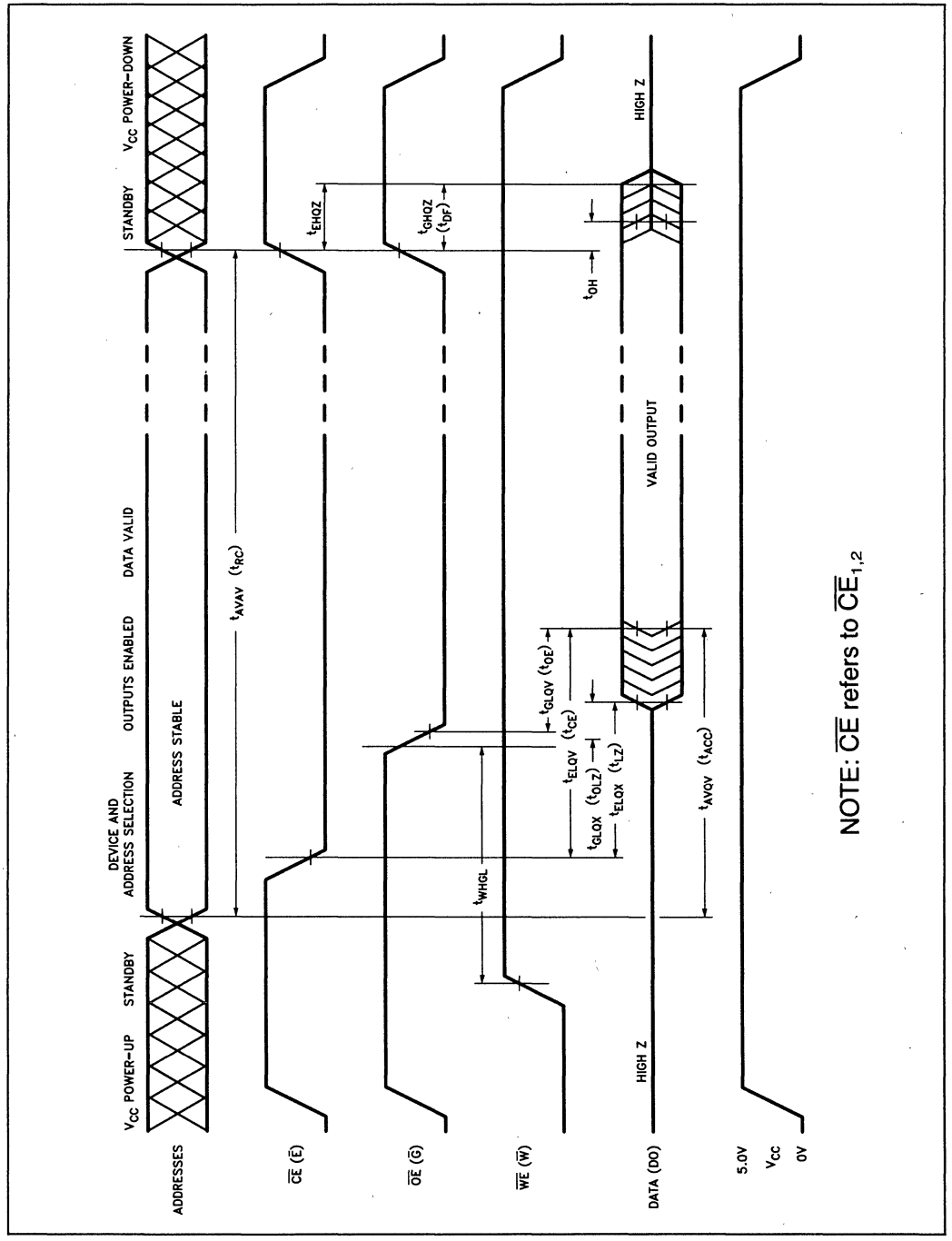


Figure 10. AC Waveforms for Read Operations

AC CHARACTERISTICS — For Write/Erase Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{WC}	Write Cycle Time	1,2	250		ns
t_{AVWL}/t_{AS}	Address Set-up Time	1,2	0		ns
t_{WLAX}/t_{AH}	Address Hold Time	1,2	100		ns
t_{DVWH}/t_{DS}	Data Set-up Time	1,2	80		ns
t_{WHDX}/t_{DH}	Data Hold Time	1,2	30		ns
t_{WHGL}	Write Recovery Time Before Read	1,2	6		us
t_{GHWL}	Read Recovery Time Before Write	1,2	0		us
t_{WLOZ}	Output High-Z from Write Enable	1,2	5		ns
t_{WHOX}	Output Low-Z from Write Enable	1,2		60	ns
t_{ELWL}/t_{CS}	Chip Enable Set-up Time Before Write	1,2	40		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	1,2	0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	1,2	100		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	1,2	20		ns
t_{WHWH1}	Duration of Write Operation	1,2,3	10		us
t_{WHWH2}	Duration of Erase Operation	1,2,3	9.5		ms
t_{VPEL}	V_{PP} Set-up Time to Chip Enable Low	1,2	100		ns

Notes:

1. Read timing parameters during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Rise/Fall time ≤ 10ns.
3. The integrated stop timer terminates the write/erase operations, thereby eliminating the need for a maximum specification.

6

ERASE/WRITE PERFORMANCE

Parameter	Notes	Min	Typ	Max	Unit
Zone Erase Time	1,3,4		2.0	30	sec
Zone Write Time	1,2,4		4.0	25	sec
MTBF	5		10^6		Hrs

Notes:

1. 25° C, 12.0V V_{PP}.
2. Minimum byte writing time excluding system overhead is 16 usec (10 usec program + 6 usec write recovery), while maximum is 400 usec/byte (16 usec x 25 loops allowed by algorithm). Max chip write time is specified lower than the worst case allowed by the write algorithm since most bytes write significantly faster than the worst case byte.
3. Excludes 00H writing Prior to Erasure.
4. One zone equals 256K Bytes.
5. MTBF = Mean Time Between Failure, 50% failure point for disk drives.

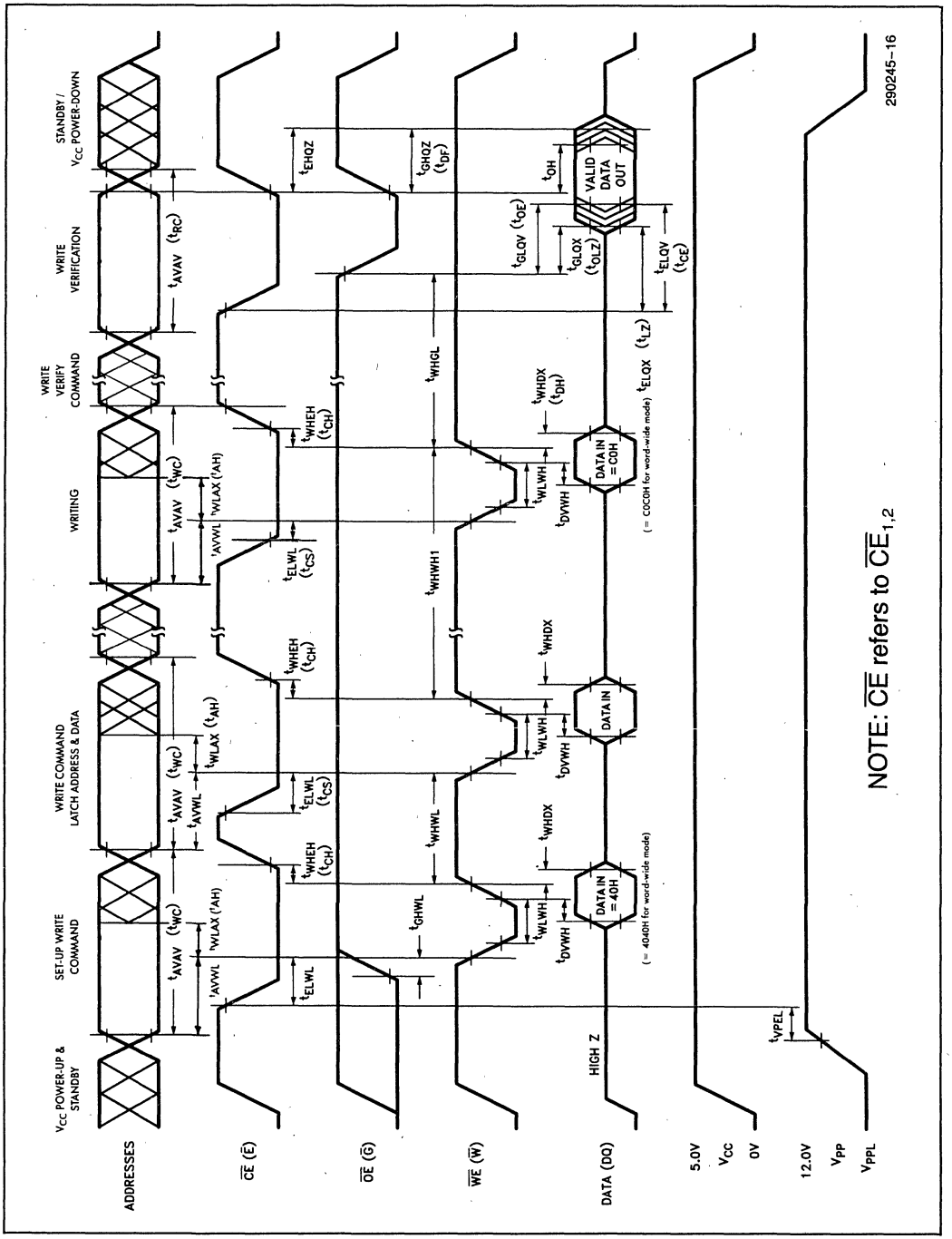


Figure 11. AC Waveforms for Write Operations

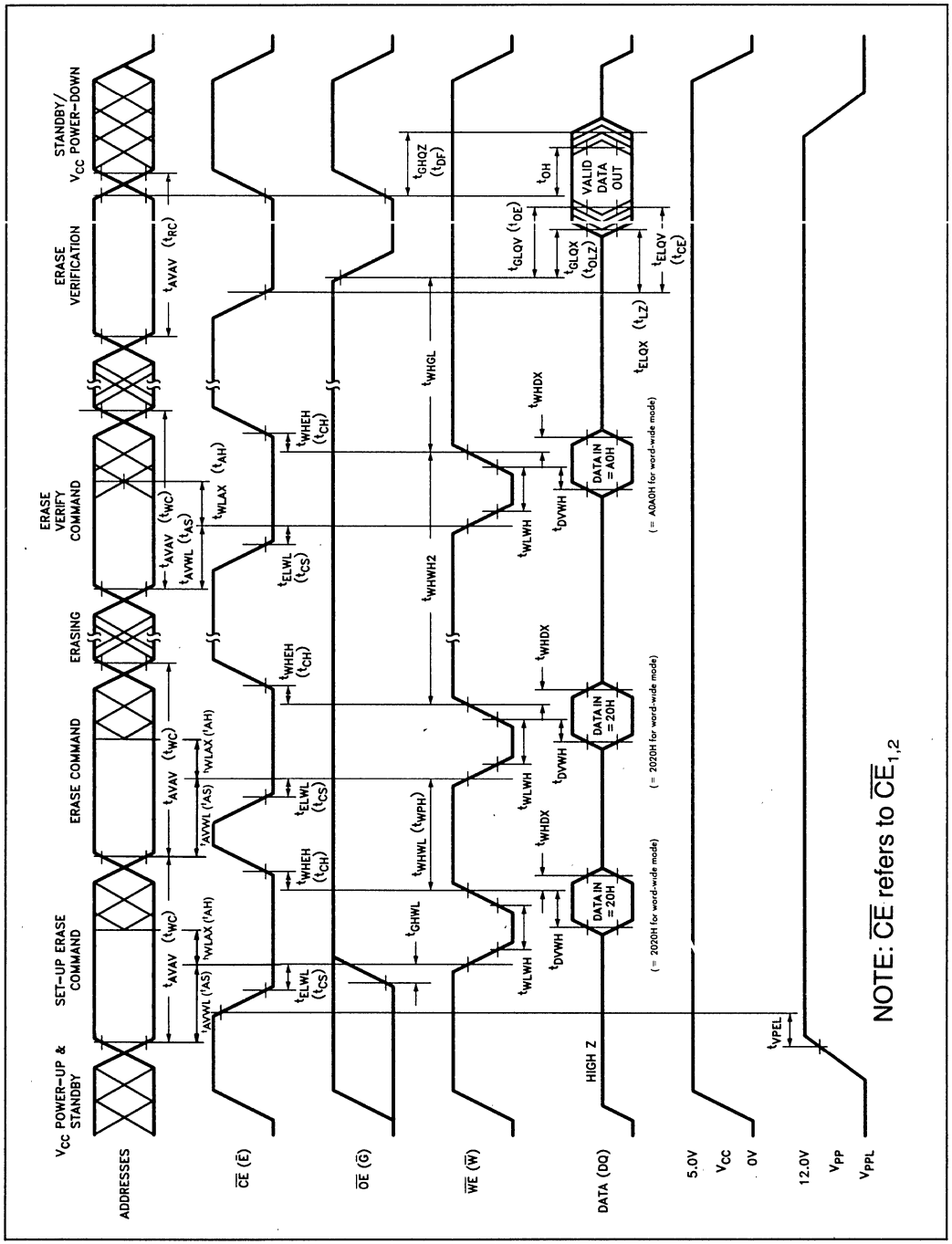


Figure 12. AC Waveforms for Erase Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		250		ns
t_{AVEL}	Address Set-up Time		0		ns
t_{ELAX}	Address Hold Time		100		ns
t_{DVEH}	Data Set-up Time		80		ns
t_{EHDX}	Data Hold Time		30		ns
t_{EHGL}	Write Recovery Time Before Read		6		us
t_{GHEL}	Read Recovery Time Before Write		0		us
t_{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		ns
t_{EHWH}	Write Enable Hold Time		0		ns
t_{ELEH}	Write Pulse Width	1	100		ns
t_{EHEL}	Write Pulse Width High		20		ns
t_{PEL}	V_{PP} Set-Up Time to Chip-Enable Low		100		ns

Notes:

1. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width (with a longer Write Enable timing waveform) all set-up, hold and inactive Write Enable times should be measured relative to the Chip Enable waveform.

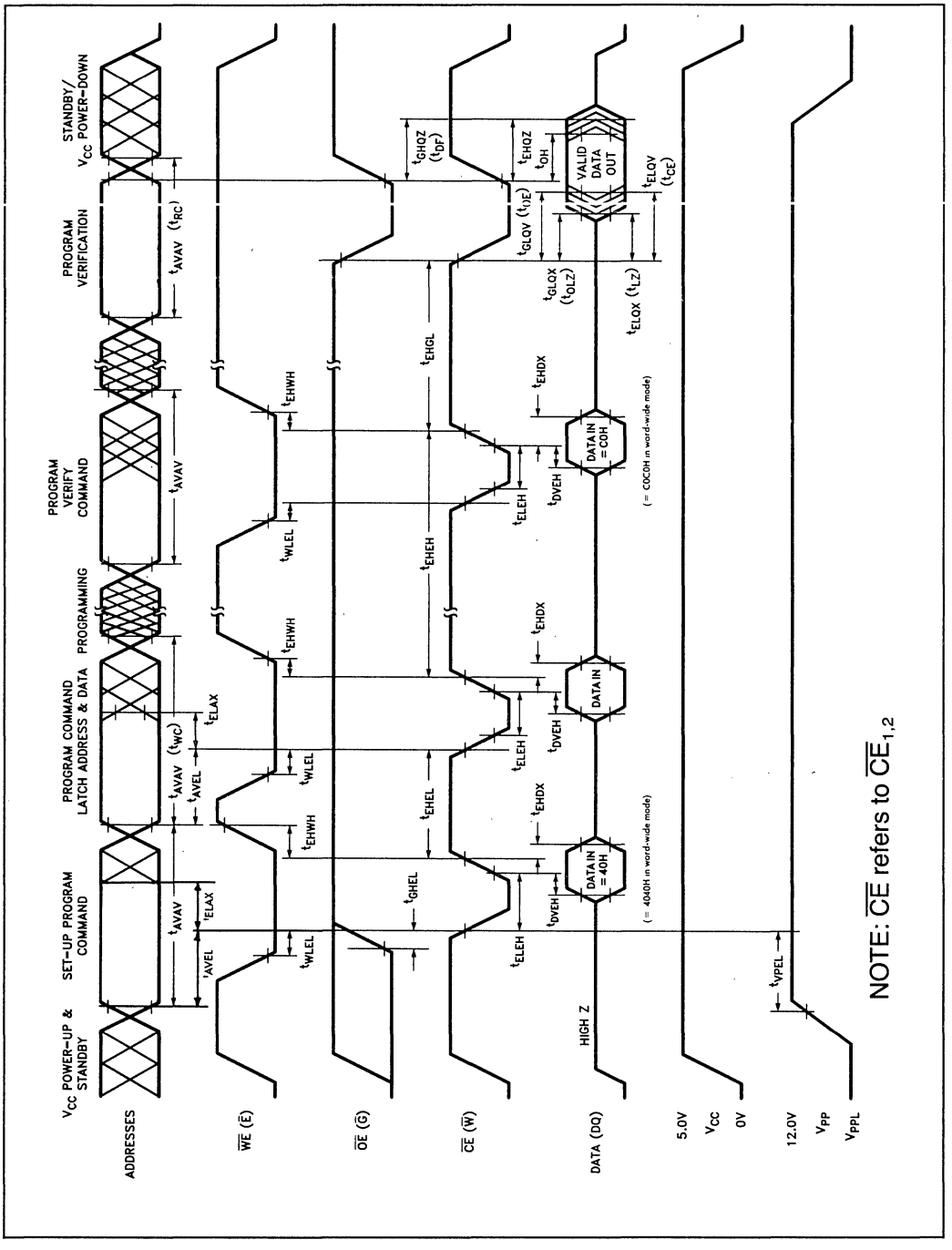
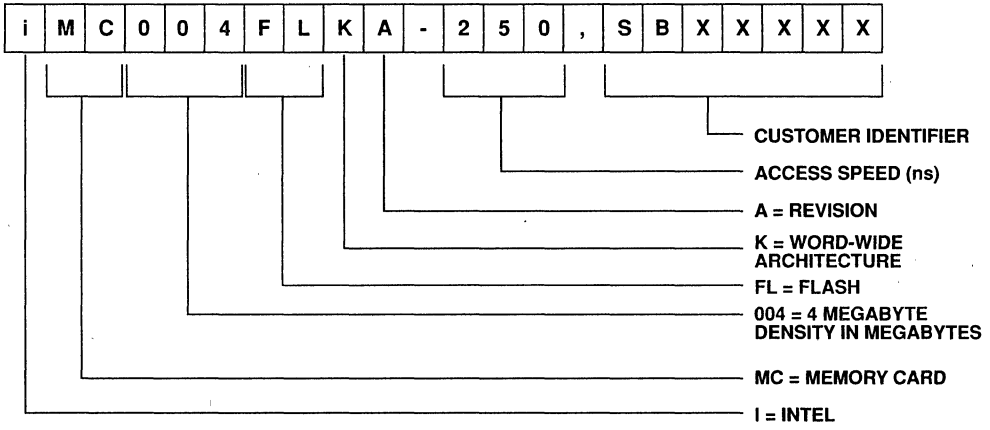


Figure 13. Alternate AC Waveforms for Write Operations

6

ORDERING INFORMATION



ADDITIONAL INFORMATION	Order Number
ER-20, "ETOX II Flash Memory Technology"	294005
RR-60, "ETOX II Flash Memory Reliability Data Summary"	293002
AP-343, "Solutions for High Density Applications using Flash Memory"	292079

October 1990

Using Flash Memory for In-System Reprogrammable Nonvolatile Storage

SAUL ZALES
DALE ELBERT
APPLICATIONS ENGINEERING
INTEL CORPORATION

Order Number: 292046-003

USING FLASH MEMORY FOR IN-SYSTEM REPROGRAMMABLE NONVOLATILE STORAGE

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1.0 INTRODUCTION

Intel's ETOX™ II (EPROM tunnel oxide) flash memory technology uses a single-transistor cell to provide in-system reprogrammable nonvolatile storage. Reprogramming entails electrically erasing all bits in parallel and then randomly programming any byte in the array. This new technology offers designers alternatives for two of industry's needs: 1) a cost-effective means of updating program code; and 2) a solid-state approach for non-volatile data accumulation or storage.

This application note:

- introduces you to the concepts of in-system writing;
- discusses the hardware and software considerations for reprogramming flash memories in-system;
- offers a checklist for integrating Intel's flash memories into microprocessor- or microcontroller-based systems; and
- shows an example of an 80C186 design which incorporates flash memory.

1.1 PROM Programmer vs System-Processor Controlled Programming

While soldered to a printed circuit board, one of two sources controls flash memory reprogramming: 1) a PROM programmer connected to the board, or 2) the system's own central processing unit (CPU). These are called on-board programming (OBP), and in-system writing (ISW), respectively. With OBP, the PROM programmer supplies the programming voltage (V_{PP}) and the programming intelligence; with ISW, V_{PP} is generated locally and the system itself drives the reprogramming process. Both methods offer a variety of benefits. However this application note focuses on ISW.

NOTE:
See Appendix A for OPB design considerations.

1.2 Information Download and Upload

ETOX II flash memory technology programs extremely quick, permitting "on-the-fly" programming with unbuffered 19.2K baud data input. The remote ISW system handles the serial communication link for the host interface, as well as the flash memory reprogramming.

Version Updates (Download)

Flash memories enable code version updates using simple hardware designs. Beyond the basic system, a local V_{PP} supply is all that is needed for remote code download.

A central host computer can download program code to many remote systems. Flash memory offers this capability without the drawbacks of other technologies. It is solid-state and nonvolatile, thus eliminating mechanical component wear-out (common with disk drives) and the risk of losing updates (a concern with battery-backed RAM). These aspects of flash memory offer major advantages in automated factories, remote systems, portable equipment and other applications. Finally, flash memories provide this capability at a much lower cost than byte-alterable EEPROM and battery-backed SRAM.

Data Acquisition (Upload)

Intel's flash memories allow single-byte programming for data accumulation applications. A remote data-logger uploads its information to a central host via serial link. The flash memory device is then in-system erased

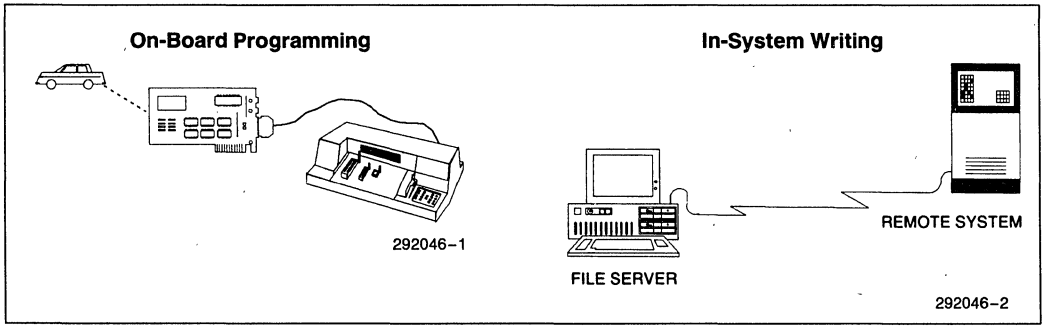


Figure 1. These diagrams illustrate OBP and ISW. In OBP, a PROM programmer updates a system's flash memory. The ISW diagram shows a host updating remote flash memory via serial link. The remote system performs the flash reprogramming with its own CPU.

Intel's ETOX flash memory process has patents pending.

for resumption of data acquisition. This is useful in an advanced electrical power meter, for example. It could be configured to track and monitor power usage and report the data to a central computer for billing and utility management. This reduces the cost of manual door-to-door meter reading.

2.0 DEVICE FEATURES AND ISW APPLICATION CONSIDERATIONS

This section gives a brief overview of Intel's flash memory features and explains how they facilitate ISW design.

2.1 Flash Memory Pinouts

The 32-pin DIP memory site is forward-compatible from the 256K bit to the 2 Mbit flash memory density. It fits into the 27C010 Mbit EPROM pinout and requires no multiplexed pins. Also, with just a single circuit-board jumper trace, a 28-pin EPROM can be placed in the lower pins of the 32-pin flash memory site. (See Figures 2A and 2B, Flash Memory Pinouts.) For more information on intertechnology pin compatibility see Ap Brief AB-25.

Byte-Wide Flash Memory in 32-Pin DIP

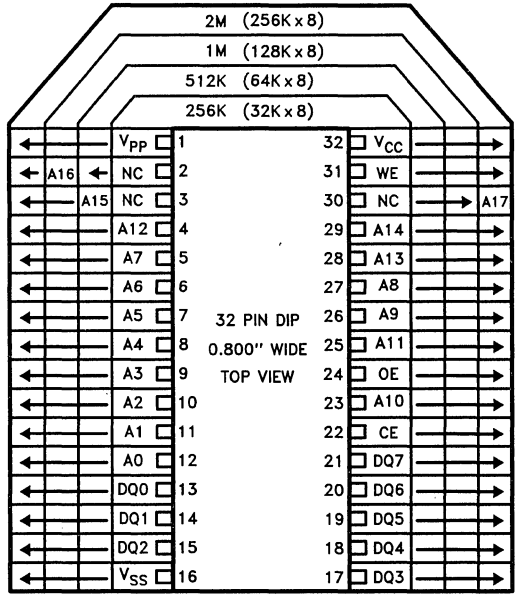


Figure 2A. Flash Memory Pinouts

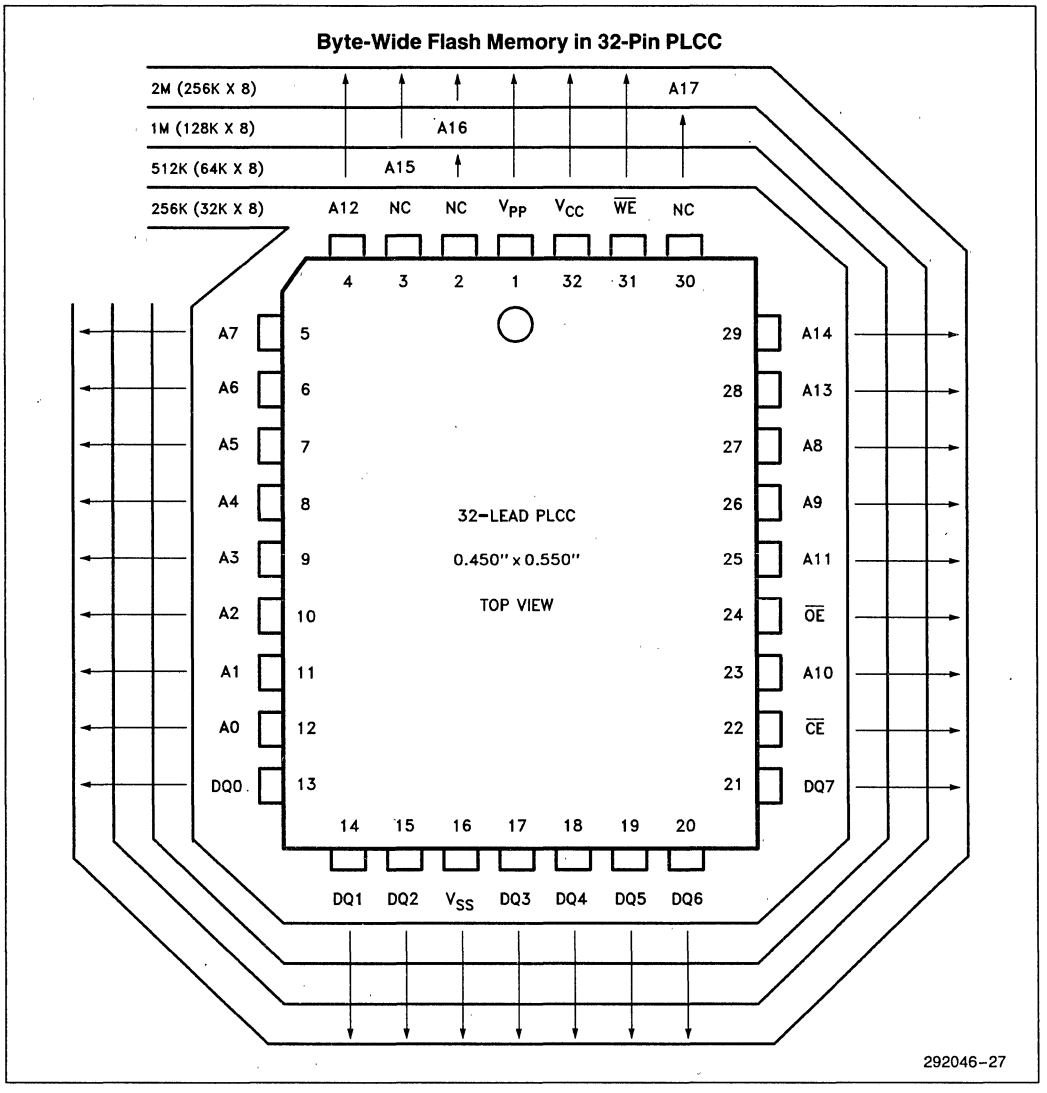


Figure 2B. Flash Memory Pinouts

Table 1. Command Register Instructions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Addr(1)	Data(2)	Operation	Addr(1)	Data(2)
Read Memory(3)	1	Write	X	00H	Read	Valid	Valid
Read int$_e$ligent Identifier™	1	Write	X	90H	Read	00/01H	ID
Set-Up Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Set-Up Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset(3)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Addresses are latched on the falling edge of the Write-Enable pulse.
EA = Address of memory location to be read during erase verify.
PA = Address of memory location to be read during program verify.
2. EVD = Data read from location EA during erase verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
PVD = Data read from location PA during program verify. PA is latched on the Program command.
3. The second bus cycle must be followed by the next desired command register write, given the proper delay times.

2.2 Command Register Architecture

Simplified Processor Interface

Intel's command register architecture simplifies the processor interface. The command register allows CE\, WE\, and OE\ to have standard read/write functionality. All commands such as "Set-up Program" or "Program Verify" can be written with standard system timings. Raising V_{PP} to 12V enables the command register for memory read/write operation, while lowering V_{PP} below V_{CC} + 2V restores the device to a read only memory.

Writing to the register toggles an internal state-machine. The state-machine output controls device functionality. Some commands require one write cycle, while others require two. The command register itself does not occupy an addressable memory location. The register simply stores the command, along with address and data needed to execute the command. With this architecture, the device expects the first write cycle to be a command and does not corrupt data at the specified address. Table 1 contains a list of command register instructions.

The following sections describe the commands in relation to device operation. For more information on the command register see the appropriate flash memory data sheets, and Section 4.4 "Reprogramming Routines".

Read Memory Command—00H

This command allows for normal memory read operations with V_{PP} turned on. After writing the command and waiting 6 μs, the CPU can read from the memory at system speeds. Once placed in the read mode no further action is required on the command register for subsequent read operations.

Read int$_e$ligent Identifier™ Command—90H

Most PROM programmers read the device's int$_e$ligent Identifier to select the proper programming algorithm. On EPROMs, raising A9 to the V_{PP} level configures the device for this purpose. Since this is unacceptable in-system, you can read the flash memory int$_e$ligent Identifier by first writing command 90H. Follow this by reading address 0000 and 0001H for the manufacturer and device ID. Reset the device with the Read Memory command after you have read the identifier.

Set-Up Erase/Erase Commands—20H

Write this command (20H) twice in succession to initiate erasure. The first write cycle sets up the device for erasure. The device starts erasing itself on the second command's rising edge of Write-Enable. Erasure is stopped when the CPU issues the Erase Verify command or when the device's integrated stop timer times out. Integrated stop timers provide a safety net for complex system environments. In these environments, s/w timer accuracy may be difficult to achieve. Some method of timing is still required, however the timer need only meet a minimum specification (10 ms). This is far easier than calibrating a timer to meet both a minimum and maximum specification (10 ms ±500 μs).

NOTE:
Prior to erasure, it is necessary to program all bytes to the same level (data = 00H). See the Quick-Erase™ algorithm for more details.

Erase Verify Command—A0H

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified to see if they erased. Write the Erase Verify command (A0H) to stop erasure and setup verification.

Alternatively, you may allow the internal stop timer to halt erasure. You must still issue the Erase Verify command to set up verification.

The device latches the address to be verified on the falling edge of WE\ and the actual command on the rising edge. Wait 6 μs before reading the data at the address specified on the previous write cycle.

The flash memory applies an internally-generated reference voltage to the addressed byte. Reading 0FFH from the addressed byte in this mode indicates that all bits in the byte are erased with sufficient margin to V_{CC} and temperature fluctuations.

If the location is erased, then repeat the Erase Verify procedure for the next address location. Write the command prior to each byte verification to latch the byte's address. Continue this process for each byte in the array until a byte does not return 0FFH data, or the last address is accessed.

In the case where the data read is not 0FFH, perform another erase operation. (Refer to Set-up Erase/Erase). Continue verifying from the address of the last verified byte. Once you have accessed the last address, erasure is complete and you can proceed to program the device. Terminate the erase verify operation by writing another valid command (e.g., Program Set-up).

Set-up Program/Program Commands—40H

Write this command (40H) twice in succession to initiate programming. The first write cycle sets up the device for programming. The device latches address and data on the falling and rising edges of the second write cycle, respectively. It also begins programming on the rising edge. You stop the programming operation by issuing the Program Verify command, or by allowing the integrated program stop timer to time out. This timer works similiar to the erase stop timer. Again, a minimum specification replaces a tougher minimum/maximum combination (10 μs–25 μs).

Program Verify Command—C0H

Flash memory devices program on a byte-by-byte basis. After each programming operation, the byte just programmed must be verified. Write the Program Verify command (C0H) to stop programming and set-up verification. Should your software allow the integrated stop timer to halt programming, the software must resume the algorithm with the Program Verify command. The device executes this command on the rising edge of Write-Enable. The program Verify command stages the device for verification of the byte last programmed. No new address information is latched.

The flash memory applies an internally-generated reference voltage to the addressed byte. Wait 6 μs for the internal voltages to settle before reading the data at the address programmed. Reading valid data indicates that the byte programmed successfully.

Command Register Reset—FFH

Flash memories reset to the read mode during power-up, and remain in this mode as long as V_{PP} is less than V_{CC} + 2V. If your system leaves V_{PP} turned-on during a *system reset*, then incorporate a command register *device reset* into the hardware initialization routines. This is necessary because the CPU might be controlling programming or erasure when the system reset hits.

Write the reset command (0FFH) twice in succession to reset the device. The double write is necessary because of the state-machine reprogramming structure. For example, suppose the *system* is reset after a Set-up Program command. The flash memory state machine expects the next write cycle to contain valid address and data for programming, followed by another write cycle for program verification. The first Reset command will be mistaken for program data but will not corrupt the existing data. This is because the command (data = 0FFH) is a null condition for flash memory programming. Only data bits programmed to zero pull charge onto the memory cell and change the data. The second write cycle actually resets the device to the read function. Following the second reset cycle, you can write the next command (Read, Program Set-up, Erase Set-up, etc.).

If the V_{PP} supply is turned off upon system reset, the software reset is not required. The flash memory will reset itself automatically when V_{PP} powers down.

Data Protection on Power Transitions

The command register architecture offers another benefit in addition to simplified processor interface—during system power-up and power-down it protects data from corruption by unstable logic. Erasure or programming require V_{PP} to be greater than V_{CC} + 2V and the proper command sequence to be initiated. For example the CPU must write the erase command twice in succession. The odds of this occurring randomly are slim. Additionally, should V_{PP} ramp to 12V prior to V_{CC} ramping past 2.5V, the device will lock out all spurious writes and internally block 12V from the flash memory cells. For even greater security, you can switch V_{PP} as discussed in Section 3.13.

2.3 V_{PP} Specifications

Flash memories, like EPROMs, require a 12V externally-generated power supply for reprogramming. Intel's V_{PP} specifications 12.0V ±0.6V (5%) is compatible with most off-the-shelf (or available in-system) power supplies. (Note, Section 3.1 discusses V_{PP} generation techniques, and Appendix B shows different circuit alternatives.)

It is essential to use the specified V_{PP} when reprogramming the flash memory device. Once the command to erase, program, or verify is issued, the device internally derives the required voltages from the V_{PP} supply. The command register controls selection of internal reference circuitry tapped off of V_{PP}. An improper V_{PP} level causes the references to be wrong, degrading the performance of the part.

(When programming U.V. EPROMs, V_{CC} is raised to 6.5V. On flash memories, the V_{PP} reference circuitry and command register architecture provide the same function while keeping V_{CC} and V_{PP} at static levels. An incorrect V_{CC} level during U.V. EPROM programming poses similar hazards to improper V_{PP} levels on flash memories.)

The hardware design section discusses various methods for generating V_{PP}.

3.0 HARDWARE DESIGN FOR ISW

Covered in this section are the following:

- Description of ISW-specific functional system blocks including memory requirements
- V_{PP} generation techniques
- Communication Considerations

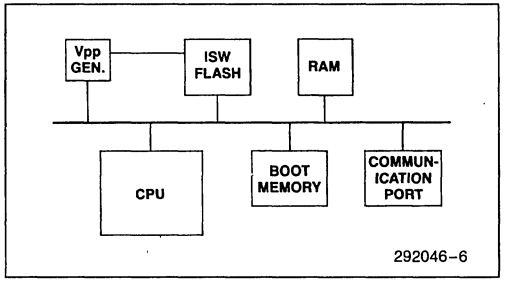


Figure 3. System Block Diagram

System Level Hardware Requirements for ISW:

- processor or controller
- limited amount EP/ROM or other flash memory devices for boot code, communications s/w, and reprogramming algorithms
- limited amount of RAM for variable storage (i.e., stacks, buffers, and other changing parameters)
- data import capability (i.e., serial line, LAN, floppy disk)
- flash memory for nonvolatile code or data storage needs
- V_{PP} generator or regulator

All of the functional blocks in Figure 3 are typical of any embedded or reprogrammable system with the exception of the V_{PP} generator. Some microcontrollers have on-chip EP/ROM, RAM and a serial port. With these devices, implementation of the ISW capability requires little additional hardware.

The next section discusses V_{PP} generation techniques and communications design considerations.

3.1 V_{PP} Generation

A static V_{PP} is needed to reprogram flash memories. The V_{PP} voltage can be generated by:

1) regulating it down from a higher voltage;
2) pumping it up from a lower voltage (i.e., charge pump, DC/DC converter, etc.); or
3) designing or specifying the system's 12V supply with the required ISW tolerances and specifications.

Sufficient current for reprogramming should be considered when selecting your V_{PP} generation option. Parallel reprogramming for flash memory in 16-bit or 32-bit systems will require, respectively, 2X or 4X additional current capability.

3.1.1 REGULATING DOWN FROM HIGHER VOLTAGE

V_{PP} is obtained from a higher voltage by using a linear regulator. Given the higher voltage, regulation offers the least expensive method of generating V_{PP}. Standard three terminal 12V ±1%, ±2%, ±4% non-adjustable regulators are available off-the-shelf. Some regulators have on/off control built-in. (See Appendix B, V_{PP} Circuit #1.) All regulators require a minimum input voltage greater than the output voltage. (See Appendix B, V_{PP} Circuit #2 and #3.)

3.1.2 PUMPING 5V UP TO 12V

V_{PP} can be obtained by pumping V_{CC} and regulating it to the proper voltage. A voltage charge-pump can be designed and built by using a charge-pump integrated circuit and some discrete components (see Appendix B, V_{PP} Circuit #4) or by using a monolithic DC/DC converter (see Appendix A, V_{PP} Circuit #5).

When using adjustable circuits containing discrete components, design the output voltage so it falls within the V_{PP} specifications for all corners of the components'

skew (i.e., V_{CC} ±10%; Rx ±1%, Ry ±1%, etc.). Include the resistors' temperature coefficients in the calculation matrix. Note that each of the various components can add error to the V_{PP} supply.

The monolithic DC/DC converter shown in Appendix B Circuit #5 fits into a 24-pin socket. It offers the advantages of close temperature tracking and ease of implementation. It has also been characterized at temperatures and meets all the V_{PP} specifications. Appendix C contains a partial list of vendors selling DC/DC converters.

Most DC/DC converters are only 50–60% efficient, so heat dissipation may be a concern. Some discrete boost circuits such as Appendix B, Circuit #4, offer much higher efficiency (70-85%). Circuit #4 as shown can supply 200 mA. Smaller inductor and capacitor component values and higher frequency boost convertors can be used where less power is required. For example, designs which reprogram one or two flash memories simultaneously might use the LT1172. (Contact Linear Technologies for more information.)

In all V_{PP} generation methods, a capacitor on the input voltage terminals reduces the output noise voltage. Some power supplies (Appendix B, Circuits #3 and #4) specify a large-valued capacitor to decrease the Effective Series Resistance (ESR). Place a 0.1 μF capacitor within 0.25 inches of each flash memory's V_{PP} input (in addition the one on the V_{PP} generator's input).

NOTE:
The ESR is inversely proportional to the capacitance value and the rated working voltage. To lower the ESR choose a capacitor with a large capacitance and a high working voltage (i.e., above 100V).

3.1.3 ABSOLUTE DATA PROTECTION—V_{PP} ON/OFF CONTROL

With V_{PP} below V_{CC} +2V or V_{CC} below 2.5V, internal circuitry disables the command register and eliminates the possibility of inadvertent erasure or programming. Switching the V_{PP} supply off provides the secondary benefits of improved power and thermal management.

There are two ways to switch V_{PP} on and off:

1) directly switch the V_{PP} generator's output, or
2) switch the input voltage supplying the regulation circuit.

Any switching circuit will cause a voltage drop, so choose a switch with this drop in mind. Some power supplies have asymmetrical tolerances on 12V (i.e. +5%, −4%). Flash memory allows the 12V supply to drop as low as −5%. The 1% difference between the supply and the device requirement allows the switch to have an ON resistance voltage drop of 0.12V. Continuing with this example, assume the system only reprograms one flash memory at a time. The current through the switch into the flash is I_{PP} = 30 mA. Solving for the allowable resistance across the switch: R = V/I = (0.12V)/(30 mA) = 4 Ohms. See Figure 4. Example Voltage Drop Across Switch. Note, one can reduce the effective R_{DS} (ON) by placing 2 or more FETs in parallel if necessary.

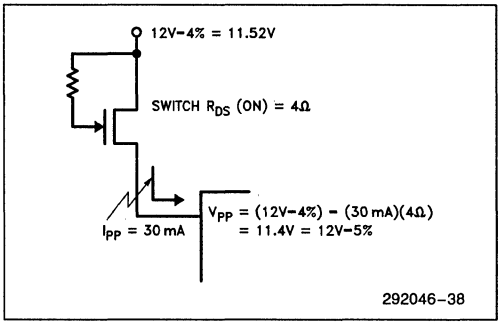


Figure 4

Controlling the input voltage of a DC/DC convertor with a MOSPOWER FET is another straightforward approach. (See Appendix B, Circuit #5.) Choose the FET switch carefully. It should have a very low on-resistance to minimize the voltage divider effect of the converter and FET switch. If the voltage across the FET switch is too high, the converter will not have the proper input voltage to meet its specifications. Always design the switching circuit with sufficient margin to maximum V_{PP} and V_{CC} load currents.

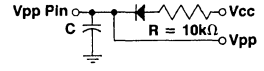
3.1.4 WRITES AND READS DURING V_{PP} TRANSITIONS

After switching V_{PP} off, the CPU can read from the flash memory without waiting for the capacitors on V_{PP} to bleed off. To do this, write the Read Memory command prior to issuing the V_{PP}_OFF instruction. Alternatively, the device resets automatically to read mode when V_{PP} drops below V_{CC} +2V.

Raising V_{PP} to 12V enables the command register. You must wait 100 ns after V_{PP} achieves its steady state value before writing to the command register. Remember that the steady state V_{PP} settling time depends on both the power supply slew rate and the capacitive load on the V_{PP} bus.

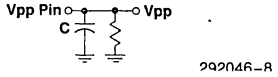
3.1.5 OTHER V_{PP} CONSIDERATIONS

The V_{PP} pin is an MOS input which can be damaged by electrostatic discharge (ESD). In OBP applications, an external power source supplies V_{PP} and then is removed. Electrostatic charge can build up on the floating V_{PP} pin. You can solve this problem by one of two means: 1) tie the pin to V_{CC} through a diode and pull-up resistor (Figure 5a) or through a resistor to ground (Figure 5b). With either approach use a 10 KΩ or larger resistor to minimize V_{PP} power consumption.



292046-7

a. V_{PP} Tied to V_{CC} for OBP



292046-8

b. V_{PP} Tied to Ground

Figure 5

NOTE:
Typically EPROMs require V_{PP} to be within one diode drop of V_{CC} for optimal standby power consumption. Either approach can be used with the flash memory.

ISW applications do not require this ESD protection as most regulators and charge pumps contain a voltage divider on the output stage. A divider provides a resistive path to ground even with the supply turned off. (Note: check the schematics of the V_{PP} supply chosen.) However, if you directly switch the V_{PP} supply, add the resistor to ground; the switch isolates the V_{PP} pin and allows charge to build up.

3.1.6 V_{PP} CIRCUITRY AND TRACE LAYOUT

You should lay out V_{PP} circuitry and traces for high frequency operation since programming power characteristics exhibit an AC current component. Use the following standard power supply design rules:

- Keep leads as short as possible and use a single ground point or ground plane (a ground plane eliminates problems).
- Locate the resistor network (or a regulator) as close as possible to the adjustment pin to minimize noise pick-up in the feedback loop. The resistor divider network should also be as short as possible to minimize line loss.
- Keep all high current loops to a minimum length using copper connections that are as wide as possible. (This will decrease the inductive impedance which otherwise causes noise spikes.)
- Place the voltage regulator as close to the flash memory as practical to avoid an output ground loop. Excessive lead length results in an error voltage across the distributed line resistance.
- Separate the input capacitor return from the regulator load return line. This eliminates an input ground loop, which could result in excessive output ripple.

3.2 Communications—Getting Data to and from the Flash Memory

The flash memory does not care about the origin of the data to be programmed. The data could be downloaded from a serial link, parallel link, disk drive, or generated locally as in data accumulation applications.

While most systems communicate via serial link, sending a font to a printer's flash memory is an example of a parallel interface. In either format, designers must decide whether or not to buffer the incoming data. Error-free serial protocols will require buffering for reconstruction of information packets. With equal capacity of RAM and flash memory in a system, the download time would only be limited by the speed of the communication link.

Both worst case and typical analysis must be done for real time download and un-buffered programming. The maximum transmission rate is 19.2K baud assuming worst case programming times. The time between characters at 19.2K baud is 520 μs; the worst case byte programming time is approximately 0.5 ms (including software overhead). Typical byte programming takes 16 μs which allows for much higher unbuffered transmission rates. However, a single byte can take up to the full 400 μs specified time (plus software overhead), so you should not base transmission rate on typical programming times.

Partial buffering or FIFO schemes can also be implemented to increase transmission rates. An argument for buffering is reduction of interconnect time and costs.

4.0 SOFTWARE DESIGN FOR ISW

6

Covered in this section are the following software requirements:

- system integration of ISW
- reprogramming considerations for single- and multiple-flash memory based designs.

4.1 System Integration—Boot Code Requirements

Boot code in remote systems should contain various ISW-specific procedures in addition to standard initialization and diagnostic routines.

The most dependable boot code for remote version updates contains some basic communications capability and the ISW reprogramming algorithms. Thus, a data-link disruption while reprogramming would be recoverable. For manufacturing flexibility, this boot memory could be an OBP 256K flash memory.

1. Bootstrap, and reset flash memory;
2. Check "HOST_INT" and "VALID_AP" flags:

   If HOST_INT is inactive and VALID_AP = 4150H, jump to application start address;
3. If VALID_AP<>4150H, loop and wait for host (the link probably went down during update);
4. When "HOST_INT" is active, vector to host interaction code.

   (See next section.)

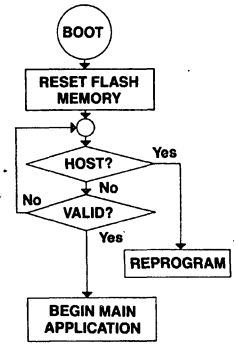


Figure 6. Example of ISW Integration to the Boot Sequence

An alternative to storing these routines in a separate boot device is storing them in the flash memory containing the program code. Prior to erasure, the CPU would transfer the ISW routines to system RAM and execute from there. This type of approach is suitable for battery-operated equipment or systems with back-up power supplies.

The communication link could be disrupted during reprogramming, leaving the device in an unknown configuration. Therefore, the boot code should reset the flash memory and check two ISW flags. The following section discusses the flag check concept.

4.1.1 ISW FLAG CHECK

After resetting the flash memories and initializing other system components, the CPU should check the communications link for a host interrupt. We will call this the HOST_INT flag. Had the communication link gone down prior to completion of downloading, then the host would have to re-establish contact to complete the task.

Assuming no HOST_INT request has been made, the boot protocol then checks a data sequence in the flash memory signifying a valid application (VALID_AP). You program this sequence into the memory array after confirmation of a successful download. If a download is interrupted midway through erasure or programming, then the VALID_AP flag locations will not contain the VALID_AP code. On the next system bootstrap the CPU recognizes this and holds up system boot until valid code is programmed. In Figure 6 an example flag protocol uses the VALID_AP sequence of 4150H (ASCII codes for "AP").

4.2 Communication Protocols and Flash Memory ISW

The remote download communications protocol must guarantee accurate transmission of flash memory instructions and program code. This protocol can be as simple as a read-back technique or as complex as an error-free transmission protocol. (See Figure 7 for possible system-level flash memory instructions.)

A simple read-back technique optimizes download for boot code memory needs and ease of implementation. The embedded CPU echoes the flash memory instruction (i.e., Erase or Program) to the host, and waits for a confirmation prior to execution. After programming the update, the remote system checks the update by transmitting it back to the host for confirmation. The remote system then programs the VALID_AP sequence. Note that programming and reading back 64 Kbytes at 19.2K baud takes about 0.57 minutes per direction:

(65,536 bytes) * (10 bits/byte) * (1 sec/19.2 Kbits) * (1 min/60 sec) = 0.57 minutes.

Implementing either software- or hardware-based error-free communications protocol improves transmission efficiency. It eliminates the possibility of errant data being programmed if not buffered and checked, and optimizes the download process for transmission time. Additionally, file compression and decompression routines can improve the transmission rate.

General ISW instructions include:
- **STATUS CHECK**
- **INITIATE REPROGRAMMING**
- **MOVE ISW ROUTINES FROM FLASH MEMORY TO RAM (If not resident in separate boot memory)**

Data accumulation-specific commands include:
- **RETRIEVE DATA**
- **ERASE FLASH MEMORY**

Figure 7. Sample System-Level ISW Instruction Set

Status Check

The host should request a status update from the remote system prior to sending a reprogramming instruction. Depending on the response, the host may break the link and reconnect later, or it may send an erasure or data-upload command. This type of handshaking is necessary when system downtime for reprogramming might not be acceptable. An example of this is an automated factory where robots handle caustic chemicals.

4.3 Data Accumulation Software Techniques

Data can be accumulated in a remote environment with flash memory and then uploaded to a host computer for manipulation. You can adapt various standard data-logging techniques for use with flash memory. With any technique, you determine the next available memory location by reading for erased data (0FFH). This address would only be located once on system bootstrap and then recalled from RAM and incremented as needed.

Given a repeating data string of known length and composition, program start and stop codes at either end of the string. Do not pick 00H or 0FFH data for these codes because they are used during erasure. The start and stop codes enable the CPU to differentiate between available memory for logging and logged data equal to 00H or 0FFH.

For non-regular data input, you can address this same issue by programming the logged data followed by the variable identifier. Again, do not pick 00H or 0FFH data for the variable identifiers.

With any technique, the host computer separates and manipulates the data after the uploading operation.

4.4 Reprogramming Routines

Intel's ETOX flash memories provide a cost-effective updatable, non-volatile code storage medium. The reliability and operation of the device is based on the use of specified erasure and programming algorithms.

Intel offers reprogramming software drivers to make it easy for you to design and implement flash memory applications. The software is designed around the CPU-family architectures and requires minimal modification to define your system parameters. For example, you supply the memory width (8-bit, 16-bit, or 32-bit), system timing, and a subroutine for control of V_{PP}.

NOTE:
Contact your nearest sales office for details.

If you prefer to implement the algorithms yourself, they are outlined in the device data sheets. Command register instructions required for the various operations are included in the data sheet flow charts.

The following sections describe both single-device and multiple-device parallel reprogramming implementations.

4.4.1 Quick-Erase™ Algorithm

Flash memories chip-erase all bits in the array in parallel. The erase time depends on the V_{PP} voltage level (11.4V–12.6V), temperature, and number of erase/write cycles on the part. See the device data sheets for specific parametric influences on reprogramming times.

Note that prior to erasing a flash memory device the processor must program all locations to 00H. This equalizes the charge on all memory cells insuring uniform and reliable erasure.

Algorithm Timing Delays

The Quick-Erase algorithm has three different time delays:

1) The first is an assumed delay when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on V_{PP}, the delay required is proportional to the number of flash memory devices times 0.1 μF/device. V_{PP} must reach its final value 100 ns before the CPU writes to the command register. Systems that hardwire V_{PP} to the device can eliminate this delay.
2) The second delay is the "Time Out TEW" function, where TEW is the erase timing width. The function occurs after writing the erase command (the second time) and before writing the erase-verify command. The erase-verify command or the integrated stop timer internally stops erasure.

   TEW for ETOX II flash memories is a minimum of 10 ms. This delay can be either software or hardware controlled. Either way, the minimum nature of the timing specification allows for interrupt-driven timeout routines. Should the interrupt latency be longer than the minimum delay specification, the stop timer halts erasure.
3) The third delay in the erase algorithm is a 6 μs time out between writing the erase verify command and reading for 0FFH. During this delay, the internal voltages of the memory array are changing from the

erase levels to the verify levels. A read attempt prior to waiting 6 μs will give false data—it will appear that the chip does not erase. Repeatedly trying to erase verify the device without waiting 6 μs will cause over-erasure. This delay is short enough that it is best handled with software timing. Again, note that the delay specification is a minimum.

High Performance Parallel Device Erasure

In applications containing more than one flash memory, you can erase each device serially or you can reduce total erase time by implementing a parallel erase algorithm.[7] You save time by erasing all devices at the same time. However, since flash memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the command register Reset command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020h twice in succession. This starts erasure. After 10 ms, the CPU writes the data word verify command A0A0h to stop erasure and setup erase verification. If both bytes are erased at the given address, then the CPU increments the address (by 2) and then writes the verify command A0A0h again. If neither byte is erased, then the CPU issues the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFh data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFh and the verify command would be A0FFh. Once the high byte verifies at that address, the CPU modifies the command back to the default 2020h and A0A0h, increments the address by 2, and writes the verify command to the next address.

See Figure 8 for a conceptual view of the parallel erase flow chart and Appendix D for the detailed version. These flow charts are for 16-bit systems and can be expanded for 32-bit designs.

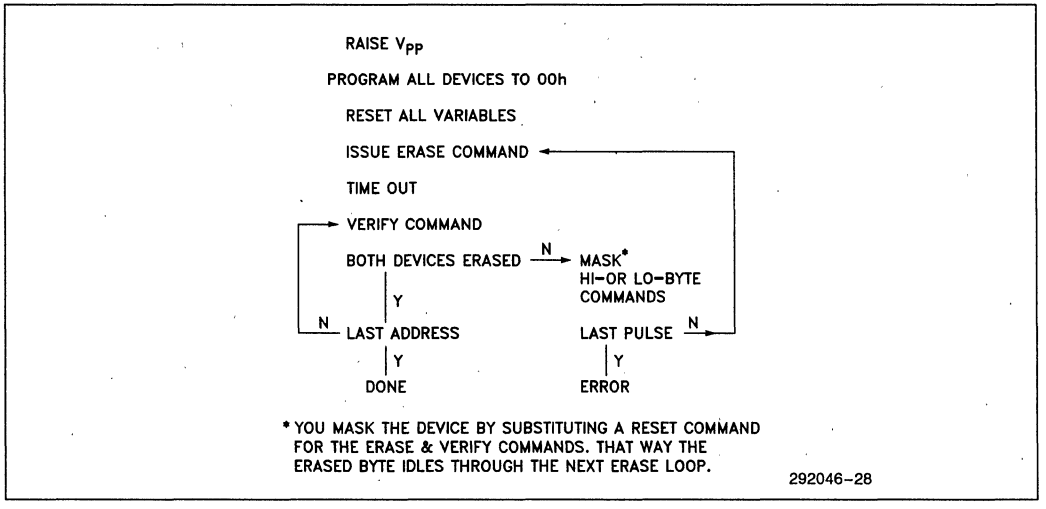


Figure 8. High Performance Parallel Erasure (Conceptual Overview)

7. Parallel Erasure and Programming require appropriate choice of V_{PP} supply to support the increased power consumption.

4.4.2 Quick-Pulse Programming™ Algorithm

Flash memories program with a modified version of the Quick-Pulse Programming algorithm used for U.V. EPROMs. It is an optimized closed-loop flow consisting of 10 μs program pulses followed by byte verification. Most bytes verify after the first pulse, although some may require more passes through the pulse/verify loop. As with U.V. EPROMs, this algorithm guarantees a minimum of ten years data retention. See the device data sheets for more details on the programming algorithm.

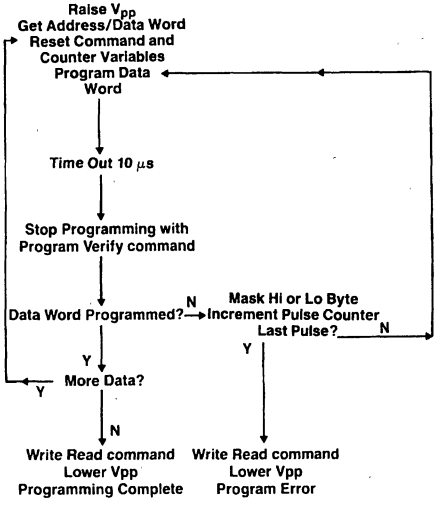
Algorithm Timing Delays

The Quick-Pulse Programming algorithm has three different time delays:

- The first and third—V_{PP} set-up and verify set-up delays—are the same as discussed in the erasure section. In this case the third delay is for the transition between writing the Program Verify command and reading for valid data.
- The second delay is the "Time Out 10 μs" function, which occurs after writing the data and before writing the program-verify command. This write command internally stops programming. The section entitled "Pulse Width Timing Techniques" gives 86-family assembly code for generating a 10 μs timer routine.

High Performance Parallel Device Programming

Software for word- or double-word programming can be written in two different manners. The first method offers simplicity of design and minimizes software overhead by using a byte programming routine on each device independently. Here you increment the address by 2 or 4 when addressing 1 of 2 or 4 devices, respectively. The second method offers higher performance by programming the word or double-word data in parallel. This method manipulates the command register instructions for independent byte control. See Figure 9 for conceptual 2-device parallel programming flow chart and Appendix E for the detailed version.



*You mask the device by substituting a Reset command for the Program and Verify commands. That way, the programmed bytes do not get further programmed on subsequent pulses.

Figure 9. Parallel Programming Flow Chart (Conceptual Overview)

6

NOTE:
Word or double-word programming assumes 2 or 4 8-bit flash memory devices.

Parallel Programming Algorithm Summary:

- Decreases programming time by programming 2 flash memories (16 bits) in parallel. The algorithm can be expanded for 32-bit systems.
- Eliminates tracking of high/low byte addresses and respective number of program pulses by directing the CPU to write data-words (16-bit) to the command register.
- Maintains word write and word read operations. Should a byte on one device program prior to a byte on the other, the CPU continues to write word-commands to both devices. However, it deselects the verified byte with software commands. An alternative is to independently program high and low bytes using hardware select capability.

4.4.3 Pulse Width Timing Techniques

Software or hardware methods can be used to generate the timing required for erasure and programming. With either method you should use an in-circuit emulator (ICE™) and an oscilloscope to verify proper timing. Also remove the flash memory device from the system during initial algorithm testing.

Software Methods and Examples

Software loops are easily constructed using a number of techniques. Timing loops need to be done in assembly language so that the number of clock cycles can be obtained from the instructions.

In order to calculate a delay loop three things are needed—

1) processor clock speed,
2) clock cycles per instruction, and
3) the duration of the delay loop.

As an example, the 80C186 divides the input clock by 2. With a 20 MHz input clock the processor's internal clock runs at 10 MHz. This translates to a 100 ns cycle time. Delays can be made by loading the CX register with a count and using the LOOP instruction. The LOOP instruction takes 16 clock cycles to execute per pass. It decrements the CX register on each pass and jumps to the specified operand until CX equals zero.

When writing a delay loop consider all instructions between the start and end of the delay. If a macro is written that delays 10 μs, add the clock cycles for all instructions in the macro.

Here is an example of a 10 μs delay and the calculation of the constant required for a 10 MHz 80C186.

```
WAIT_10 μs:
        push cx             ;10 clock cycles
        mov cx,DELAY        ;4 clock cycles
        loop $              ;see calculation
        pop cx              ;10 clock cycles

1. Start to End     = 10 μs/cycle time
                    = 10 μs/100 ns
                    = 100 cycles

2. Loop Instruction = 100–24 cycles
                    = 76 cycles

3. Loop Cycles      = 76
                    = (15 × [DELAY − 1] + 5)

4. Solving for DELAY = 6
```

Hardware Methods

Using an Internal Timer—

Many microcontrollers and some microprocessors have on-chip timers. At higher input clock speeds these internal timers have a resolution of 1 μs or better. The timers are loaded with a count and then enabled. The timer starts counting and when it reaches the terminal count a bit is set. The CPU executes a polling algorithm that checks the timer status. Alternatively, a timer-controlled interrupt can be used. After the timer has been set and the interrupt enabled, the CPU can be programmed to wait in idle mode or it could continue executing until the timed interrupt.

One thing to take into account when using interrupts is the time required for the CPU to recognize and interrupt request (interrupt latency). This is important when figuring the timer value, because the time seen by the part will be the programmed delay plus the minmum interrupt latency time.

The 80C186 has three 16-bit timers on-chip. Timer #2 can be a prescaler for the other two timers, which extends timers #0 and #1 range out to 2^32. By using two timers, 10 µs pulses and 10 ms pulses can be easily achieved.

Using an External Timer—

External timers can take many forms. One popular example is the 82C54 (CHMOS Programmable Interval Timer) which has three 16-bit timers on-chip. One timer can be used as a prescaler for the others so that a count of 2^32 can be achieved as with the 80C186 internal timers.

5.0 SYSTEM DESIGN EXAMPLE: AN 80C186 DESIGN

A general purpose controller and/or data acquisition system was built to demonstrate 86-based ISW. The 80C186 CPU drives the system, which contains 16 Kbytes of EPROM (two 27C64's), 64 Kbytes of flash memory (two 28F256's), 64 Kbytes of SRAM (two 32K x 8's) three 8-bit ports (82C55A), one serial port (82510), and a 5V to 12.0V DC/DC converter. Three 74HC573's demultiplex the address/data bus and latch the byte high enable line (BHE) and the status lines (if needed). Two data transceivers (74HC245) simulate the worst case data path for a system requiring added drive capability. If the transceivers are not needed they can be replaced with wired headers. See Appendix F for detailed schematics parts list, and changes for the 28F512 or 28F010.

The 80C186 reset (output) drives the reset input on the 82510, 82C55A, and the OE\ inputs on the address latches and data transceivers. The reset line goes inactive 5 clock cycles before the first code fetch. Also, the CPU's write signal is split into byte-write-high and byte-write-low to allow for byte or word writes.

The 80C186 has on-chip memory and peripheral chip selects. Two of the memory chip selects are dedicated. One is the Upper Chip Select (UCS, dedicated for the boot area) and the second is the Lower Chip Select (LCS, for the interrupt vector table area). See the memory map in Figure 10.

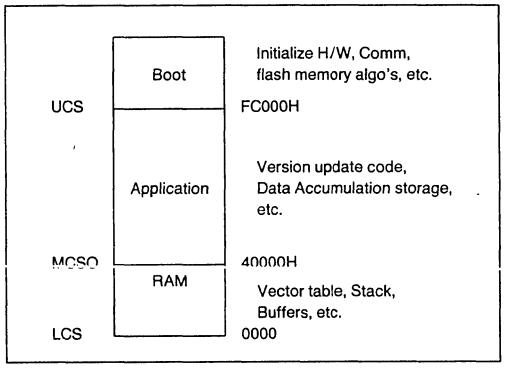


Figure 10. 80C186 Memory Map

The permanent code was placed in an EPROM in the UCS memory segment; this code includes routines for hardware initialization, communications, data uploading and downloading, erasure and programming algorithms, I/O drivers, ASCII to binary conversion tables, etc. This would be useful for systems reconfigured for different communication protocols as the last step prior to shipment.

Code and constants that might change are placed in the 64 Kbytes of flash memory. Application examples include operating systems, code for rapidly advancing biomedical technologies such as blood test software, engine-control code and parameters, character fonts for printers, postage rates, etc. The RAM is used for the interrupt table, stack, variable data storage, and buffers.

The three 8-bit ports on the 82C55A peripheral controller can be used for control and/or data acquisition. It powers-up with all port pins high. Similarly, all port pins go high after warm resets as well. Because the pins are high after a power-up/reset, an open collector invertor was used to control the MOSPOWER switch which in turn controls V_{PP}. You must drive the FET switch to one rail or the other to guarantee its low on-resistance. V_{PP} is turned off during power-up or reset as a hardware write protection solution. The DC/DC converter supplies V_{PP}.

The 82510 is a flexible single channel CHMOS UART offering high integration. The device off-loads the system and CPU of many tasks associated with asynchronous serial communications.

The part can be used as a basic serial port for the host serial link, or can be configured to support high speed modem applications. For more information on the 82510 see the 82510 data sheet and AP-401 "Designing with the 82510 Asynchronous Serial Controller".

Software was written to download code and data parameters (code updates) from a PC to the demo board through the PC's COM1 port (serial port). The system also can upload data (remote data acquisition) to the PC via the same link.

Once the download code and data has been programmed it can not be lost, even if power should fail. This is because Intel's ETOX flash memory technology is based on EPROM technology and does not need power to retain data.

The end result: rugged, solid state, low power nonvolatile storage.

6.0 SUMMARY

Intel's flash memories offer designers cost-effective alternatives for remote version updates or for reliable data accumulation in the field or factory. Designers will also benefit from time savings in any kind of code development—no 15 minute waits for U.V. EPROM erasure.

This application note covers the basics of in-system writing to flash memories and can be used as a check list for systems other than the 80C186 design shown. The basic concepts remain the same: a CPU controls the reprogramming operations; a 12V supply must be applied to the flash memory for erasure and programming; and a communications link connects the host to the remote system and supplies the code to be programmed.

APPENDIX A
ON-BOARD PROGRAMMING DESIGN CONSIDERATIONS

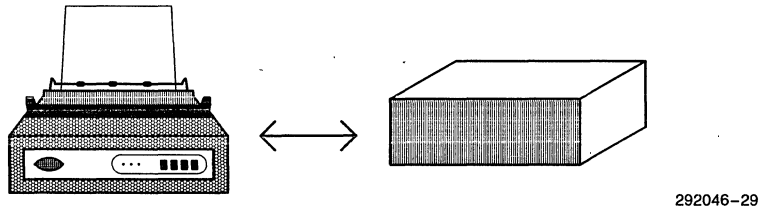
INTRODUCTION

On-board programming[1] (OBP) with Intel's flash memory provides designers with cost reduction capabilities for alterable code storage designs. When used in conjunction with on-board programming, flash memory presents opportunities for savings in two areas: greater testability in the factory, which translates to improved outgoing quality and reduced return rate; and quicker, more reliable field updates, which translates to decreased product support cost.

This appendix:

- outlines the design considerations associated with on-board programming, and the improvements afforded by Intel's flash memory;
- offers guidelines for converting current 64K EPROM OBP designs;
- designs an 8-bit system for on-board programming;
- suggests some 16-bit flash design considerations; and offers information on OBP equipment and vendors.

1. With on-board programming, non-volatile memory is programmed while socketed or soldered on the application board, rather than before hand as a discrete component. This programming method is also called in-module or in-circuit programming, and has been practiced by some major corporations since 1981. See sidebar on following pages for more information on U.V. EPROM OBP usage.



On-Board Programming Manufacturing Example—A printer is customized via OBP for international markets: 1. printer assembly completed, diagnostics code programmed and tested, and unit stored in inventory; 2. order arrives for printer with foreign language font; 3. diagnostics code flash-erased, and desired font programmed; 4. printer ships to customer.

INTEL'S FLASH MEMORY—DESIGNED TO MEET YOUR OBP NEEDS

Intel's flash memory simplifies OBP code updates by offering designers the command register architecture. As described in section 2.2, this architecture offers the full reliability of EPROM off-board programming without the hassles of elevating V_{CC}.

5 Volt Vcc Erasure and Programming Verification

Unlike EPROM OBP, flash memory enables Vcc to remain at 5.0V throughout all operations. Internal circuitry derives the erasure and programming verification levels from the voltage on Vpp rather than from Vcc. These verify modes enable use of a single Vcc bus for the entire board, as opposed to the two buses needed for U.V. EPROM OBP. (See sidebar entitled EPROM OBP).

EPROM OBP

EPROM OBP has been a proven manufacturing technique since 1981. Ingenuity and clever circuit design have enabled manufacturers to overcome the hurdles associated with OBP and enjoy the benefits.

In many cases, Intel's flash memory simplifies today's solutions and offers new capabilities to advance the state of OBP technology. The following paragraphs outline the hurdles and a few of the solutions in use today.

EPROMs require program verification at an elevated V_{CC} to insure long-term data retention. PROM programmers easily accommodate this requirement, and it is generally invisible to the end-user.

REPLACING CURRENT EPROM OBP DESIGNS WITH FLASH MEMORY

Hardware Considerations

A slight hardware modification is required to adapt most of the current EPROM OBP designs for use with Intel's flash memory. Simply convert the EPROM memory sites from 28 to 32 pins. All other board-design cirteria used for EPROM OBP apply to flash memory as well. (For discussions of these criteria see section entitled New OBP Designs).

Standard EPROM OBP requires the board designer to bus $\overline{PGM}$ to the edge connector. With flash memories' command register architecture, this same trace enables electrical erasure and programming, only now the line is called Write Enable ($\overline{WE}$). The timing for $\overline{WE}$ is similar to that of read accesses, although that is handled via software changes.

Another potential hardware change is on the board programmer side of the design–the V_{PP} supply. Many EPROMs program with 12.5-13.0V V_{PP} supplies. Intel's ETOX II flash memory requires 11.4-12.6V V_{PP}. This change should not be an issue since the V_{PP} supply on many board programmers is programmable.

Mixed memory systems containing both conventional U.V. EPROM and flash memories require special consideration. This type of memory design requires separation of the Chip Enable ($\overline{CE}$) control lines between the EPROM and flash devices to allow for independent re-programming control and access. The $\overline{PGM}$ and $\overline{WE}$ lines can be common if the board programmer can give the appropriate timings to either type of device.

Software Considerations

Manufacturers who program EPROMs on-board today will need new board-programmer software to take advantage of flash memory's feature set, specifically software for the Quick-Erase™ and Quick-Pulse Programming™ algorithms.

Benefits of Converting Your EPROM OBP Design to Flash

The most pressing reason to convert from a standard EPROM to flash memory is the total cost savings. To appreciate this, you must consider your way of doing business at the board and system levels—from the factory to installation and repair in the field. In the factory, boards can be tested with a diagnostics program in the flash memory and then erased and reconfigured for shipment in the same step. Improved testing will decrease the probability of field failures and costly customer returns. Simplified test and rework methods will decrease your inventory holding costs. Also, if in the process of converting to flash memory you include the ability to OBP via a cable-connector, service calls for code updates will be quicker, more reliable, and cost less money. Your serviceman would simply connect the programming equipment to the system without dismantling it to remove the EPROMs. (See section entitled The System/Board-Programmer H/W Connection for details.)

EPROM OBP (cont'd)

With OBP, the EPROM board-programmer handles the elevated-V_{CC} requirement easily as well. However, when V_{CC} is greater than 5V, logic devices populating the same board may draw excessive current and not operate predictably.

One solution to this issue involves running separate V_{CC} traces to the board's edge connector—one for EPROM programming, and one for powering up the rest of the board.

A second consideration when designing for EPROM OBP has been accessing manufacturer and device codes.

The identifier mode requires forcing A9 to 12V. This translates to adding extra isolation, which implies the increased costs of buffers and extra board space.

NEW OBP DESIGNS

Design Considerations

As with EPROM in-circuit programming, flash memory board programming requires the use of a board-programmer. Unlike U.V. erasure for standard EPROM OBP, electrical erasure enables flash memory OBP without removing the board from the system.

We will look at designing a board that is to remain powered-up in the system during erasure and reprogramming. The key concept is to design the board in such a way that the programmer can take control of the system during code updates. The implementation of such a design is straightforward, easy, and suited to automated production assembly.

Taking Control

The board-programmer needs to take control of the system's address bus, data bus, control lines, etc. to update the code without damaging the system. (See Figure 2. System to Board-Programmer Interface.) Taking control simply means isolating the rest of the system from these lines.

Various methods of isolating the memory from the system include using tristate buffers, latches, or even the capabilities designed into microprocessors (μP) and microcontrollers (μC). For example, Intel's 86-based μP family has HLD/HLDA signals that were set-up for multiprocessor system designs where bus control is a major concern. The HLD signal, when acknowledged, tristates the address, data, and control lines. Although not designed for multiprocessor environments, Intel's MCS®-51 and MCS-96 microcontroller families have Reset capabilities to help simplify this same task.

One issue to be aware of when using a CPU's reset control function is that it may switch from the reset to active condition at a non-standard logic level. This only presents a problem if the address/data buffer takes longer to activate than the CPU, and the CPU attempts to fetch code from a memory device isolated from it.

One approach to insure successful programming takeover (i.e. without bus contention) is to have the board-programmer's lines in a high impedance state during connection to the system. Once connection to the system has been secured, the serviceman could hit a button on the board-programmer to start the system takeover procedure. Then when total control has been established, the programmer would commence with erasure and reprogramming.

Aside from the flash device's isolation from the system, various CPU control lines ($\overline{\text{MEMRD}}$, $\overline{\text{WE}}$, $\overline{\text{PSEN}}$, etc.) may need isolation as well. If active during Reset, these lines may put the CPU into an unspecified state. When designing a board for OBP, check the μC/μP data sheets carefully for any special reset conditions.

Printed Circuit Board Guidelines for V_{CC} and V_{PP}

Programming conventional EPROM and flash memories takes 30 mA of current on V_{CC} and V_{PP}, due to the nature of hot-electron injection. Most of the charge transfers to the memory cell's floating gate in a short current spike during the first pulse. You should design both the V_{CC} and V_{PP} traces with A.C. current spikes in mind. Wherever possible, limit the inductance by widening the two traces. Bypass capacitors (0.1 μF) should be placed as close as possible to the memory device's V_{CC} and GND pins, as well as the devices V_{PP} and GND pins. The capacitor on Vcc decreases the power supply droop. The capacitor on V_{PP} supplies added charge, and filters and protects the memory from high frequency over-voltage spikes[2].

2. For a complete discussion of electrical noise, grounds, power supply distribution and decoupling see Ap-74—High Speed Memory System Design Using the 2147H, and AP-125—Designing Microcontroller Systems for Electrically Noisy Environments.

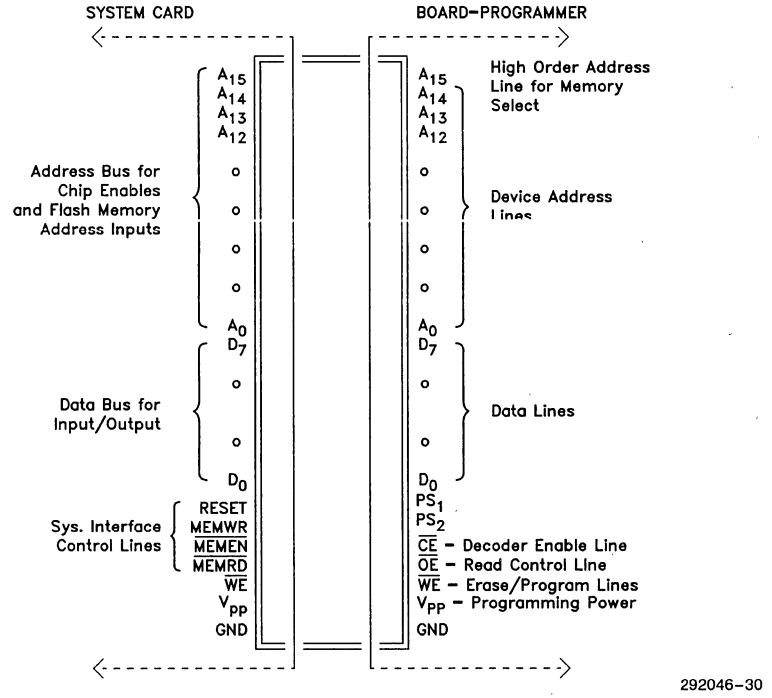
EPROM OBP (cont'd)

Some users of OBP get around this issue by programming all EPROMs with a common algorithm. However, this practice compromises the device's reliability, and should not be done.

A better solution than ignoring the identifier is to choose a qualified EPROM vendor and program with its algorithm only.

One subtle concern with EPROM OBP that designers often overlook is U.V. board erasure.

→ U.V. EPROM board erasure requires removal of the board from its host system. This incurs the hidden costs of labor, lower yields due to handling, and the reliability risks of dismantling a system. Flash memory decreases these costs by enabling a greater degree of factory automation, and increases the flexibility afforded by OBP.



NOTE:
During normal system read operation, all interface traces are left open-circuited. Some of the lines have pull-downs or weak pull-ups to insure proper device operation.

Figure 2. System to Board-Programmer Interface

6

EPROM OBP (cont'd)

→ Special U.V. board erasers must be purchased, at significant costs and with limited throughput. A low-end U.V. bulb costs $75-$100 each. A U.V. board eraser system could cost upwards of $10,000, with recurring costs of light bulbs and energy. Thus, the cost of U.V. erasure is often under-estimated.

→ Although portable board programmers are commercially available, U.V. lights by nature are not very rugged, and are not suited for out-of-factory code updates. This complicates field service.

→ Erasure can be easily controlled in a lab environment; however, it is not as clear on the manufacturing floor which label to remove for U.V. erasure, because parts other than EPROMs have windows (i.e. EPLD's, micro-controllers with embedded EPROM memory, etc.)

The System/Board-Programmer Hardware Connection

In most U.V. EPROM OBP applications, designers use the board's edge-connector as the programmer interface. This approach is the lowest cost solution for standard EPROM technology because U.V. erasable devices require system disassembly for erasure anyway. With flash memory, you can eliminate the system dismantling and capitalize on the erase feature by adding a cable connector to the board for reprogramming purposes. The connector should extend from the board through the system's chassis, and should be easy to reach by a serviceman.

Various types of cables exist on the market that could be used to connect programming equipment to the system. The key design consideration when choosing the type of cable is elimination of all transient noise that would interfere with the programming or erasure process.

Three types of noise interference and methods to diminish the noise are as follows:

1. line to line cross-talk (due to board-programmer's drivers that drive sharp step functions on adjacent address lines); solved with either ribbon cables, having alternate lines grounded, or with braided twisted-pairs that have a ground line for each active signal;
2. programmer line-driver-to-board impedance mismatches leading to transmission line effects of signal reflection, and interference; solved by limiting cable length, decreasing programmer switching speed (or allowing longer settling time between address switches) or by using matched line drivers on the programmer and high impedance buffers on the board end, or by using series termination resistors on the driving end of the cable (i.e.—board-programmer end, with the exception of the bi-directional data bus which needs series resistors at both ends);
3. rf pick-up in electrically noisy environments; use either shielded cable such as coax, ribbon cable with solid copper ground plane, or a new type that has recently become available called Flex cable.

Braided twisted-pair cables when kept under three feet in length generally reduce cross-talk to acceptable levels. This type of cable offers the most cost-effective solution which works well in most applications. Depending on the environment, the programmer and your design, you may need a combination of solutions, such as braided twisted-pairs with series termination.

At first all of these alternatives may seem expensive or superfluous, but keep in mind that the cost of a single cable and programmer gets amortized over the total number of systems programmed.

AN 8-BIT BUS DESIGN EXAMPLE

An example of an in-circuit reprogrammable controller board is an 80C31, two 28F256's and some glue chips. (See Figure 3. for a system block diagram. See Appendix A. for a detailed system schematic.)[3] The important issues for erasure and reprogramming are as follows:

1. the board-programmer must have uncontested access and control of the flash memory array; and
2. the microcontroller must be reset (un-active) during the erasure and programming cycles.

SYSTEM DESIGN

Bus Control Circuitry

The 80C31 has an active-high reset pin, which tristates the address and data bases. Route this line (RESET) to the programming connector. Tie the $\overline{OE}$ pins on the low-order address latch (74HCT573), and the $\overline{PSEN}$ buffer-enable (74HCT125)[4] together, and route that line MEMWR[5] to another pin on the programmer-interface connector.

During normal system operations when the μC reads program code from the 28F256 devices, the pull-down on MEMWR keeps the address latches and $\overline{PSEN}$ buffer active. During flash memory OBP, the board-programmer drives MEMWR active-high, which disables these outputs, and isolates the address bus and $\overline{PSEN}$ from the programming signals.

The board-programmer must independently control the RESET and MEMWR traces because they disable at different V_{IL} values (2.5V for RESET vs 0.8V for MEMWR). If controlled by the same 5V supply, on power-up or after a reset condition the μC would try to execute code while still isolated from its code source—specifically before the address latches and $\overline{PSEN}$ buffer activate.

Address Decode Circuitry

This design shows two 28F256 flash memories. Systems with more than one memory device typically decode the CPU's high-order address to select a particular device.

3. Note that the flow-through latch on the data bus is not needed with the 80C31, but is drawn as an example for CPU's that can not tristate their data bus.
4. The isolation buffer is required on $\overline{PSEN}$ in this design because the 80C31 goes into unspecified states when the Reset and $\overline{PSEN}$ lines are active simultaneously. To avoid any possible problems, buffer $\overline{PSEN}$.
5. MEMWR = > bus isolation control of $\overline{PSEN}$ and the data bus.

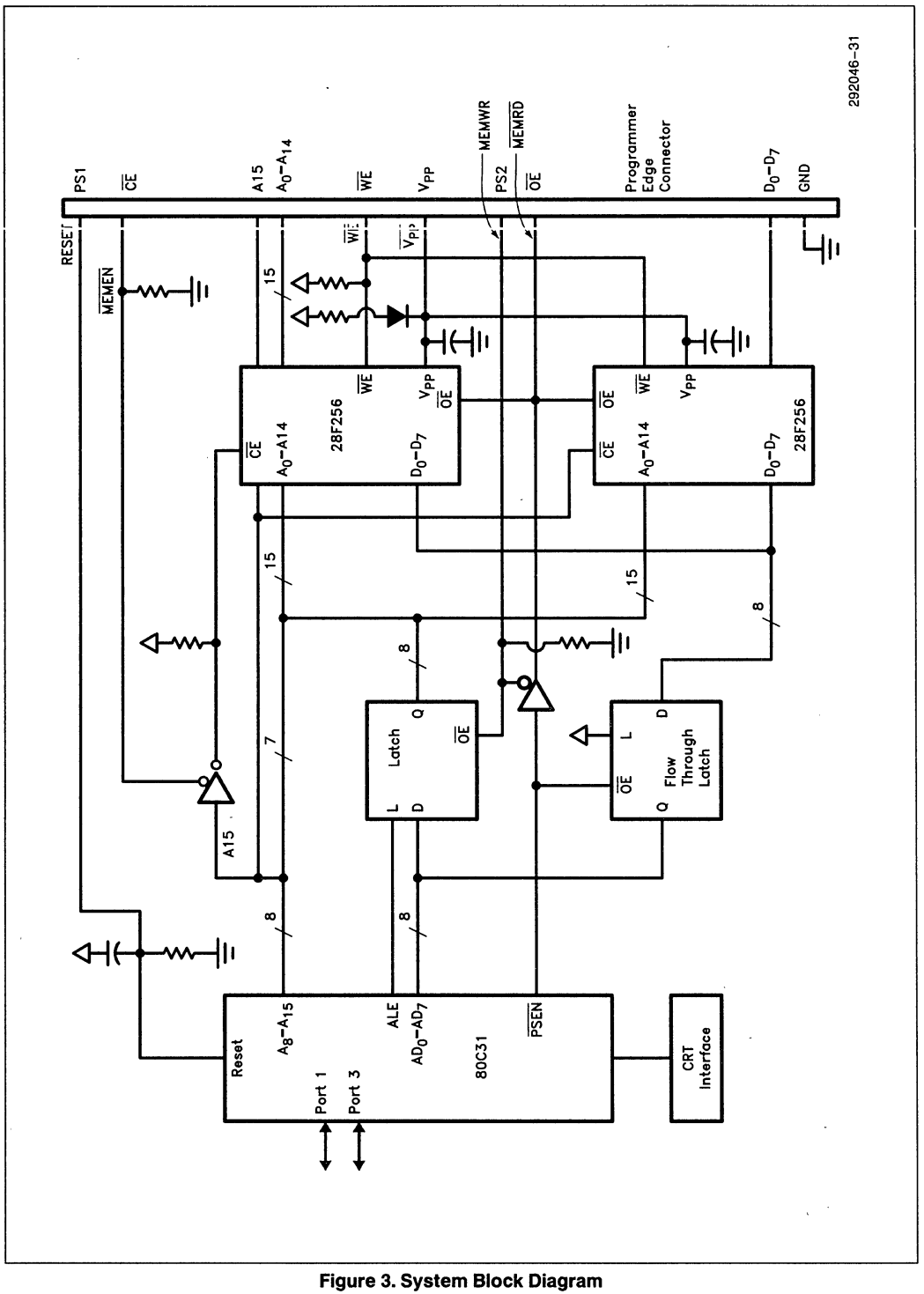


Figure 3. System Block Diagram

This is accomplished as illustrated. When A15 is low, the lower 32K bytes are selected. The output of the inverter drives the other 28F256's chip enable. This type of memory architecture promotes power savings by disabling all memories but the one being addressed.

To accomplish this two-line memory control architecture, route the inverter's input A15 to the 80C31 and to the programmer interface connector.[8] The board-programmer controls the inverter's output enable with $\overline{\text{MEMEN}}$.[9] The $\overline{\text{MEMEN}}$ line performs the function normally performed by $\overline{\text{CE}}$ in component programming. When driven to a logic "1" level $\overline{\text{MEMEN}}$ pulls the inverter's output high. This deselects all memory devices controlled by that I.C. During normal read and standby operations, the pull-down on $\overline{\text{MEMEN}}$ keeps the decoder enabled.

Erasure and Programming Control Circuitry

In this design, V_{PP} and $\overline{\text{WE}}$ are active only during reprogramming. At other times, the two inputs would be inactive. Simply tie the $\overline{\text{WE}}$ line to V_{CC} through a pull-up resistor. The pull-up limits the current to the board programmer during reprogramming. (Recall that $\overline{\text{WE}}$ is active low.) Flash memories allow V_{PP} to be at 12V, V_{CC} or ground for read operations. This design ties V_{PP} to V_{CC} through a diode and resistor to allow for EPROM OBP compatibility. If this option is not required, simply tie V_{PP} to ground through a current-limiting pull-down resistor.

Returning Control to the Host System

The board-programmer should return system-control to the host processor in an organized manner. First it should lower V_{PP} from 12V to 5V, or ground. Then the board programmer should place its address and data buses into a high impedance state. Next PS2, which controls MEMWR should be tristated thus disabling the $\overline{\text{PSEN}}$/Address latch isolation. Finally the board-programmer should switch PS1, which drives the RESET line to reactivate the μC. This sequence guarantees that the μC will begin operation at a known program code location.

16-BIT BUS DESIGN CONSIDERATIONS

An example of an On-Board programmable 16-bit system board would be an 80C186 microprocessor, two 28F010 flash memories, RAM, and some glue chips. The basic hardware design considerations would be the same as those in the previously discussed 8-bit bus example.

There are a few issues with 16-bit designs that do not arise in 8-bit designs. For the programmer to take control of the system, it must tristate and reset the μP as well as tristate the bus buffers and latches. The HOLD and RESET lines of Intel's 86-based family of microprocessors have been designed with bus isolation in mind for use in multiprocessor systems.

The designer has two options for erasing and programming the high and low bytes of the flash memory array independently.

1) The designer can route two $\overline{\text{WE}}$ lines to the programmer connector—BYTE HIGH $\overline{\text{WE}}$ and BYTE LOW $\overline{\text{WE}}$.

2) The reprogramming software can follow the masking procedure shown in section 4.4. This method allows a common $\overline{\text{WE}}$ line for the high and low bytes.

8. Note the lack of isolation buffers between the 80C31's high order addresses (Port 2) and the board-programmer interface, compared to the latch separating the low order addresses (Port 0) and the interface. In this design example, we make use of the 80C31's ability to tristate these ports, so no isolation is needed for any of the addresses. The latch on Port 0 is for the time-multiplexed address/data architecture of this microcontroller, and not specifically for isolation.
9. MEMEN = memory enable, active low.

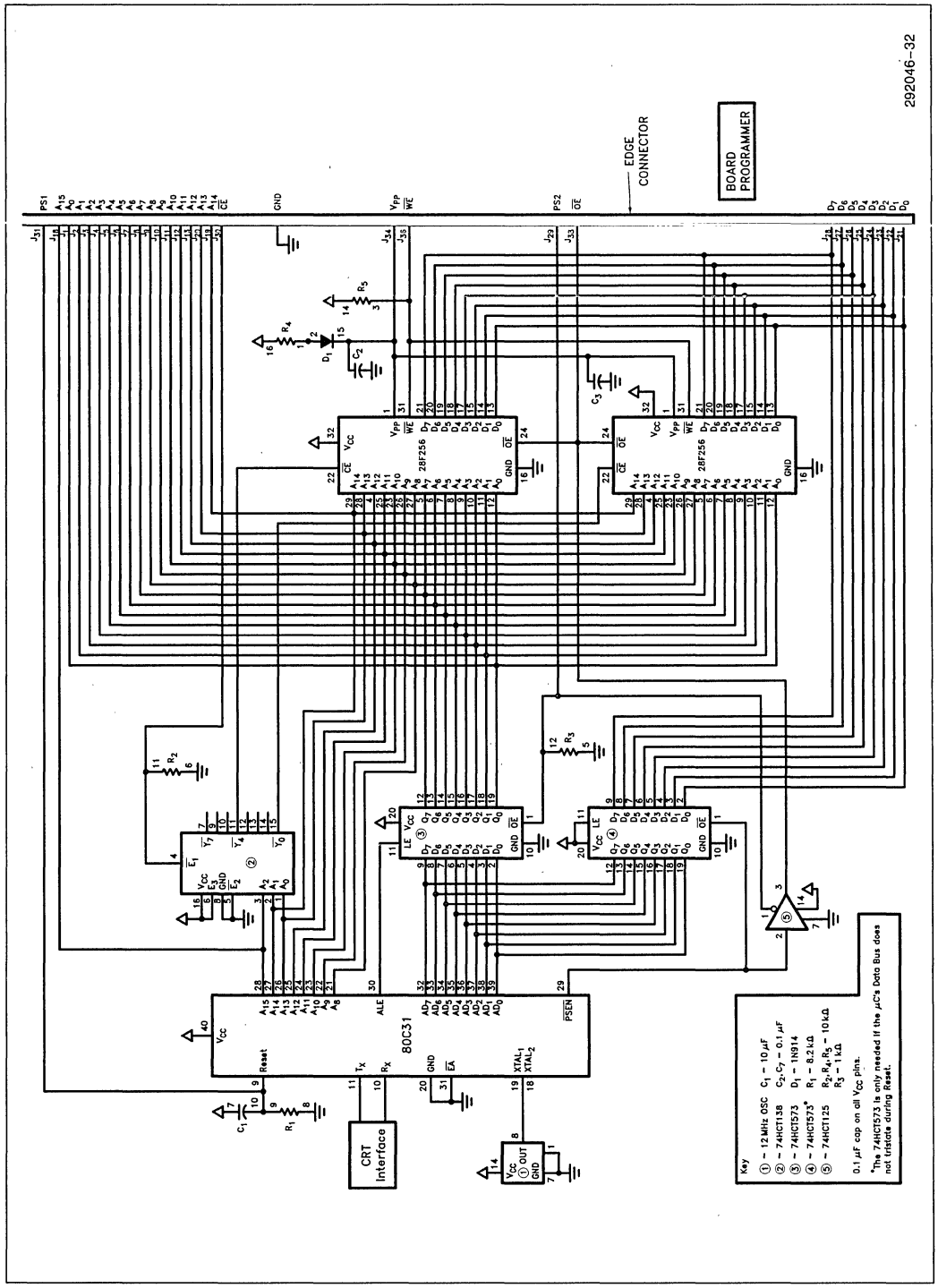


Figure 4. Detailed 8-Bit Bus Design Schematic

OBP EQUIPMENT AND VENDORS

If you are considering OBP for your next design, and have not used on-board programming before, you will need to choose a board-programmer vendor. Various suppliers offer OBP systems; therefore, it is well worth it to send out requests for programming support bids. If your production volume justifies the purchase of more than one board-programmer, you may want to negotiate a non-recurring engineering charge for development cost, followed by variable costs for additional units.

Most vendors offer a variety of basic systems, designed to easily adapt to your needs. Systems can be purchased that program either single boards serially, or a number of boards in parallel. Light-weight OBP equipment designed for field reprogramming can also be obtained from some of the vendors.

Most companies will work directly with you at the beginning of your design phase to ensure OBP compatibility. If your design is beyond the definition stage, the programmer manufacturer will request a copy of your schematics or block diagrams under non-disclosure. The vendor has an OBP design specialist that will check the design for OBP compatibility. Any potential problems will be located and corrected at this early stage.

Every board's architecture is different (i.e., based on different central processing units (CPU), decoding schemes, buffering methodologies, interface connectors, and types and densities of memories). Vendors write custom software modules for each application. Also, the vendor or the board designer typically builds an interface jig to connect the board's edge connector to the programmer. This choice is often left as a decision for the designer.

Partial List* of Companies Selling Board-Programmers

Following are a few of the companies who offer on-board programming solutions today:

Data I/O Corp.
Digelec
Elan Digital Systems
Oliver Advanced Engineering, Inc.
Stag Microsystems, Inc.

*This list is intended for example only, and in no way represents all companies that support on-board programming. Intel Corporation assumes no responsibility for circuity other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

SUMMARY

- On-board programming (OBP) has been around since 1981.
- Designing a board for OBP can be easily done by working with a board-programmer vendor's OBP-design-specialist during the initial design phase.
- In-circuit alterable code storage can be easily implemented by using flash memory and it's features.
- Time and money savings can be realized in a number of ways by taking advantage of flash memory OBP:

<> Decreased board costs and improved reliability from elimination of EPROM sockets;

<> Decreased manufacturing costs from elimination of board eraser depreciation costs, recurring U.V. light bulb and energy expenses;

<> Decreased inventory expense from simplified test and rework methods (one-step diagnostics, erasure, and board configuration);

<> Decreased product costs based on decreased board-handling loss;

<> Improved board diagnostics and testability leading to higher quality and decreased customer returns; and

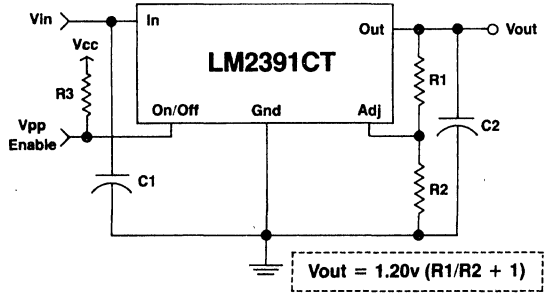
<> **Quicker, more reliable field code updates.**

APPENDIX B
V_{PP} GENERATION CIRCUITS

Circuit #1—Regulation from a higher voltage
Circuit #2—Regulation from a higher voltage
Circuit #3—Regulation from a higher voltage
Circuit #4—5V to 12V Boost
Circuit #5—5V to 12V Boost
Circuit #6—Monolithic DC/DC Convertor

Circuit # 1

Down Conversion
(From 14.0V–26.0V to 12.00V)



292046-12

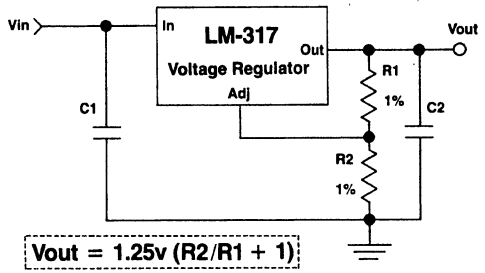
COMPONENTS	COST*
LM2391CT	$0.75
R1 = 20 KΩ, 1%	0.045
R2 = 180 KΩ, 1%	0.045
R3 = 10 KΩ	0.02
C1 = 0.1 μF	0.02
C2 = 100 μF	0.15
	$1.03

NOTES:
—The LM2391 offers an enable pin for added data protection.
—The drop out voltage is 0.6V.
—R3 is NOT required if V_{PP} enable is driven by a CMOS device.
*Cost approximations assume 10,000 piece quantity.

6

Circuit #2

Down Conversion
(From 16.00V–26.00V to 12.00V)



Vout = 1.25v (R2/R1 + 1)

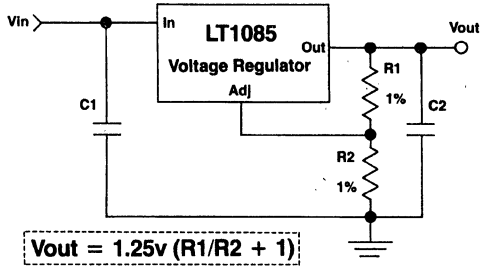
292046-13

COMPONENTS	COST*
LM-317	0.40
R1 = 124Ω, 1%	0.045
R2 = 1070Ω, 1%	0.045
C1 = 0.1 μF	0.02
C2 = 100 μF	0.15
	$0.66

NOTES:
LM-317 requires a minimum $V_{IN}-V_{OUT}$ = 3.0V
*Cost approximations assume 10,000 piece quantity.

Circuit #3

Down Conversion
(From 15.0V–40.0V to 12.00V)



Vout = 1.25v (R1/R2 + 1)

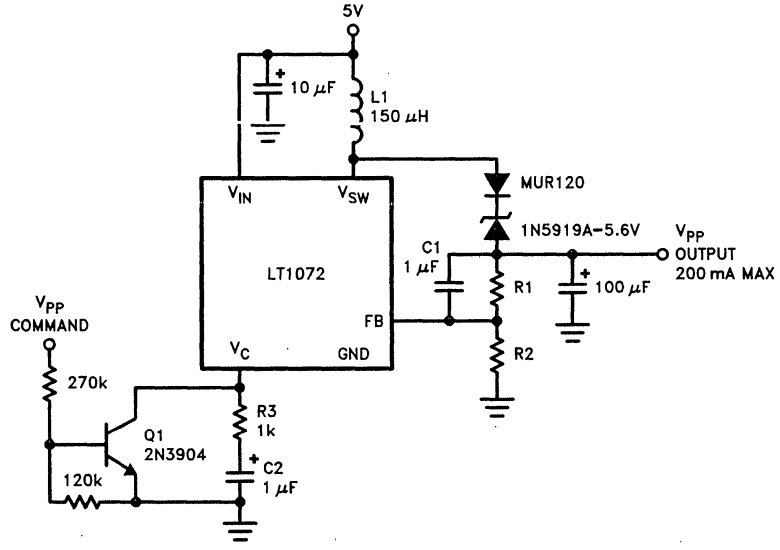
292046-14

COMPONENTS	COST*
LT-1085	2.50
R1 = 124Ω, 1%	0.045
R2 = 1070Ω, 1%	0.045
C1 = 10 μF	0.10
C2 = 10 μF	0.10
	$2.79

NOTES:
LT-1085 requires a minimum $V_{IN}-V_{OUT}$ = 1.5V
*Cost approximations assume 10,000 piece quantity.

Circuit #4

Up Conversion
(From 5V to 12.0V)



292046-33

COMPONENTS	COST*
LT1072	1.82
R1 = 10.7k, 1%	0.045
R2 = 1.24k, 1%	0.045
R3 = 1k, 5%	0.02
R4 = 120k, 5%	0.02
R5 = 270k, 5%	0.02
C1 = 1 μF	0.10
C2 = 1 μF	0.10
C3 = 10 μF	0.15
L1 = 150 μH	1.00
Q1 = 2N3904	0.10
	$3.42

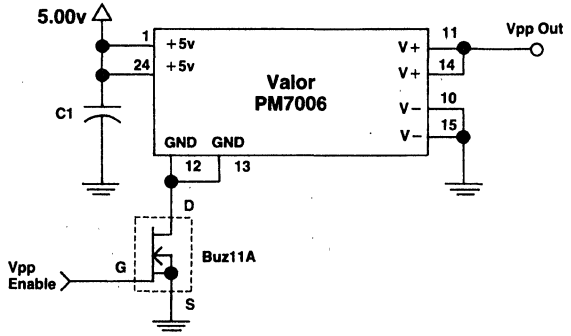
V_{PP}OUT	R1	R2	Resistor Tolerance
12.0V	10.7k	1.24k	1%

NOTES:
Drive V_{PP} COMMAND low to turn on the circuit.
*Cost approximations assume 10,000 piece quantity.

6

Circuit #5

Up Conversion Circuit
(From 5.0V to 12.0V)



292046-16

COMPONENTS	COST*
PM7006	$6.25
C1 = 0.1 μF	0.05
Buz11A	2.59
	$8.89

NOTES:
1. The capacitor decreases output noise to 140 mV pk-pk.
2. We added the Buz11A Mospower nFET to enable/disable the converter. This control minimizes power consumption which under full load can reach 600 mA.
3. The voltage drop across the switch is 0.1V. Due to this drop the PM7006 will not maintain the V_{PP} spec with 10% fluctuations in V_{CC} supply.

*Cost approximations assume 10,000 piece quantity.

APPENDIX C
LIST OF DC-DC CONVERTER COMPANIES

BURR-BROWN
P.O. Box 11400
Tucson, AZ 85734
(602) 746-1111

CARITRONICS INC.
P.O. Box 821
West Caldwell, NJ 07007
(201) 575-8916

LINEAR TECHNOLOGY CORP.
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
(408) 432-1900

NOVA-TRONIX
4701 Patrick Henry Dr. #24
Santa Clara, CA 95054
(408) 727-9530

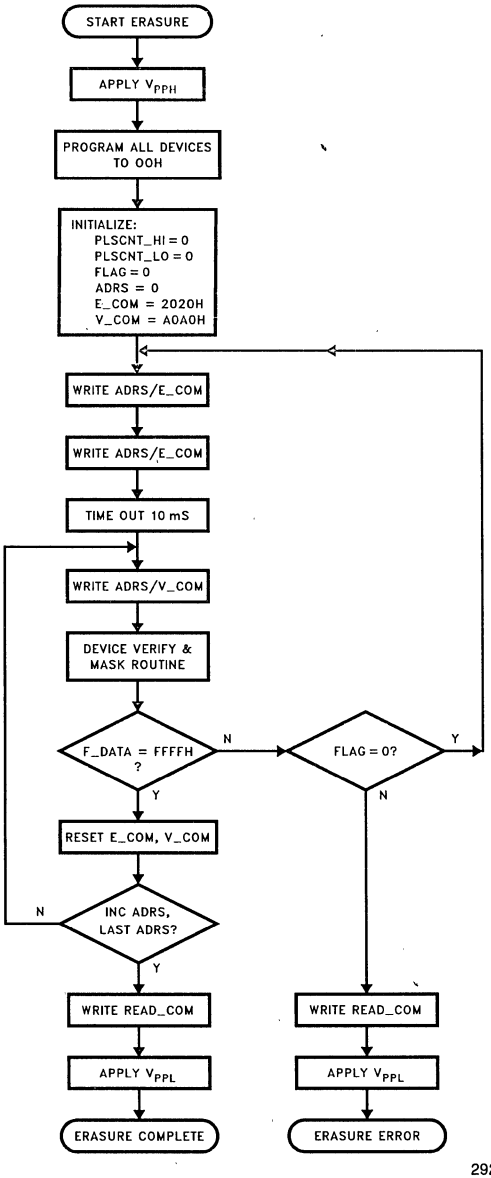
RELIABILITY INC.
(713) 492-0550

SEMICONDUCTOR CIRCUITS INC.
49 Range Road
Windham, New Hampshire 03087
(603) 893-2330

UNIVERSAL MICROELECTRONICS
Marcon Sales Inc.
2672 Bayshore Parkway, Suite 1000
Mountain View, CA 94043
(415) 964-8046

VALOR ELECTRONICS
6275 Nancy Ridge Dr.
San Diego, CA 92121
(619) 458-1471

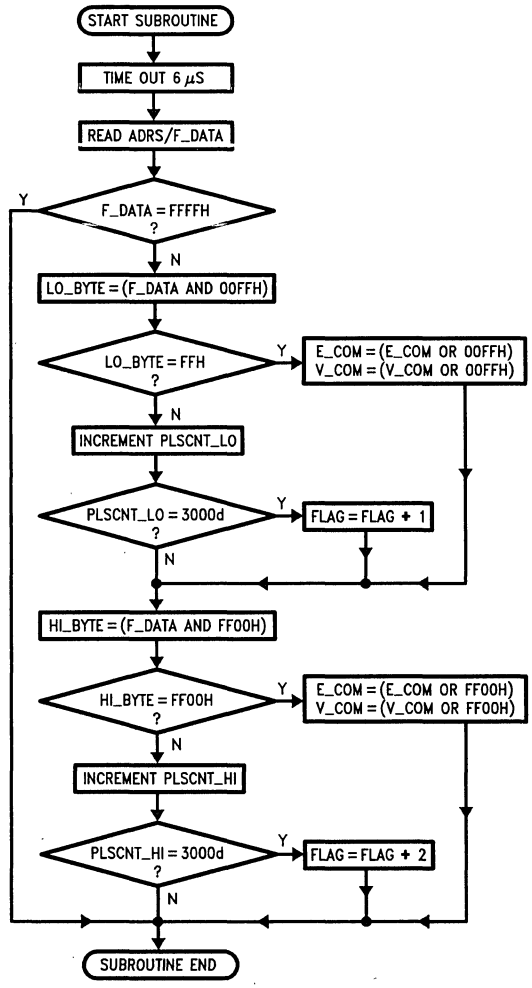
APPENDIX D
PARALLEL ERASE FLOW CHART



292046-34

COMMENTS
Wait for V_{PP} to stabilize.
Use Quick-Pulse Programming algorithm. Initialize Variables: PLSCNT_HI = HI Byte Pulse Counter PLSCNT_LO = Low Byte Pulse Counter FLAG = Erasure Error Flag ADRS = Address E_COM = Erase Command V_COM = Verify Command
Erase Set-up Command
Start Erasing
Duration of Erase Operation.
Erase Verify Command stops erasure.
See next page for subroutine.
When both devices at ADRS are erased, F_DATA = FFFFH. If not equal, increment the pulse counter and check for last pulse.
Reset commands to default (E_COM = 2020H, V_COM = A0A0H) before verifying next ADRS.
Reset devices for read operation.
Turn off V_{PP}.

Device Erase Verify and Mask Subroutine



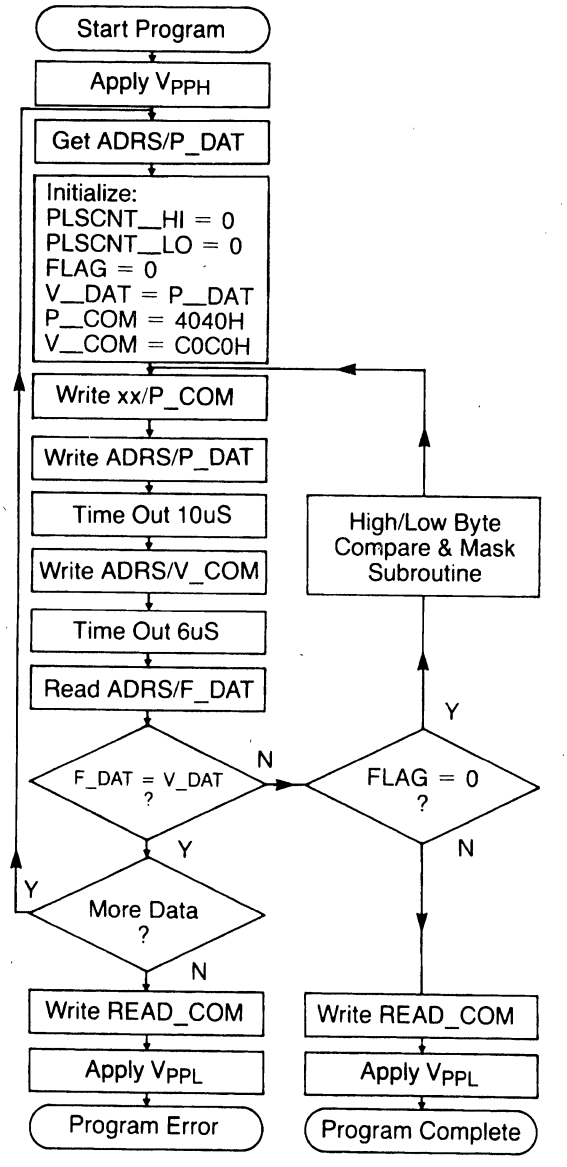
292046-35

COMMENTS
This subroutine reads the data word (F__DATA). It then masks the HI or LO Byte of the Erase and Verify commands from executing during the next operation.
If both HI and LO bytes verify, then return.
Mask* the HI Byte with 00H.
If the LO Byte verifies erasure, then mask* the next erase and verify commands with FFH (Reset).
If the LO Byte does not verify, increment its pulse counter and check for max count. FLAG = 1 denotes a LO Byte error.
Repeat sequence for the HI Byte
FLAG = 2 denotes a HI Byte error. FLAG = 3 denotes both HI and LO Byte errors.

NOTE:
*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming flash data (F__DATA), the erase commands and the verify commands. Then manipulate the HI or LO register contents.

6

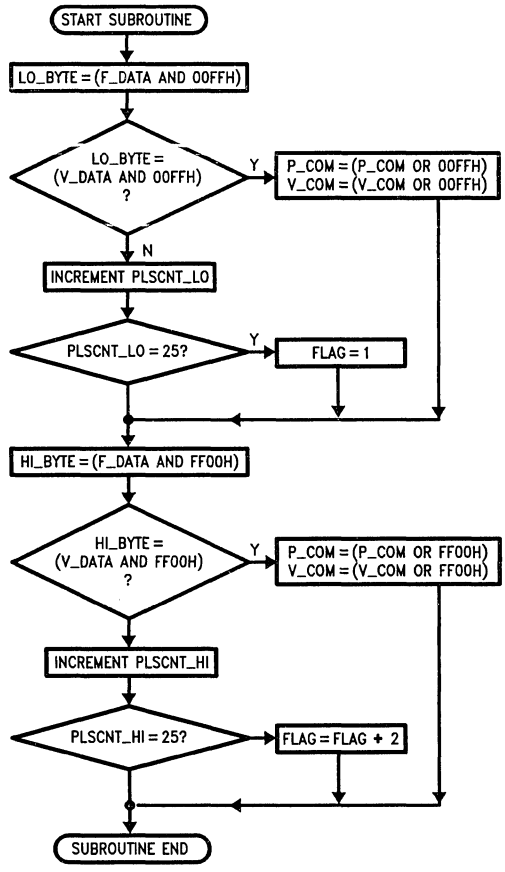
APPENDIX E
PARALLEL PROGRAMMING FLOW CHART



COMMENTS
Wait for V_{PP} ramp to V_{PPH}
ADRS = address to program P_DAT = data word to program
Initialize Data Word Variables: PLSCNT_HI = HI Byte Pulse Counter PLSCNT_LO = LO Byte Pulse Counter FLAG = Program Error Flag V_DAT = valid data P_COM = Program Command V_COM = Verify Command
Program Set-up Command xx = Address don't care
Program
See next page for subroutine
Program Verify Command
F_DAT = flash memory data
Compare flash memory data to valid data (word compare). If not equal, check for program error flag. If flag not set, compare High and Low Byte in subroutine.
Check buffer or I/O port for more data to program.
Reset device for read operation.
Turn off V_{PP}.

292046-19

Program Verify and Mask Subroutine



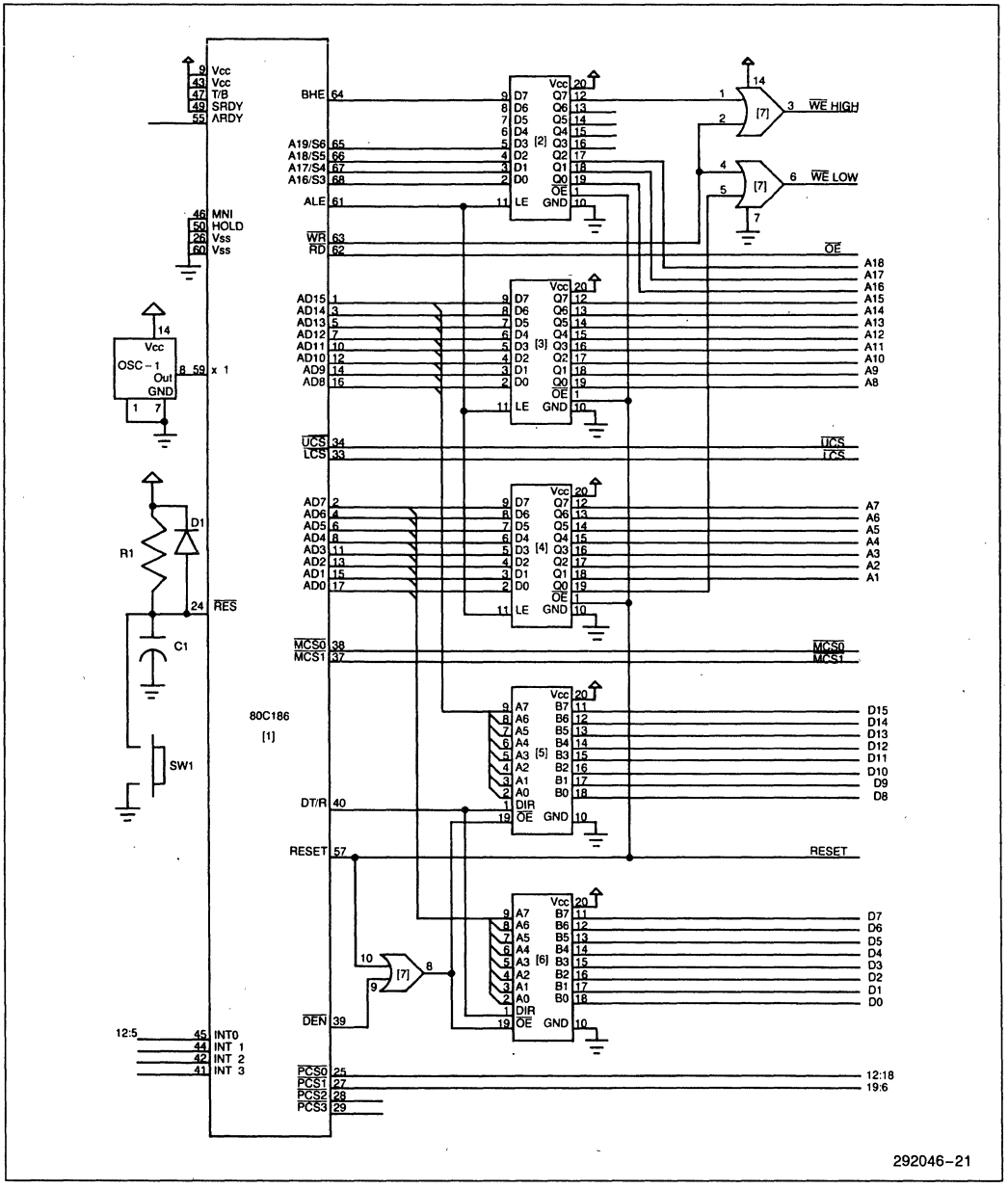
292046-40

COMMENTS
To look at the LO Byte, mask* the HI Byte with 00.
If the LO Byte Verifies, mask the LO Byte commands with the reset command (FFH).
If the LO Byte does not verify, then increment its pulse counter and check for max count. FLAG = 1 denotes a LO byte error.
Repeat the sequence for the HI Byte.
FLAG = 2 denotes a HI Byte error. FLAG = 3 denotes both HI and LO Byte errors. FLAG = 0 denotes no max count errors; continue with algorithm.

NOTE:
*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F-DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

6

APPENDIX F
DETAILED SYSTEM SCHEMATICS



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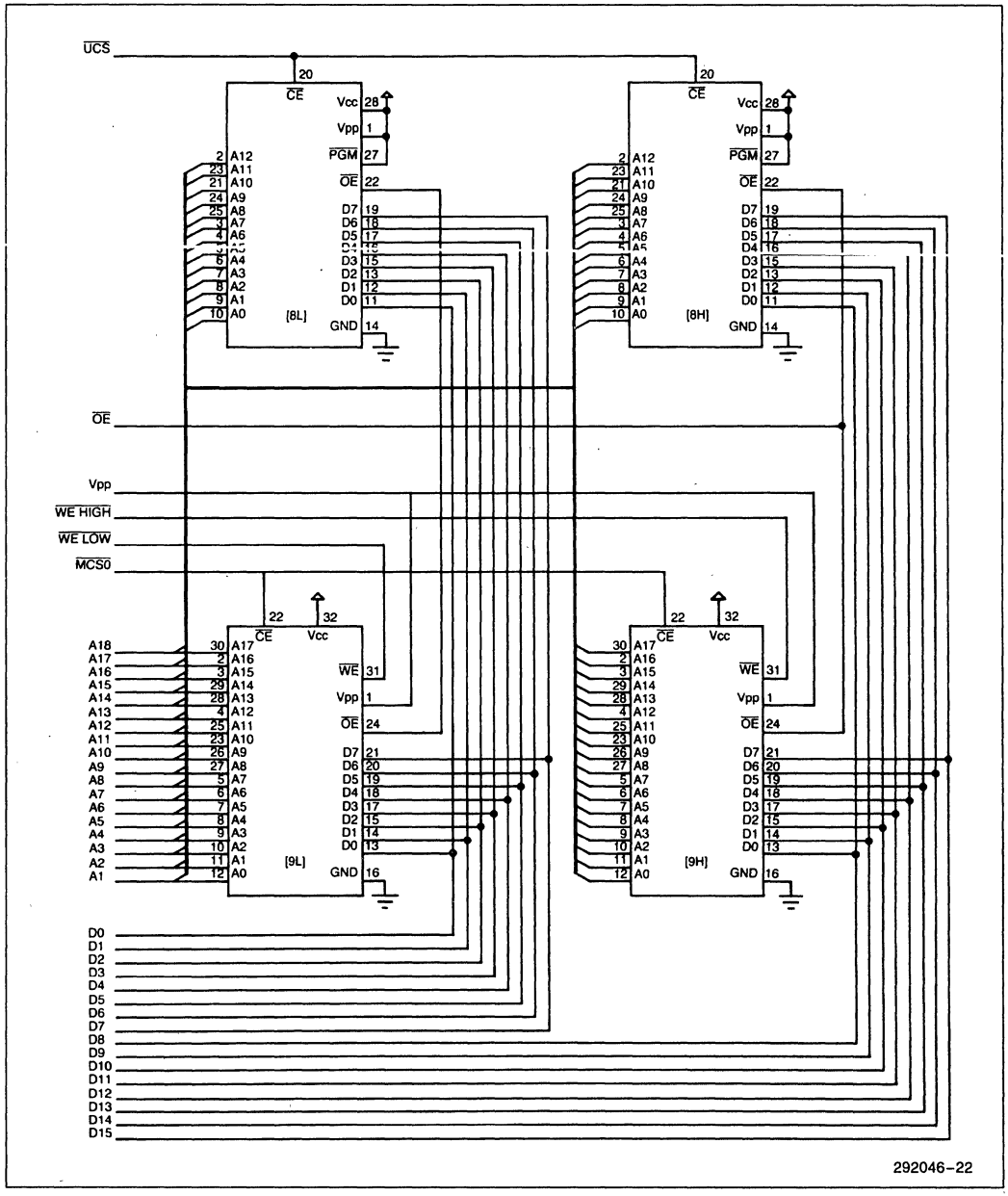
UCS
OE
Vpp
WE HIGH
WE LOW
MCS0
[8L]
[8H]
[9L]
[9H]
CE
Vcc
Vpp
PGM
OE
WE
GND
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
D0
D1
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D11
D12
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D14
D15
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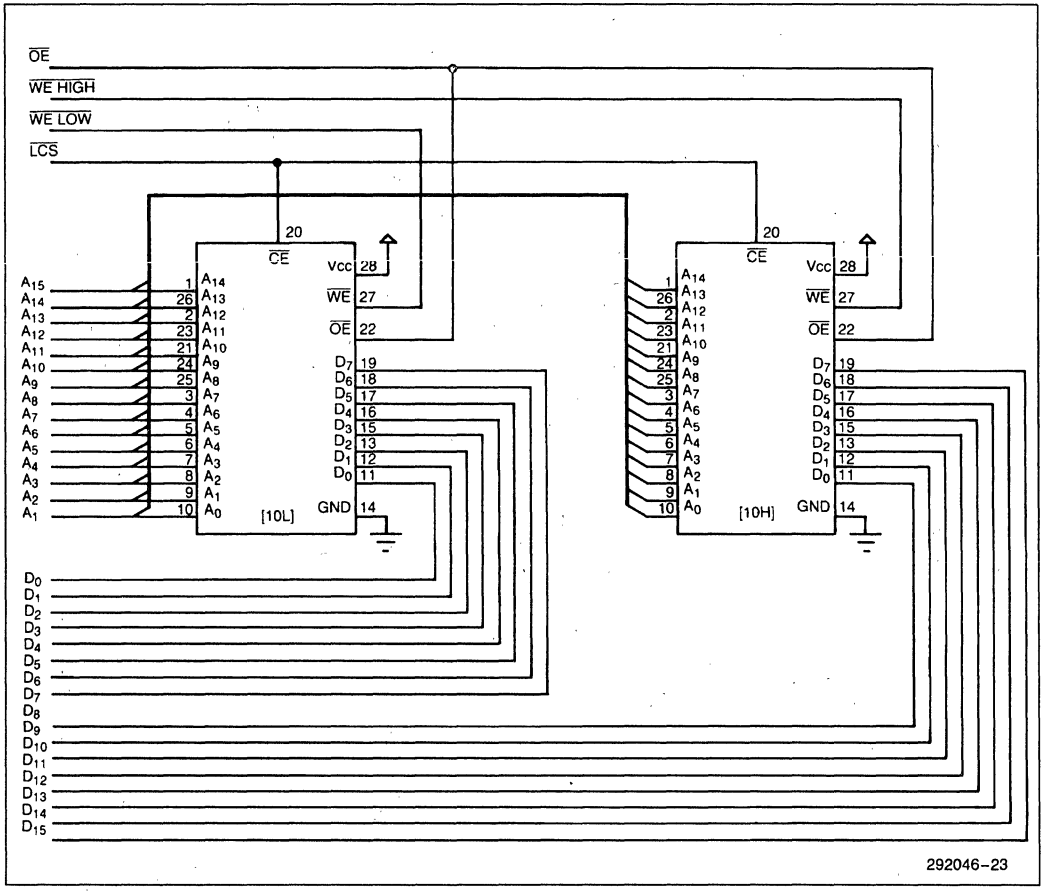
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WE LOW
LCS
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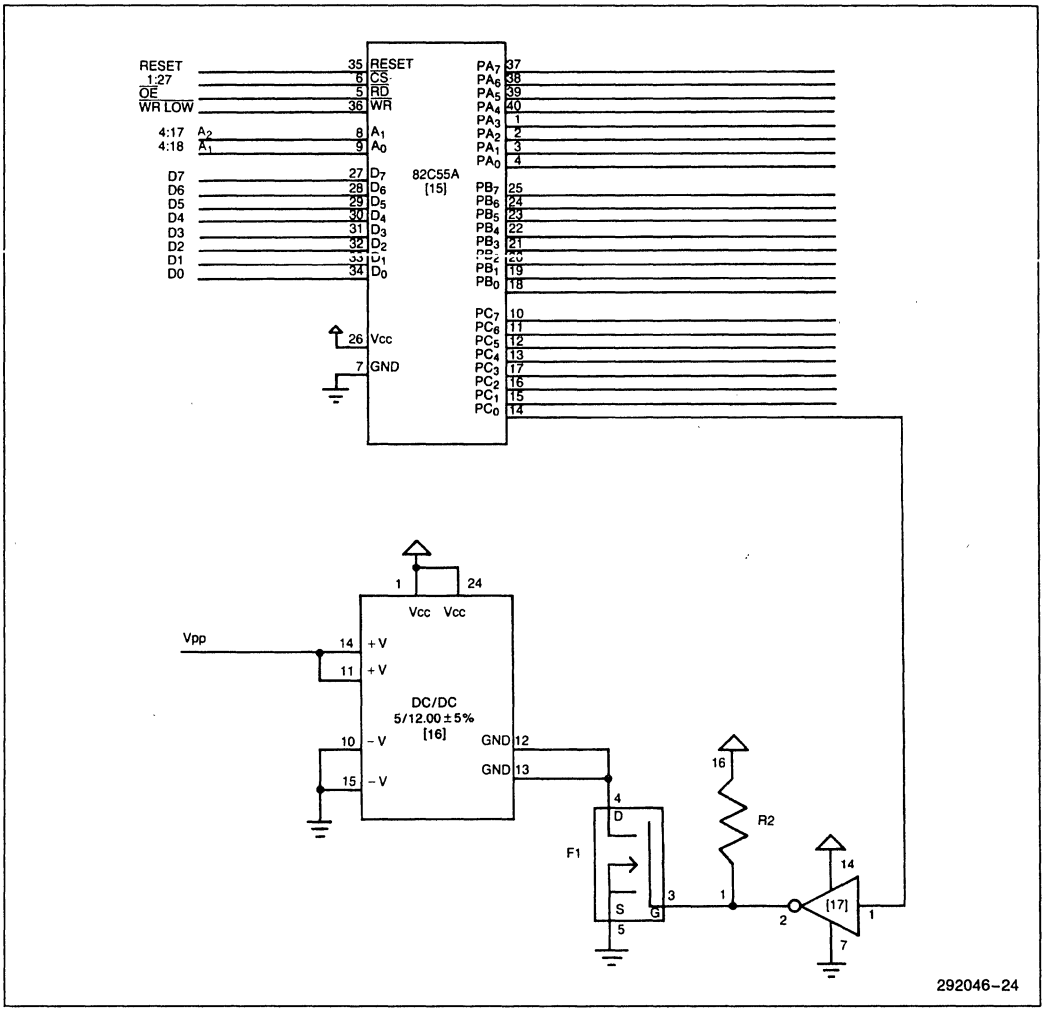
Vcc 28
WE 27
OE 22
[10L]
GND 14
[10H]
292046-23


RESET
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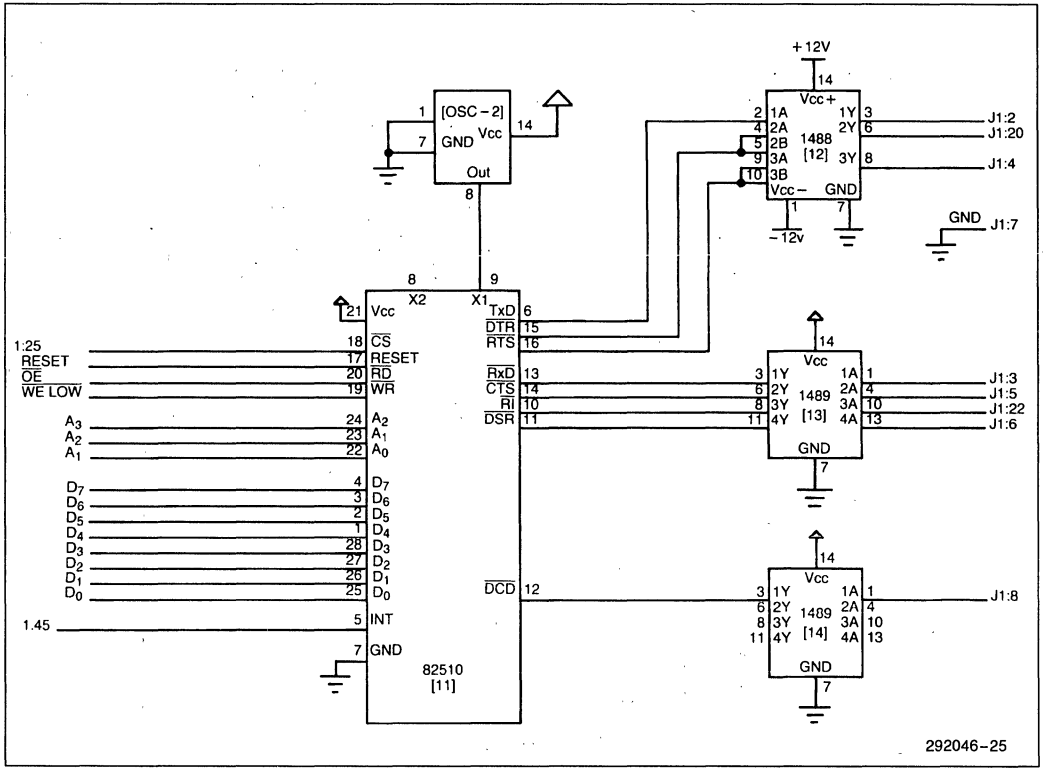
OE
WR LOW
4:17 A2
4:18 A1
D7
D6
D5
D4
D3
D2
D1
D0
35 RESET
6 CS
5 RD
36 WR
8 A1
9 A0
27 D7
28 D6
29 D5
30 D4
31 D3
32 D2
33 D1
34 D0
82C55A
[15]
26 Vcc
7 GND
PA7 37
PA6 38
PA5 39
PA4 40
PA3 1
PA2 2
PA1 3
PA0 4
PB7 25
PB6 24
PB5 23
PB4 22
PB3 21
PB2 20
PB1 19
PB0 18
PC7 10
PC6 11
PC5 12
PC4 13
PC3 17
PC2 16
PC1 15
PC0 14
1 Vcc
24 Vcc
Vpp
14 +V
11 +V
DC/DC
5/12.00±5%
[16]
10 -V
15 -V
GND 12
GND 13
16
R2
4
D
F1
S
G
3
1
5
2
[17]
14
7
1

292046-24

6


+12V
[OSC-2]
GND
Vcc
Out
82510
[11]
X2
X1
Vcc
GND
1488
[12]
1489
[13]
1489
[14]
Vcc+
Vcc−
−12v
1:25
RESET
OE
WE LOW
1.45
INT
TxD
DTR
RTS
RxD
CTS
RI
DSR
DCD
J1:2
J1:20
J1:4
J1:7
J1:3
J1:5
J1:22
J1:6
J1:8
292046-25

256K FLASH MEMORY DEMO PARTS LIST

Device	Component	Pins	Description
[1]	80C186	68	16-bit high integration CPU
[2,3,4]	74HC573	20	Latch
[5,6]	74HC245	20	Transceiver
[7]	74HC32	14	OR gate
[8L,8H]	27C64	28	16 Kbyte EPROM
[9L,9H]	28F256	32	64 Kbyte flash memory
[10L,10H]	32K x 8 SRAM	28	64 Kbyte SRAM
[11]	82510	28	Asynchronous Serial Controller
[12]	14C88	14	RS-232 Line Driver
[13,14]	14C89	14	RS-232 Line Receiver
[15]	82C55A	40	Programmable Peripheral Controller
[16]	PM7006	24	DC/DC Convertor (5V–12.00V)
[17]	7406	14	Invertor—Open Collector (O.C.)
C1	20 μF	2	Capacitor for CPU reset
D1	1N914	2	Diode for CPU reset
F1	BUZ11A	3	MOSPOWER nFET
J1	DB-25	25	Connector (male)
OSC-1	20 MHz	14	CPU Oscillator
OSC-2	18.432 MHz	14	Serial Controller Oscillator
R1	10 KΩ	2	¼W, 10% Resistor for CPU reset
R2	1 KΩ	2	¼W, 10% Resistor for O.C. pull-up
SW1		3	Momentary Push Button for CPU reset

NOTES:
1. Place a 0.1 μF bypass capacitor at the V_{CC} input of each IC.
2. Place a 0.1 μF bypass capacitor on the V_{PP} input of each 28F256 flash memory.

28F512 UPGRADE FOR THE 80C186/FLASH MEMORY DESIGN

To upgrade the 80C186/Flash memory design to handle 28F512's, the range of the $\overline{CE}$ signal has to be increased. There are a number of ways to generate a $\overline{CE}$ signal that will span the 128 Kbyte address range of two 28F512 devices.

1. AND two of the current MCS lines together (defined for 64 Kbytes each); or
2. Change the MCS individual block-select size from 64 Kbytes:
   MMCS_VALUE = 41F8H,
   MPCS_VALUE = 0A0B8H

   to 128 Kbytes:
   MMCS_VALUE = 01FEH,
   MPCS_VALUE = 0C0BEH

   Also, cut the $\overline{CE}$ trace to the RAM sockets. Then wire $\overline{MCS0}$ to the RAM $\overline{CE}$. This eliminates the $\overline{MCS0}$ and $\overline{LMCS}$ range overlap caused by increasing the MCS range to 128 Kbytes. See 80C186 Data Sheet page 21 and 22 (Order # 270354).

6

28F010 UPGRADE TO THE 80C186/FLASH MEMORY DESIGN

To upgrade the 80C186/Flash memory design to handle 28F010's, a $\overline{CE}$ signal has to be generated. There are a number of ways to generate a $\overline{CE}$ signal that will span the 256 Kbyte address range of two 28F010 devices.

1. **AND two of the MCS lines together** (defined for 128 Kbytes each as noted in the 28F512 modifications):

   Cut the LMCS trace to the RAM sockets. Connect $\overline{MCS0}$ to $\overline{CE}$ on the RAM sockets (U10L,UH).

   Cut the $\overline{MCS2}$ trace to the flash memory. Add an AND gate. Connect $\overline{MCS2}$ (cut trace) and $\overline{MCS3}$ to the inputs of the AND gate. Then wire the AND gate output to the $\overline{CE}$ of the flash memories.

   Also, change the onboard memory MCS register to:
   MMCS__VALUE=01FEH, MPCS__ VALUE=0C0BEH [128K blocks],

   and delete:
   LMCS__REG and LMCS__Value.

2. **Add a decoder;**

   Add a decoder (74HC138). Connect address lines A18 and A19 to the B and C inputs of the decoder. Tie the A input of the decoder low, and enable all the enables. By using outputs Y0, Y2, Y4, and Y6, you have four $\overline{CE}$ lines decoding 256 Kbyte blocks each.

   Cut the $\overline{MCS2}$ trace to the flash memories. Connect the Y2 output from the decoder to the $\overline{CE}$ input of the flash memory.

3. **Replace the address latch (U2) with a PLD** that latches and decodes.

   Program a 5C032 as an integrated latch and decoder. Replace the upper address latch [U2] with the Intel 5C032 EPLD. Cut the $\overline{CE}$ trace to the flash memories. Connect the flash memories' $\overline{CE}$ to the 5C032 pin 12. This maps the address space 40000H to 7FFFFH. See Figures 1 and 2 for a comparison of the 74HC573 (U2) and programmed 5C032 pin outs. Figure 3 is the source code for the EPLD.

   Also, change the value of the MMCS and MPCS registers to 64 Kbyte blocks so that the $\overline{MCS0}$ range does not overlap the LMCS range.
   MMCS__VALUE=41F8H, MPCS__ VALUE=0A0B8H.

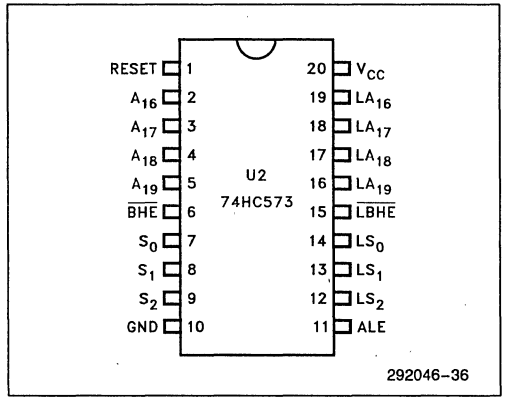


Figure 1. Latch Pinout

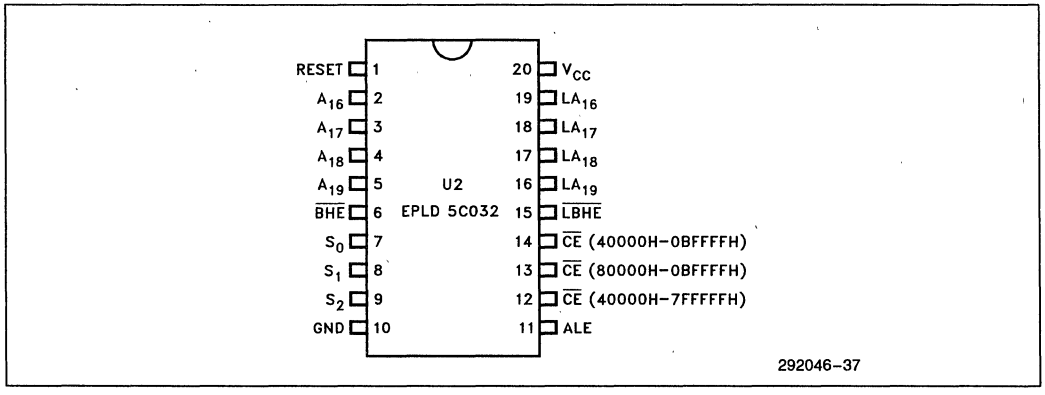


Figure 2. Integrated Latch and Decoder

```
Thom Bowns - PLFG Applications
Intel
January 13, 1989
EPLD HOTLINE: 1-800-323-EPLD
002
5C032
Custom Latched Decoder
OPTIONS: TURBO=ON
PART: 5C032

INPUTS: ALE@11, RESET@1, A19@5, A18@4, A17@3, A16@2, nBHE@6

OUTPUTS:  LA18@17, LA17@18, LA16@19, LnBHE@15, nCE3@14, LA19@16,
          nCE2@13, nCE1@12

NETWORK:
          ALE = IN (ALE)
          RESET = INP (RESET)
          nRESET = NOT (RESET)
          A19 = INP (A19)
          A18 = INP (A18)
          A17 = INP (A17)
          A16 = INP (A16)
          nBHE = INP (nBHE)
          LA19, LA19 = COIF (LA19d, nRESET)
          LA18, LA18 = COIF (LA18d, nRESET)
          LA17, LA17 = COIF (LA17d, nRESET)
          LA16, LA16 = COIF (LA16d, nRESET)
          LnBHE, LnBHE = COIF (LnBHE, nRESET)
          nCE3, nCE3 = COIF (nCE3, nRESET)
          nCE2, nCE2 = COIF (nCE2, nRESET)
          nCE1, nCE1 = COIF (nCE1, nRESET)

EQUATIONS:
          LA19d = A19 * ALE + LA19 * !ALE;
          LA18d = A18 * ALE + LA18 * !ALE;
          LA17d = A17 * ALE + LA17 * !ALE;
          LA16d = A16 * ALE + LA16 * !ALE;
          LnBHEd = nBHE * ALE + LnBHE * !ALE;
          nCE3d = nCE3EQN * ALE + nCE3 * !ALE;
          nCE2d = nCE2EQN * ALE + nCE2 * !ALE;
          nCE1d = nCE1EQN * ALE + nCE1 * !ALE;
          nCE2EQN = !(A19 * !A18);
          nCE1EQN = !(!A19 * A18);
          nCE3EQN = !(!A19 * A18 + A19 * !A18);

END$
```

Figure 3. Source Code for the Integrated Latch and Decoder

intel®

APPLICATION NOTE

AP-341

October 1990

Designing an Updatable BIOS Using Flash Memory

DON VERNER
APPLICATION ENGINEER

Order Number: 292077-001

CONTENTS

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Intel, ETOX II are trademarks of Intel Corporation
Patents are still pending on Intel's ETOX memory

1.0 INTRODUCTION

As PC computing platforms increase in complexity, so does the associated BIOS code. Sophisticated hardware and BIOS software increase the potential for revisions. Time-to-market goals require faster completion of designs from conception to production, leaving less time for test and debug of PC platforms and greater potential for hardware/software bugs. Once a computer is out the door, code revisions are far more difficult and costly. Code revisions with EPROM require either a service call or sending EPROMs to the end user, assuming nothing else goes wrong in the process.

Flash memory offers the same nonvolatile storage as EPROM, but additionally offers in-system write capability. Using Intel's flash memory for BIOS storage, code updates are done quickly in the factory during test and debug, while allowing cost-effective field updates to end users via floppy disks.

This application-note describes various methods of implementing a flash BIOS. Design targets are both laptop and desktop systems. The primary emphasis is on application of flash for BIOS and ROM executable software applications. Detailed information on flash memory is covered in other references, including data sheets and other application notes.

2.0 FLASH MEMORY

This section provides a brief overview of Intel's flash memory. It covers the following:

- Flash memory's EPROM roots
- Stop Timers
- Pin-outs and physical layout for different packages
- V_{PP} specifications

Major benefits of flash memory are in-system write, SRAM-like command interface (for programming and erasure), fixed V_{CC} and V_{PP} supplies, V_{CC} and V_{PP} lockout protection, and stop timers for erase and program operations.

2.1 EPROM Roots; Review of Flash Process vs. EPROM & EEPROM

Intel's ETOX™ II (**E**PROM **T**unnel **OX**ide) flash memory is a single-transistor cell providing nonvolatile storage like EPROM, with electrical erase similar EEPROM. Reprogramming flash memory entails electrically erasing all data bits in parallel, then randomly programming data into any byte in the array. The programming operation is achieved via channel hot electron injection (CHE), just like EPROMs. Flash electrical erasure however, is accomplished through Fowler-Nordheim (FN) tunneling. Using separate program and erase methods (CHE vs. FN Tunneling), in different cell locations, drain vs. source, permits process optimization for high cycling endurance — the number of complete erase and re-writes. Traditional low-density EEPROMs tunnel through the same memory cell junction for both programming and erasure. Because EEPROMs erase before programming each byte, these processes must occur very fast. Therefore, voltages used to program or erase EEPROM memory cells are high (e.g. 18-30 volts). The combination of higher voltage with programming and erasing through the same junction contributes to EEPROM's oxide breakdown and reduced cycling capability.

Intel's flash memory erasure (tunneling) voltage is below the critical oxide breakdown voltage. By using block erasure instead of EEPROM's byte erasure, erase times are relaxed, reducing tunneling voltages. Programming Intel's flash memory is non-destructive to the floating gate oxide compared to EEPROM's use of tunneling for programming. These features for erase and programming provide Intel's flash memory with the highest endurance (typically over 100K cycles) compared to that of traditional EEPROM cycling. Furthermore, flash memory exhibits lower failure rates at any given cycle count.

2.2 Stop Timers

Programming and erasing Intel flash memory requires time delays of 10μS and 10mS, respectively. Internal stop timers assist debugging by stopping individual programming or erase timeouts, preventing violations of specified programming or erase timing requirements. For instance, when single-stepping through code, you accidentally leave the device in erase mode while you take your coffee break. The erase timeout requirement would certainly be violated, but since stop timers are present the erase operation is halted internally, providing you with a functional flash device when you return.

2.3 Flash Memory Pinouts and Physical Layout

Intel's flash memory is offered in three standard 32-pin packages: **P**lastic **D**ual **I**n-line **P**ackage (PDIP), **P**lastic **L**eaded **C**hip **C**arrier (PLCC), and **T**hin **S**mall **O**utline **P**ackage (TSOP). 256Kb to 2Mb densities are available in PDIP and PLCC, while 1Mb and 2Mb densities also come in TSOP versions. See figures 1, 2, and 3 for pinout details.

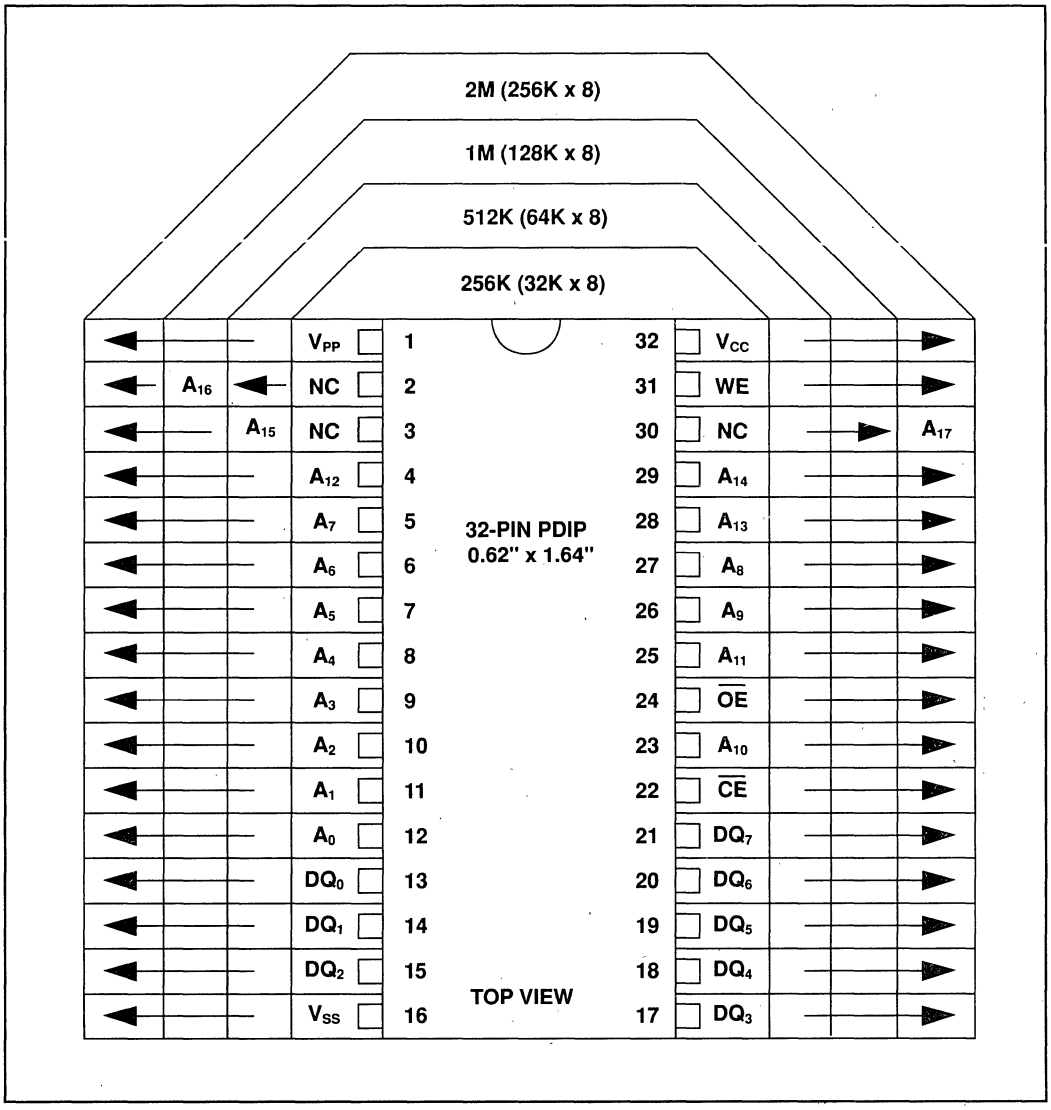

Figure 1. PDIP Pinouts from 256Kb to 2Mb

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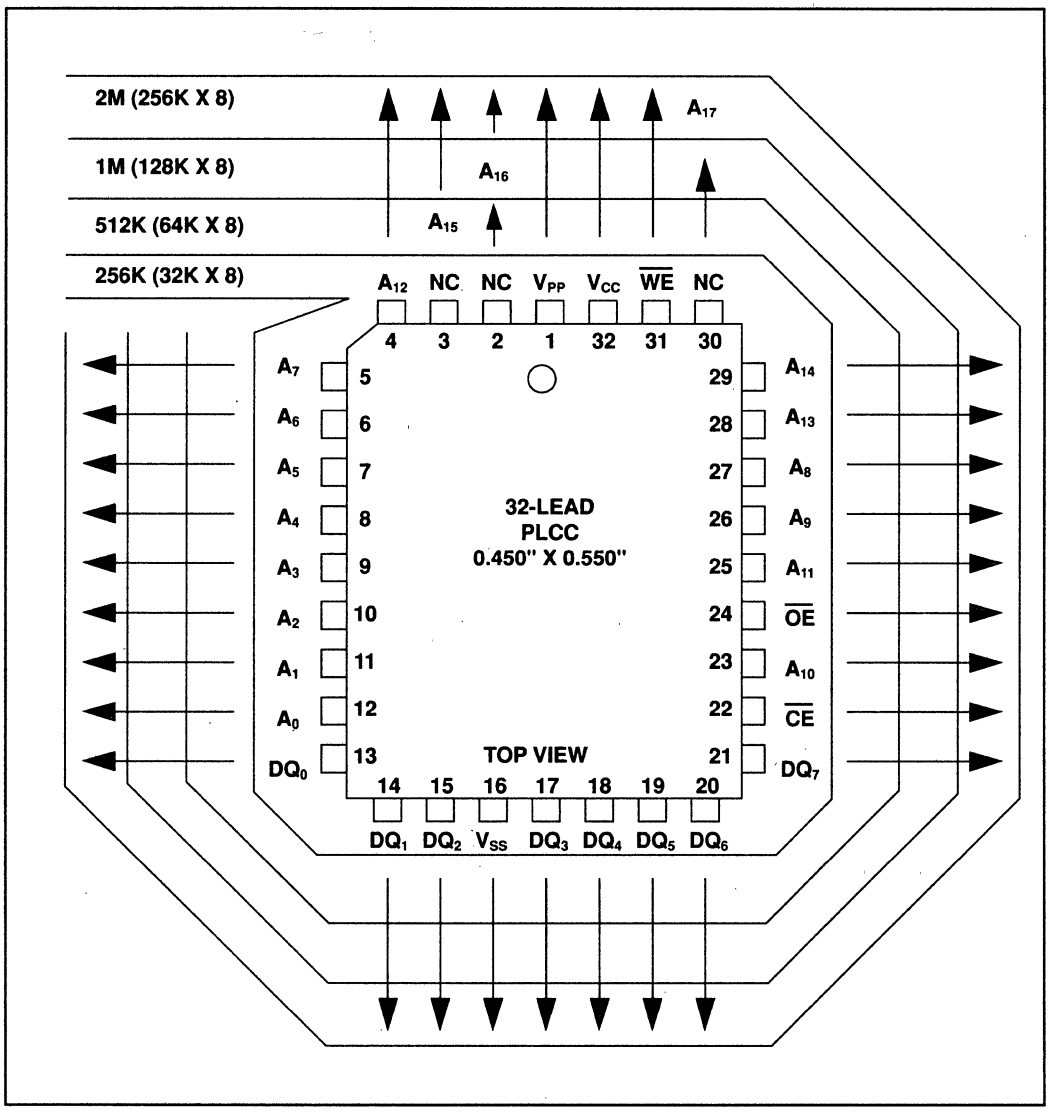


Figure 2. PLCC Pinouts from 256Kb to 2Mb

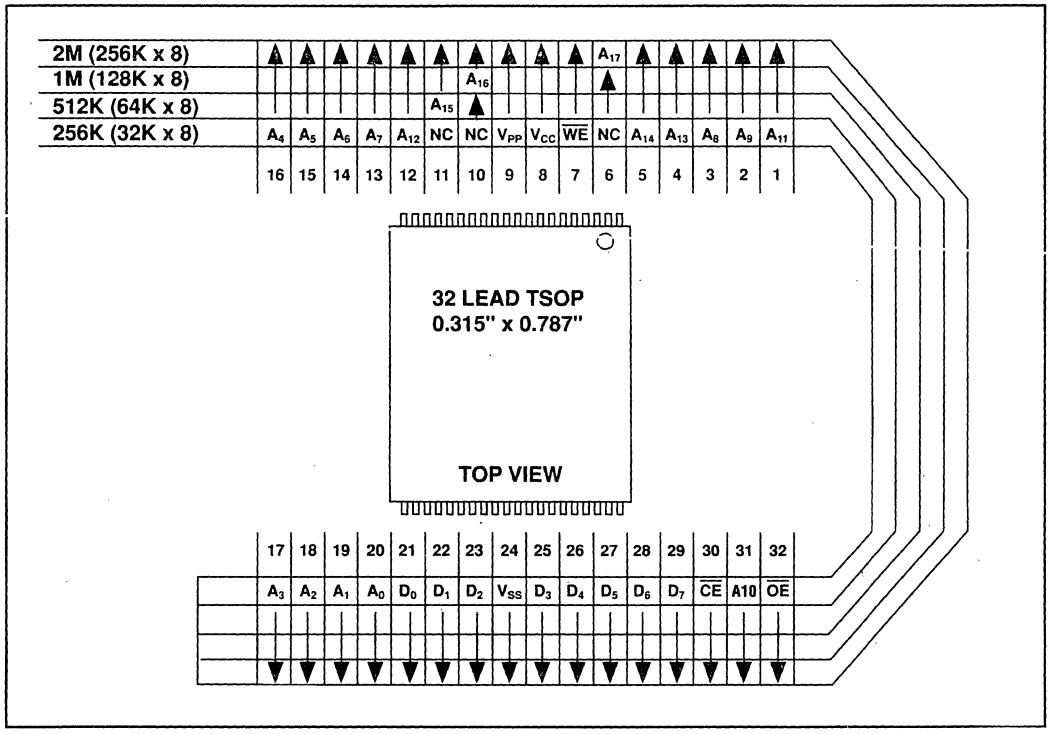


Figure 3. TSOP Pinouts from 256Kb to 2Mb

6

Plastic Dual In-line Package

PDIPs with sockets provide an excellent way to prototype and debug new designs. 1Mbit and 2Mbit flash memories are pin-compatible with the corresponding EPROMS. Lower-density EPROM can be placed pin-for-pin in the lower 28 pins of a 32-pin flash memory socket. Simply jumper V_{CC} to pin 30 of the higher density socket.

Plastic Leaded Chip Carrier

Most system designs today require surface mount technology (SMT) due to shrinking board real estate and portable form factors. PLCC is one SMT component that uses as little as 35% of the overall board space compared to PDIP. Its small size is attributed to the center-to-center lead spacing of 50 mils versus 100 mils as well as its four-sided pinout. The J-lead design allows the PLCC to be directly soldered to the circuit board. Most SMT manufacturing equipment can easily handle the PLCC's 50-mil lead pitch.

Recently, AMP introduced a SMT socket for PLCCs (P/N 821977-1) that has an identical footprint for 32-pin devices. This socket can be used in place of directly soldering a PLCC for prototype build and code testing. Once the reprogramming code is tested and debugged, flash PLCCs can then be surface-mounted without socketing during production-runs.

Thin Small Outline Package

TSOP is the package of choice for hand-held equipment or palmtop/laptop computers. These compact systems require minimal height and area for all components, for which TSOP excels. TSOP height measures 1.2mm versus 3.5mm for PLCC. TSOP area is 8mm x 20mm compared to PLCC's 11.43mm x 13.97mm. Therefore, TSOP has significantly less total volume: TSOP = 172.8mm^3, while PLCC = 656.3mm^3, and DIP = 1872.3mm^3. State-of-the-art center-to-center terminal spacing of 20 mils yields a smaller package with narrower conductor traces than PLCC or PDIP. Location of pins on both ends of the package allow traces for TSOP to be routed underneath the chip, reducing board layers. TSOP is available in standard and reverse pin configurations (see figure 4) allowing components to be laid out end-to-end and side-to-side (in serpentine fashion) for highest board density (see figure 5). Note how pins 32-17 on the standard pinout match pins 1-15 on the reverse pinout, and how pins 1-16 on the standard pinout match pins 32-17 on the reverse pinouts.

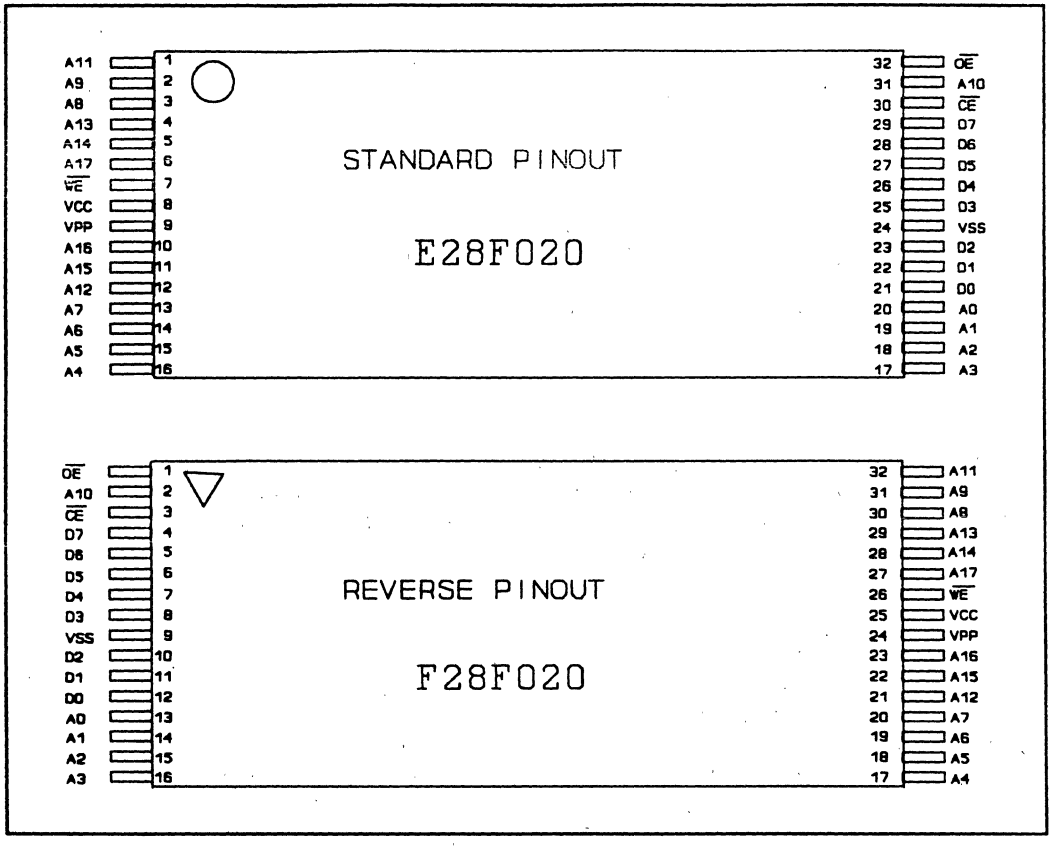


Figure 4. TSOP Standard and Reversed Pinouts

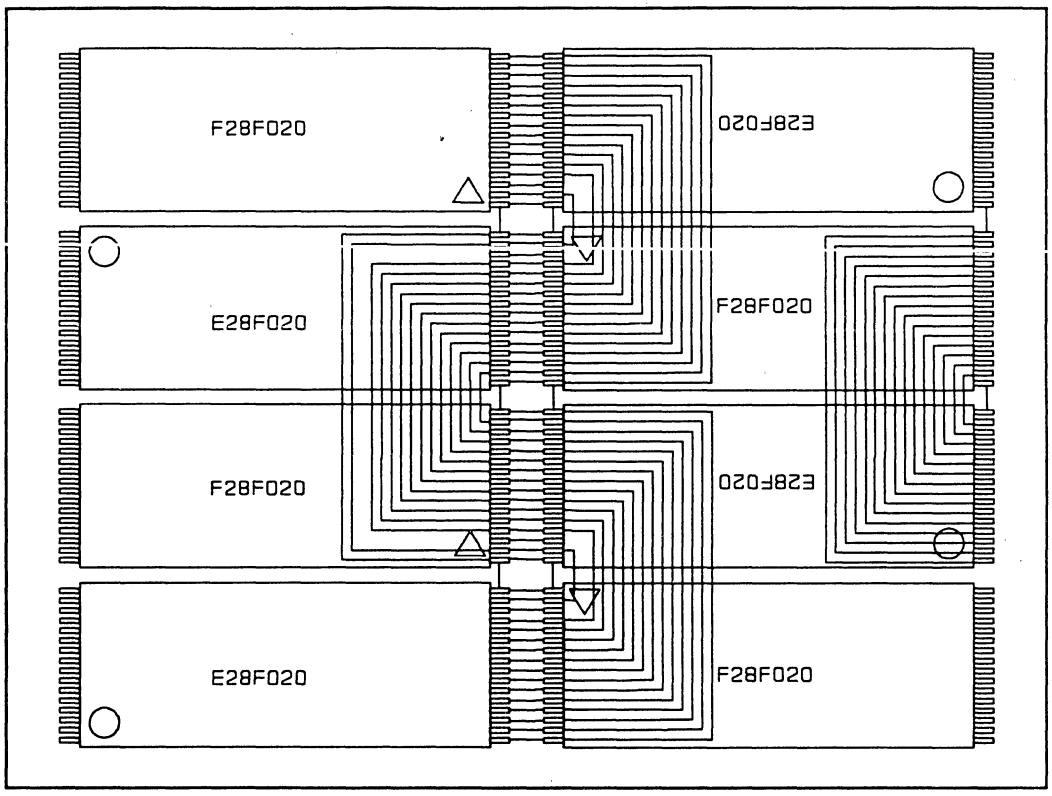


Figure 5. TSOP Serpentine Layout

2.4 V_{PP} Specifications

Fixed V_{PP} and V_{CC}

Flash memories, like EPROMs, require a 12V programming power supply. Unlike EPROMs, however, the V_{PP} for flash memory is a fixed, standard level. When combined with the Command Register erase/write control, Intel flash memories use a simple, SRAM-like hardware interface with standard microprocessor timing.

Intel's flash memory V_{PP} specification is 12.0V ± 0.6V (5%), compatible with most off-the-shelf system power supplies. The IBM PC* technical reference manual specifies the 12V power supply at 12.0V, +5% and −4%. Additionally, some hard and floppy drives require 12V ± 5%. Therefore, most PC power supplies have 12V supplies with ±5% or better tolerance. Possible exceptions to this are laptop and/or palmtop PCs. Some of these require 5-volt-only designs, in which case 5 volts is charge-pumped to 12V.

It is essential to use the specified V_{PP} when programming and erasing flash. Once the commands to program, erase or verify are issued, the device internally derives the required voltage references

from the V_{PP} supply. Therefore, an improper V_{PP} level degrades the performance of the part. The hardware design section discusses various methods of V_{PP} generation if your 12 volt power supply does not meet the proper tolerances or 12 volts is not available.

V_{CC} and V_{PP} Lockout Protection

Intel flash memory provides additional protection for designs that tie 12 volts directly to the device. Since the 12 volt supply is less capacitively loaded than the 5 volt supply, the 12 volt power supply reaches full value faster during power-on. If command register lockout protection was not provided, a small, finite possibility exists that inadvertent writes may occur during power-on. For this case, Intel flash memory affords command register lockout protection when V_{CC} is below 2.5 volts and V_{PP} is below 6.5 volts, preventing any writes to flash memory from occurring. Since CMOS logic is valid at 2.0 volts, a 0.5 volt margin of protection exists, providing extra time for control signals to settle before the Command Register is activated. Once V_{CC} reaches 2.5 volts and V_{PP} is greater than 6.5 volts, the Command Register begins processing valid commands. At this point, the system is responsible for write filtering.

3.0 HARDWARE DESIGN CONSIDERATIONS

The system level hardware requirements for implementing BIOS and application storage in flash are:

- Write Enable available to all of the flash memory
- 12V routed to flash location or generated on-board
- CMOS control-signal interface, or $\overline{WE}$ gated by a power-good signal
- Data buffer or transceiver that works in both write and read directions
- Space in memory map allocated for each application's size

The VIP 8000 (Vadem, Intel, Phoenix) laptop demo board was chosen as a flash BIOS system design example because it demonstrates the modification of an existing laptop chipset. The VIP 8000 chipset consists of an 80386SX™ processor, an 82344 bus controller, an 82343 system controller, and a Vadem power management chip. The bus controller and system controller contain configuration registers that must be set for flash BIOS updates. Some particulars relating to this chipset are:

1) Configuration register RAMMAP bit 7, when changed to a 0 will not generate a $\overline{ROMCS}$, but accesses to F0000-FFFFF still does.
2) The EAXS and FAXS registers must be set to 00H in order for $\overline{ROMCS}$ to be generated.
3) If any of the 4 EMS Page registers in the E0000-EFFFF range are active, they create a 16K window with no $\overline{ROMCS}$.
4) The XD (82343) 8-bit data bus transceiver is prevented (internal logic) from writing data out to the BIOS address range.
5) $\overline{ROMCS}$ and $\overline{MEMWR}$ is not a valid condition, so flash CE must be generated externally.

Other chipsets may have similar restrictions. Figure 6 is a block diagram for a flash BIOS implementation on the VIP 8000 chipset, which will be referenced throughout the rest of the hardware and software sections of this application note.

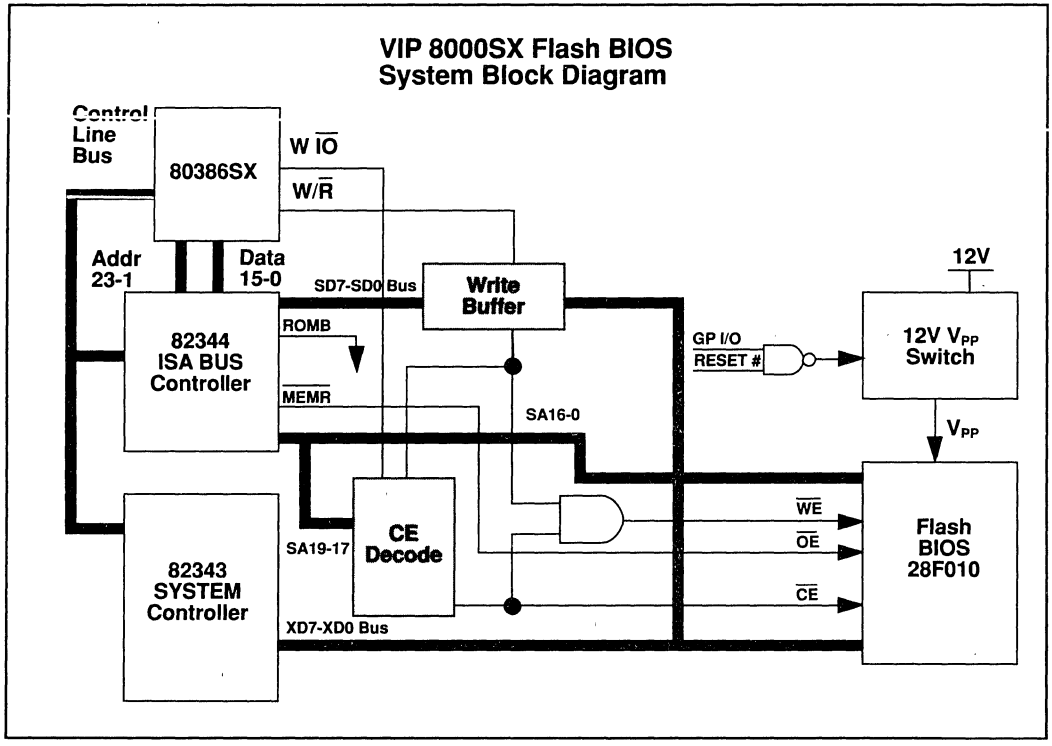


Figure 6. VIP8000 Flash BIOS Block Diagram

A write buffer is used on the SD bus since data for writes is not allowed on the XD bus in BIOS memory address locations. Data for reads is passed on the XD bus using the 82343 internal data buffer. The 82344 provides internally-latched system address lines to address the 28F010. The flash write enable signal is generated using the 386SX™ write signal in combination with the $\overline{CE}$ signal from the decoder. The 82344 $\overline{MEMRD}$ signal controls output enable while the decoder controls chip enable. The V_{PP} switch block controls the application of 12 volts to flash memory and is discussed in section 3.2.3.

3.1 Modifying an Existing Motherboard

If you are modifying an existing motherboard design to accommodate a flash BIOS, there are a few things you should consider. First, check the logic design to determine if $\overline{WE}$ is decoded out to the BIOS EPROM location. Typical motherboard logic designs do not allow writes to the EPROM locations and treat EPROM writes as invalid (e.g. $\overline{ROMCS}$ not generated with $\overline{MEMWR}$). This is overcome by generating the BIOS location's $\overline{WE}$ externally by either adding the necessary discrete logic or adding a 3-to-8 decoder (see figure 7 for an example). In either case, tap into the 386SX™ M/$\overline{IO}$ and $\overline{W}$/R control lines and configure the decoder to provide a logic low for the { $\overline{M}$ "OR" $\overline{W}$ "OR" BIOS address } condition. Secondly, check to see if the BIOS code transceiver or buffer for the EPROM location works in both directions. The transceiver may need a special BIOS call to unlock it in the "write" direction, or you may have to reprogram the logic for that portion of your board. If your chipset data buffer works only in one direction, a transceiver and direction logic must be added to the CPU bus to pass data to and from flash memory.

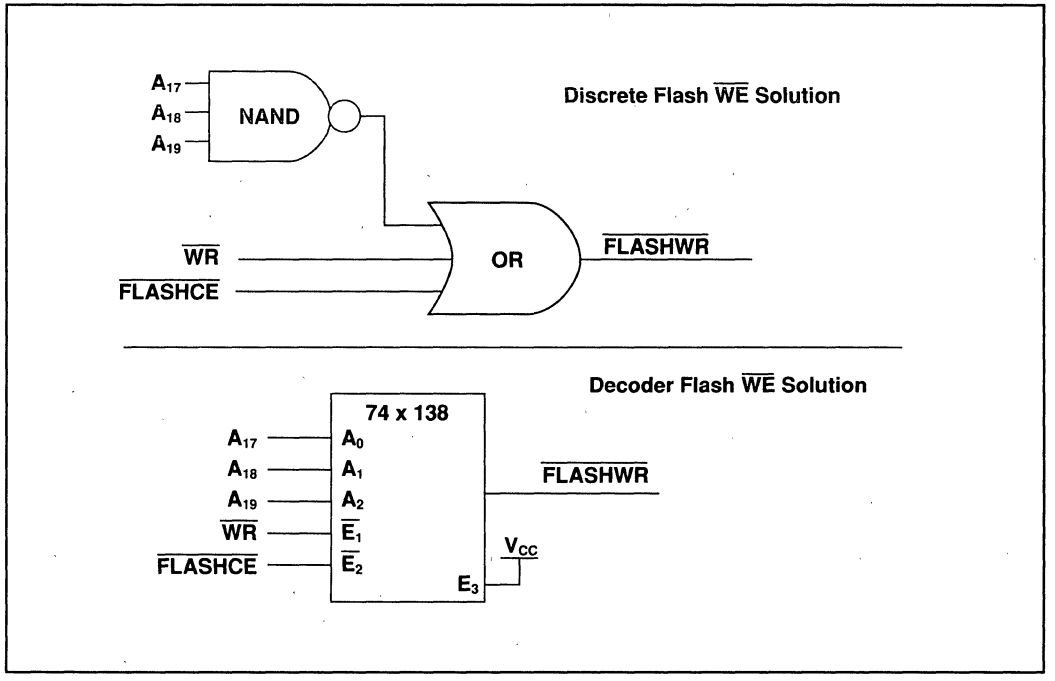


Figure 7. Discrete and single-chip decoder $\overline{WE}$ solutions

3.2 Vpp Generation

For flash BIOS designs, the 12V V_{PP} can be provided by:
1) Using existing 12V supply from PC Power Supply;
2) Generating 12V using a charge pump or DC-DC converter from the 5V supply.
Flash typically requires only 10 mA for program or erase (30 mA max); otherwise only 100 μA is drawn in standby mode.

3.2.1 USING SYSTEM 12V DIRECTLY

As stated earlier, the IBM PC technical reference manual specifies the 12V supply as +5% and −4%, which meets the Intel flash memory V_{PP} requirement. If your power supply meets this condition and has CMOS logic, 12V from the PC power supply can be tied directly to flash memory, eliminating the need to add extra circuitry for V_{PP} generation. This is possible due to V_{CC} and V_{PP} lockout protection offered in Intel's flash memory. However, it is recommended that you switch V_{PP} if writes to the BIOS location occur (e.g. loading the GDT from BIOS location) during boot loading or normal operations.

3.2.2 PUMPING 5V TO 12V

If your system does not provide 12V or does not meet flash memory specifications, several 5-to-12V converters are available, including surface-mount versions. AP-316 lists several V_{PP} solutions which offer on/off control of V_{PP} and provide a steady V_{PP} rise and little overshoot.

Figure 8 shows one example of one charge pump design. On power-up, system reset or when V_{CC} is below 4.5V, V_{PP} is forced off. It is enabled (or disabled) by writing to the VPPEN I/O port address. On/off capability is essential for battery-operated equipment and eliminates the need for $\overline{WE}$ filtering. The VPPEN signal "OR'ed" with the system memory write (MEMWR) functions as the clock signal for the 74FC74 D-flip-flop. The D-input is latched when MEMWR goes high. Writing a one or a zero turns V_{PP} on or off, respectively. Linear Technology's LT1072, a switching regulator, is used as a 5V to 12V charge pump. The 10.7K and 1.24K resistors are used to establish the correct reference voltage to obtain 12 volts. The 100 uF capacitor at the output is used to handle up to 200 mA. For a single- or double-chip BIOS design, this capacitor value can be halved or even quartered to allow selection of a SMT capacitor value, since the maximum I_{PP} current per device is only 30ma (10ma typical). Sufficient time should be allowed when switching V_{pp} on, allowing the charge pump to level out and enabling the command register to receive commands(1). The diode, MUR120, keeps the inductor from absorbing current from the charged output capacitor. The 5.6 volt zener diode ensures that when V_{PP} is less then 5.6 volts, the V_{PP} output is held at zero volts(2).

Notes:
1. See section on Software Timing Delays for V_{PP}-on times.
2. This is optional if the power draw with V_{PP} @ 5 volts or less is tolerable.

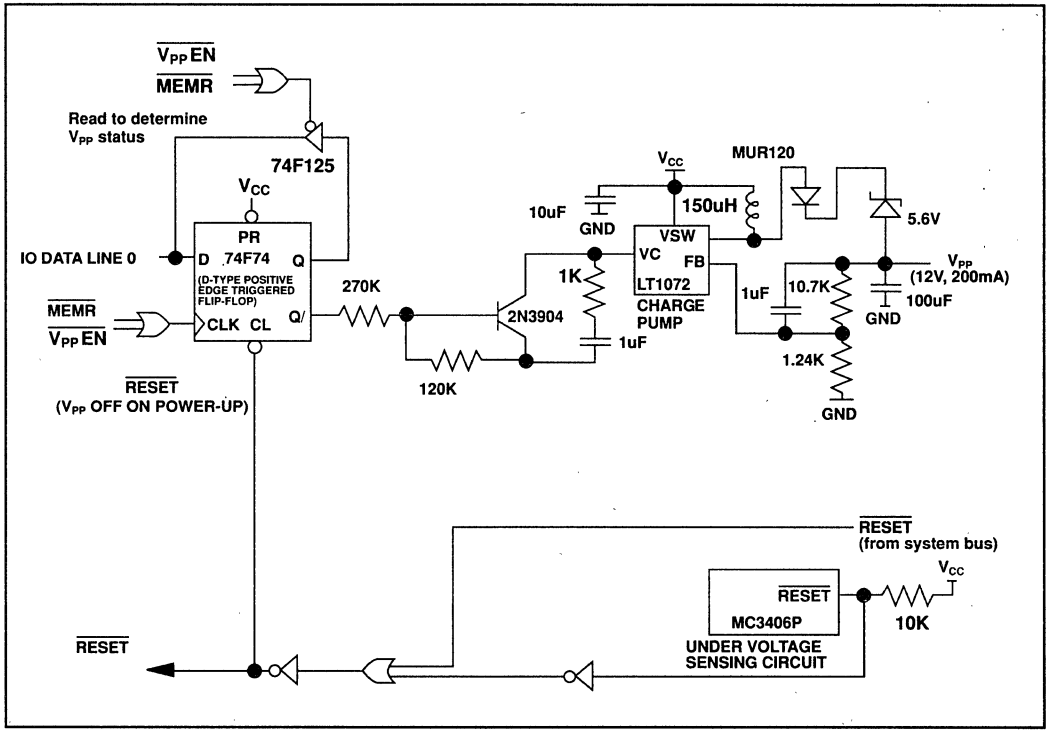


Figure 8. V_{PP} Generation with $\overline{WE}$ protection.

Controlling V_{PP} provides an additional benefit of system security. Beyond this, you can design for even higher security levels. The first level could be the design of a simple software password routine that would only turn on V_{PP} when a correct password is given. Alternatively, you can provide a jumper to allow 12V to the part for a BIOS update and then return it when reprogramming is finished. The system should check this pin to see if the jumper was left in the programming position and remind the user to move it. Unless V_{PP} is at 12 volts, the flash memory contents cannot be changed and acts just like ROM.

Disabling V_{PP} until voltages have stabilized provides additional power-up protection. The Motorola component, MC34064, is an under-voltage sensing circuit that begins functioning when V_{CC} is above 1 volt. Between 1 and 4.6 volts, the RESET output is active. The RESET output (or a system RESET) clears the 74FC74, keeping V_{PP} off when V_{CC} is less than 4.6 volts. Alternatively, if you use CMOS logic, you could make use of Intel's flash memory V_{PP} and V_{CC} lockout function. While V_{CC} is below 2.5 volts and V_{PP} is below 6.5 volts, the Command Register is locked out. Since CMOS control logic is active at 2.0 volts, a 0.5 volt safety margin exists for control logic to settle down before the part becomes active. For designs that do not use CMOS logic (i.e. control logic active at 2.0V), gate $\overline{WE}$ with the power supply's "Power Good" signal or the MC34064's RESET output (Figure 8).

3.2.3 USING A MOSFET SWITCH

For laptops/palmtops, an always-active 12V may not provide acceptable power management. Additionally, there may not be enough space for a charge pump, but 12V is provided — VIP8000 for example. For these systems, a MOSFET switch will work adequately. Several DC switches exist, but there are a few issues to consider in your selection. The "ON" resistance must be very small for the V_{PP} voltage to stay within flash memory specifications. The system 12V power supply must be specified to a tighter range to allow for the voltage drop through the switch. An I/O line (V_{PP} enable) must be allocated to turn the switch on and off. To handle "warm $\overline{\text{RESETS}}$" the V_{PP} enable must be gated with the system $\overline{\text{RESET}}$ line. The Motorola MTD3055E is one example of a surface-mount switch with low drain-source resistance. Assuming a 12V +5% and −4% supply:

$R_{DS} = 0.15\Omega$ $\quad I_{PP} = 30mA$ (worst case)
ΔV_{switch} Drop = 30mA x 0.15Ω = 0.0045 V, << 5% of V_{PP} = 0.6V.

Figure 9 shows a schematic of a V_{PP} switch design.

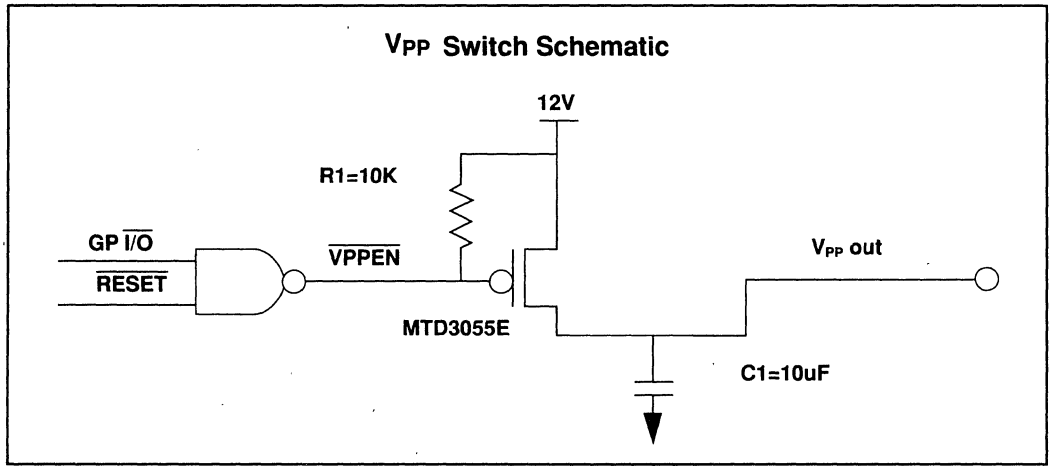


Figure 9. V_{PP} Switch using MTD3055E

3.3 Ideas for Using Extra Adaptor Space

Laptop systems may have extra adaptor space available since there typically isn't much room for add-in boards. The extra space can hold ROM executable programs (e.g. Tandy* Deskmate) like Lotus 123*, Wordstar*, etc. Using Intel's flash TSOPs, a small application cache can reduce a laptop's disk access and increase battery life. Additionally, Microsoft's ROM-Executable DOS Version 3.22* can be placed anywhere in adaptor space. "MS-DOS ROM Version 3.22" requires 64KB of adaptor space today (this may change on subsequent revisions).

One location for MS-DOS ROM executable 3.22 is directly under the BIOS (see figure 10). Today's typical BIOS consumes 64KB; consequently, both the BIOS and MS-DOS ROM executable can reside in a single 28F010 (128 K-bytes), yielding reduced chip count. However, if power management code is added to the BIOS (e.g. VIP 8000), system BIOS code could grow to 80KB or more. Therefore, designs that include both power management and MS-DOS ROM executable should consider using the larger 28F020 (256 K-bytes) flash device. This leaves extra space for BIOS and DOS in ROM to grow in the design, while providing additional storage for the video BIOS.

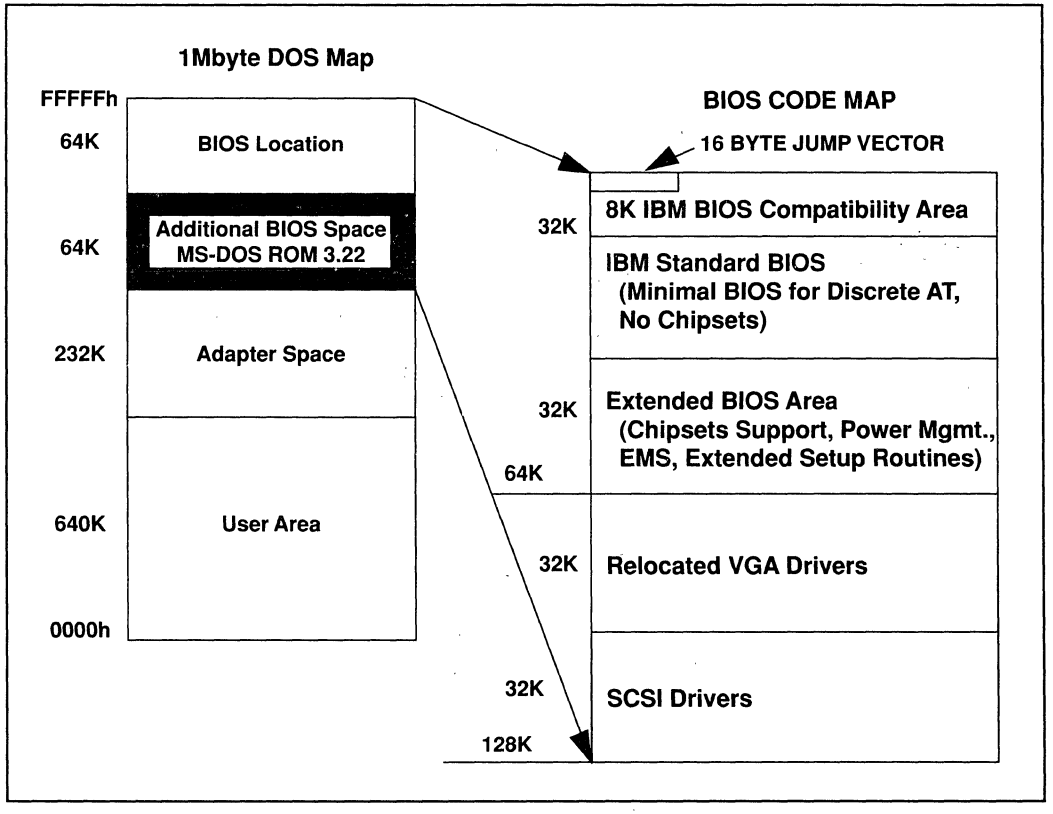


Figure 10. DOS Memory Map

3.4 BIOS Boot Code Requirements

A key flash memory benefit is soldering it directly onto a circuit board, eliminating sockets for production runs. A concern some designers might have when implementing a SMT flash BIOS is: what to do in the unlikely event that the BIOS update is incomplete (e.g. power failure during update)? One manufacturer looked at the probability of something else failing in the system versus an incomplete BIOS update. Their analysis showed a far higher probability of other system hardware failures (typically the hard disk or power supply) verses the probability of an incomplete BIOS update. Consider that a BIOS update for two 28F512's only takes 7 seconds[1] — including the loading of MS-DOS ROM executable. The chances are very slim — (# of power outages/ year * 7seconds / 31.5 x 10^6seconds/year) for an incomplete update to occur, once the update code is tested and verified. However unlikely BIOS updates may be, you may choose to provide special protection against power loss during BIOS updates. The following section discusses three methods of implementing designs that can handle the incomplete update scenarios.

3.4.1 SOCKETING A FLASH-ONLY DESIGN

Sockets, both DIP and PLCC, provide update protection by allowing the removal of an incompletely updated flash part. PLCC sockets are no higher than the PLCC itself and just 2mm wider on each side. If an incomplete update occurs, the socketed parts can be removed and reprogrammed locally by the OEM. Another benefit for flash-only designs is that no changes to the BIOS code are needed, just add your standard BIOS code in file form for use by the update utility software.

One manufacturer who uses a socketed flash BIOS design stated that even if a few updates were unsuccessful, all the other successful updates on other systems would easily cover the cost of the few updates that might not succeed. This scenario is still-cost effective compared to updating all machines with EPROMs or having users update machines with EPROMs.

3.4.2 SMALL EPROM FOR BOOT RECOVERY, FLASH THE REST

Adding a small 8KB boot EPROM, in addition to flash, provides maximum security for incomplete BIOS updates. The EPROM could be placed above or below the flash memory in the system address map. The next two sections discuss each option. Both methodologies require some external logic and additions to the BIOS code.

8KB Boot at TOP (see figure 11)
This scenario places the processor jump vector, BIOS check-sum and initialization code, and the basic system start-up code (if an invalid BIOS is detected), within a small 8KB EPROM. The regular 64KB BIOS code (including the jump vector) is placed in flash starting from the top (1FFFFH). This positions all the regular BIOS code 8K below where the system expects it. At boot time the processor jumps to the EPROM and starts setting the system up. It also checks the BIOS code in flash. After the flash BIOS is determined to be valid, system RAM is checked, then the BIOS code is copied into shadow RAM. The system finishes boot and is ready to use.

Notes:
1. Demonstrated on Intel's 386™, 16MHz, 301Z flash BIOS demo

When a BIOS check determines an invalid BIOS, the system RAM and floppy drive (or possibly a modem) are initialized with the boot recovery code located in the 8KB EPROM. Next, a request to install the BIOS update floppy disk is written to the screen while the floppy driver routine polls the drive until a floppy is loaded. A search on the floppy is performed for the file[1] with the correct BIOS file name. Once the file is found, the update code is loaded to RAM and the update utility proceeds to erase and reprogram flash with the loaded BIOS file.

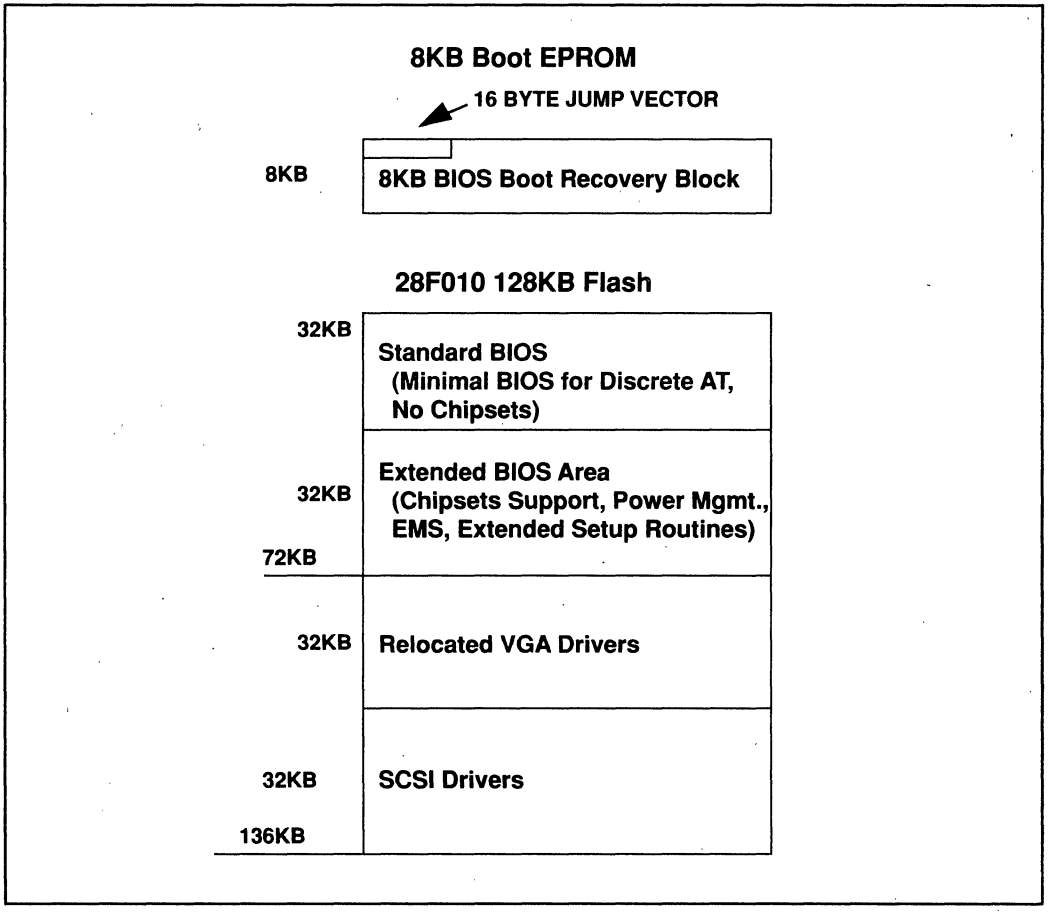


Figure 11. Top EPROM Boot/Flash BIOS Code Combination

Some systems require capability to turn shadowing off and directly execute BIOS code. Since the BIOS code is shifted off by 8KB for the Boot EPROM, an address shifter is needed to allow direct execution of BIOS code. Figure 12 shows an EPLD address shifter with a SHIFT8K input. Once the signal to direct execute is given, the EPLD shifts all address requests by 8KB to the flash part and generates the proper chip select.

Note:
Alternatively, the BIOS recovery code can contain specific, non-DOS, sector/track information pertaining to the location of the new BIOS update file. Thus, the file is not readable to basic DOS users and is protected.

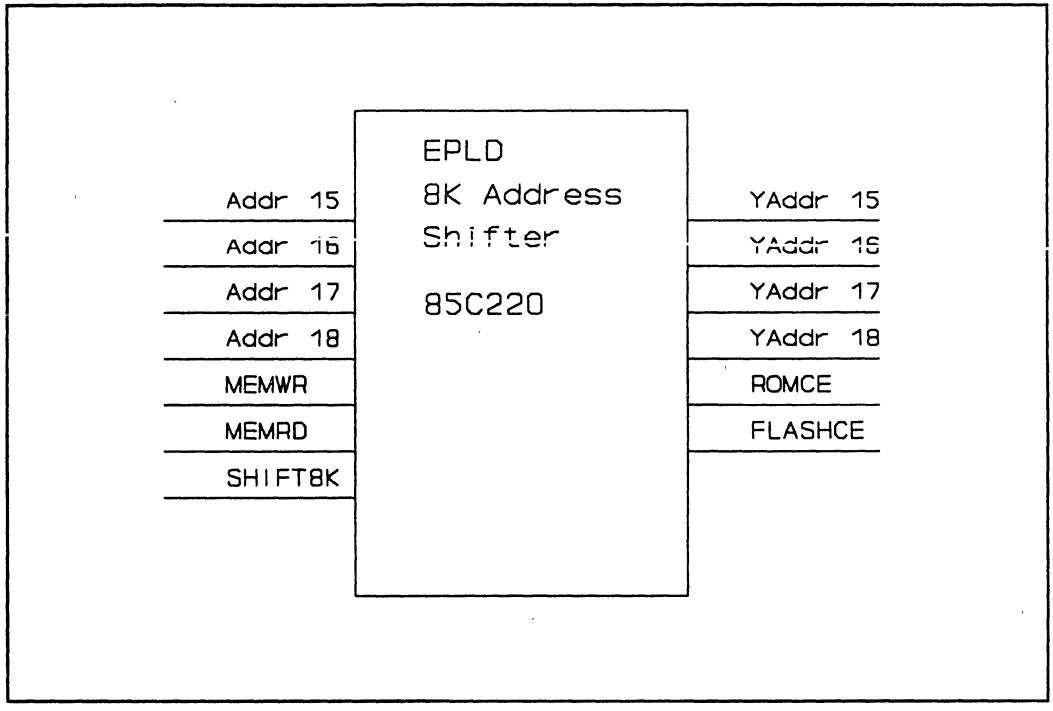


Figure 12. 8KB Address Shifter

8KB Boot at Bottom (see figure 13)
In this scenario, the 8KB EPROM with boot recovery code resides below flash memory in the system address map. The regular 64KB BIOS code is stored starting from the top of flash memory starting. As long as updates are successful, no changes are needed for the system to freely shadow or direct-execute the BIOS code. If an update is incomplete, the system may boot partially or won't boot at all. The user would then move a jumper or an external switch, which places the 8KB boot EPROM at the top of the 1MB system memory map. When the processor reboots, it jumps to the EPROM and begins the BIOS recovery process just like the previous top boot solution. Once the BIOS update is finished, remind the user to move the jumper back, moving the EPROM below flash. Until this is done, the system will keep trying to run the update utility.

Since standard BIOS code does not support boot recovery, your BIOS software engineers must design the boot recovery code for the 8KB EPROM. Alternatively, your BIOS vendor can be contracted to develop the code. The rest of the BIOS code located in flash memory stays the same.

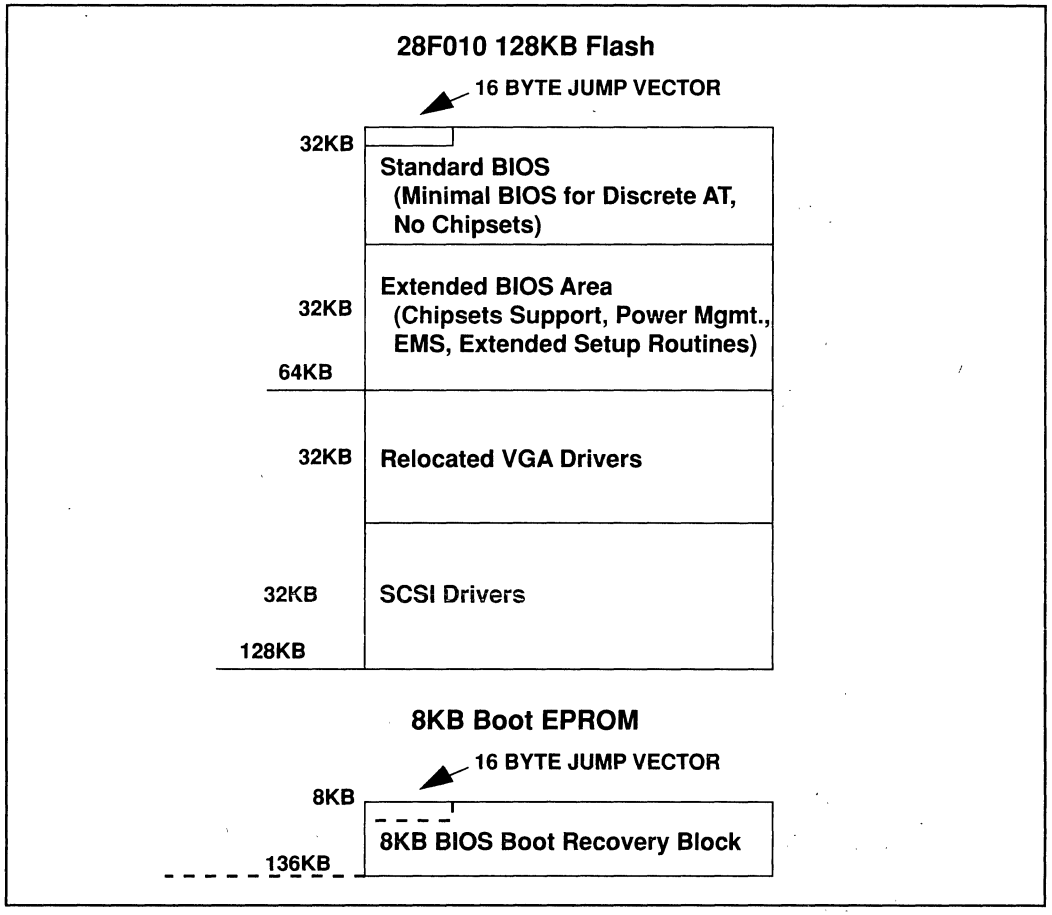


Figure 13. Bottom Boot EPROM/Flash BIOS Combination

3.4.3 HALF EPROM, HALF FLASH

Another alternative is to put half the BIOS code in EPROM and half in flash memory. One positive is that the system would have enough EPROM to reboot itself but still have some flash memory for partial code updates. There are a few negatives to this solution, however. One is that a direct-execute x16 system would require 4 chips, actually increasing chip count. Another is that only half of the BIOS code could be updated.

3.5 In-System Write vs. On-Board Programming

When devices are soldered directly to a printed circuit board, one of two sources control flash memory reprogramming: 1) the system's own processor, or 2) a PROM programmer connected to the board. These options are called In-System Write (ISW) and On-Board Programming (OBP), respectively. Their respective benefits are discussed in detail in AP-316.

With ISW, the system drives the reprogramming process and generates V_{PP} locally. A good design practice for ISW-type designs is to socket the first few flash BIOS prototypes. SMT-only designs can also socket using PLCC SMT sockets. Socketing enables the system designer to easily work out any bugs with in-system flash reprogramming by allowing the removal of a flash part for external reprogramming in a prom programmer. Once ISW reprogramming is fully debugged, pre-programmed flash parts can be soldered directly to the circuit board without a socket. All flash memory components are exposed to a data-retention bake testing and checked for any data loss before shipping. It is extremely unlikely that data in a production flash device can be corrupted from heat by a production-run soldering application.

OBP uses a PROM programmer to supply V_{PP} and control the programming process. Certain design considerations must be evaluated prior to laying out the design. Some manufacturers using TSOP may also want to remove a handling step from the manufacturing process by providing the capability to program flash for the first time after being soldered directly onto the circuit board. OBP can accomplish this if the design is first laid out correctly to support OBP.

NOTE: See AP-316 appendix A for OBP design considerations.

4.0 SOFTWARE DESIGN CONSIDERATIONS

Intel's flash memory provides a cost-effective, updatable, nonvolatile code storage medium. The reliability and operation of the device is based on the correct use of specified erasure and programming algorithms. To assist debug and prototyping, Intel's flash memory features stop timers, which terminate a single erase or programming operation at the maximum spec allowed by the silicon. **However, please note that the stop timers on the 28F256A, 28F512, 28F010, or 28F020 do not provide fully automated erase or programming.** More detail on this feature is covered in each part's respective data sheet.

Intel offers standard software drivers to assist software engineers implementing flash memory reprogramming for update utilities. The software is tailored around each CPU family (i.e., x86, 51, 196, and 960) and requires modification of the timings to your specific application. For example, you supply the memory width (8-, 16-, or 32-bit), system timing, and a subroutine for control of V_{PP}. PC-specific timers are discussed in this application note. If you use another CPU from Intel, call your FAE who has access to the drivers or call the Intel Embedded Controller Operation (ECO) Bulletin Board System (BBS). Look under the flash memory section for drivers. You'll find 51, 186, 196, and 960 drivers in archived form.

Note: Please contact your sales office for details.

If you prefer to implement the flash memory algorithms yourself, flow-chart outlines appear in the flash re-programming section.

Covered in this section are the major software steps for a flash BIOS update utility:

- Update software for a modified system
- Pseudo-Code overview
- Initializing the system
- Code loader routine
- Flash re-programming
- Timing calibration options

The software code patches used in this example are specific to a "flash-only" hardware design for a demo flash BIOS add-in board. Modifications for flash writing and reading on the VIP8000 must still be made for your design. Other hardware/software designs can easily build upon the concepts and code patches discussed here. For a more detailed source listing, call your FAE or the ECO BBS.

4.1 Update Software for a Modified System

Our design example assumes BIOS shadowing for BIOS code execution while allowing BIOS writes to the flash socket. Many systems provide a port by which BIOS writes and reads are enabled by toggling the port bit. Some systems may not allow BIOS reads from RAM while performing BIOS writes to the flash socket, or vice versa. The reasons may be simple — there is no shadow RAM in the system (8088 or 8086 systems) — or as complicated as system logic treating it as an invalid operation. In these cases, perform all your required BIOS calls before you erase and program the flash memory. But keep in mind, to update the user on the progress of flash programming and indicate when programming is finished, you should add some basic screen BIOS routines to your update utility.

4.2 Pseudo-Code Overview

The following pseudo-code for an update utility provides a brief description of the process of updating a BIOS in-situ. It is based on an Intel BIOS update demo and must be modified for your particular chipset and hardware environment. The code for the BIOS demo was initially developed by Phoenix Technologies* and later modified by a consultant for new flash devices.

Pseudocode for Flash Update Routine

Initialize system (calibrate timers, set up user screen, check battery power, check device ID)

Get BIOS file (from floppy or modem)

If file not present,

send error message to insert BIOS update floppy, or press esc to exit

If extra space available, prompt user with space size and binary application file option

If user indicates yes, prompt for file and load

If file invalid,

Prompt for file or exit

Else save what was in the extra space to a buffer

Inform user what is about to happen, with option to continue or exit

If user continues, inform them to not turn off the power

Disable all interrupts

Erase flash memory

Write file[s] into flash memory

Indicate to user flash reprogramming is over

Reboot the system

4.3 Initializing the System

Checking Power

If your application is a laptop or palmtop computer, first check the battery to make sure there is enough power to do the update. If not, inform the user to re-charge the system before continuing the update and exit the update program. This ensures that the system won't stop in the middle of an update. Next, initialize access to flash for reads and writes, then try reading the device ID through the command register. Checking the device ID before programming or erasing helps determine if V_{PP}, writes and reads work correctly and that the flash memory in the system matches your code before starting to reprogram the part.

Device ID Check and Table

Since varieties of flash BIOS components (256Kb - 2Mb) and configurations (x8, x16) are possible, a device-unspecific update utility is preferred over a device-specific utility. Intel's flash memories contain a unique device ID for each density and/or device configuration. To read the device ID, turn on V_{PP} (if it is not directly connected), wait the appropriate on-delay time, then write a 90H anywhere within memory address range of the part you are checking. Next execute two read cycles in succession from the flash device, first from address 0000H, second from address 0001H of the flash memory. The data returned on the first read cycle 89H, the manufacturing code, while the second read cycle returns the device ID code (see the Device ID Table below). If the part does not read correctly, then exit the update program.

Device Type	Device ID
28F256 P1C2 Sb62	B1H
28F256A	B9H
28F512	B8H
28F010	B4H
28F020	BDH

Note: During the initialization, you can also perform a scan of the adaptor space to ascertain if there is more flash in the system. This will help determine if there is any flash applications present that may need to be updated. See code example in appendix B "Get_Flash_ID."

4.4 Code Loader Routine

The routine used for the BIOS demo prompts the user for file type (Hex or Binary) and then the file name. System OEMs may want to encode the BIOS file name into the generic loader utility ".COM" or ".EXE" file. This allows automatic reading of the new BIOS file into a program buffer, bypassing the user prompt. Otherwise, you may want to duplicate the process listed here. First, the file loader portion of the utility checks for available space left in flash memory, assuming the size of the BIOS file is known. Since the available flash memory check is accomplished in the initialization section (under device ID check), sizing information is already known. Extra space within a chip is determined by subtracting out the BIOS file size from the total flash memory space found. This extra space can easily be used for MS DOS ROM-executable (or similar OS), or other ROM-executable software packages that can fit in whatever space is left over by the BIOS.

Once the files are loaded, inform the user what is about to be done and provide the option to exit if they wish. If they continue, give a warning message telling the user to not turn off the power during the BIOS update procedure. Next, disable all interrupts to ensure an uninterrupted reprogramming operation.

4.5 Flash Reprogramming Routines

4.5.1 QUICK ERASE™ ALGORITHM

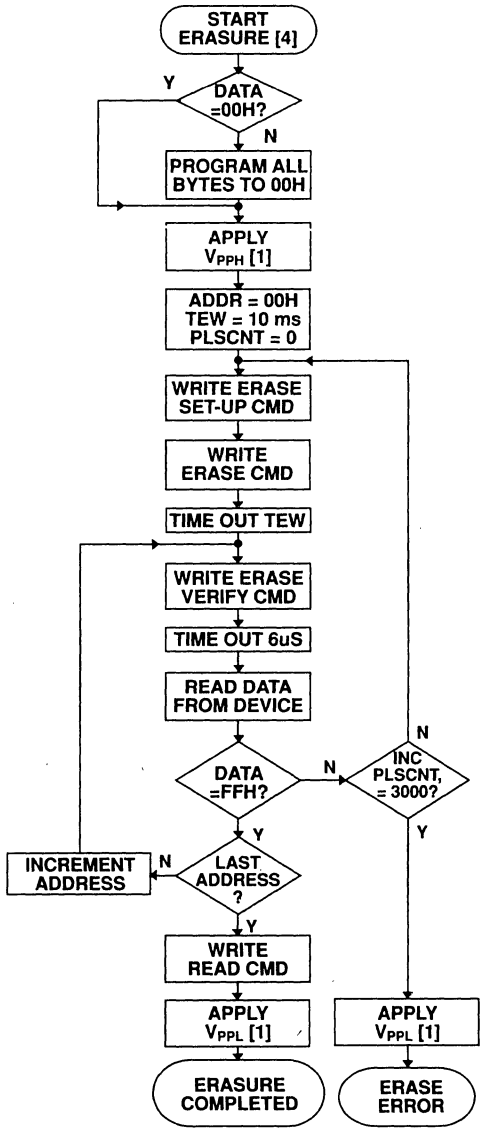
Flash memories chip-erase all bits in the array in parallel. The erase time depends on the V_{PP} voltage level (11.4V-12.6V), temperature and the number of erase/write cycles on the part. See individual device data sheets for specific parametric influences on reprogramming times.

Please note that all flash memory locations must be programmed to 00H before erasing the device. This provides equal charge throughout the array, insuring uniform and reliable erasure.

The algorithm has three different timing delays (Figure 14). The first is an assumed delay when V_{PP} first turns on. Systems that direct-wire 12 volts need not worry about this delay. The other two delays are the Erase Pulse (10mS) and Erase Verify Pulse (6μS). See section "Timing Calibration" for a discussion of how to generate time delays for PC systems.

4.5.2 QUICK-PULSE™ PROGRAMMING ALGORITHM

Flash memories program with a modified version of the Quick-Pulse Programming™ algorithm used for U.V. EPROMs (Figure 15). Programming is accomplished via a closed loop algorithm consisting of 10μS program pulses followed by the 6μS program verify pulse. See section "Timing Calibration" for a discussion of how to generate time delays for PC systems.



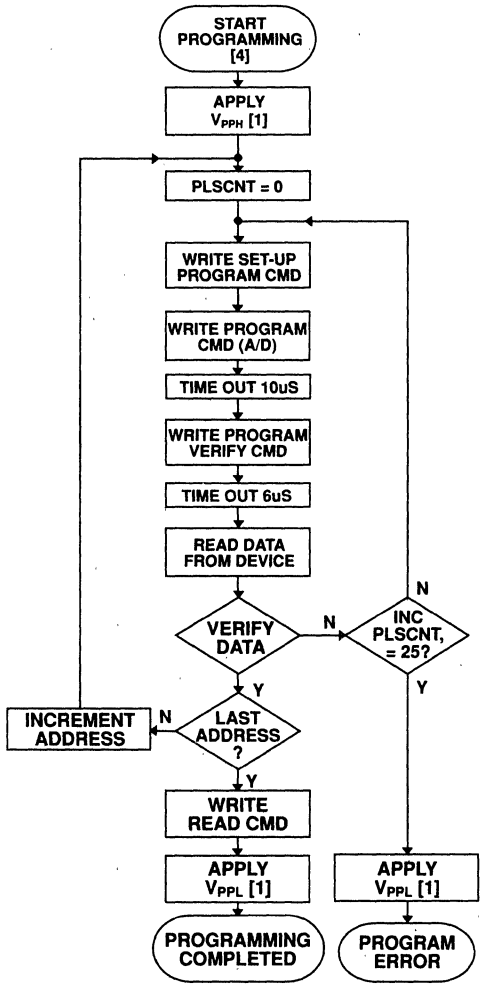
BUS OPERATION	COMMAND	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [1]
		Use Quick-Pulse Programming™ (Fig. 4)
		Initialize Addresses, Erase Pulse Width, and Pulse Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase Verify [2]	Addr = Byte to verify; Data = A0H; Stops Erase Operation [3]
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pusle count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [1]

Notes:

1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Erase Verify is only performed after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 14. ETOX II Erase Algorithm

6



BUS OPERATION	COMMAND	COMMENTS
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) [1]
		Initialize pulse-count
Write	Set-up Program	Data = 40H
Write	Program	Valid address/data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Write [2] Program	Data = C0H; Stops [3] Program Operation
Standby		t_{WHGL}
Read		Read byte to verify Programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} [1]

Notes:

1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 15. ETOX II Programming Algorithm

4.6 Timing Calibration

Intel's flash memory uses the following time delays:

- V_{PP} turn-on delay (for systems w/out hardwired V_{PP})
- 10μS timeouts for program
- 10mS timeouts for erasure
- 6μS timeouts for program or erase verify.

V_{PP}-on delay
Capacitors on the V_{PP} bus cause an RC ramp. After switching on V_{PP}, the delay required is proportional to the number of flash memory devices times 0.1uF/device. 100nS must pass after V_{PP} reaches its final voltage threshold before the CPU writes to the command register. Systems with hardwired V_{PP} eliminate this delay.

Erase, Program & Erase/Program Verify timeouts
By using the 10μS programming pulse width for program/erase verify delay (which has no maximum value), all three timeouts are reduced to two individual timing loops, a 10μS loop and multiple 100μS loops. There are essentially two methods for PC time delays. One utilizes the CPU and the other uses the CPU plus a standard system timer (8254) available in all PC architectures.

4.6.1 USING THE PROCESSOR

PC platform CPUs range in performance from the 5MHz 8086 to the new 33MHz 80486. Each processor has multiple running speeds and whether it uses a cached or non-cached I/F, so software timings tailored around one processor will not necessarily work for another. Therefore, separate timing routines are needed for each processor and each possible configuration. For an OEM with a small product offering, this may be acceptable. For an OEM with a wide range of systems and processor speeds, this becomes a software support issue. In the latter case, system timers provide a more universal solution.

4.6.2 USING THE SYSTEM TIMERS TO SELF-CALIBRATE SOFTWARE DELAYS

System timers help make time delays more consistent across processor lines. Caching can affect timing, so this should be turned off before starting a BIOS update. The software timer example in Appendix C uses the 8254 system timer to calibrate the necessary software delays for flash. First the timer is initialized to the correct mode. Second, a 100μS loop is checked by starting the timer, then starting the software loop. Once the software loop is finished, check the 8254. Adjust delay loop value accordingly. Next, the 10μS is checked in the same fashion as the 100μS delay and adjusted. The values found are then used for program and erase time delays.

Once reprogramming flash is completed, provide a message to user letting them know and then reboot the system.

5.0 SUMMARY

5.1 Traditional BIOS Storage and Disadvantages

Traditional BIOS storage has been in EPROM, which offers nonvolatility and external programming capability. In earlier PCs, the BIOS code was fairly simple (relative to today's software) and updates were infrequent, so EPROMs were an acceptable BIOS storage medium. Today's systems are much more sophisticated with many designs supporting the Intel 386™/486™ processors and new bus architectures like MCA™ and EISA™ for the first time. Therefore, the potential for a change in the BIOS code is much greater and the frequency of change is likely to increase. A system designer may use EPROMs for BIOS storage to reduce initial system (component) costs, but the long-term update cost is much more than the difference between EPROM and flash memory components. A major manufacturer of PCs stated that a service call for a BIOS update with EPROMs can cost upwards to $300.00 for one update at one site. EPROM updates are also susceptible to bent leads during insertion by the technician, or more likely, the end user. Service is becoming a key differentiator between the multitudes of PC makers. Reducing the number of times a PC has to be opened for any reason increases customer confidence and promotes a reliable image.

5.2 Advantages of an Updatable BIOS

Using flash memory for BIOS storage provides a flexible code storage medium that allows the BIOS code to adapt to changing hardware and software conditions. BIOS updates in flash are inexpensive, via a floppy disk or modem[1], and thereby remove EPROM inventories, reduce packaging requirements, reduce total postage costs and reduce service cost for BIOS code updates by removing the need for a technician to do the update. A company that supports multiple OEMs can reduce version management control by using a flash BIOS and floppys for updates. An additional benefit is that not only the BIOS, but DOS itself can be stored in the same flash memory device.

5.3 Advantages of Adding DOS in ROM

Once the requirements for flash BIOS are met, all the capability is also in place for adding DOS in ROM. "Why put DOS in ROM?," one might ask. For laptop/palmtop PCs, battery longevity is of paramount concern, followed closely by weight and increasing user RAM (640KB) space. Extra user RAM is needed for applications that need more than the typical 570K bytes (640KB-70KB) available with disk-based DOS. Digital Research Incorporated* and Microsoft both make DOS-in-ROM products that address these needs. MS-DOS ROM-executable 3.22 for example, reduces power and increases available RAM. Microsoft's ROM-executable version of DOS is a full-function version of MS-DOS 3.2. It features instant-on and employs only 15KB of the 640KB MS-DOS user space, leaving the rest for applications. Since MS-DOS ROM-executable 3.22 loads from adaptor space, both disk access and DOS load time are reduced. For laptops, anything that can reduce disk access equates to battery longevity. Laptops can reduce weight by using DOS in ROM and replacing the floppy drive with an IC card. Adding ROM-DOS to desktops also liberates additional user RAM for the same above reasons, but may not be beneficial on high speed 32-bit systems.

Note:
1. Intel's fast flash memory programming allows modem updates at 19.2K baud.

5.4 Advantages of Adding 1-4MB of Resident Code Storage

There is a growing need for systems to be able to provide a small suite of bundled applications. Benefits to the user are reduced hard or floppy disk access, no power used to store the resident code, and instant-on as there is little time wasted transferring data over a disk I/O interface, the code loaded to RAM with a simple memory copy function or procedure or, in some cases, code is directly executed by the processor. Tandy Deskmate* is an example of such a system. Future versions of Deskmate-like user interfaces could easily be made flash-updatable.

SRAM is too expensive and requires power to just store files. Furthermore, battery backup is not a reliable means of providing nonvolatility. Intel's flash memory can provide user configurability for 1-4 M-bytes of code storage for just 2x-3x the cost of EPROMs, less than half the cost of SRAM. Applications such as Lotus 123™ and Wordstar™ also come in either a direct-execute "ROM" version, or a copy-from-ROM format. Many other ROM application software packages are in development, servicing the successful and growing needs of the laptop/palmtop computers. Therefore, if an application can be stored or runs from ROM, it can be stored, run and additionally updated from flash.

Appendices

A. Software Routines to Enable Flash Writes and Reads
B. Flash ID Software Routines
C. Software Calibration Timers
D. MS-DOS ROM executable-DOS Overview

APPENDIX A
ENABLE FLASH WRITES AND READS

```
before_get_flash    proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:
;
;       This routine is called during system initialization before any
;       access is attempted to the flash memory parts.  The usage of this
;       routine is dependent on the system architecture.
;
;       The known usages are:
;
;       1. System can be placed in a state where F000 segment reads come
;          from ROM, and F000 segment writes go to ROM.
;
;          In this event, the system is placed into that state here.
;
;       2. System cannot be placed in a single state where F000 segment
;          reads and writes are addressed to the ROM.
;
;          If the system protects the access to the shadow register via
;          an I/O lock mechanism, then the I/O lock is unlocked here.
;
;          If the system will be placed in states where shadow RAM read
;          access is enabled (e.g. while writing ROM), then this routine
;          must perform a shadow copy of the BIOS ROM (and if DOS is in
;          ROM, it must also be copied) here.
;

        push    ax
        push    cx
        push    di
        push    si
        push    ds
        push    es
        call    wfibe                   ;In 301Z, lock port is Kbd controller
        cli
        mov     al, SHADOW_UNLOCK
        out     SHADOW_LOCK_PORT, al    ;unlock shadow control register
        call    read_rom_enbl                   ;set to read ROM / write RAM state
        mov     ax, 0F000h              ;shadow the BIOS
        mov     ds, ax                  ;This is necessary for the 301Z
        mov     es, ax                  ;because shadow may have not been
        xor     si, si                  ;enabled, and enabling write ROM
```

6

```
        xor     di, di                  ;access in the 301Z relies on the
        mov     cx, 8000h               ;presence of a shadowed BIOS.
        rep     movsw                   ;
        mov     ax, 0E000h              ;set up for possible E000h option
        mov     ds, ax                  ;ROM shadow
        mov     es, ax
        xor     si, si
        xor     di, di
        cmp     ds:[si], word ptr 0AA55h    ;test for option ROM
        jne     unlock_done
        mov     cx, 8000h               ;if present, then shadow it
        rep     movsw
                                        ;
unlock_done:
        sti
        pop     es
        pop     ds
        pop     si
        pop     di
        pop     cx
        pop     ax
        ret

before_get_flash        endp

write_rom_enbl          proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Enable writes to the ROM area to go through to the
;                       Flash parts
;

        push    ax
        mov     al, SHADOW_ON           ;enable ROM writes
        out     SHADOW_PORT, al
        pop     ax
        ret

write_rom_enbl          endp
```

```
read_rom_enbl       proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Enable reads to the ROM area to go through to the
;                       Flash parts
;

        push    ax
        mov     al, SHADOW_OFF          ;enable ROM reads
        out     SHADOW_PORT, al
        pop     ax
        ret

read_rom_enbl       endp

raise_vpp       proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Raise the Vpp voltage, and wait for it
;

        push    ax
        push    cx
        push    dx
        mov     dx, VPP_CONTROL         ;Vpp control port
        mov     al, VPP_ON          ;On value
        out     dx, al

        mov     cx, 500
delay_loop:
        call    wait_100_micro              ;call 100 microsecond delay
        loop    delay_loop
        pop     dx
        pop     cx
        pop     ax
        ret

raise_vpp       endp
```

```
lower_vpp    proc   near
;
;       Input: Nothing
;
;       Output:        All registers preserved
;
;       Function:      Lower the Vpp voltage, and wait for it
;

        push   ax
        push   cx
        push   dx
        mov    dx, VPP_CONTROL          ;Vpp control port
        mov    al, VPP_OFF          ;Off value
        out    dx, al

        mov    cx, 500
delay_loop2:
        call   wait_100_micro               ;call 100 microsecond delay
        loop   delay_loop2
        pop    dx
        pop    cx
        pop    ax
        ret

lower_vpp    endp
```

```
wfibe       proc   near
;
;       Input: Nothing
;
;       Output:     All registers preserved
;
;       Function:   Wait for the 8042 input buffer to be empty, and
;                   then exit.
;

        push   ax
        push   cx
        xor    cx, cx
        jmp    wfibe_check
retry:
        call   wait_100_micro      ;wait 100 microseconds
wfibe_check:
        in     al, 64h
        test   al, 02h             ;check input buffer full
        loopnz      retry
        pop    cx
        pop    ax
        ret

wfibe       endp

code    ends
        end



code    ends
        end
```

APPENDIX B
GET FLASH ID

```
get_flash_type          proc    near
;
;       Input:  Nothing
;
;       Output:         cy - set if not flash installed
;               All other registers preserved
;

        push    ax
        push    bx
        push    cx
        push    dx
        push    si
        call    get_flash_id            ;send read flash ID command,interpret
        mov     FlashType, al           ;save the Flash type code
        cmp     al, NO_FLASH
        je      bad_flash
        clc
        jmp     get_flash_exit
bad_flash:
        mov     bl, ErrorAttr           ;attribute of prompt
        mov     cx, NoFlashLen          ;display File read error
        mov     dh, NOFLASH_ROW         ;row position
        mov     dl, NOFLASH_COL         ;column position
        mov     si, offset NoFlashMsg
        call    put_string
        xor     ah, ah
        Int     16h
        stc
get_flash_exit:
        pop     si
        pop     dx
        pop     cx
        pop     bx
        pop     ax
        ret

get_flash_type          endp
```

```
get_flash_id  proc   near
;
;       Input: Nothing
;
;       Output:       al - flash memory space / ID types
;
;       Function:     Return code for Flash part types and memory
;                     map.  Possible codes specified in flash.inc
;

READ_ID_CMD_OLD_256 equ   080h
READ_ID_CMD_256           equ   090h
READ_ID_CMD_512           equ   090h
READ_ID_CMD_1024    equ   090h
MANU_CODE           equ   089h
ID_CODE_OLD_256           equ   0B1h
ID_CODE2_OLD_256    equ   0B2h
ID_CODE_256         equ   0B9h
ID_CODE_512         equ   0B8h
ID_CODE_1024        equ   0B4h

        push   di
        push   es
        mov    RmForDos, byte ptr FALSE ;default state
        call   raise_vpp          ;Set Vpp = 12 volts

;------------------------------;Tests for 128K of flash

        mov    ax, 0E000h         ;BIOS ROM segment
        mov    es, ax             ;E000:0000 is the address to test for
        xor    di, di             ;Two 512s or One 1024

;------------------------------;512 x 2 test

;The 512 x 2 test tests the high ROM.  This will prevent accidental
;mis-detection of a pair of 512K ROMs in systems that have only
;one 512K part, and memory accesses to E000 segment are mapped into
;the F000 segment.  This also allows an independent test for two 512K
;parts that are not odd-even byte interleaved.
;
        call   write_rom_enbl     ;enable write of command to ROM area
        mov    es:[di+1], byte ptr READ_ID_CMD_512
        call   word ptr Delay10Rout       ;wait 10 microseconds
        call   read_rom_enbl              ;enable read of results from ROM area
        mov    al, es:[di+1]      ;test at high ROM byte 0
        cmp    al, MANU_CODE              ;test for manufacturers code
        jne    test_one_1024
        mov    al, es:[di+3]      ;look at High ROM byte 1 for ID
```

```
        cmp     al, ID_CODE_512             ;test for part ID
        jne     test_one_1024
        mov     al, TWO_512         ;Found two 512s
        mov     RmForDos, byte ptr TRUE
        jmp     have_flash

;------------------------------;1024 x 1 test

test_one_1024:
        call    write_rom_enbl              ;enable write of command to ROM area
        mov     es:[di], byte   ptr READ_ID_CMD_1024
        call    word ptr Delay10Rout        ;wait 10 microseconds
        call    read_rom_enbl               ;enable read of results from ROM area
        mov     al, es:[di]
        cmp     al, MANU_CODE               ;test for manufacturer's code
        jne     test_64k_flash
        mov     al, es:[di+2]           ;look at offset 1 of chip 0
        cmp     al, ID_CODE_1024    ;test for part ID
        jne     test_64k_flash
        mov     al, ONE_1024                ;Found one 1024
        mov     RmForDos, byte ptr TRUE
        jmp     short have_flash

;------------------------------;Tests for 64K of flash only

test_64k_flash:
        mov     ax, 0F000h          ;BIOS ROM segment
        mov     es, ax              ;F000:0000 is the address to test for
        xor     di, di              ;TWO 256s or ONE 512

;------------------------------;256 x 2 test
;The 256 x 2 test tests the high ROM.  This allows an independent test
;for two 256K parts that are not odd-even byte interleaved.
;
        call    write_rom_enbl              ;enable write of command to ROM area
        mov     es:[di+1], byte ptr READ_ID_CMD_256
        call    word ptr Delay10Rout        ;wait 10 microseconds
        call    read_rom_enbl               ;enable read of results from ROM area
        mov     al, es:[di+1]           ;test at high ROM byte 0
        cmp     al, MANU_CODE               ;test for manufacturers code
        jne     test_one_512
        mov     al, es:[di+3]           ;look at High ROM byte 1 for ID
        cmp     al, ID_CODE_256             ;test for part ID
        jne     test_one_512
        mov     al, TWO_256         ;Found two 256s
        jmp     short have_flash
```

```
;------------------------------;512 x 1 test
test_one_512:
        call    write_rom_enbl              ;enable write of command to ROM area
        mov     es:[di], byte ptr READ_ID_CMD_512
        call    word ptr Delay10Rout        ;wait 10 microseconds
        call    read_rom_enbl               ;enable read of results from ROM area
        mov     al, es:[di]
        cmp     al, MANU_CODE               ;test for manufacturer's code
        jne     test_two_old_256
        mov     al, es:[di+1]           ;look at offset 1 of chip 0
        cmp     al, ID_CODE_512             ;test for part ID
        jne     test_two_old_256
        mov     al, ONE_512             ;Found one 512
        jmp     short have_flash
;------------------------------;Old 256 x 2 test
test_two_old_256:
        call    write_rom_enbl              ;enable write of command to ROM area
        mov     es:[di], byte ptr READ_ID_CMD_OLD_256
        call    word ptr Delay10Rout        ;wait 10 microseconds
        call    read_rom_enbl               ;enable read of results from ROM area
        mov     al, es:[di]
        cmp     al, MANU_CODE               ;test for manufacturer's code
        jne     not_two_256
        mov     al, es:[di+2]           ;look at offset 1 of low ROM
        cmp     al, ID_CODE_OLD_256             ;test for part ID
        je      is_two_256
        cmp     al, ID_CODE2_OLD_256    ;test for 2nd possible part ID
        jne     not_two_256
is_two_256:
        mov     al, TWO_OLD_256             ;Found two 256s
        jmp     short have_flash
not_two_256:
        mov     ah, al                  ;debugging code
        mov     al, NO_FLASH
have_flash:
        call    write_rom_enbl              ;enable write of command to ROM area
        mov     es:[di], byte ptr READ_MEM_CMD      ;Allow memory read
        call    lower_vpp               ;Clear Vpp
        pop     es
        pop     di
        ret

get_flash_id    endp
```

APPENDIX C
CALIBRATION TIMERS

```
;*****************************************************************************
;
;       Timer.asm - Timer utilities for flash.com
;
;
;       Included in this file are:
;
;       rpt_1_milli     - execute 1 millisecond delay "cx" times
;       wait_1_milli    - wait 1 millisecond and exit
;       wait_100_micro      - wait 100 microseconds and exit
;       wait_10_micro       - wait 10 microseconds and exit, loop version
;       wait_10_micro2      - wait 10 microseconds, push/mov r,m/pop/ret
;       wait_10_micro3      - wait 10 microseconds, push/pop/ret
;       wait_10_micro4      - wait 10 microseconds, ret only
;       calc_spd10      - calibrate 10 microsecond loop
;       calc_spd100     - calibrate 100 microsecond loop
;       try_calb        - test 10 or 100 microsecond loop
;       beep_spkr       - beep the speaker

TRUE            equ     1
FALSE           equ     0

Include         Flash.inc       ;flash utility specific equates

code    segment byte public 'code'
        assume          cs:code

PUBLIC      calc_spd10, calc_spd100, wait_100_micro, wait_1_milli, beep_spkr PUBLIC
rpt_1_milli

TICKS           equ     175     ;ticks in 100 microseconds
PIT_MODE    equ     43h     ;Timer 0, Timer 2 control register
PIT0_CNT    equ     40h     ;Timer 0 count register
PIT2_CNT    equ     42h     ;Timer 2 count register
SYS_PORT_A      equ     61h     ;System Control Port A

PUBLIC      Delay10Rout
DELAY_ROUT_MAX      equ     3
Delay10Rout dw      ?       ;Routine used for delaying 10 microseconds
DelayRoutNum        dw      ?       ;Index into table of delay routines
DelayRoutTbl        dw      wait_10_micro
                dw      wait_10_micro2
                dw      wait_10_micro3
                dw      wait_10_micro4
DelayCnt10  dw      ?
DelayCnt100 dw      ?
CalbLoopSiz dw      ?
```

```
rpt_1_milli    proc    near
;
;       Input:  cx - number of times to wait 1 millisecond
;
;       Output:         All registers preserved
;
;       Function:       Do nothing for a period equal to 1 millisecond
;                       times the repeat count in cx.
;

        push    cx
loop_1_milli:
        call    wait_1_milli  ;wait 1 millisecond
        loop    loop_1_milli
        pop     cx
        ret

rpt_1_milli    endp

wait_1_milli   proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Wait 1 millisecond and then exit
;

        push    cx
        mov     cx, 10
loop_100_micro:
        call    wait_100_micro      ;wait 100 microseconds
        loop    loop_100_micro
        pop     cx
        ret

wait_1_milli   endp
```

```
wait_100_micro      proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Wait 100 microseconds and then exit. Uses a purely
;                       software delay loop. The initial value of the
;                       delay loop is stored in the variable DelayCnt100.
;
        push    cx
        mov     cx, DelayCnt100
self100:
        loop    self100
        pop     cx
        ret

wait_100_micro      endp

wait_10_micro       proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Wait 10 microseconds and then exit. Uses a purely
;                       software delay loop. The initial value of the
;                       delay loop is stored in the variable DelayCnt10.
;

        push    cx
        mov     cx, DelayCnt10
self:
        loop    self
        pop     cx
        ret

wait_10_micro       endp
```

```
wait_10_micro2      proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Wait 10 microseconds and then exit.  Uses only
;                       some instructions to kill time.
;

        push    cx
        mov     cx, DelayCnt10
        pop     cx
        ret

wait_10_micro2      endp

wait_10_micro3      proc    near
;
;       Input:  Nothing
;
;       Output:         All registers preserved
;
;       Function:       Wait 10 microseconds and then exit.  Uses only
;                       some instructions to kill time.
;

        push    cx
        pop     cx
        ret

wait_10_micro3      endp
```

```
calc_spd100   proc    near
;
;       Input: Nothing
;
;       Output:         All registers preserved
;
;       Function:       Attempt to calculate the loop count by testing
;                       different values for the loop delay for a 100
;                       microsecond wait routine.
;

        push    ax
        push    bx
        push    si
        mov     CalbLoopSiz, word ptr 10    ;10 * 100 = 1000
        mov     DelayCnt100, byte ptr 100   ;try 100 first
        mov     si, offset wait_100_micro
        mov     Delay10Rout, si
retry_calb100:
        call    try_calb            ;see what delay cnt value is returned       cmp    bx,
2350            ;see if its too low
        jbe     inc_delay100        ;if so increment delay value
        cmp     bx, 2750            ;see if its too high
        jae     dec_delay100        ;if so decrement delay value
        jmp     delay100_cnt_set
inc_delay100:
        inc     byte ptr DelayCnt100
        jmp     retry_calb100
dec_delay100:
        cmp     DelayCnt100, byte ptr 1     ;see if we bottomed out
        je      delay100_cnt_set
        dec     byte ptr DelayCnt100
        jmp     retry_calb100
delay100_cnt_set:
        pop     si
        pop     bx
        pop     ax
        ret

calc_spd100   endp
```

```
calc_spd10    proc    near
;
;       Input:  Nothing
;
;       Output:         ax - loop count for 10 microsecond delay
;
;       Function:       Attempt to calculate the loop count by testing
;                       different values for the loop delay for a 10
;                       microsecond wait routine.
        push    ax
        push    bx
        push    si
        mov     CalbLoopSiz, word ptr 100  ;100 * 10 = 1000
        mov     DelayCnt10, byte ptr 20    ;try 20 first
        mov     DelayRoutNum, word ptr 0   ;start with loop routine
        mov     si, offset wait_10_micro   ;start with standard routine   mov    Delay10Rout, si
retry_calb:
        call    try_calb                ;see what delay cnt value is returned          cmp    bx,
2200            ;see if its too low
        jbe     inc_delay               ;if so increment delay value
        cmp     bx, 2600                ;see if its too high
        jae     dec_delay               ;if so decrement delay value
        jmp     delay_cnt_set
inc_delay:
        inc     byte ptr DelayCnt10
        jmp     retry_calb
dec_delay:
        cmp     DelayCnt10, byte ptr 1          ;see if we bottomed out
        je      delay_rout_chg
        dec     byte ptr DelayCnt10
        jmp     retry_calb
delay_rout_chg:
        inc     word ptr DelayRoutNum
        mov     ax, DelayRoutNum
        cmp     ax, DELAY_ROUT_MAX
        ja      delay_cnt_set
        shl     ax, 1                   ;convert to word index
        mov     si, offset DelayRoutTbl
        add     si, ax
        mov     si, [si]                ;fetch new delay routine offset
        mov     Delay10Rout, si                 ;put in standard vector
        jmp     retry_calb
delay_cnt_set:
        pop     si
        pop     bx
        pop     ax
        ret
calc_spd10    endp
```

```
try_calb        proc    near
;
;       Input:  Nothing
;
;       Output:         bx = elapsed timer count
;               all other registers preserved
;
;       Function:       Test current delay routine for 10 microseconds
;                       and see how many time ticks go by when it is called
;                       10 times.  Return timer tick count in bx.

        push    ax
        push    cx
        cli                     ; Disable Ints
try_calb1:
        mov     cx, CalbLoopSiz         ;count out 1 millisecond delay
        xor     al, al          ; Set counter latch for 8254
        out     43h, al
        WaForIo
        in      al, 40h                 ;Read high byte
        mov     ah, al
        WaForIo
        in      al, 40h                 ;Read low byte
        xchg    ah, al
        mov     bx, ax          ;save count
try_calb2:
        call    word ptr Delay10Rout
        loop    try_calb2
        xor     al, al          ; Set counter latch for 8254
        out     43h, al
        WaForIo
        in      al, 40h
        mov     ah, al          ;Read low byte
        WaForIo
        in      al, 40h                 ;Read high byte
        xchg    ah, al
        sub     bx, ax          ;Check for rollover
        jnc     calb_exit       ;Return, if no rollover
        jmp     try_calb1       ;otherwise, repeat
calb_exit:
        sti
        pop     cx
        pop     ax
        ret

try_calb        endp
```

```
beep_spkr   proc   near          ;Make a sound at the speaker
;
;       Input: Nothing
;
;       Output:     All registers preserved

TIME_K_HI  equ   18                    ;Timer time constant
TIME_K_LO  equ   12772
FREQUENCY       equ   2000                    ;Hertz

        push   ax
        push   cx
        push   dx
        mov    al, 0B6h          ;notify 8253 that freq. data coming      out    PIT_MODE, al
        mov    dx, TIME_K_HI
        mov    ax, TIME_K_LO
        mov    cx, FREQUENCY
        div    cx                ;count = 1,193,280 / frequency
        out    PIT2_CNT, al              ;send low byte
        mov    al, ah            ;prepare high byte
        out    PIT2_CNT, al
        in     al, SYS_PORT_A            ;activate speaker
        or     al, 003h          ;1 to low two bits
        out    SYS_PORT_A, al
        mov    cx, 0A00h         ;time delay for sound
beep1:
        call   wait_10_micro             ;10 us delay
        loop   beep1

        in     al, SYS_PORT_A            ;deactivate speaker
        and    al, 0FCh          ;0 to low two bits
        out    SYS_PORT_A, al
        pop    dx
        pop    cx
        pop    ax
        ret

beep_spkr   endp

code    ends
        end
```

APPENDIX D
MS-DOS ROM VERSION OVERVIEW

Technical Highlights (Taken from Microsoft Product Overview)

Ram Economy

Because MS-DOS Rom Version executes from ROM, only 15KB of system RAM space is required for MS-DOS. For a typical user, this will result in a savings of about 40KB of RAM over disk-based MS-DOS. As a result of this savings, the user is able to run more programs and work with larger data files with the ROM Version than with disk-based MS-DOS.

Instant-On

MS-DOS ROM Version provides a significant reduction in "boot time," or the amount of time it takes from the completion of the power-on self test until a DOS prompt appears. With the ROM Version, this typically takes one second.

No End-User Installation

MS-DOS ROM Version is pre-installed by the OEM (original equipment manufacturer) in the system, thus freeing end users from the task of installing MS-DOS.

Adaptable to OEM Hardware Platforms

MS-DOS ROM Version is structured such that it allows the OEM to include a specific routine to determine which drive to boot from and any specific parameters if booting from the ROM drive. This makes it possible to easily port the ROM Version to a wide variety of hardware environments. MS-DOS ROM Version is also positioned independent, in that it can reside anywhere in the "reserved" space (the area between 640KB and 1MB). This provides an additional level of flexibility in allowing the OEM to adapt MS-DOS ROM Version to the specific requirements of the OEM's hardware platform.

ROM Economy

MS-DOS ROM Version occupies only 62 KB of ROM space, thus minimizing the amount of ROM that an OEM must include in the system. Three modules reside in the reserved space Command.com, IO.sys and the DOS Kernel. All three are position independent, so an OEM can decide where to place these modules in the reserved area.

National Language Support

Microsoft offers a full compliment of localized version of MS-DOS ROM Version, including Kanji and Chinese translations.

Ease of Development

As PCs become the engines for many embedded applications, manufacturers would like to develop new applications utilizing existing PC software tools. MS-DOS ROM allows manufacturers to take full advantage of these tools. For instance, a programmer can develop and debug an application onto a PC subsystem which may be embedded into a larger system. This benefit translates into a cost savings when developing a solution for vertical markets.

October 1990

Solutions for High Density Applications Using Intel Flash Memory

MARKUS A. LEVY
DALE ELBERT
APPLICATIONS ENGINEERING
INTEL CORPORATION

Order Number: 292079-001

Solutions For High Density Applications Using Intel Flash Memory

CONTENTS

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INTRODUCTION

Mass storage encompasses many different technologies. Though commonalities exist, mass storage strives for nonvolatility, low cost per bit, and high density. Disk drives provide the best known example. However, many environments now require higher performance and reliability with lower power consumption, even at the expense of capacity. Flash memory uniquely meets these demands.

Flash memory can be used as a mass storage medium in applications including factory automation, notebook computers, high-end workstations, point of sale terminals, and data acquisition systems. Even desktop computers benefit from solid-state storage. The motivation to incorporate flash memory in any of these applications becomes obvious to the system designer who understands flash memory's benefits and density projections.

In an effort to understand these benefits, this document includes both conceptual and application oriented discussions. These discussions will be kept to a minimum with the real focus being on specific design techniques and considerations.

ADVANCED PACKAGING

Mass storage is synonymous with high density. Disk drives have increased the bit density of the rotating media via material improvements and closer tolerances. For semiconductors, density requires advanced packaging as well as higher capacity silicon (improved photolithography). Intel's Flash Memory devices are based on the company's EPROM Tunnel Oxide (ETOX™) technology that enables the high degree of scaling required to achieve high density.

Intel offers the high density flash memories in several package types. The standard packages are the **P**lastic **D**ual **I**n-line **P**ackage (PDIP), the **P**lastic **L**eaded **C**hip **C**arrier (PLCC), and the **T**hin **S**mall **O**utline **P**ackage (TSOP). Advanced modular packaging in the form of **S**ingle **I**n-line **M**emory **M**odules (SIMM) and IC memory cards (small enough to fit in your shirt pocket), provide the total solution.

Which package would be best for your application?

Plastic Leaded Chip Carrier (PLCC)

The engineer striving to reduce board space is already using surface-mounted technology, such as PLCC. The PLCC is seen frequently on PC add-in cards and motherboards. Compared to the DIP, PLCC uses as little as 35% the overall board space. Its small size, compared to the DIP, is attributed to the terminal center-to-center spacing—50 mils versus 100 mils—as well as its four-sided pinout. No drilling or lead-cutting is necessary as leads are soldered directly to pads on the circuit board. The PLCC's 50-mil pad pitch is compatible with most circuit board manufacturing equipment. Additionally, components can be mounted on both sides of the board. However,the four-sided PLCC generally requires the use of a multi-layered board to lay out conductor traces for maximum compaction.

Thin Small Outline Package (TSOP)

When overall space constraints are critical, the TSOP is the best choice. This is best exemplified by IC memory cards. Low height is the key attribute of the TSOP, measuring 1.2 mm versus 3.5 mm for the PLCC. (Mechanical drawings in Appendix.) State-of-the-art center-to-center terminal spacing of 0.5 mm yields a smaller package and narrower conductor traces than the PLCC or DIP. In comparison, the volume of the TSOP is 172.8 mm^3 versus 656.3 mm^3 for the PLCC and 1872.3 mm^3 for the DIP.

The TSOP is available in standard and reverse pin configurations (Figure 1). Pins are located on only two ends of the package. This approach simplifies trace layout while reducing the number of board layers because traces can be routed out the non-leaded sides of the devices. Very dense board layouts are accommodated because components can literally be laid out end-to-end and side-by-side. Figure 2 displays an optimal layout best utilizing the TSOP's attributes. The close spacing allows one bypass capacitor to be used for two devices (provided they are not simultaneously selected). This optimal component layout can be mirror-imaged through the board to easily double the memory capacity.

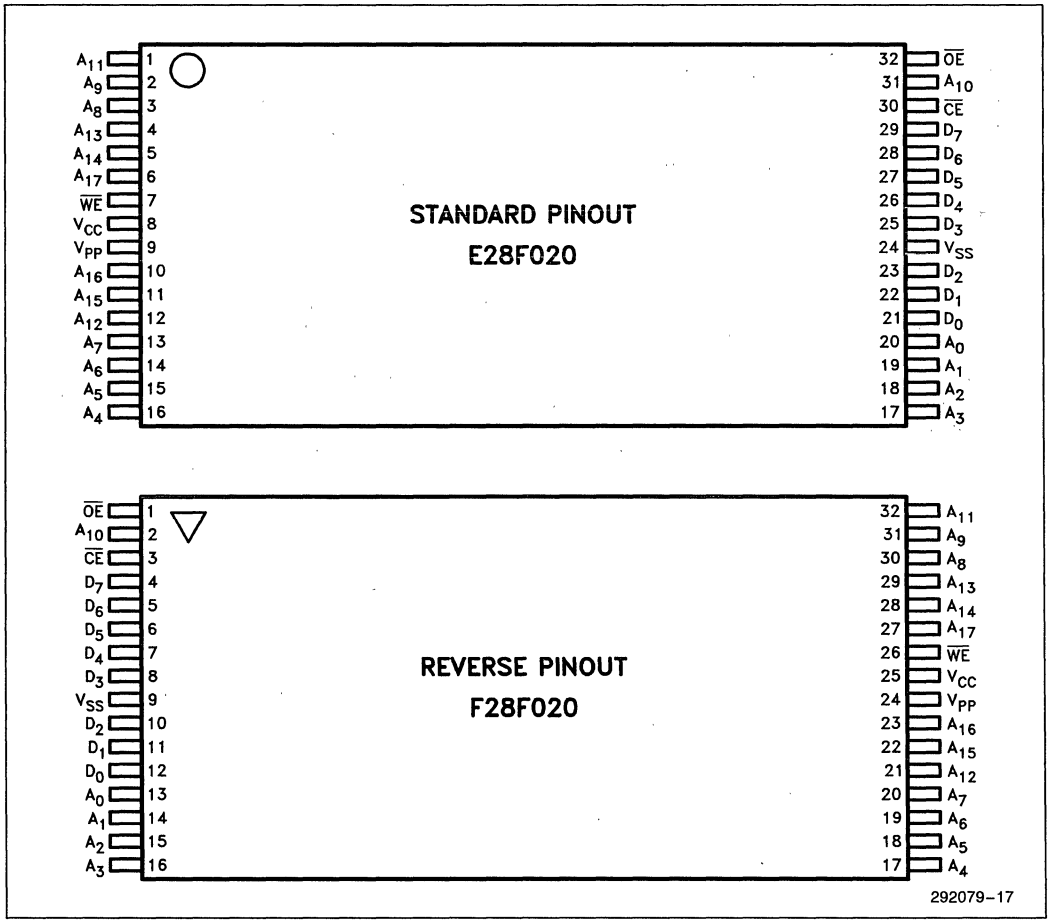

Figure 1. 28F020 32-Lead TSOP—Standard and Reverse Pinouts

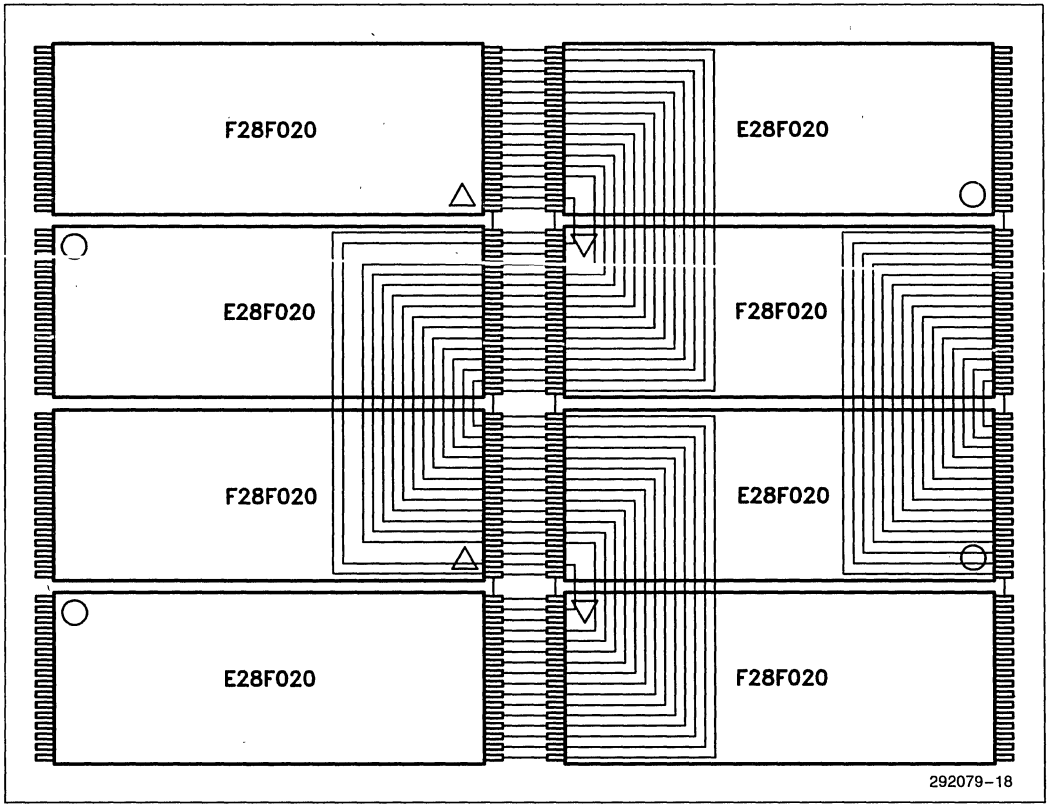

Figure 2. TSOP Optimal Layout: Highest Density Configuration

Single In-Line Memory Module (SIMM)

The SIMM is optimal where minimized board space and upgrade capability are required. Compared to using 8 discrete PLCCs plus capacitors (3019.4mm^2), the equivalent memory capacity SIMM (926.1mm^2) consumes 70% less motherboard real estate.

The Intel Flash Memory SIMM is an 80-pin, 0.050 mil centerline lead spaced, insertable module designed with a 16-bit wide data bus interface. Intel's SIMM pin configuration allows convenient implementation:

- No Address or Data Bus Multiplexing—RAS# and CAS# are not needed;
- Reserved Pins—For product expansion and enhancements: Upgrade capability to 128 Mbytes;
- Presence Detect Eliminates Jumpering—Simplifies user installation.

The 80-pin definition of the flash memory SIMM includes 7 pins for Presence Detect (PD). (See Appendix or SIMM Data Sheet.) The PD pins are read to determine module memory capacity and speed of the devices. The PD pins are either Open circuit or Shorted to ground. By attaching a pull-up resistor to each pin, Open circuits will read as a binary 1 and Shorts as a binary 0. Before implementing the presence detect feature, define your system criteria:

How many modules will be used?

Decide how much total memory your system is to contain. The limit is dictated by the space available, as well as cost.

Flash memory SIMMs can easily accommodate different memory capacities and speeds. Could your system handle mismatched SIMMs?

There are two basic design implementations for interpreting presence detect information. The first approach requires that matching SIMMs are used. The PD pins of all SIMMs are tied to one transceiver that is read as an I/O port (Figure 3).

Invalid reads occur if the user installs mismatched SIMM configurations. Any PD pin shorted to ground makes an open circuit pin appear as a binary zero (0). Mixing module speeds is acceptable, but the PD pins reflect the slower module.

The second approach, allowing any mixture of flash SIMMs, requires more hardware and software for interpretation. The PD pins from each SIMM have separate transceivers, resistors, and I/O ports (Figure 4). Flexibility is increased at the expense of board real estate.

Assume your system accommodates several SIMMs but complete population is not needed. Can the system handle empty sockets?

SIMM upgrade capability is not limited to increases in memory density. A system may be designed with several SIMM sockets on the circuit board. To keep initial end-customer costs down, the system ships with only one SIMM installed. This provides the option of populating the empty sockets at a later time. The PD pins are designed to eliminate jumper or software setups by the end-user when SIMM upgrades are made.

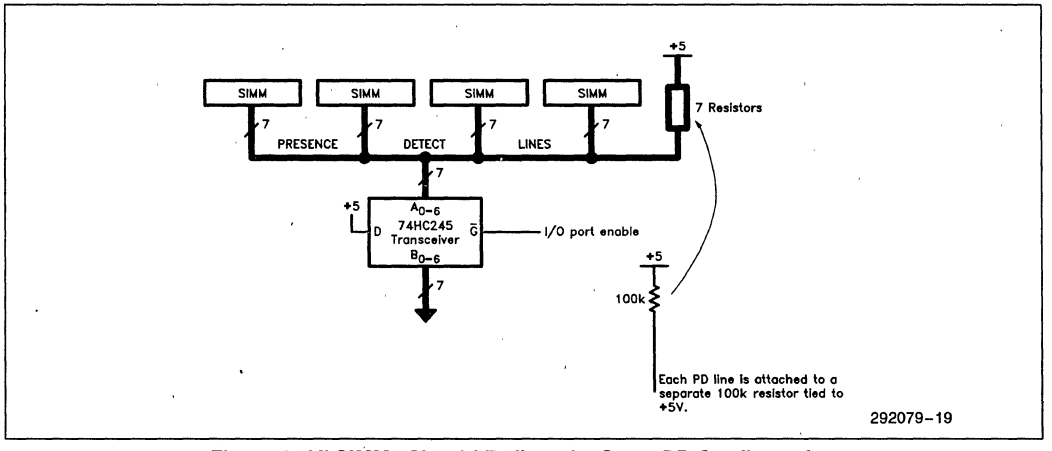

Figure 3. All SIMMs Should Reflect the Same PD Configuration

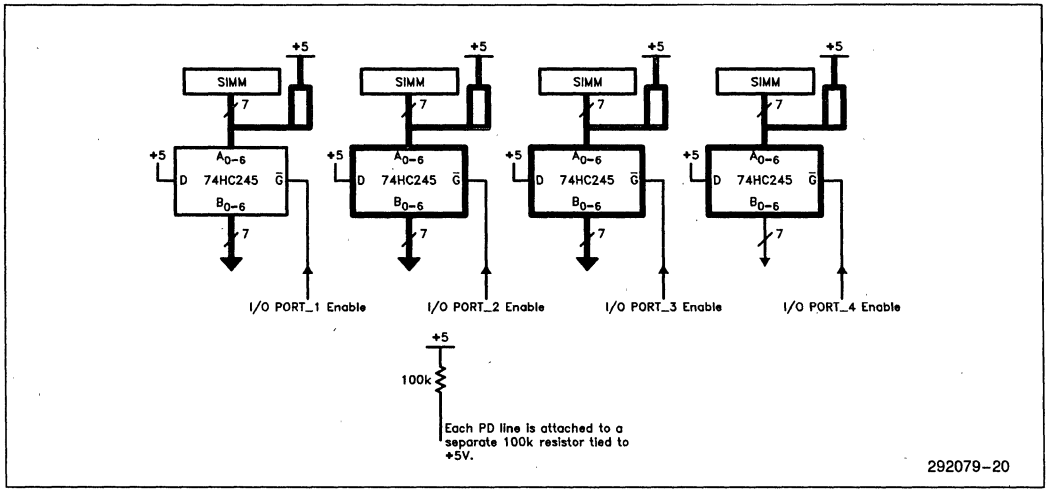

Figure 4. Multiple I/O Transceivers Are Needed if Mismatched SIMMs Are Used

Using the previous scenario, will it matter which socket is used? In other words, what is the installation procedure?

With respect to the PD feature, it does not matter which sockets are full. (However, most designers request that sockets are filled in sequential order to minimize hardware and softwear requirements.) To explain this, look again at the bit-level interpretation of the PD pins. An empty socket also appears as an open circuit. Your software can determine a full (or empty) socket in one of two ways:

Method One (Figure 3)—Reading the PD pins is insufficient. An empty socket will reflect the value of the full socket. Your software will have to read the chip level device identifier hardwired in each flash memory device. (See Intel Flash Memory data sheets regarding int$_e$ligent™ identifiers.) Reading an invalid device identifier from a SIMM address signifies an empty socket. Software demonstrating the use of this method to determine memory capacity is discussed further in the section on "Verifying Paged Memory Board Functionality".

Method Two (Figure 4)—Each SIMM's PD pins are read separately. Reading all ones (the result of all Open circuits) signifies an empty socket. The chip level device identifiers should still be read to establish the number of flash memory devices on the SIMM.

Presence Detect for WAIT-State Interpretation

Using Method One or Method Two from above, the device speed information is read from the pins. This information can be interpreted by software to issue the proper command to the system's programmable WAIT-state generator. By guaranteeing the use of matching SIMMs, the WAIT-state generator would not have to be reprogrammed each time a different SIMM is accessed.

A hardware driver alternative implements an 85C220 EPLD configured with an internal counter (Figure 5). The rising edge of the clock, following Chip Enable going active, latches the count value derived from the PD speed pins (Figure 6).

Each subsequent rising edge of the clock input decrements the counter. A $\overline{\text{READY}}$ signal is output to the CPU (or the system's READY logic circuitry) when the count reaches zero (0). The $\overline{\text{READY}}$ signal remains active until LOAD (Chip Enable, $\overline{\text{CE}}$) goes inactive at the completion of the bus cycle.

The clock signal for the internal EPLD counter is derived directly from the CPU, therefore the count rate and WAIT-states will be system dependent. An EPLD Advanced Design File was generated to demonstrate this application. (See Appendix A.) This is a straightforward approach until designing systems, such as power-saving laptops, that have changeable system clock rates.

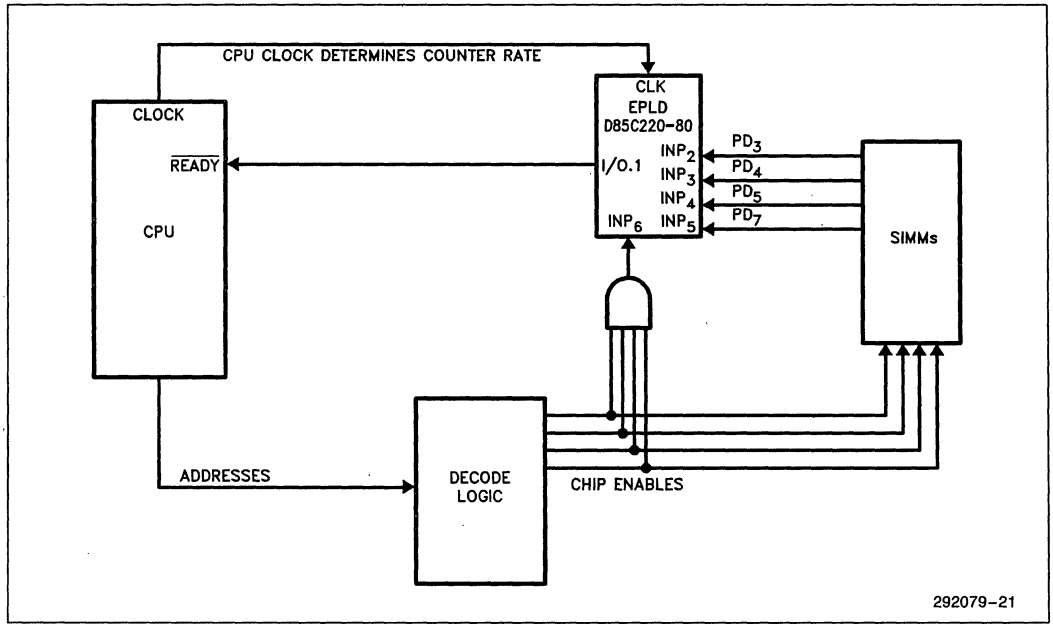

Figure 5. WAIT-State Generator Using an EPLD Configured as a Counter

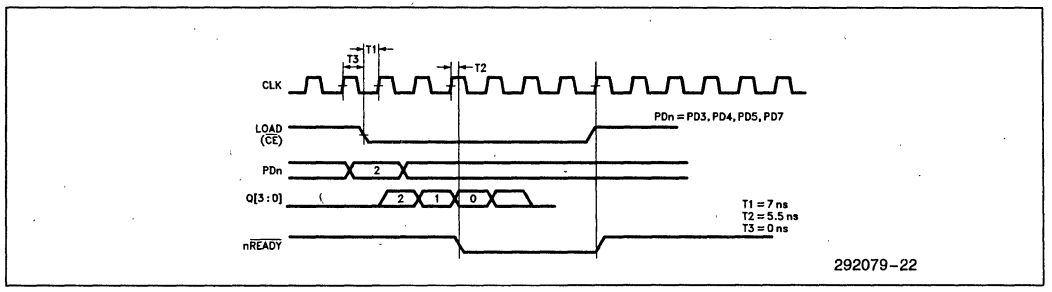

Figure 6. Timing for SIMM Presence Detect WAIT-State Generator

Memory Cards

Many laptop and notebook computer manufacturers are pursuing the IC memory card to incorporate a removable mass storage medium. This is an ideal application for the Intel Flash Memory TSOP, due to the package's minimal height.

Solid-State Memory Alternatives

ROM and SRAM are currently the dominant IC card memory technologies. ROM has the advantage of being inexpensive, but is not changeable. When newer software revisions (e.g. Lotus* 123, Wordstar**, etc.) are available, the user must buy a new ROM card for each upgrade. Intel Flash Memory's reprogrammability minimizes the user's expense and the OEM's inventory risk.

SRAM is reprogrammable but batteries are required to maintain data, risking data loss. Like magnetic disks, flash memory is truly nonvolatile and thus has virtually infinite storage time with power off (10 years minimum, 100 years typical). Additionally, SRAM is expensive and not a high density solution. Intel Flash Memory provides a denser, more cost effective and reliable solution.

System level cost is about the same for Intel Flash Memory and SRAM + battery—

Flash memory requires 12V for programming and erasing. If a 12V supply is not available, 5V can easily be boosted. (See Application Note AP-316.) SRAM + battery requires battery state detect circuitry.

Card level cost differences are substantial (Figure 7)—

SRAM must have a battery to retain data. It also requires a V_{CC} monitor and Write Lockout circuitry. Intel's Flash Memory only requires Write Lockout circuitry (switching V_{PP} to 0V is an alternative write protect). This leads to increased area for memory components. More importantly, Intel's Flash Memory density is 4 times that of static RAM, yielding for lower cost per bit.

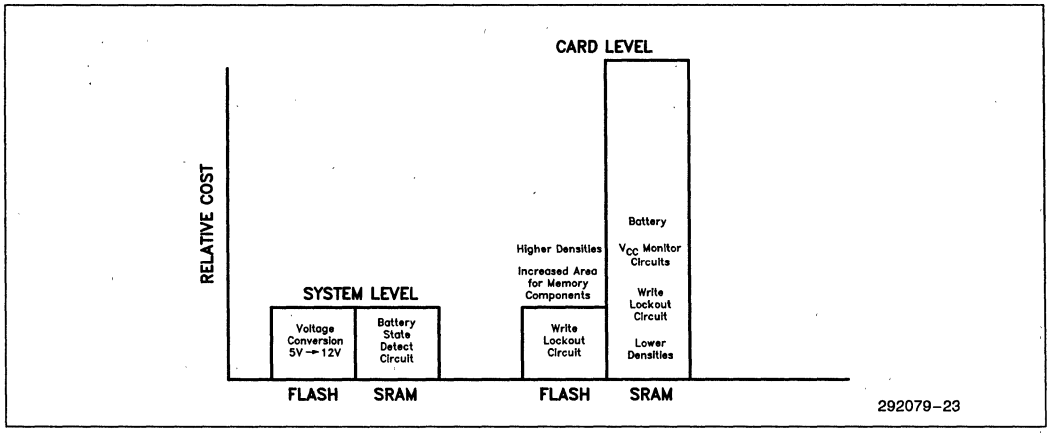

Figure 7. Support Circuitry Cost Comparison

*LOTUS® is a registered trademark of LOTUS Development Corporation.
**WORDSTAR® is a registered trademark of MICROPRO.

Designing a PCMCIA/JEIDA Standard Memory Card

Choosing among IC card design options depends on card architecture (standardization), memory capacity, data bus width, card intelligence, V_{PP} generation, and reliability.

What are the advantages of a standardized memory card pinout?

From the computer system's viewpoint, a standardized pinout enables the use of multiple third-party memory cards. This ensures competitive pricing and wide availability. From the memory card point of view, standardization allows use in a variety of systems.

The Personal Computer Memory Card International Association/Japan Electronic Industry Development Association (PCMCIA/JEIDA) 68-pin format is the emerging IC memory card standard. Several proprietary formats are also available from their respective manufacturers, but these same manufacturers now offer PCMCIA/JEIDA versions. The PCMCIA/JEIDA standard specifies physical, electrical, information structure, and data format characteristics of the card. This standard accommodates either 8- or 16-bit data bus widths.

The following 2 Mbyte memory card design provides a byte-addressable interface using 8-28F020s (2 Mbit, 256k x 8 devices) as shown in Figure 8. While TTL equivalent interfacing is shown, most cards will use gate arrays to reduce chip count. Address lines A18 and A19 are decoded with a 2-to-4 decoder (74HC139) to generate high and low byte chip select signals for each of the 4 pairs of flash memory devices (one pair = high and low byte). The PCMCIA/JEIDA format specifies inputs $\overline{CSL}$ and $\overline{CSH}$ (along with the A0 address line) which select the low and high byte, respectively.

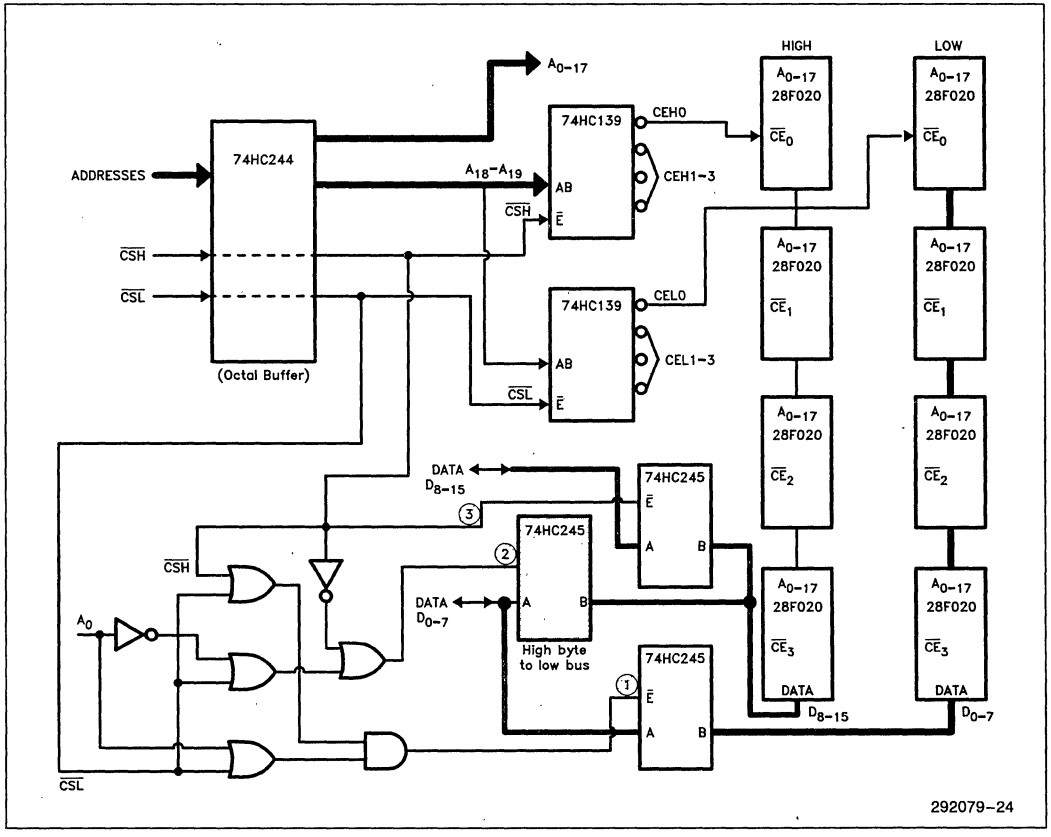

Figure 8. Decoding for PCMCIA/JEIDA Standard Bus Interface

According to the PCMCIA/JEIDA standard, the memory card is designed with the flexibility to have both an 8-bit or a 16-bit interface, dependent upon the machine it is plugged into. When the memory card is plugged into an 8-bit system, the high byte transceiver is multiplexed to the low byte of the system. In Figure 8, the highlighted transceiver (#2), maps the upper byte to the lower byte of the data bus (i.e., D_{8-15} to D_{0-7}). Signals are decoded according to the truth table in the Appendix. (1, 2, and 3 denote transceiver numbers of Figure 8.)

One can double the memory capacity and select from among 8 pairs of flash memory devices by using a 3 to 8 decoder with inputs A_{18-20}. Notice that additional transceivers are not needed to support the additional data fanout. (See section on capacitive loading.)

HARDWARE DESIGN IMPLEMENTATIONS

Paged, linear, and I/O are the three fundamental addressing methods that can be used for accessing an array of memory devices. Linear addressing offers the fastest and most direct access to a memory array. It consumes the largest portion of the system's memory and is only practical in a 386™ microprocessor (or other 32-bit processor) family system because of the large memory space available above 1 Mbyte. The I/O mapped memory array consumes the smallest amount of the system address space but has the lowest performance. A page-mapped memory array, also called a sliding AT window, is a hybrid of the linear and I/O designs. The memory array is usually very large relative to the system interface, consisting of pages typically ranging in size from 8 Kbytes to 64 Kbytes. (LIM-EMS use four to twelve 16 Kbyte pages.)

Design Example—A Paged-Mapped Memory Board

A paged design employs addressing techniques similar to the Lotus-Intel-Microsoft expanded memory specification (LIM-EMS). It allows access to one or more sections (or pages) of the flash memory array at a time. This minimal interface is particularly useful within the DOS 1 Mbyte memory space. The DOS map (Figure 9) shows 128 Kbytes of memory space available in the Optional I/O Adapter ROM area. LIM-EMS, LAN, the flash memory design discussed in the following sections, and other accessory cards can use this area.

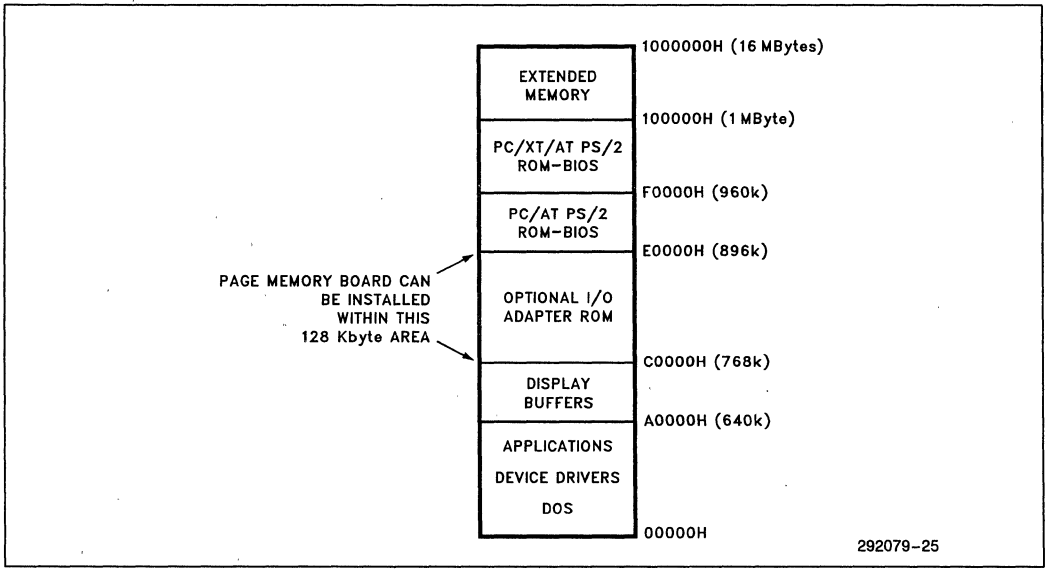

Figure 9. DOS Memory Map

Figure 10 shows the block diagram of the page-mapped flash memory board design. (Except for the addressing method, all the functional components of this board could be used on a linear or I/O mapped flash memory array.) This PC-AT*** compatible design example consists of a flash memory array (using SIMMs) and the corresponding memory and I/O decoding, V_{PP} generation, and the interface to the system bus. (Component numbers shown with the following diagrams correlate with the actual schematics in the appendix.) A page size of 64 Kbytes is used. Depending on the system's configuration, memory contention may require a smaller page size. (Note that the LIM EMS 4.0 standard uses 4 contiguous 16 Kbyte pages. Multiple pages can exist as space permits.)

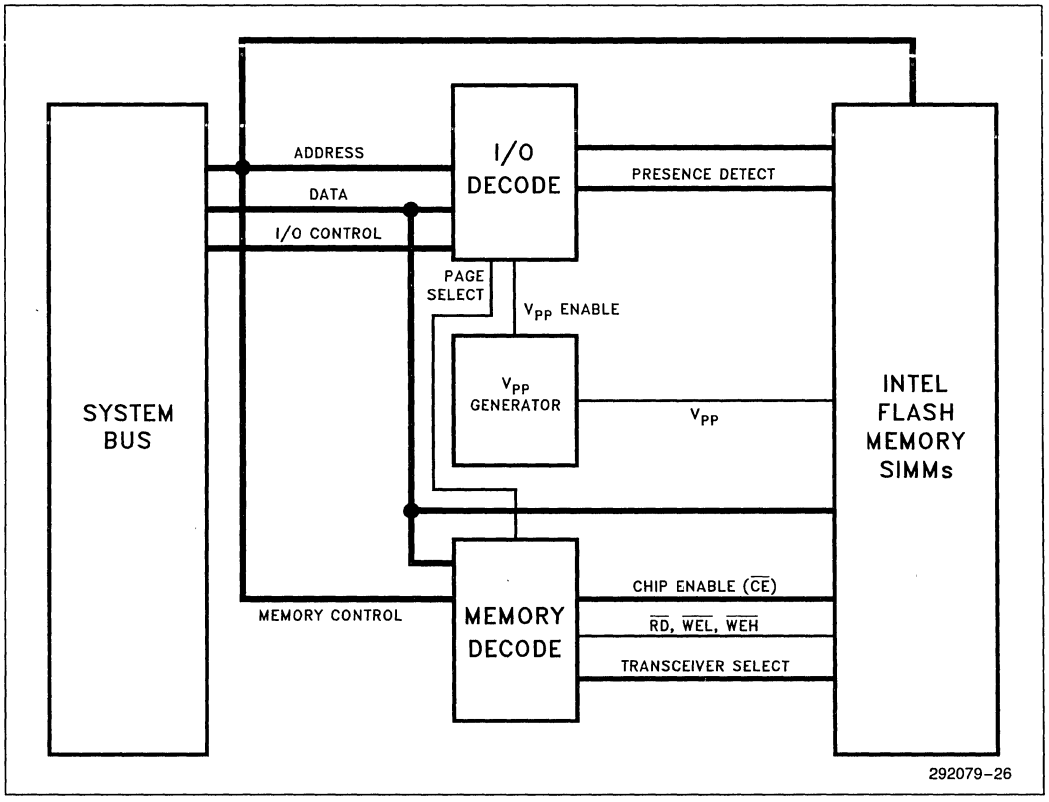

Figure 10. Page-Mapped Flash Memory Board

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***PC-AT® is a registered trademark of International Business Machine Corporation.

The Decoding Scheme

The Intel Flash Memory on this board is installed in 4 SIMM sockets. With a fully populated board, the memory capacity ranges from 4 Mbytes to 16 Mbytes depending on the SIMM density used.

Depending on the density, up to eight chip enables, $\overline{CE}_0$–$\overline{CE}_7$, are used on a SIMM (4 $\overline{CE}$s for 8-chip, 8 $\overline{CE}$s for 16-chip SIMMs). Standard decoding techniques generate separate chip enables, output enables, and write enables. This method has the disadvantage of having to accommodate a large number of traces. The addressing scheme incorporated in this design minimizes the number of board traces neeed to select individual devices. Device selection is made on a row-column basis where: rows are Output Enables ($\overline{OE}$s), Write Lows ($\overline{WRL}$s), and Write Highs ($\overline{WRH}$s) and columns are Chip Enables ($\overline{CE}$s). (For low-powered systems, this method may be unacceptable because each chip enable activates a maximum of 8 components.) These signals are generated by decoding the page lines P_3–P_7 (Figure 11, U22). (See Page Number section.) Pages within a component are selected by tying P_0, P_1 and P_2, respectively, into pins 37 (A_{15}), 36 (A_{16}), and 35 (A_{17}) on the SIMM (Pin 35 on the iSM001FLKA is a no-connect (NC)).

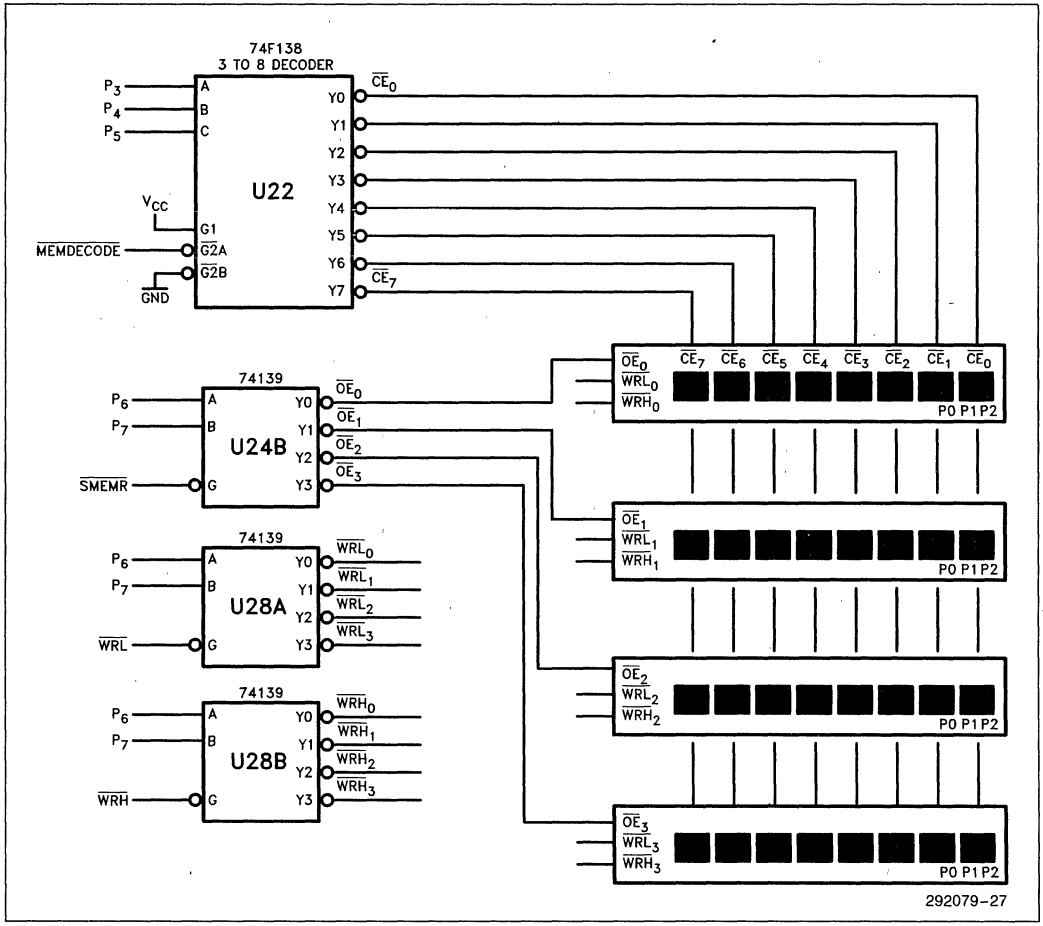


Figure 11. Individual Components Selected by Row-Column Addressing Saves Board Traces

Planning for upgrades also presents another interesting situation. The iSM001FLKA (1 Mbyte SIMM) has four chip enables ($\overline{CE_0}$–$\overline{CE_3}$), one for each pair of components. The pair of components represent high and low bytes and are selected by $\overline{WRH}$ and $\overline{WRL}$, respectively.

The iSM001FLKA represents sixteen 64-Kbyte pages (eight 128-Kbyte components). To accommodate upgrade capability, pages within the iSM001FLKA will not be contiguous because a "4-page hole" exists every 4 pages (P2 is attached to a no connect). To overcome this rearrange the page select lines with jumpers (Figure 12):

1 Mbyte	SIMM	[(iSM001FLKA)	8 * 28F010s]	JP2, JP4, JP6, JP8
2 Mbyte	SIMM	(16 * 28F010s)		JP2, JP3, JP7, JP9
2 Mbyte	SIMM	(8 * 28F020s)		JP1, JP3, JP5, JP7
4 Mbyte	SIMM	(16 * 28F020s)		JP2, JP3, JP6, JP7

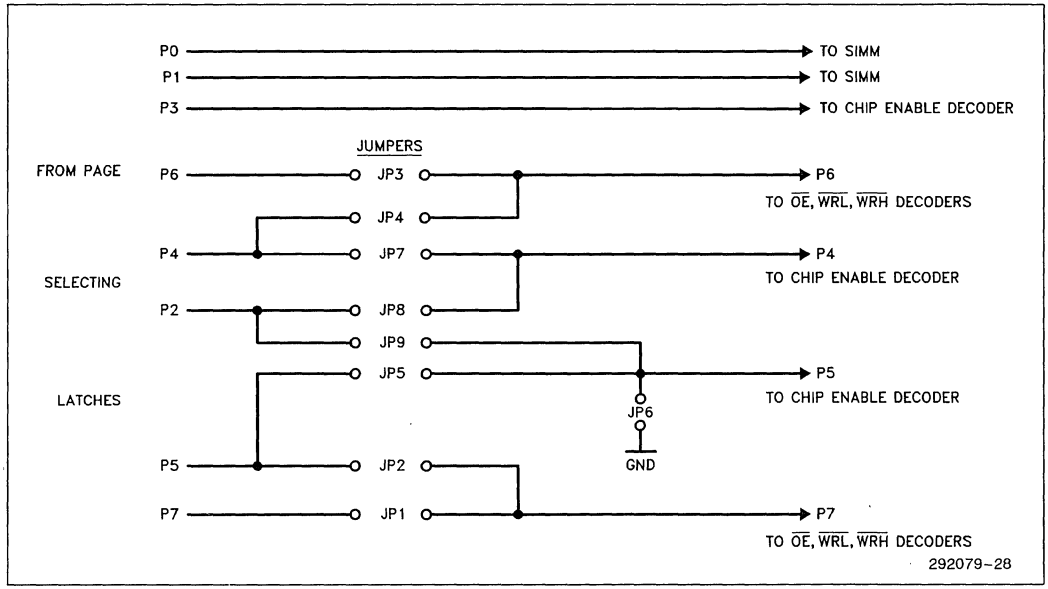


Figure 12. SIMM Density Upgrading Jumpers

6

If a system is designed that uses PCMCIA/JEIDA standard memory cards instead of SIMMs, this decoding is greatly simplified. The memory card is treated like a large memory array. Using a 64 Kbyte page size as an example:

Address lines A_{0-15} are supplied directly from the system address bus (after buffering). Address lines A_{16-23}, which select the pages, are sent as data to a latch before entering the memory card (Figure 13).

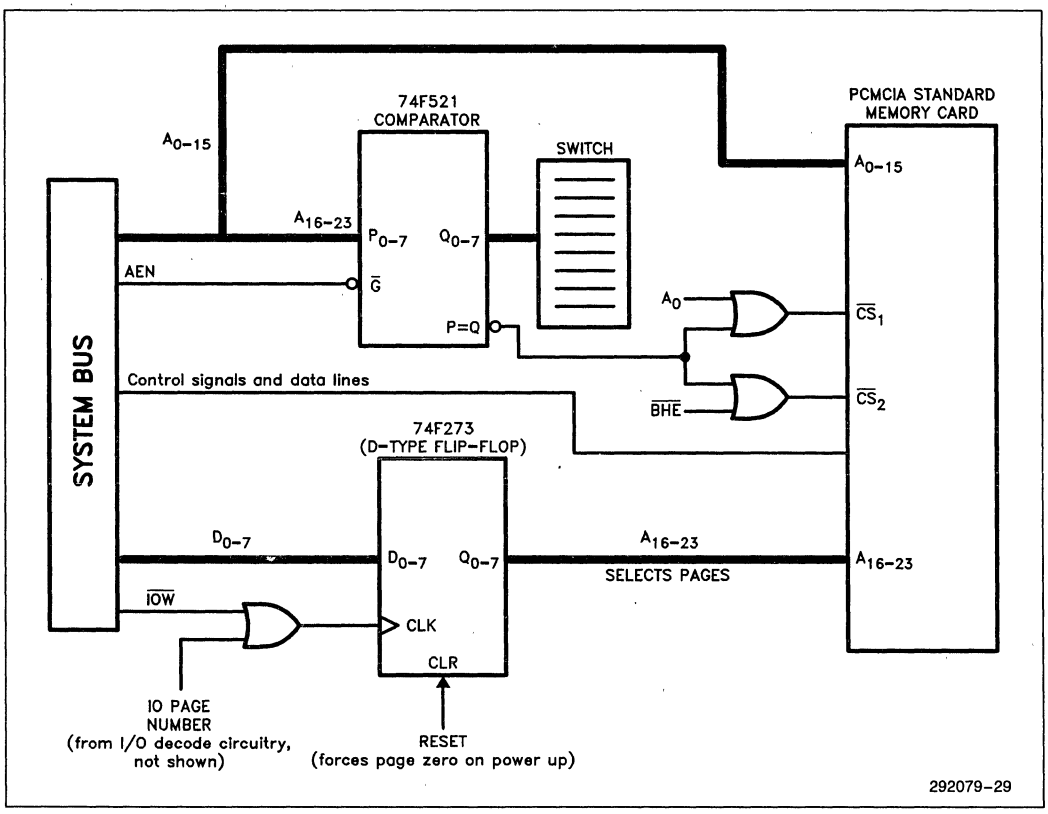


Figure 13. Memory Card Interfacing

The page inputs to the "Chip Enable" decoder (Figure 14, U22) are redefined as follows:

P3 = P3, P4 = P2, P5 = GND,

P6 = P4, and P7 = P5.

For a better understanding, you should verify the bit combinations while stepping through the first few pages. Notice that the sequencing of page numbers does not correspond linearly with the Chip Enables. This is not significant because the data is read the same way it is written.

Page Numbers	Chip Enable
0, 1, 2, 3	0
4, 5, 6, 7	2
8, 9, 10, 11	1
12, 13, 14, 15	3

NOTE:
Linear Page Selection Results in Nonlinear Chip Enable.

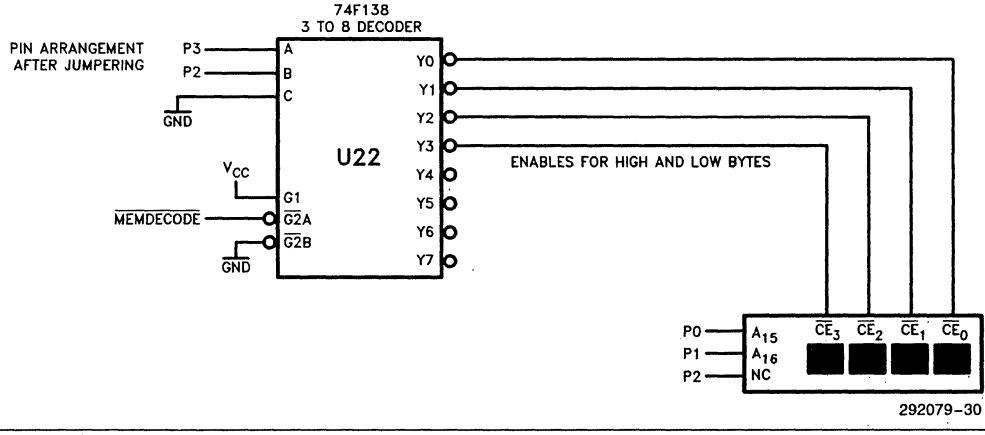


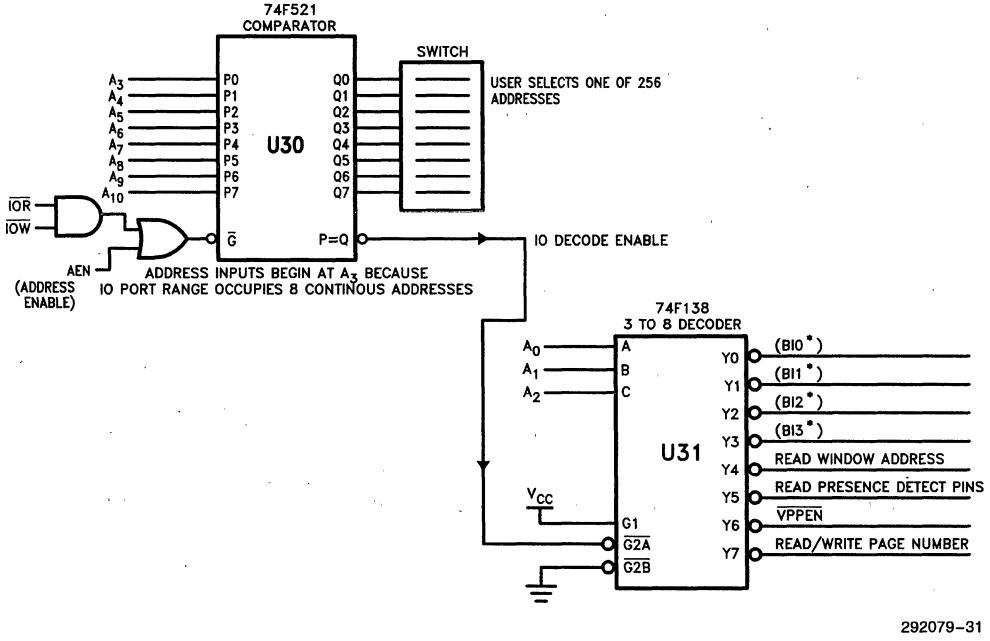
Figure 14. Component Selection Relative to Page Number for 1 Mbyte SIMM (iSM001FLKA)

6

I/O Decoding

Multiple functions can be implemented with I/O decoding access. Some examples include: reading the current window address, reading the presence detect pins, enabling V_{PP}, and reading/writing the page number. The eight consecutively addressed I/O ports on this board (4 reserved for optional features) are located at a user-selectable address. This base I/O port address is setup on an 8-byte boundary by using A_{3-10} as inputs to the 74F521 comparator (Figure 15, U30). When any of the eight consecutive I/O port addresses matches the dip switch settings (and AEN is low), the comparator outputs the I/O Decode Enable (to decoder U31).

AEN (address enable), the chip select for the 74F521 comparator, is supplied by the PC I/O channel. It distinguishes processor bus cycles from DMA bus cycles. A high on AEN indicates that a DMA (or DRAM refresh) cycle is in progress and we must stay off the bus. The enables for the 74F138 IODECODER (U31) are provided by IODECODE ENABLE along with the "ANDing" of $\overline{IOR}$ and $\overline{IOW}$. This decoder selects the I/O ports that access the page window address, the SIMM presence detect pins, the V_{PP} Enable, and the page number. Each of these I/O ports are described in detail:



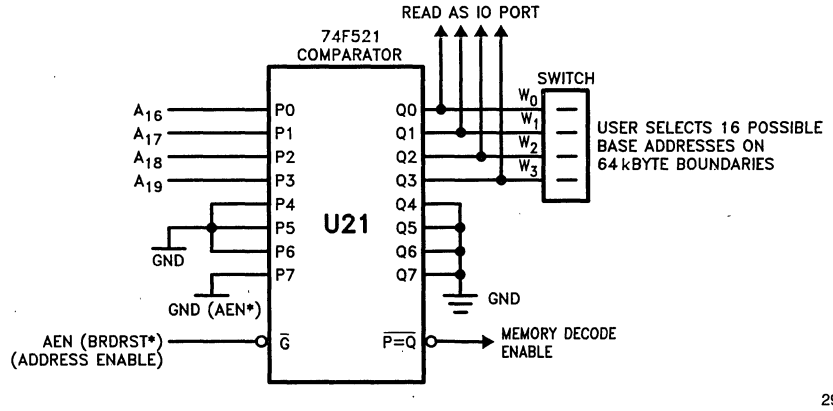
NOTE:
*Discussed in Board Identifier section of optional features.

Figure 15. User Selectable I/O Base Address for I/O Decoding

The Window Address

The user-selectable window address can be set up on any 64K boundary below 1 Mbyte. (The memory window should be placed between C0000h and E0000h to be DOS compatible.) A DIP switch (connected to a transceiver for reading) and the four address lines A_{16-19} are the inputs to the 74F521 comparator (Figure 16, U21). There are 16 possible window addresses. The comparator outputs the "Memory Decode Enable" signal when an address is selected that is within the 64 Kbyte window. This signal (with AEN low) allows board level memory decode.

The location of this 64 Kbyte window can be moved above 1 Mbyte by adding A_{20-23} to the comparator's inputs P_4 to P_7 of the 74F521. Bits D_{4-7} of the data bus can be connected to the comparator's pins Q_4 to Q_7 to allow reading of the full base memory address.



***NOTE:**
Ignore the contents within parentheses. This is used for section on master/slave configuration.

Figure 16. User Selects Base Memory Address

6

Presence Detect

The method shown earlier in Figure 3, is used to configure the PD pins in this design. SIMMs can be added incrementally only in similar densities. The SIMM PD pins are read by selecting the appropriate I/O address that enables the 74F245 transceiver.

V_{PP} Generation

V_{PP} is generated locally (on this board) to ensure a stable, switchable 12V (±5%) supply. (Many systems generate their own 12V power supply. However, it should not be used if its regulation is greater than 5%.) On power-up, system reset, or when V_{CC} is below 4.5V, V_{PP} is forced off. It is enabled (or disabled) by writing to the I/O port address (Figure 15, U31) that generates the $\overline{VPPEN}$ signal. This on/off capability is essential for battery-operated equipment and eliminates the need for $\overline{WE}$ filtering (as discussed below). (See Intel data sheet for V_{PP} standby current.) The $\overline{VPPEN}$ signal "ORed" with the system I/O write, $\overline{IOW}$, functions as the clock signal for the 74F74 D-flip flop (Figure 17, U42A). The D-input is latched when $\overline{IOW}$ goes high. Writing a one or a zero turns V_{PP} on or off, respectively.

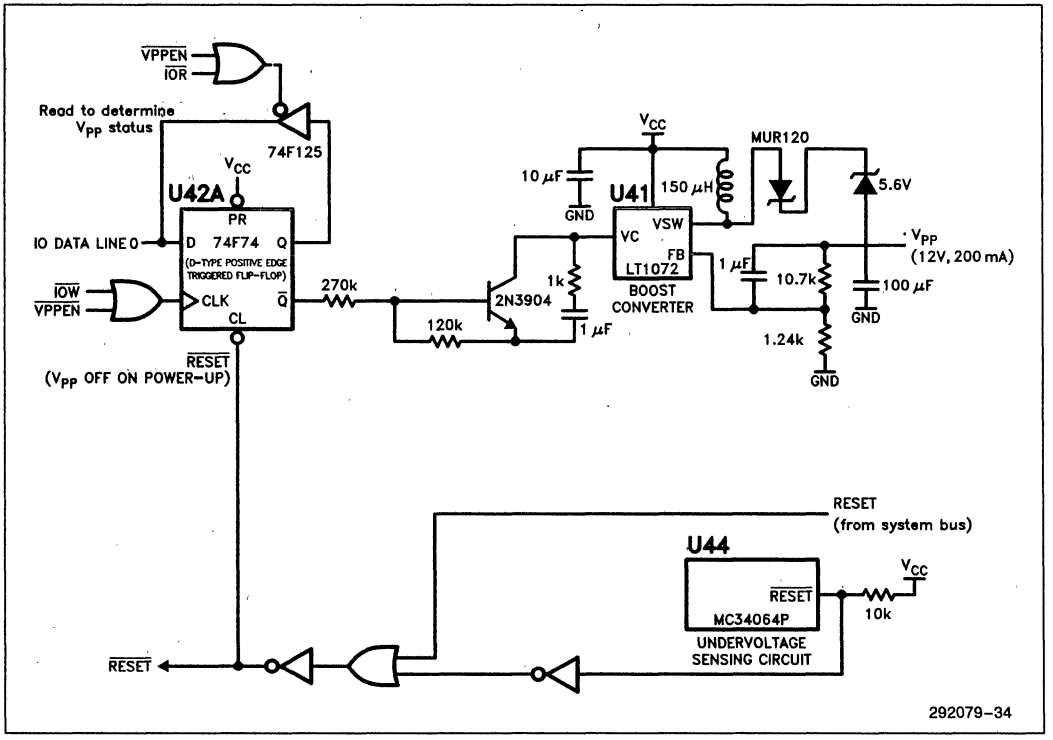
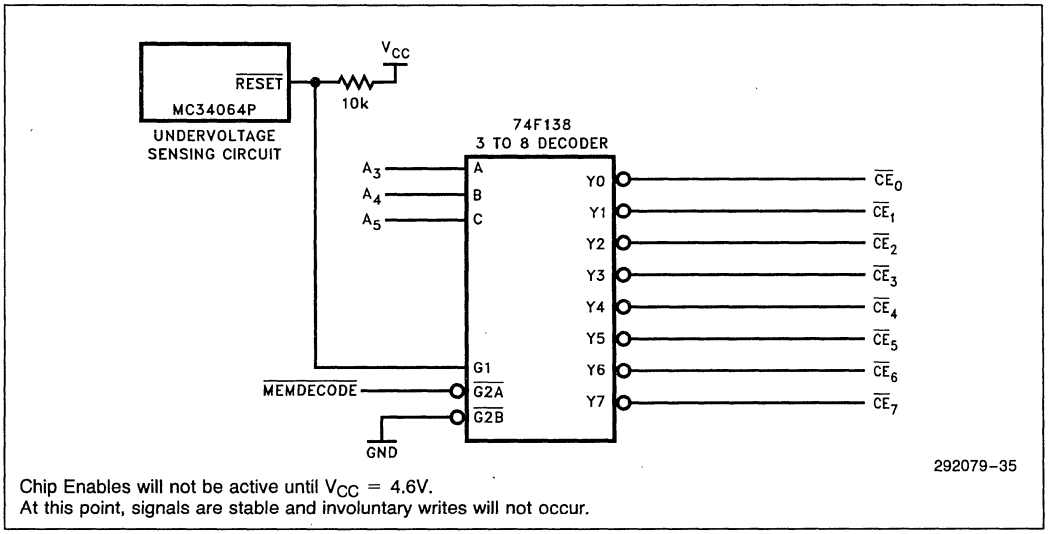


Figure 17. V_{PP} and $\overline{RESET}$ Generation

Linear Technology's LT1072 (U41) switching regulator is used as a 5V to 12V boost converter. The FB input regulates the voltage output. The 10.7k and 1.24k resistors are used to establish the correct reference voltage to obtain 12V. The 100 μF capacitor at the output is used to handle up to 200 mA. (See Linear Technology's LT1072 data sheet for more information.) Typically this will be much more than needed and a smaller capacitor can be used. However, this will accommodate interleaving of 8 components but may not be practical in a battery-operated system. (See section on interleaving in the Software Design Implementation chapter.) Additionally, sufficient time should be allowed when switching V_{PP} on. The delay is a factor of the load on the line and the quality of the passive components chosen. The diode, MUR120, keeps the inductor from absorbing current from the charged output capacitor. The 5.6V zener diode ensures that when V_{PP} is less than 5.6V, the V_{PP} output is held at 0V. (This is optional if $V_{PP} \leq 5V$ is tolerable.)

During system power-up, some probability exists that noise may generate spurious writes which are actually the sequence of flash memory commands that initiate erasure or programming. Power-up protection in this design is provided by disabling V_{PP} until voltages have stabilized. The Motorola component, MC34064P (U44), is an undervoltage sensing circuit that begins functioning when V_{CC} is above 1V. Between 1V and 4.6V, the $\overline{RESET}$ output is active. The $\overline{RESET}$ output or a system RESET clears the 74F74 (U42A), keeping V_{PP} off when V_{CC} is less than 4.6V. Alternatively, this signal, or a supply's "POWERGOOD" signal, may gate $\overline{WE}$ or $\overline{CE}$, as is common with battery-backed SRAM or EEPROM designs. As an example, the $\overline{RESET}$ output of the MC34064P can be tied to the active-high enable of the decoder to disable any $\overline{CE}$s until $V_{CC} = 4.6V$, as shown in Figure 18.



Chip Enables will not be active until $V_{CC} = 4.6V$.
At this point, signals are stable and involuntary writes will not occur.

Figure 18. Protecting the Circuit from Involuntary Erasure and Programming. Use an Undervoltage Sensing Circuit, or a System's "POWERGOOD" Signal, to Control Chip Enables

6

How is V_{PP} Switched on (Refer to Figure 17):

Latching a one into the 74F74 D-input (U42A) puts a zero on the output $\overline{Q}$. This turns off the transistor 2N3904. When the 2N3904 is off, the VC input of the LT1072 (U41) is 5V and the VOLTAGE SWITCH (VSW) output generates 12V.

Page Number Selection and Reading

It is standard practice to use an I/O port to generate the page number for this type of memory array. The potential number of pages that can be selected is determined by the size of the data bus as well as the amount of decoding the system can practically handle. In this design, this I/O port allows selection of 256 64-Kbyte pages, for a total of 16 Mbytes of flash memory. The page number is written to the 74F273, Octal D-Type Flip-Flop (Figure 19, U37). It is latched by the rising edge clock signal derived by the "ORing" of the corresponding 74F138 decode signal (I/O PAGE NUMBER) and the system $\overline{IOW}$.

Page zero is automatically selected on power-up because the 74F273 clear input is connected to $\overline{RESET}$ (generated as part of the V_{PP} circuitry). This feature ensures that the board will power up in page zero. Given the proper software, this board can be turned into the system's bootable drive. (See section on Software Design Implementations.)

The current page number can be obtained by reading the same I/O port. The I/O decoder output, I/O PAGE NUMBER, "ORed" with the system $\overline{IOR}$, produces the signal enabling the 74F245 bus transceiver (that is tied to the output of the 74F273).

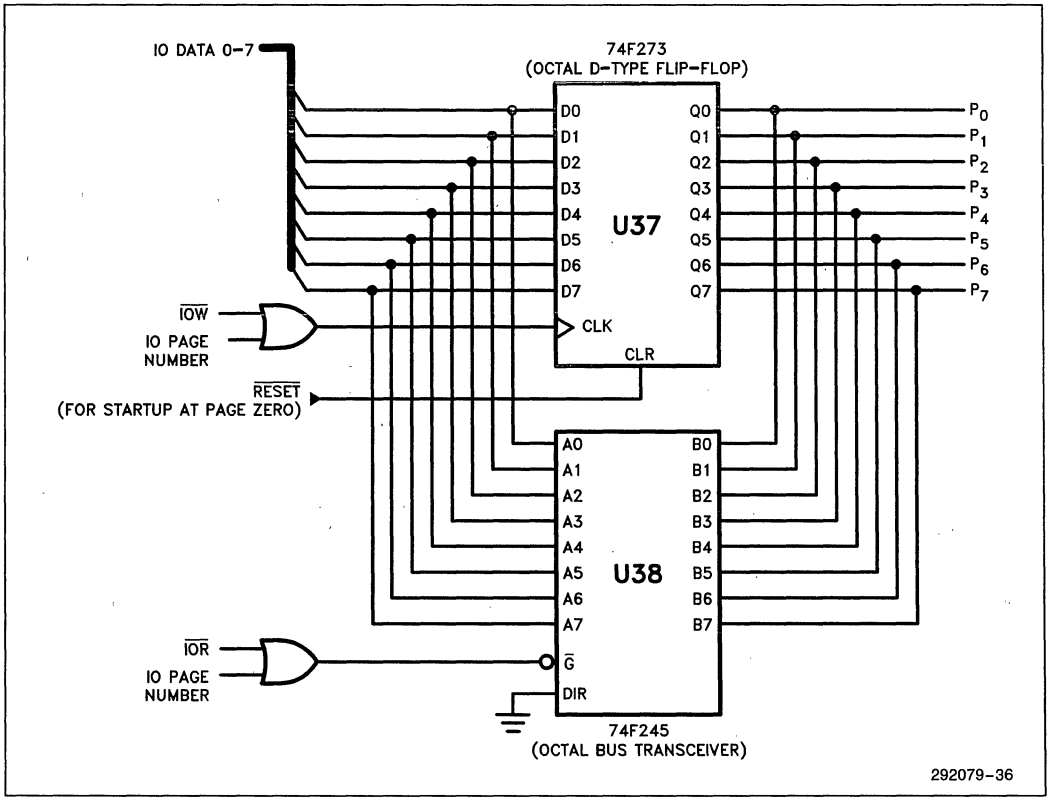


Figure 19. Selecting or Reading Page Number

Design Considerations

The SIMMs high and low bytes are enabled by $\overline{WEH}$ and $\overline{WEL}$, respectively. Using a high and low byte transceiver for each SIMM limits the capacitive loading and prevents performance degradation of the data bus. (This becomes important when upgrading to Intel Flash Memory SIMMs that have 16 components. See section on capacitive loading.) Also, the PC I/O channel bus specification requires that no more than 2 TTL loads be present on any one line. Therefore, the SIMM transceivers must be routed through two additional transceivers at the PC bus interface (refer to "Switchable Data Bus Width" section). In this paged memory board design, the SIMM transceivers are enabled by a 2 to 4 decoder which uses page pins P_6 and P_7 as decode signals. The enable for the decoder is supplied by the $\overline{MEMDECODE}$ signal; transceivers are disabled unless an address within the 64 Kbyte page is accessed.

Optional Board Features

So far we have described the components required to design a functional flash memory array. Optional features can be added to make this board more versatile in an application environment:

Switchable Data Bus Width

This feature allows the board to execute in a PC XT* (8-bit bus) or a PC AT system (16-bit bus). Memory card designs for adopting the PCMCIA/JEIDA format must include similar provisions as shown earlier. At the PC-I/O channel interface, (for use in an 8-bit system), an extra transceiver is used to redirect the upper data bus (D_{8-15}) to the lower data bus (Figure 20, U9). The $\overline{16BIT}$ signal is generated from a ground on the PC AT I/O channel extension; it will be high (because of the pull-up resistor) when a PC XT is used. (The $\overline{16BIT}$ signal can be read by software through the 8th bit of the Presence Detect port.)

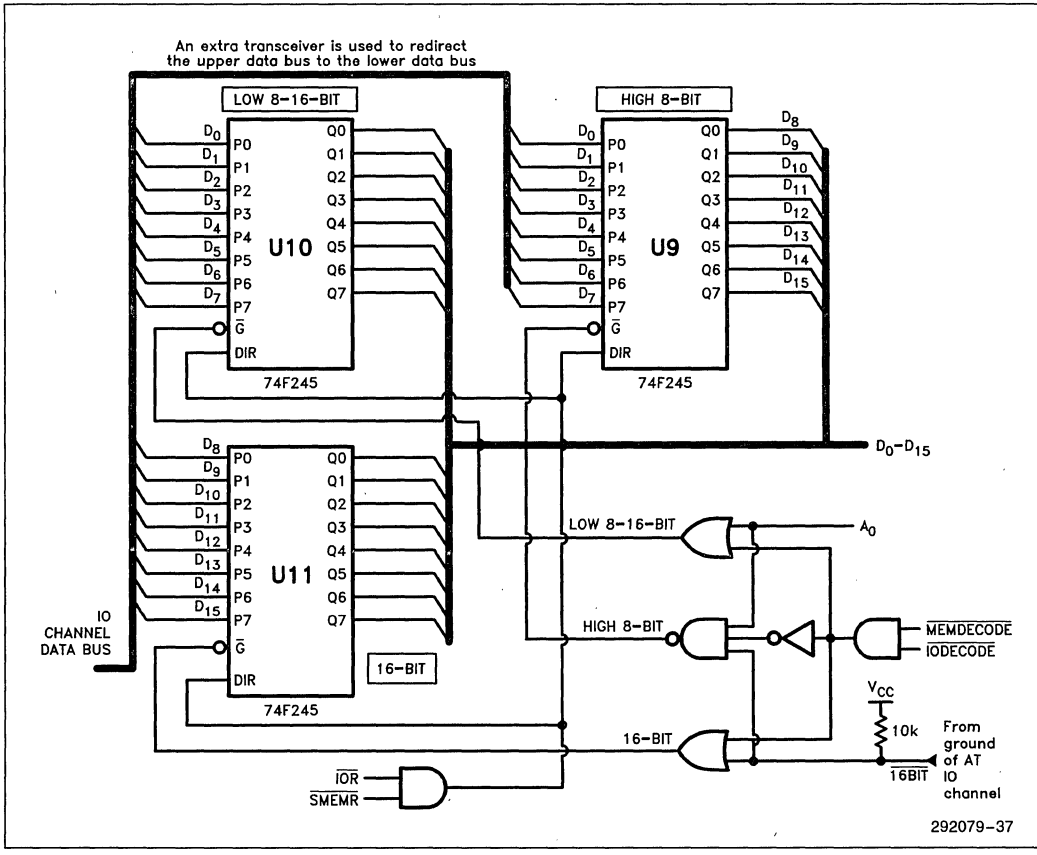


Figure 20. I/O Channel Transceiver Interface for 8- or 16-Bit Data Bus Selection

*PCXT® is a registered trademark of International Business Machine Corporation.

Access to a word (2 bytes) requires two bus cycles to generate two addresses in an 8-bit system. As an example referring to Figure 20, when accessing a memory word at address zero (0):

$$\overline{16BIT} = 1, \overline{MEMDECODE} = 0;$$

During access to the low byte → A0 = 0, so the signal "LOW 8/16 BIT" is active;

During access to the high byte → A0 = 1, so the signal "HIGH 8 BIT" is active.

The high byte from the SIMM is multiplexed onto the low byte of the system bus.

The circuitry at the SIMM transceiver interface determines whether to use the Bus High Enable ($\overline{SBHE}$) signal or A_0 to select the high byte. The $\overline{16BIT}$ signal selects the "A" or "B" inputs of the 74F157 multiplexer (Figure 21, U27). Regardless of the bus size, the $\overline{WRL}$ signal is generated on a system memory write ($\overline{SMEMW}$) to an even address (A0 = 0). During a 16-bit write, the $\overline{WRH}$ signal is generated by a system memory write to the high bus ($\overline{BHE}$). However in an 8-bit system, where $\overline{SBHE}$ is absent, the $\overline{WRH}$ signal is generated by a system memory write to an odd addressed byte (A_0 = 1).

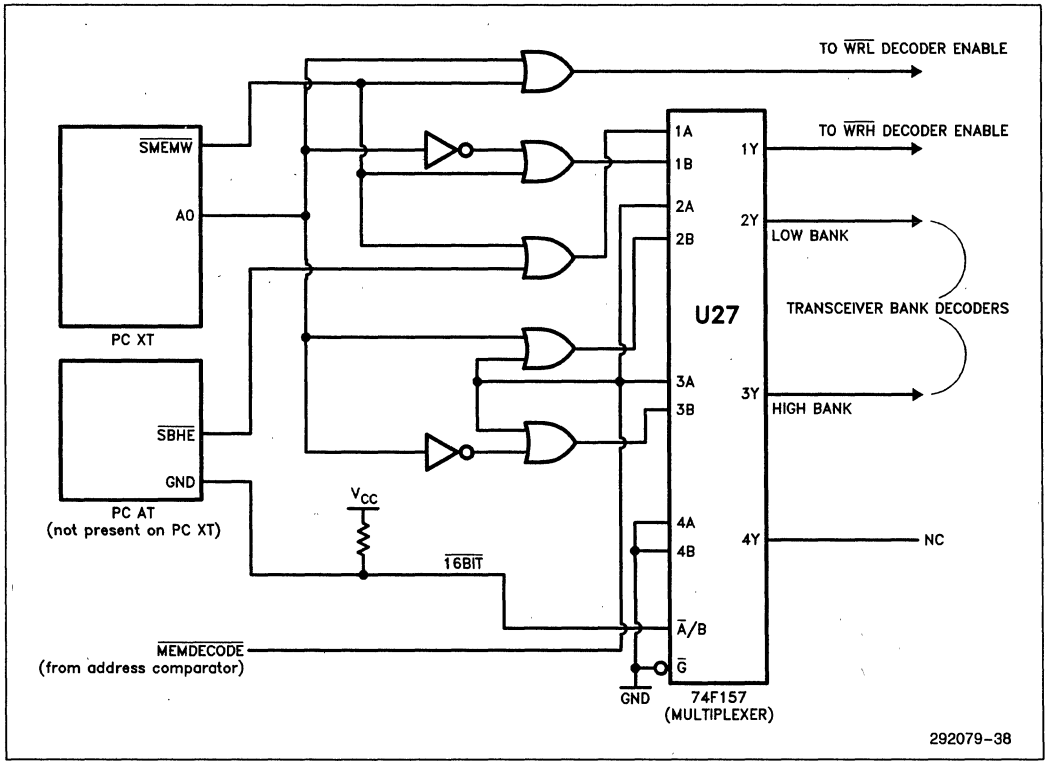


Figure 21. 8- or 16-Bit Data Bus Selection at the SIMM Transceiver Interface

The eight transceivers for the four SIMMs are selected by signals T_{0-7}. Even (T_0, T_2, T_4, T_6) and odd (T_1, T_3, T_5, T_7) numbered signals decode for the SIMM low and high bytes, respectively. The signals T_{0-7} are derived by decoding P_6 and P_7 (Figure 22, U24A) and the transceiver bank decoders (Figure 21, U27).

For a 16-bit system, the $\overline{\text{MEMDECODE}}$ signal selects both the low and high banks. For an 8-bit system, the low bank is selected by generating an even address (A_0 = 0) in conjunction with the $\overline{\text{MEMDECODE}}$ signal. Since $\overline{\text{SBHE}}$ is absent (in an 8-bit system), the high bank is selected by an odd address (A_0 = 1) in conjunction with the $\overline{\text{MEMDECODE}}$ signal.

Master/Slave Configuration

This feature allows the system to accommodate more than one board. The board reset signal, $\overline{\text{BRDRST}}$, of Figure 23 is used to enable the board. The comparator (Figure 16, U21) that generates the MEMORY DECODE ENABLE must be reconfigured:

1. AEN is connected to P_7;
2. $\overline{\text{BRDRST}}$ is connected to the chip enable, $\overline{G}$.

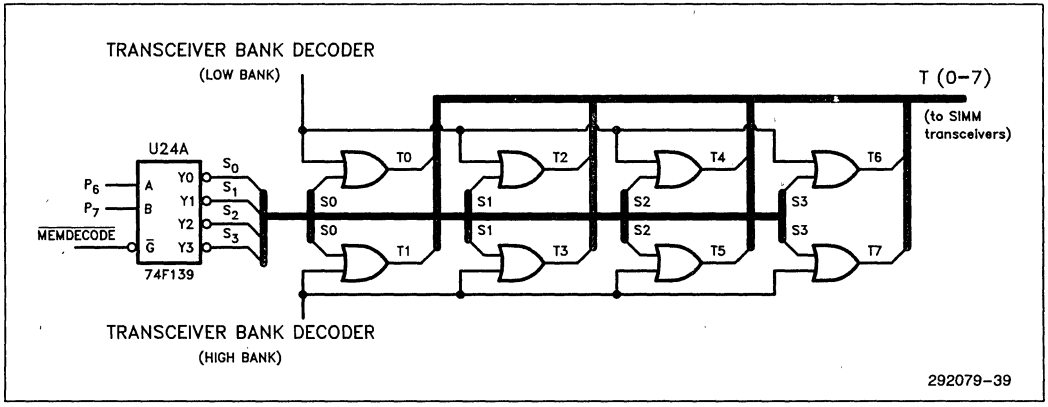


Figure 22. Transceiver Selection at the SIMM Interface

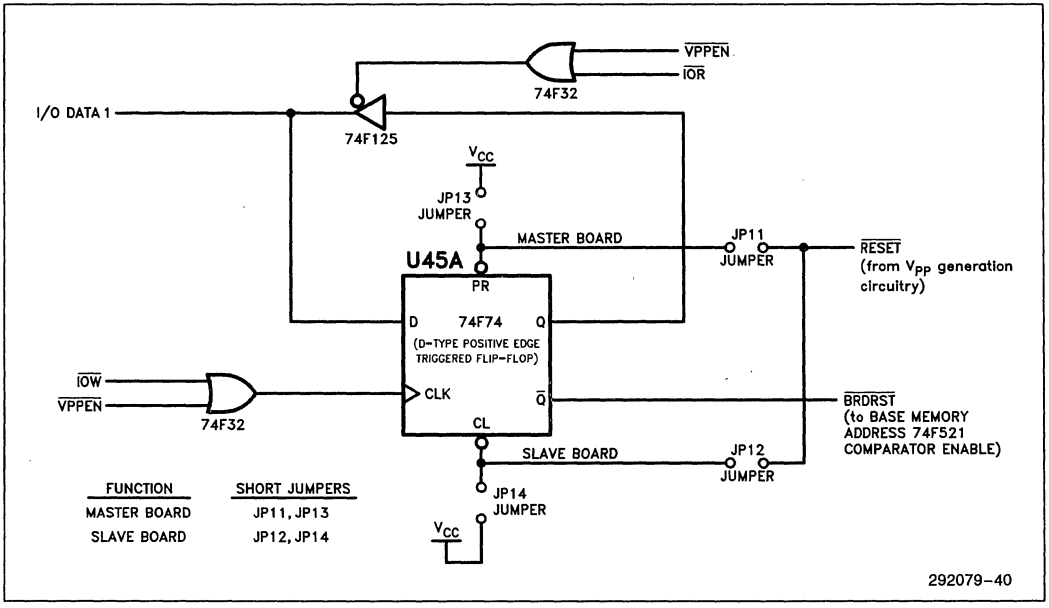


Figure 23. Master/Slave Configuration for Multiple Boards

The jumper settings determine if the board is "active" on system reset ($\overline{BRDRST}$ will be low). The Master/Slave port is shared with V_{PP} enble; therefore to change the "active" status of the board, write to the $\overline{VPPEN}$ I/O port. Software should first read this port to determine the status of "V_{PP} Enable", then use the appropriate mask technique to activate or deactivate the board.

Board Identifier

The board identifier, occupying 4 additional I/O ports, is used for two functions:

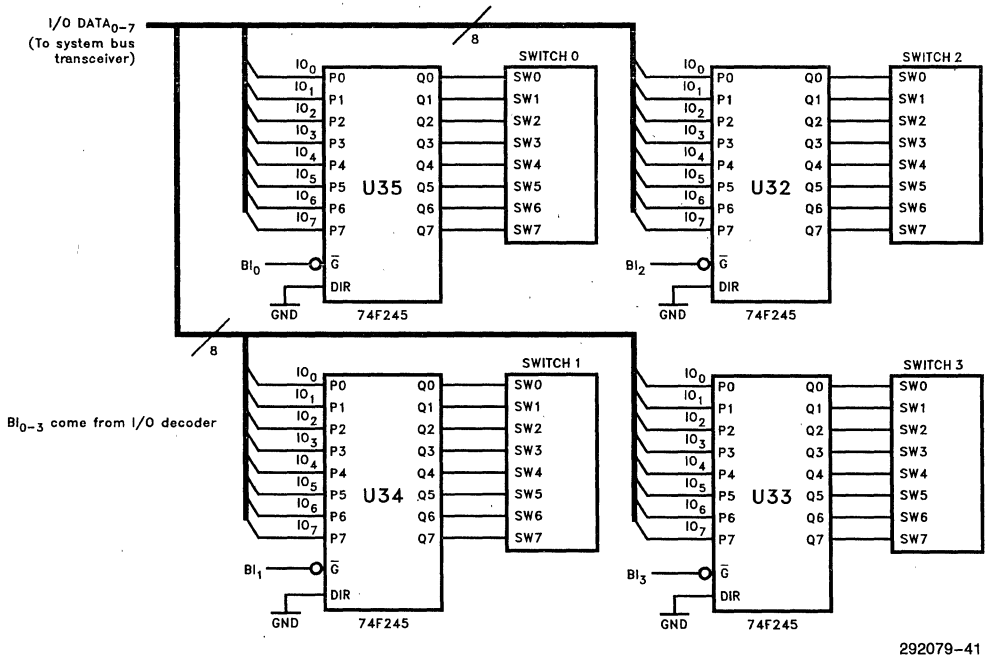
1. To locate the board within the system I/O space, and
2. To identify the board version to assure the software matches the hardware.

The hardware consists of 4 DIP switches and associated 74F245 transceivers (Figure 24, U33–U36). Each switch is read by selection of its I/O address (Figure 15, use $\overline{BI_0}$–$\overline{BI_3}$). The DIP switches can be replaced by EPLDs that permanently "hardwire" the settings. In this case, the identifier is changed by reprogramming the EPLDs.

Zero-Wait-State Selection

The zero-WAIT selection feature is only applicable in a PC AT system. Driving a low input to the 0WS pin of the PC I/O channel within 21.5 ns of $\overline{MEMR}$ or $\overline{MEMW}$ going low keeps the system from inserting the standard WAIT-states into the I/O channel bus cycle. On the page memory board, the 0WS signal is generated by the Boolean equation:

$$(\overline{SMEMW} * \overline{SMEMR}) + \overline{MEMDECODE} = 0WS.$$



NOTE:
DIP switches can be replaced with EPLDs.

Figure 24. Hardware Used to Locate and Identify Page Memory Board

Initializing Software for the Paged Memory Board

(The assembly language software is included in the Appendix.)

In the following sections, algorithms will be shown that verify the page-memory board's functionality. To access this board, first find the location of the base I/O address. From Figure 15, the board's I/O ports are accessed as offsets of the I/O base address:

Board Identifier *n*	@ Base Address + *n* (n = 0, 1, 2, 3)
Window Base Address	@ Base Address + 4
Presence Detect Pins	@ Base Address + 5
Master/Slave and $V_{\overline{PPEN}}$	@ Base Address + 6
Page Number	@ Base Address + 7

Next, the Window Base Address I/O port is used to locate the "page" in DOS's memory space. It is then necessary to determine the density of the SIMMs and the total memory available.

Locating the Base I/O Address

Use the board identifiers to locate the base I/O address. The software reads I/O locations until the correct byte sequence is found (Figure 25). Some discretion should be made when choosing the board's I/O address. (See table of I/O port usage in Appendix.) The PC XT and PC AT specification allocates 32 I/O ports at 0300h to 031Fh for prototype cards. We will use this address range for this example. Because the I/O ports for the paged-memory board must begin on an 8-byte boundary, the only possible base addresses are 300h, 308h, 310h, 318h.

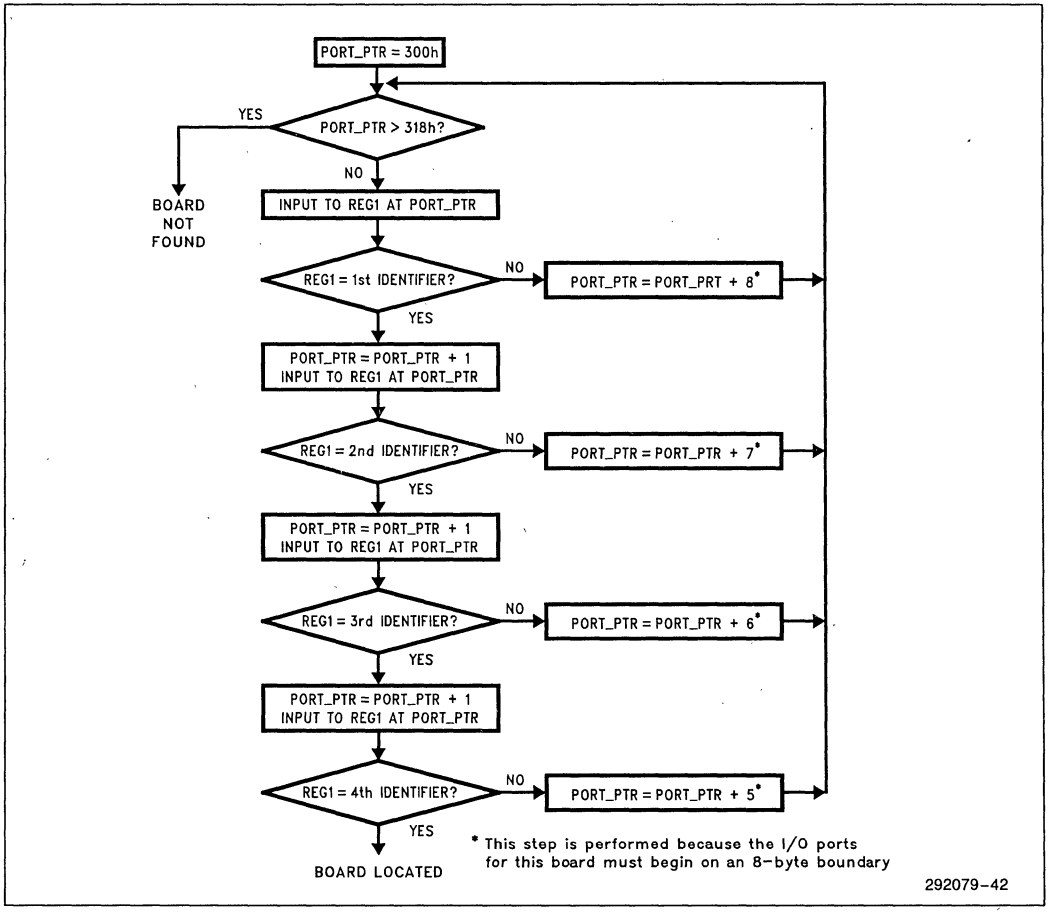


Figure 25. Locating the Page-Memory Board

Locating the Base Memory Address

The base memory address gives the location of the page within the system's memory space. The address switch settings for A_{16}–A_{19} are read from the correct I/O port, Base Address + 4 (Figure 15). After reading these address lines they are stored in the ES segment register used as a pointer to access that memory segment. A_{16}–A_{19} must be shifted into the upper nibble of the ES register to allow proper address generation.

Determining Memory Capacity

First ensure the board is set to read from Page 0. The PD pins are read and translated, using a lookup table of SIMM densities, to a functional value. (See 28F001AX data sheet for Presence Detect pin definitions.) Then the device identifiers should be read to determine:

1. The number of components on each SIMM;
2. the number of SIMMs installed on the board;
3. and which sockets are used.

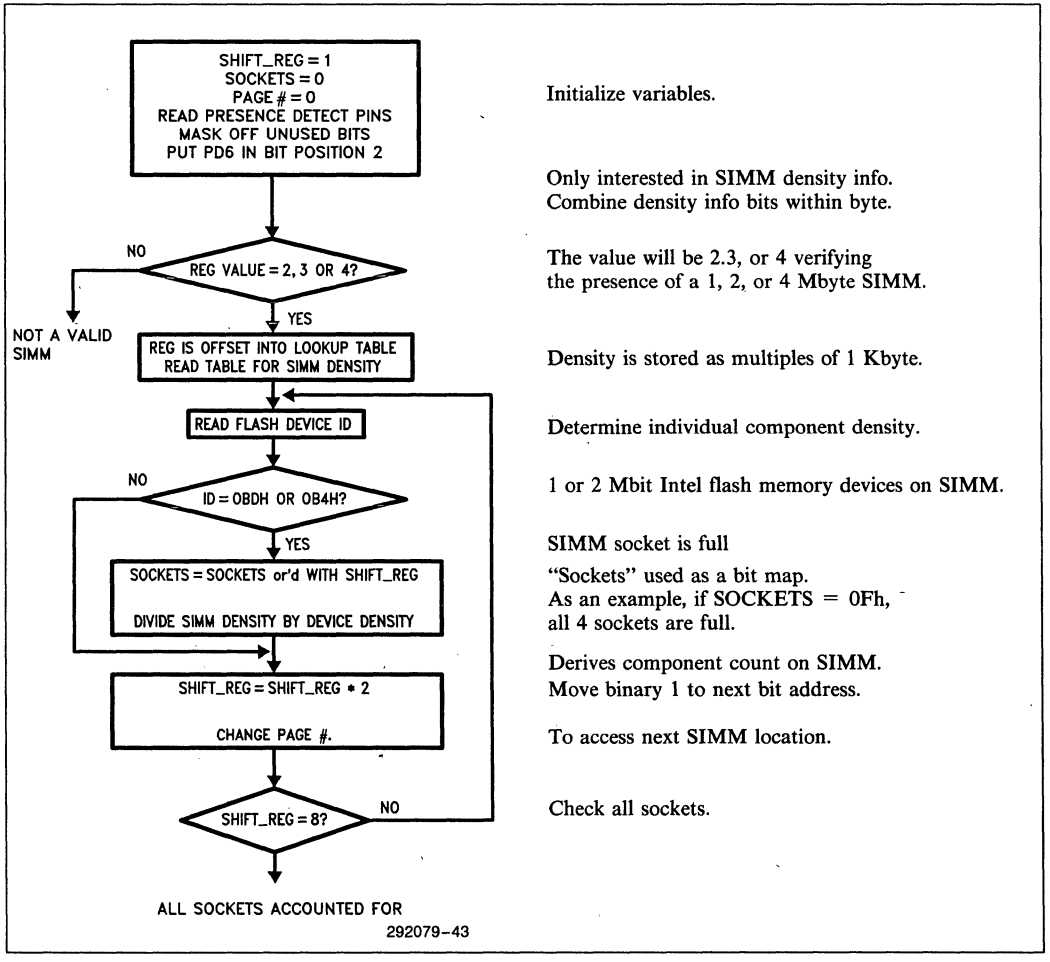


Figure 26. Determining SIMM and Component Densities and Locations

Linear Addressing

Linear addressing directly maps the flash memory array into the system's memory space. "Instantaneous Access" of the entire array is the obvious advantage over paging. Additionally, the decode circuitry is simplified. Figure 27 shows an example for accessing 16 Intel Flash Memory 28F020s arranged in a 4 Mbyte linear array.

The number of address lines used, as well as the decoder type (2 to 4, 3 to 8, etc.), is determined by the flash memory device size. The address lines A_1–A_{18} are used for byte selection within each device (256 Kbytes * 8).

The decodes for the individual devices can be designed in a row-column method similar to that used for the page memory board. An alternative design uses an individual chip enable for each of the 16 devices.

The enable for the 74HC138 (3 to 8 decoder) is governed by a 74F521 comparator. System address inputs to the comparator are chosen to locate this array on a 4 Mbyte boundary. (The array base address could be located on a non-4 Mbyte boundary but this would add to the decoding complexity.) With the inputs chosen in this example (A_{22}–A_{23}), the array base address will be between address 0 and 12 Mbytes to confine this memory array within the PC AT defined address space of 16 Mbytes. A_{19}–A_{21} are inputs to the decoder which generates one of the eight chip enables ($\overline{CE}$). (Use a 74F245 transceiver for the data bus of every 8 flash memory devices. The address lines also need buffering when connected to a PC bus.)

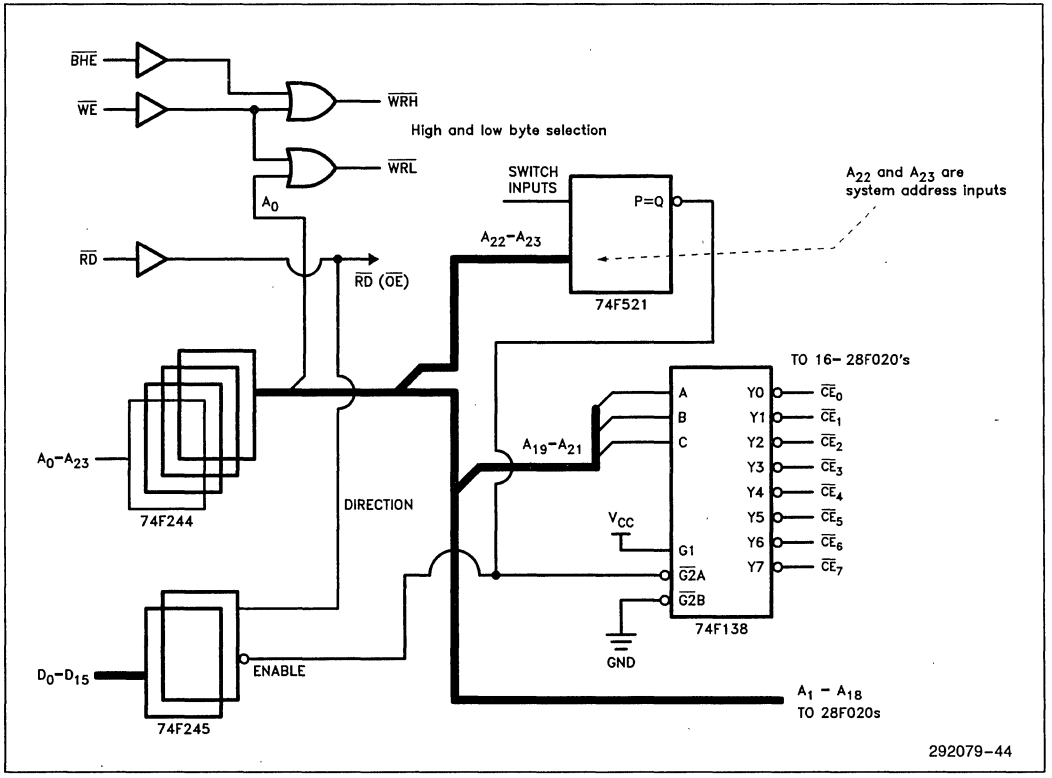


Figure 27. Linear Addressing Hardware Block Diagram

I/O Addressing

From the standpoint of the system's address space usage, I/O addressing provides a conservative solution. As an example, four gigabytes of a flash memory array can be addressed through only two I/O ports. An I/O write sends the flash memory addresses out on the data bus. This "data" is latched (using '574s) and made available to the flash memory devices and decoding circuitry (Figure 28). A third I/O port, used as an enable for the flash memory device decoder and transceivers, helps conserve power when the array is not being accessed.

Relative to linear addressing, I/O addressing generally has limited access speed capability because of the I/O "bottleneck". Read speed can be increased to match linear addressing by replacing the '574 latches with '191 counters.

In the following circuit example, decoding for I/O is accomplshed with a 74F138, 3 to 8 decoder (Figure 29, U1). The base address for these I/O ports is on an 8-byte boundary. When any one of the 8 I/O addresses is selected, the comparator (U2) generates the enable signal (if AEN is low) for the decoder.

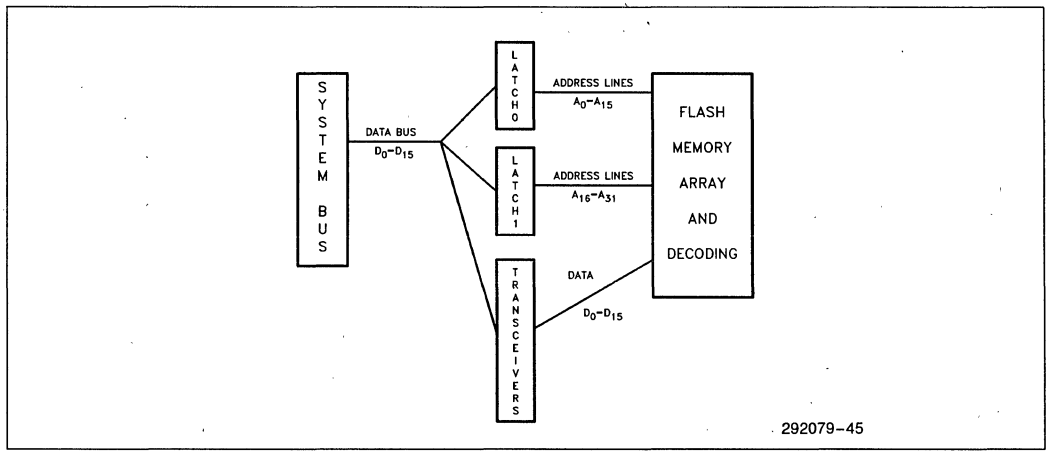


Figure 28. Data Bus Generates Flash Memory Addresses

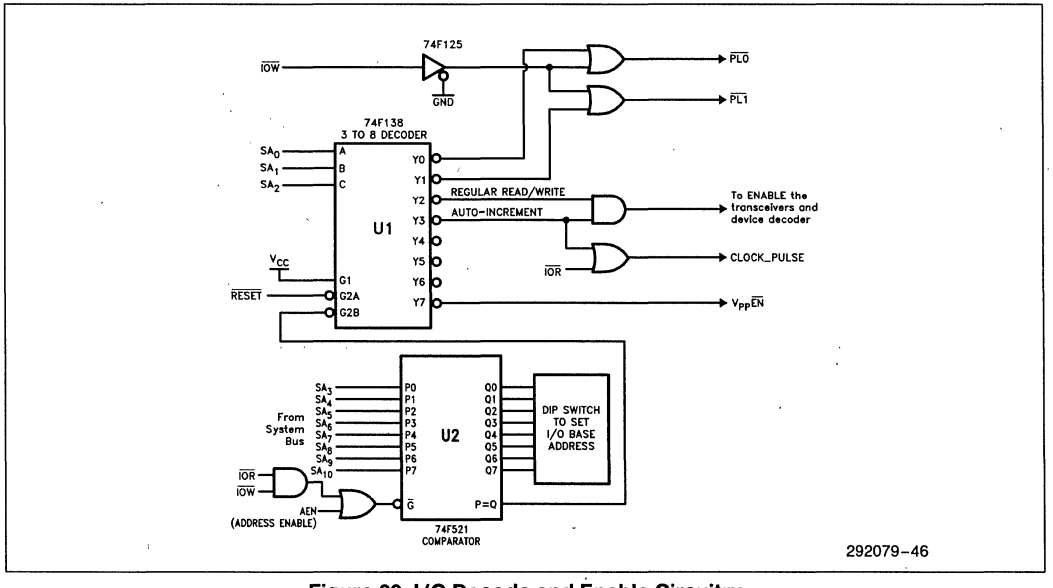
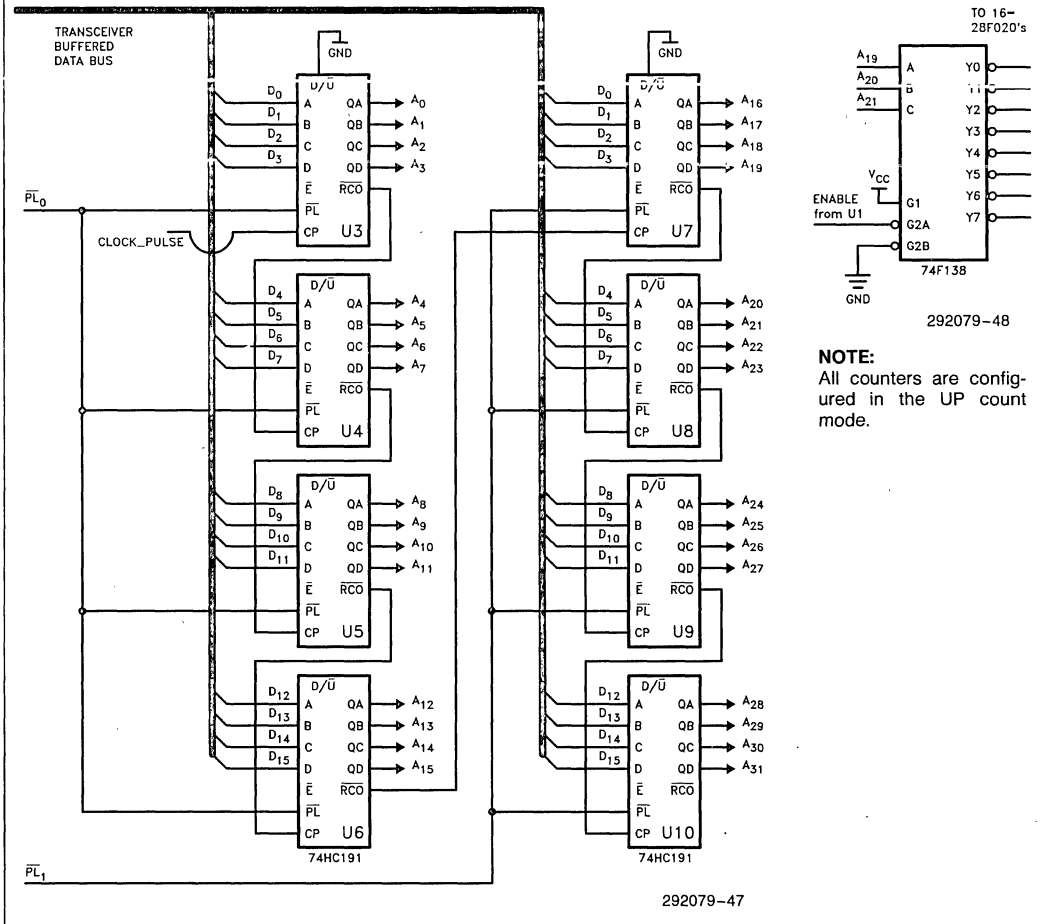


Figure 29. I/O Decode and Enable Circuitry

An I/O write to the first and second ports generates parallel load signals, $\overline{PL_0}$ and PL_1. These signals latch the "data" (addresses) into the 4-bit counters (Figure 30, U3–U10). This latched data represents the address for the flash memory devices.

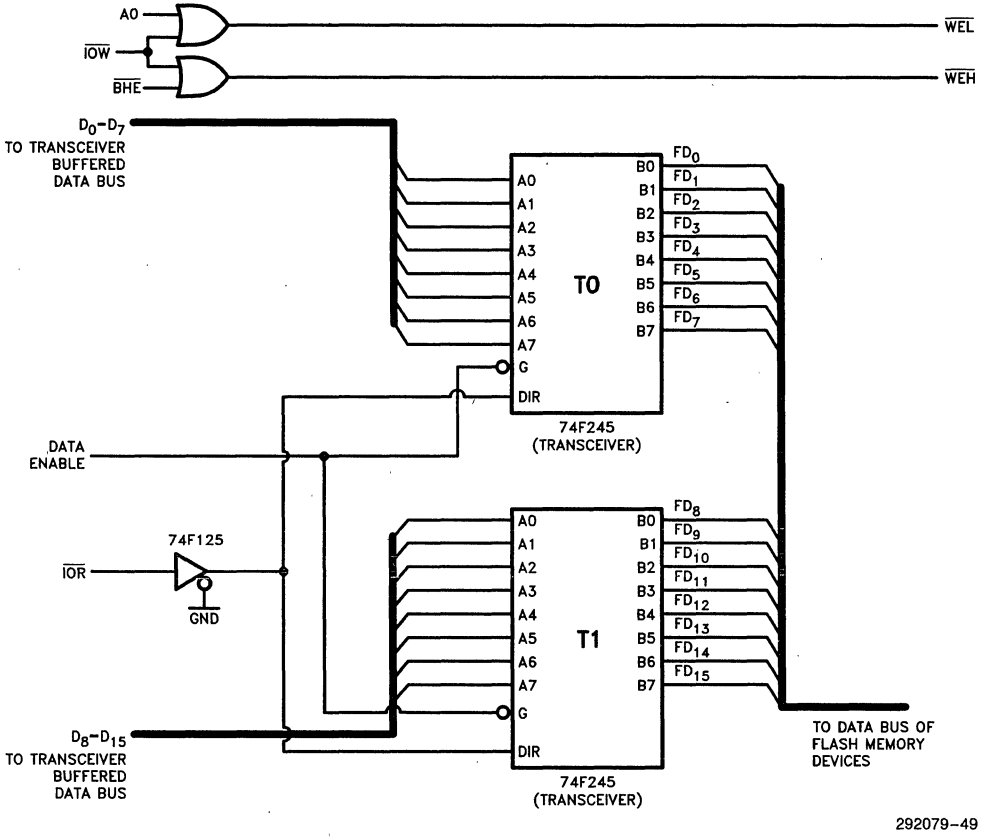
A read or write from the selected flash memory address is performed when the third I/O port is accessed (Figure 29, U1); this generates an enable for the flash memory device decoder and associated transceivers (Figure 31, T_0 and T_1).



NOTE:
All counters are configured in the UP count mode.

NOTE:
A_0–A_{31} are inputs to flash memory devices. Only address lines A_0–A_{18} are used for the 28F020s.

Figure 30. Counter Circuitry



NOTE:
The 16-28F020's are arranged as a 16-bit word configuration. $\overline{WEL}$ and $\overline{WEH}$ are for the low and high bytes, respectively.

Figure 31. Transceiver Enable Circuitry

The fourth I/O port activates the circuitry that obtains very high performance from an I/O board. A read from the fourth I/O port address generates the clock signal for the 74HC191s, CLOCK__PULSE. The counter increments on the rising edge of the clock (read signal), selecting the next flash memory address. This rising edge occurs at the end of the I/O read cycle and the data has already been read. This method is analogous to address pipelining. It is perfect for a "string" read because continuous reads from the fourth I/O port automatically increments the address to access the next word of data stored in the flash memory array.

Capacitive Loading

Capacitive loading is an important consideration for a solid-state mass storage device. If proper buffering techniques are not followed, performance degradation will occur.

The specifications for Intel's Flash Memory devices are based on a test capacitive load of 100 pF. Each data line contributes 12 pF, therefore 8 devices connected to one data transceiver will not experience speed derating (12 pF * 8 = 96 pF). Additional flash memory devices

on that transceiver will increase the loading seen by any one device.

Degradation is calculated as follows (Q = Amount of Charge, T = Time, C = Capacitance, V = Voltage, and I = Current):

COULOMBS LAW STATES:

$$Q = I\Delta T$$

AND GIVEN THE RELATION:

$$V = \Delta Q/C \rightarrow I = C\,\Delta V/\Delta T$$

FROM THIS RELATION, THE CHANGE IN ACCESS TIME CAN BE EXPRESSED IN TERMS OF CAPACITIVE LOAD:

$$\Delta T = C\,\Delta V/I$$

For example, using four SIMMs, each with 8 components in a 16-bit configuration (4 components on high byte and 4 components on low byte), each Intel Flash Memory device sees a load of 15 devices (12 pF * 15 = 180 pF). This loading is 80 pF in excess of the device specification so therefore:

$$\text{Time Change} = \text{Additional Capacitance} \times \frac{(V_{CC} - V_{OL})}{I_{OL}}$$

$$= 80\text{ pF} \times \frac{(5.0 - 0.4)\text{V}}{5.8\text{ mA}} = 64\text{ ns}$$

(Reflecting worst case conditions.)

SOFTWARE DESIGN IMPLEMENTATIONS

Each hardware implementation discussed above can be used in several types of mass storage applications. The general categories include: data recoders, Write-Once-Read-Many (WORM) drives for storing application programs and fixed data, and magnetic disk emulators.

Data Recording

The applications for data recording represent an endless list. Examples include digital imaging, digital photography, point-of-sale terminals, patient monitors, and flight recorders. These systems will use Intel Flash Memory as a more economical and reliable replacement for SRAM + battery. Alternatively, mechanical disks will also be replaced by Intel's Flash Memory when higher reliability, lower power consumption, higher performance, and lighter weight are required.

Interleaving

Although the basic concept of data recording is similar from system to system, variations in implementation exist. For instance, some applications require high-speed data acquisition. Data programming rates are improved considerably by employing interleaving techniques. The majority of time spent programming or erasing a flash memory device results from the delay times in the software algorithms. (It is advised to review the standard algorithms first. See any Intel Flash Memory data sheet for Quick-Pulse Programming™ algorithm.) Interleaving takes advantage of these delay times to begin programming consecutive devices.

There are hardware and software mechanisms for interleaving. The flash memory array for hardware interleaving requires special decoding techniques (Figure 32). Contrary to linear decoding, the system address lines A_0–A_3 are decoded to provide the chip select signals and individual bytes are selected with the address lines A_4–A_{20}. (For the Intel 28F010.) This decoding technique allows software to automatically access sequential devices by writing or reading sequential memory addresses. (Data accumulated with program interleaving will not be stored consecutively within a single device.)

The interleaving algorithm to program the 2 Mbyte flash memory array is shown in Figure 34 and 35. The basic goal is to utilize the delay times. To simplfy the algorithm for this discussion, the data will be programmed on a byte-wide basis. Word-wide and double word-wide techniques, discussed later, will further increase programming speeds.

During multi-component programming, the number of pulses required could vary between different devices. Code is reduced if the programming loop does not have to selectively "decide" if a byte has programmed correctly (verified). However, continual programming of a programmed byte is not necessary and should be avoided. This is done by masking the command sent to that particular device. The RAM table in Figure 33 is used as a data and flash memory command buffer. After a programmed byte has verified, its associated data and commands in the RAM table are written with the value 0FFH (RESET command for Intel flash memory). The data is also written as an 0FFH since this is null program data.

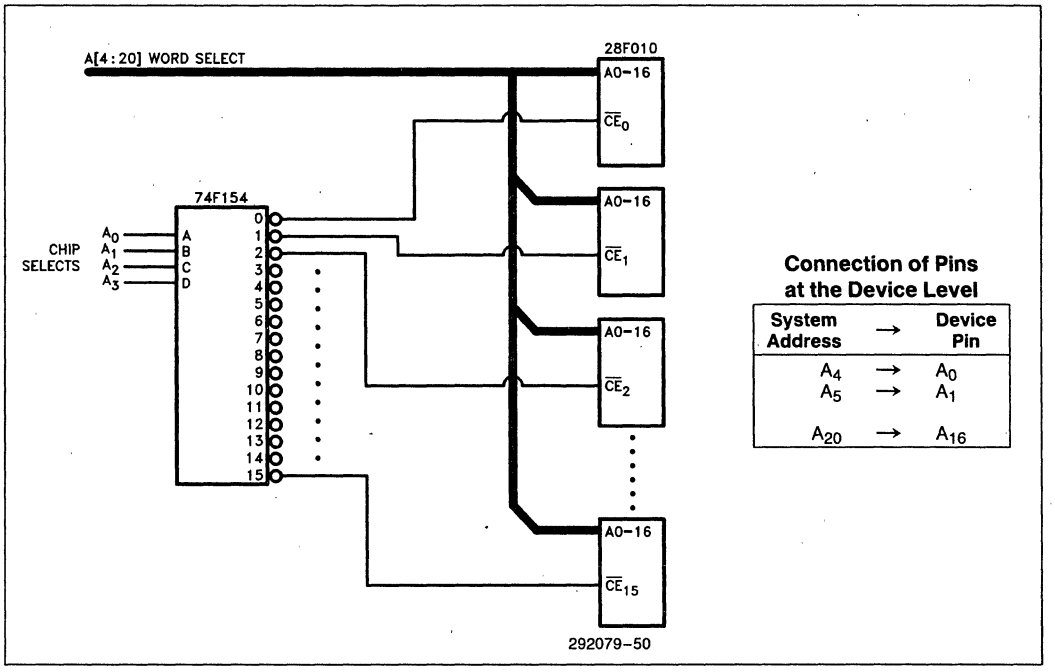
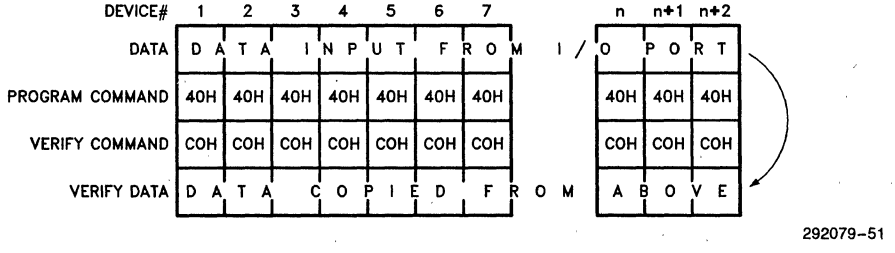


Figure 32. Hardware Interleaving Block Diagram



NOTE:
n = 14 for the example shown in text.

Figure 33. RAM Array Used as Data Buffer and Command Mask Storage

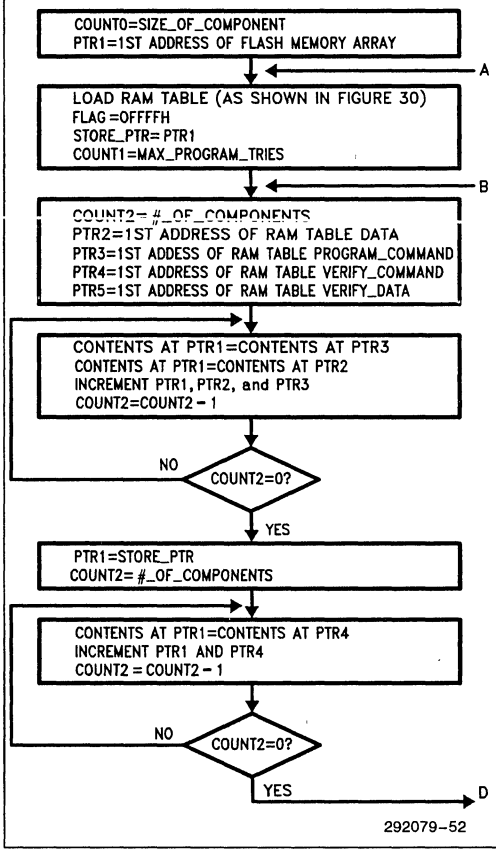


Figure 34. Program Interleaving Algorithm

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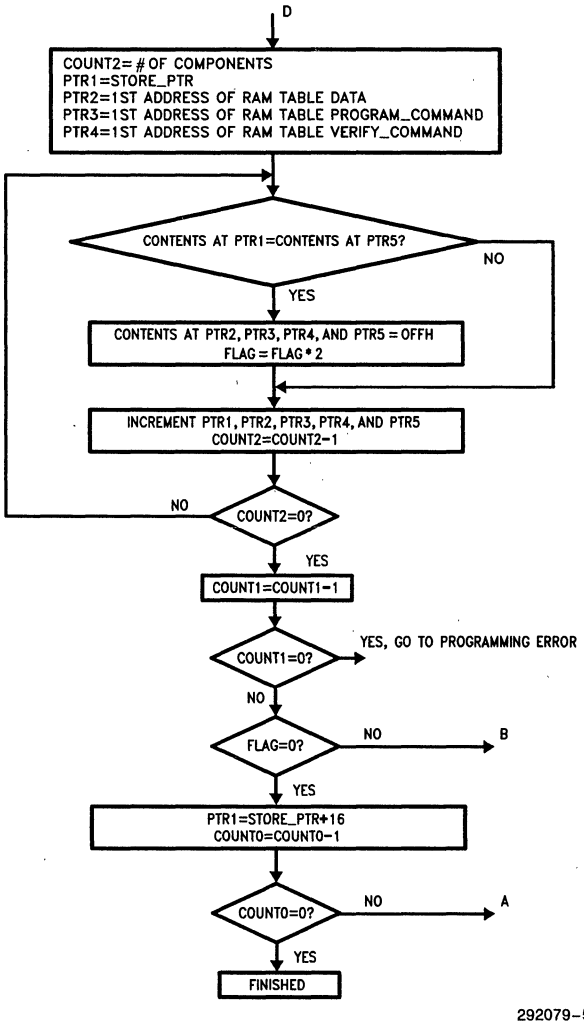


Does Flash Memory Byte = Verify Byte?

Shift bits of flag left.

Exceeded program tries, go to error.

All 1's shifted out?

To access next byte of each device.

Figure 35. Program Interleaving Algorithm (Continued)

Software and hardware interleaving are very similar. Software interleaving is performed using conventional decoding and addressing methods. Instead of incrementing flash memory addresses by one to access the next byte (as with hardware decoding), the address is incremented by the size of the component. While allowing the use of "general-purpose" (non-interleaved) hardware, software interleaving requires reading back the data in the same, non-sequential fashion as was used for recording.

Interleaved erase is useful for erasing an array of flash memory devices. This approach greatly reduces the total subsystem format time. As specified in the erase algorithm, each erase pulse requires a 10 ms delay. (See Quick-Erase™ algorithm in Intel Flash Memory data sheet.) Without interleaving, the processor is idle during this delay time. As with program interleaving, this time is used to begin the erasure of consecutive devices, thereby reducing the overall erase time.

Further program and erase time can be saved by supplementing the byte-wide algorithm with 16- or 32-bit interleaving. Extra data and commands are added to the RAM Mask Table. The major difference in the algorithms involves the verify operation. Depending on the bus width, 2 or 4 bytes are verified simultaneously as shown in Figure 36 (for a 16-bit algorithm).

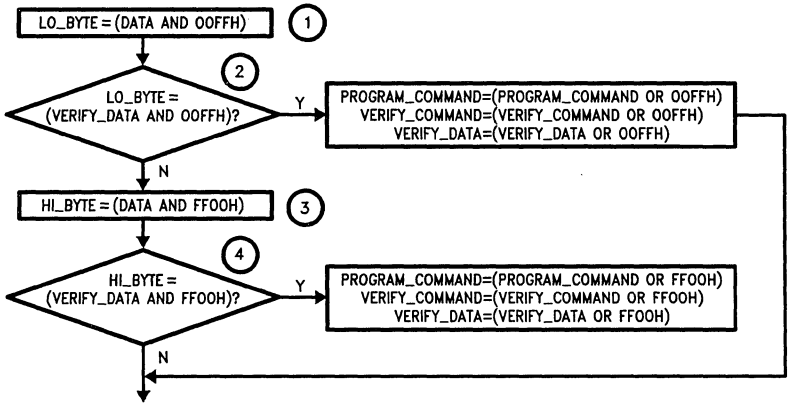
Power Requirements for Interleaving

Current consumption is an important consideration for interleaving. During programming, each device typically consumes 9 mA (1 mA I_{CC} and 8 mA I_{PP}) while programming or erasing; this translates to about 100 mW. If interleaving with 16 devices, about 144 mA (16 devices * 9 mA) or 1.6W, is drawn. Battery powered systems will have a practical limit on the number of components in the interleaving loop. Failure to accommodate these current levels, resulting in V_{PP} voltage drop, will compromise programming and erase reliability.

Write-Once-Read-Many (WORM) Drives

The optical disk is an example of a typical WORM drive application. Its strengths are extremely high densities and low cost per bit. However, it is an unacceptable solution for a low powered, lightweight laptop computer system. It is this environment that solid-state drives offer the greatest benefit. Solid-state ROMs have historically been used in laptop systems to store software programs that seldom change. When the software does change, the ROM "application hardfile" is discarded and a new one is programmed.

Unlike the ROM drive, Intel Flash Memories can be reused and reprogrammed in a true WORM fashion. A computer user can load favorite software programs on the flash memory drive. Adding revised programs to the drive is accomplished by writing to the next free space or by erasing and reprogramming the entire drive. Software drivers can be written to implement this functionality in most operating systems.



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NOTES:
1. MASK the HI Byte with 00H.
2. If the LO Byte verifies, then mask the data, program, and verify command with 00FFH (RESET).
3. Mask the LO Byte with 00H.
4. If HI Byte verifies, then mask the data, program, and verify command with 00FFH (RESET).

Figure 36. 16-Bit Masking for Verify Operation

Microsoft has a flash memory file system for DOS. It stores and retrieves data or application programs in a manner that, to the end user, appears similar to a disk drive. Employing "WORM" functional characteristics, new files are written sequentially from beginning of memory. However, when the disk is full, it can be erased (saving the "good" files) and reused.

When an application accesses a disk through INT 21H, the MS-DOS* kernel checks the drive letter (Figure 37). If the drive has been declared as a flash memory disk, the Installable File System (IFS) intercepts the call. (This is very similar for accesses to a networked drive.) Otherwise, if the drive letter is that of a floppy or hard disk, the call is handled by the standard DOS block device driver. The Installable File System (IFS) provides the link between DOS and the Microsoft* Flash File System driver. (The Flash File System and Installable File System Driver are purchased through Microsoft.) It changes all DOS commands into a form understood by this unique file structure.

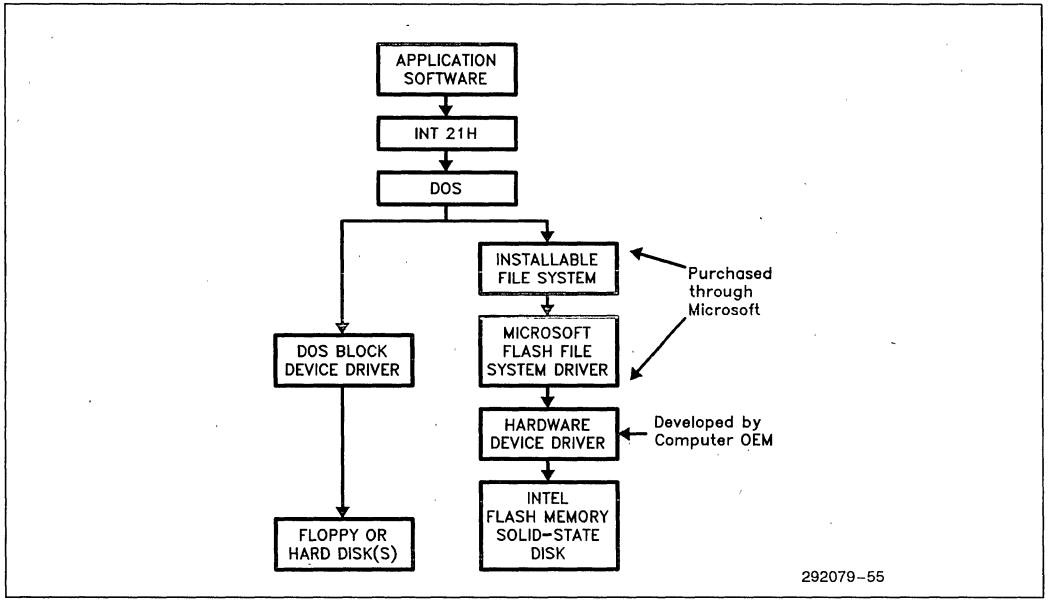

Figure 37. Disk Interface Levels

*MS-DOS® and Microsoft® are registered trademarks of Microsoft Corporation.

The Flash File System Driver is the "intelligence" of this file system. It consists of:

1. A Boot Record that identifies the file system and version, and locates the start of the data area;
2. The Root Directory Entry Record and many Directory and File Entry Records.

The file system driver is independent of the hardware interface to the flash memory disk. The hardware device driver, developed by the OEM or BIOS software vendor, interfaces the flash memory disk to the flash file system. It is responsible for the low level calls to the Intel flash memory devices. The actual implementation of the interface is dependent on the hardware configuration of the disk (I/O, paged, and linear addressing are examples).

The flash memory drive is treated as a WORM drive with a bulk erase feature. To minimize fragmentation losses and allow arbitrary extension of files, the flash memory file system uses variable sized blocks rather than the standard sector/cluster method of more traditional file systems. The fundamental structure employed to offer this flexibility is based on linked list concepts; files are chained together using address pointers located within directory entries for each file.

Files and directories are written to the flash memory disk using sequentially free memory locations—a stack-like operation (Figure 38). Furthermore, file sizes can be variable, abandoning the traditional sector/cluster approach of DOS. When "the stack" is full, the user copies the desired files to another disk and erases the current disk for reuse.

File and subdirectory information is attached to the beginning of each file, unlike the standard DOS approach of directory and FAT placement. As directory and file entries are added, they are located by building a linked-list. Besides containing the customary fields (e.g., name, extension, time, date of creation, etc.), a directory and file entry contains a status byte and various pointers used for the linked-list process. The status byte, besides indicating whether a file/subdirectory exists or is deleted, is also used to signify valid sibling and/or child pointers and to determine if a directory entry pertains to a file or a directory.

When a directory or file is requested or added, the flash memory disk is searched beginning at the bottom of the linked-list. The chain is followed from pointer to pointer until the correct entry is found. If the search arrives at the chain's end (an FNULL is encountered), the system responds analogously to DOS with a "File not found" message.

This linked-list chain consists of two basic types of pointers: sibling and child. Sibling pointers are used to locate directories or files at the same hierarchial level. Child pointers are used to locate subdirectories or the first file of a particular directory. The following examples elaborate these concepts.

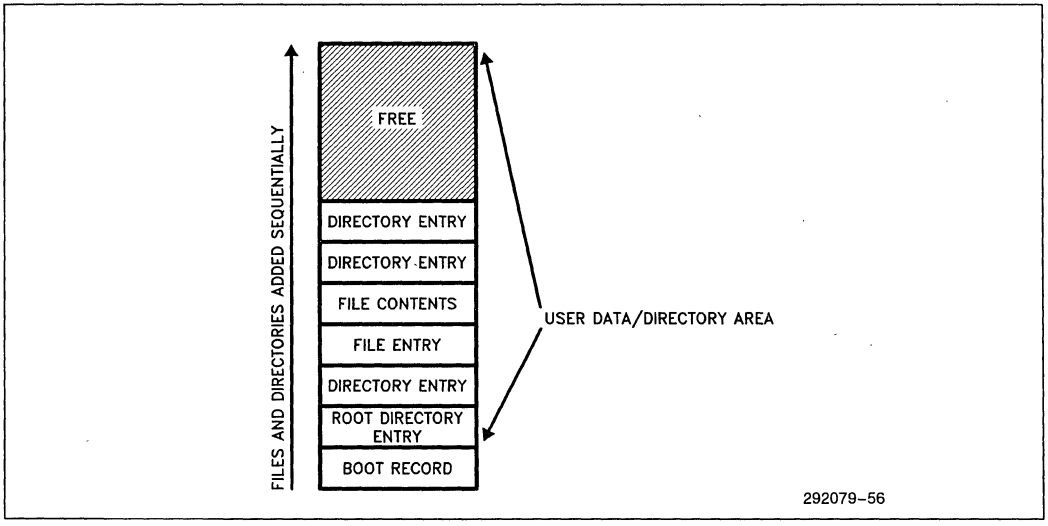

Figure 38. FFS Storage

In Figure 39, Directories B and C are subdirectories of Directory A. Specifically, Directory C is a sibling of Directory B and both are children of Directory A. FNULL indicates the end of the chain.

Figure 40 shows two files (File A and File B) added to a directory (Directory A). File A and File B are at the same level, therefore they are siblings. A file's directory entry contains a Primary and Secondary pointer that indicates the start of its data area.

An important function of FFS is related to deleting or renaming files. Each file's directory entry contains a primary and secondary pointer. When a file is first created, the primary pointer is set to point to the beginning of the data. If that file is modified and rewritten to the flash memory disk (because the original file cannot be overwritten), the primary pointer is marked as invalid (in the status byte). To make use of the existing directory entry for that file, the secondary pointer is used (see Figure 41).

When a file appears multiple times (because of deleted versions) on the flash memory disk, the file system must find the most recent version. The status byte contains bit fields that indicate whether that particular file is a valid or deleted file. The directory information of a deleted file is used for pointers of the linked list and the search would proceed until the most recent version is found.

A key point to be made for using this method of file storage is that the user is in control of the rate in which the disk becomes full; using the flash memory disk predominantly for application code storage and non-temporary data files reduces the frequency of disk "clean-up". However, flash memory will typically perform 100,000 cycles and eliminates reliability concerns when used as a hard or floppy disk replacement.

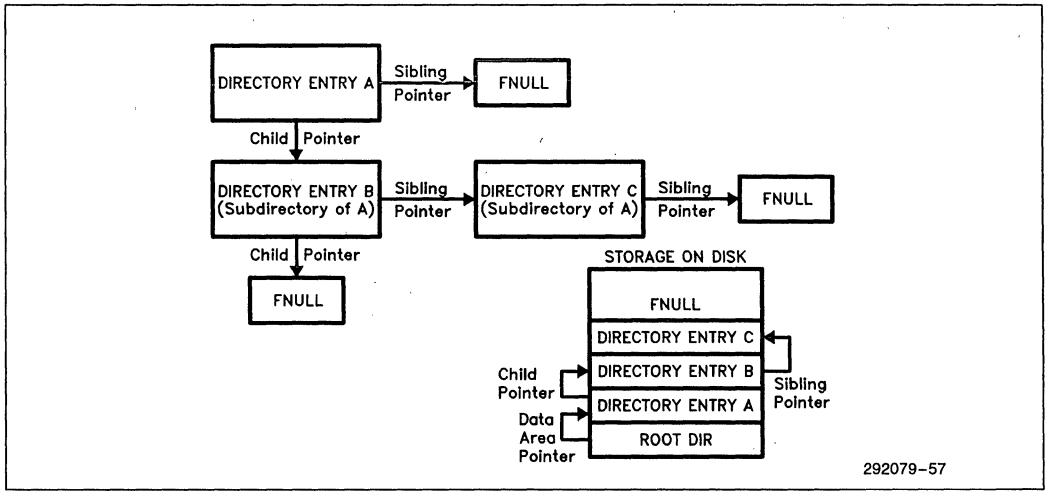

Figure 39. Directory Arrangement

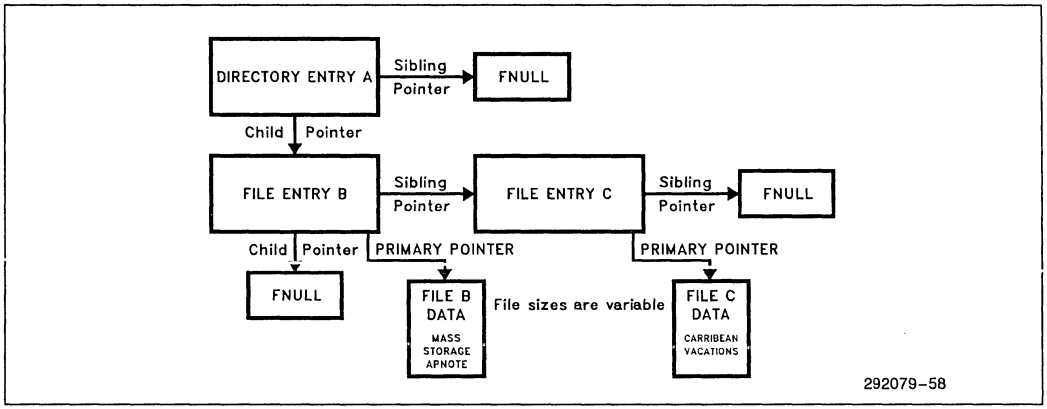

Figure 40. File Arrangement

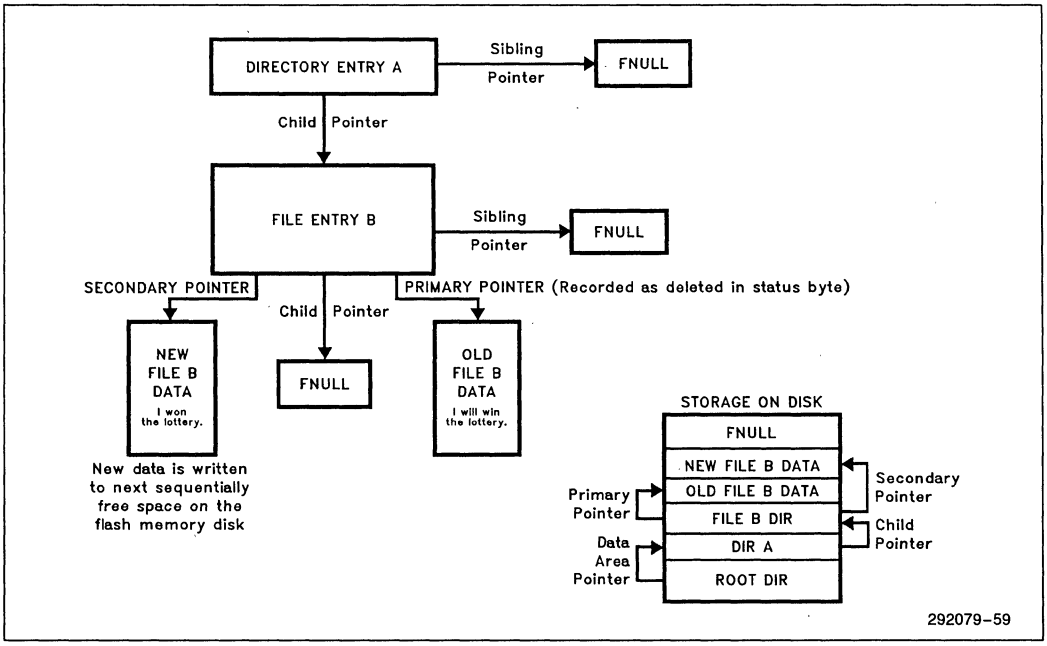

Figure 41. Modifying a File

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Disk Emulation

A disk emulator represents the optimal use of flash memory as a mass storage medium. However, this also embodies the most sophisticated software implementation. Block erasability of flash memory requires modifications to the base level constructs of the magnetic disk. Ideally these changes are transparent to the system user.

Creating a Bootable Drive

The startup time of the PC can be decreased by booting from a flash memory disk instead of the magnetic disk. To do this, a "disk-image" is installed on the flash memory disk which is located in the system memory space between C0000H and E0000H (Figure 10). (The "disk image" contains the Boot Record, Directory, and FAT.) This memory space is referred to as Expansion ROM. During the system Power-On-Self-Test (POST), the system searches this memory area for the ROM adapter signature, 055AAh, marking the beginning of the disk image. Once this signature is found, the BOOTSTRAP process begins. The software to create and install this "disk image" is available as a product from Microsoft Corporation as ROM executable MS-DOS.

WHY FLASH?

CHARACTERISTICS OF INTEL FLASH MEMORY

Power consumption, weight, performance, and reliability are the key criteria for a system design. The discussion of Intel flash memory as a mass storage medium would not be complete without a performance analysis and comparison to other technologies.

Power Consumption

Portability of a computer demands battery longevity and consequently minimal power consumption. Small form factor disk drives are being designed specifically for the size and power requirements of laptops.

A drive has three basic operating modes: active, power savings, and standby. The active mode consists of reading, writing, and ready. Ready condition allows "instantaneous" transitions into the read or write states. In the power-savings mode only the drive motor continues to run. Standby shuts off all functionality except for the circuitry needed to "spin-up" the drive. From the standby mode, extra power and considerable time, is required to "spin-up" the disk.

Power Consumption Comparison (Watts)

(Based on typical performance characteristics. The 20 Mbyte Flash Memory disk is based on the use of 80-28F020s. Only two of the forty devices are accessed at a time, the remainder are in standby mode.)

Active Modes	Hard Disk Drive (2.5", 20 Mbytes)	INTEL Flash Memory (20 Mbytes)
Ready	1.7–2.0	0.05 (Same as Standby)
Read	3.5-4.0	0.15
Write	3.5–4.0	0.25
Power Savings	1.5	0.05 (Same as Standby)
Standby	0.1–0.5	0.05
Spinup (from Standby)	9.3	0

For a battery-powered system, 3–4 hours of operation is unacceptable. Battery longevity is achieved by using Intel Flash Memory solid-state storage as a disk replacement. The following table relates battery life and the different functions of disk operation. A "AA" battery with a capacity of 2215 mAH is used for the comparison. Obviously, for a truly accurate representation, other components of the system should be included. But from the data storage point of view, the flash memory disk will operate many more hours than the hard disk drive on a set of batteries.

Hours of Operation for a "AA" Battery (Based on Data from Previous Table and 2215 mAH Battery Capacity)

	Hard Disk Drive (2.5", 20 Mbytes)	INTEL Flash Memory (20 Mbytes)
Read	0.83	22.15
Write	0.83	13.29
Standby	6.64	66.45

Data Access Time

Reading data from a magnetic disk is a very slow process compared to a solid-state disk (SSD). Disk transfer time is lengthy due to four time components: spin-up, seek time, latency, and data transfer time. Spin-up is a factor to consider for battery-powered systems, where most disk accesses are begun from the standby mode. During the seek time, the arm is repositioned to the correct track. Latency is the delay from arm repositioning until the first sector of the transfer moves under the

read/write head. This is dependent on the speed of rotation. The actual transfer of data is the third component. The standard SCSI interface transfers data between 5 Mbits and 10 Mbits per second, with which flash memory compares very favorable.

For this example it is reasonable to assume a transfer rate of 1.0 Mbytes per second. Using a full word-wide (x16) bus bandwidth (120 ns access speed of the device), flash achieves a transfer rate of 16.6 Mbytes per second.

Read Speed Comparisons

	Hard Disk (Standard SCSI Interface)	Floppy Disk	Flash Memory (16-Bit Bus, 120 ns Access)
Seek Time	28 ms		0
Latency	8.3 ms	100 ms	0
Transfer Rate	1.0 Mbyte/s	62 Kbyte/s	16.6 Mbyte/s
Total for 10 Kbyte File	46.54 ms	261.3 ms	0.62 ms

(Floppy disk drive specifications combine access into one category.)

In this example, the flash memory disk has 75 times the read performance over the hard disk. Smaller files result in even greater differences. Additionally, the 5 second spin-up of the hard disk gives the flash memory disk over 8,000 times the performance!

A byte will typically program in Intel Flash Memory in one pulse. (See Intel Flash Memory Data sheet for programming algorithm.) Based on this and the parameters used in the example above, a 10 Kbyte file is written to the flash memory disk in 87.04 ms. Because writes to a hard disk typically begin from spin-down, the flash memory disk is still over 50 times faster. Since reads are 80% of disk access, flash memory's user-perceptible performance advantage is substantial.

Reliability

The definition of hard disk mean-time-before-failure (MTBF) is extremely ambiguous. There are no industry-wide standards for making a reliable calculation. Disk drive manufacturers choose whichever method best suits their product's reliability perception.

One method uses the overall mean failure. The MTBF of all critical components is computer analyzed and the lowest one is selected. A second method tests 100 drives. The hours of the first ones to fail are multiplied by the number of drives. How many reads or writes are performed? Is the disk stopped and started during the process? Standard answers do not exist.

The vagueness of the test procedures makes it difficult to compare the MTBF for a flash memory solid-state disk and a hard disk. Based on the fact that disk usage is 80% reads and 20% writes, a reasonable comparison can be made. (What is not taken into account is that disks are an 'infinite' write, but finite read medium. Continuous reading causes reduced magnetic field strength, a failure mechanism hidden by re-writing the disk.)

Intel's Flash Memory typically performs 100,000 erase/program cycles. (Failure does not occur at this point. The only noticeable change is a gradual increase in program and erase times.) Assume a flash memory disk size of 4 Mbytes that functions like a WORM drive; it is erased and reused after filling.

Based on a typical disk MTBF of 50,000 hours and the 80/20% division, 10,000 hours are used for writing files. Assume the average file size written to disk is 10 Kbytes. A 4 Mbyte flash disk can store approximately 400 × 10 Kbyte files (4 Mbyte/10K = 408) before erasure is necessary.

These 400 files could be writen to the disk 40×10^6 times − (400 files × 100,000 cycles = 40×10^6). The result is that within a 10,000 hour period, one 10 Kbyte file could be written once every 0.9 seconds.

$$\frac{10{,}000 \text{ hours}}{40 \times 10^6 \text{ Files}} \times \frac{3600 \text{ Seconds}}{1 \text{ Hour}} = \frac{0.9 \text{ Seconds}}{\text{File}}$$

It would be more realistic (although still extremely aggressive) to assume that this 10 Kbyte file is written to this disk every 10 minutes. At 100,000 cycles, 40×10^6 files will have been written. The MTBF can be calculated as follows:

$$40 \times 10^6 \text{ Files} \times \frac{10 \text{ Minutes}}{\text{File}} \times \frac{1 \text{ Hour}}{60 \text{ Minutes}} = 6.6 \times 10^6 \text{ Hours}$$

This is an MTBF of over 6 million hours! (See Reliability Report RR60 for more details.)

A flash memory solid-state disk outlasts its mechanical counterpart by at least two orders of magnitude, especially if head parking problems and limited start/stop cycles of the mechanical disk are taken into account.

6

Weight

Lowering the power consumption of your portable system also lowers the weight. Reduced battery demands mean smaller and lighter batteries and power supplies. Weight savings is also gained by the proper choice of the mass storage medium. The small 20 Mbyte 2.5″ disk drives weigh between 9 and 21 ounces. The equivalent capacity of flash memory using 80-2 Mbit TSOPs (which individually weigh 1.16×10^{-2} ounces) weighs 0.93 ounces plus the weight of the circuit board. (See section on Intel flash memory packaging.) This difference is critical when the computer weight requirement is under five (5) pounds.

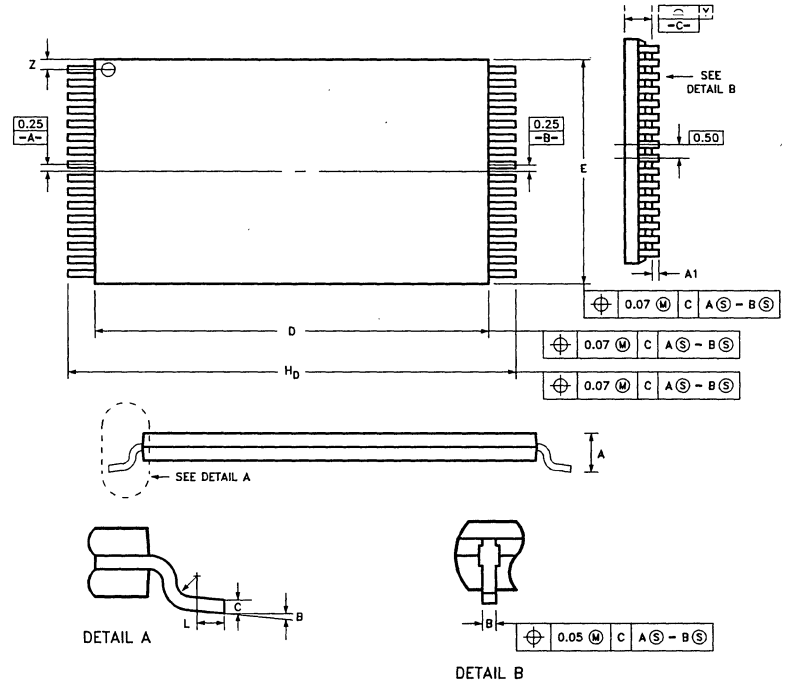
SUMMARY

The advent of Intel Flash Memory has led to the evolution of solid-state mass storage. This application note has provided the building blocks that will allow the innovative manufacturer to remain on the forefront of technology.

- Advanced packaging, such as the TSOP, SIMM, and IC memory cards, is necessary for high-density applications.
- Intel Flash Memory allows flexible system interfacing by using I/O, paged, or linear addressing methods.
- Software variations enable an unlimited number of mass storage applications for Intel Flash Memory.
- Intel Flash Memory offers superior performance over the magnetic disk.

APPENDIX A

TSOP Dimensions



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Symbol	Description	Dimensions in mm		
		Min	Nom	Max
A	Package Height			1.27
A_1	Standoff	0.15	0.20	0.25
A_2	Package Body Height	0.96	1.01	1.06
B	Lead Width	0.15	0.20	0.30
C	Lead Thickness	0.10	0.15	0.20
D	Package Body Length	18.20	18.40	18.60
E	Package Body Width	7.80	8.00	8.20
H_D	Terminal Dimension	19.80	20.00	20.20
L	Lead Tip Length	0.30	0.33	0.35
N	Lead Count		32	
Y	Seating Plane Coplanarity	0.00		0.10
Z	Lead to Package Offset	0.20	0.25	0.30
Ø	Lead Tip Angle	1	3	5

TSOP Physical Dimensions Drawings and Specifications

TSOP Sockets and Wands

32-Lead TSOP test sockets are available from the following vendors:

Yamaichi Eletronics
1420 Koll Circle, Suite B
San Jose, CA 95112
(408) 452-0797

Enplas
Distributed by:
Tesco International Inc.
1825 S. Grant Street, Suite 745
San Mateo, CA 94402
(415) 572-1683

32-Lead TSOP to DIP adapter sockets are available from the following vendor:

California Integration Coordinators Inc.
582 Main Street
Placerville, CA 95667
(916) 626-6168

Suction wands for transferring units are available from the following vendor:

H-Square Corp.
1289-H Reamwood Avenue
Sunnyvale, CA 94089

1	V_{SS}	21	$\overline{CE3}$	41	A_{11}	61	DQ9
2	V_{CC}	22	$\overline{CE2}$	42	A_{10}	62	DQ8
3	V_{PP}	23	$\overline{CE1}$	43	A_9	63	DQ7
4	$\overline{OE}$	24	$\overline{CE0}$	44	A_8	64	DQ6
5	$\overline{WEH}$	25	V_{SS}	45	A_7	65	DQ5
6	$\overline{WEL}$	26	NC	46	A_6	66	DQ4
7	NC	27	NC	47	A_5	67	DQ3
8	RES	28	NC	48	A_4	68	DQ2
9	RES	29	NC	49	A_3	69	DQ1
10	RES	30	NC	50	A_2	70	DQ0
11	RES	31	NC	51	A_1	71	V_{PP}
12	RES	32	NC	52	A_0	72	V_{CC}
13	RES	33	NC	53	RES	73	PD1
14	RES	34	NC	54	V_{SS}	74	PD2
15	RES	35	NC	55	DQ15	75	PD3
16	RES	36	A_{16}	56	DQ14	76	PD4
17	RES	37	A_{15}	57	DQ13	77	PD5
18	RES	38	A_{14}	58	DQ12	78	PD6
19	RES	39	A_{13}	59	DQ11	79	PD7
20	RES	40	A_{12}	60	DQ10	80	V_{SS}

Figure 43. iSM001FLKA (1 Mbyte SIMM) Pinout

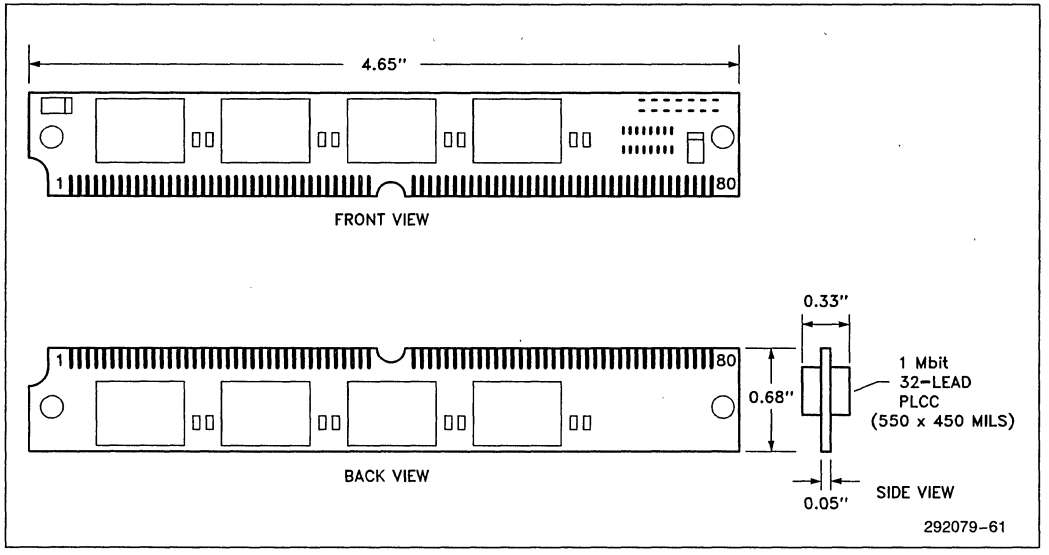


Figure 44. iSM001FLKA (1 Mbyte SIMM) Dimensions

Module Capacity Idenfitication

Module Capacity Word Depth	PD6	PD2	PD1
No Module	O	O	O
256K/32M	O	O	S
512K/64M	O	S	O
1M/128M	O	S	S
2M/256M	S	O	O
4M/512M	S	O	S
8M/1G	S	S	O
16M/2G	S	S	S

Module Speed Identification

Maximum Access Time	PD7	PD5	PD4	PD3
>300 ns	S	S	S	S
300 ns	S	S	S	O
250 ns	S	S	O	S
200 ns	S	S	O	O
185 ns	S	O	S	S
150 ns	S	O	S	O
135 ns	S	O	O	S
120 ns	S	O	O	O
100 ns	O	S	S	S
85 ns	O	S	S	O
70 ns	O	S	O	S
60 ns	O	S	O	O
50 ns	O	O	S	S
40 ns	O	O	S	O
30 ns	O	O	O	S
ND	O	O	O	O

O = Open Circuit On Module
S = Short Circuit to Ground on Module
ND = Not Defined

```
EPLD ADF for Presence Detect WAIT-State Generator
PLFG Applications    1-800-323-EPLD
Intel Corp.
June 6, 1990
U999
002
85C220
Pre-loadable wait state down counter/READY generator
OPTIONS: TURBO = ON

PART: 85C220

INPUTS: CLK@1, nLOAD@2, PD7@3, PD6@4, PD5@5, PD4@6
OUTPUTS: nREADY@19, Q3@18, Q2@17, Q1@16, Q0@15, nDL@14

NETWORK:
    CLK = INP(CLK)              % System clock input %
    nLOAD = INP(nLOAD)          % Load count input %
    PD7 = INP(PD7)              % PD[7:4] Wait state %
    PD6 = INP(PD6)              % count size inputs %
    PD5 = INP(PD5)              % to lookup table %
    PD4 = INP(PD4)
    nREADY, nREADY = RORF(nREADYd,CLK,GND,GND,VCC) % /READY Output %

    Q3,Q3 = RORF (Q3d,CLK,GND,GND,VCC)          % counter outputs . . . %
    Q2,Q2 = RORF (Q2d,CLK,GND,GND,VCC)          % not externally %
    Q1,Q1 = RORF (Q1d,CLK,GND,GND,VCC)          % necessary %
    Q0,Q0 = RORF (Q0d,CLK,GND,GND,VCC)
    nDL,nDL = RORF (nDLd,CLK,GND,GND,VCC)

EQUATIONS:
    Q0d = Q0EQN * !READY * !COUNT_ZERO          % count if not ready %
        + Q0 * (READY + !LOAD)                  % hold if ready %
        + X0 * LOAD * !READY * COUNT_ZERO;      % read inputs on LOAD %
        Q0EQN = !Q0;

    Q1d = Q1EQN * !READY * !COUNT_ZERO
        + Q1 * (READY + !LOAD)
        + X1 * LOAD * !READY * COUNT_ZERO;
        Q1EQN = Q1 * Q0 + !Q1 * !Q0;

    Q2d = Q2EQN * !READY * !COUNT_ZERO
        + Q2 * (READY + !LOAD)
        + X2 * LOAD * !READY * COUNT_ZERO;
        Q2EQN = Q2 * (Q1 + Q0) + !Q2 * !Q1 * !Q0;

    Q3d = Q3EQN * !READY * !COUNT_ZERO
        + Q3 * (READY + !LOAD)
        + X3 * LOAD * !READY * COUNT_ZERO;
        Q3EQN = Q3 * (Q2 + Q1 + Q0) + !Q3 * !Q2 * !Q1 * !Q0

    nREADYd' = !Q3 * !Q2 * !Q1 * LOAD * !nDL;   % Anticipate counter %
                                                % to provide READY%
    nDLd = nLOAD;                               % hold until LOAD is%
                                                % taken away %
```

EPLD ADF for Presence Detect WAIT-State Generator

6

```
    COUNT_ZERO = !Q3 * !Q2 * !Q1 * !Q0;
    LOAD = NLOAD';
    READY = nREADY';

    X3 = GND;                                    % Wait State Scrambler %
    X2 = 3CNT;                                   % lookup table %
    X1 = 8CNT + 7CNT + 6CNT + 5CNT;
    X0 = 5CNT;

    8CNT =  PD7 * !PD6 * !PD5 * !PD4;
    7CNT = !PD7 *  PD6 *  PD5 *  PD4;
    6CNT = !PD7 *  PD6 *  PD5 * !PD4;
    5CNT = !PD7 *  PD6 * !PD5 *  PD4;
    4CNT = !PD7 *  PD6 * !PD5 * !PD4;
    3CNT = !PD7 * !PD6 *  PD5 *  PD4;
    2CNT = !PD7 * !PD6 *  PD5 * !PD4;

END$
```

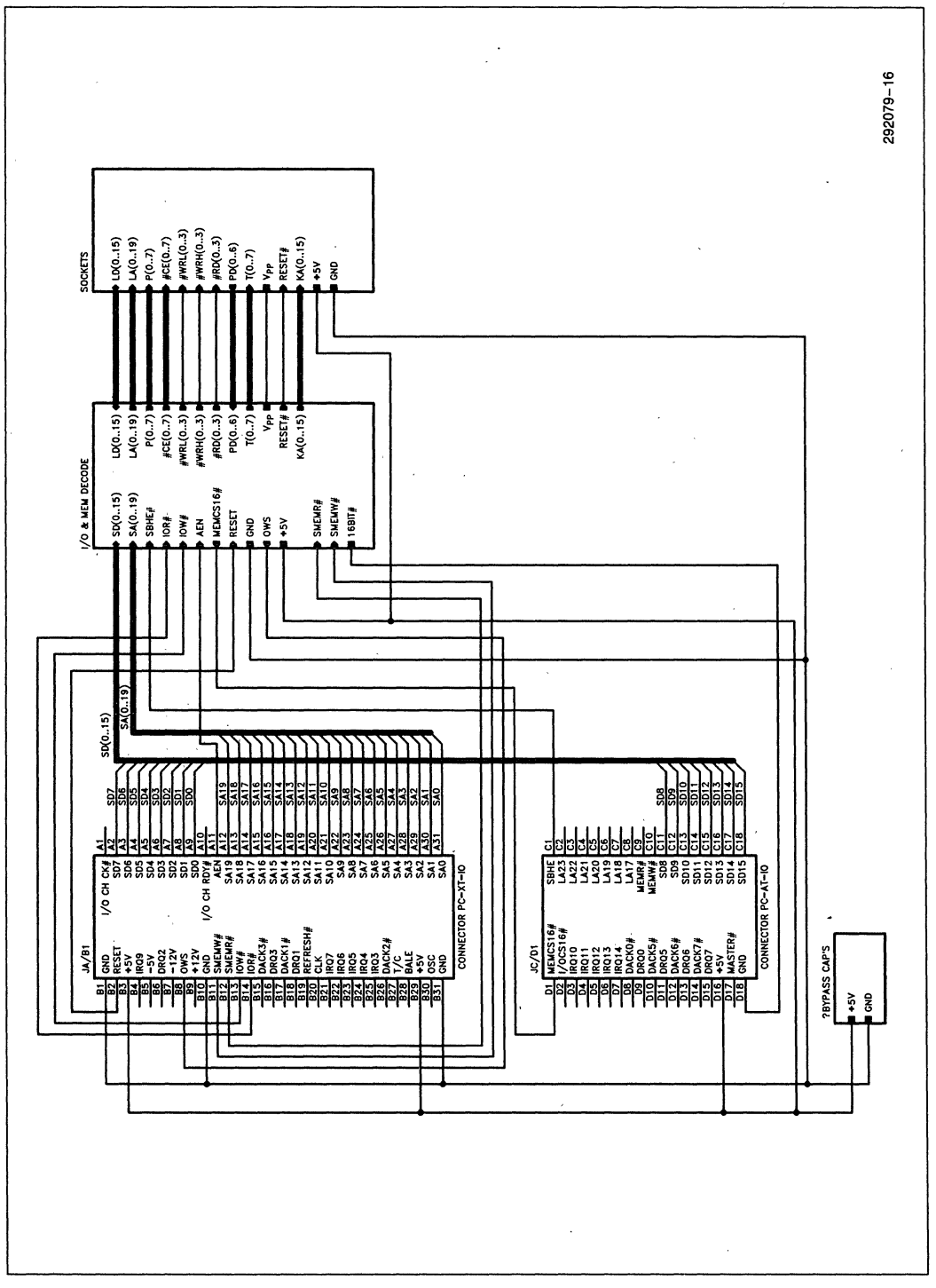
EPLD ADF for Presence Detect WAIT-State Generator (Continued)

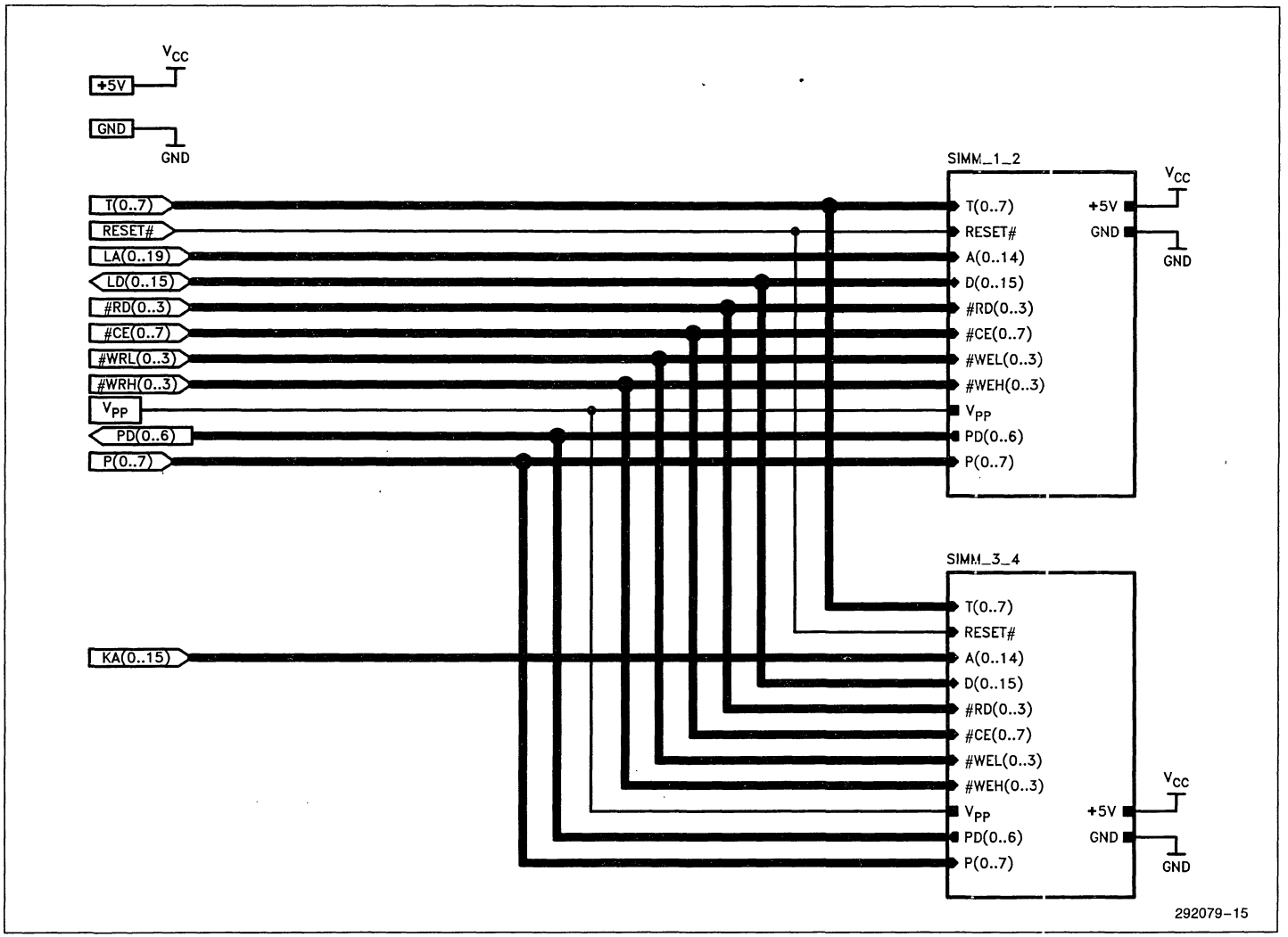
Decoding Truth Table for "Multiplexing" Data Bus of PCMCIA/JEIDA Memory Card

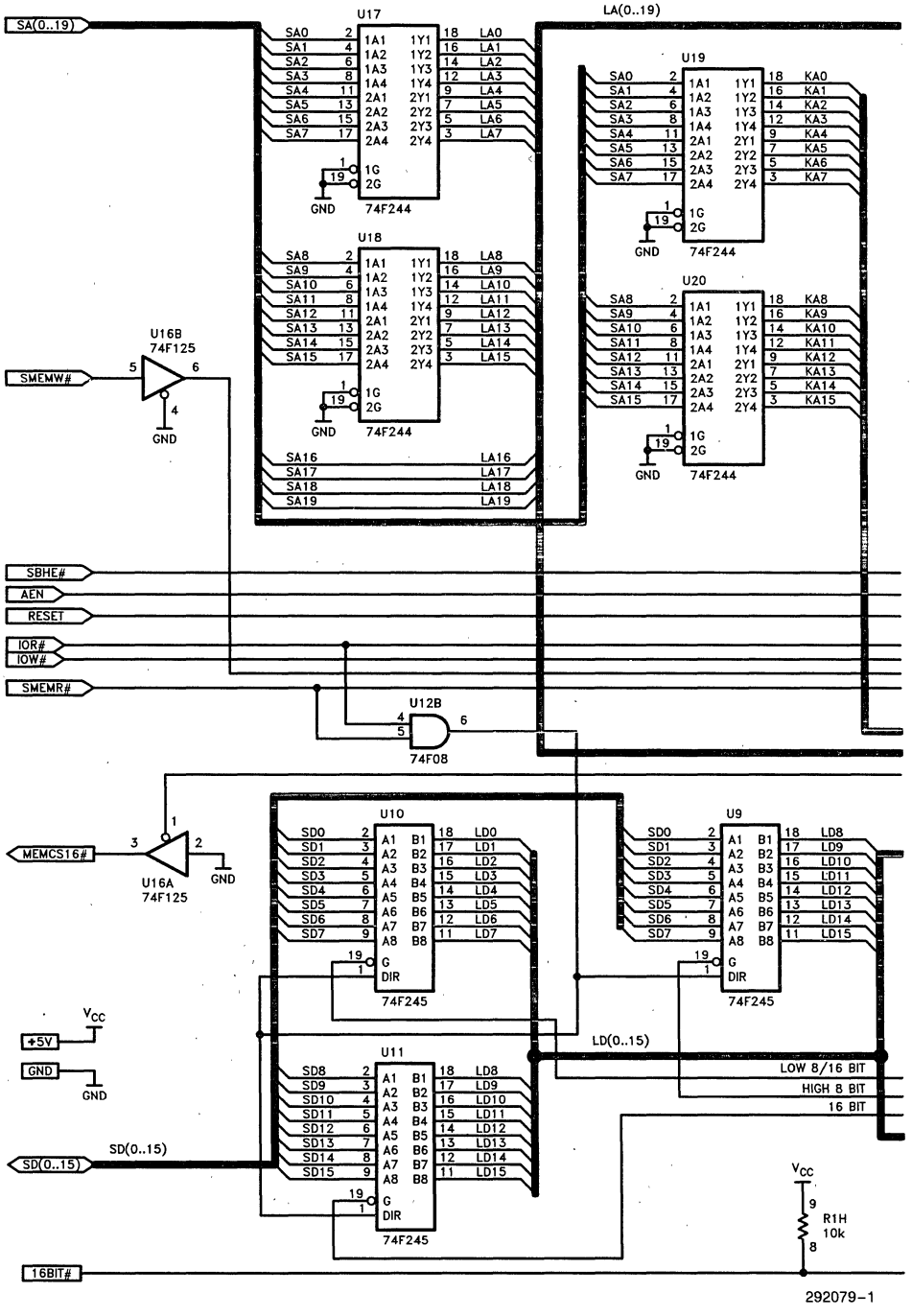
System Bus Width	Data Transfer	$\overline{CSH}$	$\overline{CSL}$	A_0	1	2	3
8 or 16	None	1	1	x	1	1	1
8 or 16	Lo-Byte	1	0	0	0	1	1
8	Hi-Byte to Lo-Byte	1	0	1	1	0	1
16	Hi-Byte	0	1	x	1	1	0
16	Low and High Byte	0	0	x	0	1	0

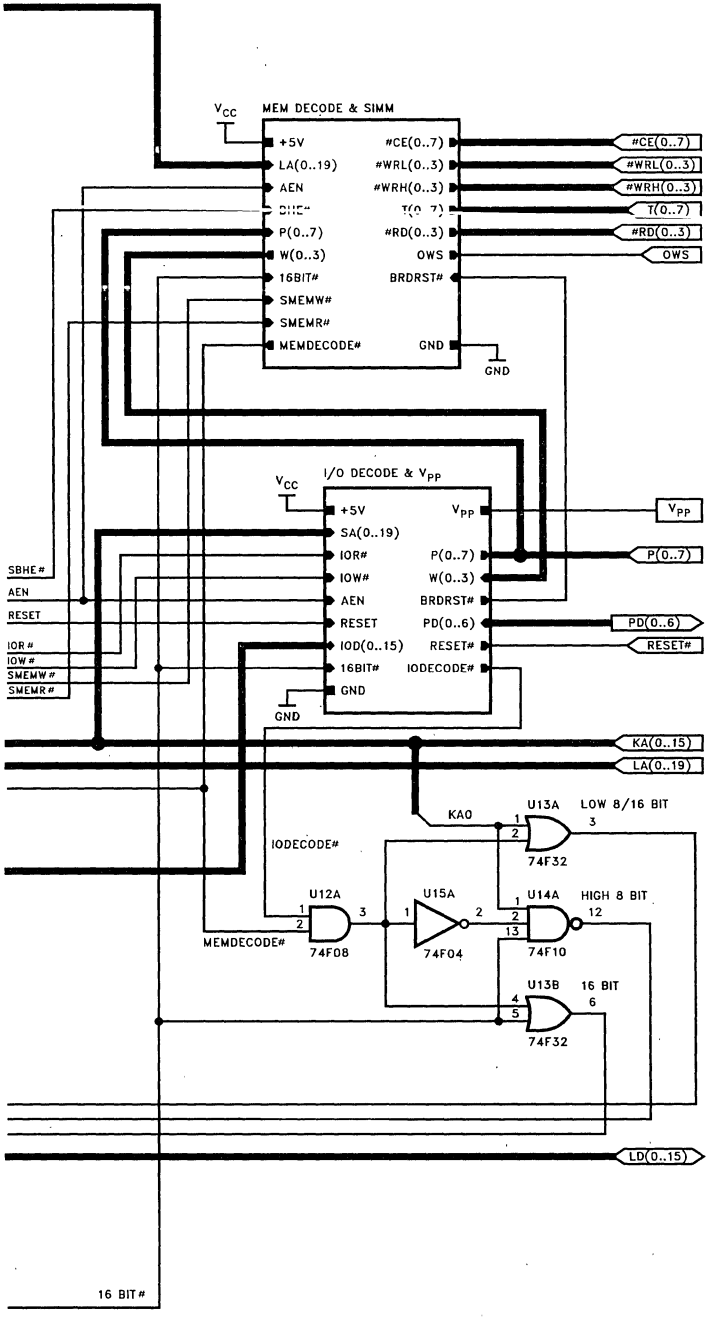
NOTE:
References Figure 8 in Memory Card Section.

PAGE MEMORY BOARD SCHEMATICS


292079-16
SOCKETS
LD(0..15)
LA(0..19)
P(0..7)
#CE(0..7)
#WRL(0..3)
#WRH(0..3)
#RD(0..3)
PD(0..6)
T(0..7)
VPP
RESET#
KA(0..15)
+5V
GND
I/O & MEM DECODE
SD(0..15)
SA(0..19)
SBHE#
IOR#
IOW#
AEN
MEMCS16#
RESET
GND
OWS
+5V
SMEMR#
SMEMW#
16BIT#
SD(0..15)
SA(0..19)
JA/B1
I/O CH CK#
RESET
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW#
SMEMR#
IOW#
IOR#
DACK3#
DRQ3
DACK1#
DRQ1
REFRESH#
CLK
IRQ7
IRQ6
IRQ5
IRQ4
DACK2#
T/C
BALE
+5V
OSC
GND
I/O CH RDY#
AEN
CONNECTOR PC-XT-IO
JC/D1
MEMCS16#
I/OCS16#
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
DACK0#
DRQ0
DACK5#
DRQ5
DACK6#
DRQ6
DACK7#
DRQ7
+5V
MASTER#
GND
SBHE
LA23
LA22
LA21
LA20
LA19
LA18
LA17
MEMR#
MEMW#
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
CONNECTOR PC-AT-IO
?BYPASS CAP'S
+5V
GND

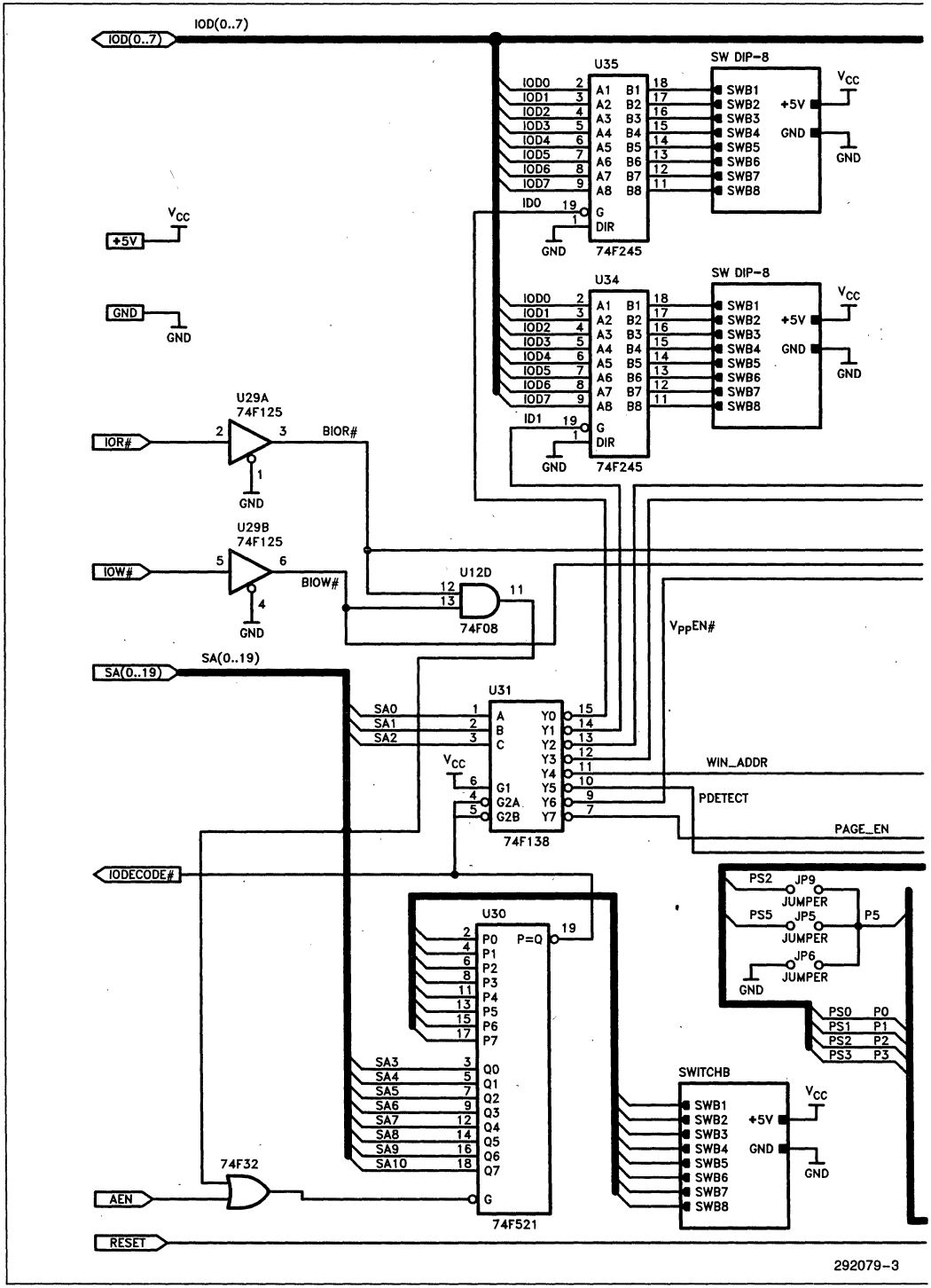

VCC
+5V
GND
GND
T(0..7)
RESET#
LA(0..19)
LD(0..15)
#RD(0..3)
#CE(0..7)
#WRL(0..3)
#WRH(0..3)
VPP
PD(0..6)
P(0..7)
KA(0..15)
SIMM_1_2
T(0..7)
RESET#
A(0..14)
D(0..15)
#RD(0..3)
#CE(0..7)
#WEL(0..3)
#WEH(0..3)
VPP
PD(0..6)
P(0..7)
+5V
GND
VCC
GND
SIMM_3_4
T(0..7)
RESET#
A(0..14)
D(0..15)
#RD(0..3)
#CE(0..7)
#WEL(0..3)
#WEH(0..3)
VPP
PD(0..6)
P(0..7)
+5V
GND
VCC
GND
292079-15

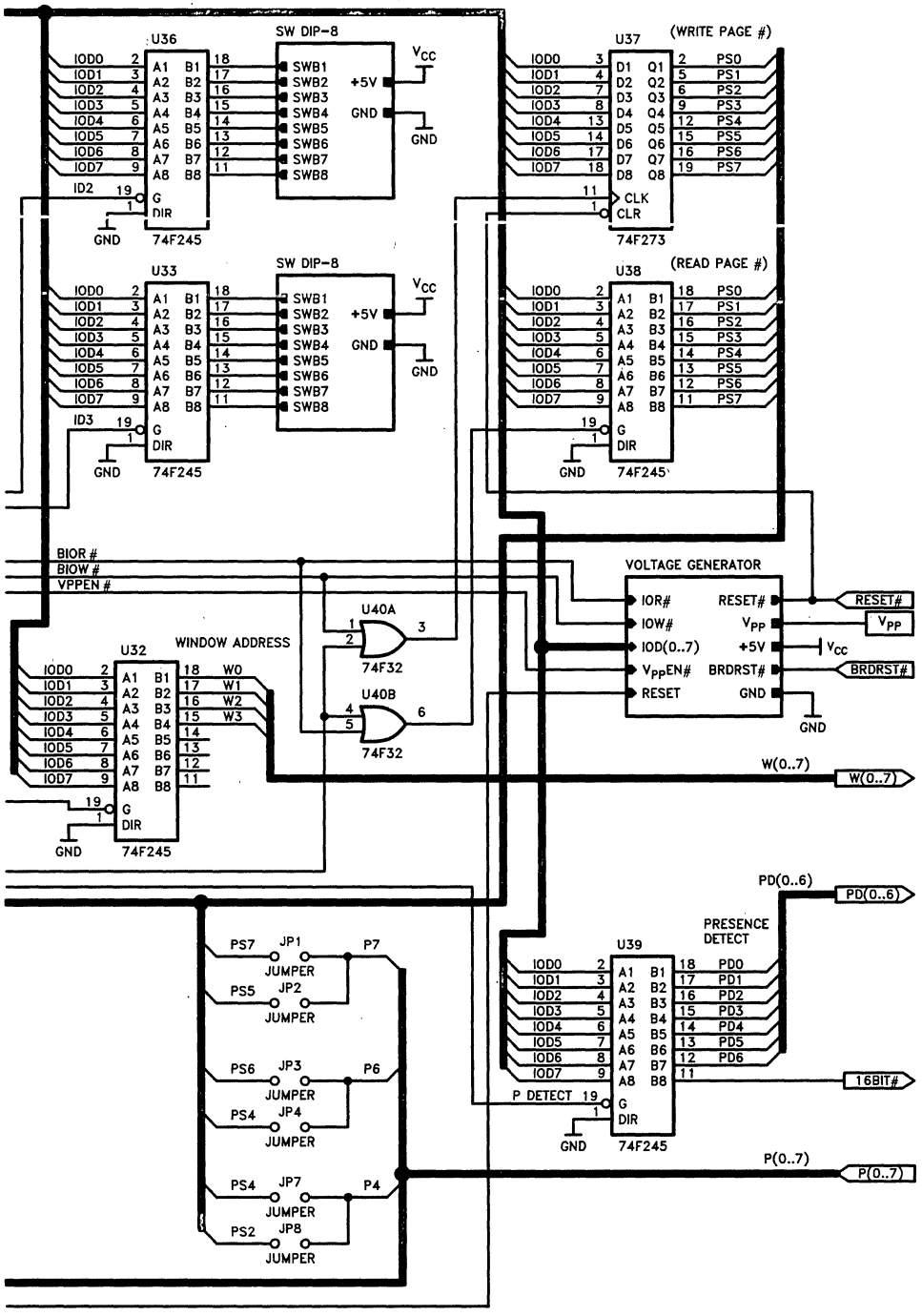

SA(0..19)
LA(0..19)
U17
U18
U19
U20
74F244
GND
U16B
74F125
SMEMW#
SBHE#
AEN
RESET
IOR#
IOW#
SMEMR#
U12B
74F08
MEMCS16#
U16A
74F125
U10
U11
U9
74F245
LD(0..15)
LOW 8/16 BIT
HIGH 8 BIT
16 BIT
SD(0..15)
VCC
+5V
R1H
10k
16BIT#
292079-1

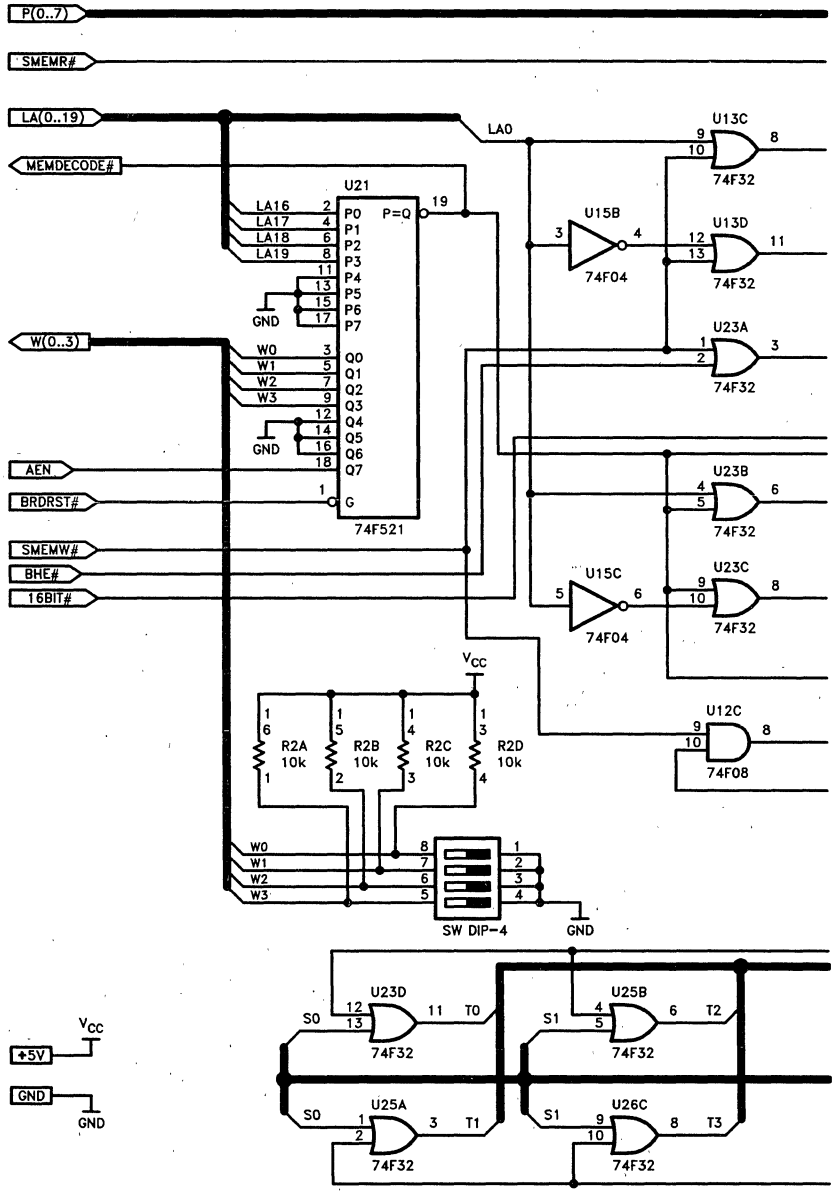

MEM DECODE & SIMM
+5V
LA(0..19)
AEN
P(0..7)
W(0..3)
16BIT#
SMEMW#
SMEMR#
MEMDECODE#
#CE(0..7)
#WRL(0..3)
#WRH(0..3)
#RD(0..3)
OWS
BRDRST#
GND
#CE(0..7)
#WRL(0..3)
#WRH(0..3)
#RD(0..3)
OWS
I/O DECODE & VPP
+5V
SA(0..19)
IOR#
IOW#
AEN
RESET
IOD(0..15)
16BIT#
GND
VPP
P(0..7)
W(0..3)
BRDRST#
PD(0..6)
RESET#
IODECODE#
VPP
P(0..7)
PD(0..6)
RESET#
SBHE#
AEN
RESET
IOR#
IOW#
SMEMW#
SMEMR#
KA(0..15)
LA(0..19)
KA0
U13A
LOW 8/16 BIT
74F32
IODECODE#
U12A
74F08
MEMDECODE#
U15A
74F04
U14A
HIGH 8 BIT
74F10
U13B
16 BIT
74F32
LD(0..15)
16 BIT#

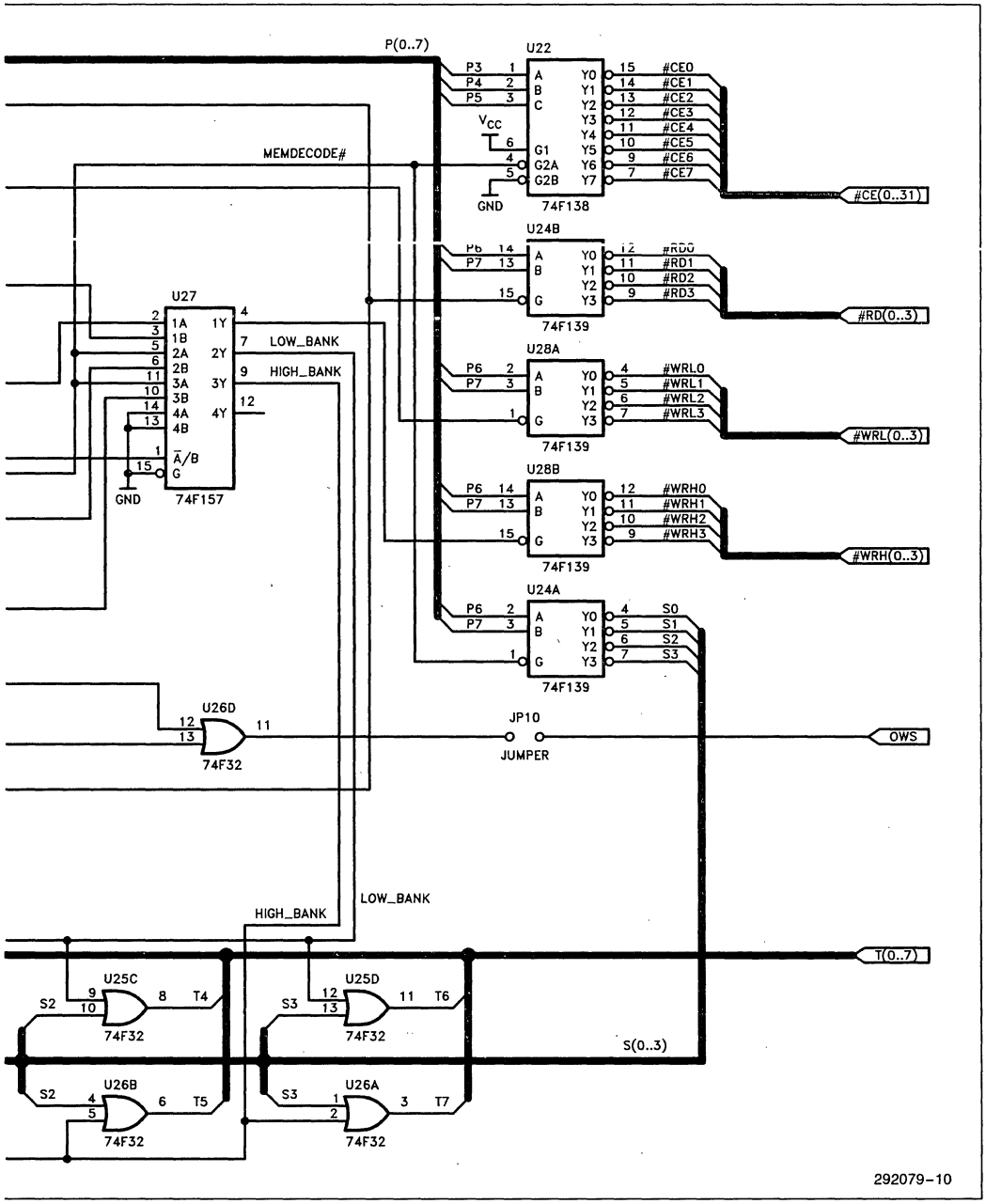
292079-2

6

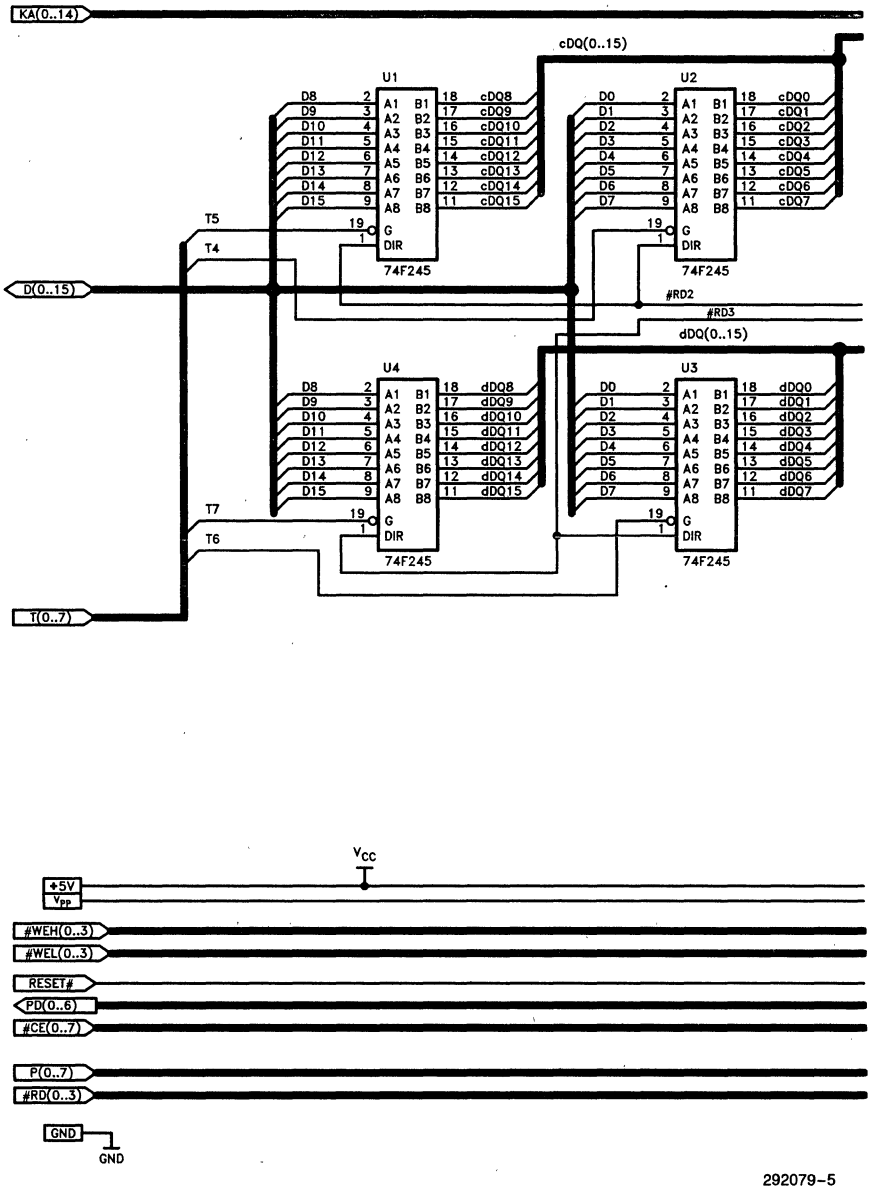

IOD(0..7)
U35
SW DIP-8
74F245
U34
SW DIP-8
74F245
+5V
GND
U29A
74F125
IOR#
BIOR#
U29B
74F125
IOW#
BIOW#
U12D
74F08
SA(0..19)
U31
74F138
VPPEN#
WIN_ADDR
PDETECT
PAGE_EN
IODECODE#
U30
74F521
74F32
AEN
RESET
SWITCHB
JUMPER
292079-3


U36
SW DIP-8
U37
(WRITE PAGE #)
U33
SW DIP-8
U38
(READ PAGE #)
74F245
74F273
BIOR #
BIOW #
VPPEN #
VOLTAGE GENERATOR
U40A
U40B
74F32
WINDOW ADDRESS
U32
RESET#
BRDRST#
W(0..7)
PD(0..6)
PRESENCE DETECT
U39
16BIT#
P(0..7)
JUMPER
JP1
JP2
JP3
JP4
JP7
JP8
292079-4

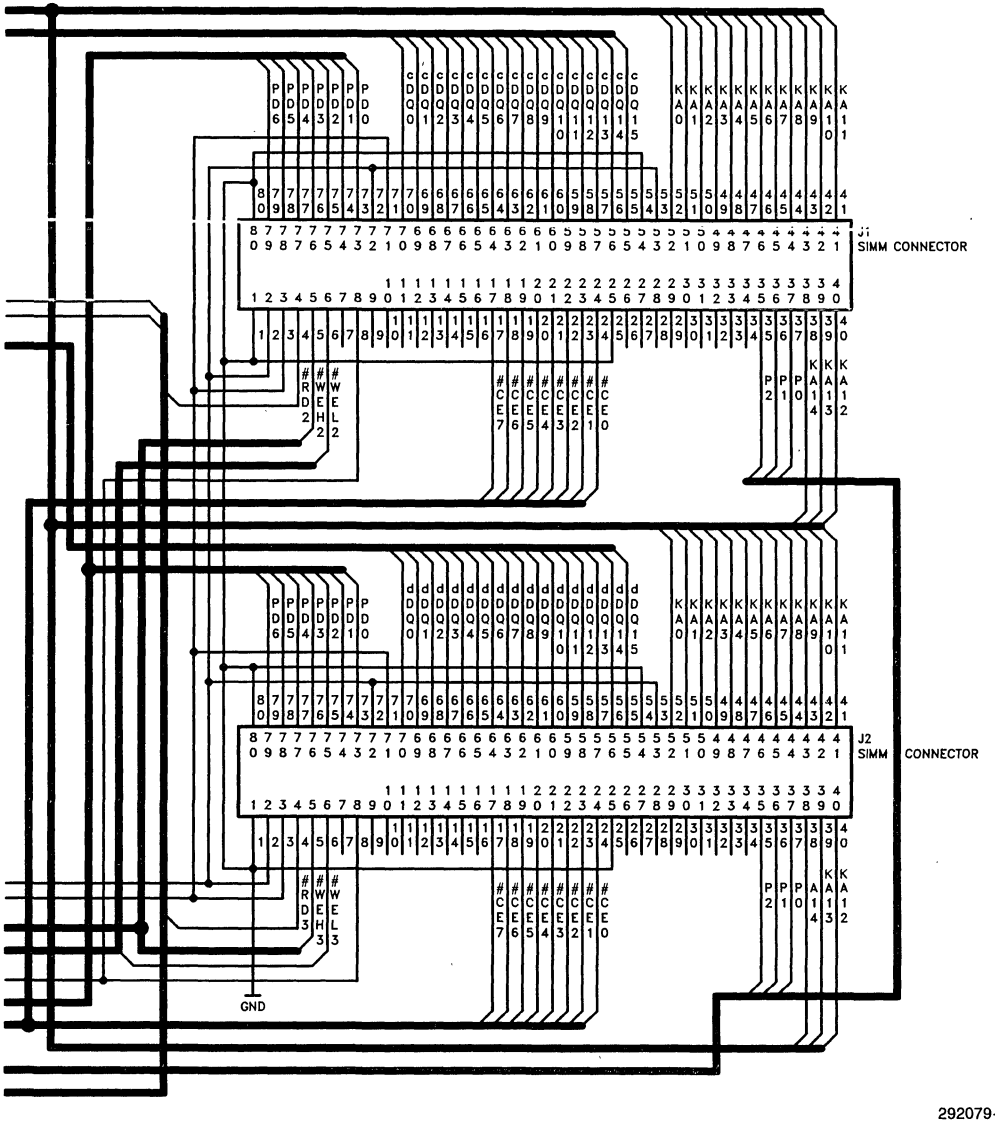

P(0..7)
SMEMR#
LA(0..19)
MEMDECODE#
W(0..3)
AEN
BRDRST#
SMEMW#
BHE#
16BIT#
LA0
U21
74F521
LA16
LA17
LA18
LA19
GND
WO
W1
W2
W3
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
P0
P1
P2
P3
P4
P5
P6
P7
P=Q
G
U13C
U13D
U23A
U23B
U23C
U12C
74F32
74F08
U15B
U15C
74F04
R2A 10k
R2B 10k
R2C 10k
R2D 10k
VCC
SW DIP-4
U23D
U25B
U25A
U26C
S0
S1
T0
T1
T2
T3
+5V
292079-9

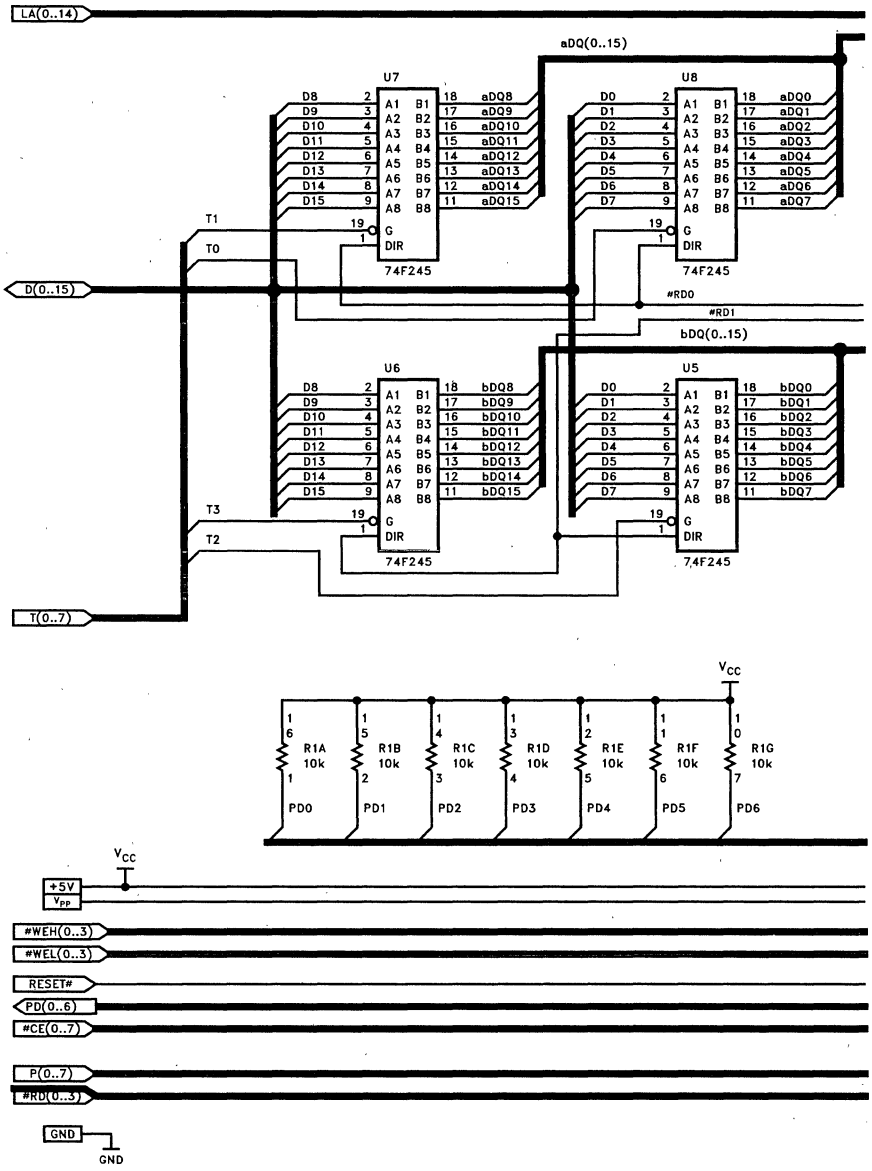

P(0..7)
U22
P3
P4
P5
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
#CE0
#CE1
#CE2
#CE3
#CE4
#CE5
#CE6
#CE7
VCC
GND
74F138
#CE(0..31)
MEMDECODE#
U24B
P6
P7
G
#RD0
#RD1
#RD2
#RD3
74F139
#RD(0..3)
U27
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
A/B
G
LOW_BANK
HIGH_BANK
74F157
U28A
#WRL0
#WRL1
#WRL2
#WRL3
#WRL(0..3)
U28B
#WRH0
#WRH1
#WRH2
#WRH3
#WRH(0..3)
U24A
S0
S1
S2
S3
U26D
74F32
JP10
JUMPER
OWS
HIGH_BANK
LOW_BANK
T(0..7)
U25C
T4
U25D
T6
S(0..3)
U26B
T5
U26A
T7

292079-10

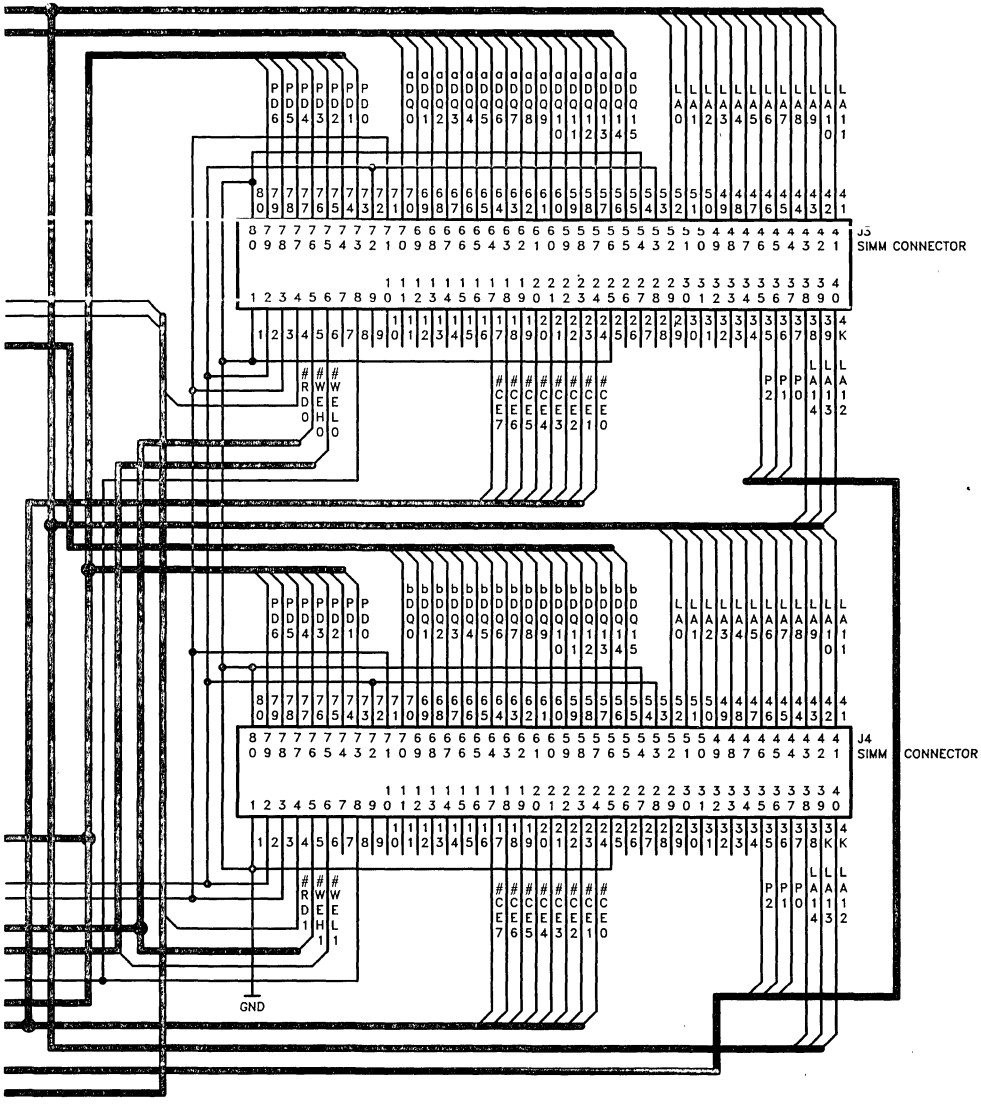

KA(0..14)
cDQ(0..15)
U1
U2
D8 D9 D10 D11 D12 D13 D14 D15
cDQ8 cDQ9 cDQ10 cDQ11 cDQ12 cDQ13 cDQ14 cDQ15
D0 D1 D2 D3 D4 D5 D6 D7
cDQ0 cDQ1 cDQ2 cDQ3 cDQ4 cDQ5 cDQ6 cDQ7
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
G
DIR
74F245
T5
T4
D(0..15)
#RD2
#RD3
dDQ(0..15)
U4
U3
dDQ8 dDQ9 dDQ10 dDQ11 dDQ12 dDQ13 dDQ14 dDQ15
dDQ0 dDQ1 dDQ2 dDQ3 dDQ4 dDQ5 dDQ6 dDQ7
T7
T6
T(0..7)
VCC
+5V
VPP
#WEH(0..3)
#WEL(0..3)
RESET#
PD(0..6)
#CE(0..7)
P(0..7)
#RD(0..3)
GND
GND

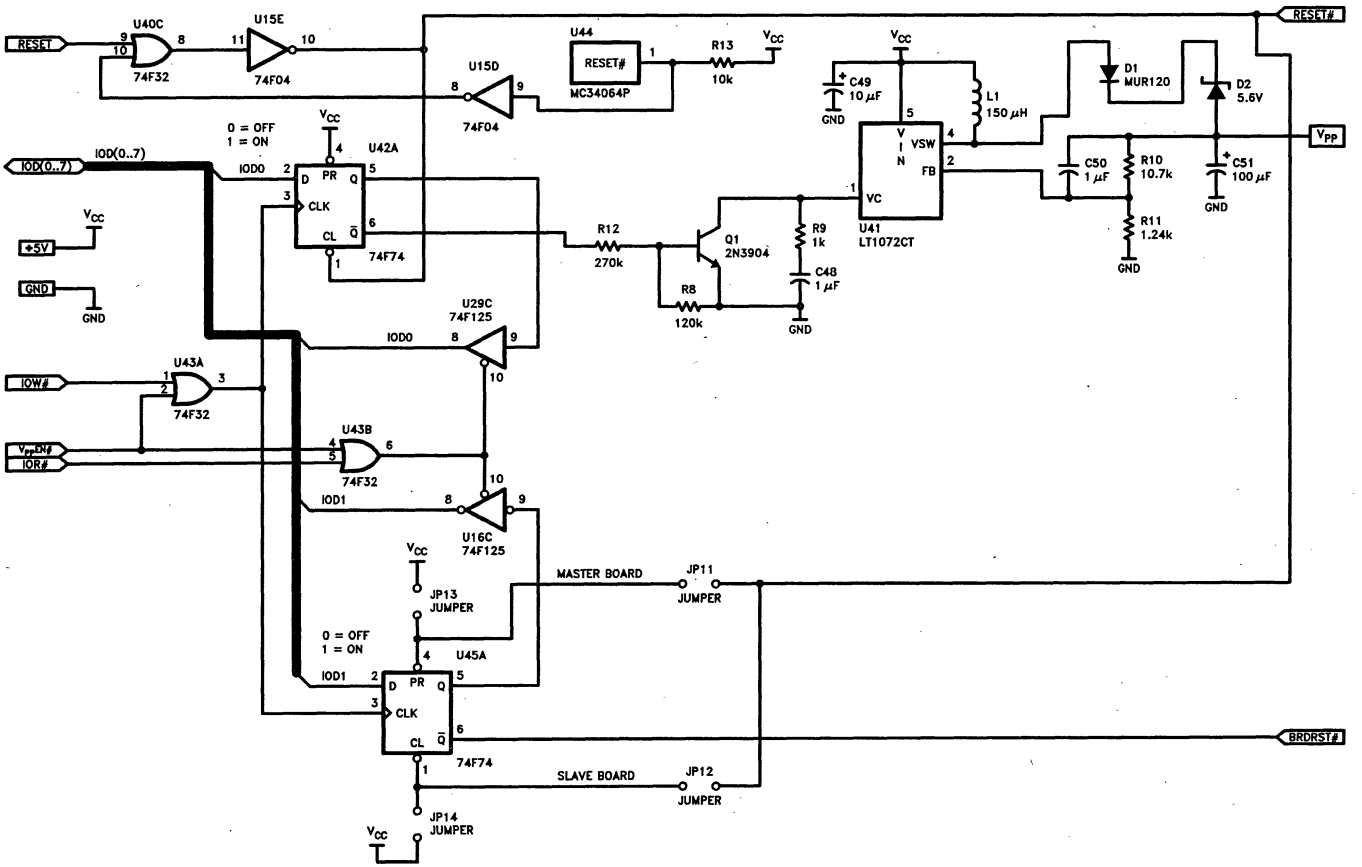
292079-5

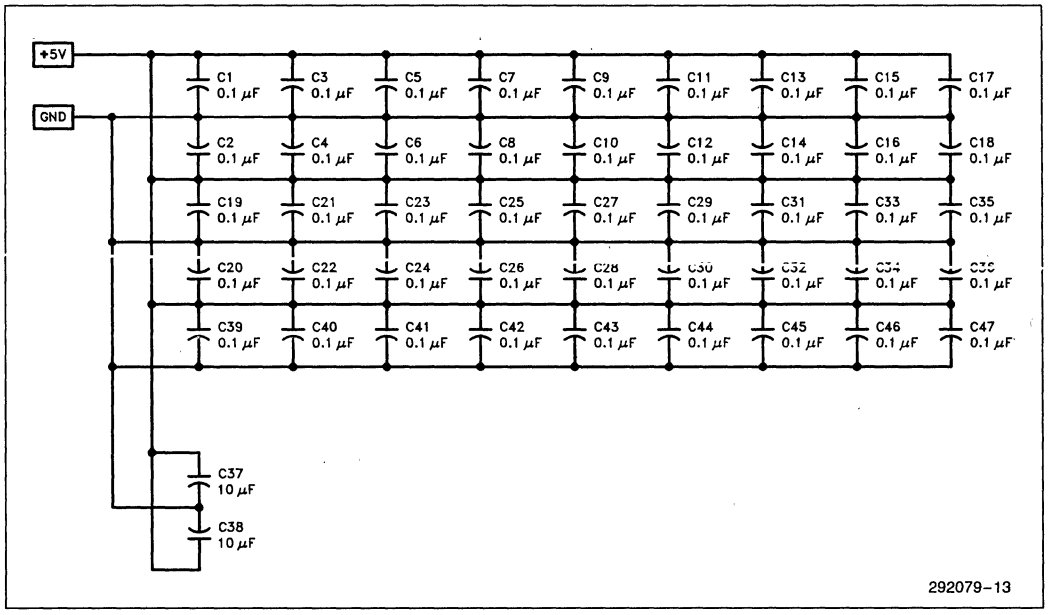

J1
SIMM CONNECTOR
J2
SIMM CONNECTOR
GND
292079-6

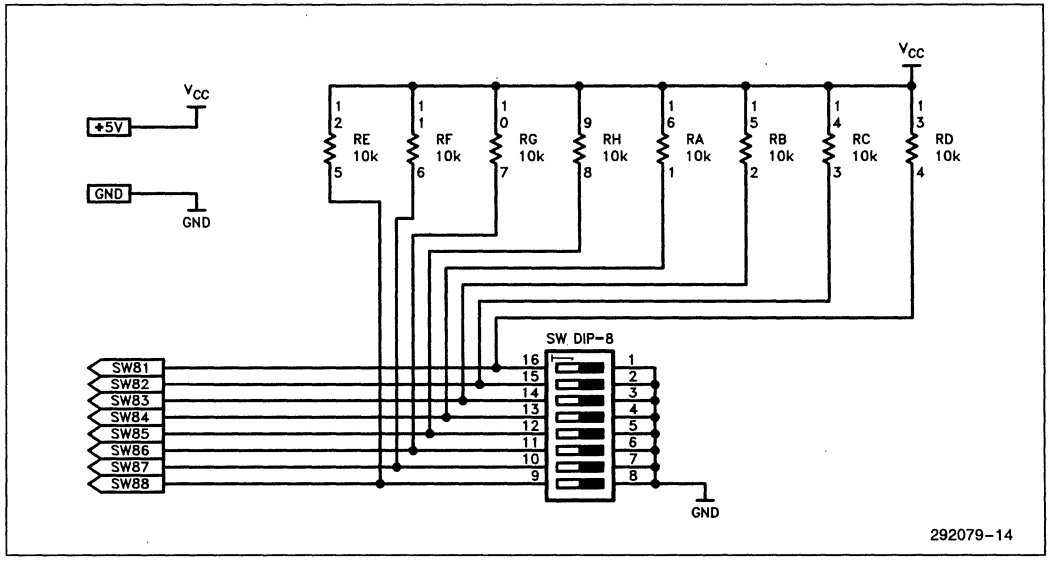

LA(0..14)
aDQ(0..15)
U7
U8
D8 D9 D10 D11 D12 D13 D14 D15
D0 D1 D2 D3 D4 D5 D6 D7
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
aDQ8 aDQ9 aDQ10 aDQ11 aDQ12 aDQ13 aDQ14 aDQ15
aDQ0 aDQ1 aDQ2 aDQ3 aDQ4 aDQ5 aDQ6 aDQ7
G
DIR
74F245
T1
T0
D(0..15)
#RD0
#RD1
bDQ(0..15)
U6
U5
bDQ8 bDQ9 bDQ10 bDQ11 bDQ12 bDQ13 bDQ14 bDQ15
bDQ0 bDQ1 bDQ2 bDQ3 bDQ4 bDQ5 bDQ6 bDQ7
T3
T2
T(0..7)
VCC
R1A 10k
R1B 10k
R1C 10k
R1D 10k
R1E 10k
R1F 10k
R1G 10k
PD0
PD1
PD2
PD3
PD4
PD5
PD6
+5V
VPP
#WEH(0..3)
#WEL(0..3)
RESET#
PD(0..6)
#CE(0..7)
P(0..7)
#RD(0..3)
GND

292079-7


J3
SIMM CONNECTOR
J4
SIMM CONNECTOR
GND
292079-8


RESET
U40C
74F32
U15E
74F04
U15D
74F04
U44
RESET#
MC34064P
R13
10k
VCC
C49
10 µF
GND
L1
150 µH
D1
MUR120
D2
5.6V
RESET#
VPP
U41
LT1072CT
VIN
VSW
FB
VC
C50
1 µF
R10
10.7k
R11
1.24k
C51
100 µF
IOD(0..7)
0 = OFF
1 = ON
U42A
74F74
IOD0
R12
270k
Q1
2N3904
R9
1k
C48
1 µF
R8
120k
+5V
U29C
74F125
IOW#
U43A
74F32
VPPEN#
IOR#
U43B
74F32
IOD1
U16C
74F125
JP13
JUMPER
MASTER BOARD
JP11
JUMPER
U45A
74F74
SLAVE BOARD
JP12
JUMPER
JP14
JUMPER
BRDRST#
292079-11


+5V
GND
C1 0.1 µF
C3 0.1 µF
C5 0.1 µF
C7 0.1 µF
C9 0.1 µF
C11 0.1 µF
C13 0.1 µF
C15 0.1 µF
C17 0.1 µF
C2 0.1 µF
C4 0.1 µF
C6 0.1 µF
C8 0.1 µF
C10 0.1 µF
C12 0.1 µF
C14 0.1 µF
C16 0.1 µF
C18 0.1 µF
C19 0.1 µF
C21 0.1 µF
C23 0.1 µF
C25 0.1 µF
C27 0.1 µF
C29 0.1 µF
C31 0.1 µF
C33 0.1 µF
C35 0.1 µF
C20 0.1 µF
C22 0.1 µF
C24 0.1 µF
C26 0.1 µF
C28 0.1 µF
C30 0.1 µF
C32 0.1 µF
C34 0.1 µF
C36 0.1 µF
C39 0.1 µF
C40 0.1 µF
C41 0.1 µF
C42 0.1 µF
C43 0.1 µF
C44 0.1 µF
C45 0.1 µF
C46 0.1 µF
C47 0.1 µF
C37 10 µF
C38 10 µF
292079-13


VCC
+5V
GND
GND
RE 10k
RF 10k
RG 10k
RH 10k
RA 10k
RB 10k
RC 10k
RD 10k
SW_DIP-8
SW81
SW82
SW83
SW84
SW85
SW86
SW87
SW88
GND
292079-14

6

I/O Port Usage for PCAT

Range	Usage
0000–000fh	DMA Controller 1, 8237A
0020–0021h	Interrupt Controller 1, 8259A
0040–005fh	Programmable Timer, 8254
0060–006fh	Keyboard Controller, 8042
0070–007fh	CMOS Real-Time Clock, NMI Mask
0080–009fh	DMA Page Registers, 74LS612
00a0–00a1h	Interrupt Controller 2, 8259A
00c0–00dfh	DMA Controller 2, 8237A
00f0–00ffh	Math Coprocessor
01f0–01f8h	Fixed Disk
0200–020fh	Game Controller
0278–027fh	Parallel Printer Port 2
02b0–027dfh	EGA (Alternate)
02e1h	GPIB (Adapter 0)
02e2–02e3h	Data Acquisition (Adapter 0)
02f8–02ffh	Serial Communications (COM2)
0300–031fh	Prototype Card
0360–036fh	PC Network
0378–037fh	Parallel Printer Port 1
0380–038ch	SDLC Communications

Range	Usage
0390–0393h	Cluster (Adapter 0)
03a0–03a9h	BSC Communications (Primary)
03b0–03bfh	Monochrome/Parallel Printer Adapter
03c0–03cfh	EGA (Primary)
03d0–03dfh	CGA
03f0–03f7h	Floppy Disk Controller
03f8–03ffh	Serial Communications (COM 1)
06e2–06e3h	Data Acquisition (Adapter 1)
0790–0793h	Cluster (Adapter 1)
0ae2–0ae3h	Data Acquisition (Adapter 2)
0b90–0b93h	Cluster (Adapter 2)
0ee2–0ee3h	Data Acquisition (Adapter 3)
1390–1393h	Cluster (Adapter 3)
2390–2393h	Cluster (Adapter 4)
42e1h	GPIB (Adapter 2)
62e1h	GPIB (Adapter 3)
82e1h	GPIB (Adapter 4)
a2e1h	GPIB (Adapter 5)
c2e1h	GPIB (Adapter 6)
e2e1h	GPIB (Adapter 7)

ASSEMBLY LANGUAGE CODE FOR PAGED BOARD

```
;*****************************************************************************
;Locating the Base I/O Address.
;BOARD_NOT_FOUND is an error procedure and is not shown.

    BRD_ID0          dw 4 dup (?)
    Window_Base      dw ?
    Presence_Detect  dw ?
    VPPEN            dw ?
    Page_Number      dw ?

    mov dx,02F8h          ;Set port pointer to 02F8H.

KEEP_LOOKING:
    add dx,8              ;First valid address after adding.
    cmp dx,318            ;Port pointer = 8 less than highest port address?
    jg board_not_found    ;Hey, you forgot to install the board!!!

    in al,dx              ;Read port data into al register.
    cmp al,0Dh            ;Does register = 1st identifier value?
    jne KEEP_LOOKING      ;Not equal --> Not located yet

    inc dx
    in al,dx
    cmp al,0Ah            ;Does register = 2nd identifier value?
    jne KEEP_LOOKING

    inc dx
    in al,dx
    cmp al,01h            ;Does register = 3rd identifier value?
    jne KEEP_LOOKING

    inc dx
    in al,dx
    cmp al,0Eh            ;Does register = last identifier value?
    jne KEEP_LOOKING      ;TOO BAD, you almost had it!

;FOUND-Good Job!
    sub dx,3              ;Restored to base address.
    mov BRD_ID0,dx        ;Save the value in RAM.
```

Locating the Base I/O Address

NOTE:
A review of 8086 asembly language programming fundamentals might be necessary at this point.

6

```
;Locating the Base Memory Address

;*************************************************************************

;This Information is loaded into a segment register to access data

;*************************************************************************
    mov ax,0                ;Clear register
    mov dx,Window_Base      ;Port pointer = I/O to read base memory address
    in al,dx                ;Read port
    mov bx,256
    mul ax                  ;Shifts address information left.
    mov es,ax               ;es used as segment register for board.
```

```
;*****************************************************************************
;Determining Memory Capacity

    Density_Lookup_Table dw ?,?,0fffh,7ffh,03ffh
    DENSITY dw ?

    mov ax,0                ;Clears register.
    mov dx,Page_Number      ;Port pointer accesses page number.
    mov al,0
    out dx,al               ;Write a zero to page number hardware.
    mov dx,Presence_Detect ;Port pointer accesses presence detect pins.
    in al,dx
    and al,23H              ;Clears all but density information.
    cmp al,20H              ;Checks if PD6 is set.
    jng skip_or
    or al,4                 ;If greater than 20H, set bit 2 of al.

;Go to density lookup table, translate value from PD pins, store in RAM
;variable DENSITY. Density value must be 2, 3, or 4 to be valid.
 skip_or:
    cmp al,4
    je okay
    cmp al,3
    je okay
    cmp al,2
    je okay
    jmp Unknown_Device      ;Invalid or no SIMMs present, routine not shown.

;Base address of density lookup table stored in bx register.
    mov bx,offset Density_Lookup_Table
    mov si,ax               ;si register will be pointer into density table
;Density values for 1M-4M, multiples of 1 Kbytes, stored in lookup table.
    mov ax,[bx+si]          ;Density read into ax register
    mov DENSITY,ax
;Read the device identifier. Use the es segment register for the base
;address of the memory.
;28F010 = 0B4h,28F020 = 0BDh
    mov ax,DENSITY          ;Put RAM held density info into ax.
    mov bx,1
    mov es:[bx],90H         ;Write ID command.
    mov bx,es:[bx]          ;Read device identifier.
    cmp bx,0B4h
    je 1MEG
```

Determining Memory Capacity

```
    cmp bx,0BDh
    je 2MEG

    jmp Unknown_device      ;If other than 28F010 or 28F020.

;Divide SIMM density by component density to determine number of components
;on SIMM.

1MEG:
    mov bx,3FFh
    div ax                  ;Divide ax/bx, # of components stored in al.
    jmp NEXT_OPERATION

2MEG:
    mov bx,7FFh
    div ax
    jmp NEXT_OPERATION

;Read from the next SIMM location to verify its presence.
;As an example, assume that the SIMM's density is 1 Mbyte.
;A 1 Mbyte SIMM has 16 pages.
    mov dx,Page_Number
    mov al,16
    out dx,al               ;Switch to Page 16 for next SIMM location.
    mov bx,1
    mov ex:[bx],90H         ;Write ID Command to first device of next SIMM.
    mov ax,es:[bx]          ;Read the identifier. Invalid data = empty socket
                            ;Repeat the process for all SIMMs.

;*****************************************************************************
```

Determining Memory Capacity (Continued)

May 1990

Designing In Flexibility With A Universal Memory Site

DALE ELBERT
APPLICATIONS ENGINEERING

Order Number: 292061-001

DESIGNING IN FLEXIBILITY WITH A UNIVERSAL MEMORY SITE

CONTENTS

INTRODUCTION

A universal memory site permits end-product flexibility and cost reduction at product maturity. This application brief illustrates the design of a universal DIP site that accepts Intel's ETOX™ flash memory, EPROM, EEPROM, and SRAM.

ETOX™ FLASH MEMORY

Intel's ETOX flash memory offers the most cost-effective and reliable alternative for read-write random-access nonvolatile memory. Flash memory adds electrical chip-erasure and rewrite capability to EPROM density and nonvolatility. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after sale. Flash memory increases memory flexibility while contributing to time- and cost-savings.

Flash memory is ideal for storing code and data tables in embedded control applications where periodic updates are required. With extended cycling capability, Intel flash memory also offers an innovative alternative for mass storage.

Figure 1 illustrates the flash memory density upgrade path for both 32-pin DIP and 32-lead PLCC configurations. System designs using the 256 K-bit device can increase memory capacity eightfold with no hardware change.

FLASH MEMORY—EPROM SITE

In most systems, code is more volatile during the prototyping and early production stages of the system's life cycle. EPROMs must be removed from the system for replacement or reprogramming. EPROM updates are labor intensive and hence expensive, adding cost to system design, manufacturing, and after-sale service. Other alternatives have been more costly or less reliable.

The remote update capability of flash memory simplifies updates. New code can be introduced over any serial communication line. No disassembly as such, many designers have opted to use flash memory prototyping and early production. As the system matures and code updates cease, the balance of production can be converted to EPROM for further cost reduction when a compatible memory site is used. This is the most cost-effective approach, since flash memory equals EPROM in density while its cost difference is far less than that of manually updating EPROMs.

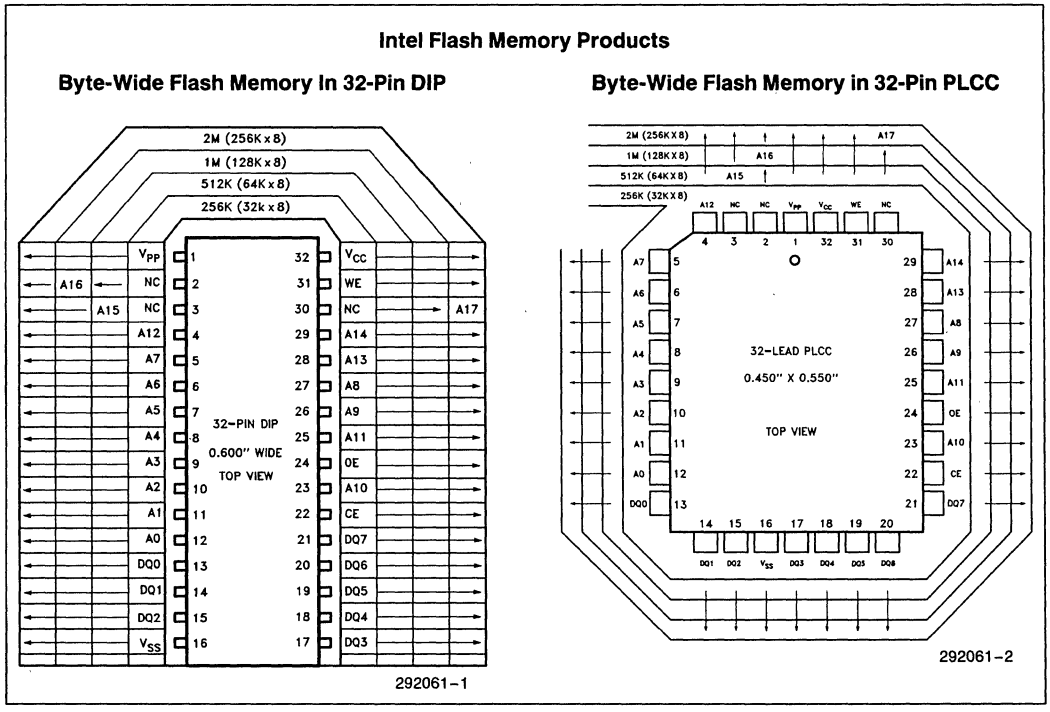


Figure 1. Intel Flash Memory DIP and PLCC Pinouts

Figure 2 illustrates the jumpers necessary to convert between 32-pin flash devices and 28-pin or 32-pin EPROM devices. For 256K or 512K densities, jumpers A, C, and F would be used for flash memory operation. Jumpers B, D, and E would be used for EPROM.

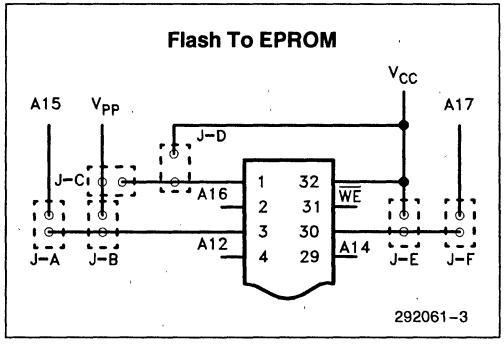


Figure 2. Flash Memory—EPROM DIP Site

The conversion is simpler for one-megabit and two-megabit densities as both flash memory and EPROM share the 32-pin configuration. Jumper C would connect the V_{PP} supply for flash memory operation. Jumper D would route V_{CC} to the V_{PP} pin for EPROM read-only operation.

The write-enable trace used for flash memory can remain hard-wired. The PGM input to EPROMs is a "don't care" for read operations, when the voltage applied to the V_{PP} pin is between V_{CC} and ground.

When PLCC EPROMs were first introduced, the packaging technology used leads 1 and 17 for mechanical support of the die. Pins 1 and 17 were unavailable and were labeled "don't use". As packaging technology evolved, different means of mechanical support allowed the use of leads 1 and 17.

Flash memory and one-megabit EPROMs use this newer packaging technology. In 32-lead PLCC, as in the 32-pin DIP, flash is upgradable from 256K through two-megabits with no hardware change. However, a conversion from 256K or 512K PLCC flash to a like-density EPROM requires relayout of the board, as the address lines and power supplies have a different orientation. At the 1M and 2M densities, the conversion is quite simple and is the same as the DIP strategy. A jumper removes V_{PP} and applies V_{CC} to the V_{PP} pin for EPROM read-only operation.

FLASH MEMORY—SRAM SITE

In recent years, designers have turned to battery-backed SRAMs for flexible nonvolatile storage, especially in consumer-oriented or very price-sensitive designs. In applications desiring updatable code or data table storage, or data accumulation, flash memory offers a more dense, cost-effective, and reliable alternative to battery-backed SRAMs.

The SRAM memory cell requires four or six transistors to store a bit of information. Intel's flash memory employs a single transistor cell. As such, flash memory garners an immediate density advantage. And since density translates into cost-per-bit effectiveness, flash memory is roughly one-half the price of the battery-backed SRAM solution.

Beyond the cost/density advantage, flash memory provides greater data integrity. Battery failure is unpredictable, resulting in system downtime and loss of critical data. Eliminating the battery means eliminating battery limitations—mechanical holders, special access required for battery maintenance, and limited durability in harsh environments.

It is still useful to be able to design an SRAM/flash memory-compatible site for a general-purpose memory board. This allows custom configuration of the memory map = SRAM for working data (scratchpad) and flash memory for non-volatile code and archival data storage.

Figure 3 illustrates the jumpers required to reroute A14, A15, and the write-enable signal. Jumpers A, C, and F are used for flash memory operation. Jumpers B, D, and E are used for SRAM.

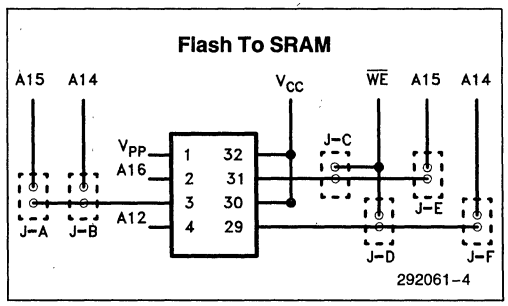


Figure 3. Flash Memory—SRAM DIP Site

FLASH MEMORY—EEPROM SITE

EEPROM has long-promised flexible, dense, and cost-effective nonvolatile storage. EEPROM offers a high degree of functionality—the ability to alter data on an individual-byte basis. However, EEPROM is burdened with high cost, low density, and erase/write cycling wearout.

The EEPROM memory cell consists of two transistors, a floating gate for charge storage and a select transistor. Intel's flash memory employs a single transistor cell. Immediately, flash garners a density advantage. Again, density leads to cost-effectiveness, making flash less than half the price of EEPROM.

Often, the high level of functionality of EEPROM is overkill for many applications. Designing the memory site to accommodate flash, in addition to EEPROM, allows manufacturing to easily switch to flash when EEPROM functionality is not required or where like the SRAM, it allows flexibility in combining EEPROM and flash memory on a general-purpose memory board.

Figure 4 illustrates the jumpers required to reroute A14, A15, and write-enable (256K only). Jumpers A and D are connected for flash memory operation. Jumpers B and C are used for 256K EEPROM operation. Jumpers A and D are used for one-megabit EEPROM operation.

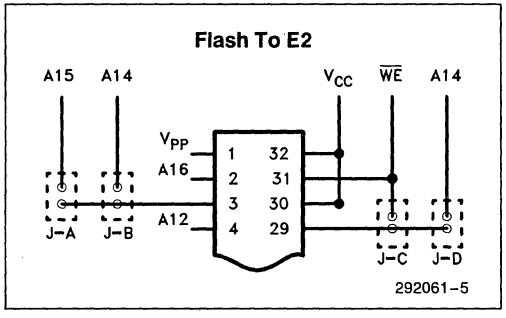


Figure 4. Flash Memory—EEPROM DIP Site

DESIGNING THE UNIVERSAL SITE

The site in Figure 5 combines the strategies in the previous sections and illustrates the design of a universal site to accept flash memory, EPROM, SRAM, or EEPROM. Table 1 is a pin-by-pin comparison of devices on each technology for use with the universal memory site.

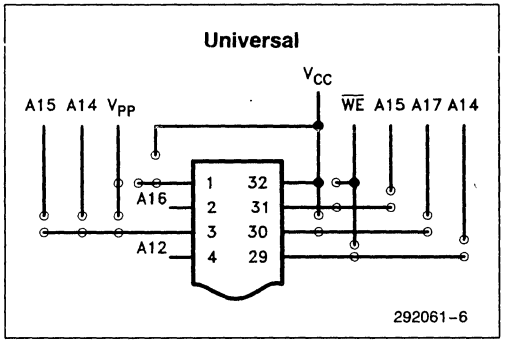


Figure 5. Universal Memory Site

SUMMARY

This application brief has illustrated the hardware design steps needed to specify a universal memory stie that accommodates Intel's flash memory, EPROM, SRAM, and EEPROM. By designing memory sites for multiple memory technologies, production can be easily retrofitted to use the device that makes most sense during the different stages of the product life cycles or to customize a general-purpose design for unique applications.

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SRAM		E2		EPROM				FLASH				DIP Pin		FLASH				EPROM				E2		SRAM	
1M	256K	1M	256K	2M	1M	512K	256K	2M	1M	512K	256K	Number		256K	512K	1M	2M	256K	512K	1M	2M	256K	1M	256K	1M
NC		NC		V_{PP}	V_{PP}			V_{PP}	V_{PP}	V_{PP}	V_{PP}	1	32	V_{CC}	V_{CC}	V_{CC}	V_{CC}			V_{CC}	V_{CC}		V_{CC}		V_{CC}
A16		A16		A16	A16			A16	A16	NC	NC	2	31	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$			$\overline{PGM}$	$\overline{PGM}$		$\overline{WE}$		A15
A14	A14	A15	A14	A15	A15	A15	V_{PP}	A15	A15	A15	NC	3	30	NC	NC	NC	A17	V_{CC}	V_{CC}	NC	A17	V_{CC}	NC	V_{CC}	CS2
A12	A12	A12	A12	A12	A12	A12	A12	A12	A12	A12	A12	4	29	A14	A14	A14	A14	A14	A14	A14	A14	$\overline{WE}$	A14	$\overline{WE}$	$\overline{WE}$

Table 1. Pin Configurations by Technology and Density

intel®

ENGINEERING REPORT

ER-20

September 1989

ETOX™II Flash Memory Technology

JASON ZILLER
PRODUCT ENGINEERING

6

Order Number: 294005-006

ETOX™II FLASH MEMORY TECHNOLOGY

CONTENTS

INTRODUCTION

Intel's ETOX™ II (EPROM tunnel oxide) flash memory technology is derived from the CHMOS** III-E EPROM technology. It replaces ultraviolet erasability with a non-volatile memory cell that is electrically erasable in bulk array form. Intel flash memory combines the EPROM programming mechanism with EEPROM erase, producing a versatile memory device that is highly reliable and cost effective. This report describes the fundamentals of the ETOX II flash memory cell in comparison to the standard EPROM, and gives insight into its operation in a system environment.

The ETOX II flash memory cell is nearly identical in size to CHMOS III-E EPROM. This allows comparable densities. The primary difference between ETOX II flash memory and EPROM cells is the flash memory cell's thinner gate oxide, which permits the electrical erase capability. (See Photo 1.)

ETOX™ II FLASH MEMORY CELL

Intel's ETOX II flash memory cell is composed of a single transistor with a floating gate for charge storage, like the traditional EPROM. (See Figure 1.) In contrast, conventional two-transistor EEPROM cells are typically much larger. Intel produces ETOX II flash memory devices on 1.0μ photolithography.

The ETOX II cell's programming mechanism is identical to the EPROM; that is, hot channel electron injection. The device programming mode forces the cell's control gate and drain to a high voltage while leaving the source grounded. The high drain voltage generates "hot" electrons that are swept across the channel. These hot electrons collide with other atoms along the way, creating even more free electrons. Meanwhile, the high voltage on the control gate attracts these free electrons across the lower gate oxide into the floating gate, where they are trapped. (See Figure 2.) Typically, this process takes less than 10 μs.

Flash memory's advantage over EPROM is electrical erasure, discharging the floating gate without ultraviolet light exposure. The erase mechanism is an EEPROM adaptation which uses "Fowler-Nordheim"[1] tunneling. A high electric field across the lower gate oxide pulls electrons off the floating gate. The erase mode routes the same external voltage used for programming to the source of the memory cell, while the gate is grounded and the drain is left disconnected. (Figure 3.)

MEMORY ARRAY CONSIDERATIONS

The ETOX II flash memory cells have the same array configuration as standard EPROM, thereby matching EPROM in density. Also, identical peripheral circuitry for normal access achieves the same read performance as the Intel CHMOS III-E EPROMs.

Intel flash memory's programming circuitry is also identical to Intel's EPROM designs. Row decoders drive the selected wordline to high voltage, while input data combined with column decoders determine the number of bitlines that are gated to high voltage. This provides the same byte programmability as an EPROM. Intel flash memories offer the efficient Quick-Pulse Programming™ algorithm that is featured on advanced EPROMs.

Array erase is unique to flash memory technology. Unlike conventional EEPROMs, which use a select transistor for individual byte erase control, flash memories achieve much higher density with single transistor cells. Therefore, the erase mode supplies high voltage to the sources of every cell simultaneously, performing a full array erasure. A programming operation must be performed before every erase to equalize the amount of charge on each cell. Then Intel's Quick-Erase™ algorithm intelligently erases the array down to the appropriate minimum threshold level required to read all "ones" data. This procedure ensures a tight distribution of erased cell thresholds throughout the array.

ETOX™ II FLASH MEMORY RELIABILITY

The reliability of Intel's CHMOS ETOX II flash memory process is equivalent to its sister EPROM technology. The ETOX II and EPROM processes share the same data retention characteristics. Preliminary qualification data shows that 1 Megabit flash memories produced on the ETOX II process provide at least 10,000 program and erase cycles with no cycling failures due to oxide stress or breakdown. In fact, several 1 Megabit flash memories were cycled past 100,000 cycles with no apparent oxide damage. This extended cycling capability is attributed to improvements in tunnel oxide processing and advantages inherent in the ETOX II cell approach.

[1]M. Lenzlinger, E.H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO2," Journal of Applied Physics, Vol. 40 (1969), p. 278.

*Intel's ETOX II flash memory process has patents pending.

**CHMOS is a patented process of Intel Corporation.

SUMMARY

ETOX II flash memory technology is the optimal combination of EPROM and E²PROM technologies. Intel's new ETOX II flash memory process offers extended cycling capability with the density and manufacturability of EPROMs. From an application standpoint, flash memory technology provides the capability to improve overall system quality throughout the product development and manufacturing stages. Also, flash memory density is ideally suited for applications requiring version updates of entire programs which, in turn, suit the "flash" characteristics of erasing the entire array at once. In addition, individual byte programming allows for data acquisition. Flash memory devices produce on the ETOX II process provide a high density, low cost solution to many system memory storage requirements which were previously unavailable.

Table I

	EPROM	ETOX™II Flash Memory	EEPROM
Normalized Cell Size	1.0	1.2–1.3	3.0
Programming:			
Mechanism	Hot Electron Injection	Hot Electron Injection	Tunneling Byte
Resolution	Byte	Byte	5 ms
Typ. Time	< 100 μs	< 10 μs	
Erase:			
Mechanism	UV Light	Tunneling	Tunneling
Resolution	Bulk Array	Bulk Array	Byte
Typ. Time	20 Min.	< 1 Sec.	5 ms

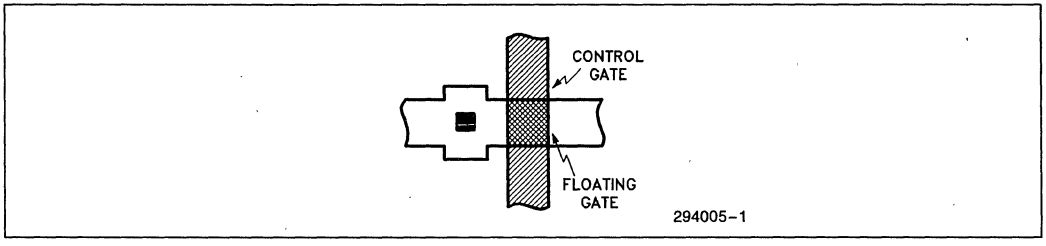


Figure 1. ETOX™II Flash Memory Cell Layout (Top View)

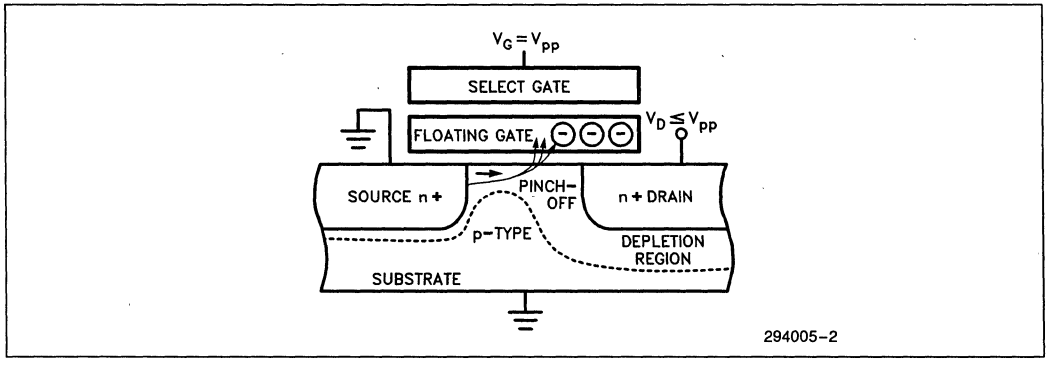


Figure 2. ETOX™II Flash Memory Cell during Programming (Side View)

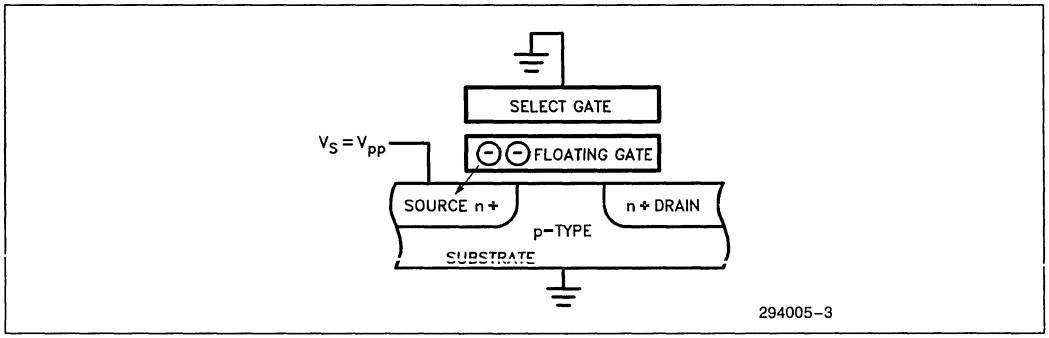
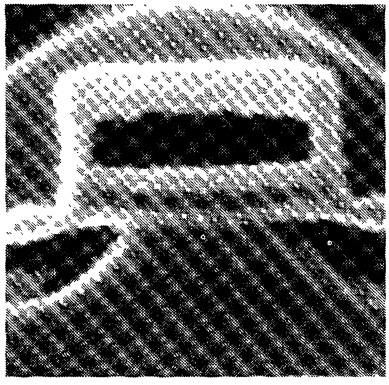


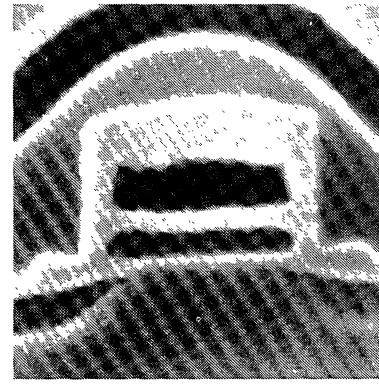
Figure 3. ETOX™II Flash Memory Cell during Erase (Side View)

PHOTO 1



294005-4

ETOX™II Cell
(50,000 x Magnification)



294005-5

CHMOS III-E EPROM Cell
(50,000 x Magnification)

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intel®

ENGINEERING REPORT

ER-24

October 1990

The Intel 28F010 Flash Memory

Order Number: 294008-004

THE INTEL 28F010 FLASH MEMORY

CONTENTS

INTRODUCTION

Intel's 28F010 ETOX™ II (EPROM tunnel oxide) flash memory adds electrical chip erasure and reprogramming to EPROM non-volatility and ease of use. Advances in tunnel oxides and photolithography have made it possible to develop a double-polysilicon single-transistor read/write random access nonvolatile memory, capable of greater than reprogramming cycles (typical 100,000). The 28F010 flash memory electrically erases all bits in the array matrix via electron tunneling. The EPROM programming mechanism of hot electron injection is employed for electrical byte programming.

A command port interface, internal margin voltage generation, power up/down protection and address and data latches augment standard EPROM circuitry to optimize Intel's 28F010 for microprocessor-controlled reprogramming.

Read timing parameters are equivalent to those of CMOS EPROMs, EEPROMs, and SRAMs. The 120 ns access time results from a memory cell current of approximately 50 μA, low resistance poly-silicide wordlines, advanced scaled periphery transistors, and an optimized data-out buffer.

The dense one-transistor cell structure, coupled with high array efficiency, yields a one megabit die measuring 225 by 265 mils.

TECHNOLOGY OVERVIEW

Intel's ETOX II flash memory technology is derived from its standard CMOS EPROM process base. Using advanced 1.0 μm double-polysilicon n-well CMOS technology, the 131,072 x 8 bit flash memory employs a 3.8 μm x 4.0 μm single transistor cell, affording equivalent array density as comparable EPROM technology. The flash memory cell structure is identical to the EPROM structure, except for the thinner gate (tunnel) oxide. Figure 1 compares the flash memory cell to the EPROM cell.

High quality tunnel oxide under the single floating polysilicon gate promotes electrical erasure. All cells in the array are simultaneously erased via Fowler-Nordheim tunneling. Applying 12V on the source junctions and grounding the select gates erases the entire array in one second (typical). Programming is accomplished with the standard EPROM mechanism of hot electron injection from the cell drain junction to the floating gate. Programming is initiated by bringing both the select gate and the cell drain to high voltage. Programming occurs at a rate of 10 μs pulses per byte.

DEVICE ARCHITECTURE

Command Port

One feature which differentiates Intel's one-megabit flash memory is the command port architecture, illustrated in Figures 2 and 3.

The command port simplifies microprocessor control of the erase, erase verify, program, program verify, and read operations, without the need for additional control pins or the multiplexing of high voltage with control functions. On-chip address and data latches minimize system interface logic and free the system bus during erase and program operations. High voltage (12V) on the V_{PP} pin enables the command port. In the absence of this high voltage, the command port defaults to the read operation, inhibiting erasure or programming of the device.

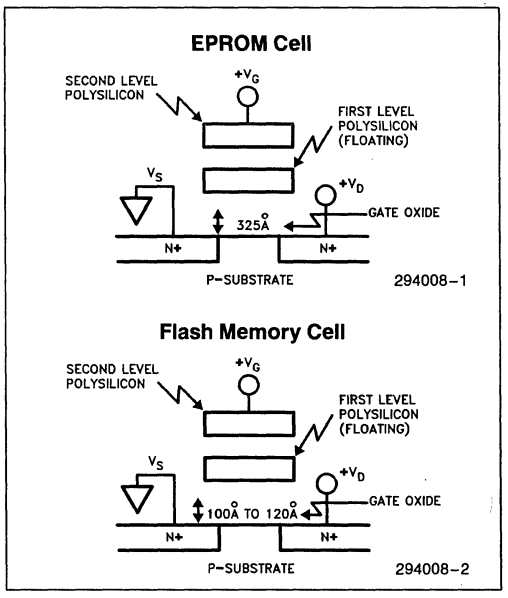

Figure 1. EPROM Cell vs. Flash Memory Cell

The command port consists of a command register, command decoder and state latch, the data-in latch, and the address latch. The command decoder output directs the operation of the high voltage flash-erase switch, program voltage generator, and the erase/program verify voltage generator.

Functions are selected via the command port in a microprocessor write cycle controlled by the Chip-Enable and Write-Enable pins. Contents of the address latch are updated on the falling edge of Write-Enable. The rising edge of Write-Enable latches the command and data registers, and initiates operations.

Erasure

Erasure is achieved through a two-step write sequence. The erase set-up code is written to the command register in the first cycle. The erase confirmation code is written in the second cycle. The rising edge of this second Write-Enable pulse initiates the erase operation. The command decoder triggers the high voltage flash-erase switch, connecting the 12V supply to the source of all bits in the array, while all wordlines are grounded. Fowler-Nordheim tunneling results in the simultaneous erasure of all bits.

The array source switch, shown in Figure 4, switches high voltage onto the source junctions. During erasure, the high voltage latch formed by M5 through M8 enables transistor M15. Transistor M15 pulls the array source up to 12V. Transistor M16 pulls the source to ground during read and program operations.

To obtain fast erase times, the device must supply the grounded gate breakdown current which occurs on the sources of the memory array. The upper boundary for current sourcing capability of M15 is set by the maximum allowable substrate current. If V_{PP} is raised to 12V before V_{CC} is above approximately 1.8V, the low V_{CC} detect circuit formed by transistors M1 to M4 drives the node LOW V_{CC} to 9V. Transistors M9 to M11 then force the erase circuit into a non-erase state with M15 off and M16 on. When V_{CC} rises above 1.8V, the chip will be reset into the read state.

Writing the erase verify code into the command register terminates erasure, latches the address of the byte to verify, and sets the internally-generated erase margin voltage. The microprocessor then accesses the output from the addressed byte using standard read timings. The verify procedure repeats for all addresses. Should a byte require more time to reach the erased state, another erase operation is applied. The erase and verify operations continue until the entire array is erased.

Programming

Programming follows a similar flow. The program set-up command is written to the command register on the first cycle. The second cycle loads the address and data latches. The rising edge of the second Write-Enable pulse initiates programming by applying high voltage to the gates and drains of the bits to be programmed.

Writing the program verify command to the register terminates the programming operation and applies the program verify voltage to the newly programmed byte. Again, the addressed byte can be read using standard microprocessor read timings. Should the addressed byte require more time to reach the programmed state, the programming operation and verification are repeated until the byte is programmed.

DEVICE RELIABILITY

Cell Margining

Erase and program verification ensure the data retention of the newly altered memory bits. The cell margining performed in the Quick-Pulse Programming™ and Quick-Erase™ algorithms is more reliable than historical overpulsing schemes as margining tests the amount of charge stored on the floating gate.

Intel's flash memories employ a unique circuit to internally generate the erase and program verify voltages. Figure 5 shows a simplified version of the circuit. The circuit consists of a high voltage switch and the verify voltage generator. Transistors M1 through M4 constitute the high voltage switch which disconnects V_{PP} from the resistor when the device is not in the verify mode. The verify voltage generator includes a resistor divider and a buffer. Internal margin voltage generation maintains microprocessor compatibility by eliminating the need for external reference voltages.

Erase/Program Cycling

One of the most significant aspects of the 28F010 is its capability for a minimum of 10,000 erase/program cycles (typical 100,000). Destructive oxide breakdown has been a limiting factor in extended cycling of thin oxide EEPROMs. Intel's ETOX II flash memory technology extends cycling performance through: improved tunnel oxide processing that increases charge carrying capability ten-fold; reduced oxide area under stress minimizing probability of oxide defects in the region; and reduced oxide stress due to a lower peak electric field (lower erase voltage than EEPROM).

A typical cell erase/program margin (Vt) is shown as a function of reprogramming cycles in Figure 6. After 10,000 reprogramming cycles, a 2.5V program read margin exists, ensuring reliable data retention. Accelerated retention bake experiments, for devices cycled 10,000 times, show minimal program Vt shift.

Reliable erase/program cycling also requires proper selection of the erase Vt maximum and maintenance of a tight Vt distribution. The maximum erased Vt is set to 3.2V via the erase algorithm and the internal erase verify circuits. Superior oxide quality gives an erased Vt distribution width that improves slightly with cycling (Figure 7). The tight erase Vt distribution gives an order of magnitude of erase time margin to the fastest erasing cell (Figure 8).

Figures 9 and 10 illustrate typical programming performance as a function of cycling, temperature, and V_{PP}. Figures 11 and 12 depict typical erase performance as a function of cycling, temperature, and V_{PP}.

SUMMARY

Intel's ETOX II flash memory technology is a breakthrough in adding electrical chip-erasure to high-density EPROM technology. Intel's 28F010 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access non-volatile memory. Microprocessor-compatible specifications, straightforward interfacing, and in circuit alterability allow designers to easily augment memory flexibility and satisfy the need for nonvolatile storage in today's designs.

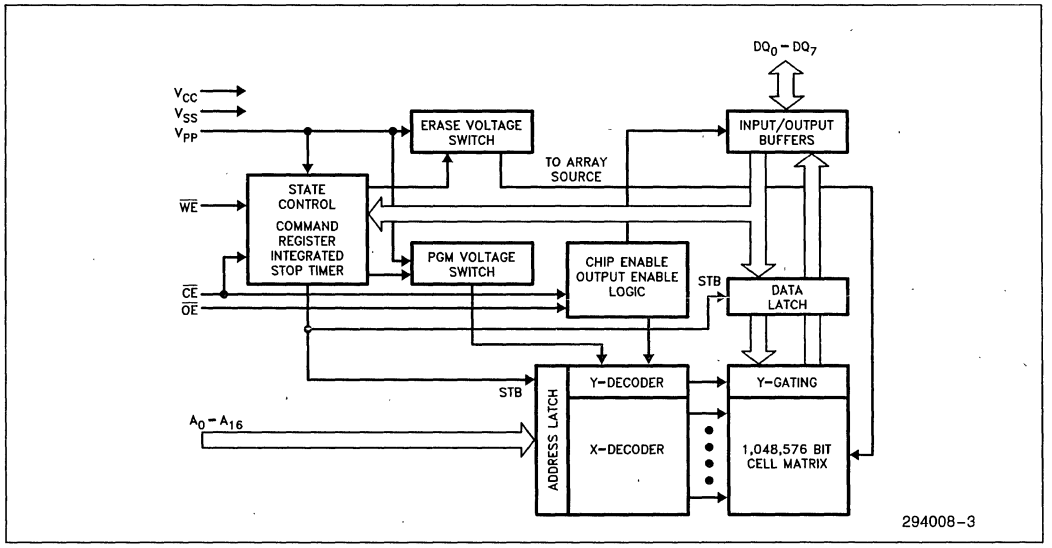

Figure 2. 28F010 Block Diagram

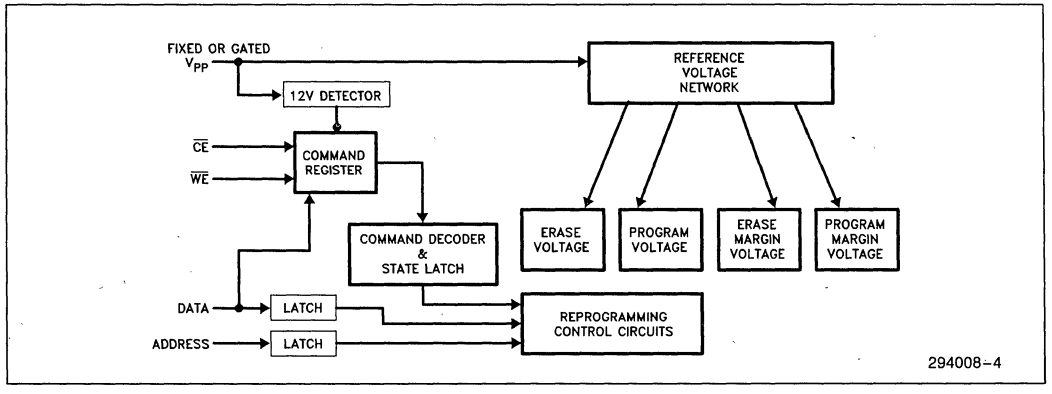

Figure 3. Command Port Block Diagram

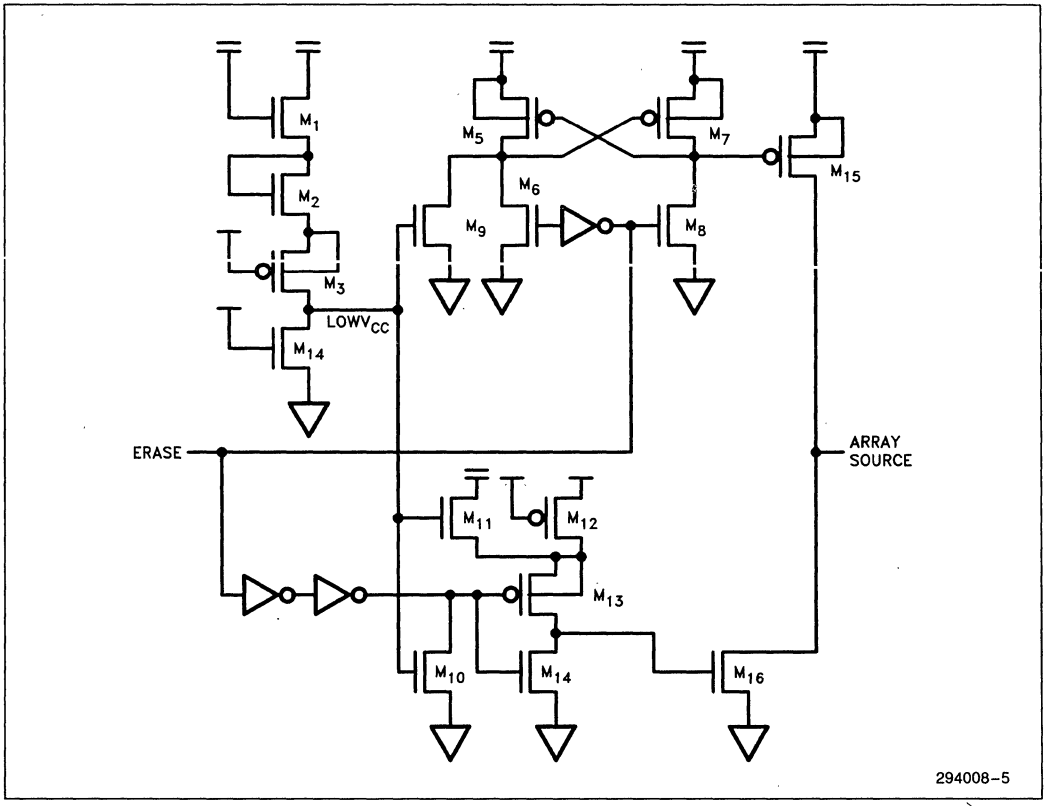

Figure 4. Array Source Switch

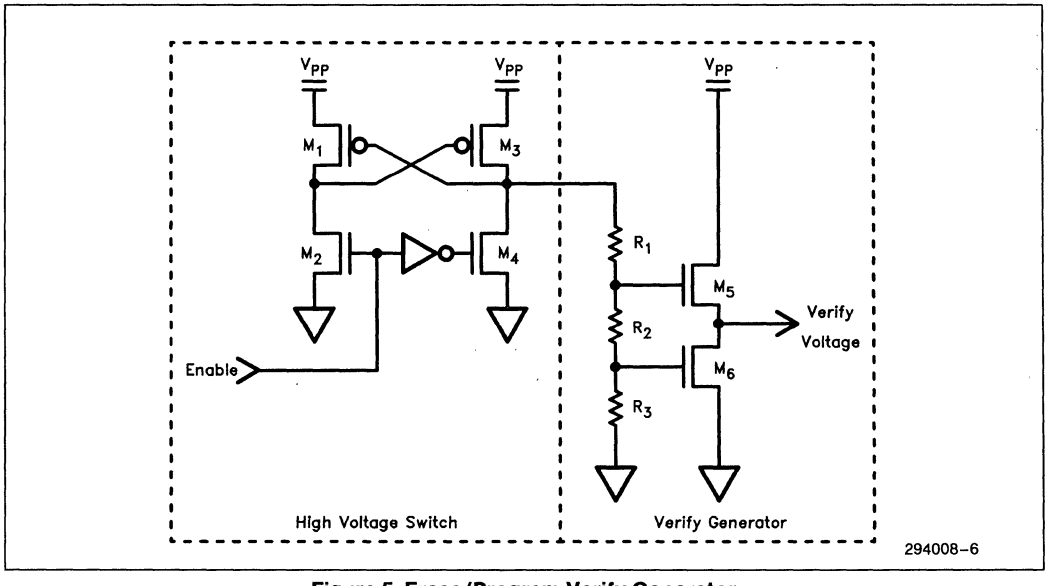

Figure 5. Erase/Program Verify Generator

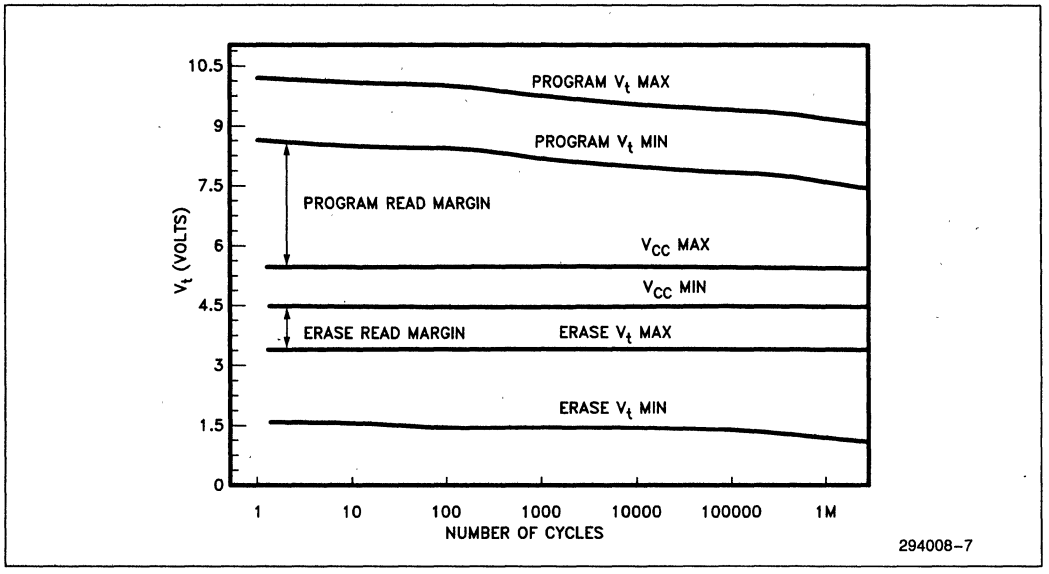

Figure 6. 1M Array V_t vs Cycles

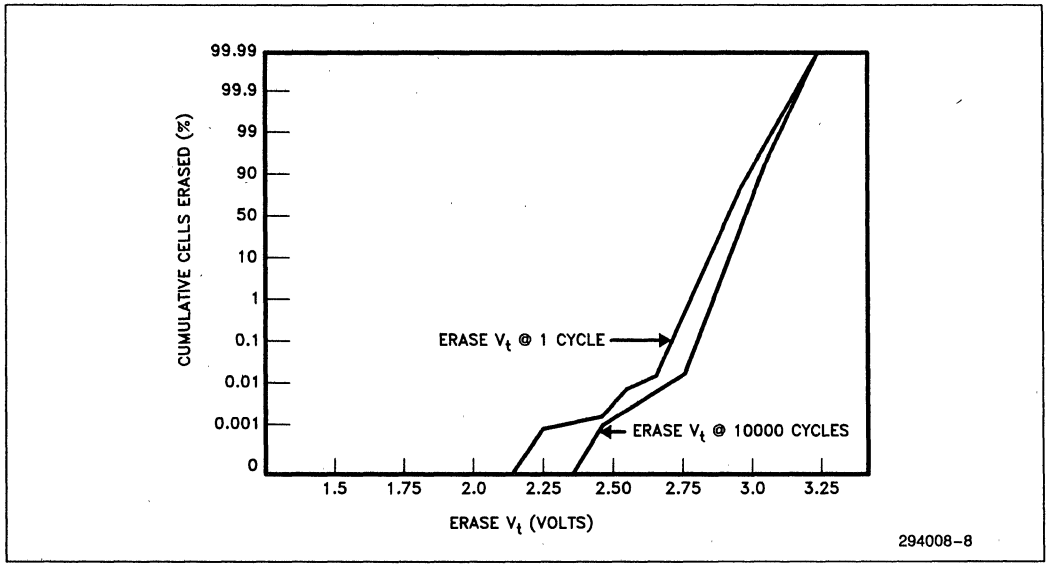

Figure 7. Erase V_t Distribution vs Cycling

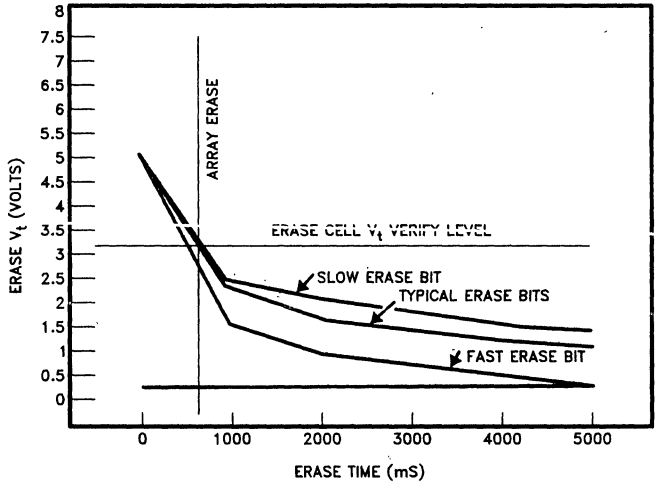

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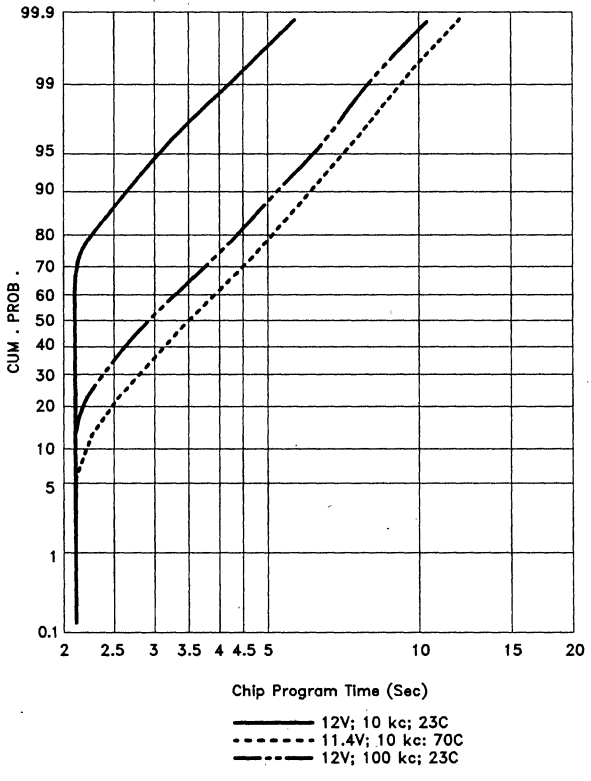
Figure 8. Array Erase V_t vs Erase Time



294008-10

Figure 9. 28F010 Typical Programming Capability

6

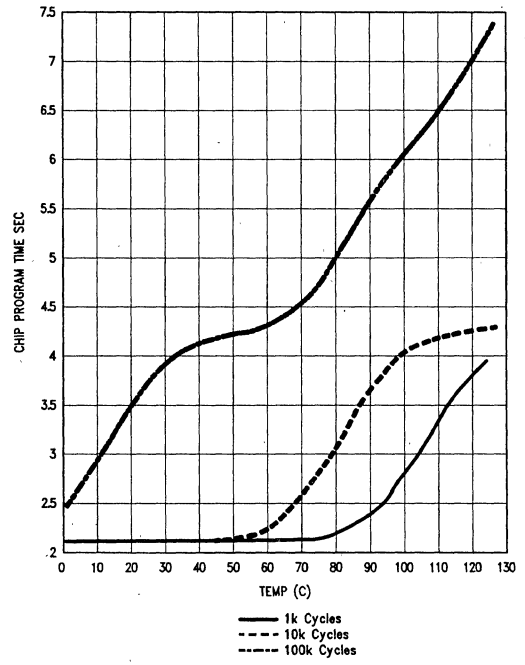


Figure 10. 28F010 Typical Program Time at 12V

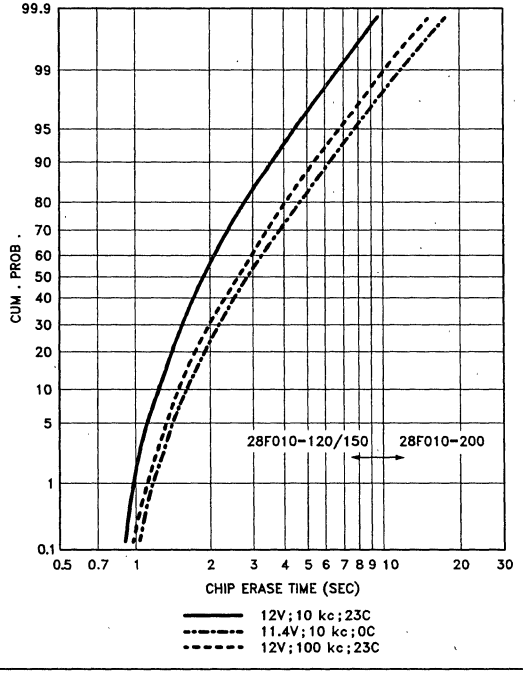


Figure 11. 28F010 Typical Erase Capability

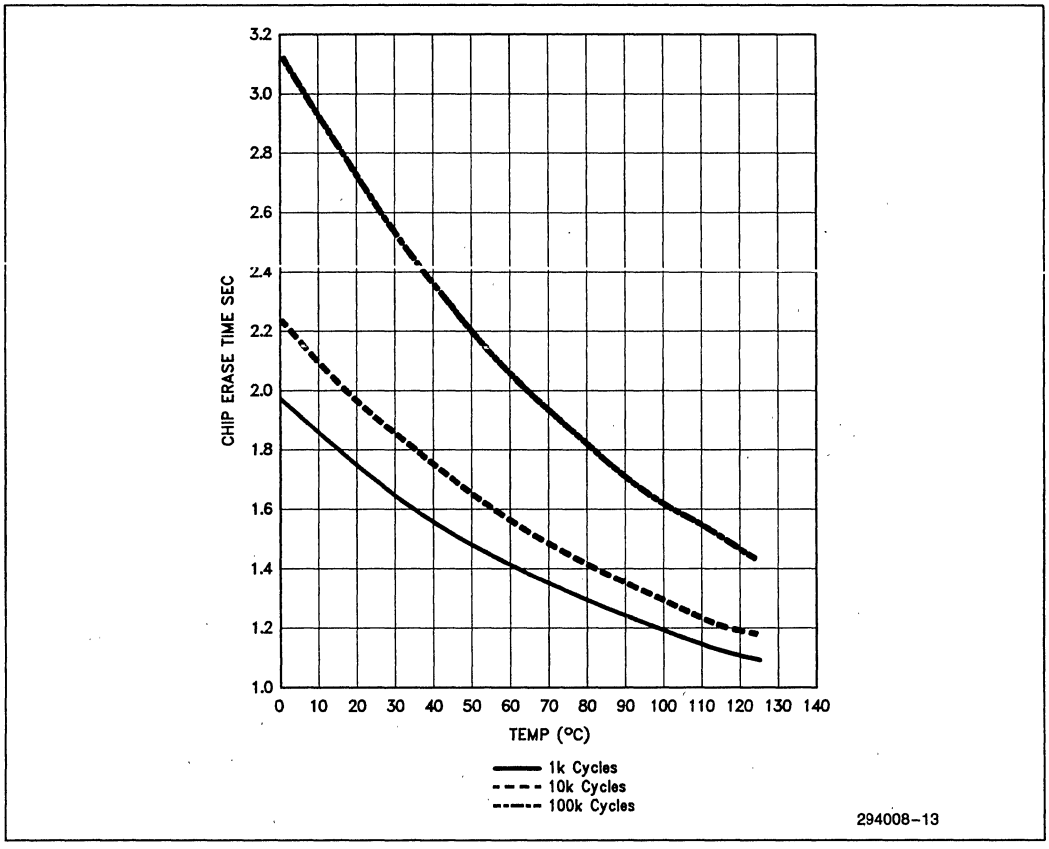


Figure 12. 28F010 Typical Erase Time at 12V

6

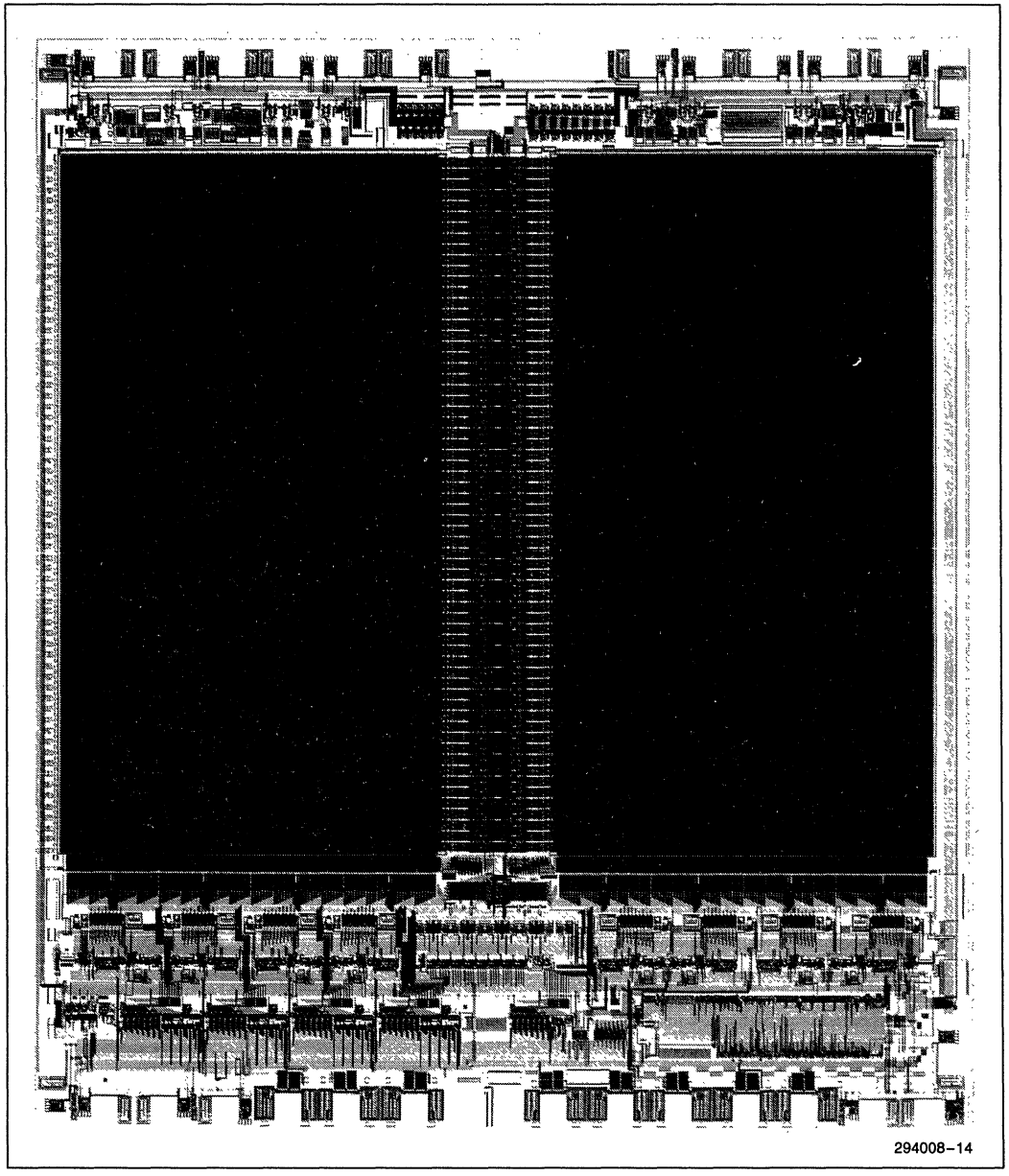
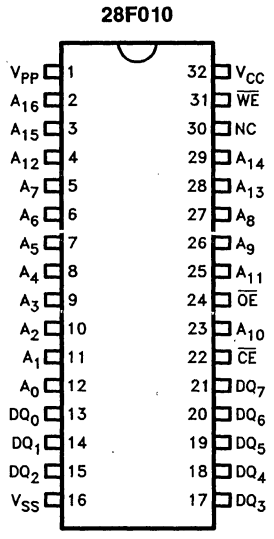
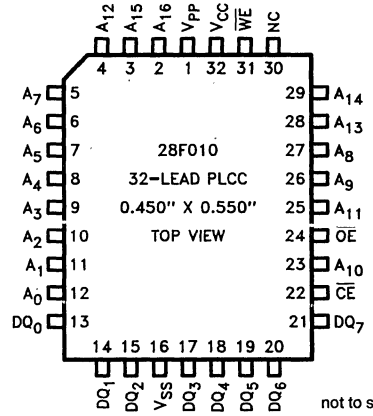


Figure 13. 28F010 Die Photograph



294008-15



not to scale

294008-16

Pin Names

A_0–A_{16}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{PP}	Program/Erase Power
V_{CC}	Device Power
V_{SS}	Ground

Figure 14. 28F010 Pin Configurations

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Columns are number 0 through 511 beginning with the column nearest the X-decoder.
Outputs are grouped as follows:

Array Organization:							Left Half Array IO_0 IO_1 IO_2 IO_3 $BL_{384} \leftarrow BL_0$		Right Half Array IO_4 IO_5 IO_6 IO_7 $BL_0 \rightarrow BL_{384}$	
Address							Bitlines			
A_{16}	A_{15}	A_{10}	A_2	A_1	A_0	A_3	IO_0 & IO_7	IO_1 & IO_6	IO_2 & IO_5	IO_3 & IO_4
0	0	0	0	0	0	0	BL_{384}	BL_{256}	BL_{128}	BL_0
0	0	0	0	0	0	1	BL_{385}	BL_{257}	BL_{129}	BL_1
0	0	0	0	0	1	0	BL_{386}	BL_{258}	BL_{130}	BL_2
0	0	0	0	0	1	1	BL_{387}	BL_{259}	BL_{131}	BL_3
0	0	0	0	1	0	0	BL_{388}	BL_{260}	BL_{132}	BL_4
0	0	0	0	1	0	1	BL_{389}	BL_{261}	BL_{133}	BL_5
0	0	0	0	1	1	0	BL_{390}	BL_{262}	BL_{134}	BL_6
0	0	0	0	1	1	1	BL_{391}	BL_{263}	BL_{135}	BL_7
•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	0	0	BL_{508}	BL_{380}	BL_{252}	BL_{124}
1	1	1	1	1	0	1	BL_{509}	BL_{381}	BL_{253}	BL_{125}
1	1	1	1	1	1	0	BL_{510}	BL_{382}	BL_{254}	BL_{126}
1	1	1	1	1	1	1	BL_{511}	BL_{383}	BL_{255}	BL_{127}

Figure 15. Bitline Decoding

X Address										Row
A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_{13}	A_{11}	A_9	A_8	WL
0	0	0	0	0	0	0	0	0	0	XL_0
0	0	0	0	0	0	0	0	0	1	XL_1
0	0	0	0	0	0	0	0	1	0	XL_2
0	0	0	0	0	0	0	0	1	1	XL_3
0	0	0	0	0	0	0	1	0	0	XL_4
0	0	0	0	0	0	0	1	0	1	XL_5
0	0	0	0	0	0	0	1	1	0	XL_6
0	0	0	0	0	0	0	1	1	1	XL_7
0	0	0	0	0	0	1	0	0	0	XL_8
0	0	0	0	0	0	1	0	0	1	XL_9
0	0	0	0	0	0	1	0	1	0	XL_{10}
0	0	0	0	0	0	1	0	1	1	XL_{11}
0	0	0	0	0	0	1	1	0	0	XL_{12}
0	0	0	0	0	0	1	1	0	1	XL_{13}
0	0	0	0	0	0	1	1	1	0	XL_{14}
0	0	0	0	0	0	1	1	1	1	XL_{15}
0	0	0	0	0	1	1	1	1	1	XL_{16}
0	0	0	0	0	1	1	1	1	0	XL_{17}
0	0	0	0	0	1	1	1	0	1	XL_{18}
0	0	0	0	0	1	1	1	0	0	XL_{19}
0	0	0	0	0	1	1	0	1	1	XL_{20}
0	0	0	0	0	1	1	0	1	0	XL_{21}
0	0	0	0	0	1	1	0	0	1	XL_{22}
0	0	0	0	0	1	1	0	0	0	XL_{23}
0	0	0	0	0	1	0	1	1	1	XL_{24}
0	0	0	0	0	1	0	1	1	0	XL_{25}
0	0	0	0	0	1	0	1	0	1	XL_{26}
0	0	0	0	0	1	0	1	0	0	XL_{27}
0	0	0	0	0	1	0	0	1	1	XL_{28}
0	0	0	0	0	1	0	0	1	0	XL_{29}
0	0	0	0	0	1	0	0	0	1	XL_{30}
0	0	0	0	0	1	0	0	0	0	XL_{31}

Figure 16. Wordline Decoding

X Address										Row
A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_{13}	A_{11}	A_9	A_8	WL
0	0	0	0	1	0	0	0	0	0	XL32
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	0	1	0	1	1	1	1	XL47
0	0	0	0	1	1	1	1	1	1	XL48
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	0	1	1	0	0	0	0	XL63
0	0	0	1	0	0	0	0	0	0	XL64
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	1	0	0	1	1	1	1	XL79
0	0	0	1	0	1	1	1	1	1	XL80
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	1	0	1	0	0	0	0	XL95
1	1	1	1	1	0	0	0	0	0	XL992
•	•	•	•	•	•	•	•	•	•	• • •
1	1	1	1	1	0	1	1	1	1	XL1007
1	1	1	1	1	1	1	1	1	1	XL1008
•	•	•	•	•	•	•	•	•	•	• • •
1	1	1	1	1	1	0	0	0	0	XL1023

Figure 16. Wordline Decoding (Continued)

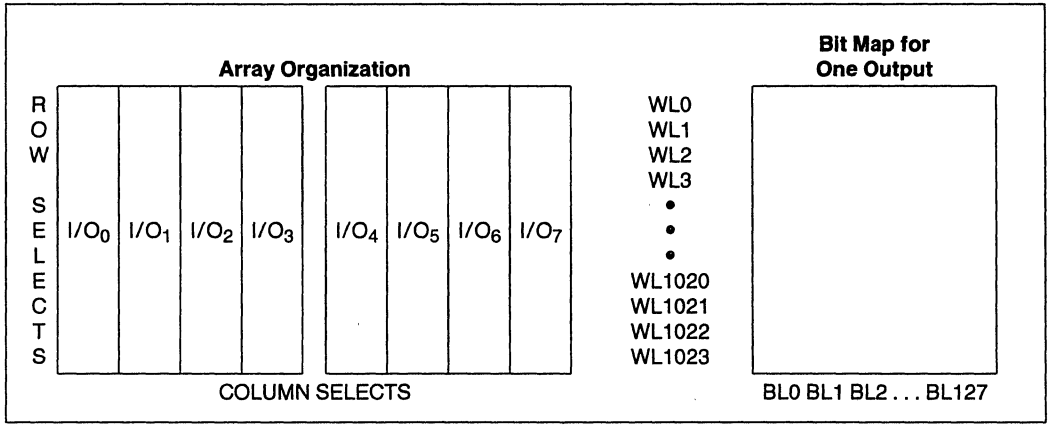

Figure 17. Bit Map

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FYI
MARCH 3, 1988

DON'T WRITE OFF THE U. S. IN MEMORY CHIPS!

The Japanese may own the dynamic RAM world, but the Americans are taking the lead in what ultimately may be the more important technology

Don't be too quick to write off the Americans in semiconductor memories—a business that's by far the biggest chip market going these days. The longer-term memory picture is definitely turning brighter for U. S. chip makers. This dramatic turnabout wasn't the subject of any paper or panel at the recent International Solid State Circuits Conference. But it was the biggest story, as far as senior technical editors Sam Weber and Stan Runyon were concerned, at a meeting they had already labeled the strongest ISSCC ever.

It seems clear that American memory technology now has a good shot at making a surprising and perhaps overwhelming comeback. While many foreign governments and corporate giants were investing hundreds of millions of dollars in chip plants to turn out millions of low-cost, low-profit dynamic RAMS, several U. S. semiconductor houses have been working quietly for several years to develop a new kind of memory that now stands an excellent chance of eclipsing the dynamic RAM's influence on computer design.

The potential of this new challenger, called the flash memory, is staggering (see p. 47). If the new class of memory moves into volume production as expected—and there seem to be few technological reasons for it not to—it will be denser, maybe faster, and more reliable than any other type of semiconductor memory. Flash memory not only will restore the memory-chip leadership to the U. S. if it pans out as we think it will, but also will radically alter computer architecture. It will likely displace magnetic disks for program storage as well as allow computers to be designed with all nonvolatile memory. The potential of the dense flash memories is so vast that Intel, which has been working hard on flash processes for four years, has decided to fold its triple-poly EEPROM program and concentrate instead on flash.

Flash may also be arriving just in the nick of time. Despite the glamour of reaching 16-Mbit parts, the dynamic RAM is running out of steam in density improvement. Trench capacitors and other processing and circuit tricks are troublesome and require painstaking care in processing. Flash memories, on the other hand, can be made with one-transistor cells, are highly scalable, and do not need elaborate engineering. While the Japanese may own the dynamic RAM world, the U. S. is in a strong position to take the lead in what ultimately may be the more important memory technology. **ROBERT W. HENKEL**

PROBING THE NEWS

HIGH-DENSITY FLASH EEPROMS ARE ABOUT TO BURST ON THE MEMORY MARKET

They could end up being the dominant low-cost, high-density memory

by J. Robert Lineback

The market is about to be hit with a wave of new electrically erasable nonvolatile memory chips that may soon match the bit density of dynamic random-access memories. This emerging breed of programmable read-only memories—built with single-transistor cells and called flash EEPROMs—could pack 64 Mbits on a chip by the turn of the century.

At least a half dozen silicon merchants—among them such giants as Intel, National Semiconductor, Texas Instruments, and Toshiba—are working on flash EEPROMs, using a variety of cell layouts (see figure). First out of the gate will be a CMOS 512-Kbit flash EEPROM, coming this month from Seeq Technology Inc. in San Jose, Calif. Right on Seeq's heels is Intel Corp., which has developed what executives will only say is a significant "process trick" for its flash parts that allows it to use the same design as in its ultraviolet erasable PROMs.

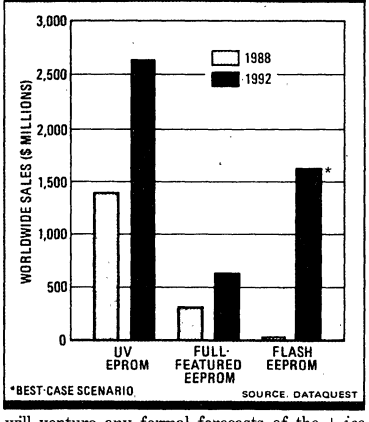
RADICAL CHANGE. Intel believes that by the year 2000, flash memories will emerge as the low-cost, high-density champion memory. If they are right, flash EEPROMs could radically change system architectures, making it possible to build computers with all-solid-state memory systems. The flash EEPROMs would be the only direct-access mass storage in the system, replacing disk drives feeding DRAM-based main memory.

Flash memories are a marriage of conventional EEPROM and EPROM technologies, offering the high densities of EPROM thanks to one-transistor cells. The write operation is like that of EPROMs, using hot-electron injection. The erase operation borrows the mechanism of floating-gate EEPROMs—electrical erasure by cold-electron tunneling.

Most full-featured EEPROMs have two-transistor cells and can reprogram individual bytes one at a time. In contrast, the entire contents of flash-EEPROM arrays are erased quickly and simultaneously. The flash memory trades selective-erase capabilities for space-saving single-transistor cells.

"Flash" also describes the way the new memory's market segment is expected to grow, surging from near nothing today to over $1 billion in the early 1990s (see chart, left). The flash movement has become so explosive that market researcher Dataquest Inc., San Jose, Calif., is waiting for key product unveilings before it will venture any formal forecasts of the business's growth. "We have made some initial estimates that show it could represent a third of the total nonvolatile area [by 1992], if all of the companies we think are going to be in the business are actually in volume production," says Mary Olsson, an industry analyst at Dataquest.

A BRIGHT OUTLOOK FOR FLASH EEPROMS



The potential density of EEPROMs is what has got everyone excited. DRAMs are hitting a density barrier, says Bruce McCormick, product marketing manager at Intel—it is getting harder and harder to reduce the space needed for the capacitors that store charge in each cell to retain data. Many flash-memory proponents agree. They see nothing but problems for DRAM makers trying to push the density of their parts in coming years.

Most observers also agree, though, that flash parts will not threaten DRAMs right away. Nor will they cut quickly into EEPROM sales. Right now they pose a real threat to EPROMs. Because of their high cost, conventional EEPROMs did not, as some thought they would, push EPROMs out of the market. Flash EEPROMs, however, could succeed where full featured EEPROMs failed.

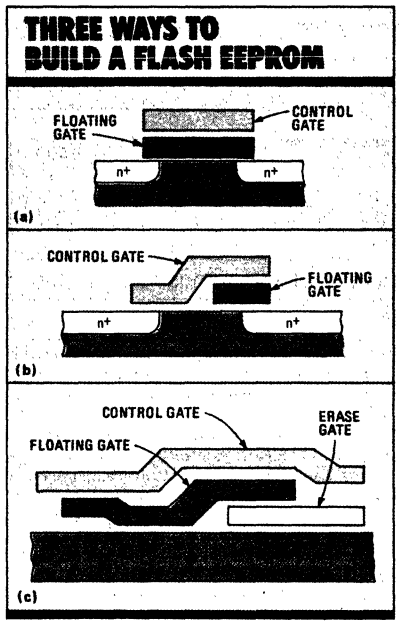
Although flash has tremendous market potential, vendors are being cautious about projections. "There will be room for all three types of nonvolatile memory: flash, UV-EPROM, and full-featured EEPROM," says Mike Vilott, vice president of marketing at Seeq. "There is a slight price and space penalty for flash, but there are also benefits." The benefits are electrical erasability and the ability to test parts, which can not be done for EPROMs in cheap windowless packages.

Two styles of flash memories are being developed by most suppliers. One is aimed at EPROM sockets, the other at price-sensitive EEPROM jobs that don't require byte erasure. Seeq is working on products in both styles.

Seeq, the first company to move flash EEPROMs into the marketplace with an nMOS part [*Electronics*, Aug. 21, 1986, p. 53], uses a split-gate layout. The top layer of polysilicon forms the control gate, slopping down over a portion of the channel to form a select device. The folded-structure cell takes up about 10% more space than a conventional EPROM cell, says Gary Rauh, strategic marketing manager at Seeq, which will use its split-gate design in the CMOS flash memories being introduced later this month.

Allied with Seeq and also working on the design of the two flash families is National Semiconductor Corp. The pact between Seeq and National, signed last fall, is aimed at establishing feature-set standards quickly in the emerging market. They need to move fast; coming up behind them are a host of major semiconductor merchants, notably Intel.

Managers at Intel won't say much



Intel stacks gates (a). Seeq extends a gate over the channel (b). Toshiba uses a three-level layout (c).

about the process fiddling they've done, except that it makes it possible to use an EPROM structure in flash memories. More than 100,000 256-Kbit chips have been produced at Intel's newly renamed Flash Memory Operation in Folsom, Calif., say managers there, and the new technique has helped Intel reach tight voltage-threshold margins in arrays. Control over the margins means Intel can make flash memories with cells that are very similar to those used in its high-density UV-EPROMs. The principal difference between Intel's flash EEPROM and its EPROM is that the gate oxide is thinner—100 Å instead of 350 Å.

At the 256-Kbit level, the cell size of Intel's flash is exactly the same as its EPROM, says Richard Pashley, general manager of Intel's Flash Memory Operation. Many competitors' cells are larger—they have had to modify stacked-gate circuit layouts to emulate the effects of phantom select devices. The devices prevent error-generating current leakage and maintain voltage thresholds.

Intel executives will not talk about timetables for specific product introductions, but they're promising big things ahead. "We are confident that our technology is scalable, and it will catch up with the density levels of DRAMs and UV-EPROMs. We see 20 years of scalability in this technology," says McCormick. The company plans to apply the flash process quickly to each new EPROM generation. "When you get out into future generations, there might be a slight size penalty, but today it is zero. We think we see ways of holding the size difference between future EPROM cells and flash memories to about 2%," says Pashley.

Also moving in is Toshiba Corp. The Kawasaki, Japan, company says it has begun selectively providing samples of 256-Kbit nMOS flash parts, which are based on a complex triple-level polysilicon structure using a relatively thick gate oxide region (500 Å). Toshiba officials decline to say when parts will become widely available, but observers believe the firm is working on a new CMOS design based on a recently disclosed NAND structure that shrinks cell size by some 30%.

And Hitachi Ltd. of Tokyo is also pursuing flash memory, specifically a 1-Mbit chip. Like Intel, Hitachi eliminates the select transistor to build a small cell, but its approach is different, using a double-diffused profile in the source and drain regions of the channel to prevent leakage.

Despite all the activity in flash EEPROMs, and the evident interest of major semiconductor companies, not everyone thinks they're the wave of the future. At Xicor Inc., for example, executives continue to believe that full-featured EEPROMs will be the EEPROMs of choice. "There are limits on write-erase cycles, and standards are not well defined when it comes to programming voltages," points out Krish Panu, Xicor marketing manager. "Some people are talking 21 V; others 12 V. But how long will it be before they have 5-V-only flash parts?" he asks. Xicor will use its thick-oxide technology to introduce a 1-Mbit full-featured 5-V EEPROM by the year end.

Although most flash proponents agree that 5-V programming would be an attractive feature, many believe it is not worth the price of adding charge-pumping circuitry to each chip. Still, several firms are reportedly exploring 5-V flash parts. Topping the list of those rumored to be doing so is TI, which will only confirm that it is working on products based on its its Array Contactless EPROM technology [*Electronics*, Nov. 27, 1986, p. 70]. Managers at its nonvolatile memory operations in Houston believe Texas Instrument's technology makes a good starting point for small flash cells, since 1.5-μm feature sizes are currently producing EPROM cells measuring 13.5 μm^2. Some of today's smallest flash memory cells are just over 20 μm^2. □

Nonvolatility: Semiconductor vs. Magnetic

Nonvolatility: Semiconductor vs. Magnetic

Organizer/Moderator: Richard Pashley, Intel Corp., Folsom, CA

Semiconductor nonvolatile memory is on the verge of challenging magnetic media for future computer storage applications. With solid-state costs dropping faster than rotating magnetic media costs, the cost of semiconductor nonvolatile memory should reach parity with magnetic disks before the end of the century. The advent of CPU miniaturization and personal computing may accelerate the conversion to solid-state by changing the traditional main-store user requirements. With distributed, processing, user memory requirements will shift to lower power, no wait state-access times, and a small light-weight for factor. How each technology will meet this challenge in the year 2000, will be reviewed.

Since their invention, rotating magnetic memories have dominated the computer main-store market. Their low cost and high density combined with their high endurance have been unsurpassed. The magnetic disk market has grown to a $20B annual sales level. The average hard disk cost is between $10 and $20 per Megabyte with densities of over a Gigabyte. Historically, magnetic disk costs have reduced 20% per year, which by the year 2000 should allow magnetic disks to break the $1 per Megabyte barrier.

The semiconductor nonvolatile memory revolution started with the disclosure of a 2Kb EPROM at ISSCC in 1971. EPROM nonvolatility was achieved by storing electrons on a *floating* gate. Unfortunately, EPROM erasure required a 15-minute ultraviolet light exposure to neutralize the electrons stored on the floating gate. Because of the relative difficulty of erasing an EPROM once it was in a system, the search began for an electrically-erasable memory. The solution was found with the announcement of a byte-erasable 16Kb E^2PROM in 1980. Still utilizing the floating gate for the storage element, the E^2PROM introduced electron tunneling for programming and erasing. Typically, writing was limited to the 10^4-10^5 cycles. But this was still not the cost-effective solution users wanted, as E^2PROM memory was 6-10 times more expensive than EPROM and trailed EPROM by 4x in density. Enter the *flash* memory. In 1985, a single transistor electrically-erasable flash memory cell, that writes like an EPROM and erases like an E^2PROM, was invented. Long term, *flash* memory density and cost could approach EPROM values. However, *flash* is a block erase memory with write endurance limited to 100 cycles today. Is *flash* the ultimate nonvolatile memory? Can *flash* endurance be extended to the 10^4-10^6 cycle range? Will there be an E^2PROM breakthrough that brings byte alterable memory costs closer to EPROM? Today, the combined nonvolatile semiconductor annual market size is under $1.5 billion with EPROM cost per Megabyte in the $100 range. Assuming the proven 70% silicon cost learning curve, *flash* memory will cost under a $1 per Megabyte and reach the 1Gb per chip density by the turn of the century.

Comparing today's cost of rotating memory to semiconductor nonvolatile memory, disks enjoy a 100x cost advantage over E^2PROMs. However, by the turn of the century, *flash* memory will achieve cost parity with disks. For low-density memory systems, cost parity may be reached much sooner. Magnetic media has a floor price that is limited by the cost of the disk drive itself, while semiconductor memory system cost is fairly linear with memory size. Clearly, magnetic disks will maintain their endurance advantage, but solid-state memory will offer substantially improved reliability without disk drive crashes, eliminating the need for tape drive backup. Furthermore, users can execute directly from semiconductor memory, whereas disk drive latency requires downloading into DRAM. This could be a 10x performance advantage for disk bound multitasking, multi-user systems. For portable systems, credit card format solid-state memory will offer a significant reduction in system weight, power, and space.

Will we see a major nonvolatile memory system architecture departure from disk to semiconductors? Can solid-state memory maintain its accelerated density/cost treadmill to catch disks? Is solid-state endurance of 10^4 write-erase cycles adequate? The panel will explore these issues and discuss the system interaction with evolving memory technologies.

Nonvolatility: Semiconductor vs. Magnetic

Synopses of Introductory Statements by Panelists

The nonvolatile data storage requirements for information processing and display applications increase as subsystems become more complex. During the past twenty years, developers of memory technologies have made enormous advances in improving memory device densities, speed and reliability. Nonvolatile memory systems are required in applications where it is vital that stored information not be lost in case of power failure. It is impractical, and in some cases impossible, to reload the memory under realistic operational conditions. The advent of nonvolatile and NDRO (Non-Destructive Read Out) memory technologies was a major milestone for the information processing system designer; as a result of this, significant commercial, aerospace, and military applications are currently emerging, utilizing these attributes. — *R. Fedorak*

In large nonvolatile memory systems, magnetic memories such as floppy disks and magnetic tapes have dominated the market. The cost of magnetic memories is very inexpensive. Magnetic memories, however, require mechanical mechanisms to operate the memory. The mechanical portion of the disk limits the reliability and the access speed of magnetic memory systems. E^2PROMs offer the nonvolatility, but do not have high density or low cost to replace magnetic memories. To realize a high-density electrically-erasable memory, the *flash* E^2PROM was introduced in 1984. In the near future, these *flash* high-density E^2PROMs will be expected to replace the magnetic memory. — *F. Masuoka*

Semiconductors are gaining exponentially on magnetic storage in density/component and cost at a particular density. A single transistor nonvolatile R/W technology will become the clear winner for converting this market. Recent advancements in microprocessor memory management facilities marry well with newly-developed flash technology to produce solid-state diskless computer-systems. Combined with anticipated R/W optical technologies, high-end systems are also envisioned. — *B. McCormick*

The current trend towards larger, more powerful, and more distributed 'personal' computers is also a trend towards machine-oriented, impersonal use. One way for the next breakthrough in personal computing to occur is to allow the customer to feel more powerful . . . more enabled through the use of a tool that is truly a personal aid, or agent. Solid-state memory components will play an important role in the coming generation of such tools. — *R. Mohme*

Todays high-density EEPROM is really a complete, random-access nonvolatile semiconductor memory system on a chip. EEPROMs are currently used in systems up to 4Mb to provide enhanced speed, reliability, power or temperature range operation. As 1Mb and 4Mb EEPROMs are developed, their cost per bit will continue to decrease and EEPROMs will become the best solution for larger nonvolatile memory systems in the future. — *W. Owen*

The user cost of rotating memories is currently between $10 and $20 per Mb. Historical cost reduction of 20% a year for disks will bring the ultimate user costs down the $3 to $6 per Mb range in five years. Smaller form factor, mass-produced disk drives also address the space, power and portability issues. All of this leads to the conclusion that both magnetic and semiconductor technologies will coexist for the foreseeable future. — *G.M. Scalise*

Organizer/Moderator/Panel Members

Fedorak, R., Project Engineer/Memory Technology-Information Processing, Naval Air Dev. Ctr., Warminster, PA
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McCormick, B., Marketing Manager/EEPROM, Intel Corp., Folsom, CA
Mohme, R., Project Manager/CPU Engineering, Apple Corp., Cupertino, CA
Owen, W., Vice President/Product Planning, Xicor Corp., Milpitas, CA
Pashley, R., General Manager/EEPROM Business, Intel Corp., Folsom, CA
Scalise, G.M., President, Maxtor Corp., San Jose, CA


R. Fedorak


F. Masuoka


B. McCormick


R. Mohme


W. Owen


R. Pashley


G.M. Scalise

Order Number: 295027-001

A 90ns 100K Erase/ Program Cycle Megabit Flash Memory

by Virgil Niles Kynett, Jim Anderson, Greg Atwood, Pat Dix, Mick Fandrich, Owen Jungroth, Susan Kao, Jerry A. Kreifels, Stefan Lai, Ho-Chun Liou, Benedict Liu, Richard Lodenquai, Weh-Juei Lu, Roy Pavloff, Daniel Tang, J.C. Tzeng, George Tsau, Branislav Vajdic, Gautam Verma, Simon Wang, Steven Wells, Mark Winston, and Lisa Yang

6

ABSTRACT

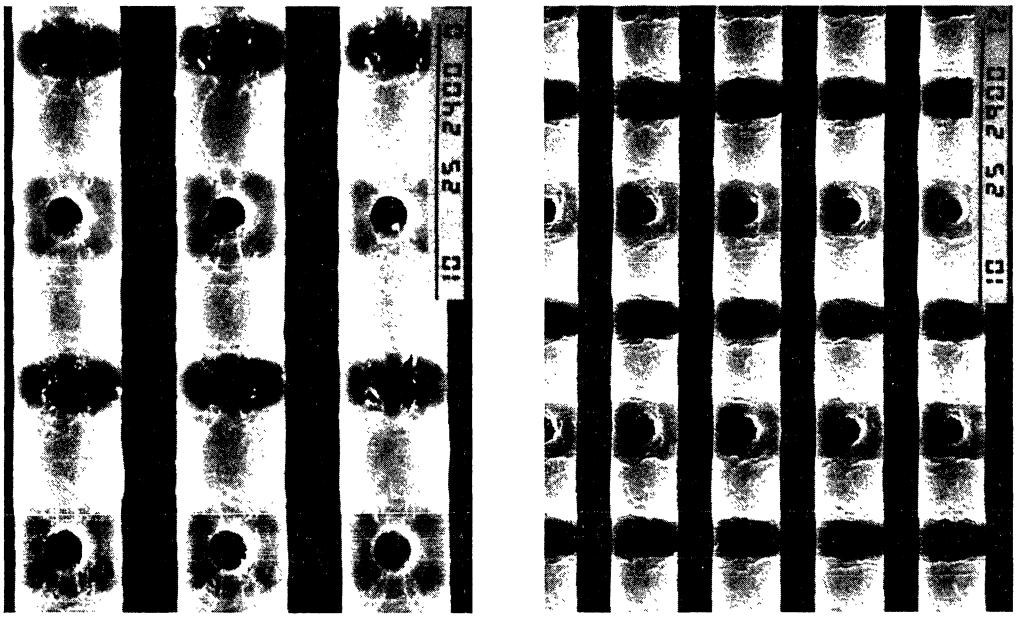
Using advanced 1.0μm CMOS technology, a 245 mil square 131072 × 8 device has been fabricated with a 3.8μm × 4.0μm cell. The memory exhibits a 90ns read access time with a 900ms electrical array erase and 10μs/byte program time. The device has been optimized for in-system microprocessor-controlled reprogramming with endurance performance greater than 100,000 erase/program cycles. Column redundancy is implemented with the utilization of flash memory cells to store repaired addresses.

ADVANCES in photolithography have made it possible to develop an electrically erasable reprogrammable 90ns 1Mb flash memory which is capable of greater than 100,000 erase/program cycles. This 1Mb memory implements a command port and an internal reference voltage generator, allowing microprocessor-controlled reprogramming [1].

The 90ns access time results from a high memory cell current (95μA), low resistance poly-silicide wordlines, advanced scaled periphery transistors, and a di/dt optimized data-out buffer. Using CMOS inputs, power dissipation is 40mW in the active state and 20μW in the standby mode. The memory electrically erases in 900ms and programs at the rate of 10μs/byte. The device contains thirty-two columns of redundant elements and utilizes flash memory cells to store the address of repaired columns. The use of the flash memory cell reduces the required silicon area significantly over the commonly found large metal-shielded EPROM cells [2].

The 1Mb flash memory was fabricated on a 1.0μm double poly n-well CMOS process. Silicide was utilized on the wordlines to help achieve the 90ns access time performance. The CMOS periphery circuits were constructed with 0.9μm L_{eff}, 250 Å gate oxide LDD transistors. The density of this 1μm flash technology is demonstrated on the 1.0μm and 1.5μm memory cell comparison shown in Figure 1. The 1.0μm memory cell has a 15.2μm² area, which is over twice as small as the 1.5μm memory cell. A microphotograph of the 245 mil², 128K × 8 flash memory is shown in Figure 2. The process/device characteristics are summarized in Table 1.

1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, New York, NY, February 15-17, 1989.



a) 1.5μ Lithography
(5,000 x magnification)

b) 1.0μ Lithography
(5,000 x magnification)

Figure 1. Array SEM microphotograph: (a) 1.5μm memory cell (6μ × 6μ) (b) 1.0μm memory cell (3.8μ × 4μ)

One of the most significant aspects of this device is its 100,000-cycle capability. A typical cell erase/program Vt margin is shown as a function of reprogramming cycles in Figure 3. After 100,000 cycles there still exists a 2.5V program read margin to insure reliable data retention. Accelerated retention bake experiments done at 250°C for 168 hours indicate that after 10,000 cycles the memory will exhibit only 0.7V program Vt shift. Program and erase time degrade slightly due to normal charge trap-up in the tunnel oxide (Figure 4). In addition, endurance reliability has been excellent with no tunnel oxide breakdown.

Table 1. Device Parameters

Technology	Cell	Periphery	Device
1.0-μm Lithography	Area = 3.8μm × 4μm	Tox = 250 Å	Die Size: 60116 mils²
1-Ploly, 1-Silicide	Gate Oxide > 100 Å	Leff N+P = 0.9μm	Organized: 128K × 8
N-Well CMOS	Read Current = 95μA	Xjn = 0.3μm	Access Time: 90ns
Epi on P+	Terase = 900ms	Xjp = 0.6μm	Active Power: 8mA
	Tprog = 10μs/byte		Standby Power: 4μA
			Package: 32-pin Cerdip

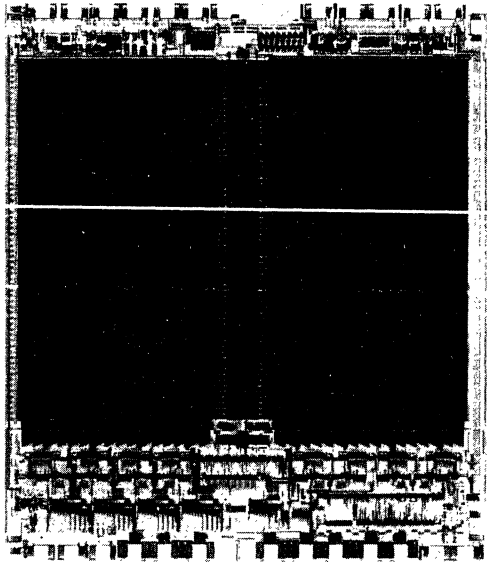


Figure 2. 1Mb die photograph

However, to build a manufacturable 1Mb flash memory, it is essential to be able to control the memory array erase Vt. The key is the proper selection of the erase Vt maximum and maintenance of a tight Vt distribution. The maximum erased Vt is set to 3.2V via the erase algorithm and the internal erase verify circuits [3]. Good oxide quality gives an erased Vt distribution width that does not change appreciably with cycling (Figure 5). The tight erase Vt distribution gives an order of magnitude of erase time margin to the fastest erasing cell (Figure 6).

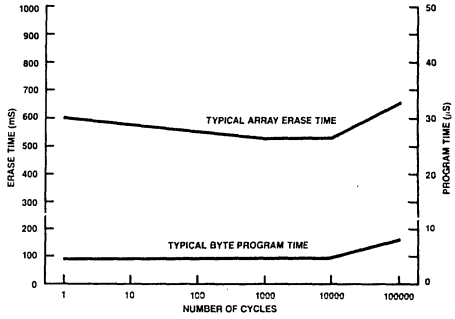


Figure 4. Erase/program time vs. cycling

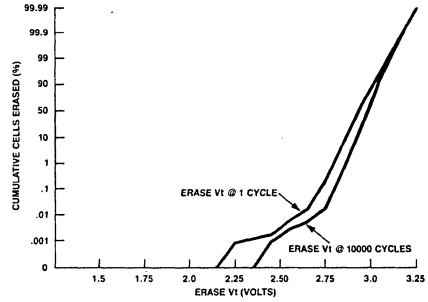


Figure 5. Erase Vt distribution vs. cycling

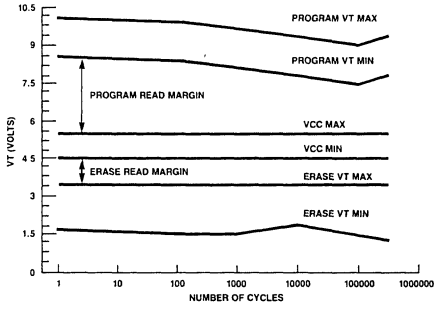


Figure 3. Array Vt vs. cyles

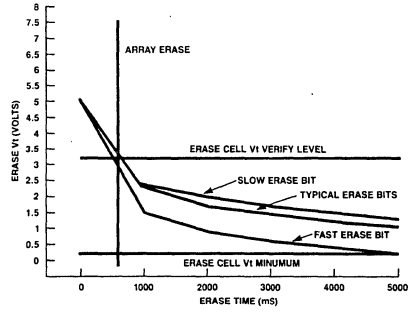


Figure 6. Array erase Vt profile vs. erase time

Array erase is executed by switching high voltage onto the source junction of all cells and grounding all select lines. The array source switch, shown in Figure 7, switches high voltage onto the source junctions. Transistor M16 is a very large device which pulls the source to ground during read and program modes. During erase mode, the high voltage latch formed by M5-M8 enables transistor M15, which then pulls the array source up to 12V. To obtain fast array erase times, this device must be made large enough to supply the grounded gate breakdown current which occurs on the sources of the memory array. The upper boundary on M15 current sourcing capability is set by the maximum allowable substrate current. If VPP is raised to 12V before VCC is above approximately 1.8V, the low VCC detect circuit formed by M1-M4 drives the node LOWVCC to 9V. Transistors M9-M11 then force the erase circuit into a non-erase state with M15 off and M16 on. When VCC rises above 1.8V, the chip will be reset into a read state.

Redundancy circuits consist of two flash memory cells combined with a cross-coupled bias and sense circuit ensuring low power consumption (Figure 8). When either M7 or M8 is programmed, the latch no longer draws power. By setting the levels of CLAMP and BIAS to Vt and 2Vt respectively, the B and BB levels are held to approximately one Vt. The signals F and FB along with the address signal drive the inputs to the XNOR circuits. The MATCH signals for all column addresses are combined to create the full match signal which enables a redundant column.

In summary, a 90ns 1Mb flash memory has been developed through the ability to scale the flash memory cell onto a standard CMOS 1.0μm technology. This memory has been optimized for in-system microprocessor-controlled reprogramming for more than 100,000 erase/program cycles.

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[3] V. Kynett et al., "An In-System Reprogrammable 32K × 8 CMOS Flash Memory," IEEE J. Solid-State Circuits, vol. 23, pp. 1157-1163, Oct. 1988.

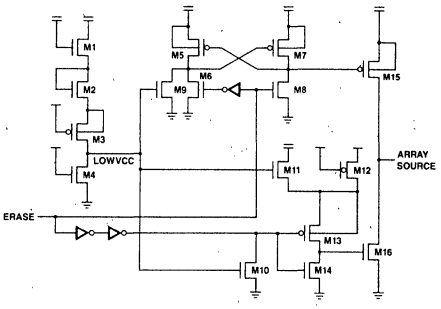

Figure 7. Array source switch

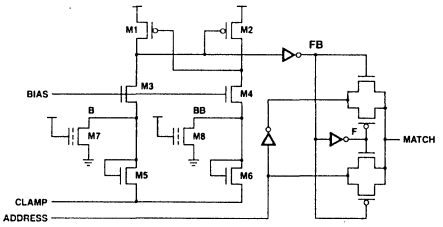

Figure 8. Redundancy circuits

SILICON BITS

Stan Baker

The Memory Driver

The primary driving force behind the personal computer revolution has been memory, not microprocessors. While one cannot give all the credit in one place, and microprocessors and software have their essential roles, the architectures and viability of these small computers has been due mostly to memory technologies—both semiconductor and magnetic.

That situation continues and more memory trends are afoot that will force computer systems in new directions in the near future. DRAMs are running out of the economic gas that has propelled the memory costs downward, not only leaving the door open for other memory technologies but demanding they enter.

Today's memory technologies are bubbling with new possibilities that will further revolutionize systems. At the heart of the changes will be nonvolatile devices. And the major player there will be flash technology.

The initial personal computers could have been made with CPUs that were not fully integrated, using gate arrays, LSI discrete logic or 2901 bit-slice architectures. But they could not have been made without low-cost, dense DRAM chips and low-cost floppy disk drives. The success of PCs then gave the economic stimulus to miniaturize hard disks which stimulated the PC business further.

The center of the computing universe is the data, not the processing engine. And the data is in the memory. And the ideal memory is nonvolatile.

Besides changing systems, the nonvolatile technologies will also alter the architecture of the semiconductor business internationally, with large scale impact on trade, political, and macro-economic issues. The leaders in the nonvolatile technologies are American companies. And they will not license their technology so readily as in the past.

There is a host of possibilities from flash, EPROM, EEPROM, battery backing, magnetic, optical, and the more remote ferroelectric technologies. Ferroelectric comes the closest to being the ideal nonvolatile RAM, but it is the furthest from reality. However, flash is here and, for the first time, promises to bring nonvolatile devices into the processing heart of computing systems in a big way.

Flash memories can have smaller cells than DRAMS and will be able to get more benefit from the latest lithographic and other processing equipment than DRAMs will. With only a year on the market the bit-count of flash devices has caught up with EPROMs and DRAMs, all now at 1 megabit per chip.

The 1-Mbit flash device just introduced by Intel has a die of 60,000 square mils. Current 1-Mbit DRAMs are larger, at about 70,000 square mils, and 256 kilobit SRAMs use about 75,000 square mils. 1-Mbit EEPROMs are about double, on the order of 130,000 square mils.

Flash will continue to track EPROM densities and soon outstrip even DRAMs, according to Richard Pashley, general manager of Intel's nonvolatile memory business. The only memory technologies that continue to track lithography in their cell size are EPROMs and flash devices.

Flash devices can be read as rapidly as EPROMs or DRAMs. But writing into them takes tens of microseconds per byte. And they are bulk erased in tens to hundreds of milliseconds.

Such long erase and write times may seem extremely limiting at first thought. But actually, the bulk of program and data storage does not need fast erase/write. That is why magnetic storage is so important. And that is what has some flash memory marketeers so excited—especially at Intel, which is nowhere in the DRAM and SRAM businesses, but the world leader in EPROMs. For flash devices are very similar to EPROMs.

Consider this example. If a computer were constructed with megabytes of fast volatile RAM directly serving the CPU, that can be erased and rewritten rapidly, massive blocks of nonvolatile flash RAM can take the place of magnetic storage backing that volatile memory. A few 4-Mbit flash chips will carry more data than most floppy disks.

That backup storage will significantly speed-up system performance and eliminate electro-mechanical reliability problems, as well as lots of weight and power drain. The flash devices can also be used to reduce the amount of volatile RAM, because some is used to store programs and data that seldom needs to be erased and changed. Such write-seldom sections of memory can be updated in a second or so, which is less than would irritate a human operator.

Fitting in this scenario, future microprocessors will have more and more memory on their die. That will be a good place for the fast RAM, made even faster by eliminating the inter-package wiring. And these internal RAMs will be organized to match the processing characteristics of the CPU which is not the case now with discrete RAMs. The flash and EPROM devices can then connect directly to the microprocessor package, eliminating discrete DRAMs and SRAMs.

Memory companies everywhere are working on flash devices. But Seeq Technology and Intel were the first to market. Since then, Texas Instruments and Toshiba have introduced versions. But Intel seems to be the only one supplying in significant volume, and it's Intel that has put the most corporate commitment—money and talent—behind flash. At Intel, flash technology plays directly off its EPROM technology in which Intel is still the world leader.

A passion for flash

According to Pashley, "flash is the way Intel will get back in the read-write memory business." In Pashley, Intel and perhaps the industry has its flash champion, and the success of any new technology depends on having the capable individuals that have the faith and lead the charge.

Pashley was the pioneer of scaling, the technique of shrinking MOS devices that is fundamental to the evolution of more and more dense MOS ICs. His process at Intel was termed "HMOS."

At the recent ISSCC in New York Intel described its 1-Mbit flash memory chip. Seeq Technology and National Semiconductor, who are jointly working on flash devices, described a 1-Mbit as well. And Texas Instruments described its latest flash, a 256k device that uses only a single 5-V supply.

Executive Comment

By Laurence R. Hootnick

Memory Life-Cycle Costs

Today's memory market is inundated with competing alternatives.

Given so many choices, designers will tend to specify a part based on its density, read/write speeds, flexibility, reliability and space and power requirements. Purchasers, however, are more sensitive to a given memory's price (cost per bit) and availability.

Without question, these are the proper criteria on which to judge a memory's merits and identify the right mix for specific application needs. But there should be one more: life-cycle cost. Those who specify memories must consider how much a technology is costing them over the lifetime of the system because of its inherent performance and/or reliability limitations. Such costs are incurred in several ways:

• **Manufacturing/Assembly.** Systems manufacturers who use ROMs to store code know they have little flexibility if that code ever needs to be changed. New masks must be made, old inventory scrapped, nonrecurring engineering (NRE) charges paid and weeks of potential production wasted.

EPROMs remedy these problems to a certain degree. However, if the EPROM has already been programmed and code changes are required, then the manufacturer is faced with the undesirable task of disassembling the system, pulling out the EPROM (and running the risk of damaging it), erasing and reprogramming the device and reassembling the system.

If, instead, a manufacturer decides to pay a high unit cost up front to obtain the in-system electrical erasure of EEPROMs, it is likely to mount them in sockets because of relatively high failure rates, thereby incurring even more costs from the socket, the added space and failed products. In-system electrical erasure eliminates the inventory problems of ROMs and the update limitations of EPROMs, yet EEPROMs frequently lack the required density and ongoing reliability needed by many systems.

On the other hand, Flash memory offers a mix of performance characteristics to provide the optimum cost efficiency: in-system electrical read/write capability and proven reliability.

• **Customer Service.** If your company has a service organization chartered to maintain systems once they're sold, then chances are your service technicians travel to customer sites, pull apart systems, diagnose problems and perhaps end up reprogramming the EPROMs or replacing dead batteries. Because of the handling required for reprogramming and the likelihood of damage, they may even be replacing the old memories with entirely new ones because each unit is so "inexpensive." But how much does this procedure cost—in time, labor, parts ... and in customer inconvenience?

With Flash memory, a technician can read the memory remotely over a phone line, diagnose the problem and perhaps correct it through an immediate rewrite of the memory—or at least identify the exact problem and take the correct replacement parts with him on the initial service call. This reduces the number of service calls as well as the duration of those calls still required.

This level of service could save a systems supplier with a large installed base a tremendous amount of service labor and time, as well as improve its customer relationships through improved product reliability.

• **Response to Market Needs.** Most systems have their own carefully formulated cost-effectiveness lifetime, after which their features may become obsolete because of continually emerging state-of-the-art alternatives. Premature obsolescence makes for a costly system.

Consider the possibilities instead if your embedded system could be updated in the field. For example, a printer or copy machine or modem could be feature customized using an in-system read/write nonvolatile memory. The system could be updated not only at the very end of your manufacturing line, but potentially also by your reseller to meet a customer's immediate requirements—or, at some point in the future, at the customer's site over a phone line to provide added or enhanced features as they become available or desired.

The memories available previously, such as static RAMs and EEPROMs, that could achieve this level of functionality, come up short on some of the other key criteria used by the design/purchasing team, such as density, cost per bit and reliability.

In contrast, Flash memory combines the key memory characteristics (fast read/write capability, inherent nonvolatility, low cost per bit, reliability and density) to provide a balanced solution.

The most-effective memory purchase decision, therefore, is not limited to short-term price and availability issues. Rather, an analysis of how a particular technology might impact different organizational bottom lines can yield much more significant, long-term cost savings for your company.

The most-effective memory purchase decision is not limited to short-term price and availability issues.

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Flash Memories: The Best Of Two Worlds

By
RICHARD D. PASHLEY
STEFAN K. LAI
INTEL CORPORATION

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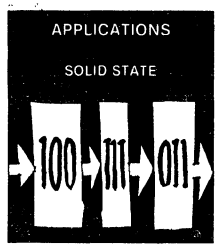
Flash memories: the best of two worlds

Filling a niche between conventional EPROMs and EEPROMs, these dense memories offer the latter's reprogramming convenience at relative cost advantages



In evolving from a concept paper in 1984 to megabit devices only five years later, flash memories have moved up the transistor-density curve faster than any previous semiconductor memory IC. They are based on the technology of either erasable programmable ROMs (EPROMs) or electrically erasable programmable ROMs (EEPROMs), and in price and functionality fall somewhere between the two, suiting any applications that require the former's denser storage plus the latter's ability to be reprogrammed without removal from a system. They also share these memories' nonvolatility and fast read access.

Those flash devices more akin to EPROMs cost less and promise rapid device and price scaling; their suppliers include Intel Corp., Santa Clara, Calif.; Seeq Technology Inc., San Jose, Calif.; and Tokyo's Toshiba Corp. The others, which utilize the more complex EEPROM technology, are slightly more expensive but provide more flexible reprogramming. They are made by Texas Instruments Inc., Houston, Texas, and sampled by Atmel Corp., San Jose, Calif., among others.

Of these three types of reprogrammable memory, EPROMs remain the best choice for applications where data almost never needs changing. Otherwise, flash memory devices should be considered. Although the average EPROM may sell for about $7, and a flash memory for about $25, the differential is wiped out by the expense of a single reprogramming. The in-system reprogramming of a flash device may cost as little as $1, whereas pulling an EPROM out of a system to erase it by exposure to 20 minutes of ultraviolet (UV) light may cost over $80 when equipment, downtime, and labor are factored in.

Meanwhile, EEPROMs should remain popular wherever it is necessary to erase bytes selectively. But flash products, which are erased in their entirety or section by large section, might do better for updating stored logic, when this must be done more than once but less often than in main memory, cache memory, or registers. Reprogramming costs are similar, but flash memories are less than half the price of EEPROMs.

Flash memories may even oust some battery-backed static RAMs (SRAMs), a bulky combination. In laptop computers, the flash device would occupy less space, at a lower cost per bit, and eliminate the dependency of memory on battery power.

Most flash memories have the same pinout as EPROMs, so that substituting them in a system requires primarily software alterations. (The densest flash ICs may have a few extra pins, however.) Furthermore, whereas a flash memory will nearly always be surface-mountable, that is not the case for some applications of EPROMs, whose packages include a window that must be accessible to UV reprogramming equipment. A flash-for-EEPROM swap, though, will almost certainly require rerouting the printed circuit, because flash memories may be up to four times denser.

Also, flash ICs closer to EEPROM technology need only a 5-volt supply, whereas those closer to EPROMs require a 12-V one as well, to drive the high-energy electrons that write data into them. This kind also requires a multistep algorithm that verifies erasure. Its makers say that the 12-V supply helps protect the IC against accidental erasure; those that supply 5-V-only versions counter that there are software techniques that may be employed to render such an accident too rare to be worth consideration.

The choice between the two flash memory types is sometimes determined by the application. In small embedded controller systems, missiles, or remote battery-powered systems, a 5-V-only flash memory is preferable. On the other hand, a 12-V supply is already available in some systems, such as desktop personal computers and laser printers.

With software of all kinds becoming more complex, the likelihood of changes to it, to update it or eliminate bugs, increases proportionately. That, in turn, argues for efficiently reprogrammable nonvolatile memories, and bodes well for the popularity of flash memory.

Consider the basic I/O system of a PC. It is typically stored in ROMs or PROM. Flash memory would allow the changing of I/O system code over a network or modem within minutes.

Also, portable computer systems' hard-disk drives may be replaced by flash memory modules offering lower cost, size, and weight, plus the greater reliability of solid state.

The operating system for an IBM PC AT or an Apple Macintosh is big enough as a rule to need storing on magnetic hard disk. With each year, however, flash ICs become more economical for greater amounts of storage; up to 2M bytes of flash memory are available with a new laptop from Psion Inc., Watertown, Conn., for example [see photo]. As this trend continues, flash ICs may supplant hard-disk drives of small capacity (up to 10 megabytes) in systems that could use a small, reliable memory with low power

Richard D. Pashley and Stefan K. Lai Intel Corp.

Defining terms

Electron trapping: the accumulation of electrons in imperfections in silicon dioxide, so that negative charge builds up and delays erasure of programmable memory devices.
Fowler-Nordheim tunneling: a quantum mechanical process in which electrons tunnel through a thin dielectric from (or to) a floating gate to (or from) a conducting channel—the erase mechanism in flash memories and the program and erase mechanism in electrically erasable programmable ROMs (EEPROMs).
Hot-electron injection: in this context, the injection into the memory cell's floating gate by a vertical electric field of electrons with excess energy acquired from a high source-to-drain channel electric field.
Nonvolatile memory: memory that does not lose stored bits after power is switched off (includes ROMs, PROMs, EPROMs, EEPROMs, and flash memories).

Psion Inc

The MC400 laptop computer from Psion Inc., Watertown, Conn., uses flash memory modules to replace disk drives. The computer has four module slots, and each module contains four Intel 128K-bit flash ICs in plastic leaded chip-carriers for a total of 2M bits of memory. The primary requirement for switching from disk to solid-state memory is rewriting the operating system's memory management code. Psion also makes an accessory that lets the user plug the MC400's modules into any IBM Corp. or compatible personal computer.

consumption. In such cases, though, another software modification becomes necessary. Data is stored in serial form on hard disk, and must be reformatted into bytes before it can be sent to RAM. Data stored on flash ICs is already in byte format, and operating systems are being rewritten to accommodate this.

At present, the programs for embedded controllers, such as those that operate automobiles and production machinery, are kept in other forms of nonvolatile memory. But flash ICs could serve here, too. And they could also speed up laser printers. Much of the formatting font and size information, along with the data to be printed, must now be loaded for each page from the central processing unit to the laser printer. Flash memory in a laser printer could store the font information for an entire print session just the once, so that pages would print out one after the other with less delay. A change in print session parameters would simply invoke an erase/reprogram cycle.

Flash memories are also candidates for use in flight data recorders and in communication equipment where parameters change often to accommodate different data communication formats.

Flash technology

Even as semiconductor memory began displacing magnetic core memory in the early 1970s, the inability of RAMs to retain data after power was turned off remained a problem. The invention of the nonvolatile EPROM deserved to be successful, despite the clumsiness and low repeatability of UV erasure. EEPROMs subsequently offered speedy in-system erasure with a strong electric field, which, however, at 12 megavolts per centimeter, so stressed the device's tunnel oxide as to limit the number of erase and write cycles possible. Also, the EEPROM memory cell, larger than the EPROM's, meant less favorable economics.

Accordingly, the challenge for semiconductor engineers was to fabricate a memory with the EEPROM's electric erasability but priced more like an EPROM, of comparable memory retention and cell size, and higher read/write cycling capability. Like both devices, the new one was to have high-speed read access. The flash memory is the response to this challenge.

Most flash memories are programmed with the EPROM's hot-electron injection technique. Each memory cell's field effect transistor (FET) is turned on or off by the absence or presence of charge on a floating gate sitting above the conducting channel. Electrons accumulate on the floating gate because of the field produced by a large positive voltage on the select gate above the floating gate, and a similar voltage on the drain while the source is grounded. Once on the floating gate, the electrons are trapped there by the surrounding nonconducting oxide. The electric field they produce will then turn off the FET, storing a logic 0 in that bit location. Where no excess electrons are trapped on the floating gate, the FET's channel can conduct current and the cell has a logic value of 1. Thus, both in cell structure and in programming technique, the flash memory is very similar to the EPROM.

All flash memories are erased electrically in the system and in 1 or 2 seconds, like EEPROMs, but in bulk, like EPROMs. Electrons tunnel back into the source region in response to an electric field between gate and source. Some devices have been designed to make programming and erasing consistent with microprocessor control. The EEPROM's individual byte erasure is made possible by equipping each memory cell with a second, select transistor, and by forgoing the select transistor to obtain bulk erasure, flash memories can be built with much higher densities than EEPROMs.

Structurally, the flash memory cell is like the EPROM cell, being only slightly larger and with a thinner gate-oxide layer, usually 10–20 nanometers deep. But each supplier of flash memories has taken a slightly different approach to the device. Intel uses its ETOX (EPROM tunnel oxide) technology. Seeq employs a "phantom transistor" approach, which has a stepped-gate structure. Toshiba employs a triple-polysilicon, three-gate design. TI's is also a stepped, two-gate structure, with a thin dielectric to ease electron tunneling to the floating gate. The first three designs are programmed by hot-electron injection and erased via Fowler-Nordheim tunneling. TI's design depends on tunneling for both the write and erase mechanisms.

The Seeq cell puts a second transistor in series with the first to control erasure and also enable the erasure of small subsections. The approach in effect lengthens the channel, however, and limits programming performance. Programming and erasure occur through the same junction, stressing the gate oxide and guaranteeing fewer than 10 000 cycles, although up to 100 000 is typical.

Toshiba's flash cell is the most complex and largest of these three. It has a phantom transistor like Seeq's, also to control erasure. It has another layer of polysilicon for erasure through a polysilicon-to-polysilicon oxide. The poly-to-poly-oxide erase path requires higher voltage than either the Intel or the Seeq flash cell. Tunneling through poly-to-poly oxide tends to trap more electrons, so that the cell threshold increases with cycling. As a consequence, Toshiba's memory cells are specified for 100 cycles, and to 1000 cycles with special electrical screening tests.

TI calls its flash memory a merged-transistor advanced contactless EEPROM. The cell transistor and pass transistor are

merged so that its flash memory cell is structurally similar to Seeq's phantom cell, except that it has a thin (10-nanometer) oxide tunnel window for programming erasure.

Intel's cell is programmed through the drain, and erased through the source, which results in the reduction of stress on the gate oxide and a typical cycling capability in the 100 000 to 1 million range. The cell is smaller than the other three, which means not just smaller chips and more of them per wafer but a faster-to-program device with a shorter channel length.

The Intel cell uses a single FET with a floating gate for storage. To program a row of eight cells (a byte), the row decoder selects them and drives them to 12 V. The bits within the byte that are to be programmed as logic 0 are selected by the column decoders, which takes them to about 7 V.

Typically, hot-electron programming takes less than 10 microseconds per byte while tunneling takes between 5 and 20 milliseconds per page for programming, per chip for erasing. For bulk erasure, a second is more than adequate, and the reduced stress on the flash memory's gate oxide (compared with the EEPROM's) markedly ameliorates oxide-related problems that affect memory retention, time to program, and time to erase. All involve mechanisms affecting device quality and reliability.

Quality vs. reliability

IC quality is not to be confused with IC reliability. Quality describes how closely a chip conforms to its specifications upon delivery and is a manufacturing concern, dependent on the thoroughness of testing processes. Reliability describes how closely an IC continues to conform to its specifications over years of use, measured by failure rates of components that have been qualified and installed in fielded systems. Reliability will bear on the overall cost of ownership of a system because repair in the field costs far more than repair during production.

The failure mechanisms usually associated with program/erase cycling of electrically erasable memories (EEPROMs and flash memories) are charge loss due to latent oxide breakdown and electron trapup. Both manifest themselves when a device cannot be reliably programmed or erased within the maximum time specified.

To reduce oxide breakdown, a chip manufacturer can both improve oxide quality and attempt to reduce the stress on the tunnel oxide during programming and erasing. With Intel's flash IC, for example, the area of oxide involved (and the area that is stressed by the electric field) is confined to an overlapping area between source and gate. In addition, the reduction in electric field intensity across the tunnel oxide in flash memories to 10 MV/cm from the 12 MV/cm typical for an EEPROM theoretically should increase its reprogramming durability. In experiments where over 2000 Intel 1M-bit flash memories were cycled more than 20 000 times, none of the devices failed because of oxide breakdown, and several devices survived 1 million program/erase cycles.

The smaller the memory cell, the less capacitance it has, and the less charge need be added or removed for programming or erasing. Trapup is directly related to the amount of charge moving through the oxide, so the smaller charge requirement will tend to postpone its occurrence, stretching it out over many more program/erase cycles than for larger cells, with higher capacitance. Thus, the larger the cell, the more susceptible it is to trapup, and the more programming or erase pulses it will take to push sufficient electrons onto or off the floating gate.

Beyond the cell itself, peripheral chip functions and oxides are affected by repeated program/erase cycles. In general, the higher those voltages, the more vulnerable the peripheral circuitry is to functional failures. Intel's flash memories need no more than 11.4 V to meet their program/erase specifications. Other flash memories that require the same nominal 12-V external supply have on-chip charge pumps and internal voltage levels of 20 V and higher. These voltages put more stress on peripheral circuit oxides, to the possible detriment of reliability.

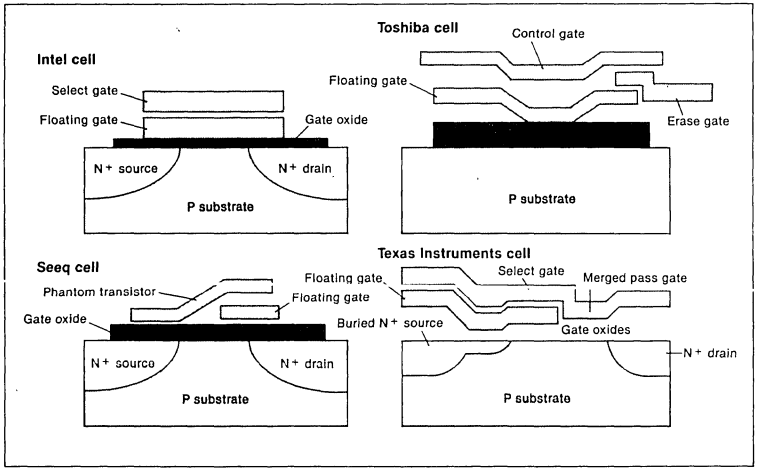
Looking down the road

CMOS is today's mainstream technology for both logic and memories. Within that technology, EPROMs and flash memories should be more scalable than dynamic RAMs (DRAMs) or SRAMs and EEPROMs. At a first level, there are differences in memory cell complexity. SRAM cells have four or six transistors. Turning transistors on or off to store logic levels (writing) is faster than storing charge in a capacitive well (DRAMs) or on a floating gate (EPROMs, flash memories, and EEPROMs). Sensing logic levels (reading) on SRAMs is also faster than on the other devices. But the price of that speed is increased cell complexity. Absolute SRAM cell sizes are over 10 times larger than for single-transistor devices (EPROMs and some flash memories) and scaling is more complicated because all dimensions cannot be reduced proportionately without upsetting some minimum spacing rules between lines and active devices. For example, distances between devices may not be allowed to shrink proportionately with line widths.

An EEPROM cell, employing both a bit-storage and a select

A comparison of flash ICs, EPROMs, and EEPROMs

Company, location	Density	Access time, nanoseconds	Power consumption, milliamperes	Erase/write cycles	Minimum erase area	Erase/write times	Voltage requirements, volts
Flash memories							
Intel Corp., Santa Clara, Calif.	1M bit	120	30	10^4	Bulk	1 second/chip, 10 μs/byte	5/12
Seeq Technology Inc., San Jose, Calif.	1M bit	200/250	30	10^3	Sector, bulk	12 seconds/chip, 525 μs/byte	5/12
Texas Instruments Inc., Houston, Texas	256K bits	170	15	10^3	Bulk	15 ms/chip, 15 ms/page	5
Toshiba America Electronic Components Inc., Irvine, Calif.	256K bits	170	30	10^2	Bulk	100 ms/chip, 200 μs/byte	5/12.75
Electrically erasable programmable ROMs (EEPROMs)							
Simtek Corp., Colorado Springs, Colo.	256K bits	120	80	10^5	Byte	10 ms/chip, 160 μs/byte	5
Xicor Inc., Milpitas, Calif.	1M bit	200	50	10^5	Byte	5 ms/page	5
Erasable programmable ROMs (EPROMs)							
Microchip Technology Inc., Chandler, Ariz.	256K bits	55	65	Up to 100	Blanket, ultraviolet	20 minutes max.	5/12
Texas Instruments Inc., Houston, Texas	1M bit	170	50	Up to 100	Blanket, UV	20 minutes max.	5/12



Of the four approaches to flash memory technology, Intel Corp., Toshiba Corp., and Seeq Technology Inc. have chosen designs closer to EPROM technology, Texas Instruments Inc. one closer to EEPROM technology. Flash memory cells are similar to an EPROM cell, except they have shallower gate oxides, usually 10–20 nanometers deep, to allow Fowler-Nordheim electron tunneling. Intel's cell employs a single field-effect transistor with a floating gate for storage, and is programmed and erased through different areas of its gate oxide. Seeq employs a stepped-gate, two-transistor structure; the second transistor helps control erasure and also enables the erasure of small subsections. Toshiba's cell has a triple-polysilicon, three-gate design; it also uses an additional transistor to control erasure. The source and drain of the Toshiba cell are perpendicular to the plane of the page. These three designs are programmed by hot-electron injection and erased by tunneling. TI's cell is also a stepped-gate, two-transistor design, but its oxide layer is constructed to ease tunneling, upon which it depends for both its write and erase mechanisms. Though several of these designs have more than one transistor, only the memory cell is depicted. Intel and Seeq are currently the only two companies producing 1M-bit flash memory products.

transistor, is over 2.5 times the size of a flash cell. Here, too, the added complexity and high voltages required may make proportionate scaling (equal reduction of dimensions and spacings) somewhat elusive. Surprisingly, even the DRAM cell, composed of a select transistor and a storage capacitor, is over 1.5 times as large as the flash memory cell. But on today's submicrometer scale, planar DRAM capacitors hold too little charge for reliable bit sensing, so that designers have gone to three-dimensional structures, such as stacked or trench capacitors. These constructions complicate manufacturing, reducing reliability and raising costs.

Having an active memory-cell transistor sense current like an SRAM and lacking the soft-error sensitivity of DRAMs, flash and EPROM technology may well be the most scalable memory technologies by the year 2000.

In geological terms, 10 years is insignificant, but in solid-state technology, 10 years is one-fourth the age of the transistor. However, by the year 2000, a 256M-byte flash memory using 0.25-micrometer geometry on a die 0.7 inch on a side is projected to sell for $1 per megabyte. Alternatively, less flash memory could be combined on the same die with application interfaces, such as high-speed data transfer interfaces, similar to today's burst mode, page mode, and "nibl" mode transfer schemes.

Several 256M-bit flash devices, without today's on-chip control features, may form a multichip memory subsystem run by a single controller IC, akin to the DRAM and DRAM controller subsystems of today. In embedded control systems, the flash memory device may be combined with other application-oriented logic to simplify and shrink the design and lower its cost. Such chips will be similar to EPROM-resident microcontrollers (such as Intel's 8748, 8749, and 8751) but have far more memory and can be much more functional than microcontroller processors.

The tendency is to view nonvolatile memories as vehicles for software modification; but in the future they may also be used to change the functions of hardware. Just as some of today's programmable logic devices (PLDs) use SRAM to control logic programming, tomorrow's PLDs may use flash memories for the same function. One other area in which flash memories promise to contribute is neural network systems, or processors that mimic the way the human brain works. It is likely that computers based upon neural networking concepts will use flash memories or EEPROM memories as key elements of their processing units.

To probe further

The first concept paper on flash memories was presented by Toshiba Corp., Tokyo, at the 1984 International Electron Devices Meeting. The 1984 *IEDM Technical Digest* can be ordered from the IEEE New Jersey Service Center, at 445 Hoes Lane, Piscataway, N.J. 08855; or call 201-562-5493.

The nonvolatile memory section of the 1989 International Solid- State Circuits Conference (ISSCC) *Digest of Technical Papers* contains papers on flash technology from Intel Corp., Santa Clara, Calif.; Seeq Technology Inc., San Jose, Calif.; and Texas Instruments Inc., Houston, Texas. It is also available from the service center.

The paper, "A 90ns One-Million Erase/Program Cycle Megabit Flash Memory," from Intel Corp., was published in the October 1989 *Journal of Solid State Circuits* special issue on logic and memory.

About the authors

Richard D. Pashley (SM) has served as general manager of Intel's Flash Memory Operation, Folsom, Calif., since April 1986. The previous five years he was director of Intel's Technology Development group in Santa Clara, and before that, he managed Intel's static RAM, static logic, bipolar memory, EPROM and EEPROM technology development activities. In 1976, Pashley developed Intel's HMOS (high-performance metal oxide semiconductor) process technology. He holds a doctorate in electrical engineering from the California Institute of Technology in Pasadena.

Stefan K. Lai (SM) has been engineering manager for Intel flash memories since 1986. As program manager for flash memory technology development during the two years prior to that, he co-invented Intel's ETOX (EPROM tunneling oxide) flash memory process technology. From 1979 to 1982, he worked at IBM Corp.'s Thomas J. Watson Research Center, Yorktown Heights, N.Y., where he was involved in tunnel oxide dielectric research. He holds a B.S. in applied physics from the California Institute of Technology and a Ph.D. in applied quantum physics from Yale University, New Haven, Conn. ◆

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PC Standard in the Cards

BY TOM WOLFE

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AGREEMENT AT HAND FOR IC-BASED STORAGE MEDIUM

PC standard in the cards

BY DAVID LAMMERS

Tokyo — Agreement could be imminent on a Japan–U.S. standard for the "PC Card," a 2 × 3-inch IC-based card to be used as a removable data-storage medium for portable computers.

Expectations are high that this transPacific standard will do for notebook and laptop computers what MS-DOS, the floppy disk and the IBM PC did for desktop machines: allow software to be sold for, and data to be exchanged over, a medium compatible across a broad range of portables from a long list of manufacturers worldwide.

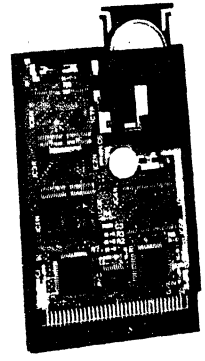
With notebook and low-end laptops expected to constitute half of Japan's PC market by 1994—and perhaps a third of PC sales around the world by then—approval of the standard is especially important to U.S. computer and software companies. Proponents of the PC Card concept hope that, with the standard approved, software vendors will quickly begin porting applications to the cards and users here and in Japan will embrace the new technology.

The PC Card standard is being forged by the Personal Computer Memory Card International Association (PCMCIA) and the MITI-affiliated Japan Electronics Industry Development Association (JEIDA), which includes about 40 major Japanese companies. The 70-member PCMCIA includes nearly all of the personal computer industry's movers and shakers, with IBM, Lotus Development Corp. and Microsoft Corp. playing particularly active roles.

Today and tomorrow in Seattle, Microsoft will host the May meeting of the PCMCIA, at which members are expected to approve a draft agreed to in Tokyo on May 10 by PCMCIA members and the memory card working group of JEIDA. The agreement specifies the JEIDA V. 4.0 format, 68-pin card; the DOS file format; a means for the system to know what kind of card it is dealing with; and other hardware and system-software specifications.

It's expected that Poqet Computer's (Sunnyvale, Calif.) Poqet PC, a palmtop unit that accepts the IC cards, will spearhead penetration of the U.S. market.

Dan Sternglass, founder of Databook Inc. (Ithaca, N.Y.), which manufactures a series of IC-card reader/writers and programmers, said: "What's going to drive the market first are portable systems, starting with the Poqet. We still have to see how much of the market will be penetrated by the handheld-type computers. Then,



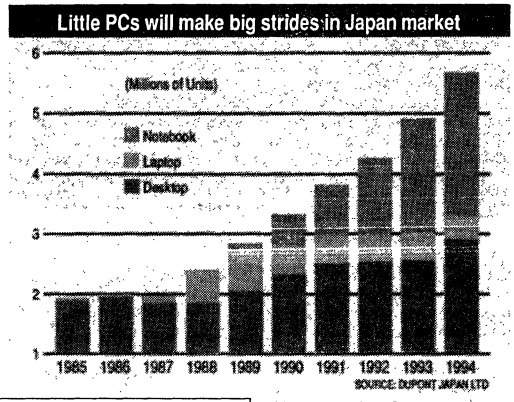
Fujitsu's version of the credit-card-size 'PC Card.'

PC Card standard drafted

if everyone owns a handheld, IC cards might be used in desktops."

A host of notebook machines coming to market in Japan is expected to fuel use of the new cards there.

Last week at the Japan Business Show, NEC Corp., Fujitsu Ltd. and Mitsubishi Electric Corp. all introduced powerful new notebook computers that include IC reader/writers compatible with the new 68-pin standard. Fujitsu offered a half dozen applications in ROM-based IC card format, along with various data file cards using SRAMs.



How standard came about

Tokyo — The people who hammered out the IC card standard between Japan and the United States described it as an exercise in quick compromises—and a demonstration that good will exists in abundance between Japan and America.

Basically, the standard took most of the hardware specifications developed over the past five years by the Japanese and added software standards prompted by the U.S.'s Personal Computer Memory Card International Association (PCMCIA).

Fujitsu Microelectronics memory card manager John Reimer said Poqet Computer executives realized a year ago that a standard for the cards would expand the software base for their palmtop machine. Reimer—described as "the driving force" behind the formation of the PCMCIA—sent out letters in June 1989 about the new association and got quick acceptance from U.S. companies. About 70 companies joined PCMCIA.

Reimer: Instigator.

Late last year, the Americans sent a letter to the Japan Electronic Industry Development Association (JEIDA), an association that focuses on personal computers. The JEIDA working committee, already five years in existence, sent 10 Japanese representatives to the PCMCIA's January meeting, in Dallas.

Japanese and American executives began crossing the ocean each month, attending each other's meetings. The Americans, accustomed to voting on issues after a period of discussion, worried that the Japanese would "want to keep talking, talking, talking, until they reached a consensus," Reimer said.

Instead, the Japanese accepted U.S. proposals about the pin lengths for the 68-pin connector; Japanese software companies—including Microsoft Japan, Just Systems and Ascii Corp.—provided important input to the software discussions.

—David Lammers

New notebook wave

Those A-4-sized systems are in the 6-lb. (2.7 kg) range, similar in size to the popular "Dynabook" from Toshiba. One model of NEC's PC98 Note is also the first built around Intel's 386SX processor, partly because it expects that users of notebook computers will want to run the same Windows interface they use on their desktops.

Though the Dynabook does not include an IC card slot, future Toshiba systems will. Both the chairman of the JEIDA working group and the software subcommittee are Toshiba executives.

Though several companies are developing notebook machines in the United States, the portable field here is currently focused on the larger, heavier laptop PCs, like those made by Zenith Data Systems (now part of the Bull Group), Compaq and Tandy.

But that could change. According to Japanese sources, IBM Corp. is expected late this year to introduce a notebook computer, now under development at IBM Japan, that would use IC cards manufactured at a new IBM plant in Toronto. By using the PC Card, IBM might try to leapfrog its competitors and make a comeback in portables, just as it's trying to do in workstations. The June meeting of the PCMCIA will be hosted by IBM in Toronto.

For now, hopes for the PC Card's success in the U.S. market rest mainly with the Poqet computer. Poqet is pioneering IC card use with versions of Lotus 1-2-3, an integrated package called AlphaWorks from Alpha Software (Burlington, Mass.), and other applications. The system it now uses is upward-compatible with the new standard.

John Reimer, the Fujitsu Microelectronics (San Jose, Calif.) memory card manager who serves as the PCMCIA's chairman, said he got interested in IC cards because of Fujitsu's investment in Poqet Computer. Fujitsu is doing back-up manufacturing for Poqet in Japan and is a card supplier to Poqet.

Reimer said he expects the success of Poqet's $2,000 system to drive demand for IC cards in the United States for the time being. But, he said, ultimately, "every executive will want to have some kind of notebook computer," and that will create the market for IC cards.

Not an expansion card

The PC Card should not be confused with the memory expansion cards that some vendors offer for adding DRAM to laptops. Partly to avoid confusion with these DRAM cards, PCMCIA uses the name "PC Card" and has developed a logo that will mark the cards that comply to the standard.

PC Cards, rather than being analogous to add-on memory, are actually a form of removable media, like the 3½-inch diskettes being used in today's laptops. Like floppies, they

Japan/U.S. PC Card standard at hand

not only store programs and data but will allow dissimilar notebook machines to share that data, thanks to the standard. Further, by using PC Cards, notebook computers could exchange data with pocket computers or even with new versions of the electronic organizers which have sold millions in Japan, but have been based to date on proprietary card schemes.

IC cards are seen as the key to eventually replacing floppy disk drives in notebook computers. Ryozo Yamashita, an ASCII Corp.

Dynabook engineer Terry Moore (left), key figure in standards development, with president Dan Sternglass and PC Card.

(Tokyo) engineering vice president, attended several PCMCIA meetings in the United States and said he grew tired of carrying the six-pound Dynabook along in his rucksack.

"With a floppy disk drive in the computer, there is not much more than can be done to reduce the weight. And a floppy drive consumes a lot of power."

But before the ubiquitous floppy is designed out of notebook computers, software companies must port more software to PC Cards. Yamashita said he believes the market will be driven first by the Poqet computer (though he believes the Poqet keyboard needs improvement) and later this year by less expensive portable computers.

"By the end of this year the IC memory card will be used as the primary media on pocket-type computers from many companies," Yamashita said, with the fall Comdex show in November a target date. With the PC Card, he noted, the system CPU can directly access the memory on the card itself. "That will eliminate the huge memory needed on the main unit," he said.

Once a large installed base of hardware is on the market, more software will be ported to PC Cards, he said. However, software companies are cautious because of the high cost of putting software into silicon. A 1-Mbyte ROM card that costs $50-70 now may come down to half that over the next year, as 8- and 16-Mbit mask ROM chips proliferate. But compared with distributing applications on floppies, ROM IC cards are a big financial risk, especially for the thousands of small software companies.

Japan's software houses, including ASCII, have a lot of experience selling Nintendo game software stored in ROM, Yamashita said. But Nintendo software can sell in millions of units, while the computer market is marked by higher prices but smaller unit volumes. The big merit of IC card software, he said, is that it cannot be copied by individuals, giving software companies the incentive to strive for potentially higher margins.

One other potential hurdle for getting software into PC Cards could be settled at this week's PCMCIA meeting. There, Microsoft and Lotus Development Corp., two of the biggest promoters of the standard, will try to work out their differences on how to implement "execute in place" (XIP). XIP permits a small system to run software stored on a PC Card and access memory on the same card, rather than relying solely on the system's memory. XIP is an important issue for the optimal execution of large programs adapted to IC cards, such as Lotus 1-2-3 running on the Poqet system. The issue brings to the IC card level a bigger issue: how to get around the 640-kbyte barrier of the original PC architecture while maintaining PC compatibility, said Yoshinobu Akimoto, an engineer at Microsoft Japan.

Mike Dreyfoos, chief engineer of Microsoft's MS-DOS division, who is active in the PCMCIA, and Jim Prelack, a Lotus Development executive who serves as president of PCMCIA, are both said to be taking a "market oriented" approach toward resolving the snag.

An informal meeting on the XIP issue, held here May 14, resulted in some progress, sources here said. Even without an immediate agreement on XIP, companies can take the basic standard and begin porting software and building IC card-based hardware.

"Both companies [Lotus and Microsoft] realize we've got to get the show on the road," said Fujitsu's Reimer.

U.S. to get the jump

T. Shigeta, a senior staff manager at Microsoft Japan, said the U.S. market may adopt the software cards faster than the Japan market. In Japan, Fujitsu, NEC and other companies all support proprietary versions of MS-DOS, making applications incompatible. That fracture is continuing down to the notebook and palmtop systems, which will support proprietary versions of MS-DOS.

"The big issue is not only the high cost of the [IC card-based] software, but having to support different cards for the different architectures here in Japan," Shigeta said.

He believes the data cards will sell well in Japan. "The importance of this standard is that notebook-, laptop- and desktop-type computers will be able to exchange data on the cards."

He predicted small ISVs will maintain a cautious stance toward IC card-based software. The lack of software support has hurt previous attempts to market IC card-only notebook computers, including NEC's "UltraLite," sold in the U.S. market, Epson's "Note Executive" and Sharp's "Brain."

Asked if Microsoft will port its applications to the cards, Shigeta said, "I can't say anything explicit, but from the level of our activity in JEIDA and PCMCIA, you can see that we see a bright future in IC memory cards."

Ryosuke Takahashi heads up the five-person IC card team at DuPont Japan Ltd. As a neutral player in between Japan's competing electronics companies, DuPont buys memories, has them assembled by third-party suppliers and markets the IC cards to Japan's computer makers. DuPont also supplies most of the two-piece (header and female) connectors used in the JEIDA format cards.

A 1988 market study done by DuPont and Nomura Research Institute predicted that the IC card market in Japan would grow by a 33 percent compound average growth rate, rising to about $1 billion in 1995. That's about five times larger than the total expected for 1990, and the Japan market estimate preceded the unexpected joint standard with the U.S.

In about two years, when flash EPROM-based cards are in wider use, the price of most of the cards will drop to half, Takahashi said. Now, a 512-kbyte SRAM card is sold to OEMs for about 40,000 yen, or about $240.

Takahashi believes that palmtop-size computers will be the biggest market for the next couple of years, with most notebook computers continuing to use floppy disk drives. Beyond that, some companies may migrate to IC card-based notebooks, sans floppy drive.

But other markets will be important. Already, robots and measurement equipment, laser printers, and medical equipment use IC cards. "My personal view is the digital still cameras will be a big market for IC cards in years to come, replacing film," Takahashi said. Toshiba and Fuji Film already have a camera on the market that uses IC cards, and Sony may change from a floppy to a card based still camera. The FBI put in a major order for Sony's camera last week.

ASCII's Yamashita said a potentially huge market for IC cards is in distribution of specialized information. A number of Japanese software, printing and publishing companies have initiated the International Card Media Publishing Association. Stock exchange data and financial news, train timetables and other forms of changeable data could be stored on IC cards. One idea is to provide vending machines that would download data on to a card at a train kiosk or newsstand.

"When flash memory gets cheap enough, then you might stop by and download certain kinds of news and view it on the train; information could be personalized," Yamashita said.

The way to look at IC cards is as the next step in the evolution of computer media, from paper tape to magnetic tape and floppy/hard/optical disks, and now to a silicon-based media, he said.

Mask ROMs normally are used to store software in IC cards. The market for Nintendo game cartridges has helped drive the price of a 1-Mbyte ROM card down to about $60 to $70. That may drop by half over the next year.

Before IC cards become popular the cost of data storage cards must come down, an area where flash EPROMs are expected to play a key role.

"All of the PCMCIA members expect that flash will replace a good chunk of the SRAM-based cards," said Reimer, noting that Intel Corp., Texas Instruments, Inc. and Toshiba Corp.—the larger companies in the flash memory field—are active members of PCMCIA. Fujitsu and other Japanese companies have major flash development efforts under way.

William Howe, president of Intel Japan, said IC-card related product announcements from Intel, based on flash EPROMs, "are not very far away." Though he said Japanese semiconductor companies have accelerated their own flash development efforts, they are turning to Intel for flash EPROMs to be built into IC cards.

Takemae said flash memories will make an impact on IC card pricing, probably beginning next year.

"In the last few months the interest from our customers in flash (for use in IC cards) has increased by an order of magnitude. It's not just Company A or Company B, it's everybody," Howe said.

Though flash is considerably more expensive than EPROM memory now, Howe said he expects the price to come down to 10 to 15 percent above the tags on EPROMs, and far less than the price of SRAMs now used in IC data cards.

Yoshihiro Takemae, a Fujitsu Ltd. semiconductor manager who served as chairman of the JEIDA hardware subcommittee, said flash memories will make an impact on IC card pricing, probably beginning next year. The PC Card pin layout scheme reserves pin No. 18 for programming the card, which would accommodate the 12 volts needed to electrically rewrite a flash memory.

While research continues into ways in which sectors of a flash EPROM can be selectively erased, Takemae said, "I think that deletions can better be handled by the software. People should think about the format and handling of the IC memory card just as they think about floppy disks now."

The hardware specifications included a write-protect switch, the position of the battery, a green-yellow-red light system to indicate the strength of the battery, and a variety of electrical specifications, all of which can be obtained from the PCMCIA once the standard is published.

The decision to move from 60-pin cards, which had been used by several Japanese companies, had been agreed upon earlier by the JEIDA group in its V 3.0 specifications.

The cards are about 3.3 mm thick, so that four-layer, double-sided cards can be housed. Fujitsu and other companies have been putting 20 to 24 chips on the double-sided cards, using TSOP (thin small-outline packages), an emerging form of surface-mount packaging, Reimer said.

Takemae said the most difficult issue facing the hardware group was how to deal with "hot insertion/hot removal," i.e., pulling out a card while the system is still operating, which can result in data loss. A major future issue is how to develop an I/O specification so that interface cards can be built into portable computers, "talking to" fax machines, telephones and pagers, printers, and other external devices.

Yamashita, of ASCII, and Terry Moore at Databook worked together to develop the META card interface format, with input from Dreyfoos of Microsoft.

META is a header format that tells the system what kind of card (such as an application or data card) is in the slot, what kind of semiconductor memory—and how much of it—is on the card, and so on.

"We really have worked hard so the consumer can just plug in the card and make it look like a floppy disk. We want this to be a consumer product," Sternglass said.

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Flash Memory Outshines ROM and EPROM

SAUL ZALES

INTEL CORPORATION

Order Number 295050-001

Flash Memory Outshines ROM and EPROM

SAUL ZALES, INTEL CORP., FOLSOM, CALIF.

Flash memories may improve product costs and reliability in many markets

As competitive pressures continue to mount, project and design leaders find themselves taking on more responsibility for overall system costs. In many cases, systems designers are expected to design with an eye toward controlling costs in all phases of the product life cycle, from conception through design and manufacturing—even up to post-sales service.

Beyond paying strict attention to total life-cycle costs, today's systems designers face other significant challenges. These include choosing the most efficient CPU architecture, designing for cross-vendor system connectivity, maintaining component and system quality, and building systems that can be serviced easily. Software issues facing project and design leaders include planning for past and future compatibility, minimizing code size, and balancing system performance and stability with time-to-market concerns.

Memory designs have coalesced around basic choices: disk and DRAM architectures, and EPROM-based designs. Although these technologies have been improved over the years, they still require designers to make some trade-offs for certain applications. One such application that has taken on a growing importance for many manufacturers is embedded control.

In the past decade, designers of electromechanical systems have come to rely heavily on the use of embedded microcontrollers. These parts have vastly improved control functionality and performance. Consider, for instance, the growing number of consumer-electronics items that are microprocessor controlled: microwave ovens, washing machines, VCRs, audio systems, and exercise equipment, to name but a few. These products ship with operating code stored in ROM or EPROM; the manufacturer assumes that the code stored in these memories will never change.

Consumer products are not the only items equipped with embedded microcontrollers, of course. Industrial machines, office-automation equipment, medical equip-

ment, communications equipment, avionics systems, and data loggers all include code stored in ROM or EPROM. In nonconsumer products, code changes are more likely to occur, requiring frequent memory fixes. Reasons for such changes include evolving customer needs, frequent demands for new features, improved algorithms, changing connectivity protocols, and eliminating software bugs.

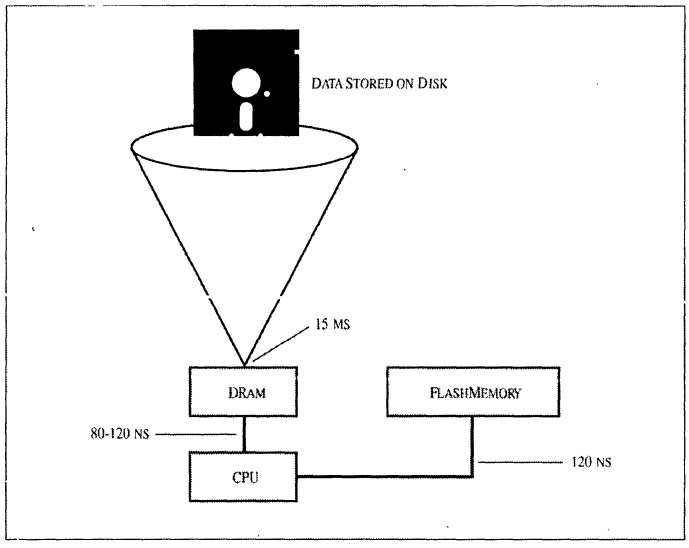
Code updates are impossible with some memory technologies; with others, they incur high costs and threaten product reliability (see box, "Memory Alternatives: Major Trade-Offs"). Designers of products that are likely to require code updating in the course of their life cycles should look beyond conventional memory options and investigate a technology that is well suited to such applications: reprogrammable flash memory.

Reprogrammable flash memories have the potential to improve product costs and reliability in many market segments. For example, ROM and EPROM parts are currently used in electronic engine controllers for automobiles. These parts cannot be replaced; they are sealed under a moisture-resistant coating. To change the code enclosed in one EPROM, the service center must replace the entire controller module, which costs about $200.

Starting in 1993, Delco and a few automakers will begin using flash memory in these modules. With flash memory in place, if a code change is required—for instance, if the Environmental Protection Agency mandates a code change to reduce exhaust emissions—the service center can simply reprogram the memory using a serial link from the service bay's diagnostic computer. No parts need to be replaced, eliminating the risk of damage to other components in the module.

Although flash-memory parts are more expensive than EPROM components, the additional up-front costs eliminate expenses that occur later in the product's life cycle—that is, when code has to be updated. Although customers generally assume the burden of paying for code upgrades, there are certain hidden costs to manufacturers that, taken together, can be significant. For example, consider the cost difference between transferring an upgrade electronically—as can be done with flash memory—and sending a highly paid technician to make a service call.

For whatever reason, most manufacturers do not include upgrade costs in their overall system cost estimates. If a year or two after a product is sold a code update is required, that expense usually is unaccounted for in the system's overall cost. But just because the expense is unaccounted for doesn't mean money isn't spent. Costly updates to existing products will show up on the organization's bottom line somehow. For this reason, even if only one code change is anticipated in the lifetime of a product, designers should opt for flash memory.



In a typical computer, the CPU's performance is slowed by the data bottleneck created by relatively sluggish disk access times. Embedding code in flash memory can eliminate this bottleneck for key operations.

■ PC APPLICATIONS

Flash memory fits extremely well in the embedded-control world, but its usefulness is not limited to such applications. It is becoming more apparent that flash memory will play a critical role in the reprogrammable environment as well. For example, today's personal computers are based on DRAM and disk drives. Obviously, these systems provide acceptable performance to users. Their performance can be improved more, however, by employing firmware based on flash memory.

ONE AREA IN WHICH FLASH MEMORY COULD BOOST PC PERFORMANCE IS IN THE COMPUTER'S BIOS

One area in which flash-memory firmware could greatly boost PC performance is in the computer's basic input/output system (BIOS). A PC's BIOS contains the system initialization, a power-on self-test, and basic component-level drivers. Currently, a computer's BIOS typically is stored in ROM or EPROM, which means that, in essence, it is an embedded-control memory. Without the nonvolatility these memories offer, the system could not initialize itself sufficiently to load software from the disk. This is because the CPU cannot read directly from disk—the disk's access time is much too slow.

Although the average PC user does not think about changing a machine's BIOS, a number of major PC vendors are planning to use flash memory for storing BIOS for several reasons. One is the rapidly changing nature of microcomputer technology. Consider the increase in system complexity from the PCs of 10 years ago to today's top-of-the-line machines. Today's 32-bit PCs offer the computing power of minicomputers. Computer makers need technology that allows for rapid adaptation to ever-changing situations.

The open nature of microcomputer systems adds to the need for flexible BIOS. Multiple vendors develop products that rely on the system's BIOS. In other words, the BIOS drivers hold the key to compatibility with both older hardware and software and newer products. The average stand-alone user who buys a computer, adds in a couple of boards, and runs a half dozen or so popular software packages usually doesn't need to worry about BIOS compatibility. But what about MIS or DP managers at Fortune 500 organizations? They may be responsible for hundreds or

even thousands of PCs fitted with any number of different add-in boards and running hundreds of different software packages. Incompatibilities are likely to abound in this type of environment.

With BIOS stored in EPROM or ROM devices, revisions to BIOS code are impractical. The end result is that many users must make do with systems that do not act predictably with certain software or hardware. If BIOS is stored in flash memory, however, vendors can provide a disk with new code and a simple upgrade utility.

Designing a flash-memory-based BIOS poses similar considerations as designing for the embedded-control environment (see box, "Designing with Flash Memory"). The system must contain a 12-V power supply regulated to ±5 percent. In addition, designers must deal with issues regarding the boot code. If power goes down midway through the BIOS upgrade, from where will the system boot? A boot PROM with the basic hardware initialization code could be included for safety's sake. It could be shadowed out once the flash memory has been properly initialized. Still, including a boot PROM incurs added costs and uses board space.

Designers at Ing. C. Olivetti have built a flash-memory BIOS without the PROM safety net. The Italian company's new 80486-based microcomputer includes a flash-memory BIOS without a boot PROM. Designers decided that the risks involved in eliminating the PROM were minimal. A typical flash-memory upgrade takes 7 to 10 seconds. The chances of power going down during those 7 to 10 seconds are not great enough to merit inclusion of the PROM, Olivetti decided.

■ BEYOND BIOS

BIOS is only one PC component that can benefit from the flexible-firmware concept. The setup and diagnostics programs

WITH FLASH MEMORY, IF OPERATING SYSTEMS ARE UPGRADED, USERS CAN SIMPLY REPROGRAM EMBEDDED PARTS

that ship with every system can be stored in flash memory. Another design improvement is to put the operating system into flash memory. Consider the PC's boot sequence. When the system is powered up, the CPU executes the BIOS hardware initialization, performs a power-on self-test, and spins the disk up to speed. Only after the disk stabilizes at its operating velocity can the CPU begin to read the operating system.

Most operating-system code is read-only, which means that, theoretically, it could be included in the BIOS ROM to allow for faster system power up. The reason that this has not been done on a wide scale is simple: Systems designers recognize that operating systems evolve and improve over time, and that a flexible environment is required. With flash memory, however, concerns about upgrades are eliminated. If operating systems are upgraded, users can simply reprogram flash memories, as with flash-memory BIOS. Two major operating-systems houses, Microsoft Corp. and Digital Research Inc., now offer their operating systems in a form suitable for storage on ROM or flash memory.

In addition to storing the operating system in desktop or laptop systems, flash memory can increase network performance for intelligent terminals and diskless engineering workstations. Large networks, such as those used in airline-reservation systems or retail point-of-sale systems, often bog down during peak transaction periods. The load on the network can be reduced by storing the operating system, LAN protocols, or even scheduling or pricing tables in flash memory. Updates can occur during off hours through the network itself. Curtis Inc. (St. Paul, Minn.), which has offered EPROM or SRAM solutions to this problem for a number of years, now also offers flash-memory products to improve network performance.

■ OFFICE APPLICATIONS

Firmware based on flash memory can lead to significant efficiency improvements in several office applications. For instance, most offices now deploy laser printers for high-quality output. Laser printers allow users to produce typeset-quality memos, presentations, and the like. In many cases, the type fonts used with laser printers are stored in software on a PC's hard-disk drive. Users download these fonts as they are needed to the printer's RAM. Every time a font is changed, the downloading process must take place. Alternatively, many laser printers are equipped to take fonts from ROM- or EPROM-based cartridges that plug directly into the printer. The problem with ROM cartridges is that fonts stored in them cannot be changed. Any given cartridge may contain only a couple of desired fonts, which severely limits the flexibility of laser technology.

Flash memory could greatly enhance the speed and flexibility of laser printers. Using a flash-memory-based cartridge, users or work groups could develop their own font libraries. Since flash memory is nonvolatile, these fonts will stay resident in the printer without the use of batteries or uninterruptible power supplies.

Flash technology is well suited to application storage as well. Software stored on disk greatly reduces system performance, since disk access times are very slow compared with memory and CPU speeds (see figure). Of course, this speed bottleneck is not critical to most PC users; if a program takes a few seconds to load, so be it. For high-end systems, however, flash memory can boost system speed significantly by functioning as a code accelerator by storing programs or code that are accessed most often.

One high-end application that could benefit greatly from flash memory is CAD. Some CAD programs minimize the RAM used for program storage in order to maximize the data-memory space. To do this, the complex software swaps submodules into memory from disk as needed. Accessing the disk for a new module or library ties up the system and degrades performance.

Many CAD users install large add-in memory boards set up as RAM disks to avoid the transfer bottleneck. Whenever the system resets or powers down, however, this RAM disk loses its memory. A system containing a flash-memory disk emulator would not have this problem. Such a system for CAD and engineering applications is available from Digipro (Huntsville, Ala.).

■ PORTABLE PCs

Laptop and notebook-sized portable computers stand to benefit greatly from flash-memory technology. Although small, relatively efficient 2.5-inch disk

FOR HIGH-END SYSTEMS, FLASH MEMORY CAN BOOST SPEED BY FUNCTIONING AS A CODE ACCELERATOR

drives have come onto the market for laptop computers, their efficiency rating is derived primarily from power-management schemes. If no access has been made to the disk for a certain period of time, the

drive goes into a low-power standby mode. Unfortunately, the delay caused by switching from standby back to operational mode further impedes the already-slow disk-to-memory transfer.

From a power perspective, these small drives use relatively less power than desktop disk drives. Active power specifications in the 1-W range are attainable, as opposed to the multiple watts consumed by desktop-system drives. Compared with flash memories, which use about 50 mW during active reads, the 2.5-inch drives are power hungry. In addition, in standby mode flash memories use only 150 μW of power.

Notebook-sized computers do not have space for even the smallest of drives. Additionally, users of notebook-sized systems demand much longer battery operation than is typical of laptops. Typical battery operation for notebooks range from 50 to 100 hours, compared with two to five hours for laptops.

The typical notebook computer contains ROM cards for applications and SRAM for storage of data files. This architecture has a few flaws. Users who purchase software for a desktop system may not want to spend another few hundred dollars for ROM-card versions. If flash-memory storage is provided, users can download software at a much lower cost.

Some notebook-sized computers let users load applications into SRAM or low-refresh DRAM (pseudo-SRAM). This procedure, however, is highly dependent on the system's battery; when the battery dies, memory is erased. With flash memory, no power is consumed when the system is off. Additionally, flash memory is less expensive for bulk storage than is SRAM.

Psion, a company based in the United Kingdom, recently introduced a notebook computer based on flash memory. Psion compared the price differences between SRAM and flash memory and found flash memory to be much more cost-effective. Based on the power savings of flash memory and very tight system design criteria, Psion built a 60-hour operational system.

■ FILE STORAGE UNDER DOS

Given the compelling reasons to adopt flash memory in the various PC environments, designers can then ponder the question: How can a bulk-erasable memory be used for file storage under DOS? The DOS directory and file-allocation tables (FATs) require the ability to erase and rewrite single bytes and files. The answer to this has many facets and depends on the degree of flexibility needed.

The most inflexible, but easiest to implement, approach involves creating a fixed disk image. Before programming the flash memory, the vendor combines the operating system, utilities, and specific applications onto a disk. It then runs this suite of programs through a utility that adapts the software for ROM or flash-memory storage. Finally, another utility creates the DOS directory and FATs and assembles the disk image. Digital Research offers both a ROM-format DOS version and disk-image utilities. Microsoft offers an optimized ROM-format DOS for the portable market as well.

SOFTWARE EMBEDDED IN FLASH MEMORY CAN BE CHANGED WITHOUT COMPROMISING SYSTEM PERFORMANCE

Makers of notebook-sized computers, intelligent terminals, and dedicated handheld computers might consider this strategy. A laptop vendor that offers a low-power disk might consider this approach as well. The most-used software, such as the operating system, calendar, alarm, and communications software, will load more quickly and not burn as much power on each access. Upgrade-software disks could be sold to registered system owners already formatted with a new disk image.

Another approach currently used by Digipro involves adapting RAM-disk emulator drivers to flash memory. This entails trapping disk writes and programming the information algorithmically.

From the user perspective, the flash-memory disk operates as a hard disk, but with 100 times the typical read performance of a hard disk. To load the flash-memory disk emulator, a user simply issues the DOS Copy command.

A drawback to this approach is that loading any application or its libraries forces a rewrite of the entire directory and FATs. For example, a file that contains only 2 Kbytes and should program in 50 ms may take several seconds to store because of file-system overhead. Note that this drawback may not be important as far as code acceleration is concerned. Files are loaded to the flash-memory disk as an off-line task, so the write-performance impact is minimal to read-mostly performance.

A third solution to the DOS compatibility problem comes from Microsoft, which has developed a flash-memory file system that loads under MS-DOS and other compatible operating systems. When a user adds a directory or a file to the flash-memory disk, the file system adds the information in a linked list. Should the user delete the directory or file, the file system marks an attribute field as being inactive. When the disk fills up, the user copies the active files and directories to a hard disk on the desktop system or to another disk on a portable system. Since the DOS Copy command only grabs active files, the newly transferred version contains a clean, unfragmented linked list. The user then erases the original flash-memory disk.

As these examples illustrate, flash memory offers alternatives to current problems in system architecture. To offer true solutions, a memory technology must also satisfy three objectives: It must provide acceptable density, incur a reasonable cost, and offer EPROM-level reliability.

Intel's ETOX flash-memory technology is the first new technology in nearly 20 years to satisfy all three objectives. It is dense—the 1-Mbit 28F010 has been shipping in production units since April 1989. Costs have decreased dramatically as volume has ramped. And because the ETOX process and memory cell so closely parallel mainstream EPROM technology, flash memory has reliably doubled in density three times in the last two years. Additionally, a flash-memory device can be reprogrammed about 100,000 times—a sufficient number for most firmware and disk applications.

Current Intel flash-memory product offerings include the 28F256, 28F512, and 28F010. These devices are 32-Kbit × 8, 64-Kbit × 8, and 128-Kbit × 8, respectively. All products ship in either surface-mounted ceramic DIP or PLCC. Higher densities, plastic DIPs, and smaller packages will be available shortly. Additionally, for those designs requiring a bulk-memory solution similar to that offered by DRAM vendors, Intel offers eight 28F010 PLCC units mounted on a single in-line memory module (SIMM).

With flash-memory technology, software can be changed without compromising the performance of disk access. The task can be accomplished in a reliable manner and without the high costs associated with service calls by field technicians. Finally, flash memory is nonvolatile—data stay resident even when the power supply is cut off. Together, these attributes enable flash-memory technology to provide users with flexible firmware and improved system design. ■

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6

Designing with Flash Memory

For many embedded-control applications, whether the control is of the sequential, closed-loop, or data-control variety, flash memory offers dense, reliable, rewritable, nonvolatile storage. From a systems perspective, the memory reads the same way as an EPROM, EEPROM, or SRAM, with access speeds of up to 120 ns. Intel fabricates flash-memory devices using its EPROM Tunnel Oxide (ETOX) process. ETOX is based on Intel's high-volume CMOS EPROM process. Because of this, flash memory reprograms in the same way as an EPROM—via CPU-controlled algorithms.

With flash memory, the designer implements the reprogramming algorithms, which are simple closed-loop algorithms that require 500 to 1,000 bytes of code. (Intel offers sample code generated for different base processors to minimize the software effort.) Because flash memory is bulk-erasable, this code must be stored and executed from another memory while the main code is updated. For this process, many designs rely on internal ROM space on microcontrollers or small EPROM boot loaders on Intel 80X86 systems. The boot loader contains sufficient code to initialize the system and reprogram the flash memory.

As with EPROM, flash memory requires a programming power supply of 12 V ±5 percent. Some systems feature a 12-V supply, but others do not. Systems with analog circuitry, for instance, often contain rails of 15 V or higher. In these systems, the programming power supply can be generated by regulating the higher voltage using an LM317-type regulator.

For memories that have a power supply of 5 V, designers can opt for either monolithic or discrete charge pumps, such as those as offered by Valor Electronics and Linear Technologies. Since flash memory requires only 30 mA per device from the programming power supply during active programming and erasure, these boost circuits can be made fairly small.

Some flash-memory manufacturers claim to have simplified programming and erasure by developing automatic controls and 5-V-only programming. The 5-V technologies are based on EEPROM-programming rather than EPROM-programming techniques and generate high voltages internally. They require larger board spaces and are less dense, more costly, and less reliable than 12-V designs. And although they are called flash memories, these parts tend to be nothing more than EEPROM technologies.

COMPUTER TECHNOLOGY REVIEW ■ MASS STORAGE

Flash Memory Operates 10-20 Times Longer

by **Markus Levy**

Major technology changes in the 1990's will place new demands on memory devices. Mainframe computing performance is now available in a laptop PC, and hand-held solid-state calculators have become sophisticated organizers. The convergence of these two trends has led to the evolution of the notebook PC and the emergence of Flash memory.

With a minimum battery life of 20 hours and weight not exceeding five lbs, the completely solid-state notebook PC will reliably handle all performance requirements of the traveler. Flash memory helps make the design goals of the notebook computer a reality by replacing the majority of the memory technologies in the system. Psion, a leader in the notebook computer market, has created a product in which Flash memory is used for BIOS, OS, and secondary storage. This completely solid-state, DOS-compatible machine weighs only 4.5 lbs and operates on eight AA batteries for 25 hours.

To incorporate rapidly improving power management techniques for battery-powered systems, the BIOS must be software updatable—remotely over a modem or with a floppy disk sent by the OEM. As such, the EPROM no longer fulfills its classic role for code storage. However, designed with a similar memory cell structure based on ETOX technology (EPROM Tunnel Oxide), Intel Flash memory provides equivalent reliability and nonvolatility with the added advantage of one sec, chip-level, electrical erasability (hence the name 'flash'). Flash memory can occupy the EPROM's socket with minor hardware modifications, primarily, 12V (Vpp) and write enable (W/E) must be supplied to enable the software controlled erase and program operations.

Traditionally, when the computer boots up, the operating system (namely DOS) is read from the disk and downloaded to DRAM. Digital Research and Microsoft offer ROM-executable versions of DOS. Originally designed for the unchangeable ROM, this product now accommodates Flash memory which can easily be reloaded with newer revisions without removal from the system. Flash-executable DOS benefits the notebook computer because it reduces the system RAM required for DOS from 70K to 15K, reflecting both power and component savings. Additionally, the system bootup is almost instantaneous, commonly referred to as 'instant-on.'

Solid State Secondary Storage

Solid-state secondary storage has had the greatest overall impact on the notebook computer (See Fig). In this environment, the power consumption, reliability, size, and weight of the mechanical disk drive is unacceptable. For example, the active and standby modes of the small form factor (2 1/2-in.), 20 Mbyte disk drive typically consume 4W and 0.5W, respectively. As a comparison, the active and standby modes of the equivalent capacity of Flash memory, consisting of low power CMOS circuitry, typically consume only 0.15W and 0.04W, respectively. Obviously, for a truly accurate analysis, other components of the system should be included, but from the data storage point of view alone, the Flash memory disk will operate 10-20 times longer than the mechanical disk on a set of batteries.

Reliability issues will always exist with mechanical media in any type of portable equipment because of shock and vibration, but it is difficult to perform a theoretical analysis on this subject. Suffice it to say, that from an MTBF standpoint (as measured by disk drive manufacturers under normal operating conditions), a mechanical disk will typically run 50,000 hours. A Flash memory device (capable of 100,000 erase/program cycles) should continue to function past 1.6 million hours—a difference of two

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Order Number: 295054-001

Flash Memory Should Offer 1.6 Million Hr MTBF

orders of magnitude.

Size and weight are also critical factors in the notebook computer. Two Mbits of Flash memory is now available in a thin small outline package (TSOP) with a height of 1.2 mm. Minimally, 16 of these tiny packages can be put into a pocket-sized IC memory card (15,789 cm^3 vs 215,384 cm^3 for the 2 1/2-in. mechanical disk drive) to make up a four Mbyte disk, an adequate supply of memory for the notebook computer. Flash memory is not the only technology used as a solid-state alternative to secondary storage. ROM and battery-backed SRAM drives are actually more common because of familiarity. However, each has inherent drawbacks. ROMs have historically been used in laptop systems to store unchangeable, preloaded software programs. To upgrade with software revisions, the ROM application hardfile is discarded and a new card is purchased—an undesirable expense for the user.

Battery-backed SRAMs enable the flexibility to continuously modify files. SRAMs are used both as floppy and hard drive replacements, only where very low densities are required. Besides not being practical for high-density applications, SRAMs also draw concern from unpredictable battery life.

Unlike the ROM drive, flash memories can be reprogrammed many times. Unlike SRAMs, the single transistor memory cell of flash (compared to 4-6 transistors for SRAM) is very scalable for photolithographic processes, promoting very high density devices. In an environment where high density is synonymous with secondary storage, flash will outsell and outlast volatile SRAMs because of cost and reliability advantages.

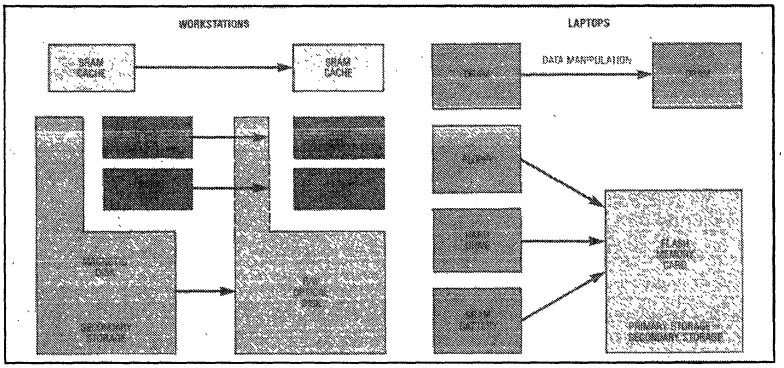

Fig Whereas in workstations Flash memory is used as cache for the OS and code, the laptop uses Flash memory for direct execution.

Using Flash memory

The adoption of Flash memory in a solid-state disk comes with the design challenge of interfacing a bulk-erasable memory with a file system requiring byte-level alterability. The simplest solution is to use a ROM-like approach and use the drive as an application hardfile with the extra benefit of being able to erase and reuse the disk. Microsoft has made major advances over this approach by developing a special file system it calls Flash File System. Based on linked-list techniques, this DOS-compatible file system, with superior performance over the mechanical disk, takes advantage of the chip-level erasability of Flash memory.

Although we have only discussed Flash memory applications in the notebook computer, its usage spreads well beyond. BIOS modification in desktop computers is also unavoidable due to increasing system complexity. Primarily aimed at fixing bugs, this technique also alleviates compatibility problems that might arise from the installation of the myriad of add-in boards and software packages. In addition, the OEM can promote upgrade service as a market distinction, as done by NCR and Olivetti.

Flash memory disks are useful as application caches in high-end systems because of their nonvolatility and RAM-disk equivalent access speeds. Many types of industrial equipment are using Flash memory for code storage and data accumulation, replacing all forms of disk drives, both mechanical and solid-state.

Flash memory will continue to play a dominant role in the evolution of the notebook computer as well as every other application requiring a nonvolatile, reprogrammable, reliable, high density, and low cost memory. The flexibility of this new memory technology is driving costs down and generating an important alternative to disk memory. ■

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UPDATE

October 1990

Memory breakthrough drives miniaturization

You can use it like RAM and carry it around like a disk. Flash EPROM technology is poised to change the way portables are made.

Last year—a year in which assumptions about the world seemed to fall with bewildering regularity—a truism about computers suddenly became irrelevant. Intel Corp. in Santa Clara, Calif., unveiled a new type of memory chip, the flash EPROM, which combines the flexibility of RAM with the permanence of disks. The distinction between RAM and disk started crumbling like the Berlin Wall.

Now the implications of flash EPROMs for portable computing—particularly notebooks and handhelds—are becoming clearer. If supporters of the technology are correct, flash EPROMs could eventually replace bulky, power-sapping disk drives in computers and serve as a universal storage medium for nearly every electronic device that uses memory.

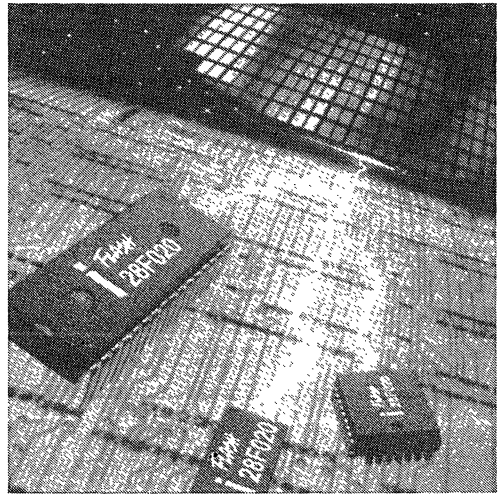
Based on older EPROM (erasable programmable read-only memory) technology, flash EPROMs do not need a backup power supply to retain data. Like regular EPROMs and dynamic RAMs (DRAMs), they can be packaged in plastic cases and plugged into computer motherboards. And like static RAMs (SRAMs), they can be integrated on credit-card-size memory cards, providing a removable storage medium for software. Intel guarantees 10 years of data life.

Flash EPROMs are likely to rearrange the mix of chip- and disk-based storage in all computers, especially the smallest portables. When used on removable cards, they can replace floppy drives, eventually for one-quarter the cost of currently available SRAM cards, according to Intel. At this writing, however, computer makers were waiting for lower prices before making the jump from SRAMs to the new chips.

Flash EPROMs could also be used to store programs (such as Tandy's Deskmate interface or MS-DOS) which now take several seconds to load from hard disk to RAM while sucking up precious electricity. Programs stored in flash EPROMs load nearly instantaneously. One company, Cardinal Technologies Inc. (Lancaster, Pa.) plans to offer an expansion board containing Digital Research's DR DOS in regular ROM paired with 2MB of flash EPROM for storing applications.

Engineers also envision flash EPROMs bringing major changes to the embedded computers and controllers that are becoming mainstays of modern life. Computerized engines could be reprogrammed to reflect evolving fuel mixtures as a car ages (currently, such programmable memory is dependent on battery power). Digital electronic cameras will use flash EPROMs instead of digital tape or film to store photographs with sharpness comparable to that of 35-millimeter cameras.

Although London-based Psion PLC is first out of the gate with two flash-based notebook computers, the MC200 and MC400 (available this summer) you can expect to see other innovative



Intel's flash EPROM chips can store data without a constant supply of electricity.

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machines using the new technology by early next year, according to Intel.

Hardware and software vendors are already using flash EPROMs to store vital code normally residing on ROM chips that can't be conveniently reprogrammed. When encoded in flash EPROMs, the computer's ROM BIOS, which manages hardware's interaction with software, can be updated via modem or floppy disk. (Phoenix Technologies Ltd., the largest BIOS maker, began offering flash EPROM versions of its products last spring.) BIOS upgradability will let you take advantage of new power-management breakthroughs and laptop peripherals without buying a new machine.

Flash EPROMs have one disadvantage that slightly limits their use: writing data to them takes nearly as much time as writing to a floppy. For this reason, they aren't as efficient as regular RAM at running applications like word processors and databases, which involve opening and closing files regularly. Flash EPROM proponents admit that computers based on the technology will sometimes use traditional DRAM storage for data manipulation, with flash EPROM cards taking the place of floppy and hard disks.

All the major laptop vendors are considering flash EPROMs, according to Kurt Robinson, Intel's product line architect for flash EPROMs. "Just about everybody is updating the BIOS portion of their machines from ROM to flash," Robinson says. In addition, Microsoft has thrown its support behind the technology by releasing file-management software that lets MS-DOS treat flash EPROMs like disk drives.

Intel expects steady increases in flash EPROM storage density at least through 1996. One-megabit chips are selling now, two-megabit versions should be available later this year, and four-megabit chips should follow in 1991. When 16-megabit chips arrive by 1994, vendors could introduce 32MB and 48MB "hard drives" on a card roughly two by three inches.

Texas Instruments (TI) is offering a similar technology that uses less power than Intel's flash EPROMs during data writing. In the typical flash-EPROM computer, all logic and memory operations require five volts of electricity, except for writing to the flash EPROM, which takes 12 volts. TI's new chips eliminate the need for a 12-volt power supply anywhere in the machine, saving space and weight. 256-kilobit chips are already available, with one-megabit versions expected by the end of this year.

Production efficiencies and price competition are likely to drive flash EPROM prices down to the level of dynamic RAM chips by 1994, Robinson asserts. By then, the whir of disk drives could be little more than a fast-fading memory.

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Hamilton/Avnet Computer
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190 Colonade Road
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